Energy-Efficient Wake-up Receivers for 915-MHz ISM Band Applications

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Abstract

"Energy-Efficient Wake-up Receivers for 915-MHz ISM Band Applications"

Wake-up receiver (WuRx) is a well-known approach for optimizing the latency and power consumption of ultra-low power transceivers in wireless sensor nodes.

Tuned RF (TRF) or Envelope Detection architecture is an appropriate topology for short-range Wireless Body Area Network (WBAN) applications, where achieving a very high sensitivity is not a priority. However, the demand for an improved sensitivity gets emphasized for longer transmission ranges. Regardless of the application, considering the existing trade-off between the power and sensitivity, design techniques and novel architectures are usually employed to optimize the power-sensitivity product. Moreover, considering the negative impact of higher data rate on the sensitivity, the energy-sensitivity product can be a more reasonable figure of merit when comparing WuRx designs.

In this thesis, the RF-subsampling architecture has been combined with the TRF receiver architecture as a first approach for improving the power-sensitivity product. The overall power consumption is reduced as a result of employing the subsampling topology with a low-frequency local oscillator (LO). Post layout simulations show that the proposed WuRx draws only 56 μA from a 0.5 V supply and exhibits an input sensitivity of -70 dBm for a data rate of 100 kbps. The chip occupies an area of 0.15 mm^2 and is fabricated with TSMC 90nm CMOS technology.

Another major contribution of this work is to propose and implement a novel dual-mode ultra-low-power WuRx based on the subsampling topology, which not only reduces the overall power consumption but also optimizes the energy-sensitivity product of the receiver. During the typical mode of operation known as the Monitoring (MO) mode, the start frame bits are received at a rate of as low as

10 kbps. Having received the true preamble bits in the MO mode, the remaining wake-up pattern bits are received at a higher rate of 200 kbps during the Identifier (ID) mode. By lowering the gain of the front-end amplifier in the MO mode, the power dissipation is reduced, which in turn causes an increase in the overall noise figure of the receiver. However, adequate sensitivity and hence an optimized energy-sensitivity product is maintained by intentionally lowering the data rate as well as the detection bandwidth of the receiver in the MO mode.

The proposed wake-up receiver has been designed and fabricated in IBM 130 nm technology with a core size of about 0.2 mm^2 for the target frequency range of 902-928 MHz. The measured results show that the proposed dual-mode receiver achieves a sensitivity of -78.5 dBm and -75 dBm while dissipating an average power of 16.4 µW and 22.9 µW during MO and ID modes, respectively.

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List of Abbreviations

BB	Base Band
BER	Bit Error Rate
BFSK	Binary Frequency-Shift Keying
BPSK	Binary Phase-Shift Keying
DAC	Digital to Analog Converter
ESD	Electrostatic Discharge
FOM	Figure of Merit
FSK	Frequency Shift Keying
FSPL	Free Space Path Loss
GBW	Gain-Bandwidth
ID	Identifier
IF	Intermediate Frequency
ISM	Industrial, Scientific, Medical
LAN	Local Area Network
LO	Local Oscillator
MIM	Metal-Insulator-Metal
MO	Monitoring
MOSFET	Metal Oxide Silicon Field Effect Transistor
NF	Noise Figure
OOK	On-Off Keying
PLL	Phase-Locked Loop
PSK	Phase Shift Keying
PVT	Process, Voltage, and Temperature
RF	Radio Frequency
RFID	Radio Frequency Identification
S/H	Sample and Hold
SFB	Start Frame Bits
SNR	Signal to Noise Ratio
SNR_{min}	Minimum Signal to Noise Ratio
T/H	Track and Hold
TCC	Temperature Compensation Circuit
TRF	Tuned Radio Frequency
TVC	Time to Voltage Conversion
ULP	Ultra-Low Power
VCO	Voltage Controlled Oscillator
WBAN	Wireless Body Area Network
WSN	Wireless Sensor Network
WuRx	Wake-up Receiver

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Concordia University, Montreal

"To my amazing wife Zahra,

and to my loving parents,

without whom this would not have been possible"

Chapter 1

Introduction

1.1 Motivation

Ultra-Low Power (ULP) transceivers have been vastly employed in Wireless Sensor Networks (WSN) and Wireless Body Area Networks (WBANs) and can have biomedical applications particularly in the dedicated Industrial, Scientific, and Medical (ISM) band [1]–[12]. In a WSN, the transceiver dissipates the largest portion of the total power. Therefore, it has to be designed to consume as low power as possible from the supply. However, most of the time a node in a WSN neither receives nor transmits any data. In other words, the transceiver could be shut-off thereby dissipating no power during the *sleep* mode. Moreover, it is desired to maximize the transmitted data rate in the *active* mode (i.e. for a short duty cycle) and to optimize the energy efficiency of the transceiver.

The receiver should become aware of a transmission request from the transmitter in order to change its mode from *sleep* to *active* and to initiate data reception. There are *Synchronous* and *Asynchronous* protocols for this purpose [13]. The former assumes that all the nodes in a WSN are synchronized by a global clock and so they could operate simultaneously. However, the total power consumption will increase as a result of synchronization. In the other protocol, the receiver periodically scans the channel for a transmission request. Since the receiver and transmitter are no longer synchronized, the transmitter should repeatedly send request until both receiver and transmitter requests happen simultaneously. Thus, the *Asynchronous* method has a tendency to add latency to the system. A different approach that was initially presented in [14] is to make use of a dedicated receiver known as the Wake-

Up Receiver (WuRx) whose job is to wake up the main data receiver upon detecting a transmission data (or request). A wakeup event in its simplest case could be detection of RF energy. However, in practice, a wakeup signal is in terms of a particular bit sequence, which is unique for every wireless sensor node for activating the main data receiver. The duty cycle of the main receiver will then be determined by the wakeup signal.

Total power consumption specifications in a WuRx depend on the main data receiver as well as on the network traffic. Since the WuRx is always listening to the channel for a transmission request, its power consumption should be a small ratio of that of the main receiver. Considering the fact that employing an ultra-low power WuRx could enhance the performance of a complete WSN by reducing both power and latency of the system, the future of WSNs can be dependent on WuRxs.

1.2 Communication Requirements

WuRx receivers are expected to operate in a very dense network environment with only a few nodes ready to communicate while rest of nodes are in a deep sleep mode only monitoring the channel for a wakeup request. As a result, wake-up receivers should be robust to the channel traffic. In other words, the best WuRx is the one that successfully wakes up the corresponding data receiver only once a true code has been detected and also doesn't miss any wake-up request.

From a functional point of view, a WuRx is not required to meet the same Bit Error Rate (BER) performance as in the data receiver. Typically, a BER of better than 0.01% would be sufficient for this purpose. The corresponding SNR_{min} for this BER requirement can be found to be around 12 dB for On-Off Keying (OOK) modulation scheme. On the other hand, the signal power which is received at the input of the WuRx can be attenuated dramatically by the path loss and therefore

might not satisfy the desired SNR_{min} requirement after detection. In other words, sensitivity requirement should also be met in designing a WuRx.

Sensitivity in this context is defined as the smallest signal power at the input of a receiver (usually expressed in dBm) which achieves a minimum Signal to Noise Ratio (SNR_{min}) at the output of the receiver. A complete mathematical expression of the receiver sensitivity will be elaborated in Chapter 2.

1.3 WuRx Design Metrics

There is not one single Figure of merit (FOM) for evaluating ultra-low-power wake-up receivers. Dissipating ultra-low power from the supply, achieving the highest possible sensitivity, and waking up the main receiver with the shortest delay bring a considerable design challenge for wake-up receiver designers [15]–[27]. However, most of the work in this area considers the power and sensitivity as the two critical factors, where meeting the ultra-low power requirement of the WuRx is in the priority.

There is an inherit trade-off between the power dissipation and the overall sensitivity of every receiver. We will explore this trade-off in details in the next chapter. However, to enlighten the situation, let us consider the sensitivity to be a function of the input referred noise of the whole receiver chain, where the noise performance of the receiver would determine the sensitivity. We also know that in order reduce the noise, the circuit should provide more gain and more gain would translate into more power dissipation. Thus, by knowing the existing trade-off between the noise and power of every circuit, the above trade-off can be easily understood. Considering this, wake-up receivers are designed to consume ultra-low power from the supply while maintaining the sensitivity below some margin depending on the application. For example, the accepted power dissipation in WuRxs that are intended to be employed in wireless LAN, where data rates are

high, can be in the order of several milliwatts while the sensitivity is high [28]. Whereas, the accepted power dissipation for the WuRxs used in wireless sensor networks is typically below 100 μW.

In order to improve the sensitivity, the receiver must dissipate more power. The sensitivity can be also improved by lowering the data rate or the required channel bandwidth, which can be achieved independently of the power dissipation. However, reducing the data rate will be at the cost of increased latency for the wake-up receiver. Therefore, a more complete way of evaluating a wake-up receiver is the energy-sensitivity product, which also takes into account the latency of the wake-up receiver.

1.4 Background and Literature Review

As mentioned earlier, there is a trade-off between the sensitivity and power consumption of receivers.

In general, traditional receiver architectures such as super-heterodyne and homodyne receivers [1]–[3] consume a large amount of power (i.e. > 1 mW) due to the large power dissipated by the Local Oscillator (LO) whose power is proportional to the operating frequency.

The super-regenerative architecture [9], [10], [26], [29]–[31] on the other hand achieves high sensitivity at a lower power consumption but requires frequent calibration for frequency stability.

A BPSK super-regenerative receiver is shown in Fig. 1.1 and is presented in [29]. The receiver consists of a power divider, two injection-locked *RC* oscillators followed by limiting buffers, and an XOR at the output stage. The operation of the receiver can be summarized as follows. The BPSK signal with certain power to lock both oscillators is received at the front-end. The free running frequencies f_{r1} and f_{r2} generated by the oscillators would undergo a phase change by -90° and

+90° respective, resulted from 180° phase change in the input signal. Finally the output XOR circuit acts as a demodulator to recover the digital signal.

Their proposed receiver consumes 216 μW from 1.2 V supply, and performs a sensitivity of -50 dBm at a data rate of 2 Mbps. The sensitivity of the receiver is limited by the required RF power to lock the oscillators, which is normally larger than the input-referred noise floor. However, adding a pre-amplifier before the oscillators could improve the sensitivity at the expense of larger power dissipation.

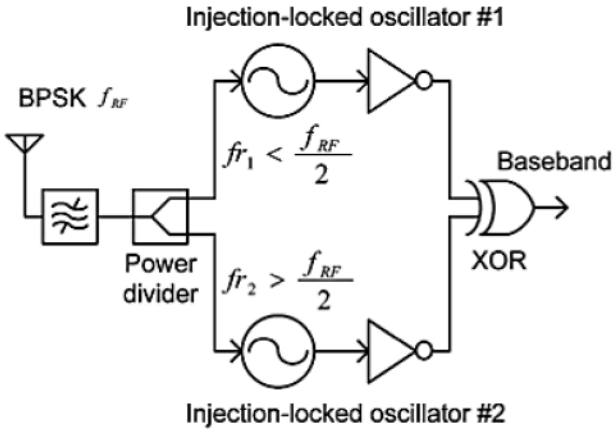


Fig. 1.1: Block diagram of an ultra-low-power BPSK receiver based on injection-locked oscillators [29]

Another super-regenerative BFSK ultra-low-power receiver is presented in [9]. The receiver is claimed to minimize the power consumption while maintaining very high energy-efficiency. The simplified block diagram of this receiver is shown in Fig. 1.2. The super-regenerative oscillator samples the received signal at two different frequencies (f_1 and f_2) within a bit period and the sampled data are compared. The oscillator is initially tuned to f_1 and the resulting oscillation due to the incoming signal is rectified and stored. Then the oscillator is tuned to f_2 and the same procedure is repeated. Finally, if the stored rectified voltage due to the

oscillation at f_1 is larger than the voltage due to the oscillation at f_2, it shows that the input bit is "0" and vice versa.

The sensitivity of the receiver depends on the Q of the oscillation as well as on how much the two frequencies (f_1 and f_2) are apart. This is because higher Q_{osc} results in larger time difference to build oscillation and thereby higher comparator sensitivity. The total receiver dissipates 215 µW when operating with a data rate of 250 kbps and a sensitivity of -86 dBm.

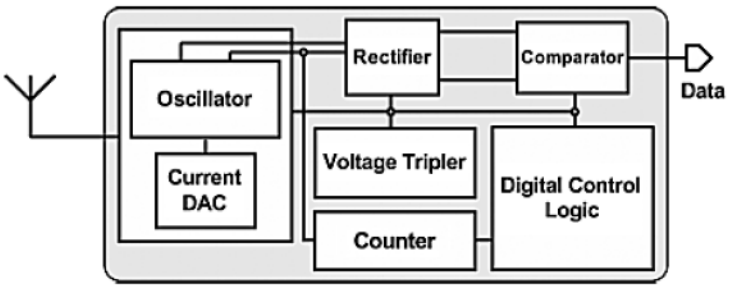


Fig. 1.2: Block diagram of the low-power super-regenerative receiver [9]

Tuned Radio Frequency (TRF) receivers have the simplest architecture comprising an antenna, a low-noise amplifier and an envelope detector [18]–[22], [32]–[39]. Aside from its simplicity, the power consumption of such a receiver is substantially lower than that of a homodyne or super-heterodyne receiver. The simplest example of this type of receiver is the remotely powered RFID integrated system that dissipate only 1 µW as in [40].

One of the challenges in designing TRF receivers is the issue of filtering or channel selection at RF that requires high-Q filtering. Heterodyne receivers reduce this Q by moving some of the filtering to the IF section. Another disadvantage of TRF receivers is their incompatibility with frequency-modulated signals. Envelope detection is only consistent with amplitude modulation schemes such as OOK, which is more power efficient but less spectrally efficient compared to other complex modulation schemes such as FSK, PSK and the like. Adding a

discriminator circuit may resolve the incompatibility problem at the expense of more complexity and power dissipation.

Another critical drawback of TRF receivers is their low sensitivity due to the use of envelope-detector circuits with small conversion gain. A practical approach to mitigate the sensitivity problem is to improve the gain in the preceding stages prior to the detector by making use of power dissipating RF amplifiers with high gain. In spite of the above drawbacks, TRF receivers have been widely employed in designing ULP receivers as a result of their low power and simplicity and thus are suitable candidates for wake-up receivers.

The TRF receiver shown in Fig. 1.3 employs a mixer to downconvert the signal from RF to IF region where the prior-to-detection amplification would be less power consuming [22]. Also, in order to save power, an inverter-based ring-oscillator is used to generate the LO frequency. However power efficient ring-oscillators have inferior phase noise performance and worse frequency uncertainty than power hungry LC resonators. Therefore, in order to relax the requirements, the LO frequency is allowed to vary over a relatively wide range (i.e. 100 MHz) around the RF frequency allowing the down-converted signal to lie close to DC within a bandwidth of IF-uncertainty. This receiver topology is known as the "*Uncertain-IF*" topology.

The disadvantage of this architecture is sensitivity to interference since any undesired signal within the LO bandwidth will be downconverted and detected by the envelope detector if not fully rejected through front-end filtering. Therefore, in order to improve the robustness to interferers, a high Q bandpass filter is required at the receiver's front-end. In fact, selectivity of the LO has been shifted to that of RF filter. Another drawback of this architecture is the limited sensitivity of the receiver due to the amplifier's noise integrated over the wide IF-bandwidth. The reported power consumption and sensitivity of this 2.4 GHz ISM band WuRx are 52 μW and -72 dBm at a data rate of 100 kbps respectively.

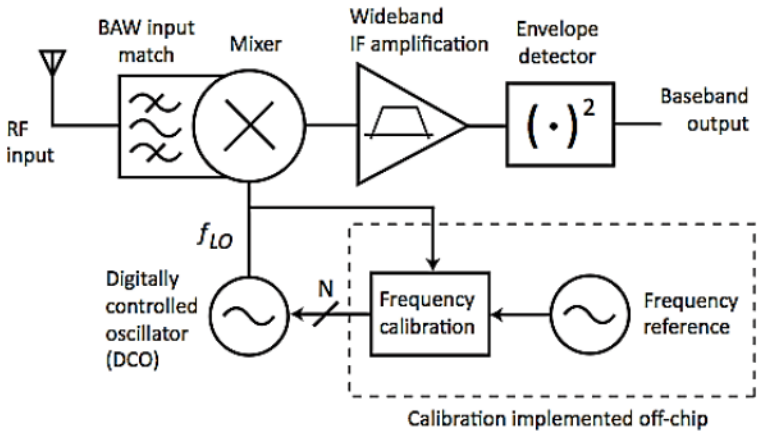


Fig. 1.3: Block diagram of the *Uncertain-IF* WuRx architecture [22]

Another TRF receiver using a double-sampling technique has been presented in [34] as a WuRx operating at 915 MHz and 2.4 GHz frequency bands. Fig. 1.4 shows the block diagram of the receiver. The double-sampling technique has been used not only to suppress the *1/f* noise and DC offset but also to flatten the output noise floor of the receiver. The receiver consumes 51 µW of power while achieving sensitivity of -75 dBm for a data rate of 100 kbps at 915 MHz and a sensitivity of -64 dBm at 2.4 GHz frequency.

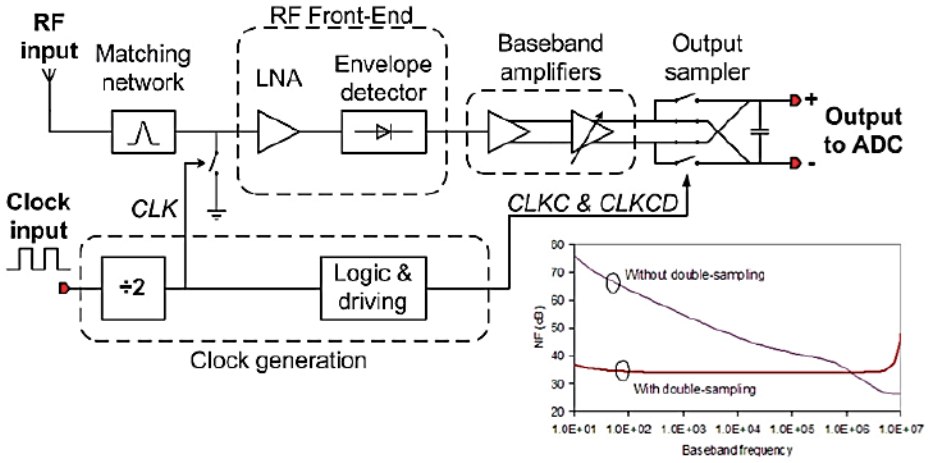


Fig. 1.4: Block diagram for a WuRx with double sampling technique [34]

In conclusion, considering the inevitable trade-off between the power consumption and sensitivity, RF designers have improved the power/sensitivity of wake-up receivers either by lowering the power consumed by the LO in FSK receivers with substantially better sensitivity, or by improving the sensitivity of the envelope-detector in low-power OOK receivers.

Down-converting an RF signal to IF can be performed using a subsampling element instead of a commonly used mixer. RF Subsampling receivers are known to be less power consuming compared to other traditional receiver architectures by employing LO operating at a much lower frequency. Subsampling receivers are composed of a sample and hold circuit, which down-converts the RF signal to IF without requiring a power hungry LO, since the sampling frequency can be much lower than the incoming RF frequency. The implementation of such a receiver also requires designing a bandpass anti-aliasing filter in order to reject the inevitable images associated with subsampling. A block diagram of a subsampling receiver [41] is shown in Fig. 1.5. Several low-power receivers have been designed using this technique where the sampler is usually preceded by a front-end amplifier stage [42]–[45] .

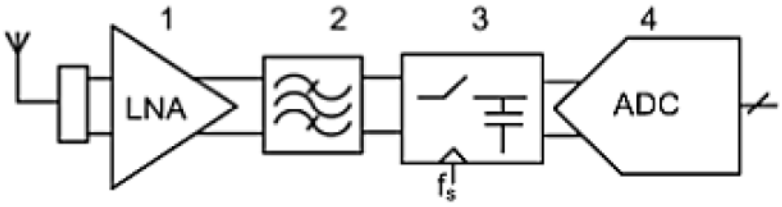


Fig. 1.5: Block diagram of a simplified subsampling receiver [41]

Duty-cycling schemes can be also applied to wake-up receivers in order to further reduce the average power consumption while maintaining sensitivity [46]–[49]. However, this approach may increase the latency of the receiver [50]. A new method to overcome this limit has been presented in [51] by offering two modes of operation for the wake-up receiver. The Start Frame Bits (SFB) bits are received in

the Monitoring mode (MO) while the rest of the wake-up packet is received during the Identifier mode (ID). Bit-level duty-cycling of 0.6% has been only applied in the MO mode with a data rate of 1 kbps and the ID bits are received with 100% duty-cycling and at higher data rate of 200 kbps. The block diagram of the dual - mode wake-up receiver is shown in Fig. 1.6.

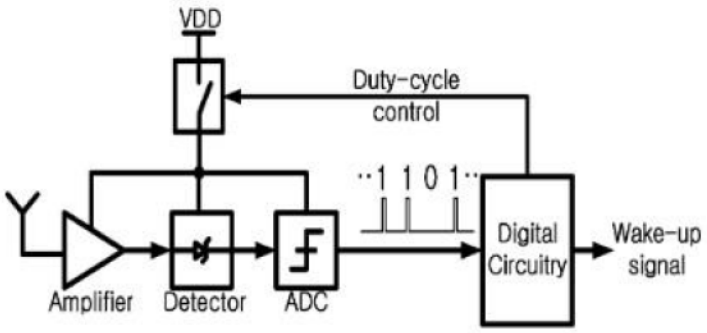


Fig. 1.6: Block diagram of a dual-mode wake-up receiver [51]

The reported measurement results for the sensitivity and power are -73 dBm and 8.5 µW, respectively. However, the downside of this implementation is that the power dissipation during the ID mode is still high (1078 µW) due to the use of a power hungry amplifier at the front-end of the receiver.

1.5 Objectives and Design Specifications

So far, some of the recently published ultra-low power receivers and wake-up receiver architectures have been reviewed.

Fig. 1.7 shows the plot of the dissipated energy per bit vs. sensitivity for the recent ultra-low power receivers. In order to distinguish between the wake-up receivers and other low-power receivers, only ultra-low power receivers with total power dissipation below 100 µW are considered in this plot.

The objective of this work is to design and implement a novel wake-up receiver for 915-MHz ISM band and in particular for wearable and implanted biomedical devices, which should not only be ultra-low power, but also has to ensure a relatively high energy efficiency while at the same time maintains an acceptable sensitivity.

It can be seen from the plot of Fig. 1.7 that the lowest power dissipation for wake-up receivers is about 3 µW with a sensitivity of -83 dBm [47]. This ultra-low-power operation has been achieved through the use of duty cycling. However, the sensitivity has been reported for a data rate of 64 bps and hence the energy efficiency of this receiver is clearly worse than the other wake-up receivers.

The free-space path loss (FSPL) grows with the square of the carrier frequency. It is also proportional to the n^{th} power of the distance between the transmitter and receiver, where n is the empirical path loss exponent and is typically equal to 3 [52], [53]. For our target biomedical implantable device with the operating frequency of 915 MHz, the link distance will be in the range of 10s of meters. Therefore, for a typical 15 meters' link, the receiver sensitivity must be better than about -67 dBm assuming 0 dBm power at the output of the transmitter.

From the above discussion, the desired margin for the target wake-up receiver has been specified in Fig. 1.7.

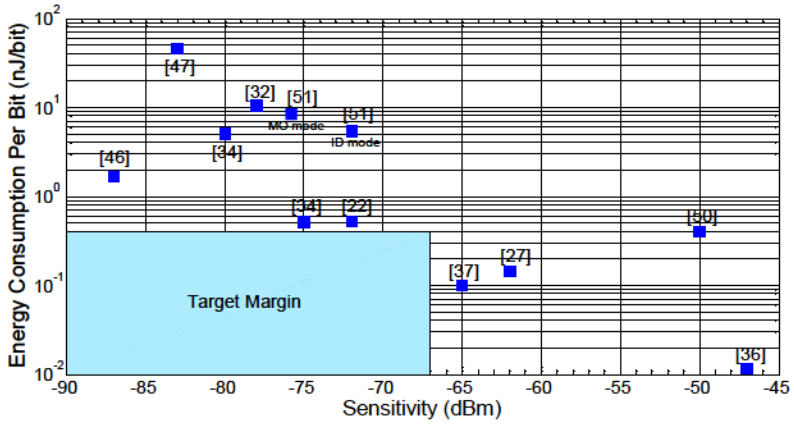


Fig. 1.7: State-of-the-art ultra-low power wake-up receivers

One can define the frequency spectrum in the 915-MHz ISM band as depicted in Fig. 1.8, which is composed of 50 frequency-hopping channels, each having 100 kHz of bandwidth and 200 kHz spacing. The 5.6 MHz margin at the two sides of the spectrum is to provide a better immunity to interferences.

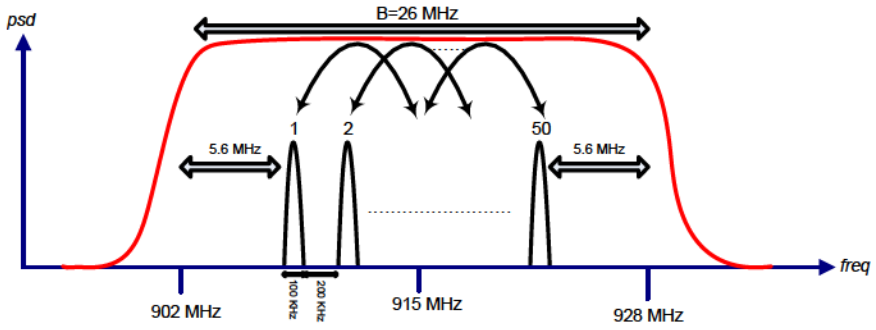


Fig. 1.8: Frequency spectrum of the 915-MHz ISM band channels

Some of the design specifications of the target wake-up receiver are summarized in Table 1.1. As stated earlier, the OOK modulation is a simple power-efficient scheme and since it is consistent with the TRF receiver topology, it has been employed in our design. The minimum required SNR of 12 dB for the wake-up receiver that uses OOK modulation approach ensures the desired BER of 10^{-3} at the output of the receiver.

Table 1.1: General design specifications for the target wake-up receiver

Frequency (MHz)	915-MHz ISM band
Modulation type	OOK
Sensitivity (dBm)	Better than -67
Minimum Output SNR (dB)	12
Data Rate	10s to 100s kbps
Power (µW)	<< 50

1.6 Thesis Organization

Chapter 2 begins with a thorough analysis of the existing trade-off between the power and sensitivity in a TRF receiver architecture and defines the terms and equations that have been used throughout the thesis. According to the power-sensitivity requirement presented in Chapter 2, the subsampling based wake-up receiver architecture is introduced in Chapter 3. In this Chapter, the circuit-level design procedure for each block of the receiver as well as the layout view of the proposed receiver followed by the simulation results for the implemented receiver have been presented.

Chapter 4 covers the core of this dissertation by presenting a novel architecture for an energy-efficient ultra-low power wake-up receiver based on the combined subsampling receiver topology described in Chapter 3 with the dual-mode architecture. A detailed test plan as well as the complete measurement results for the implemented wakeup receiver is in Chapter 5.

Finally, Chapter 5 concludes the thesis and presents some of the potential future works in this area of research.

Chapter 2

Power-Sensitivity Trade-off in TRF Receivers[54]

In the first chapter, some of the existing low-power receiver architectures were reviewed. The TRF topology was found to be one of the frequently used candidates for WuRx architecture. It is also known that most of the dissipated power in a TRF receiver is due to the amplifier stage at the front-end. On the other hand, considering the limited *gain-bandwidth* (GBW) product for a single stage amplifier, analog designers often prefer to use multistage-amplifiers with an optimum number of stages for a given total gain in order to maximize the overall gain-bandwidth product. From the sensitivity point of view of a receiver, there is a trade-off between the sensitivity and power dissipation, meaning that improving the sensitivity involves more gain and hence more power dissipation by the receiver.

This chapter begins with a discussion on the use of multistage amplifiers and the optimum number of cascades stages. Later, required terms and equations for defining the sensitivity in a generic TRF receiver will be presented.

Ultimately, the power-sensitivity trade-off in TRF receivers will be explored and the impact of design parameters such as the operating frequency, the effective bandwidth of the amplifier at the receiver front-end, conversion gain of the envelope detector, as well as the number of cascaded amplifier stages on this trade-off will be investigated from the theoretical equations and later justified by circuit-level simulation results.

2.1 Optimum Number of Cascaded Stages

Achieving very high gain values can become impossible with a single stage amplifier. This is because the required gain-bandwidth product may become much more than the f_T of the transistor. However, this can be realized with multistage amplifiers.

Multistage amplifiers can boost the total gain-bandwidth product (GBW_{tot}) with respect to that of a single stage amplifier (GBW_{S}) by a large number.

As a first order approximation, assume an N-stage amplifier is comprised of N identical single-pole amplifiers with a gain of G and a dominant pole of f_H at each stage. It can be shown that the overall bandwidth of an N-stage amplifier is shrunk according to the following expression [57], where f_H is the bandwidth of each stage of the amplifier:

$$f_{H^T} = f_H(\sqrt{\sqrt[N]{2}-1}) \tag{2.1}$$

It is obvious that (2.1) sets a limit on the maximum number of cascaded stages as GBW_{tot} starts to fall beyond the optimum number of stages N_{opt}. This is the point that the $GBW_{\text{tot}}/GBW_{\text{S}}$ ratio known as the GBW extension ratio has been maximized.

The optimum number of stages N_{opt} that maximizes the $GBW_{\text{tot}}/GBW_{\text{S}}$ ratio can be derived by differentiating this ratio with respect to the number of cascaded stages N and equating it to zero. Thus, taking the total gain of the multistage amplifier as G_T one can write:

$$\frac{GBW_{tot}}{GBW_S} = \frac{G_T\sqrt{\sqrt[N]{2}-1}}{\sqrt[N]{G_T}} \tag{2.2}$$

And hence:

$$\frac{\partial(\frac{GBW_{tot}}{GBW_S})}{\partial N} = \frac{1}{N^2} G_T^{1-1/N} \times \ln(G_T) \times \sqrt{2^{1/N}-1}$$
$$- \frac{\frac{1}{N^2} G_T^{1-1/N} \times \ln(2) \times \sqrt[N]{2}}{2\sqrt{2^{1/N}-1}} = 0$$

$$\frac{G_T^{1-1/N}}{N^2}\left[\ln(G_T)\sqrt{2^{1/N}-1} - \frac{\sqrt[N]{2}\ln(2)}{2\sqrt{2^{1/N}-1}}\right] = 0 \tag{2.3}$$

Equation (2.3) leads to the following expression:

$$G_T = G^{N_{opt}} = e^{\frac{N_{opt}\sqrt[N_{opt}]{2}\ln(2)}{2(\sqrt[N_{opt}]{2}-1)}} \tag{2.4}$$

According to (2.4), one can plot the optimum number of stages with the respect to the total gain on the logarithmic scale as shown in Fig. 2.1. It is obvious that as the total gain increases, more stages will be required to maximize the GBW_{tot}/GBW_S ratio.

From another point of view, one may want to study the total dissipated current in an N-stage amplifier in order to find the optimum number of stages that minimizes the overall dissipate current for a given GBW_{tot}.

Consider that $I_{tot} = N.I_S$, where I_S defines the current at every stage of the amplifier. Also note that I_S is linearly proportional to the transconductance of the active transistor g_m (assuming weak-inversion operation) and to the unity gain frequency f_u. Therefore, the overall current can be written in term of the GBW_S as below:

$$I_{tot} \propto f_u \times N = \mathrm{GBW_S} \times N = \sqrt[N]{G_T} \times \frac{f_{H^T}}{\sqrt{2^{1/N}-1}} \times N \tag{2.5}$$

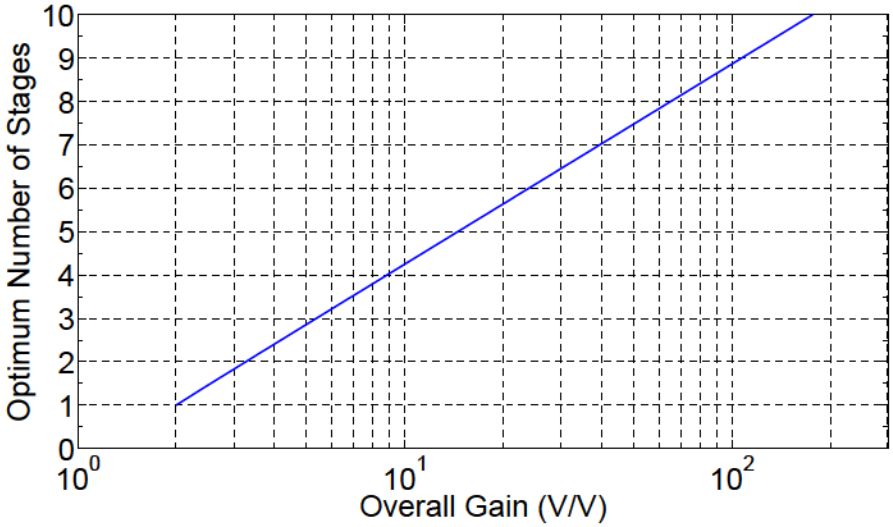


Fig. 2.1: The optimum number of stages vs. the total gain in a multistage amplifier leading to the maximized *GBW* extension ratio

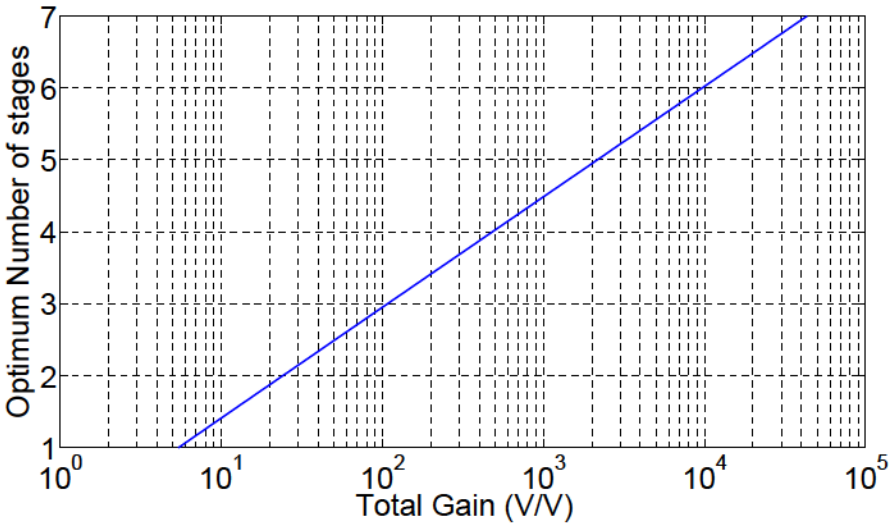


Fig. 2.2: The optimum number of stages vs. the total gain for a multistage amplifier leading to the minimum required total current consumption

By differentiating (2.5) with respect to N and equating it to zero, the optimum number of stages which yields the minimum total current consumption for a given total gain can be found by solving the following equation:

$$G_T = G^{N_{opt}} = e^{\frac{2N_{opt}\times(\sqrt[N_{opt}]{2}-1)+\sqrt[N_{opt}]{2}\ln(2)}{2(\sqrt[N_{opt}]{2}-1)}} \tag{2.6}$$

Note that (2.6) assumes that the required GBWs can be achieved using the given technology. The optimum number of stages yielding the minimum current consumption for a given total gain can be found by plotting (2.6) as shown in Fig. 2.2.

Aside from designing the multistage amplifier for maximum GBW extension ratio as well as for minimum current consumption discussed above, finding the optimum number of stages to achieve the minimum power-sensitivity product is another interesting aspect when dealing with N-stage amplifiers that are used at the front-end of a receiver. In order to address this point, a complete noise and sensitivity analysis for a TRF receiver will be necessary prior to finding the optimum value of N.

2.2 Sensitivity Calculation in a TRF receiver

Fig. 2.3 depicts a generic TRF receiver including an envelope-detector circuit, which has been implemented using NMOS transistors. It can be shown that the conversion-gain of the envelope-detector K is dependent on the magnitude of the AC signal V_s at the detector input such that $K = kV_s$, where k is a circuit-dependent parameter for high frequency signals at the detector input.

For the envelope detector circuit shown in Fig. 2.3, the conversion gain has the following expression [22], [58]:

$$K = \frac{ENV_{out}}{V_s} = kV_s = \frac{V_s}{4nV_T} \tag{2.7}$$

where V_s is the signal amplitude prior to the envelope detector, n is the subthreshold slope factor of M_1, which approximately equals to 1.5 in 90nm CMOS technology, and finally V_T is the thermal voltage at room temperature.

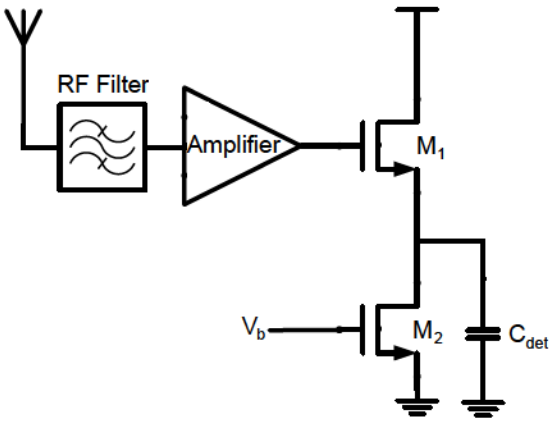


Fig. 2.3: Block diagram of a general TRF receiver with NMOS-based envelope detector circuit [22], [53], [58]

The overall noise factor for a generic TRF receiver that has been used in several works including [51], [53], [58] has the following expression:

$$F_{tot} = 2F_{amp} + \frac{N_{LF}K_{DC}^2 + N_{o,ED} + N_{o,amp\_ED}}{N_{source}A_v^2K^2} \tag{2.8}$$

This equation has been firstly derived in [58] having $N_{source} = 4K_BTR_s$ and K_BT is equal to -174 dBm/Hz at room temperature and R_s is the source resistance. The first term in (2.8) is known as the linear term as it linearly depends on the noise factor of the front-end amplifier F_{amp} with a factor of 2. Note that in this equation, A_v represents the total voltage gain of the front-end amplifier, including passive voltage gain in the input matching network.

The second term (2.8) is known as the non-linear component of the noise factor. The reason is that it inversely depends on the input power through the conversion gain of the envelope detector expressed by (2.7). The non-linear term also includes the low frequency noise density of the amplifier N_{LF}, the envelope detector noise density $N_{o,ED}$, and the density of front-end noise integrated at the amplifier's output and transferred to the output of detector N_{o,amp_ED}. Note that $K_{DC} \approx 1$ is the linear transfer function of the envelope detector for low frequency input signals including noise at frequencies below the envelop detector's bandwidth.

The low frequency noise density of the amplifier N_{LF} including the flicker noise depends on the particular design of the amplifier as well as on transistor sizes. For the envelope detector circuit shown in Fig. 2.3, the noise density can be written as below:

$$N_{o,ED} = 4K_B T\gamma \frac{1}{g_{m1}}(1+\frac{g_{m2}}{g_{m1}}) \tag{2.9}$$

where g_{m1} and g_{m2} are the transconductances of M1 and M2, K_B is the Boltzmann constant, and γ is approximately 2/3 for a long-channel-length transistor in the saturation region. However, the real value for γ for accurate noise estimation should be found for every technology.

We may introduce the effective bandwidth of the amplifier (or the noise bandwidth) as BW_{RF}=BW_{noise}. Having defined the variance of the noise at the amplifier's output by σ^2, the corresponding noise density at the output of the envelope-detector N_{o,amp_ED} will have the following expression as presented in [53]:

$$N_{o,amp\_ED} = (\frac{2\sigma^2}{4nV_T})^2 \frac{1}{BW_{noise}} \tag{2.10}$$

By calculating the total noise factor of the receiver as explained above, the input-referred noise power for matched input termination will be found as below:

$$P_{n,in} = -174 + 10\log(BW_{channel}) + NF_{tot} \tag{2.11}$$

In (2.11), NF_{tot} is the overall noise figure of the receiver expressed in dB, and $BW_{channel}=BW_{BB}$ is the channel or baseband bandwidth that is determined by the detector's output bandwidth.

Finally, the sensitivity of the receiver is defined as the minimum detectable signal P_{mds} yielding a minimum signal to noise ratio (SNR_{min}) at the receiver's output. The sensitivity can be found by solving the following equation where P_{in} is the input power in dBm.

$$P_{in}\,|_{P_{in}=P_{mds}} = P_{n,in} + SNR_{\min} \tag{2.12}$$

Now, let's derive the overall noise factor and sensitivity equations by initially writing the noise density contributions of different noise sources at the output of the receiver. The block diagram for a generic TRF receiver including the breakdown of noise sources have been shown in Fig. 2.4. The baseband amplifier and the low pass filter are assumed to be noiseless. Also note that the input termination is matched to the source resistance such that $N_i = K_B T$.

To obtain the variance of the noise at the output of the non-linear envelope detector, we start by writing the output y as a squared function of the input x containing both signal and noise, where $y=kx^2$.

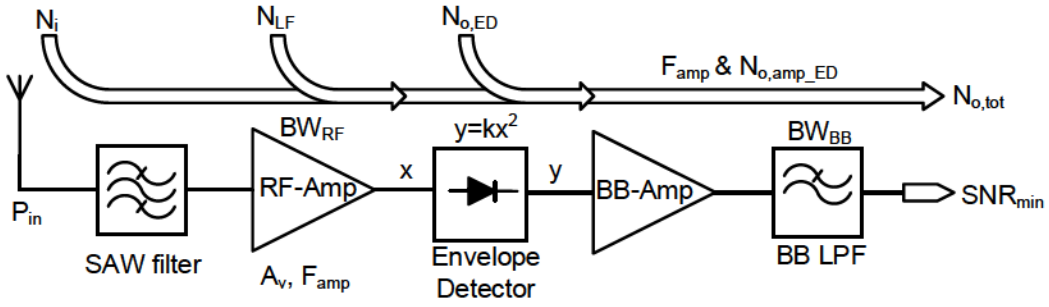


Fig. 2.4: Block diagram of a generic TRF receiver including the breakdown of noise sources

$$\begin{aligned} y = kx^2 &= k(S_{ED,in} + N_{ED,in})^2 \\ &= k(S_{ED,in}^2 + N_{ED,in}^2 + 2S_{ED,in}N_{ED,in}) \end{aligned} \tag{2.13}$$

where $S_{ED,in}$ and $N_{ED,in}$ are the signal and noise at the input of the envelope detector:

$$\begin{aligned} S_{ED,in}^2 &= P_{in}A_v^2 \\ PSD_{N_{ED,in}} &= N_i F_{amp} A_v^2 \end{aligned} \tag{2.14}$$

The variance of the output noise σ_y^2 can then be found by assuming that the input noise of the envelope detector would have zero mean and variance of $\sigma_{ED,in}^2$. Note that $\sigma_{ED,in}^2$ is in fact the total noise power at the input of the envelope detector which is integrated over BW_{RF}.

$$\sigma_{ED,in}^2 = PSD_{ED,in}.BW_{RF} \tag{2.15}$$

$$
\begin{aligned}
&\sigma_y^2 = \overline{y^2} - (\overline{y})^2 \\
&= k^2 E(S_{ED,in}^2 + N_{ED,in}^2 + 2S_{ED,in}N_{ED,in})^2 \\
&- k^2 (E(S_{ED,in}^2 + N_{ED,in}^2 + 2S_{ED,in}N_{ED,in}))^2 \\
&= k^2 (S_{ED,in}^4 + E(N_{ED,in}^4) + 6S_{ED,in}^2 E(N_{ED,in}^2) \\
&+ 2S_{ED,in}^3 E(N_{ED,in}) + 2S_{ED,in}N_{ED,in}^3) \\
&- k^2 (S_{ED,in}^2 + E(N_{ED,in}^2) + 2S_{ED,in}E(N_{ED,in}))^2
\end{aligned}
\tag{2.16}
$$

Taking into account the odd and even central moments of Gaussian distribution for the noise, (2.16) will be reduced to:

$$
\sigma_y^2 = 4k^2 S_{ED,in}^2 \sigma_{ED,in}^2 + 2k^2 \sigma_{ED,in}^4 \tag{2.17}
$$

where only half of this noise power will be located at the desired BB frequency:

$$
\sigma_{ED,out}^2 = \sigma_y^2 / 2 = 2k^2 S_{ED,in}^2 \sigma_{ED,in}^2 + k^2 \sigma_{ED,in}^4 \tag{2.18}
$$

Note that the first term in (2.18) comes from the mixing between the signal and noise while the second term is due to the noise self-mixing. The noise power spectral densities of the first and second terms in (2.18) can be found by convoluting the signal and noise as well as noise with itself for the frequency band between DC and BW_{RF}, respectively [59].

Finally, the total noise power at the receiver's output due to the RF stage can be derived by integrating the noise power spectral densities from 0 to the baseband signal bandwidth BW_{BB} as below:

$$
\sigma_{out}^2 \approx (4k^2 S_{ED,in}^2 \sigma_{ED,in}^2 + 2k^2 \sigma_{ED,in}^4) \frac{BW_{BB}}{BW_{RF}} \tag{2.19}
$$

Hence, the RF portion of the output noise density can be found from the following expression:

$$N_{o,RF} \approx (4k^2 S_{ED,in}^2 \sigma_{ED,in}^2 + 2k^2 \sigma_{ED,in}^4) / BW_{RF} \tag{2.20}$$

However, the total noise density at the receiver's output will contain other noise densities that are already illustrated in Fig. 2.4.

$$N_{o,tot} = N_{o,RF} + N_{LF} + N_{o,ED} \tag{2.21}$$

The overall RF and baseband gain from the receiver's input to the output of the envelope detector by considering only half of the signal resides at BB are found as below:

$$\begin{aligned} & S_{ED,out}^2 = k^2 S_{ED,in}^4 / 2 \\ & \rightarrow G_{tot\_RF}^2 = \frac{S_{ED,out}^2}{P_{in}} = \frac{k^2 (P_{in}.A_v^2)^2 / 2}{P_{in}} = k^2 P_{in} A_v^4 / 2 \end{aligned} \tag{2.22}$$

$$\begin{aligned} & S_{out,BB} = k(V_{in} A_v)^2 / 2 = k(\sqrt{2}.V_{in,rms} A_v)^2 / 2 \\ & \rightarrow G_{tot\_BB}^2 = \frac{S_{out,BB}^2}{V_{in,rms}^2} = \frac{k^2 V_{in.rms}^4 A_v^4}{V_{in,rms}^2} = k^2 V_{in,rms}^2 A_v^4 = k^2 S_{ED,in}^2 A_v^2 \end{aligned} \tag{2.23}$$

Therefore, the total noise factor of the receiver can be obtained from the following equation:

$$F_{tot} = \frac{N_{o,tot}}{N_i G_{tot}^2} = \frac{N_{o,RF}}{N_i G_{tot\_RF}^2} + \frac{N_{o,BB}}{N_i G_{tot\_BB}^2}$$
$$= \frac{(4k^2 S_{ED,in}^2 \sigma_{ED,in}^2 + 2k^2 \sigma_{ED,in}^4)/BW_{RF}}{N_i P_{in} k^2 A_v^4 / 2} \qquad (2.24)$$
$$+ \frac{N_{LF} K_{DC}^2 + N_{o,ED}}{N_i S_{ED,in}^2 k^2 A_v^2}$$

Finally, by replacing $S_{ED,in}^2$ and $\sigma_{ED,in}^2$ from (2.14) and (2.15) into (2.24), the total noise factor will be reduced to:

$$F_{tot} = 8F_{amp} + \frac{N_{o,amp\_ED} + N_{LF} K_{DC}^2 + N_{o,ED}}{N_i A_v^2 K^2} \qquad (2.25)$$

where $N_{o,amp\_ED} = (2\sigma_{ED,in}^2)^2 . k^2 / BW_{RF}$ and $K^2 = S_{ED,in}^2 . k^2$

The equations of (2.8) and (2.12) are in fact identical to each other and the difference between the factor of 8 and 2 in the first terms are coming from the fact that the input port of the receiver in deriving (2.8) has been assumed to be prior to the input matching network which leads to the noise voltage from the source resistance of $N_{source} = 4K_B T R_s$, while in the latter equation, the input port for calculating the noise factor has been taken after the input matching network so that the input noise power density is $N_i = K_B T$. However, by considering the above delicate point, it can be shown that both equations will result in the same input referred noise power and sensitivity expressions.

In order to calculate the sensitivity, one has to replace the expression for the total noise factor obtained in (2.25) in the sensitivity equation that is given by (2.11) and (2.12) and solve the final first order equation for the minimum detectable signal.

$$P_{mds} = N_i F_{tot} BW_{BB} SNR_{\min} =$$

$$8N_i F_{amp} BW_{BB} SNR_{\min} + \frac{4(N_i A_v^2 F_{amp})^2 BW_{RF} BW_{BB} SNR_{\min}}{P_{mds} A_v^4} +$$

$$\frac{(N_{LF} K_{DC}^2 + N_{o,ED}) BW_{BB} SNR_{\min}}{P_{mds} A_v^4 k^2}$$

$$\rightarrow P_{mds} = 4N_i F_{amp} BW_{BB} SNR_{\min} +$$

$$\sqrt{\begin{aligned}&16 \times (N_i F_{amp})^2 .(BW_{BB} SNR_{\min})^2 \\ &+[4 \times (N_i F_{amp})^2 BW_{RF} + \frac{(N_{LF} K_{DC}^2 + N_{o,ED})}{A_v^4 k^2}].(BW_{BB} SNR_{\min})\end{aligned}} \tag{2.26}$$

Three different scenarios can be inferred from (2.26):

In the first two cases, assume that there is enough gain provided by the front-end amplifier such that low-frequency noise components (including N_{LF} and $N_{o,ED}$) have been suppressed. Therefore, the sensitivity will only be limited by the RF stage noise:

$$\rightarrow P_{mds} = 4N_i F_{amp} BW_{BB} SNR_{\min} +$$

$$\sqrt{16 \times (N_i F_{amp})^2 .(BW_{BB} SNR_{\min})^2 + 4 \times (N_i F_{amp})^2 BW_{RF} BW_{BB} SNR_{\min}} \tag{2.27}$$

Now, if BW_{RF} is small or comparable to BW_{BB}, then the total noise factor is mainly dominated by the first term in (2.27), which is due to the mixing between the RF signal and noise. Therefore, the overall sensitivity can be reduced to:

$$P_{mds,SN} = 8N_i F_{amp} BW_{BB} SNR_{\min} \tag{2.28}$$

On the other hand, if BW_{RF} is large such that $BW_{RF} >> BW_{BB}$, then the output noise will be dominated by the self-mixed noise and the sensitivity can be approximated by:

$$P_{mds,N^2} = 2N_i F_{amp} \sqrt{BW_{RF} BW_{BB} SNR_{\min}} \tag{2.29}$$

Assuming BW_{BB} is 10 kHz for the data rate of 10 kbps, (2.27) has been plotted in Fig. 2.5 for different values of F_{amp} (shown on the plot by NF). The boundary point between the two approximations can be can be found to be BW_{RF}=16.BW_{BB}. SNR_{min}. It is shown that for BW_{RF} beyond around 2 MHz, the receiver sensitivity is obtained from the approximation of (2.29).

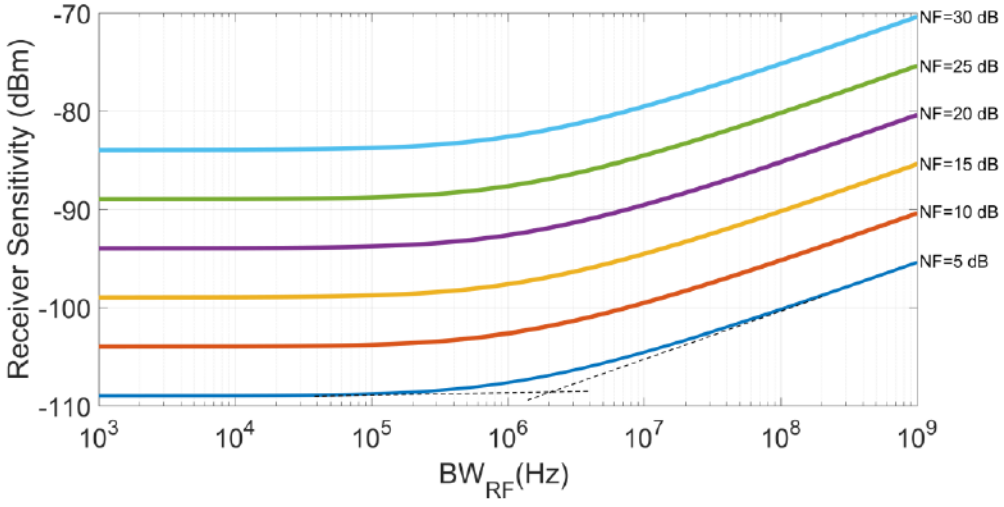


Fig. 2.5: Receiver Sensitivity as a function of NF and RF bandwidth at the data rate of 10 kbps when dominated by the RF stage noise

In the last scenario, the front-end gain is assumed to be not enough for suppressing the low frequency noise. As a result, sensitivity equation of (2.26) will be reduced to:

$$P_{mds,BB} = \frac{1}{kA_v^2}\sqrt{(N_{LF}K_{DC}^2 + N_{o,ED}).(BW_{BB}SNR_{\min})} \tag{2.30}$$

It is observed that A_v in this case has a quadratic impact on the overall sensitivity. It is also noted that the sensitivity is inversely proportional to the scaling factor of the envelope detector k.

Recall that the baseband amplifier and the low pass filter in Fig. 2.4 have been assumed noiseless in order to be consistent with the assumption made in [53], [58] in the derivation of equation (2.8). However, in a general case, all the baseband noise including the noise from the baseband amplifier as well as the low pass filter noise must be added to the existing low frequency noise components so that:

$$P_{mds,BB} = \frac{\sqrt{\overline{v_{n,eq}^2}.SNR_{\min}}}{kA_v^2} \tag{2.31}$$

where $\overline{v_{n,eq}^2}$ is the overall input-referred noise power at the input of the BB stages.

As a conclusion in this section, in order to improve the sensitivity in a general TRF receiver, it is preferred to use a narrowband filtering at the front-end (small BW_{RF}). This is usually difficult to satisfy especially when the data-rate is low and furthermore there is a limit on the power budget. Obviously, a lower NF from the front-end is also desirable. Finally, it was observed that the sensitivity can also be improved either by increasing the front-end gain A_v within the available power budget in order to suppress the BB noise or by trying to minimize the total input referred BB noise so that a lower A_v is required.

2.3 Power-Sensitivity Relationship

So far, the sensitivity of a generic TRF receiver has been studied and the effective parameters have been explored. In order to a gain better understanding on the existing trade-off between the power and sensitivity, the expressions for power consumption and sensitivity should be written in terms of circuit parameters. Also, to further simplify the analysis, following assumptions have been:

- An *N-stage* differential pair amplifier with resistive loads has been used as the RF front-end amplifier.
- Since most of the power is usually dissipated by the RF stage, the total power dissipation of the receiver can be approximated by the RF amplifier's power consumption.
- The low-frequency noise density of the envelope detector $N_{o,ED}$ has been estimated based on the design parameters used in [53]: $N_{o,ED}=9.46\times10^{-16}\ V^2/Hz$.
- The low-frequency noise of the amplifier N_{LF} as well as the flicker noise are initially ignored in this analysis for the sake of simplicity.
- The amplifier is biased in the weak inversion region so that the transconductance of each amplifying transistor can be estimated as $g_m=I_D/nV_T$.
- Data rate of 100 kbps has been chosen for the baseband bandwidth of BW_{BB}=100 kHz.
- The RF bandwidth BW_{RF} is assumed to be BW_{RF}=80 MHz which is much larger than BW_{BB}
- The required SNR_{min} is assumed to be 12 dB, which is the minimum SNR value for OOK modulation in order to get a BER less than 0.001

The first two stages of the multistage differential amplifier are depicted in Fig. 2.6. The odd stages including the first stage have a capacitor connected between the

sources of the two transistors. This capacitor adds a zero and a low-frequency pole to each stage. The high-frequency poles are created by the load resistance R_L and the total load capacitance C_L at each stage. As a result of adding a zero/pole at low frequencies, the effective bandwidth of the complete amplifier has a band-pass characteristic, meaning that:

$$BW_{eff} = f_{H^T} - f_{L^T} \tag{2.32}$$

where $BW_{eff}=BW_{RF}$ and f_{H^T}, f_{L^T} are the overall high and low 3-dB poles, respectively.

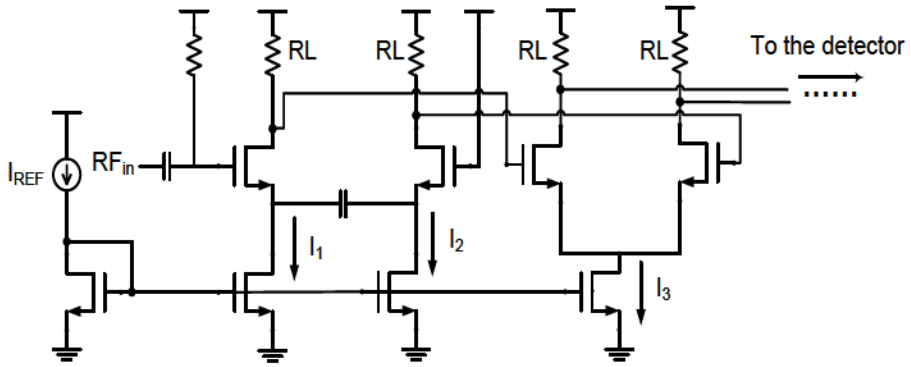


Fig. 2.6: Differential N-stage amplifier showing only the first two stages[53]

The overall midband voltage gain of the N-stage amplifier A_v assuming equal g_m and R_L can be written as:

$$A_v = (g_m R_L)^N \tag{2.33}$$

Having found the required bandwidth at each amplifier stage f_H for a desired f_{H^T} from equation (2.1), the required load resistance at each stage will be given by:

$$R_L = \frac{1}{2\pi f_H C_L} \tag{2.34}$$

Therefore, the required g_m at each stage for a desired total gain will be driven from:

$$g_m = \frac{\sqrt[N]{A_v}}{R_L} \tag{2.35}$$

The total dissipated current in the N-stage amplifier I_{diss} can be written in terms of the half-circuit current I_{hc} assuming $I_1=I_2=I_3/2=I_{hc}$. Also assume that the amplifying transistors in the differential amplifier of Fig. 2.6 are sized such that they will be operating in the weak or moderate inversion region for all values of N and A_v.

$$I_{diss} = N \times 2I_{hc} = N \times 2nV_T \times g_m \tag{2.36}$$

The overall noise factor and consequently the sensitivity expressions can also be derived in terms of the circuit parameters. Assuming equal noise factor F_1 and voltage gain A_{v1} for individual stages of the N-stage differential amplifier, the overall noise factor can be written using the Friis formula [60] as below:

$$F_{amp} = 1 + \sum_{i=0}^{N-1} (F_1 - 1)\left(\frac{1}{A_{v1}^2}\right)^i \tag{2.37}$$

This geometric equation can be simplified as:

$$F_{amp} = \frac{F_1 A_{v1}^2 - 1 - \frac{1}{A_{v1}^{2N-2}}(F_1 - 1)}{A_{v1}^2 - 1} \tag{2.38}$$

Assuming moderate value for A_{v1}, the noise contribution of the first stage will become dominant. Therefore, the simplified noise factor can be written as:

$$F_{amp} \approx F_1 = \frac{\overline{v_{n,out1}^2}}{\overline{v_{n,source}^2} A_{v1}^2} = \frac{K_B T R_s \times (g_m R_L)^2 + 2 \times 4 K_B T R_L (1 + \gamma g_m R_L)}{K_B T R_s \times (g_m R_L)^2} \quad (2.39)$$

In (2.39), $\overline{v_{n,out1}^2}$ is the thermal noise power at the output of the first stage and $\overline{v_{n,source}^2}$ is the noise power at the input source. Note that the factor of 2 in the numerator takes into account the two output branches of the differential amplifier.

In order to be compatible with the differential output of the multistage amplifier, a differential NMOS based envelope detector circuit as depicted in Fig. 2.7 has been used. It can be shown that the conversion gain K in the differential structure is 4 times smaller than K in the single-ended input envelope detector (which was presented earlier in Fig. 2.3), that is:

$$K = kV_s = \frac{V_s}{16nV_T} \quad (2.40)$$

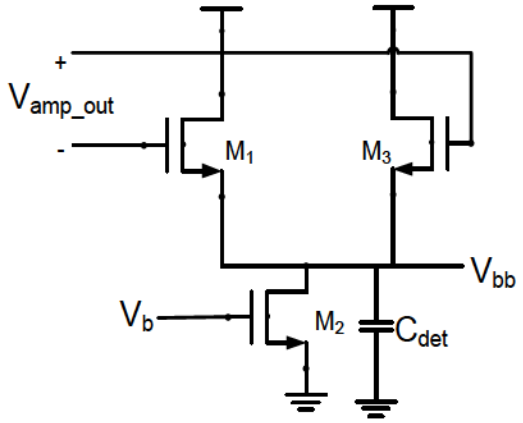


Fig. 2.7: Schematic of the differential envelope detector circuit [53]

The amplitude of the signal at the input of the envelope detector V_s can be expressed in terms of the input power P_{in} for a given front-end gain A_v and the source resistance R_s as below:

$$V_s = \sqrt{2 \times R_s \times 10^{(P_{in}+20\log(A_v)-30)/10}} \tag{2.41}$$

Eventually, the complete expression for the sensitivity given by (2.26) can be rewritten as below:

$$\rightarrow P_{mds} = 4N_i F_{amp} BW_{BB} SNR_{\min} + \sqrt{16 \times (N_i F_{amp})^2 .(BW_{BB} SNR_{\min})^2 + [4 \times (N_i F_{amp})^2 (f_{H^T} - f_{L^T}) + \frac{N_{o,ED}}{A_v^4 k^2}].(BW_{BB} SNR_{\min})} \tag{2.42}$$

where F_{amp} can be expressed in terms of amplifier's parameters by combining (2.33) to (2.35) and (2.39).

2.4 Theoretical Analysis

For the following analysis, f_{H^T} and f_{L^T} in the multistage amplifier have been taken as 106 MHz and 26 MHz, which gives the earlier assumed RF bandwidth of BW_{RF} =80 MHz. By following the equations (2.35) to (2.39), it can be shown that increasing the operating frequency f_{H^T} for a given total gain will result in a larger power consumption and a smaller amplifier noise factor. However, according to FSPL, the sensitivity requirement for the receiver will become more stringent as the operating frequency increases.

The effect of number of amplifier stages N on the current consumption as well as on the sensitivity for a given A_v is illustrated in Fig. 2.8 and Fig. 2.9, respectively. In these plots, N varies from 1 to 5 and A_v is increasing from 10 dB to 50 dB.

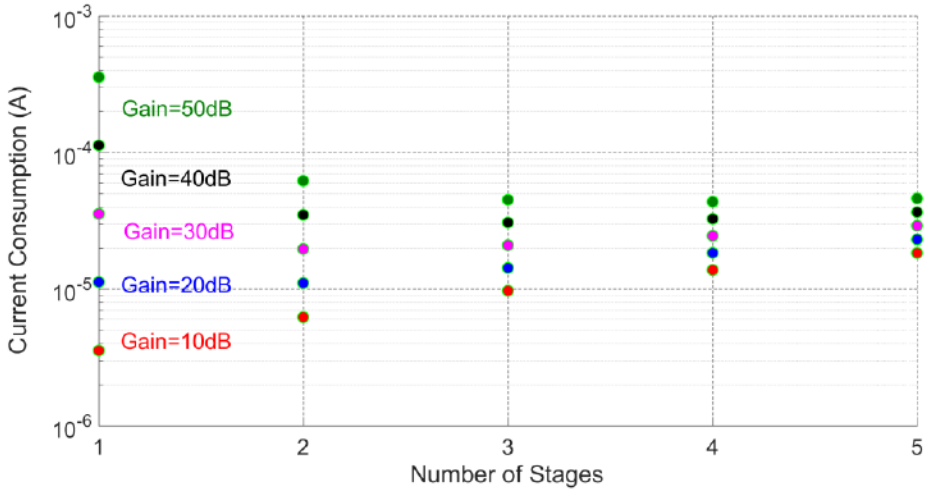


Fig. 2.8: Effect of number of amplifier stages on the current consumption by varying the total gain from 10 dB to 50 dB

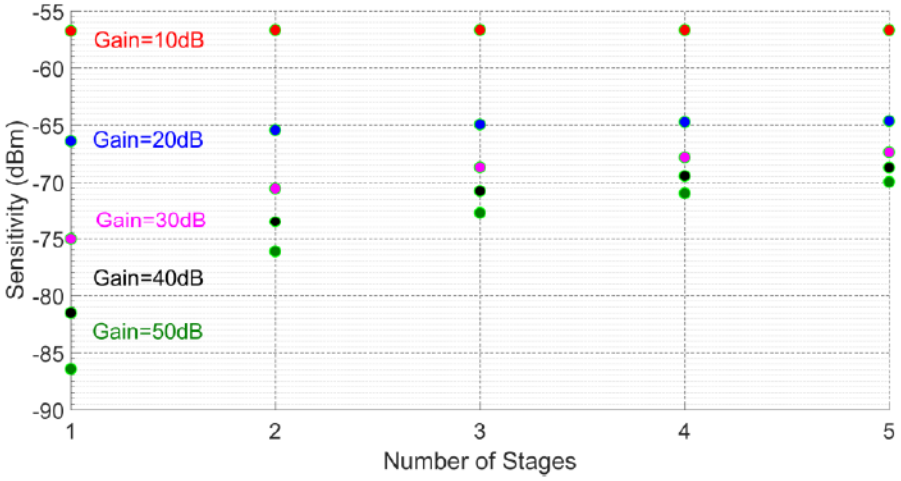


Fig. 2.9: Effect of number of amplifier stages on the sensitivity by varying the total gain from 10 dB to 50 dB

The optimum number of stages for each total gain value can be found from the plot of Fig 2.8, which clearly confirms our previous finding in Fig. 2.2.

It should be noted that in order to have a rough estimation for the value of the load capacitance C_L, which is required for this analysis according to (2.34), a side simulation has been performed in in TSMC90nm technology. It has been found that an NMOS transistor with a size of (W/L) = (10/0.2) µm/µm will ensure the required weak inversion operation for the above range of current variation. As a result, a total load capacitance value of C_L=26 fF has been derived from the simulation.

Regardless of the number of stages, the amplifier must clearly burn more power to achieve a higher gain as illustrated in Fig. 2.9. From the perspective of sensitivity, as A_v starts to grow from very small values as low as 10 dB, it is observed that the sensitivity improves significantly which is also expected from the sensitivity estimation of (2.30). However, as A_v becomes large enough to suppress all the BB and low frequency noise components (i.e. $N_{o,ED}$ in this simplified analysis), then the sensitivity will continue to improve at a slower rate, where the sensitivity is estimated by (2.29) since $BW_{RF}>>BW_{BB}$.

By combining the above two plots as shown in Fig. 2.10, it is observed that the multistage amplifier with fewer number of stages would in fact give a smaller value of *current×sensitivity* for a given A_v. In this plot, the dissipated current is expressed in *Amperes* and the sensitivity is in *Watts*. Since the value of the load resistance R_L has been already used to adjust the required f_{H^I} of the amplifier according to (2.34), the value of g_m for smaller number of stages has to rise in order to achieve the same total gain according to (2.35). As a result, smaller noise figure according to (2.39) and hence an improved sensitivity can be obtained for smaller number of stages at the expense of higher current dissipation based on (2.36).

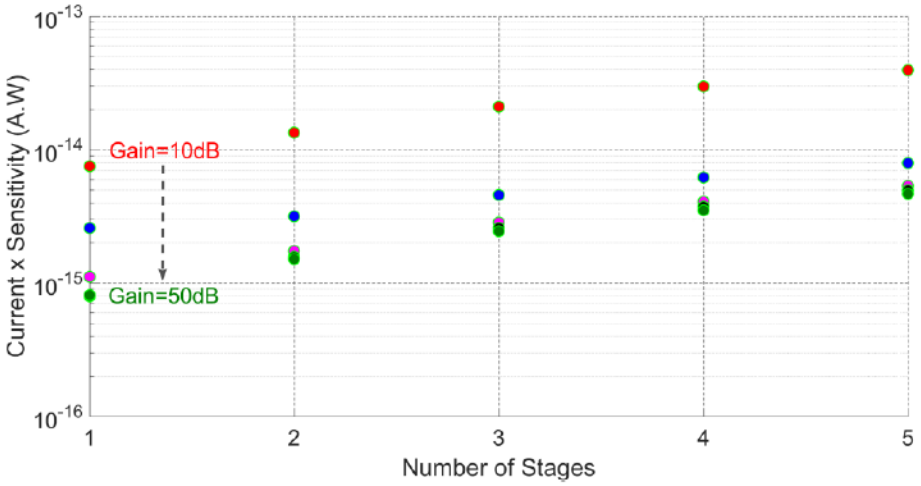


Fig. 2.10: Effect of number of amplifier stages on the *current×sensitivity* by varying the total gain from 10 dB to 50 dB

As shown in Fig. 2.10, from the perspective of *current×sensitivity*, the single stage amplifier seems to be the best option to be employed in a TRF receiver. Yet, there is another important factor that has to be taken into account for the *power×sensitivity* point of view. It is known that in order to keep a subthreshold MOSFET in saturation, the drain-source voltage must be greater than 4 times the thermal voltage (i.e. $V_{DS} > 4V_T$). which is approximately 100 mV at room temperature. Therefore, for proper operation, the required supply voltage that also effects the power dissipation should ensure this saturation criterion for the differential transistors in the multistage amplifier. The voltage drop across R_L is a suitable factor that can be used to determine the required minimum value for the supply voltage. In other words, the required supply voltage will be proportional to this voltage drop and therefore, the smaller the voltage drop across R_L, the lower supply voltage can the circuit accommodate.

Based on above, the *power×sensitivity* figure of merit can be expressed in the form of *current×sensitivity×IR drop* and is plotted for different gain values and number of amplifier stages as shown in Fig. 2.11.

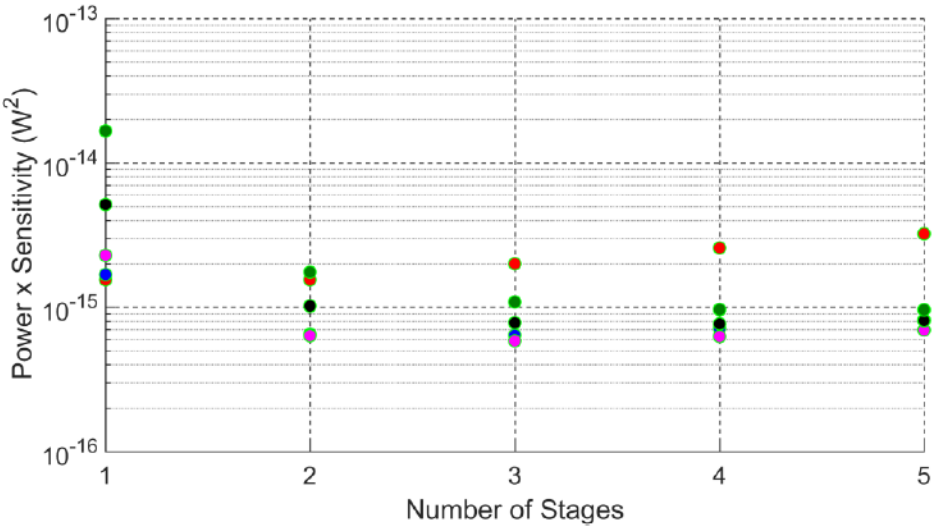


Fig. 2.11: Effect of number of amplifier stages on the *power×sensitivity* by varying the total gain from 10 dB to 50 dB

An interesting finding obtained from the plot of Fig. 2.11 is that a single stage amplifier is no longer a good candidate from the aspect of the *power×sensitivity*. This is mostly due to the higher required supply voltage that should sufficiently overcome the voltage drop across R_L in order to ensure saturation for all the transistors. Instead, a 2 or 3 stage amplifier with moderate total gain values (i.e. A_v =30 to 40 dB) seems to be better alternatives when the goal is to minimize the *power×sensitivity* rather than just the *current×sensitivity*.

To conclude this chapter, the power and sensitivity expressions for a generic TRF receiver were explored. Later, the power-sensitivity trade-off for a simplified receiver including a multistage amplifier have been analyzed and studied in terms of circuit parameters. It was discovered for instance that the optimum number of amplifier stages from the *power×sensitivity* point of view cannot be determined intuitively. However, depending on the application of the receiver, one design may sacrifice the sensitivity to achieve lower power consumption or burn more power to gain higher sensitivity.

Chapter 3

Subsampling-based Wake-up Receiver[20]

In previous chapter, a complete noise analysis for a general TRF receiver was presented. The analysis led to the plots of power and sensitivity for a simplified TRF receiver, which helped to a better understanding of the power-sensitivity trade-off. One thing that was surmised though not clearly mentioned in deriving these plots is that the input RF signal has been assumed to be initially downconverted to a lower frequency by means of a down-converting element such as a mixer in order to save the power dissipation in the front-end amplifier. Down-converting the high frequency signals to low frequency domain can be achieved by employing either a mixer or a subsampling circuit. In this chapter, an architectural approach to design and implement a subsampling-based wake-up receiver operating in 915-MHz ISM band will be presented.

3.1 The Subsampling Architecture

A Subsampling circuit in its simplest form is a sample and hold (S/H) or a tack and hold (T/H) circuit whose sampling frequency is only a portion of the incoming RF signal. The subsampling architecture is used to downconvert the RF signal to IF by aliasing. This is in contrast with the super-heterodyne architecture where downconversion is achieved through mixing rather than through sampling.

Let's assume the incoming RF signal is given in the time and frequency domains by $x(t)$ and $X(f)$, respectively. Therefore, the sampled signal at the output of the S/H circuit $x_s(t)$ can be written mathematically from the multiplication of $x(t)$ with Dirac impulses:

$$x_s(t) = x(t).\sum_{k=-\infty}^{\infty}\delta(t - k/f_s) \tag{3.1}$$

Taking the Fourier transform from both sides of the above equation will give the spectral representation of $x_s(t)$ as:

$$X_s(f) = X(f)f_s * \sum_{k=-\infty}^{\infty}\delta(f - kf_s) = f_s\sum_{k=-\infty}^{\infty}X(f - kf_s) \tag{3.2}$$

Therefore, the downsampled signals at the output of the subsampler are spaced f_s apart from each other. In other words, a subsampling receiver down-samples the RF signal to the intermediate frequency f_{IF} according to the following equation:

$$f_{IF} = \mid f_{RF} - nf_s \mid \tag{3.3}$$

where f_{RF} is the RF frequency, f_s is the sampling frequency generated by an LO and n is the sampling ratio. It should be noted that as a result of subsampling, the signal with the lowest frequency content is considered the IF.

Also, in order to avoid overlapping of the aliased signals in the 915 MHz-ISM band shown earlier in Fig. 1.8, Nyquist theorem states that:

$$f_{IF} > BW/2$$
$$f_s/2 > f_{IF} + BW/2 \tag{3.4}$$

where BW is the total bandwidth of the 915 MHz RF band.

A simplified model for the proposed sub-sampling based WuRx is shown in Fig. 3.1. The sampling frequency $f_s = 200MHz$ has been initially chosen to satisfy (3.4). However, as will be shown later there are other factors that have been considered in selecting f_s.

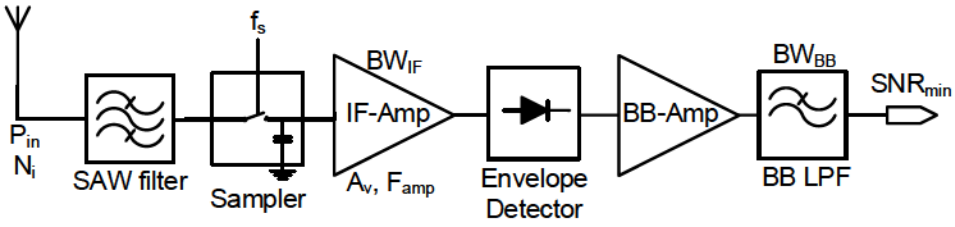


Fig. 3.1: Proposed architecture for the sub-sampling based WuRx

In practice, the sampling frequency, especially if generated by a ring oscillator may vary significantly over temperature, process, and mismatch [41], [42], [44], [45]. For this reason, as stated earlier, the uncertain-IF topology has been used in our design such that f_s could vary by ±5% from 200 MHz. Consequently, the bandwidth of the IF amplifier shown in Fig. 3.2 should be wide enough to take into account this LO inaccuracy.

Fig. 3.2 shows the variation in the sampling frequency f_s and the corresponding first harmonic of the down-converted signal f_{IF}, where the RF frequency is assumed to be at the center of the band; that is $f_{RF} = 915MHz$. It can be verified that the sampling ratio is 4 for sampling frequencies between 190 MHz and 203.3 MHz and is 5 for sampling frequencies between 203.4 MHz and 210 MHz.

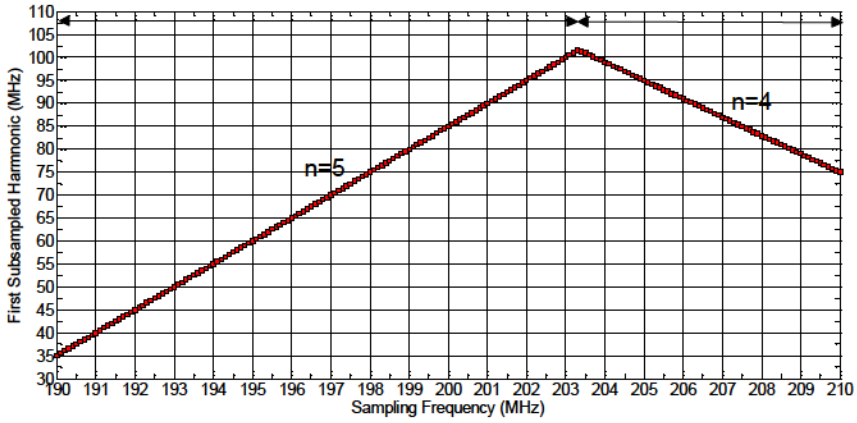


Fig. 3.2: IF signal vs. sampling frequency for $f_{RF} = 915MHz$ and for ±5% LO inaccuracy in the sampling frequency

According to the plot of the frequency spectrum for the 915-MHz ISM band that was already given in Fig. 1.8, it can be seen that for 20 MHz variation of the sampling frequency (i.e. 190-210 MHz), the subsampled signal varies from 35 to 100 MHz. Taking into account all 50 channels instead of only the center of the band, the total required bandwidth for the subsampled frequency would be $BW_{IF} = 65 + 15 = 80MHz$.

It is worth mentioning that the variation range of the sampling frequency should not include certain points (i.e. $f_s = f_{RF} / n$) for which the subsampled frequency would lie at DC. It can be verified that our desired LO frequency range from 190 to 210 MHz does not include any of these points.

3.2 Noise Analysis

The complete noise analysis for a TRF receiver was performed in Chapter 2 of this thesis. Consider the overall noise factor expression in (2.8) and assume that the total contribution of the baseband noise is negligible compared to that of the RF noise, that is:

$$F_{total} \cong 2F_{linear} + N_{o,amp\_ED} / (N_{source} A_v^2 K^2) \tag{3.5}$$

The parameters in (3.5) have been defined earlier in (2.8).

The noise factor of a standalone subsampler can be estimated through the following expression [41]:

$$F_{sampler} = (1 + 3.3/x^2) + 1/(2R_s C_s f_s) \tag{3.6}$$

The first term in (3.6) is due to the noise folding effect of the subsampler, where 1 accounts for the in-channel noise and $3.3/x^2$ takes into account the summation of all the noise powers at different image frequencies. The factor 3.3 is shown up as a result of using the solution to Basel's problem in finding the total contribution of the noise folding. Also, $x = Q/n$, where Q is the quality factor for the front-end filter, R_s is the source resistance, C_s is the sampling capacitor and f_s is the sampling frequency.

Assuming a high quality filter at the front-end of the receiver, the first term ideally approaches to 1. However, the second term in (3.6) that is due to the intrinsic noise of the sampler and can be plotted with respect to f_s for different values of C_s as shown in Fig. 3.3.

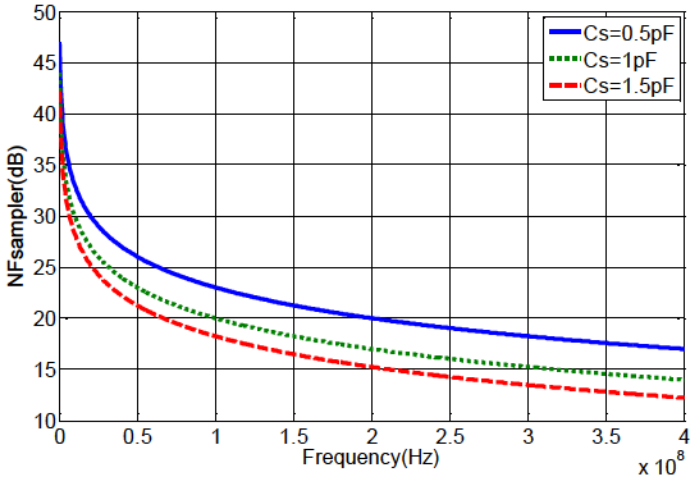


Fig. 3.3: Noise Figure of the subsampler vs. sampling frequency for three values of the sampling capacitor C_s

The selected value for f_s will affect the noise contribution of the subsampler according to Fig. 3.3. Therefore, the corresponding NF of the sampler can be estimated as 15 dB for $C_s = 1.5pF$ and $f_s = 200MHz$.

According to Friis formula, the total linear noise factor is found from:

$$F_{linear} = F_{sub-sampler} + (F_{amp} - 1) / G_{sampler} \tag{3.7}$$

where $G_{sampler}$ is ideally assumed to be 1 for the first downsampled harmonic. Note that the actual power gain of the subsampler can be smaller than 1. This will be revisited in Chapter 4.

3.3 Design Methodology

In this section, the design procedure for each block of the proposed WuRx is presented. Note that considering the target indoor application, the ultra-low power design requirement has been initially prioritized over the high sensitivity performance of the receiver. Furthermore, we have optimized the analog blocks of the receiver in order to operate from a single 500 mV analog power supply.

3.3.1 Differential Subsampling circuit

A differential sample and hold circuit as shown in Fig. 3.4 has been used to downconvert the RF signal to IF. The *W/L* for NMOS switches M1 and M2 are chosen to be large enough in order to lower the *on* resistance (R_{on}) of the switches thereby improving the speed of the sample and hold circuit for accurately receiving the input RF frequency. It is worth mentioning that M1 and M2 are chosen to be of ultralow-threshold voltage types and are biased in the triode region with their gate voltage varying between 0 and 0.5 V.

Note that the differential structure and dummy transistors M3 and M4 are employed in order to reduce the effect of charge injection and to cancel the even-order nonlinear distortion. As discussed earlier, the sampling capacitor C_s and the sampling frequency f_s have been chosen to be 1.5 pF and 200 MHz, respectively.

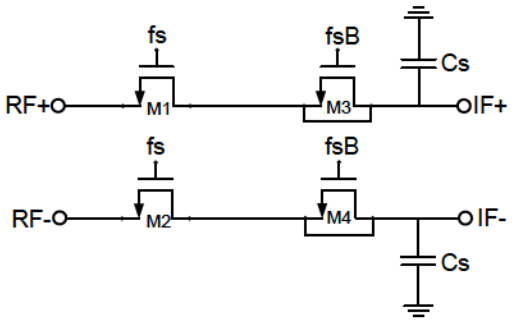


Fig. 3.4: Differential sample and hold circuit with dummy transistors

Assume an RF signal of 915 MHz with a power of -70 dBm (which is equal to a peak voltage of V_p = 100 μV for a source resistance of R_s = 50Ω) has been applied to the input of the S/H circuit of Fig. 3.6. The time domain plot of the sampled and held signal at the output of the S/H circuit is shown in Fig. 3.5. The frequency spectrum of this signal is also observed in Fig. 3.6. It can be seen that the first harmonic of the downconverted signal is located at 85 MHz (i.e f_{IF} = 85 MHz), which corresponds to f_s = 200 MHz and n = 5 for the subsampler.

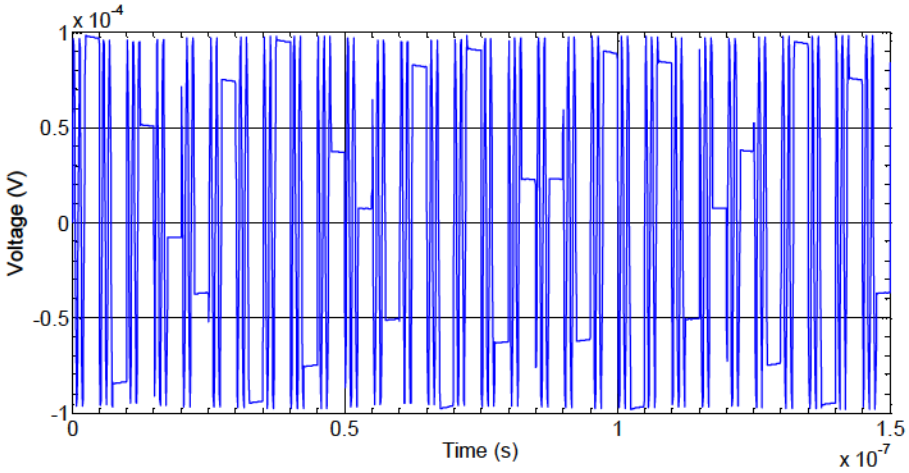


Fig. 3.5: Plot of the subsampled signal at the output of the S/H circuit

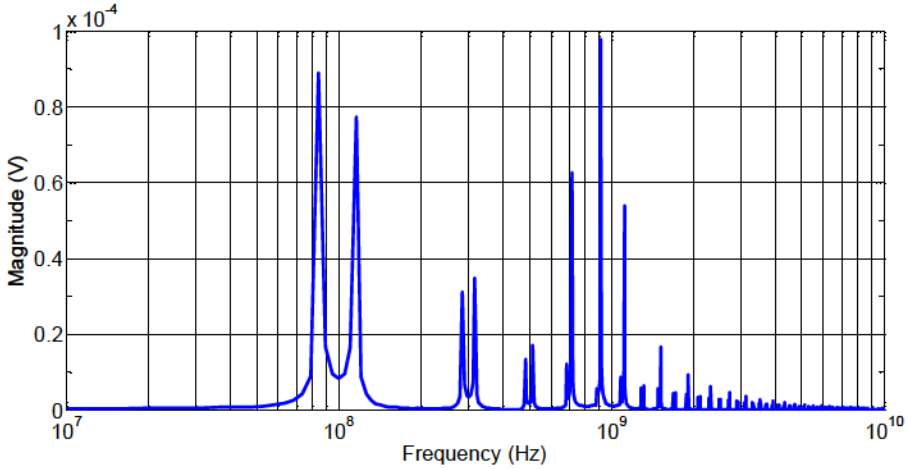


Fig. 3.6: Frequency spectrum of the subsampled signal

3.3.2 Three-Stage Temperature Invariant Ring-Oscillator

A simplified schematic for the 3-stage inverter-based ring oscillator is shown in Fig. 3.7. Two complementary signals with equal frequencies (i.e. f_s and f_{sB}) are generated after the buffers, which will be used by the subsampler circuit. The oscillator dissipates a total average power of 4 μW (including the buffers) from the 500 mV power supply.

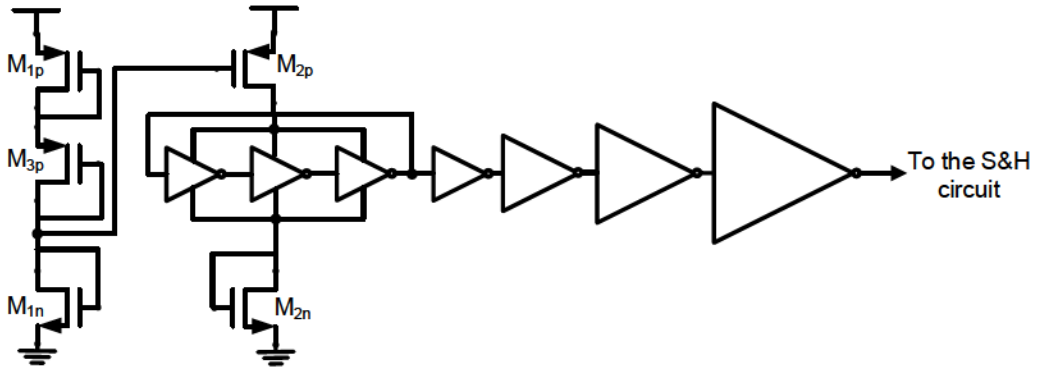


Fig. 3.7: The 3-stage ring oscillator with the temperature compensation circuit (TCC) and output buffers

In general, an increase in the temperature would lower the threshold voltage of MOS transistors [61]. Assuming a fixed voltage at the gate of M_{2p}, this will result in a larger drawn current from the supply and hence larger frequency of oscillation.

A Temperature Compensation Circuit (TCC) has been employed in order to lower the frequency variations due to temperature change. The transistors M_{1p}, M_{3p}, and M_{1n} are sized in a way that the gate voltage of M_{2p} varies in correspondent with the temperature in order to limit the frequency variations of the ring-oscillator. Variations of the sampling frequency as a result of a rise in the temperature from 10ºC to 80ºC with and without the TCC have been shown in Fig. 3.8. It is observed that using the TCC, the sampling frequency is kept within the range of 190 MHz to 210 MHz.

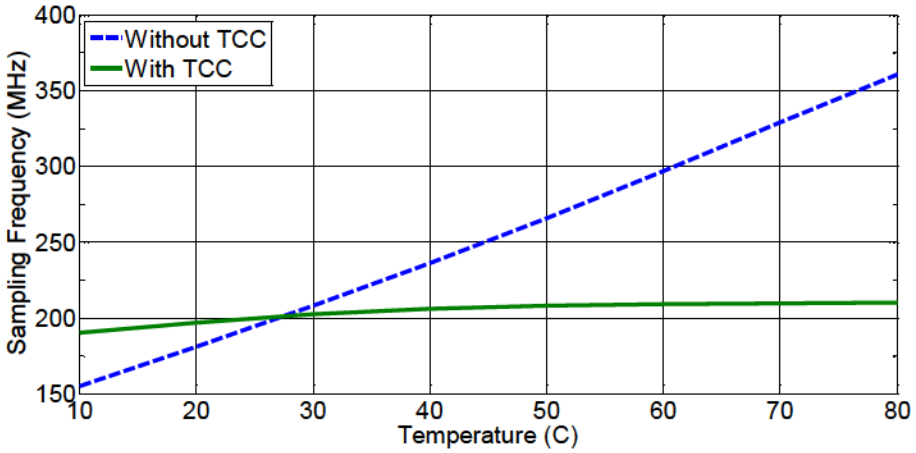


Fig. 3.8: Variation of sampling frequency with temperature in the presence and absence of the temperature compensation circuit (TCC)

The effect of process and mismatch variations on the sampling frequency has been shown in Fig. 3.9, which has be achieved for 100 iterations of Monte-Carlo simulation. In practice, transistor M_{2p} is replaced by a 32-bit switched resistive network based on triode region MOSFETs that are controlled by 5 serial input bits in order to compensate for local and global process variations.

The PMOS transistors of the 32-bit switched resistive network are sized such that the smallest size transistor (corresponding to the first address bit) causes the oscillator to generate a sampling frequency of 50 MHz, while the maximize size transistor (corresponding to the 32^{nd} address bit) leads to sampling frequency of 350 MHz. This gives a frequency resolution of around 9.7 MHz per 1 bit of the switched resistive network, which is sufficient considering the allowed ±5% variation for the nominal sampling frequency of 200 MHz.

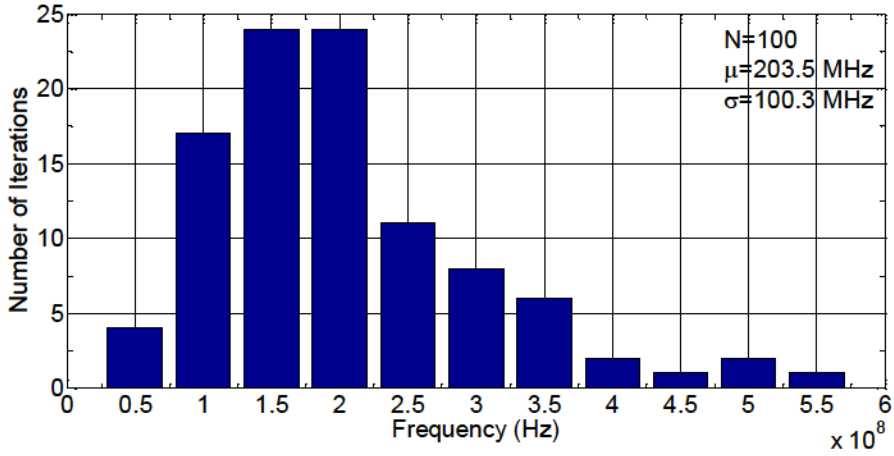


Fig. 3.9: Variations of the sampling frequency due to local and global process variations

Therefore, according to the histogram of Fig. 3.9, the 32-bit switched resistive network in the ring-oscillator can be used to efficiently compensate for a frequency deviation of around ±1.5σ from the mean value of 203 MHz, which covers almost 90% of the total variations.

3.3.3 Wideband IF-Amplifier and Envelope detector

The differential *N*-stage amplifier and the envelope detector circuit used in this design have the same schematic as described in Fig. 2.6 and Fig. 2.7 of Chapter 2, respectively.

It was studied in Chapter 2 of this thesis that for small front-end gain values, the overall sensitivity of a TRF receiver is almost dominated by the baseband noise that is approximated by the given expression in (2.30). However, as the front-end gain increases, for large RF bandwidth, the sensitivity will be estimated by the expression in (2.29). Therefore, the IF-amplifier has to be designed to achieve a sufficient voltage gain (i.e. 50 dB) in order to overcome the baseband noise and

therefore improve the sensitivity by providing enough input signal amplitude at the input of the envelope-detector.

The optimum number of amplifier stages yielding the minimum current consumption for a given gain has been previously estimated according to (2.6) and was plotted in Fig. 2.2. By revisiting this plot, it is observed that a 4-stage amplifier would get the lowest current consumption for an overall gain of 50 dB. However, from the point of view of the minimum power dissipation, for a given overall gain, the optimum number of stages for a total gain of 50 dB has been found to be 5 according to simulation results. This is because in spite of dissipating less current, the 4-stage amplifier requires slightly higher supply voltage (i.e. 0.54 V) compared to the 5-stage amplifier in order to satisfy the saturation requirement for the transistors based on (2.35).

The differential pair transistors of every stage of the N-stage amplifier shown in Fig. 2.6 are sized to be (W / L) = (10/0.2) μm/μm. This ensures the transistors to stay in the weak or moderate inversion region for all values of N and gain.

The overall gain and the noise factor of the 5-stage amplifier can be varied for the same bandwidth by adjusting the design parameters including the current consumption and the load resistance. As a result, the frequency response and the noise performance of a stand-alone 5-stage amplifier are obtained as shown in Fig. 3.10 and Fig. 3.11, respectively.

The total power consumed by the wideband amplifier has been found about 23 μW while the simulated voltage gain is 50 dB and the bandwidth is around 80 MHz. Fig. 3.12 demonstrates the frequency response of the circuit-level and extracted layout of the 5-stage IF-amplifier.

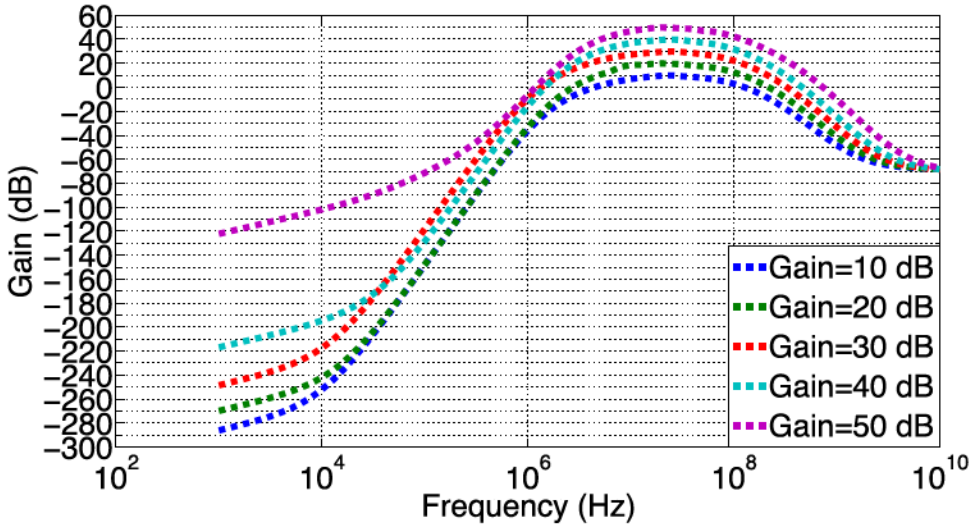


Fig. 3.10: Frequency response of the 5-stage IF-amplifier by varying the overall voltage gain for a fixed bandwidth

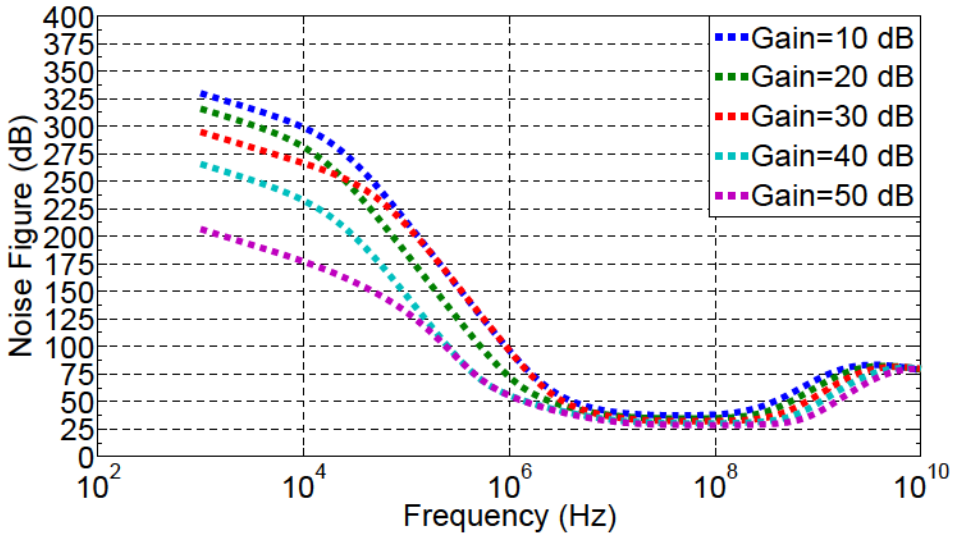


Fig. 3.11: Noise Performance of the 5-stage IF-amplifier

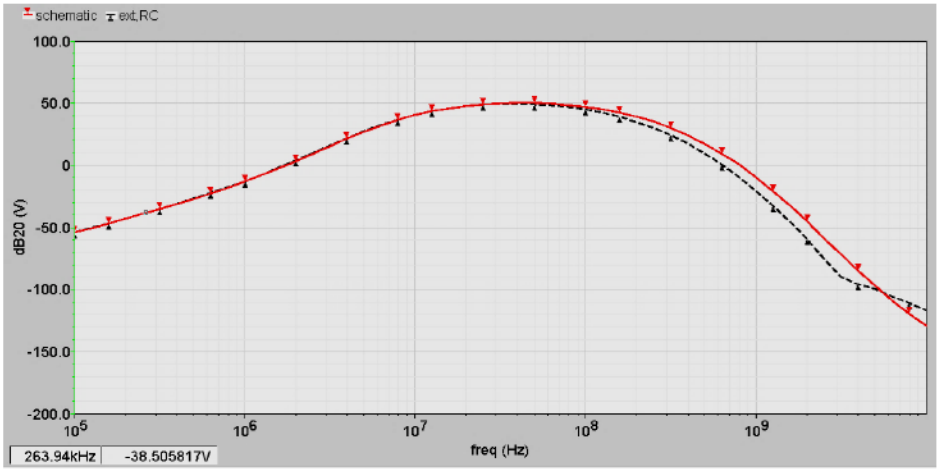


Fig. 3.12: Frequency response of the extracted 5-stage amplifier

The AC to DC conversion operation of the envelope-detector circuit presented in Fig. 2.7 of Chapter2 has been shown in Fig. 3.13. The magnitude of the envelope-detected signal, can be found according to the expression for the conversion gain in (2.40) for a given input AC signal amplitude. According to the simulation results, a 20 mV signal at the input of the envelope detector will lead to a baseband signal of about 666 µV at the output of the detector for n = 1.5. The differential envelope detector circuit dissipates about 1 µW from the 0.5 V supply.

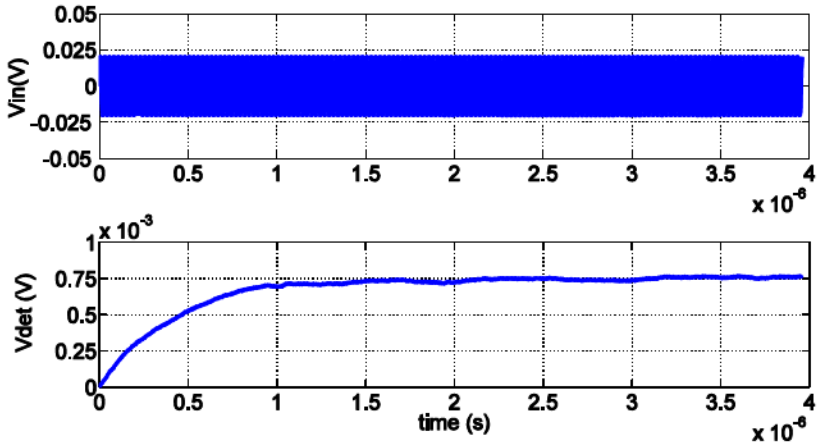


Fig. 3.13: Input and output signals of the designed envelope detector

3.4 Sensitivity Calculation and Comparison

Having found all the noise density values from the simulation, the overall noise factor and the input referred noise power can be calculated as described earlier. It is worth mentioning that the amplifier's low frequency noise as well as the flicker noise are also found from the circuit simulation by initially integrating the noise over the entire band and then normalizing the overall noise to the detector bandwidth. This gives an equivalent noise density for the flicker and low frequency noise that has been added in the noise factor calculation of out circuit simulation.

Now, by plotting the input referred noise power $P_{n,in}$ and ($P_{n,in}$-$SNR_{\min}$) versus the input power P_{in} and finding the intersection, the minimum inpout power or the sensitivity can be found.

In Fig. 3.14, plots of input-referred noise and input power derived from simulations are used to calculate the minimum detectable signal for SNR_{min}. It can be seen that the sensitivity is around -70 dBm, which satisfies the requirement. The total power consumption is found to be 28 μW based on simulation.

The layout of the WuRx in TSMC 90nm CMOS has been also shown in Fig. 3.15. In spite of achieving successful results in the post-layout simulation prior to the fabrication, unfortunately the implemented WuRx didn't work as expected.

Although too much effort was put in order to debug the implemented chip, we postulated the following to be the main reasons for the chip's failure: Difficulty in matching the input resistance of the S&H circuit to the source resistance due to different total resistance values seen from the input of the receiver during the ON and OFF states of the switch in the S&H circuit, absence of an on-chip analog to digital converter as well as a detection circuitry which suggested us to build all these component off-chip that resulted in more added parasitics than expected and total failure of the whole chip. Therefore, instead of continue trying to debug the

first unsuccessful chip, we decided to start a new design for an enhanced version of this wake-up receiver and try to avoid these issues from the beginning of the design.

Table 3.1 compares this work to the recently published wake-up receivers. In spite of a moderate sensitivity, our design shows lower power consumption.

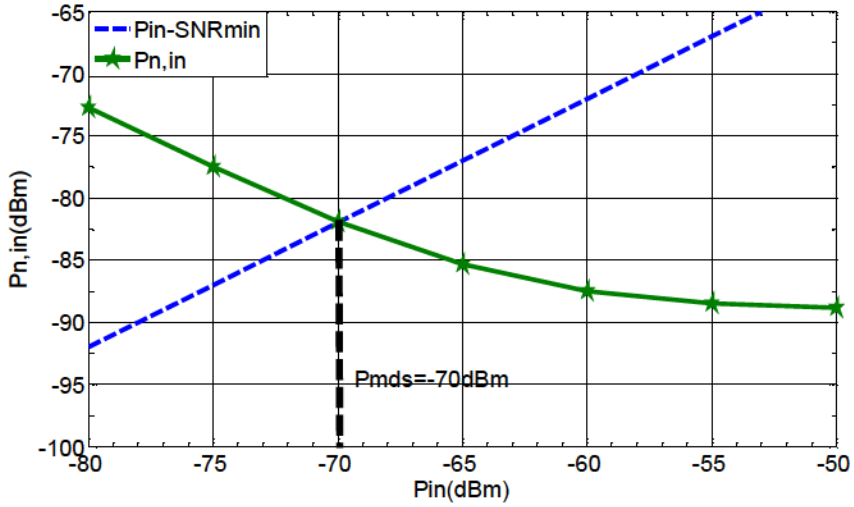


Fig. 3.14: Calculated sensitivity based on extracted simulation results

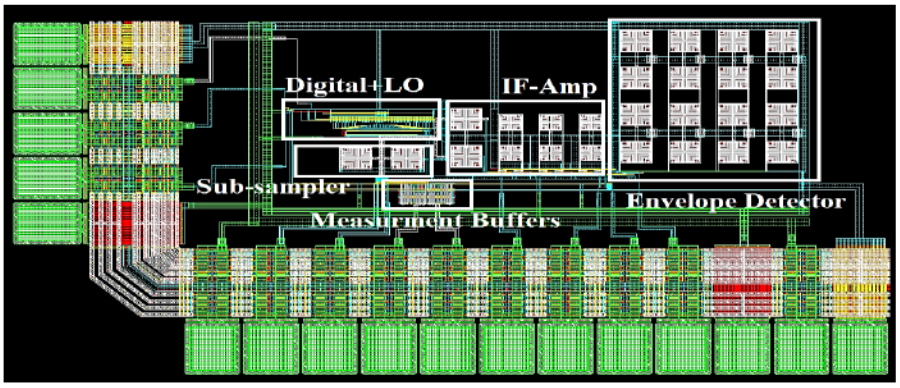


Fig. 3.15: Layout view of the complete WuRx in TSMC90nm technology

Table 3.1: Comparison of recently published wake-up receivers

WuRx Designs	Power (µW)	Sensitivity (dBm)	Frequency (Hz)	Data rate (kbps)
[34]	51	-64	2.4 G	100
[34]	51	-75	915 M	100
[22]	52	-72	2.4 G	100
[10]	44	-70	402 M	200
This Work [20]	28	-70	915 M	100

3.5 Conclusion

As a conclusion for this chapter, two techniques of sub-sampling and uncertain-IF topology have been combined in order to design an ultra-low power WuRx in the 915-MHz ISM band. Comparing to other recently published wake-up receivers, this design showed a superior performance in terms of the total power consumption that is our design priority. Despite the sensitivity is in the moderate range, it is still better than the required target value of -66 dBm defined earlier in Table 1.1. Moreover, taking into account the power-sensitivity metric, our design achieves comparable or even better performance.

Chapter 4

Ultra-Low-Power Energy-Efficient Dual-Mode Wake-Up Receiver [56]

As mentioned in the first chapter, adoption of two different data rates for transmission of wake-up patterns was employed in [51] through the use of duty cycling during the Monitoring (MO) mode, when the receiver is searching for a true Start Frame Bit (SFB) in order to start data reception at higher rate in the Identifier (ID) mode. However, the power dissipation during the ID mode using this technique is still high due to the use of a power hungry amplifier at the front-end of the receiver.

Our previously designed ultra-low power wake-up receiver presented in Chapter 3 employed the subsampling architecture for down-converting the incoming signal from RF to the mid-band frequency. However, the sensitivity was still limited by the large noise bandwidth of the IF-amplifier, which was allocated to overcome the VCO frequency variation resulting from the uncertain-IF topology. A complete period-based VCO calibration circuit based on frequency comparison technique will be proposed and used in the new design so that LO frequency variation is minimized. This enables a reduction in the IF-amplifier bandwidth, which improves the sensitivity of the receiver. The wideband amplifier with resistive network will be also replaced by a multistage amplifier with active inductors to reduce the bandwidth to less than 15 MHz for further improvement of the sensitivity. The operating frequency of the IF amplifier is also centered at around 37 MHz, which results in lower overall power dissipation compared to the previous center frequency of 85 MHz.

In addition to the above improvements in the previous design, a new approach for minimizing the power consumption during the MO mode will be proposed in this chapter, which optimizes the energy efficiency in both modes. This approach is based on employing different detection bandwidths in the two modes of operation. Having received the preamble bits at a low data rate (i.e. 10 kbps), the ID-bits will be received at a higher rate (i.e. 200 kbps), which helps to minimize the latency in waking up the main receiver whose ID-bits are being received.

This chapter begins with a brief overview on the proposed dual-mode wake-up receiver architecture and follows by the implementation of such receiver with a detailed discussion of each building block. The simulation and measurement results of the implemented receiver in IBM 130nm technology will be presented at the end of this chapter.

4.1 Proposed Dual-Mode WuRx Architecture

The block diagram of a generic TRF receiver and a subsampling-based receiver are shown in Fig. 4.1.a and Fig. 4.1.b, respectively.

Assuming the baseband circuits in Fig. 5.1.a are noiseless, the minimum detectable input power or the sensitivity of a TRF receiver has been already given in Chapter 2 as below:

$$P_{MDS} = 4SNR_{\min} BW_{BB} F_{FE} N_i + 2F_{FE} N_i \sqrt{4BW_{BB}^2 SNR_{\min}^2 + BW_{RF} BW_{BB} SNR_{\min}} \quad (4.1)$$

where F_{FE} is the total front-end noise factor before the envelope detector, N_i is thermal noise floor at the input of the receiver, BW_{RF} is the bandwidth of the front-end amplifier, BW_{BB} is the detection bandwidth of the baseband signal and is determined by the envelope detector's output load, and $SNR_{\min}$ is the desired signal

to noise ratio at the output of the receiver, which should be better than 12 dB in order to demodulate an OOK (on/off keying) modulated signal with a bit error rate better than 10^{-3}.

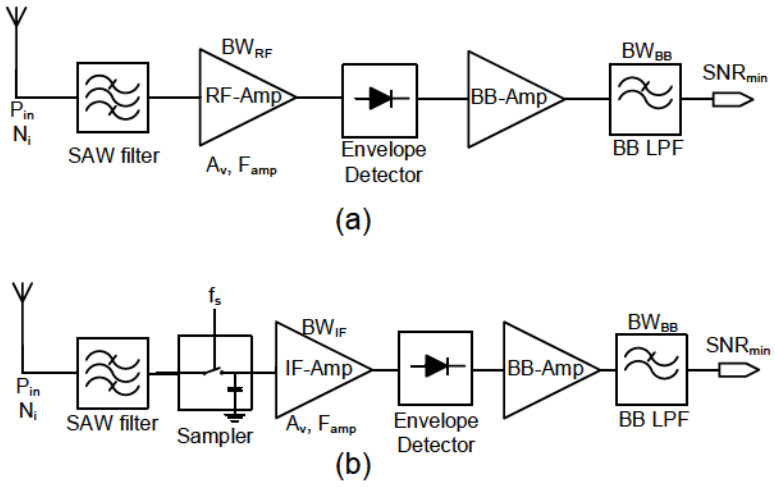


Fig. 4.1: Block diagram of a (a) generic TRF and (b) subsampling-based receivers

It was also observed that for large BW_{RF} with respect to BW_{BB} ($BW_{RF} >> BW_{BB}$) equation (4.1) can be reduced to:

$$P_{MDS} = 2N_i F_{FE} \sqrt{BW_{RF} BW_{BB} SNR_{\min}} \tag{4.2}$$

Also, recall from Chapter 3 that the noise factor of a subsampler can be estimated by the following equation:

$$F_{sampler} = (1 + 3.3/x^2) + 1/(2R_s C_s f_s) \tag{4.3}$$

where $x=Q/n$ represents the ratio of the quality factor of the front-end SAW filter Q to the sampling ratio of the subsampler n, R_s is the source resistance, which is 50 Ω, C_s is the sampling capacitor, and f_s is the sampling frequency.

Therefore, equation (4.2) can be used for estimating the sensitivity of a subsampling-based receiver in Fig. 4.1.b by replacing the RF bandwidth of the front-end amplifier, BW_{RF} with the IF-bandwidth of the IF amplifier, BW_{IF} and by writing the total front-end noise factor F_{FE} in terms of a series combination of the sampler and the IF-amplifier as below:

$$F_{FE} = F_{sampler} + (F_{amp} - 1) / G_{sampler} \tag{4.4}$$

The sensitivity in the first subsampling-based receiver presented in Chapter 3 was limited by the wide bandwidth of the IF-amplifier. Moreover, it always draws the same current from the supply even when searching for a SFB sequence during the MO mode. Considering the very low duty cycle of a typical wireless sensor node, this is not an energy efficient approach.

The proposed receiver is shown in Fig. 4.2. The new design improves the energy-sensitivity of the subsampling-based wake-up receiver by minimizing the bandwidth of the IF-amplifier and by adopting two modes of operation that allow the receiver to lower its power dissipation during the MO mode. Lowering the power is at the cost of reduced amplifier gain and hence a higher noise factor contribution. Thus, by intentionally lowering the data rate as well as the detection bandwidth in the MO mode, the sensitivity is almost the same in the two modes of operation.

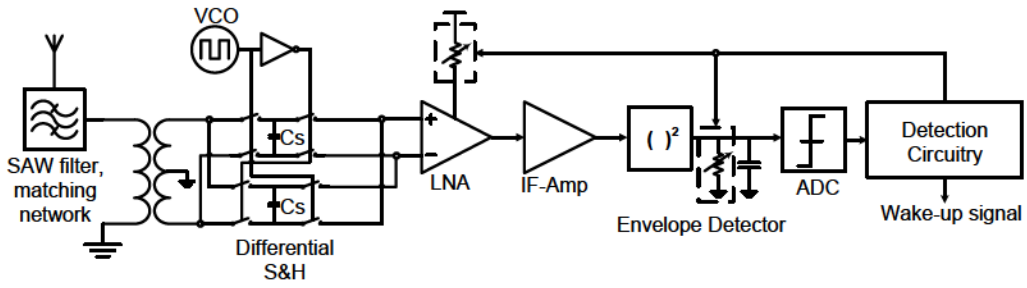


Fig. 4.2: Block diagram of the proposed dual-mode wake-up receiver

In order to ensure that the receiver will enter the ID mode after having received the SFB, the receiver was designed to have slightly better sensitivity in the first mode such that:

$$P_{MDS}(MO) \leq P_{MDS}(ID) \tag{4.5}$$

This can be done in two ways; lowering the detection bandwidth down to as low as 10 kHz, which limits the data rate to a maximum of 10 kbps and secondly by allocating slightly more power budget than predicted by the equations (i.e. overdesigning the MO mode).

4.2 Differential Sample and Hold Circuit

In Chapter 3, the subsampling technique was employed as a means to down-sample the incoming RF signal to IF through a sample (or track) and-hold process. Although the noise contribution from the sample and hold circuit could be significant, it was shown earlier that this contribution will still be a small portion of the combined sample and hold+amplifier's noise factor.

It was discussed earlier that in order to ensure aliasing of the RF signal bandwidth as well as to avoid overlap of the aliased bands after subsampling, the sampling frequency f_s must satisfy (3.2). However, two other factors have been considered

here for choosing the right f_s for this design; the noise contribution of the sampler, and the ratio of the power dissipation of the VCO to the total power dissipation of the receiver.

Based on above, the sampling frequency of this subsampler has been chosen to be 136 MHz. A higher subsampling frequency such as 200 MHz would lower the noise factor of the subsampler by 32% but increases the power dissipation of the VCO by approximately 50%. On the other hand, choosing a lower sampling frequency such as 100 MHz reduces the power dissipation by 26% and increases the noise factor of the subsampler by 34%.

The schematic view of the updated sample and hold circuit is shown in Fig. 4.3. To ensure sufficient track and hold speed that is dictated by the analog input bandwidth, the ON resistance R_{on} of the NMOS switch as well as the value of the sampling capacitor C_s must be minimized. However, in order to improve the accuracy that can be estimated by the sampling pedestal error [44] as well as to reduce the thermal noise estimated by (4.3), it can be shown that the value of C_s has to be increased.

The NMOS switches (M1, M2, M3, and M4) are sized large enough (i.e. 20 µm/0.2 µm) to satisfy the speed requirement. The complementary NMOS switches (M5, M6, M7, and M8) with a size of 5 µm/0.2 µm have been added to the modified differential sample and hold circuit. These complementary switches will aid to improve the accuracy by reducing the sampling pedestal error. Furthermore, they would facilitate the input matching by maintaining a constant impedance between the RF and IF sections during both sample and hold periods.

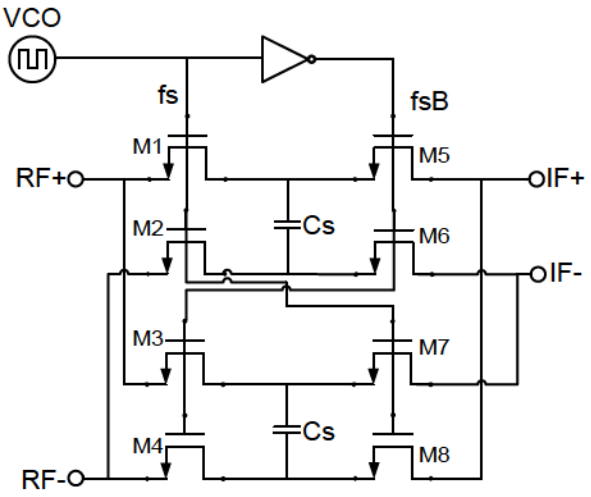


Fig. 4.3: Differential sample and hold circuit with complementary switches

Assuming a high-Q anti-aliasing filter prior to the subsampler, the first term in (4.3) that is due to the noise folding will approach to 1. However, the second term, which is due to the intrinsic noise of the sampler will be dependent on f_s and C_s. Considering the speed-accuracy-thermal noise trade-off, the value of C_s has been chosen to be 1.5 pF for this design. Therefore, for the sampling frequency of 136 MHz, this will lead to a $F_{sampler}$ of around 50.

It is worth mentioning that the sampling ratio n is not a function of C_s. In other words, once the sampling frequency f_s the been chosen, the sampling ratio n, and the corresponding first down-sampled IF signal fIF will be determined according to the sub-sampling theory. In our design, the combination of the 915 MHz RF signal and the sampling frequency of 136 MHz will lead to n=7 and f_{IF} = 37 MHz:

$$f_{IF} = min\{|f_{RF}\text{-}nf_s|\} = 915\text{-}7\times136 = 37 \text{ MHz} \quad (4.6)$$

The simulation results for the differential sample and hold circuit MHz is shown in Fig. 4.4. For this simulation, an RF signal with a voltage amplitude of 100 μV at

915 MHz has been applied to the input of the subsampler and the subsampled signal using a sampling frequency f_s of 136 MHz. According to the simulated frequency response of the subsampled signal, it can be seen that the first harmonic is located at 37 MHz, while the rest of the harmonics are further away in the frequency. The desired subsampled harmonic shows a voltage gain of about 0.85 V/V which is slightly smaller than the gain of 1 for an ideal subsampler. Following to this observation, the actual power gain of the subsampler can be found to be around 0.72 W/W, which has been taken into account in all our further analysis.

One interesting feature of the redesigned differential sample and hold circuit is that it completely filters out all the subsampled harmonics that are caused by even sampling ratio values. Looking closely at the frequency response of the subsampled signal, the available harmonics including the first desirable at 37 MHz are located at the following frequencies:

$$f_{IF} = |f_{RF} - nf_s| = \left\{ \begin{array}{c} |915-1\times136|=779\ \text{MHz} \\ |915-3\times136|=507\ \text{MHz} \\ |915-5\times136|=235\ \text{MHz} \\ \mathbf{|915-7\times136|=37\ MHz} \\ |915-9\times136|=309\ \text{MHz} \\ |915-11\times136|=581\ \text{MHz} \\ |915-13\times136|=853\ \text{MHz} \end{array} \right\} \quad (4.7)$$

It can be shown that as a result of this advantage, the requirement for the anti-aliasing filter prior to the sample-and-hold operation can be relaxed to some extent.

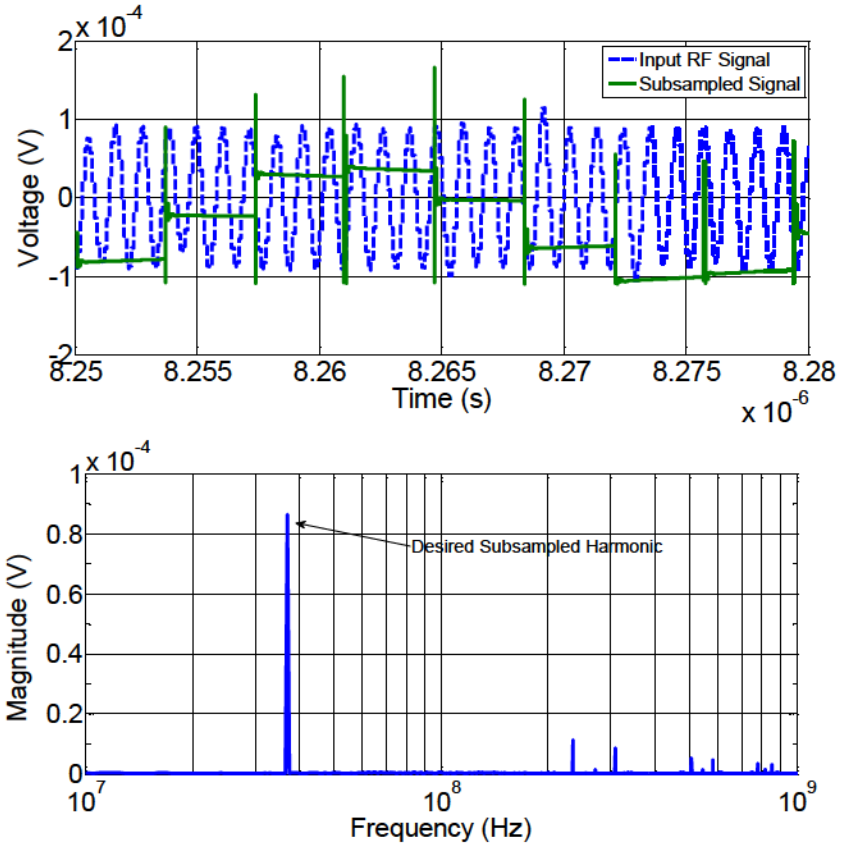


Fig. 4.4: Simulation results for the subsampled signal and its frequency response

4.3 Multistage Active Inductor-Based Amplifier

According to our discussion in previous chapters, the overall noise performance as well as the power dissipation of the receiver can be largely dominated by the noise performance of the front-end amplifier stage. Therefore, the goal is to design an IF-amplifier with a narrow bandwidth, which not only achieves a large overall gain and low noise contribution, but also dissipates as low a current as possible from the supply.

Fig. 4.5 shows the simplified model of the front-end amplifier, which is connected to the output of the differential subsampler circuit. Since the output of

the subsampler is differential, the first stage is a differential amplifier with resistive loads, which is followed by a differential to single-ended converter stage.

The last two identical stages of the front-end amplifier employ an active inductor structure [62] in order to save area compared to large passive inductors with the same quality factor. The active inductor employed here is comprised of M11, M13, and M14 at the load of a cascode common-source amplifier stage made up of M10 and M12.

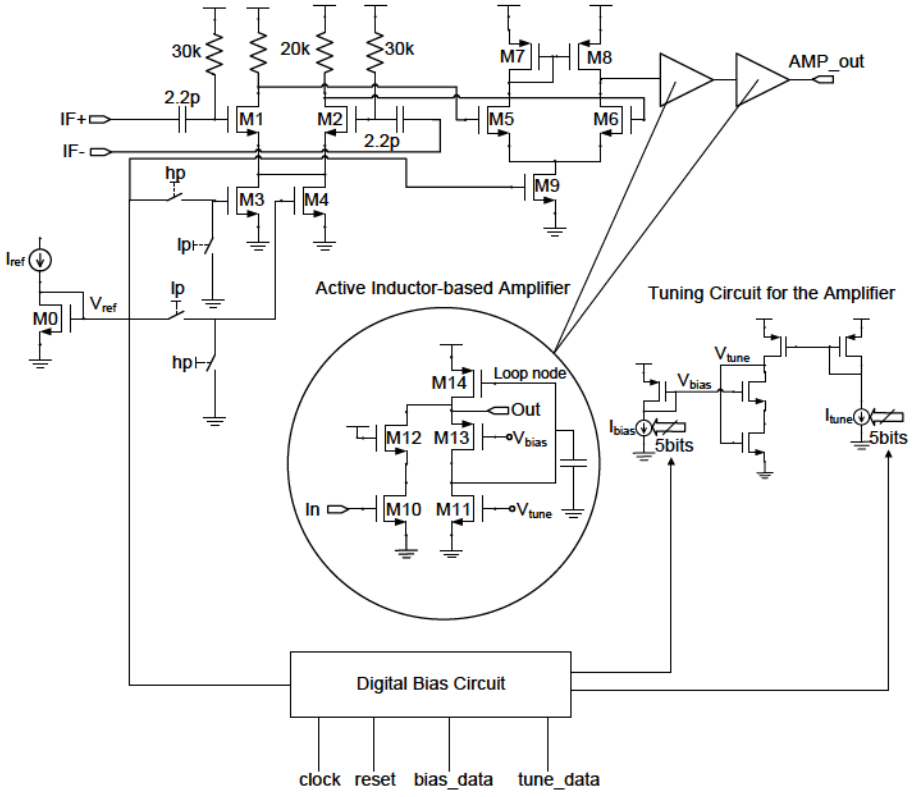


Fig. 4.5: Schematic of the multistage front-end amplifier

Most of the current in M14 flows through the cascode amplifier while a fraction of it is drawn by M11 and M13. At low frequencies, the impedance seen from the source of M13 is low due to the loop gain that is provided by M14 and M13. However, as the frequency increases, the loop gain reduces due to the total

capacitance at the loop node. This will cause the output impedance to increase. At higher frequencies, the impedance is lowered as it gets dominated by the capacitance at the output node.

The two active-inductor based amplifier stages provide about 13 MHz bandwidth while each dissipating around 2 μW from the supply. The center frequency as well as the bandwidth of the amplifier can also be tuned using the tuning circuit for the amplifier. The *bias* and *tune* currents of the tuning circuit as well as the biasing and tuning voltage V_{bias} and V_{tune} are adjusted using two DAC blocks (not shown) and 5 control bits. The *bias* and *data* bits are serially received at the rising edges of the clock in the digital biasing circuit.

The first stage of the front-end amplifier has the largest noise contribution. Changing the current consumption of the first amplifier stage can vary its noise contribution. Therefore, by controlling the amount of the current drawn from the supply in the first amplifier stage, one will be able to change the noise factor of the receiver. Thus, complementary digitally-controlled signals *lp* and *hp* are employed in this design in order to allow the receiver to operate in the MO and ID modes, respectively.

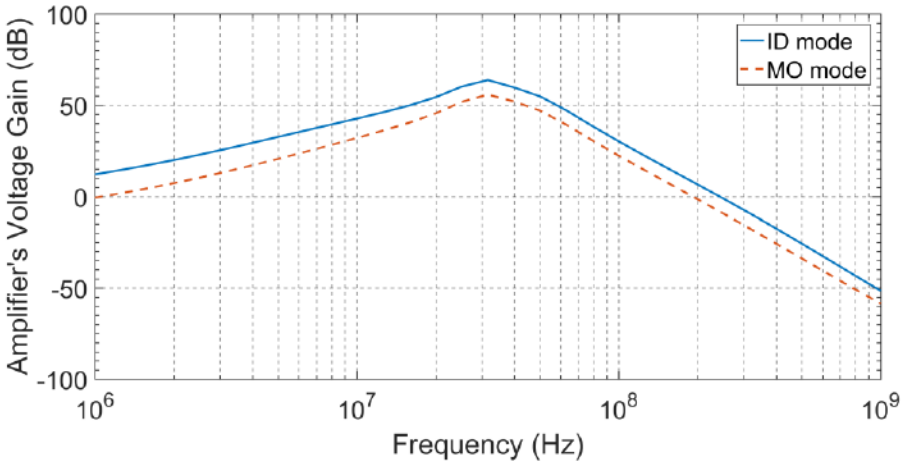


Fig. 4.6: Frequency response of the multistage front-end amplifier

The total front-end amplifier dissipates about 15.6 µA and 26 µA from a 500 mV supply. According to the extracted simulation results shown in Fig. 4.6, the multistage amplifier provides an overall voltage gain of 51 dB and 57.5 dB at the center frequency of about 37 MHz during MO and ID modes, respectively. The bandwidth is found to be about 13 MHz in both modes. Finally, the total noise figure of the combined sample and hold and amplifier according to post-extraction simulation results is about 28 and 23 dB during the MO and ID modes, respectively.

Table 4.1: DC simulation results for the multistage front-end amplifier

	W/L (µm/µm)	**g_m (µA/V)**	**I_{ds} (µA)**
M1,2	12/0.4	211.1 (ID)	7.64 (ID)
		78.69 (MO)	2.6 (MO)
M3	9/1	274.2 (ID)	15.15 (ID)
		11.56 (MO)	0.44 (MO)
M4	3/1	3.443 (ID)	0.131 (ID)
		86.71 (MO)	4.767 (MO)
M5,6	12/0.4	66.71	2.184
M7,8	30/0.4	52.16	2.184
M9	3/1	79.02	4.368
M10	16/0.12	44.35	1.803
M11	1.5/0.12	3.76	0.153
M12	8/0.12	44.07	1.803
M13	6/0.12	3.704	0.153
M14	6/1	33.91	1.956

Table 4.1 shows the sizing of all the transistors in the front-end amplifier as well as the DC operating points. According to simulation results, the current dissipation in the first stage of the amplifier is 15.3 µA and 5.2 µA during the ID and MO modes, respectively.

4.4 Period-based Calibrated VCO

The sensitivity of the ultra-low power wake-up receiver presented in Chapter 3 was limited by the large bandwidth of the IF-amplifier, that had been allocated to overcome the VCO frequency variation according to the employed uncertain-IF receiver architecture. In order to reduce the bandwidth of the IF-amplifier and hence to improve the overall sensitivity of the receiver, a VCO calibration circuit can be employed to minimize the variations in the LO frequency.

Three types of VCO calibration techniques can be found in the literature: closed-loop [63], open-loop [64], and period-based or time-to-voltage conversion (TVC) techniques [65], [66]. In the closed-loop configuration, the VCO is inside the PLL and it calibrates once the PLL is settled. Thus, the calibration speed is limited by the long settling time. On the other hand, continuous loop operation of the PLL burns a lot power.

In the second configuration, a counter with sufficient amount of counts is required to achieve a desired frequency precision, whereas the analog TVC requires a few cycles of oscillation for the same precision. Thus, the most energy- efficient calibration scheme is the period-based configuration. However, the precision can be affected by various analog impairments such as the mismatch between the current sources of the TVC circuits, the peak-detectors, and the TVC load capacitances as well as the offset voltage of the comparator. Some of these issues can be solved by using larger size transistors in order to reduce the mismatch effects or by careful layout in order to eliminate the gradient effects.

In the case of a single TVC, where the other input of the comparator is connected to the external reference voltage V_{ref} , the absolute accuracy of the TVC only can be achieved if a PVT invariant current source has been employed [66]. However, in order to obtain the absolute accuracy for the case of a TVC pair, the two TVCs must be exactly identical [65].

Prior to describing the complete design of the VCO calibration circuit, a novel period-based VCO frequency comparison circuit will be presented here that obviates the need for having two TVC circuits as well as the external reference voltage source.

4.4.1 Frequency Accuracy Estimation

Assuming a reference frequency f_{ref} is applied to a general analog TVC as shown in Fig. 4.7, the TVC is supposed to convert the period of the input signal T_{ref} (considering only a single period) to the corresponding voltage V_{ref}. One can quickly infer from the above statement that higher frequency would be translated to lower V_{ref}. Also, any change in the input frequency Δf or period ΔT will lead to a change in the output voltage ΔV such that:

$$\frac{\Delta T}{T_{ref}} = \frac{\Delta V}{V_{ref}} \tag{4.8}$$

If two TVCs are used to compare two signals through the use of a comparator, according to (4.8), the voltage difference at the comparator ΔV will depend on the reference voltage V_{ref} as well as on the desired frequency accuracy. In other words, for a given reference voltage of 500mV, and assuming 1% for the precision of the frequency, the errors contributed from the target calibration circuit should not be greater than 5 mV.

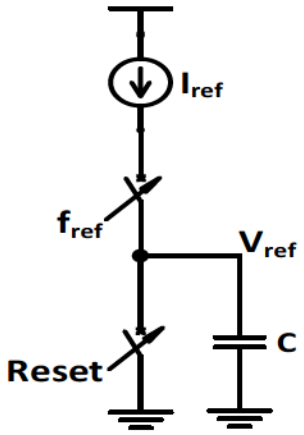


Fig. 4.7: Simplified view of a general TVC circuit

From another point of view, the final calibrated accuracy of any period-based calibration circuit can be estimated as [64]:

$$\left(\frac{\sigma_f}{f_{ref}}\right)^2 \approx \left(\frac{\sigma_C}{C}\right)^2 + \left(\frac{\sigma_I}{I_{ref}}\right)^2 + \max\left\{\left(\frac{\sigma_{CP,off}}{V_{ref}}\right)^2, \left(\frac{V_{LSB}K_{VCO}}{f_{ref}}\right)^2\right\} \tag{4.9}$$

where σ_f , σ_C , σ_I and $\sigma_{CP,off}$ are the standard deviations of the reference frequency f_{ref} , the TVC's output capacitor C , the charge pump current I_{ref} , and the comparator's offset voltage $V_{CP,off}$ respectively. Also, V_{LSB} represents the finite resolution of a Digital to Analog Converter (DAC) that is normally used in a complete calibration circuit to tune the oscillator and K_{VCO} is the VCO gain.

Assuming a DAC with sufficient resolution to be employed in the complete calibration circuit, designing a TVC with minimized variations of C , I_{ref} and $V_{CP,off}$ will improve the calibration accuracy. In other words, the calibration precision is limited by σ_C , σ_I and $\sigma_{CP,off}$.

4.4.2 Proposed Frequency Comparison Circuit

According to the above discussion, the overall calibration precision can be estimated from the frequency comparison circuit, since most of the errors occur at this stage. Fig. 4.8 depicts the schematic of the proposed frequency comparison method. Unlike any other period-based frequency comparison circuit, our proposed technique employs a single TVC circuit to charge both output capacitors up to their corresponding voltages depending on the incoming frequency. In practice, a single reference current that is generated by an NMOS transistor in the saturation region is being steered by two NMOS switches depending on which frequency is applied to the circuit. This in fact eliminates the effect of the variation of the reference current σ_I due to the mismatch on the comparator output. Here we are going to explain the role of each part in the circuit.

4.4.2.1 Principle of Operation

Before performing any comparison between the two frequencies, we have to make sure that the duty cycle of the signals is exactly 50%. Therefore, two frequency dividers as shown in Fig. 4.8 are used to initially divide the frequency of VCO as well as the reference signal by two.

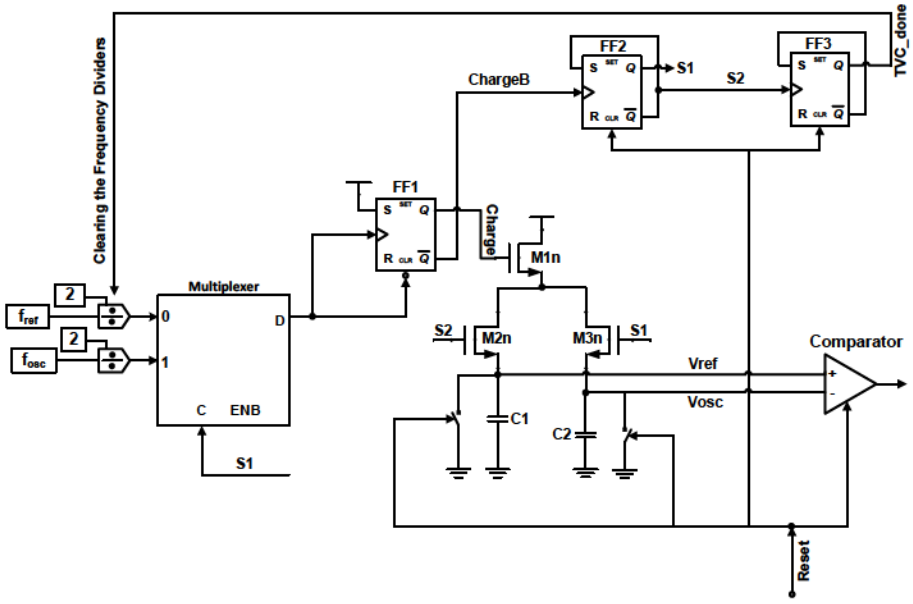


Fig. 4.8: Simplified view of the proposed frequency comparison method

An external *Reset* signal as shown in Fig. 4.8 is used to disable the frequency comparison circuit in order to save power as well as to prepare the circuit for a new comparison cycle. Once the *Reset* signal is disabled, since the *Q* output of *FF2* is already *zero*, the $f_{ref}/2$ input will be selected by the MUX and hence the reference frequency feeds the clock input of the edge detector flip-flop *FF1*. As the rising edge of the input signal is detected, the *Charge* signal becomes *one*. As a result, the TVC circuit starts charging C_1 using M_{1n} and M_{2n} up to V_{ref}. At the falling edge of the input frequency, the *CLEAR* and *CLOCK* inputs of *FF1* both become *zero*, leading to *ChargeB* signal becoming *one*. As a consequence, the *Q* output of *FF2* toggles from *zero* to *one* and hence the other input signal i.e. $f_{osc}/2$ would undergo the same path but this time in order to charge C_2 up to the corresponding voltage V_{osc} via M_{1n} and M_{3n} transistors. After the falling edge of the second input signal, the comparison is ready to be done and hence no more time-to-voltage conversion is required. This is when the *TVC_done* signal generated by *FF3* clears the frequency dividers as shown in Fig. 4.9.

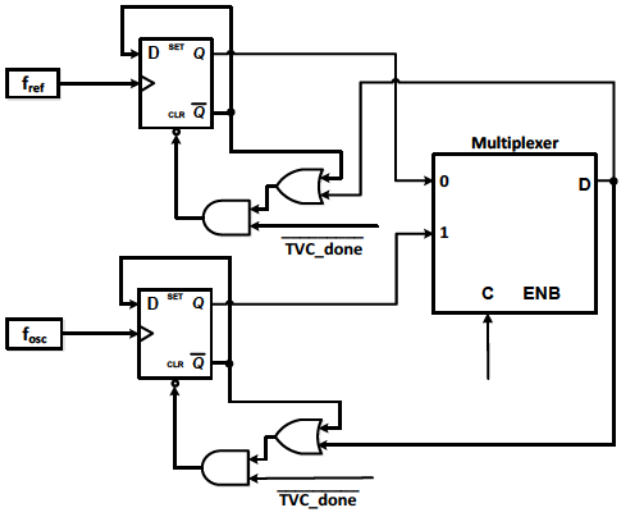


Fig. 4.9: The input frequency dividers along with the control gates

Now, assume the following scenario: If $f_{osc}/2$ is already at the high-state and suddenly it is selected by the MUX, *FF1* will experience a change from 0 to 1 on its *CLOCK* input, which causes M_{1n} to start charging the output capacitor C_2 through M_{3n} from somewhere around the middle of the input cycle. Therefore, the capacitor voltage V_{osc} will not correspond to the complete input cycle. To avoid this problem, the control gates as shown in Fig. 4.9 have been added to the circuit. Therefore, if the above scenario occurs, since the MUX output going to the OR gate as well as the $\overline{Q}$ of the ($f_{osc}/2$ generator) flip-flop are both 0, the $f_{osc}/2$ signal will become 0 and there will be no change to the *CLOCK* input of *FF1* until the next clock cycle of f_{osc}.

4.4.2.2 Design Considerations

All digital blocks are taken from the standard digital library of the TSMC90nm CMOS technology. The comparator used in the proposed design is realized as a dynamic comparator [63], [64] and is depicted in Fig. 4.10. The operation of the comparator is as follows: The same *Reset* signal explained earlier initially shorts

both outputs V_{on} and V_{op} of the comparator to the ground. Once the *Reset* and the *TVC_done* signals become 0 and 1 respectively, the two differential PMOS transistors start conducting current from the supply. Depending on the values of the input voltages V_{ref} and V_{osc}, one of outputs becomes 1 in less than 2 ns while the other remains 0. The load capacitances C_1 and C_2 (Metal-Insulator-Metal (MIM) type capacitors) as well as the sizes of M_{1n}, M_{2n}, and M_3 are chosen to provide the reference voltage of 500 mV at the comparator input. Also, M_{1n} has a larger length in order to reduce the channel length modulation effect.

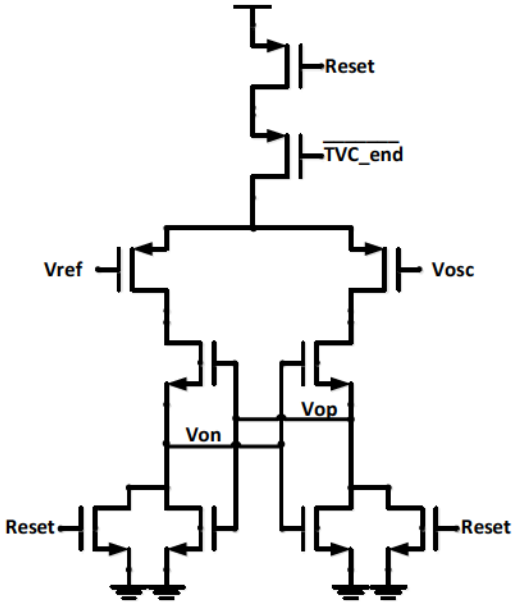


Fig. 4.10: The dynamic comparator with power-saving PMOS switches

4.4.2.3 Results and Discussion

The simulation results of the proposed period-based frequency comparison circuit will be shown here and the calibration accuracy will be estimated according to (4.1) and (4.2). As explained earlier, our comparison circuit is part of a complete calibration building block. In order to simplify the analysis, the simulation results

of a single calibration operation i.e. one frequency comparison of the proposed circuit will be shown and compared with the other designs. The results of a complete VCO calibration (coarse tuning) will be shown later.

According to the proposed architecture, the term σ_I / I_{ref} in (4.9) do not have any effect on the calibration accuracy as any variation in the reference current due to the mismatch will have equal effect on the voltages of both capacitors. According to Monte-Carlo simulation for process and mismatch variations with 1000 iterations, $\sigma_C \approx 0.31 fF$ was found for $C = 1\ pF$ and $\sigma_{CP,off} < 5mV$ was obtained for $V_{ref} = 500$ mV. Variations of the offset voltage in the dynamic comparator as a result of process and mismatch effect have been shown in Fig. 4.11.

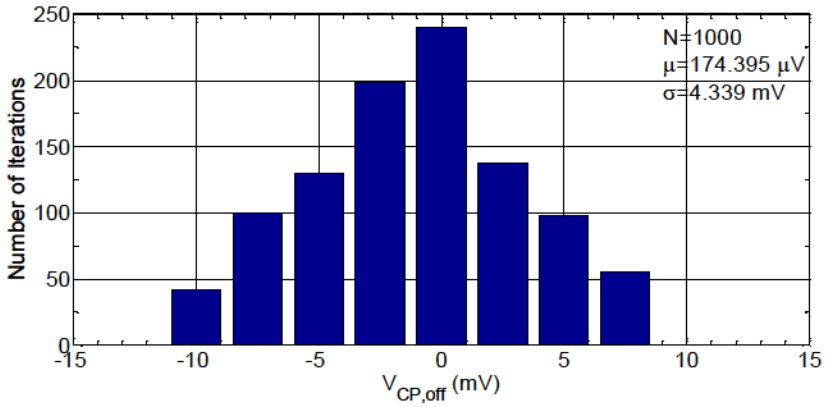


Fig. 4.11: Histogram for the input offset voltage of the dynamic comparator for process and mismatch variations with 1000 Monte-Carlo iterations

Based on the results of Fig. 4.11, the overall frequency accuracy can be estimated to be better than 1% according to (4.9). Based on this, it is required to show that our proposed circuit keeps the estimated ±1% calibration accuracy against mismatch and process variations. Fig. 4.12 depicts the simulation results of a single calibration when the oscillator frequency is running at 201.6MHz (i.e. 0.8% higher than f_{ref}). We observe a 4 mV voltage difference at the comparator inputs as a result

of the 0.8% frequency difference while V_{on} and V_{op} are correctly decided by the comparator to be 0 and 1, respectively.

It is expected that for a given frequency difference, the outputs of the comparator V_{on} and V_{op} are not flipped over due to mismatch and process variations. In order to validate the results, we run Monte-Carlo simulations with 1000 iterations against mismatch and process variation as shown in Fig. 4.13. It turned out that 995 out of 1000 samples resolve the 0.8% frequency difference. It is clear that once the oscillation and reference frequencies get closer to each other, the frequency comparison circuit would get more errors. For instance, with the same number of Monte-Carlo iterations the yield is found to be about 85% for 0.5% frequency difference. For each Monte-Carlo iteration, we have considered both cases of frequency difference between f_{ref} and f_{osc} (i.e. $f_{ref} > f_{osc}$ and $f_{ref} < f_{osc}$) and the estimated frequency accuracy includes both simulation results. It shows a 4 mV voltage difference at the comparator inputs as a result of the 0.8% frequency difference. This corresponds to a standard deviation of about 1.6 MHz for the reference frequency of 200 MHz.

Ultimately, in order to verify the sensitivity of our circuit against voltage and temperature variations, one may sweep V_{DD} as well as the temperature and see if the desired comparator output will be obtained for the given accuracy. According to the simulation results, the supply voltage can vary by 10% (from 0.95V to 1.05V) while the temperature can change from -50°C to 90°C in order to keep the frequency accuracy to better than ±0.8%.

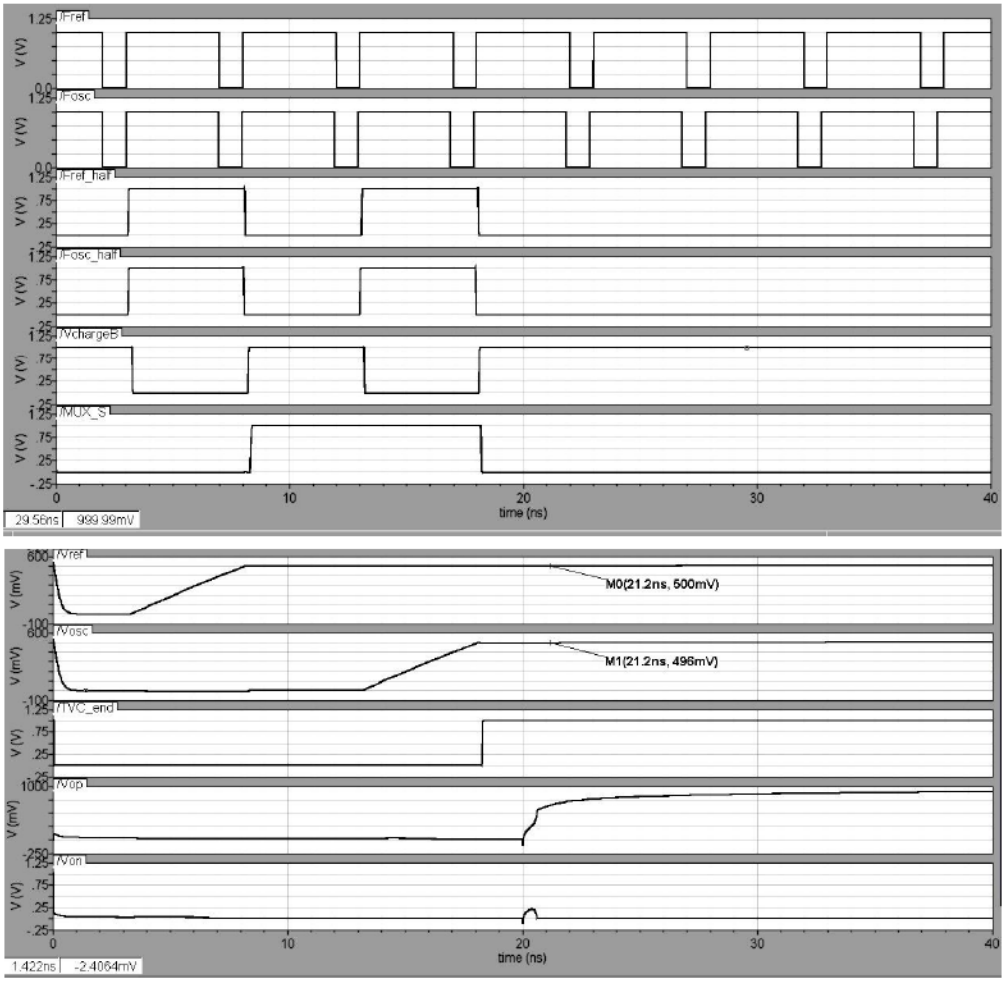


Fig. 4.12: Transient simulation results for the proposed frequency comparison circuit for f_{osc}=201.6MHz and f_{ref}=200MHz. From top to bottom: The reference and VCO signals along with their 50% duty-cycled signals, the *ChargeB* signal, the MUX selection signal, V_{ref} and V_{osc} voltages, the *TVC_end* signal, and finally V_{on} and V_{op} decision outputs.

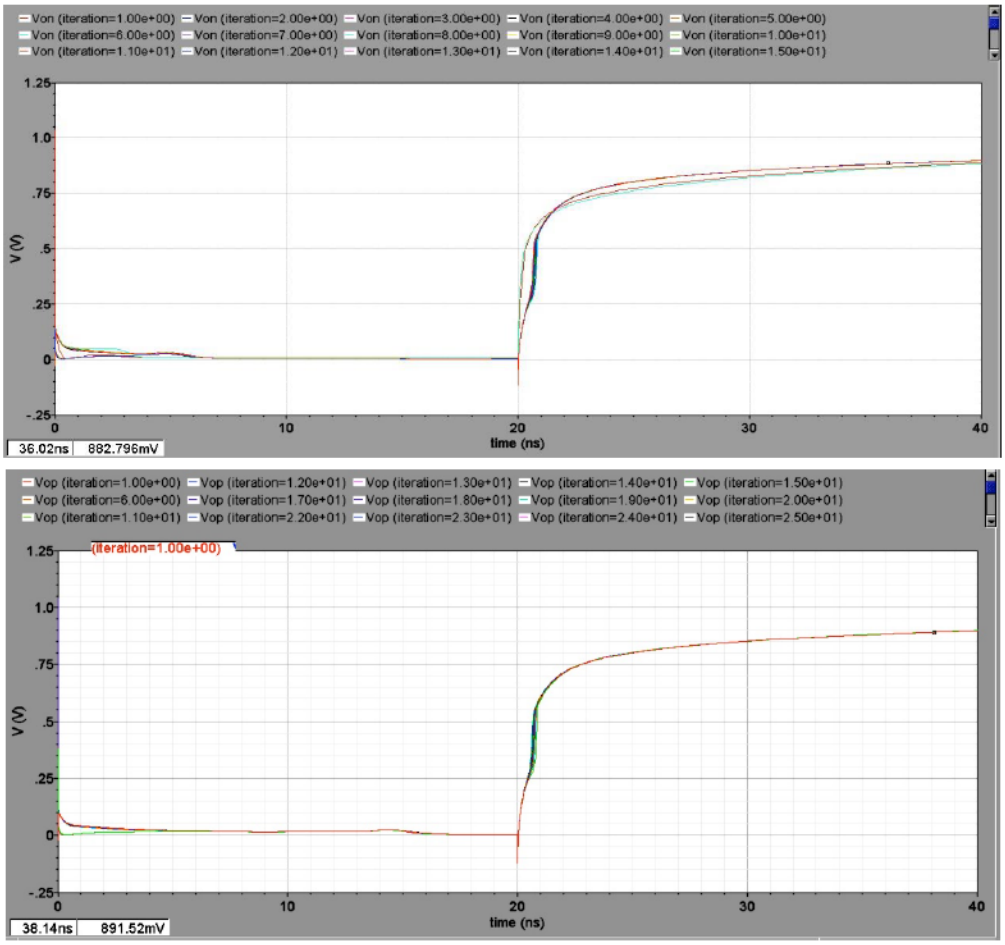


Fig. 4.13: Results of the Monte-Carlo simulation for V_{on} (upper figure) and V_{op} (lower figure) where f_{osc} is 0.8% lower and higher than f_{ref}, respectively. The simulations are with 100 iterations for mismatch and process variations

Table 4.2 summarizes the simulation results of the proposed frequency comparison circuit. Compared to other period-based calibration schemes, our circuit achieves a high-frequency accuracy of 0.8% within 4 reference cycles dissipating a power consumption of as low as 80μW. In practice, the calibration circuit will be duty-cycled, which leads to a much smaller average power consumption.

Table 4.2: Comparison of Different Frequency Calibration Circuits

	[65]	[64]	[63]	This work: [55]
Type of circuit	VCO frequency calibration	PVT compensated VCO	VCO frequency calibration	Frequency comparison
Technology	0.18µm CMOS	65nm CMOS	0.6µm CMOS	90nm CMOS
Cal. Type	Period-based	Period-based	Closed-loop	Period-based
Frequency	40MHz	0.8~2GHz	40MHz	200MHz
Accuracy	1%	2.24%	1%	0.8%
V_{DD} range	1.8V	0.85V~ 1.15V	3V	0.95V~ 1.05V
Temperature	-	-5°C~75°C	-	-50°C~90°C
Single cal. time (ref. cycles)	8	32	30	4
Power	3mW*	226µW**	7.5mW***	80µW

* Including a dual-edge phase detector, two charge pumps, etc.

** Including a DAC and a VCO in addition to the TVC circuit

*** Power of the frequency synthesizer including the VCO

Compared to other techniques and according to both simulation results as well as the equation-based estimation for the frequency accuracy, the proposed mismatch-robust period-based frequency comparison circuit achieves a frequency accuracy of 0.8% with a single calibration time of 4 reference cycles. This has been achieved through the use of a single TVC circuit in order to reduce the overall mismatch effect of the system. Therefore, our proposed circuit can be a better candidate for a TVC-based frequency calibration circuit. The complete calibration circuit based on the proposed method will be used in our enhanced wake-up receiver explained below.

4.4.3 Complete VCO Calibration Circuit

A three-stage ring-oscillator has been used for generating the sub-sampling frequency of 136 MHz as shown in Fig. 4.14. As discussed earlier, frequency calibration would be necessary in order to compensate for PVT variations. It is shown that the VCO circuit is placed inside a period-based frequency calibration loop, which is based on our mismatch-robust frequency comparison technique presented above. The inverters as well as the output buffers are sized such that they can drive the MOS switches in the sample and hold circuit.

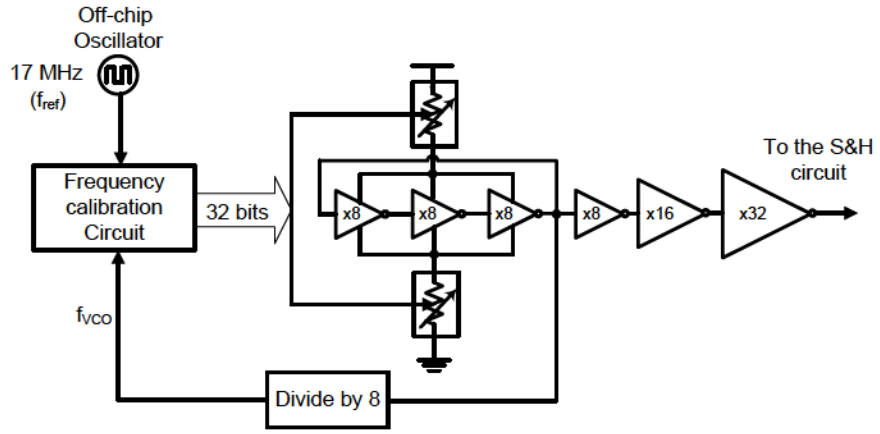


Fig. 4.14: Ring-oscillator inside the frequency calibration loop

The simplified block diagram of the overall frequency calibration system is depicted in Fig. 4.15, where the frequency comparison circuit and the VCO are part of the complete system. The frequency calibration circuit works as follows:

By applying the *start_calibration* signal, all blocks are reset. The frequency comparison circuit compares f_{VCO} and f_{ref}. If f_{VCO} is smaller than f_{ref}, V_{on} becomes 1 while V_{op} becomes 0. This will make the digital controlling circuitry generate a 1 for the up/down and *clk* inputs of the 5-bit counter. This ultimately will lead to a higher frequency at the output of the VCO by increasing the current flow through the resistive networks in the ring oscillator. The increase in the frequency continues

after each comparison cycle until V_{on} becomes 0 and V_{op} becomes 1. As soon as this occurs, the counter stops counting and V_{supply} gets shorted to ground thereby turning off the calibration circuit.

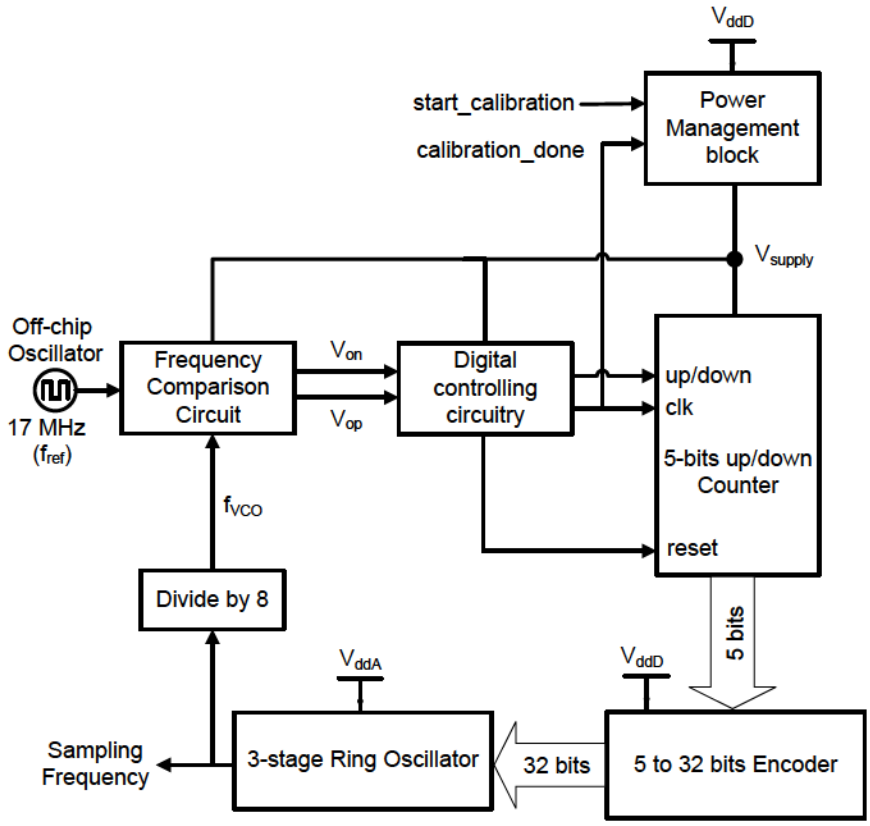


Fig. 4.15: Block diagram of the VCO calibration system

Note that for every calibration procedure, the counter resets to all 0 bits and then starts counting up from that point. As a result, the oscillation frequency will start increasing with a step size of about 4.5 MHz/LSB from the lowest possible value until it reaches the desired frequency.

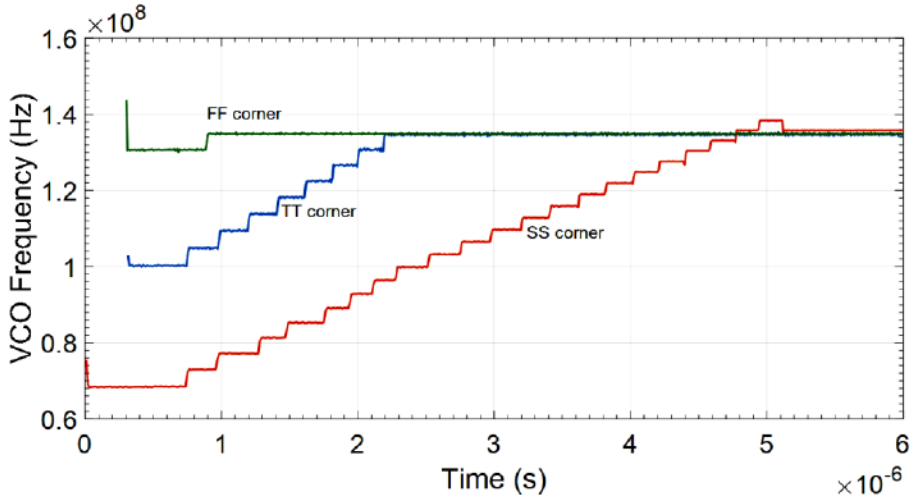


Fig. 4.16: Simulation results for the calibrated VCO at different corners

The simulation result of the calibrated VCO frequency for TT (Typical N/PMOS, Typical Temperature, and Typical Supply Voltage), SS (Slow N/PMOS, Low Temperature, and Low Supply Voltage), and FF (Fast N/PMOS, High Temperature, and High Supply Voltage) corners are depicted in Fig. 4.16. It is observed that the desired oscillation frequency of 136 MHz is achievable for these corners. For the TT corner, the capturing range of the digitally controlled ring-oscillator is from 100 MHz to 244 MHz for the 32 steps.

The average power dissipation of the ring-oscillator according to the simulation results is about 5 µW from the analog supply voltage of 500 mV. The overall power dissipation of the VCO calibration circuit (ignoring the ring-oscillator) when active is about 10 µW from a 1 V digital supply voltage. The calibration will be performed at least once at power-on of the VCO.

For this design, a 1 degree of temperature change from 27 to 28 will lead the oscillation frequency to increase by 800 kHz from its desired frequency of 136 MHz (i.e. 800 kHz/˚C), or a 1% change in the supply voltage corresponds to about 1.16% variation in the frequency of oscillation (i.e. 300 kHz/mV).

The 13-MHz IF bandwidth of the multistage amplifier corresponds to approximately 9.5% of the 136 MHz. However, taking into account the sampling ratio of 7, this would allow the sampling frequency to deviate by only 1.35%. Therefore, an external reference frequency that guaranties around 0.67% accuracy over process and temperature variation would be sufficient. This requirement is still around 100 times less stringent compared to the performance of a typical quartz crystal. As an example, a typical quartz crystal oscillator from TXC Corporation [67] that dissipates around 20 µW from a 1 V supply voltage at 16.934 MHz has a frequency accuracy of ±10ppm, which is much better than required for generating the reference frequency.

Calibration of the VCO during typical operation can be done with a low duty cycle. However, as a worst case scenario suppose that during a large and sudden temperature fluctuation the chip's VCO needs to be calibrated every 100 ms. Therefore, if we operate the whole calibration circuit including the off-chip crystal that consume a total of 10 µW +20 µW =30 µW every T_{int} =100 ms, it will lead to an average power of (T_{on} / T_{int})×30 µW=0.3 µW assuming every calibration takes about T_{on} =1 ms. This ON time includes the start-up time of the crystal. It is also worth mentioning that some WSN applications such as implanted or skin mounted devices are fairly temperature controlled. However, for environments where temperature does change significantly, VCO alternatives that show lower sensitivity to temperature should be considered [68] allowing for longer intervals between success calibration cycles.

4.5 Envelope Detector

The envelope detector used in this work has the simple NMOS-based detector structure shown in Fig. 4.17. In this circuit, M1 operates as a voltage-dependent current source and M2 is the rectifying component that operates in the subthreshold

region with its gate connected to the bulk using the triple-well process to achieve an efficient non-linear conversion gain.

The output bandwidth can be varied for the two modes of operation by changing the gate voltage of M1. Increasing the bias voltage will result in larger current draw from the 500 mV analog supply and hence larger g_m for M2.

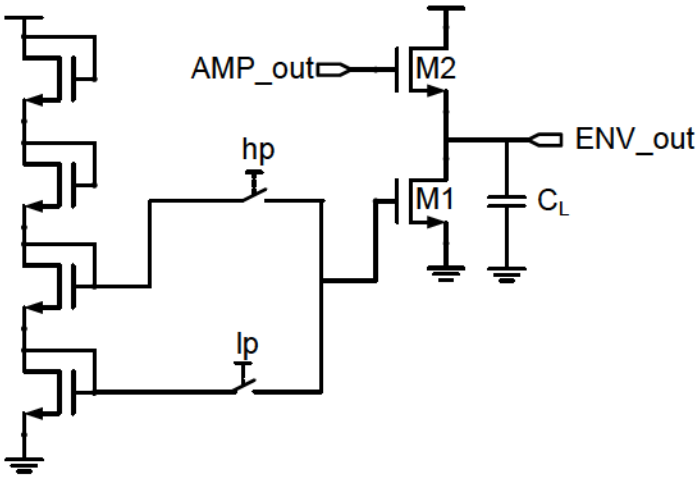


Fig. 4.17: The schematic of the NMOS-based envelope detector

Therefore, the equivalent resistance seen from the source of M2 ($1/g_m$) will decrease, which leads to a larger bandwidth when combined with the load capacitor C_L.

Note that *lp* and *hp* signals in Fig. 4.17 represent the control signals for the MO and ID modes, which provides the required input voltages of 125 mV and 250 mV for the gate of M1, respectively.

In our design, M1 has a sizing ratio of 1 µm/1 µm and M2 is sized with 10 µm/0.2 µm ratio to ensure very low current density and hence subthreshold operating region. The load capacitor in the envelope detector is a dual MIM type with a large value of C_L=16.8 pF.

4.6 Baseband Amplifier Stage

The baseband signal from the envelope detector needs to be amplified and further filtered in order to be used by the following digital stages. Two amplifier stages shown in Fig. 4.18 are used to amplify the baseband signals ranging from about 2.5 kHz to 300 kHz in order to cover the data rates of the Manchester encoded baseband signals for both MO and ID modes. C_i is a DC blocking capacitor and R_i has a large value. The output capacitance, C_L is controlled via the digital block according to the required bandwidth for the two modes of operation.

The first output inverter is employed to provide a CMOS rail-to-tail analog baseband signal. It is followed by a standard-cell inverter, which works as a level-shifter for delivering a compatible digital signal to the digital detection block.

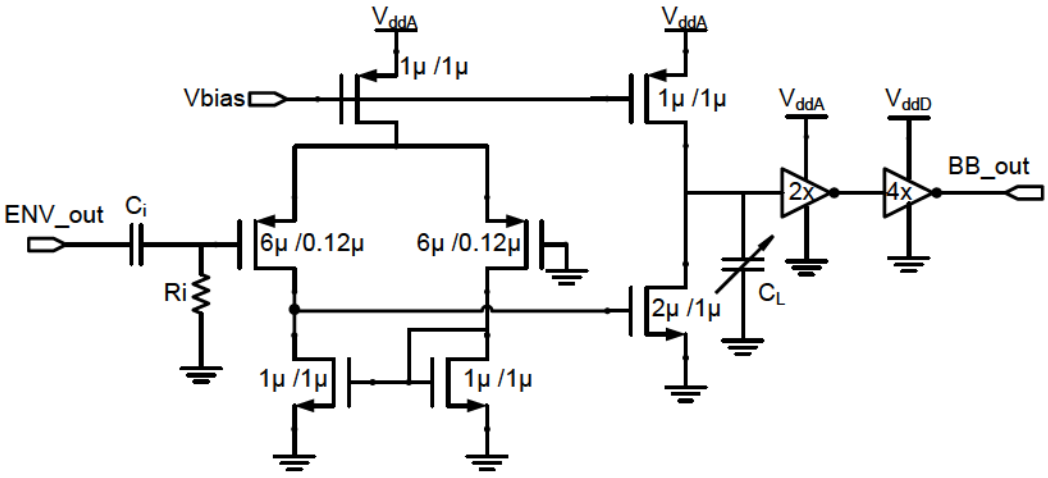


Fig. 4.18: Schematic of the two-stage baseband amplifier and inverters

4.7 Digital Detection Circuitry

An on-chip digital detection circuit is implemented for the wake-up receiver. The simplified block diagram is shown in Fig. 4.19.

Manchester coding is used in order to define 0 and 1 bits as transitions from 0 to 1 and 1 to 0, respectively. The detection circuitry is comprised of an edge-detection circuit, a monostable multivibrator, shift registers and several logic gates. The true wake-up signal is triggered upon detection of a true ID-code after having received the preamble bits by the monostable multivibrator. We have defined 8 preamble bits and 22 Manchester-coded ID-bits, whose first 6 are used as the start bits and the remaining 16 coded bits (8 bits uncoded) are the unique wake-up code of the receiver.

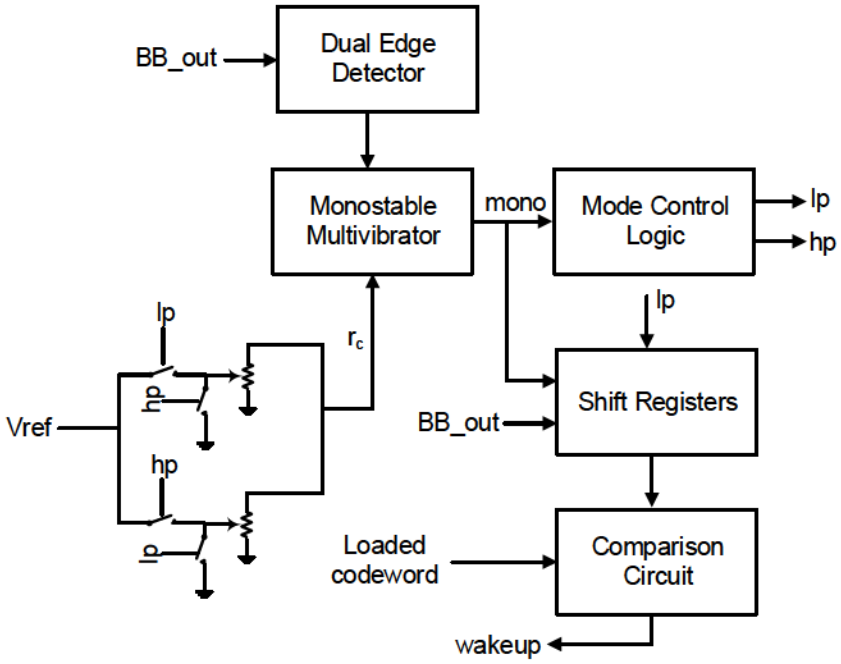


Fig. 4.19: Block model for the on-chip digital circuitry

Thanks to the use of Manchester encoding, there has been no need to use an extra baseband clock for detection circuitry. In fact, the baseband clock has been embedded in the transmitted data. That is the 0 and 1 bits can be detected on the rising and falling edges of data transition from 0 to 1 and 1 to 0, respectively. Therefore, frequency mismatch will no longer be a concern at this stage. The digital

detection circuitry has been designed such that it sees all the incoming bits as Manchester-encoded bits.

The timing constraint of the *mono* clock relates to the period of the clock being with some broad range of the data period T during each mode. In other words, the high state of the *mono* signal must be between T and $2T$ to ensure that the right data will be clocked into the shift registers. This has been determined by the *rc* signal of the multivibrator whose time constant varies according to the operating mode. The transient simulation results for the *rc* and *mono* signals are shown in Fig. 4.20.

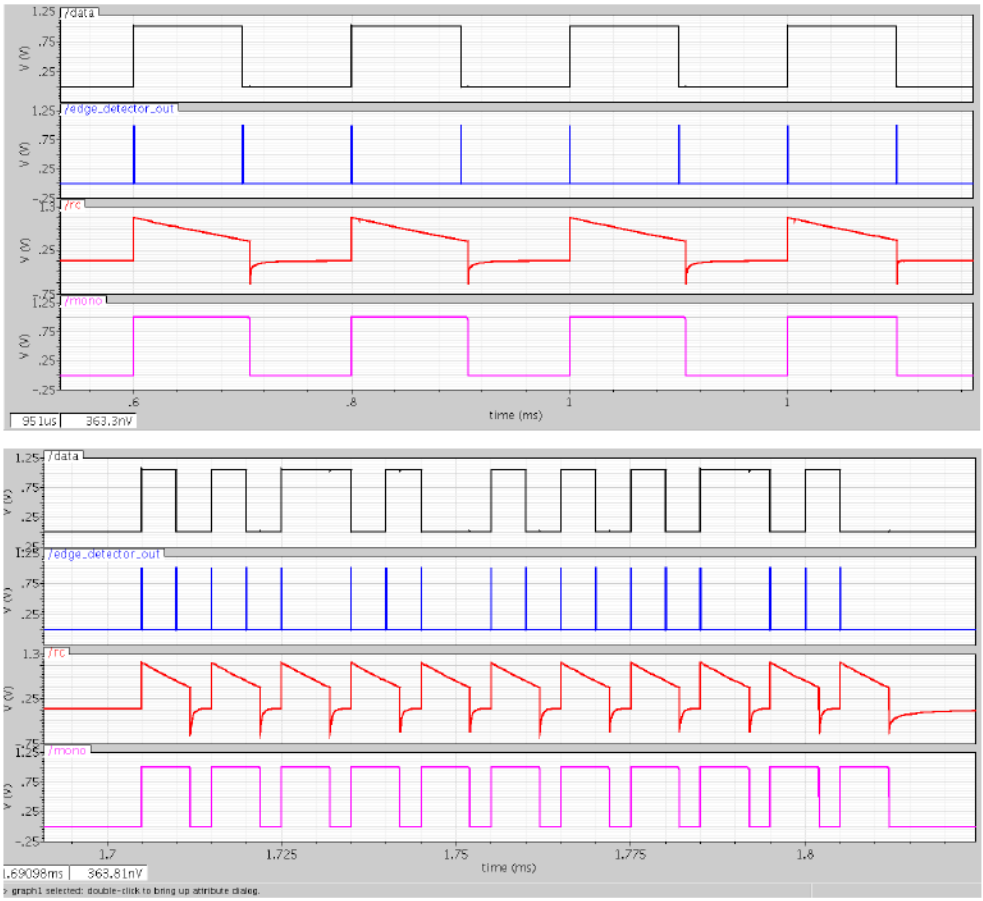


Fig. 4.20: Transient simulation results of the detection circuitry in the MO mode at 10 kbps (Top), and in the ID mode at 200 kbps (Bottom)

The preamble codes are defined as 8 alternating bits starting from 1 and ending in 0. The parameters of the monostable multivibrator are chosen corresponding to the low data-rate of 10 kbps in the preamble mode (MO). Once the preamble bits are detected, the multivibrator's parameters are altered automatically to be able to receive the incoming data at the rate of 200 kbps. That is, the *lp* signal changes from high to low, which lowers the resistance at node *rc* thereby reducing the time constant of the multivibrator. The resistances as well as the switches in Fig. 4.19 are implemented by NMOS transistors as shown in Fig. 4.21. The sizing for the transistors has been chosen from the simulation for the two modes. The local process variation and mismatch for the two configurations has been minimized by using relatively large size transistors as well as suitable layout techniques. However, temperature and global process variation still affect the time constant of the multivibrator. Also, note that the reference voltage V_{ref} has been internally generated by a process and temperature independent circuit that is only sensitive to digital supply variation.

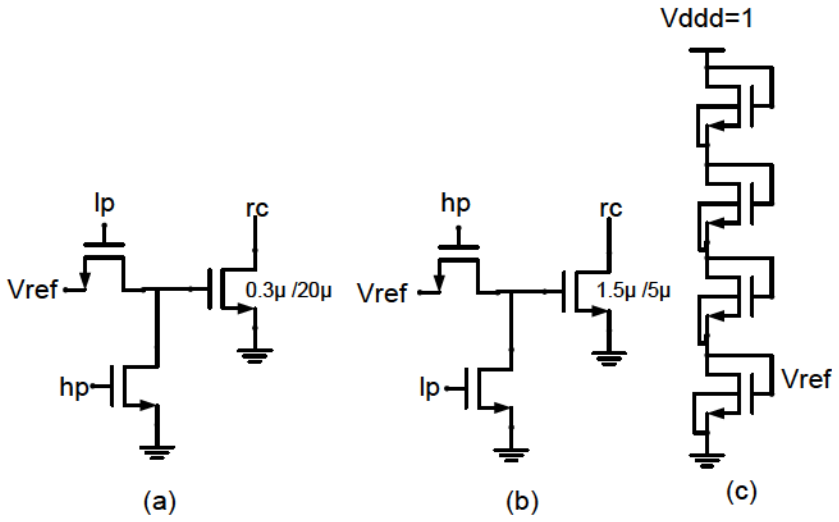


Fig. 4.21: Realization of the resistance of the multivibrator circuit in the (a): MO mode and (b): ID mode (c): Block model for the on-chip digital circuitry for the V_{ref} generator used in the digital detection circuitry

According to simulation results, a 1°C increase in the temperature results in a decrease in the width of the *mono* signal by 842 ns and 64 ns during the MO and ID modes, respectively. Nevertheless, the *mono* clock is correctly generated for a temperature range of 2 °C to 36°C during both modes. The width of the *mono* clock is also increased due to a 10 mV decrease in the digital supply voltage by 4.4 µs and 250 ns during the MO and ID modes, respectivelyAccording to Monte-Carlo simulation results with 100 iterations for the combined process and mismatch variations, 70% of the cases in the MO mode and 60% of the cases in the ID mode yield the mono clock within the desired range. In order to increase the yield as a future work, one can allocate a bank of resistances at node *rc* rather than only one resistance in order to control the time constant of the multivibrator whenever the width of the mono signal is not within the desired range.

The first 6 (coded) starting bits could be 010101 or 010110 depending on the first bit of the rest of the code beginning with a 1 or a 0, respectively. The uncoded 8 bits of the wake up code that are generated at the output of the shift registers are then compared to the one that has been already loaded to another shift registers and the wake-up signal is only generated once the codes are matched. The unique 8-bit codeword for this wake-up receiver is chosen to be 01000011.

Finally, the Mode Control Logic block controls the operating modes for the all the building blocks in the receiver chain. The user can control the mode of operation manually for measurement purposes especially for BER testing in both modes. The average power dissipation of the digital circuitry is about 280 nW from a 1 V digital power supply.

4.8 Buffer Amplifiers

Aside from the standard cell inverters used to buffer digital signals, two source follower amplifiers are employed in this design for measuring the output of the IF-

amplifier as well as the envelope detector. The simplified model of the analog output buffer is shown in Fig. 4.22. These source follower buffers are used in order to isolate the analog circuits from the loading of the bonding pad and the measurement equipment modeled as R_L and C_L. The analog output buffers are biased at the pad-ring voltage of V_{dd_ring} =2.5 V and draw 10 mA from the supply. Also, large high-voltage transistors are used in order to avoid transistors breakdown. Since the buffers only present to allow testing, their power dissipation is not included in the total power dissipation of the receiver.

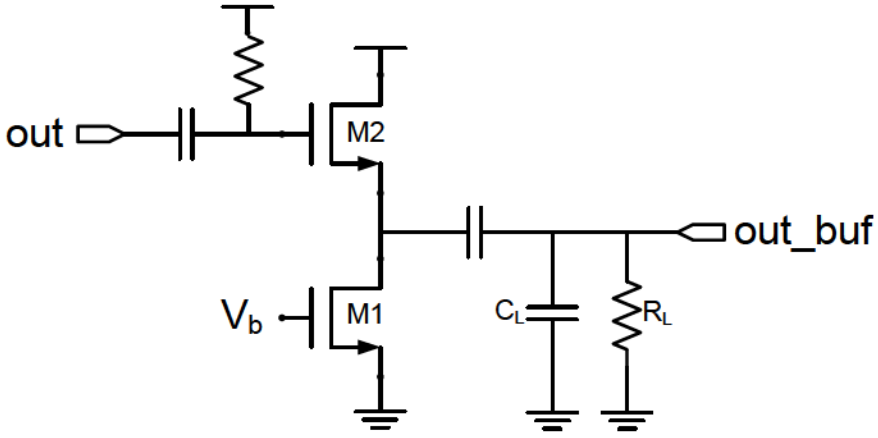


Fig. 4.22: Schematic of the output source follower used for analog signals

4.9 Simulation Results

Simulation results for the complete receiver chain starting from the transmitted wake-up pattern all the way to the generation of the wake-up signal at the output of the wake-up receiver are shown in Fig. 4.23. These results are obtained from the extracted post-layout simulation and include all the parasitics from the I/O pads as well as from the CQFP44 package model, the board and the equipment loading. The wake-up pattern (Fig. 4.23.a) OOK modulates an RF signal at 915 MHz with -70 dBm power (Fig. 4.23.b). Since the gain of the amplifier is relatively large

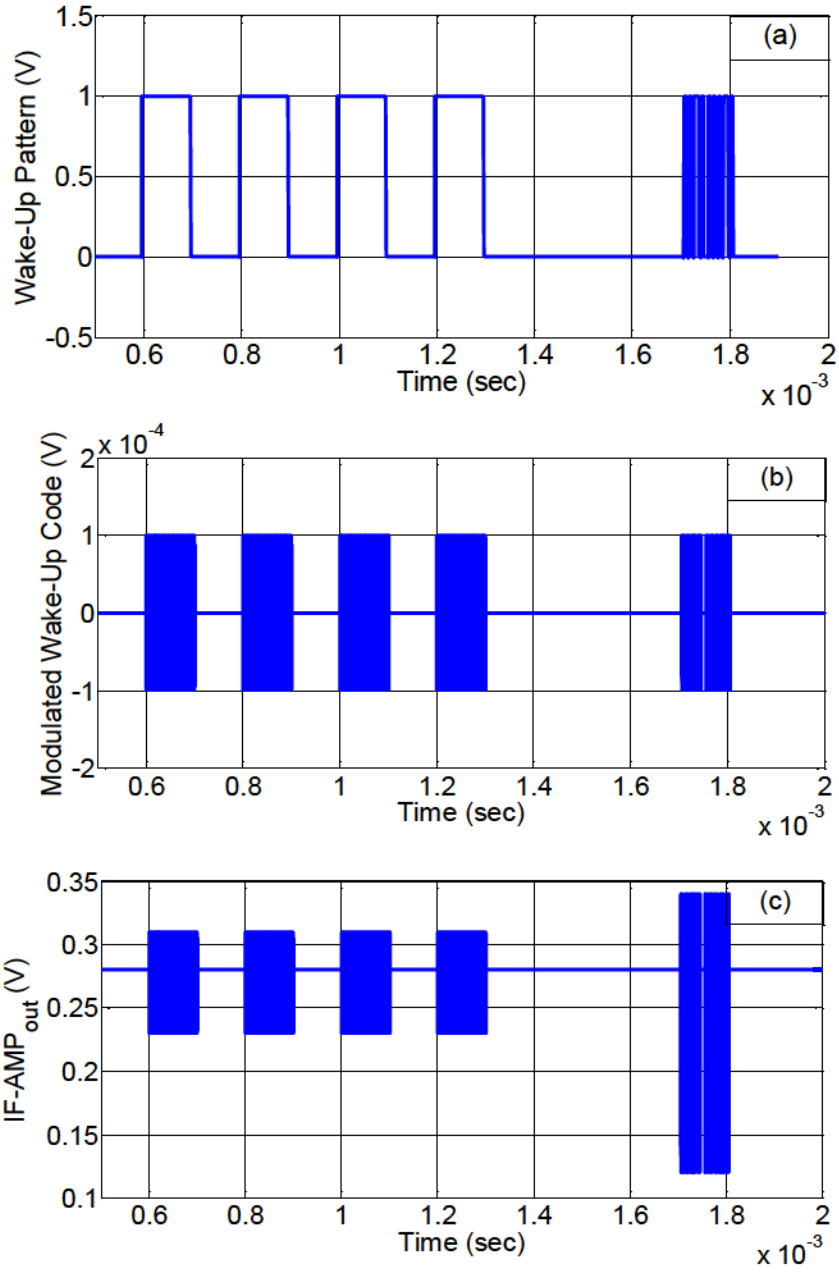
particularly during the ID mode, the transistors of the last stages of IF amplifier are prone to be fed with large input and manifest nonlinear effects such as the observed asymmetric response around the DC level that is due to the generation of signals at harmonics of the desired frequency. However, this will not occur for practical input power levels to the wake-up receiver particularly for the minimum detectable input power.

The received modulated signal is downconverted to IF using the subsampler and later amplified before detection (Fig. 4.23.c). The envelope detected signal (Fig. 4.23.d) is then digitalized at the end of the baseband amplifier (Fig. 4.23.e) and the wake-up signal (Fig. 4.23.f) is generated at the output of the detection circuit.

The sensitivity of the wake-up receiver can be estimated in the two modes by plotting the input referred noise derived from the simulation results vs. the input power as shown in Fig. 4.24.

It is observed that the sensitivity is better during the MO mode (i.e. -80 dBm), which is as a result of using a lower data rate and lower bandwidth than required in this mode. It can be concluded that the receiver can still achieve a sensitivity of about -77 dBm with a higher data rate during the MO mode.

Finally, the breakdown of power dissipation for individual constituting blocks in the two modes of operation has been summarized in Table 4.3.


(a)
Wake-Up Pattern (V)
1.5
1
0.5
0
-0.5
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Time (sec)
x 10^-3
(b)
Modulated Wake-Up Code (V)
x 10^-4
2
1
0
-1
-2
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Time (sec)
x 10^-3
(c)
IF-AMP_out (V)
0.35
0.3
0.25
0.2
0.15
0.1
0.6
0.8
1
1.2
1.4
1.6
1.8
2
Time (sec)
x 10^-3

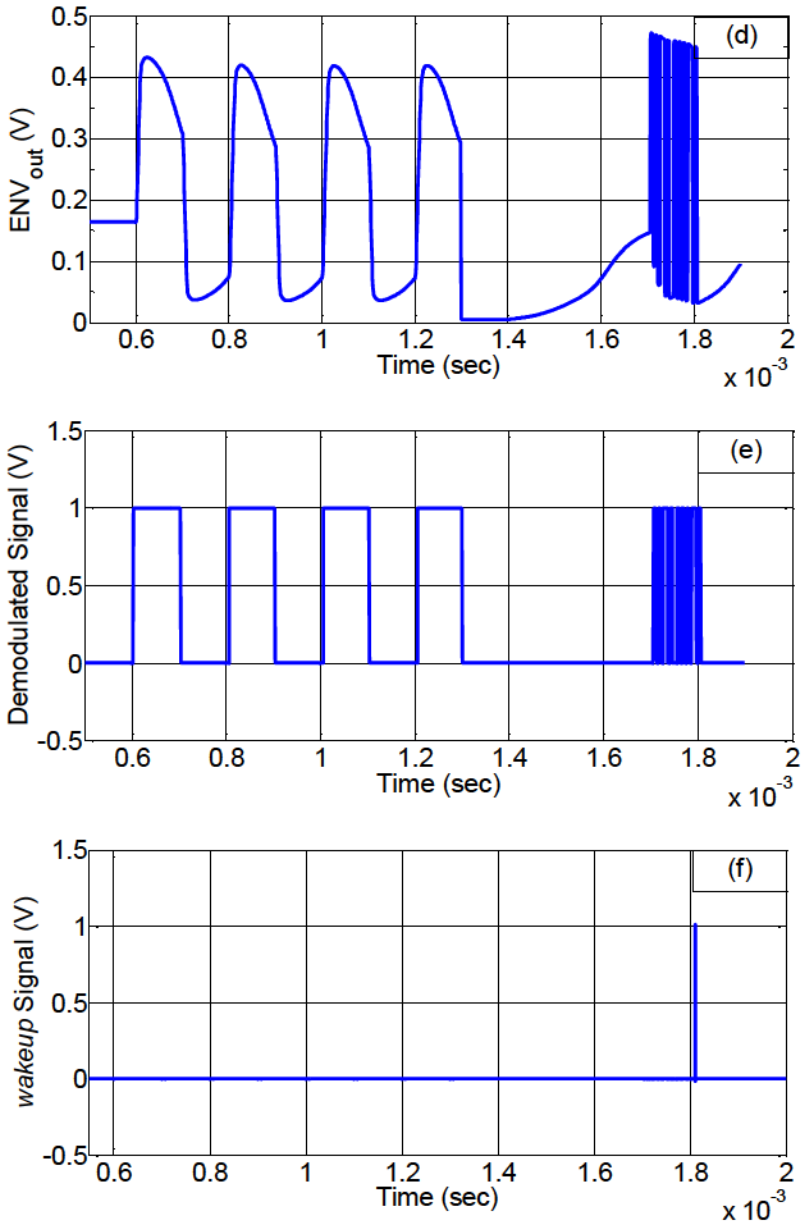


Fig. 4.23: Simulation results of the complete WuRx chain: a) wake-up pattern, b) received OOK modulated data, c) subsampled and amplified signal, d) envelope-detected signal, e) digital demodulated data, f) wake-up signal at the output of the receiver

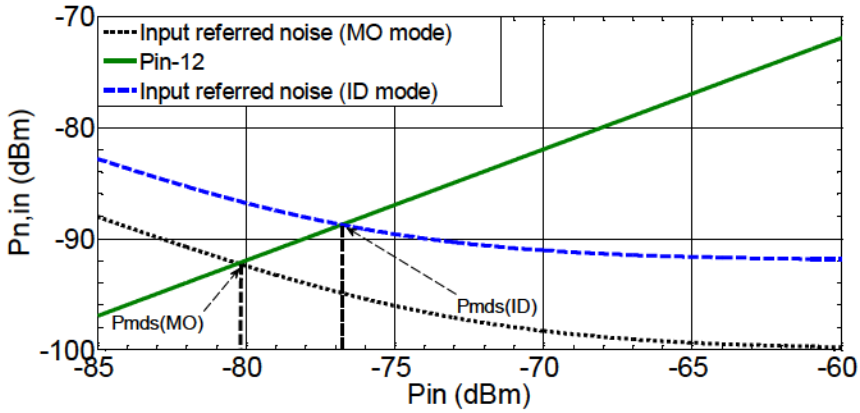


Fig. 4.24: Calculation of the sensitivity based on the simulation results

Table 4.3: Power Dissipation Breakdown for Individual Blocks

	VCO	IF Amp	Envelop Detector	BB Amp	Digital Circuit	Biasing Circuits	Total
MO	5µ	7.8µ	16.5n	2.7µ	280n	250n	**16µ**
ID	5µ	13µ	500n	2.7µ	280n	250n	**21.7µ**

Table 4.4 compares the performance of some of the best wake-up receivers to date. It can be seen that the proposed dual-mode wake-up receiver operates with a relatively high sensitivity, while consuming ultra-low power from the supply. Also, unlike [51], the power dissipation in the ID mode is still very low as a result of using the subsampling architecture. The energy consumption per bit for this wake-up receiver has been calculated in each mode by calculating the measured power dissipation to data rate. For a fair comparison, the FOM has been defined as the dissipated energy per bit (J/bit) for each mode of operation multiplied by the measured corresponding sensitivity in Watts:

$$\text{FOM} = (Energy/bit) * P_{MDS}(W) = (nJ/bit) * 10^{\left(\frac{P_{MDS}(dBm)-30}{10}\right)} \qquad (5.6)$$

Table 4.4: Performance Comparison of the Published Wake-Up Receivers

	[47]	[22]	[34]	[46]	[51]		This Work [56]	
Freq. (GHz)	0.868	2	0.915	2.4	0.915		0.915	
Technology	130 nm	90 nm	90 nm	65 nm	0.18 µm		130 nm	
Data Rate (bit/s)	64	100 k	10 k	250 k	1 k/200 k		10 k/200 k	
Sensitivity (dBm)	-83	-72	-80	-87	-75.8/-72		-78.5/-75	
Power (µW)	3	52	51	415.2	8.5/1078		16.4/22.9	
Energy Efficiency (nJ/bit)	46.87	0.52	5.1	1.66	8.5	5.39	1.64	0.11
FOM ($x10^{-20}$)	23.5	3.2	5.1	0.33	22.3	34	2.3	0.34

It is worth noting that although the FOM of the receiver in [46] is comparable to that of our receiver in ID mode, the former has been achieved at the cost of much larger power dissipation, that is higher than the typical value of 100 µW for an ultra-low power wake-up receiver. Therefore, employing the dual-mode architecture with two different detection bandwidths has enabled our receiver to be the most energy-efficient wake-up receiver to date operating with an input power of as low as -78.5 dBm. The detailed test plan as well as the complete measurement results of this novel wakeup receiver will been elaborated in the next chapter.

The graphical locations of our subsampling-based wake-up receiver [20] presented in Chapter 3 as well as the dual-mode wake-up receiver [56] presented in this chapter have been shown in comparison to other ultra-low power receivers in Fig. 4.25.

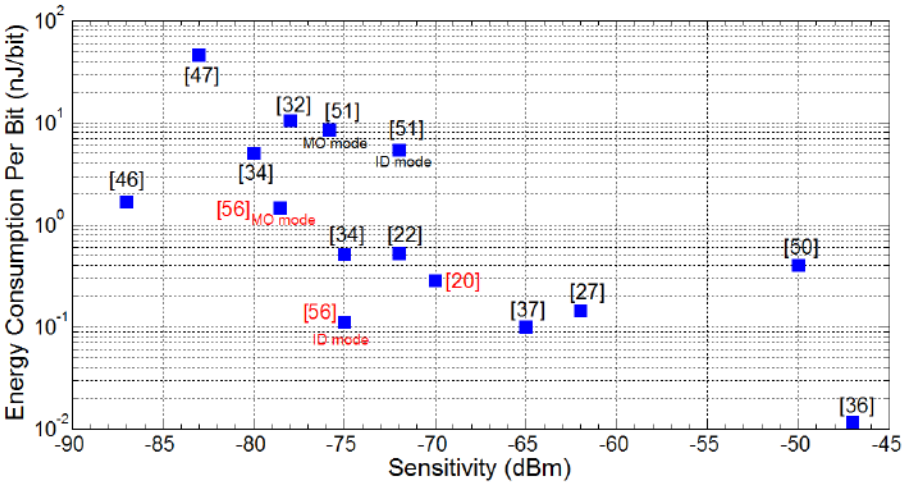


Fig. 4.25: Location of our receivers among other ultra-low power receivers

4.10 Conclusion

In this chapter, a novel wake-up receiver based on the subsampling architecture is proposed. Using this architecture, the energy consumption is reduced by adopting two modes of operation with different power dissipations and detection bandwidth. During the Monitoring mode (MO), the start frame bits are received at a data rate of 10 kbps, while during the ID mode the remaining wake-up pattern is transmitted at 200 kbps. The gain of the front-end amplifier and hence the power dissipation is reduced in the MO mode, which in turn causes an increase in the overall noise figure of the receiver. However, this is compensated by intentionally lowering the data rate as well as the detection bandwidth of the receiver.

The proposed wake-up receiver is designed and fabricated in 130 nm CMOS technology with a core size of 0.2 mm^2 for the target frequency range of 902-928

MHz dedicated for ISM band applications. The measured results showed that the proposed dual-mode receiver achieves a sensitivity of -78.5 dBm and -75 dBm while dissipating an average power of 16.4 µW and 22.9 µW during MO and ID modes, respectively. The proposed receiver achieves the smallest energy per bit-sensitivity product among other published ultra-low power wake-up receiver designs.

Chapter 5

Test Plan and Measurement

The wake-up receiver presented in Chapter 4 has been laid out and fabricated with IBM 130nm CMOS process. Fig. 5.1 shows the magnified view of the die. The core size of the wake-up receiver is around 0.2 mm^2 and the total area of the chip including the pads is 1 mm^2. The total current consumption of the receiver during MO and ID modes are 16.4 µW and 22.9 µW, respectively.

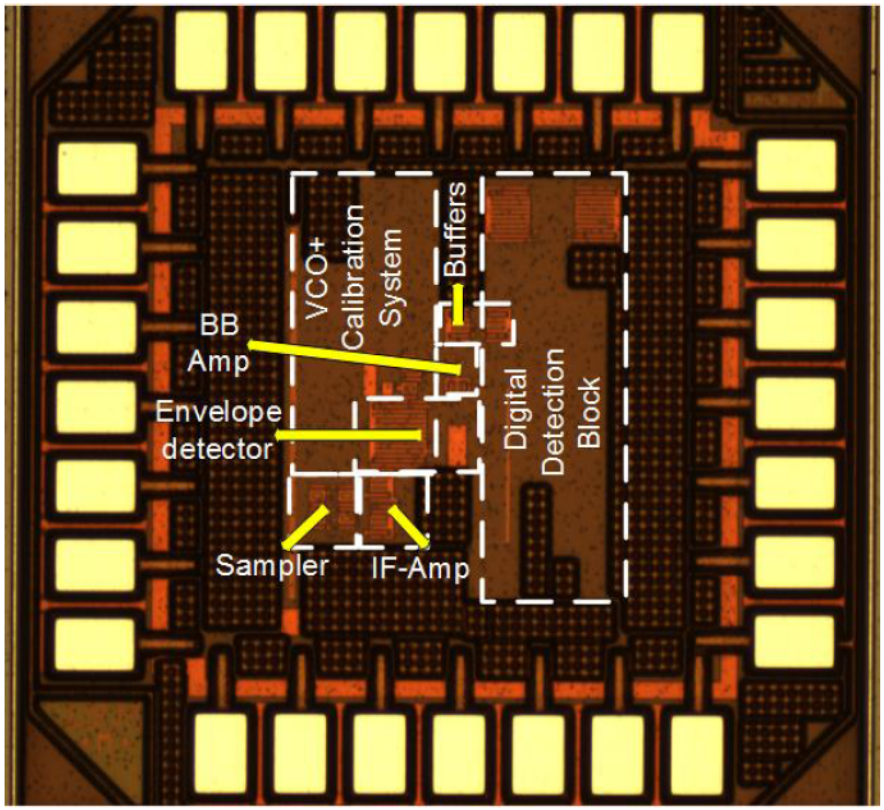


Fig. 5.1: Photo of the wake-up receiver die

5.1 Definition of the Pins

The die has been placed inside a 44 pins Ceramic Quad Flat Package, CQFP44, where only 28 pins are being used by the chip. Table 5.1 includes the definition of the Input (I) and Output (O) pins for Analog (A) and Digital (D) signals as well as power supply nets.

Table 5.1: Description of the Pins inside the CQFP44 Package

Pin	Pin Name	Type	Description
2	*AMP_BIAS*	I/D	Biasing Data for the Front-End Amplifier
3	*AMP_TUNE*	I/D	Tuning Data for the Front-End Amplifier
4	*RESET*	I/D	Reset Signal
5	*CLK_BIAS*	I/D	Clock for Biasing the Front-End Amplifier
6	*IEXT1*	I/A	External Biasing for Front-End Amplifier
7	*EXT1_EN*	I/D	Enable Signal for Biasing the Front-End Amplifier
8	*HP_EXT*	I/D	External power-mode selection
9	*BER_TEST*	I/D	BER Test Selection
13	*VSSRING*	Power	Ground
15	*IEXT2*	I/A	External Biasing for Baseband Amplifier
16	*EXT2_EN*	I/D	Enable Signal for Biasing the Baseband Amplifier
17	*VDDRING*	Power	1V Pad Ring Power Supply
18	*MONO*	O/D	Output of the Monostable Multivibrator block
19	*CLK_ID*	I/D	Clock for the ID-Code Input Data
20	*DATA_ID*	I/D	ID-Code Input Data
24	*WAKEUP*	O/D	Output Wakeup signal
25	*RESET_DIG*	I/D	Digital Block Reset Signal
26	*ENV_OUT*	O/A	Output of the Envelope Detector

28	*AMP_OUT*	O/A	Output of the Front-End Amplifier
30	*VSS*	Power	Ground
31	*DIG_OUT*	O/D	Demodulated Digital Baseband Data
32	*VCO_OUT*	O/D	VCO Output Signal
35	*FREF*	I/A	External Reference Oscillator
36	*START_CAL*	I/D	VCO Calibration ON/OFF
37	*VDDD*	Power	1V Digital Power Supply
38	*VDD*	Power	500mV Analog Power Supply
39	*RF-*	I/A	Negative Port of the Input RF Signal
40	*RF+*	I/A	Positive Port of Input RF Signal

5.2 Test Equipment

The following test equipment is used to setup the test environment and to initiate the measurements:

- **DC Power Supply/Meter (Keithley 2400 SourceMeter):** To generate *VDD*, *VDDD*, *VDDRING* power supplies, to feed external bias currents *IEXT1*, *IEXT2* (If required), and to accurately measure the power dissipation
- **Parallax board of education with a PIC16C57 Microcontroller:** To feed in the following 12 digital control signals: *AMP_BIAS* (5-bits serial data), *AMP_TUNE* (5-bits serial data), *RESET*, *CLK_BIAS*, *EXT1_EN*, *EXT2_EN*, *HP_EXT*, *BER_TEST*, *CLK_ID*, *DATA_ID* (8-bits serial data), *RESET_DIG*, and *START_CAL*
- **Agilent E5071B Network Analyzer:** To analyze the input matching of the receiver
- **Agilent E4438C ESG Vector Signal Generator:** To generate the OOK modulated signal to the receiver and to perform the BER measurement

- **Agilent E4445A Spectrum Analyzer**
- **DPO7254 Digital Phosphor Oscilloscope**

5.3 Preliminary Test Plan

Table 5.2 summarizes the minimum, typical, and maximum bias voltage and current values for test pins. The values have been obtained from the extracted simulation results across the PVT corners prior to the measurements.

Table 5.2: Operating Conditions and Expected Bias Voltages and Current

Parameter	Test Pin	Min	Typical	Max	Unit	Condition
Analog Power Supply	*VDD*	475	500	610	mV	-
Digital Power Supply	*VDDD*	0.9	1	1.12	V	-
Front-End Amplifier's Bias Voltage	*IEXT1*	130	159	200	mV	-
BB Amplifier Bias Voltage	*IEXT2*	160	297	500	mV	-
Current Consumption from 0.5 V Supply	*VDD*	25.67	26.96	32.97	µA	MO mode
		36.53	38.37	46.92	µA	ID Mode
Current Consumption from 1 V Supply	*VDDD*	2.45	2.58	3.14	µA	-

The output of the front-end amplifier (*AMP_OUT*) is also expected to behave according to what has been described in Table 5.3.

Table 5.3: Operating Conditions of the Front-End Amplifier

Parameter	Min	Typical	Max	Unit	Condition
Voltage Gain	388	500	850	V/V	digital tuning input varies from 00000 to 11111 during the ID mode
Center Frequency	18	30	35	MHz	
Bandwidth	10	15	18	MHz	

The digital control signals as well as the clocks are fed into the chip through the programmed microcontroller for the following modes of operation: VCO calibration mode, wakeup or normal mode, and BER test mode. This has been described in Table 5.4.

Table 5.4: Digital control signals during calibration, wakeup, and BERT mode

Pins	VCO Calibration Mode	After VCO Calibration (Wakeup Mode)	External BER Test Mode
AMP_BIAS	-	00111	00111
AMP_TUNE	-	00111	00111
RESET	1	0	0
CLK_BIAS	OFF	ON	ON
EXT1_EN	0	0	0
HP_EXT	0	0	1
BER_TEST	0	0	1
EXT2_EN	0	0	0
CLK_ID	OFF	ON	ON
DATA_ID	-	Programmable	-
RESET_DIG	1	0	-
START_CAL	1	0	0

The codeword for the *AMP_BIAS* and *AMP_TUNE* has been found based on the typical extraction and PVT corner. Note that external biasing may be only needed (i.e. *EXT1_EN*=1 and *EXT2_EN* =1) if the measured gate-source voltage of the diode-connected NMOS transistors (connected to the IF and BB Amplifier stages, respectively) is out of the expected range.

In the wakeup-testing mode, the programmable 8-bits unique wakeup code defined as *DATA_ID* will be clocked into the internal 8 shift registers via *CLK_ID* prior to reception of data. However, the actual wakeup code in the ID mode is received in the forms of 16-bits Manchester-coded word. For instance, the uncoded 8-bits wake-up code of 11000011 would correspond to the following Manchester-coded bits: 10-10-01-01-01-01-10-10.

Table 5.5 specifies the preamble bits as well as the staring bits and Manchester coded wakeup bits during the wakeup-testing mode. As a result, having received the preamble and starting bits, the true wakeup signal is only generated once the received wakeup code matches the pre-loaded 8-bits wakeup data.

Table 5.5: Preamble, starting, and wakeup code bits in wakeup-testing mode

Preamble bits (MO Mode)	Starting bits (ID mode)	Wakeup Code (ID mode)
1,0,1,0,1,0,1,0	0,1,0,1,0,1	1,code[14:0]
	0,1,0,1,1,0	0,code[14:0]

5.4 Input Matching

Having verified that all the measurable voltages and currents described earlier are within the expected range, the first critical parameter to investigate is the input matching of the wake-up receiver. For this purpose, an RF balun of 0915BM15A0001E from Johanson Technology, which also behaves as a bandpass filter for the frequency range between 902 MHz to 928 MHz, has been employed

at the front-end of the receiver and is soldered on the printed circuit board. This component is supposed to provide the single-end to differential conversion for the input RF signal as well as the required high-Q filtering. Fig. 5.2 shows the schematic of the input matching components for the chip. The on-board matching components of *L1*=*L2*=20 nH, and *C1*=*C2*=0.8 pF are soldered close to the packaged chip in order to provide the required impedance see from the output of the RF balun.

The S11 parameter is measured using the Agilent E5071B Network Analyzer. However, the additional matching elements of *L0*=6 nH and *C0*=12 pF are found after the first S11 measurments and are soldered close to the edge of the pcb in order to fine tune the input matching to 50 Ω. Fig. 5.3 shows the measured S11 parameter.

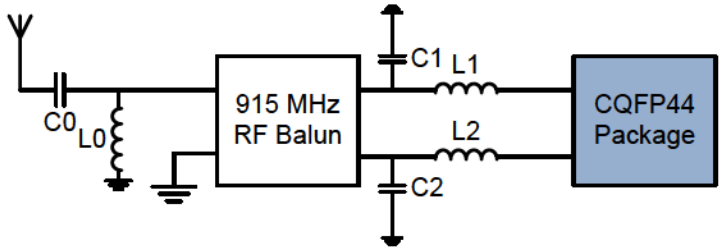


Fig. 5.2: Schematic of the external components for input matching

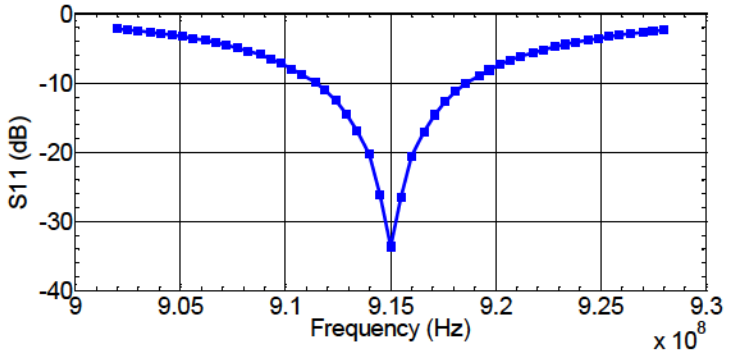


Fig. 5.3: Measured input matching using external *LC* components

5.5 VCO Frequency Calibration

In practice, the output frequency of the VCO has been measured after an on-chip divide-by-8 block followed by an output buffer. The measured plot of f_{VCO} is shown in Fig. 5.4. It can be seen that the output frequency increases gradually from its initial frequency of 10.4 MHz, which translates to 83.2 MHz for the internal VCO frequency. The final calibrated frequency is close to 17 MHz that is translated to an internal desired VCO frequency of 136 MHz. Fig 5.5 depicts the spectrum frequency of the VCO, which has been measured by the spectrum analyzer.

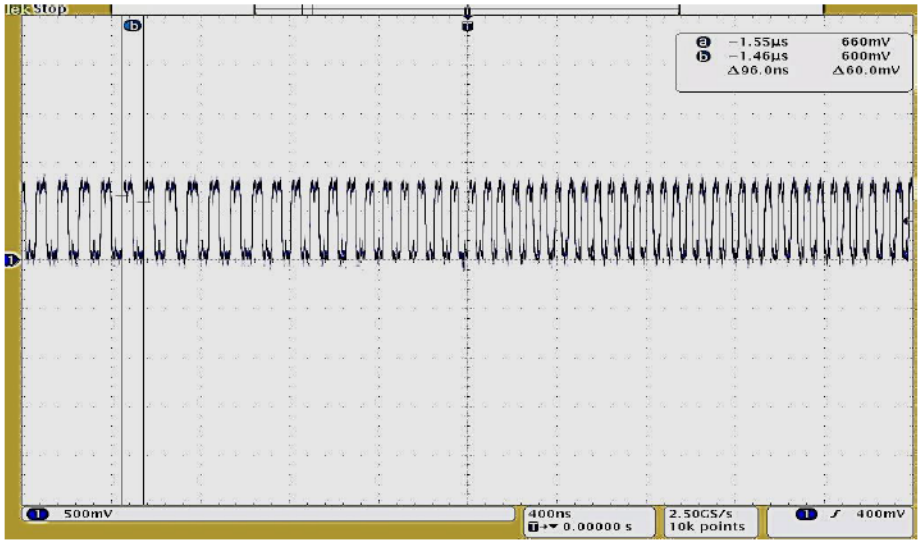


Fig. 5.4: Plot of the measured f_{VCO} as a function of time as the frequency is automatically calibrated

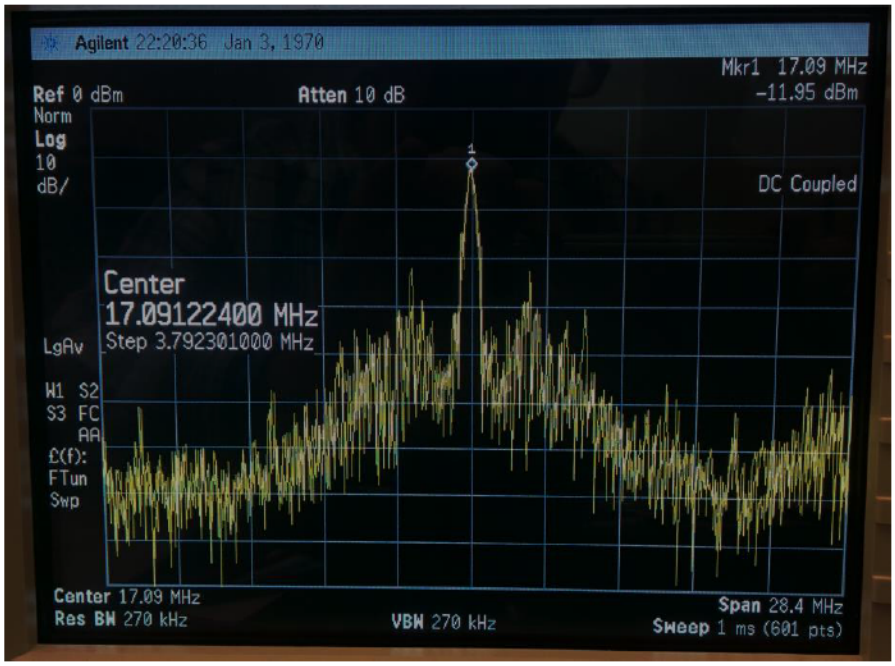


Fig. 5.5: Snapshot for the measured frequency spectrum of the f_{VCO} using the spectrum analyzer

5.6 Subsampler+IF-amplifier

As mentioned earlier, an external RF balun has been used on the test board, which also acts as a bandpass filter to provide the required filtering of the RF signal centered at 915 MHz with a bandwidth of 26 MHz. In order to verify the performance of the combined on-chip subsampler/IF-amplifier after the external RF filtering, the following test procedure has been performed:

By intentionally varying the sampling frequency of the VCO from the desired 136 MHz, the RF signal at 915 MHz will be downconverted to a frequency other than the center frequency of 37 MHz. As a result, a plot of the frequency spectrum for the subsampled and amplified signal will be obtained through measuring the value of the signal at the output of the IF-amplifier for every subsampling frequency.

Fig. 5.6 shows the simulated and measured frequency response of the combined blocks of the subsampler and IF-amplifier (including the output buffer). However, due to a limitation in the frequency resolution of the VCO calibration circuit, some of the nearby frequencies cannot be easily obtained. Instead, the supply voltage has been slightly tuned in order to acquire and plot the missing points that are very close to the desired frequency of 136 MHz,

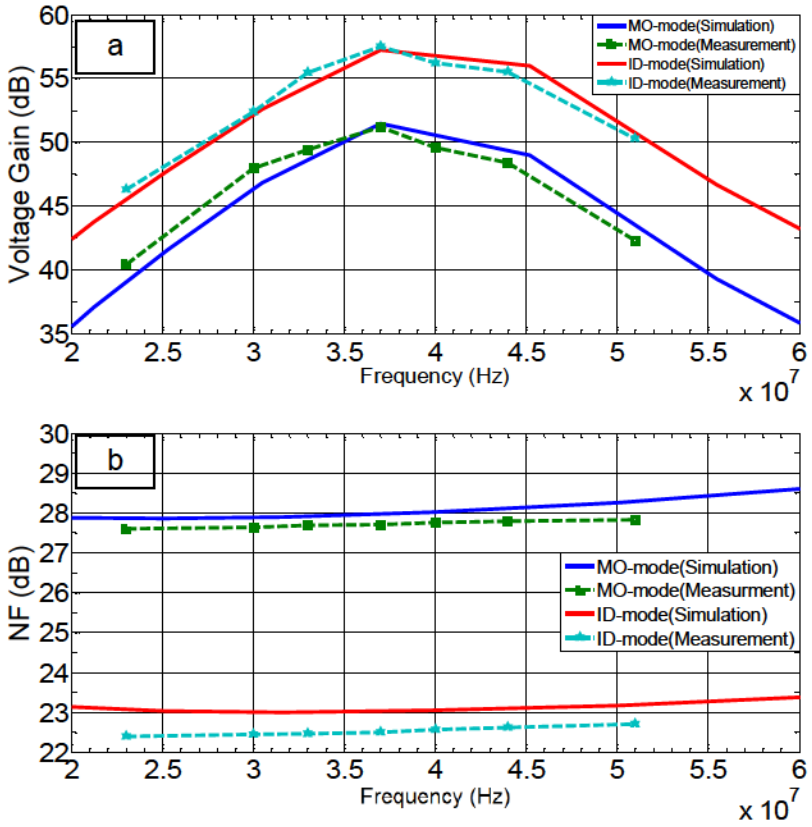


Fig. 5.6: Simulated and Measured a) Frequency response and b) Noise Figure of the combined subsampler+IF-amplifier in the two modes

Using the above technique, the measured points are obtained by adjusting the subsampling frequencies to 125 MHz, 126 MHz, 134 MHz, 135 MHz, 136 MHz, 137 MHz, and 138 MHz that bring the RF signal at 915 MHz down to corresponding IF frequencies of 40 MHz, 33 MHz, 23 MHz, 30 MHz, 37 MHz, 44

MHz, and 51 MHz all with the sampling ratio of 7, respectively. It can be seen from Fig. 5.6.a that the 3-dB bandwidth of the IF-amplifier is around 13 MHz in the two modes of operation. The measured values of the voltage gains using the spectrum analyzer are close to the ones already obtained from the post-layout simulation.

Fig. 5.6.b shows the noise contribution of the combined subsampler and IF-amplifier in the two modes obtained from post-layout simulation and measurement results. The total noise factor of the receiver prior to the envelope detector during the MO mode is about 5 dB higher than the noise factor during the ID mode, which agrees with the results of the post-layout simulation.

5.7 Wakeup and BER Tests

Once the on-chip VCO block has been calibrated to the desired sampling frequency and the operation of the combined front-end amplifier/subsampler circuit has been fully verified, the chip will be ready to perform two critical measurements: Wakeup and BER.

Not all of the existing wakeup receivers that are implemented for academic purposes include an on-chip detection circuitry for generating the wakeup signal, mainly due to the large required area for digital circuits. Therefore, the digital detection is usually performed off-chip.

We have included a dedicated all-digital detection block in our design, whose job is to detect the transmitted data that are only received at the expected data rate of 10 kbps and 200 kbps during the MO and ID mode, respectively and to ultimately generate the wakeup signal as soon as the correct programmable wakeup code has been received.

In order to perform this test, we initially modulate the complete wake-up pattern according to the same timing used in the simulation results of Fig. 4.23 and measure the received demodulated signal at the output of the IF-amplifier as well as the

envelop detector. Fig. 5.7 shows the measured waveform at the output of the IF-amplifier.

Unfortunately, the output of the envelop detector failed to be measured properly. However, the demodulated digital signal at the output of the receiver in the two modes as well as the wake-up signal have been successfully measured by probing the *DIG_OUT* and *WAKEUP* output pins as shown in Fig. 5.8. This confirms the functionality of the envelope detector as well as the digital detection block.

Note that although the receiver will be able to detect signals with much lower amplitudes, the measured result has been shown for a moderate input power of -70 dBm, only to demonstrate that the complete receiver including the detection circuitry is working properly as expected.

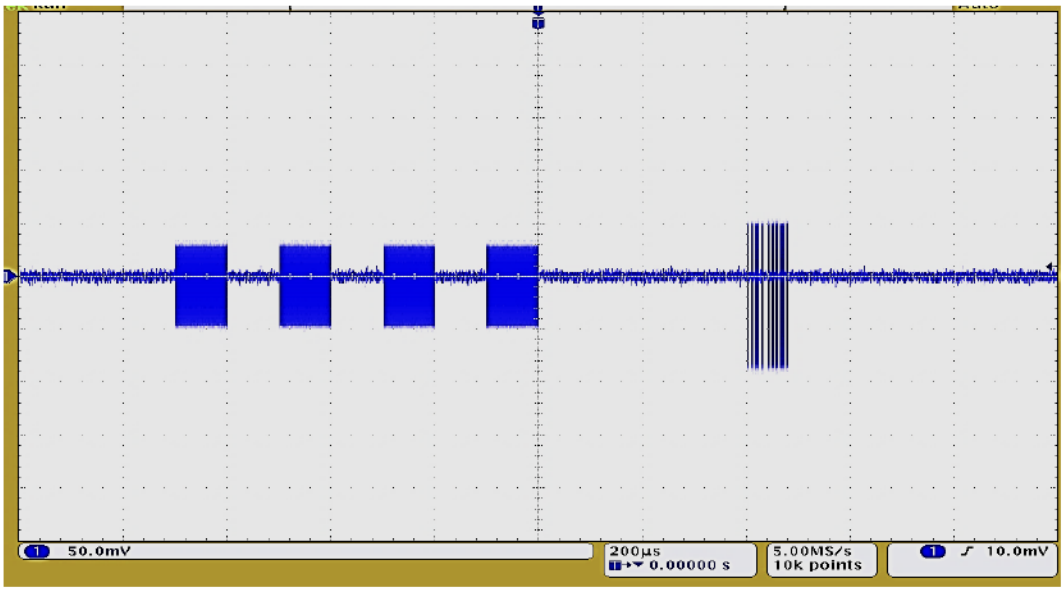


Fig. 5.7: Measured waveform of the output of the IF amplifier

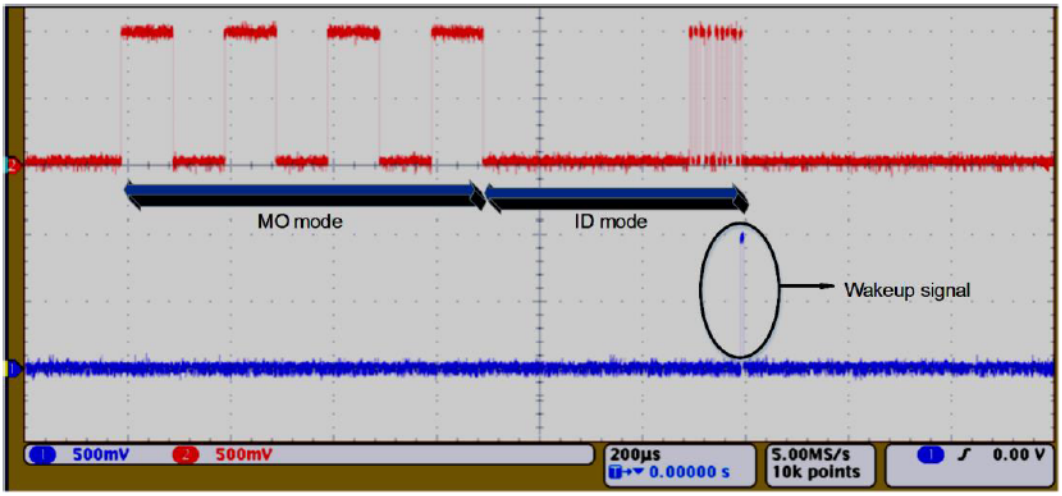


Fig. 5.8: Top: Measured demodulated wake-up bits, bottom: The wakeup signal measured at the output of the detection block

The sensitivity of the wake-up receiver has been measured in the MO and ID modes with a 915 MHz OOK-modulated signal. As mentioned earlier, the BER test is performed using an Agilent E4438C ESG Vector Signal Generator with an internally generated PN23 pseudo-random pattern. The test setup for BER measurement of the wakeup receiver has been shown in Fig. 5.9.

Unlike the wakeup test that is only performed for the two data rates of 10 kbps and 200 kbps during MO and ID modes, the BER measurement includes different data rates and input power in order to find the sensitivity at a BER of 10^{-3}. Plots of the measured BER vs. sensitivity during the MO and ID modes are shown in Fig. 5.10a and Fig. 5.10.b, respectively. Based on the measured results, the sensitivity is about -75 dBm for a data rate of 200 kbps during the ID mode and -78.5 dBm for a data rate of 10 kbps during the MO mode.

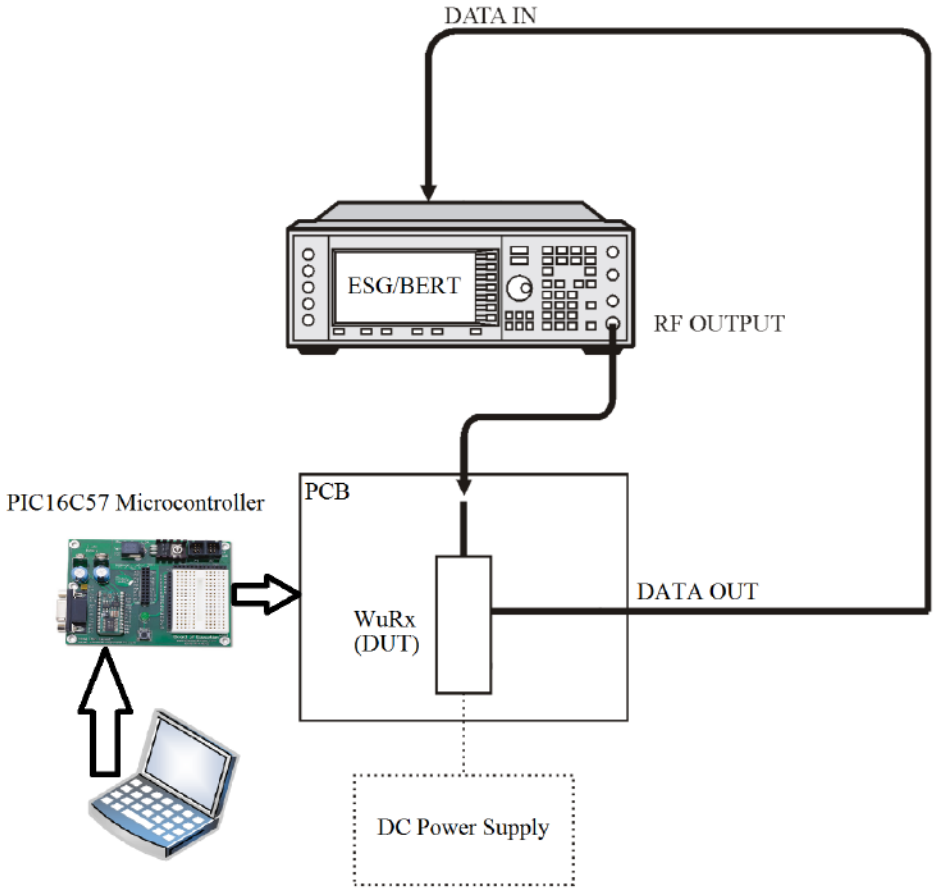


Fig. 5.9: Test setup for BER measurement of the wakeup receiver

It should be noted that employing the large PN23 pseudo-random pattern for an accurate measurement of the BER would take some time for performing the complete test. This may increase the probability of a change in temperature and hence the VCO frequency. Thus, the VCO and the IF signal have been continuously examined and the VCO frequency is manually adjusted either by slightly varying the analog supply voltage or recalibration of the VCO whenever a frequency deviation is observed. Therefore, a given test have been repeated in some cases.

However, this has not been the issue when measuring the gain and NF of the receiver as the temperature and other environmental parameters do not vary abruptly over the duration of a given measurement.

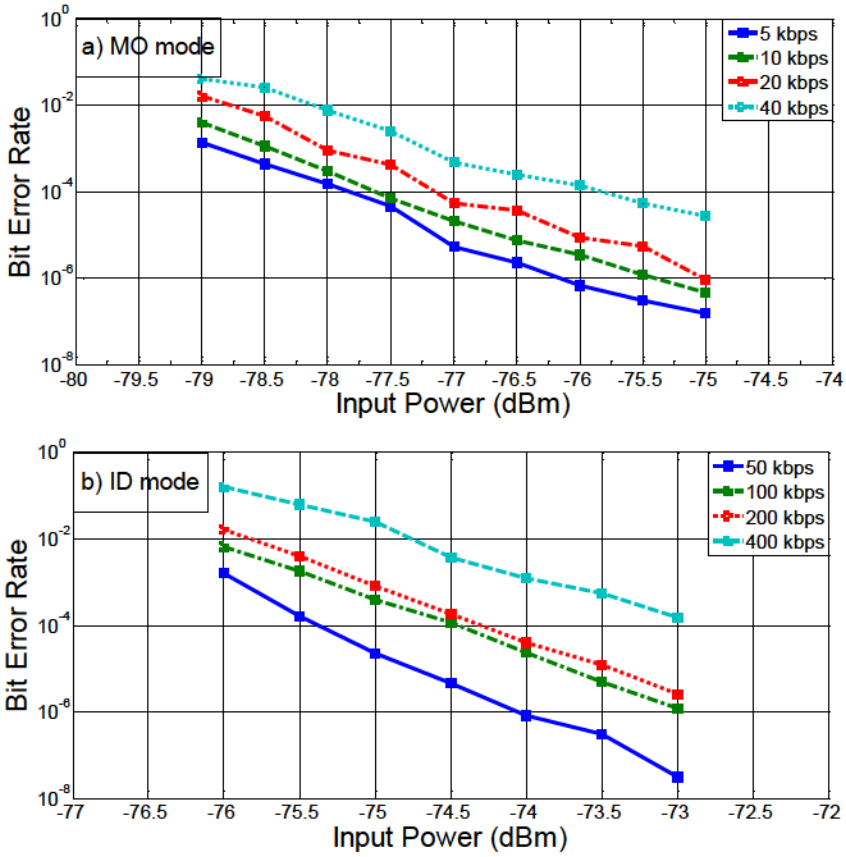


Fig. 5.10: Measured BER vs. sensitivity of the wake-up receiver during the a) MO and b) ID mode

We would also like to study the effect of RF modulation frequency on the sensitivity in order to find the bandwidth for which the receiver sensitivity is better than -70 dBm. Shown in Fig. 5.11, the sensitivity points are obtained by measuring the minimum input power to the receiver which yields the BER of 0.1% for a

frequency range of 900 MHz to 930 MHz. This test has been done for both MO and ID modes for a data rate of 10 kbps and 200 kbps, respectively.

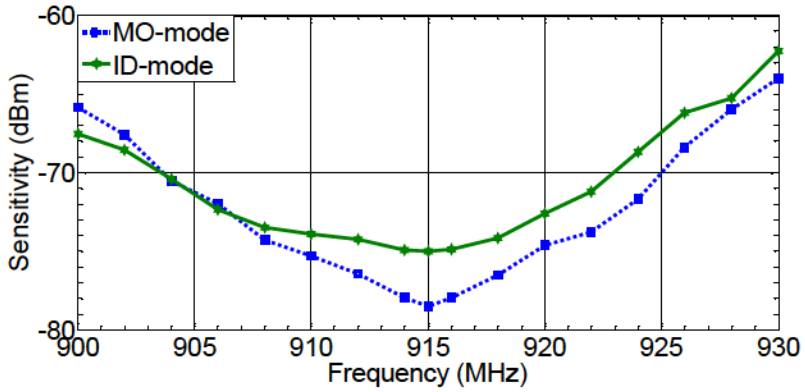


Fig. 5.11: Measured sensitivity bandwidth during MO and ID modes

Chapter 6

Conclusion and Future Works

6.1 Conclusion

The goal of this thesis was to employ the available receiver architectures and techniques to present a new topology for wake-up receivers. These wakeup receives can be potentially used in wireless sensor networks and mainly for indoor biomedical and body area network applications.

By combining the subsampling and the Tuned Radio Frequency (TRF) receiver topologies as a first approach, the total power consumption of wake-up receivers was successfully lowered while maintaining the sensitivity at a moderate range for indoor wireless channel applications. According to the extracted post-layout simulation results, the proposed WuRx draws 56 μA from a 0.5 V supply and has a sensitivity of -70 dBm. It occupies an area of 0.15 mm^2 in the TSMC 90nm CMOS technology.

Another ultra-low-power WuRx was also proposed based on our previously designed subsampling-receiver topology in order to reduce the energy consumption through adoption of two wake-up modes of operation with different power dissipations and detection bandwidths. During the Monitoring (MO) mode, the start frame bits are received at a data rate of 10 kbps, while during the Identifier (ID) mode the remaining wake-up pattern is transmitted at 200 kbps. By lowering the gain of the front-end amplifier in the MO mode the power dissipation is reduced, which in turn causes an increase in the overall noise figure of the receiver. However, adequate sensitivity is maintained by intentionally lowering the data rate as well as the detection bandwidth of the receiver. The proposed wake-up receiver was

designed and fabricated in IBM 130 nm technology with a core size of about 0.2 mm^2 for the target frequency range of 902-928 MHz. The measured results showed that the proposed dual-mode receiver achieves a sensitivity of -78.5 dBm and -75 dBm while dissipating an average power of 16.4 µW and 22.9 µW during MO and ID modes, respectively.

6.2 Future Works

Clearly, our implemented wakeup receiver has several impairments that should be addressed and improved in the future. One of the most critical issues of this design is that only regular I/O pads has been employed in the layout of the chip without any on-chip ESD protection. Instead, off-chip ESD protection ICs are soldered on the PCB. As a result, we ended up having very sensitive packaged chips that must be handled with extra care before they are soldered on the PCB for measurements.

Due to the above issue, only two out of five packaged chips successfully passed the preliminary test plan as discussed in the previous chapter. However, later, only one of the chips could pass all the measurement steps including the wakeup and BER tests. Therefore, one of the most crucial amendments to the existing wakeup receiver chip is to include enough ESD protection diodes in the layout to prevent the internal circuits from "blowing".

Aside from the above layout related issues, one can think of the following improvements as potential research works in this area.

6.2.1 LC Oscillator for VCO

Throughout the thesis, ring-oscillator based VCO has been preferred over the LC oscillator due to its lower power consumption and inherit small required area. However, the known disadvantages of the ring-oscillator including degraded phase noise and high frequency variation across PVT have created constraint for our

design, increased the noise bandwidth, and deteriorated the sensitivity of the receiver.

Unlike the ring-oscillator, the LC oscillator could potentially be a better option when it comes to its phase noise and jitter performance. By using the LC-based instead of a ring-oscillator based VCO for generating the sampling frequency in our receiver, the noise bandwidth be reduced and hence the overall sensitivity could be improved significantly. Although this would imply more dissipated power and may not be a perfect solution for a short-range ultra-low power design, but it may be an appealing alternative for longer-transmission channels where improving the sensitivity is more critical.

6.2.2 Dual-Tone Architecture

In spite of being immune to out-of-band interferes owing to the high-Q RF front-end filtering, the implemented wakeup receiver may still be susceptible to in-band interferes. A smart interference-rejection technique could be to transmit the signal on 2 RF carrier tones instead of only 1 tone [69]. Having received the two tones, the intermodulation signal will be generated by the squaring function of the envelope detector and can be downconverted to the baseband by a mixer.

Combining the above idea with our subsampling energy-efficient topology, one can try to build a wake-up receiver as hypothetically demonstrated in Fig. 6.1.

The two 2-tone carrier signal that are apart by Δf are initially down-converted to a IF-frequency using the T/H circuit at the front-end. The two down-converted differential signals are then converted to single-ended signals and get amplified prior to the envelope detection. The subsequent band-pass filter will then filter the intermodulation signal that is produced at the output of the envelope detector. A mixer can finally downconvert the frequency information at Δf to DC, where an on-chip detection circuitry will be used to demodulate the baseband data.

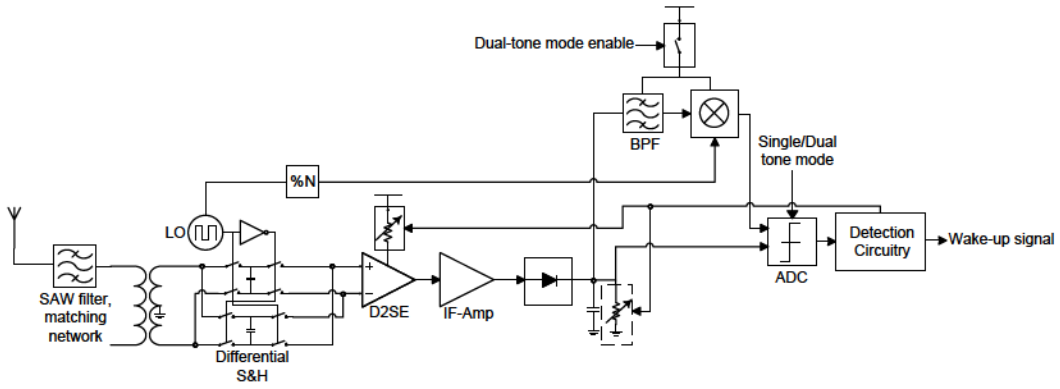


Fig. 6.1: Proposed single/dual-tone subsampling-based WuRx architecture

Least but not last, this work has opened a new prospective on ultra-low power wake-up receiver architecture, which can be combined with other novel design techniques for improved performance and to contribute to the area of WSN.

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