Design, Microfabrication, and Characterization of Polar III-Nitride HFETs

Alireza Loghmany

A Thesis

In the Department

of

Electrical and Computer Engineering

Presented in Partial Fulfillment of the Requirements

For the Degree of

Doctor of Philosophy (Electrical and Computer Engineering) at

Concordia University

Montreal, Quebec, Canada

June 2016

CONCORDIA UNIVERSITY
SCHOOL OF GRADUATE STUDIES

This is to certify that the thesis prepared

By: Alireza Loghmany

Entitled: Design, Microfabrication, and Characterization of Polar III-Nitride HFETs

and submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy (Electrical & Computer Engineering)

complies with the regulations of the University and meets the accepted standards with respect to originality and quality.

Signed by the final examining committee:

_____ Chair
Dr. N. Shiri

_____ External Examiner
Dr. Z. Mi

_____ External to Program
Dr. S. Narayanswamy

_____ Examiner
Dr. M.Z. Kabir

_____ Examiner
Dr. P. Pillay

_____ Thesis Supervisor
Dr. P. Valizadeh

Approved by: _____
Dr. W.-P. Zhu, Graduate Program Director

June 29, 2016 _____
Dr. A. Asif, Dean, Faculty of Engineering & Computer Science

ABSTRACT

Design, Microfabrication, and Characterization of Polar III-Nitride HFETs

Alireza Loghmany, Ph.D.

Concordia University, 2016

With excellent performance in high-frequency power amplifiers, AlGaN/GaN heterojunction field-effect transistors (HFETs) as next generation power amplifiers have drawn a great deal of attention in the last decade. These HFETs, however, are still quite limited by their inherently depletion-mode (D-mode: negative pinch-off voltage) nature, relatively poor gate-leakage, and questionable long-terms reliability. In addition, since AlGaN/GaN HFETs operate at extremely high-power densities, performance of these devices has so far remained quite limited by self-heating effects.

While a number of techniques have already been developed for realization of enhancement-mode (E-mode: positive pinch-off voltage) AlGaN/GaN HFETs, these techniques in addition to having a number of difficulties in achieving enhancement-/depletion-mode pairs, fall short of satisfying requirements such as low leakage-current, drain-current stability, and pinch-off voltage stability at the high operating temperatures and at elevated electric-fields. Among these techniques, fluoride-based plasma treatment is the most widely accepted. As an alternative to this mainstream technique, polarization-engineering of AlGaN/GaN HFETs through exploring the impacts of the mesa geometry is studied as a possible avenue for selective transformation of the D-mode nature of AlGaN/GaN HFETs to an E-mode character. Whereas limited experimental studies on the pinch-off voltage of HFETs realized on different isolation-feature geometries have indicated the presence of a certain correlation between the two, such observations lack the required depth to accurately identify the true culprit. This technique is expected to be ultimately capable of producing enhancement-/depletion-mode pairs without adding any extra steps to the microfabrication process.

In light of this requirement, microfabrication of AlGaN/GaN HFETs using a number of alternative isolation-feature geometries is explored in this study. In addition to developing an in-house microfabrication process, transistors designed according to these novel isolation-feature geometries have been fabricated through the services offered by Canadian Microelectronics

Corporation (CMC). Investigation of the variation of pinch-off voltage among the devices fabricated through this latter means has conclusively indicated that the pinch-off voltage shift, rather than exclusively being caused by the surrounding-field effect, is also correlated to the perimeter-to-area ratio of the isolation-features.

In addition, through characterization and thermal modeling of these groups of devices, in this study a new approach is unveiled for reducing self-heating in AlGaN/GaN HFETs. According to finite element analysis (FEA) and electrical measurement of average channel temperature, an improved heat-dissipation was observed in HFETs enjoying a more distributed nature of the two-dimensional electron gas (2DEG) channel. This is observed to be the case especially for isolation features which offered the center of the channel a smaller distance to the side walls. Observations also indicate a more distinct gain in thermal management with reduction of the gate-length and also the surface area of the isolation pattern. Results suggest that self-heating in AlGaN/GaN HFETs can be substantially nullified by reducing the island-width below a certain threshold value, while maintaining the total width of the transistor constant.

In addition to exploring these alternatives on AlGaN/GaN HFET structures, in-house microfabrication of AlN/GaN MISFETs is also studied. The results of DC characterization of these novel transistors are also presented.

Acknowledgment

Foremost, I would like to express my sincere gratitude to my advisor Dr. Pouya Valizadeh for the continuous constructive supervision, for his patience, motivation, enthusiasm, and enduring support during the course of my studies. I would also like to thank my thesis committee members for all of their guidance through this process; your discussion, ideas, and feedback have been absolutely invaluable.

I am also indeed deeply grateful to my father for his unconditional and ongoing support which has given me hope and courage to pursue my personal dreams and professional goals throughout my life. I would also like to thank my amazing wife and son for the love, support, and constant encouragement I have got over the years.

Finally, I would like to dedicate this thesis to my mother. Although it has been years since you have passed, I still take your lessons with me, every day.

All the devices used in the experimental part of this research reported in chapters 3-5 were fabricated by Canadian Microelectronics Corporation (CMC).

This research work was financially supported by the NSERC discovery grant program.

Contents

List of Figures

List of Tables

List of Symbols

Symbol	Description	Unit
a	Edge length of basal hexagon	m
b	Bond length	m
c	Height of the hexagonal prism	m
E_A	Energy level of the responsible trap-site	eV
ε_r	Relative dielectric constant	-
I_D	Drain current	A
K_B	Boltzmann constant	J/K
L_g	Gate length	m
$q\Phi_M$	Metal work-function	eV
R_0	Contact resistance	Ω
R_{DS}	Output resistance	Ω
R_{sh}	Sheet resistance	Ω/□
R_t	Transfer resistance	Ω.mm
T	Temperature	K
V_{DS}	Drain-source voltage	V
V_{GS}	Gate-source voltage	V
V_p	Pinch-off voltage	V
W	Effective gate width	m
ρ_c	Specific contact resistance	$\Omega.cm^2$
τ	Trapping/de-trapping time constant	sec
τ_0	Proportionality constant	-

List of Abbreviations

Abbreviation	Description
2DEG	Two-dimensional electron gas
AFM	Atomic force microscopy
DBS	Direct broadcasting satellite
DCTL	Direct-connected transistor logic
DLTS	Deep-level transient spectroscopy
D-mode	Depletion-mode
ECR	Electron cyclotron resonance
E-mode	Enhancement-mode
FEA	Finite element analysis
FET	Field effect transistor
HCP	Hexagonal close packed
HFET	Heterostructure field effect transistor
HVPE	Hydride vapor phase epitaxy
ICP	Inductively coupled plasma
MBE	Molecular beam epitaxy
MERIE	Magnetically-enhanced reactive ion etching
MESFET	Metal semiconductor field effect transistors
MISFET	Metal insulator semiconductor field effect transistors
MOCVD	Metal organic chemical vapor deposition
MOVPE	Metal organic vapor phase epitaxy
MRIE	Magnetron reactive ion etching
PAE	Power added efficiency
RF	Radio frequency
RTA	Rapid thermal annealing
TD	Threading dislocations

TEM	Transmission electron microscopy
TLM	Transmission line method

Chapter 1

Introduction

1.1 Research background

As the demand for high-frequency amplifiers offering higher power amplification is growing both in civilian and military applications, researchers are scrambling for new wide bandgap semiconductor technologies to satisfy these needs. Multitude of technologies (i.e., GaAs, AlAs, GaP, InP, SiC, GaN, etc.) are competing for this market [1].

Among the aforementioned technologies, nitrides of group III of periodic table (i.e., III-nitrides: GaN, InN, AlN, and their alloys) due to their good transport properties, and ability to form high electron concentration polar heterostructures, are deemed most suitable to satisfy these market demands. Considering the room temperature bandgaps of 0.7 eV for InN [2], 3.4 eV for GaN, and 6.2 eV for AlN [3], III-nitride alloys can cover a very broad range of bandgaps. This widely tunable bandgap is an asset in realization of different forms of band bending. Such a property naturally yields the possibility of tuning the electron concentration at the heterostructures realized in the III-nitride system.

Among III-nitrides, GaN is the most studied semiconductor as the channel of power amplifier field effect transistors (FETs). Transistors that take advantage of GaN as their channel offer five key characteristics: high breakdown field, high operating temperature, high current density, high-speed switching, and low on-resistance. In Figure 1.1, operating temperature,

breakdown filed, oscillation frequency, noise factor, and maximum current density of GaN-based heterostructure field-effect transistors (HFETs) are compared to those of transistors fabricated in two competing FET technologies [4]. Such a comparison clearly highlights the suitability of GaN channels, and generally speaking III-nitride heterostructures, for high-power, high-frequency, and high-temperature power amplification applications. To this list we can also add the radiation-hardness of this material system, which makes it suitable for extra-terrestrial applications. The radiation hardness is an outcome of the large bond-strength in most of the members of III-nitride family. Such advantages are also extended to high-voltage switches operating in high-temperature environments.

These advantages are certainly accompanied by a number of challenges. The large bond-strength and high melting-temperature of most III-nitrides impose tremendous challenges on both production of native substrates (for example GaN) and development of damage-less etching recipes for selective material removal. Although, on the etching front an ongoing research has so far resulted in a number of guidelines to minimize the damage of physical etch on the etched semiconductor surfaces, on the substrate production front, affordable native substrates of sufficiently large sizes are still to be found. Lack of affordable native substrates and lattice mismatch between GaN and the most suitable of presently available substrates (i.e., in the order of performance merit: SiC, Sapphire, and Si) has resulted in persistence of threading and screw dislocations throughout the heterostructures grown in the III-nitride material system. The resulting surface states have been observed to be especially damaging to the performance of the devices built on these structures.

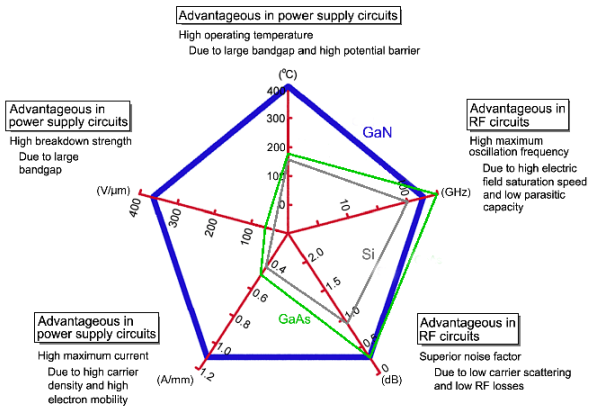


Figure 1.1 Comparison of breakdown field, maximum oscillation frequency, noise factor, maximum current density, and operating temperature of GaN-, GaAs-, and Si-based FETs [4].

HFETs, which are transistors incorporating at least one junction between two materials with different bandgaps, are now widely used in civilian and military telecommunication applications. The existing band-bending at the heterointerface of these two materials provides the ability to achieve a high carrier-concentration channel with little or no overlap between the carrier wave-function and the dopants. A channel realized in this fashion enjoys a diminished ionized impurity scattering, and as a result an improved carrier mobility. Formation of an almost triangular quantum well and confinement of the carriers at the smaller bandgap side of the heterointerface gives a two dimensional character to channel electrons of these heterointerfaces. As a result, electron population of these channels is referred to as two-dimensional electron gas (2DEG). The heterostructures described here are referred to as type-I heterostructures. The wider bandgap semiconductor in such a heterostructure is known as the barrier-layer.

In contrast to AlGaAs/GaAs HFETs where a doped AlGaAs layer (i.e., barrier) is needed to create the 2DEG, AlGaN/GaN HFETs enjoy a widely different source of channel electrons. In these devices existence of a strong polarization at the heterointerface is the root cause for the induction of the channel's 2DEG. Even in absence of intentional barrier doping, this mechanism yields an electron concentration which is about an order of magnitude higher than other heterointerfaces [5] - [6]. The first AlGaN/GaN HFET was demonstrated by Khan *et al.* in 1994 [7]. Figure 1.2 shows a typical device structure of a two-finger AlGaN/GaN HFET. Several variations to this technology such as implementation of recessed gate [8], incorporation of zero strain AlInN barriers [9], implementation of InGaN and AlGaN back barriers [10] - [11], and use of ion implantation in Ohmic contact and device isolation [12] - [13] have been explored over the years to improve RF performance of GaN-channel HFETs. In addition to these studies, study of AlN/GaN MISFETs presents itself as attractive avenue for exploring high speed and high power limits of GaN-channel HFETs. The wider barrier bandgap of these structures and the larger piezoelectric and spontaneous polarizations are expected to yield even more interesting results in terms of tunability of pinch-off voltage, maximum drain-current density, breakdown voltage, gate-leakage current, and performance stability.

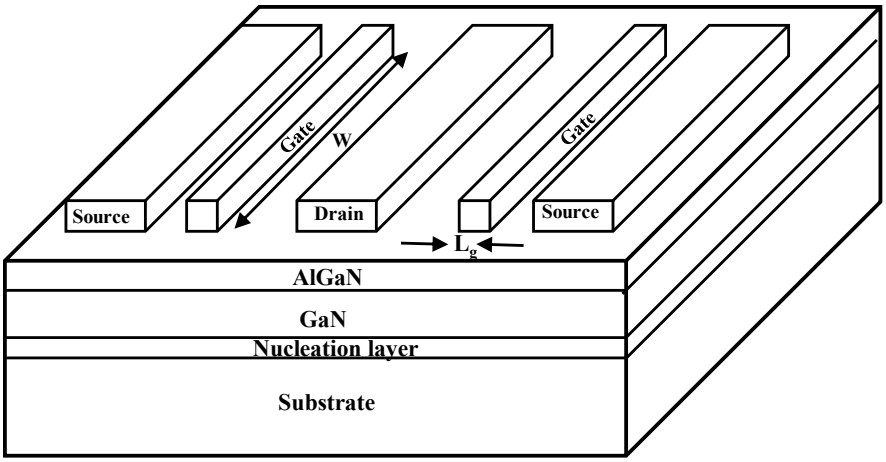


Figure 1.2 Typical device structure of a two-finger AlGaN/GaN HFET. L_g is the gate length and 2W is the gate width of the HFET.

In spite of many enticing advantages, AlGaN/GaN HFET technology has been proven challenging towards realization of enhancement-mode transistors. Normally, these HFETs due to their vastly superior polarization-induced 2DEG concentrations manifest negative pinch-off voltages (i.e., depletion-mode), which is quite unyielding to the ordinary techniques of realization of enhancement-mode HFET employed in other HFET technologies. The depletion mode of operation, for a large number of both digital and analog applications presents an inferior operation compared to the enhancement-mode. While a number of techniques have already been developed for realization of enhancement-mode AlGaN/GaN HFETs, these techniques in addition to having a number of difficulties in achieving enhancement-/depletion-mode pairs, fall short of satisfying requirements such as low leakage-current, drain-current stability, and pinch-off voltage stability at the high operating temperature and electric-fields. Among these techniques, fluoride-based plasma treatment is the most widely accepted [14].

1.2 Research motivation

1.2.1 Motivations of the study of alternative isolation-feature geometries of polar AlGaN/GaN HFETs

As an alternative to the mainstream techniques so far employed in realization of E-mode AlGaN/GaN HFETs, polarization-engineering of AlGaN/GaN HFETs through mesa geometry

has been studied as a possible avenue for selective transformation of the depletion-mode nature of AlGaN/GaN HFETs to an enhancement-mode character. This technique has positively demonstrated potential for realization of enhancement-/depletion-mode pairs without adding any extra steps to the microfabrication process.

Limited experimental studies on the pinch-off voltage of HFETs realized on different isolation-feature geometries have indicated the presence of a certain correlation between the geometry and the pinch-off voltage. A possible cause for these observations is deemed to be the evolution of peel-forces around the boundaries of isolation feature and the dependence of this evolution on the boundary's curvature. Evolution of these forces at the boundaries is expected to yield an avenue towards engineering the strain (hence, piezoelectric polarization) and as a result pinch-off voltage of polar AlGaN/GaN HFETs. Nonetheless, due to presence of differences among the surrounding field-effects imposed on the 2DEG channel of the devices built on these isolation features, so far such observations have remained inconclusive. Whereas only a limited body of experimental and theoretical work exists on comparing these two causes of pinch-off voltage dependence on the isolation-feature size and geometry [15] - [17], a more detailed look on the matter is deemed necessary.

Shedding light on the principle contributor to this phenomenon can potentially open a new avenue to microfabrication of polar HFETs (i.e., in III-nitride family as well as polar heterostructures realized on semiconductors such as ZnO). Such a fabrication opportunity is expected to yield the possibility to realize both E- and D-mode HFET side by side one another, which is essential to commercialization of the III-nitride technology.

In order to distinguish between the impacts of peel-forces (developed around the boundaries of the isolation-feature) and the surrounding-field effect, in this study a number of mesa geometries among which the perimeter-to-area ratio of the isolation-features are different while the lateral proximity of the gate electrode to channel is kept intact, are proposed. Due to novelty of these technological variations, studying the stability in operation is deemed essential.

Another motivation in the study of isolation-feature geometries other than the usual cubic mesas is to assess the validity of this design avenue in improving the heat exchange and lowering the self-heating concerns of high power AlGaN/GaN HFETs. AlGaN/GaN HFETs normally operate at exceptionally high-power densities, therefore sizable self-heating negatively impacts

the reliability and power rating of these transistors. As a result, thermal management must be carefully considered to minimize the channel temperature and ensure reliable long-term device operation. In addition to the usual adoption of a more thermally conductive substrate such as SiC to remedy this problem, since power is predominantly dissipated in the very small region of the channel in the proximity of the drain-edge of the gate, thermal management via the surface of this hotspot is also deemed attractive. On the basis of this latter consideration (i.e., heat management at the surface instead of substrate), a seemingly promising heat-management strategy is based on the exploration of alternative geometries of isolation-features that offer improved surface areas for heat exchange.

1.2.2 Motivation of the study and fabrication of polar AlN/GaN MISFETs

After the demonstration of the first AlGaN/GaN HFET in 1994 [7], in addition to exploring AlGaN barriers with different thicknesses, and Al compositions, several alternative barrier designs, including AlN [18] - [21], lattice matched InAlN [22] - [24], and quaternary InAlGaN [25] - [26] have been employed to improve the performance and reliability of GaN-channel HFETs. Among the aforementioned alternative barriers, AlN presents the largest bandgap and polarization discontinuity at the barrier to channel heterointerface. Assuming a thick enough barrier, these properties are invaluable towards securing unprecedented high 2DEG concentration, high drain-current density, high breakdown voltage, low gate leakage current, and diminished deterioration by the hot carrier effects under normal operating conditions. In spite of these advantages, AlN/GaN metal-insulator-semiconductor field-effect transistors (MISFETs) have been seldom studied [27] - [28].

In spite of the enticing anticipations, the large lattice mismatch between AlN and GaN (hence, the chance for forming cracks during the growth process of the epilayer), has so far limited the thickness of realizable barriers in these MISFETs. This limitation, from a device perspective, contributes to lower channel population, lower drain-current density, larger gate-leakage, smaller breakdown voltage, less reliable resistance to hot-carriers, and inferior frequency response than anticipated.

In light of improvements in crystal growth capabilities, barrier thicknesses in the range of 10 nm have been recently made possible (i.e., about twice as much as the values previously reported). An ongoing research is being pursued across the globe to develop and tune a proper recipe for microfabrication of AlN/GaN MISFETs of these larger barrier thicknesses, which constitutes one of main thrusts of the present work.

1.3 Proposed research objectives and framework

According to the discussions of section 1.2, the objectives of this PhD research are defined according to the present challenges of the cutting edge technology of III-nitride HFETs. The research objectives are categorized as follows,

- To develop a conclusive assessment on the possibility of evolution of peel force around the boundaries of isolation-features etched into the epilayer, and evaluation of its likely contribution to modifying the pinch-off voltage of HFETs realized on these features.
- To develop a conclusive assessment on the possibility of heat exchange at the boundaries of isolation-features etched into the epilayer, and evaluation of its likely contribution to modifying the self-heating of HFETs realized on these features.
- To develop in-house recipes for realization of HFETs and MISFETs in III-nitride technology to be used in future explorations in this material system.

To achieve the aforementioned objectives, the following research tasks were planned,

Task 1: Exploring alternative isolation-feature geometries for polarization-engineering of polar AlGaN/GaN HFETs:

1.1 Designing the mask layout for polar AlGaN/GaN HFETs of alternative isolation-feature geometries. These devices were fabricated through CMC.

1.2 Experimental investigation of the DC characteristics of AlGaN/GaN HFETs of alternative isolation-feature geometries.

1.3 Experimental investigation of performance stability (i.e., current collapse, gate leakage, stressed degradation) of HFETs of alternative isolation-feature geometries.

Task 2: Study of the dependence of self-heating on isolation-feature geometry among polar AlGaN/GaN HFETs designed under task 1:

2.1 Studying the pulse-mode DC characteristics of AlGaN/GaN HFETs of alternative isolation-feature geometries and characterizing the channel temperature according to these measurements.

2.2 Developing an ANSYS model for assessing the heat exchange among the experimentally explored devices under task 2.1 and on the basis of which project a guideline for effective elimination of self-heating in AlGaN/GaN HFETs.

Task 3: Process recipe development for microfabrication of AlGaN/GaN HFETs:

3.1 Microfabrication and process optimization of AlGaN/GaN HFETs (at McGill University's microfabrication facilities).

3.2 Experimental investigation of the DC characteristics and stability in performance of in-house microfabricated AlGaN/GaN HFETs.

Task 4: Process recipe development for microfabrication of AlN/GaN MISFETs:

4.1 Microfabrication and process optimization of AlN/GaN MISFETs (at McGill University's microfabrication facilities).

4.2 Experimental investigation of the DC characteristics and stability in performance of in-house microfabricated AlN/GaN MISFETs.

1.4 Outline of this work

This thesis is organized into seven chapters. Following the introduction (chapter 1), literature review related to III-nitride material system, AlGaN/GaN HFETs, AlN/GaN MISFETs, and reliability and degradation issues in AlGaN/GaN HFETs are presented in chapter 2.

Chapter 3 presents the impact of isolation-feature geometry on self-heating of AlGaN/GaN HFETs.

Chapter 4 is dedicated to alternative isolation-feature geometries and polarization-engineering of polar AlGaN/GaN HFETs.

Reliability studies of AlGaN/GaN HFETs of alternative isolation-feature geometries are presented in chapter 5.

Chapter 6 presents microfabrication process of AlGaN/GaN HFETs and AlN/GaN MISFETs.

Chapter 7 is devoted to concluding remarks, contributions of this thesis, and future work suggestions.

1.5 List of publications

The research work of this thesis has so far resulted in the following peer-reviewed journal publications,

1. A. Loghmany, P. Valizadeh, and J. Record, "Impact of isolation-feature geometry on self-heating of AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 61, no.9, pp. 3152-3158, Sept. 2014.

2. A. Loghmany and P. Valizadeh, "Alternative isolation-feature geometries and pinch-off voltage variation in polar AlGaN/GaN HFETs," *J. Solid State Electron.*, vol. 103, pp. 162-166, Jan. 2015.

Chapter 2

Literature review

2.1 III-nitride material system

The III-nitride family of semiconductors consisting of InN, GaN, AlN and their ternary and quaternary alloys has found a wide range of electronic and optoelectronic device applications over the last two decades. Widely tunable direct bandgap, high thermal and mechanical stability, and excellent electro-optical properties of III-nitride semiconductors have enabled a number of devices in this technology which are not normally feasible otherwise.

2.1.1 Crystal structures of III-nitrides

There are three common crystal structures shared by the group III-nitrides: wurtzite hexagonal close packed (HCP), cubic zinc-blende, and rocksalt [29]. These crystal structures are shown in Figure 2.1. The equilibrium crystal structure of III-nitrides is that of wurtzite for bulk AlN and GaN [30]. The zinc-blende structure has a cubic unit cell, containing four group III and four nitrogen atoms. This structure can be stabilized via epitaxial growth of thin films on cubic substrates such as Si, MgO and GaAs [30]. In these cases, the intrinsic tendency to form the wurtzite structure is overcome by the topological compatibility. The rocksalt structure cannot be stabilized through the epitaxial growth and is only produced at extreme pressures [29].

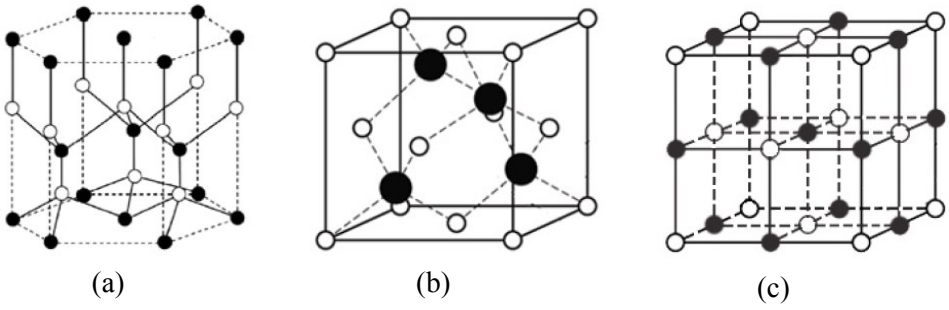


Figure 2.1 Crystal structure of: (a) wurtzite, (b) zinc-blende, and (c) rocksalt.

The wurtzite crystal has a hexagonal unit cell and thus is characterized by two lattice parameters a (i.e., edge length of basal hexagon) and c (i.e., height of the hexagonal prism) as well as by the *u*-value (where *u*=b/c and b is the bond length). The wurtzite structure consists of two interpenetrating hcp sublattices, offset along the c-axis by $\frac{5}{8}^{\text{th}}$ of the cell height (i.e., 5c/8). Figure 2.2 demonstrates a GaN unit cell.

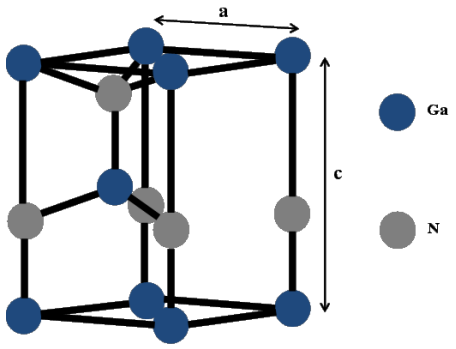


Figure 2.2 GaN unit cell.

2.1.2 Epitaxial growth of III-nitride semiconductors

First synthesis of III-nitride semiconductors (i.e., AlN) was reported by Fichter in 1907 [31]. Following that, in 1938, synthesis of GaN was reported by passing ammonia over hot gallium by Juza and Hahn [32]. However, due to the challenges in III-nitrides synthesis, research focused on GaAs and silicon while for many decades no significant progress was made on III-nitrides

growth. In 1969, growth of GaN thin films on sapphire with hydride vapor phase epitaxy (HVPE) was reported for the first time by Murusaka and Tietjen [33]. Shortly after, GaN growth was reported using metal organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE) in 1971 and 1976, respectively [34] - [35]. In the absence of good quality GaN substrates, investigation was led into several different substrates for epitaxial growth of GaN. Due to the large lattice mismatch, several methods have been adapted to optimize the nucleation and growth of GaN layers on these substrates [36] - [38]. Currently, the main technique for the growth of III-nitrides is metal organic vapor phase epitaxy (MOVPE) which is performed at temperatures around 1000 °C using a gas mixture of ammonia and hydrogen [39]. The growth at very high temperatures limits the available substrates to GaN single crystalline substrate, sapphire, SiC, and silicon [40]. GaN single crystalline substrate would be the ideal substrate as there would be no lattice mismatch and it would reduce the density of defects. Due to significant difference between the thermal expansion coefficient and the lattice constant between III-nitride epilayers and the substrates other than the native GaN, crystal defects in the form of threading dislocations are inevitable [41]. In 1986, the first growth of high-quality GaN layers was reported by Amano *et al.* by introduction of a low-temperature AlN nucleation layer [38]. However, even with nucleation layer, GaN on SiC and sapphire is plagued with a defect density in the range of 10^8 cm^{-2} to 10^{10} cm^{-2}.

Figure 2.3 presents two different atomic arrangements of GaN wurtzite structure. Depending on the growth technique and conditions, growth surface is terminated by either nitrogen atoms or gallium atoms. The gallium terminated surface is termed Ga-face and the nitrogen terminated surface is called the N-face. Ga-face and N-face correspond to planes normal to $[0001]$ and $[000\bar{1}]$ directions, respectively. The most common growth direction for III-nitrides is normal to {0001} plane (i.e., c-plane). GaN grown in MOCVD reactors on c-plane SiC or sapphire substrates results in crystals with Ga-face [42].

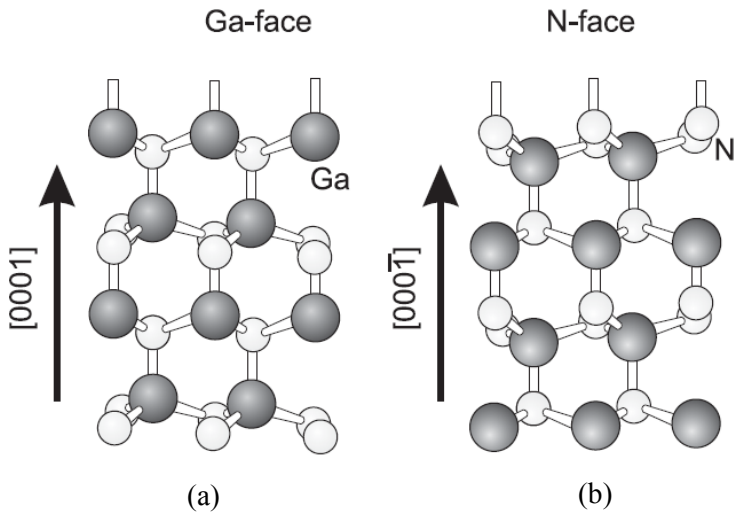


Figure 2.3 A stick-and-ball diagram of Ga-face (a) and N-face (b) GaN crystal structure [43].

In terms of processing and manufacturing, scaling up the wafer size is necessary to reduce the cost per die. While high quality Si substrate is available up to 12" in diameter, sapphire, SiC, and GaN are commercially available only to a maximum diameter of 6", 4", and 2", respectively [44]. Properties of the available substrates for III-nitrides epitaxy are presented in Table 2.1 [40]. Among these, SiC offers the best thermal conductivity, which makes it suitable for high power electronics. Relatively low thermal expansion coefficient mismatch with GaN offer the SiC substrate another advantage against other non-native substrates. In spite of these advantages, based on the lure of integration with Si electronics, enticingly larger wafer, and good thermal conductivity, Si is increasingly studied as an attractive substrate for GaN electronics.

Table 2.1
Properties of available substrates for III-nitride epitaxy [40].

Substrate	Thermal-Conductivity (W/m·K)	Electrical Resistivity	Cost, Wafer size
GaN	130	High	Very expensive, 2"
SiC	300-380	High	Expensive, 4"
Sapphire	50	High	Moderate cost, 6"
Silicon	100-150	Medium	Low cost, 12"

2.1.3 Material properties of III-nitrides

The large difference in electronegativity between nitrogen and group V elements results in very strong chemical bonds among III-nitrides. The strong chemical bonding of III-nitrides in turn results in radiation hardness, high melting temperature, and superb mechanical strength among these semiconductors. III-nitrides also enjoy high thermal conductivity. These properties make III-nitrides potential candidates for making of electronics intended for operation in harsh environment. Table 2.2 presents a short list of physical properties of GaN, AlN, InP, GaAs, and Si at room temperature [45].

Table 2.2
Physical properties of GaN, AlN, InP, GaAs, and Si at room temperature [45].

	GaN	AlN	InP	GaAs	Si
Bandgap energy (eV)	3.39	6.2	1.34	1.424	1.12
Lattice constant, a(Å)	3.160	3.112	5.868	5.653	5.431
Lattice constant, c(Å)	5.125	4.982	N/A	N/A	N/A
Electron affinity (eV)	4.1	0.6	4.38	4.07	4.05
Break down field (MV/cm)	5	1.8	0.45	0.4	0.3
Refractive index	2.29	8.5	3.1	3.3	3.42
Thermal conductivity (W/cm.K)	1.3	2.85	0.68	0.55	1.3
Melting point (°C)	2500	3023	1333	1240	1412
Relative dielectric constant, ε_r	8.9	9.14	12.4	12.5	11.7

2.1.4 Polarization effect in III-nitrides

The non-centro-symmetric nature of wurtzite structure in III-nitrides leads to the formation of a spontaneous polarization even in absence of external strain and/or electric-field. These crystals constitute of two hexagonal sublattices (i.e., cation and anion), the non-overlapping charge-center of which is the cause for aforementioned spontaneous polarization. In III-nitrides, asymmetry of inversion is present only along the c-axis. Hence, spontaneous polarization is parallel to the c-axis. Therefore c-plane III-nitrides are often called polar III-nitride. The spontaneous polarization is defined by a vector pointing from a metal atom toward a nitrogen atom. Hence, the direction of the spontaneous polarization depends on the growth face [46].

In addition to the spontaneous polarization, a sizable piezoelectric polarization exists among the heterojunctions realized in this material system. This is due to the induction of strain through pseudomorphic growth of two lattice-mismatched crystals and the large values of piezoelectric coefficients among III-nitrides [46]. The built up of stress energy through

increasing the thickness of the pseudomorphically overgrown layer eventually triggers the relaxation of this material to its native lattice constant. As a result of this relaxation the thickness of the overgrown layer, especially in the case of growth under tensile strain, is quite limited. Relaxation may occur in the form of delamination, generation of dislocations, cracking or a combination of these. When relaxation occurs, piezoelectric polarization becomes zero.

2.1.5 Polarization-induced two dimensional carrier concentration

Piezoelectric effect and the difference between spontaneous polarizations of the GaN channel- and the AlGaN barrier-layer, cause the formation of a sizable 2DEG at the AlGaN/GaN heterointerface. Figure 2.4 shows the spontaneous and piezoelectric polarization vectors in a Ga-face wurtzite AlGaN/GaN heterostructure [47]. Due to the dominant presence of these polarization vectors, these heterostructures are known as polar heterostructures. In this figure, the spontaneous polarization in each material is shown by the vector $\mathbf{P}_{sp}$ and the piezoelectric polarization in the tensile-strained AlGaN barrier is represented by the vector $\mathbf{P}_{pz}$. Since the thick GaN is assumed to be relaxed to its freestanding lattice constant, only the spontaneous polarization is present within this layer. Among III-nitrides, the value of the spontaneous polarization increases from GaN to InN, and to AlN [3]. As suggested by the directions of the polarization vectors demonstrated in Figure 2.4, a net positive charge should be induced at the bottom of the AlGaN barrier-layer. For the charge neutrality to be satisfied, a layer of negative charges (i.e., electrons) needs to be induced at the top of the GaN surface. These electrons form the 2DEG.

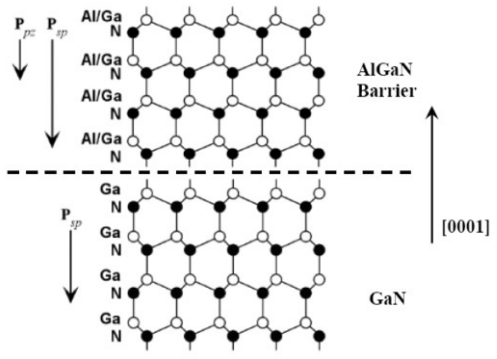


Figure 2.4 Spontaneous and piezoelectric polarization vectors in a metal-face wurtzite AlGaN/GaN heterostructure [47].

2.2 AlGaN/GaN heterojunction field effect transistors

HFETs as high frequency low noise amplifiers are now widely used as extremely low noise devices in telecommunications systems, space radio telescopes, active electronically scanned array radars, direct broadcasting satellite television (DBS) receivers, microwave and high power amplifiers, cellular phones, and car navigation receivers. These transistors take advantage of at least one type-I heterointerface formed between two materials of different bandgaps, where the wider bandgap material serves as the barrier against leaking of the almost two-dimensionally confined electrons accumulated on the small bandgap side of the heterointerface to the gate. Figure 2.5 presents a cross sectional view of a traditional AlGaAs/GaAs HFET. In this technology the carrier mobility of the 2DEG, formed at the vicinity of the heterointerface of the buffer- and the barrier-layer, is improved by resolving the ionized-impurity scattering problem through spatially separating the 2DEG from these scatterers. In these structures, ionized-impurity scattering can be further reduced through incorporation of a thin undoped spacer-layer between the barrier- and the buffer-layer at the cost of the reduction of gate-transconductance [48].

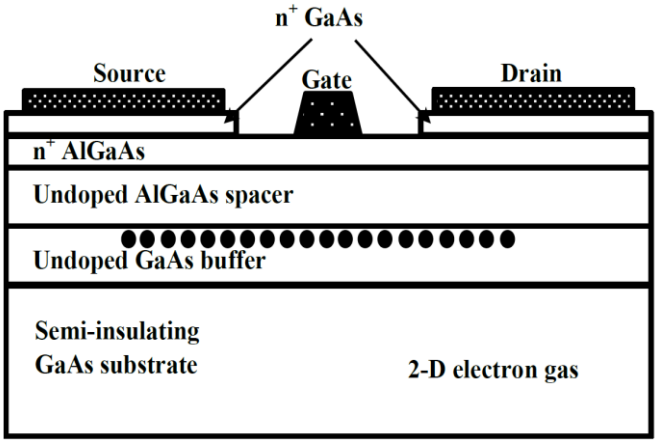


Figure 2.5 Cross sectional view of a traditional AlGaAs/GaAs HFET device structure.

Over the past two decades, AlGaN/GaN HFETs have demonstrated considerably larger output power and temperature tolerance compared to the AlGaAs/GaAs HFETs, which are among the primary candidates for high power applications. This is due to wider bandgap and the ability to achieve outstanding 2DEG densities on the polar AlGaN/GaN heterostructures without the need for intentional doping of the barrier-layer. The first AlGaN/GaN HFET with 0.25 μm gate length, current density of 60 mA/mm and maximum gate-transconductance of 27 mS/mm was demonstrated by Khan *et al.* in 1994 [7]. Material and processing improvements have now

yielded considerable improvements to these records. In terms of current density and maximum gate-transconductance values above 1 A/mm and 300 mS/mm, respectively, are readily available among devices of these dimensions.

Figure 2.6 demonstrates the typical layer structure of an AlGaN/GaN HFET. Not unlike AlGaAs/GaAs HFETs, in this structure there exists a potential well at the GaN side of the AlGaN/GaN heterointerface. This is due to the differences among the bandgaps and electron-affinities of the two materials forming the heterojunction. The presence of this quantum-well results in the formation of a 2DEG in the undoped GaN layer. Existence of strong polarization at the heterointerface of the AlGaN/GaN HFET causes an extra band-bending and reversal of the curvature of the barrier's conduction band-edge (i.e., in comparison to that of the AlGaAs), which leads to enhanced 2DEG concentration even when the AlGaN barrier-layer is undoped. Figure 2.7 offers a behavioral depiction of the conduction-band diagram of an AlGaN/GaN HFET.

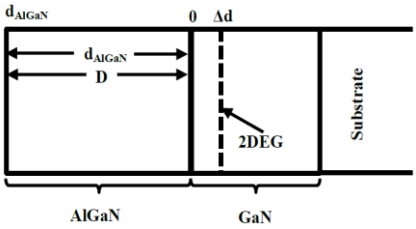


Figure 2.6 AlGaN/GaN HFET structure.

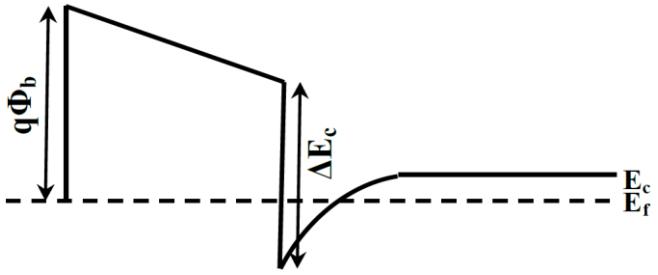
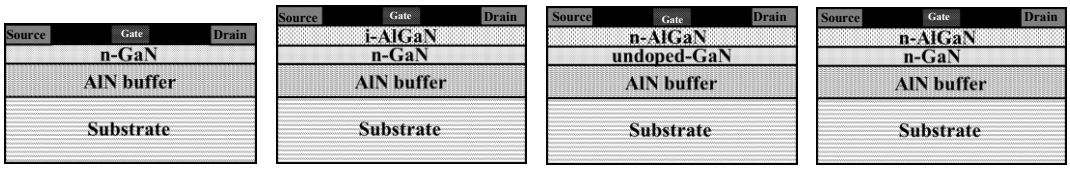


Figure 2.7 Conduction-band diagram of AlGaN/GaN HFET.

Figure 2.8 presents schematics of different GaN-based FETs including metal semiconductor field effect transistors (MESFETs), metal insulator semiconductor field effect transistors (MISFETs), AlGaN/GaN HFETs, and doped channel AlGaN/GaN HFETs (DC-HFETs).



(a) (b) (c) (d)

Figure 2.8 Schematic structure of different GaN-channel FETs: GaN MESFET (a), AlGaN/GaN MISFET (b), AlGaN/GaN HFET (c), and AlGaN/GaN DC-HFET (d).

Ohmic contact resistance (i.e., R_c) of 0.129 Ω.mm, minimum specific contact resistance (i.e., ρ_c) of 3.22×10^{-7} Ω.cm^2, drain current density of 1.6 A/mm, comprise some of major records established in AlGaN/GaN HFET technology [49]. Due to their high breakdown voltage, AlGaN/GaN HFETs can operate in range of biases that are not readily extendible to many other device technologies.

2.3 AlN/GaN metal-insulator-semiconductor field effect transistors

The growing demand for high power transistors capable of operating at higher frequencies has recently instigated an interest in AlN/GaN MISFETs realized on Ga-face wurtzite epilayers. Compared to AlGaN/GaN HFETs, these transistors are expected to yield higher breakdown voltage, higher drain current density, and better frequency response. These expectations are owing to a number of factors including the elimination of remote alloy scattering, very large bandgap of AlN, and the superior spontaneous polarization developed in this polar barrier. The superior polarization of these heterostructures is expected to yield a sizeable 2DEG concentration even when the barrier thickness is smaller than that of a traditional AlGaN/GaN HFET. This smaller barrier thickness is expected to allow a boost in gate-transconductance (and as a result in the frequency response). However, from the crystal growth perspective, sizeable lattice mismatch between AlN and GaN inhibits the realization of high-quality AlN layers on GaN, when the AlN thickness is beyond just a few nanometers. Despite the limited thickness of this barrier-layer, relative recent developments in the area of crystal growth (which has made the growth of about 10 nm thick AlN layer a reality) have raised the expectation for achieving 2DEG densities over 3×10^{13} cm^{-2}. These channels have been observed to enjoy a room-temperature mobility exceeding 1000 cm^2/V.s and low sheet resistance in the range of ~170 Ω/□ [28], [50].

Although AlN/GaN MISFETs are expected to offer higher 2DEG densities and larger breakdown fields, compared to the AlGaN/GaN HFETs they have been shown to suffer from more surface sensitivity, higher gate-leakage current, and higher Ohmic contact resistance. Among other improvements, further developments in realization of Ohmic contacts across the wide bandgap AlN barrier-layer is required to fully achieve the promised advantages of AlN/GaN MISFETs.

2.4 Reliability and degradation issues in AlGaN/GaN HFETs

Although the RF performance of III-nitride HFETs has quickly improved over the past few years, commercialization of this technology has stayed limited by the device reliability [51]. Among other things, operation under high electric-fields has been observed to result in hot electron-induced degradation in the peak transconductance and the saturation drain current. At high power levels, long terms exposure to RF signal (i.e., under the so-called RF stress) has been observed to create new traps within the epilayer and to manifest degradations in DC and RF performance. Also, due to the high power density of these transistors, self-heating has been observed to take a dominant position towards producing a negative output conductance. Degradation of RF performance expressed in terms of factors such as power added efficiency (PAE) and RF gain has been the topic of a large number of studies [52].

2.4.1 Electrical manifestations of performance degradation

Although remarkable progress has been made in recent years, AlGaN/GaN HFETs still suffer from problems such as drain current collapse, drain- and gate-lag, gate leakage, and leakage through substrate whose mechanisms are not well understood.

2.4.1.1 Drain current collapse

Observation of drain current collapse in AlGaN/GaN HFETs was first reported in 1994 [7]. Figure 2.9 demonstrates the current collapse phenomenon in AlGaN/GaN HFETs. Early reports indicated the correlation of these observations to the application of the RF signal to the gate

electrode. Under these test conditions the observed collapse in the dynamic value of the drain current and the output resistance have been shown to limit the RF output power of AlGaN/GaN HFETs to values much smaller than the predictions based on the DC characteristics [53]. In addition to these so-called transient observations, it has been shown that even under modest conditions of drain and gate bias the long term application of DC bias can semi-permanently increase the output resistance of an HFET (i.e., while its drain current drive undergoes a sizeable collapse compared to its value before stress) [54]. It has been speculated that the latter observations are due to injection of hot carriers from the channel either to the deep surface states in the high electric-field regions of the channel [54], deep trap levels within the AlGaN barrier-layer [53], or those present in the GaN buffer-layer [55] - [56]. In addition to these descriptions in terms of a phenomenon related to pre-exiting traps, researchers have described the current collapse mechanism of AlGaN/GaN HFETs via a number of alternative explanations. These explanations include: current collapse due to evolution of a gate bias-induced non-uniform strain [57], collapse due to presence of piezo-related charge states [58], and current slump caused by electron trapping in hot carrier-generated new trap sites [59].

Whereas until now the exact cause of current collapse among AlGaN/GaN HFETs is not known, upon improvements in the crystalline quality of the AlGaN/GaN epilayer and electrically passivating the surface traps a tangible reduction in both manifestations of current collapse and the resulting limitations of RF output power has been observed [60] - [61]. Some of these improvements are thanks to SiN surface passivation [62], incorporation of surface charge control cap layers [63], incorporation of field-plates [64], implementation of pre-passivation plasma treatment [65], and the implementation of deep recessed gate structures [66]. More recently, deposition of a polycrystalline AlN film as the passivation layer has been shown to be promising in eliminating the surface-related drain current collapse [67].

One of the manifestations of the transient performance degradation of AlGaN/GaN HFETs has been the dependence of the output resistance and gate-transconductance of these devices on the excitation frequency. Reduction in these metrics with the excitation frequency has been reported even when this frequency is in the range of a few megahertz.

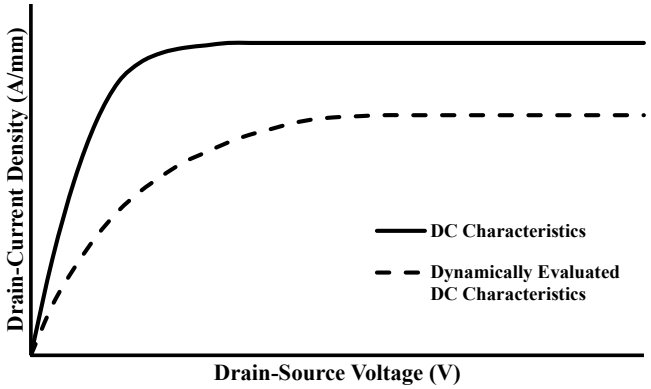


Figure 2.9 Current collapse phenomenon in AlGaN/GaN HFETs.

2.4.1.2 Drain- and gate-lag

In AlGaN/GaN HFETs, a slow current transient is often observed if the gate-voltage (or, the drain-voltage) changes abruptly. The observations of a time lag in the drain current's response to the abrupt variation of the drain and gate-voltage are often referred to as drain- and gate-lag, respectively. Gate-lag refers to the drain current transient in response to gate voltage pulses while drain-voltage is constant. Likewise, the drain-lag identifies with the drain current transient in response to a drain-voltage pulse when gate-voltage is constant.

It is commonly accepted that electron trapping in the shallow traps of the buffer is the cause of the drain lag [68], while trapping in the shallow states of the surface is accepted as the cause of the gate-lag [69]. In addition, there are some studies that suggest that shallow bulk defects in the GaN buffer may be also responsible for gate-lag [70]. Gate-lag due to electron trapping in the buffer is believed to be instigated by the hot electrons generated in the 2DEG [71]. Studies show a considerable reduction in the amount of gate-lag by post annealing of the gate and surface passivation [72].

2.4.1.3 Gate leakage

In spite of the promises of the wide bandgap of the barrier-layer of AlGaN/GaN HFETs for realization of a semi-insulated gate, the reported levels of gate leakage current among these devices are often quite disappointing.

While still a vigorous research on the origins of this higher than expected leakage current is being pursued, a number of explanations have been so far presented. Among these are: barrier-thinning caused by charged traps, trap- and defect-assisted tunneling, and hopping through dislocations [73] - [74]. According to these studies, existence of a distributed band of traps located within the AlGaN barrier acts as the facilitator in tunneling through the barrier [74]. Additionally, surface roughness has also been shown to have a major role in gate leakage [75]. Techniques such as surface passivation with Si_3N_4 [76], use of insulating SiO_2 [76], adopting a GaN cap layer [77], and implementing post gate anneal [78] have been all shown to be effective in reducing the gate leakage current in AlGaN/GaN HFETs.

2.4.1.4 Leakage through substrate

Lattice mismatch and differences in thermal expansion coefficients of epitaxially-grown III-nitride epilayers and the common substrates such as sapphire, Si, and SiC results in high defect densities within these epilayer. This is a limiting factor on the performance of AlGaN/GaN HFETs. The impacts of these imperfections are often observed in terms of unintentional doping of the buffer layer, which results in soft pinch-off and leakage through buffer. Transition metal doping is often used to change the conductive substrate into a semi-insulating substrate, which as a result yields a smaller leakage through the substrate [79].

2.4.2 Material origin

Maturity and manufacturability of the starting structure is a major challenge to the commercialization of AlGaN/GaN HFETs. This section lists the main phenomena related to material origins in this technology.

2.4.2.1 Uniformity

The uniformity of the starting structure is a critical factor for high yield and tighter device specification. Around 1,000 ºC susceptor temperature is needed for high quality AlGaN/GaN structure growth. Small fluctuation of the temperature during the growth leads to a significant

change in growth rate and compositional ratio of AlGaN layer, which leads to huge variations in device performance of the AlGaN/GaN HFETs, especially for larger size substrates. Temperature gradient inside the substrates degrades the flatness of the wafer and increases bowing of the wafer, which leads to loss of temperature uniformity on the wafer surface during the growth [80]. Thus, in order to achieve high uniformity on the wafers in MOVPE reactors, controlling of the heater and susceptor balance is one of the most crucial steps in the growth process. To further improve the manufacturability of the AlGaN/GaN HFETs, also developments in MOCVD reactor geometry have been made to ensure more streamlined gas flow in the chamber.

2.4.2.2 Crystalline defects

Crystal defects of various types (such as: point, line, and planar) have been observed in epitaxially grown pseudomorphic III-nitride heterostructures. A large point-defect concentration in the order of 10^{16} cm^{-3} is often observed in GaN layers grown on SiC or sapphire [81]. These point defects can be categorized into three basic categories: atoms missing from lattice sites (i.e., vacancies), anions sitting on cation sites or vice versa (i.e., anti-sites), and additional atoms in between the lattice sites (i.e., interstitials). The line defects are mainly threading dislocations (TD). In addition to point-defects, GaN layers contain a very high density of TDs in the range of 10^{8}-10^{10} cm^{-2} [82].

2.4.3 Metallurgy

Persistent performance degradation of electronic devices during operation, whether or not leading to device failure, constitutes a reliability concern. While some device degradations are only observable under RF measurement circumstances, the others persist even during DC evaluations. As a result, such degradations can have either a permanent or a transient nature. Among III-nitride HFETs such degradations include: pinch-off voltage walk-out, reduction in DC drain current, drooping RF gain/output power, and increasing gate leakage current. As the material quality and processing technology of AlGaN/GaN HFETs is improving, incorporation of a number of remedies to device design and microfabrication have already produced a tangible

improvement to some of the reliability concerns. One of these important remedies has been the incorporation of a passivation layer such as silicon-nitride on the exposed surfaces of the barrier-layer [53]. In spite of these improvements, there are still several metallurgy related reliability issues and degradation mechanisms which require attention. These metallurgy-related degradation mechanisms can be divided into three main categories: contact degradation, hot-electron effect, and inverse piezoelectric effect.

2.4.3.1 Contact degradation

Stable drain and source Ohmic contacts are important features in the operation of HFETs. Due to the high electric-fields generated in the vicinity of the gate, maintaining a thermally stable Schottky barrier is also a key concern in reliable device operation. Among AlGaN/GaN HFETs, both Ohmic and Schottky contacts have shown excellent stability below 290 °C. Degradation of the Ohmic contact has been observed under thermal storage after 2000 h at 290 °C and beyond. [83]. In this technology Ohmic contacts are often formed in the form of a stack of metal layers such as Ti/Al/Ti/Au, which through undergoing very high temperature rapid thermal annealing (RTA) produces an alloyed Ohmic contact to the 2DEG. The Schottky contacts are also formed in the form of a stack of metals such as Ni/Au.

Decrease of drain current and transconductance, increase of channel-on-resistance, and passivation cracking have been reported for thermal storage test stress at temperatures over 300 °C. These are due to Ga out-diffusion from the epilayers, Au inter-diffusion among the layers of the Ohmic metal stack, and the growth of Au-rich grains that eventually lead to crack formation in the passivation layer [84].

Among AlGaN/GaN HFETs an increase in the Schottky barrier height has been also observed for Schottky contacts exposed to DC stress at elevated junction temperatures [85]. This can be due to the consumption of Ni layer after the RTA, causing a positive shift in the Schottky barrier height and drain current degradation [86].

2.4.3.2 Hot electron-induced traps

It is widely known that hot electrons are one of the most important concerns for the reliable operation of FETs. Owing to the typical operation of AlGaN/GaN HFETs of sub-micrometer gates at very high drain voltages, these devices are often operating under extremely high electric-fields prone to hot electron generation. So far, for reducing the peak value of the electric-field and hence the hot electron-induced reliability concerns a number of features such as field-plate and recessed-gate have been adopted to the III-nitride technology [87]. Figure 2.10 presents cross sectional view of a device taking advantage of these features. The presence of these features serves to lower the peak electric-field on the drain side of the gate.

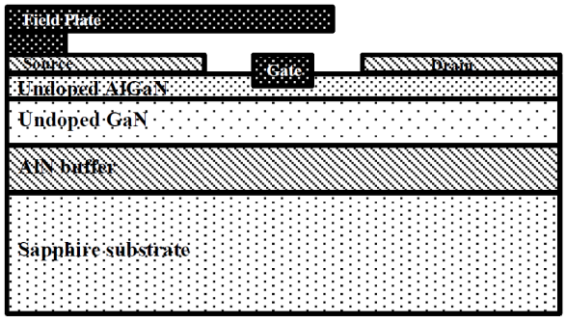


Figure 2.10 Cross sectional view of the AlGaN/GaN HFET taking advantage of source-connected field-plate and gate-recessed features.

Hot electrons are not only capable of surmounting the potential barriers confining the 2DEG (hence, contributing to the gate and the substrate current in addition to electron migration to the existing trap sites within the barrier), but are also capable of generating defects within the epilayer. Such defects can be formed at the interface between the passivation layer and the AlGaN barrier-layer, within the AlGaN barrier, or within the GaN buffer-layer. Electron trapping if the traps are of acceptor nature can induce a partial depletion of the 2DEG at their vicinity, and accordingly degradation in device characteristics such as output conductance and the drain-current drive. The observed degradation is sometimes reversible and the original condition can be restored via UV lighting or with unbiased room temperature storage [88].

2.4.3.3 Inverse piezoelectric effect

Relatively recently defect formation induced by the inverse piezoelectric effect has been revealed to be one of the main mechanisms of degradation among AlGaN/GaN HFETs exposed to off-state bias stress [88][1].

In an AlGaN/GaN HFET operating under large bias voltages, a large electric-field across the barrier-layer evolves at the drain edge of the gate. This electric-field can in turn induce a very large mechanical stress within this very small region. This mechanical stress has been observed to induce additional tensile strain across the AlGaN barrier-layer. Once the electric-field reaches a critical value, the AlGaN layer starts to relax through the formation of crystal defects (i.e., leading to performance degradation) [89]. In this case, removal of the bias does not allow the recovery of the device performance. Generation of deep traps in degraded devices has been confirmed by current-DLTS measurements [90]. Also, the formation of pit-shaped defects has been confirmed by TEM and AFM measurements. This type of degradation is characterized by a critical voltage, at which defect formation due to an increased electric-field occurs [91].

2.5 Conclusion

This chapter discussed the properties of III-nitride material system such as crystal structures, epitaxial growth of III-nitride semiconductors, material properties, polarization effect, and polarization-induced two dimensional carrier concentration. Device structures and current challenges facing AlGaN/GaN HFETs and AlN/GaN MISFETs were also explored.

[1] $V_{GS} = V_{GD} = -21$ V

Chapter 3

Impact of isolation-feature geometry on self-heating of AlGaN/GaN HFETs[2]

3.1 Introduction

In this chapter, the correlation between the geometry of the isolation feature and average channel temperature of biased AlGaN/GaN HFETs is investigated. In response to the growing demand for high-frequency amplifiers, offering higher power amplification, both in civilian and military applications, over the past two decades AlGaN/GaN HFETs have drawn a great deal of attention. Since AlGaN/GaN HFETs operate at exceptionally high-power densities, a sizable amount of self-heating negatively impacts the reliability and power rating of these transistors [92]. This is due to the fact that the elevation in the channel temperature leads to degradation in electrical transport properties of the channel, reduction in the effective Schottky barrier height of the gate, and strain relaxation of the barrier-to-channel heterointerface [92].

As a result of these drawbacks, thermal management must be carefully considered to minimize the channel temperature and ensure reliable long-term device operation. Self-heating in AlGaN/GaN HFETs has been well documented in [93] - [95]. Based on these studies, several remedies for reducing the channel temperature have been explored [96] - [98]. Since the presence of a considerable thermal boundary resistance at the interface with the buffer layer

[2] Most of the material presented in this chapter has been previously published: A. Loghmany, P. Valizadeh, and J. Record, "Impact of isolation-feature geometry on self-heating of AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 61, no. 9, pp. 3152-3158, Sept. 2014.

imposes a sizeable self-heating on the operation of AlGaN/GaN HFETs, these remedies are mostly based on incorporation of a high thermal-conductivity substrate [99]. However, since power is predominantly dissipated in the very small region of the channel in the proximity of the drain-edge of the gate, thermal management closer to this hotspot has also been targeted via incorporation of high thermal-conductivity passivation layers such as AlN to spread heat at the surface [67]. On the basis of this latter consideration (i.e., heat management at the surface instead of substrate), in this chapter, a promising heat-management strategy founded on exploring alternative geometries of isolation feature is presented.

3.2 Device structure and characteristics

The transistors used in the studies presented in this chapter were fabricated on an AlGaN/GaN HFET structure grown on a SiC substrate. The epitaxial structure was composed of a 20 nm $Al_{0.3}Ga_{0.7}N$ barrier, 1 nm AlN spacer layer, 200 nm unintentionally doped GaN channel layer, 2 μm GaN buffer layer, and 20 nm nucleation layer. The process followed a standard recipe for the fabrication of AlGaN/GaN HFETs. This recipe starts with the definition of isolation features of 300 nm height, using a chlorine-based reactive ion etching process. Following this step, Ohmic and gate contacts are formed. The unexposed surfaces are passivated by SiN.

According to this recipe, six categories of two-finger HFETs, with different isolation-feature geometries, were fabricated side-by-side one another. Figure 3.1 presents micrographs of these six categories of devices. Although traditionally HFETs are fabricated on cubic mesa-isolation features of lateral dimensions, the size of the gate-width, the six categories of devices reported here have alternative geometries resembling: 1) array of islands [which as shown in Figure 3.1(a) and (b) are simply small-size mesas]; 2) fins [which as shown in Figure 3.1(c) and (d) are simply narrow mesas]; 3) ladders [which as shown in Figure 3.1(e), the channel is formed on the steps of a ladder like structure]; or 4) combs [which as shown in Figure 3.1(f), the channel is formed on the teeth of a comb-like structure]. The difference between the two types of fin-isolated HFETs is in terms of the orientation of the fin versus the gate (i.e., one in parallel and one normal to the gate-finger). The two types of island-isolated HFETs differ in the size of each island.

Details of the dimensions of the isolation features are indicated in Figure 3.1. The total width of the transistors from any of the six categories is 98 μm. Since the 2DEG channel is formed only in those parts of the epitaxial layer which remain unetched upon the definition step of the isolation feature, the transistor width is calculated through multiplying the width of the island, fin, comb-tooth, and ladder-step by the number of these features intersecting a gate-finger. The minimum dimensions were limited by the foundry's constraints. Devices with two different values of gate-length (i.e., 1 and 0.5 μm) were designed and fabricated in each category. All fabricated devices[3] have a gate–drain spacing of 2 μm and gate–source spacing of 1.1 μm.

[3] All devices were fabricated by Canadian Microelectronics Corporation (CMC) with GaN500 process.

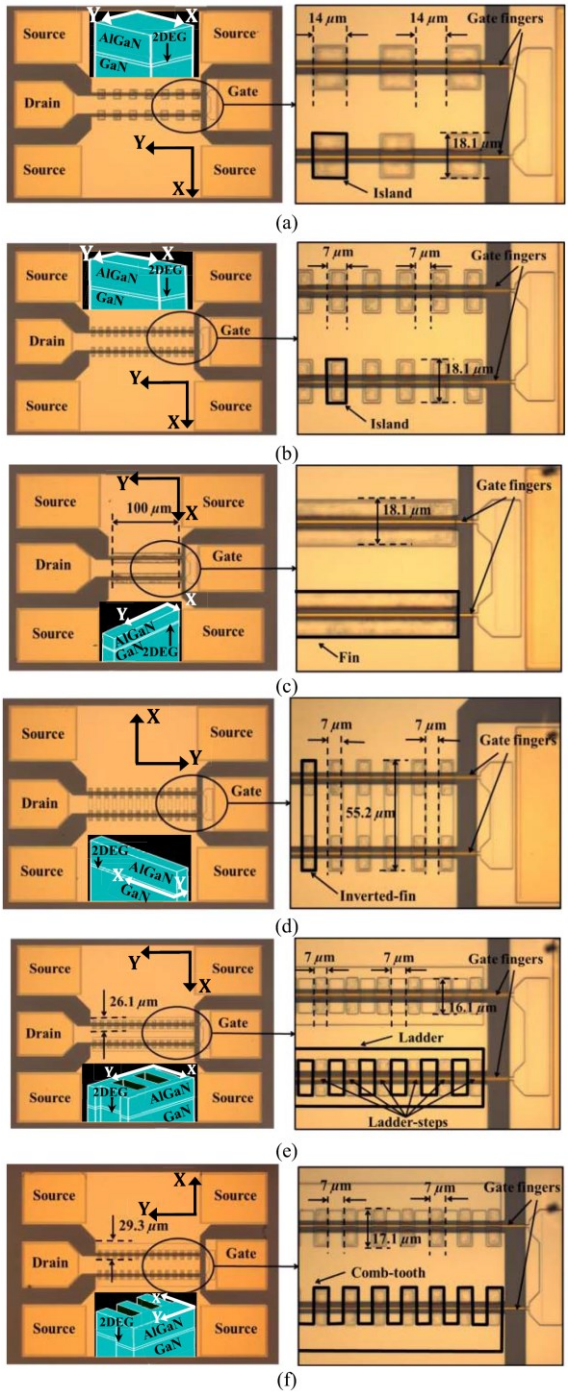


Figure 3.1 Micrographs of (a) seven-island island-isolated HFET, (b) 14-island island-isolated HFET, (c) fin-isolated HFET, (d) inverted-fin fin-isolated HFET, (e) ladder-isolated HFET, and (f) comb-isolated HFET. Gate-length, lengths of drain- and source-access regions are 1, 2, and 1.1 μm, respectively. Insets: 3-D schematic diagram representing a minimum set of isolation features. Panels on the right present a magnified view of each device in the area approximately indicated by the oval. On these magnified images, the highlighted boundaries in black identify the etching patterns of some of the isolation-features. In panels (a), (b), and (d), this is done only for one out of many identical features. In (c), (e), and (f), the highlighted boundary indicates one out of two identical features.

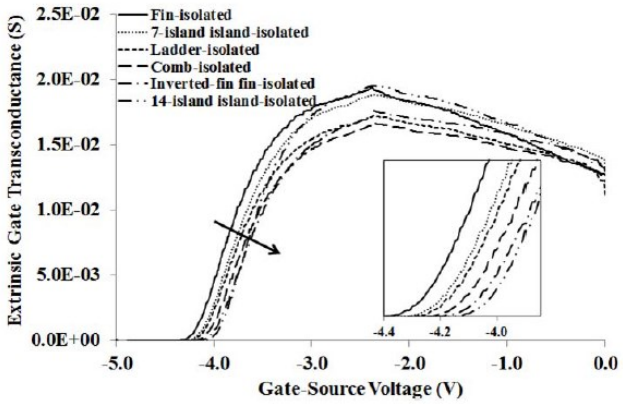


Figure 3.2 Typically observed extrinsic gate-transconductance versus gate-source voltage characteristic, for the six categories of devices. Gate-length is 1 μm and drain-source voltage is 7 V. Inset: close-up around the pinch-off voltage. Arrow: growing order of the positive-shift along the named order of isolation feature categories.

Keithley 4200-SCS semiconductor characterization system was used to obtain the DC characteristics of the devices. Despite different levels of self-heating, devices from all categories almost identically demonstrate proper drain-current saturation, effective channel pinch-off, and acceptable gate leakage. Maximum drain-current density and normalized extrinsic gate-transconductance in the order of 0.7 A/mm and 200 mS/mm are observed, respectively. Figure 3.2 presents the variation of the extrinsic gate-transconductance of these devices with the gate–source voltage.

3.3 Assessment of self-heating in transistors of alternative isolation-feature geometry

On the basis of finite element analysis (FEA), temperature distribution for the six categories of devices in response to the heat generated within the channel of the biased HFETs was evaluated in ANSYS Mechanical. This evaluation was subjected to relevant boundary conditions in terms of the ambient and base temperature (i.e., 300 K), convection, and heat generation associated with self-heating. Isolation features of each of the six device categories were defined on a 1-mm× 1-mm area of the epitaxial layer structure identified in section 3.2. The room-temperature values of the material properties relevant to this evaluation are presented in Table 3.1. The temperature dependence of these characteristics was also built into the model [100] - [101]. In defining the thermal properties of this epitaxial layer structure, the interface between the III-nitride and SiC was assumed to be perfect with no interfacial thermal resistance.

In these simulations, self-heating was analyzed by creating a heat-generator element within the high electric-field region of the 2DEG channel. The heat-generator operated at a power level corresponding to the DC bias (i.e., $I_D \times V_{DS}$). This was done because in AlGaN/GaN HFETs, like other FETs, most of the potential drop, and thereby self-heating, takes place in the vicinity of the drain-edge of the gate. In this study, the length of this high electric-field region was approximately taken as the length of the channel operating under at least eighty percent of the maximum longitudinal electric-field. This length was evaluated on the basis of the model presented in [102]. The center of the improvised heat generator was defined at the drain-edge of the gate, whereas its thickness was taken as 2 nm. For each gate-finger of the fin-isolated HFET, the heat was assumed to be uniformly dissipated along the width of a continuous channel. The corresponding heat generator for each gate-finger in the other five categories of devices shown in Figure 3.1 was defined in terms of an array of discrete uniform heat generators improvised in the high electric-field region of each isolation feature intersecting the gate-finger. At a given bias condition, due to similarity of the drain *I–V* characteristics among all of the devices shown in Figure 3.1 and their equivalent gate-width, the sum of the power delivered by these heat generators was identical among all devices.

Table 3.1
Material properties of GaN, AlGaN, and SiC at 300 K.

Material	Thermal-Conductivity (W/m·K)	Specific Heat Capacity (J/kg·K)	Density (kg/m^3)
GaN	130	490	6150
AlGaN	176	379	5184
SiC	490	690	3200

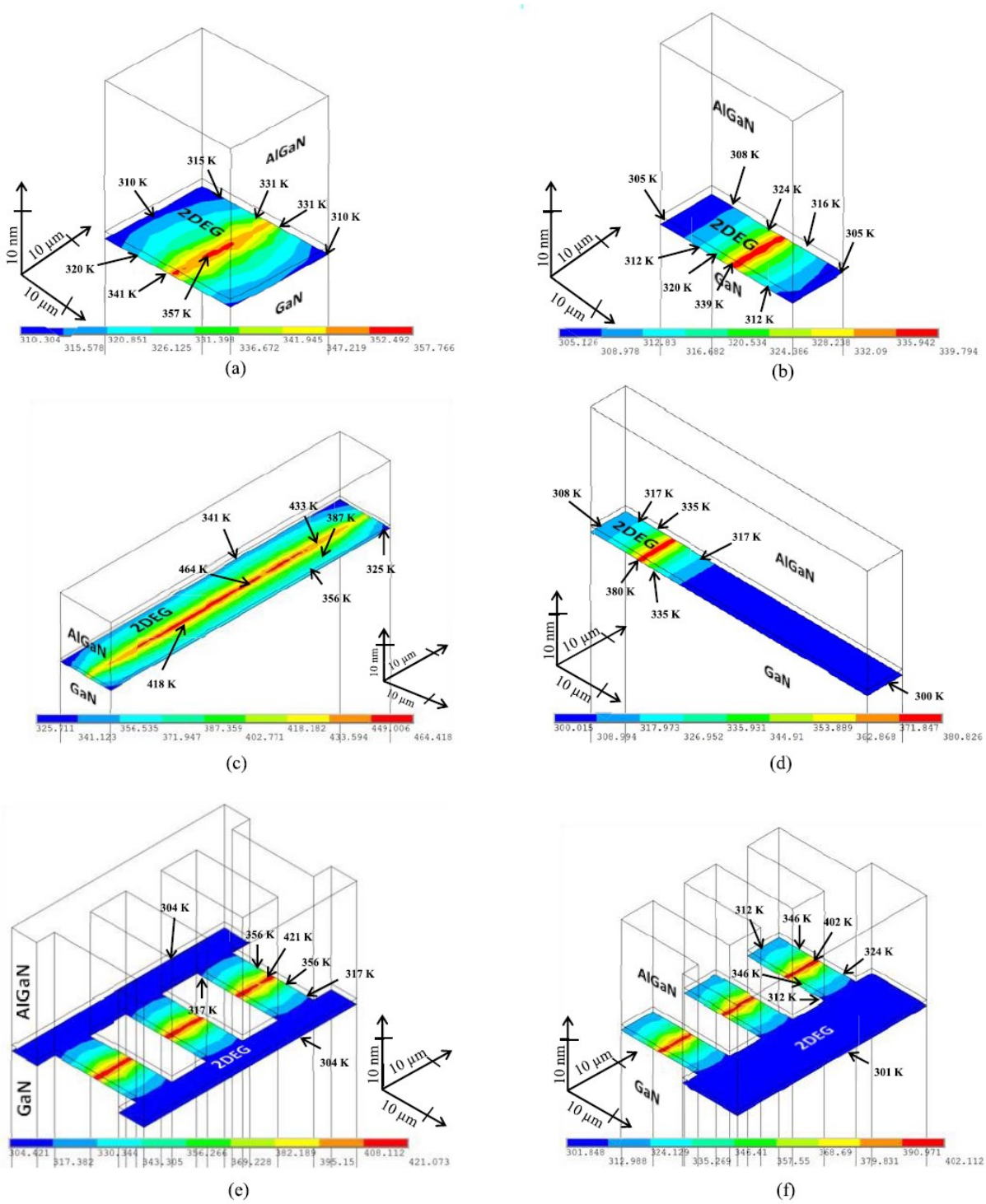


Figure 3.3 Channel-temperature distribution according to heat dissipation of 5 W/mm across the high electric-field region of the 2DEG for a representative set of patterns in (a) 7-island island-isolated HFET, (b) 14-island island-isolated HFET, (c) fin-isolated HFET, (d) inverted-fin fin-isolated HFET, (e) ladder-isolated HFET, and (f) comb-isolated HFET based on ANSYS simulations. Gate-length is 1 μm.

Figure 3.3 presents the channel-temperature distribution across the 2DEG of all six categories of devices when a total power of ~0.5 W is dissipated in each device (i.e., ~5 W/mm corresponding to the 98 μm width of these devices). In this figure, due to much larger thickness of SiC substrate and GaN buffer layer compared with the 2DEG and the barrier, these thicker layers are not shown. In this thermal assessment, only one, and not both gates, of the HFETs of Figure 3.1 were biased. In addition, instead of defining all of the isolation features intersecting a gate in ANSYS, only a smaller set of these features was considered, whereas the dimensions and amount of power dissipated in each case corresponded to the devices shown in Figure 3.1, when biased identically. Considering the chance of heat exchange between neighboring features, the number of isolation features explored in this evaluation was observed to provide a minimal set for properly evaluating the channel temperature.

According to the data presented in Figure 3.3, the maximum channel temperature demonstrates quite a wide range of variation among the six device categories. Among these, the 14-island island-isolated HFET has the lowest maximum temperature developed in the vicinity of the heat generator, whereas the fin-isolated HFET has the overall highest temperature. The difference between the two cases is ~125 K. In addition, in this figure different spatial gradients in the channel temperature of devices from the six categories are observed. On the basis of these data, the more relevant metric of average channel temperature, to transport properties of 2DEG channel, is obtained by calculating the average temperature among the involved nodes of the mesh defined in the active region of the devices.

3.4 Assessment of dependence of self-heating on the size of the isolation feature among transistors built on simple cubic mesas

Based on the results from section 3.3, it is speculated that reducing the dimensions and enhancing the distributed nature of the channel, especially in the form of the island-isolation, can further improve the self-heating metric of performance. In order to further investigate the extent of efficiency of this design technique towards eliminating the self-heating problem among AlGaN/GaN HFETs channel temperature distribution for island-isolated HFETs of different island-width were investigated in ANSYS Mechanical environment. The epilayer structure is

already identified in section 3.2. As previously indicated in the design of island-isolated devices, the devices studied in this ANSYS investigation are built into islands etched with a 300 nm height into the epilayers. While the gate-length and length of the drain and source access regions of the transistors are identified in section 3.2, with the change in the dimensions of the island the number of island incorporated in each device is changed accordingly to preserve the total width of the transistor at 98 μm. Table 3.2 provides different combinations for the island-width and the number of islands of simulated devices. The length of each island is similar to the value expressed in section 3.3.

Following the description from section 3.3, average channel temperature for devices of different island sizes in response to the heat generated within the channel of the biased HFETs was evaluated.

Table 3.2 Different combinations for the island-width and the number of islands in the simulated AlGaN/GaN HFETs.

Island-width (nm)	Number of islands
14000	7
7000	14
3500	28
1750	56
850	115
425	230
200	490
100	980
50	1960
25	3920
12.5	7840

Among the devices identified in Table 3.2, channel temperature distribution according to heat dissipation of 5 W/mm across the high electric-field region of the 2DEG of AlGaN/GaN HFET is evaluated in ANSYS mechanical. As an example, for the case of islands of width 200 nm, the distribution of channel-temperature for this level of heat dissipation is depicted in Figure 3.4. Figure 3.5 presents the dependence of the simulated average channel temperature on the

island-width according to two different levels of heat dissipation (i.e. 5 W/mm and 7 W/mm). The gate-length of each of the transistor investigated in these graphs is 1 µm.

Results indicate that island-width is a critical factor in thermal management considerations. Among all island-isolated devices, since the combined top-surface area of the isolation features and total dissipated power are identical, the volumetric density of the dissipated power is identical.

Figure 3.5 indicates that beyond a threshold value of island-width, the average channel temperature at different power levels reaches the ambient temperature. This shows that for island-isolated devices with island-width smaller than this threshold value, self-heating effects has been totally eliminated. This is an effective approach to improve performance of AlGaN/GaN HFETs and a viable thermal management solution.

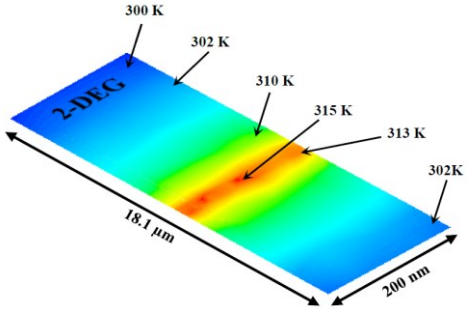


Figure 3.4 Channel-temperature distribution according to heat dissipation of 5 W/mm across the high electric-field region of the 2DEG for island-isolated HFET, based on ANSYS simulations. Island-width and number of islands are 200 nm and 490, respectively. Gate-length is 1 µm.

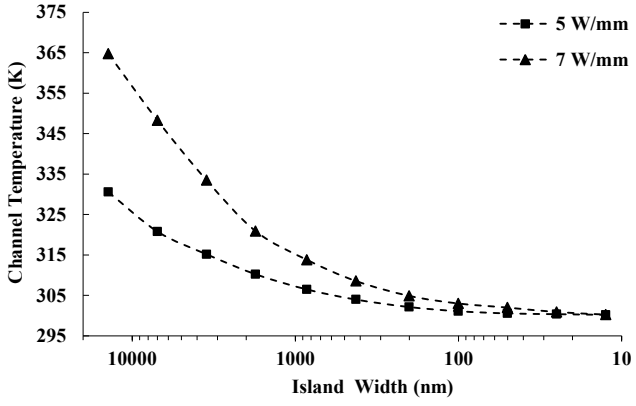


Figure 3.5 Simulated average channel temperature according to heat dissipation of 5 W/mm and 7 W/mm across the high electric-field region of the 2DEG as a function of the width of each island for gate-length of 1 µm. Lengths of drain- and source-access regions are 2 and 1.1 µm, respectively.

3.5 Discussion

To check the validity of the FEA, average channel temperature measurements for devices from each of the six categories were carried out according to the electrical technique proposed in [103] (and later reformulated in [104]). In this technique, a calibration curve is constructed by externally raising the lattice temperature and measuring the variation of the drain-current as a function of this ambient temperature when self-heating is negligible.

To be able to neglect self-heating in the channel, pulsed mode drain-current characteristics were obtained using drain voltage pulses of 175 ns on-time, pulse base-voltage of 0 V, maximum drain-voltage of 10 V, and duty cycle of 0.01%. These measurements were carried out under vacuum at different ambient temperatures from 300 to 440 K using an MMR-LTMP4 probe station. Figure 3.6 presents the variation of drain-current with ambient temperature, when self-heating is negligible. The linear fit slope (θ) in this figure is calculated as -0.15 mA/mm.K. Following this calibration step, DC and pulsed-mode measurements of drain-current were performed under the same bias condition for a given ambient temperature ($T_{ambient}$). Temporal information of pulses is as indicated above, whereas synchronous pulses of base-level of zero and different maximum values matched to DC bias condition are applied to the drain and gate. Based on the difference between DC and pulsed-mode values of the drain-current at the same bias, average channel temperature ($T_{channel}$) can be determined as

$$T_{channel} = T_{ambient} + \frac{\left(I_{D-dc} - I_{d-pulsed}\right)}{|\theta|} \tag{3.1}$$

where $I_{d-pulsed}$ is the pulsed-mode drain-current, and I_{D-dc} is the drain-current under continuous DC condition.

Figures 3.7 (a) and (b) present the measured and simulated average channel temperature as a function of dissipated power for the six categories of devices for gate-length of 1 and 0.5 μm, respectively. In order to compare the results from the six categories of devices with devices fabricated on traditionally sized mesas, a mesa-isolated device with 1 μm gate-length and same source- and drain-access region lengths realized on a 70 × 100 μm^2 mesa has been also investigated in this study. Gate-width of this transistor is 100 μm. In these measurements, identical to section 3.3, only one gate-finger was biased. The impressive agreement between

experimental and FEA results is a testimony to the proper assessment of temperature distribution in the model explained in section 3.3. As expected from the magnifying role of the reduction in the gate-length on the maximum longitudinal electric-field [105], Figures 3.7 (a) and (b) demonstrate that for each device category and at a given dissipated power level, self-heating worsens as the gate-length is reduced from 1 to 0.5 μm.

As observed in Figure 3.7, while an almost identical trend in increasing average channel temperature with dissipated power is observed, in devices where the side-walls of the isolation feature are closer to the drain-edge of the gate, less pronounced self-heating is recorded. Among these devices, the 14-island island-isolated HFET indicates the least self-heating and, as a result, shows the least degradation in current under continuous bias. For 1 μm gate-length, the mesa-isolated device shows the highest channel temperature due to farther distance between the side-walls of the isolation feature and drain-edge of the gate.

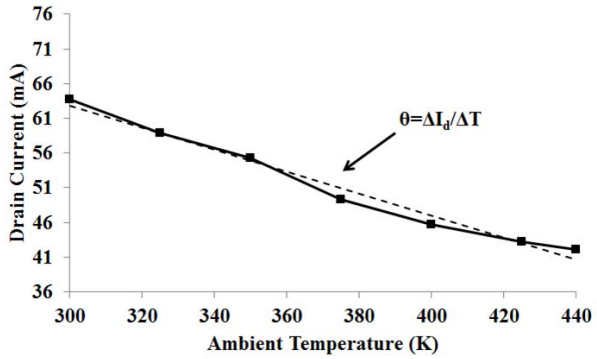


Figure 3.6 Drain-current versus ambient temperature when self-heating is negligible. In terms of the slope, this characteristic is equivalently observed among all device categories and both values of gate-length. Gate-source voltage is 0 V.

In assessing this situation, we must appreciate the distributed nature of the channel among all of the newly proposed device categories with the exception of the fin-isolated HFET (i.e., for a single gate only). Among the five other device categories, the share of the drain-current in each discrete part of the channel is less than the total drain-current, therefore less heat is generated in the device hotspot at the drain-edge of the gate. Between the two island-isolated devices and fin-isolated device, since the combined top-surface area of the isolation features and total dissipated power are identical, the volumetric density of the dissipated power is identical. As shown in Figure 3.3, however, corresponding to the reduction in distance between the transverse side-walls (i.e., to the channel) of the isolation feature and channel hotspot of the

drain-edge of the gate, 14-island island-isolated HFET shows the lowest maximum temperature, whereas the fin-isolated HFET offers the least favorable self-heating performance. In addition, among these device categories, according to the temperature distribution of Figure 3.3, Figure 3.7 illustrates an improvement in average channel temperature in the same order.

Figures 3.3 and 3.7 also indicate a better self-heating performance in the inverted-fin fin-isolated HFET compared with the fin-isolated HFET. This is again supported by our earlier observation on the link between the distance from the transverse side-walls of the isolation-feature and its maximum temperature. However, in the case of the inverted-fin fin-isolated HFET, in spite of the smaller volumetric heat density compared with the 14-island island-isolated HFET and identical distance between the transverse side-walls, the larger distance between the channel hotspot and other two side-walls gives the inverted-fin fin-isolated devices inferior performance compared with the seven-island island-isolated HFETs.

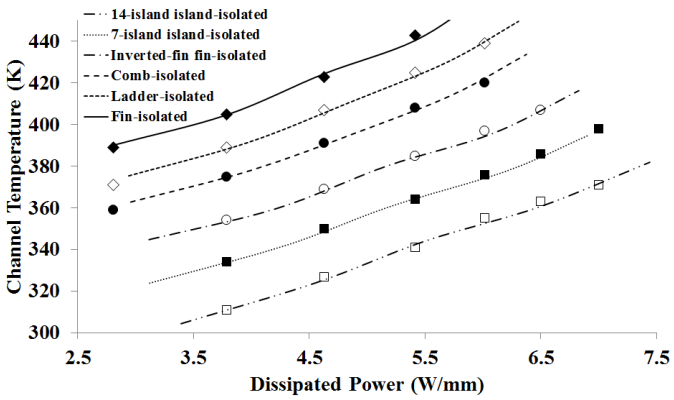
Among the ladder-isolated and comb-isolated HFETs, whereas the distance between the channel hotspot and transverse side-walls of the isolation feature is the same, the presence of one closer side-wall parallel to the channel to this hotspot gives the comb-isolated HFET a boost in terms of reduced self-heating. Both of these device categories, although superior to the fin-isolated HFETs, demonstrate an inferior self-heating performance compared with the inverted fin structure. This is since the isolation feature in both of these categories present a larger volume and as a result a larger thermal mass.

The aforementioned differences in the self-heating characteristic of the devices from the six categories, as shown in Figure 3.7, is in addition observed to be further pronounced at smaller values of gate-length.

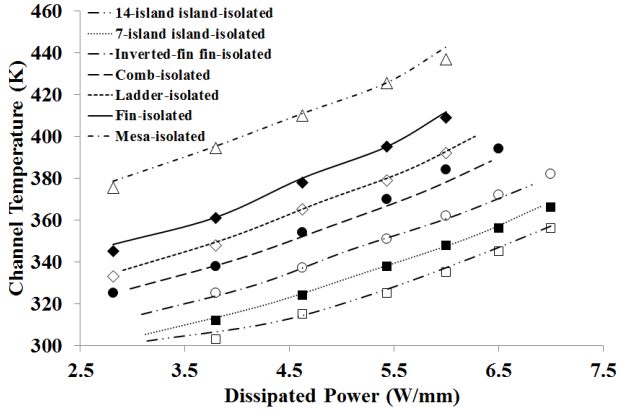
In support of the observations made on Figure 3.7, Figure 3.8 presents the sweeping- and pulsed-mode drain-current–voltage characteristic of the best and worst performing devices with regards to self-heating (i.e., 14-island island-isolated and mesa-isolated HFETs, respectively) of 1 μm gate length. Pulsed-mode measurements were carried out using drain-voltage pulses of 5 ms on-time, with a base voltage of 0 V, and duty cycle of 10%. While for the 14-island island-isolated transistor, the difference between the DC and pulsed-mode characteristics is minimal, Figure 3.8(b) demonstrates a considerable reduction in the drain-current of the mesa-isolated

HFET recorded using the sweeping-mode measurement. The observed linear reduction in the saturation drain-current with the increase in the drain-voltage represents self-heating. Supporting this observation, the extent of this reduction is much less under the pulsed-mode measurement, with the aforementioned pulses of short duration and small duty cycle.

In spite of the indication of the requirement for reducing the dimensions of the isolation features to reduce self-heating, the selected set of isolation-feature geometries that are presented in this study indicate that a compromise between the expected damage from dry-etching of sub-micrometer-size isolation features and improvement in self-heating can be made via exploring other isolation-feature geometries (i.e., geometries other than islands). While it has been reported that the closer proximity of the etched side-walls to the channel and interaction between the etching-generated defects and channel electron population of island-isolated devices can negatively impact the noise performance of these devices [106], the aforementioned compromise seems promising toward improving the self-heating at an acceptable cost to low-frequency noise performance of the transistor.

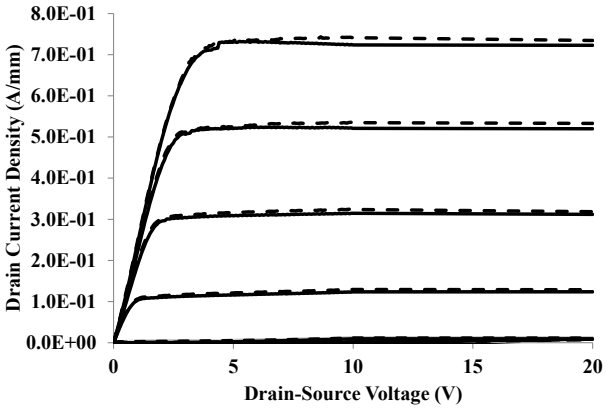


(a)

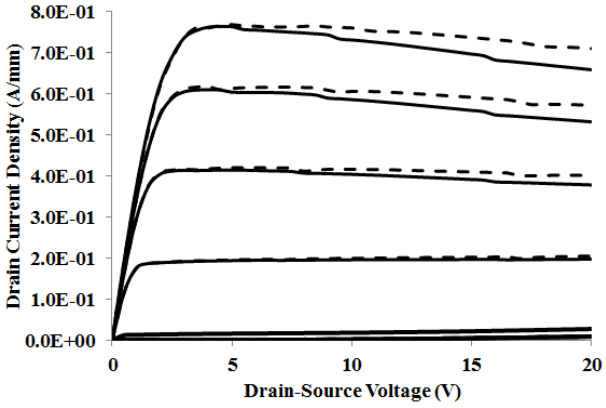


(b)

Figure 3.7 Measured and simulated average channel-temperature as a function of dissipated power for the six categories of devices. Gate-length is (a) 0.5 µm and (b) 1.0 µm. Only in (b) data on a 1 µm gate-length device fabricated on traditionally-sized mesa (i.e., 70 × 100 µm^2) is provided. Measurements are shown by the curves. Markers show the simulation results, while the order of symbols ♦, ◊, ●, ○, ■, and □ are according to the order of devices in the inset from top to bottom. Symbol Δ represent the control mesa-isolated HFET in (b).



(a)



(b)

Figure 3.8 Drain-current versus drain-source voltage for (a) a 14-island island-isolated HFET, (b) a mesa-isolated HFET. Gate-length of both devices is 1 μm. V_{GS} varies from −5 to 0 V, with a step of 1 V. Continuous characteristics represent the sweeping-mode measured data, while the dashed characteristic are obtained through pulsed-mode measurement.

3.6 Conclusion

A new approach for reducing self-heating in AlGaN/GaN HFETs was presented. According to FEA and electrical measurement of average channel temperature, an improved heat-dissipation was observed in HFETs enjoying a more distributed nature of the 2DEG channel, especially for isolation features which offered the center of the channel a smaller distance to the side walls. Observations indicate a more distinct gain in thermal management with reduction of the gate-length and also the surface area of the isolation pattern. Results suggest that self-heating in island-isolated AlGaN/GaN HFETs can be completely ruled out by reducing the island-width beyond a threshold value.

Chapter 4

Alternative isolation-feature geometries and polarization engineering of polar AlGaN/GaN HFETs[4]

4.1 Introduction

In this chapter, correlation between the isolation-feature geometry and the DC current-voltage characteristics of AlGaN/GaN HFETs is investigated. The large piezoelectric and spontaneous polarizations of the metallic-face Wurtzite AlGaN/GaN heterointerfaces have been the center of much attention over the past two decades [107]. Whereas these polarizations contribute to a substantially enhanced concentration of 2DEG, and a superior drain-current density, they also grant a D-mode character to AlGaN/GaN HFETs. Although in switching applications these transistors offer very appealing current sources, as switches they suffer from large amounts of stand-by power consumption. While in realization of switching circuits according to the direct-connected transistor logic (DCTL) configuration, both D-mode (i.e., current-source) and E-mode (i.e., switch) transistors are required, AlGaN/GaN HFET technology has shown difficulties in yielding an E-mode character.

The quest for realization of E-mode AlGaN/GaN HFETs on metallic-face wurtzite epilayers has so far resulted in a number of alternative approaches for transforming their

[4] Most of the material presented in this chapter has been previously published: A. Loghmany and P. Valizadeh, "Alternative isolation-feature geometries and pinch-off voltage variation in polar AlGaN/GaN HFETs," *J. Solid State Electron.*, vol. 103, pp. 162-166, Jan. 2015.

typically-negative pinch-off voltage to positive values. The most viable of these alternatives are based on barrier-thinning [108], fluoride-based plasma treatment [14], reduction of the size of the isolation mesa [15] - [16],[109] - [113], polarization-engineering through replacing the tensile strained AlGaN barrier with the compressively strained AlInGaN barrier [114], incorporation of InGaN back-barrier [10], and incorporation of a p-type gate contact [115].

Among these techniques, the first three, without modifying the growth recipe of the epilayer, extend the possibility of producing D-mode and E-mode AlGaN/GaN HFETs side by side one another. Whereas such a possibility is vital in implementation of DCTL configuration, in the first two techniques this is accompanied by larger gate-leakage current and possibility of hysteresis in the gate characteristics of E-mode HFETs. These are due to the surface damage and ease of tunneling through the thinned-barrier in the first technique and movement of fluorine ions in the techniques based on fluoride plasma treatment [116].

Technique of the reduction of the size of the isolation mesa, however, yields the possibility of parallel processing of D-mode and E-mode HFETs without adding any major step to the fabrication process, or additional damage to the top-surface of the mesa. Ohi *et al.* through realization of multi-mesa HFETs have successfully demonstrated the capabilities of this technique in transforming AlGaN/GaN HFETs to E-mode transistors [15], [109]. Although they have attributed the positive-shift in the pinch-off voltage to a triple-gate surrounding-field effect, reports on transformation of the pinch-off voltage even in absence of this triple-gate effect suggest that other factors such as development of peel forces around the boundaries of the smaller mesas, and a reduction in piezoelectric polarization, can also be contributing factors to this positive-shift [17].

Whereas realization of the multi-mesa channel HFETs reported by Ohi *et al.* has been made possible through formation of trenches between mesas of widths smaller than 100 nm, and as a result under stringent etching requirement, clarification of the origin of the observed shift on the pinch-off voltage might result in reducing the burden of this etching step. Towards that end, two alternative isolation-feature geometries (i.e., resembling the structures of ladder and comb) are studied for the first time. The DC characteristics of AlGaN/GaN HFETs fabricated on these alternative geometries of isolation-feature are compared to those of devices fabricated according to the two previously proposed isolation-feature geometries (i.e., island and fin) [17]. NextNano,

a 3D nano device simulator, was also used in order to simulate the 2-D carrier distribution of the channel among these devices.

4.2 Device structure and characteristics

Whereas this study uses the same devices as those experimentally explored in chapter 3, for the sake of completeness of this chapter's discussion the description of the device types are repeated here. The transistors explored in this study were fabricated on an AlGaN/GaN HFET structure grown on insulating SiC substrate. The epitaxial structure was composed of a 20 nm $Al_{0.3}Ga_{0.7}N$ barrier, a 1 nm AlN spacer layer, a 200 nm unintentionally doped GaN channel layer, a 2 μm GaN buffer layer, and a 20 nm nucleation layer. Process technology followed a standard recipe for the fabrication of AlGaN/GaN HFETs, with no modification in recipe in implementing devices having any of the aforementioned isolation-feature geometries. This recipe starts with the definition of isolation-features of 300 nm height, using a chlorine-based reactive ion etching process. Following this step, Ohmic and gate contacts are formed. The unexposed surfaces are then passivated by SiN and openings are created for electrical access to the drain-, source-, and gate-pads.

According to this recipe, six categories of two-finger HFETs, with different isolation-feature geometries, were fabricated side by side one another. Figure 4.1 presents micrographs and 3-D schematics of these six categories of devices. Although traditionally HFETs are fabricated on cubic mesa isolation-features of lateral dimensions the size of the gate-width, the six categories of the devices which are reported here have alternative geometries resembling: array of islands (which as shown in Figure 4.1(a)-(b) are simply small-size mesas), fins (which as shown in Figure 4.1(c)-(d) are simply narrow mesas), ladders (in which as shown in Figure 4.1(e) channel is formed on the steps of a ladder-like structure), or combs (in which as shown in Figure 4.1(f) channel is formed on the teeth of a comb-like structure). In this figure, whereas the difference between the two types of fin-isolated HFETs is in terms of the orientation of the fin versus the gate (i.e., one in parallel and one normal to the gate-finger), the two types of island-isolated HFETs differ in the size of each island.

Details of the dimensions of the isolation-features are found in Figure 4.1. The total width for one gate-finger of the transistors from any of the six categories is 98 μm. This is calculated

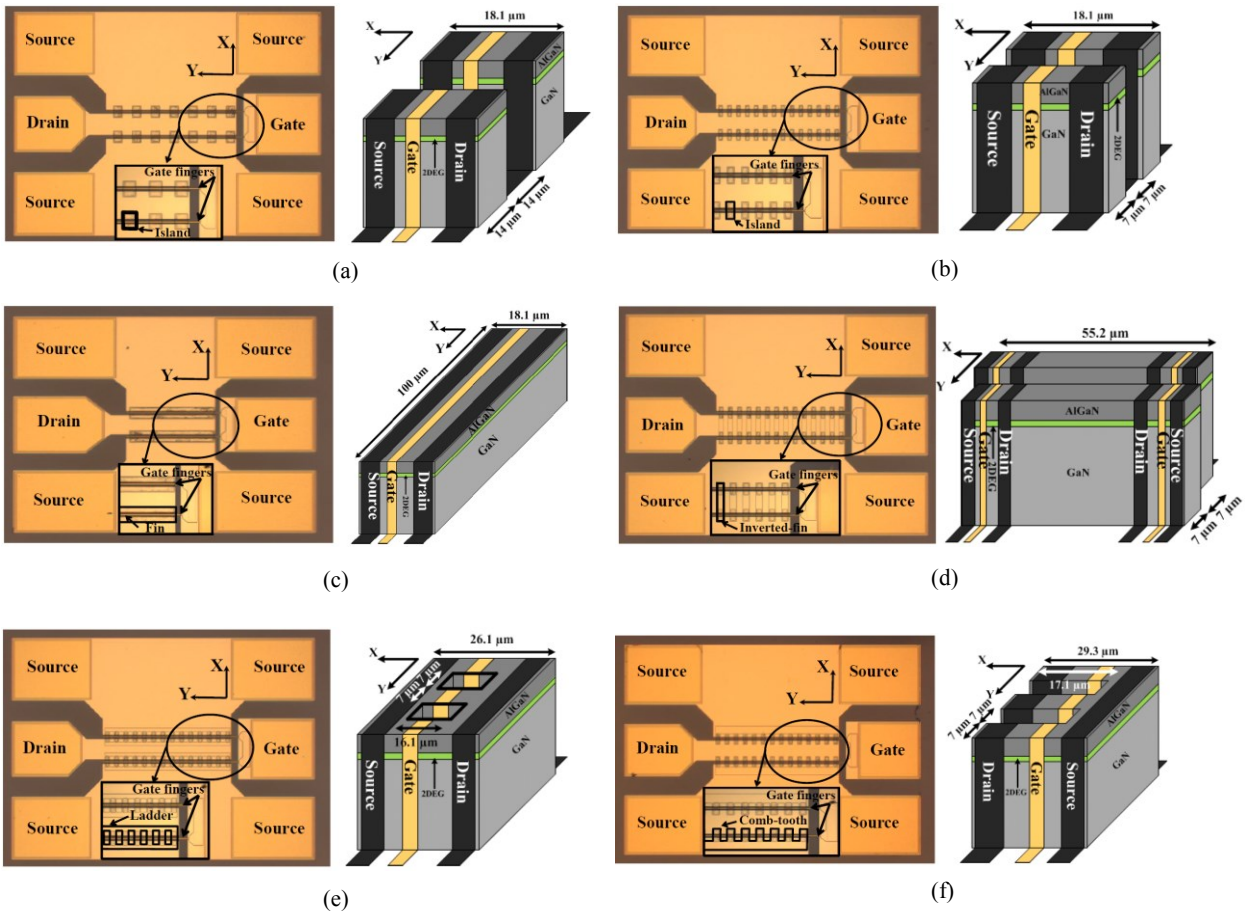


Figure 4.1 Micrographs of (a) 7-island island-isolated HFET, (b) 14-island island-isolated HFET, (c) fin-isolated HFET, (d) inverted-fin fin-isolated HFET, (e) ladder-isolated HFET, and (f) comb-isolated HFET. Gate-length, lengths of drain-, and source-access regions are 1 µm, 2 µm, and 1.1 µm, respectively. Insets on the left panels present a magnified view of each device in the area approximately indicated by the oval. On these magnified images, the highlighted boundaries in black identify the etching patterns of some of the isolation-features. In panels (a), (b), and (d) this is done only for one out of many identical features. In (c), (e), and (f) the highlighted boundary indicates one out of two identical features. Panels on the right present a 3-D schematic representing a minimum set of isolation-features.

through multiplying the width of the island, fin, comb-tooth, and ladder-step by the number of these features intersecting a gate-finger. The minimum dimensions were limited by the foundry's constraints. In each category, devices with two different values of gate-lengths (i.e., 1.0 and 0.5 µm) were fabricated. All fabricated devices have a gate-source spacing of 1.1 µm, and gate-drain spacing of 2 µm.

Figure 4.2 presents typically observed DC and pulsed-mode drain and gate current-voltage (*I–V*) characteristics from a single finger of the devices from each of the six identified categories, with gate-length of 1 µm. The pulsed-mode characteristics were obtained using drain-

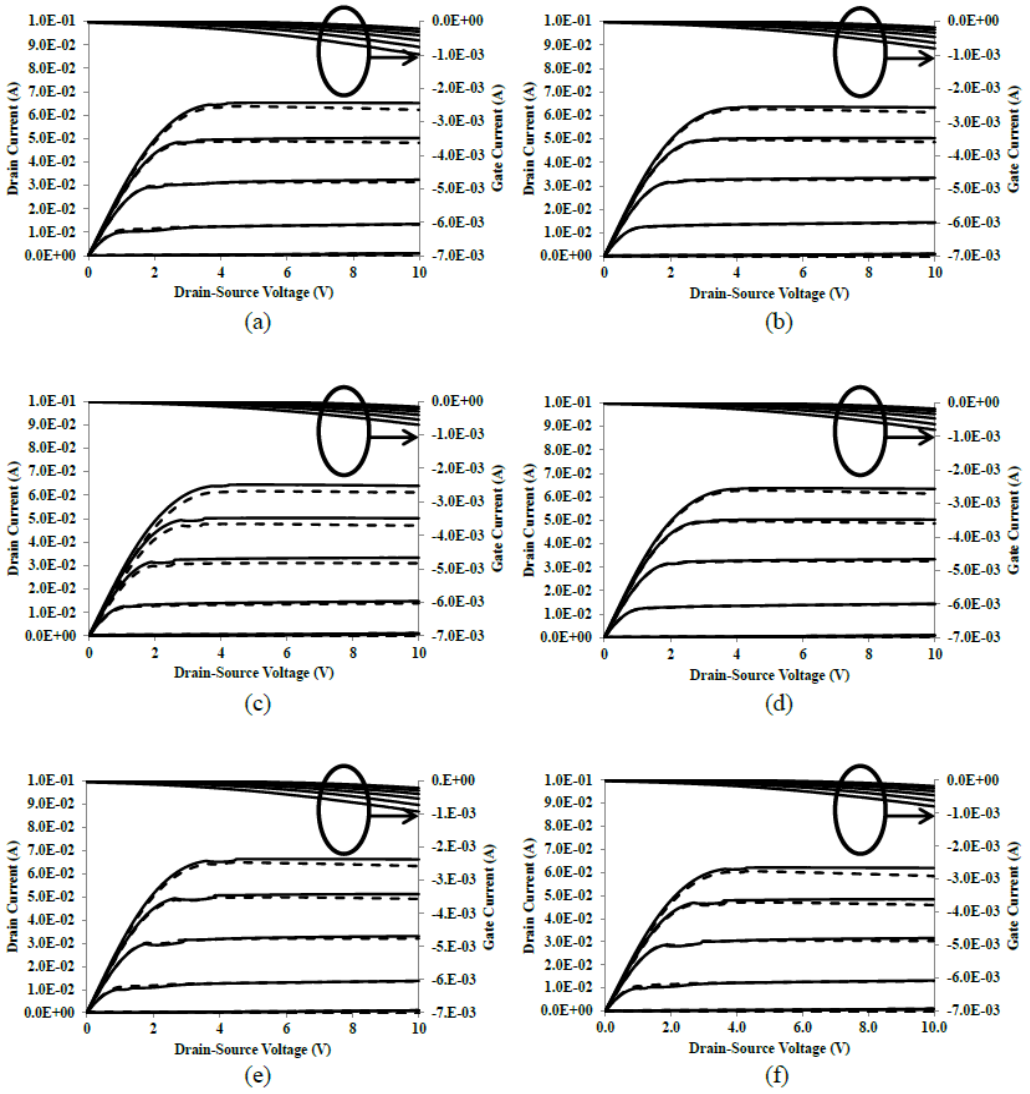


Figure 4.2 Drain and gate current versus drain-source voltage for (a) a 7-island island-isolated HFET, (b) a 14-island island-isolated HFET, (c) a fin-isolated HFET, (d) an inverted fin fin-isolated HFET, (e) a ladder-isolated HFET, and (f) a comb-isolated HFET. Gate-length of all devices is 1 µm. V_{GS} varies from −5 to 0 V, with a step of 1 V. Continuous drain-current characteristics represent the pulsed-mode measured data.

voltage pulses of 5 ms on-time, with a base voltage of 0 V, and duty cycle of 10%. Devices from all categories demonstrate proper drain-current saturation, effective channel pinch-off, and acceptable gate-leakage. Maximum drain-current density and normalized extrinsic gate-transconductance in the order of 0.7 A/mm and 200 mS/mm were observed, respectively. Figure 4.3 presents the variation of the extrinsic gate-transconductance of these devices with the gate-source voltage. This figure demonstrates a certain correlation between the pinch-off voltage and the isolation-feature geometry.

4.3 Discussion

Investigations over a large number of devices from the six categories, identified in the previous section, indicate that a correlation similar to the one presented in Figure 4.3 exists between the pinch-off voltage and the isolation-feature geometry of all samples. The scatter-plot presented in Figure 4.4, summarizes these observations. Values of pinch-off voltage were extracted by intersecting the rising edge of the transconductance characteristics with the V_{GS} axis. As shown in Figure 4.4, since distinct clusters for the six categories of devices are identifiable in the scatter-plot, the observed variations of pinch-off voltage cannot be treated as random incidences. According to the data presented in this figure, pinch-off voltages of the devices from each sample demonstrate a growing positive-shift along the order of: fin-isolated, 7-island island-isolated, ladder-isolated, comb-isolated, inverted-fin fin-isolated, and 14-island island-isolated devices. This trend is supportive of the previously reported observations on the correlation between the size of the isolation-feature and the positive-shift of the pinch-off voltage [17].

Whereas Ohi *et al.*, also observed a correlation between the geometry of the isolation-feature and the pinch-off voltage, they attributed this effect to the improved proximity of the gate electrode's side-wall coverage of the isolation-feature to the center of the channel, and essential manifestation of a triple-gate effect [15], [109]. However, on the basis of the dimensions presented in Figure 4.1, this explanation is incapable of justifying the trend observed among the pinch-off voltages of 14-island island-isolated, comb-isolated, inverted-fin fin-isolated, and ladder-isolated HFETs in Figure 4.4. This is since among all of these device categories, identical distances between the side-wall coverage of the isolation-feature and the center of the channel, and as a result identical chance for manifesting triple-gate effects, exist. The cross-sectional schematic view of Figure 4.5 illustrates this situation.

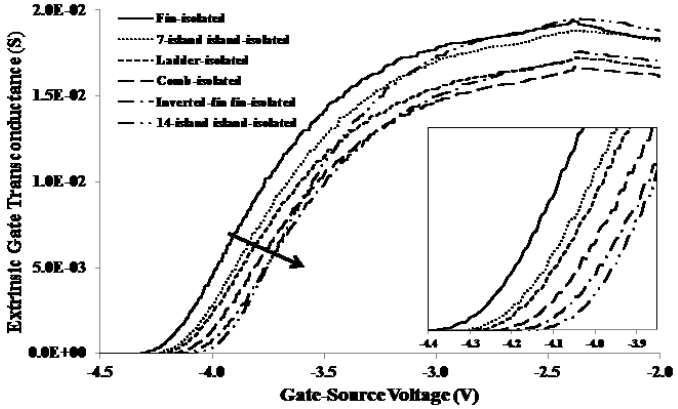


Figure 4.3 Typically observed extrinsic gate-transconductance versus gate-source voltage characteristic, for the six categories of devices. Gate-length is 1.0 μm and drain-source voltage is 7 V. A close-up around the pinch-off voltage is provided in the inset. Arrow shows the growing order of the positive-shift along the named order of isolation-feature categories.

Although the trend observed in Figure 4.4, seems unjustifiable on the basis of a triple-gate effect, as suggested in [17] the evolution of peel-forces around the perimeter and the convex corners of the isolation-feature, and the resulting degradation in the piezoelectric polarization across the heterointerface, seem to be capable of explaining this trend [117]. In terms of this explanation, Table 4.1 presents the calculated values of perimeter-to-area ratio among the six categories of devices. With the exception of comb-isolated HFETs, it is observed that a device with larger perimeter-to-area ratio demonstrates a slightly less negative pinch-off voltage. Since devices from the six categories are otherwise identical, the observed correlation suggests the presence of a link between the development of peel-forces around the perimeter and reduction in the piezoelectric polarization at the AlGaN/GaN heterointerface. Although the perimeter-to-area ratio of the isolation-feature of the comb-isolated HFETs is smaller than those values of 7-island island-isolated and ladder-isolated HFETs, the comb-isolated HFETs demonstrate a less negative pinch-off voltage than the other two device types. While the comb-isolated structure is the only asymmetric structure among the six reported in this study, it is speculated that in this case the uncompensated peel-forces at the convex corners of the comb tooth yield the possibility of reducing the piezoelectric polarization to the extent larger than the ladder-isolated HFET [117]. This is in spite of the fact that the dimensions of the gated HFET among these two isolation geometries (i.e., step of the ladder and tooth of the comb) closely match. Whereas Figures 4.3

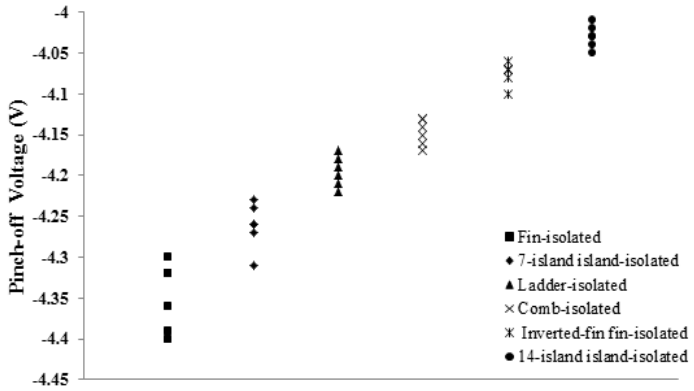


Figure 4.4 Scatter-plot of the variation of the pinch-off voltage among the six device categories. Gate-length is 1 μm. For each category, several devices were measured.

and 4.4 present devices with a 1.0 μm gate-length, same trends are also observed among devices with 0.5 μm gate-length.

Although the variations among the pinch-off voltages presented in Figure 4.4 are not very substantial, it is anticipated that intensified presence of peel-forces in isolation-features of much smaller dimensions, with larger perimeter-to-area ratio, and a more pronounced presence of convex corner effects, can yield a substantial positive-shift in pinch-off voltage in the orders reported by Ohi *et al.* [15], [109]. Due to limitations imposed by the foundry, however, devices presented in this work had relatively large dimensions.

Although the increase in the in-plane strain relaxation, and hence reduction in the contribution of piezoelectric polarization to the 2DEG concentration, with reduction of the width of the mesa to values in the order of a few hundreds of nanometers have been already reported through experimental [10] and theoretical means [16], the present observations suggest that even in larger scales of isolation-feature geometry this strain-relaxation can have a tangible impact on the pinch-off voltage. Whereas the previous reports on this issue have focused on the correlation between the amount of shift in the pinch-off voltage and the width of isolation-features (i.e., of island- or fin-types), the observation made in this work in terms of relevance of presence of concave and convex corners, in case of ladder- and comb-shaped isolation-features, to the amount of observed shift are unique to this study. In addition, the relatively broad range of isolation-feature geometries explored here has helped to highlight the relevance of strain-relaxation to the observed shift in pinch-off voltage, while the dimensions among many of the

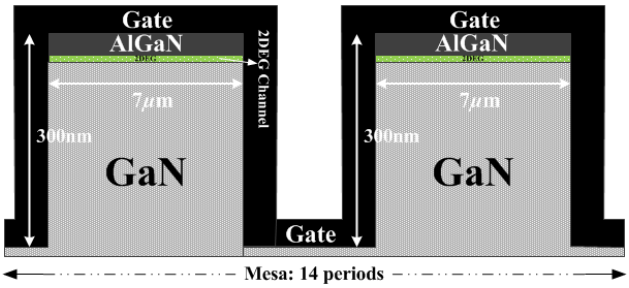


Figure 4.5 Schematic of a cross-sectional view of two islands of the 14-island-, inverted-fin, comb-isolated, and ladder-isolated AlGaN/GaN HFETs. Schematic is not drawn in scale.

explored alternatives suggest an equal presence of the other probable culprit to this shift (i.e., triple-gate effect).

Table 4.1
Perimeter-to-area ratio for the six categories of devices with 1 μm gate length.

Isolation-type	Perimeter-to-area ratio (μm^{-1})
Fin-isolated	0.14
Comb-isolated	0.22
7-island island-isolated	0.25
Ladder-isolated	0.30
Inverted-fin fin-isolated	0.32
14-island island-isolated	0.40

In order to better understand the effect of the body width, development of peel forces around the boundaries of the smaller mesas, reduction in piezoelectric polarization, and sidewall gate effect on the average 2DEG concentration, a 2-D simulation has been performed using NextNano simulator [118].

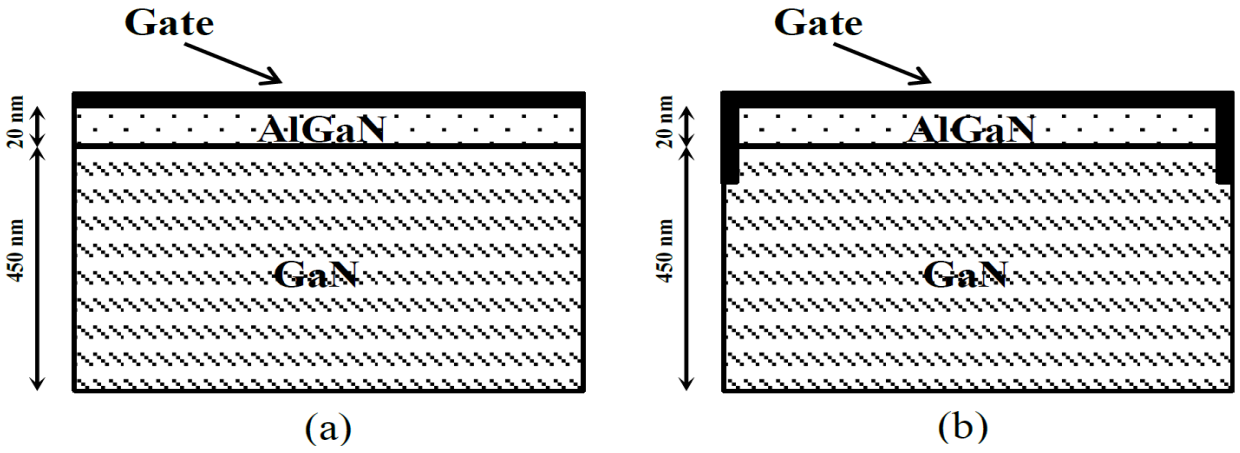


Figure 4.6 Body cross sections of the investigated AlGaN/GaN HFETs with top gate (a) and triple-gate (b) structures.

The epitaxial structure defined in the simulator was composed of an undoped 20 nm $Al_{0.3}Ga_{0.7}N$ barrier and a 450 nm unintentionally doped GaN channel layer. The material parameters needed for the simulations are obtained from [16]. Two different structures, one with top gate and one with triple-gate (i.e., top and side-wall gating effect) were simulated to study the improved gate control due to the presence of two sidewall gates in addition to the top gate in triple-gate structure. Figure 4.6 presents cross-sectional view of the simulated devices. To be able to study the reduced piezoelectric polarization due to strain relaxation in the AlGaN barrier of narrow width structures, simulations were also performed for devices with two different device widths (i.e., 75 nm and 500 nm). These simulations were performed for both top gate and triple-gate structures. The results shown in Figure 4.7 clearly demonstrate that for a given gate voltage, the 2DEG sheet concentration rapidly decreases for shrinking body widths. Results also indicate that for a device without the presence of sidewall gates 2DEG sheet concentration is higher in comparison with triple-gate structure with the same device dimensions. For devices with narrower body structures this difference is more pronounced (i.e., 75 nm width device).

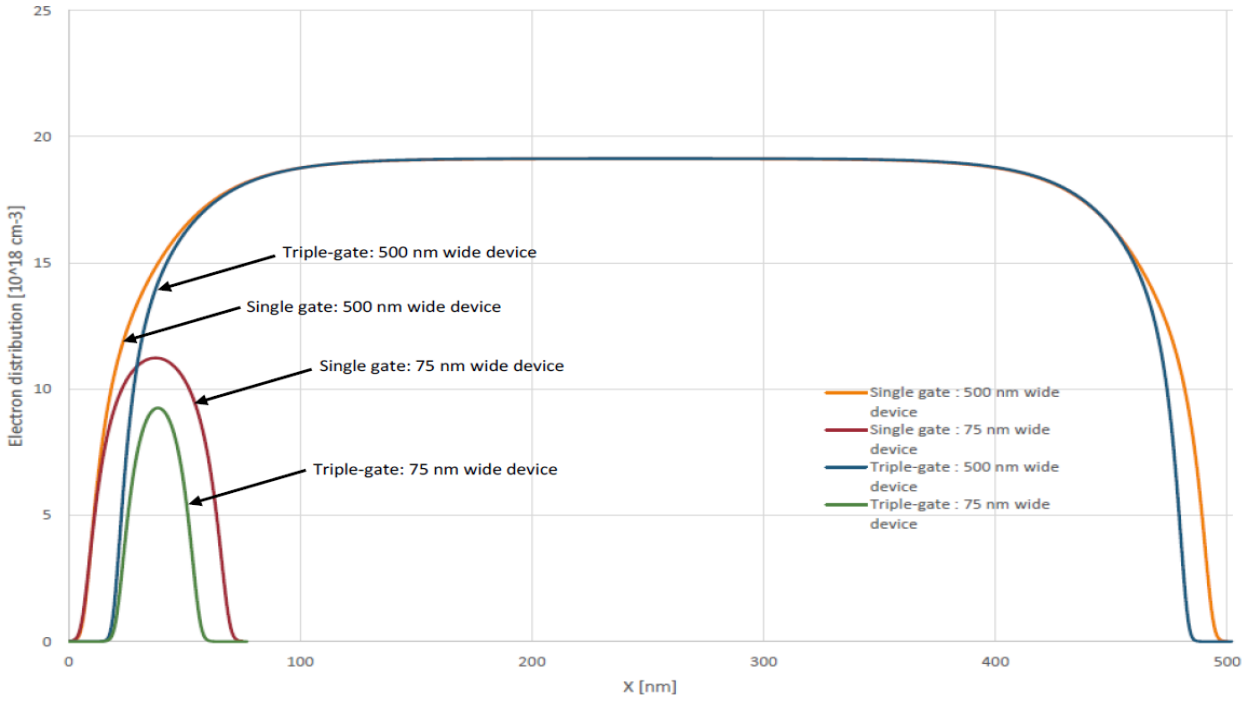


Figure 4.7 Effect of body width reduction and the gate structure on the electron distribution in the 2DEG of the structures from Figure 4.6 for zero applied gate voltage. Shown are the electron concentrations at width/2 where for each structure the maximum electron concentration occurs.

It can also be observed from Figure 4.7 that for triple-gate structure and due the gate sidewall effect, gate has more control over the channel which results in lower 2DEG sheet concentration. Development of peel forces around the boundaries of the smaller mesas (i.e., 75 nm width device) and reduction in piezoelectric polarization in narrower body structures also results in lower carrier concentration in 2DEG. Simulation results confirm that triple-gate effect and strain relaxation are both responsible for lower 2DEG concentration and as a result less negative pinch-off voltages in island-isolated devices with smaller island width.

4.4 Conclusion

Through implementation of six different geometries for isolation-features of polar AlGaN/GaN HFETs, it was shown that the correlation between the isolation-feature geometry and the observed shift in the pinch-off voltage is not fully explicable in terms of a multiple-gate effect. The reported observations of this study suggest a link between the increase in the perimeter-to-area ratio of the cross-section of the isolation-feature, and an improved positive-shift in the pinch-off voltage. It has been illustrated that the 2DEG sheet concentration depends strongly on the device width and the gate structure.

Chapter 5

Reliability studies of AlGaN/GaN HFETs of alternative isolation-feature geometry

5.1 Introduction

As indicated earlier in chapter 2, one of the important concerns on the marketability of AlGaN/GaN HFETs is their long-term reliability. Along with reliability assessment, studies of issues such as gate/drain lag, and frequency dispersion of the output resistance and gate transconductance occupy a pivotal position in evaluating any technological variant to the traditional HFETs. This is especially true if the technological variant is exposing the active region of the transistor to a different setting of surface states. Since the technological variants presented in the previous two chapters, which employ different isolation-feature geometries, impose different levels of involvement of etched surfaces (hence, surface states) on the vicinity of the active region of the transistor, these technological variants require a careful assessment from the aforementioned points of view. In this chapter, results of the gate-lag and frequency-dispersion studies over a wide range of temperatures are presented alongside the long term reliability assessment of AlGaN/GaN HFETs which are designed according to these novel isolation-feature geometries.

5.2 Device structures

Since the layer structure and the dimensions of the transistors used in these studies are already presented in the previous two chapters, for the sake of brevity the reader is referred to section 3.2 for the information on the structures of these devices.

5.3 Experimental results and analysis

5.3.1 Gate-lag

As mentioned previously in chapter 2, charge trapping within the epilayer and at the exposed surfaces has been reported to be a cause for the usually observed delay between the drain current and the pulsed gate (or, drain) voltage [119]. This delayed response often presents a characteristic such as the one illustrated in Figure 5.1(a).

As illustrated in Figure 5.1(a), this form of temporal response indicates an original jump in the value of the drain current, when the gate potential is elevated to values larger than the pinch-off voltage (i.e., V_P). However, it is observed that drain current originally jumps only to values short of the DC drain current expected when V_{GS} is equal to the high-value of the gate pulse. Nonetheless, especially for long enough gate pulses it is observed that either in terms of a single saturating exponential, or exponentials with multiple time-constants, the drain current increases and eventually saturates. The saturation level reached even for long gate pulses can still remain short of the value of the DC drain current.

The snapshots presented in Figure 5.1(b) for each of the three temporal behaviors (i.e., the original almost-instantaneous response, incremental increase, and saturation), attempt to illustrate the role of negative charging of the surface states (if of acceptor type) or neutralization (if the states of donor type are contributors to the polar 2DEG formation at the AlGaN/GaN heterointerface), towards developing a different value of 2DEG concentration and drain current under each regime. It is often believed that it is the trapping of electrons originating from the surface component of the gate current, or the hot carriers migrating from the 2DEG, that yield the partial depletion of the polar 2DEG concentration in the area of the channel located beneath the charge-trapped surface. Since the drain edge of the gate observes the highest electric-field, the surface of this region is deemed most relevant to this problem. The reason for the time

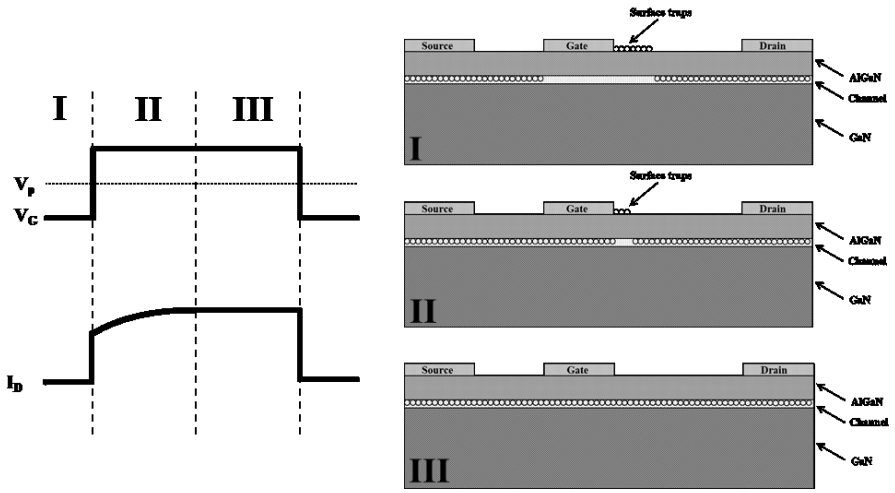
dependence of this behavior and observation of one or multiple time-constants under the regime of incremental increase is the presence of a chance for removal (i.e., detrapping) of the carriers transferred to the trapping sites (i.e., upon pulsing the gate voltage). However, the possibility of detrapping is a function of trap energy level (i.e., deep or shallow) and existence of a sufficient source of kinetic energy. Accordingly, study of the aforementioned time constants involved in the drain current recovery as a function of lattice temperature is expected to have clues into the energy level of the traps involved in these processes. This is since in presence of a dominant trap, the detrapping time-constant follows an Arrhenius characteristic, given by [120] - [121],

$$\tau = \frac{\tau_0}{T^2} exp\left(\frac{E_A}{K_B T}\right) \tag{5.1}$$

where, T is the temperature in Kelvin, E_A is the energy level of the responsible trap-site, K_B is the Boltzmann constant, and τ_0 is a proportionality constant.

According to (5.1), based on the values of trapping/de-trapping time constants (i.e., τ_1 and τ_2) acquired at two different temperatures (i.e., T_1 and T_2, respectively), the energy level of the responsible trap-site can be calculated as:

$$E_A = \frac{K_B}{\left(\frac{1}{T_1}-\frac{1}{T_2}\right)} \ln\left(\frac{\tau_1/\tau_2}{(T_2/T_1)^2}\right) \tag{5.2}$$



(a) (b)

Figure 5.1 (a) Typically observed delay between the drain current and the pulsed gate voltage. (b) Depiction of the occupation status of surface states in the drain-access region of the transistor provided progressively as snapshots immediately after pulsing the gate (instant I), briefly after the gate turn-on pulse (instant II), and upon saturation of the pulsed drain current (instant III). It is often suggested that the occupied surface states forming a negatively biased virtual gate partially deplete the 2DEG of electrons and cause the gate-lag behavior (virtual gate model).

Figure 5.2 illustrates the measurement setup for the gate-lag studies. The temperature-controlled chamber of a MMR-LTMP4 low temperature micro-probe station was used to perform the measurements. This probe station has an operation temperature range of 80-500 K. During measurements, the chamber of the probe station was operated under low pressure and the temperature was controlled and monitored by the MMR-K20 temperature controller. To prevent the unwanted noise, coaxial cables were used. In the gate-lag measurements, for generating the gate pulse, HP 8116A 50 MHz pulse/function generator was used. Tektronix DP04054 digital oscilloscope was also employed for recording the temporal variation of V_1 and V_2. Measurements were conducted in the order of 80, 150, 220, 300, 350, and 400 K. Fresh devices showing a typical behavior in the DC sweeping mode characteristics, such as the one presented in Figure 3.8, were used in performing all the measurements. After each gate-lag measurement, the DC gate and drain characteristics were verified versus the previously recorded sweeping mode characteristics to make sure that no significant device degradation has taken place.

In the gate-lag measurements, a voltage step is applied to the gate terminal, while maintaining a fixed drain bias of $V_{D\text{-}DC}$=7 V. This gate-pulse drives the transistors from the initial pinch-off to an open channel condition with low and high values of V_{GS} equal to -10 V and 0 V, respectively. Gate pulses have a nanosecond rise-time, 20 µs on-time, and duty cycle of 20%. The low-state of the gate pulse is chosen well below the pinch-off voltage to ensure an effectively negligible drain-current. Potentials V_1 and V_2 versus time were recorded using the digital oscilloscope. In this study, according to Figure 5.2, the drain-current (i.e., I_D) is evaluated as:

$$I_D = \frac{\Delta(V_1 - V_2)}{R_2} \tag{5.3}$$

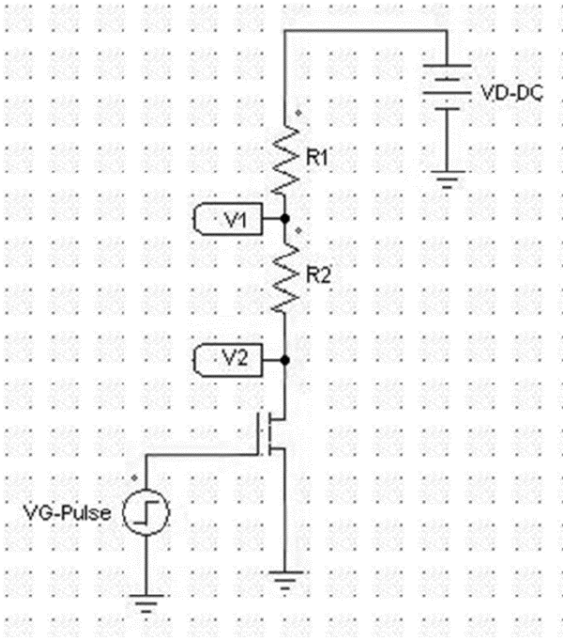


Figure 5.2 Gate-lag measurement setup. R_1 and R_2 are both 51 Ω.

A gate-lag pattern not unlike the one indicated in Figure 5.1 is observed among all of the devices of isolation-feature geometries presented in Figure 3.1, at all of the indicated measurement temperatures and among devices of both 0.5 and 1 μm gate-length. As an example, Figure 5.3 depicts the gate-lag patterns observed in a typical 14-island island-isolated HFETs of 1 μm gate-length at all measurement temperatures. Figure 5.4 presents the results of gate-lag measurement at different measurement temperatures for a transistor fabricated on traditionally sized mesa of dimensions 70 × 100 μm^2 using the same epilayer structure, while gate-length and the length of drain and source access regions are the same as the other categories.

As typically observed among Figures 5.3 and 5.4, all of the explored devices exhibit gate-lag patterns indicated by a single time constant incremental increase in the drain current of region II at all measurement temperatures.

Figure 5.5 shows room-temperature values of the pulsed-mode drain current during one gate pulse for one device from each of the aforementioned transistor varieties as a percentage of the maximum pulsed-mode drain current level of each device. While interpolation to a single time-constant saturating exponential seems applicable to all these measurements, Figure 5.6 presents the scope of variability of this time constant among a large number of seemingly

identical devices and over a wide range of lattice temperatures. As mentioned earlier, existence of a single time-constant exponential gives evidence on the relevance of a dominant trap level in each device.

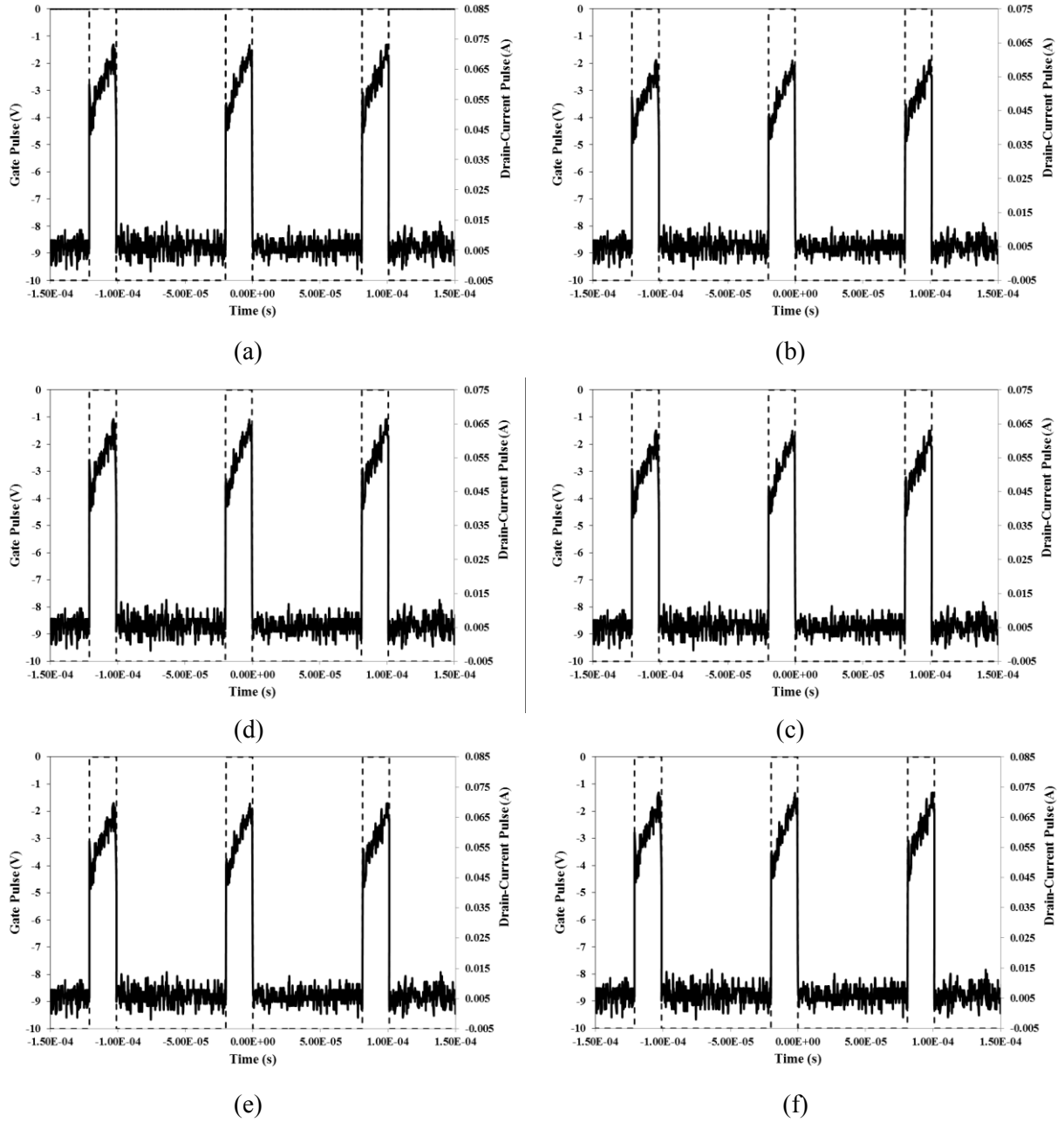


Figure 5.3 Pulsed-mode drain-current data for a typical 14-island island-isolated device at 80, 150, 220, 300, 350, and 400 K in (a), (b), (c), (d), (e), and (f), respectively. Dashed lines represent the gate voltage pulses and solid lines represent the drain-current pulses.

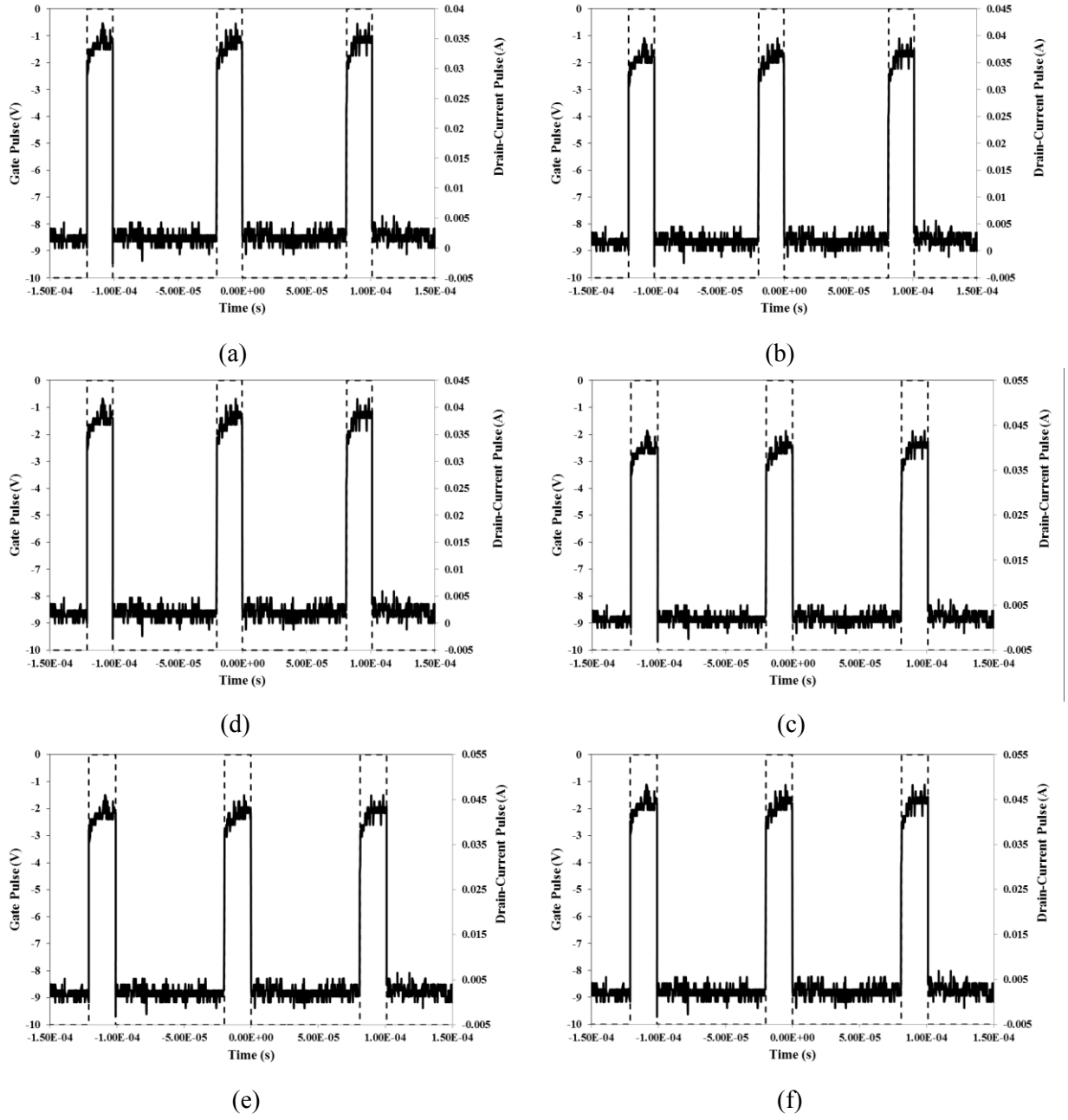


Figure 5.4 Pulsed-mode drain-current data for a mesa-isolated device at 80, 150, 220, 300, 350, and 400 K in (a), (b), (c), (d), (e), and (f), respectively. Dashed lines represent the gate voltage pulses and solid lines represent the drain-current pulses.

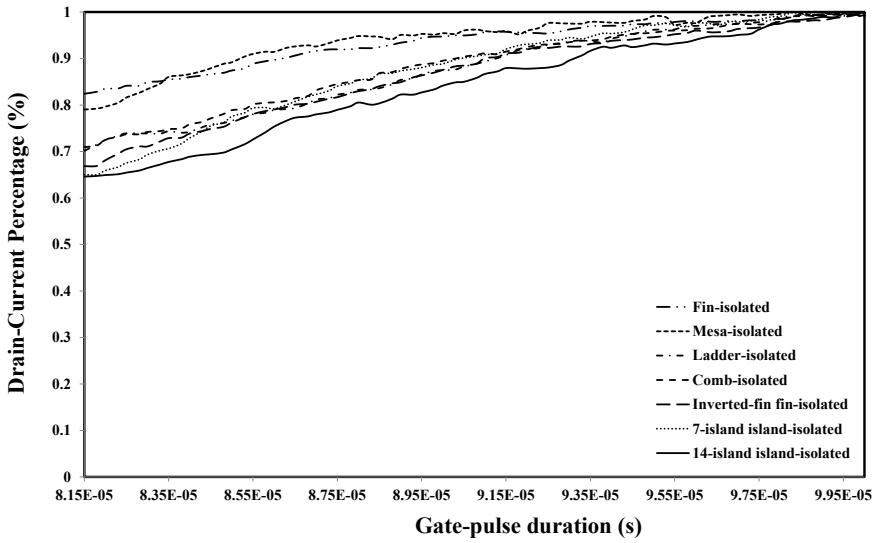


Figure 5.5 Pulsed-mode drain-current as a percentage of the maximum value of the drain-current reached at the end of the gate pulse for different types of devices tested at lattice temperature of at 300 K.

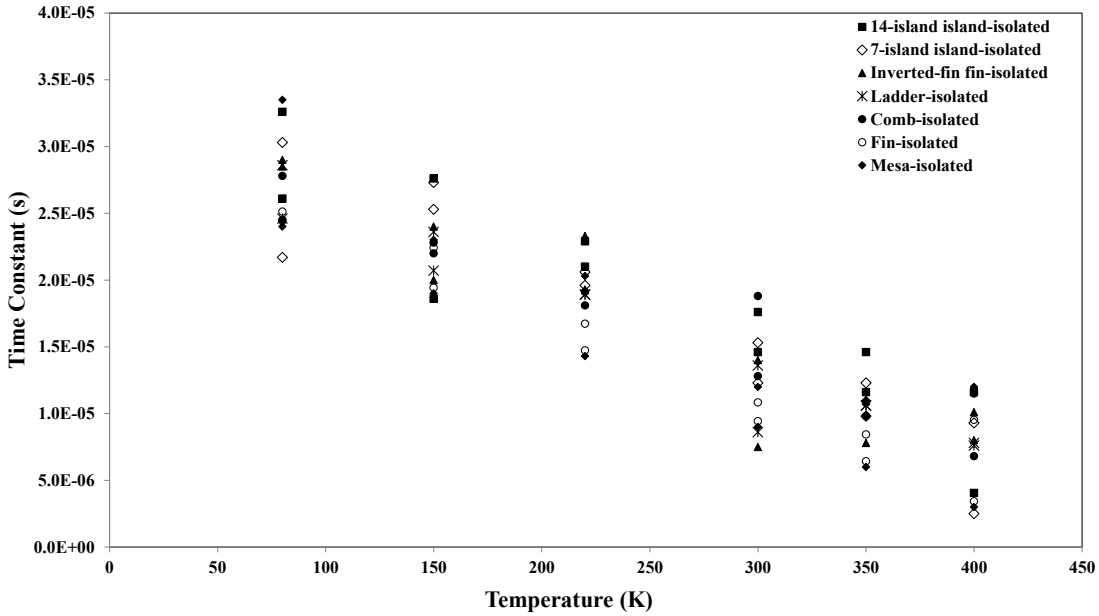


Figure 5.6 Calculated time constants of drain current recovery at 80, 150, 220, 300, 350, and 400 K for all types of devices explored in this study. In each case a number of seemingly identical devices are explored.

The data presented in Figure 5.6 illustrate that the relative variability among the time constants observed on macro-structurally identical devices masks any meaningful difference among the time constants of devices of different isolation feature geometry. As a result, this observation suggests a common phenomenon as the root cause for the gate-lag among the studied device varieties.

According to (5.2) and taking the average value of the time constants presented in Figure 5.6 at each measured temperature, the trap energy level for all of the studied device varieties is approximately evaluated to be equal to 60 meV. This trap energy level is indicative of the existence of a shallow trap level among these device types.

The fact that gate-lag is observed among all of the device varieties explored in this study is an indication of the presence of shallow trapping/detrapping centers among all these device types. For AlGaN/GaN epilayers an exhaustive number of trap levels of different varieties (i.e., deep or shallow, acceptor or donor) has been already reported in literature [122] - [124]. These traps are either induced by the growth conditions of the heterostructure or they are products of process damage. One of the processes which causes surface-damage and contributes to introduction of trap levels is the dry-etching used in the formation of the isolation-feature. The link between dry-etching of III-nitrides and formation of trap-states has been reported in a number of studies [125] - [128].

Since all of the explored device types were fabricated side by side one another (i.e., on the same epilayer), the typically observed differences presented in Figure 5.5 (i.e. in terms of the percentage of change in the pulsed-mode drain current during the gate-pulse) and the almost identical mean time constant of the detrapping process identify the involvement of a different number of traps of almost identical energy level responsible for the aforementioned gate-lag behaviors. As shown in Figure 5.5, mesa- and fin-isolated devices exhibit the lowest percentages of change in the pulsed-mode drain-current during the on-time of the gate pulse, while the highest changes were observed in island-, inverted-fin fin-, comb-, and ladder-isolated devices. Since throughout the processing of the devices studied in this chapter the only distinction among the device types is in term of the isolation-feature geometry, the damage of this processing step is deemed responsible for any difference observed among the gate-lag behaviors of these device types. As shown in Fig. 5.5, the device types with larger interfaces of the gate electrode with dry-etched sidewalls and GaN floors in between the isolation features (hence, those in which the gate is in the proximity of a larger number of trap sites) produce a larger percentage of change in the pulsed-mode drain current in comparison with mesa- and fin-isolated devices. The aforementioned differences in the exposure of gate to etched surfaces have been already highlighted in Figure 4.1.

According to these observations, trap levels introduced by the dry-etching process are deemed to be the origin of the observed gate-lag in the transistors explored in this study. Surface passivation after isolation step, for compensating the traps associated with plasma etch damage, seems to be the most promising solution to reduce the gate-lag in these device types.

5.3.2 R_{DS}-dispersion

As previously indicated in chapter 2, despite showing promising results as high-power amplifiers, the frequency-dispersion of the output resistance, which is commonly observed among AlGaN/GaN HFETs, is a cause for concern. Not unlike the gate-lag, degradation of the output resistance with the frequency of the excitation is a manifestation of the presence of electron trapping/detrapping at trap sites existing at different interfaces in the structure, buffer layer, or the surface. Depending on the time constants of these processes, traps fail to respond to the excitation frequency if it is higher than the counterpart identified by the inverse of this time constant.

Figure 5.7 illustrates the setup used in R_{DS}-dispersion measurements. Using the probe station, signal generator, and the oscilloscope identified in section 5.3.1, measurements were conducted at different temperatures starting from 80 K and following to 150, 220, 300, 350, and 400 K. In these measurements, the small-signal frequency of the AC signal generator was varied from 20 Hz to 20 MHz, while maintaining a quiescent gate bias of -1 V and drain bias of 10 V. The amplitude of the AC small-signal was 0.1 V. After each R_{DS}-dispersion measurement, the DC characteristics were verified versus the previously recorded characteristics to make sure that no significant degradation has taken place. According to Figure 5.7, R_{DS} is calculated using the following expression:

$$R_{DS} = \frac{\Delta(V_2).R_2}{\Delta(V_1 - V_2)} \tag{5.4}$$

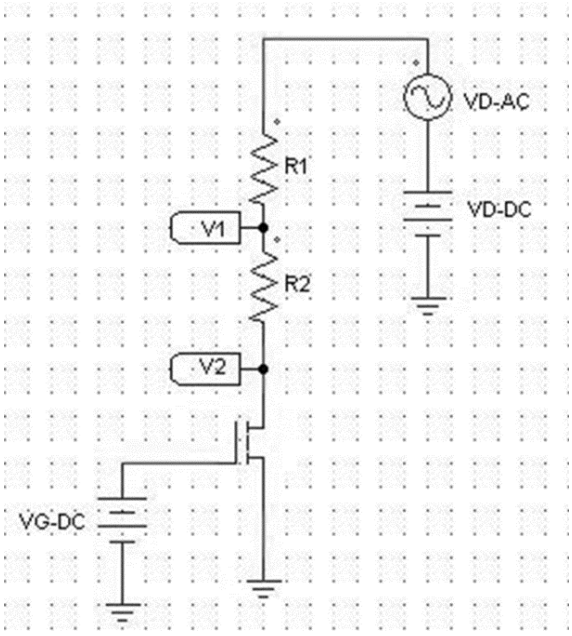


Figure 5.7 R_{DS} dispersion measurement setup. R_1 and R_2 are both 51 Ω.

All device types exhibited an R_{DS}-dispersion at all measurement temperatures. As a few examples, these dispersion characteristics for the case of 1 μm gate transistors of all of the aforementioned devices varieties tested at 80 K are presented in Figure 5.8. A resembling behavior is observed among devices of 0.5 μm gate-length.

Whereas the isolation technology among the studied devices differs in terms of the isolation-feature geometry, the almost identical presence of mean R_{DS}-dispersion among these devices indicates a common cause for this observation. Hence, R_{DS} dispersion is seemingly prompted by the presence of defects common among the device types. This common cause could be the pre-existing defects within the buffer. While in the epilayer structure used in the fabrication of the devices reported in this study the buffer layer is carbon-doped, this characteristic can be the common cause for the observed R_{DS}-dispersion. Although carbon-doped GaN buffer layers enjoy a higher resistance (hence, a smaller substrate leakage), they have been reported to suffer from the presence of doping-induced traps. Formation of very deep traps related to carbon-doping of GaN buffer layer was reported by Klein *et al.* [129] - [130]. AlGaN interlayer between GaN buffer and AlN nucleation layer is suggested to avoid negative results of the Carbon-doping of the GaN buffer layer [131].

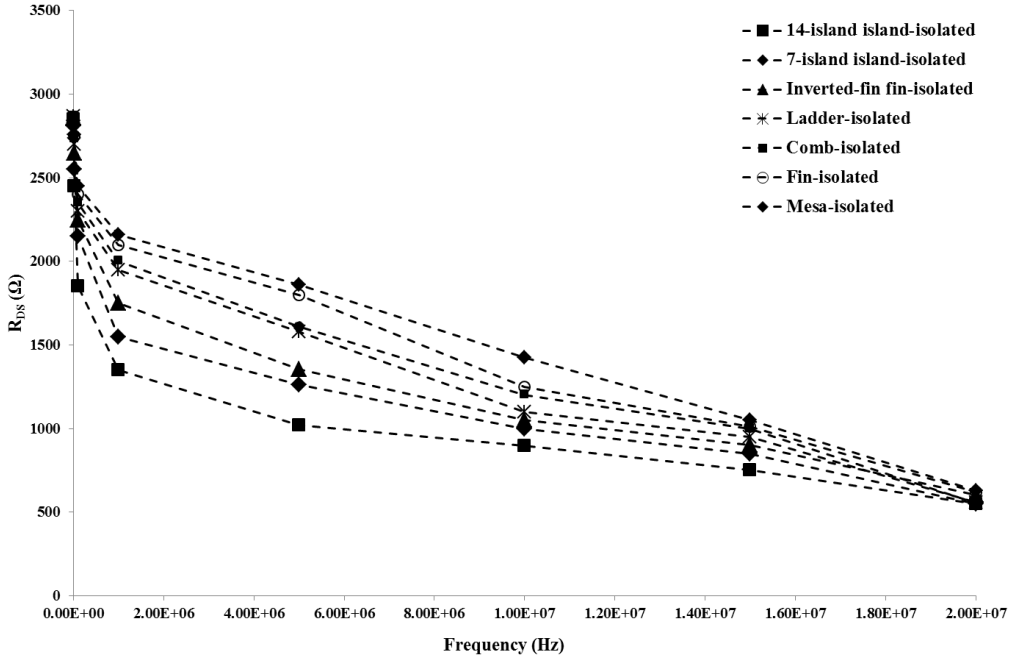


Figure 5.8 Variation of small-signal output-resistance versus frequency for 14-island island-isolated, 7-island island-isolated, inverted-fin fin-isolated, ladder-isolated, comb-isolated, fin-isolated, and mesa-isolated devices at 80 K.

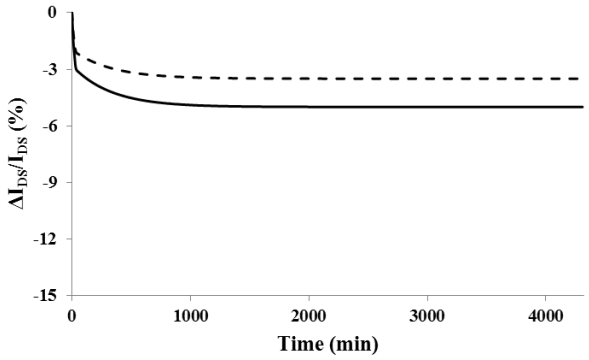
5.3.3 Long term stability of drain current drive

As indicated earlier, the gradual slump in the drain current drive of AlGaN/GaN HFETs upon long hours of operation is another major concern in commercialization of this technology. In order to assess the long term stability of the drain current drive of the transistors employing different isolation-feature geometries, each of these transistors was kept under DC bias in the on-state for more than 72 hours, while its current level was regularly monitored and recorded. DC stress tests were performed at room temperature and at two different values of drain bias of 10 and 15 V, while a constant gate bias of 0 V kept the channel open.

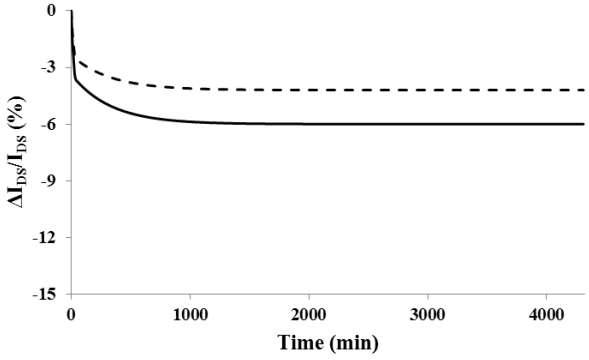
The percentage of change in the drain-current as a function of stress time, for devices presented in section 3.2 and the traditionally-sized mesa with gate-length of 1 μm, is presented in Figure 5.9. As observed in this figure, under these DC conditions the drain current had an almost instantaneous drop of 3 to 7 percent within the first few minutes of stress, while after this a slowly falling drain current was observed among all devices. In this regime, the devices that were stressed at higher drain voltages degraded with a smaller time constant. Since a higher drain voltage indicates a higher maximum electric-field in the drain access region, this can be an

indication of the role of hot carriers in inducing the degradation in the drain current. As shown in Figure 5.9, the drain current degradation takes on a saturating characteristic as the stress time prolongs. The level at which this saturation happens is different between the two cases of drain bias. This can be explained in terms of higher electric-field at the drain-edge of the gate and defect formation in the AlGaN barrier. At this saturating level the drain current showed a decrease of 5, 6, 6.5, 7.2, 9, 10, and 10.8% among mesa-isolated, fin-isolated, comb-isolated, ladder-isolated, inverted-fin fin-isolated, 7-island island-isolated, and 14-island island-isolated devices, respectively. The 14-island island-isolated device exhibits the highest degradation in drain-current while mesa-isolated device has the least drop in the drain-current. DC characteristics of the devices were measured after 24 hours and while the devices were kept at room temperature. Upon this de-stressing period, the drain-current was observed to have recovered for all device types, which indicates that no permanent damage such as crack formation under the gate electrode has happened during the experiments.

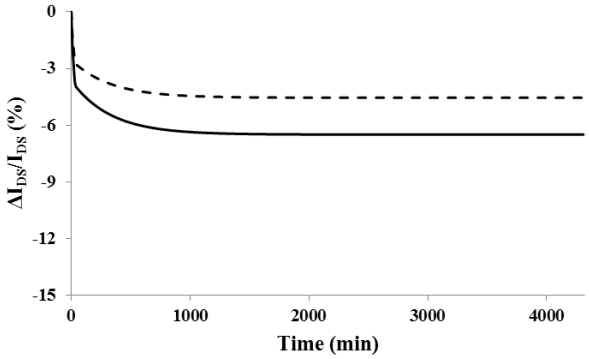
In agreement with the results from section 5.3.1, in Figure 5.9 it is observed that in device types with more dry-etched sidewalls and GaN floors in between the isolation features (which impose a higher number of traps on the gate-electrode), highest degradation in the DC drain current occurs.


0
-3
-6
-9
-12
-15
ΔIDS/IDS (%)
0
1000
2000
3000
4000
Time (min)

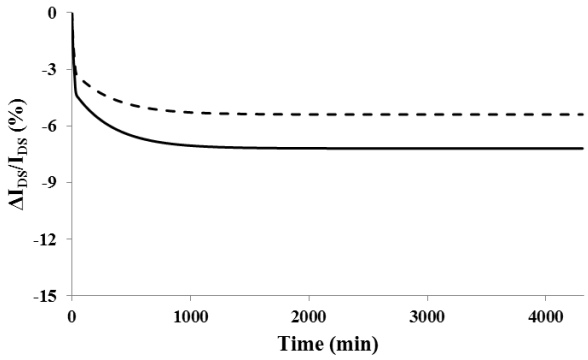
(a)


0
-3
-6
-9
-12
-15
ΔIDS/IDS (%)
0
1000
2000
3000
4000
Time (min)

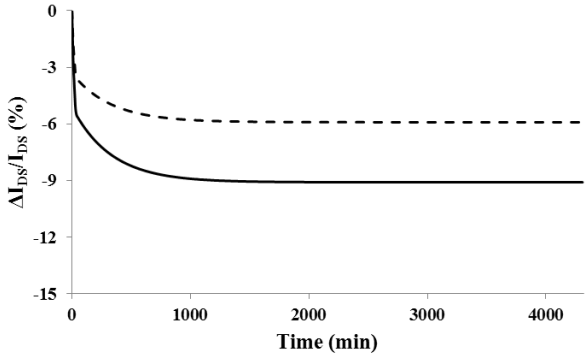
(b)


0
-3
-6
-9
-12
-15
ΔIDS/IDS (%)
0
1000
2000
3000
4000
Time (min)

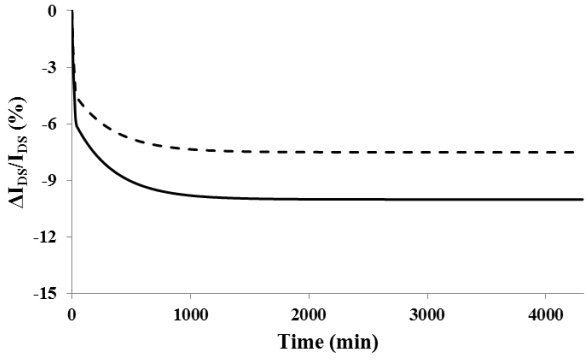
(c)


0
-3
-6
-9
-12
-15
ΔIDS/IDS (%)
0
1000
2000
3000
4000
Time (min)

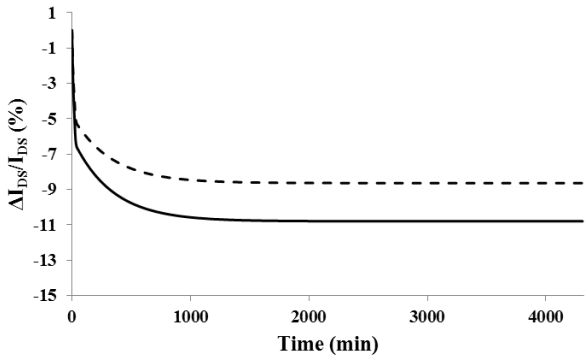
(d)


0
-3
-6
-9
-12
-15
ΔIDS/IDS (%)
0
1000
2000
3000
4000
Time (min)

(e)


0
-3
-6
-9
-12
-15
ΔIDS/IDS (%)
0
1000
2000
3000
4000
Time (min)

(f)



(g)

Figure 5.9 Degradation of drain-current as a function of stress time at 300 K for drain-voltage of 10 V (dashed line) and 15 V (solid line) for (a) mesa-isolated, (b) fin-isolated, (c) comb-isolated, (d) ladder-isolated, (e) inverted-fin fin-isolated, (f) 7-island island-isolated, and (g) 14-island island-isolated devices.

5.4 Conclusion

Gate-lag, R_{DS}-dispersion, and long term stability of the drain current among traditional and the newly proposed AlGaN/GaN HFETs of alternative isolation-feature geometry were experimentally investigated. All devices exhibited gate-lag with a time constant identified by the modified Arrhenius characteristics. Process damages (i.e., exposure of electrodes to additionally dry-etched sidewalls and dry-etched GaN floors in between the isolation features in island-, inverted-fin fin-, comb-, and ladder-isolated devices) are believed to be responsible for the observed gate-lag. Surface passivation is suggested to reduce gate-lag in the newly developed device types. R_{DS}-dispersion with frequency was also observed in all device types. Doping-induced trap-centers in the buffer layer are deemed responsible for this observation. Conventional mesa-isolation exhibited the best long-term stability among all of the explored isolation-feature geometries, which is speculated to be due to having the least amount of dry-etching caused damage to the heterostructure. The observed gate-lag, R_{DS}-dispersion, and degradation of the drain-current under the on-state condition provided an important link between the fabrication technology of these new device types and reliability concerns.

Chapter 6

Microfabrication of AlGaN/GaN HFETs and AlN/GaN MISFETs

6.1 Introduction

In this chapter, the process recipe developed for microfabrication of AlGaN/GaN HFETs and AlN/GaN MISFETs is presented. Far from being a routine microfabrication process, prompted by the variation of the operating conditions of different existing equipment and lack of process recipes developed by the manufacturers, any microfabrication facility is in need of developing its own combination of cleaning/etching/metallization recipes to realize III-nitride transistors. Variations in the composition and thickness of the cap layer, barrier, and also the channel layer, evidently demand re-tuning the parameters of this process recipe. This work was the first effort in the area of III-nitride processing at cleanroom facilities of McGill University. As a result, fabrication processes needed to be developed from the earliest stages. In section 6.2, process recipe development for microfabrication of AlGaN/GaN HFETs is described. Process recipe development for microfabrication of AlN/GaN MISFETs is presented in section 6.3. Conclusion is presented in section 6.4.

6.2 Process recipe development for microfabrication of AlGaN/GaN HFETs

In spite of the advantages of the application of wide bandgap III-nitrides to HFETs, which were previously outlined in chapter 2, difficulties in etching and obtaining Ohmic characteristics across the wide bandgap semiconductor, in addition to sensitivity of the polar 2DEG concentration to surface conditions (i.e., charge-status of surface states) have rendered the realization of III-nitride HFETs specially challenging.

The process recipe presented in this chapter has been developed for AlGaN/GaN HFET epilayers grown on sapphire, which have been purchased from Cree Inc. The choice of sapphire as the substrate (and not the more thermally conductive SiC substrate), is of economical reasons. A set of clear field photomasks, with different designs in terms of gate-width and gate length of 2 μm, was employed in defining the device features. An EVG620 mask aligner system with a 365 nm Hg i-line source was used for this purpose.

6.2.1 Sample preparation

The high sensitivity to surface conditions among III-nitrides aggravates the problems associated with cross-contamination. Over the past two decades a number of surface preparation/passivation-, etching-, and Ohmic contact-recipes have been proposed to solve these important challenges. It has been recognized that the exposed AlGaN surface plays a key role in the quality of Ohmic and Schottky contacts formed on AlGaN/GaN heterostructures [132] - [133]. Cleanliness of the surface is important not only to photoresist adhesion but also to proper device operation in terms of realization of etching profiles and metal-semiconductor contacts. The contamination layer, which is normally covering the AlGaN barrier, consists both of organic and inorganic contaminants including native oxide. The organic contaminants can be removed through bathing the sample in methanol, acetone, and propanol, and also through employing oxygen plasma descum (i.e., in a plasma asher). Native oxide and the other inorganic contaminants can be removed through HCl and HF bathing. HCl-based solutions have been shown to be more effective in removing oxides, while leaving less oxygen residue, whereas HF is more effective in removing carbon-based contaminants [134].

In this microfabrication process, in preparation of the wafers in smaller pieces for processing, wafers were covered by a protective photoresist layer before dicing in order to prevent deposition of the particles onto the samples. Dicing was done using ESEC 8003 dicing saw. To clean the samples after dicing, samples were submerged in acetone with ultrasonic agitation for at least 2 minutes followed by a 2 minutes isopropyl alcohol dip. After this step the samples were rinsed in DI water and then dried using a nitrogen gun. Following this step, these samples were optically inspected under microscope to ensure that both the photoresist and any particle created by the dicing process have been removed. This preparation procedure ensures that the surface is free of any debris from the wafer dicing or any other type of contaminants.

As the need for cleaning was outlined earlier in this section, dicing was followed by a more or less standard two step surface treatment procedure. This initial sample cleaning procedure includes [134]:

1) Organic contaminant removal using methanol, acetone, and propanol bath.
2) Inorganic contamination and native oxide removal using HCl:DI water (1:1) bath.

Succeeding the cleanings step, the samples were placed in a DI water bath for a few seconds, after which they were rinsed in streaming DI water and dried using a nitrogen gun. Once the sample surface is cleaned and dried, a dehydration bake was performed at about 150-200^{o}C for about 2 minutes to remove water from the sample surface. This dehydration bake should be performed after each cleaning step.

After dehydration bake, the sample was allowed to briefly cool before swiftly proceeding to spin coating with photoresist. The swift move to spin coating would greatly reduce the risks of rehydration or contamination of the samples and the growth of native oxide. After coating with photoresist, the samples underwent a soft-bake to remove the resist solvent and to increase the adhesion to the wafer.

6.2.2 Mesa isolation

Definition of the active device area, and realization of isolation between neighboring devices, is the next step in microfabrication of AlGaN/GaN HFETs. Often times, in this step through etching the epilayer (and essentially removing the 2DEG) in the passive areas of the wafer, electrical insulation between neighboring active areas (i.e., transistors) is established. The

electrical insulation between neighboring transistors can be achieved either through employing this so-called mesa-etching recipe (i.e., physical removal of the semiconductor between the neighboring transistors), or through amorphization of the AlGaN/GaN heterointerface in the passive area of the chip through ion implantation [135]. Due to unavailability of ion implanters in many of the III-V microfabrication facilities, the first solution is more main-stream.

Caused by the large bond-strength of most III-nitrides (i.e., in comparison to other compound semiconductors) physical etching of these materials, especially in absence of Al, has been proven challenging. A number of dry etching methods have been so far developed for etching GaN and its alloys [136] - [139]. In addition to the problems of dry etching, due to the exceptional bond strength and chemical stability of GaN, only a very limited indication of successful wet etching of GaN exists. These limited experiments rely on using KOH and NaOH aqueous at temperatures above 250 ºC [140]. Since these etching schemes are observed to offer etch sensitivity in the presence of defects (hence, capability of producing a grassy surface upon etching a material containing defects), wet etching of GaN in NaOH and molten KOH have been also employed in tallying the micro-defects such as dislocations and nano-pipes [29].

As a result of the aforementioned challenges in etching III-nitrides, a significant effort has been devoted to developing various dry etching techniques [141] - [145]. Dry-etching techniques used in III-nitride processing mostly rely on the chlorine-based ion bombardment etching. In order to achieve an acceptable etch rate, and a high-resolution anisotropic etch-profile, highly energized chlorine ions are required in these processes.

However, in light of the aforementioned sensitivity of the operation of polar AlGaN/GaN HFETs to surface conditions, the surface damage resulting from this physical etch is a considerable reliability concern. These concerns limit the applicable etching systems to electron cyclotron resonance (ECR), inductively coupled plasma (ICP), and magnetron reactive ion etching (MRIE), which through offering a higher plasma density relieve the energy requirement (and as a result the inflicted surface damage).

In the present work, after lithography, mesa etching was performed by using Cl_2/Ar plasma in an Applied-Materials P5000 magnetically-enhanced reactive ion etching (MERIE) system. Different recipes were explored on AlGaN/GaN epilayers to study the effect of process parameters on etch rate and surface morphology. These parameters include Cl_2 and Ar flow rate, chamber pressure, DC bias on the platen, and RF power. The most critical parameter affecting

the etch rate was found to be the RF power. Figure 6.1 shows the improvement of the etch rate with RF power. However, the improved etch rate at higher RF powers is accompanied by a larger surface damage. This is a factor that has been known to contribute to inter-mesa leakage, poor isolation, and ineffective gate action. It was also observed that the etch rate increases linearly with the flow rates of Ar. In developing the recipe for etching, samples were inspected under optical microscope and mesa height was measured using Ambios XP200 profiler.

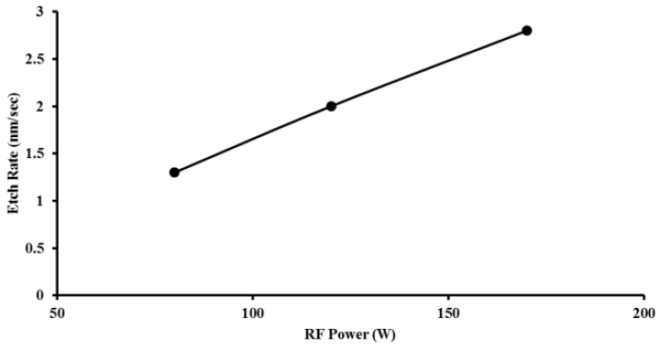
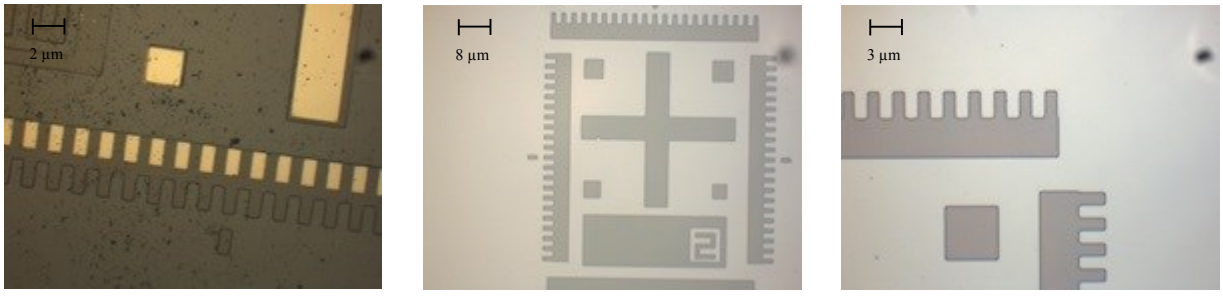


Figure 6.1 Etch rate versus RF power for MRIE process.

Figure 6.2 attempts to show the impact of different RF power levels on the surface morphology of the etched samples. Lower RF power seems to provide the best surface morphology and the least amount of defect seen as dark spots among these figures. However, the prolonged time required to perform the etching at low RF power level demands a thicker photoresist mask, which is in turn limiting to the etched feature's resolution. Considering this requirement, balancing between the two requirements, the RF power level of 120 W was deemed well suited for this process. The etch step-height and uniformity across the sample were characterized by means of an Ambios XP200 stylus profiler. Upon etching for 110 sec under these conditions, a mesa-height of 240 nm was achieved at an etch rate of 2 nm/sec.



(a) (b) (c)

Figure 6.2 Micrographs of alignment marks etched into AlGaN/GaN heterostructure using (a) 170 W, (b) 150 W (c) 120 W RF power in an MRIE chamber.

6.2.3 Ohmic Contacts

In order to take full advantage of the properties of AlGaN/GaN HFETs and to achieve high current densities, high extrinsic gain, and low Joule heating loss (i.e. to allow high temperature operation), it is essential to realize low resistance source and drain Ohmic contacts to the 2DEG. These contacts are expected to offer high thermal and chemical stability. Due to the wide bandgap of the AlGaN barrier, realization of these types of Ohmic contacts in the AlGaN/GaN system has been found to be challenging. However, as a result of an intensive research, over the past two decades alloyed Ohmic contacts of acceptable quality have become a reality in this material system.

In this metallization scheme, annealing the contact at high temperatures causes melting and mixing of the metal with the AlGaN barrier. This alloy formation process, however, produces a rough surface morphology, which in addition to limiting the line-edge definition, and as a result the minimum feature size, produces an unacceptable surface for interconnect formation. Consequently, in order to avoid these difficulties, Ohmic contacts formed to AlGaN/GaN heterostructures instead of using one metal layer, often take advantage of the presence of a stack of metals. Among the elements of this stack, only the layer touching the AlGaN barrier is envisioned to form an alloy with the semiconductor. This is while the other layers are there to protect this metal against oxidation, and to improve the overall surface morphology [146] - [147].

The metallization schemes used for making Ohmic contacts on AlGaN/GaN heterostructures are originally taken from the adjusted Ohmic contact processing implemented on n-type GaN. According to Schottky's theory and the experimental observations, in this situation best results are achieved using metals with relatively low work-function ($q\Phi_M$) as the first layer of Ohmic contact, whose nitride alloys are conductive and stable. Such properties are often optimally found in Titanium (i.e. with $q\Phi_M$=4.3 eV). Several metallization schemes (including Ti/Al/Ti/Au, Ti/Al/Pt/Au, Ti/Al/Ni/Au, Ti/Al/Cu/Au, where gold is the topmost layer) have been reported to form acceptable Ohmic contacts to AlGaN/GaN HFETs [134], [148] - [152]. Among these combinations, the Ohmic contact formation is based on the extraction of N from the AlGaN layer by Ti, throughout the high-temperature rapid thermal annealing process [153]. Upon formation of TiN, N-vacancies of the barrier act as n-type dopants in inducing a highly doped region near the metal interface. Pinning of the Fermi level at the energy level of the

N-vacancies, results in a tunneling-Ohmic behavior [154] - [155]. Creation of the TiN interfacial layer has been also reported to offer a thermally stable and low-resistive contact to the 2DEG [154] - [155].

The use of a Ti/Al layers, instead of a single Ti layer, is more commonly adapted. Al layer in this metallization scheme is known to react with Ti to form an Al_3Ti layer that prevents oxidation of the underlying Ti [156] and helps in contact formation [157]. Al has been also observed to react with the semiconductor to form AlN, resulting in N vacancies, which yield a heavily doped interface underneath the contact (hence, enabling electrons to tunnel easily to the 2DEG) [158]. As the topmost layer, Au is used to prevent oxidation of the Ti/Al bilayer, to improve the Ohmic contact's conductivity [159], and to guarantee long-term device stability. A blocking layer (such as Ni or Ti) is also needed to prevent high-temperature mixing of Au and Al (which produces a highly resistive alloy). This metal layer also plays an important role in forming a good surface morphology for the Ohmic contacts after annealing at high temperature [160].

Through optimizing the thickness of the metal layers and annealing conditions (i.e. maximum anneal temperature and duration of the exposure to this temperature), specific contact resistances (i.e. ρ_c) as low as 7.3×10^{-7} and 4.7×10^{-7} Ω-cm^2 have been achieved using Ti/Al/Ni/Au and Ti/Al/Mo/Au multi-layers, respectively [161] - [162].

Transmission line method (TLM) test patterns, which are illustrated in Figure 6.3, are commonly used in evaluating the electrical properties of Ohmic contacts. In addition to the specific contact resistance, TLM-based measurements produce insight into other electrical parameters such as the sheet resistance (i.e. R_s). This method was proposed by Reeves and Harrison in 1982 [163]. For the accuracy of TLM measurements, the rectangular TLM test patterns should sit on the mesa-isolated structure. This is because the mesa structure confines the current flow within one mesa and the current direction perpendicular to the edge of the metal contacts.

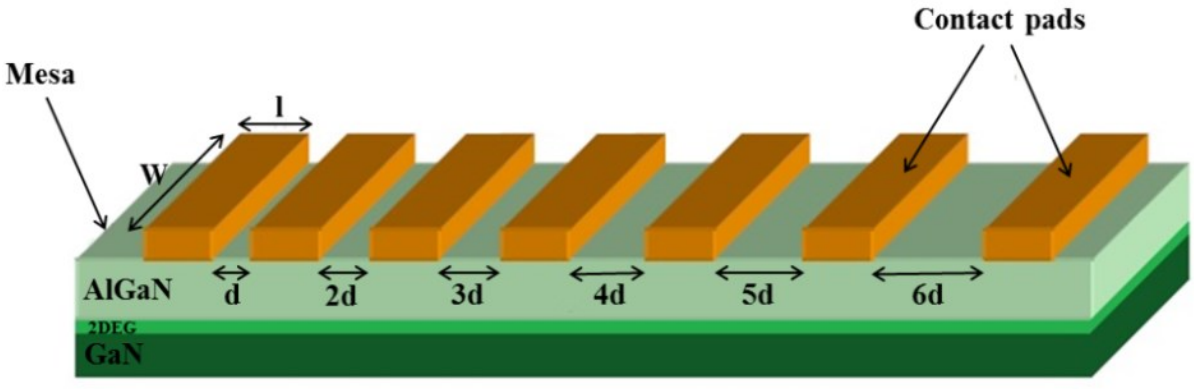


Figure 6.3 Typical TLM patterns.

As illustrated in Figure 6.4, according to theory of TLM, by applying a potential difference between the neighboring contact pads of variable distance (and recording the total resistance via measuring the current flowing across these contacts) the value of contact resistance (i.e., R_0) can be extracted. Table 6.1 presents the method for calculating the sheet resistance, transfer resistance, and specific contact resistance based on TLM measurements.

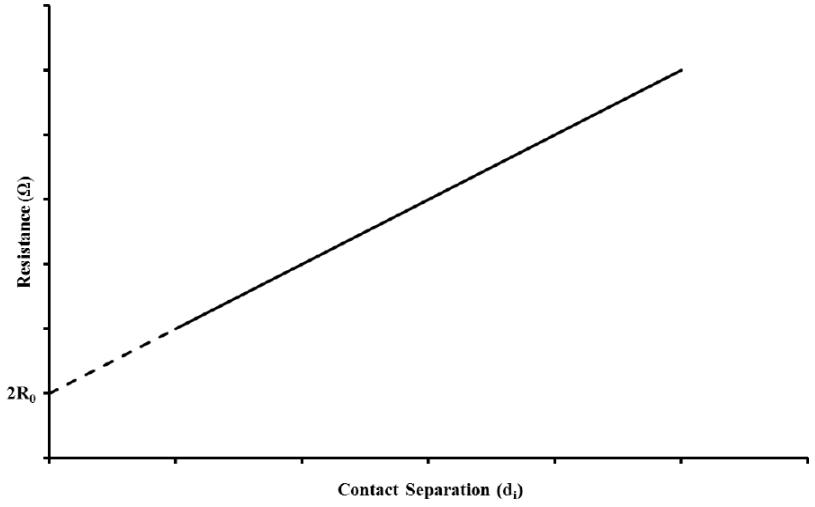


Figure 6.4 Resistance versus contact separation characteristic of the TLM measurement.

Table 6.1
Sheet resistance, transfer resistance, and specific contact resistance calculation based on TLM measurements.

Parameter	Unit	Derivation
Sheet Resistance (R_s)	Ω /□	Slope × W
Transfer Resistance (R_t)	Ω.mm	$R_0 \times W$
Specific Contact Resistance (ρ_c)	$\Omega.cm^2$	$(R_t)^2/R_s$

In the present work, through studying the effects of different metal combinations/thicknesses, and maximum annealing-temperature/time, Ohmic contact formation process to AlGaN/GaN HFETs of the previously indicated layer structure was adjusted.

Ohmic contacts were patterned through the lift-off process developed for a clear field-mask using the image reversal photoresist AZ5214. Developing this recipe for use on AlGaN/GaN epilayers grown on the transparent sapphire substrate was one of the early challenges of this microfabrication endeavor. This recipe has been developed for the first time at McGill's microfabrication facilities. Negatively sloped sidewall profile achieved in this step ideally suits the lift-off process. Perfecting this process required painstaking trial and error, and substantial modification to the manufacturer's standard recipe. Standard recipe for image reversal process of AZ5214 photoresist on Silicon substrate (which is provided by the manufacture), and the adjusted recipe for AlGaN/GaN HFET structures on sapphire substrate are summarized in Table 6.2.

Table 6.2
Standard and adjusted image reversal recipe parameters for AZ5214 photoresist.

Step	Standard Image Reversal Recipe	Adjusted Image Reversal Recipe
Soft Bake	50 sec at 110 ºC	55 sec at 90 ºC
Exposure	34 mJ/cm^2	2.5 mJ/cm^2
Reversal Bake	120 sec at 120 ºC	120 sec at 105 ºC
Flood Exposure	200 mJ/cm^2	250 mJ/cm^2
Develope	MF726 developer for 25 sec	MF726 developer for 25 sec
Post Bake	50 sec at 120 ºC	N/A

Figure 6.5 presents the processing steps of the image reversal recipe. Figure 6.6 illustrates the improvement in the lift-off metallization process achieved through optimization of the image reversal recipe. As shown in Figure 6.6(a), results show that performing the standard recipe of

AZ5214 for image reversal process creates crosslinking problems (i.e., the area covered by mask is also exposed so not being developed), which result in total failure of lift-off. In order to adjusted the image reversal recipe, first exposure dose was adjusted and then post bake temperature was adjusted for final recipe. Figures 6.6(b) presents the results after optimization of the exposure time. Figure 6.6(c) shows the results for the final recipe with the full set of adjusted values listed in Table 6.2. Development of all the fine features of the alignment marks is a testimony to the perfection of this recipe. Post baking of the samples made the lift off process difficult. As a result this step was eliminated.

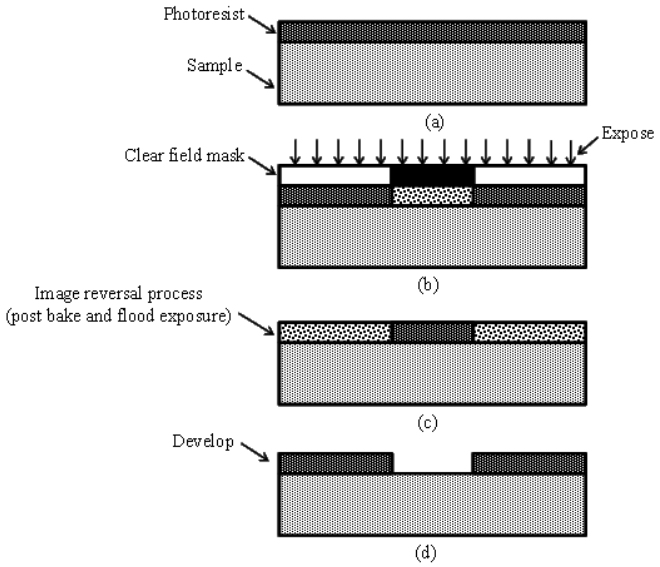
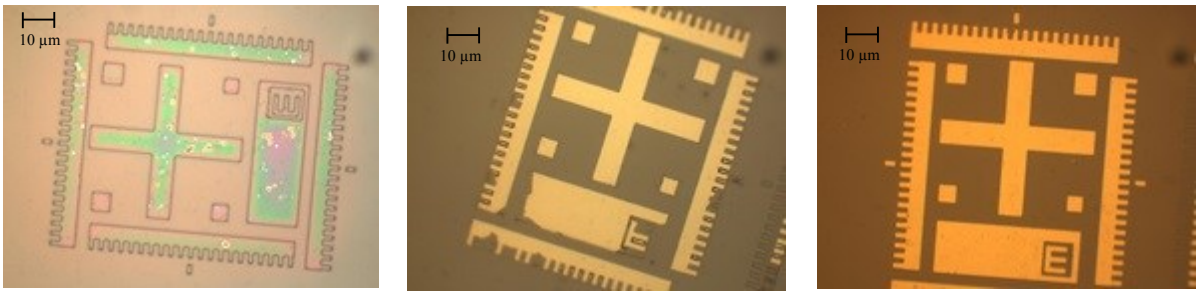


Figure 6.5 Process steps for image reversal recipe for AZ5214 photoresist: (a) coat and softbake (90 °C), (b) exposure, (c) post bake (105 °C) and flood exposure (250 mJ/cm^2), (d) develop.



(a) (b) (c)

Figure 6.6 Micrographs of the samples after lift-off process using (a) image reversal standard recipe, (b) adjusted exposure time recipe, (c) final adjusted recipe.

After the aforementioned patterning step of photoresist, electron-beam deposition of a four layer stack of Ti/Al/Ti/Au was used in this process. The succeeding lift-off process proceeds to removing the metal stack from the places that the metal is deposited on the photoresist.

Adjusted thickness of each metal layer, Ti:Al ratio and rapid thermal annealing temperature and duration, were determined through trial and error on a large number of AlGaN/GaN epilayers, and studying the Ohmic behavior using TLM patterns at room temperature.

Prior to the Ohmic contact deposition, the native oxide was removed by dipping the samples in $HCl:H_2O$ (1:1) solution for 30 seconds. The samples were then rinsed in DI water, dried with nitrogen gun, and immediately transferred into the chamber of a NEXDEP E-beam evaporator. To investigate the role of the Ti/Al ratio, the Al thickness was varied while the thicknesses of the first and the second Ti-layer, and the Au layer were set to 250, 100 and 500 Å. This selection is biased by the published data of other laboratories [164]. As shown in Figure 6.7, a Ti:Al thickness ratio of 1:6 was found to provide the best Ohmic contact performance among all the examined samples using the epilayer structure identified earlier in this chapter. Overall, it was observed that the lowest specific contact resistivity and Ohmic contact resistance can be obtained by evaporating respective thicknesses of 250/1500/100/500 Å for Ti/Al/Ti/Au.

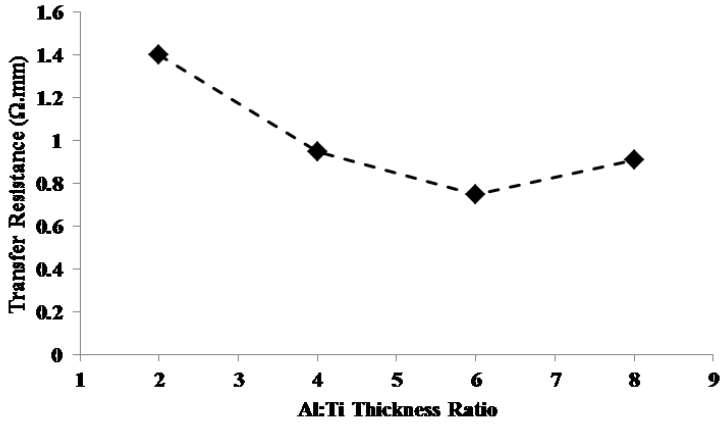


Figure 6.7 Transfer resistance versus Al:Ti ratio. Samples were annealed at 850°C for 30 seconds under N_2 ambient.

As previously mentioned, in addition to the thickness of each metal layer, annealing is a critical step in the formation of Ohmic contacts. Since annealing the Ohmic contact at the required temperatures higher than 800ºC introduces several reliability problems in the device performance (such as lateral overflow and rough surface morphology), annealing conditions required a thorough examination. Annealing temperature, slope of the ramp, and duration were adjusted to form low resistance Ohmic contacts with excellent surface morphology. Better surface morphology was observed for a slower ramp. Figure 6.8 illustrates the adjusted process

recipe for RTA in which the samples were annealed in JetFirst200 rapid thermal annealing (RTA) system at 850°C for 30 seconds under N_2 ambient with the flow rate of 4000 sccm/min. In order to prevent temperature overshoot a two-step ramp up process was defined in the recipe.

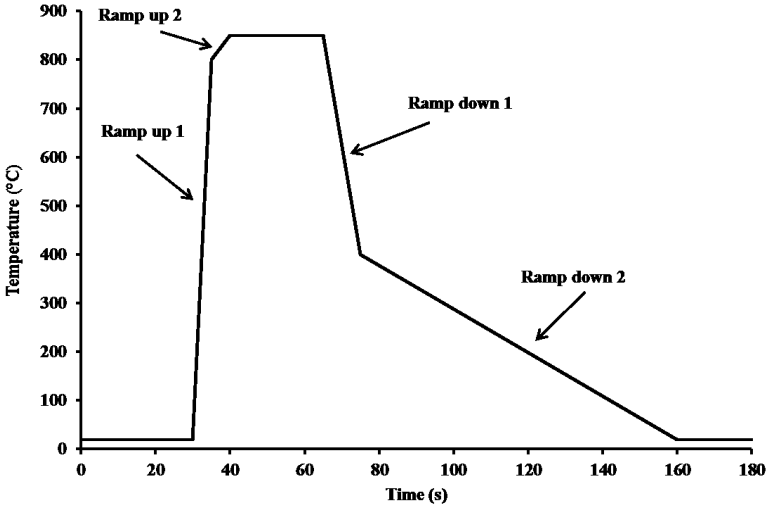


Figure 6.8 Adjusted recipe for RTA using JetFirst200 rapid thermal annealing system.

Figure 6.9 shows micrographs of the TLM patterns for different annealing conditions. In this work, the Ohmic contact resistance was measured on the linear TLM test structures using Keithley 4200-SCS Semiconductor Characterization System at room temperature. Figure 6.10 illustrates the resistance plotted against TLM contact spacing.

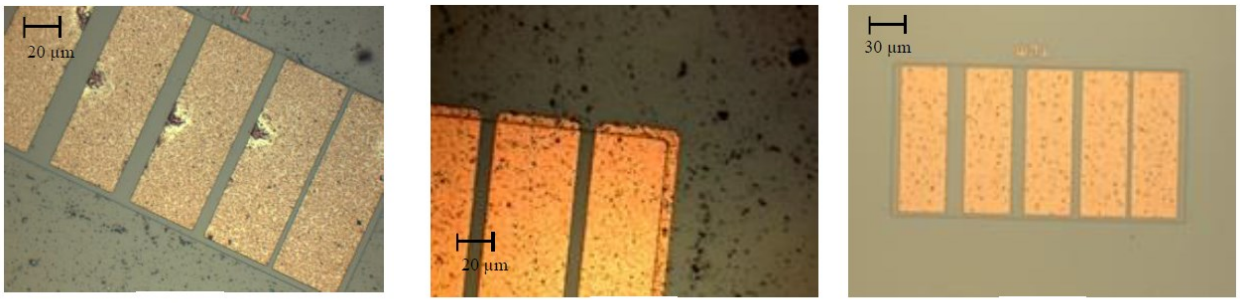


Figure 6.9 Micrographs of TLM patterns after (a) 30 sec at 900 ºC (b) 30 sec at 870 ºC, (c) 30 sec at 850 ºC of rapid thermal annealing.

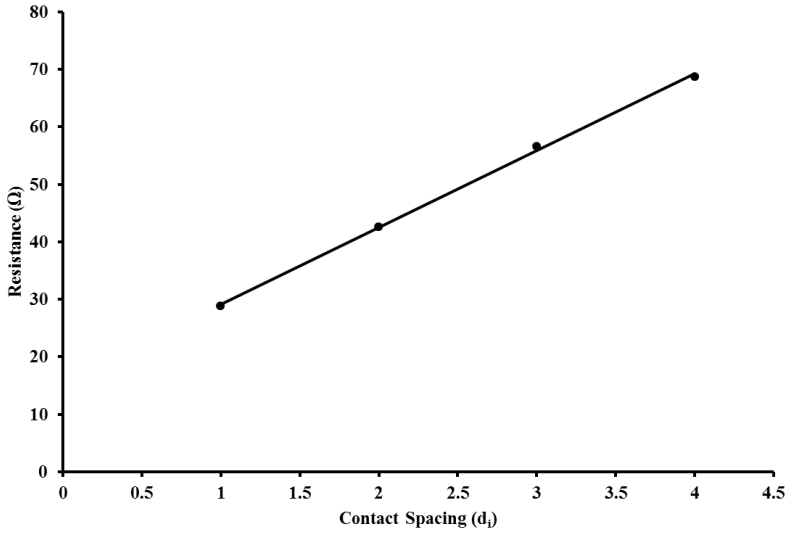


Figure 6.10 Resistance plotted versus TLM contact spacing. Transfer resistance is 0.75 Ω.mm and sheet resistance is 1310 Ω /□.

6.2.4 Schottky contact

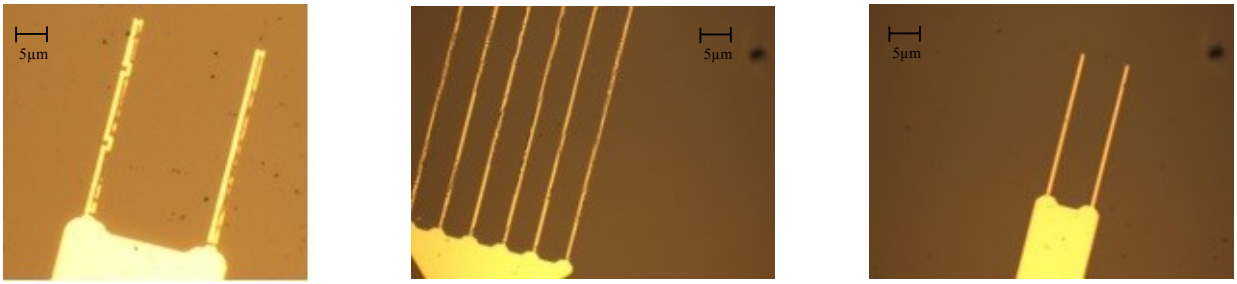
The need for a low-leakage gate contact, capable of maintaining electrostatic integrity of the gate, is determinant to the choice of a large work-function metal as the gate electrode of AlGaN/GaN HFETs. This requirement is also further boosted by the need to modify the highly populated polar channel of AlGaN/GaN HFETs to ideally reduce the standby power to zero. As expressed earlier, although the polar-nature of AlGaN/GaN HFETs produces a D-mode HFET characteristic, the need for reducing the power consumption is pushing for modifying this character at least in parts of the III-nitride chip to an enhancement-mode (or E-mode) character. In this regard, one of the explored avenues is defined in terms of the use of a large work-function gate metal, and extension of gate's depletion region throughout the 2DEG channel. Some of the typical values of Schottky barrier height achieved to AlGaN barriers of different Al-compositions are: 1.1 eV for Pt [165], 1.15 eV for Au [166], 0.6 eV for Ti [167], 0.94 eV for Pd [168], and 0.99 eV for Ni [169]. Table 6.3 presents metal work-functions of different metals explored in GaN technology [170].

Table 6.3
Contact characteristics of a number of explored metals in processing of n-Type GaN along with their metal work-function [170].

Metal	Metal Work Function (eV)	Contact Behaviour
Sc	3.50	Ohmic
Hf	3.90	Ohmic
Zr	4.05	Ohmic
Al	4.28	Ohmic
V	4.30	Ohmic
Nb	4.30	Slightly rectifying
Ti	4.33	Slightly rectifying
Cr	4.50	Slightly rectifying
W	4.55	Slightly rectifying
Mo	4.60	Slightly rectifying
Ag	4.26	Schottky
Cu	4.65	Schottky
Co	5.00	Schottky
Au	5.10	Schottky
Pd	5.12	Schottky
Ni	5.15	Schottky
Pt	5.65	Schottky

Whereas large work-function metals such as Pt and Ni are the suitable candidates for the first gate metal layer, not unlike the Ohmic contacts, this high work function metal is usually covered by the high-conductivity/low-reactivity over-layer of Au. In III-nitride processing, despite having a lower metal work function, Ni has been employed more often than Pt. One major reason for using Ni over Pt is the stronger adhesion of Ni to AlGaN.

In this work, 500/500 Å of Ni/Au was evaporated using NEXDEP e-beam evaporator as the gate contact. Same lift-off process as Ohmic contact was used for patterning. Figure 6.11 presents the micrograph of the patterned gate-fingers for a number of multiple-gate-finger transistors. Using the adjusted lift-off process, the fine 2 μm gates were quite acceptably realized across the sample (Figure 6.9(c)).



(a) (b) (c)

Figure 6.11 Micrographs of the gate fingers on the samples after lift-off process using (a) image reversal standard recipe, (b) adjusted exposure time recipe, and (c) final adjusted recipe.

6.2.5 Interconnect contacts and device characteristics

For on-chip characterization of the microfabricated AlGaN/GaN HFETs contact pads had to be evaporated on these devices. Since the pads are to withstand the wear and tear of probing, especially for high temperature stability testing, they have to be mechanical stable with ability to perform at high temperatures. In this project, 500 Å of Ti and Au was evaporated using the e-beam evaporator to make the pads. This was follow by the same lift-off process as the previous two metallization steps. Figure 6.12 presents micrographs of a variety of 2- and multi-finger AlGaN/GaN HFETs fabricated at McGill's microfabrication facilities. Figure 6.13 illustrated a typically observed DC drain and gate current-voltage (*I–V*) characteristics. Devices demonstrate a pinch-off voltage slightly smaller than -4 V, and a superb saturation and knee voltage characteristics. A maximum drain current of 0.6 A/mm was observed for L_G=2 µm. Figure 6.14 presents a typically observed extrinsic gate-transconductance characteristics of the device with the variation of the gate–source voltage.

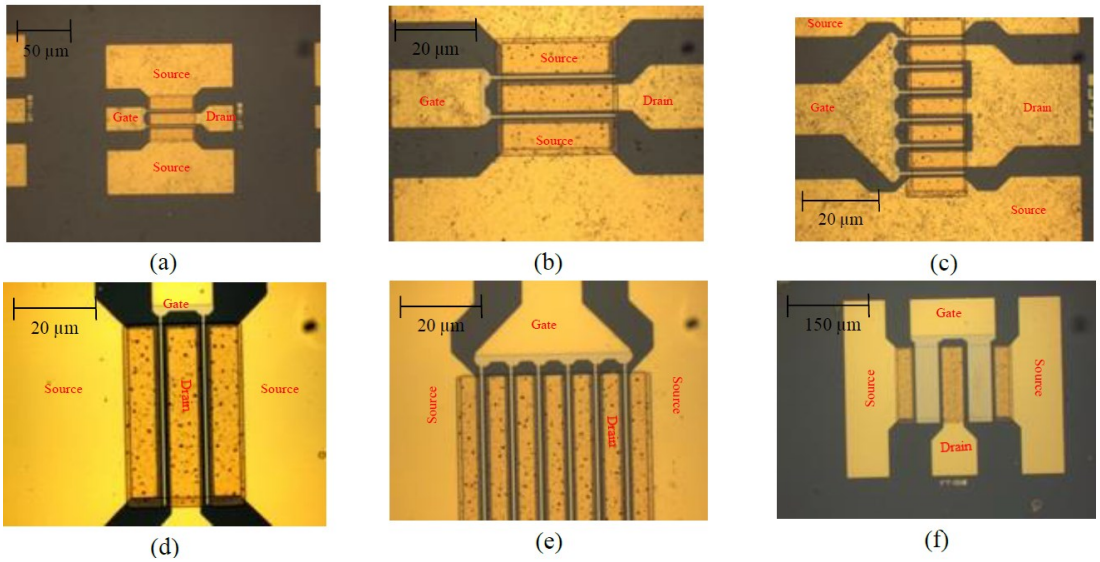


Figure 6.12 Micrographs of a number of microfabricated devices.

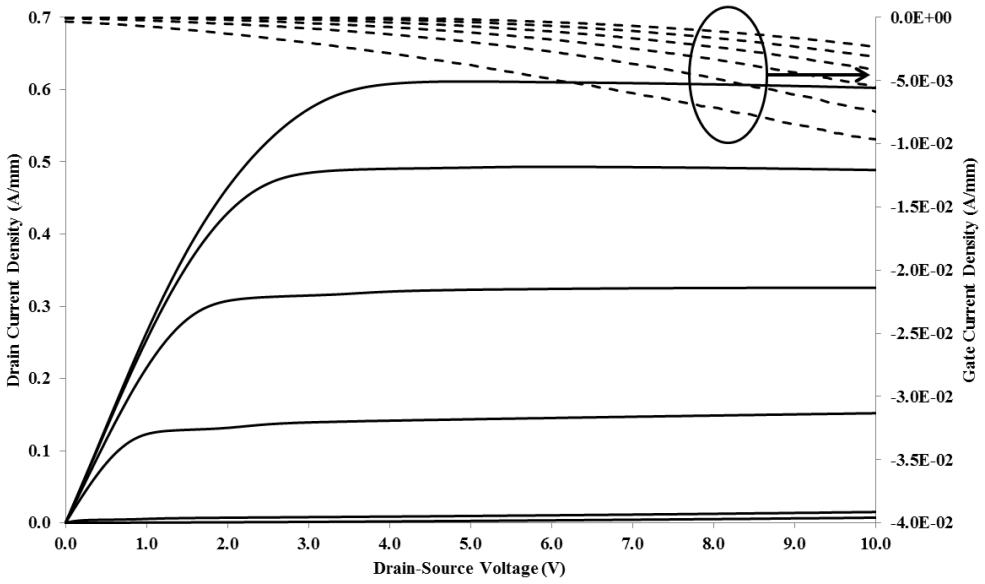


Figure 6.13 Typically observed drain and gate current density versus drain-source voltage of the fabricated AlGaN/GaN HFETs. V_{GS} varies from −5 to 0 V, with a step of 1 V. Gate-length is 2 µm.

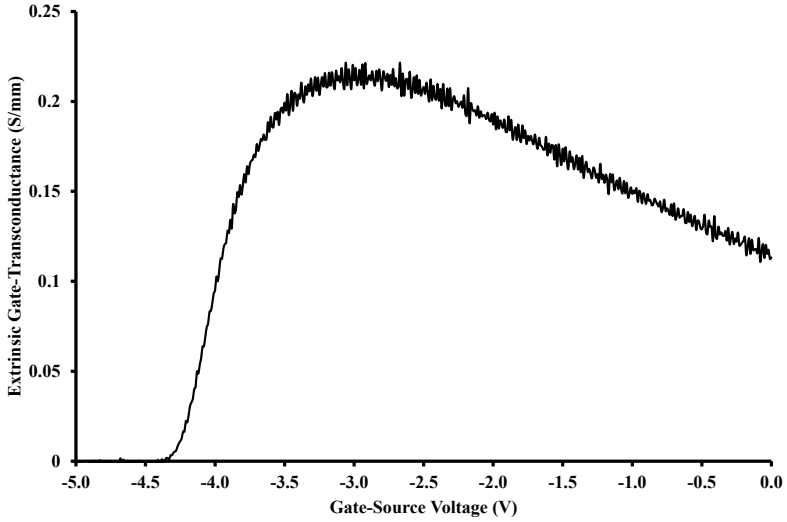


Figure 6.14 Typically observed extrinsic gate-transconductance versus gate-source voltage characteristic of the fabricated AlGaN/GaN HFETs. Gate-length is 2 μm and drain–source voltage is 7 V.

Table 6.4 presents the details of the developed AlGaN/GaN HFET microfabrication process recipe. Challenges and solutions are also detailed in this table. A full disclosure of all the details of processing is presented in Appendix A.

Table 6.4
Process steps of device microfabrication along with the challenges and solution in each step.

Process step	Challenges	Solutions
Wafer dicing	1) Dicing residue	1) Photoresist protective layer has been used before dicing. 2) Ultrasonic agitation performed. 3) Optical inspection under microscope performed.
Sample cleaning	1) Organic contamination 2) Inorganic contamination 3) Native oxide layer	1) A two-step cleaning process performed.
Mask cleaning	1) Photoresist residues	1) Optical inspection under microscope after cleaning process performed.
Mesa isolation	1) Standard recipe of photoresist does not work due to transparent substrate(i.e. Sapphire) 2) Recipe for GaN etch not included in predefined recipes of MERIE	1) AZ5214 photoresist recipe developed. 2) GaN etch recipe developed and adjusted.
Ohmic contacts formation	1) Clear-field mask set needs either negative photoresist or image reversal process 2) Negative photoresist makes the lift-off process tough due to positive slope of the features 3) Recipe for RTA process is not included in predefined recipes of the equipment 4) Samples need to be immediately transferred into the vacuum system for metal deposition to prevent native oxide formation	1) Image reversal recipe developed and adjusted. 2) RTA recipe developed and adjusted. 3) Thin Silicon wafer used in order to reach 850 °C.
Schottky gate contact formation	1) Sensitivity of the image reversal recipe to the post bake temperature 2) Due to small features of the mask cross-linking happened	1) Site coater's hotplate used for accurate post bake temperature 2) Exposure time has been adjusted.
Interconnect contact formation		

6.3 Process recipe development for microfabrication of AlN/GaN MISETs

Formation of a good Ohmic contact to the 2DEG of AlN/GaN epilayers is more difficult than achieving Ohmic contact across the AlGaN/GaN epilayers. This is due to the wider bandgap of AlN (i.e. 6.2 eV). This issue has been one of the major challenges in fabricating high

performance AlN/GaN MISFETs, and is yet to be overcome. Contact resistances as low as 0.36 Ω.mm was reported by Xing et al. on an AlN/GaN sample with a 3 nm thick AlN barrier. In the same study, it has also been shown that Ohmic contact formation on AlN/GaN heterostructures mostly depends on the sheet resistance of the channel [171].

In the present study we attempted fabricating AlN/GaN samples of thicker barriers in the order of 10 nm. The thicker barrier, although making the Ohmic contact formation more challenging, is expected to yield higher polar 2DEG concentration, less gate-leakage, and better drain current drive. While up until recently the growth challenges have inhibited the pseudomorphic growth of a thick tensile-strained AlN barrier on GaN, lately promising results on the growth of these structures have been made available [172].

Since the number of the AlN/GaN samples of these characteristics which were made available to the present study was limited to two, it was decided to apply the same recipe developed for AlGaN/GaN HFETs for the microfabrication of AlN/GaN MISFETs. Following this recipe, after the cleaning process, the samples were etched to realize mesa isolation. The etch rate was found to be 1.9 nm/sec, based on which a 228 nm mesa height was realized. The optical observations demonstrated the etch steps to be uniform across the samples with very low surface damage. As for the next step, the same Ohmic metal stack of Ti/Al/Ti/Au of corresponding thicknesses 250/1500/100/500 Å was evaporated and annealed with the same condition as indicated in section 6.2.3. Figure 6.15 illustrates the resistance plotted against TLM contact spacing. As can be seen in this figure the AlN/GaN samples suffer from very high sheet resistance of 2080 Ω/□. This can be due to the problems during the growth stage, or high sensitivity of the surface to the chemicals used during the process. Next, 500/500 Å of Ni/Au was evaporated using NEXDEP e-beam evaporator as the gate contact. Same lift-off process as Ohmic contact was used for patterning. Finally, 500/500 Å of Ti/Au was evaporated using the e-beam evaporator to make the pads. This was follow by the same lift-off process as the previous two metallization steps.

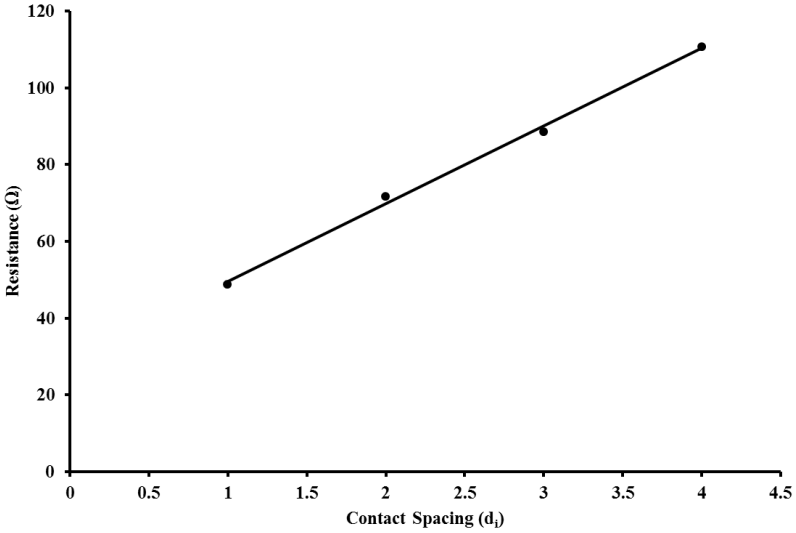


Figure 6.15 Resistance plotted versus TLM contact spacing. Transfer resistance is 1.5 Ω.mm and sheet resistance is 2080 Ω /□.

Figure 6.16 illustrates a typically observed DC drain and gate current-voltage (*I–V*) characteristics. Devices demonstrate a pinch-off voltage slightly smaller than -6 V, and a superb saturation and knee voltage characteristic. A maximum drain current of 0.11 mA/mm was observed for device with gate-length of 2 µm. Figure 6.17 presents a typically observed extrinsic gate-transconductance versus gate-source voltage characteristic of device. Due to much higher Ohmic contact and sheet resistance of fabricated AlN/GaN MISFET compared to the fabricated AlGaN/GaN HFET, this device is showing a much lower current density. Due to limited number of AlN/GaN MISFET samples, Ohmic contact optimization could not be further studied.

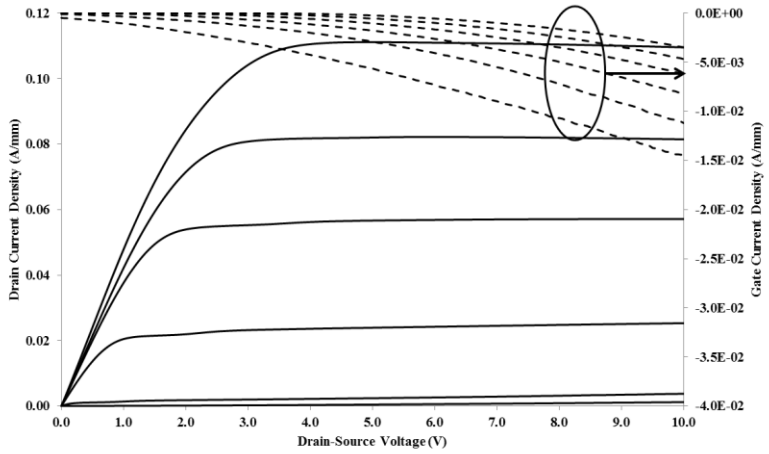


Figure 6.16 Typically observed drain and gate current density versus drain-source voltage of the fabricated AlN/GaN MISFETs. V_{GS} varies from −5 to 0 V, with a step of 1 V. Gate-length is 2 µm.

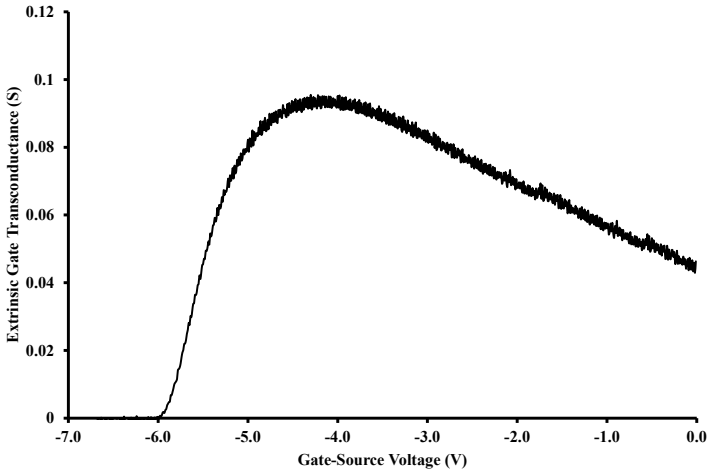


Figure 6.17 Typically observed extrinsic gate-transconductance versus gate-source voltage characteristic of the fabricated AlN/GaN MISFETs. Gate-length is 2 μm and drain–source voltage is 7 V.

6.4 Conclusion

Process recipes were developed for microfabrication of AlGaN/GaN HFETs and AlN/GaN MISFETs at cleanroom facilities of McGill University. The fabricated AlGaN/GaN HFET with gate length of 2 μm demonstrated maximum drain current density of 0.6 mA/mm and transconductance of 0.22 S/mm. The fabricated AlN/GaN MISFET with gate length of 2 μm demonstrated maximum drain current density of 0.11 mA/mm and transconductance of 0.1 S/mm.

Chapter 7

Concluding remarks, contributions, and future work suggestions

The research work of this thesis is focused on microfabrication and characterization of AlGaN/GaN HFETs with alternative isolation features and microfabrication and characterization of AlN/GaN MISFETS.

7.1 Concluding remarks

In chapter 3, a new approach for reducing self-heating in AlGaN/GaN HFETs was presented. According to FEA and electrical measurement of average channel temperature of AlGaN/GaN HFETs of different isolation features, an improved heat-dissipation was observed in devices enjoying a more distributed nature of the 2DEG channel. Observations also indicate a more distinct gain in thermal management for devices with shorter gate-length. Results suggest that self-heating in island-isolated AlGaN/GaN HFETs can be completely ruled out by reducing the island-width beyond a threshold value.

In chapter 4, it was shown that the correlation between the isolation-feature geometry and the observed shift in the pinch-off voltage is not fully explicable in terms of a tri-gate effect. The reported observations of this study suggest a link between the increase in the perimeter-to-area ratio of the cross-section of the isolation-feature, and an improved positive-shift in the pinch-off voltage. It has turned out that the 2DEG sheet concentration depends strongly on the device width and the gate structure.

In chapter 5, Gate-lag, R_{DS}-dispersion, and degradation characteristics of newly proposed AlGaN/GaN HFETs were experimentally investigated. All devices exhibited gate-lag and R_{DS}-dispersion with frequency. Exposure of electrodes to additionally dry-etched sidewalls and dry-etched GaN surfaces in between the isolation features of the new device types, presence of trapping centers induced by growth conditions of the structure, pre-existing defects in the epilayer, and carbon doping-related defects in the buffer layer are believed to be responsible for gate-lag and R_{DS}-dispersion in these devices. Degradation of the drain-current of these newly proposed devices under on-state condition is also studied. In this regard, conventional mesa-isolation exhibits the highest performance among all isolation technologies, which is speculated to be due to imposing the lowest amount of dry-etched damage.

In chapter 6, the process recipe developed for microfabrication of AlGaN/GaN HFETs and AlN/GaN MISFETs is presented. Fabricated devices exhibit acceptable drain current density and extrinsic gate-transconductance.

7.2 Contributions

Chapter 3:

The contributions of this work include the followings,

- A new approach for reducing self-heating in AlGaN/GaN HFETs was presented for the first time.
- Correlation between the geometry of the isolation feature and average channel temperature of AlGaN/GaN HFETs is investigated
- Correlation between gate-length and the surface area of the isolation pattern and self-heating is investigated.

Chapter 4:

The main contributions of this work are as follows,

- Correlation between the isolation-feature geometry and the DC current-voltage characteristics of AlGaN/GaN HFETs is investigated.

- Through implementation of six different geometries for isolation-features of polar AlGaN/GaN HFETs, the correlation between the isolation-feature geometry and the observed shift in pinch-off voltage was investigated.
- The average 2DEG sheet concentration and tri-gate effect was simulated for devices with different body widths.

Chapter 5:

The contributions of this work include the followings,

- Gate-lag, R_{DS}-dispersion, and degradation characteristics of newly proposed AlGaN/GaN HFETs are experimentally investigated.

Chapter 6:

The main contributions of this work are as follows,

- Process recipe for microfabrication of AlGaN/GaN HFETs and AlN/GaN MISFETs was developed and adjusted at McGill University's microfabrication facilities.
- DC characteristics of in-house microfabricated AlGaN/GaN HFETs and AlN/GaN MISFETs is investigated.

7.3 Future work suggestions

The following future works are suggested for the continuing study of III-nitride HFETs,

1. Study of island-isolated AlGaN/GaN HFETs of smaller island sizes

The high-power dissipation in AlGaN/GaN HFETs induces a self-heating in the active layers. Self-heating does not only limit the electron transport by enhancing the phonon scattering which results in decreasing the carrier mobility and electron saturation velocity but also damages the gate. Results from chapter 3 suggest that the self-heating issues in island-isolated AlGaN/GaN can be effectively ruled out by reducing the island-width beyond a threshold value. In this study, the minimum dimensions were limited by the foundry's constraints. Such an experimental investigation of island-isolated AlGaN/GaN HFET with island-width of 12.5 nm or lower using E-beam lithography can be considered as a complementary study of self-heating in this type of devices.

2. Polarization-engineered AlGaN/GaN HFETs

As mentioned earlier in chapter 4, III-nitride based devices normally operate in depletion-mode. Reduction of the carrier-concentration of the 2DEG is necessary in order to realize enhancement-mode devices in this technology. This can be achieved through appropriate design with more distributed 2DEG channel and larger perimeter-to-area ratio which were also pointed out in chapter 4. Such an experimental investigation can be considered as a complementary study.

Bibliography

[1] U. Mishra, L. Shen, T. Kazior, and Y. Wu, "GaN-based RF power devices and amplifiers," *Proc. of the IEEE*, vol. 96, no. 2, pp. 287-305, Feb. 2008.

[2] J. Wu, W. Walukiewicz, K. Yu, J. Ager III, E. Haller, H. Lu, W. Schaff, Y. Saito, and Y. Nanishi, "Unusual properties of the fundamental bandgap of InN," *App. Phys. Lett.*, vol. 80, no. 21, pp. 3967-3969, May 2002.

[3] M. Levinshtein, S. Rumyantsev, and M. Shur, *Properties of advance semiconductor materials*, J. Wiley and sons, 2001.

[4] www.gansystems.com, accessed Nov. 2013.

[5] U. Mishra, P. Parikh, and Y. Wu, "AlGaN/GaN HEMTs-An overview of device operations and applications," *Proc. of the IEEE*, vol. 90, no. 6, pp. 1022-1031, June 2002.

[6] O. Ambacher, J. Smart, J. Shealy, N. Weimann, K. Chu, M. Murphy, W. Schaff, L. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, and J. Hilsenbeck, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures," *J. Appl. Phys.*, vol. 85, no. 6, pp. 3222-3233, Mar. 1999.

[7] M. Khan, J. Kuznia, D. Olson, W. Schaff, J. Burm, and M. Shur, "Microwave performance of a 0.25 μm gate AlGaN/GaN heterostructure field effect transistor," *App. Phys. Lett.*, vol. 65, no. 9, pp. 1121-1123, Aug. 1994.

[8] C. Chen, S. Keller, E. Haberer, L. Zhang, S. DenBaars, E. Hu, and U. Mishra, "Cl_2 reactive ion etching for gate recessing of AlGaN/GaN field-effect transistors," *J. Vac. Sci. Technol. B*, vol. 17, no. 6, pp. 2755-2758, Nov. 1999.

[9] M. Neuburger, T. Zimmermann, E. Kohn, A. Dadgar, F. Schulze, A. Krischill, M. Gunther, H. Witte, J. Blasing, A. Krost, I. Daumiller, and M. Kunze, "Unstrained AlInN/GaN FET," *Int. J. High Speed Electron. Syst.*, vol. 14, no. 3, pp. 785-790, Sept. 2004.

[10] T. Palacois, A. Chakraborty, S. Heikman, S. Keller, S. DenBaars, and U. Mishra, "AlGaN/GaN high electron mobility transistors with InGaN back-barriers," *IEEE Electron Device Lett.*, vol. 27, no. 1, pp. 13-15, Jan. 2006.

[11] M. Micovic, P. Hashimoto, M. Hu, I. Milosavljevic, J. Duvall, P. Willadsen, W.Wong, A. Conway, A. Kurdoghlian, P. Deelman, J. Moon, A. Schmitz, and M. Delaney, "GaN double heterojunction field effect transistor for microwave and millimeter wave power applications," *IEDM Tech. Dig.*, pp. 807-810, Dec. 2004.

[12] F. Recht, L. McCarthy, S. Rajan, A. Chakraborty, C. Poblenz, A. Corrion, J. Speck, and U. Mishra, "Non-alloyed Ohmic contacts in AlGaN/GaN HEMTs by ion implantation with reduced activation annealing temperature," *IEEE Electron Device Lett.*, vol. 27, no. 4, pp. 205-207, Apr. 2006.

[13] M. Werquin, N. Vellas, Y. Guhel, D. Cucatteau, B. Boudart, J. Pesant, Z. Bougrioua, M. Germain, J. De Jaeger, and C. Gaquiere, "First results of AlGaN/GaN HEMTs on sapphire substrate using an argon-ion implant isolation technology," *Microw. Opt. Technol. Lett.*, vol. 46, no. 4, pp. 311-315, Aug. 2005.

[14] Y. Cai, Y. Zhou, K. Lau, and K. Chen, "High performance enhancement-mode AlGaN/GaN HEMTs using fluoride-based plasma treatment," *IEEE Electron Device Lett.*, vol. 26, no. 7, pp. 435-437, July 2005.

[15] K. Ohi and T. Hashizume, "Drain current stability and controllability of threshold voltage and subthreshold current in a multi-mesa-channel AlGaN/GaN high electron mobility transistor," *Jpn. J. Appl. Phys.*, vol. 48, no. 8, pp. 081002-1-081002-5, Aug. 2009.

[16] M. Alsharef, R. Granzner, and F. Schwierz, "Theoretical investigation of trigate AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3355-3341, Oct. 2013.

[17] P. Valizadeh and B. AlOtaibi, "Fin-and island-isolated AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 58, no. 2, pp. 1404-1407, May 2011.

[18] I. Smorchkova, L. Chen, T. Mates, L. Shen, S. Heikman, B. Moran, S. Keller, S. DenBaars, J. Speck, and U. Mishra, "AlN/GaN and (Al, Ga) N/AlN/GaN two-dimensional electron gas structures grown by plasma-assisted molecular-beam epitaxy," *J. Appl. Phys.*, vol. 90, no. 10, pp. 5196-1-5196-6, Aug. 2001.

[19] S. Taking, D. MacFarlane, and E. Wasige, "AlN/GaN MOS-HEMTs with thermally grown Al_2O_3 passivation," *IEEE Trans. Electron Devices*, vol. 58, no. 5, pp. 1418-1424, May 2011.

[20] T. Zimmermann, D. Deen, Y. Cao, J. Simon, P. Fay, D. Jena, and H. Xing, "AlN/GaN insulated-gate HEMTs with 2.3 A/mm output current and 480 mS/mm transconductance," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 661-664, July 2008.

[21] D. Deen, T. Zimmermann, Y. Cao, D. Jena, and H. Xing, "2.3 nm barrier AlN/GaN HEMTs with insulated gates," *Phys. Status Solidi (C)*, vol. 5, no. 6, pp. 2047-2049, May 2008.

[22] J. Chung, O. Saadat, J. Tirado, X. Gao, S. Guo, and T. Palacios, "Gate-recessed InAlN/GaN HEMTs on SiC substrate with Al_2O_3 passivation," *IEEE Electron Device Lett.*, vol. 30, no. 9, pp. 904-906, Sept. 2009.

[23] Y. Yue, Z. Hu, J. Guo, B. Sensale-Rodriguez, G. Li, R. Wang, F. Faria, T. Fang, B. Song, X. Gao, S. Guo, T. Kosel, G. Snider, P. Fay, D. Jena, and H. Xing, "InAlN/AlN/GaN HEMTs with regrown Ohmic contacts and f_T of 370 GHz," *IEEE Electron Device Lett.*, vol. 33, no. 7, pp. 988-990, July 2012.

[24] R. Wang, P. Saunier, Y. Tang, T. Fang, X. Gao, S. Guo, G. Snider, P. Fay, D. Jena, and H. Xing, "Enhancement-mode InAlN/AlN/GaN HEMTs with 10^{-12} A/mm leakage current and 10^{12} on/off current ratio," *IEEE Electron Device Lett.*, vol. 32, no. 3, pp. 309-311, Mar. 2011.

[25] R. Wang, G. Li, G. Karbasian, J. Guo, B. Song, Y. Yue, Z. Hu, O. Laboutin, Y. Cao, W. Johnson, G. Snider, P. Fay, D. Jena, and H. Xing, "Quaternary barrier InAlGaN HEMTs with f_T /f_{max} of 230/300 GHz," *IEEE Electron Device Lett.*, vol. 34, no. 3, pp. 378-380, Mar. 2013.

[26] R. Wang, G. Li, J. Verma, B. Sensale-Rodriguez, T. Fang, J. Guo, Z. Hu, O. Laboutin, Y. Cao, W. Johnson, G. Snider, P. Fay, D. Jena, and H. Xing, "220-GHz quaternary barrier InAlGaN/AlN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 32, no. 9, pp. 1215-1217, Sept. 2011.

[27] S. Imanaga and H. Kawai, "Simulation of the piezoelectric effect on the device characteristics of AlGaN/GaN insulated-gate heterostructure field effect transistors," *Jpn. J. Appl. Phys.*, vol. 37, no. 11, pp. 5906-5913, Nov. 1998.

[28] S. Seo, "High frequency MIS-based III-nitride transistor and integrated bio-sensor technology," Ph.D. dissertation, Univ. Michigan, Ann Arbor, MI, 2009.

[29] H. Morkoç, *Handbook of Nitride Semiconductors and Devices, vol. 1: Materials Properties, Physics and Growth*, Weinheim: Wiley, 2009.

[30] S. Strite and H. Morkoç, "GaN, AlN, and InN: A review," *J. Vac. Sci. Technol. B*, vol. 10, pp. 1237-1266, July 1992.

[31] F. Fichter, "Uber Aluminiumnitrid," *Z. Anorg. Chem.*, vol. 54, p. 322, 1907.

[32] R. Juza and H. Hahn, "Über die kristallstrukturen von Cu_3N, GaN und InN metallamide und metallnitride," *Z. Anorg. Chem.*, vol. 239, no. 3, pp. 282-287, Oct. 1938.

[33] H. Maruska and J. Tietjen, "The preparation and properties of vapor-deposited single-crystal-line GaN," *Appl. Phys. Lett.*, vol. 15, no. 10, pp. 327-329, Nov. 1969.

[34] H. Manasevit and F. Erdmann, "The use of metalorganics in the preparation of semiconductor materials, IV. The Nitrides of Aluminum and Gallium," *J. Elecchem. Soc.*, vol. 18, no. 11, pp. 1864-1867, Nov. 1971.

[35] I. Akasaki and I. Hayashi, "The use MBE in the preparation of semiconductor materials," *Ind. Sci. Tech.*, vol. 17, pp. 48-52, 1976.

[36] K. Ploog, O Brandt, H. Yang, B. Yang, and A. Trampert "Nucleation and growth of GaN layers on GaAs, Si, and SiC substrates," *J. Vac. Sci. Technol. B*, vol. 16, no. 4, pp. 2229-2236, July 1998.

[37] S. Yoshida, S. Misawa, and S. Gonda "Improvements on the electrical and luminescent properties of reactive molecular beam epitaxially grown GaN films by using AlN-coated sapphire substrates," *Appl. Phys. Lett.*, vol. 42, no. 5, pp. 427-429, Mar. 1983.

[38] H. Amano, N. Sawaki, I. Akasaki, and Y. Toyoda "Metalorganic vapor phase epitaxial growth of a high quality GaN film using an AlN buffer layer," *Appl. Phys. Lett.*, vol. 48, no. 5, pp. 353-355, Feb. 1986.

[39] H. Amano, I. Akasaki, K. Hiramatsu, N. Koide, N. Sawaki, "Effects of the buffer layer in metalorganic vapour phase epitaxy of GaN on sapphire substrate," *Thin Solid Films*, vol. 163, pp. 415-420, Dec. 1988.

[40] L. Liu and J. Edgar, "Substrates for gallium nitride epitaxy," *Mater. Sci. Eng.: R-Rep.*, vol. 37, no. 3, pp. 61-127, Apr. 2002.

[41] T. Hino, S. Tomiya, T. Miyajima, K. Yanashima, S. Hashimoto, and M. Ikeda, "Characterization of threading dislocations in GaN epitaxial layers," *App. Phy. Lett.*, vol. 76, no. 23, pp. 3421-3423, June 2000.

[42] S. Ren and J. Dow "Lattice-matching SiC substrates with GaN," *Appl. Phys. Lett.*, vol. 69, no. 2, pp. 251-253, July 1996.

[43] C. Wood and D. Jena, *Polarization Effects in Semiconductors: From Ab Initio Theory to Device Applications*, Springer, 2008.

[44] S. Kukushkin, A. Osipov, V. Bessolov, B. Medvedev, V. Nevolin, and K. Tcarik "Substrates for epitaxy of Gallium nitride: new materials and techniques," *Rev. Adv. Mater. Sci.*, vol. 17, pp. 1-32, Mar. 2008.

[45] S. Adachi, *Properties of Group-IV, III-V and II-VI Semiconductors*, John Wiley and Sons, Chichester, England, 2005.

[46] F. Bernardini, V. Fiorentini, and D. Vanderbilt, "Spontaneous polarization and piezoelectric constants of III-V nitrides," *Phys. Rev. B*, vol. 56, no. 16, pp. Rl-0-024-Rl-0-027, Oct. 1997.

[47] E. Yu and E. Manasreh, "Spontaneous and piezoelectric polarization in nitride heterostructures," *III-V Nitride Semiconductors: Applications and Devices (Optoelectronic Properties of Semiconductors and Superlattices)*, pp. 161-193, Taylor & Francis, 2003.

[48] U. Mishra and J. Singh, *Semiconductor device physics and design*, Springer, 2008.

[49] Y. Wei, Z. Renping, D. Yandong, H. Weihua, and Y. Fuhua, "Analysis of the Ohmic contacts of Ti/Al/Ni/Au to AlGaN/GaN HEMTs by the multi-step annealing process," *J. Semicon.*, vol. 33, no. 6, pp. 064005-1-064005-6, June, 2012.

[50] Y. Cao and D. Jena, "High-mobility window for two-dimensional electron gases at ultrathin AlN/GaN heterojunctions," *Appl. Phys. Lett.*, vol. 90, no. 18, p. 182112-1-182112-3, Apr. 2007.

[51] R. Trew, D. Green, and J. Shealy, "AlGaN/GaN HFET reliability," *IEEE Microwave*, vol. 10, no. 4, pp. 116-127, June 2009.

[52] M. Shur, R Gaska, and A Bykhovski, "GaN-based electronic devices," *Solid-State Electron.*, vol. 43, no. 8, pp. 1451-1458, Aug. 1999.

[53] R. Vetury, N. Zhang, S. Keller, and U. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 560-566, Mar. 2001.

[54] P. Valizadeh and D. Pavlidis, "Low frequency noise-based monitoring of the effects of RF and DC stress on AlGaN/GaN MODFETs," *proc. of GaAs IC Symp.*, pp. 78-81, Nov. 2003.

[55] X. Hu, A. Koudymov, G. Simin, J. Yang, M. Khan, A. Tarakji, M. Shur, and R. Gaska, "Si_3N_4/AlGaN/GaN-metal-insulator-semiconductor heterostructure field effect transistors," *App. Phys. Lett.*, vol. 79, no. 17, pp. 2832-2834, Oct. 2001.

[56] H. Leier, A. Vescan, R. Dietrich, A. Wieszt, and H. Sledzik, "RF characterisation and transient behaviour of AlGaN/GaN power HFETs," *IEICE Trans. Electron.*, vol. E84-C, no. 10, pp. 1442-1447, Oct. 2001.

[57] G. Simin, A. Koudymov, A. Tarakji, X. Hu, J. Yang, M. Asif Khan, M. Shur, and R. Gaska, "Induced strain mechanism of current collapse in AlGaN/GaN heterostructure field-effect transistors," *Appl. Phys. Lett.*, vol. 79, no. 16, pp. 2651-2653, Oct. 2001.

[58] S. Arulkumaran, T. Egawa, H. Ishikawa, and T. Jimbo, "Comparative study of drain-current collapse in AlGaN/GaN high-electron mobility transistors on sapphire and semi-insulating SiC," *Appl. Phys. Lett.*, vol. 81, no. 16, pp. 3073-3075, Oct. 2002.

[59] H. Kim, A. Vertiatchikh, R. Thompson, V. Tilak, T. Prunty, J. Shealy, and L. Eastman, "Hot electron induced degradation of undoped AlGaN/GaN HFETs," *Microelectron. Rel.*, vol. 43, no. 6, pp. 823-827, June 2003.

[60] W. Lu, V. Kumar, R. Schwindt, E. Piner, and I. Adesida, "A comparative study of surface passivation on AlGaN/GaN HEMTs," *Solid-State Electron.*, vol. 46, no. 9, pp. 1441-1444, Sept. 2002.

[61] B. Green, K. Chu, E. Chumbes, J. Smart, J. Shealy, and L. Eastman, "The effect of surface passivation on the microwave characteristics of undoped AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 21, no. 6, pp. 268-270, June 2000.

[62] W. Tan, P. Houston, P. Parbrook, G. Hill, and R. Airey, "Comparison of different surface passivation dielectrics in AlGaN/GaN heterostructure field-effect transistors," *J. Phys. D: Appl. Phys.*, vol. 35, no. 7, pp. 595-598, Apr. 2002.

[63] T. Kikkawa, M. Nagahara, N. Okamobo, Y. Tatero, Y. Yamaguchi, and N. Hara, "Surface-charged controlled AlGaN/GaN power HFET without current collapse and g_m dispersion," *IEDM Tech Dig.*, pp. 585-588. Dec. 2001.

[64] W. Saito, Y. Kakiuchi, T. Nitta, Y. Saito, T. Noda, H. Fujimoto, A. Yoshioka, T. Ohno, and M. Yamaguchi, "Field-plate structure dependence of current collapse phenomena in high-voltage GaN-HEMTs," *IEEE Electron Device Lett.*, vol. 31, no. 7, pp. 659-661, July 2010.

[65] A. Edwards , J. Mittereder, S. Binari, D Scott Katzer, D. Storm, and J. Roussos, "Improved reliability of AlGaN-GaN HEMTs using an NH_3 plasma treatment prior to SiN passivation," *IEEE Electron Deice Lett.*, vol. 26, no. 4, pp. 225-227, Apr. 2005.

[66] L. Shen, R. Coffie, D. Buttari, S. Heikman, A. Chakraborty, A. Chini, S. Keller, S. DenBaars, U. Mishra, "High-power polarization-engineered GaN/AlGaN/GaN HEMTs without surface passivation," *IEEE Electron Device Lett.*, vol. 25, no. 1, pp. 7-9, Jan. 2004.

[67] N. Tsurumi, H. Ueno, T. Murata, H. Ishida, Y. Uemoto, T. Ueda, K. Inoue, and T. Tanaka, "AlN passivation over AlGaN/GaN HFETs for surface heat spreading," *IEEE Trans. Electron Devices*, vol. 57, no. 5, pp. 980-985, May 2010.

[68] O. Mitrofanov, M. Manfra, "Mechanisms of gate lag in GaN/AlGaN/GaN high electron mobility transistors," *Superlattices and Microstruct.*, vol. 34, no. 1-2, pp. 33-35. July 2003.

[69] P. Klein, S. Binari, K. Ikossi-Anastasiou, A. Wickenden, D. Koleske, R. Henry, and D. Katzer, "Investigation of traps producing current collapse in AlGaN/GaN high electron mobility transistors," *Electron. Lett.*, vol. 37, no. 10, pp. 661-662, May 2001.

[70] X. Zhou, Z. Feng, L. Wang, Y. Wang, Y. Lv, S. Dun, S. Cai, "Impact of bulk traps in GaN buffer on the gate-lag transient characteristics of AlGaN/GaN HEMTs," *Solid-State Electron.*, vol. 100, pp. 15-19, Oct. 2014.

[71] N. Braga, R. Mickevicius, R. Gaska, M. Shur, M. Khan, and G. Simin, "Simulation of gate lag and current collapse in gallium nitride field-effect transistors," *Appl. Phys. Lett.*, vol. 85, no. 20, pp. 4780-4782, Nov. 2004.

[72] H. Kim, J. Lee, and W. Lu, "Post-annealing effects on trapping behaviors in AlGaN/GaN HEMTs," *phys. status solidi (a)*, vol. 202, no. 5, pp. 841-845, Apr. 2005.

[73] T. Hashizume, J. Kotani, A. Basile, and M. Kaneko, "Surface control process of AlGaN for suppression of gate leakage currents in AlGaN/GaN heterostructure field effect transistors," *Jpn. J. Appl. Phys.*, vol. 45, no. 4, pp. L111-L113, Jan. 2006.

[74] E. Miller, X. Dang, and E. Yu, "Gate leakage current mechanisms in AlGaN/GaN heterostructure field-effect transistors," *J. Appl. Phys.*, vol. 88, no. 10, pp. 5951-5958, Nov. 2000.

[75] J. Zhang, J. Yuan, Y. Ma, and A. Oates, "Surface roughness effect on gate leakage and C-V characteristics of deep submicron MOSFETs," *Integrated Reliability Workshop*, California, USA, pp. 133-136, Jan. 2001.

[76] S. Arulkumaran, T. Egawa, H. Ishikawa, T. Jimbo, and Y. Sano, "Surface passivation effects on AlGaN/GaN high-electron-mobility transistors with SiO_2 , Si_3N_4 , and silicon oxynitride," *Appl. Phys. Lett.*, vol. 84, no. 4, pp. 613-615, Jan. 2004.

[77] G. Meneghesso, G. Verzellesi, F. Danesin, F. Rampazzo, F. Zanon, A. Tazzoli, M. Meneghini, and E. Zanoni, "Reliability of GaN high-electron-mobility transistors: state of the art and perspectives," *IEEE Trans. Dev. Mat. Rel.*, vol. 8, no. 2, pp. 332-343, June 2008.

[78] H. Kim, J. Lee, D. Liu, and W. Lu, "Gate current leakage and breakdown mechanism in unpassivated AlGaN/GaN high electron mobility transistors by post-gate annealing," *Appl. Phys. Lett.*, vol. 86, no. 14, pp. 143505-1-143505-3, Mar. 2005.

[79] Y. Oshimura, K.Takeda, T. Sugiyama, M. Iwaya, S. Kamiyama, H. Amano, I. Akasaki, A. Bandoh, and T. Udagawa, "AlGaN/GaN HFETs on Fe-doped GaN substrates," *Phys. Status Solidi (c)*, vol. 7, no. 7-8, pp. 1974-1976, July 2010.

[80] M. Belousov, B. Volf, J. Ramer, E. Armour, and A. Gurary, "In situ metrology advances in MOCVD growth of GaN-based materials," *J. Crys. Growth*, vol. 272, no. 1-4, pp. 94-99, Dec. 2004.

[81] J. Neugebauer, C. Van de Walle, "Atomic geometry and electronic structure of native defects in GaN," *Phys. rev. B*, vol. 79, no. 11, pp. 8067-8070, Sept. 1994.

[82] T. Mukai, K. Takekawa, and S. Nakamura, "InGaN-based blue light-emitting diodes grown on epitaxially laterally overgrown GaN substrates," *Jpn. J. Appl. Phys.*, vol. 37, no. 7, pp L839-L841, July 1998.

[83] M. Piazza, C. Dua, M. Oualli, E. Morvan, D. Carisetti, and F. Wyczisk, "Degradation of TiAlNiAu as Ohmic contact metal for GaN HEMTs," *Microelectron. Rel.*, vol. 48, no. 9-11, pp. 122-1225, Sept. 2009.

[84] Y. Chou, D. Leung, I Smorchkova, M. Wojtowicz, R. Grundbacher, L. Callejo, Q Kan, R. Lai, H. Liu, D. Eng, and A. Oki, "Degradation of AlGaN/GaN HEMTs under elevated temperature life testing," *Microelectron. Rel.*, vol. 44, no. 7, pp 1033-1038, July 2004.

[85] N. Miura, T. Nanjo, M. Suita, T. Oishi, Y. Abe, T. Ozeki, H. Ishikawa, T. Egawa, and T. Jimbo, "Thermal annealing effects on Ni/Au based Schottky contacts on n-GaN and AlGaN/GaN with insertion of high work function metal," *Solid-State Electron.*, vol. 48, no. 5, pp. 689-695, May 2004.

[86] S. Singhal, J. Roberts, P. Rajagopal, T. Li, A. Hanson, R. Therrien, J. Johnson, J. Kizilyalli, and K. Linthicum, "GaN-on-Si failure mechanisms and reliability improvements," *Proc. of 44th Annual IEEE International Rel. Phys. Sym.*, San Jose, CA, USA, pp. 26-30 Mar. 2006.

[87] Y. Okamoto ,Y. Ando, K. Hataya, T. Nakayama, H. Miyamoto, T. Inoue, M. Senda, K. Hirata, M. Kosaki, N. Shibata, and M. Kuzuhara, "Improved power performance for a recessed-gate AlGaN–GaN heterojunction FET with a field-modulating plate," *IEEE Trans. on Microw. Theory Tech.*, vol. 52, no. 11, pp. 2536-2540, Nov. 2004.

[88] J. del Alamo and J. Joh, "GaN HEMT reliability," *Microelectron. Rel.*, vol. 49, no. 9-11, pp. 1200-1206, Sep. 2009.

[89] R. Gaska, A. Osinsky, J. Yang, and M. Shur, "Self-heating in high-power AlGaN-GaN HFETs," *IEEE Electron Devices Lett.*, vol. 19, no. 3, pp. 89-91, Mar. 1998.

[90] A. Chini, V. Di Lecce, M. Esposto, G. Meneghesso, and E. Zanoni, "RF degradation of GaN HEMTs and its correlation with DC stress and I-DLTS measurements," *Proc. European Microw. Integr. Circuits Conf.*, Rome, Italy, pp. 28-29, Sept. 2009.

[91] J. Joh, J del Alamo, K. Langworthy, S. Xie, and T. Zheleva, "Role of stress voltage on structural degradation of GaN high-electron-mobility transistors," *Microelectron. Rel.*, vol. 51, no. 2, pp. 201-206, Feb. 2011.

[92] B. Benbakhti, A. Soltani, K. Kalna, M. Rousseau, and J. De Jaeger, "Effects of self-heating on performance degradation in AlGaN/GaN based devices," *IEEE Trans. Electron Devices*, vol. 56, no. 10, pp. 2178-2185, Oct. 2009.

[93] R. Gaska, A. Osinsky, J. Yang, and M. Shur, "Self-heating in highpower AlGaN-GaN HFETs," *IEEE Electron Device Lett.*, vol. 19, no. 3, pp. 89-91, Mar. 1998.

[94] M. Kuball, J. Hayes, M. Uren, T. Martin, J. Birbeck, R. Balmer, and B. Hughes, "Measurement of temperature in active high-power AlGaN/GaN HFETs using Raman spectroscopy," *IEEE Electron Device Lett.*, vol. 23, no. 1, pp. 7-9, Jan. 2002.

[95] I. Ahmad, V. Kasisomayajula, M. Holtz, J. Berg, S. Kurtz, C. Tigges, A. Allerman, and A. Baca, "Self-heating study of an AlGaN/GaN-based heterostructure field-effect transistor using ultraviolet micro-Raman scattering," *Appl. Phys. Lett.*, vol. 86, no. 17, pp. 173503-1-173503-5, Apr. 2005.

[96] K. Chabak, J. Gillespie, V. Miller, A. Crespo, J. Roussos, M. Trejo, D. Walker, G. Via, G. Jessen, J. Wasserbauer, F. Faili, D. Babic, D. Francis, and F. Ejeckam, "Full-wafer characterization of AlGaN/GaN HEMTs on free-standing CVD diamond substrates," *IEEE Electron Device Lett.*, vol. 31, no. 2, pp. 99-101, Feb. 2010.

[97] J. Pomeroy, M. Bernardoni, D. Dumka, D. Fanning, and M. Kuball, "Low thermal resistance GaN-on-diamond transistors characterized by three-dimensional Raman thermography mapping," *App. Phys. Lett.*, vol. 104, no. 8, p. 083513-1-083513-5, Feb. 2014.

[98] M. Seelman-Eggebert, P. Meisen, F. Schaudela, P. Koidla, A. Vescanb, and H. Leier, "Heat spreading diamond films for GaN-based high power transistor devices," *Diamond Relat. Mater.*, vol. 10, no. 3-7, pp. 744-749, Mar./July 2001.

[99] A. Sarua, H. Ji, K. Hilton, D. Wallis, M. Uren, T. Martin, and M. Kuball, "Thermal boundary resistance between GaN and substrate in AlGaN/GaN electronic devices," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3152-3158, Dec. 2007.

[100] *Electronic Archive of New Semiconductor Materials, Characteristics and Properties: Gallium Nitride* [Online]. Available: http://www.ioffe.rssi.ru/SVA/NSM/Semicond/GaN/index.html, accessed Mar. 15, 2014.

[101] *Electronic Archive of New Semiconductor Materials, Characteristics and Properties: Silicon Carbide* [Online]. Available: http://www.ioffe.rssi.ru/SVA/NSM/Semicond/SiC/index.html, accessed Mar. 15, 2014.

[102] M. Moradi, "Analytical modeling of drain-current characteristics of AlGaN/GaN HFETs with incorporation of the impacts of virtual-gate and transferred-electron effect," MASc. thesis, Dept. Electr. Comput. Eng., Univ. Concordia, Montreal, QC, Canada, June 2010.

[103] J. Joh, J. del Alamo, U. Chowdhury, T. Chou, H. Tserng, and J. Jimenez, "Measurement of channel temperature in GaN high electron mobility transistors," *IEEE Trans. Electron Devices*, vol. 56, no. 12, pp. 2895-2901, Dec. 2009.

[104] S. Martin-Horcajo, A. Wang, and M. Romero, "Simple and accurate method to estimate channel temperature and thermal resistance in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 60, no. 12, pp. 4105-4111, Dec. 2013.

[105] J. DiLorenzo and D. Khandelwal, *GaAs FET Principles and Technology*. Norwood, Artech House, 1982, pp. 308-347.

[106] F. Manouchehri, P. Valizadeh, and M. Z. Kabir, "Temperature-dependent investigation of low frequency noise characteristics of mesa-, fin-, and island-isolated AlGaN/GaN HFETs," *Solid-State Electron.*, vol. 89, pp. 1-6, Nov. 2013.

[107] V. Fiorentini, F. Bernardini, and O. Ambacher, "Evidence for nonlinear macroscopic polarization in III-V nitride alloy heterostructures," *Appl. Phys. Lett.*, vol. 80, no.7, pp.1204-1206, Feb. 2002.

[108] W. Lanford, T. Tanaka, Y. Otoki, and I. Adesida, "Recessed-gate enhancement-mode GaN HEMT with high threshold voltage," *Electron. Lett.*, vol. 41, no. 7, pp. 449-450, Mar. 2005.

[109] K. Ohi, J. Asubar, K. Nishiguchi, and T. Hashizume, "Current stability in multi-mesa-channel AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 2997-3004, Oct. 2013.

[110] S. Liu, Y. Cai, G. Gu, J. Wang, C. Zeng, W. Shi, Z. Feng, H. Qin, Z. Cheng, K. Chen, and B. Zhang, "Enhancement-mode operation of nano-channel array (NCA) AlGaN/GaN HEMTs," *IEEE Electron Devices Lett.*, vol. 33, no. 3, pp. 354-356, Mar. 2012.

[111] B. Lu, "AlGaN/GaN-based power semiconductor switches," Dept. of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA, Ph.D. dissertation, June 2013.

[112] K. Im, C. Won, Y. Jo, J. Lee, M. Bawedin, S. Cristoloveanu, and J. Lee, "High-performance GaN-based nanochannel FinFETs with/without AlGaN/GaN heterostructure," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3012-3018, Oct. 2013.

[113] S. Takashima, Z. Li, and T. Chow, "Sidewall dominated characteristics on Fin-Gate AlGaN/GaN MOS-channel-HEMTs," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3025-3031, Oct. 2013.

[114] H. Hahn, B. Reuters, A. Wille, N. Ketteniss, F. Benkhelifa, O. Ambacher, H. Kalisch, and A. Vescan, "First polarization-engineered compressively strained AlInGaN barrier enhancement-mode MISHFET," *Semicond. Sci. Technol*., vol. 27, no. 5, pp. 0550041-0550046, Mar. 2012.

[115] I. Hwang, J. Kim, H. Choi, H. Choi, J. Lee, K. Kim, J. Park, J. Lee, J. Ha, J. Oh, J. Shin, and U. Chung, "p-GaN gate HEMTs with tungsten gate metal for high threshold voltage and low gate current," *IEEE Electron Devices Lett.*, vol. 34, no. 2, pp. 202-204, Feb. 2013.

[116] T. Lalinský, G. Vanko, A. Vincze, Š. Haščík, J. Osvald, D. Donoval, M. Tomáška, and I. Kostič, "Effect of fluorine interface redistribution on performance of AlGaN/GaN HEMTs," *Microelectron. Eng.*, vol. 88, no. 2, pp. 166-169, Feb. 2011.

[117] S. Senturia, Microsystem Design. New York: Springer-Verlag; 2000.

[118] http://www.nextnano.com/nextnano3, accessed Nov. 2013.

[119] G. Meneghesso, F. Rampazzo, P. Kordos, G. Verzellesi, and E. Zanoni, "Current collapse and high-electric-field reliability of unpassivated GaN/AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 53, no. 12, pp. 2932-2941, Dec. 2006.

[120] G. Meneghesso, G. Verzellesi, R. Pierobon, F. Rampazzo, A. Chini, U. Mishra, C. Canali, and E. Zanoni, "Surface-related drain current dispersion effects in AlGaN-GaN HEMTs," *IEEE Trans. on Electron Devices*, vol. 51, no. 10, pp. 1554-1561, Oct. 2004.

[121] O. Mitrofanov and M. Manfra, "Mechanisms of gate lag in GaN/AlGaN/GaN high electron mobility transistors," *Superlattices Microstruct.*, vol. 34, no. 1-2, pp. 33-53, July/Aug. 2003.

[122] Z. Fang, B. Claflin, D. Look, D. Green, and R. Vetury, "Deep traps in AlGaN/GaN heterostructures studied by deep level transient spectroscopy: Effect of carbon concentration in GaN buffer layers," *J. Appl. Phys.*, vol. 108, no. 6, pp. 063706-1-063706-6, Sept. 2010.

[123] A. Polyakov and I. Lee, "Deep traps in GaN-based structures as affecting the performance of GaN devices," *Mater. Sci. Eng.*, vol. 94, pp. 1-56, Aug. 2015.

[124] R. Cuerdo, Y. Pei, Z. Chen, S. Keller, S. DenBaars, F. Calle, and U. Mishra, "The kink effect at cryogenic temperatures in deep submicron AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 30, no. 3, pp. 209-212, Mar. 2009.

[125] K. Choi, H. Jang, and J. Lee, "Observation of inductively coupled-plasma-induced damage on n-type GaN using deep-level transient spectroscopy," *App. Phys. Lett.*, vol. 82, no. 8, pp. 1233-1235, Feb. 2003.

[126] Z. Fand, D. Look, X. Wang, J. Han, F. Khan, and I. Adesida, "Plasma-etching-enhanced deep centers in n-GaN grown by metalorganic chemical-vapor deposition," *App. Phys. Lett.*, vol. 82 , no. 10, pp. 1562-1564, Mar. 2003.

[127] H. Cho, F. Khan, I. Adesida, Z. Fang, and D. Look, "Deep level characteristics in n-GaN with inductively coupled plasma damage," *J. Phys. D: Appl. Phys.*, vol. 41, no. 15, pp. 15531-15534, July 2008.

[128] L. Fang, S. Bo, L. Li-Wu, L. Xin-Yu, W. Ke, X. Fu-Jun, W. Yan, M. Nan, and H. Jun, "Identification and elimination of inductively coupled plasma-induced defects in $Al_xGa_{1-x}N$/GaN heterostructures," *Chin. Phys. B*, vol. 20, no. 7, pp. 077303-1-077303-6, Mar. 2011.

[129] P. Klein, S. Binari, K. Ikossi, A. Wickenden, D. Koleske, and R. Henry, "Current collapse and the role of carbon in AlGaN/GaN high electron mobility transistors grown

by metalorganic vapor-phase epitaxy," *App. Phys. Lett.*, vol. 79, no. 21, pp. 3527-3529, Nov. 2001.

[130] P. Klein and S. Binari, "Photoionization spectroscopy of deep defects responsible for current collapse in nitride-based field effect transistors," *J. Phys.: Condens. Matter.*, vol. 15, no. 44, pp. R1641-R1667, Oct. 2003.

[131] Z. Chen, Y. Pei, S. Newman, R. Chu, D. Brown, R. Chung, S. Keller, S. Denbaars, S. Nakamura, and U. Mishra, "Growth of AlGaN/GaN heterojunction field effect transistors on semi-insulating GaN using an AlGaN interlayer," *App. Phys. Lett.*, vol. 94, no. 11, pp. 112108-1-112108-3, Mar. 2009.

[132] P. Jogai, "Influence of surface states on the two-dimensional electron gas in AlGaN/GaN heterojunction field-effect transistors," *J. Appl. Phys.*, vol. 93, no. 3, pp. 1631-1635, Feb. 2003.

[133] T. Hashizume, S. Ootomo, S. Oyama, M. Konishi, and H. Hasegawa, "Chemistry and electrical properties of surfaces of GaN and GaN/AlGaN heterostructures," *J. Vac. Sci. Technol. B*, vol. 19, no. 4, pp. 1675-1681, July 2001.

[134] Q. Liu and S. Lau, "A review of the metal-GaN contact technology," *Solid-State Electron.*, vol. 42, no. 5, pp. 677-691, May 1998.

[135] S. Binari, H. Dietrich, G. Kelner, L. Rowland, K. Doverspike, and D. Wickenden, "H, He, and N implant isolation of n-type GaN," *J. Appl. Phys.*, vol. 78, no. 5, pp. 30080-3011, Sept. 1995.

[136] Y. Lee, H. Kim, G. Yeom, J. Lee, M. Yoo, and T. Kim, "Etch characteristics of GaN using inductively coupled Cl_2/Ar and Cl_2/BCl_3 plasmas," *J. Vac. Sci. and Technol. A*, vol. 16, no. 3, pp. 1478-1482, Sept. 1998.

[137] R. Shul, C. Willison, M. Bridges, J. Han, J. Lee, S. Pearton, C. Abernathy, J. MacKenzie, S. Donovan, L. Zhang, and L. Lester, "Selective inductively coupled plasma etching of group-III nitrides in Cl_2- and BCl_3-based plasmas," *J. Vac. Sci. Technol. A*, vol. 16, no. 3, pp.1621-1626, May 1998.

[138] D. Basak, M. Verdú, M. Montojo, M. Sánchez-García, F. Sánchez, E. Muñoz, and E. Calleja, "Reactive ion etching of GaN layers using SF_6," *Semicond. Sci. Technol.*, vol. 12, no. 12, pp. 1654-1657, Sept. 1997.

[139] D. Basak, T. Nakanishi, and S. Sakai, "Reactive ion etching of GaN using BCl_3, BCl_3/Ar and BCl_3/ N_2 gas plasmas," *Solid-State Electron.*, vol. 44, no. 4, pp. 725-728, Apr. 2000.

[140] S. Pearton, C. Abernathy, F. Ren, J. Lothian, P. Wisk, and A. Katz, "Dry and wet etching characteristics of InN, AlN, and GaN deposited by electron cyclotron resonance metalorganic molecular beam epitaxy," *J. Vac. Sci. Technol. A*, vol. 11, no. 4, July 1993.

[141] R. Dimitrov, V. Tilak, W. Yeo, B. Green, H. Kim, J. Smart, E. Chumbes, J. Shealy, W. Scha, L. Eastman, C. Miskys, O. Ambacher, and M. Stutzmann, "Influence of oxygen and methane plasma on the electrical properties of undoped AlGaN/GaN heterostructures for high power transistors," *Solid-State Electron.*, vol. 44, no. 8, pp. 1361-1365, Aug. 2000.

[142] A. Ping, A. Schmitz, I. Adesida, M. Asif Khan, Q. Chen, and J. Yang, "Characterization of reactive ion etching-induced damage to n-GaN surfaces using Schottky diodes," *J. Electron. Mater.*, vol. 26, no. 3, pp. 266-271, Mar. 1997.

[143] F. Ren, J. Lothian, S. Pearton, C. Abernahty, C. Vartuli, J. Mackenzie, R. Wilson, and R. Karlicek, "Effect of dry etching on surface properties of III-nitrides," *J. Electron. Mater.*, vol. 26, no. 11, pp. 1287-1291, Nov. 1997.

[144] S. Pearton, C. Abernathy, C. Vartuli, J. Lee, J. MacKenzie, R. Wilson, R. Shul, F. Ren, and J. Zavada, "Unintentional hydrogenation of GaN and related alloys during processing," *J. Vac. Sci. Technol. A*, vol. 14, no. 3, pp. 831-835, May 1996.

[145] B. Molnar, C. Eddy, and K. Doverspike, "The influence of CH_4/H_2/Ar plasma etching on the conductivity of n-type gallium nitride," *J. Appl. Phys.*, vol. 78, no. 10, pp. 6132-6134, Nov. 1995.

[146] L. Wang, F. Mohammed, and I. Adesida, "Dislocation-induced nonuniform interfacial reactions of Ti/Al/Mo/Au Ohmic contacts on AlGaN/GaN heterostructure," *Appl. Phys. Lett.*, vol. 87, no. 14, pp. 1419151-1419153, Sept. 2005.

[147] L. Wang, F. Mohammed, and I. Adesida, "Differences in the reaction kinetics and contact formation mechanisms of annealed Ti/Al/Mo/Au Ohmic contacts on n-GaN and AlGaN/GaN epilayers," *J. Appl. Phys.*, vol. 101, no. 1, pp. 013702-1-013702-11, Jan. 2007.

[148] D. Qiao, L. Yu, L. Jia, P. Asbeck, S. Lau, and T. Haynes, "Transport properties of the advancing interface Ohmic contact to AlGaN/GaN heterostructures," *Appl. Phys. Lett.*, vol. 80, no. 6, pp. 992-994, Feb. 2002.

[149] C. Jeon, H. Jang, K. Choi, S. Bae, J. Lee, and J. Lee, "Fabrication of AlGaN/GaN heterostructure field effect transistor using room-temperature Ohmic contact," *Solid-State Electron.*, vol. 46, no. 5, pp. 695-698 , May 2002.

[150] S. Ruvimov, Z. Liliental-Weber, J. Washburn, D. Qiao, S. Lau, and P. Chu, "Microstructure of Ti/Al Ohmic contacts for n-AlGaN," *Appl. Phys. Lett.*, vol. 73, no. 18, pp. 2582-2584, Nov. 1998.

[151] D. Ingerly, Y. Chen, R. William, T. Takeuchi, and Y. Chang, "Low resistance Ohmic contacts to n-GaN and n-AlGaN using NiAl," *Appl. Phys. Lett.*, vol. 77, no. 3, pp. 382-384, June 2000.

[152] J. Shealy, V. Kaper, V. Tilak, T. Prunty, J. Smart, B. Green, and L. Eastman, "An AlGaN/GaN high-electron-mobility transistor with an AlN sub-buffer layer," *J. Phys.: Condens. Matter*., vol. 14, no. 13, pp. 3499-3509, Mar. 2002.

[153] J. Kim, H. Jang, and J. Lee, "Mechanism for Ohmic contact formation of Ti on n-type GaN investigated using synchrotron radiation photoemission spectroscopy," *J. Appl. Phys.*, vol. 91, no. 11, pp. 9214-9217, June 2002.

[154] J. Neugebauer and C. Van de Walle, "Atomic geometry and electronic structure of native defects in GaN," *Phys. Rev. B*, vol. 50, no. 11, pp. 8067-8070, Sept. 1994.

[155] D. Look, G. Farlow, P. Drevinsky, D. Bliss, and J. Sizelove, "On the nitrogen vacancy in GaN," *Appl. Phys. Lett.*, vol. 83, no. 17, pp. 3525-3527, Oct. 2003.

[156] B. Van Daele, G. Van Tendeloo, W. Ruythooren, J. Derluyn, M. R. Leys, and M. Germain, "The role of Al on Ohmic contact formation on n-type GaN and AlGaN/GaN," *Appl. Phys. Lett.*, vol. 87, no. 6, pp. 061905-061905, Aug. 2005.

[157] A. Soltani, A. BenMoussa, S. Touati, V. Hol, J. Jaeger, J. Laureyns, Y. Cordier, C. Marhic, M. Djouadi, and C. Dua, "Development and analysis of low resistance Ohmic contact to n-AlGaN/GaN HEMT," *Diamond Relat. Mater.*, vol. 16, no. 2, pp. 262-266, Feb. 2007.

[158] B. Luther, S. Mohney, T. Jackson, M. Khan, Q. Chen, and J. Yang, "Investigation of the mechanism for Ohmic contact formation in Al and Ti/Al contacts to n-type GaN," *Appl. Phys. Lett.*, vol. 70, no. 1, pp. 57-59, Jan. 1997.

[159] Z. Qin, Z. Chen, Y. Tong, X. Ding, X. Hu, T. Yu, and G. Zhang, "Study of Ti/Au, Ti/Al/Au, and Ti/Al/Ni/Au Ohmic contacts to n-GaN," *Appl. Phys. A: Mat, Sci. Process.*, vol. 78, no. 5, pp. 729-731, Mar. 2004.

[160] F. Mohammed, L.Wang, D. Selvanathan, H. Hu, and I. Adesida, "Ohmic contact formation mechanism of Ta/Al/Mo/Au and Ti/Al/Mo/Au metallizations on AlGaN/GaN HEMTs," *J. Vac. Sci. Technol. B*, vol. 23, no. 6, pp. 2330-2335, Nov. 2005.

[161] B. Jacobs, M. Kramer, E. Geluk, and F. Karouta, "Optimisation of the Ti/Al/Ni/Au ohmic contact on AlGaN/GaN FET structures," *J. Cryst. Growth*, vol. 241, no. 1-2, pp. 15-18, May 2002.

[162] V. Kumar, L. Zhou, D. Selvanathan, and I. Adesida, "Thermally-stable low-resistance Ti/Al/Mo/Au multilayer Ohmic contacts on n-GaN," *J. Appl. Phys.*, vol. 92, no. 2, pp. 1712-1714, May 2002.

[163] G. Reeves and H. Harrison, "Obtaining the specific contact resistance from transmission line model measurements," *IEEE Trans. Electron Devices*, vol. 3, no. 5, pp. 111-113, May 1982.

[164] B. Jacobs, M. Kramer, E. Geluk, and F. Karouta, "Optimisation of the Ti/Al/Ni/Au Ohmic contact on AlGaN/GaN FET structures," *J. Cryst. Growth*, vol. 241, no. 1-2, pp. 15-18, May 2002.

[165] S. Mohammad, Z. Fan, A. Botchkarev, W. Kim, O. Aktas, A. Salvador, and H. Morkoç, "Near-ideal platinum-GaN Schottky diodes," *Electron. Lett.*, vol. 32, no. 6, pp. 598-599, Mar. 1996.

[166] R. Sporken, C. Silien, F. Malengreau, K. Grigorov, R. Caudano, F. Sánchez, E. Calleja, E. Muñoz, B. Beaumont, and P. Gibart "XPS study of Au/GaN and Pt/GaN contacts," *MRS Internet J. Nitride Semicond.*, vol. 2, no. 23, pp. 23-32, Jan. 1997.

[167] S. Binari, H. Dietrich, G. Kelner, L. Rowland, K. Doverspike, and D. Gaskill, "Electrical characterization of Ti Schottky barriers on n-type GaN," *Electron. Lett.*, vol. 30, no. 11, pp. 909-911, May 1994.

[168] J. Guo, M. Feng, R. Guo, F. Pan, and C. Chang, "Study of Schottky barriers on n-type GaN grown by low-pressure metalorganic chemical vapor deposition," *Appl. Phys. Lett.*, vol. 67, no. 18, pp. 2657-2659, Oct. 1995.

[169] A. Schmitz, A. Ping, M. Khan, Q. Chen, J. Yang, and I. Adesida, "Schottky barrier properties of various metals on n-type GaN," *Semicond. Sci. Technol.*, vol. 11, no. 10, pp. 1464-1467, Oct. 1996.

[170] A. Schmitz, A. Ping, M. Khan, Q. Chen, J. Yang, I. Adesida, "Metal contacts to n-GaN," *J. Electron. Mater.*, vol. 27, no. 4, pp. 255-260, May 1998.

[171] H. Xing, D. Deen, Y. Cao, T. Zimmermann, P. Fay, and D. Jena, "MBE-grown ultra-shallow AlN/GaN HFET technology," *ECS Trans.*, vol. 11, no. 5, pp. 233-237, Oct. 2007.

[172] J. Kim, C. Won, D. Kim, Y. Jo, J. Lee, Y. Kim, S. Cristoloveanu, and J. Lee, "Growth of AlN/GaN HEMT structure using Indium-surfactant," *J. Semicon. Technol. Sci.*, vol. 15, no. 5, pp. 490-496, Oct. 2015.

Appendix A: Summary of the Process Steps

WAFER NUMBER				SAMPLE NUMBER			
1	MASK 1 CLEANING						
ACCETONE	10 min						
IPA	10 min						
DI WATER	3 cycles						
NITROGEN GUN							
COMMENTS: • Optical inspection under microscope.							
2	SAMPLE CLEANING						
HF:DI WATER (1:1)	1 min						
HCl:DI WATER (1:1)	1 min						
METHANOL	1 min						
ACCETONE (50 °C)	3 min						
IPA	1 min						
DI WATER	3 cycles						
NITOGEN GUN							
COMMENTS:							
3	DEHYDRATION BAKE						
TEMPERATURE	200 °C			TIME	120 sec		
COMMENTS: • After cool down spin coat as soon as possible.							
4	PHOTORESIST 1						
TYPE	SHPLEY1318						
EQUIPMENT	LAURELL			PROGRAM	C		
PARAMETERS				SPREAD	500 rpm, 5 sec, 1305 rpm/s		
				SPIN	4000 rpm, 30 sec, 1305 rpm/s		
				DECELERATION	0 rpm, 5 sec, 1044 rpm/s		
COMMENTS: • Check the program parameters before starting the process!							
5	SOFT BAKE 1						
TEMPERATURE	115 °C			TIME	60 sec		
COMMENTS: • Edge bid removal after softbake if needed.							
6	EXPOSURE 1						
EQUIPMENT	EVG620			FILE	GaN		
TYPE	DOSAGE CONS			DOSAGE	60 mJ/cm^2		
COMMENTS: • Check UV lamp before starting the process.							
7	DEVELOPE 1						
DEVELOPER	MF319			TIME	60 sec		
COMMENTS: • Optical inspection under microscope to check the alignment. Redo this step if development not complete.							
8	HARD BAKE 1						
TEMPERATURE	90 °C			TIME	90 sec		
COMMENTS:							
9	ETCH (MESA)						
EQUIPMENT	P5000			FILE	GaN		
PARAMETERS	Cl_2	20	Ar	10	70 G	0	100 mtorr	30 sec
	Cl_2	20	Ar	10	70 G	120 W	100 mtorr	110 sec
	Cl_2	0	Ar	60	0 G	50 W	0 mtorr	10 sec
COMMENTS: • Use Silicon wafer, polished side, as career wafer. Not oxide wafer! 1 sample at a time.								
10	PHOTORESIST REMOVAL							
TEMPERATURE	20 °C			ULTRASONIC	POWER	1	TIME	9 min
COMMENTS: • Optical inspection under microscope to check if all the resist has been removed. • Redo this step if the photoresist removal is not complete.								
11	PROFILOMETER							
ETCH HEIGHT	240			ETCH RATE	2 nm/sec			
COMMENTS: • Use 0.1 mm/sec for scan speed and 5 mg for stylus force.								

12	MASK 2 CLEANING
ACCETONE	10 min
IPA	10 min
DI WATER	3 cycles
NITROGEN GUN	
COMMENTS: • Optical inspection under microscope.	

13	SAMPLE CLEANING
METHANOL	1 min
ACCETONE (50 °C)	3 min
IPA	1 min
DI WATER	3 cycles
NITOGEN GUN	
COMMENTS:	

14	DEHYDRATION BAKE		
TEMPERATURE	200 °C	TIME	120 sec
COMMENTS: • After cool down spin coat as soon as possible.			

15	PHOTORESIST 2 (IMAGE REVERSAL)		
TYPE	AZ5214		
EQUIPMENT	LAURELL	PROGRAM	B
PARAMETERS		SPREAD	500 rpm, 5 sec, 1305 rpm/s
		SPIN	3000 rpm, 30 sec, 1305 rpm/s
		DECELERATION	0 rpm, 5 sec, 1044 rpm/s
COMMENTS: • Check the program parameters before starting the process!			

16	SOFT BAKE		
TEMPERATURE	90 °C	TIME	55 sec
COMMENTS: • Edge bid removal if needed			

17	EXPOSURE 2		
EQUIPMENT	EVG620	FILE	Image_Reversal
TYPE	TIME CONS	TIME	0.6 sec
COMMENTS: • Check UV lamp before starting the process.			

18	POST BAKE		
TEMPERATURE	105 °C	TIME	120 sec
COMMENTS: • Use Site Coater hotplate. Has to be exactly 105°C.			

19	FLOOD EXPOSURE		
EQUIPMENT	EVG620	FILE	Flood_Exposure
TYPE	DOSAGE CONS	DOSAGE	250 mJ/cm^2
COMMENTS:			

20	DEVELOPE 2		
DEVELOPER	MF 726	TIME	24 sec
COMMENTS: • Optical inspection under microscope to check the alignment. • Redo if development not complete. • No hardbake needed!			

21	METALIZATION (OHMIC CONTACTS)											
EQUIPMENT	NEXDEP											
1	Ti	250 Å	2	Al	1500 Å	3	Ti	100 Å	4	Au	500 Å
COMMENTS:												

22	LIFT OFF						
TEMPERATURE	20 °C	ULTRASONIC		POWER	1	TIME	7 min
COMMENTS: • Optical inspection under microscope to check if the lift off is complete. • Redo if lift off is not finished.							

23	RTA				
EQUIPMENT	JESTFIRST200		FILE		850_Fast
STEP	TYPE	T/R	TEMP	N_2	SEN
1	DLY	30 s		ON	TC
2	RAMP1	150 °C/s	800	ON	TC
3	RAMP2	150 °C/s	850	ON	TC
4	SS	25 s	850	ON	TC

5	DLY	200 s		ON	TC
SHEET RESISTANCE (R_s)					Ω/□
TRANSFER RESISTANCE (R_T)					Ω-mm
SPECEPIC CONTACT RESISTANCE (R_c)					Ω/cm^2

COMMENTS:
- Use thin Silicon wafer as career wafer.
- Make sure the parameters have been change to proper ones.
- TLM measurements have to be performed after RTA.
- Redo the recipe if the Ohmic contact is not acceptable.

24	MASK 3 CLEANING
ACCETONE	10 min
IPA	10 min
DI WATER	3 cycles
NITROGEN GUN	

COMMENTS:
- Optical inspection under microscope.

25	SAMPLE CLEANING
METHANOL	1 min
ACCETONE (50 °C)	3 min
IPA	1 min
DI WATER	3 cycles
NITOGEN GUN	

COMMENTS:

26	DEHYDRATION BAKE		
TEMPERATURE	200 °C	TIME	120 sec

COMMENTS:
- After cool down spin coat as soon as possible.

27	PHOTORESIST 3 (IMAGE REVERSAL)		
TYPE	AZ5214		
EQUIPMENT	LAURELL	PROGRAM	B
PARAMETERS		SPREAD	500 rpm, 5 sec, 1305 rpm/s
		SPIN	3000 rpm, 30 sec, 1305 rpm/s
		DECELERATION	0 rpm, 5 sec, 1044 rpm/s

COMMENTS:
- Check the program parameters before starting the process!

28	SOFT BAKE		
TEMPERATURE	90 °C	TIME	55 sec

COMMENTS:
- Edge bid removal if needed

29	EXPOSURE		
EQUIPMENT	EVG620	FILE	Image_Reversal
TYPE	TIME CONS	TIME	0.6 sec

COMMENTS:
- Check UV lamp before starting the process.

30	POST BAKE		
TEMPERATURE	105 °C	TIME	120 sec

COMMENTS:
- Use Site Coater hotplate. Has to be exactly 105°C

31	FLOOD EXPOSURE		
EQUIPMENT	EVG620	FILE	Flood_Exposure
TYPE	DOSAGE CONS	DOSAGE	250 mJ/cm^2

COMMENTS:

32	DEVELOPE 3		
DEVELOPER	MF 726	TIME	24 sec

COMMENTS:
- Optical inspection under microscope to check the alignment.
- Redo if development not complete.
- No hardbake needed!

33	METALIZATION (SCHOTTKY GATE CONTACT)				
EQUIPMENT	NEXDEP				
1	Ni	250 Å	2	Au	500 Å

COMMENTS:

34	LIFT OFF					
TEMPERATURE	20 °C	ULTRASONIC	POWER	1	TIME	7 min

COMMENTS:

• Optical inspection under microscope to check if the lift off is complete. • Redo if lift off is not finished.							
35	**MASK 4 CLEANING**						
ACCETONE	10 min						
IPA	10 min						
DI WATER	3 cycles						
NITROGEN GUN							
COMMENTS: • Optical inspection under microscope.							
36	**SAMPLE CLEANING**						
METHANOL	1 min						
ACCETONE (50 °C)	3 min						
IPA	1 min						
DI WATER	3 cycles						
NITOGEN GUN							
COMMENTS:							
37	**DEHYDRATION BAKE**						
TEMPERATURE	200 °C	TIME	120 sec				
COMMENTS: • After cool down spin coat as soon as possible.							
38	**PHOTORESIST 4 (IMAGE REVERSAL)**						
TYPE	AZ5214						
EQUIPMENT	LAURELL	PROGRAM	B				
PARAMETERS	SPREAD	500 rpm, 5 sec, 1305 rpm/s					
	SPIN	3000 rpm, 30 sec, 1305 rpm/s					
	DECELERATION	0 rpm, 5 sec, 1044 rpm/s					
COMMENTS: • Check the program parameters before starting the process!							
39	**SOFT BAKE**						
TEMPERATURE	90 °C	TIME	55 sec				
COMMENTS: • Edge bid removal if needed							
40	**EXPOSURE 4**						
EQUIPMENT	EVG620	FILE	Image_Reversal				
TYPE	TIME CONS	TIME	0.6 sec				
COMMENTS: • Check UV lamp before starting the process.							
41	**POST BAKE**						
TEMPERATURE	105 °C	TIME	120 sec				
COMMENTS: • Use Site Coater hotplate. • Temperature has to be exactly 105°C							
42	**FLOOD EXPOSURE**						
EQUIPMENT	EVG620	FILE	Flood_Exposure				
TYPE	DOSAGE CONS	DOSAGE	250 mJ/cm^2				
COMMENTS:							
43	**DEVELOPE 4**						
DEVELOPER	MF 726	TIME	24 sec				
COMMENTS: • Optical inspection under microscope to check the alignment. • Redo if development not complete. • No hardbake needed!							
44	**METALIZATION (PAD CONTACTS)**						
EQUIPMENT	NEXDEP						
1	Ti	500 Å	2	Au	500 Å		
COMMENTS:							
45	**LIFT OFF**						
TEMPERATURE	20 °C	ULTRASONIC	POWER	1	TIME	7 min	
COMMENTS: • Optical inspection under microscope to check if the lift off is complete. • Redo if lift off is not finished.							