Design of Low-Phase-Noise and Low-Power

Current-Controlled Oscillators

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ABSTRACT

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Oscillators are widely employed in many electronic systems for signal generations, conversions, and detections. There are two categories of oscillators, voltage-controlled oscillators (VCOs) and current-controlled oscillators (ICOs). The development of device technology and the sensor systems lead to more and more applications of ICOs. Moreover, many of applications require ICOs to operate under very restricted conditions.

The objective of the work presented in this thesis is to design ICO circuits that meet the requirements of wide frequency range, high sensitivity to the control signal, low phase noise, low power dissipation, and small circuit space. To this end, the work of the design starts with a latch-based oscillator that has a simple structure and wide frequency range, but very modest performance of phase accuracy. A method to reduce the phase noise by introducing a Slope-Enhancement-Block (SEB) is proposed. The SEB is used to make the voltage variation at the critical node in the circuit enhanced so that the short-circuits currents are reduced. This method can hence help not only to reduce the phase noise, but also the power dissipation. With this method, two ICO circuits have been designed. By means of Spectre simulations, the performances of the two ICOs have been evaluated. The results show that by introducing the SEB each consisting of two cascaded inverters into the minimum-sized latch-based ICO, the phase noise can be reduced by at lest 5dBc/Hz. Such a simple SEB also helps to reduce significantly the power dissipation, in particular, at the lower part of the frequency range. Compared with the existing

oscillators having a similar frequency range, the designed ICOs have a better performance in terms of phase noise and the comparable power dissipation when they are made to operate at the same current level. The phase noise of the first designed ICO circuit, ICO_NA, is -114.7 dBc/Hz at the offset frequency of 1 MHz from the carrier of 916 MHz with the power dissipation of 26.05 mW. The phase noise of the second designed ICO circuit, ICO_NB, is -113.9 dBc/Hz at the offset of 1 MHz from 913 MHz with the power dissipation of 19.64 mW. Moreover, they require much smaller silicon space of only 3933 μm^2.

Acknowledgements

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List of Acronyms and Abbreviation

CMOS	complementary metal oxide semiconductor
ICO	current-controlled oscillator
ISF	impulse sensitivity function
LTV	linear time-variant
LPF	low pass filter
MOSFET	metal oxide semiconductor field effect transistor
NMOS	N-channel metal semiconductor
PLL	phase lock loop
PMOS	P-channel metal semiconductor
Pnoise	periodic noise
PSS	periodic steady state
SEB	slope-enhancement block
VCO	voltage-controlled oscillator

List of Primary Symbols

ICO_W	current-controlled oscillator in [1]
ICO_NA	first design of ICO using the proposed method
ICO_NB	second design of ICO using the proposed method
$\Delta\tau$	time shift of the toggling point
Inv1, Inv2	inverters in the latch
Inv3, Inv4	inverters in the delay device
V_a, V_b	input voltages of the SEB
V_{ax}	output voltage of the SEB
V_c, V_d	output voltages of the latch
V_{ref}	reference voltage
ΔV_{ref}	fluctuation of the reference voltage
V_{th}	threshold voltage of the SEB
ΔV_{th}	variation of the threshold voltage of the SEB

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Chapter 1

Introduction

Oscillators are among the basic building blocks in many electronics systems, such as those for tests, measurements and communications. The performance of an oscillator can be measured by several specifications, such as oscillation frequency range, sensitivity, phase noise, power dissipation, and circuit space. Oscillators can be divided into two categories, voltage-controlled oscillators (VCOs) and current-controlled oscillators (ICOs). The oscillation frequency of a VCO circuit is controlled by a voltage signal and its frequency range is related to that of the voltage. The technology development makes the device feature size decrease and, consequently, the supply voltage reduced. The dynamic range of voltage signals is, therefore, reduced with that development, which has some impact on the design of voltage-mode circuits and makes current-mode ones more attractive. The ICO design is, therefore, an interesting subject to study. Furthermore, there are more and more current-based sensors applied in various systems. ICO circuits can be made to suit the applications in current detections to meet different critical requirements. Hence, besides the function of signal generation, an ICO can also be used for signal conversions and detections.

In this chapter, the motivation and objective of the work of this thesis are presented. The scope of the work and the organization of the thesis are also described.

1.1 Motivation and Objective of the Work

As mentioned above, current-mode circuits become more appealing with the technology development because their dynamic range is not directly limited by the reduced supply voltage, and ICOs are increasingly used in many applications. Some applications require the wide frequency range, others may need a high sensitivity of the output signal to the variation of the control current, and most of them demand low phase noise and low power dissipation with low cost. It is commonly known that ICOs often find their applications in phase-locked loops (PLLs) and current-based sensor systems.

If an ICO is used in a PLL, as shown in Fig. 1.1, the performance of the PLL depends very much on that of the ICO. The frequency range of the ICO determines the capture and lock ranges of the PLL. Also, the static phase error is related to the sensitivity of the output frequency of the ICO to its input control current. Furthermore, this sensitivity determines the settling time of the PLL. Thus, a wide-range and high-sensitivity ICO is desirable for a high performance PLL. Needless to say, a low noise and power efficient ICO with smaller silicon space makes the PLL even more attractive in various systems.
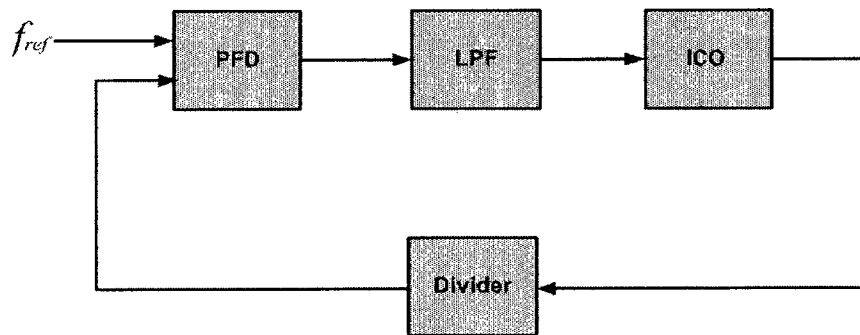
Fig. 1.1 Diagram of a PLL with an ICO included.

The development of integrated sensor systems has been going on since last decade. Current-based sensors, such as those converting the incident light into currents, have widely been used in signal acquisition and processing systems. It should be noted that an optical signal can vary over a very wide range, for example, five decades, while that of electronic circuits is usually much narrower, particularly in the case of voltage-mode ones. If the optical intensity variation is converted into a variation of frequency of a voltage or current, the limit of dynamic range of sensor circuits will be eased. An ICO can very well fit for such a conversion task. One example is shown in Fig. 1.2 [1]. Moreover, the integration of sensor devices in very-large-scale integrated (VLSI) circuits makes it possible to have an entire sensor system in a single chip, but the fabrication technology which is designed to implement electronic circuits, limits the performance of the integrated sensors. Thus, the current signals delivered by integrated sensors are usually very weak, typically in a sub-nA level in case of a micro-sized sensor. The electronic circuit in such a sensor system needs to be sensitive enough to respond to a very weak signal variation. Hence, the ability of an ICO to operate with a control current in a very low level is a critical issue in the design.
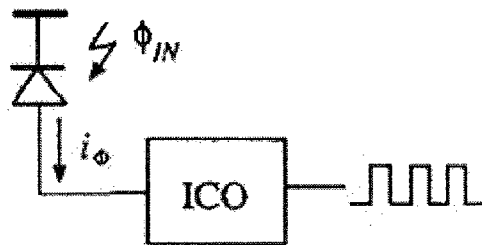
Fig. 1.2 ICO used to convert the current delivered by an optical sensor [1]. The cycle duration of the output signal is determined by the input current.

Similarly, for the emerging bioengineering systems, integrated sensors and electronic circuits operating in very low current level are demanded. Fro example, currents provided by biomolecular sensors are in nA level [2][3]. In many existing sensor circuits applied in this area, the current signals are first converted into analog voltage signals and then into digital data for the signal processing. However, if a functional block can convert directly the currents to digital pulse signals, the signal acquisition and processing will be much more efficient. An ICO driven by weak input currents is suitable in such a case.

Needless to say, the low power dissipation and small circuit space are of good quality of sensor systems. In particular, more and more systems are made portable to meet increasing demand of signal detections and communications. In certain circumstances, power and silicon space issues are even more critical than the operation speed in the circuit design. However, if the circuits are designed to operate under low current conditions, to suit the applications and to be power efficient, the noise in the circuits can be very critical. In order to make the ICO circuits functional with the requirements of the operating current, frequency range, and power dissipation, effective measures for the noise reduction should be taken in the design process.

The objective of the work presented in this thesis is to design ICO circuits that are able to operate over a very large frequency range, with very weak control currents, low phase noise and low power dissipation. The design work also aims at low cost implementation with the standard CMOS technology and small silicon space for an easy integration of the ICO circuits in the target systems.

1.2 Scope and Organization of the Work

For this thesis work, the investigations of the performance matrix of existing oscillators, including frequency range, sensitivity, phase noise, power dissipation and circuit space, are to be conducted. Based on this investigation, a particular structure of ICO that has better performance in terms of wide frequency range and low current operation, is to be identified. The design work consists of two aspects, to develop a method of reducing phase noise and power dissipation, and to design ICO circuits with the method developed to evaluate and demonstrate the effectiveness of the method.

The thesis is organized as follows. In Chapter 2, the basics of the oscillator designs and of the performance measurements are described. Also, some of the existing oscillator circuits relevant to the new designs described in this thesis are presented. Chapter 3 is dedicated to the analysis of the problems of phase noise and power dissipation in ICO circuits and the description of the design method for low noise and low power ICO circuits. Two new ICO circuits are designed based on the proposed method which is found also in Chapter 3. In Chapter 4, the performance evaluations of the designed ICO circuits are presented, and the simulation results demonstrated. Chapter 5 summarizes the work of this thesis and highlights its technical contributions to the field.

Chapter 2

Background

Voltage/current-controlled oscillators (VCOs or ICOs) are an integral part of phase-locked loops, clock recovery circuits, and frequency synthesizers. And the recent exponential growth in wireless communication has increased the demand for more available channels of local oscillators. This has imposed more stringent requirements on the phase noise of oscillators. Similarly, the large frequency-tuning range and the trend toward large-scale integration with low cost make the inductorless oscillators, also called RC oscillators, more attractive in the applications of integrated sensor systems including optical sensors and biomolecular detections. But their typically inferior phase noise properties limit the usefulness of RC oscillators. Aiming to benefit from the attractive integrated nature and the merit of large frequency range, the phase noise performance of RC oscillators needs to be improved.

In this chapter, the oscillator fundamentals together with their different performances are presented in Sub-Chapter 2.1. Several representatives of the existing oscillators which are relevant to the work of this thesis, together with their merits and demerits, are introduced in Sub-Chapter 2.2. An emerging current-controlled oscillator with the simple structure is introduced in Sub-Chapter 2.3 to be served as the starting point of the work in this thesis. Sub-Chapter 2.4 summarizes this chapter.

2.1 Oscillator Fundamentals

An oscillator can produce sustained periodical output without any input signal. Although oscillators are inherently nonlinear systems we can use linear modeling to analyze their performance and get a tolerable approximation. This can be seen clearly after the introduction of the feedback model of oscillators.

2.1.1 Feedback Model of Oscillators

A basic linear oscillator model is a close-loop system with positive feedback as shown in Fig. 2.1 [4]. The loop consists of an amplifier with a gain of A(ω) and a feedback network with a gain of B(ω).
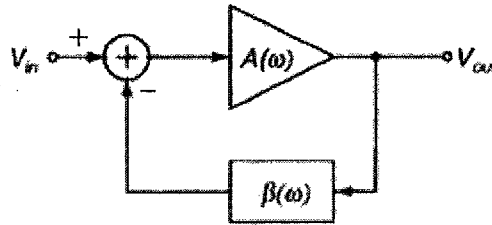
Fig. 2.1 Linear oscillatory system.

The close-loop transfer function of the system is given

$$V_{out} = \frac{A(\omega)}{1 + A(\omega)\beta(\omega)} \cdot V_{in} \tag{2.1}$$

In order to obtain sustained oscillation the loop gain has to satisfy the following two conditions which are also called "Barkhausen Criteria" [4]:

1) $|A(\omega_0)\beta(\omega_0)| = 1$ and

2) $\angle A(\omega_0)\beta(\omega_0) = (2j+1)\pi$, $j = 0,1,2,3\cdots\cdots$

Actually to start the oscillation the loop gain needs to be large than unity at first. When the output swing is large enough the devices go into the saturation region and the loop gain reduces to unity. This amplitude limiting mechanism is essential for stable oscillatory action.

2.1.2 Categorization of CMOS Oscillators

There are mainly two different categories of CMOS integrated oscillators: LC oscillators and ring oscillators.

A. LC Oscillators

LC oscillators include an LC tank and work on the principle of resonance. When the real and imaginary parts of the impedance at a specific frequency of the LC tank equal zero, the oscillator starts to oscillate. But the losses of the tank will make the oscillation to decay. In order to obtain the sustained oscillation, an active energy restorer needs to be added.

In recent years, LC oscillators have been known with good phase noise performance, but their tuning range is relatively small (around 10-20%) and on-chip spiral inductors occupy a lot of chip area [5]. On the other hand, ring oscillators usually have a wide tuning range and occupy much less on-chip integration area [6].

B. Ring Oscillators

A ring oscillator consists of a number of identical gain stages in a loop. Thanks to its better comparability with standard digital technology, larger frequency tuning range and smaller die area compared with LC-based oscillators, the ring oscillators find a widely applications in digital PLL and integrated sensor systems [4].

There are three different topologies of ring oscillators [7]. The first one is inverter-chain ring oscillators which use a simple CMOS inverter as the delay stage and have odd-number delay stages in the loop. This type of ring oscillator has no frequency tuning mechanism. The only way to change the output frequency is to modify the number of stage in the loop. The second one is current-starved inverter-chain ring oscillators which is the result of adding extra current-controlling devices on the fist type. Frequency tuning is achieved by adjusting the current for every stage. The third one is differential ring oscillators which consist of even number of delay stages, and every delay stage includes a differential pair and a tail current source to tune the oscillation frequency. The third type has the largest tuning range.

2.1.3 Performance of CMOS oscillators

When the output frequency of an oscillator is the function of its control input current, we call it current-controlled oscillator (ICO for short) as shown in Fig. 2.2. If the control input is voltage, the oscillator is called VCO.
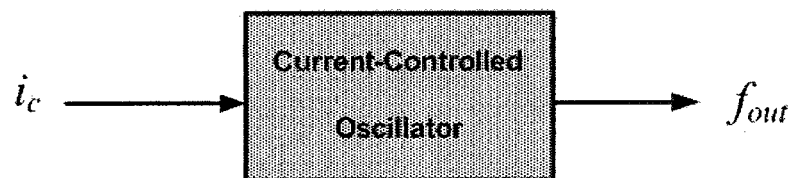
Fig. 2.2 Block diagram of ICO.

The output frequency of an ICO is given by

$$f_{out} = f_0 + K_{ICO}i_c \qquad (2.2)$$

where f_0 is the center frequency, i_c is the control input current and K_{ICO} denotes the gain or sensitivity of the oscillator and is equal to $\Delta f_{out}/\Delta i_c$.

We can build a VCO or ICO from a ring oscillator through adding frequency-tuning circuit. The performance matrix of a VCO or ICO is listed in Table 1.

TABLE 1
DIFFERENT PERFORMANCES OF VCO/ICO

	Performance	Description
1	Phase noise	See Sub-Sub-Chapter 2.1.3 B.
2	Power dissipation	The power dissipated by the whole oscillator circuit.
3	Frequency range	The frequency range of the output signal obtained from an oscillator.
4	Sensitivity	Denoted by K_{ICO}, which is equal to $\Delta f_{out}/\Delta i_c$.
5	Tuning linearity	An oscillator is called to have a linear tuning range if K_{ICO} is constant over its frequency range.
6	Oscillating output waveform and voltage swing	The quality of the output signal of an oscillator.
7	Layout area	The area occupied by the layout of an oscillator.

The different noise sources in CMOS integrated circuits and the performance of phase noise will be introduced in the following.

A. Noise sources in CMOS Integrated Circuits

Noise exists in every CMOS integrated circuits and influences the circuit performance [8]. There are two different types of noise in analog integrated circuits: device electronic noise and environmental noise. Thermal noise and flicker noise are device electronic noise. Supply and substrate noise are environmental noise.

Thermal noise is caused by the random thermal motion of electrons at any temperature above 0^0K in a dissipative medium. The thermal noise of a resistor can be modeled by a parallel current source with the single-sided spectral density as

$$\overline{i_n^2} / \Delta f = \frac{4kT}{R} \tag{2.3}$$

where k is Boltzmann's constant and T is the resistor temperature in Kelvin.

Thermal noise also exists in MOS transistors resulting from channel resistance and parasitic resistance at the gate, source and drain ohmic sections. The most significant contributor is the thermal noise in the channel which can be modeled as a current source connected between the drain and source terminals as shown in Fig. 2.3.
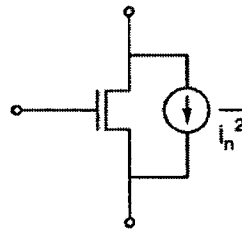
Fig. 2.3 Thermal noise of a MOSFET.

For long-channel MOS devices working in saturation the spectral density of the thermal noise in the channel is given by

$$\overline{i_n^2} / \Delta f = 4kT\gamma g_m \tag{2.4}$$

where k is Boltzmann's constant, g_m is the transconductance of the transistor, T is the transistor temperature in Kelvin, and γ is a coefficient .

The coefficient γ is derived to be 2/3 for long-channel transistors and may need to be replaced by a larger value for short-channel MOSFETs.

Another type of noise existing in the drain current of MOS transistors is flicker noise, which is caused by the extra energy stages of dangling bonds at the interface between the gate oxide and the silicon substrate of a MOS transistor. Flicker noise is also called 1/f noise and the noise spectral density is inversely proportional to the frequency.

With the trend of SoC(system on chip) oscillators are always built with high-speed digital circuits on the same chip. The fast switching of the digital part will produce disturbances on the power supply and substrate. As the different nodes in the oscillator experience almost the same supply and substrate noise the differential topology is suitable to use to resist this common-mode noise. Another ways to reduce the effect of supply and substrate noise are voltage regulators and isolation techniques.

In this thesis, only the thermal noise is considered.

B. Phase Noise

Phase noise is a frequency-domain representation of random fluctuations in the phase of an oscillation wave [9]. An ideal oscillator would generate a pure sinusoid wave (here the sinusoid oscillators are considered for simplicity). And its power spectrum is only one tone at the oscillator's frequency (positive and negative frequency for double-side-band (DSB) and only positive frequency for single-side-ban(SSB)). But for real oscillators the signal power is spread adjacent frequency resulting sidebands around the carrier frequency of the oscillator, as shown in Fig. 2.4. Jitter is the time-domain representative of phase noise [10][11].
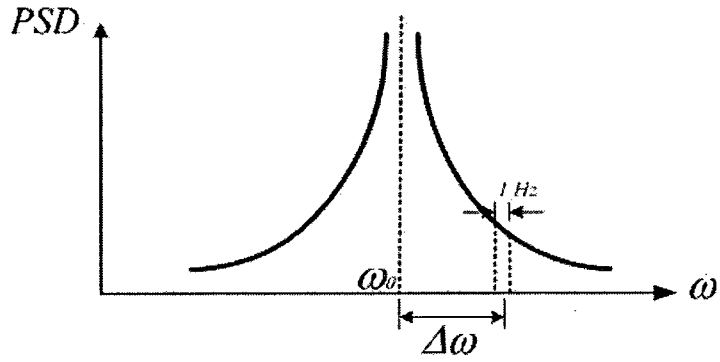
Fig. 2.4 Illustration of the phase noise in an oscillator.

Phase noise is typically expressed as the dB value of the ratio of the phase noise power in 1Hz bandwidth at various offset frequency to the carrier power. Phase noise has the unit of dBc/Hz and should be given with the offset frequency and the carrier frequency .

$$L\{\Delta\omega\} = 10 \cdot \log\left[\frac{P_{sideband}(\omega_0 + \Delta\omega, \ 1 \ Hz)}{P_{carrier}}\right] \qquad (2.5)$$

where $P_{carrier}$ is the power of the carrier and $P_{sideband}(\omega_0 + \Delta\omega, \ 1 \ Hz)$ represents the single sideband power at a frequency offset of $\Delta\omega$ from the carrier with a measurement bandwidth of 1 Hz. The typical plot of the phase noise of an oscillator versus offset from the carrier is shown in Fig. 2.6 [12].
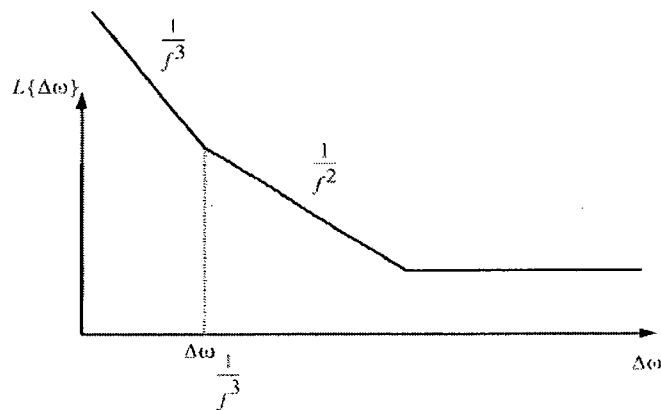
Fig. 2.5 Typical plot of the phase noise of an oscillator versus offset from the carrier.

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In the $\frac{1}{f^3}$ region of the phase noise of an oscillator, as shown in Fig. 2.6, the frequency-modulated flicker noise is dominant while the thermal noise is dominant in the $\frac{1}{f^2}$ region. As only the thermal noise is considered in this thesis, the phase noise of an oscillator in the $\frac{1}{f^2}$ region is important and its value at the offset frequency of $\Delta\omega$ from the carrier is given by [13]

$$L\{\Delta\omega\} = 10 \cdot \log\left[\frac{\Gamma_{rms}^2}{q_{max}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{2 \cdot \Delta\omega^2}\right] \qquad (2.6)$$

where Γ_{rms} is the rms value of the impulse sensitivity function (ISF) $\Gamma(x)$, which represents the time-varying sensitivity of the oscillator's phase to perturbations, $\overline{i_n^2}/\Delta f$ is the power spectral density of an input noise current, q_{max} is the maximum charge displacement across the capacitor on the node. For more than one input noise sources, the noise powers from different sources are added if they are uncorrelated.

From the equation (2.6), one can see that there are three ways aiming at reducing the phase noise of an oscillator: reduce the rms value of ISF, Γ_{rms}, reduce the power spectral density of an input noise current, $\overline{i_n^2}/\Delta f$, and increase the maximum charge displacement across the capacitor on the node, q_{max}. In order to reduce Γ_{rms}, the fast rail-to-rail switching is required [14][15].

2.2 Previous Differential Ring Oscillators and their Performance

The increasing growth in the different applications of VCO/ICO has imposed much more stringent requirements on the performance of VCO/ICOs. Only one or two good performance of oscillators cannot meet different specifications to guarantee the quality of the operation. In many applications nowadays, the wide frequency range, low phase noise, low power dissipation and small silicon space are required at the same time to provide the acceptable oscillating waveform at the low cost. In different kinds of VCO/ICOs, the differential ring oscillators (DROs) have the merits of the wide frequency range and small silicon space. In DROs, the phase noise due to white noise arises mainly from the differential pairs [16]. Designing DROs with the low phase noise, low power dissipation or both of them at the same time is a hot research topic for many years [17]. Here, several representative DROs are presented as follows and will be served as the references to compare with the work in this thesis. DROs can be classified into three types based on their delay cells, source-coupled DROs, cross-coupled DROs and dual-inverter DROs [18].

2.2.1 Source-coupled DROs

The delay cell of source-coupled DROs includes one pair of MOS transistors whose sources are connected to a tail current source [18]. And their drains are connected to active or passive resistance load. The source-coupled DRO with the typical delay cell is shown in Fig. 2.6. The voltage V_{cont} at the gate of the active resistance load tunes the frequency of the oscillator. The swing of the output oscillation waveform is restricted by

the overdrive voltage of the tail current source. The phase noise of source-coupled DROs is poor due to their low voltage swing.

(a)

(b)
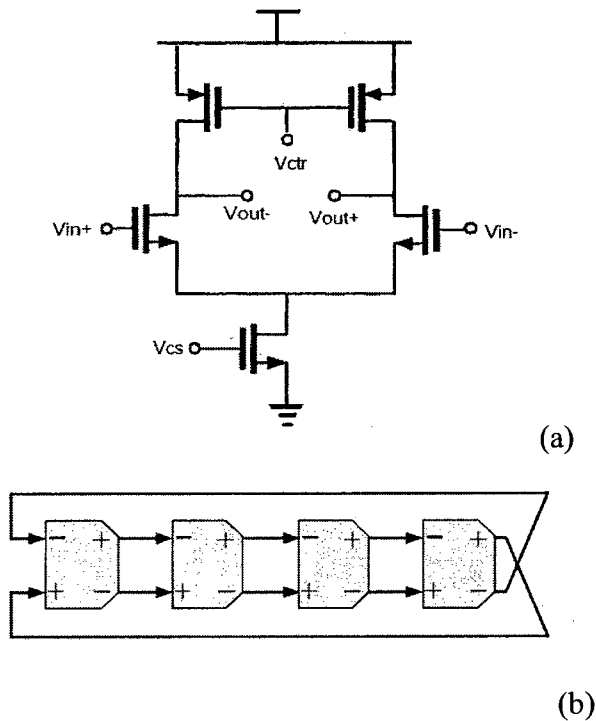
Fig. 2.6 Source-coupled DRO. (a) Typical delay cell, (b) the DRO structure.

2.2.2 Cross-coupled DROs

The delay cell of cross-coupled DROs includes one positive feedback pair of MOS transistors aiming to fulfill complete switching and maximize the output swing. As a result, the low phase-noise performance is achieved. The first cross-coupled DRO is shown in Fig. 2.7 [19]. Through adding a latch into a typical differential delay cell, as shown in Fig. 2.7(a), the delay cell performs complete switching and reduces the portion of on-time in the oscillation period in order to obtain the low phase noise. The latch consists of two cross-coupled NMOS transistors and a pair of PMOS transistors. The

control voltage is used to control the strength of the latch, and therefore to control the delay time of the cell.
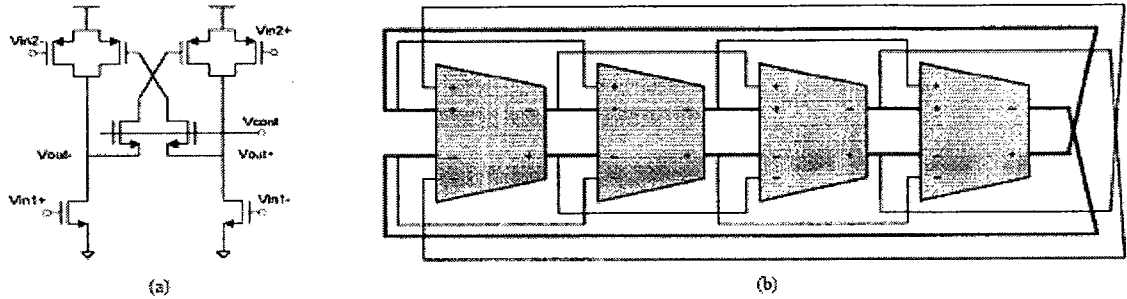
Fig. 2.7 Cross-coupled DRO of Park(99) in [19]. (a) Delay cell and (b) the oscillator structure.

Another representative of the cross-coupled DRO, as shown in Fig. 2.8, included only two delay cells to minimize the power dissipation [20]. The delay cell consists of one NMOS input pair, one PMOS positive feedback pair for maintaining oscillation and lowering phase noise, one diode-connected PMOS pair and one PMOSE transistor for frequency tuning. As the source nodes of Mp_1, as shown in Fig. 2.8 (a), are directly connected to the supply voltage to eliminate the current limitation of the output nodes and thus maximize the output swing. Because of the large output swing and transistors turning off periodically, the carrier power is increased and the noise power is reduced simultaneously. As a result, the phase-noise performance is improved.
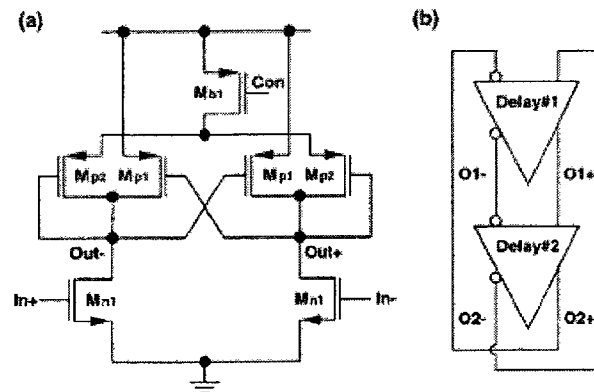
Fig. 2.8 Cross-coupled DRO of Yan(01) in [20]. (a) Delay cell and (b) the oscillator structure.

2.2.3 Dual-inverter DROs

The dual-inverter differential ring oscillator was first proposed by Badillo in 2003 as shown in Fig. 2.9 [21]. The delay cell of this dual-inverter DRO is formed by two input inverts, two local feedback transistors and four current starving transistors. The local feedback transistors prohibit the ring oscillator from latching up. The current starving transistors provide the frequency control. The performance of phase noise and power dissipation of this oscillator is good compared with previous ring oscillators because of its simple structure and large voltage swing.

(a)   (b)
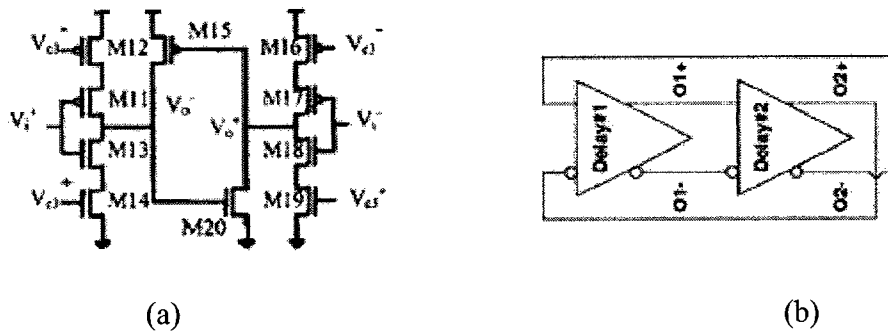
Fig. 2.9 Dual-inverter DRO of Badillo(03) in [21]. (a) Delay cell and (b) the oscillator structure.

In 2006 Samadian found the problem of Badillo delay cell that the latch transistors do not turn off at proper time [22]. Aiming at better current use, Samadian revised Badillo's dual-inverter DRO and achieved the lower power dissipation. Again in 2008 Li found the problem in Samadian's design of the current mismatch between the pull-up path and pull-down path [23]. To overcome this problem two transistors are added and their gates are connected to the frequency-tuning voltage. The schematic of the revised delay cell and the oscillator structure are shown in Fig. 2.10. After this revision the frequency tuning range of the oscillator was doubled while the performances of low phase-noise and low power dissipation were preserved.

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(a)   (b)
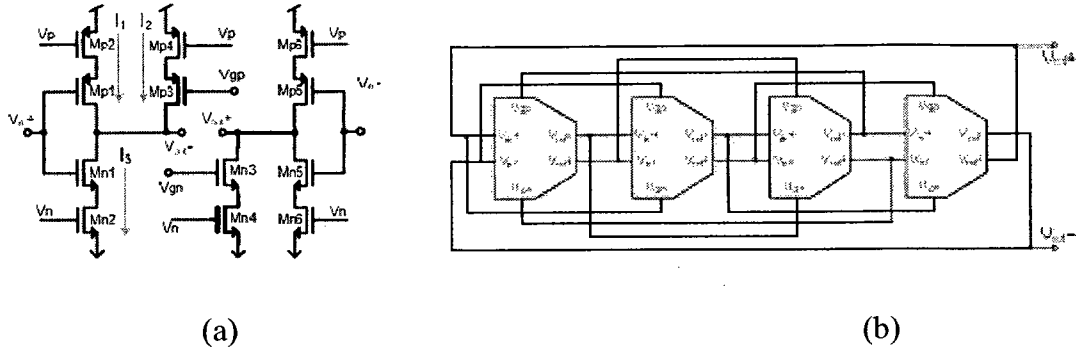
Fig. 2.10 Dual-inverter DRO of Ke(08) in [23]. (a) Delay cell and (b) the oscillator structure.

Because the half latch existing in the delay cells extends the voltage swing of the oscillating output and makes the transition time shorter, the cross-coupled and dual-inverter DROs have the performance of low phase-noise. But in order to make these two kinds of oscillators to work on a wide frequency range, they need to balance the speed of their pull-up and pull-down process, which means that the faster speed of pull-up (or pull-down) must be sacrificed and slowed to match the speed of pull-down (or pull-up). However, this scarification is not good for the performance of low phase-noise.

2.3 ICO_W Circuit

In 2003, [1] proposed a current-controlled oscillator with the simple structure, which will be called ICO_W in this thesis. The circuit and the functioning of ICO_W will be introduced and the reason why it is chosen as the base of our low phase-noise and low power-dissipation design will be given in this sub-chapter. The circuit of ICO_W is shown in Fig. 2.11. The frequency of the output oscillation waveform is tuned by the input control current i_c.

Fig. 2.11 Circuit of ICO_W in [1].

The PMOS transistors P_1 and P_2 of ICO_W work as switches to control the path of the input current. When P_1 is on and P_2 is off the input current will flow through P_1 and charge the parasitic capacitance at the gate node of N_3 of ICO_W. For the oscillator working correctly PMOS P_1 and P_2, with their gate voltages coming from the output of the latch, can not be in the on-state at the same time. When the gate voltage of NMOS transistors N_1 or N_2 of ICO_W goes high enough, the NMOS will be on and start to discharge the output of the latch and then change the state of the latch. The NMOS N_3 and N_4 in Fig. 2.11, with their gate voltages coming from the output of the latch, work to discharge the parasitic capacitance and make them ready to the next charging. Through this alternative setting and resetting mechanism the oscillation output waveform can be obtained at the output of the latch.

The simple structure of ICO_W makes it to be designed easily and to occupy the small silicon space. The capacitance involved in the working of ICO_W is only parasitic ones, which brings the performance of high sensitivity to the oscillator. As only the charging process is involved in the time scheme of the output oscillation, the large

frequency tuning range is obtained easily from the circuit of ICO_W. The highest frequency of ICO_W is limited by the strength of the latch. If we reduce the strength of the latch, as long as the latch turns on P_1 and P_2 in the different time, the delay for changing the state of the latch will decrease and the whole period will decrease too. This means that the oscillation frequency will increase. There is no limitation for the lowest frequency of ICO_W. This is because that N_1 or N_2 can take as long time as needed to turn on and change the latch state.

2.4 Summary

In this chapter, the fundamentals of oscillators and their different performances, especially the phase noise, are introduced. Several representatives of the existing oscillators which are relevant to the work of this thesis, together with their merits and demerits, are also introduced to serve as the compared reference. Finally, the circuit structure and work scheme of the current-controlled oscillator, ICO_W, is introduced as the starting point of the work in this thesis. ICO_W is an emerging current-controlled oscillator with the merits of large frequency range, high sensitivity and small structure. But the performances of phase noise and power dissipation of ICO_W need to be improved before finding applications.

In the next chapter, the problems of phase noise and power dissipation in the circuit of ICO_W will be analyzed, and a method to solve the problems and reduce the phase noise and power dissipation of ICO_W will be proposed. Based on the proposed method, two new versions of ICO circuits are designed.

Chapter 3

ICO Design

In the proceeding chapter, the fundamentals of oscillator are described together with some of existing circuits relevant to the work presented in this thesis. As mentioned previously, the objective of this work is to design current-controlled oscillators of simple structure, low phase noise, low power dissipation and wide frequency range. The oscillator circuit of ICO_W has good features of simple structure and wide frequency range. However it does not have significant advantage in term of phase-noise level compared to others. It is thus used as the basic structure of the new oscillators to be designed, while new techniques need to be developed to improve the performance related to the phase-noise. Moreover, as any improvement of a specific aspect of the performance is generally obtained at the expense of power dissipation, the emphasis of the work of designing the oscillators is also on the reduction of power dissipation.

In this chapter, an analysis of the performance, in terms of phase noise, is given in Sub-Chapter 3.1. Based on the analysis, a method of phase-noise reduction is proposed in Sub-Chapter 3.2. Using this method the designs of two oscillator circuits are described and the performance analysis presented in Sub-Chapter 3.3. The work of the low phase-noise designs is summarized in Sub-Chapter 3.4.

3.1 Analysis of the Circuit of ICO_W

The designs presented in this thesis are based on the circuit of ICO_W, represented in [1]. In this sub-chapter the timing characteristics of ICO_W is analyzed in detail and its performance about phase noise described. The principle of the current-controlled oscillator of ICO_W has been presented in Sub-Chapter 2.3. For the readers' convenience, the circuit diagram is resketched in Fig. 3.1.
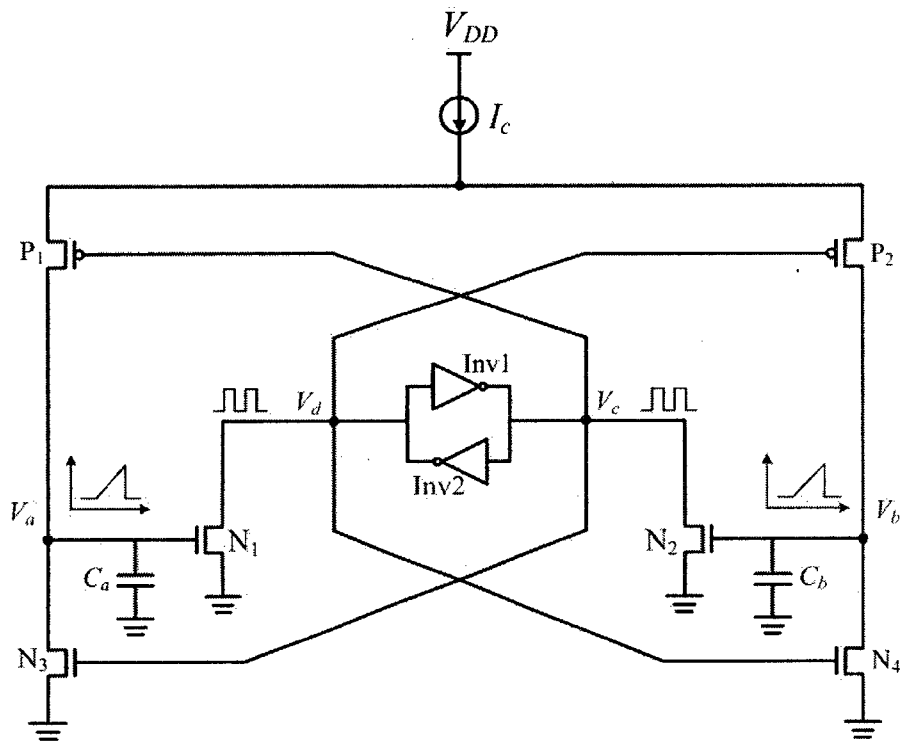
Fig. 3.1 Resketched circuit of ICO_W.

In the circuit shown in Fig. 3.1, the output voltage of the latch, V_c or V_d, swings between the two voltage levels, and the oscillation is achieved by setting and resetting alternatively the latch. The cycle duration of the oscillation is determined by that of setting-then-resetting process. This duration is related to three elements, i_c, the input current, the capacitance at V_a and V_b nodes, and V_{ref}, the reference voltage required at V_a,

or V_b, for toggling the state of the latch. The current i_c is charging, at any given time, one of the capacitance at V_a or V_b node.

In an ideal case, the circuit is noise-free, the current i_c is ideally steered to charge the capacitance at V_a or V_b node, and the reference voltage, V_{ref}, is fixed at a given level. In such a case, the latch will be toggled at the exact moments in each cycle as shown in Fig. 3.2, and the duration of the cycle depends only on the current i_c.
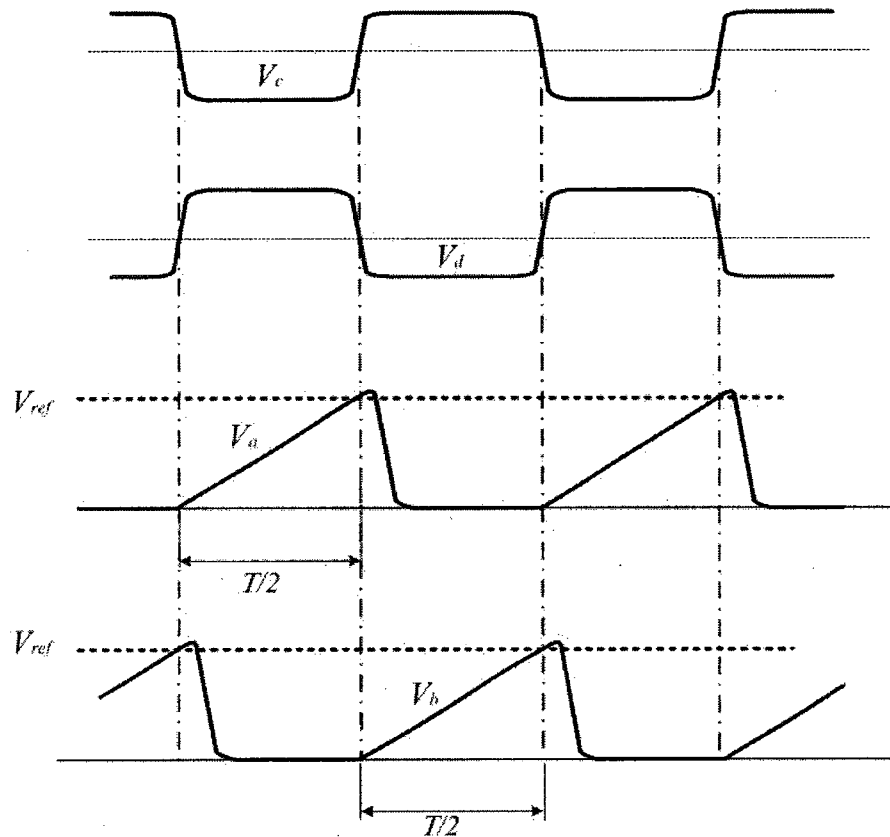
Fig. 3.2 Waveforms of the voltages in the oscillator shown in Fig. 3.1 in the ideal case.

In the circuit shown in Fig. 3.1, the capacitance at V_a node is made of the parasitic capacitors of the transistors connected, namely N_1, P_1, and N_3 in Fig. 3.1, if there is no capacitor added. These capacitances may be modulated by the voltage applied to them, which causes a modulation of the duration of the cycle. Also, the quality of the current

steering by the PMOS transistors P_1 and P_2 can have an effect on the charging current and thus on the voltage variation at V_a or V_b. This current steering operation is related to the quality of the square wave of V_c or V_d. In this circuit, there is no external reference voltage applied for the comparison purpose, and V_{ref} is determined by the static and dynamic characteristics of the transistors involved. These characteristics can have fluctuation related to both spatial device mismatch and time-dependent variation. Any shift of V_{ref} can result in a shift of the toggling point. The effect of V_{ref} shifting is usually more critical than those caused by the variation of capacitance and the current steering. The analysis about the effect of V_{ref} is elaborated in the following paragraph.

In order to demonstrate the setting-then-resetting process of the latch, the detail of the part of the latch and the pull-down NMOS transistors in the circuit of ICO_W is shown in Fig. 3.3. If the latch is initially in the state of $V_d = V_{DD}$ and $V_c = 0V$, to change the state to $V_d = 0V$ and $V_c = V_{DD}$, the voltage V_a need to be raised to the level of V_{ref} so that i_1, the current in the transistor N_1, is significant enough to pull V_d down quickly, despite the presence of i_2, the current in the PMOS transistor $P|_{Inv2}$ controlled by V_c. One can see that a time interval, called the transition time, is required to switch the state of the latch. The transition time starts when the discharging of capacitance at V_d node begins and ends with $V_d = 0V$. These two time points correspond to, respectively, two voltage levels. It is evident that the transition time is related to i_c. To make V_{ref} less input-current-dependent, it is defined as the mid point of the two levels, and the time at which V_a reaches the level of V_{ref} is defined as the toggling point of the latch. As there is a voltage pull-down process involving at least two currents, the transconductance of the devices concerned have importance effect in the process.
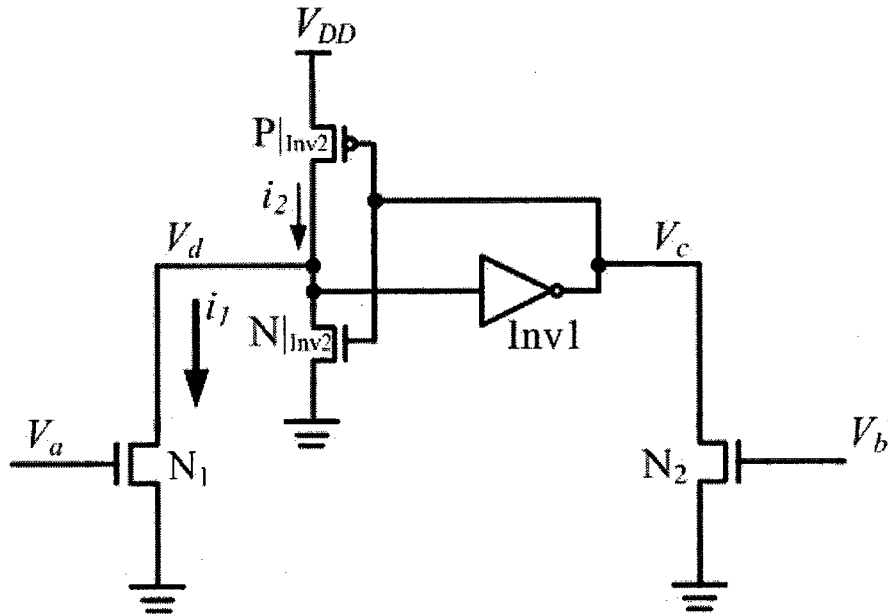
Fig. 3.3 Latch and its pull-down transistors in the circuit shown in Fig. 3.1.

If the transconductances of the devices are not time-varying, the latch will be switched at the same toggling point in each cycle and the transition time will remain the same. However, it is common that the device characteristics can not be constant because of the existence of noise in each transistor. One should expect to see the shifting of the toggling point, which causes the time jitter and phase noise at the output of the oscillator. The noise in the devices employed in the oscillator can result in a variation of the reference voltage, ΔV_{ref}, as shown in Fig. 3.4. In reality, the latch can be toggled when V_a or V_b reaches any point between $(V_{ref} - \Delta V_{ref}, V_{ref} + \Delta V_{ref})$, and the toggling point can be shifted within the interval of $\pm\Delta\tau$, as illustrated in Fig. 3.4. One can notice that $\Delta\tau$ is proportional to ΔV_{ref} and the time rate of the variation of V_a or V_b determined by i_c. One would attempt to minimize ΔV_{ref} in order to reduce time jitter and phase noise. However, this approach may not be cost-efficient as the device noise can not be removed or easily

compensated. Therefore, one should consider some approach that could lead to an effective reduction of the impact on the phase noise caused by ΔV_{ref}.
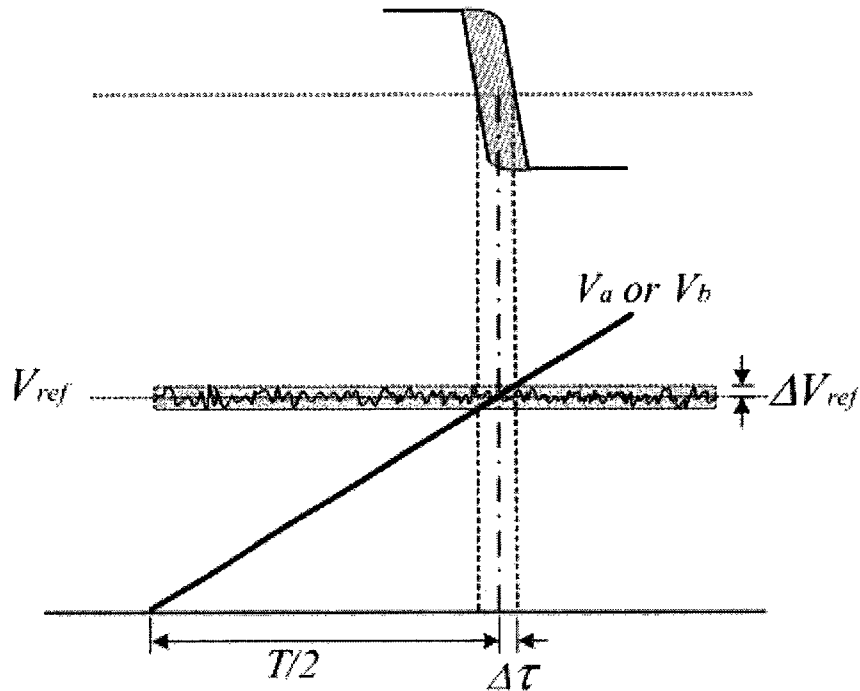
Fig. 3.4 Fluctuation of the reference voltage ΔV_{ref} and the range of the shift of the toggling point, $\Delta\tau$, in the circuit of ICO_W. This $\Delta\tau$ is determined by ΔV_{ref} and the voltage slope of V_a or V_b.

3.2 Method of the Phase-Noise and Power-Dissipation Reduction

As mentioned previously in Sub-Chapter 3.1, the maximum shift of the toggling point $\Delta\tau$ is proportional to ΔV_{ref} and inversely proportional to the time rate of the voltage variation dV_a/dt or dV_b/dt. Instead of attempting to reduce ΔV_{ref}, the approach used in the design presented in this thesis is to reduce the impact of the phase noise resulting from ΔV_{ref}. One would first consider to increase the voltage variation rate to reduce $\Delta\tau$ if ΔV_{ref} remains the same. As shown in Fig. 3.5, if V_a or V_b varies faster, $\Delta\tau$ will be visibly reduced. Evidently, the phase noise can be reduced by employing this idea. However, it

should be mentioned that the voltage variation, dV_a/dt, or dV_b/dt, is also used to determine the cycle time of the oscillation of the current-controlled oscillator, as shown in Fig. 3.6. Hence the signal variation needs to be undisturbed in the circuit operation.
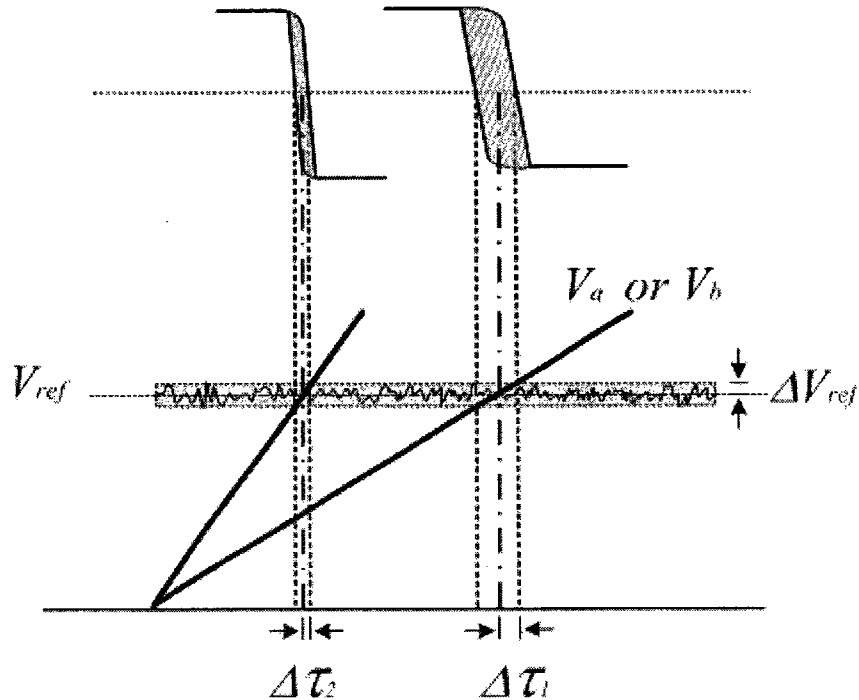
Fig. 3.5 Phase reduction method of increasing the voltage slope.

The challenge of developing a method to reduce the phase noise involves a preservation of the timing scheme, so that the oscillation frequency mainly depends on the input current. One would wish that any measures to reduce phase noise should not affect the range of oscillation frequency and the power dissipation of the circuit.
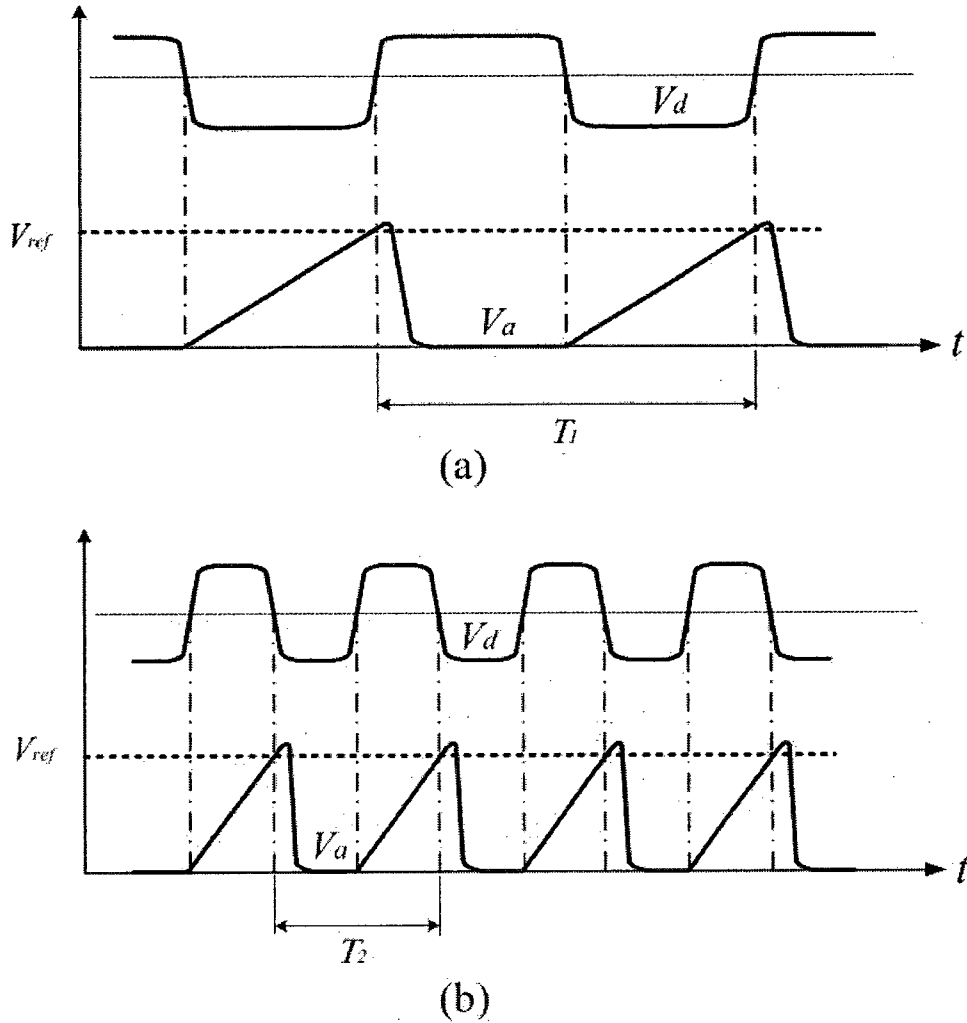
Fig. 3.6 Cycle duration of the oscillation determined by the input current. It is based on dV_a/dt(or dV_b/dt) $= i_c/C$. As the input current i_c in the case (b) is larger than that in (a), the duration of the cycle time T_2 is shorter than T_1.

The method proposed in this thesis for a phase-noise reduction is to make the process of setting-then-resetting the latch to be controlled by fast varying signals in order to reduce $\Delta\tau$, while keeping the variation rate of V_a and V_b intact. The fast varying signals V_{ax} and V_{bx}, generated from V_a and V_b respectively, as shown in Fig. 3.7, are to be used to toggle the latch. In this case, the maximum shift of the toggling point, $\Delta\tau$, is expected to be reduced, while the oscillation frequency is not affected by the generation of V_{ax} and V_{bx}.
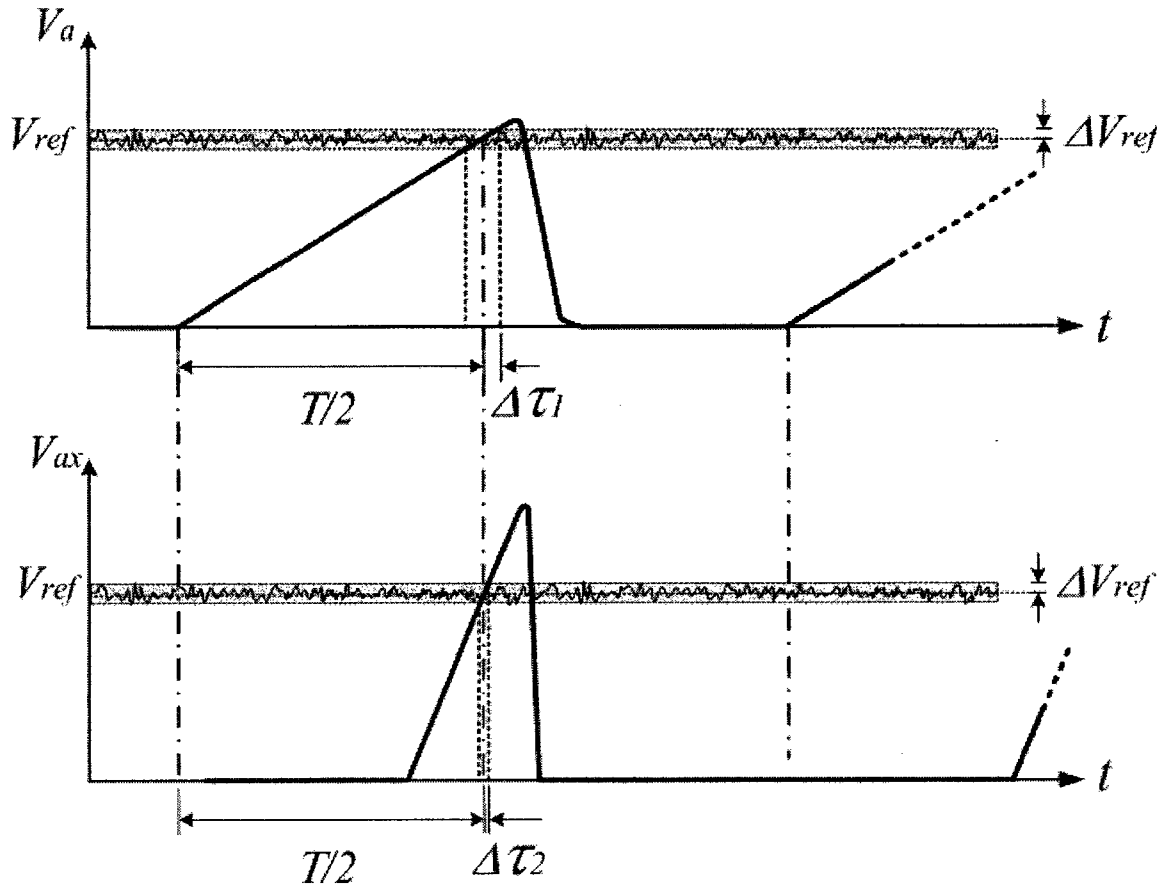
Fig. 3.7 Relationship between the new generated signal V_{ax} and V_a.

To implement the proposed method described above for the phase-noise reduction, one needs to generate the signals V_{ax} and V_{bx} from V_a and V_b respectively. The unit for the signal generation, called Slope-Enhancement Blocks (SEB) in this thesis, is to be incorporated in the circuit of ICO_W. The new version of the ICO is shown in Fig. 3.8. The signals in this circuit are expected to be as shown in Fig. 3.9. The voltage V_a or V_b is applied to the SEB that converts it into a fast-varying pitch signal. The latch is set or reset by this pitch signal, making the change of the latch state much faster than the case without SEB. Hence, the unit SEB serves for the two purposes. The first is to reduce $\Delta\tau$ meanwhile it makes the signals used for the latch toggling, i.e. V_{ax} and V_{bx}, from those for

30

the oscillation timing, i.e. V_a and V_b. The second is to provide the separation between these two types signals.
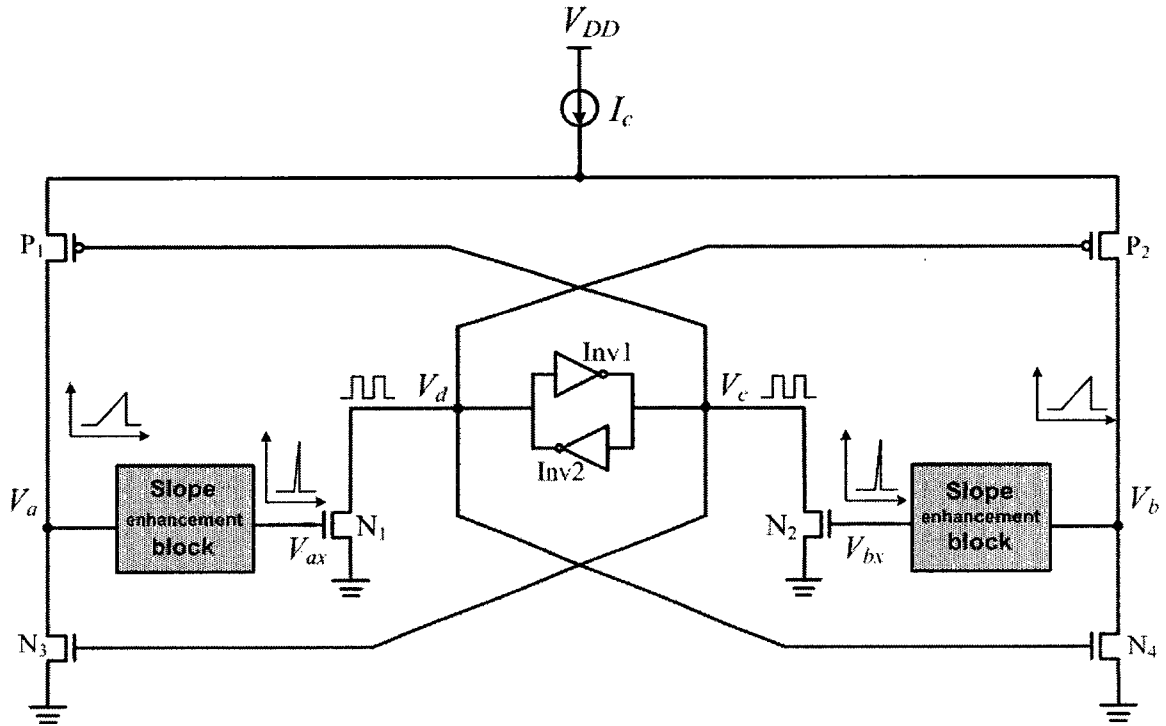
Fig. 3.8 Function blocks of the proposed low phase-noise oscillator.
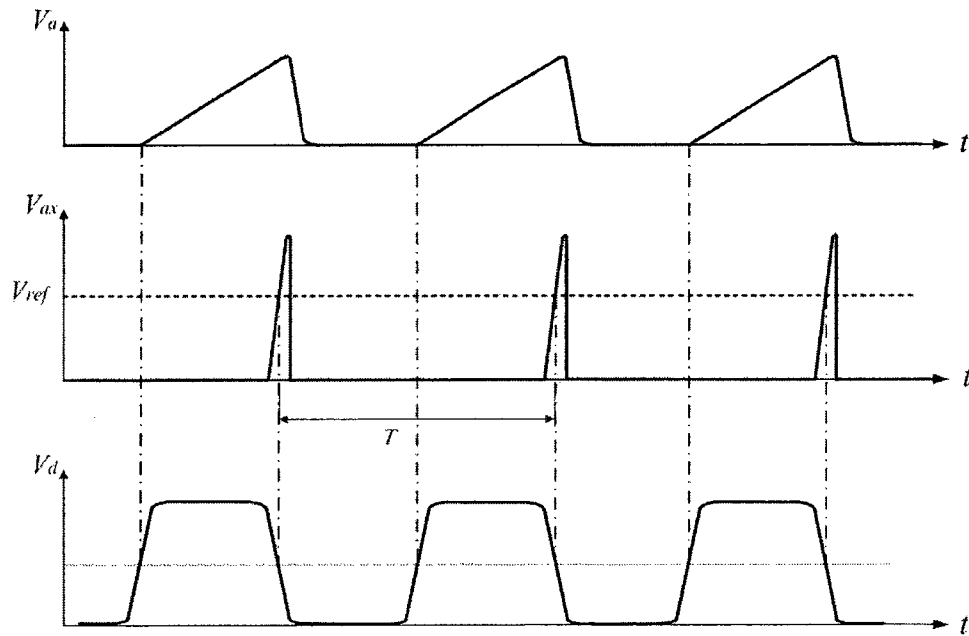
Fig. 3.9 Time relationship of the voltage signals V_a, V_{ax} and V_d.

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It is evident that the introduction of the unit SEB may result in additional noise. The design of the SEB should be in such a way that the phase noise caused by the SEB will be much smaller than the amount reduced by using the unit.

One can also see in the circuit shown in Fig. 3.8 that, V_{ax} and V_{bx} generated by the unit SEB vary much faster that V_a and V_b for the set and reset of the latch. The waveform quality of the output signals V_c and V_d are improved to be more square-shaped. Consequently, the current steering by the PMOS transistors can also be improved, which will, in turn, help to reduce the phase noise. Furthermore, the faster setting-then-resetting the latch will reduce the power dissipation caused by the short-circuit currents during the toggling of the latch [24]. In ICO_W, more than 90% of the total power dissipation results from the short-circuit current of the latch, depending on the oscillation frequency. A significant reduction of the short-circuit current will have positive effect in the total power dissipation.

Using the method of the phase-noise reduction proposed above, two ICO circuits have been designed. In the following Sub-chapter, the design of these circuits are presented in detail.

3.3 ICO Designs with the Proposed Method

In this Sub-chapter, an ICO circuit involving a unit of SEB is presented. As mentioned previously the unit of SEB should be designed in such a way that it is able to generate a fast varying $V_{ax}(t)$ from a slow-changing voltage $V_a(t)$, as shown in Fig. 3.10. By involving this unit, the signal used to switch the state of the latch is separated from that determining the oscillation frequency, but the former is dependent on the latter. To preserve the circuit timing scheme while reducing the phase noise, the slow-varying

signal is applied to the unit of SEB, and when the signal reaches a pre-set level, the output of the unit should change quickly from its low level to its high level. This pre-set level is denoted as V_{th}, the threshold of the unit.

$$\frac{dV_a}{dt} \ll \frac{dV_{ax}}{dt}$$
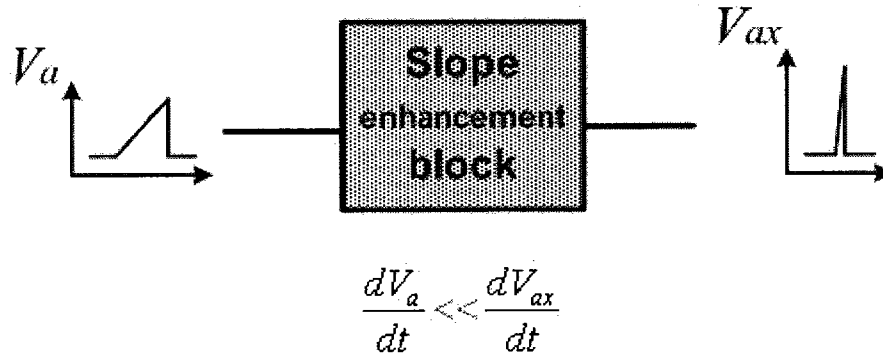
Fig. 3.10 Unit of SEB and its input and output signals.

Needless to say, introducing the unit of SEB brings additional phase noise, delay and power dissipation. To have the effective reduction of the overall phase noise of the ICO circuit, the unit of SEB should meet the following requirements.

- Due to various noises in the unit of SEB, its threshold V_{th} can be shifted. The variation of the threshold, ΔV_{th}, is as shown in Fig. 3.11. This ΔV_{th} should be much smaller than ΔV_{ref} of the latch to make its negative effect insignificant.

- The power dissipated in the unit should be negligible compared to that in the latch to maintain the overall power dissipation low.

- As the oscillation frequency is determined by the overall delay of the circuit, adding the unit of SEB modifies the oscillation cycle time. However, if the delay of the unit is minimal, the modification will not be significant.

Two different units of SEB have been designed. Their structures are presented in the following parts of the Sub-chapter.
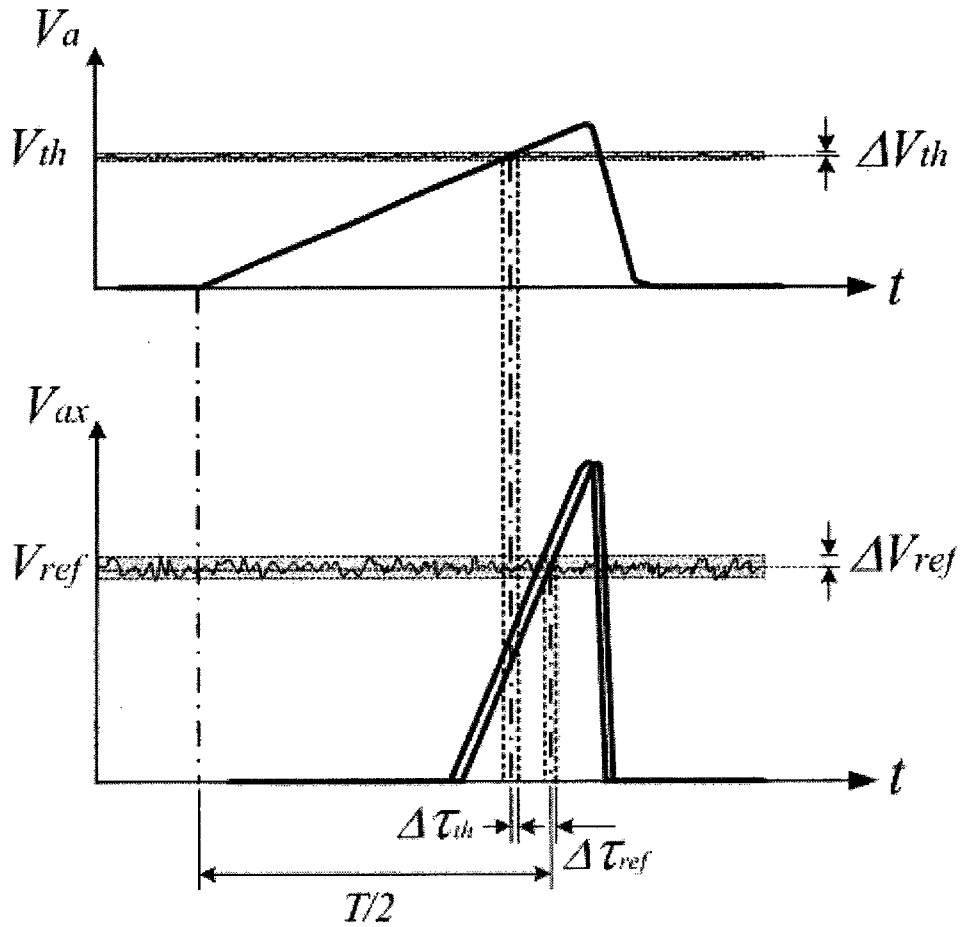
Fig. 3.11 Anticipated input and output waveforms of the unit of SEB. The maximum time shift caused by ΔV_{th}, the variation of V_{th}, can be $\pm\Delta\tau_{th}$.

3.3.1 Design of the Circuit of ICO_NA

For the unit of SEB to function as illustrated in Fig. 3.11, it should have such a character that, during a given time interval Δt, the variation of V_{ax}, denoted as ΔV_{ax}, is much larger than that of V_a, as shown in Fig. 3.12. Therefore, the unit should have a voltage transfer characteristics with a high dV_{ax}/dV_a. The unit of SEB should behave as a voltage comparator with a high gain around its threshold.

V_{ax}

$\Delta V_{ax}|_{\Delta t}$

V_a

$\Delta V_a|_{\Delta t}$
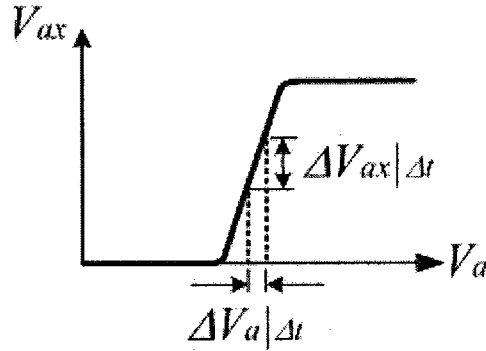
Fig. 3.12 Voltage transfer characteristic of the unit SEB.

To implement the unit of SEB, one can use an OpAmp-based voltage comparator with a DC voltage input as V_{th}. However, this implementation results in a significant static power dissipation of the unit as it needs bias currents. Another option is to use CMOS gate for the same purpose.

A CMOS inverter has its non-linear voltage transfer characteristic as shown in Fig. 3.13 (a). Its dV_o/dV_i around its threshold level is quite high, and thus it can be used as a voltage comparator. In terms of power dissipation, it operates without bias currents, i.e. no static power dissipation. Moreover, if the same voltage is applied to switch V_o in (a) and V_d in (b) from one level to the other, the CMOS inverter in (a) dissipates much less power caused by short-circuit currents in its transition than that of the latch in (b).

The threshold of an inverter and V_{ref} of the latch shown in Fig. 3.13 are determined by the parameters of the devices involved. The noise in each of the devices contributes to the variation, ΔV_{th} or ΔV_{ref}. Under the same conditions, e.g. temperature variation in the environment, ΔV_{th} is expected to be smaller than ΔV_{ref}. Also, as mentioned above, with the same input V_a, the transition time in the inverter is much shorter than that of the latch, which makes the device noise less effective to shift the level of V_{th} than that of V_{ref}. Moreover, as the noise of a device is related to its conducting condition, short-circuit

currents contribute significantly to ΔV_{th} or ΔV_{ref} during the transition. The duration of the short-circuit current in the inverter is much shorter than that in the latch under the condition of V_a specified in Fig. 3.13 (b). Therefore, the threshold variation ΔV_{th} should be much less than ΔV_{ref}.
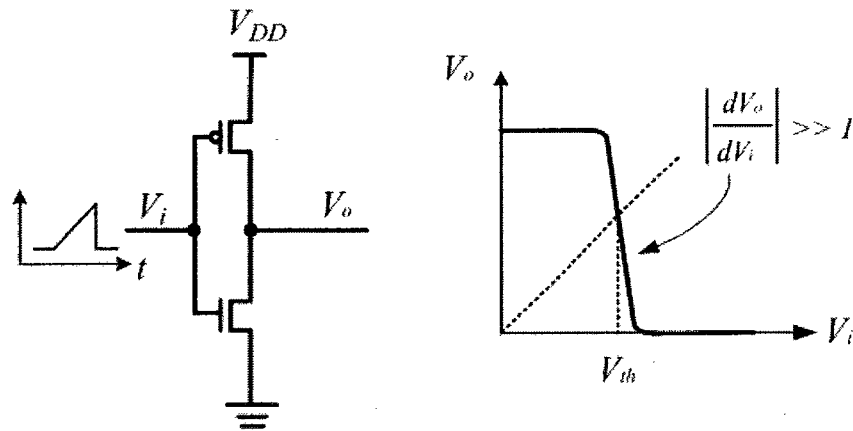
(a)
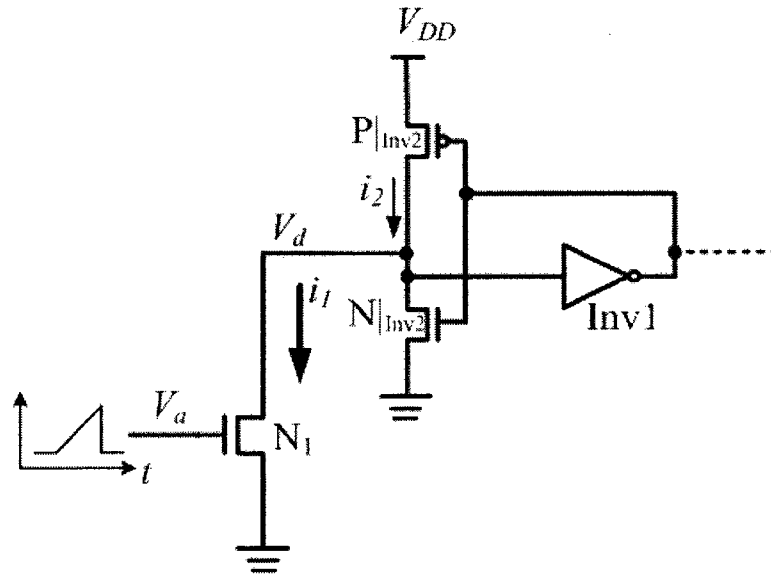
(b)

Fig. 3.13 Threshold of an inverter and V_{ref} of the latch. (a) A CMOS inverter and its non-linear voltage transfer characteristic. (b) The latch with the pull-down NMOS transistor.

From the above discussion about the SEB based on CMOS inverters, one can see that by incorporating such a block, the performance, in terms of phase accuracy and power dissipation, of the ICO can be improved. However, one should note that V_a in Fig. 3.8 is a rising voltage used to pull the voltage V_d down and V_{ax} should also be a rising one, but with a much higher rate. A single CMOS inverter can convert the slow-rising V_a to a fast-falling voltage, but not a fast-rising one. Thus, straightforwardly, one can use two cascaded inverters to generate V_{ax} from V_a for the pull-down of the voltage V_d. A SEB can, therefore, be built, in general, with two cascaded inversion stages that make effectively the conversion of the voltage rising rate. CMOS inverters can evidently be used for this purpose. The circuit shown in Fig. 3.14, named as ICO_NA, is an example.
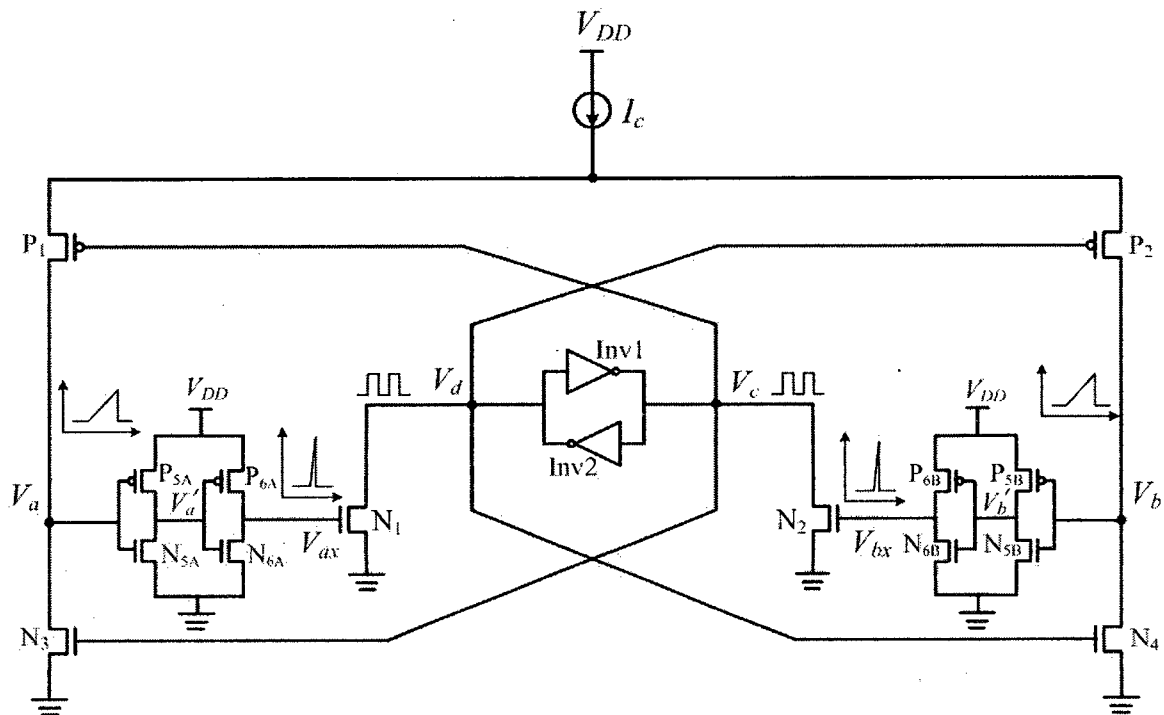
Fig. 3.14 Circuit diagram of ICO_NA.

The circuit shown in Fig. 3.14 is based on ICO_W but with two SEB inserted, one for the conversion of V_a to V_{ax} and the other V_b to V_{bx}, to reduce the phase noise and the

power dissipation. Each SEB consists of two cascaded CMOS inverters. Each of the inverters contributes to the conversion of a slow dV_a/dt to a much faster dV_{ax}/dt. Among the two inverter stages, the first one is more important than the other as its input signal is a slow-varying one that makes both transistors in the first stage, for example P_{5A} and N_{5A} in the left side, conduct during a relatively long interval. In this case, the NMOS N_{5A} should be much more conducting than the PMOS P_{5A} so that $V_a{}'$ can be reduced quickly in order to improve $|dV'_a/dt|$. With a given size of P_{5A}, the aspect ratio of N_{5A} is critical determining the time rate of dV'_a/dt that determines the rate of dV_{ax}/dt. In general, N_{5A} should be sized a few times lager than P_{5A}, as shown in Fig. 3.15, so that it can provide a much stronger current than P_{5A} to make $V_a{}'$ decrease quickly.
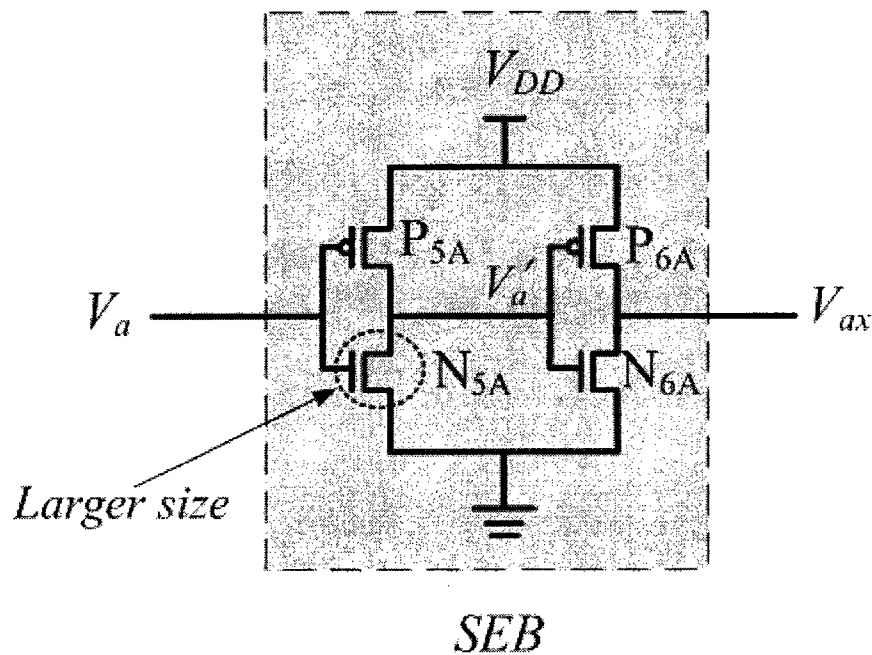
Fig. 3.15 SEB consisting of two inverters. The NMOS N_{5A} is sized larger in order for $V_a{}'$ to fall quickly when a slow-varying V_a is applied.

This sizing may make the short-circuit current increase during the transition when V_a is increasing. It should be noted that, such a transistor sizing can also change the short-

circuit current when V_a is falling. However, as V_a falls quickly, the short-circuit current in the inverter does not last long. Also, as mentioned previously, it is the rising edge of V_a determining the time of switching the latch, the falling edge has little effect on the phase-noise performance of ICO_NA, as the timing scheme of the oscillator is not based on it.

In general, the aspect ratios of the transistors in the CMOS inverter in the SEBs determine its characteristics. Adjusting the transistor sizing, one can modify the propagation delay of the inverters, and thus the frequency range. However, if the most of devices are minimal sized, to have the minimum values of capacitances, the delay of the SEBs will not be significant compared to that of the latch.

Based on the analysis presented above, one can see that by means of the slope-enhancement blocks (SEBs) based on the cascaded CMOS inverters, the time rate of the voltages applied to switch the latch can be improved significantly without varying the timing of the circuit. This improvement should result in a much reduced transition time for toggling the latch on one hand, and reduced short-circuit current on the other hand. The SEBs dissipate certain power but the amount is expected to be much less than that of the latch switched with V_a and V_b applied directly to its pull-down transistors. The additional delay introduced by the CMOS-inverter-based SEBs is also expected to be negligible compared to the duration of the oscillation cycle.

3.3.2 Design of the Circuit of ICO_NB

The introduction of the CMOS-inverter-based SEBs into the ICO circuit helps to reduce the phase noise by improving the time rate of the voltage used to switch the latch. The slow-varying V_a is applied to the CMOS inverters, instead of the pull-down NMOS

of the latch. As described in the preceding sub-sub-chapter, if the V_a is applied to the inverter, its transient time is much shorter than that in the case V_a applied directly to the pull-down NMOS of the latch. However, as this slow-varying V_a is applied to both NMOS and PMOS of the inverter, there has to be a period when the short-circuit current is not zero. This period can not be shorten by simply adjusting the device sizes. If this period is shorten and the amplitude of the short-circuit current is reduced, the V_a' will be made to fall faster, as shown in Fig. 3.16, resulting in a reduction of the phase noise and power dissipation.
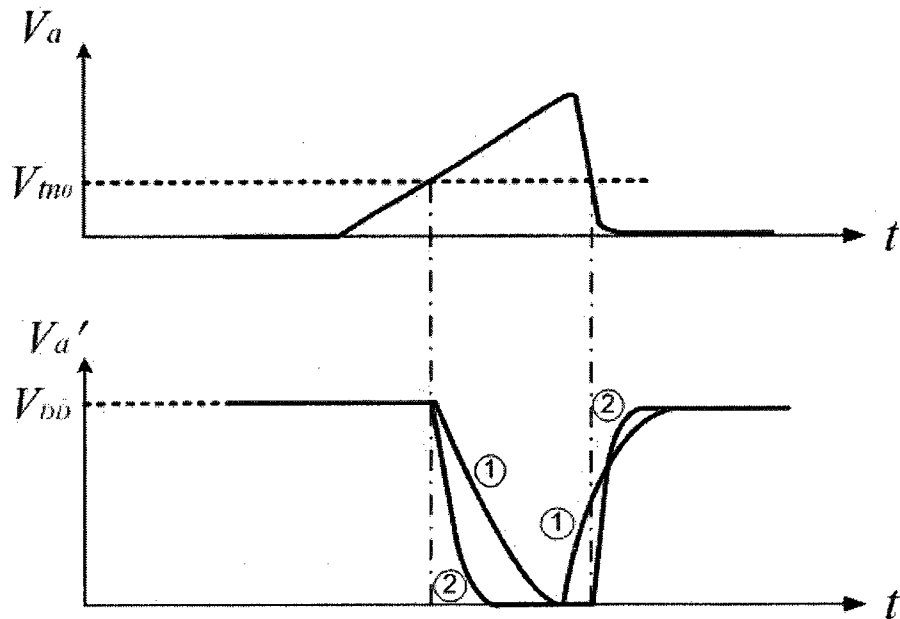
Fig. 3.16 Waveforms of V_a and V_a' in two cases. The voltage V_a is applied to two inverters. The waveform (2) is produced in the inverter that is designed to have a lower short-circuit current and shorter transient period than that produces the waveform (1).

In order to reduce the period of the non-zero-short-circuit current in the first inverter, the PMOS and NMOS should not be made conduct simultaneously. That requires a

separation of the gate voltage of the PMOS from that of the NMOS in such a way that, while the NMOS is conducting when V_a rises to be higher than the threshold voltage of the NMOS. The desirable gate voltage of the PMOS is shown in Fig. 3.17.

(a)   (b)
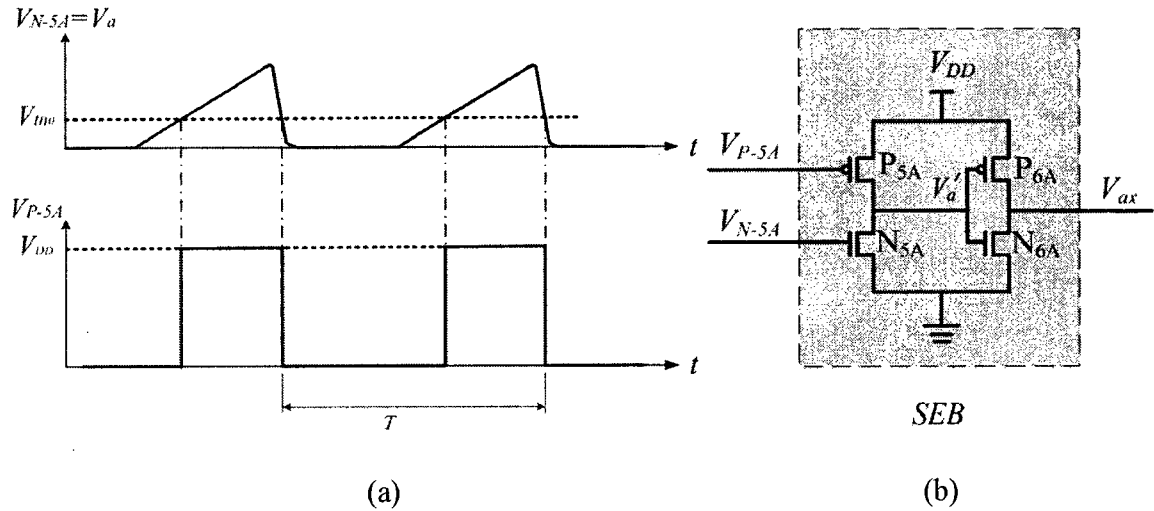
Fig. 3.17 Anticipated waveforms in (a) of the gate voltages of the first inverter of the SEB in (b). The slow-varying voltage V_a is applied to the NMOS gate while the PMOS gate voltage is in its high level when V_a is higher than V_{tn0}.

As shown in Fig. 3.17, the waveform of the gate voltage of P_{5A} needed to reduce the short-circuit current has some dependency on V_{N-5A}. Hence, the voltage signal should be generated in the ICO circuit to secure the dependency.

Fig. 3.18 shows the waveforms of the voltage signals in the ICO circuit. Among the voltages, V_d has the closet waveform shape to that of V_{P-5A}. Comparing the two voltages, one can find that V_d is at its high level of V_{DD} during most time of the period when V_a is greater than V_{tn0}. However, it goes to the low level shortly before the end of the period. Let t_d denotes the interval between the moment when V_d is turned to its low level and that when V_a is reset to zero volt by the rising edge of V_c. During t_d, as V_a is still at its high level, if the gate voltage of P_{5A} is low, the magnitude of the short-circuit current of the

first inverter can be very large, dissipating significant power. Therefore, V_d can not be applied directly to the gate of P_{5A}. Nevertheless, one can used a delay device to produce a delayed version of V_d and the delay should at least be t_d.
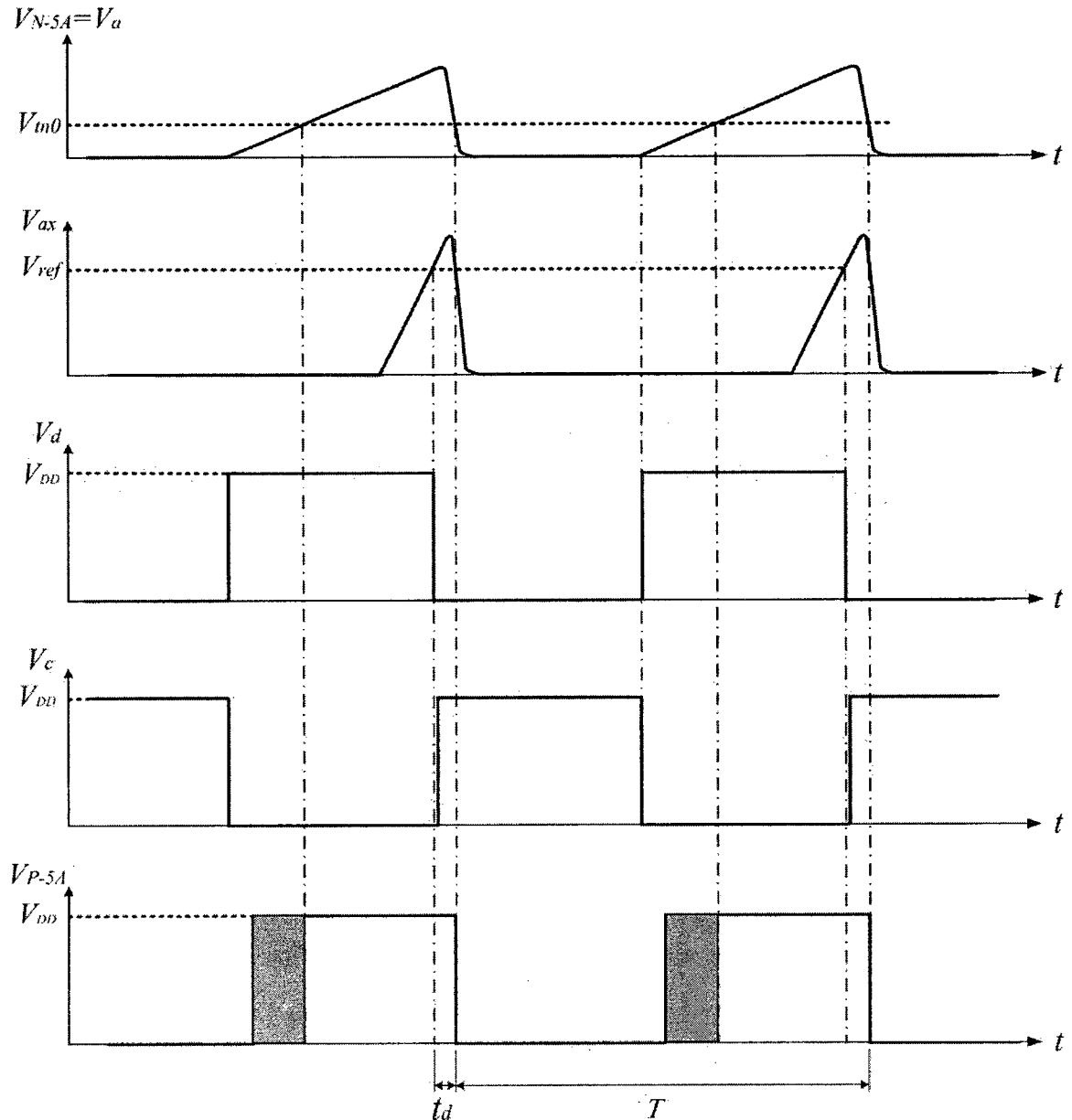
Fig. 3.18 Waveforms of the voltage V_a, V_{ax}, V_d and the anticipated V_{P-5A}. The level of V_{P-5A} is not critical during the interval marked gray.

Based on the analysis described above, two cascaded inverters are used as the delay device to generate V_{P-5A} from V_d. Using this delay device and the SEBs of two inversion stages, the ICO circuit is transformed as shown in Fig. 3.19, and it is called ICO_NB. In this circuit, the delay between V_{P-5A} and V_d is approximately the sum of those of two small inverters, considering t_d is, in fact, the sum of the time needed for the latch to switch and that for V_a to reset. The total delay of the two inverters in the delay device is approximately sufficient for the falling edge of V_{P-5A} to come after V_a becomes low enough to turn off the NMOS N_{5A}. With such a gate voltage applied to P_{5A} and V_a to N_{5A}, a much small amplitude of the short-circuit current and shorter transient time should be expected in the first inversion stage of the SEBs.
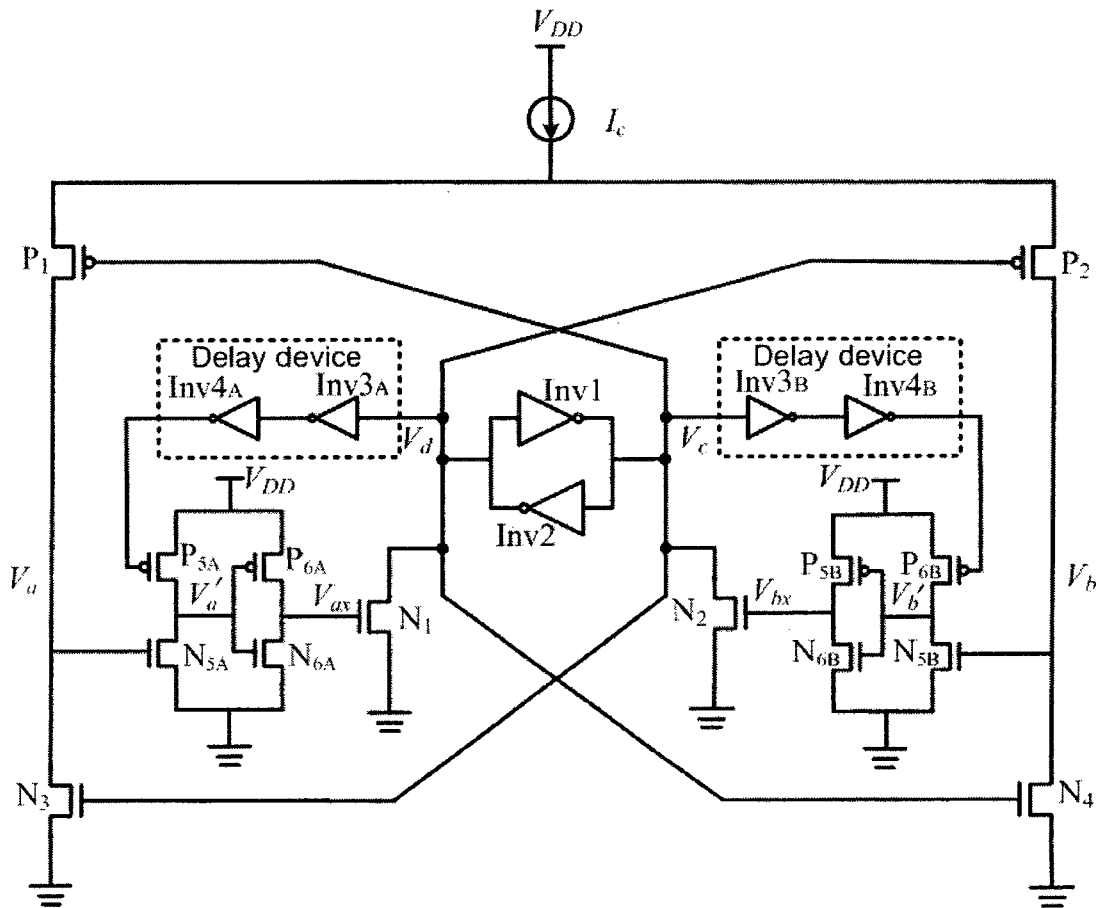
Fig. 3.19 Circuit diagram of ICO_NB.

It should be noted that the two-inverter delay devices are placed at the two outputs, respectively, of the ICO circuit, as shown in Fig. 3.19. In case that the inverters of the latch and those in the delay devices are all minimum-sized, the introduction of the delay devices increases the load capacitances of the latch and thus modulate the transient time when the latch is switched. Therefore, while a significant reduction of power dissipation is expected, one should not anticipate the reduction of the phase noise by ICO_NB.

3.4 Summary

In this chapter, the problems of phase noise and power dissipation in ICO_W circuit have been analyzed. This analysis led to a proposal of a method to solve the problems. It is to introduce a Slope-Enhancement-Block (SEB) to the ICO circuit, aiming at a faster switching of the state of the latch without interfering the timing scheme of the ICO circuit. Two different SEBs have been designed and incorporated in ICO_W circuit resulting in two new versions of ICO circuits. A significant reduction of the phase noise and power dissipation is anticipated in these two ICOs.

In the next chapter, the simulation results of the two new ICOs will be presented to evaluate their performance. The comparison of the two ICOs with ICO_W and other ICO/VCO circuits in the similar category will also be presented.

Chapter 4

Performance Evaluation and Simulation Results

In Chapter 3, the two versions of the current-controlled oscillators based on the circuit ICO_W have been designed using the method proposed in this thesis. In this chapter, the performance evaluation of the new ICO circuits with the simulation results is presented. The models of a CMOS 0.18µm technology is used in Spectre simulation.

For an assessment of the phase noise reduction, Periodic Steady State(PSS) analysis and Periodic Noise (Pnoise) analysis in SpectreRF simulator are used [25,26]. The circuit simulation consists of two phases. In the first phase, the transistors are mostly minimum-sized as those in ICO_W, to evaluate the effectiveness of the noise reduction by the application of the proposed method. In the second phase, the device sizes are tuned to suite the high frequency oscillation in order to validate the proposed method in the application in high frequency ranges.

4.1 Performance Evaluation of the Minimum-Sized ICO_NA and ICO_NB

The current-controlled oscillator ICO_W is designed with all the transistors minimum-sized. For a good assessment of the performance improvement resulting from

the application of the proposed method, the circuits of ICO_NA and ICO_NB are simulated, in the first step of this phase, with all the transistors minimum-sized. Then, in the second step, some transistors are tuned for further improvement. In both steps, the phase noise and power dissipation characteristics of the circuits are obtained for the performance evaluation and presented in this sub-chapter.

4.1.1 Simulation of ICO_NA and ICO_NB with All the Transistors Minimum-Sized

The first characteristics of the circuits obtained in the simulation are of the oscillation frequency versus the input current. The results are shown in Fig. 4.1.
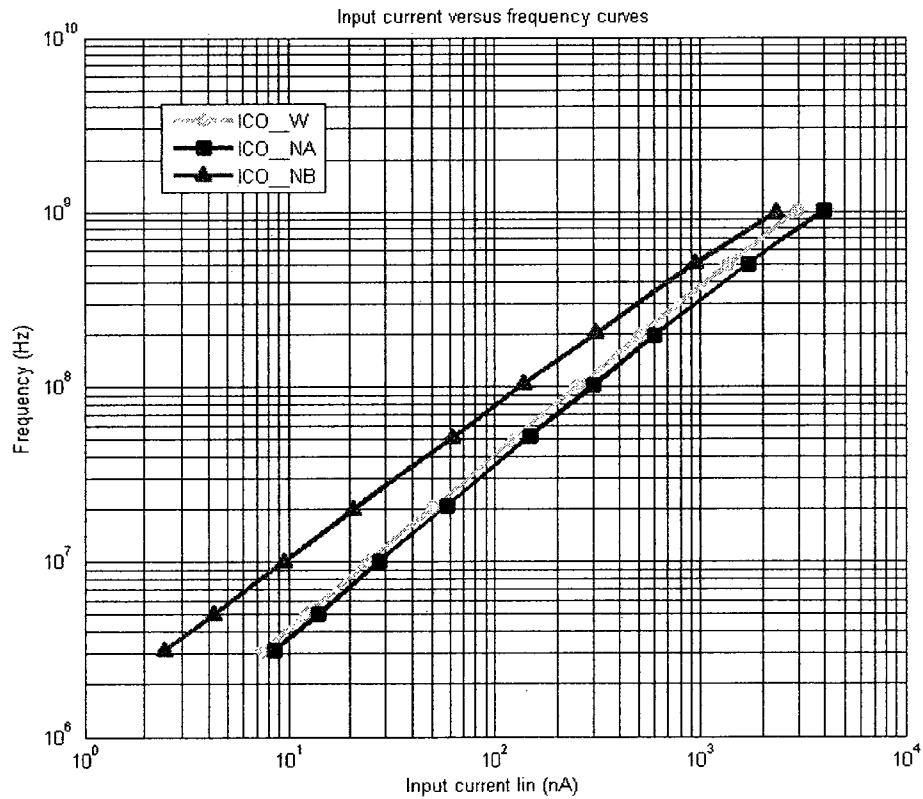
Fig. 4.1 Characteristics of oscillation frequency versus input current of ICO_W, ICO_NA and ICO_NB.

It is observed from Fig. 4.1 that if the input current in ICO_NA is ranged from 8.5 nA to 4 µA, the corresponding oscillation frequency range is from 3 MHz to 1 GHz. It demonstrates that, the frequency range of the ICO is almost the same as that of ICO_W. The introduction of the two Slope-Enhancement-Blocks (SEBs) affects little the timing scheme of the ICO circuit and thus neither the frequency range. The operation range of ICO_NB is slightly shifted towards the lower current end compared to that of ICO_W, but not narrowed.

As the performance of an ICO is also characterized by the power and noise, the simulation results of the phase noise and power dissipation of these three ICO circuits, namely ICO_W, ICO_NA and ICO_NB, are shown in Fig. 4.2 and Fig. 4.3, respectively.
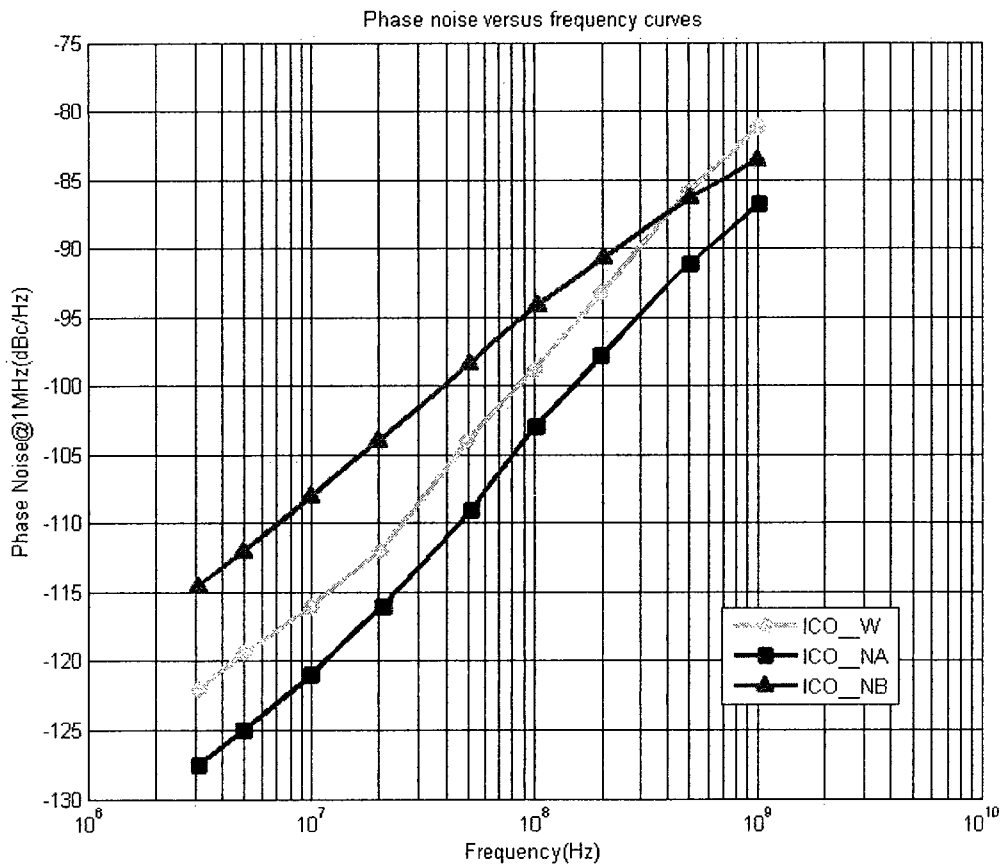
Fig. 4.2 Phase noise of ICO_W, ICO_NA and ICO_NB versus oscillation frequency at 1MHz offset frequency from each carrier.
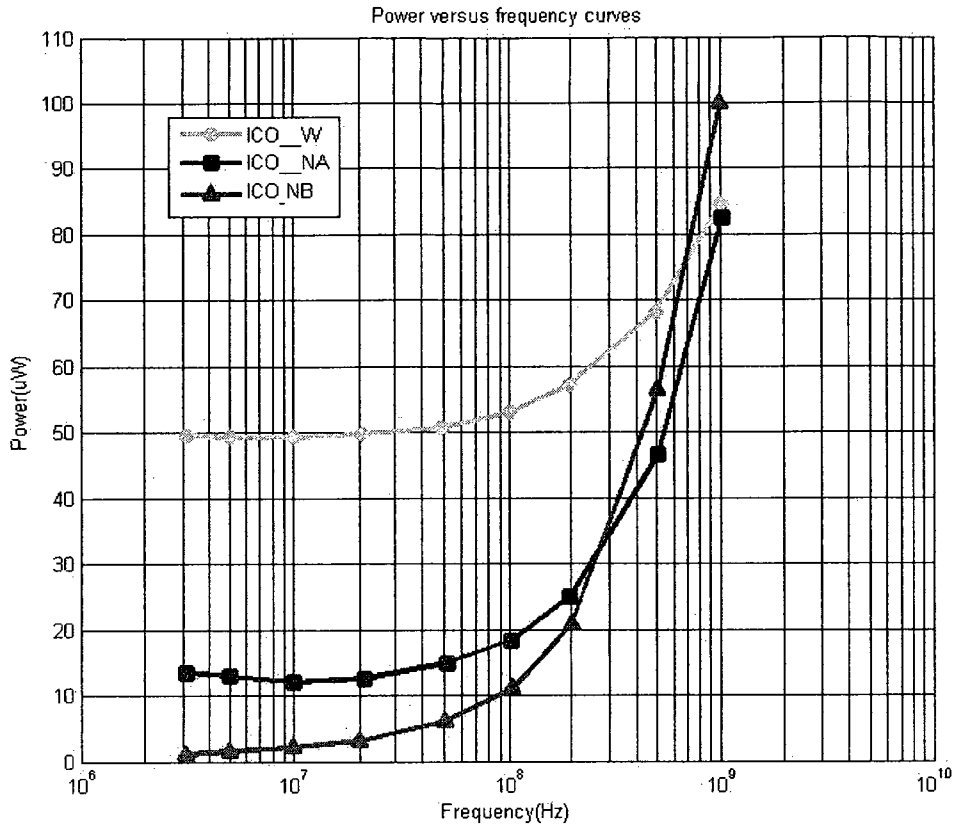
Fig. 4.3 Power dissipation of ICO_W, ICO_NA and ICO_NB versus oscillation frequency.

Table 2, Table 3 and Table 4 provide the numeric data of the phase noise and power dissipation of the three circuits extracted from the characteristics presented in Fig. 4.2 and Fig. 4.3.

TABLE 2

PERFORMANCE COMPARISON OF ICO_NA, ICO_NB AND ICO_W AT 3 MHz

	ICO_W	ICO_NA	ICO_NB
size	Minimal size	Minimal size	Minimal size
frequency	3 MHz	3 MHz	3 MHz
Phase noise@1MHz	-122 dBc/Hz	-127.5 dBc/Hz	-114.5 dBc/Hz
power	49.7 uW	13.5 uW	1.09 uW

TABLE 3
PERFORMANCE COMPARISON OF ICO_NA, ICO_NB AND ICO_W AT 100 MHz

	ICO_W	ICO_NA	ICO_NB
size	Minimal size	Minimal size	Minimal size
frequency	100 MHz	100 MHz	100 MHz
Phase noise@1MHz	-98 dBc/Hz	-103 dBc/Hz	-94 dBc/Hz
power	53.0 uW	18.3 uW	11.1 uW

TABLE 4
PERFORMANCE COMPARISON OF ICO_NA, ICO_NB AND ICO_W AT 1GHz

	ICO_W	ICO_NA	ICO_NB
size	Minimal size	Minimal size	Minimal size
frequency	1 GHz	1 GHz	1 GHz
Phase noise@1MHz	-81 dBc/Hz	-87 dBc/Hz	-84 Bc/Hz
power	84.5 uW	82.5 uW	100 uW

The characteristics in Fig. 4.2 demonstrated that the phase noise in ICO_NA is at lest 5dBc/Hz lower than that in ICO_W over the entire frequency range. As analyzed in Chapter 3, this reduction of phase noise in ICO_NA results from the increase of the time rate of the voltage applied to the pull-down NMOS of the latch by using the two SEBs. As expected, the same SEBs also help to lower the power dissipation in ICO_NA with respected to that of ICO_W, as shown in Fig. 4.3. The power dissipation is reduced with the short-circuit current in the latch as its switching time is shortened by the SEBs.

By observing the characteristics in Fig. 4.2 and 4.3, and the data in the three tables as well, one can make a comparison between ICO_NB and ICO_W. As anticipated, the

power dissipation in ICO_NB is reduced in a considerably manner, which is shown in Fig. 4.3, especially in two lower decades of the frequency range. As shown in Table 1 and 2, the circuit ICO_NB dissipates only 1/50 of the power that ICO_W does at the frequency of 3 MHz and 1/5 at the frequency of 100 MHz. The power dissipation of ICO_NB is slightly higher when the frequency is above 700 MHz. For example, at the oscillation frequency of 1 GHz, it dissipates 100 µW, compared to 84.5 µW in ICO_W, which is only 20% higher.

It is also observed that ICO_NB does not yield a better performance in terms of phase noise, compared to ICO_W and ICO_NA. As described in Chapter 3, it is due to the larger number of transistors used in the circuit, as each of them contributes a noise source. In the case of ICO_NA, the noise reduced by the SEBs is more significant than that added by the transistors in the SEBs, resulting in a good noise reduction. Adding the delay devices in case of ICO_NB leads to a better performance in terms of power, but the added transistors add more noise, making the noise performance degraded.

The output oscillation waveforms of the three ICOs, namely ICO_W, ICO_NA and ICO_NB, at 3 MHz, 100 MHz and 1 GHz are shown in Fig. 4.4. It is visibly that the quality of square-wave voltage produced by ICO_NA or ICO_NB is much better than that of ICO_W. The waveforms show that, the use of the SEBs helps not only the reduction of the phase noise and the power dissipation, but also improves the quality of the signals generated in the ICO, without adding the buffers to shape the signals.
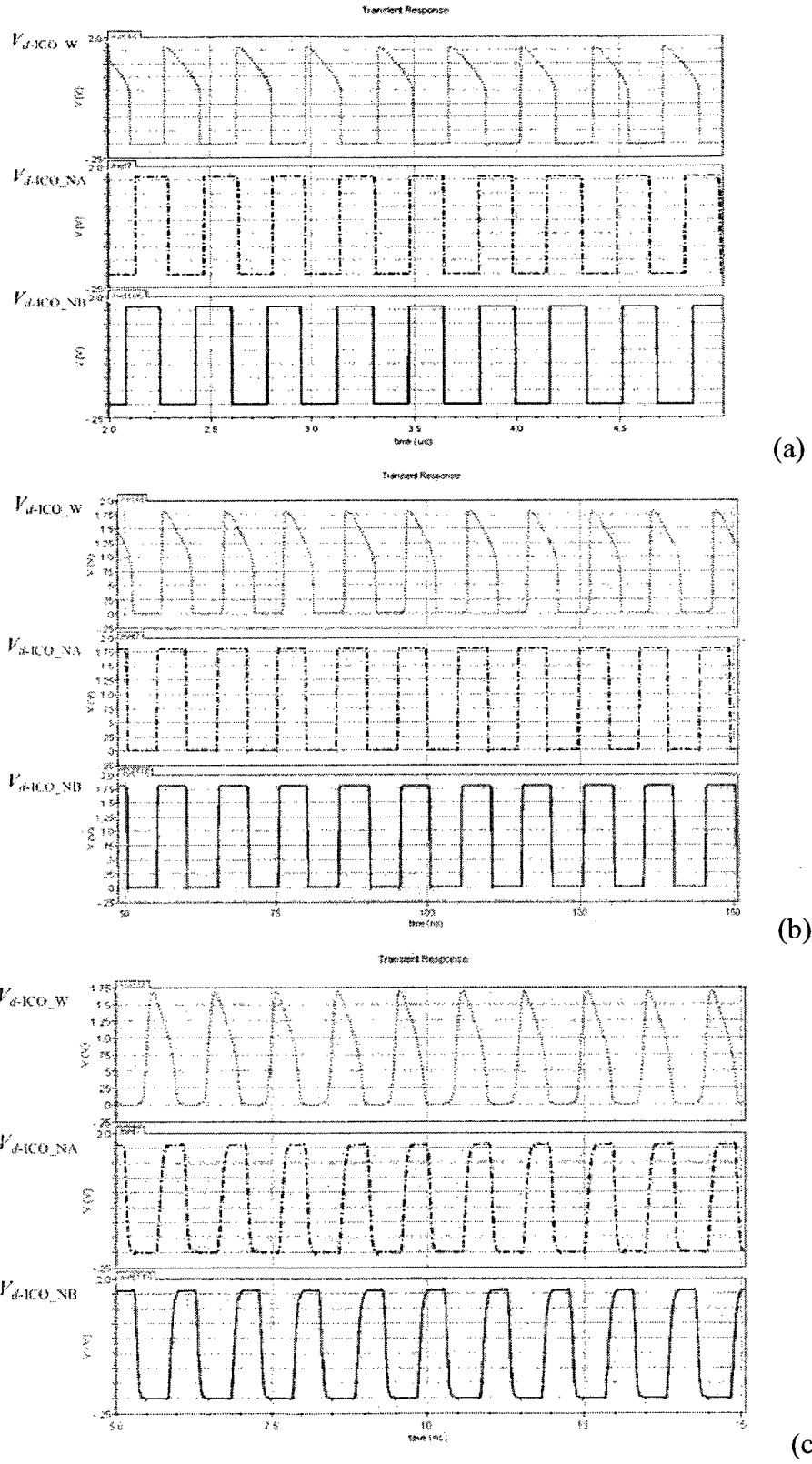
Fig. 4.4 Simulation waveforms of the output voltages at V_d node generated by ICO_W, ICO_NA and ICO_NB at 3MHz in (a), at 100MHz in (b) and at 1GHz in (c).
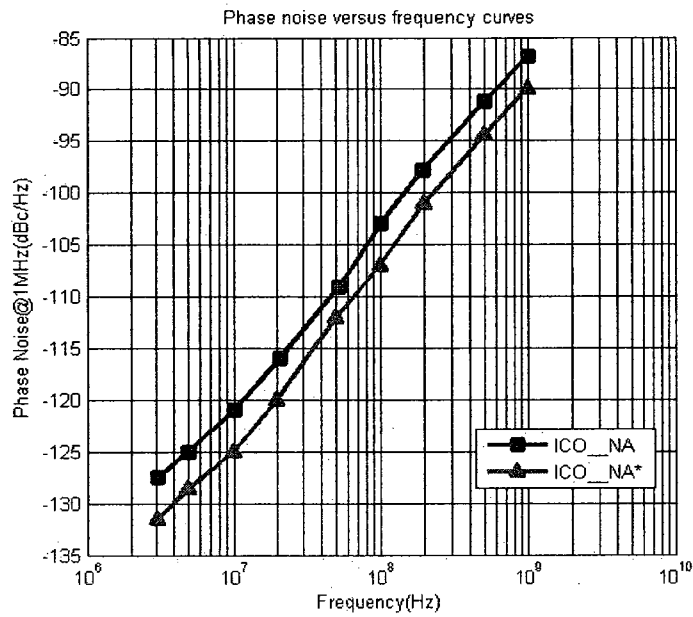
4.1.2 Performance Comparison of ICO_NA and ICO_NA*

In previous sub-sub-chapter, the transistors in ICO_NA and ICO_NB are all minimum-sized to have a fair comparison of the performance with the circuit of ICO_W. However, if a moderate size change of a few transistors is allowed, the circuit ICO_NA can have a further reduction of the phase noise.

In each of the SEBs employed in ICO_NA, their input voltage V_a, or V_b, is slow-varying signal. The objective of using SEB is to convert this signal into a fast-varying one in order to reduce the phase noise. In other words, the SEB is to make the conversion ratio $\left|\dfrac{dV_a'/dt}{dV_a/dt}\right|$, where V_a' is the voltage obtained after the first inverter in the SEB, as large as possible. The change rate dV_a'/dt is related to the sized of the transistors in the first inverter. The condition of the all-minimum-size in ICO_NA makes constrains for maximizing the conversion ratio. The circuit ICO_NA* is based on ICO_NA, and the only difference is that the NMOS transistor in the first inverter in each of the two SEBs is made about 7 times wider compared to the minimum width. The wider NMOS gate helps to accelerate the output voltage falling of the inverter. It should be mentioned that, an increase of the power dissipation should be expected with this device-size change.

The characteristics of phase noise and power dissipation versus frequency obtained in the SpectreRF simulation of ICO_NA* and ICO_NA are shown in Figs. 4.5 (a) and (b), respectively. The numeric data of the phase noise and power dissipation of the two oscillators extracted from the characteristics presented in Fig. 4.4 are listed in Table 5. The results show that, by means of changing only one transistor in the SEB to improve the conversion ratio, a further reduction of the phase noise, which is 3 dBc/Hz over the entire frequency range, is achieved. The increase of the power dissipation is from 28% to

36% over the frequency range, which is less significant than the improvement of the phase-noise reduction.

(a)
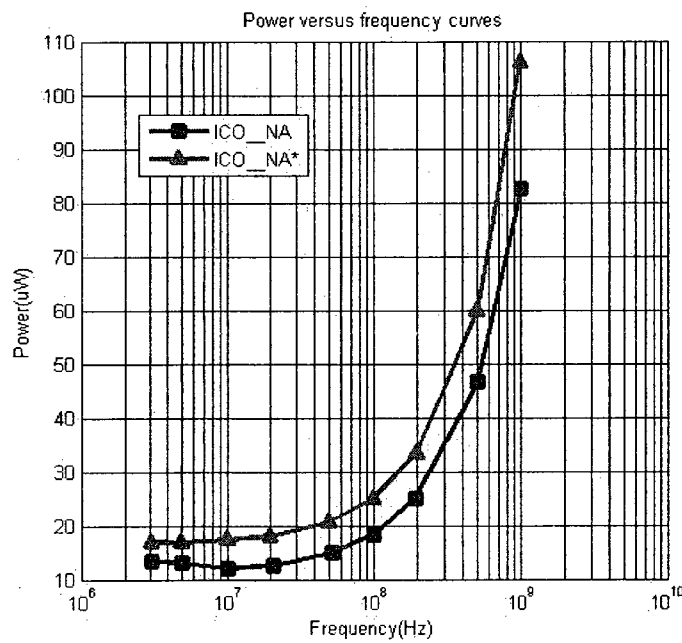
(b)

Fig. 4.5 Performance comparison of ICO_NA and ICO_NA*. (a) Phase noise of ICO_NA and ICO_NA* versus the oscillation frequency at 1MHz offset frequency from each carrier. (b) Power dissipation of ICO_NA and ICO_NA* versus the oscillation frequency.

TABLE 5

PERFORMANCE COMPARISON OF ICO_NA WITH ICO_NA*

	ICO_NA	ICO_NA*	ICO_NA	ICO_NA*
size	Minimum-size	W/L of N_{5A} is 1.5 /0.18 Other transistors are minimum-sized	Minimum-size	W/L of N_{5A} is 1.5 /0.18 Other transistors are minimum-sized
frequency	100 MHz		1.00 GHz	
power	18.3 uW	25.0 uW	82.5 uW	106 uW
Phase noise @1MHz	-103 dBc/Hz	-107 dBc/Hz	-87 dBc/Hz	-90 dBc/Hz

The circuits of ICO_NA and ICO_NB are able to operate in the current range from 2.5 nA to 4 μA that corresponds to the frequency range from 3 MHz to 1 GHz. It has been demonstrated by the simulation that the introduction of the SEBs to the circuit of ICO_W make the significant improvement of the phase-noise reduction with an insignificant power increase. Therefore, both ICOs have better performance than that of ICO_W, without losing the ability of operating under a weak input current. In the next sub-chapter, the simulation of the ICO circuits having the exactly same structure but the device sizing more radically to achieve the performance of low phase noise are presented.

4.2 Performance Evaluation of ICO_NA and ICO_NB without the Size Restriction

In the previous sub-chapter, the simulation has been done under the condition that minimum-sized transistors are used in ICO_NA and ICO_NB in order to have a fair

comparison of the performance with that of ICO_W. This sub-chapter is to present the simulation results of the ICO circuits that have the same structures as those in the previous sub-chapter, but without the restriction of the minimum size.

The ICOs of minimum-sized transistors have advantages of high sensitivity to input current signal, i.e. a high ratio of the frequency variation to that of the current. This features an excellent capacity of detecting weak current variation. However, the weak current in the different parts of such an oscillator does not make a favorite condition for low phase noise. It is thus evident why most of the oscillators of low phase noise found in literature have high biasing currents. To compare the performance of the proposed ICO circuits with those in literature, the sizes of the transistors need to be changed to have stronger currents. Nevertheless, it should be noticed that, this change of the device sizes will lead to a lower sensitivity of current detection, if the frequency range remains the same.

In this phase of simulation, the transistor sizing of the circuit ICO_NA and that of ICO_NB are presented in Tables 6 and 7. With such device dimension, the frequency range versus the input current is modified, compared to the circuits of minimum-sized devices, as shown in Fig. 4.6. As expected, the range of the frequency of the output voltage is as wide as that presented in Fig. 4.1. However, for the same amount of frequency variation, the current variation needs to be 1000 times larger.

TABLE 6

SIZE RATIOS (W/L) OF TRANSISTORS IN THE NON-MINIMUM-SIZED ICO_NA (μM/μM)

NMOS in Inv1,Inv2 N_3, N_4, N_{6A}, N_{6B}	25 / 0.18	PMOS in Inv1,Inv2 P_1, P_2, P_{4A}, P_{4B}	40 / 0.18
N_1,N_2	45 / 0.18	P_{3A}, P_{3B}	70 / 0.18
N_{5A},N_{5B}	900 / 0.18		

TABLE 7

Size ratios (W/L) of transistors in the non-minimum-sized ICO_NB (μM/μM)

NMOS in Inv1,Inv2 N_3, N_4, N_{6A}, N_{6B}	25 / 0.18	PMOS in Inv1,Inv2 P_1, P_2, P_{4A}, P_{4B}	40 / 0.18
NMOS, PMOS in Inv3$_A$,Inv3$_B$	2.5 / 0.18	NMOS, PMOS in Inv4$_A$,Inv4$_B$	1.5 / 0.18
N_1, N_2	45 / 0.18	P_{3A}, P_{3B}	70 / 0.18
N_{5A}, N_{5B}	900 / 0.18		

Input current versus frequency curves

Legend: ICO_NA_mini, ICO_NB_mini, ICO_NA_non-mini, ICO_NB_non-mini

Frequency (Hz) vs Input current Iin (uA)
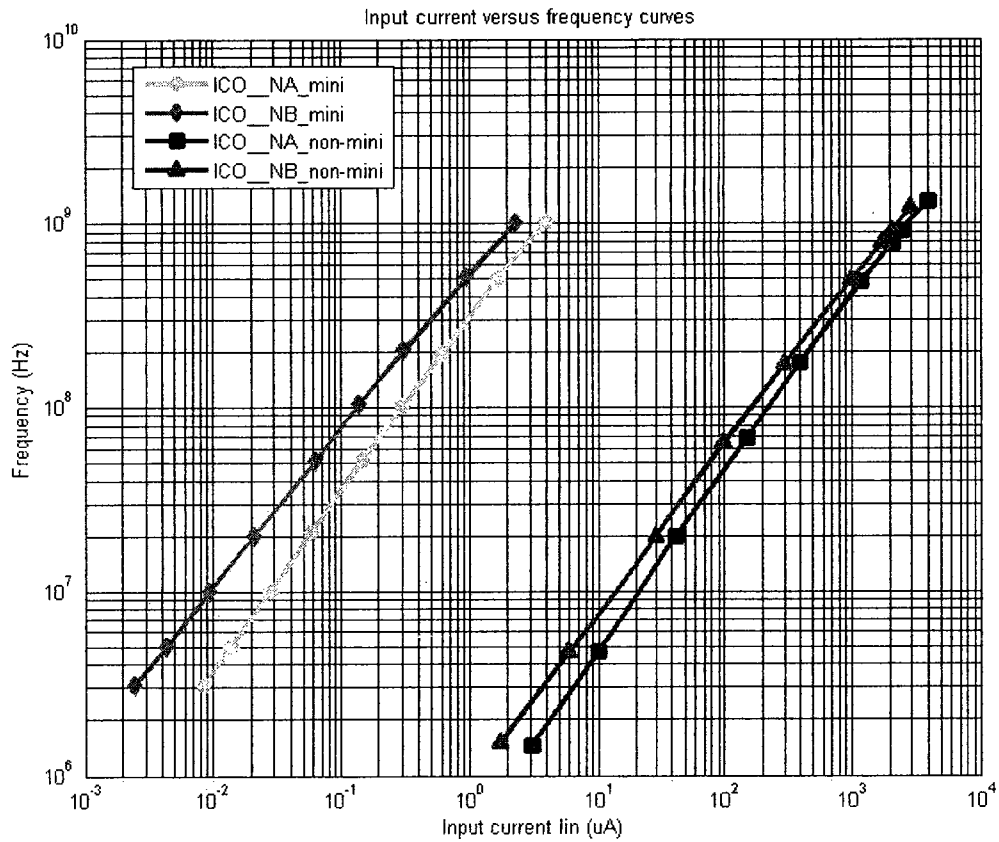
Fig. 4.6 Characteristics of oscillation frequency versus input current of ICO_NA and ICO_NB with non-minimum-sized transistors. The results obtained in the simulation of the circuits with minimum-sized devices are also presented in the figure for comparison.

The simulation results of the phase noise and power dissipation of these two ICO circuits are shown in Figs. 4.7 and 4.8, respectively. By increasing the device sizes, i.e. the operating currents, the phase noise over the frequency range has been reduced about 30 dBc/Hz in the ICOs, compared to the results obtained in case of the minimum sizing. The power dissipation of the ICOs with non-minimum-sized transistors is approximately 200 times higher than that of the ICOs with minimum-sized transistors. In other words, the reduction of the phase noise of 30 dBc/Hz has been achieved at the expense of the power-dissipation increase of only 200 times.
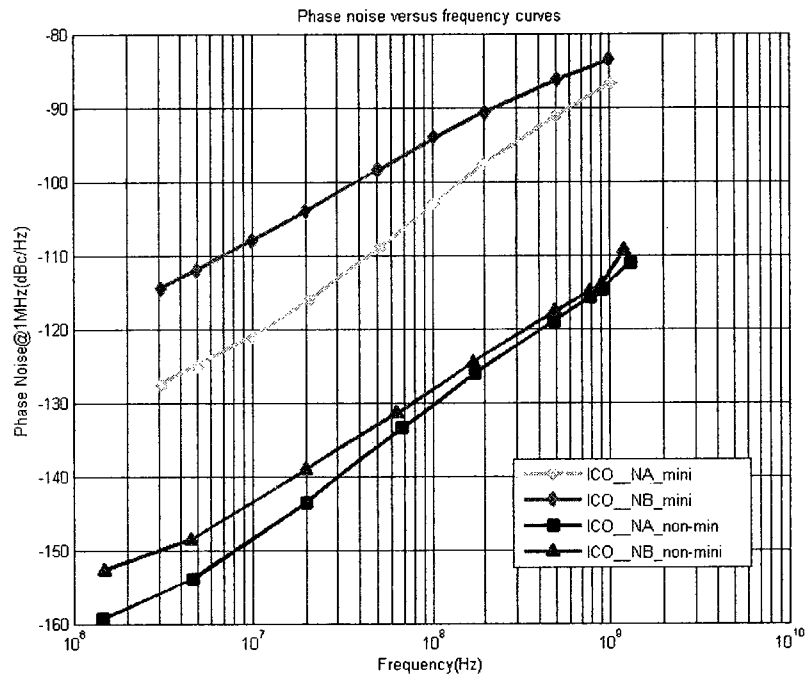
Fig. 4.7 Phase noise of ICO_NA and ICO_NB versus the oscillation frequency. The results obtained in the simulation of the circuits with minimum-sized devices are also presented in the figure for comparison.
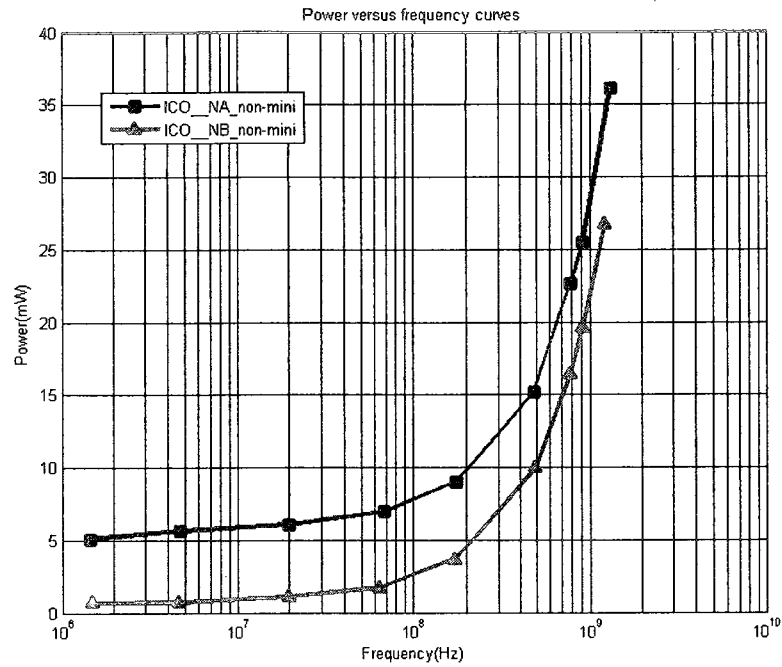
Fig. 4.8 Power dissipation of ICO_NA and ICO_NB versus oscillation frequency.

The layout of ICO_NA and that of ICO_NB have been sketched with the transistor sizes specified in Table 5 and 6. They are shown in Fig. 4.9. The area for each of the circuits is $57 \times 69 \mu m^2$. The post-layout simulation of the phase noise and power dissipation has been conducted, and the results are very similar to those obtained from their schematic simulation.
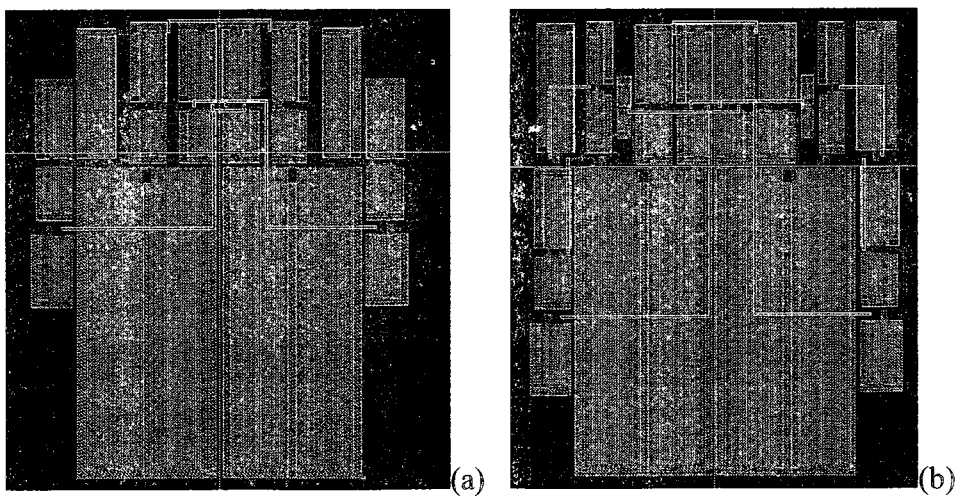
Fig. 4.9 Layout of ICO_NA in (a) and ICO_NB in (b).

Table 8 presents the specification of some of the existing oscillators considered most relevant to the designs described in this thesis. The proposed circuits, ICO_NA and ICO_NB, have the widest frequency range compared to those listed in the table. The only circuit having a comparable range is that in [23], however its range is still 33% less than that of ICO_NA. The performance of the phase noise of ICO_NA or ICO_NB is much better than that of [23] over the entire frequency range except a small part around the point of 900 MHz, which is also shown in Fig. 4.10. The power dissipation of ICO_NA and ICO_NB is comparable to that in [23], as shown in Fig. 4.11. However, taking the amplitudes of the supply voltages in those designs into account, the circuit of ICO_NA or ICO_NB is little more power-efficient than that in [23]. The last, not the least, data listed in Table 8 is about the silicon space consumption. Even with the larger transistor feature size, the circuit of ICO_NA or that of ICO_NB occupies approximately only one-third of the space required for that in [23].

TABLE 8 PERFORMANCE COMPARISON OF ICO_NA AND ICO_NB WITH OTHER REFERENCE

	Source-coupled	Cross-coupled		Dual inverter		This work	
	Hajimiri (99) [7]	Park(99) [19]	Yang(01) [20]	Badillo(03) [21]	Ke(08) [23]	ICO_NA	ICO_NB
Frequency range (MHz)	285~1190	750~1200	660~1270	475~1000	4.75~989	1.46~1315	1.51~1221
Phase noise (dBc/Hz)					-125.7 @ 1M (f_o = 4.75 MHz)	-153.9 @ 1M (f_o = 4.71 MHz)	-148.5 @ 1M (f_o = 4.66 MHz)
	-100.2 @ 1M (f_o = 1190 MHz)	-117 @ 600K (f_o = 900 MHz)	-106 @600K (f_o = 900 MHz)	-109 @600K (f_o = 900 MHz)	-106.6 @ 1M (f_o = 516 MHz)	-119.0 @ 1M (f_o = 482 MHz)	-117.6 @ 1M (f_o = 497 MHz)
					-115.4 @ 1M (f_o = 913 MHz)	-109.4 @ 600K -114.7 @ 1M (f_o = 916 MHz)	-108.6 @ 600K -113.9 @ 1M (f_o = 913 MHz)
Power dissipation	20 mW	30 mW	15.4 mW	19.2 mW	19.88 mW	26.05 mW	19.64 mW
Power supply	2.5 V	3.0 V	2.5 V	1.8 V	1.2 V	1.8 V	1.8 V
Technology	CMOS 0.25μm	CMOS 0.6μm	CMOS 0.5μm	CMOS 0.18μm	CMOS 0.12μm	CMOS 0.18μm	CMOS 0.18μm
Area	---	33066 μm²*	---	---	11680 μm²	3933 μm²	3933 μm²

* The layout of VCO took up around 1/3 of the active area of 57×69μm² for the whole chip.
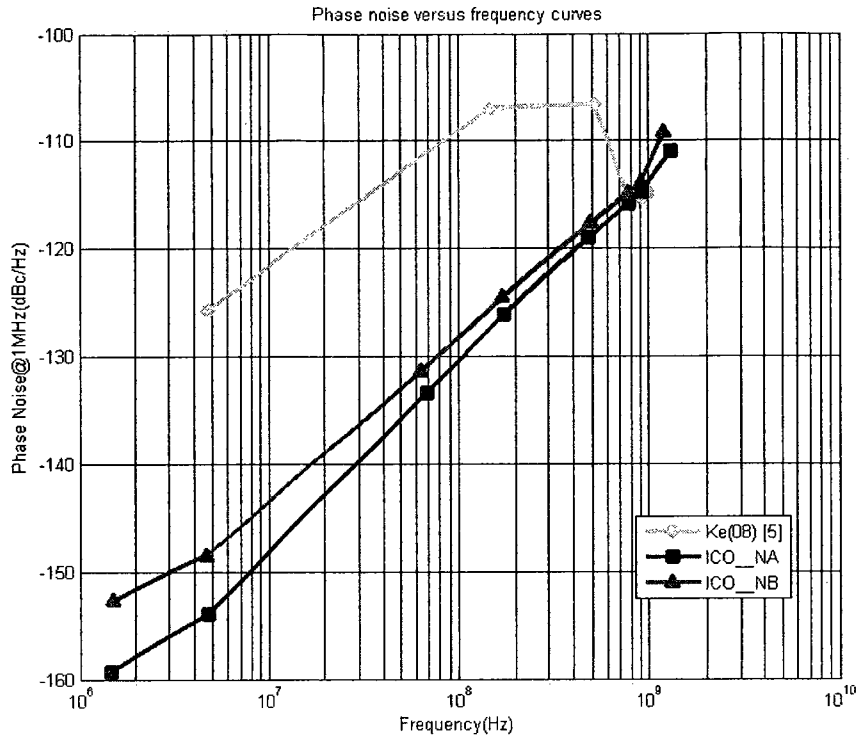
Fig. 4.10 Phase noise comparison of ICO_NA and ICO_NB with [23] versus oscillation frequency at 1MHz offset frequency from each carrier.
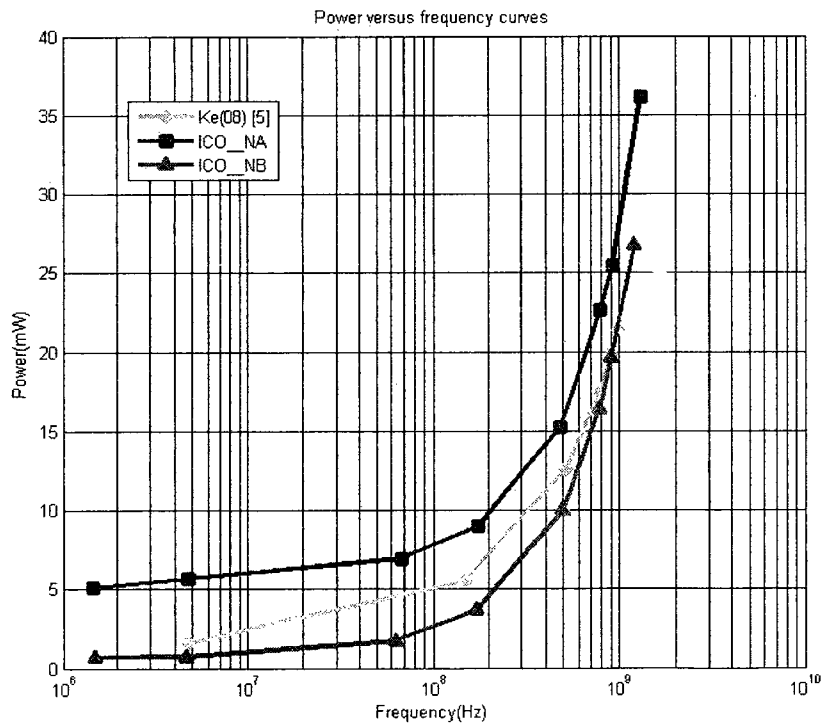
Fig. 4.11 Power dissipation comparison of ICO_NA and ICO_NB with [23] versus oscillation frequency.

4.3 Summary

This chapter is dedicated to the performance evaluation of ICO_NA and ICO_NB through Spectre simulations. The simulations have been done in two steps: one with all transistors minimum-sized and the other without that restriction.

The ICO circuits have been proposed based on that of ICO_W in which all the transistors are minimum-sized. In the first step, the circuits of ICO_NA and ICO_NB with all transistors minimum-sized have been simulated and compared with those of ICO_W. The simple structure and the wide frequency range of ICO_W are preserved in the circuits of ICO_NA and ICO_NB. As the result of the introduction of the SEBs, the phase noise and power dissipation of ICO_NA are both lower than those of ICO_W over the entire frequency range. Moreover, it has been confirmed that the insertion of the delay devices helps ICO_NB to further reduce the power dissipation, especially in the low frequency range. However, the phase noise of ICO_NB is a little degraded due to the increased number of the transistors. The quality of square-wave outputs of ICO_NA and ICO_NB have been improved compared to that of ICO_W.

In the second step, the simulation has been conducted without the device size restrictions in the two ICOs. This made the circuit operating currents stronger to be at the similar level as those of some relevant existing oscillators. The results of the simulation show that, ICO_NA and ICO_NB have much wider frequency range compared to the listed cases. The performance of phase noise of the two oscillators is better than that of the most, if not all, of them. In terms of the power dissipation, the performance of the two ICOs is comparable with others. The structure of ICO_NA, or that of ICO_NB, is

significantly simpler than most of the existing ones, which leads to a much smaller silicon space occupation than that of the others.

In conclusion, the simulation results have confirmed that the proposed oscillators have the advantages of low noise, low power, wide frequency range and small space in silicon. They can therefore be applied in different systems with low cost.

Chapter 5

Conclusion

The work presented in this thesis is in the topic area of the current-controlled oscillators. The objective of this work is to design ICO circuits with the performance of wide frequency range, high sensitivity to the control signal, low phase noise, low power dissipation, and small circuit space for the low cost with the standard CMOS technology.

Starting from the base of the work in this thesis, the ICO_W circuit, the problems of phase noise and power dissipation in ICO_W have been analyzed, which led to a proposal of a method to solve the problem. The method is to introduce a Slope-Enhancement-Block (SEB) to the ICO circuit, aiming at a faster switching of the state of the latch without interfering the timing scheme of the ICO circuit. This led to the performance of low phase-noise. As the faster switching reduced the short-circuit current in the latch at the same time, the performance of low power-dissipation also resulted from the proposed method. Two different SEBs have been designed and incorporated in ICO_W circuit resulting in two new versions of ICO circuits, ICO_NA and ICO_NB.

The performance evaluation of ICO_NA and ICO_NB has been done through the Spectre simulations in two steps: one with all transistors minimum-sized and the other without that restriction. In the first step, the circuits of the two ICOs with all transistors minimum-sized have been simulated and compared with those of ICO_W. The simple

structure and the wide frequency range of ICO_W are preserved. As the result of the introduction of the SEBs, the phase noise and power dissipation of ICO_NA are both lower than those of ICO_W over the entire frequency range. And it has been confirmed that the insertion of the delay devices helps ICO_NB to further reduce the power dissipation, especially in the low frequency range. In the second step, the simulation has been conducted without the device size restrictions in the two ICOs and their performances were compared with some relevant existing oscillators having the similar level of the operating currents. The results of the simulation show that, ICO_NA or ICO_NB has the widest frequency range, the lower phase noise than most of the listed cases, the comparable power dissipation, and a much smaller silicon space occupation than others.

The newly designed ICOs can be used in PLL, optical sensor systems or the biomolecular detection systems with their performance of low noise, low power, wide frequency range and small space in silicon.

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