A Study of Novel Fabrication Techniques for Development of 3-D Silicon Nano-structure Array

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ABSTRACT

A Study of Novel Fabrication Techniques for Development of 3-D Silicon Nano-structure Array

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The large surface area and high aspect ratio of nano-structures make them promising candidates as a fundamental building block for manufacturing various devices. The potential applications of silicon nano-structure array include, but are not limited to, electron emitters, sensors, solar cells, rechargeable batteries, and hydrogen storage devices. With advances in nanotechnology, various techniques have been reported for synthesis and fabrication of nano-structures. However, these techniques like chemical vapor deposition and vapor liquid solid suffer from the need of very sophisticated and high cost equipment. Furthermore, the need of high operating temperature, high vacuum, and catalyst material such as gold are major challenges of these techniques. On the other hand some fabrication techniques such as top-down approaches involve complicated fabrication steps that ultimately increase the cost of the device.

Therefore, a rising impetus has been devoted to development of less complicated and low-cost fabrication techniques of silicon nano-structure.

The goal of this thesis was to introduce novel and cost-effective fabrication methods which also maintain the benefits of CMOS compatibility. Two non-lithography top-down approaches were introduced for fabrication of silicon nano-structures array with capability of controlling the structure characteristics.

The first fabrication approach consists of three steps: 1) patterning of silicon surface in TMAH using anisotropic etching technique, 2) formation of porous layer on patterned silicon surface using electrochemical anodic etching, and 3) treatment of porous silicon layer using an alkaline etching to reveal the silicon nano-structure array.

The second fabrication approach consisted of two steps, namely: Anisotropic etching followed by electrochemical etching. The main idea behind this approach was that unlike

the first approach the electrochemical etching is performed in transition regime not porous silicon formation regime.

These techniques allowed for the controlling the characteristics and morphology of silicon nano-structures.

Completely different morphologies of nanostructures were achieved as a result of transforming the electrochemical process from porous silicon formation to transition regime.

A study on effect of type of dopant, p- and n-type, on over-mentioned fabrication methods was also investigated.

To my Family

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List of Acronyms

NH4OH	Ammonium hydroxide
CVD	Chemical vapor deposition
CrO_3	Chromium trioxide
CMOS	Complementary metal–oxide–semiconductor
FE-SEM	Field Emission Scanning Electron Microscopy
F^-	Fluoride ion
HF	Hydrofluoric acid
H^+	Hydrogen
H_2	Hydrogen molecule
H_2O_2	Hydrogen peroxide
OH^-	Hydroxide
h^+	Hole carrier
IPA	Isopropyl alcohol
LPCVD	Low-pressure chemical vapor deposition
MEMS	Microelectromechanical systems
NEMS	Nanoelectromechanical systems
HNO_3	Nitric acid
PECVD	Plasma-enhanced chemical vapor deposition
$KBrO_3$	Potassium bromate
$K_2Cr_2O_7$	Potassium dichromate
KOH	Potassium hydroxide
KIO_3	Potassium iodate

RCA	Radio Corporation of America
SiH_4	Silane
Si	Silicon
SiO_2	Silicon dioxide
SiF_6	Silicon hexafluoride
Si_3N_4	Silicon nitride
NaOH	Sodium hydroxide
$NaNO_2$	Sodium nitrite
SCR	Space chrage regien
3-D	Three dimensions
TMAH	Tetramethylammonium hydroxide
UV	Ultraviolet

List of Symbols

E_a	Activation energy	[eV]
K	Boltzmann constant	[J/K]
Q	Charge	[C/cm^2]
J_{ps}	Critical current density	[Acm^{-2}]
J	Current density	[Acm^{-2}]
$c^{3/2}$	HF concentration	[wt.%]
α^{-1}	Penetration depth	[mm]
Ω	Resisttance	[Ohm]
T	Temperature	[Kelvin]

1. Introduction

A very brief history of nanotechnology is given. The motivations behind this research work and objectives of the thesis are indicated. The contents of each chapter of this thesis are also described.

1.1 A brief history of nanotechnology

"There's plenty room at the bottom." It is the talk given by Richard Feynman in 1959 at an annual meeting of American Society at Caltech. He pointed out that:

"*I don't know how to do this on a small scale in practical way, but I do know that computing machines are very large; they fill rooms. Why can't we make them very small, make them of little elements, and by little, I mean little*?"

In fact, the idea of miniaturization can be traced back to the World War II, with the drive to reduction in the size of vacuum tubes. The invention of the transistors and replacement of vacuum tubes with transistors in the 1960's began the trend toward miniaturization. Since the evolution in microelectronics, miniaturization has had a great impact in human lives. Miniaturization plays an important role in silicon electronics industries to enable continuation of the Moore's law.

The current pace of miniaturization in microelectronics devices requires new engineering and fabrication techniques to go further to sub-micron features. Recent development in nanotechnology has paved the way to miniaturize the device thousand times smaller than human hair. However, pushing the cost of fabricated devices as comparable as to conventional ones still is a major challenge.

Apart from the smallness point of view, nanotechnology plays a major role in introducing new properties into materials. The electrical, optical, physical, and mechanical properties of material change as the size of the materials shrink to the nano-scale. Furthermore One-dimensional structures, due to their large surface area and high aspect ratio, are promising candidates as fundamental building blocks for the manufacturing of various devices [1]. The potential applications of nano-structures are varied and included-but not limited to-electron emitters [2], sensors [3], solar cells [4], and rechargeable batteries [5].

Such precision engineering and/or altering of materials can be done from two major approaches:

1. The “bottom up” approach which is building of functional nano-structures starting from basic atoms and molecules
2. The “top down” approach in which a bulk material is reduced to generate a nano-scale structure.

Both techniques have been used widely towards fabrication of nano-structures such as nanowires, nanotubes, pillars, and porous layers.

Due to their many advantages, silicon nanostructures play a prominent role in nanotechnology research and applications. Silicon is the most abundant material on Earth’s crust after oxygen, which makes it a low-cost material. Moreover, the integration of silicon-based nano-devices with CMOS driving circuitry is quite feasible.

Various approaches have been introduced and employed for the fabrication of silicon nanowires such as chemical vapour deposition [6], thermal evaporation [7], and electro deposition techniques [8]. These approaches however require equipment, which operate in high vacuum and/or at high temperatures. Additionally, poisonous gases such as SiH_4, used as a silicon source, or high-cost catalysts such as gold and silver, are needed. Also, the presence of catalysts material in fabrication process results in contamination of silicon nanowires. This contamination can increase the impurity level in the band gap of semiconductor. Therefore, a rising impetus has been devoted to development of alternative techniques for fabrication of silicon nano-structures.

1.2 Motivation

The low-cost, sustainable and accessible sources of energy, the more sensitive and accurate diagnosis, the early detection of disease and treatment, a peaceful and secure environment are the growing necessities of modern societies. Tremendous researches are going on in each of these areas to meet the needs of socialites. Among them nanotechnology and nano-science have been contributing significantly in these matters.

Fabrication of silicon nano-structures attracted considerable interest. The trace of silicon nanowires as powerful nanotechnological building blocks can be found in almost all research areas, from energy to security. Silicon can offer a wide range of applications by fashioning the bulk silicon material into silicon nano-structures. A combination of factors including large surface area and surface-dependent physical and chemical properties has made silicon nano-structure a key element for many nano-scaled devices.

From the standpoint of energy, silicon nanowires have exhibited remarkable antireflection ability owing to the large surface area, which make these structures a suitable candidate in solar cell applications [4]. Also, the conversion of waste heat to electricity using silicon nanowires has been reported by research group at University of California Berkeley [9]. They have engineered the surface of the silicon nanowire and introduced a set of defects on the surface in order to make the surface of the wires rough with the aim to slow down the flow of phonons (the acoustic vibrations in the crystal lattice of a material that carry heat).

Silicon nanowires have proven their characteristics of exemplary in diagnostic, cancer therapy and drug delivery applications. An ultra-high drug-loading capacity of 20800 mgg^{-1} is reported for silicon nano-structures [10].

The silicon nanowires are capable of carrying the drug molecules on the surface by physisorption mechanism and then release the molecules into target cells [11]. The gold decorated silicon nanowires have also shown to be an effective structure for sufficient destruction of cancer cells [12].

When it comes to safety and security, dozens of publications have been recorded on suitability of silicon nanowire. Reliable hydrogen gas detection has been reported by researchers at University of Berkeley by adoption of silicon nanowires in field effect transistor [13]. They have designed and fabricated an electronic nose based on silicon nanowire field-effect-transistor with palladium contacts (source and drain). Palladium-decorated silicon nanowires has also shown a reliable sensitivity upon exposure to 5% H2 [14].

Silicon nanowires have shown to be more effective than trained dogs at sniffing out explosives materials including TNT, PETN, and RDX. Scientists at Naval research laboratory have engineered an electronic nose for detection of explosive materials using an array of vertical silicon nanowires [15]. The ultra-sensitivity of parts-per-billion and even parts-per-trillion are achievable using this sensor.

Introducing techniques that eliminate or mitigate many of the problems associated with current fabrication methods such as need of high temperature and/or high vacuum process, contamination of final product, the noisy wire to wire junctions and incompatibility with current CMOS technology is very demanding.

The aim of this work is to suggest novel techniques for fabrication of large arrays of vertical silicon nano-structures etched from single silicon wafer with one eye on

overcoming the above-mentioned challenges and one eye on keeping the fabrication cost low.

Over the past few decades, electrochemical etching of silicon in an HF environment has significantly contributed to the fabrication of porous silicon layers [16-18]. Electrochemical dissolution of silicon in diluted HF has proven to be a very powerful and versatile technique that can be employed for the fabrication of more complex nano/micro-structures (e.g., spiral arrays, micro-tube arrays, trenches, and pillars) [19-21].

Electrochemical techniques profit from salient advantages, which include low-cost and ease of application. Moreover, electrochemical methods, most of the time, do not require high temperature. These features make the electrochemical technique an attractive approach to implement lab-scale technology at an industrial scale.

Fabrication of silicon nanowires using an electrochemical technique has been reported by several groups [22-26]. Electrochemical etching process results in formation of macro-pore arrays that can be used as a building-block for synthesis of 3-D nano-structure array.

One major problem for applying of electrochemical process for synthesis of 3-D structure is random formation of porous silicon layer. The root of problem comes from the fact that the surface defects such as sharp spots at the surface act as seeding points at electrochemical etching process. As a result, porous silicon layer randomly is created on a surface of a polish silicon wafer.

Taking advantages of surface defect as initiation points of electrochemical process, researchers purposely created specific defect sites on the silicon surface. These specific defect sites consist of inverted pyramid which are fabricated on the desired positions. The conventional approach to create macro-pore array on silicon wafers starts with deposition

of a thin layer (140-300 nm) of Si_3N_4 on front side of the silicon wafer using plasma-enhanced chemical vapor deposition (PECVD) [27] or low-pressure chemical vapor deposition (LPCVD) [28]. The silicon surface was then patterned using lithography. The patterned silicon wafer was dipped in diluted KOH solution in order to form the inverted-pyramid-shaped pits. These pits predetermine the initiation sites for pores formation and as a result prevent the random formation of porous silicon layer.

However, due to use of lithography, the fabrication process time increases. Aside from the time, itself, that adds to the ultimate manufacturing cost, the in use equipment, (lithography, mask, and CVD) and materials, (photoresist, and developer) additionally increases the fabrication cost. Also, photolithography techniques cannot be easily employed for a surface with a large area.

Most obviously, engineering solutions must always be designed with economic considerations in mind, low-cost technologies often remain preferred over more expensive technologies.

Seeking ways to overcome economic barriers that block the way to transport novel approaches from lab-scale into industrial-scales remain an ongoing research.

1.3 Objectives

This study is intended to propose two novel and cost-effective top-down approaches towards fabrication of 3-D silicon nano-structure array on low p-type silicon wafer. These methods of synthesizing silicon nano-structure arrays are appealing since they are catalyst-free techniques and also are compatible with current CMOS process. Furthermore, the process is non-lithographic and can lead to a low-cost route for fabricating micro/nanoelectronic devices.

The first fabrication approach consists of a three consecutive etching steps. First, the silicon surface is textured using anisotropic wet etching technique. Then the textured surface is served as working electrode for electrochemical anodic etching to create a porous silicon layer. Finally the porous silicon layer is partially etched in an alkaline solution to dissolve the interconnected walls and to reveal the desired nano-structure array.

The second proposed fabrication approach consists of only two fabrication steps. The silicon surface is textured using wet etching, followed by electrochemical anodic etching. According to this method, the latter etching process is conducted in the transition regime (between porous formation and electro-polishing regime), with the aim of elimination of the third fabrication step, fine etching, of the first proposed technique and also manipulation of surface morphology of the silicon nano-structure.

The detailed studies on growth mechanism of the nanowires helped to develop methods for controlling the array density and nano-structure size characteristics. The effectiveness of proposed approaches on n-type silicon wafer also is investigated.

1.4 Overview of this thesis

In this thesis the applicability of wet/electrochemical etching of silicon as a proper tool for fabricating 3-D micro/nano structures is studied. The electrochemical etching process is very suitable for the fabrication of porous silicon array with very smooth walls. The morphology of these pores can be controlled and tailored by etching parameters. This gives a great freedom in the design of various structures.

In chapter 2 an overview of the wet/electro chemical etching of silicon is given. Etching mechanism and some specific properties of the electrochemical process are discussed.

The formation of porous silicon, which is used as building blocks for formation of 3-D structures, is also described.

Chapter 3 a new approach for formation of 3-D nano-structures is presented. This technique gives a great freedom in controlling the characteristics of the structure. The main techniques used towards achievement of nano-strcuture are anisotropic wet chemical etching and electrochemical etching. The nano-structure array was achieved as a result of three consecutive etching steps. An interesting nano-layered structure obtained owing to the unique anisotropic behaviour of last etching step.

Chapter 4 describes the second novel approach for formation of 3-D structures that requires only two etching steps. Optimum conditions of the electrochemical etching of silicon for formation of nano-structure array were determined by etching p-type silicon substrates at various HF concentrations. Purposely, electrochemical etching conditions are optimized in such a way that the silicon etching reaction follows the tetravalent path, as opposed to the first approach. Nano-structures with smooth walls were achieved in contrast to the first approach.

In chapter 5 the effectiveness of first approach on low-doped n-type silicon is described. The photo-electrochemical etching technique is presented. This method involves the illumination of pattern on the surface of an n-type silicon sample, using a halogen lamp. The photo-electrochemical etching conditions are optimized for formation of even and uniform pore array with smooth walls. An array of Eiffel-tower-shape silicon nano-structures was synthesized.

In chapter 6 conclusions are drawn and suggestions for future research are given.

2. Overview of silicon chemical/ electrochemical etching

This chapter is divided into two main sections: wet-chemical etching of silicon and electrochemical etching of silicon. These are the two well-known processes in semiconductor fabrication process that are adopted in this work for fabrication and development of vertical nano-structure arrays.

2.1 The Etching of silicon

Etching in the context of this work refers to the dissolution process that uniformly or preferentially removes material from silicon immersed in a solution. Since its first introduction in 1950s [29-31] etching of silicon, has been widely explored due to its useful applications in fabrication of electronic devices. Numerous investigations have been carried out to develop and characterize the etching systems for micromachining applications.

Two major types of etching can be identified: isotropic and anisotropic. In isotropic etching, the etching rate is same for all crystal directions, while the etching rate depends on crystal orientation for anisotropic etching. Figure 2.1 illustrates a schematic of cross-section of a cavity that was etched in isotropic and anisotropic etchants.

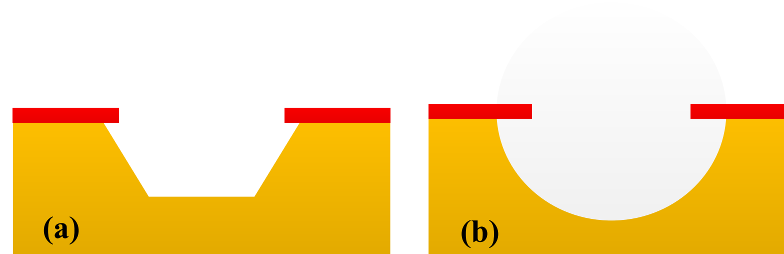


Figure 2.1 Schematic representation of a cross-section of a silicon etched (a) anisotropically (b) isotropically

The isotropic etching of silicon is known by the works of H. Robbine and B. Schwartz [29-31]on chemical etching of silicon and works of A. Uhlir's on electrochemical etching of silicon in 1950s [32]. The primer works on anisotropic etching of silicon have been done by Bell Telephone Laboratories in mid-1960s.

2.2 The anisotropic wet-chemical dissolution of silicon

About 30% of the total number of process steps for manufacturing an integrated circuit involves wet etching process. Alkaline solutions are well-known etchants for chemical wet etching of silicon. Alkaline etchants are aqueous solutions of inorganic including, potassium hydroxide (KOH) [33], sodium hydroxide (NaOH) [34], ammonium hydroxide(NH_4OH) [35] or organic solutions including hydrazine [36] and tetramethylammonium hydroxide (TMAH) compounds [37]. All these etchants show the dependency of etch rate to crystal orientation, which is the basis for anisotropic etching behaviour. The etch rate for the (111) planes of the silicon is smaller by about two orders of magnitude than the etch rate of any other plane. The etch rate ratio between other planes like (100) and (110) depends on etchant concentration and temperature, but does not usually exceed a factor of two [38]. Regardless of the common anisotropic behaviour that these etchants share, they possess some different properties that may be considered in their selection. KOH has been widely used in studies involving anisotropic etching of crystalline silicon. Despite a very good anisotropic behaviour for some orientations, 110 >100> 111, it is very corrosive etchants, and it shows a low selectivity with respect to the masking layer. Another problem that arises from KOH is the presence of metal contamination of KOH etchant solution which is a major issue in CMOS technology compatibility [39].

Ammonium hydroxide (NH_4OH) is one hydroxide which is free of alkali metal, but it is really ammonia which is dissolved into water [40]. Ammonia will rapidly evaporate from solution at higher temperature, 90°C that is a requirement for etching process.

Hydrazine is very dangerous because of being highly toxic and instable that makes handling very difficult [41]. TMAH etchant has been developed more recently for

anisotropic etching of silicon that fulfils CMOS compatibility requirement [42]. Moreover, it is relatively safe to use and presents no special disposal issues [37]. It shows an excellent selectivity to masking layer. It has a very low oxide etch rate, SiO_2 and does not attack aluminum if the solution contains a certain amount of silicates. Also, it does not decompose below 130 ºC [35].

Etching of silicon in alkaline etchants is a thermally activated process and the etching rate increase with temperature. Silicon dissolves chemically in alkaline etchant by reacting with hydroxide (OH^-) ions at elevated temperature [43]. Hydroxide ions play an important role in etching process [44]. The etching process occurs under evolution of hydrogen with a ratio of two molecules H_2 per dissolved Si atom [45].

The morphology of the etched surface depends on various parameters such as solution concentration, solution composition, temperature, orientation and added surfactants to the solution. The morphologies of the silicon surface can be varied depending on silicon crystal orientations. Formation of pyramid-shaped structure on 100 surface, triangular pits on 111 surface [46], and zigzag structures on 110 surface [47] have been reported (See Figure 2.2).

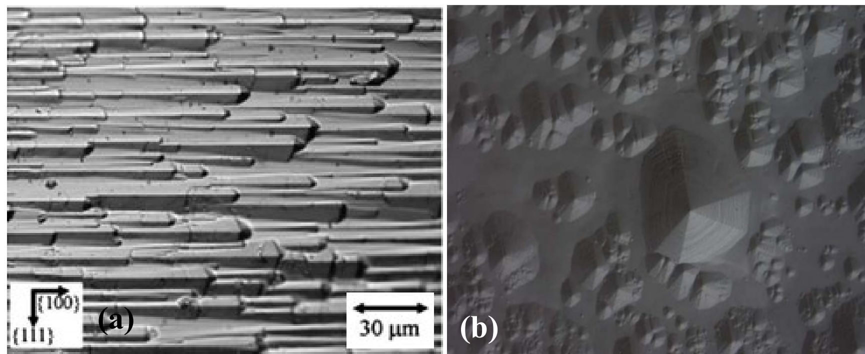


Figure 2.2 (a) Zigzag pattern on Si (110) [47]. (b) Formation of deep pits on (111) due to dislocations. Experimental image from Sato Laboratory, Nagoya University [48]

The morphology of alkaline-etched (100) silicon surfaces varies from rough surfaces that exhibit pyramid-shaped structures [49] to smooth surfaces [50].

The surface morphology of (100) silicon planes in alkaline solutions depends strongly on etchant concentration. High OH^{-} concentrations (e.g. > 40% for KOH) produce smooth, while the tendency of formation of pyramids increases at low OH^{-} concentrations. Although, surface smoothness is an important factor in the performance and reliability of electronic devices, but rough surfaces have wide applications, for instance, they have been used for decades as antireflective surface to reduce the reflectivity of solar cells [51].

However, there is no consensus among researchers regarding the origin of this surface morphology. The formation of the pyramids has been attributed with the sticking of hydrogen bubbles to the surface [52] which are elevated during etching process. Palik et al. has proposed that the hydrogen bubbles act like a mask layer and result in cessation of etching of the underneath surface (See Figure 2.3).

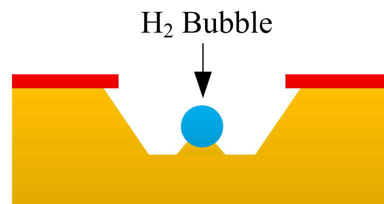


Figure 2.3 Natural etching mask caused by hydrogen bubbles [53].

It has been reported by Schnakenberg and et al. that formation of pyramids can be suppressed by addition of certain amounts of hydrogen peroxide into etchant solution [54]. They suggested that the formation of smooth surface is due to the fact that no hydrogen bubbles were evolved during the etching process.

It has been reported that detachment of hydrogen bubbles can be improved by adding of surfactants such as isopropyl alcohol (IPA) to the etchant solution [43, 55]. Also an ultrasonic source can be used to remove the hydrogen bubbles from the surface [56]. Adding of silicon powder, and using a metal grid for trapping the hydrogen bubbles [57] are other substantial procedures have been reported in order to get rid of sticking of hydrogen bubbles and improve the etching process.

2.3 Electrochemical anodic dissolution

Silicon can be dissolved chemically or electrochemically in presence of acidic environment. Acidic solution was used for the first time by H. Robbins and B. Schwartz to chemically etch the silicon crystal. They have used a mixture of HF, HNO_3 and H_2O for etching of silicon. Acidic etchants add another degree of freedom to the design of micromechanical structures, since silicon crystal is etched isotropically in acidic environments. Silicon etching rate is too low in acidic solution at room temperature (~0.1nm min^{-1}) [58] due to the low concentration of the OH^- ions in acidic solutions.

The dissolution of silicon occurs in two steps involving, oxidation and dissolution. The oxidation reaction can be occurred through two distinct methods: first, through adding some oxidant to the etchant solution. A considerable enhancement of etching rate was reported in the presence of oxidizing agents such as H_2O_2 [59], HNO_3 [60], $NaNO_2$, $KBrO_3$, $K_2Cr_2O_7$ [61], KIO_3 or CrO_3 [62].

Second, through supplying hole carriers into silicon surface. The former process is called electro-less etching and the latter is known as anodic electrochemical etching.

In order to conduct an electrochemical etching, two electrodes are required. One supplies the electrons into the solution, cathode, and the other removes the electron from the

solution, anode. The term anodic electrochemical etching comes from the fact that silicon material is the anodic electrode where the oxidation reaction takes place. With no applied bias, the rate of hole transport across the silicon-electrolyte interface is low, while an applied bias results in accumulation of charge carriers at the interface, (see Figure 2.4)

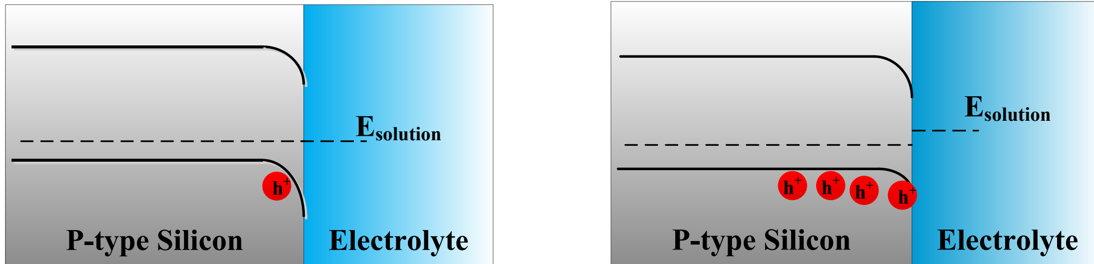


Figure 2.4 Charge transport processes at the semiconductor/electrolyte interface for a p - type silicon. The increase in hole current across the interface under forward bias (silicon positive relative to the Pt counter - electrode in solution) is depicted [63].

The role of the valence band hole carriers in controlling the anodic oxidation of the silicon ties the etching process to the hole carriers supply sources and also their transport mechanism toward the silicon/electrolyte interface.

For p-type silicon these hole carriers are present in material, while n-type silicon requires an external hole supply. Usually, the required hole carriers are provided through illumination of the n-type silicon which results in generation of electron-hole carriers [64]. This approach is known as photo-electrochemical etching.

Hole injection from a pn junction has been reported as an alternative approach for electrochemical etching of n-type silicon [65]. However, the extension of this approach to n-type low-doped silicon has not been successful.

2.4 IV Characteristics

The specific nature of the electrochemical etched surface can be modified and tailored from polished surface to porous surface through a precision-control of parameters involved in electrochemical etching system. Figure 2.5 shows a typical IV characteristic of electrochemical etching of silicon. The first peak observed in this curve is commonly termed J_{ps} and correspond to the critical current density. The involved parameters in electrochemical etching determine the amount of J_{ps} on the etching system. It is this J_{ps} that delimits three distinct regimes in IV plot: Porous silicon formation regime, $J<J_{ps}$, transition regime $J \sim J_{ps}$, and polishing regime $J>J_{ps}$ [64, 66, 67].

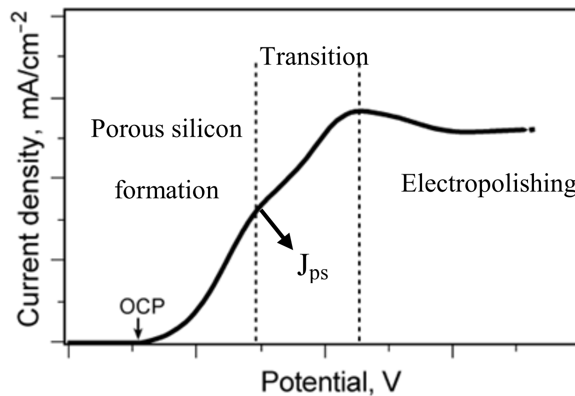


Figure 2.5 A typical IV curve of silicon wafer in HF solution, showing the regimes of porous silicon formation, transition and electropolishing [67].

2.5 Etching mechanism

The first proposed models for electrochemical etching of silicon in HF were based on fluoride-terminated silicon surface [68, 69]. However, the in-situ infrared study of chemistry of silicon surface using IR spectroscopy revealed that the silicon surface is terminated with hydrogen atoms [70]. It is well-known that the H-terminated surface is chemically stable and shows an extraordinarily low reactivity [71].There is an unanimous agreement between

researches that holes are responsible for initial oxidation steps of anodiztion and weakening of the Si-Si bonds [72, 73]. It has been reported that the sticking coefficient of F^- ions increases by 11 orders of magnitude in the presence of the holes [74]. As a result the Hydrogen abstraction from silicon is enhanced by Fluoride ions [75].

In general, anodic etching of silicon in HF environments involves two competing reaction paths: 1) direct dissolution of silicon and 2) indirect dissolution of silicon through silicon oxide formation. The first direction is known as divalent electrochemical dissolution and the second path is known as tetravalent electrochemical dissolution [63]. Figure 2.6 shows a reaction mechanism in HF solution, which is proposed by V. Lehmann and H. Foll [76]. Path (1) is corresponding with potential lower than the potential of peak current at IV curve which results in porous layer formation and path (2) is corresponding with potentials higher than the potential of peak current which results in electro-polishing of the surface.

The divalent dissolution starts with approaching of hole at the valence band of the silicon atom, which activates the absorption of fluoride ions. The absorption of fluoride ions is accompanied by injection of an electron into electrolyte. The presence of Si-F bond enhances the polarization and causes the detachment of another hydrogen atom and absorption of second fluoride ion. A hydrogen molecule is elevated as a result of these reactions. The Si-Si back-bond is destabilized as a result of strong polarization and is attacked by fluoride ions. This reaction results in production of tetrafluoride molecules, SiF_4, which has a gaseous state, but it reacts with HF to form a highly stable SiF_6.

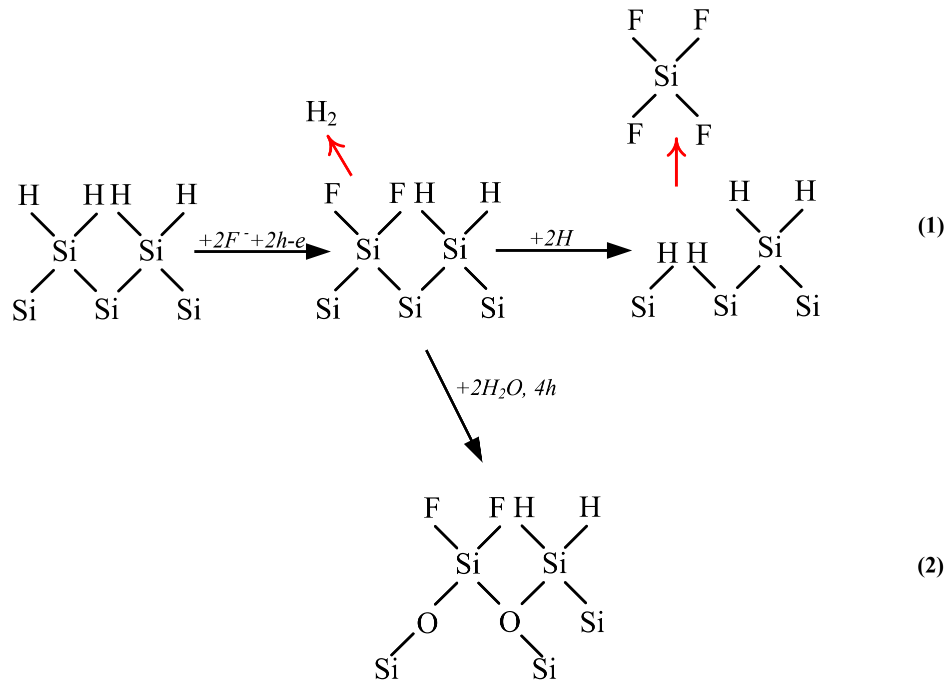
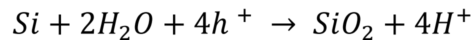
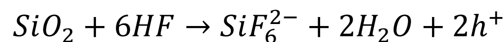


Figure 2.6 Possible reaction paths for the electrochemical reaction in HF solution.

The tetravalent dissolution of silicon on HF solution can be divided in two parts: formation of anodic oxide followed by dissolution of the oxide in HF. The overall reaction of the dissolution of Si in the polishing regime is:



$$Si + 2H_2O + 4h^+ \rightarrow SiO_2 + 4H^+$$



$$SiO_2 + 6HF \rightarrow SiF_6^{2-} + 2H_2O + 2h^+$$

As the reactions show, no hydrogen is elevated during the tetravalent corrosion of silicon where electro-polishing of silicon surface take places.

The divalent path is pre-dominated at lower potential, when the rate of holes transforming to the surface is higher than fluoride diffusion rate and the tetravalent path is taken at higher potential which is responsible for electro-polishing of the surface. The high current density or the low concentration of HF can lead to this path.

2.6 Porous silicon formation

Isotropic etching of silicon using electrochemical etching already started in 1950s. The first paper of electropolishing of silicon by anodic electrochemical etching was reported in 1958 [77]. The electrochemical formation of porous silicon was reported for the first time by the A. Uhlir at Bell Laboratories in 1950s, while they were working on an electropolishing process on silicon. It was observed that depending on etching parameters, a brownish layer can form on the silicon surface. The characterization of this brown layer revealed that it consists of randomly distributed and interconnected pores which today is known as porous silicon. The porous silicon layers are classified in three categories by IUPAC (The International Union of Pure and Applied Chemistry) depending on their pore size: micropore (< 2 nm), mesopore (2-50 nm) and macropore (> 50 nm) [78]. Experimental parameters that are involved in etching process, determine the specific morphology and characteristics of a porous layer. Experimental parameters are namely: electrolyte composition, HF concentration, etching anodic current density, the doping type, orientation and resistivity of the substrate, temperature of electrolyte, the light intensity -determining the number of generated holes in the bulk-the light wavelength and the direction of illumination, back-side or front-side illumination.

The critical polishing current, J_{ps}, is directly proportional to HF concentration, resistivity of substrate and also temperature. Critical polishing current increases with increasing each one of these parameters. The relation between J_{ps} and HF concentration and temperature is given by V. Lehmann [64],

$$J_{ps} = Cc^{3/2} \times \exp(-E_a/KT)$$

where c is the HF concentration (in wt%), T the temperature (in Kelvin), K $=1.38 \times 10^{-23}$ J/K, C = 3300 A/cm^2, and E_a = 0.345 eV.

Selection of an adequate illumination source is critical for n-type silicon, since it is responsible for generation of hole carriers. The light wavelength, which corresponds to energy of the photons, is important for selection of a light source. The photons of wavelength below 1100 nm have sufficient energy; excess the silicon band gap energy of 1.1 eV, for generation of electron-hole pairs. No photon absorption occurs in bulk silicon at wavelength longer than 1100 nm. The white light sources such as halogen lamps have a broad spectrum between 380- 750 nm. Also they are very useful for uniform illumination of the whole surface. Laser can be used for area-selective illumination of the surface.

Illumination can be conducted from both side of the silicon, either the surface that is exposed to electrolyte, front-side, or from the surface that provides ohmic-contact, back-side. Figure 2.7 illustrates the depth where the hole-electron pairs are generated and the distance hole carriers have to travel to reach the silicon/electrolyte interface, where they are consumed and silicon corrosion occurs.

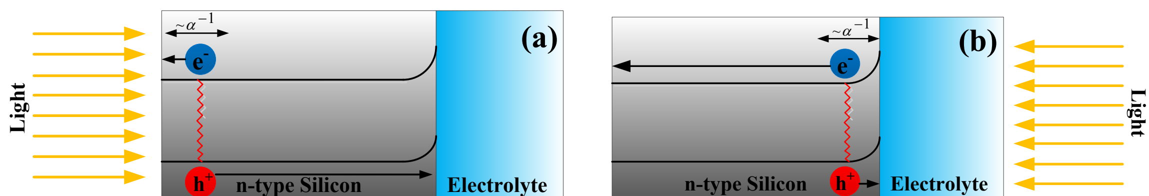


Figure 2.7 Diagram illustrates the depth where the hole-electron pairs are generated and the distance hole carriers have to travel to reach the silicon/electrolyte interface. (a) back-side illumination, (b) front-side illumination.

As Figure 2.7(a) shows, under back-side illumination the generated hole carriers have to diffuse the whole thickness of the silicon wafer. A large fraction of generated carriers

will be lost due to the bulk recombination, hence, hole diffusion length delimits the number of hole carriers reach toward the interface. It is why the thickness of silicon wafer plays a key role in formation of n-type silicon wafers that are illuminated from the back-side [79].

2.6.1 Area-selective etching of porous silicon

A numerous studies have been done on electrochemical etching of polished/flat silicon surface. It has been observed that the silicon surface is covered with pores that are randomly distributed on the surface, for the case that electrochemical etching was conducted on polished silicon wafer. Any roughness or defects on the flat silicon surface can act as a seeding point for pore formations.

The porous layer also can be formed on the desired area of the surface. Area-selective etching can be done using different approaches. Selective chemical etching of doped layers has been used since the early days of device fabrication.

As it discussed earlier in section 2.6 the critical anodic current is proportional to properties of the substrate such as type of doping. Therefore, the areas which are doped differently with respect to the host material show different IV characteristics. The sharp selectivity of HF anodic etching between p-Si and n-Si has been used for micromachining of silicon [80].

For *n*-type silicon, a selective-etching can be performed using localized light source such as lasers. Lithography patterning of the desired surface is another approach for area-selective etching. In this scenario a mask layer is used to preserve the arbitraries areas against etching.

However, in all above cases still the pores are randomly formed and distributed on the silicon surface. In order to stop the random distribution of the pores, the initiation points can be arbitrary chosen by patterning the silicon surface. Photolithography technique followed by KOH etching is a very common and well-known approach for pre-patterning the silicon surface. This approach has been used by several groups to create different geometries such as inverted pyramid, and trapezoidal [81] pits on the silicon in order to pre-determine the location of pore formations. It has been reported that the size and shape of these pits affect the pore formations. Figure 2.8 shows the cross-section view of some typical pits etched using KOH and their corresponding schematics after electrochemical etching.

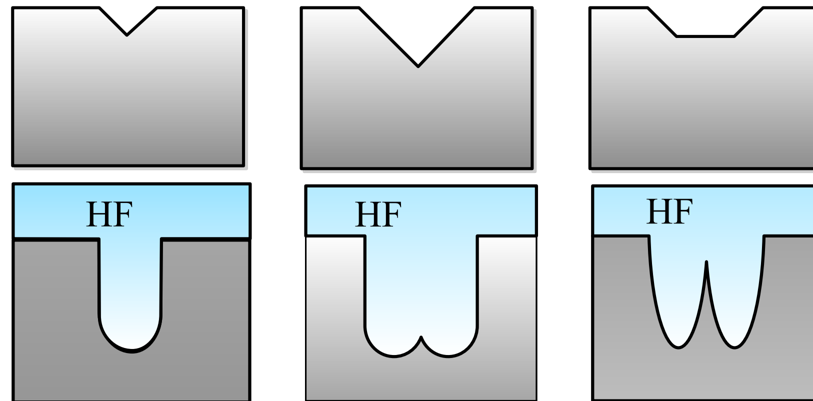


Figure 2.8 Schematic illustrates the effect of shape and dimension of the tips on electrochemical etching of silicon [19].

2.6.2 Application of porous silicon layer

Since its first report by A. Uhlir in 1950s, the porous silicon has been intensely investigated due to its unique and rich morphology. Ideas on the applications of PS in microelectronics, optoelectronics, solar cells, and sensors have continuously been generated since its first discovery.

The first report by L. Canham in 1990 that efficient visible light can be emitted from high porosity structures opened the way for further investigations on fabrication of electroluminescent solid-state devices [22].

The large internal surface area of porous silicon layer makes them promising candidate in fabrication of chemical sensors such as biosensors [82] and gas sensors [83]. Also it can be used as an excellent light-trapping site in solar cell devices [84]. Porous silicon also has been widely used in micromachining process as a sacrificial layer [85]. Different features make them suitable candidate as sacrificial layer: the high etch rate compared to bulk silicon, and also it can be formed selectively in favoured area. Various devices such as cantilevers, bridges [86], and flow channels have been fabricated using porous silicon as sacrificial layer. In the above-mentioned cases the porous silicon layer is etched completely in alkaline environment such as KOH, and NaOH.

Porous silicon layer also has been used as building blocks for formation of free-standing pillars. In contrast to total removal, porous silicon structures are partially preserved and formed the pillars. The micro-pores that are randomly formed on silicon surface are used mainly in sacrificial layer applications while the pre-patterned macro-pore arrays are used for fabrication of pillars.

Different post processing techniques have been applied on the porous layer in order to modify the pores structure and fabricate different micro/nanostructure. The widening of the pore diameter and reforming it to square shaped pores using KOH, and TAMH solutions has been reported by V. Lehmann [87].

The first report on fabrication of silicon nanowire using electrochemical etching process was proposed in 1990s by L. Canham [22]. This proposed approach consists of two steps:

randomly electrochemical growth of pores and subsequent enlarging of the pores with chemical etching. L. Canham has claimed that, the porosities greater than 80% are prerequisite for formation of nanowires. In this approach, nanowires are randomly formed wherever that the neighboring pores meet/overlap each other. However, this fabrication approach is not very reliable since obtaining the essential condition (interconnected walls of the neighboring pores should meet each other) is not feasible for randomly grown pores. Figure 2.9 shows a scheme of the idealized plan view for fabrication of nano-structure array from randomly distributed pores.

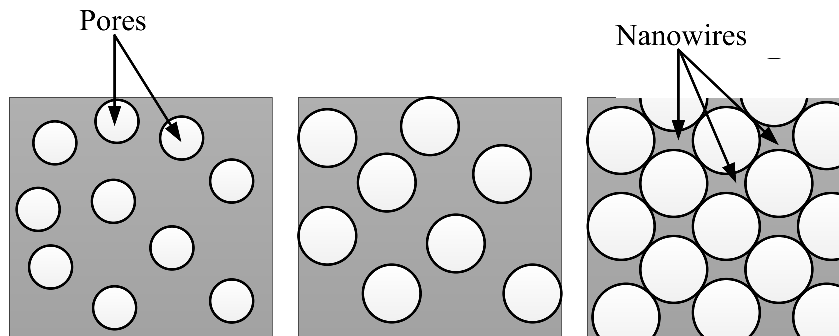


Figure 2.9 Idealized plan view of porous silicon layer with different porosities [22]

An adapted approach of L. Canham technique has been used by several groups for formation of silicon nanowires. The main idea behind this revised approach is that the locations of pores formation are pre-determined in order to avoid the random distribution of the pores.

This approach involves different fabrication steps: patterning of the silicon surface by lithography and then etching of the silicon surface using KOH to create the inverted pyramid as a seeding point for pore initiation and therefore, avoiding the random

formation of the pores. Finally, the process followed by a post processing to enlarge the pores that ultimately results in revealing of the desired nanowire structure.

A combination of thermal oxidation and wet etching post-processing technique has been employed by H.W. Lau, et al. [23, 88] to widen the pores and eventually fabricate the free-standing pillar array. In this approach a SiO_2 layer has been grown on the porous layer, followed by etching of the SiO_2 in HF solution. This process should be repeated until the walls oxidized and completely removed in diluted HF solution. Disadvantages with this process are the need of very high temperature (e.g. 1147 ºC) and also the fabrication process is time consuming (Oxidation and oxide removal should be done repeatedly to remove the walls). Wet-chemical etching using KOH is an alternative process for pores enlargement and formation of free-standing pillars [24].

In all above-mentioned approaches where the inverted pyramids are used as seeding points, the rod is formed in the area where the four neighbouring pores meet each other. In other word, the relation between the number of pores and number of resulting rods can be expressed as: $N = (\frac{n}{2}) - 1$. Where N represents the number of rods and n, is the number of pores. This conclusion shows its importance in large scales where the density of rods, number of rods in specific area, matters such as field emission applications.

Aside from the loss of surface, these fabrication methods are suffering from the need of expensive and sophisticated equipment and materials. Furthermore, added steps to the processing procedure will eventually increase the ultimate cost of the manufactured device.

New and reliable techniques, where there is no need to expensive equipment and materials and also possess lesser processing steps are in demand in micro/nanoelectronics industries.

3. Fabrication of vertical nano-structure array on silicon wafer: Electrochemical etching at porous formation regime

In this chapter, a new multi-stage technique for the fabrication of arrays of silicon nano-structures is introduced; the growth mechanism of the developed nano-structures is investigated. A combination etching methods including anisotropic-wet-chemical etching and electrochemical etching are used for formation of nano-structure array. In this technique, surface of silicon wafers were textured using anisotropic etching method to generate pyramid structures. The textured surfaces were then etched by electrochemical anodic etching. To develop the nano-structures, at the final fabrication stage, the interconnected walls of porous structure have been etched using NaOH. The effect of anodic electrochemical parameters such as current density and etching time on the fabrication of the silicon nano-structure were investigated.

3.1 Introduction

Electrochemical etching of silicon in HF solution has attracted a great attention for the fabrication of various micro-structures such as porous silicon [66], trenches [21], and pillars [25]. Recently, fabrication of one-dimensional n-type silicon nanowires from porous silicon has been developed using photo-assisted electrochemical etching [19]. This fabrication method uses oxidation and/or wet etching as post-processing techniques leading to the creation of pillars and nanowires.

In order to pre-determine the location of the fabricated silicon nanowires, in the conventional method, the silicon surface is first patterned using lithography technique followed by wet etching [20, 24]. This technique leads to the creation of inverted pyramids on the silicon surface followed by the formation of porous silicon starting at the pit of these inverted pyramids.

In this work, a new non-lithographical method was used for the fabrication of silicon nano-structure arrays. In this approach, the pyramid shape seeding points were first created on the surface of the silicon. Each of these pyramids will become the tip of the silicon nano-structures created in the subsequent fabrication stages. However, the anisotropic etching creates randomly distributed pyramids on silicon surface; the position of the created nano-structures in the subsequent fabrication stages is pre-determined by the location of these pyramids. This method of synthesizing silicon nano-structure arrays is appealing because the process is non-lithographic and can lead to a low-cost route for fabricating micro/nanoelectronic devices.

The detailed studies on growth mechanism of the nanowires helped develop methods to control the array density and nano-structure size characteristics. The impact of anodic

electrochemical conditions and pyramid surface coverage on the fabrication of silicon nano-structure array are investigated.

3.2 Experimental procedure and setup

Silicon wafers with (100) orientation (10-20 Ω-cm) were purchased from Silicon Inc. and were used for all experiments. All experiments were carried out on p-type silicon, so that, due to the existence of hole majority carriers, no illumination of the sample is required. All samples were cleaned prior to experiments using the Radio Corporation of America (RCA) process [89]. 25 wt.% TetraMethylAmmoniumHydroxide (TMAH) was purchased from Sachem Inc. and diluted with DI water to reach the desired 1.5 wt.% concentration used in all experiments. 99% isopropyl alcohol (IPA) was purchased from VWR International and added to the etching solution to obtain 1.5 wt.% and 6 wt.% weight concentrations. 99.5% ethanol, and 97+% NaOH were purchased from Sigma-Aldrich. 48.8% HF was purchased from ACP Chemicals Inc. Canada. The anodic electrochemical etching was performed using Allied Research galvanostat potentiometer. The developed nano-structures were characterized using Hitachi S-4700 field emission scanning electron microscopy (FE-SEM). The population density of structures and surface coverage measurements were all obtained by performing image analysis of the SEM photos using ImageJ image processing program developed by the US National Institute of the Health.

This novel approach requires three stages of fabrication to create the desired nano-structure array. The three stages are as follows:

1. Anisotropic wet etching to create textured silicon surface

2. Anodic electrochemical etching of the textured silicon to create a porous layer
3. Fine-etching of porous silicon layer to achieve the desired nano-structure array

Sketches of experimental setups for anisotropic etching and electrochemical etching, as used in this work, are shown in Figure 3.1 and 3.2 respectively.

Figure 3.1 illustrates the schematic view of the apparatus used for the anisotropic etching of silicon to form the pyramid-shaped structures. The glass beaker filled with etchant solution, TMAH and IPA, was used for etching the silicon samples. Teflon basket was used to hold the silicon samples inside the glass beaker. The beaker was placed on a hot plate and heated at constant temperature at 90 °C. This operating temperature is chosen since it is below the boiling point of the etchant solution. The experiments were carried out in a closed system consisting of a beaker with a flux cap cooled through an internal circulation of cold, 5-6 ºC, running water resulting in the condensation and return of any evaporated component back to the solution. These precautions were taken in to account to assure that the concentration of all volatile components in the solution remain constant for the duration of etching.

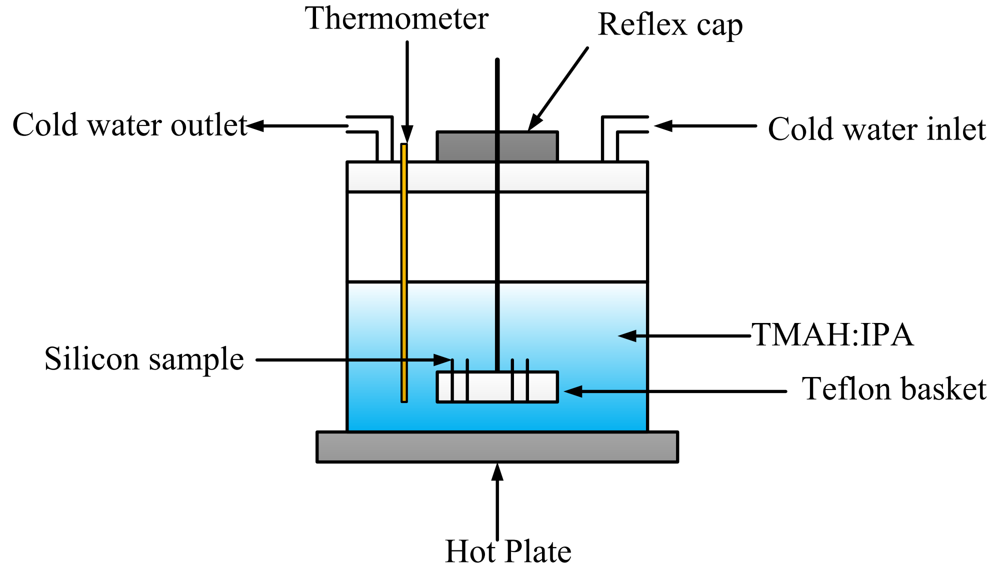


Figure 3.1 Schematic view of wet chemical anisotropic etching apparatus.

Figure 3.2 illustrates a two electrodes electrochemical etching cell, as used in this work. The cell is made of Teflon, which is resistant to HF. A Platinum electrode is mounted as counter electrode and silicon wafer is served as working electrode.

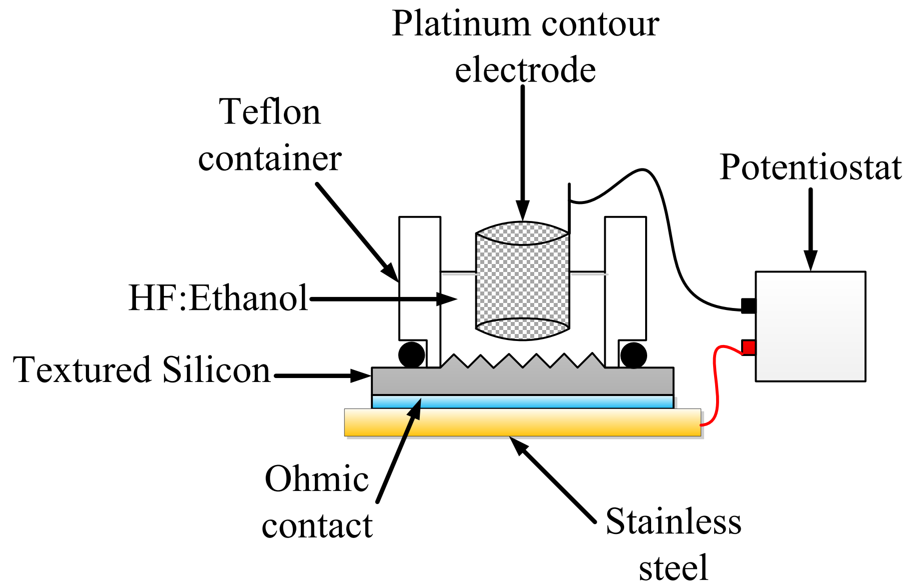


Figure 3.2 Schematic of a two - electrode electrochemical cell used to make porous silicon. Silicon is the working electrode. The counter - electrode is platinum.

3.3 The fabrication process flow

3.3.1 Fabrication of the pyramids (1st stage)

Surface of a 1 cm^2 samples of silicon wafer were textured using anisotropic etching process in 1.5 wt.% TMAH for 30 minutes. Pyramids with various sizes were developed on the surfaces of the samples. During the process IPA was added to TMAH solution in order to remove the hydrogen bubbles from surface of the sample faster to facilitate the etching process. It has been reported that the concentration of the added IPA affects the size and surface coverage of the pyramids [90]. In this stage, samples etched in TMAH with added various IPA concentrations (0, 1.5, & 6 wt.%) are used. The samples were used to study the effect of pyramids concentrations on the developed final nano-structures.

3.3.2 Creation of porous silicon (2nd stage)

An anodic electrochemical etching was performed on the textured silicon surface to create a layer of porous silicon. The etching was done in a two-electrode Teflon cell with metal base plate to form a back ohmic contact. A thin layer (~ 1 μm) of aluminum was deposited on the back side of the silicon wafer to obtain an ohmic contact. The silicon wafer is served as working electrode (anode) and the platinum mesh served as counter electrode (cathode). Experiments were performed with various anodic current densities and etching time in such a way that the total charge participating in the reaction, Q, was kept constant at 144 C/cm^2. Q can be calculated by multiplying the current density (0.08 $C/s\text{-}cm^2 = 0.08\ A/cm^2$) times the etching time (1800 s). Therefore, two parameter values that affect this total charge are: 1) the current density, and 2) the etching time. In order to

keep this charge constant, if the value of one parameter increases then the other parameter value must decrease and vice versa. The etching solution (electrolyte) consisted of 1:3 (HF:Ethanol) mixture for all experiments. Ethanol was added as a surfactant to facilitate the detachment of the hydrogen bubbles from the surface of the silicon, therefore, resulting in the formation of a more uniform porous layer.

3.3.3 The creation of silicon nano-structure array (3rd stage)

Alkaline solution, consisting of a diluted NaOH (0.2 Molar), was used to fine-etch the porous silicon layer in order to achieve the desired nano-structure. In this fabrication stage, the walls connecting the pillars in the porous silicon were etched until the desired nano-structure array was achieved. A few drops of IPA were applied to the surface of the sample (porous silicon) to increase its wet-ability before immersing it into the NaOH solution. The temperature was kept constant at 35 ºC, and some agitation was applied using a magnet stirrer.

3.4 Results and discussion

3.4.1 Characterization of the textured silicon surface

Samples with different pyramid surface coverage (during the first stage of anisotropic etching) were achieved as a result of various IPA concentrations. Figure 3.3(a) illustrates the SEM image of a sample textured using 1.5 wt. % concentration for IPA (high surface coverage) and the inset shows the higher magnification of the pyramid structure. Figure 3.3(b) illustrates the use of image analysis of SEM image to calculate the surface coverage and the number of pyramids per unit area. Figure 3.3(c) depicts an enlarge view of the pyramids to illustrate the tip, edge and face of the pyramids.

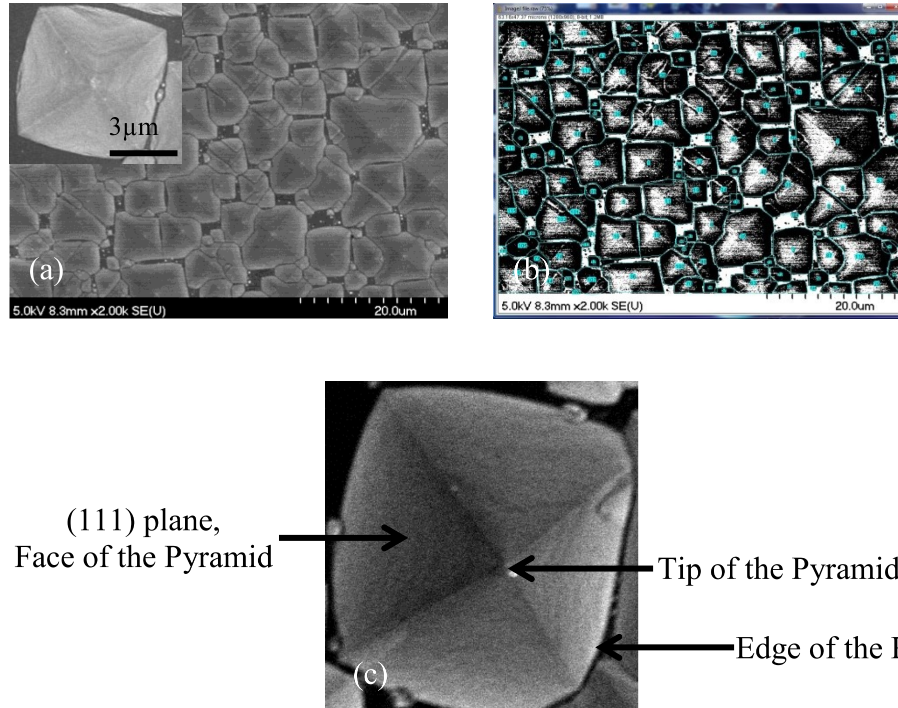


Figure 3.3 (a) Textured silicon surface, (b) image analysis of the textured silicon surface, (c) an enlarge view of the pyramid structure, the tip, edge and face of the pyramid are indicated using arrows

Table 3.1 summarises the influence of various IPA concentrations on the resulting pyramids surface coverage and the number of pyramids per unit area. In order to obtain an average of the measured values, the same experiment was repeated a few times. As it may be observed from Table 3.1, as the IPA concentration increases so do the average pyramids surface coverage and the average number of pyramids per unit area.

Table 3.1 Calculated surface coverage and number of pyramids per 1000 μm^2 using image analysis

	Sample1	Sample2	Sample3
IPA concentration (wt.%)	0	1.5	6
Average Surface coverage of pyramids (%)	48	82	100
Average No. of pyramids per 1000 μm^2	31	41	51

These results were used to correlate the morphology and density of the fabricated nano-structure array to that of the pyramid-textured surface. The density of the pyramids and

how closely packed they were, influenced the creation of the nano-structure array in subsequent fabrication stages.

3.4.2 Characterization of the porous silicon layer created at 2nd stage

To investigate the effect of anodic electrochemical etching parameters on the desired nano-structure, experiments were conducted with various anodic current density and anodic etching time but under constant total charge, Q = 144 C/cm^2. The HF:Ethanol concentration ratio was kept constant at 1:3 for all experiments.

3.4.2.1 Pores initiation and growth mechanism

Figure 3.4 illustrates the progress of the pore formation during the anodic etching stage. The textured surface illustrated in Figure 3.4(a) was prepared under the texturing condition of sample 2 listed in Table 3.1. Figure 3.4(b) shows the pore formation progress after 1 minute. It was observed, that the pore formation initiated from the edge of the pyramids. Image 3.4(c) is the top view of the silicon sample after 3 minutes of anodic etching. The etching had initially started at the edges (Figure 3.4b), followed by the etching of the pyramid faces. The tip of the pyramid identified in Figure 3.4(c) by a square, has remained passivated and unetched. The arrows in Figure 3.4(c) identify the four 111 faces of the pyramid where the etching took place during the porous formation. Figure 3.4(d) shows the cross sectional view of the same sample where the two arrows illustrate the etched pyramid faces.

As it has been reported in the literature, in the case of the inverted pyramids textured surface, the pore formation started from the pit of the inverted pyramids due to the higher electric field [91]. As it was shown in Figure 3.4(b), unlike the inverted pyramid the pore formation initiation points are the edges of the pyramids and not the sharp tips. This may

be attributed to the roughness that had been created as a result of the anisotropic etching during the first fabrication stage. It has been reported that the roughness of the (111) planes leads to the formation of di-vacancies and tri-vacancies [92, 93]. During anoding etching, the dangling bonds on silicon surface are terminated by hydrogen atoms in the forms of mono, di, and trihydride in HF solution [94]. However, the number of hydride depends on the orientation and roughness of the surface [94, 95]. The dihydride ($Si\text{-}H_2$) and trihydride ($Si\text{-}H_3$) termination on silicon surface results in a stronger polarization of the back Si-Si bonds. This polarization is considered to be responsible for weakening the back Si-Si bonds and therefore, facilitate their removal. The initiation of the etching at the edges of the pyramids followed by the 111 faces may be attributed to the trihydride termination of the surface atoms which leads to the preferentially attacked 111 faces.

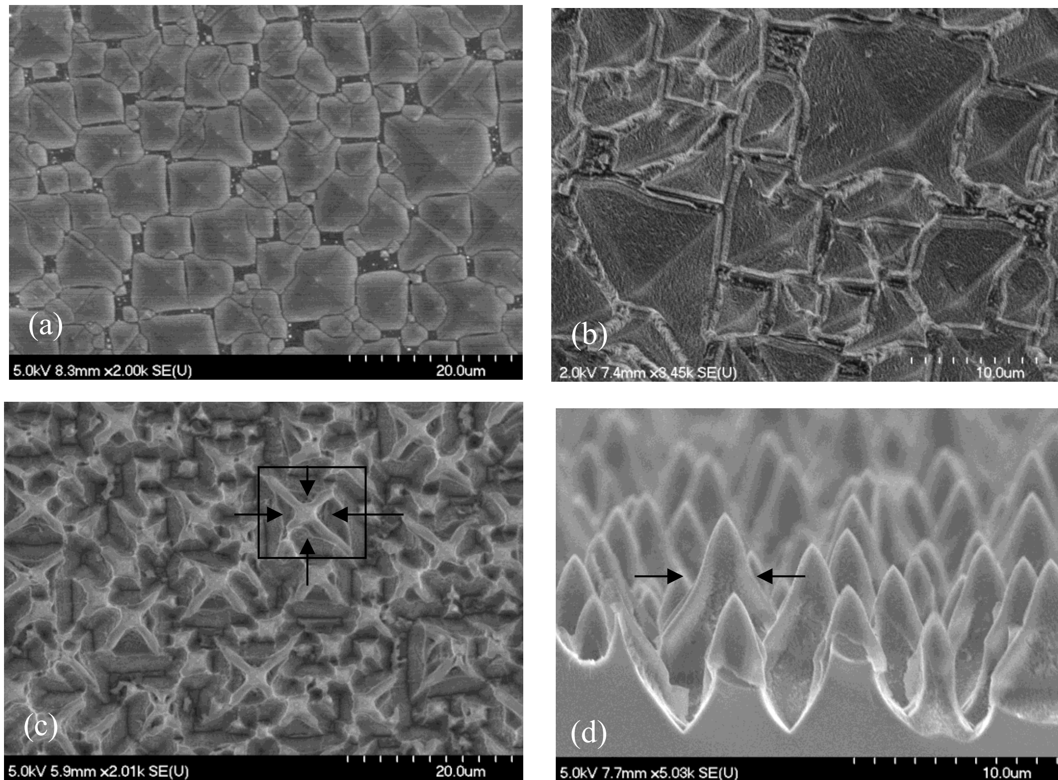


Figure 3.4 The top view of start and progression of the porous layer, (a) textured surface, (b) after 1 minute anodic etching time, (c) after 3 minute anodic etching time, (d) cross section view of the structures (c)

3.4.2.2 Porous formation under various anodic etching conditions with constant charge passed

The effect of various anodic current density and anodic etching time (at constant charge passed) on the formation of silicon porous layer were investigated using sample 2 (Table 3.1) as the substrate. Furthermore, the impacts of these anodic conditions on the fabrication of the desired silicon nano-structure array in the subsequent stages were studied. The current density and the etching time were altered such a way that Q remained the same for all experiments.

Figure 3.5(a) illustrates top view of the morphology of the porous silicon layer created on sample 2 using 80 mA/cm^2, and 30 minutes for anodic current density and etching time respectively. The figure shows the porous silicon consisting of pillars and walls connecting them. It also shows the passivated and unetched tip of the pyramids after 30 minutes of etching time. The circled area in Figure 3.5(a) is magnified and illustrated in Figure 3.5(b) identifying the pillars and the walls. Figure 3.5(c) illustrates the 45-degree tilted view of Figure 3.5(a).

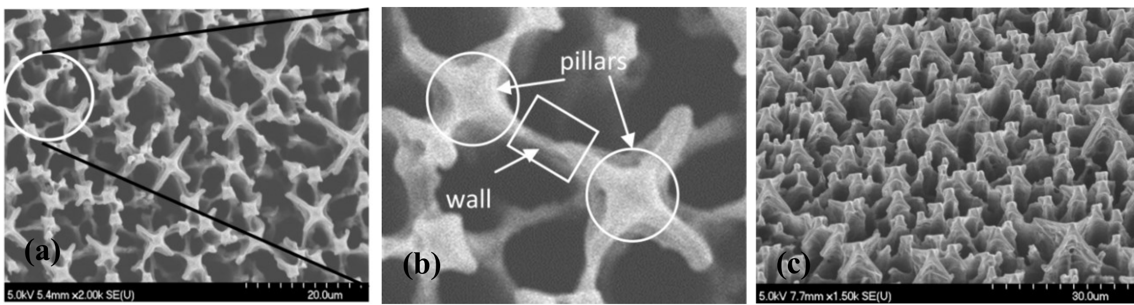


Figure 3.5 (a) The top view of silicon porous layer after 30 min, (b) enlarged image of circled area, and (c) 45 degree tilted view of the image

This morphology may be attributed to the etching of the edges followed by the faces of the pyramids.

Table 3.2 lists the experimental parameter values used for anodic current density and etching time.

Image analysis was performed on the SEM images of the anodically etched samples to obtain the average number of pillars per unit area, the average surface coverage of pillars, as well as the porous layer depth also listed in Table 3.2.

Table 3.2 Characteristics of the samples after electrochemical etching for various anodic conditions (anodic current and etching time).

Anodic Current density (mA/cm^2)	100	80	40	20
Etching time (min)	24	30	60	120
No. of pillars per 1000 μm^2	0	25	31	39
Surface coverage of pillars (%)	0	10.2	19.6	27.6
Porous layer depth (μm)	0	15	35	47

Experiments showed that, at current higher than 80 mA/cm^2, the samples were polished and no porous silicon layer was created. It can also be observed from Table 3.2 that, as the current density was decreased while the etching time was increased (under constant charge passed condition), the average number of pillars per unit area, i.e. pillars surface coverage, as well as the porous layer depth were increased.

Comparing the results in Table 3.1 with those in Table 3.2, one may observe that, for the same surface area, the number of created pillars is less than the number of pyramids. This may be due to the completely etched of the smaller pyramids during the anodic etching stage.

3.4.3 Characterization and analysis of the nano-structure array created at 3rd stage

3.4.3.1 Effect of anodic etching conditions with constant Q

As it was listed earlier in Table 3.2, samples with different morphology of porous layer were obtained as a result of various anodic etching conditions. The porous silicon layer can be removed using different alkaline solutions like KOH, NaOH, and TMAH [96, 97]. In this work, low concentration of NaOH (caution should be taken to keep etching rate low enough to avoid destroying the nano-structures) was used to remove the interconnected walls between the pillars to reveal the nano-structures. Figure 3.6 illustrates the effect of anodic etching conditions on the number of pillar (pre-NaOH etching) as well as the number of nano-structures (post-NaOH etching) per 1000 μm^2. It can be observed that with a constant charge passed, a combination of lower current density and higher etching time results in higher number of pillars.

However, only a specific anodic etching condition (80 mA/cm^2 and 30 min) results in the creation of nano-structure arrays at the end of the final stage of the fabrication. In fact, further away from this optimal condition, almost no nano-structure was achieved. As the anodic current was reduced the pore diameter decreased resulting in the creation of thicker walls. On the other hand, as the etching time increased, the depth of the pores increased as well. A combination of thicker wall (connecting the pillars) and deeper pores created at the 2nd fabrication stage may hinder the formation of the nano-structures in the 3rd stage.

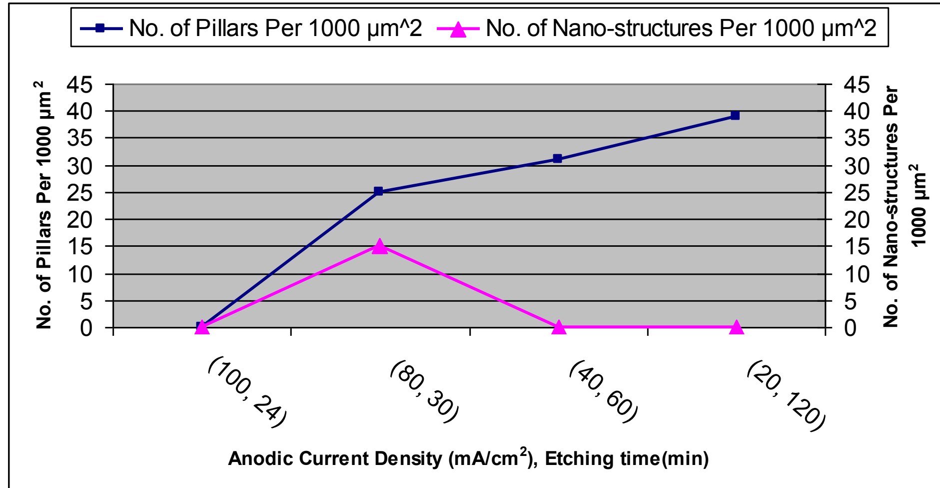


Figure 3.6 Number of pillars per 1000 μm^2 and number of nano-structures per 1000 μm^2 at various anodic etching conditions.

3.4.3.2 Effect of anodic etching condition at various Q values

As it was shown in Figure 3.6, the nano-structures were obtained only under certain anodic etching condition (80 mA/cm^2 , 30 min). In order to investigate the effect of anodic etching conditions with various Q on the creation of nano-structure arrays, the current density was kept constant at 80 mA/cm^2 , while the anodic etching time was changed. Shallower pores with thicker walls were fabricated under 80 mA/cm^2 current density when the samples were etched for 5 and 15 minutes. However, to acheive the nano-strucures, the NaOH fine-etching time needed to be increased in order to compensate for the thicker walls. Figure 3.7 illustrates the nano-structures when the anodic current density was kept at 80 mA/cm^2 for various anodic etching times. The NaOH fine-ecthing time was increased to obtain the desired nano-structure arrays.

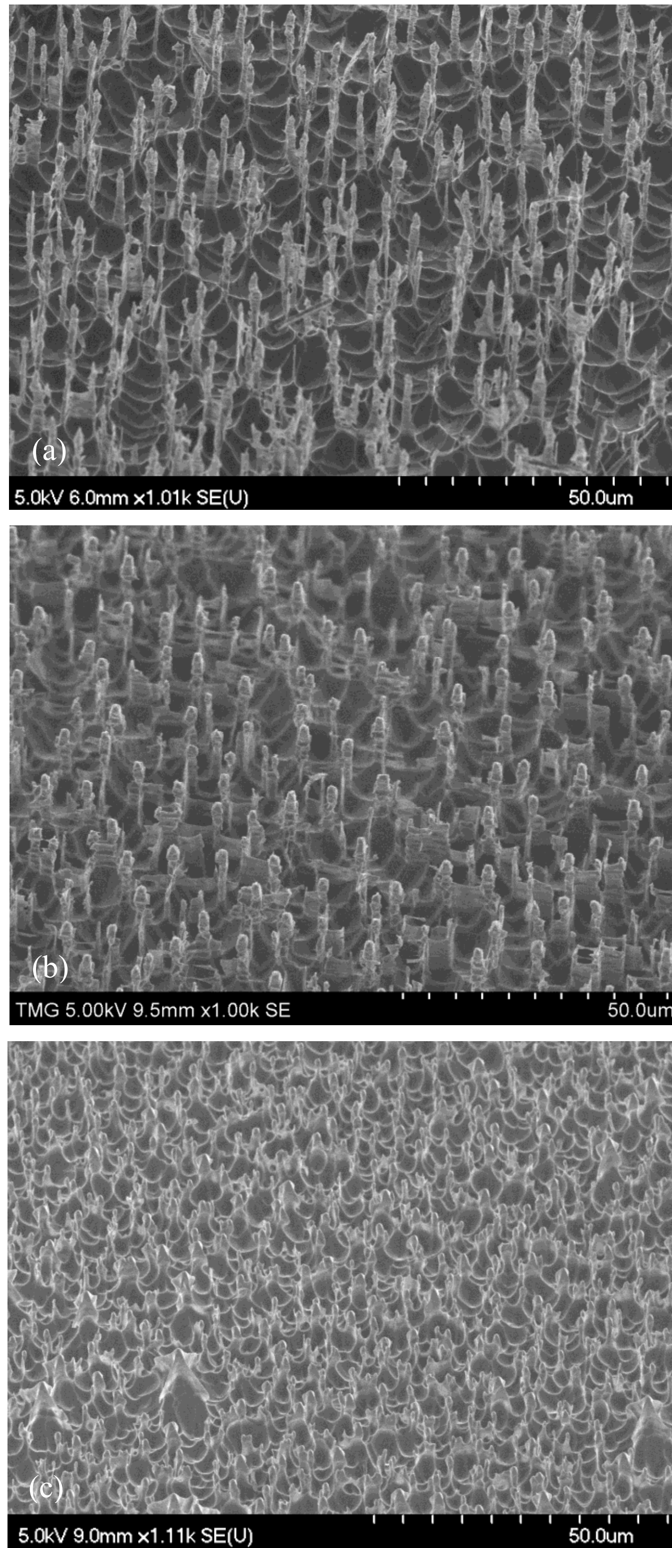


Figure 3.7 The nano-structure array fabricated under constant 80 mA/cm^2 and various etching time, (a) anodic etching time (30 min), NaOH etching time (2.5 min), (b) anodic etching time (15 min), NaOH etching time (4 min), (c) Anodic etching time (5 min), NaOH etching time (5min).

Table 3.3 summarises the influence of the anodic etching time on the geometry and aspect ratio of the fabricated nano-structure arrays. The longer the anodic etching time, the higher aspect ratio was acheived. It can also be observed from the Table 3.3 that as the anodic etching time is increased, the tip diameter of the nano-structure becomes smaller.

Table 3.3 Measured geometric characteristics of nano-structures for samples under different etching times

	Anodic etching time (min)	Tip diameter (nm)	Length (μm)	Rod diameter (μm)	Aspect ratio
(a)	30	50	15	2	7.5
(b)	15	100	10	3	3.3
(c)	5	500	4	2.5	1.6

3.4.3.3 Effect of pyramid surface coverage

As it was shown in Figure 3.4, the tip of the pyramids resist against electrochemcial etching. On the other word, the pyramid-shaped structures act like a mask layer that preserves the strcuture underneath during progress of anodic etching. Samples with various densities, pyramid surface coverage, were created using different IPA concentration. The goal is to study the effect of density of the pyramid-shape structures on formation of silicon nano-strcuture arrays.

Figure 3.8 illustrates the SEM images of textured samples as a result of anisotropic wet etching of silicon in a mixture of TMAH/ IPA(as detailed in section 3.3.1). The charactristics of these samples were listed in Table 3.1.

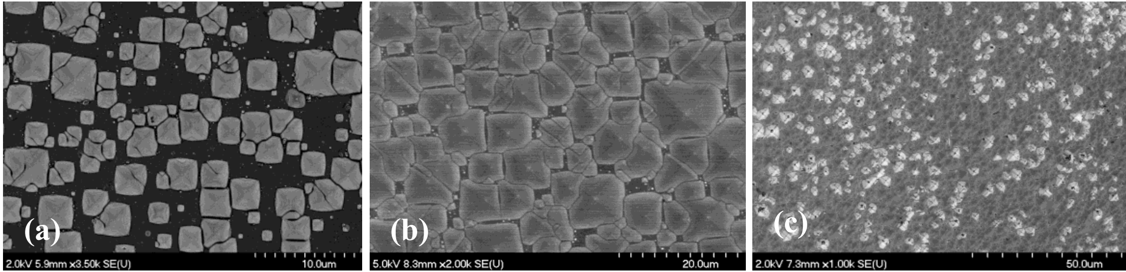


Figure 3.8 Pyramid-shape structures created on silicon surface in the presence of different IPA concentrations. (a) No IPA, (b) 1.5 wt.% IPA, and (c) 6 wt.% IPA

Then the samples were anodically etched under the best set of anodic etching conditions, 80 mA/cm^2 and 30 minute (as illustrated in Figure 3.6). Figure 3.9 illustrates the tilted view of porous layers created using sample (a) and sample (b) (shown in Figure 3.8) respectively. As shown in Figure 3.9, the tip of the pyramids acts like a mask layer and as a result the underneath silicon remained unetched as anodic etching is progressed.

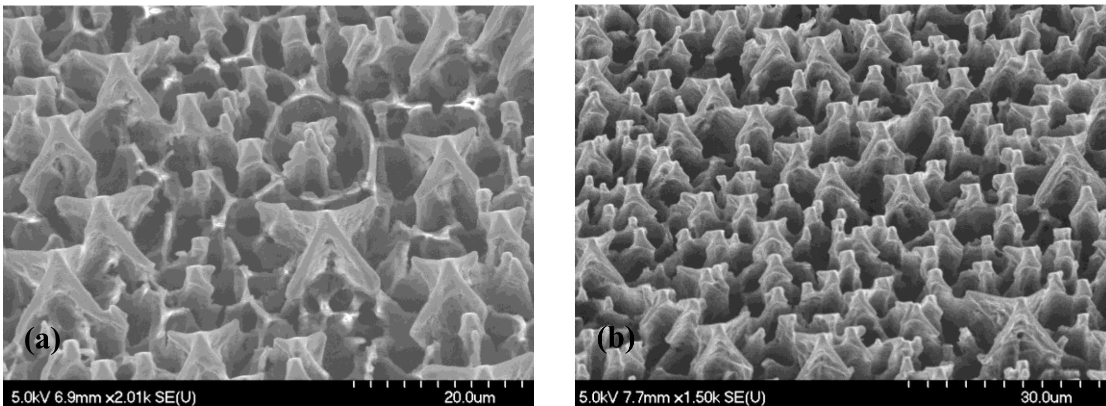


Figure 3.9 The tilted view of porous silicon layer after 30 minutes of etching time (a) using sample (a), (b) using sample (b).

As it can be observed from Figure 3.9(a) , a non-uniform porous silicon layer created when anodic etching has been performed on sample (a). The non-uniformity of the porous layer is due to the lower density of the pyramid-shape structures. Interestingly, it was observed that the electrochemical etching was initiated exactly from the edges of the pyramids and not from the uncovered spaces between the pyramids. It was also observed

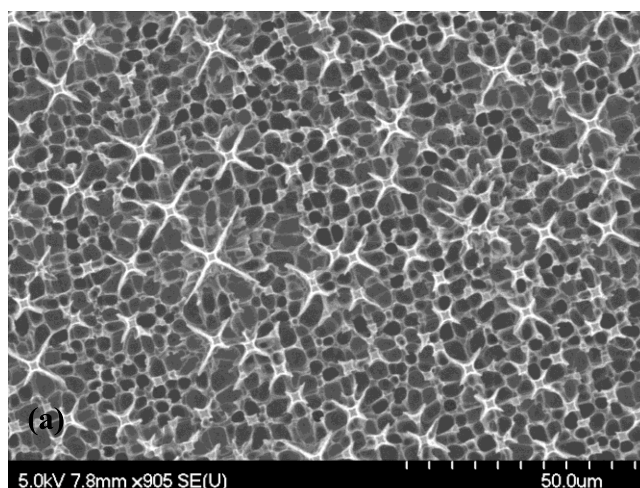
that these spaces between the pyramids were covered with random distributed pores later as anodization continued.

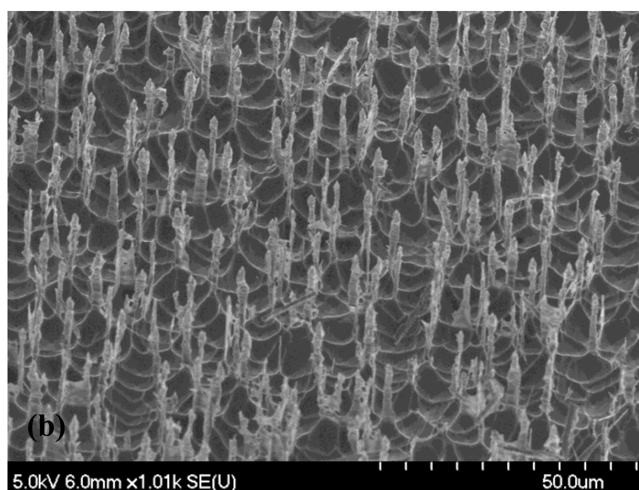
Following the anodic etching of the samples they were then etched in NaOH solution to generate the final nano-structures. Figure 3.10(a)-3.10(c) illustrates the SEM images of the samples after immersing in 0.2 Molarity NaOH solution. Figures 3.10(a)-3.10(c) are resulted after conducting the two steps processing (anodization and NaOH treatment) on Figures 3.8(a)-3.8(c)respectively.

Figure 3.10(a) shows the SEM image of the structure obtained after NaOH treatment of sample shown in Figure 3.9(a). As it can be obsrved, not only the nano-structures are not developed also the porous morphology of the sample has been still preserved after NaOH treatment. It can be observed from this figure that the pillar structures are surrounded by randomly distributed pores. The obtained result can be attributed to the existence of the random pores that are generated due to the low pyramid surface coverage. The development of free-standing nano-structure depends on dissolution of these pores. It was found from the experiments that higher concentrations of NaOH solution and longer etching time did not result in formation of nano-structure but annihilation of the entire structure.

Figure 3.10(b) shows the SEM image of free-standing nano-strcuture achieved by NaOH treatment of anodized sample shown in Figure 3.9(b). This structure shape is achieved by pruning away the excess parts of the anodized sample (sidewalls) using NaOH. Accordingly, the tip of the pyramids and the underneath structure are the survivor parts of the anodized samples after NaOH treatment that form the free-standing nano-strcuture.

As shown in Figure 3.10(c), the same shape structures as the Figure 3.10(b) are achieved after NaOH treatment of anodized sample that was prepared using sample (c). Although, there is a difference in density of the nano-structure array, the denser array is achieved using sample (c).





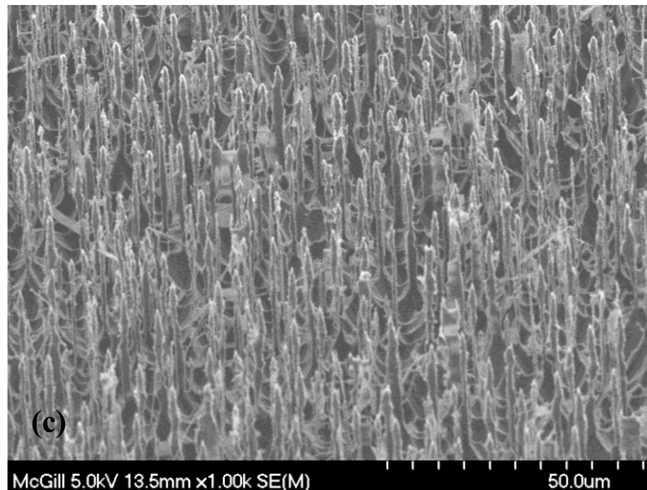


Figure 3.10 SEM image of silicon nano-structure fabricated using samples with various pyramid surface coverage (a) sample (a) 48%, (b) sample (b) 82%, and (c) sample (c) 100%.

Figure 3.11 shows the relation between the surface concentration of pyramids to the concentration of produced nano-structures. It was observed, that there is a correlation between the pyramid surface coverage and the number of generated nano-structures. As the pyramid surface coverage increases, so do the number of nano-structures. It may also be noted, that the number of nano-structures decreases dramatically as the pyramid surface coverage gets below 80%. This may be attributed to the fact that, as pyramids surface coverage decreases, the spaces between the pyramids increase. This results in random pores creation in the empty space between the pyramids. The creation of random pores with smaller diameters (and therefore thicker walls) hinders the removal of the walls (to generate nano-structures) during the NaOH etching stage. The number of nano-structures is increased as the rate of pyramid surface coverage goes above 80%. However, at much higher rates, the ratio of the pyramid to nano-structure stayed practically the same. This shows that the number of nano-structures per a certain surface area may be increased (higher density) without having an impact on the conversion rate.

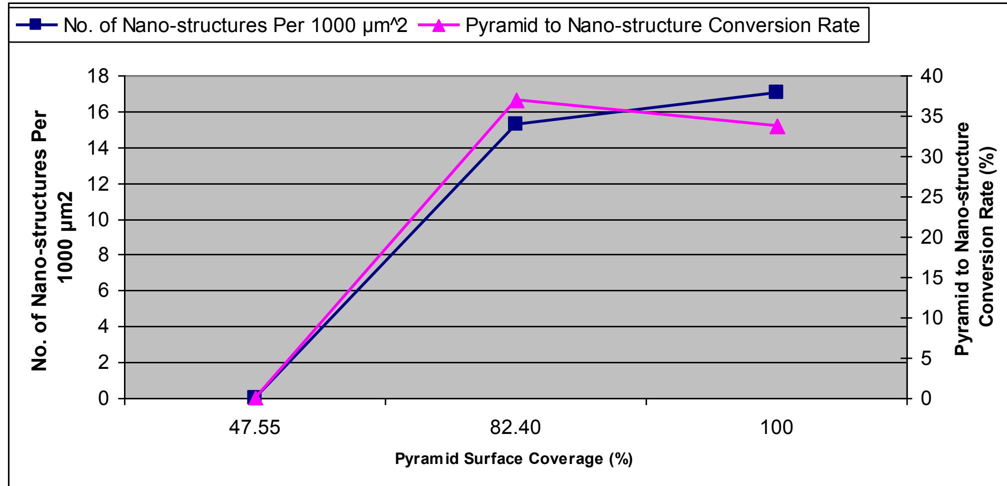


Figure 3.11 Number of nano-structures per 1000 μm^2 and pyramid to nano-structure conversion rate at various pyramid surface coverage.

3.4.4 The morphology of the nano-structure

Figure 3.12 shows the SEM images of the rods created after NaOH treatment. Figure 3.12(b) shows the high magnification SEM of a rod, and Figure 3.12(c) shows the close up of the nano-structure tip.

As it can be observed in Figure 3.12(b) and 3.12(c), the structure has a unique layered morphology and consists of the square shape flakes sitting on top of each other along <100 > direction. The length of the synthesized nano-structure is roughly 15 μm, the thickness of each flake is around 20 nm and the space between the flakes is around 200 nm.

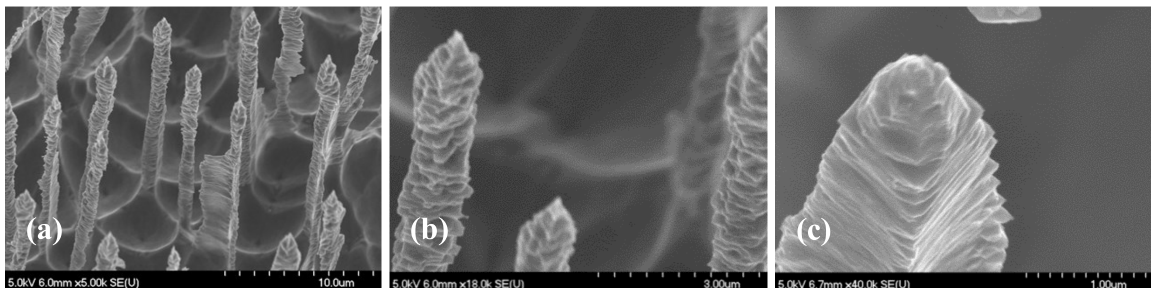


Figure 3.12 (a)SEM image of nano-layered rods formed after NaOH treatment, (b) higher magnification of the rod, (c) nano-layered tip of the rod.

The formation of the layered structure can be attributed to the anisotropic behavior of NaOH solution. In order to examine this hypothesis, the morphology of the porous structure after electrochemical etching was investigated. Figure 3.13 shows the SEM image of cross-section of porous silicon layer before immersing in NaOH. As it can be observed in the figure the pillars of the porous layer are almost smooth and no evidence of progression of etching into pillars was observed.

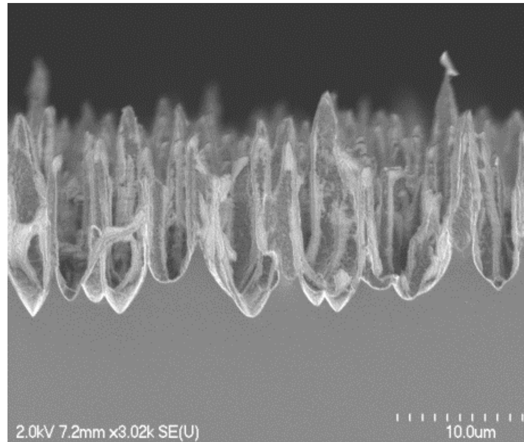


Figure 3.13 Cross-sectional view of macro-pores befor NaOH treatment.

The formation of this morphology can be interpreted using the anisotropic etching of silicon in alkaline solution. At the third fabrication stage, when the samples are immersed into NaOH solution the reaction of porous silicon layer with OH^- ions starts. Although the total porous layer reacts with OH^- ions, but the thinner pore sidewalls are dissolved faster than the pillar structure. Consequently, a nano-layered structure is generated along 100 direction.

The proposed technique in this work is not only a simple and low-cost technique due to the inherent self-mask behaviour that it shows, it also enjoys from the efficient usage of the surface.

As it discussed earlier in chapter 2, section 2.6.1, the size and shape of the seeding sites affect the pore formations (See Figure 2.8). Figure 3.14 schematically illustrates the nanowire formation when the inverted pyramids are used as seeding sites. In this figure, each square, solid line represents a macro-pore formed by etching progression of the pits of the inverted pyramid and the dashed lines represent the enlarged macro-pore after post-processing treatment. As it illustrates the nanowire is created at the cross point of each four inverted pyramids. According to this schematic, the number of nanowire follows this relation:

$$N = \left(\frac{n}{2}\right) - 1$$

Where N, presents the number of nanowires and n, presents the number of pits (inverted pyramids). In contrast to the inverted pyramid pattern, the pyramid-shape pattern that was used in this work offers a better way for sufficient use of the surface. Owing to its self-mask behaviour, pyramid-shape pattern results in roughly twice denser nano-structures. It is due to the fact that each pyramid corresponds with one nano-structure.

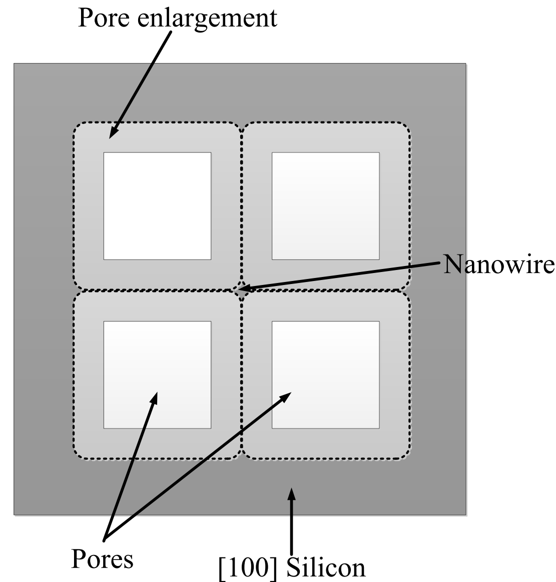


Figure 3.14 Schematic that shows the formation of nanowire only at cross-points of each four inverted pyramids, the location of each pore corresponds with the pit of the inverted pyramid [24].

From applications point of view, the density of the nano-strcuture is an important factor. For instance, for field emission display applications a minimum of 10^6 nanorods/cm^2 is required [98]. The average number of nano-structures produced using the three-step approach was calculated to be 1.8 million per square centimetre.

3.5 Conclusions

Silicon nano-structure array was fabricated through a novel low-cost multi-stage approach. The pyramid structures practically covered the entire silicon surface as a result of anisotropic wet etching technique. This stage was followed by electrochemical anodic etching. The etching initiated at the four edges of the pyramids and progressed inward through 111 faces. The pores are grown vertically along the [100] direction at each face. In the final stage the interconnected porous walls are etched, to form the nano-structure array.

The first fabrication stage is a vital step towards the fabrication of silicon nano-structure arrays. The highly packed pyramids surface coverage is a prerequisite for fabrication of silicon nano-structure array, as the number of nano-structures drops dramatically below 80% and no nano-structures were obtained at low surface coverage values of around 50%.

Experiments revealed that, for a constant charge passed, as the current density decreases the pillar density increases. On the other hand, the higher number of pillars per surface area does not necessarily result in higher number of nano-structures. Accordingly, the optimal current density value seems to be around 80 mA/cm^2 as greater values resulted in no nano-structure formation (due to surface polishing) and at lower values, the creation of thick walls prevented the transformation of the created pillars into nano-structures.

The anodic etching time may be used as a practical parameter to control some nano-structure characteristics such as length and thickness.

The fabricated nano-structure arrays may have wide applications in MEMS/NEMS, energy storage and harvesting, solar cells and electron emitters in field emission devices.

4. Fabrication of vertical nano-structure array on silicon wafer: Electrochemical etching at transition regime

Electrochemical etching of silicon can be performed in three distinct regimes, porous silicon formation, transition and electropolishing. The first regime offers the possibility of formation of porous silicon layer with various kinds of morphologies. In chapter 3, the electrochemical etching was performed at porous silicon formation, with the aim of creation of macro-pores array as building blocks for development of silicon nano-structure array. In this chapter, the electrochemical etching method on transition regime is studied. The electrochemical etching is purposely performed at this regime with the aim of development of the silicon nano-structure in a one-run electrochemical etching process. Therefore, the NaOH treatment step (discussed in Chapter 3) is mitigated from the fabrication process. The electrochemical etching parameters including HF concentration and etching time are optimized for formation of nano-structures.

4.1 Introduction

As it was mentioned and elaborated in section 2.4, the process of electrochemical etching of silicon exhibits three distinct regimes known as porous formation, transition, and electro-polishing [18]. The regime in which the electrochemical etching takes place can be mainly determined by etching parameters (e.g., doping type of the sample, HF concentration, anodic current, etc.)

In chapter 3, a novel lithography-free fabrication technique to grow silicon nanostructures was introduced. The experimental results were presented describing the fabrication of silicon nano-structures by electrochemical etching in a *porous formation regime* which consists of three consecutive steps: texturing the silicon surface, formation of a porous silicon layer, and finally a fine-etching step.

The texturing of the silicon results in creation of highly-packed pyramids, which predetermine the location of nano-structure formations during the following steps. The textured surface is electrochemically etched to create a porous silicon layer. This step is then followed by fine-etching of the walls between the pores using a diluted alkaline solution, to generate nano-structure arrays.

This chapter addresses and investigates the possibility of fabrication of free-standing nano-structure arrays through a two-step process using anisotropic wet etching, followed by electrochemical etching process. According to this method, the latter etching process is conducted in the transition regime (between porous formation and electro-polishing regime), which in turn eliminates the third fabrication step fine etching, described in chapter 3.

In order to obtain a better insight into the formation of nano-structures, the effect of the anodic etching time on their morphology is investigated. In addition, the effects of

pyramid size uniformity and HF concentration on the creation of silicon nano-structures are studied.

4.2 Experimental Procedure

The fabrication process begins with generating pyramid structures on the surface of the samples using anisotropic etching of the silicon, followed by an electrochemical etching process to develop silicon nano-structures. These two stages are described in detail in the following sections.

4.2.1 Fabrication of the pyramids (1st stage)

The surface of the silicon wafer was textured using an anisotropic etching process in TMAH for 30 minutes. The TMAH was diluted with DI water to reach the desired 1.5 % concentration and used in all experiments. The etchant temperature was kept constant at 90° C, for the duration of all experiments. IPA was added to the TMAH solution in order to facilitate the hydrogen bubbles detachment from the surface of the silicon. The effect of adding IPA with different concentrations on the developed pyramids' size uniformity, at this stage, was studied.

4.2.2 Development of silicon nano-structure (2nd stage)

An anodic electrochemical etching was performed on the textured silicon surface, using a two-electrode Teflon cell. A layer of aluminum (~1 μm) was deposited on the back side of the silicon wafer to obtain an ohmic contact. The silicon wafer, then, served as a working electrode (anode), and a platinum mesh served as a counter electrode (cathode). The anodic current was kept constant, at 120 mA, during the entire process. The etching solution, electrolyte, consisted of a mixture of HF and ethanol. The textured surface was

exposed to the electrolyte. Ethanol was added to serve as a surfactant to reduce the surface tension, and to remove the hydrogen bubbles generated during the etching process.

4.3 Results and Discussion

4.3.1 Characterization of the textured silicon surface (1st stage)

It has been evident from the experiments that the concentration of the added IPA to the solution affects the size uniformity and the surface coverage of the pyramids. The concentration of IPA was changed from 1.5 to 9% with the step of 1.5%. The obtained results revealed that for IPA concentrations as high as 6%, the surface coverage of the pyramids is increased and reached a maximum, full surface coverage. Experimental observation showed that the size of the pyramids is decreased as the IPA concentration is increased. Both pyramids surface coverage and their size uniformity are improved as the IPA concentration is increased to 6 %. A higher concentration of IPA however, reduces both the surface coverage and the uniformity of the pyramids sizes. Adding 9% IPA to the solution generated pyramids with a very wide range of sizes (between 1-12 μm).

An SEM image of a textured surface etched in 1.5% TMAH, and added 1.5% IPA is shown in Figure 4.1.

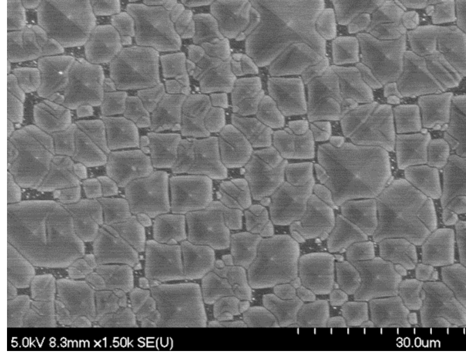


Figure 4.1 Top view of a textured silicon surface. The TMAH concentration was 1.5%, The IPA concentration was 1.5%, the etching time was 30 minutes and the temperature of electrolyte was 90 ºC.

The surface coverage, the average base area of the pyramids, and the standard deviation values were obtained by performing image analysis of the SEM photos, using ImageJ image processing program, developed by the US National Institute of Health. Table 4.1 summarizes the influence of IPA concentration on the resulting pyramids surface coverage and size. The results shown in Table 4.1 are the average of several experiments repeated under the same conditions. The calculated standard deviation of the pyramid size confirms that the uniformity of the pyramids size, considerably improves by increasing the IPA concentration to 6%. This uniformity however, dramatically is decreased as the IPA concentration is increased further to 9%. The influence of these pyramids size uniformity on development of silicon structures, formed during the second stage, is investigated in section 4.3.3.

Table 4.1 Calculated average pyramid surface coverage and base area of the pyramids using image analysis.

	Sample 1	Sample 2	Sample 3
IPA concentration (wt.%)	1.5	6	9
Average surface coverage of pyramids (%)	82	100	90.78
Pyramid size distribution (μm)	6-8	3-4	1-12
Average base area of the pyramids (μm^2)	19.88	6.2	18.47
Standard deviation (μm^2)	16.04	2.68	26.57

4.3.2 The creation of silicon nano-structure arrays (2nd stage)

In order to gain a better insight into the formation of silicon nano-structures, a set of experiments was performed at several anodic etching times, under a constant current of 120 mA. The HF:ethanol concentration ratio was kept constant at 1:4, for all experiments. All the anodization experiments were performed on surfaces textured with the same characteristics of the surface of sample 1 listed in table 4.1 unless otherwise mentioned.

Figure 4.2 illustrates the progress of formation of the nano-structure arrays during the anodic etching stage after 3, 7, and 10 minutes of etching, respectively.

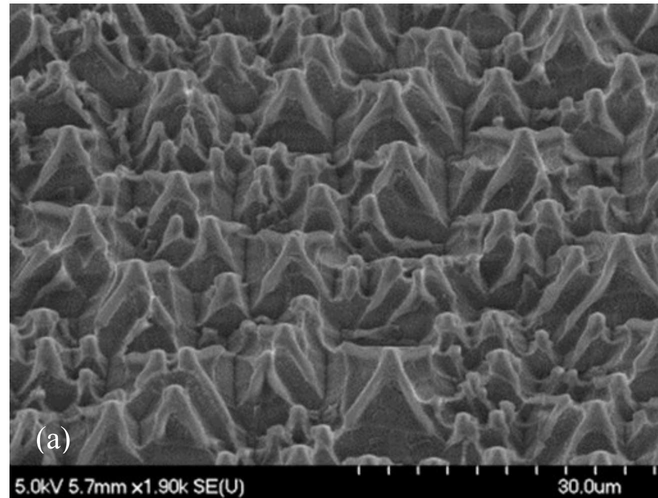
Figure 4.2(a) shows the view of the tilted silicon sample after 3 minutes of anodic etching. As can be observed, the etching had initially started at the edges of a pyramid, followed by etching of the four pyramid faces. From Figures 4.2(b), etched for 7 minutes, and 4.2(c), etched for 10 minutes, one can see that as anodization progresses the pyramid structures evolve to new structures. The new structures consist of pillars that are linked to each other by sidewalls, shown by arrows in the Figures 4.2(b) and 4.2(c).

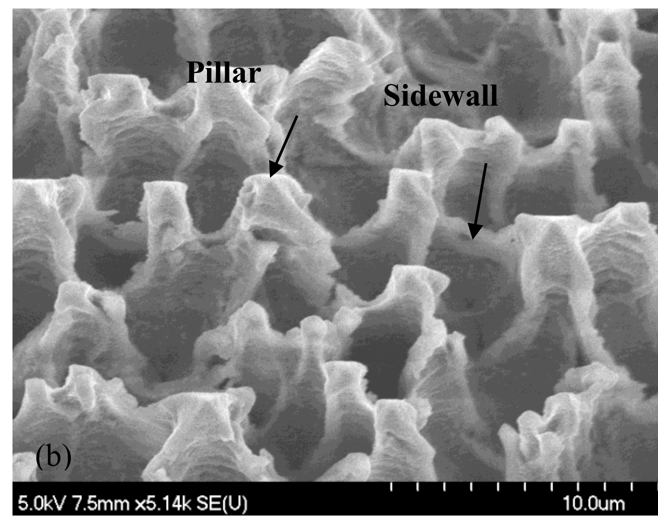
Figures 4.3(a)-4.3(c) show cross-sectional views of the same samples of Figures 4.2(a)-4.2(c), respectively. The results show that as the etching continues, the pyramids are etched laterally and vertically until the average diameter of the pyramids reaches 1.5 μm (about 10 minutes). Based on our experimental observations, the average of pyramids' diameters is not affected by further etching. Vertical etching of the structures however, continues until the final nano-structures are obtained. As Figure 4.4 illustrates, a complete structure of rods appeared after 30 minutes of anodic etching.

The characteristics of the structures developed under various etching time are summarized in Table 4.2.

Table 4.2 Characteristics of the samples developed under various etching times.

Anodic etching time (min)	Diameter of the structure (μm)	Length of the structure (μm)
3	3	5
7	2	9
10	1.5	12
30	1.5	20





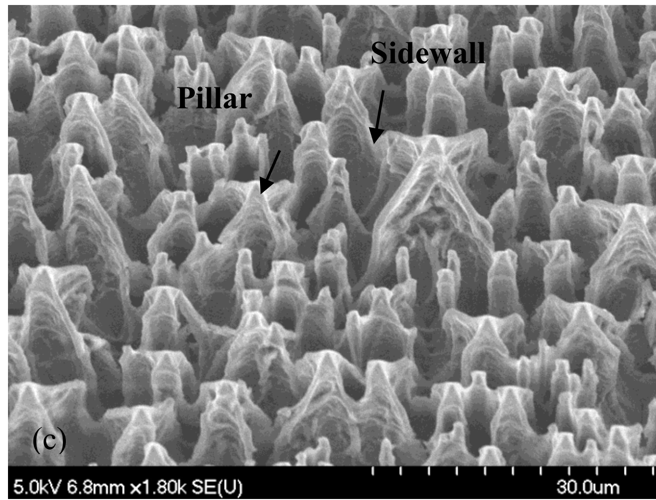
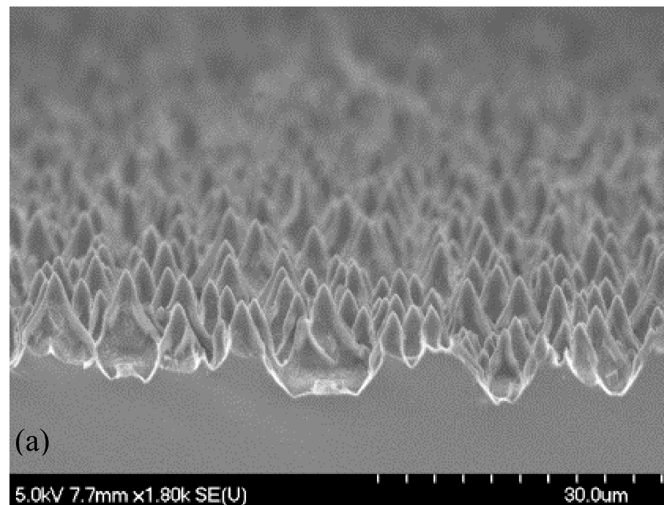


Figure 4.2 Tilted view SEM images of silicon structures formed after anodization of silicon, for etching times of 3 minutes (a), 7 minutes (b), and 10 minutes (c). The HF:ethanol ratio was 1:4, and the anodic current was 120 mA in all cases.



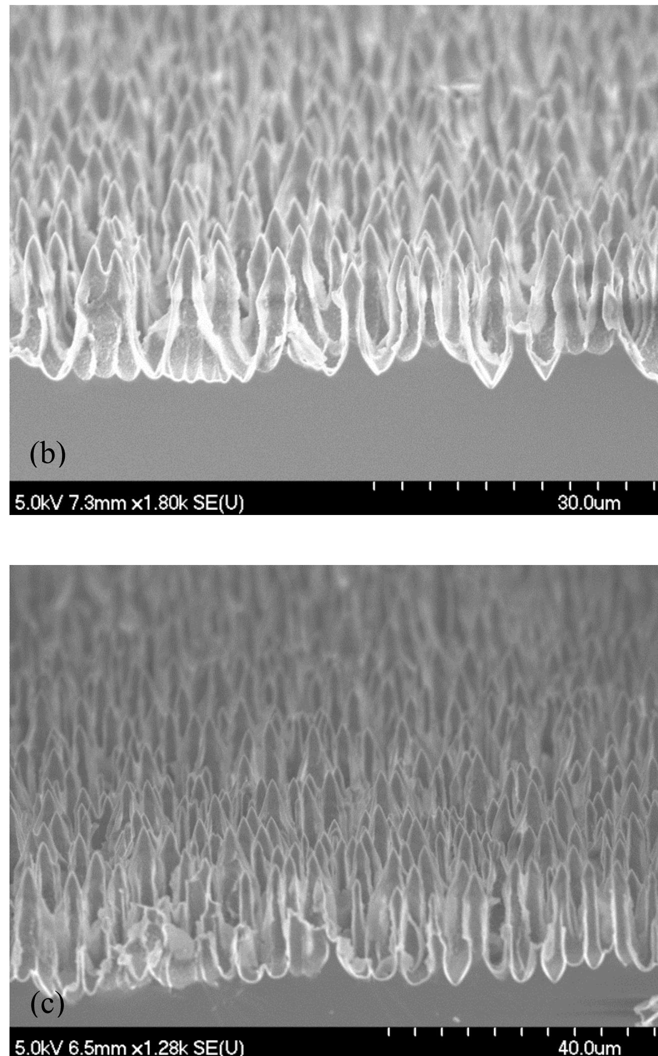


Figure 4.3(a) - 4.3(b) Cross-section SEM images of the same samples shown in Figure 4.2(a)-4.2(c) respectively.

The cessation of lateral etching can be attributed to the width of the space charge region (SCR), as suggested by the macropore formation model of V. Lehmann and S. Ronnebeck [91]. According to this model as the electrochemical etching continues, the space charge region extends into the silicon nano structures. Therefore, the extension of SCR region will deplete the silicon from hole carriers, which are responsible for the

etching process taking place in the electrolyte and hence stops the lateral etching of the structures.

In fact, the lateral etching of the structure continues until the diameter of the structure reaches the SCR width. The theoretically calculated SCR width for p-type silicon with 10-20 Ω-cm resistivity is reported to be 0.87-1.2 μm [99]. This value is in good agreement with the average diameter of the silicon nano-strcutures obtained in our experiments.

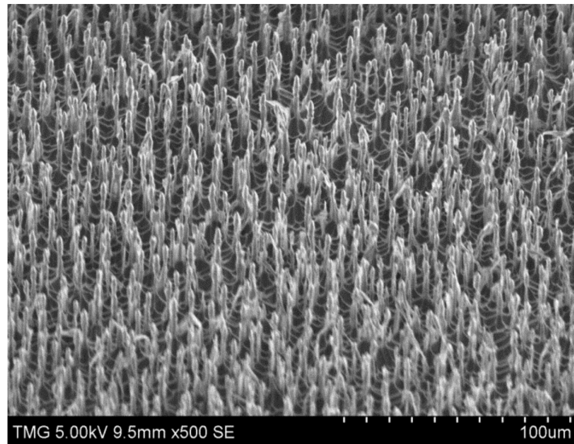


Figure 4.4 A tilted view of silicon nano-structures after 30 minutes anodization. The average diameter of the nano-strcutures is 1.5 μm, the average diameter of the tip is 250 nm, and the length of the structure is 20 μm.

Using ImageJ program, the average number of free-standing nano-structure on the silicon surface was calculated to be 1.1 million per square centimetre.

4.3.3 Effect of pyramid size uniformity on formation of the silicon nano-structures

In order to investigate the effect of size uniformity of pyramids (fabricated on the 1st step) on the formation of nano-structure arrays, electrochemical etching was applied on other samples with less pyramids size uniformity, as illustrated in Figure 4.5(a). Figure 4.5(a)

is SEM image of the sample 3 listed in Table 4.1. Figure 4.5(b) shows the tilted view of one of the samples after electrochemical etching under the same anodization conditions applied to the samples shown in Figure 4.4. One clear observation is that despite the applying of the same electrochemical etching conditions, no free-standing nano-structures were obtained. As shown in Figure 4.5(b) the pillars are still linked to each other by unetched sidewalls, shown by arrow.

Another interesting observation from Figure 4.5(b) is the presence of unetched smaller size pyramids, shown in circled areas. These observations can be attributed to the pronounced non-uniform pyramids size distribution. The pyramidal textures with a wider size distribution (1-12 μm), perturbs the uniform dissolution of the sample in the electrolyte and therefore, results in the formation of non-uniform sidewalls.

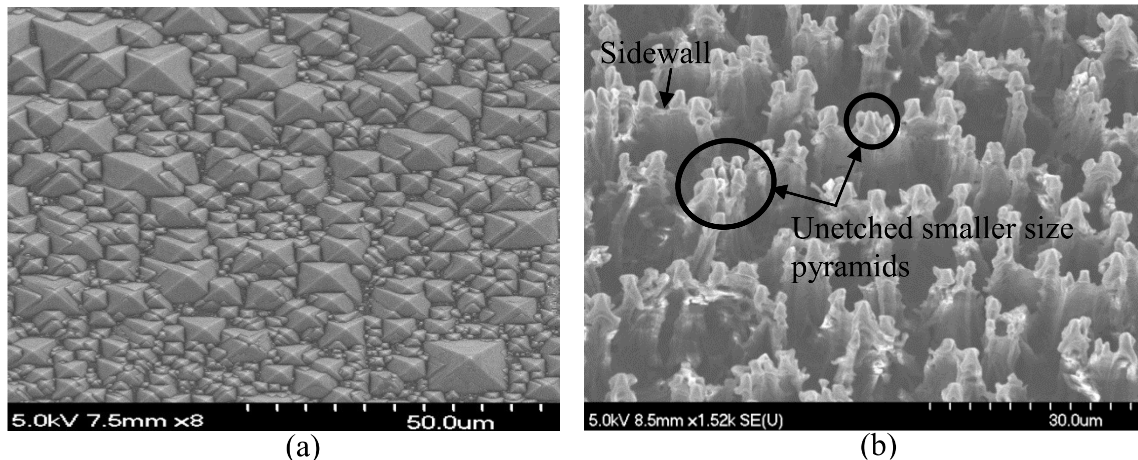


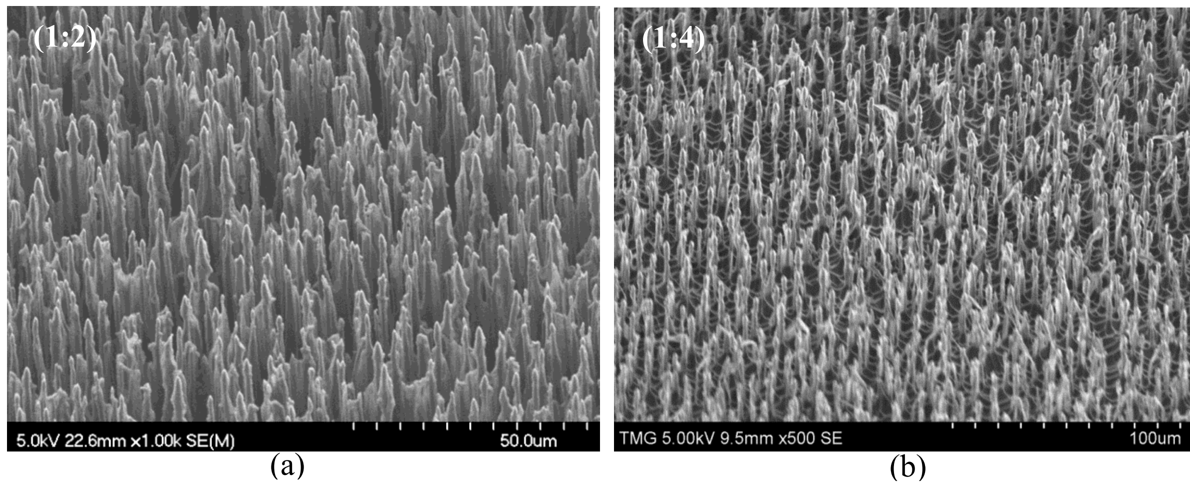
Figure 4.5 (a) A tilted view of the textured silicon surface with a non-uniform pyramids size. (b) a tilted view of the same sample after electrochemical etching. Circled areas contain unetched small pyramids.

Observation of both unetched sidewalls and smaller size pyramids can be attributed to the SCR width effect, as mentioned in section 4.3.2. Pyramids and sidewalls resist etching, whenever their sizes are equal or smaller than the SCR width, ~ 1.5 μm.

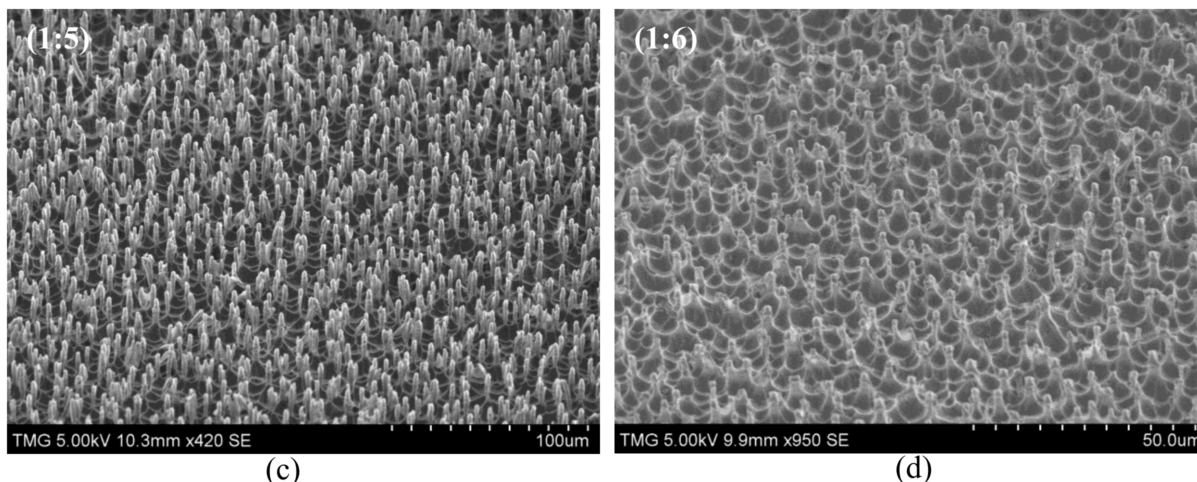
According to the experimental results, uniformity and size of the pyramids are two key essential factors in creation of nano-structures. These observations confirm that in order to realize silicon nano-structures, the size of the pyramids (obtained in the first fabrication step) is required to be greater than the SCR width.

4.3.4 Effect of HF concentration on the formation of nano-structure arrays

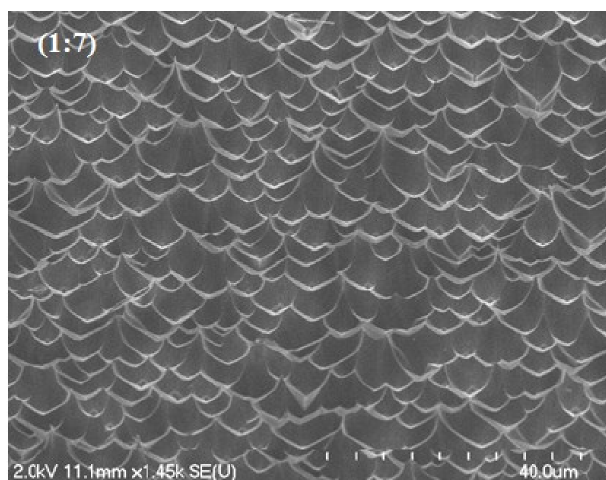
The variation of silicon nano-structures under various HF concentrations was also studied. In these experiments, several HF:ethanol ratios of 1:2, 1:4, 1:5, 1:6 and 1:7 were used to perform anodic etching of the samples. The anodization of all samples was performed for 30 minutes under an applied current of 120 mA. Figures 4.6(a)-4.6(e) show the SEM images of the structures developed during this investigation.



(a) (b)



(c) (d)



(e)

Figure 4.6 Effect of HF concentration on the creation of free-standing nano-structures, when the ratio of HF:ethanol in the electrolyte was: (a)1:2, (b) 1:4, (c) 1:5, (d) 1:6, and (e) 1:7. The anodic current was 120 mA, and the etching time was 30 minutes in all cases.

As can be seen from Figures 4.6(a)-4.6(e), the proper free-standing nano-structures formed merely at a certain concentration range of HF in the electrolyte. At a high concentration ratio of 1:2, long pillars connected with the sidewalls formed, Figure 4.6(a). On the other hand, at a very low concentration ratio of 1:7, the pyramids were completely etched away and no nano-structures formed, Figure 4.6(e).

For HF:ethanol ratios of 1:4, 1:5, and 1:6 well-structured rods were developed, Figures 4.6(b)-4.6(d). Observations showed that the length of the nano-structures were largest for the ratio of 1:4, followed by those for 1:5 & 1:6, respectively. The results show that in this range, the vertical etching rate of the sample decreases as a function of the HF concentration in the electrolyte. Therefore, the creation of shorter nano-structures can be attributed to the formation of shallower pores.

The nano-structures with the largest aspect ratio were developed at HF:ethanol ratio of 1:4. However, the concentration ratio range of 1:4 to 1:6 is believed to be an optimal one to develop nano-structures. In fact, this optimal range of HF concentration ratios defines the interval, where the anodization occurs in *the transition regime*. A lower HF concentration moves the electrochemical etching to the *porous silicon formation regime* and higher HF concentrations shift it to the *electro-polishing regime.*

4.3.5 The morphology of the nano-structure

Figure 4.7(a) shows the SEM images of the structure created after electrochemical etching step. Figure 4.7(b) shows the high magnification SEM of the structure, and Figure 4.7(c) shows the close up of structure tip.

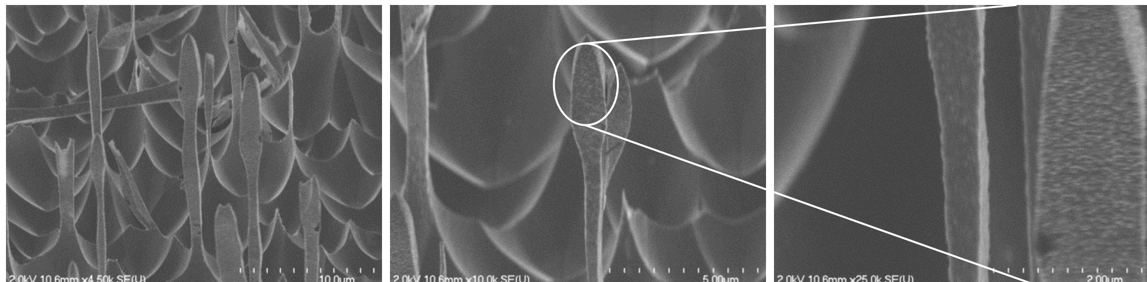


Figure 4.7 (a) SEM image of nano-structure array formed after electrochemical etching, (b) higher magnification of the nano-structure, (c) A close up of the structure tip.

The higher magnification shows that the synthesized structure consists of three distinct regions: an arrow-shaped tip with the diameter of 50 nm, a rod with roughly 18 μm length, and a submicron base. Also it shows that unlike the first approach (see chapter 3) the structure has a rather smooth morphology.

A better insight can be gained on the formation of this morphology through analysing the electrochemical process. Figure 4.8 schematically illustrates the electrochemical etching process.

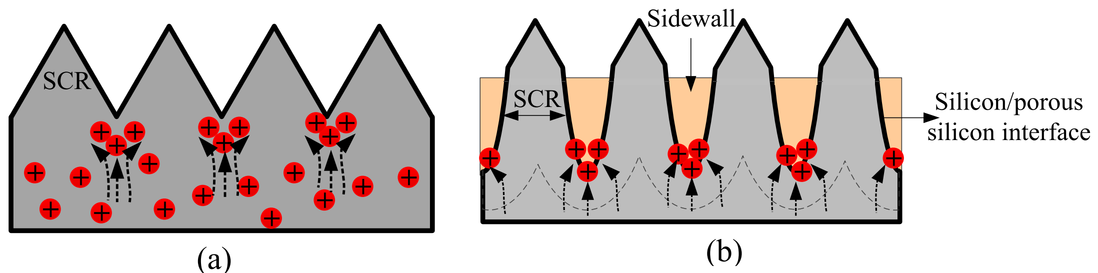


Figure 4.8 A schematic showing the cross section of silicon pyramids and hole distribution as a part of the electrochemical etching process. (a) Distribution of hole carriers at the earlier stage of etching process. (b) Redistribution of hole carriers after pillar diameter reaches to SCR width.

As experimentally were confirmed, Figure 4.8(a) shows the etching process starts from the edges of the pyramids. At this stage, current propagates inward to the faces of the pyramids (dashed arrows in Figure 4.8(a)) and results in formation of the porous structure (pillar and interconnected-walls). As the diameter of these pillars reaches the SCR width, its resistance for transport of hole carriers increases, and holes carrier do not propagate further down the length of the pillars. Therefore, the hole carriers are deviated from these regions and continue to oxidized the silicon/porous silicon interface (dashed arrows in Figure 4.8b). This deviation causes the current at silicon/porous silicon interface to increase. This behaviour, deviation of current, occurs in both porous silicon formation

and transition regimes. Therefore, the etching of the sidewalls and direct formation of silicon nano-structure from electrochemical process cannot be exclusively the result of the current deviation.

The dissolution of sidewalls can be better understood in the light of the analysis of the limiting factors in electrochemical etching process. The electrochemical process is governed by two limiting factors: hole-transport and mass-transport. The hole-transport is dominant when the concentration of fluoride ions are higher than the hole carriers. Accordingly, the porous silicon layer is formed under this condition. However, the mass-transport is dominant when the concentration of fluoride ions is less compared to that of hole carriers as illustrated schematically in Figure 4.9.

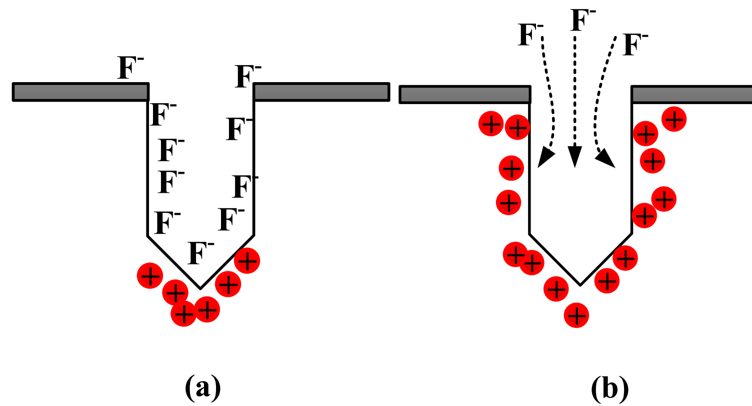
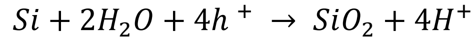


Figure 4.9 Silicon dissolution mechanism (a) hole-transport limitation (b) mass-transport limitation

As pointed out earlier, the propagation of hole carriers is increased at the porous silicon/silicon interface as a result of the current deviation. Additionally, due to lower concentration of fluoride ions, the mass transport-limit condition governs the electrochemical process. As a result of these, electro-polishing is proceeding and tetravalent reactions occur:



$$Si + 2H_2O + 4h^+ \rightarrow SiO_2 + 4H^+$$

$$SiO_2 + 6HF \rightarrow SiF_6^{2-} + 2H_2O + 2h^+$$

As it can be observed from the equation, the SiO_2 is an intermediate product that will be dissolved by HF. Therefore, the structure owes the smoothness of the surface to this chemical reaction between SiO_2 and HF.

4.4 Conclusions

In this chapter, a new lithography-free approach to fabricate free-standing silicon nano-structures was presented. This new and low-cost method utilizes only two steps etching techniques, texturing the silicon surface using an anisotropic etching process, followed by an anodic electrochemical etching.

The effect of anodization etching time on morphology of the structure is presented. This allows a better insight into the formation of silicon nano-structures. It was found that the diameter of the silicon nano-structures strongly depends on SCR width.

The first etching stage plays an important role in the formation of silicon nano-structures. It was observed that it was not possible to develop silicon nano-structure arrays when the pyramids size was smaller than or equal to that corresponding to the SCR width.

The effect of HF concentration in the electrolyte on the creation of silicon nano-structures was also investigated. It was found that, there is an optimal range of HF concentration, 1:4 to 1:6, within which silicon nano-structures can be obtained. The pyramids are etched out completely when the HF concentration is below this range. In contrast, the sidewalls remained un-dissolved as the HF concentration went above this optimal range. It was

observed that within this optimal range, as the HF concentration decreased, the length of the nano-structures decreased as well.

The fabricated nano-strcuture array may have wide applications in microelectronic and optoelectronic devices.

5. Fabrication of n-type silicon nano-structure: Light-induced electro-chemical etching

Development of vertical silicon nano-structure array on p-type silicon wafer by running the electrochemical etching in porous silicon formation regime and transition regime was discussed in chapter 3 and chapter 4 respectively. This chapter is dedicated to investigate the effect of dopant type (n-type) on formation of silicon nano-structure array. The front-side light-induced electrochemical etching is adopted for etching of silicon due to the negligible etching rate of n-type silicon wafer in dark. The effects of light intensity and current density on formation of macro-pore array are studied. The aim of this study is to synthesis a well-aligned macro-pore array with smooth walls, as building blocks for formation of vertical nano-structures.

5.1 Introduction

Porous silicon formation has been widely studied since the first observation of creation of porous layers in fluoride environment using anodization [32]. The porous layer can be used as a sacrificial layer in MEMS and NEMS applications [100] or as a template for fabrication of metallic nano/micro pillars [101, 102]. Depending on these applications, the properties and morphology of porous layer can be modified from nano-porous to macro-porous layers. These modifications can be realized by altering and adjusting various parameters including doping and orientation of silicon substrate, electrolyte (type and concentration) [103, 104], anodic current densities, anodization time, and illumination [103]. Both n-type and p-type macro-pore arrays have been used as building blocks for formation of micro-pillars and nano-structures [23, 24, 105]. The macro-pores need to be well-aligned and have straight and smooth walls to be applicable to fabrication of nanowires. Depending on illumination direction (front-side illumination and back-side illumination), n-type silicon exhibits different morphologies. A smooth and well-aligned pore array without branching can be synthesized by back-side illumination, whereas front-side illumination results in formation of two-layered porous silicon consisting of a macro-pore array, which is partially/fully filled with micro-pore arrays [106]. Considerable amount of research has been so far dedicated to development of porous silicon layer by back-side illumination [64, 76, 79, 91, and 107]. As pointed out in chapter 2, section 2.6, in case of back-side illumination, the thickness of the silicon wafer is a limiting factor. This limiting factor has been reported to be the cause of formation of uneven and non-uniform macro-pores for thick (625μm) and thin (200μm) silicon wafers [108, 109]. This issue can be mitigated by using front-side illumination.

Pore formation can be performed on a polished or patterned silicon surface. The latter one is known as area-selective formation of the pores. This chapter studies the macro-pore formation on textured n-type silicon using front-side light-induced electrochemical process. In addition, a comparison between morphologies of n-type and p-type porous silicon is investigated. In contrast to the conventional technique, the inverted pyramid pattern, the pore formation is performed on pyramid-shap structures, which are highly-packed on silicon surface. The effects of light intensity and current density on formation of macro-pore array are studied.

5.2 Experimental procedure

Several samples of (100) orientation p-type and n-type silicon with the thickness of 625 μm and a resistivity of 10-20 Ω-cm and 1-10 Ω-cm respectively (purchased from Silicon Inc.) were cut and cleaned using the RCA procedure [89].

5.2.1 Textured surface preparation

In order to obtain the almost same surface characteristics for textured silicon surface the p-type and n-type samples are anisotropically etched under different etching parameters. In the case of p-type samples the highly-packed pyramid structures are obtained using 1.5wt.% TMAH and 1.5wt.% IPA, while the TMAH and IPA concentrations are increased to 2 wt.% and 3wt% respectively, for n-type samples. The etching duration and etchant temperature were kept constant at 30 minutes and 90˚C for both n and p-type samples. The samples were then rinsed with DI water and dried in air.

5.2.2 Porous layer preparation

In order to conduct the electrochemical etching, the backside of the samples (the side which is not exposed to electrolyte) was metalized before mounting on the anodization

cell. The sample was mounted on the Teflon cell, and cell was filled with an electrolyte consisting of HF and ethanol. The ratio of the electrolyte was 1:3 for HF and ethanol respectively. The n-type samples were illuminated using Halogen lamp with the aim of generation of the hole carriers. Halogen lamps show a broad spectrum and high intensity; therefore they are suitable for homogeneously illumination of the whole sample. However, the high IR intensity leads to heating up of the sample. Therefore, halogen lamp was located on top of the cell in 13 cm distance from the surface to illuminate the sample from the side that is exposed to the electrolyte (no illumination was used for p-type samples). The 13 cm distance was chosen to avoid heating of the samples.

5.3 Results and discussion

5.3.1 Characterization of textured silicon surface

A typical SEM image of the n-type sample prepared using 2% TMAH and 3% IPA, etched for 30 minutes at 90˚C is shown in Figure 5.1. Table 5.1 presents average surface coverage of three prepared samples, which determined by the image analysis of the SEM images. According to acquired data presented in Table 5.1, the same wet etching conditions results in considerably different surface characteristics for p- and n-type doping, whereas under different wet etching parameters only slight difference is observed in terms of surface coverage. These highly-packed pyramid-shape structures that were fabricated using simple chemical lab equipment (See Figure 3.1) and low-cost materials, lead to an area-selective electrochemical process in the next fabrication step.

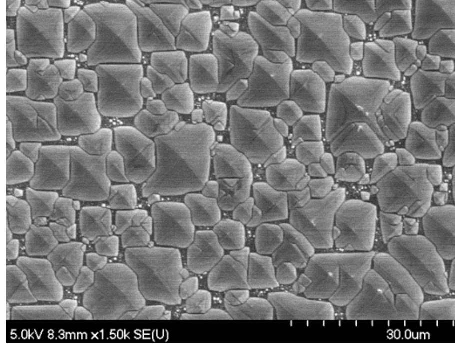


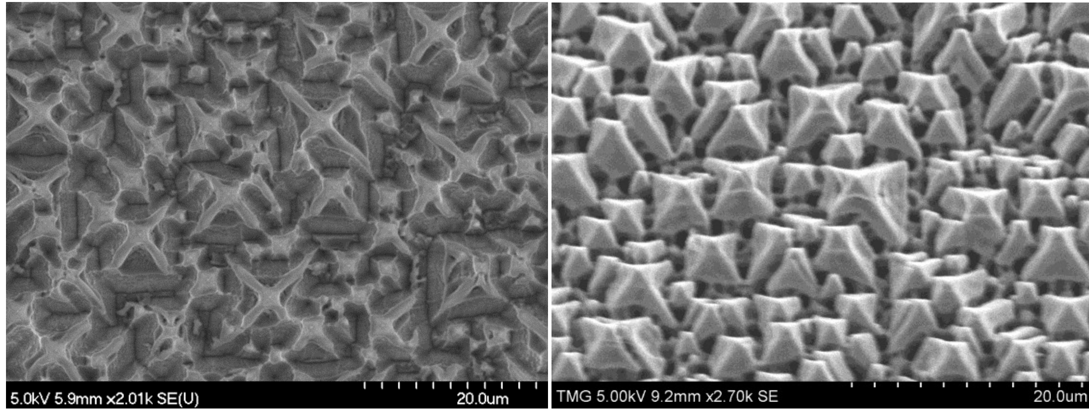
Figure 5.1 SEM image of a typical n-type textured sample prepared using 2% TMAH and 3.5% IPA.

Table 5.1 Morphological characteristics of n-type and p-type textured silicon

	p-type	n-type	n-type
TMAH concentration (wt.%)	1.5	1.5	2
IPA concentration (wt.%)	1.5	1.5	3.5
Average surface coverage of the pyramids (%)	82%	36%	92%

5.3.2 Pores initiation comparison for p- and n-type samples

Figure 5.2(a)-5.2(b) shows the top view of SEM images of n- and p-type textured samples etched for duration of 3 minutes anodization at 80 mA, respectively. As it can be observed in both cases, the pores formations are initiated from the edges of the pyramids and the tip of the pyramids are passivated against etching. This selectively etched behavior of textured samples can be explained by the etching profile of the concave structure presented in Figure 5.3.



(a) (b)

Figure 5.2 the top view of silicon samples after 3 minutes anodization under 80 mA applied current. (a) p-type (b) n-type

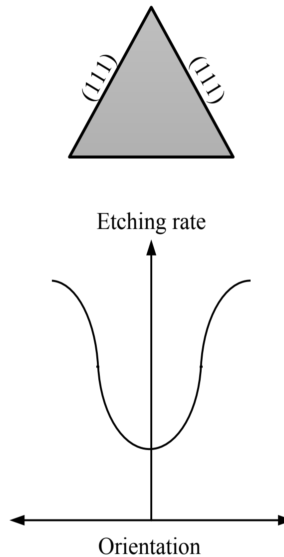


Figure 5.3 Etching profile of a pyramid-shaped structure [110]

As the etching profile shows (Figure 5.3), the tip of the pyramid, where the two (111) planes meet each other has the lowest etching rate, whereas the intersection of (100) and (111) planes has a higher etching rate [110].

A comparison of Figure 5.2(a) and 5.2(b) shows that, despite the same initiation etching points for n-type and p-type textured samples after anodization, there is a significant difference on characteristics of the etched areas. Figure 5.2(a) shows the SEM image of p-type textured sample after anodization. As it can be observed, the edges of the pyramid

are etched smoothly inward to four (111) faces of the pyramid compared to Figure 5.2(b). On the other hand, the SEM image of n-type sample, Figure 5.2(b), shows that unlike the p-type samples the intersections of the edges of the pyramids are covered by micro-pore structures.

Although, these observations confirm the area-selective electrochemical etching for both p- and n-type samples on textured silicon surface but the electrochemical etching process on p-type samples results in anisotropic etching behavior, whereas n-type samples are isotropically etched.

5.3.3 Development of macro-pore arrays

The cross-sectional SEM images of anodized n-type and p-type samples are shown in Figure 5.4(a)-5.4(b) respectively. Interestingly, despite the applying of same anodization conditions (except the light for n-type sample) on the both n-type and p-type samples, the morphologies of the anodized samples are not alike. As it can be observed from Figure 5.4(a), an uneven macro-pore array with various depths is created on n-type textured sample. Moreover, smaller size pores have been formed inside each of these macro-pores. On the other hand, anodization of p-type textured sample resulted in formation of a rather uniform and even macro-pore array as shown in Figure 5.4(b).

These observations can be explained in the light of the fact that electrochemical etching process is governed through two important factors: hole carrier concentration and rate of hole carrier supplying. The latter one is controlled by the applied bias. In the case of p-type silicon, holes are majority carriers and therefore, the rate of hole supplying determines the morphology of the pores. However, in the case of an n-type due to the insufficient hole carriers the morphology of pores depends on both factors.

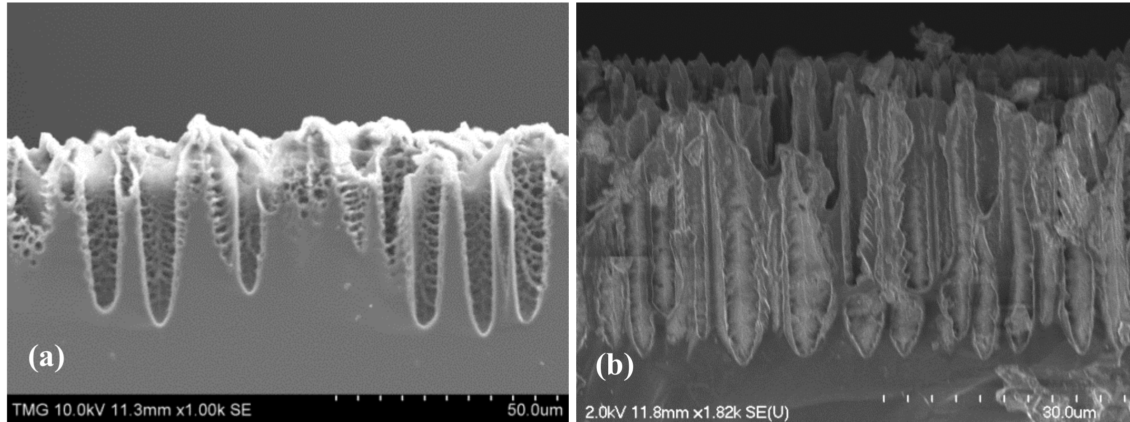
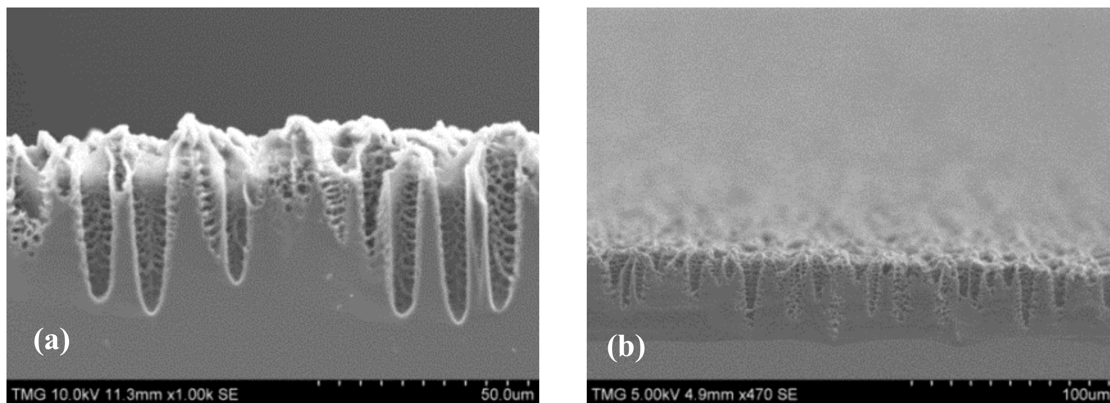


Figure 5.4 The macro-pore formation prepared using 80 mA anodic current for duration of 30 minutes. (a) n- type and (b) p-type samples

These experimental observations of n-type and p-type sample under 80 mA anodic current, hints towards the possibility of hole carrier concentration being the main reason for formation of uneven and partially filled macro-pores on n-type samples. Based on this speculation, the light intensity is increased in order to increase the hole carrier concentration, with the intention of eliminating the formation of micro-pores inside n-type macro-pore array.



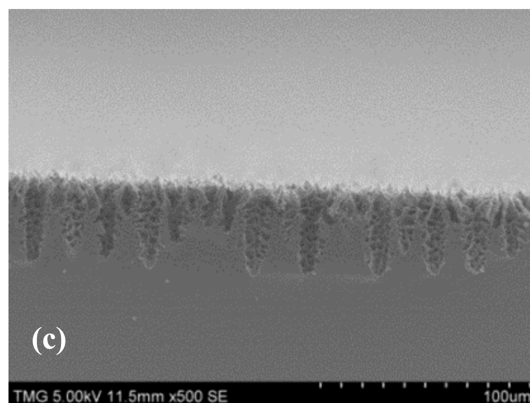


Figure 5.5 Cross-section of the n-type samples anodizied under various light power. (a) 50W, (b) 150W, (c) 300W

The light power was increased further from 50 to 150 and 300 W, in order to increase the generation of holes. Figure 5.5(a)-5.5(c) show the cross-sectional SEM images of porous layer etched under light intensities of 50, 150, and 300 W, respectively. These observations show that increasing the light intensity produced structures with higher porosity in such a way that macro-pores were also filled with micro-pores. Negligible changes were observed in morphology of the pores as the intensity of light was increased further to 300 W. This can be explained by Arita et al., [111] findings. According to their results, the effect of light intensity is almost diminished at higher applied anodic current however, this effect is more pronounced at lower anodic current.

As for experimental results shown in Figure 5.5, the high anodic current (80 mA) can be considered as a large reverse bias applied to n-type samples, in which the silicon-electrolyte interface acts as n-p junction. This large reverse bias results in increasing electron-hole pair generation, which in turn leads to avalanche breakdown and hence formation of filled macro-pores.

Accordingly, in order to find the suitable anodic current for formation of even and unifrom macro-pore arrays various current (10, 30, 40, 50, 60 mA) are applied to silicon

samples. Figure 5.6 depicts the SEM image of the n-type sample under 10 mA of anodic current. As can be seen in this figure, the body of the pyramids is mainly filled with micro-pores, and no vertical progress of the pores is observed. This observation is deemed to be the result of the penetration of hole carriers into the body of the pyramids. This penetration of hole carriers is explained by development of relatively small electric field, which is not capable of concentrating the generated hole carriers at the edges of the pyramids.

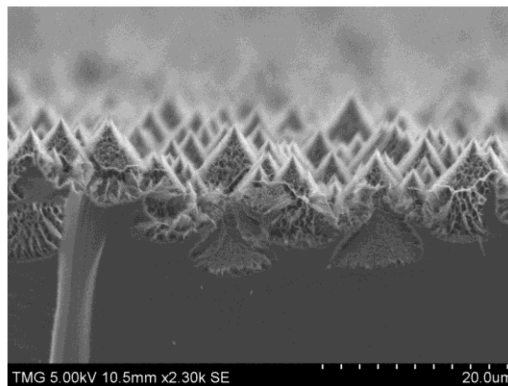


Figure 5.6 Porous silicon formation under 10 mA anodic current (150W).

Figures 5.7(a)-5.7(d) show the top-view SEM images of the porous silicon layer produced under various anodic current. It was observed that by increasing the anodic current to 30 mA the etching was progressed inward to the four (111) faces of the pyramids as shown in Figure 5.7(a). The etching rate of the four faces of the pyramids was increased by increasing the anodic current beyond 30 mA, which results in formation of pores with larger diameters. Figure 5.7(c) illustrates that the four faces of pyramid are completely etched at 50 mA however, the tip of the pyramid and structure underneath were preserved against etching. As evident from Figure 5.7(d), further increasing of the anodic current to 60 mA resulted in formation of larger pores.

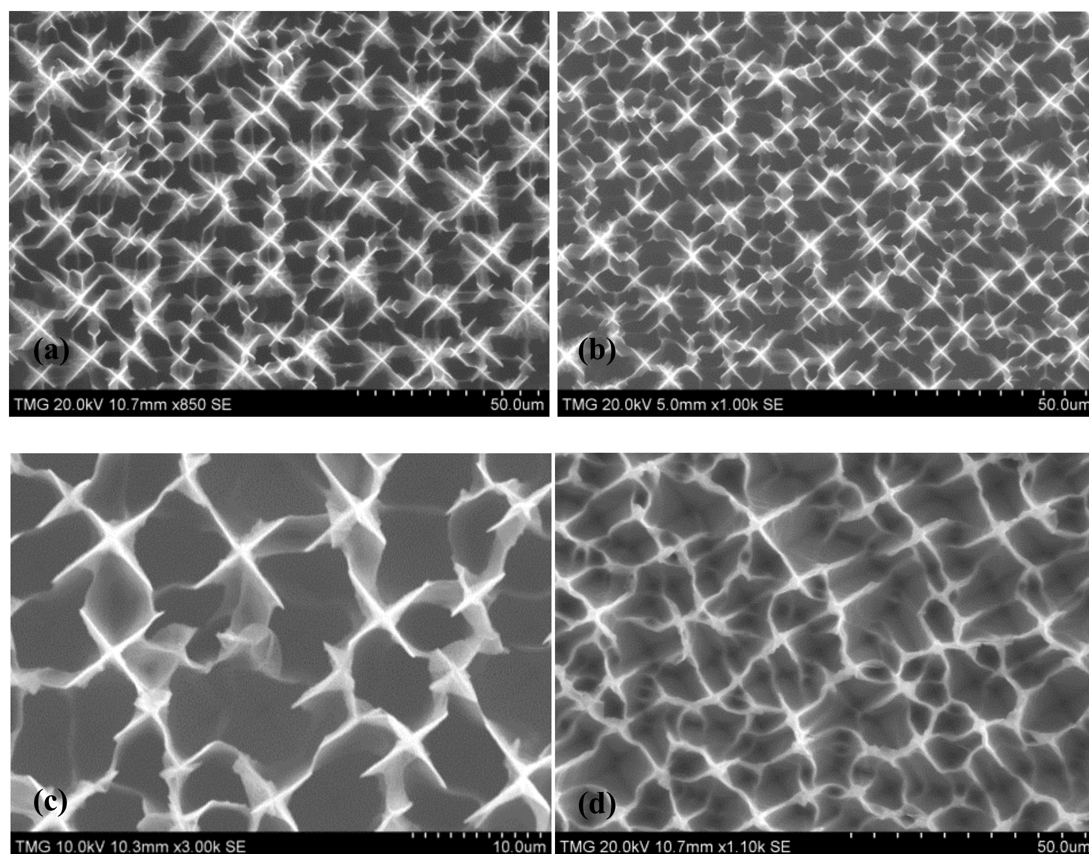


Figure 5.7 Macro-pore arrays created at various applied current and illuminated by 150W source (a) 30mA, (b) 40 mA, (c)50mA, and (d)60 mA

Figure 5.8(a)-5.8(d) show the corresponding cross-sectional view of the same samples shown in Figure 5.7(a)-5.7(d) respectively.

As it can be observed, the etching was progressed vertically. However, the macro-pores not only are not well aligned but are also partially filled with micro-pores. The formation of macro-pore array was improved by further increasing of anodic current to 50 mA. According to Figure 5.8(c) no micro-pores formed inside the macro-pores.

As shown in Figure 5.8(d) by further increasing of anodic current to 60 mA, thickness of macro-pore is decreased while pore diameter is increased. This result can be attributed to the relatively higher lateral etching rate with respect to vertical etching rate. The higher lateral etching rate can be explained by the fact that the anodization condition switches

from carrier-limit conditions to mass-limit conditions as the supplying rate of holes is increased for a constant number of fluoride ions in electrolyte. As a result, the etching of the pore walls occurs as the anodization process become mass-limited. As it was shown in Figure 5.5(b) an uneven and filled macro-pores were developed at 80 mA anodic current.

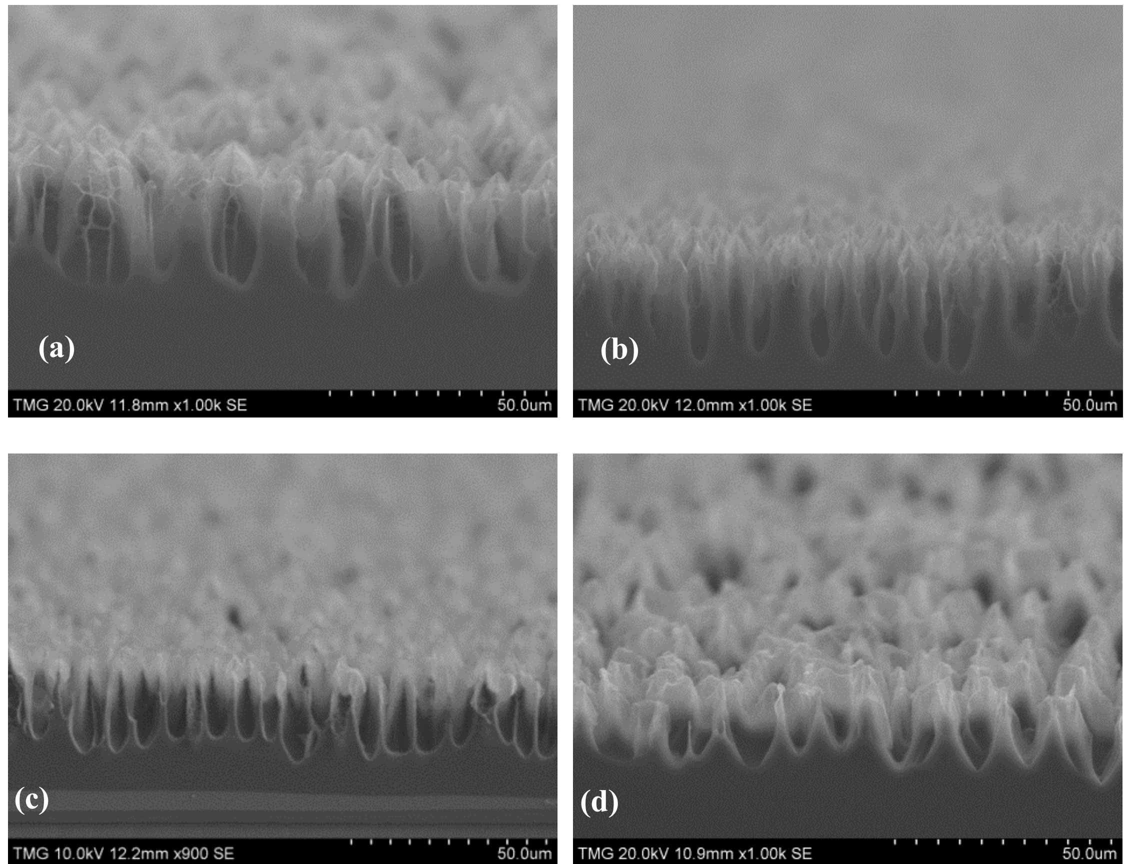


Figure 5.8(a)-5.8(b) the corresponding cross sectional view of the same samples shown in Figures 5.7(a)-5.7(d) respectively.

5.3.4 Macro-pore array as building blocks for formation of nano-structure

The macro-pore array developed on n- and p-type silicon is then used as building blocks for formation of the 3-D nano-structures. The macro-pore array is transformed into nano-structures using wet-anisotropic etching. The porous silicon layer was washed with DI

water and dried in air, and then were immersed into diluted NaOH solution of 0.2 molarity for duration of 5 minutes. Two n- type porous silicon layers that were etched for duration of 5 and 30 minutes were treated with NaOH. Figure 5.9(a)-5.9(b) show the SEM images of samples after NaOH treatment. As it is shown in Figure 5.9(a) an array of Mashroom shape silicon micro-structures has been obtained. These micro-structures correspond with the porous silicon layer that was created under electrochemical etching condition of 80 mA and light intensity of 50 W. Figure 5.9(b) shows an Eiffel-tower-shape nano-structure array synthesized, using porous silicon layer etched under electrochemical conditions of 50 mA and light intensity of 150 W. Three distinct regions can be defined in this structure: a nano-tip with diameter of 100 nm and length of 500 nm, a nano-layered structure, and a sub-micron base. The total length of the synthesized nano-structure is roughly 5 μm. The length of the nano-structure is shorter than the thickness of the macro-pore array shown in Figure 5.8(c). This could be due to the fact that thickness of pore walls is thinner near the tip. Therefore, the thinner walls were etched during the NaOH processing.

Figure 5.10 shows the SEM image of arrow-shaped nano-structures created as a result of NaOH treatment of p-type porous silicon layer. Inset shows the higher magnification of the nano-structures. It can be observed that the tip of the pyramids was well preserved during NaOH treatment. The structure also shows layered morphologies especially in the rod regions. The observed layered morphologies on n- and p- type 3-D structures can be attributed to anisotropic behavior of NaOH processing.

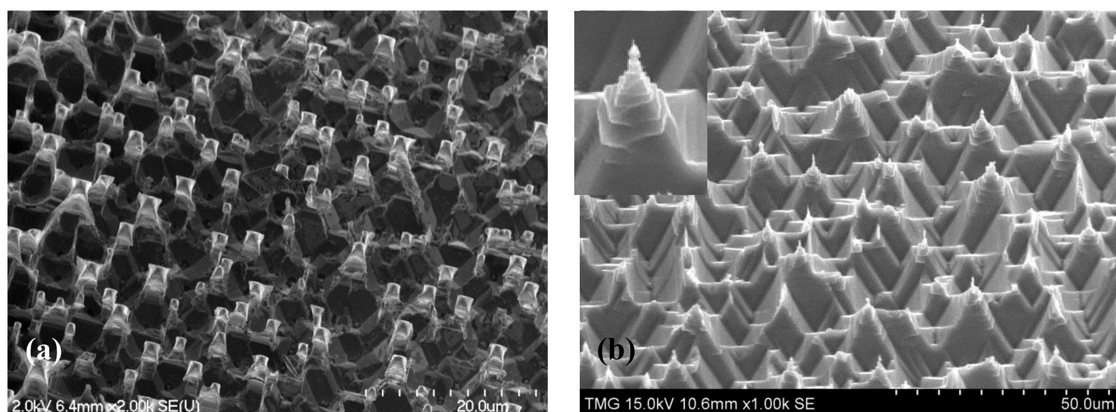


Figure 5.9(a)-5.9(b) The micro/nano structures develpoed by anisotorpic etching in NaOH using two different porous silicon layers as building blocks. (a) mushroom-like micro-structure. (b) Eiffel-tower-like nano-structure created using porous silicon layer shown in Figure 5.8 (c)

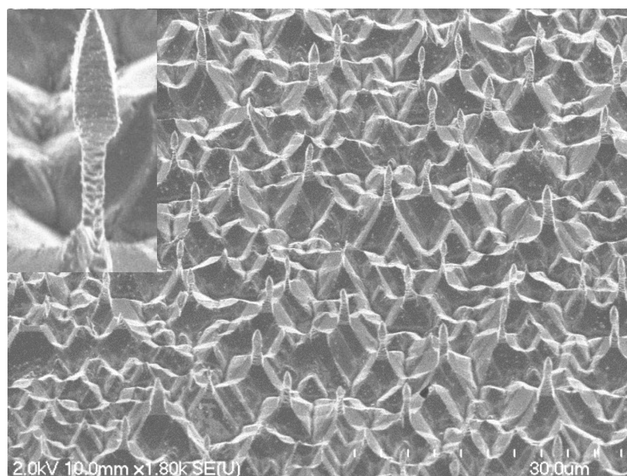


Figure 5.10 The arrow-liked micro/nano structures developed by anisotorpic etching in NaOH using p-type macro-pore array

5.4 Conclusions

An area-selective electrochemical etching was conducted on pyramid-shaped silicon structures that were highly-packed on the surface. The effect of dopant type (Boron and Phosphorous), anodic current and light intensity on formation of macro-pore array were studied. Even macro-pore array with smooth walls were obtained on both p-type and n-type samples and then were used as building blocks for formation of 3-D structures.

An array of micro/nano structure has been successfully synthesized on both n-type and p-type samples by NaOH treatment of macro-pore arrays. An array of Eiffel-tower-shape silicon nano-structures was synthesized on n-type macro-pore array. The nano-structure has a unique layered morphology. This 3-D structure consists of three distinct regions: a nano-tip with diameter of 100 nm, a nano-layered Eiffel-tower-shape structure with a length of 5 μm diameter and a sub-micron base. NaOH treatment of p-type macro-pore arrays resulted in formation of an array of arrow-like structures.

6. Conclusions, contributions and suggestions for further research

The main aim of this work was to study and introduce novel and low-cost techniques for fabrication of silicon nano-strcuture array as a promising candidate in MEMS/NEMS, solar cell, energy storage and sensing applications.

A new low-cost top-down multi-stage approach was introduced for the fabrication of arrays of silicon nano-structure. The anisotropic etching and electrochemical etching were implemented as two main tools for the purpose of nano-structure array growth. The growth mechanism of such structure was investigated and an insight of synthesis process was obtained. The new technique allows controlling the density and characteristics of synthesized structures. The synthesized structure possessed a unique layered morphology.

The second fabrication technique consists of two steps and allowed modifying the morphology of the synthesized structure. The layered morphology with rough surface that resulted using first approach tailored to a solid morphology with a smooth surface by using the second new technique.

The applicability of new technique on n-type silicon was studied. The light induced electrochemical etching method was used for

synthesis of array of silicon nano-structure on n-type silicon. An array of silicon nano-structure was successfully synthesized. The effect of different doping, n and p-type, on the fabrication process was investigated.

The contributions of this work are listed below in order of their progression through this thesis.

6.1 Contributions

The contributions of this research are listed below:

- Two novel low-cost, multi-stage methods for fabrication of array of silicon nano-strcuture is introduced.
- Silicon nano-strcuture array with a unique morphology was successfully synthesized.
- The effect of wet chemical etching parameter, IPA, on pyramid surface coverage was studied.
- The effect of electrochemical parameters, including anodic current, etching time, and HF concentration were studied and were optimized for formation of an even and uniform pore array with thin sidewalls.
- These novel approaches allow for controlling the characteristics of the synthesized structure, including length and diameter.
- The effect of pyramid surface coverage and pyramid size uniformity on development of silicon nano-structure were studied.
- A light-induced method, photo-electrochemical etching, was used for formation of silicon nano-structure on n-type samples.
- The effect of photo-electrochemical parameters, including light intensity and anodic current on formation of macro-pore array were studied.
- A well-aligned and uniform macro-pore array with smooth walls was fabricated using front-side illumination.

6.2 Future work

This work provided the fundamental steps toward fabrication of self-mask and lithography-free, of silicon nano-structure on both p-type and n-type silicon. A significant portion of this work may provide a good background for further advanced studies on (photo)electrochemical etching of silicon.

The results of this work may be extended and investigated in following topics:

- Low-doped silicon wafers with resistivity of 10-20 Ω.cm were under study in this research. The effect of wafer resistivity on formation of silicon nano-structure array can be extensively studied.
- Further work needs to be done on photo-electrochemical etching of the n-type sample. The effect of different light source, determination of an optimized wavelength and their influence on formation of desired macro-pore array can be studied. Also the effect of back-side illumination on development of macro-pore array and following formation of silicon nano-structure can be investigated.
- Implementing the silicon nano-structure in microelectronics and optoelectronics applications. The field emission and optical characteristics of the silicon nano-structure can be studied.
- The potential application of silicon nano-structure array for hydrogen storage can be investigated.

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