Computer Aided Design Approaches for Certain Classes of Low-Noise Amplifiers

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A Thesis

in

The Department

of

Electrical and Computer Engineering

Presented in Partial Fulfillment of the Requirements

for the Degree of Master of Applied Science (Electrical Engineering) at

Concordia University

Montreal, Quebec, Canada

August 2007

Your file Votre référence
ISBN: 978-0-494-34646-4
Our file Notre référence
ISBN: 978-0-494-34646-4

Abstract

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Low-noise amplifiers (LNAs) are critical components to any modern electronic communications system. LNAs are usually placed at the beginning of a multistage system and are designed with high gain to suppress the noise contributions of subsequent stages. Aside from noise and gain, other performance criteria such as, distortion effects, power consumption, and circuit size have varying degrees of importance based on the LNA's destined application. It is the way in which the LNA is designed (*i.e.* topology selection, design methodology, fine-tuning, etc.) that will determine how well the LNA performs. Currently, there is no unique or systematic approach for the design of these relatively complex circuits. Hence, the development of CAD tools for LNA design is an attractive alternative to traditional pen and paper approaches.

This thesis can be divided into two main parts; computer aided LNA design from an analog perspective and computer aided LNA design from a RF/microwave perspective. Analog engineers tend to work with traditional electronic components (*e.g.* transistors, resistors, inductors, capacitors, etc.). In this work, a computer aided approach is devised which performs appropriate topology selection, design, and fine-tuning.

In the RF/microwave world, designers tend to work at higher operating frequencies, and thus use microwave oriented components such as micro-strips and

waveguides. Given the *S*-parameters for a specified transistor, the proposed approach finds an input/output reflection coefficient that maximizes the LNA gain for a specified noise-figure. The proposed CAD approach exploits "constrained line search optimization" to increase the accuracy of the LNA circuit and to reduce the time needed in the design process.

The CAD approaches are illustrated via practical LNA examples. The resulting LNA designs are shown to have improved performance *w.r.t* the user-specifications.

Acknowledgements

I would like to express my sincere gratitude toward my supervisor Dr. Vijay Devabhaktuni for his tireless efforts in the advancement of my education, career and life goals. His continued guidance and encouragement serves as a catalyst to achieving my ambitions.

I would also like to express genuine appreciation for the expert advice and council of Dr. Rabin Raut. His extensive technical knowledge in analog design served as a backbone to this work. Additionally, this work would not have been possible without the efforts and support of my colleagues in the CAD laboratory at Concordia University. A special mention must be made for Arash Kashi, Navid Arbabi, Li Zhu, Kaustubha Mendhurwar, and Joshua Frankel for their continued support and friendship.

Lastly I'd like to extend my heartfelt appreciation to my friends and family for their ongoing guidance, support, and understanding.

To my loving parents
Mrs. Elayne & Mr. Himadri Roy

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List of Symbols and Abbreviations

B	Bandwidth
BJT	Bipolar junction transistor
CAD	Computer aided design
C_F	Constant noise-figure circle center
C_{GS}	Drain-source capacitance
C_L	Constant gain (load) circle center
C_S	Constant gain (source) circle center
f	Frequency
F	Noise factor
FET	Field effect transistor
F_{tot}	Overall noise factor of a cascaded system
G	Power gain
G_A	Available power gain
Γ_{in}	Input reflection coefficient
Γ_L	Load reflection coefficient
Γ_{opt}	Optimal source reflection coefficient
Γ_{out}	Output reflection coefficient
Γ_S	Source reflection coefficient
g_{d0}	Drain-source conductance

g_m	Transconductance
G_T	Transducer power gain
G_{TU}	Unilateral transducer power gain
IIP_3	Third order intercept point (referenced to the input)
k	Boltzman constant
L	Transistor length
L_{min}	Minimum transistor length
LNA	Low noise amplifier
MOS	Metal oxide semiconductor
N	Noise-figure parameter
NF	Noise-figure
NF_D	Desired noise-figure
OIP_3	Third order intercept point (referenced to the output)
P_1	1 dB compression point
P_3	Third order intercept point
P_{avn}	Available power from the network
P_{avs}	Available power from the source
P_L	Power dissipated in the load
P_n	Available power
q	Electronic charge
Q	Inductor quality factor
RF	Radio frequency

R_F	Constant noise-figure circle radius
R_L	Constant gain (load) circle radius
rms	Root mean squared
R_N	Equivalent transistor noise resistance
R_S	Constant gain (source) circle radius
SDE	Sequence of design equations
SNR_i	Input signal to noise ratio
SNR_o	Output signal to noise ratio
T	Temperature
T-SDE	Topology versus sequence of design equations
U	Unilateral figure of merit
V_{DS}	Drain-source voltage
W	Transistor width
Z_L	Load impedance
Z_S	Source impedance

Chapter 1

Introduction

1.1 Low-Noise Amplifiers

Amplifiers are an integral component of modern electronic circuits and systems. Specifically, low-noise amplifiers (LNAs) occupy an important subset of amplifier applications in which noise reduction is paramount. In high-frequency high-speed circuits/systems, noise can be highly destructive to signal integrity [1]. As such, keeping noise at a minimum is key to the effective functionality of sensitive electronic systems including, radio-frequency (RF) and microwave sub-circuits, wireless transceivers, and so forth. In fact, LNAs can be found in most, if not all, wireless communications systems.

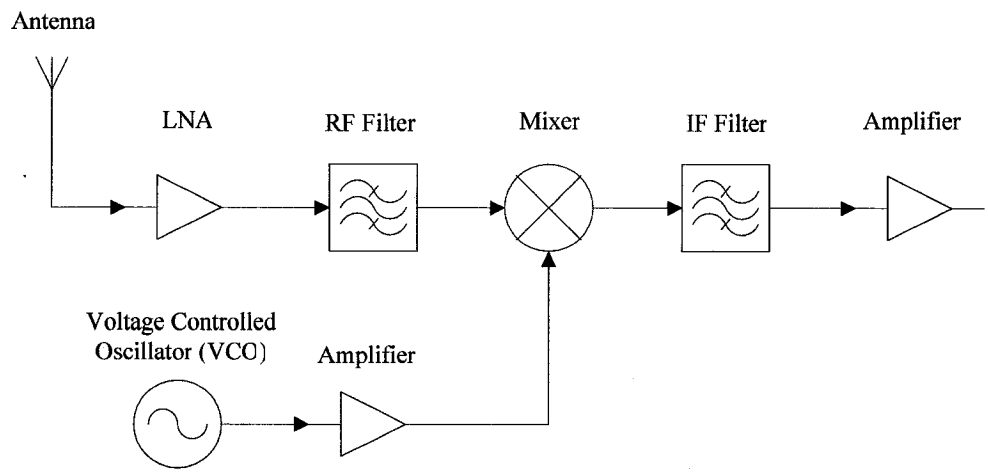


Figure 1.1 Block diagram of a typical super heterodyne receiver.

Because of the way noise propagates through a system (to be discussed in detail in Chapter 2), LNAs are placed at the front-end of wireless receiver circuits to minimize the overall noise of the system. For instance, in a typical super heterodyne receiver (as shown in Fig. 1.1) the LNA is the first component after the antenna.

When designing an LNA, several performance metrics (to be discussed in detail in Chapter 2) are to be considered, such as noise-figure, gain, power consumption, gain compression, linearity, minimum voltage supply, etc. Additionally, these metrics are interrelated, thereby requiring effective LNA designs to have trade-offs between them. Deciding which trade-offs to make is often a difficult and confusing task. It is the desired LNA application that will help determine the relative importance of each metric. For example, in portable applications, circuit size, and power consumption are a primary concern while in a simpler radio receiver, noise-figure takes precedence. Considering the

numerous constraints, available topologies, and varied specifications, formulating LNA design into a single, compact optimization routine and forcing it to converge is not practical. An alternative computer aided approach is one possible solution.

As a side note, it is important to mention that the performance of the LNA has the potential to affect several important specifications for the overall system, such as dynamic range, noise-figure, power consumption, circuit size, etc. It is therefore important that the LNA be designed with utmost care and attention.

1.2 Computer Aided Design

In the past few of decades, computer aided design (CAD), or design automation, of electronic components has greatly progressed. This is in large part due to an increase in the overall design complexity of modern electronic circuits and systems. Further, the sheer number of topologies available, the large amount of design procedures, and the many possible trade-offs between metrics has made manual (traditional) design prohibitively time consuming. Manual design processes have become, and are increasingly becoming, obsolete. At a certain point, the number of parameters that can be taken into account through a manual design process becomes limited. This can severely hamper the design process. CAD design tools have evolved and aim to make the design process simpler, faster, and more accurate.

For digital IC designers, a plethora of CAD tools, *e.g. Quartus* II, *Synopsis* etc., are available. These tools not only help in the design of a digital circuit, but also facilitate optimization of the circuit for improved performance in terms of power, size, timing, etc.

From a user's perspective, these CAD tools begin with the desired response and automatically generate the digital logic required to create the circuit. In the analog world, CAD tools are not nearly as convenient or comprehensive. Important aspects of design, such as topology selection, related design methodology, and circuit fine-tuning, demand a high-level of user-expertise.

1.3 Objectives and Motivation

This thesis is primarily motivated by the desire to reduce the complexity involved in the design of an LNA, as well as to augment the current state of available design automation tools for analog circuit designers. Therefore, the main objective of this thesis is to reduce the demand on the expertise of an engineer who is required to design an effective LNA (based on CMOS technology). From an industry stand-point, this work is practical as it means the accumulated expertises required in the design flow of a particular circuit remains with the company even when employees leave to pursue other personal career interests.

1.4 Thesis Outline

In essence, this thesis provides two new CAD approaches/tools for LNA design; one from an analog and one from an RF/microwave perspective.

Chapter 2 contains background LNA theory that is relevant to both the analog and RF/microwave perspectives. Certain electronic phenomenons pertinent to LNAs are explored and relevant metrics are discussed. These metrics include noise-figure, third-

order intercept point, gain compression, *S*-parameters, power consumption, circuit size, and voltage gain.

Chapter 3 covers LNA design from an analog perspective. Here, several LNA topologies, including the single-stage and multi-stage varieties, are explored. Related design methodologies are also reviewed. The proposed CAD approach to LNA design from an analog perspective is then presented. The chapter concludes with the application of the CAD approach to several practical design scenarios.

Chapter 4 covers LNA design from an RF/microwave perspective. The chapter begins with additional background theory that is pertinent to RF/microwave LNA design. The concept of constant gain circles and constant noise-figure circles on a Smith chart are discussed. The proposed approach to LNA design is then described for the unilateral and bilateral cases. Finally, two practical examples are presented to showcase the usefulness of the approach.

Chapter 5 contains a discussion on the thesis' contributions as well as possible future works. Finally, an Appendix for added reader comprehension is included.

Chapter 2

Theoretical Overview of LNAs

As previously mentioned, an LNA is placed at the beginning of a multi-stage system and is designed such that its gain will help suppress the noise contributions of subsequent stages. To appreciate this concept, all pertinent LNA metrics need to be discussed and analyzed. Noise, gain, linearity, etc., all play a role in determining how well an LNA performs. In this chapter, the theoretical background for LNAs is described in detail. Each LNA metric is examined to understand how it affects the overall LNA design.

Predominant among the LNA metrics is noise. The kinds of noise that exist as well as how noise propagates through a system is discussed. Distortion effects on LNAs,

as well as different types of gain, are other important metrics to be considered. It is only when the LNA metrics are fully understood/appreciated, that maximizing or minimizing them for optimal LNA performance becomes possible.

2.1 Noise

2.1.1 Thermal Noise

As described in [2] and [3], noise in resistors is a consequence of Brownian motion (*i.e.* a mathematical model used to describe random motion). "Thermally agitated charge carriers in a conductor constitute a randomly varying current that gives rise to a random voltage via Ohm's law." Because thermal noise is random and does not depend on frequency (at least up until the terahertz range), it is considered as white noise (*i.e.* it has a constant power spectral density throughout the frequency spectrum). Fig. 2.1 shows a standard resistor of value R_{noisy}. At temperature T (in degrees Kelvin), the charge carriers (in this case electrons) are thermally agitated in a random manner. This motion creates small random voltage fluctuations across the terminals. Because the motion is Brownian in nature, over time the

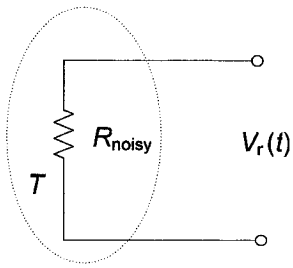


Figure 2.1 Circuit schematic illustrating a standard noisy resistor.

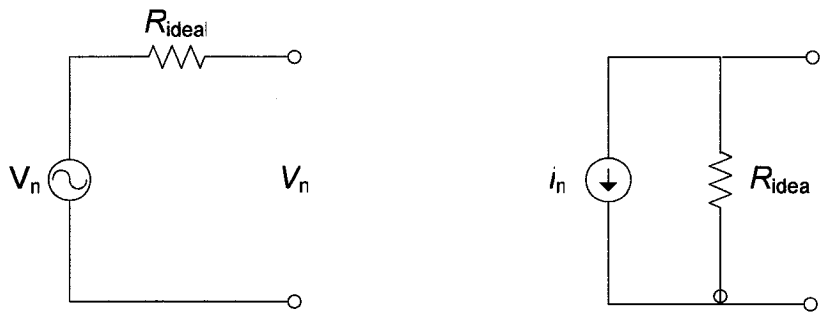


Figure 2.2 (a) Thevenin and (b) Norton equivalent noise models.

mean value of the voltage is zero. On the other hand, the root-mean squared (rms) voltage over a specific frequency bandwidth B can be expressed as

$$V_n = \sqrt{4kTBR} \ , \tag{2.1}$$

where k = 1.380x10-23 J/°K is the Boltzman constant. The rms Norton equivalent noisy current can be expressed as,

$$i_n = \sqrt{\frac{4kTB}{R}} \ . \tag{2.2}$$

Equation 2.1 is known as the Rayleigh-Jeans approximation. Fig. 2.2 shows the Thevenin/Norton equivalent circuits, where the noisy resistor is replaced with a noisy voltage/current source and an ideal resistor, R_{ideal}. The available noise power, P_n (*i.e.* the maximum power that can be delivered from the noisy source to a load), is then,

$$P_n = \left(\frac{V_n}{2}\right)^2 \frac{1}{R} = \frac{V_n^{\,2}}{4R} = kTB \tag{2.3}$$

or

$$P_n = \left(\frac{i_n}{2}\right)^2 R = i_n^{\,2} \frac{R}{4} = kTB\,. \tag{2.4}$$

The above discussion relates thermal noise to resistors. The thermal noise contributions of other devices such as transistors and diodes are analyzed by making analytical comparisons with resistors.

Both junction and metal oxide substrate semi-conductor transistors can be considered as voltage-controlled resistors. As such, depending on the mode of operation, MOSFETs can contribute significant amounts of noise in on themselves. In [4], two main sources of thermal noise are discussed *w.r.t.* MOS devices; drain current noise and gate noise.

In [4], the drain current noise in field effect transistors (FETs) is derived as,

$$\bar{i}_{nd} = \sqrt{4kT\gamma g_{d0} B}\,, \tag{2.5}$$

where g_{d0} is the drain-source conductance when $V_{DS} = 0$, and $\gamma = 1$ when $V_{DS} = 0$. In long-channel devices, $\gamma = 2/3$ in the saturation mode of operation. In short channel devices, experimentations have revealed that the value of γ can be much higher.

In [5], a circuit model is developed to account for noisy gate current. The actual noise current is derived as,

$$\bar{i}_{ng} = \sqrt{4kT\delta B \frac{\omega^2 C_{GS}^{\ 2}}{5g_{d0}}}, \tag{2.6}$$

where C_{GS} is the gate-source capacitance, and δ is approximately 4/3 in long channel devices, and unknown in short channel devices (often estimated as 2γ). As is evident, equation (2.6) is frequency dependant (*i.e.* not white noise). Another interpretation of the gate noise is presented in [6][7]. Here, a high quality factor (Q) is assumed and the equivalent noisy voltage source is derived as,

$$\bar{v}_{ng} = \sqrt{4kT\delta B \frac{1}{5g_{d0}}}. \tag{2.7}$$

2.1.2 Shot Noise

Shot noise or Schottky noise is first described in [8]. Shot noise arises when there is a direct current flow as well as a potential barrier which electrons (charge carriers) need to overcome. Hence, shot noise occurs only in devices that have a potential barrier (*i.e.* non-linear devices). For instance, in bipolar junction transistors (BJT), both the base and collector currents will be sources of shot noise. In the case of MOS devices, only the gate current will provide a source for shot noise. Since the gate current is usually quite

small, shot noise does not tend to affect MOS devices. Shot noise can be described in terms of the rms noisy current as,

$$\bar{i}_n = \sqrt{2qI_{DC}B}\,, \tag{2.8}$$

where q = $1.6\text{x}10^{-19}$ Coulombs is the electronic charge, and I_{DC} is the DC current in amperes.

2.1.3 Flicker Noise

Flicker noise, also known as pink or $1/f$ noise, is inversely related to frequency. It is caused by the random trapping and release of charge carriers by impurities or defects on the surface in which the charge travels. Since MOSFETs are "surface" devices, they tend to exhibit much more flicker noise than BJTs. The rms flicker drain noise current is derived as,

$$\bar{i}_n = \sqrt{\frac{K}{f}\frac{g_m^{\,2}}{WLC_{ox}^2}B}\,, \tag{2.9}$$

where g_m is the transistor transconductance, C_{ox} is the oxide capacitance , W and L are the lengths and widths of the gate respectively, and K is a device-specific constant. From equation (2.9) it is clear that the flicker noise is inversely proportional to frequency. Hence, as the frequency of operation increases, the flicker noise is reduced. The flicker noise can be further reduced by increasing the gate area (*i.e.* gate area =WL). At GHz frequencies, the flicker noise can usually be ignored.

2.1.4 Noise-Figure

The noise factor (F) can be defined as the loss (inverse of gain) in signal-to-noise power ratio between the input and output of a circuit or system, *i.e.*

$$F = \frac{Si/Ni}{So/No} = \frac{SNR_i}{SNR_o} \geq 1, \tag{2.10}$$

where S_i, S_o, N_i, and N_o represent the signal powers at the input and output, and the noise powers at the input and output respectively. In (2.10), SNR_i and SNR_o are the signal-to-

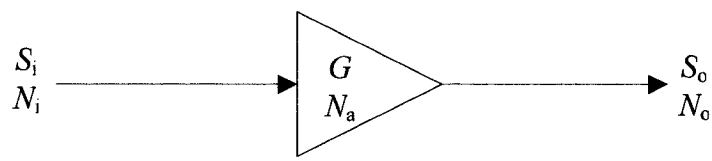


Figure 2.3 Block diagram of a typically electronic amplifier.

noise power ratios at the input and output respectively. The noise-figure, NF, of a system is simply the representation of F in decibels. Hence,

$$NF = 10\log(F) = SNR_i(\text{in dB}) - SNR_o(\text{in dB}). \tag{2.11}$$

The most ideal situation is when $F = 1$ and $NF = 0$ dB. In practice however, this is not feasible. Consider Fig. 2.3 which depicts a block diagram of a typical electronic circuit (in this case an amplifier) with power gain G and available noise power N_a. In this case the following equations hold true;

$$S_o = GS_i \tag{2.12}$$

and

$$N_o = GN_i + N_a. \tag{2.13}$$

Substituting equations (2.12) and (2.13) into equation (2.10) results in a very popular representation of the noise factor, *i.e.*

$$F = \frac{GN_i + N_a}{GN_i} = 1 + \frac{N_a}{GN_i}. \tag{2.14}$$

2.1.5 Noise Factor of a Cascaded System

Consider a system of n cascaded electronic components (amplifiers, filters, *etc.*) as shown in Fig. 2.4.

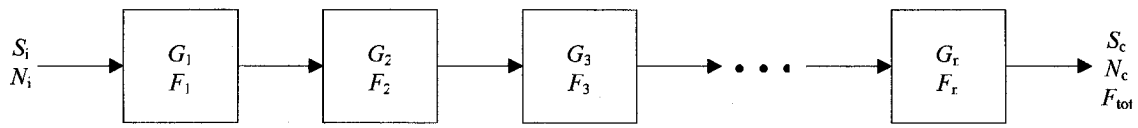


Figure 2.4 Noise-figure of a system of n cascaded electronic components.

The overall noise factor, F_{tot}, of the cascaded system can be derived as [9],

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 G_3 \cdots G_n}. \tag{2.15}$$

From (2.15), it is clear that the first stage plays a dominant role in the overall noise factor (and by association, the overall *NF*). By maximizing G_1 and by minimizing F_1, the total *NF* of the system can be reduced. For this reason, LNAs are design to have a relatively high gain and relatively low *NF* and are placed at the front-end of any cascaded system.

2.2 Distortion

A linear circuit component, such as a simple resistor, exhibits a linear voltage-current relationship. Non-linear components, such as diodes and transistors, have a non-linear voltage-current relationship. It is this non-linearity that makes these components so useful. Unfortunately, this non-linearity also causes problems such as gain compression, spurious signals, increased losses, signal distortion, etc. Consider the block diagram of a basic non-linear component shown in Fig. 2.5. Here, v_i and v_o represent the input and output voltages respectively. The input-output relationship of this component can be modeled as an n^{th} order Taylor series as [9],

$$v_o = a_0 + a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + \cdots + a_n v_i^n , \tag{2.16}$$

where the Taylor coefficients are defined as,

$$a_n = \left. \frac{d^n v_o}{dv_i^2} \right|_{v_i=0} . \tag{2.17}$$

Equation (2.16) can be manipulated to represent most if not all non-linear components. For example, an ideal amplifier could be represented by equation (2.16) with a_1 set as the only non-zero coefficient. Non-ideal components however, have other interfering terms in their Taylor series expansion. This effect can cause serious problems to the given circuit. In the following sub-sections, two forms of distortion will be discussed; gain compression and intermodulation distortion. Consequently, two new LNA metrics will then be introduced to help characterize and account for their effects on

a given circuit or system. These metrics will be useful tools in the CAD approaches to be discussed in Chapters 3 and 4.

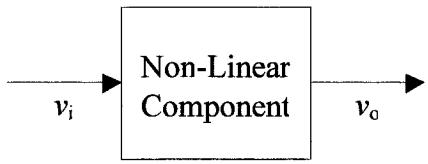


Figure 2.5 Block diagram of a non-linear electronic component.

2.2.1 Gain Compression

The phenomenon of gain compression can be observed through the following example. Suppose a non-linear amplifier (as in Fig. 2.5) is fed a single tone input voltage as,

$$v_i = V_0 \cos \omega_0 t \,. \tag{2.18}$$

Substituting (2.18) into (2.16) results in the following expression,

$$\begin{aligned} v_o &= a_0 + a_1 V_0 \cos\omega_0 t + a_2 V_0^2 \cos^2 \omega_0 t + a_3 V_0^3 \cos^3 \omega_0 t + \cdots + a_n V_0^n \cos^n \omega_0 t \\ &= (a_0 + \frac{1}{2} a_2 V_0^{\,2}) + (a_1 V_0 + \frac{3}{4} a_3 V_0^{\,3}) \cos\omega_0 t + \frac{1}{2} a^2 V_0^2 \cos 2\omega_0 t \\ &\quad + \frac{1}{4} a 3 V_0^3 \cos 3\omega_0 t + \cdots \end{aligned} \tag{2.19}$$

At a frequency of ω_0, an expression for voltage gain can be derived from (2.19) as,

$$G = \left.\frac{v_o}{v_i}\right|_{\omega=\omega_0} = \frac{a_1 V_0 + \frac{3}{4} a_3 V_0^3}{V_0} = a_1 + \frac{3}{4} a_3 V_0^2 \,. \tag{2.20}$$

Equation (2.20) suggests that the amplifier is non-ideal since the overall gain is not simply a_1. The second term in (2.20) is distortion, and since a_3 is usually negative for amplifiers it will cause the amplifier's gain to decrease with larger values of V_0. This phenomenon is known as gain compression.

To better quantify compression gain, consider the response of a typical non-linear amplifier shown in Fig. 2.6. For lower values of input power (*i.e.* P_i), the amplifier gain is relatively linear with a positive slope of 1. At a certain point, the amplifier gain begins to

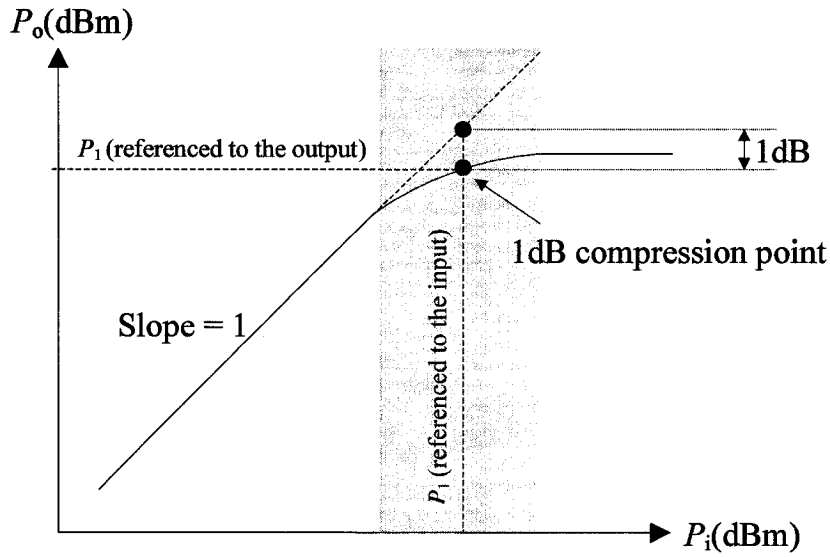


Figure 2.6 Input vs. output power and the 1 dB compression point.

saturate and the response becomes relatively more non-linear (highlighted in grey in Fig. 2.6). This is the point where the second term in equation (2.20) begins to play a more dominant role. The point at which the actual power gain is 1dB lower than the ideal curve

is known as the 1dB compression point or P_1. As shown in Fig. 2.6, P_1 can be referenced to either the input or output powers.

2.2.2 Intermodulation Distortion

The phenomenon of intermodulation distortion can be observed through the following example. Suppose a non-linear amplifier (as in Fig. 2.5) is fed a two-tone input voltage as,

$$v_i = V_0(\cos\omega_1 t + \cos\omega_2 t). \tag{2.21}$$

Substituting (2.21) into (2.16) results in the following expression,

$$\begin{aligned} v_o &= a_0 + a_1V_0(\cos\omega_1 t + \cos\omega_2 t) + a_2V_0^2(\cos\omega_1 t + \cos\omega_2 t)^2 \\ &\quad + a_3V_0^3(\cos\omega_1 t + \cos\omega_2 t)^3 + \cdots + a_nV_0^n(\cos\omega_1 t + \cos\omega_2 t)^n \\ &= a_0 + a_1V_0\cos(\cos\omega_1 t) + a_1V_0\cos(\cos\omega_2 t) + \frac{1}{2}a_2V_0^2(1+\cos 2\omega_1 t) \\ &\quad + \frac{1}{2}a_2V_0^2(1+\cos 2\omega_2 t) + a_2V_0^2(\cos(\omega_1-\omega_2)t + a_2V_0^2(\cos(\omega_1+\omega_2)t \\ &\quad + a_3V_0^3(\frac{3}{4}\cos\omega_1 t + \frac{1}{4}\cos 3\omega_1 t) + a_3V_0^3(\frac{3}{4}\cos\omega_2 t + \frac{1}{4}\cos 3\omega_2 t) \\ &\quad + a_3V_0^3[(\frac{3}{2}\cos\omega_2 + \frac{3}{4}\cos(2\omega_1-\omega_2)t + \frac{3}{4}\cos(2\omega_1+\omega_2)t] \\ &\quad + a_3V_0^3[(\frac{3}{2}\cos\omega_1 + \frac{3}{4}\cos(2\omega_2-\omega_1)t + \frac{3}{4}\cos(2\omega_2+\omega_1)t] + \cdots \end{aligned} \tag{2.22}$$

Hence, from (2.22), the output voltage contains many harmonics of varying order. The order of a harmonic is defined as the algebraic sum of the magnitudes of each frequency component. For instance, the term $a_3V_0^3¾\cos(2\omega_1 - \omega_2)$ is a third order term (*i.e.* |2|+|-1| = 3). Due to their distance in frequency from the desired signal, most of these harmonics can be easily removed using conventional filtering techniques. Unfortunately, the third

order terms of $(2\omega_1 - \omega_2)$ and $(2\omega_2 - \omega_1)$ are located fairly close to the desired signals. These harmonics will cause distortion in the output signal and the overall effect is referred to as third-order intermodulation distortion.

To better quantify the third-order intermodulation distortion, consider the responses of the first and third-order components depicted in terms of their associated power levels in Fig. 2.7. The slope of a power curve is directly related to its order. Hence, the third-order curves will have a slope of 3 while the first-order curves will have a slope of 1.The point at which the ideal first and

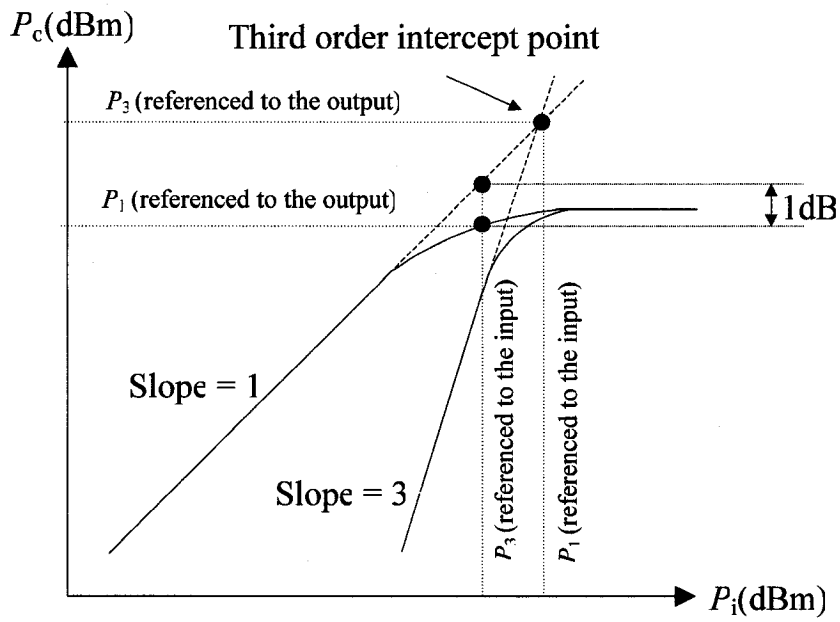


Figure 2.7 Input and output power and the third order intercept point.

third-order curves intersect is known as the third-order intercept point, P_3, or IIP_3 (referenced to the input), or OIP_3 (referenced to the output). IIP_3 and OIP_3 are metrics

that describe third-order intermodulation distortion. The larger these values, the less susceptible the component will be to this kind of distortion (*i.e.* as the input power is increased a component will suffer less intermodulation distortion if its P_3 is relatively large). As shown in Fig. 2.7, P_3 can be referenced to either the input or output powers.

2.2.3 Third-Order Intercept of Cascaded Components

Consider a system of *n* cascaded electronic components (amplifiers, filters, *etc.*) as shown in Fig. 2.8.

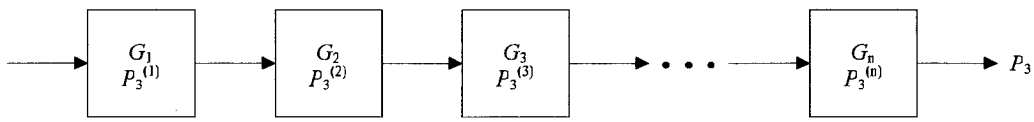


Figure 2.8 IIP_3 of a system of *n* cascaded electronic components.

The overall third-order intercept, IIP_3 of the cascaded system can be derived as [9],

$$P_3 = \frac{1}{(G_2 G_3 \cdots G_n) P_3^1} + \frac{1}{(G_3 \cdots G_n) P_3^2} + \cdots + \frac{1}{(G_n) P_3^{n-1}} + \frac{1}{P_3^{(n)}}. \qquad (2.23)$$

Therefore, from an LNA's perspective (usually the first block in a cascaded system), P_3 is not particularly critical since the contributions to P_3 from later blocks is much more dominant.

2.3 Other LNA Metrics

Aside from noise-figure, P_1, and IIP_3, there are several other useful LNA metrics. Voltage gain, power gain, input/output matching, power consumption, and circuit size are all metrics that must be considered by an LNA designer and hence, by any effective CAD design approach. To give the reader an idea of the types of numerical values to expect, Table 2.1 shows the typical design specifications for an LNA designed for Bluetooth applications. In the following sub-sections, some of the less obvious LNA metrics are briefly discussed.

2.3.1 *S*-Parameters

Scattering parameters or *S*-parameters are very useful parameters that help describe many circuit properties such as gain, return loss, reflection coefficients, and stability. LNAs can usually be considered two-port networks. As such, from an LNA point of view there are four *S*-parameters, each of which describes a different aspect of the LNA's performance. For instance, S_{11} is related to the input port reflection coefficient, and is hence used as a measure of input impedance matching. Similarly, S_{22} is a measure of output impedance matching. S_{12} and S_{21} represent the backward and forward power gains respectively. In both the analog and RF/microwave approaches to LNA design, power gain is referred to as S_{21}.

2.3.2 Power Consumption

Power consumption is often a critical metric in portable applications where considerations such as battery size and power limitations are dominant. In transistor

based circuits, power consumption is primarily a factor of biasing requirements (*i.e.* voltage sources and bias currents). In the analog CAD approach to LNA design, power consumption is among the metrics that are given considerable attention.

2.3.3 LNA Circuit Size

Compact size is often a concern to LNA designers. This is especially true in portable applications where real-estate is sparse and expensive. Specifications regarding circuit size are usually *w.r.t.* the circuit's inductors. This is because inductors tend to be physically larger than other components. An example of circuit size specifications would be the requirement that all components be built on-chip. To satisfy this specification, the inductors must be smaller than about 10nH. Hence, the LNA design may be limited not only by electrical characteristics but by physical ones as well. It will be explained in

TABLE 2.1 TYPICAL DESIGN SPECIFICATIONS FOR BLUETOOTH LNAS

Parameter	Specification	Units
Frequency range	2.45-2.85	GHz
Voltage gain	> 20	dB
Power gain (S_{21})	> 10	dB
Power Consumption	< 20	mW
Noise-figure	< 3.5	dB

Chapter 3 how the analog CAD approach to LNA design considers these physical limits/bounds.

2.4 Summary

In this chapter, fundamental theory regarding LNAs has been presented. Noise, distortion, and several other important LNA metrics have been analyzed and discussed. In the next chapter, several LNA topologies will be examined and their comparative advantages with respect to the discussed metrics will be observed. Further, several design methodologies will be reviewed. The proposed computer aided approach to LNA design will then be presented in detail.

Chapter 3

Computer Aided LNA Design –an Analogue Perspective

As discussed in the previous chapters, designing a low-noise amplifier can be a complicated task. With a plethora of topologies and design methodologies available, simply selecting the type of LNA to design may be challenging in on itself. Even for an analog expert, LNA design can be time consuming and difficult.

In this chapter, the proposed CAD approach to LNA design is described. The approach aims at reducing the required level of expertise for the designer, as well as reducing the overall time and effort needed to create an effective LNA circuit. The approach is divided into three phases; the pre-analysis phase, the design phase, and the fine-tuning phase. A concise flow-chart summarizing the role of each phase is shown in Fig. 3.1. In the pre-analysis phase, the user is encouraged to provide the LNA specifications as well as their relative importance (rankings). Based on the user-inputs, the approach will automatically select an appropriate topology and associated sequence of design equations (in this thesis referred to as SDE). In the design phase, the topology that was selected in the pre-analysis phase is used to create an initial design in Agilent *ADS*. Still in the design phase, the simulation results are checked in a specific order to see

if the user-specifications have been met. Should a specification fail to meet the user requirements, the approach proceeds to the fine-tuning phase, otherwise the current design is considered as the final design and the approach terminates. In the fine-tuning phase, 3D sensitivity plots are used to adjust certain circuit components in the hopes of improving the LNA's performance. In the following sub-sections, each phase will be described in detail.

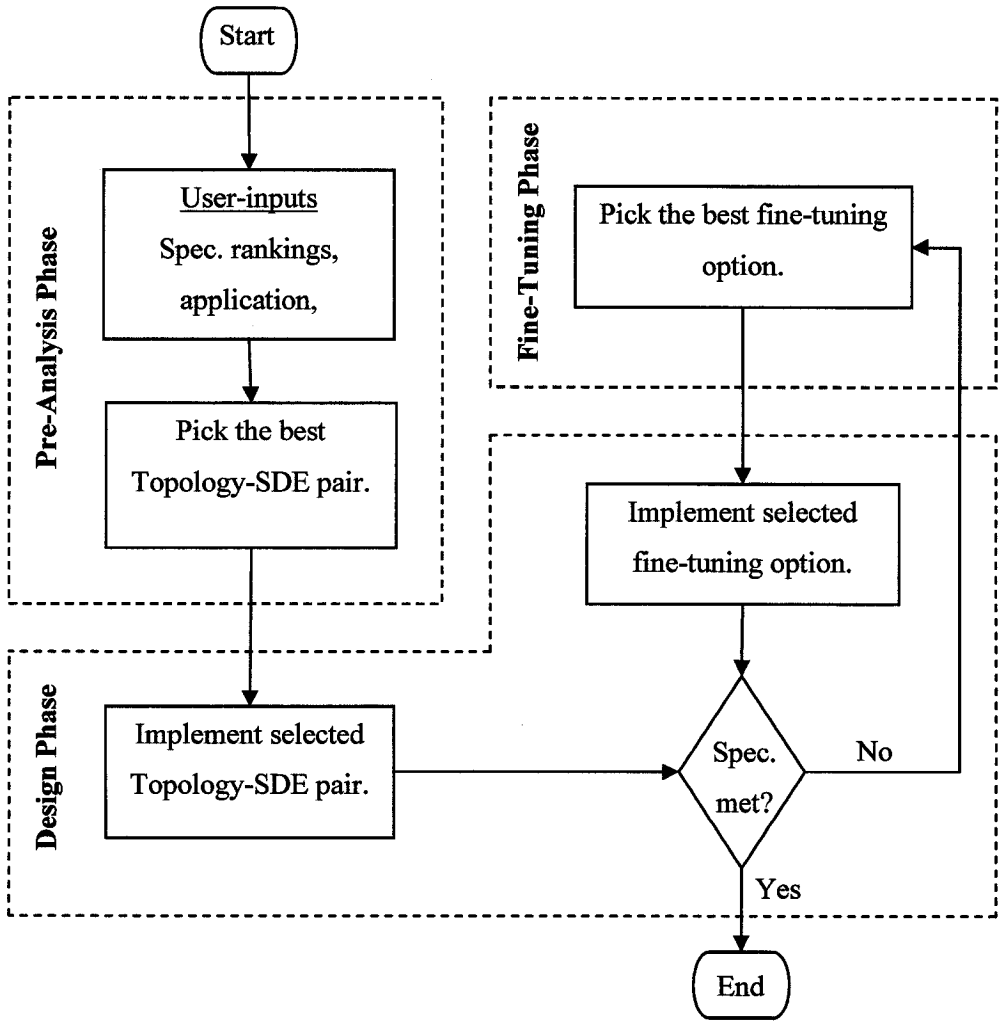


Figure 3.1 Concise flow-chart illustrating the CAD approach to analog LNA design.

3.1 LNA Design

3.1.1 LNA Topologies

For single-stage CMOS LNAs, there are two basic building blocks, namely the common-source (CS) and common-gate (CG) amplifiers shown in Fig. 3.2. Typically, single-stage LNA topologies allow for design/optimization of a small sub-set of the LNA metrics. For instance, a CS amplifier allows for a relatively lower *NF*, while a CG amplifier affords easier impedance matching at the input. On the other hand, multi-stage LNA topologies [10]-[12] combine the best attributes of the single-stage topologies and allow for design/optimization of a larger sub-set of the LNA metrics. Commonly used multi-stage topologies include the cascade, cascode, and differential topologies. Inductive source degeneration is an effective means of impedance-matching and significantly reduces the overall *NF* [13]-[16]. As such, source degeneration is included in all of the LNA topologies considered in this work (see Fig. 3.2 and Fig. 3.3).

3.1.2 Sequence of Design Equations

In this section, a brief review of the basic design methodologies associated with the above-mentioned LNA topologies is presented. These basic methodologies are based on a level one transistor model and hence use simple design equations. As technologies advance, these equations become approximate (or less accurate). In combination with the proposed fine-tuning phase to be discussed later, satisfactory results can be nevertheless achieved. As mentioned, in the proposed CAD approach to analog LNA design each of the associated design methodologies are referred to as a sequence of design equations

(SDE).

It is important to note that in the analog RFIC community, advanced LNA design methodologies based on most recent transistor models continue to evolve. For instance, several LNA design methodologies employing the cascode topology are presented in [17]. Each of these methodologies focuses on optimizing a particular set of user-specifications. It has been shown that by re-arranging the design equations (into different SDEs in the context of this thesis) and by setting constraints, better initial designs can be achieved at the expense of computational complexity. Based on a methodical literature survey, several SDEs have been identified (see Table 2.1) for incorporation into the CAD approach proposed in this thesis. The framework of the proposed approach allows easy/quick incorporation of new SDEs as they become available.

3.1.3 Common-Source (CS)

LNA design based on the CS topology of Fig. 3.2(a) can be approached in several ways. The basic design methodology of [18] (as in Table 2.1) helps solve for the circuit components using a sequence of design equations. Here, an interesting observation can be made. The order in which the equations are solved and the specific parameters being evaluated can potentially affect one or more LNA metrics. For instance, the equation for effective voltage, *i.e.*

$$V_{\text{eff}} = (V_{\text{gs}} - V_{\text{t}}) = \frac{(g_{\text{m}})(L_{\text{min}})}{\mu_{\text{n}} C_{\text{ox}} W}, \tag{3.1}$$

can be interpreted/used in several ways. If power consumption is critical, we may assume a desired value for V_{eff} and solve (3.1) for the transistor width, W. On the other hand, if

circuit size is critical, we may assume a desired value for W and solve for V_{eff}. Another example is the equation concerning the inductances of Fig. 3.2(a), *i.e.*

$$L_g = \frac{Q_L R_S}{\omega_0} - L_S, \tag{3.2}$$

which can be used to solve either for the center frequency (ω_0) or for the quality factor (Q_L). In essence, even the most basic design methodologies can be re-arranged into different SDEs based on a given LNA design problem/scenario.

3.1.4 Common-Gate (CG)

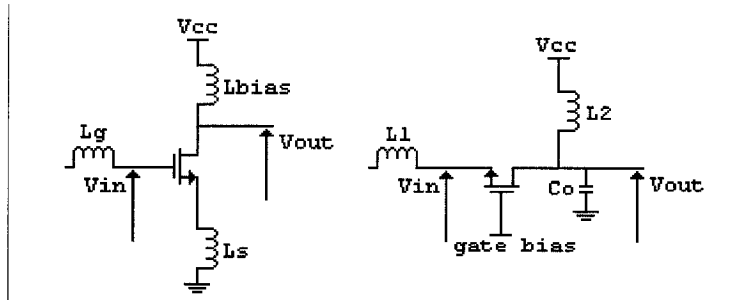
LNA design based on the CG topology of Fig. 3.2(b) can be approached in several ways. The basic design methodology in [6],[7] helps solve for the circuit components of Fig. 3.2(b) using a sequence of design equations. As in the CS case, the order in which the equations are solved and the specific parameters being evaluated can potentially affect one or more LNA metrics. For instance, the equation for transconductance, *i.e.*

$$g_m = \sqrt{2K_n I_D \frac{W}{L_{min}}}, \tag{3.3}$$

can be interpreted/used in several ways. Equation (3.3) can be solved either for W, or for I_D, depending upon the user's preference for circuit size or power consumption. It should be noted that the common-gate topology facilitates easier impedance matching owing to the fact that the input impedance is inversely proportional to g_m.

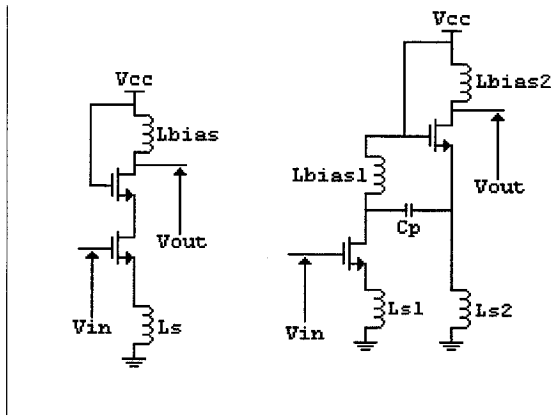
3.1.5 Multi-Stage Topologies

In contrast to single-stage LNAs, multi-stage LNAs can help meet tighter specifications. Common multi-stage topologies include the cascade, cascode, and

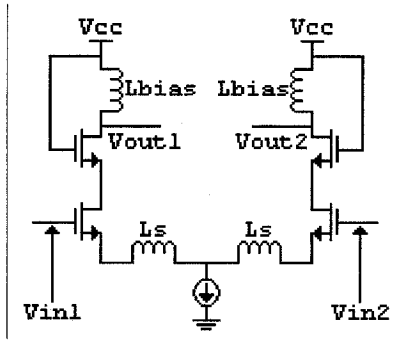


(a) (b)

Figure 3.2 Circuit schematics of (a) common-source LNA and (b) common-gate LNA.



(a) (b)



(C)

Figure 3.3 Circuit schematics of multi-stage (a) cascode, (b) cascade, and (c) differential LNAs.

Table 3.1 LNA Topologies and Corresponding SDEs

Topology	SDE # 1 (Basic)	SDE # 2	SDE # 3
Common-Source	[18]	[20]	NA
Common-Gate	[6][7]	[21]	NA
Cascade	[19]	[22]	[25]
Cascode	[19]	[23]	[26]
Differential	[19]	[24]	[27]

differential topologies. The standard approach for designing these multi-stage LNAs relies on the fact that these circuits can be decomposed into single-stage LNAs. In other words, what can be referred to as modularized design [19] becomes attractive. For instance, a cascade topology can be viewed as two single-stage common-source LNAs connected by a coupling capacitor. Similarly, a differential LNA can be seen as two identical common-source LNAs with their sources connected to the same bias.

3.2 Preliminary Work

As the current version of the CAD approach to LNA design is an extension of a previous work [19], a brief background/overview is included here to help the reader's understanding. The approach in [19] involves three phases, namely the pre-analysis phase, the design phase, and the tuning phase. In the pre-analysis phase, a knowledge-based integer scoring scheme helps select the most appropriate LNA topology (from a

menu consisting of the cascade, cascode and differential topologies). In the design phase, component values of the selected topology are calculated using the basic SDEs of Table 3.1. Where necessary, the tuning phase strives to ensure that all the given user-specifications are met. In addition to the LNA design specifications, users are expected to provide an integer ranking indicating the relative importance of the various specifications.

Motivated by feedback from peers, the CAD approach has been expanded, resulting in the latest version of the approach presented in this thesis. Several aspects have been incorporated to help increase the overall effectiveness of the CAD approach. First, the number of topologies in the topology selection menu has been increased and it is now possible to design of each of the topologies in several ways (depending upon the user-specifications). Second, the integer ranking scheme has evolved into a more robust percentage ranking scheme. Finally, qualitative analysis in the tuning phase of [19] has been replaced with a more meaningful quantitative analysis.

3.3 Pre-Analysis Phase

The user-inputs to the proposed algorithm include the LNA specifications (*e.g. NF*), the percentage rankings, and the desired application for the LNA. Starting with the user-inputs, the primary objective of the pre-analysis phase is to select both an appropriate topology and the sequence of design equations to be used in the creation of an initial LNA design. In essence, for each selected topology, there could exist several distinct SDEs. These sequences greatly affect the LNA's performance with respect to

various metrics. Considering this, the objective of the pre-analysis phase can be re-stated as selection of the most appropriate topology-SDE pair (referred henceforth as T-SDE pair) corresponding to a set of given user-specifications. A flow-chart illustrating critical steps involved in the pre-analysis phase is shown in Fig. 3.4.

Let n and m represent the number of LNA specifications and the number of candidate T-SDE pairs respectively. In [19], it is expected that the user rank the LNA specifications in order of their importance. In the new framework, the user-ranking is facilitated through a new percentage-based parameter a_i, where a_i represents the percentage by which the i^{th} specification can deviate from the corresponding nominal user-specification. The user-inputted a_i not only provides a specific order of importance, (*i.e.* a specification with a smaller a_i is of higher priority) but also offers a meaningful measure for evaluating the resulting LNA design *w.r.t.* the given user-specifications.

Based on the user-specified values of a_i and the underlying application, a feasibility index (or score) is evaluated for each of the candidate T-SDE pairs. For instance, there are three possible candidate pairs for the cascode topology resulting from three SDE options of Table 3.1, *i.e.* [19], [23] and [26]. The T-SDE pair that attains the highest feasibility index is selected and becomes an input to the subsequent phase, *i.e.* the design phase.

Here, the method for evaluating the feasibility index of a T-SDE pair, which involves generating two individual scores based on Tables 3.2 and 3.3 respectively, is described. Table 3.2 assigns a numerical value, b_{ik} ($0 \leq b_{ik} \leq 100$), to the i^{th} specification and k^{th} T-SDE pair. Based on these values, the first individual score for the k^{th} T-SDE

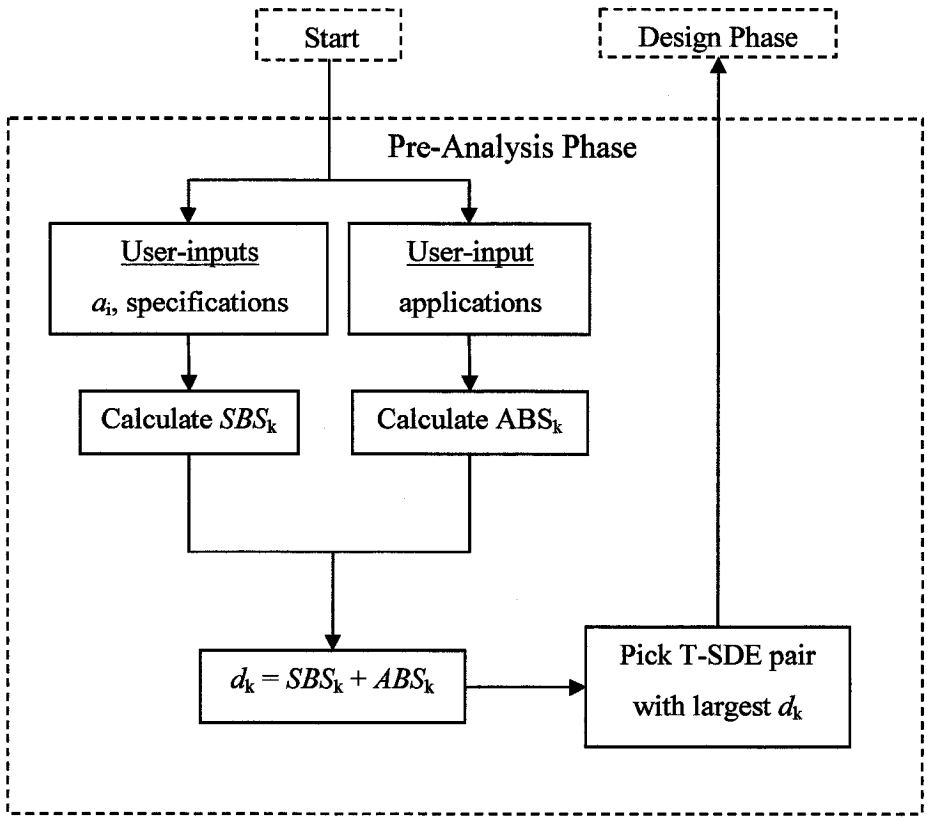


Figure 3.4 Flow-chart illustrating the pre-analysis phase of the CAD approach to analog LNA design.

pair, is generated as

$$SBS_k = \sum_{i=1}^{n} (1 - \frac{a_i}{100}) b_{ik}, \tag{3.4}$$

where SBS_k stands for specification based score. Table 3.3 assigns a numerical value, c_{jk} ($0 \leq c_{jk} \leq 701$), to the j^{th} application and k^{th} T-SDE pair. The second individual score for the k^{th} T-SDE pair, is generated as

$$ABS_k = c_{jk}, \tag{3.5}$$

where ABS_k stands for application based score. Should the user choose not to specify an application for the LNA, the *default* row of Table 3.3 is used in the generation of ABS_k. The overall feasibility index d_k for the k^{th} T-SDE pair is evaluated as an algebraic sum of the two scores, *i.e.*

$$d_k = SBS_k + ABS_k. \tag{3.6}$$

Finally, the T-SDE pair that scores the highest feasibility index is chosen and used in subsequent phases.

It may be noted that c_{jk} are assigned higher numerical values relative to b_{ik}. The reason for this is the fact that certain topologies best suit certain applications. For example, the differential topology best suits LNAs used in mixers. For ease of implementatio7yn, the highest value of c_{jk} is chosen to be greater than the maximum possible value of SBS_k *i.e.*

$$c_{jk_{max}} = [\sum_{i=1}^{n} b_{ikmax} \frac{(100 - a_{imin})}{100}] + 1. \tag{3.7}$$

In the case where $a_{imin} = 0\%$, $b_{ikmax} = 100$ and $n = 7$, $c_{jk_{max}} = 701$.

TABLE 3.2 PROPOSED SCORING DATABASE FOR SPECIFICATIONS VS. T-SDE PAIRS

T-SDE Pair (m=13)		Specification ($n = 7$)						
		Noise-Figure	Power Consump.	Power Gain	Voltage Gain	Circuit Size	P_1	IIP_3
CS	[18]	50	95	50	50	95	55	55
	[20]	60	90	55	55	95	65	65
CG	[6][7]	50	90	50	55	95	70	70
	[21]	50	95	55	45	90	75	75
Cascode	[19]	85	50	90	75	60	60	60
	[23]	85	50	95	70	60	55	55
	[26]	80	40	95	70	70	50	50
Cascade	[19]	70	70	90	70	40	65	65
	[22]	65	75	80	70	40	60	60
	[25]	60	70	80	75	45	65	65
Differential	[19]	65	40	75	60	25	50	50
	[24]	60	45	70	65	20	55	55
	[27]	60	40	75	60	25	55	55

TABLE 3.3 PROPOSED SCORING SCHEME FOR APPLICATION VS. TOPOLOGY

Application	Topology				
	CS	CG	Cascode	Cascade	Differential
Default	0	0	0	0	0
Mixers	0	0	0	0	601
Bluetooth	170	170	160	165	100
ASIC apps.	175	160	150	150	120
Portable apps.	180	180	190	140	130

3.4 Design Phase

In the analog CAD approach, the design phase receives inputs both from the pre-analysis phase (*i.e.* the selected T-SDE pair and the user-specifications) and the fine-tuning phase (to be discussed in section 3.5). The primary goal of the design phase is to create an initial design based on the selected T-SDE pair. First, the LNA topology is laid out as a circuit schematic in Agilent *ADS*. Second, the numerical values of the circuit components are systematically evaluated using the corresponding SDE.

Once an initial design becomes available, DC, AC, *S*-parameter, and harmonic balance (single- and two-tone) simulations are performed and compared with the user-specifications to decide whether or not to proceed to the fine-tuning phase. Should fine-tuning become necessary, the decision as to which of the circuit components will be adjusted is made within the fine-tuning phase. Fig. 3.5 is a flow-chart illustrating the critical steps involved in the design phase.

Let $\boldsymbol{Y}$ be a vector containing the LNA specifications, *e.g.* $\boldsymbol{Y}$ = [*NF*, power consumption, power gain, …, voltage gain]^{T}, and y_i represent the i^{th} entry of $\boldsymbol{Y}$, where i = 1, 2, 3, …, n. In this implementation, the elements in $\boldsymbol{Y}$ are ordered in descending order of their a_i. In other words, y_1 is the highest-ranked specification with least tolerance, while y_n is the lowest ranked with highest tolerance. As shown in Fig. 3.5, the performance of the initial design is compared with the given user-specifications. Keeping in mind that the users provide a percentage parameter for each of the LNA specifications, representing allowed deviation/tolerance, the condition for such comparison is either

$$(1-\frac{a_i}{100})\times y_{ispec}^{lower} \le y_{isim}, \tag{3.8}$$

or

$$(1+\frac{a_i}{100})\times y_{ispec}^{upper} \ge y_{isim}. \tag{3.9}$$

In (3.8) and (3.9), y_{ispec}^{lower} and y_{ispec}^{upper} represent the i^{th} lower and upper user-specifications respectively, and y_{isim} is the simulated result from the current/initial design. When a lower-bound of i^{th} specification is given, *e.g.* voltage gain > 20dB, eq. (3.8) is used. Alternatively, when an upper-bound of i^{th} specification is given, *e.g.* *NF* < 3.5dB, eq. (3.9) is used. Should all specifications satisfy either (3.8) or (3.9), the design phase (and hence the proposed approach) terminates and the current design becomes the final design. Each time the current design fails to meet one of the user-specifications, the CAD approach shifts to the fine-tuning phase (reverts back to the design phase once a fine-tune option is identified).

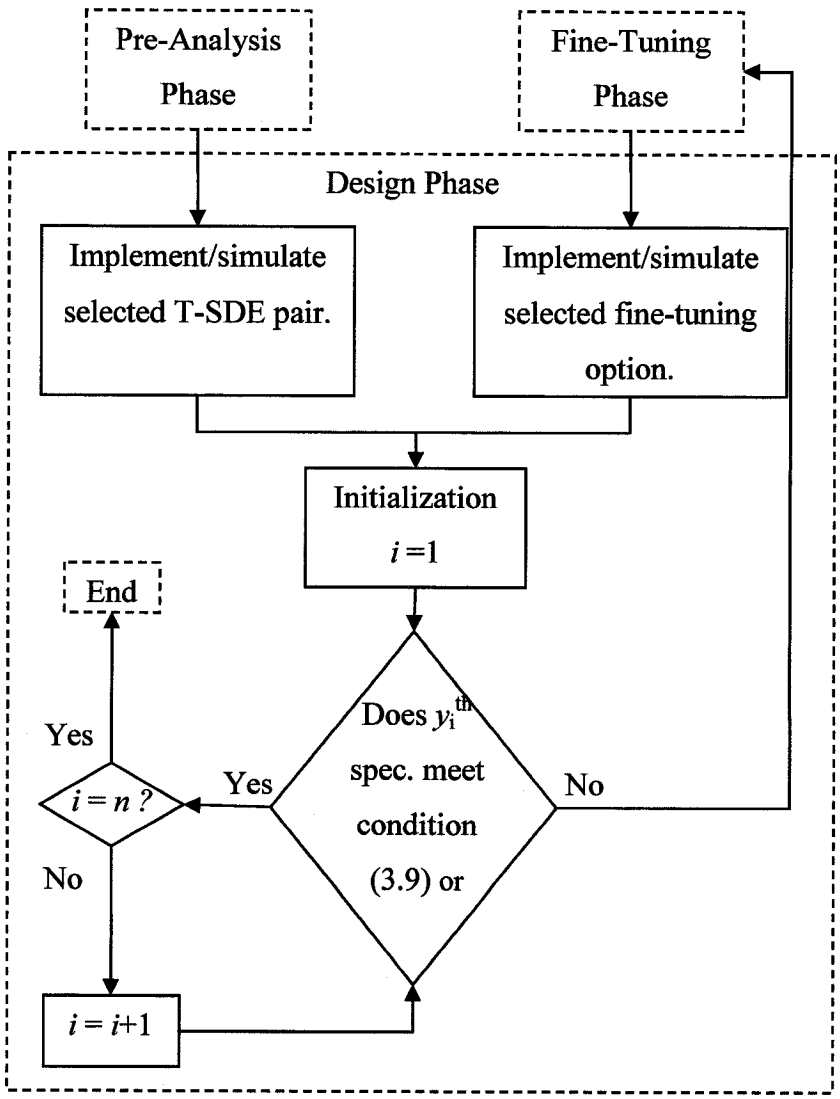


Figure 3.5 Flow-chart illustrating the design phase of the CAD approach to analog LNA design.

3.5 Fine-Tuning Phase

Inputs to the fine-tuning phase include user-specifications ($y_{\text{ispec}}^{\text{lower}}$ or $y_{\text{ispec}}^{\text{upper}}$) and simulation results (y_{isim}). The objective of the fine-tuning phase is to improve the LNA performance in terms of those specifications that failed *w.r.t.* conditions (3.8) or (3.9). A practical way to accomplish this is to slightly change or fine-tune related component values. However, the challenge is to decide which of the components should be changed and by how much. In the tuning phase of [19], only qualitative information was used. In other words, the approach relied on a simple database, which only suggested if a component value should be decreased or increased in order to fine-tune the user-specification in question. Moreover, bounds/limitations *w.r.t.* LNA components were not considered in a practical way. For example, while [19] suggests to change or fine-tune the *W/L* ratio for improving the voltage gain, it does not specify the minimum or maximum feasible values for *W/L*.

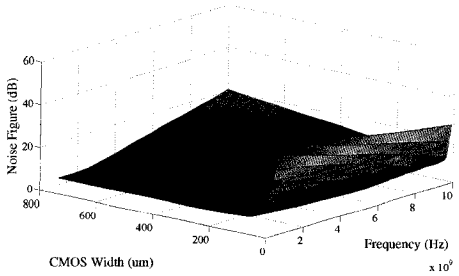
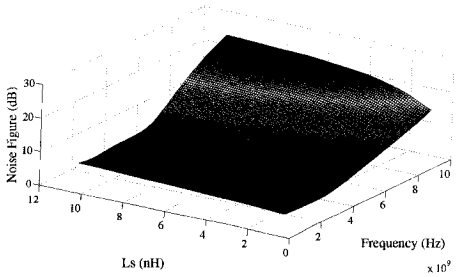
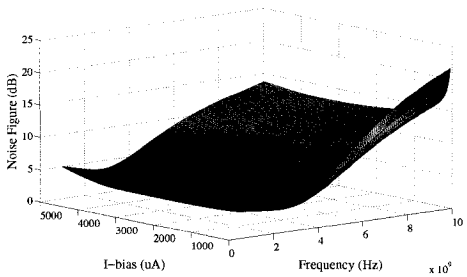
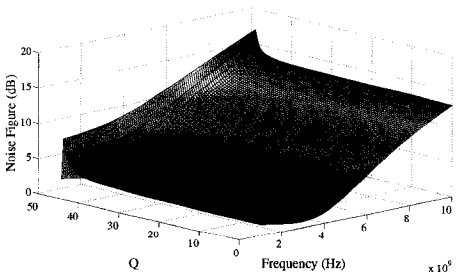
As part of the presented work, a comprehensive fine-tuning table based on an extensive study/experimentation with bounded sensitivity plots is proposed. A number of sensitivity plots have been generated using an in-house *MATLAB* script that automatically reads and interprets *ADS* simulation data. Each plot depicts the variation of a particular LNA specification *w.r.t.* an adjustable component value, while all other components are held constant. The LNA specifications considered in the study include *NF*, power consumption, power gain, voltage gain, and so forth. The LNA components considered include aspect ratio *W/L*, source inductance L_s, transistor bias current I_{bias}, gain of a CS

output stage, and so forth. Due to space limitations, only a small subset of such plots for a cascode LNA are shown in Table 3.4. For instance, one of the plots shows the variation of *NF w.r.t. W*. Since in most cases, user-specifications lie within a given frequency range of interest (as in Table 2.1), the ability to fine-tune over a range of frequencies is mandatory. Similar to other tables (or databases) in the proposed approach, Table 3.4 can be expanded as technologies evolve and additional knowledge becomes available.

It is to be noted that given a new circuit, it becomes necessary to re-generate the above 3D plots, however such an activity merely takes a few minutes of human-time. In the current implementation, a look-up table approach is used where plots are saved for each new circuit. In this way, new plot generation will only be necessary if that particular circuit has never been created (*i.e.* in other LNA designs). In the particular case where the user-specifications are to be met only at a single frequency, (*i.e.* a "critical" frequency), the 3D plots of Table 3.4 are reduced to relatively simpler 2D plots. The flow-chart of Fig. 3.6 illustrates the major steps involved in the proposed fine-tuning phase and a corresponding pseudo code follows.

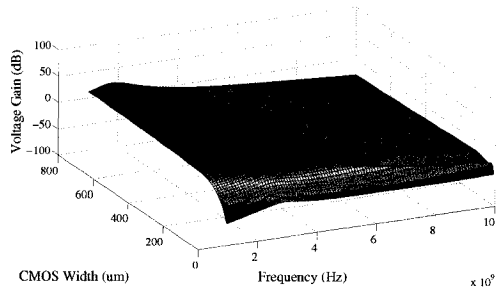
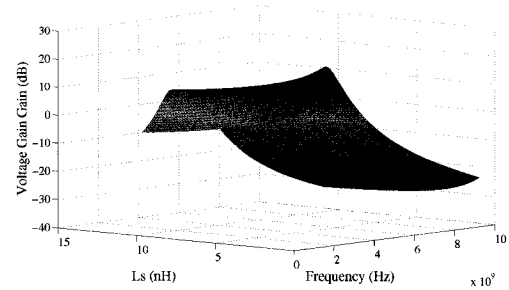
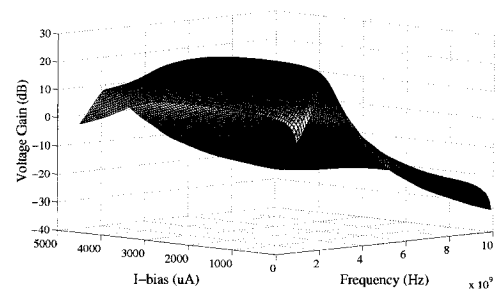
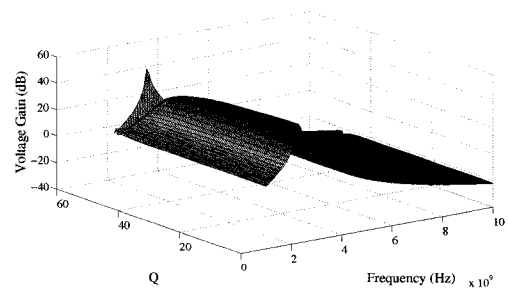
TABLE 3.4 SUBSET OF 3D SENSITIVITY FINE-TUNING PLOTS FOR THE CASCODE TOPOLOGY FOR (A) NOISE-FIGURE, (B) VOLTAGE GAIN, AND (C)S_{21}

(A)

Fine-Tuning Option	Specification
	Noise-Figure
Change the value of the transistor width.	
Change the value of L_s.	
Change the value of the bias current.	
Change Inductor quality factor.	

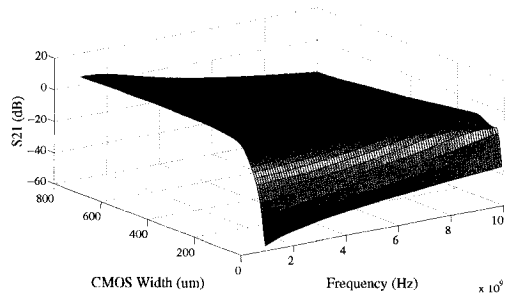
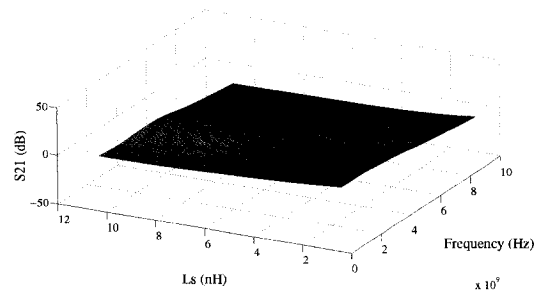
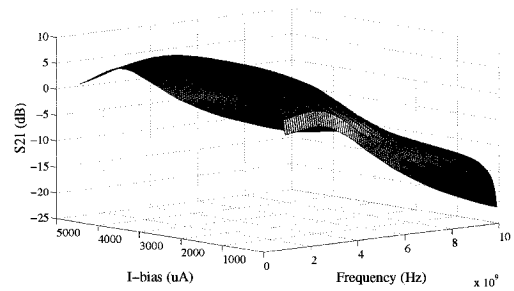
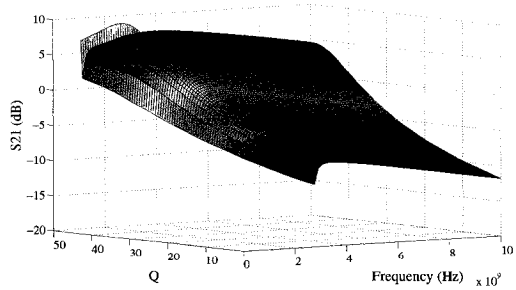
Note: Tuning options are not limited to adjustable parameters already part of the initial design. The addition of adjustable parameters (e.g. the addition of another stage) is also possible.

(B)

Fine-Tuning Option	Specification
	Voltage Gain
Change the value of the transistor width.	
Change the value of L_s.	
Change the value of the bias current.	
Change Inductor quality factor.	

Note: Tuning options are not limited to adjustable parameters already part of the initial design. The addition of adjustable parameters (e.g. the addition of another stage) is also possible.

(C)

Fine-Tuning Option	Specification
	S_{21}
Change the value of the transistor width.	
Change the value of L_s.	
Change the value of the bias current.	
Change Inductor quality factor.	

Note: Tuning options are not limited to adjustable parameters already part of the initial design. The addition of adjustable parameters (e.g. the addition of another stage) is also possible.

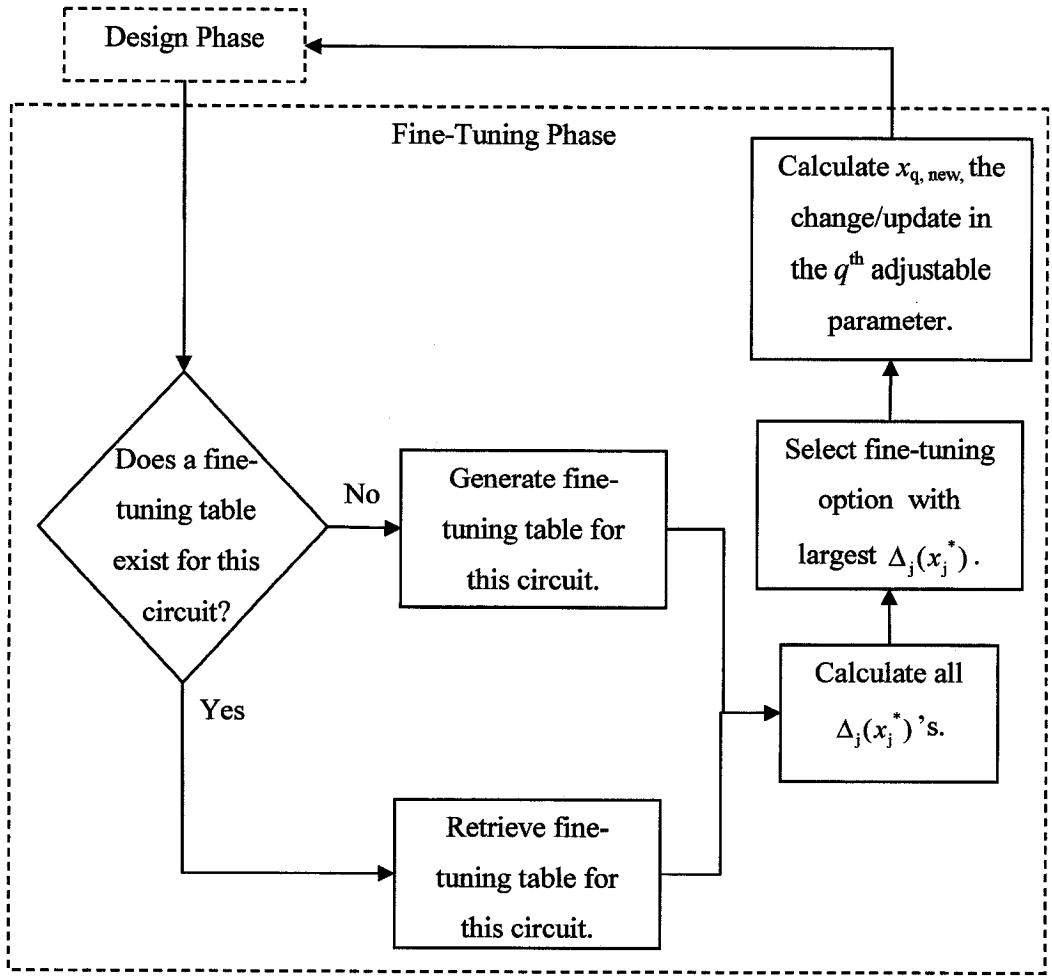


Figure 3.6 Flow-chart illustrating the fine-tuning phase of the CAD approach to analog LNA design.

Pseudo Code

Definition: Let $\boldsymbol{X}$ be a vector containing the adjustable LNA components/parameters values, *e.g.* $\boldsymbol{X} = [W, L_s, C_0, I_{bias}, \text{CS gain}, Q_L]^T$. Let x_j represent the j^{th} entry of $\boldsymbol{X}$, $j = 1, 2, 3, \ldots, M$, where M is the total number of designable parameters. Let $[x_{j,min}, x_{j,max}]$ be the lower and upper bounds/limits of the j^{th} design parameter, $[f_{min}, f_{max}]$ denote the frequency range of interest, and f_c denote the center frequency. Let $y_{iplot}(x_j, f)$ refer to a 3D sensitivity plot of Table 3.4, *i.e.* $y_{iplot}(x_j, f)$ symbolizes the sensitivity of the i^{th} specification *w.r.t.* the j^{th} adjustable parameter and frequency f. Let p denote the total number of possible values (or points on a grid) for x_j within the bounds $[x_{j,min}, x_{j,max}]$. It may be noted that in the computation of $y_{iplot}(x_j, f)$, all x_k, $k \neq j$, are kept constant, and $f \in [f_{min}, f_{max}]$. Fig. 3.7, is a graphical representation of a possible 3D sensitivity plot with the above defined values shown.

Inputs: The inputs to the fine-tuning phase include either y_{ispec}^{lower} or y_{ispec}^{upper}, and y_{isim} for the LNA metric in question, *i.e.* for the i^{th} metric that failed to satisfy either (3.8) or (3.9).

Initialization: Set $j = 1$.

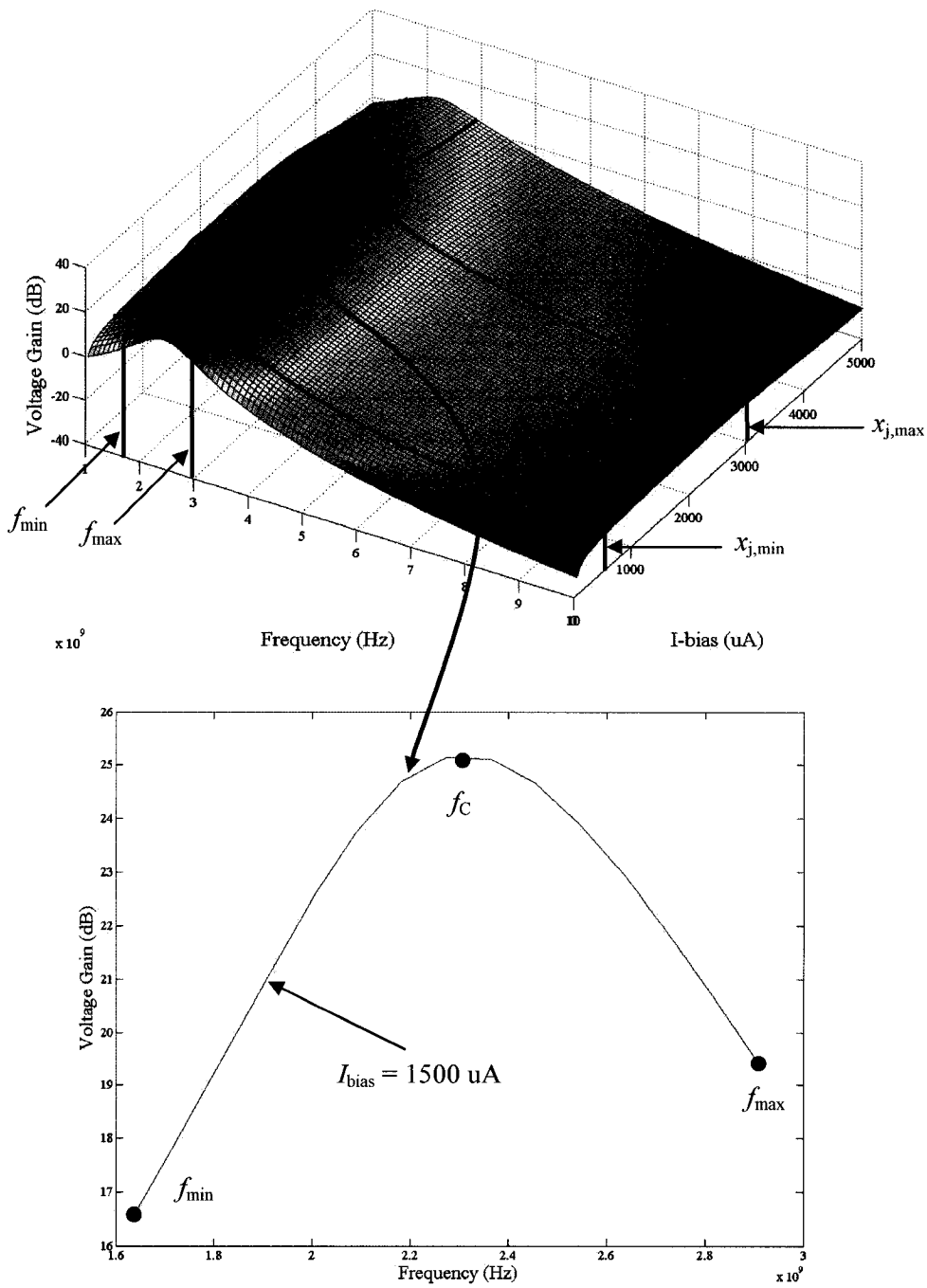


Figure 3.7 Graphical representation of a bounded 3D sensitivity plot.

Step 1: Evaluate

$$x_j^* = \arg \min_{x_j \in [x_{j,\min}, x_{j,\max}]} | \{ \frac{1}{3} [y_{\text{iplot}}(x_j, f_{\min}) + y_{\text{iplot}}(x_j, f_c) + y_{\text{iplot}}(x_j, f_{\max})] - y_{\text{ispec}}^{\text{lower}} \} | \tag{3.10}$$

or

$$x_j^* = \arg \min_{x_j \in [x_{j,\min}, x_{j,\max}]} | \{ \frac{1}{3} [y_{\text{iplot}}(x_j, f_{\min}) + y_{\text{iplot}}(x_j, f_c) + y_{\text{iplot}}(x_j, f_{\max})] - y_{\text{ispec}}^{\text{upper}} \} | \tag{3.11}$$

depending on whether the i^{th} LNA metric has a lower or an upper bound specified. In (3.10) and (3.11), x_j^* represents the specific value of the j^{th} designable component, which adjusts the LNA performance to be as close as possible to either $y_{\text{ispec}}^{\text{lower}}$ or $y_{\text{ispec}}^{\text{upper}}$ accordingly. In situations where the i^{th} design parameter is extremely sensitive, equations (3.10) and (3.11) could be modified by adding extra grid points from the 3D plots.

Step 2: Evaluate

$$\Delta_j(x_j^*) = \sum_i \left\lceil \frac{y_{\text{iplot}}(x_j^*, f_c) - y_{\text{isim}}(f_c)}{y_{\text{isim}}(f_c)} \times (100 - a_i) \right\rceil + \sum_k \left\lceil \frac{-y_{\text{kplot}}(x_j^*, f_c) - y_{\text{ksim}}(f_c)}{y_{\text{ksim}}(f_c)} \times (100 - a_k) \right\rceil, \tag{3.12}$$

where i and k are indices for the LNA metrics, for which upper and lower bounds have been specified respectively. Intuitively, Δ_j's represent a percentage improvement in the LNA performance. IF $j = M$, set $\Delta = \max_j \{\Delta_j(x_j^*)\}$ and $q = \arg\max_j \{\Delta_j(x_j^*)\}$, and GO TO *Step* 3. Otherwise, set $j = j+1$ and GO TO *Step* 1.

Step 3: Set $x_{q,new} = x_{q,current} + (\frac{x_{q,max} - x_{q,min}}{p})$ and re-evaluate $\Delta_j(x_{q,new})$ using (3.12). IF $\Delta_j(x_{q,new}) < \Delta$ GO TO *Step* 4, ELSE set $x_{q,current} = x_{q,new}$ and GO TO *Step* 3.

Step 4: Set $x_{q,new} = x_{q,current} - (\frac{x_{q,max} - x_{q,min}}{p})$ and re-evaluate $\Delta_j(x_{q,new})$ using (3.12). IF $\Delta_j(x_{q,new}) \geq \Delta$, set $x_{q,current} = x_{q,new}$ and GO TO *Step* 4. ELSE GO TO *Step* 5.

Step 5: Set $x_{q,new}$ as the changed/updated value of the q^{th} designable component and GO TO the design phase, in which the fine-tuned LNA circuit is implemented/simulated in *ADS*.

The pseudo code described above (and correspondingly the fine-tuning phase) has two distinct goals; selecting the adjustable parameter with which to fine-tune (*i.e.* steps 1 and 2) and deciding how much the selected adjustable parameter will be changed/adjusted (*i.e.* steps 3, 4 and 5). Both goals rely heavily on equation (3.12). From an optimization perspective, equation (3.12) can be seen as an l_1-weighted error measure, in which the weights are the user-defined a_i's. These weights tend to favour the specifications that are relatively more important to the user. The process for accomplishing both goals is described below.

Steps 1 and 2, selecting the adjustable parameter to fine-tune: Each candidate fine-tuning option is adjusted such that it will improve the failed specification (identified

in the design phase) as much as possible. Equation (3.12) is then calculated for each candidate fine-tuning option and can be considered as a performance index. The resulting performance indexes reveal which fine-tuning option has the largest potential of meeting the required specification (*i.e.* has the largest value from equation (3.12)).

Steps 3, 4, and 5, deciding how much to change the selected adjustable parameter: It is clear that adjusting the selecting fine-tuning option so that it maximizes or minimizes the given failed specification is not desirable (since it neglects to take into account the other specifications). When *Step* 3 begins for the first time, the selected fine-tuning option is set to be changed such that it minimizes or maximizes the failed specification. The approach now increases the adjustable parameter by one grid point and re-calculates equation (3.12). If $\Delta_j(x_j^*)$ (the performance index) increases, it is clear that, given the user-defined a_i's, the overall LNA performance will improve by increasing the change in the fine-tuning option. If on the other hand $\Delta_j(x_j^*)$ decreases, the approach recognizes that the overall LNA performance has degraded and tries to reduce the fine-tuning option by one grid point instead (*Step* 4). When the approach is unable to either increase or decrease the adjustable parameter, it terminates and returns the last change with the best performance index to the design phase for implementation.

Owing to its iterative nature, the proposed fine-tuning phase has the potential to consider/exhaust all possible fine-tuning options before termination. It should be noted that, in the implementation of the fine-tuning phase, a stopping criteria is used in the case where the user specifications cannot be met. In this case, the fine-tuning phase will

terminate after a user defined number of iterations. As can be seen through examples, the final design could be fairly different from the initial design in terms of the circuit component values, circuit topology, and most importantly the overall LNA performance.

3.6 Application Examples

In this section, the proposed CAD approach is applied to two practical LNA design scenarios. In the first example, a set of specifications and a corresponding set of a_i's are given as the user-inputs. *ADS* simulations of the resulting LNA design are compared with those from LNA designs taken from existing literature. In the second example, a set of user-specifications and multiple sets of a_i's (reflecting different priorities) are provided as user-inputs. The proposed CAD approach is shown to generate different LNA designs for different sets of a_i's. LNA designs presented correspond to 0.18μm CMOS technology and use BSIM3 models. The specific process is the IBM 0.18 7RF.

Example 1: LNA Design for ASIC Applications

In this example, an LNA for use in a ASIC is to be designed. The user-specifications and corresponding a_i's are shown in Table 3.5. The frequency range of operation is specified as f_{min} = 2.45GHz, f_c = 2.65GHz, and f_{max} = 2.85Hz. Additionally, the user requires that the inductors be no bigger than 10nH to allow on-chip fabrication. The proposed CAD approach is applied.

In the pre-analysis phase, the feasibility index, *i.e.* d_k, is calculated for each of the T-SDE pairs. The cascode topology with SDE of [19] scores the largest d_k (*i.e.* SBS_k =

424.55, $ABS_k = 150$, and $d_k = 574.55$) and is hence selected. It is to be noted that although the basic SDE is merely an approximation, the design and the fine-tuning phases of the proposed approach together correct for the inaccuracies in the initial design.

In the design phase, the selected T-SDE pair is considered, and a corresponding initial design is generated and simulated in *ADS*. As described in Fig. 3.5, these simulations are compared against the given user-specifications using (3.8) or (3.9) in ascending order of their a_i's. Should a specification fail, the design approach shifts to the fine-tuning phase, in which a designable component is identified for improving the design. The design phase is then repeated for the modified circuit and the specifications are re-checked. Thus, several iterations involving the design and the fine-tuning phases could become necessary. This example required three such iterations.

In the first iteration, *ADS* simulations of the initial design reveal that the two highest-ranked specifications, *i.e.* noise-figure and voltage gain with a_i's of 4% and 5% respectively, are satisfied. For noise-figure, equation (3.9) is used, and for voltage-gain ,equation (3.8) is used. The next highest-ranked specification, *i.e.* power gain with an a_i = 6%, deviates from the user-specification by approximately 54.4% (10.87dB versus 20dB), and hence equation (3.8) is not met. In the ensuing fine-tuning phase, a designable LNA parameter is selected to improve the power gain even at the expense of less important specifications (*e.g.* circuit size and power consumption). In this case, the fine-tuning phase recommends the addition of a common-source output stage with a voltage gain of 4.55dB. In the second and third iterations, the fine-tuning phase recommends increasing the gain on the CS stage and increasing the bias current respectively. The

circuit schematic of the final design is shown in Fig. 3.8.

A detailed breakdown of the LNA performance after each iteration is summarized in Table 3.5. Table 3.6 shows which of the specifications pass or fail in each iteration and the adjustable parameter selected for fine-tuning. In Table 3.5, the final LNA design resulting from the proposed CAD approach is compared with other cascode LNAs [26],[28]. The proposed approach is effective in obtaining a balanced design *w.r.t.* the user-specifications and corresponding priorities.

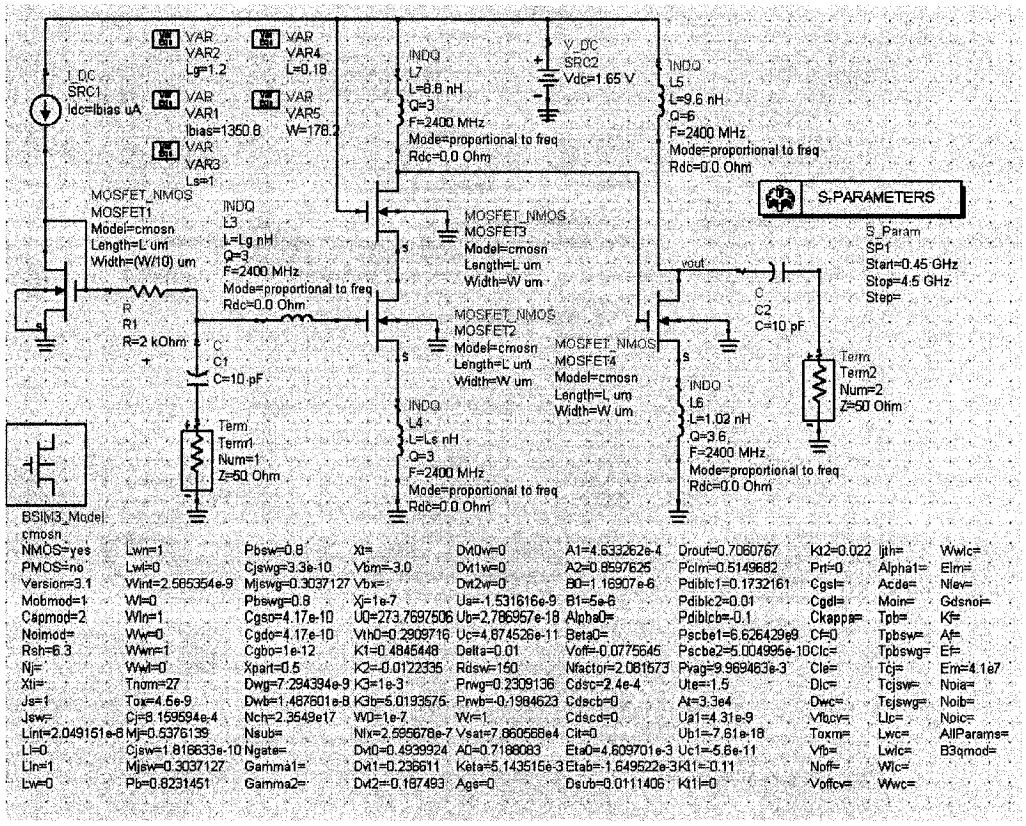


Figure 3.8 ADS schematic for the final LNA design of example 1.

Table 3.5 Breakdown of LNA Performance After Each Iteration for Example 1.

		Metric						
		Noise-Figure	Voltage Gain	Power Gain	P_1	IIP_3	Circuit Size	Power Consump.
User Inputs	a_i	4%	5%	6%	15%	19%	20%	21%
	Target Spec.	<3.5dB	>20dB	>20dB	>5dBm	>5dBm	**	<20mW
Proposed Circuit Results	Initial design	1.8dB	25.1dB	6.71dB	-0.5dBm	10.2dBm	*	12.6mW
	After first iteration	1.86dB	29.65dB	10.87dB	1.32dBm	11.3dBm	*	12.6mW
	After second iteration	3.97dB	32.13dB	26.26mW	1.45dBm	12.1dBm	*	12.6mW
	After third iteration (Final Design)	2.18dB	30.74dB	23.98mW	1.46dBm	12.1dBm	*	22.3mW
Literature Results	[26]	1.2dB	-	19.5dB	-	-	*	40.8mW
	[28]	4dB	-	12dB	-13dBm	-2dBm	*	14.3mW

***Any inductors in the design should be smaller than 10nH*

**Design does not have inductors above 10 nH (i.e. design meets user-specification)*

Table 3.6 Achieved Specifications in Each Iteration of Example 1

		Iteration Number		
		1	2	3
Pass/Fail Condition (3.9) or (3.10) in the Design Phase	Noise-Figure ($a_i = 4\%$)	Pass (3.10)	Pass (3.10)	Fail (3.10)
	Voltage Gain ($a_i = 5\%$)	Pass (3.9)	Pass (3.9)	Not Checked
	Power Gain ($a_i = 5\%$)	Fail (3.9)	Fail (3.9)	Not Checked
	P_1 ($a_i = 15\%$)	Not Checked	Not Checked	Not Checked
	IIP_3 ($a_i = 19\%$)	Not Checked	Not Checked	Not Checked
	Circuit Size ($a_i = 20\%$)	Not Checked	Not Checked	Not Checked
	Power Consump. ($a_i = 21\%$)	Not Checked	Not Checked	Not Checked
Selected Solution From the Fine-Tuning Phase		Add a CS output stage with a voltage gain of 4.55 dB	Increase voltage gain of CS stage by 2.84 dB	Increase Ibias to 1.35mA

Example 2: LNA Designs for Multiple Applications

In this example, it is shown how the proposed approach can create various LNA designs beginning from the same range of initial specifications (in this case the specifications are those outlined in Table 2.1). This is accomplished by choosing various sets of a_i's and arriving at several distinct designs which can cater to distinct practical applications. To showcase the efficiency of the CAD approach, four different sets of a_i's are considered. Specifically, the first three LNAs are specified to be used in portable applications (*e.g.* WLAN) while the fourth design is specified to be the default (see Table 3.3). The proposed approach is applied. Correspondingly, four different LNA designs are generated. Table 3.7 shows the a_i's and the corresponding simulations for each of those circuit designs. For comparative purposes, performances of three other LNAs from the existing literature are also included in the Table.

While each of the four proposed designs do not lead to improved performance *w.r.t.* all of the given specifications, those specifications with relatively higher priorities/rankings are improved. For instance, in *Design* 1, circuit size has been assigned the highest priority while power gain has been assigned the lowest. The resulting LNA is a single-stage common-source amplifier whose inductor values are $\leq$ 7nH. While this design does not exhibit the best power gain (8.56dB), it does lead to size minimization. *Design* 2 on the other hand, deemphasizes circuit size while striving for better performance *w.r.t.* noise-figure and power consumption. The resulting cascode topology exhibits considerably improved noise-figure (0.96dB) and power consumption (8mW). *Design* 3 is a balance between noise-figure, power consumption, and power gain. *Design*

4 is a cascaded LNA, which minimizes power consumption and maximizes power gain. In essence, the proposed CAD approach offers a tremendous advantage to circuit designers by providing a scope for inputting user-rankings or a_i's. Consequently, users can obtain LNA designs that satisfy varying performance and/or application scenarios.

Table 3.7 Simulation Results For Example 2

			Metric						
			Noise-Figure (dB)	Voltage Gain (dB)	Power Gain (dB)	Power Consump. (mW)	Circuit Size	IIP_3 (dBm)	P_1 (dBm)
Proposed LNA Design Results	Design 1 CS [20]	a_i	15 %	20 %	15 %	10 %	0%	21%	19%
		Spec.	3.5	12.4	8.56	8	Small	-15.3	-2.4
	Design 2 Cascode [19]	a_i	1%	10%	15%	5%	40%	15%	10%
		Spec.	0.96	24.5	15.3	8	Medium	-11.2	-1.8
	Design 3 Cascode [19]*	a_i	10%	5%	10%	10%	40%	20%	15%
		Spec.	2.1	28	25.4	11	Medium	-4.5	-3.4
	Design 4 Cascade [19]*	a_i	15%	5%	5%	0%	80%	5%	6%
		Spec.	2.3	35	30	6	Large	-21.9	-32.0
Results From Literature	[29] Cascode	*Spec.*	2.4	-	19	9	Large	-	-
	[30] Cascode	Spec.	1.6	-	25	16	Large	-8.5	-
	[22] Cascade	Spec.	1.1	-	27	4.6	Large	-30.0	-

**Refers to a design that has undergone at least one iteration of the fine-tuning phase.*

Chapter 4

Computer Aided LNA Design - an RF/Microwave Perspective

As previously discussed, LNA design can be approached in several ways. In this chapter LNAs from an RF/microwave perspective will be presented, where impedance matching takes a predominant role in the overall design flow. In Chapter 2, an LNA is described as an amplifier where noise-reduction and gain maximization are paramount. Considering this, the design of RF/microwave oriented LNA's should be very similar to standard amplifier design with special attention paid to noise and gain. Hence, this chapter begins with a brief discussion on the theoretical background necessary for the design of basic RF/microwave oriented amplifiers and LNAs. In section 4.2, the proposed

CAD approach to LNA design from an RF/microwave perspective is described. Finally, in section 4.3, the proposed CAD approach is applied to practical LNA design scenarios.

4.1 Theoretical Background on Amplifier Design [9]

4.1.1 Two-Port Power Gains

Consider the generalized two-port network with scattering matrix [*S*] and characteristic impedance Z_0 shown in Fig. 4.1. In Fig. 4.1, Z_S and Z_L represent the source and load impedances respectively, Γ_S and Γ_L represent the source and load reflection coefficients respectively, and Γ_{in} and Γ_{out} represent the input and output reflection coefficients of the two-port network respectively. The source and load reflection coefficients are given as,

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{4.1}$$

and

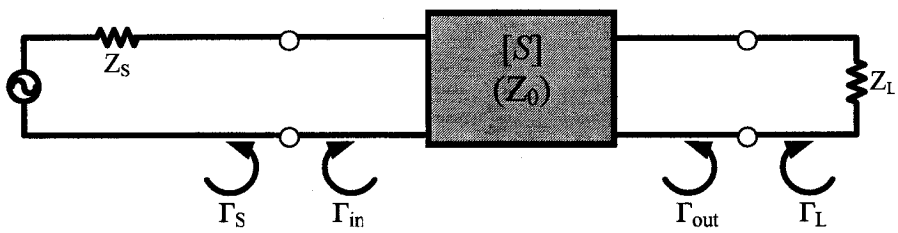


Figure 4.1 A general two port network.

$$\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0}. \tag{4.2}$$

The input and output reflection coefficients are given as,

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{4.3}$$

and

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S}. \tag{3.4}$$

For this kind of network three types of power gains have been derived [9] as,

$$Power\ Gain = G = \frac{P_L}{P_{in}} = \frac{|S_{21}|^2(1-|\Gamma_L|^2)}{(1-|\Gamma_{in}|^2)|1-S_{22}\Gamma_L|^2}, \tag{4.5}$$

$$Available\ Gain = G_A = \frac{P_{anv}}{P_{avs}} = \frac{|S_{21}|^2(1-|\Gamma_S|^2)}{|1-S_{11}\Gamma_S|^2(1-|\Gamma_{out}|^2)}, \tag{4.6}$$

and

$$Transducer\ Gain = G_T = \frac{P_L}{P_{avs}} = \frac{|S_{21}|^2(1-|\Gamma_S|^2)(1-|\Gamma_L|^2)}{|1-\Gamma_S\Gamma_{in}|^2|1-S_{22}\Gamma_L|^2}. \tag{4.7}$$

In (4.5), (4.6), and (4.7) P_L is the power dissipated in the load (*i.e.* Z_L), P_{in} is the power delivered to the input of the two-port network, P_{avn} is the power available from the two-port network, and P_{avs} is the power available from the source. Three definitions of power gain are needed as they each portray different information. G is the most commonly used definition for power gain and, as can be observed, it is independent of Z_S. Since many active circuits strongly depend on Z_S, G does not always relay meaningful information. G_A, on the other hand, depends on Z_S but not on Z_L and assumes a conjugate match at

both the input and output of the two-port network. Finally, G_T depends on both Z_S and Z_L. It is important to note that the power gain is maximized when the input and output impedances are conjugately matched to the two-port network. When both input and output ports are conjugately matched, then $G = G_A = G_T$.

4.1.2 Two-Port Transistor Amplifier Power Gains

Consider the block diagram of a typical single-stage amplifier circuit as shown in Fig. 4.2. In the most general terms, the design of an amplifier involves the appropriate calculation and design of the input and output matching networks for the transistor device.

The way in which these networks are designed will greatly affect all pertinent amplifier performance metrics (*e.g.* noise-figure, gain, linearity, dynamic range, etc.). For instance, these networks can be designed to maximize the overall power gain. Alternatively, the networks can be designed for a specific/desired noise-figure with a corresponding gain. Considering the above discussion, it is clear that in amplifier design

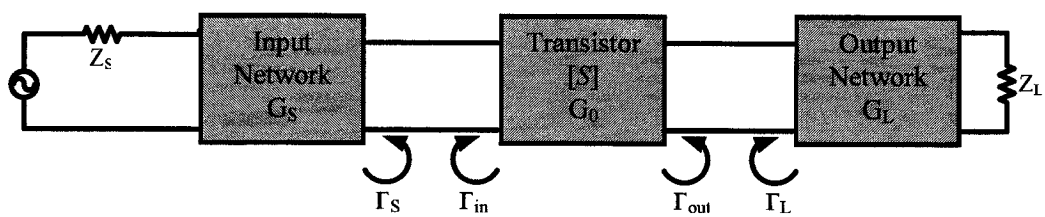


Figure 4.2 Typical transistor amplifier circuit.

G_T is the most useful gain definition as it considers both Z_S and Z_L. It is possible to define three distinct gain factors for each block in Fig. 4.2 as [9],

$$G_S = \frac{1-|\Gamma_S|^2}{|1-\Gamma_{in}\Gamma_S|^2}, \tag{4.8}$$

$$G_0 = |S_{21}|^2, \tag{4.9}$$

and

$$G_L = \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2}. \tag{4.10}$$

Through these gain factors the overall transducer gain (G_T) of Fig. 4.2 can be calculated as

$$G_T = G_S G_0 G_L. \tag{4.11}$$

In the unilateral case, where S_{12} of the transistor equals 0, then from (4.3) and (4.4), $\Gamma_{in} = S_{11}$ and $\Gamma_{out} = S_{22}$. Therefore, (4.8) may be re-written for both the bilateral case (non-unilateral), *i.e.*

$$G_S = \frac{1-\left|\frac{Z_S - Z_0}{Z_S + Z_0}\right|^2}{\left|1-(S_{11}+\frac{S_{12}S_{21}(\frac{Z_L - Z_0}{Z_L + Z_0})}{1-S_{22}(\frac{Z_L - Z_0}{Z_L + Z_0})})(\frac{Z_S - Z_0}{Z_S + Z_0})\right|^2}, \tag{4.12}$$

and the unilateral case, *i.e.*

$$G_S = \frac{1-\left|\frac{Z_S - Z_0}{Z_S + Z_0}\right|^2}{\left|1 - S_{11}\left(\frac{Z_S - Z_0}{Z_S + Z_0}\right)\right|^2}. \tag{4.13}$$

When designing an amplifier, it is often the case that the maximum gain is not desired. For instance, when designing an LNA, the overall gain may be sacrificed in order to improve the noise-figure. As such, the design of an amplifier at a specific gain is required. To accomplish this task, the concept of constant gain circles (*i.e.* on a Smith chart) needs to be reviewed for both the unilateral and non-unilateral (bilateral) design cases. Following this, the concept of constant noise-figure circles is discussed for future use in the CAD approach to LNA design.

4.1.3 Constant Gain Circles – Unilateral Design

The overall gain of an amplifier is given by equation (4.11). When designing an amplifier for a specific gain, the goal is to design the input and output matching networks such that G_S and G_L will yield the desired gain as per (4.11) (G_0 is the transistor's gain and is not to be designed). In [9], the unilateral figure of merit, U, is defined as,

$$U = \frac{|S_{11}||S_{12}||S_{21}||S_{22}|}{(1-|S11|^2)(1-|S22|^2)}. \tag{4.14}$$

Then, the error in transducer gain caused by the unilateral assumption is bounded by,

$$\frac{1}{(1+U)^2} < \frac{G_T}{G_{TU}} < \frac{1}{(1-U)^2} \tag{4.15}$$

or

$$10\log(\frac{1}{(1+U)^2}) < G_T(\text{in dB}) - G_{TU}(\text{in dB}) < 10\log(\frac{1}{(1-U)^2}), \qquad (4.16)$$

where G_{TU} is the unilateral transducer gain given as,

$$G_{TU} = \frac{|S_{21}|^2(1-|\Gamma_S|^2)(1-|\Gamma_L|^2)}{|1-S_{11}\Gamma_S|^2|1-S_{22}\Gamma_L|^2}. \qquad (4.17)$$

When the input and output of the transistor are conjugately matched (*i.e.* $\Gamma_S = S_{11}^*$ and $\Gamma_L = S_{22}^*$ in the unilateral case), the transducer gain is maximized. Therefore, from (4.10) and (4.13) an expression for the maximized gains G_S and G_L are obtained as,

$$G_{Smax} = \frac{1}{1-|S_{11}|^2} \qquad (4.18)$$

and

$$G_{Lmax} = \frac{1}{1-|S_{22}|^2}. \qquad (4.19)$$

The normalized gain factors g_s and g_L can now be defined as,

$$g_S = \frac{G_S}{G_{Smax}} = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}(1-|S_{11}|^2) \qquad (4.20)$$

and

$$g_L = \frac{G_L}{G_{Lmax}} = \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2}(1-|S_{22}|^2). \qquad (4.21)$$

Re-arranging (4.20) and (4.21) results in the equations for the centers C_S and C_L and radii R_S and R_L of constant gain circles at gains G_S and G_L as,

$$C_S = \frac{g_S S_{11}^*}{1-(1-g_S)|S_{11}|^2}, \tag{4.22}$$

$$R_S = \frac{\sqrt{1-g_S}(1-|S_{11}|^2)}{1-(1-g_S)|S_{11}|^2}, \tag{4.23}$$

$$C_L = \frac{g_L S_{22}^*}{1-(1-g_L)|S_{22}|^2}, \tag{4.24}$$

and

$$R_L = \frac{\sqrt{1-g_L}(1-|S_{22}|^2)}{1-(1-g_L)|S_{22}|^2}. \tag{4.25}$$

On a Smith chart, these equations represent constant gain circles as shown in Fig. 4.3. Any point along the radius of (4.23) represents a value for Γ_S which results in a gain of G_S. Similarly, any point along the radius of (4.25) represents a value for Γ_L which results in a gain of G_L. As shown in Fig. 4.3, in the unilateral case, the centers C_S and C_L will always lie along straight lines whose angle is that of S_{11}^* and S_{22}^* respectively.

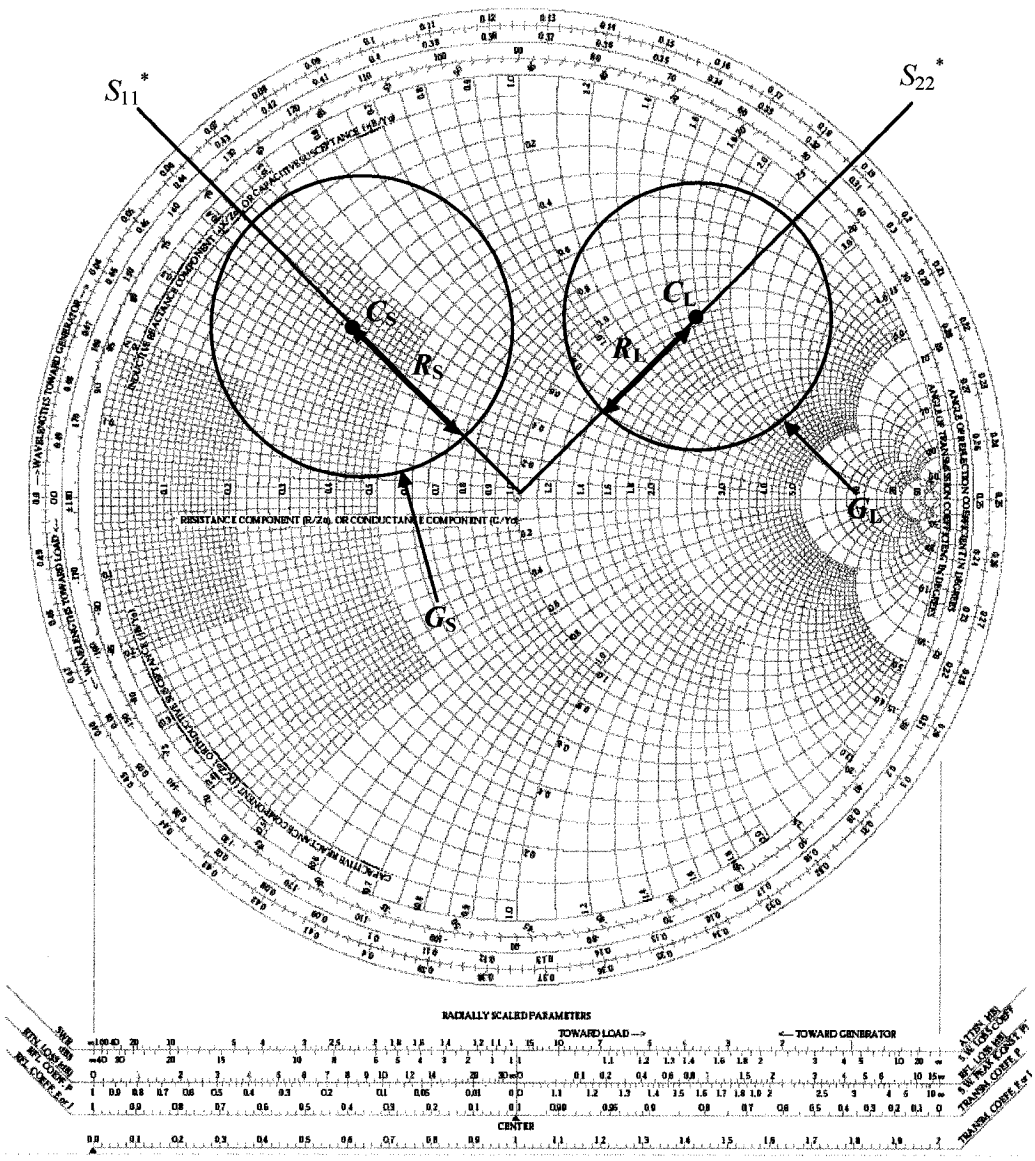


Figure 4.3 Smith Chart illustrating constant gain circles for the unilateral case.

4.1.4 Constant Gain Circles – Bilateral Design

In the bilateral case, $S_{12} \neq 0$. Therefore, any equations that depend on S_{12} need to be revisited. From equations (4.8)-(4.10), only (4.8) carries a dependency on S_{12} (*i.e.* Γ_{in} depends on S_{12}). As such, only the constant gain circle for the source port is altered (from the unilateral case). The maximized gain, G_S, in the bilateral case (*i.e.* when $\Gamma_S = \Gamma_{in}^*$) is obtained as [31],

$$G_{Smax} = \frac{1}{1-|\Gamma_{in}|^2}. \tag{4.26}$$

The normalized gain factor, g_s, can now be defined as,

$$g_S = \frac{G_S}{G_{Smax}} = \frac{1-|\Gamma_S|^2}{|1-\Gamma_{in}\Gamma_S|^2}(1-|\Gamma_{in}|^2). \tag{4.27}$$

The definitions for C_S and R_S in the bilateral case are now,

$$C_S = \frac{g_S\Gamma_{in}^*}{1-(1-g_S)|\Gamma_{in}|^2} \tag{4.28}$$

and

$$R_S = \frac{\sqrt{1-g_S}(1-|\Gamma_{in}|^2)}{1-(1-g_S)|\Gamma_{in}|^2}. \tag{4.29}$$

On a Smith chart, these equations represent the constant gain circle as shown in Fig. 4.4. Any point along the radius of (4.29) represents a value for Γ_S which results in a gain of G_S. As shown in Fig. 4.4, in the bilateral case, the center C_S will always lie along the straight line whose angle is that of Γ_{in}^*. While it may appear that the bilateral and

unilateral constant G_S gain circles are similar, the difference between them is significant. While in the unilateral case C_S and R_S depend only S_{11} and Γ_S, in the bilateral case, C_S and R_S depend on S_{11}, Γ_S, and Γ_{in}. Moreover, Γ_{in} depends on Γ_L. As such, designing the input network in the bilateral case requires that the output network be designed first.

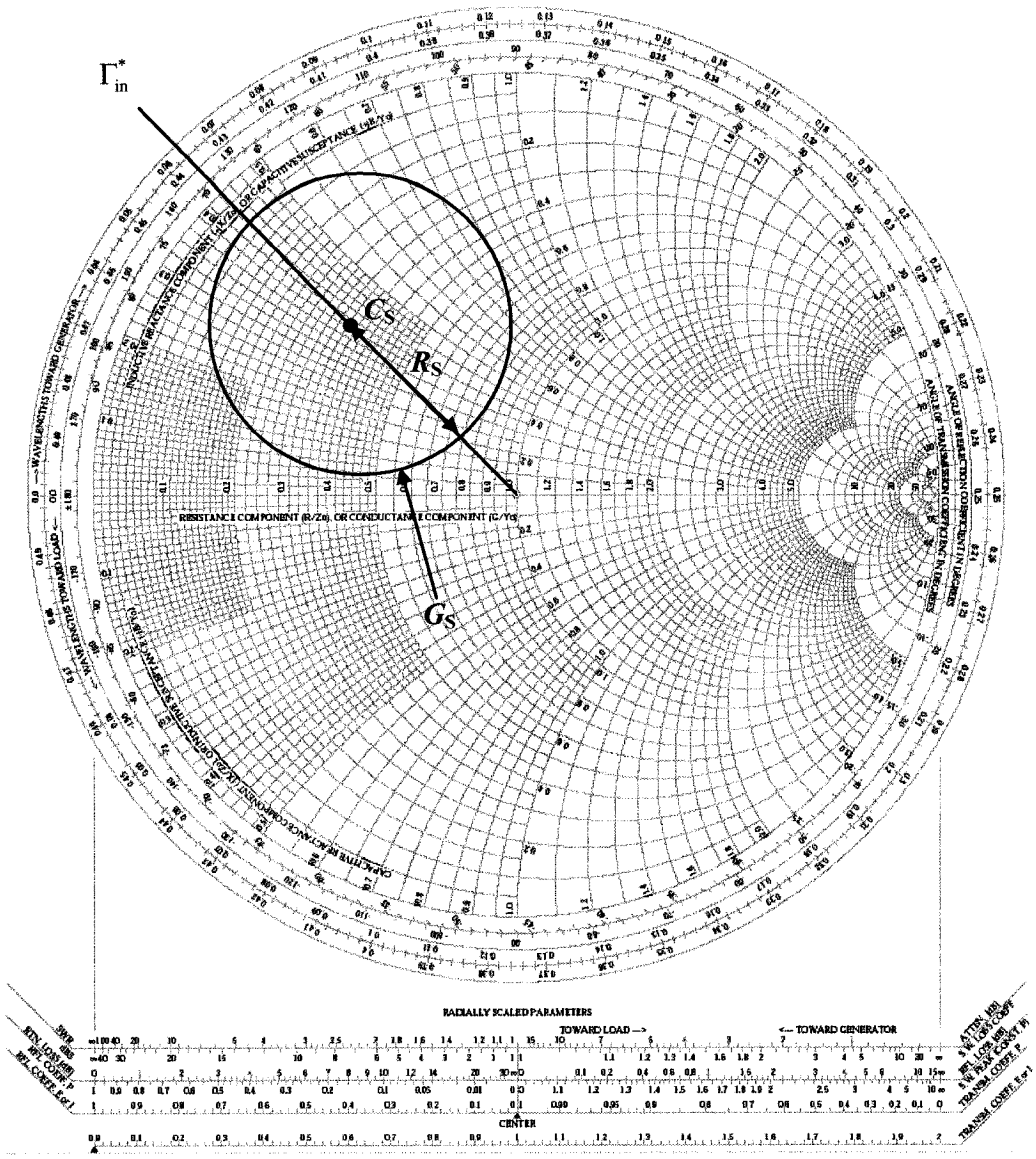


Figure 4.4 Smith Chart illustrating constant gain circles for the bilateral case.

4.1.5 Constant Noise-Figure Circles

Through derivations from [9] and [32], the equation for the center C_F and radius R_F of a constant noise-figure circle can be defined as,

$$C_F = \frac{\Gamma_{opt}}{N+1} \tag{4.30}$$

and

$$R_F = \frac{\sqrt{N(N+1-|\Gamma_{opt}|^2)}}{N+1}, \tag{4.31}$$

where C_F is a complex quantity, R_F is a scalar, Γ_{opt} is the optimum source admittance that results in the minimum noise-figure, and N is the noise-figure parameter given by

$$N = \frac{NF_D - F_{min}}{4R_N / Z_0}|1+\Gamma_{opt}|^2. \tag{4.32}$$

In (4.32), NF_D is the desired noise-figure, F_{min} is the minimum noise-figure for the transistor, R_N is the equivalent noise resistance of the transistor, and Z_0 is the characteristic impedance of the source (typically 50 Ω). Any point on the radius of the constant noise-figure circle represents a reflection coefficient that will result in a noise-figure NF_D, while the center of the circle is on a straight line whose angle is that of Γ_{opt}. Any point, *i.e.* reflection coefficient, within the circle results in a noise-figure between F_{min} and NF_D. Fig. 4.5 shows a Smith chart with one constant noise-figure circle.

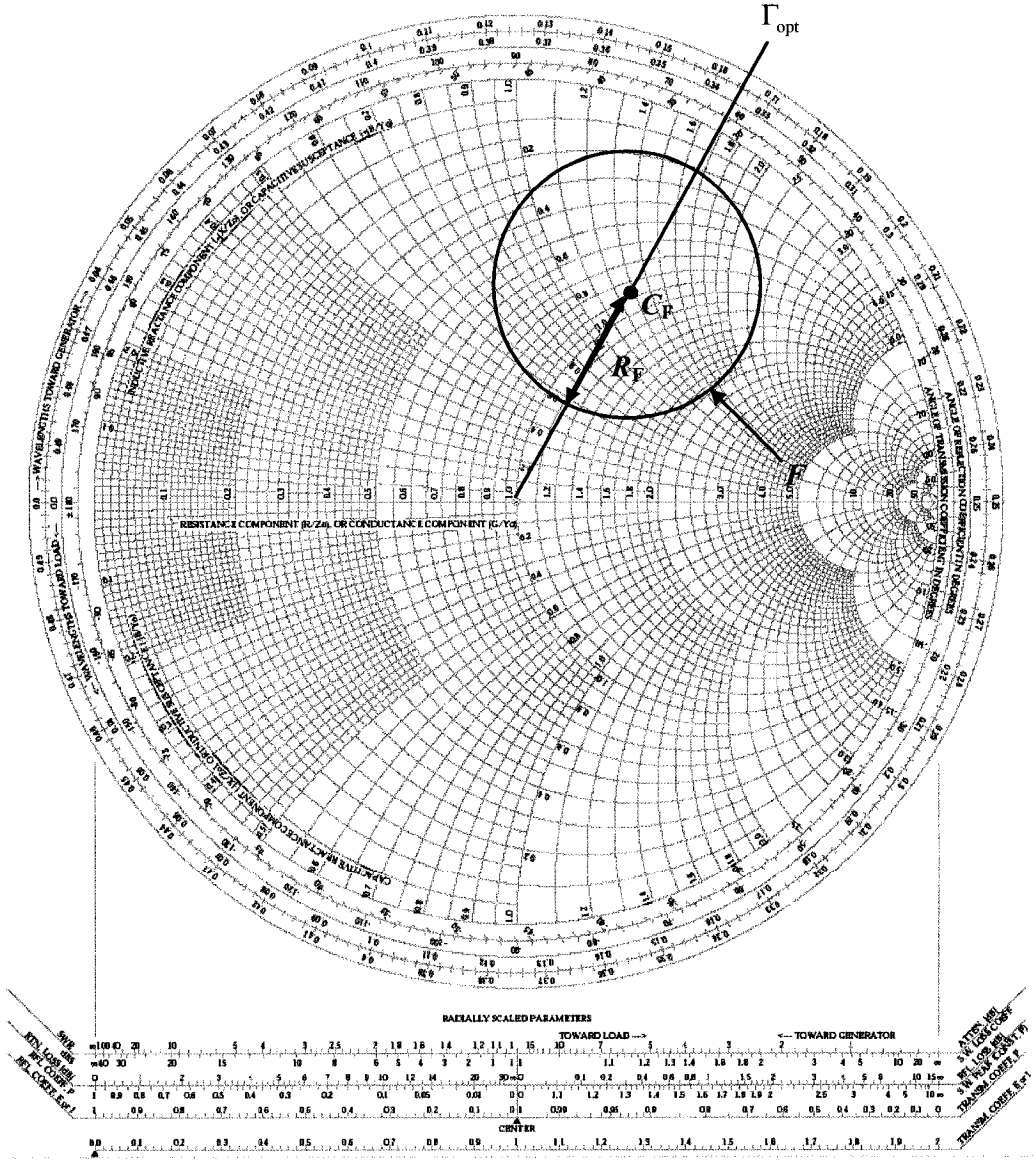


Figure 4.5 Smith Chart illustrating constant noise-figure circles.

4.1.6 The .S2P File

Critical to the automated nature of the proposed CAD approach to LNA design, is the .S2P file format. This file format is an industry standard that is recognized by most simulation software (*e.g. HFSS, ADS*, Spice etc.). For a particular device, its .S2P file will contain *S*-parameter (*i.e.* magnitude and phase) information at numerous frequency points. Moreover, many .S2P files contain noise related information such as Γ_{opt}, F_{min}, and R_N. This information can be very useful to designers as it relates actual device performance to design simulations. In the case of the proposed CAD approach, .S2P files are exploited to increase the approach's level of automation. A sample .S2P file is shown in Appendix A for a transistor device.

4.2 Proposed Approach

Recall from Chapter 2, Fig. 2.4, that the overall noise-figure of a cascaded system is given by,

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 G_3 \cdots G_n}. \tag{4.33}$$

As mentioned earlier, through equation (4.33), LNA's are placed at the beginning of a multi-staged system and are designed to have a low noise-figure (F_1) and a high gain (G_1). In the traditional approach to LNA design, a noise-figure is specified by the user, and the associated constant noise-figure circle is plotted on a Smith-chart. The goal is to

find a Γ_S (*i.e.* source reflection coefficient), which will result in a constant gain circle that touches the constant noise-figure circle at a single point. This task is achieved by a trial-and-error plotting of multiple constant gain circles until a satisfactory circle (not necessarily "the" best circle) is found. The point at which both circles meet represents the reflection coefficient that has both the desired noise-figure and the maximum possible gain at that noise level. Finally, the output reflection coefficient (*i.e.* Γ_L) is set to the conjugate of the transistor's S_{22} value so as to maximize the amplifier's overall gain. Because this approach relies on manually plotting circles on a Smith-chart and visually checking to see if the two circles meet, the accuracy of the final solution depends on how well these circles were drawn. Moreover, it may take several tedious manual iterations to find an acceptable gain circle. The RF/microwave CAD approach strives to solve these issues through the use of constrained line search optimization.

4.2.1 Unilateral Case

In this sub-section, the CAD approach for unilateral LNA design is presented. To begin, it is assumed that the transistor is unilateral (*i.e.* $S_{12} = 0$). In practice, S_{12} can often be ignored since the reverse signal path is due solely to the gate-drain capacitance which tends to be very small [9]. In fact, near-unilateral transistors are now available. Nevertheless, the assumption results in an error that is bounded by (4.15).

Considering the Smith-chart to be the complex reflection coefficient plane, it is possible to write the equation for a constant noise-figure circle as

$$(x - real\{C_F\})^2 + (y - imag\{C_F\})^2 = R_F^2, \tag{4.34}$$

where x and y represent the real and imaginary axes respectively, and C_F and R_F are given in (4.30) and (4.31). Similarly, it is possible to write the equation for a constant gain circle as

$$(x - real\{C_S\})^2 + (y - imag\{C_S\})^2 = R_S^2, \tag{4.35}$$

where C_S and R_S are given in (4.22) and (4.23). In the proposed approach, the .S2P file format is utilised to minimize the need for user-inputs and to automate the approach. In fact, the .S2P file associated with a transistor contains all the information needed to solve for the constant noise-figure circle (equation (4.34)) with the exception of desired noise-figure NF_D. An in house *MATLAB* script is used to read and extract all pertinent transistor information from the corresponding .S2P file. Since NF_D is a user-specification, all parameters in equation (4.34) are known. Hence, the LNA design problem is to find a $\Gamma_S = x + jy$, which will make equations (4.34) and (4.35) intersect. It is important to note that C_S and R_S are dependant on $\Gamma_S = x + jy$ through (4.20). Hence (4.35) can be re-written as,

$$(x - real\{C_S(x,y)\})^2 + (y - imag\{C_S(x,y)\})^2 = R_S(x,y)^2, \tag{4.36}$$

where x and y now represent the real and imaginary parts of Γ_S respectively. Re-arranging (4.34) to solve for y gives

$$y = \sqrt{R_F^2 - (x - real\{C_F\})^2} + imag\{C_F\}. \tag{4.37}$$

Substituting (4.37) into (4.36) leads to

$$\begin{aligned}&(x-real\{C_S(x)\})^2+[(\sqrt{R_F{}^2-(x-real\{C_F\})^2}\\&+imag\{C_F\})-imag\{C_S(x)\}]^2=R_S(x)^2\end{aligned}. \tag{4.38}$$

Equation (4.38) has only one unknown, *i.e.* x representing the real part of Γ_S. From a close inspection of (4.38), it may be seen that x may have two possible solutions. Geometrically, this makes sense since two overlapping circles could intersect at two points. To ensure that the two circles meet at one, and only one, point a constraint (the distance between the centers of the two circles must be equal to the sum of their radii), *i.e.*

$$\sqrt{(real\{C_S\}-real\{C_F\})^2+(imag\{C_S\}-imag\{C_F\})^2}=(R_F+R_S). \tag{4.39}$$

is added. Fig. 4.6 demonstrates this concept graphically. Equation (4.39) can be re-arranged as

$$F(x)=\sqrt{(real\{C_S-real(C_F\})^2+(imag\{C_S\}-imag\{C_F\})^2}-(R_F+R_S), \tag{4.40}$$

where $F(x)$ represents the equation to be minimized. The smaller the value of $|F(x)|$, the closer the two circles will be. When $|F(x)| = 0$, the two circles intersect at exactly one point. In the proposed approach, a line search based optimization technique is used to find a value of x that satisfies (4.38) and minimizes (4.40). It should be noted that other optimization techniques could also be employed to solve this problem. For instance, Newton methods are relatively advanced and could easily solve this sort of minimization problem. However, since the given problem has only one possible solution, the relatively

simpler line search approach is more practical. Once x is found, y can be solved for using (4.37) and hence Γ_S, C_S, and R_S become known. The line search optimization sub-routine is fully described in Appendix B. This line search optimization

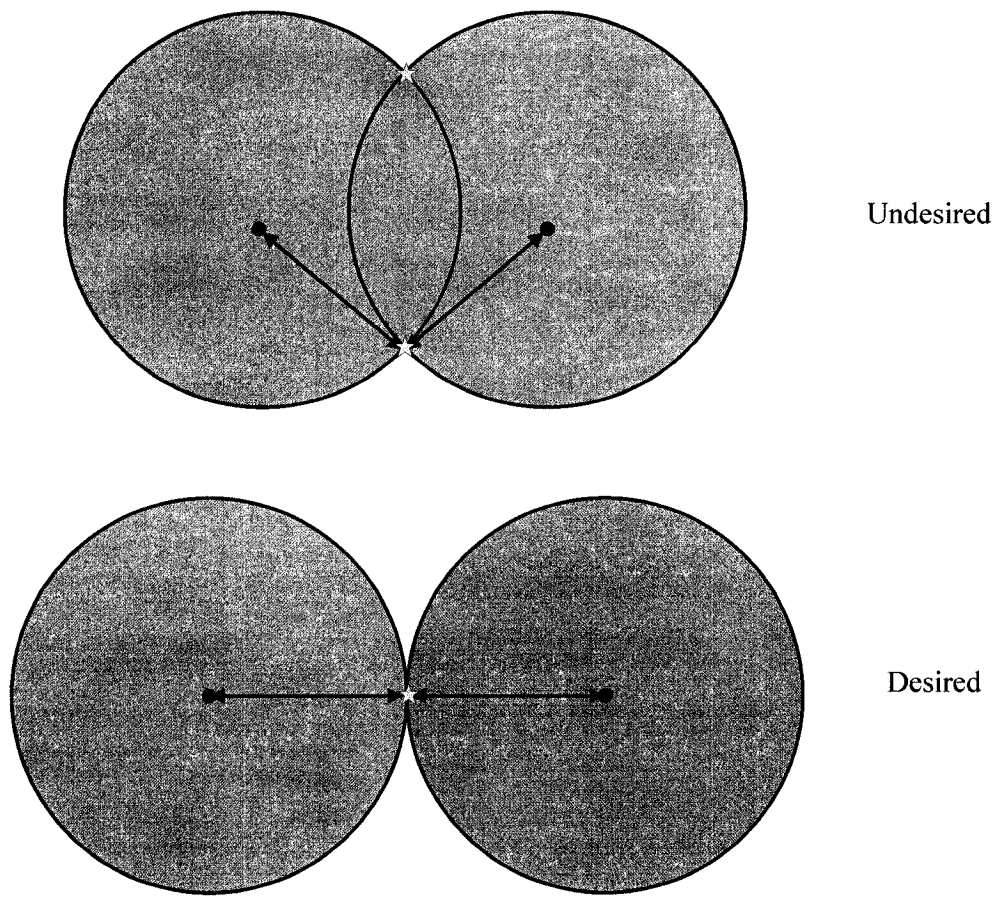


Figure 4.6 Illustration of how two circles meet at one or multiple point(s).

sub-routine allows the user to specify a resolution parameter, which determines the degree of accuracy of the final design.

4.2.2 Bilateral Case

In this sub-section, the CAD approach for bilateral LNA design is presented. As previously mentioned, the bilateral case differs from the unilateral case in that C_S and R_S now have an added dependency on Γ_{in} given in (4.3). From (4.3) it is observed that Γ_{in} depends on Γ_L. As such, in the bilateral case, the proposed CAD approach to LNA design begins by calculating the value of Γ_L. As in the unilateral case, Γ_L is set to S_{22}^* to maximize the overall gain at the desired noise level NF_D. With Γ_L known, Γ_{in} can be found using (4.3). It is now possible to write the equation for a constant gain circle as

$$(x - real\{C_S\})^2 + (y - imag\{C_S\})^2 = R_S^2, \tag{4.41}$$

where C_S and R_S are given in (4.28) and (4.29). As in the unilateral case, the LNA design problem is to find a $\Gamma_S = x + jy$, which will make equations (4.34) and (4.41) intersect. Once again it is important to note that C_S and R_S are dependant on $\Gamma_S = x + jy$ through (4.27). Hence (4.41) can be re-written as,

$$(x - real\{C_S(x,y)\})^2 + (y - imag\{C_S(x,y)\})^2 = R_S(x,y)^2. \tag{4.42}$$

Substituting (4.37) into (4.42) leads to

$$\begin{aligned}(x - real\{C_S(x)\})^2 + [(&\sqrt{R_F^2 - (x - real\{C_F\})^2} \\ &+ imag\{C_F\}) - imag\{C_S(x)\}]^2 = R_S(x)^2\end{aligned}. \tag{4.43}$$

Equation (4.43) has only one unknown, *i.e.* x representing the real part of Γ_S. To ensure that the two circles meet at one, and only one, point a constraint (4.39) is added. (4.40)

may again be used as a measure of how close the circles are to touching one another. The smaller the value of $|F(x)|$, the closer the two circles will be. When $|F(x)| = 0$, the two circles intersect at exactly one point. The line search sub-routine outlined in Appendix B is again applied to solve for the value of x in (4.43). Once x is known, the value of y, and consequently Γ_S, can be calculated using (4.37)

4.3 Illustration Examples

4.3.1 Unilateral Case

At 4 GHz, the .S2P file for a GaAs FET transistor gives the following S-parameters and noise parameters (Z_0 = 50Ω): $S_{11} = 0.6\angle -60°, S_{21} = 1.9\angle 81°, S_{12} = 0.05\angle 26°, S_{22} = 0.5\angle -60°$, F_{min} = 1.6dB, $\Gamma_{opt} = 0.62\angle 100°$, and R_N = 20 Ω. Making use of this transistor, the objective is to design an LNA that has a desired noise-figure (NF_D) of 2dB and an associated maximum gain. The RF/microwave CAD approach is employed.

From equations (4.14) and (4.15), $U = 0.059$ and the error in gain will be less than +/-0.5dB. The parameters in equations (4.30) through (4.32) are calculated and the equation for the constant noise-figure circle is found to be

$$(x + 0.097996)^2 + (y - 0.55576))^2 = (0.2416)^2. \qquad (4.44)$$

Given the user-desired resolution of 0.0001, the constrained optimization routine is executed. After 14 iterations, it is observed that $x = 0.1436$ minimizes (4.40), and

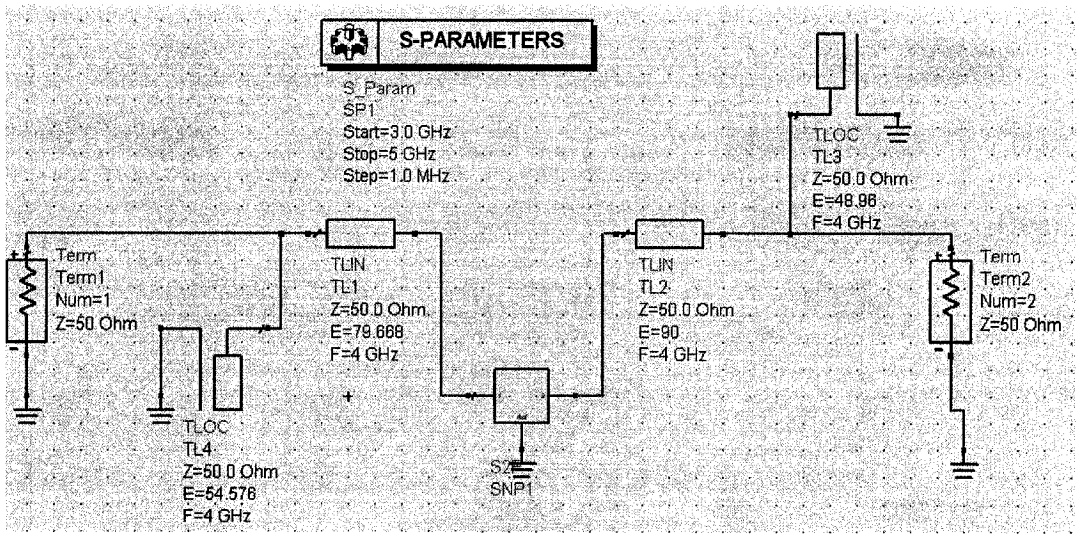


Figure 4.7 Unilateral LNA design using the RF/microwave CAD approach.

correspondingly $y = 0.5567$ and $\Gamma_S = 0.14136 + 0.5567j = 0.574\angle 75.752°$. Using stub-matching techniques and the calculated value of Γ_S, the circuit shown in Fig. 4.7 is simulated. A summary of the numerical results is shown in Table 4.1.

Comparing the value of $|F(x)|$ resulting from the traditional and the proposed approaches, it is obvious that $|F(x)|$ is much smaller in the latter case. As such, the proposed approach results in a design that meets the user-specifications to a much closer degree. Moreover, as a consequence of having a larger noise-figure, the design from the proposed approach is able to achieve a higher gain. It should be noted that in most iterative optimization routines that require an initial guess(es), the required number of iterations (to achieve convergence) greatly depends on the initial guess. In the proposed

approach, the initial guesses are limited to a number between zero and one (as is the case on the Smith chart), hence, the initial guesses are not particularly critical.

Table 4.1 Comparison of the Traditional and the Proposed Approaches

Metric	Simulation Results at 4 GHz	
	Traditional Approach [9]	Proposed Approach
C_S	$0.58\angle 60.0°$	$0.57767\angle 60.00°$
R_S	0.150	0.156
Number of gain circles solved	> 3	1
# of optimization iterations	None	14
$\|F(x)\|$	0.2376	0.0066
Gain	8.36dB	8.47dB
Noise-figure	1.47dB	1.99dB

4.3.2 Bilateral Case

At 4 GHz, the .S2P file for a GaAs FET transistor gives the following S-parameters and noise parameters (Z_0 = 50Ω): $S_{11} = 0.6\angle -60°, S_{21} = 1.9\angle 81°, S_{12} = 0.05\angle 26°, S_{22} = 0.5\angle -60°$, F_{min} = 1.6dB, $\Gamma_{opt} = 0.62\angle 100°$, and R_N = 20 Ω. Making use of this transistor, the objective is to design an LNA that has a desired noise-figure (NF_D) of 2dB and an associated maximum gain. The RF/microwave CAD approach is employed.

Recalling from sub-section 4.3.1, the calculated unilateral figure of merit, U, was 0.059. Hence, in this example, it is expected that the measured gain will be approximately +/-0.5dB more accurate. In the bilateral case, the first step is to calculate the output reflection coefficient (*i.e.* Γ_L) as the conjugate of the transistor's S_{22} value, *i.e.* $\Gamma_L = (0.5\angle -60°)^*$. Γ_{in} is now calculated as,

$$\begin{aligned}\Gamma_{in} &= S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \\ &= 0.6\angle -60° + \frac{(0.05\angle 26°)(1.9\angle 81°)(0.5\angle -60)^*}{1-(0.5\angle -60°)*(0.5\angle -60)^*} \\ &= 0.783829375\angle -55.56790046°\end{aligned} \tag{4.44}$$

The parameters in equations (4.30) through (4.32) are calculated and the equation for the constant noise-figure circle is found to be

$$(x+0.097996)^2 + (y-0.55576))^2 = (0.2416)^2. \tag{4.45}$$

Note, equations (4.44) and (4.45) are identical since the constant noise-figure circle remains the same in both the unilateral and bilateral cases. Given the user-desired resolution of 0.0001, the constrained optimization routine is executed. After 24 iterations, it is observed that x = 0.14360341 minimizes (4.40), and correspondingly y = 0.5558 and $\Gamma_S = 0.14360341 + 0.5558j = 0.57405\angle 75.513165°$. Using stub-matching techniques and the calculated value of Γ_S, the circuit shown in Fig. 4.8 is simulated. A summary of the numerical results is shown in Table 4.2.

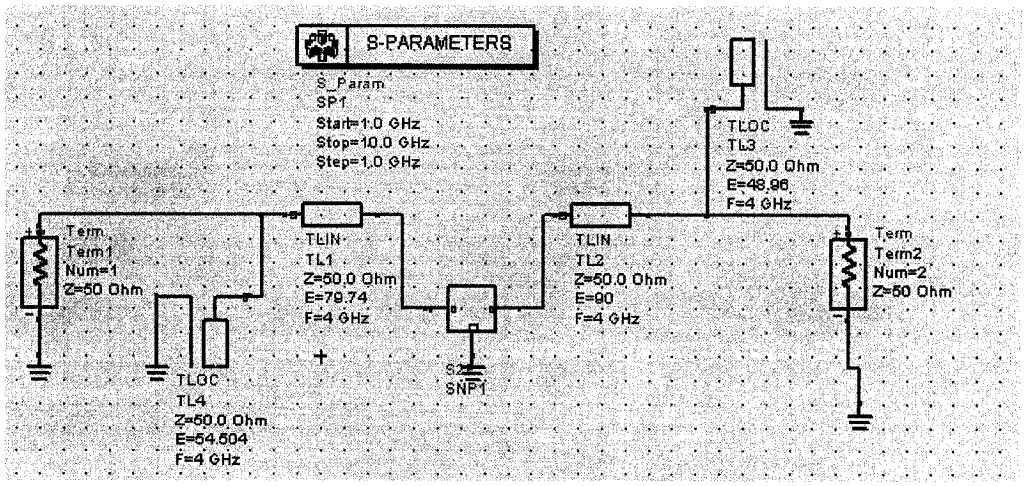


Figure 4.8 Bilateral LNA design using the RF/microwave CAD approach.

Table 4.2 Comparison of the Unilateral and Bilateral CAD Approaches

Metric	Simulation Results at 4 GHz	
	Unilateral	Bilateral
C_S	0.57767∠60.00°	0.577809∠60.0005°
R_S	0.156	0.1555
# of optimization iterations	14	24
$\|F(x)\|$	0.0066	0.0063
Gain	8.47dB	8.778dB
Noise-figure	1.99dB	1.9959dB

Comparing the value of $|F(x)|$ resulting from the unilateral and the bilateral cases, the bilateral case is able to achieve the slightly smaller value of 0.0063. As such, the bilateral case results in a design that meets the user-specifications to a closer degree. However, this added accuracy came at the expense of an additional 10 iterations of the line search sub-routine. Finally, the achieved gain in the bilateral case is 0.308dB larger, which is within the expected error gained from the unilateral assumption (*i.e.* +/-0.5dB). Note that in this example the value of S_{12} was relatively small (close to zero). In an example where S_{12} is larger, the discrepancy between the unilateral and bilateral cases will be significantly larger.

Chapter 5

Conclusions

5.1 Contributions

Traditional LNA design approaches from both analog and RF/microwave perspectives can de tedious, time consuming, and technically challenging. This thesis attempted to tackle the challenge of automating, through the use of computers, the design process for LNAs. Two separate perspectives were taken; an analog perspective and an RF/microwave perspective. While distinct in implementation, both design approaches have similar end goals:

- to reduce the required level of expertise needed;
- to ensure that the user-specifications are met/exceeded;
- to reduce the required design time;
- to increase the accuracy of LNA designs *w.r.t.* the user-specifications.

From a designer's perspective, selecting between either an analog or an RF/microwaves implementation is not obvious. Traditionally speaking, designers working with circuits below 3GHz tend to favor analog designs. The design of circuits for use above 3GHz traditionally employs RF/microwave designs. However, there is in fact no clear line. It is up to the reader to decide which perspective he/she is most comfortable with.

In this work, the analog CAD approach to LNA design is presented first. The framework integrates existing knowledge in the form of circuit topologies and pertinent sequences of design equations into a unified scheme. For the first time, the approach advocates a new perspective in terms of user-inputs, *i.e.* priority assignment to various LNA metrics. The approach is divided into multiple phases that are modular/systematic. Currently, the approach includes a topology menu, an SDE menu, an application menu, and a fine-tuning menu, all of which are expandable. For instance, with the advent of newer topologies, newer SDEs, and so forth, the tool can be easily upgraded (by updating Tables 3.1, 3.2, 3.2, and 3.4). The CAD approach has been illustrated *via* practical design examples. Simulation results show that effective designs often exceeding the user-specifications can be systematically derived. It has been shown that the CAD approach allows users to tilt the balance of the final LNA in favor of certain specifications by merely changing the corresponding a_i's. It should be noted that users of the given approach require a modest amount of design expertise. Clearly, a user must understand what specifications are of higher importance before he/she can input values of a_i. This expertise however, requires general engineering knowledge as opposed to specialized LNA design experience.

From the RF/microwave perspective, a CAD approach to LNA design which targets maximum gain for a desired noise-figure is presented. The automated approach avoids the need for both trial-and-error, as well as manual Smith-chart plots to find the largest possible constant gain circle that will meet the desired constant noise-figure circle. The problem has been formulated mathematically and solved employing constrained line search optimization. The proposed approach is shown to be highly accurate and is of practical use to RF/microwave engineers.

5.2 Future Work

Both perspectives presented in this thesis offer a scope for future work in terms of additions and improvements.

The systematic approach to analog LNA design employs concepts that can be easily applied to other electronic circuits. The concept of user-prioritized specifications has been shown to reduce circuit design and optimization times. This is because the approach is able to first concentrate on those specifications which are deemed to be of higher importance. The knowledge-base topology selection schemes and fine-tuning approaches could both be modified for other circuit types (*e.g.* power amplifiers, mixers, digital to analog converters etc.).

In the current version of the approach, the largest contributor to design time is in the generation of the 3D sensitivity plots used in the fine-tuning phase. Future work could include sub-routines aimed at reducing the required number of plots needed. Alternatively, sub-routines could be added that would reduce the time needed to generate

the fine-tuning tables (*e.g.* fully automate the link between MATLAB and *ADS*). For instance, by using interpolations techniques, the grid size (*i.e.* the number of points on the grid) required in the generation of the 3D plots could be reduced significantly.

The RF/microwave CAD approach to LNA design is based on line search optimization. This technique offers a scope for much future work. For instance, on a Smith chart it is possible to graphically plot stability bounds for the LNA design parameters. It would be worthwhile for the current approach to considering these limitations. In this way, resulting LNA designs would not only show maximum gain for a given noise-figure but would also guarantee stability. Currently, the proposed approach concentrates on gain maximization for a given noise-figure at a specific frequency. Alternatively, it is possible to offer designers the ability to maximize gain across a specified frequency range. While the center frequency gain may suffer, the overall gain bandwidth product would be improved. Additionally, it may be of interest to explore the possibility of designing an LNA for optimized performance both in terms of noise-figure and gain (as opposed to maximizing gain for a given noise-figure). By taking into account the noise and gain performance of the system in which the LNA is to be placed, the final LNA design could be ideally suited for maximizing gain and reducing noise-figure. Another interesting thought would be the application of the algorithm to other types of amplifier design, such as conjugately matched amplifier design, maximum stable gain amplifier design, power amplifier design, etc. Finally, the line search algorithm itself could be improved to reduce the number of required iterations and to increase its overall accuracy.

References

[1] T. Lee, *The Design of CMOS Radio Frequency Integrated Circuits*, Cambridge, U.K.: Cambridge Univ. Press, 1998.

[2] "Thermal Agitation of Electricity in Conductors," *Phys. Rev.*, v. 32, July 1928, pp. 97-109.

[3] "Thermal Agitation of Electric Charge in Conductors," *Phys. Rev.*, v. 32, July 1928, pp. 110-1139.

[4] A. van der Ziel, "Thermal Noise in Field Effect Transistors," *Proc. IEEE*, August 1962, pp. 1808-1812.

[5] A. van der Ziel, *Noise in Solid State Devices and Circuits*, Wiley, New York, 1986.

[6] D.K. Shaeffer and T.H. Lee, "A 1.5-V 1.5-GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, pp. 745-759, 1997.

[7] —, "Corrections to ' A 1.5-V, 1.5-GHz CMOS low noise amplifier'," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1397, Jun. 2005.

[8] "Uber spontane Stromschwankungen in verschiedenen Electrizitalsleitern" ["On Spontaneous Current Fluctuations in Various Electrical conductors"], Annalen der Physik, vol. 57, 1918, pp. 541-561

[9] D.M. Pozar, *Microwave and RF Design of Wireless Systems*, New York, NY: John Wiley & Sons, 2000.

[10] S. Di Pascoli, L. Fanucci, B. Neri, and D. Zito. "A new differential LNA topology for wireless applications," *Proc. IEEE ICECS*, Dubrovnik, Croatia, Sept. 2002, vol. 1, pp. 105-108.

[11] G. Nohra, R. Raut, and M. Sawan, "A 0.85V tunable gain 5GHz cascode low noise amplifier," *Proc. IEEE NEWCAS*, Montreal, QC, Canada, June 2004, pp. 353-356.

[12] T.K. Nguyen, C.H. Kim, G.J. Ihm, M.S. Yang, and S.G. Lee, "CMOS low-noise amplifier design optimization techniques," *IEEE Trans. Microwave Theory Tech.*, vol. 52, pp. 1433-1442, 2004.

[13] I.M. Filanovsky, "On design of narrow-band low-noise amplifiers with inductive source degeneration," *Proc. IEEE MWSCAS*, East Lansing, MI, USA, Aug. 2000, vol. 1, pp. 64-67.

[14] P. Andreani and H. Sjoland, "Noise optimization of an inductively degenerated CMOS low noise amplifier," *IEEE Trans. Circuits Systems II*, vol. 48, pp. 835-841, 2001.

[15] F. Gatta, E. Sacchi, F. Svelto, P. Vilmercati, and R. Castello, "A 2-dB noise-figure 900-MHz differential CMOS LNA," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1444-1452, 2001.

[16] M. Shouxian, M. Jian-Guo, Y.K. Seng, and D.M. Anh, "A modified architecture used for input matching in CMOS low-noise amplifiers," *IEEE Trans. Circuits Systems II*, vol. 52, pp. 784-788, 2005.

[17] L. Belostotski and J.W. Haslett, "Noise figure optimization of inductively degenerated CMOS LNAs with integrated gate inductors ,"*IEEE Trans. Circuits Systems I*, vol. 53, pp. 1409-1422, 2006.

[18] P.E. Allen and D.R Holberg, *CMOS Analogue Circuit Design*, New York, NY: Oxford University Press, 2002.

[19] N. Roy, M. Najmabadi, and V. Devabhaktuni, "A systematic approach towards the implementation of a low-noise amplifier is sub-micron CMOS technology", *Proc. IEEE CCECE*, Ottawa, Ontario, Canada, May 2006, pp. 1909-1913.

[20] K.J. Sun, Z.M. Tsai, K.Y. Lin, and H. Wang, "A noise optimization formulation for CMOS Low-noise amplifiers with on-chip low-Q inductors," *IEEE Trans. Microwave Theory and Tech.*, vol. 54, pp. 1554-1560, 2006.

[21] W. Zhuo, X. Li, S. Shekhar, S.H.K. Embabi, J.P. de Gyvez, D.J. Allstot, E. Sanchez-Sinencio, "A capacitor cross-coupled common-gate low-noise amplifier", *IEEE Trans. Circuits and Systems II*, vol. 52, pp. 875-879, 2005.

[22] M.Z. Khan, Y. Wang, and R. Raut, "A 0.65V, 2.4GHZ CMOS low-noise amplifiers design with noise optimization", *Proc. IEEE CCECE*, Saskatoon, Saskatchewan, Canada, May 2005, pp. 1751-1754.

[23] H. Fouad, K. Sharaf, E. El-Diwany, H. El-Hennaway, "An RF CMOS modified-cascode LNA with inductive source degeneration", *Proc. IEEE Radio Science Conference*, Espoo, Innopoli, Oct. 2002, pp. 450-457.

[24] Y. Wang, M.Z. Khan, and R. Raut, "A fully differential CMOS limiting amplifier with active inductor for optical receiver", *Proc. IEEE CCECE*, Saskatoon, Saskatchewan, Canada, May 2005, pp. 1751-1754.

[25] F. Beffa et al., "A 6.5-mW receiver front-end for Bluetooth in 0.18-μm CMOS," *IEEE MTT-S Int. Dig.*, Seattle, WA, USA, Jun. 2002, vol. 1, pp. 501-504.

[26] A. Pascht, J. Fischer, and M. Berroth "A CMOS low noise amplifier at 2.4 GHz with active inductor load," Silicon Monolithic Integrated Circuits in RF Systems, Digest of Papers. Topical Meeting on, Sept. 2001, pp. 1-5.

[27] L. Jeonghoon, K. Youngsik, "A 1.8V fully differential CMOS low noise amplifier with a special care for mixer input stage", Silicon Monolithic Integrated Circuits in RF Systems, Digest of Papers. Topical Meeting on, San Diego, California, Jan. 2006, pp. 4.

[28] B. Chi and B. Shi, "A 1.8V 2.4GHz CMOS ON-CHIP impedance matching low noise amplifier for WLAN applications", *Proc. IEEE ISCAS*, Bangkok, Thailand, May 2003, pp. 188-191.

[29] K. Wong-Sun, L. Xiaopeng, and M. Ismail, "A 2.4 GHz CMOS low noise amplifier using an inter-stage matching inductor," *Proc. IEEE MWSCAS*, Las Cruces, NM, USA, Aug. 1999, pp. 1040-1043.

[30] Lin Min, Li Yong Ming, and Chen Hong-Yi "A 0.18-u m CMOS LNAs with sub-2dB NF and low power for Bluetooth application," *Proc. IEEE ASIC*, Shanghai, China, Oct. 2001 pp. 815-817.

[31] G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*, Englewood Cliffs, NJ: Prentice-Hall, 1984.

[32] C. Gentile, *Microwave Amplifiers and Oscillators*, New York, NY: McGraw-Hill, 1987.

Appendix A

.S2P Example File

GHZ DB S R 50

!Freq	S11(dB)	S11(ang)	S21(dB)	S21(ang)	S12(dB)	S12(ang)	S22(dB)	S22(ang)
0.5	-6.83	-130.4	14.28	116.6	-25.96	-32.11	-6.493	88.3
0.75	-8.315	-176.6	14.39	58.17	-25.59	-76.93	-8.972	44.29
1	-9.136	137.6	14.1	5.361	-25.75	-117	-11.1	4.467
1.25	-9.681	91	13.64	-44.49	-25.6	-153.1	-13.3	-33.35
1.5	-9.933	45.01	13.1	-92.5	-25.39	173.4	-15.76	-68.61
1.75	-10.09	-0.7431	12.5	-139.4	-25.47	140.1	-18.64	-99.81
2	-10.17	-43.74	11.91	175	-25.16	107.4	-22.49	-122.1
2.25	-10.28	-83.98	11.29	130.3	-24.97	76.51	-26.44	-115.9
2.5	-10.8	-122.4	10.73	86.24	-24.05	44.2	-23.76	-101.3
2.75	-11.65	-160.1	10.2	42.44	-23.39	11.11	-19.56	-115.7
3	-13.25	161.5	9.737	-0.6358	-22.68	-22.68	-17.05	-141

0.5	1.118	0.1656	-96.62	0.1263
0.75	1.131	0.2488	-86.38	0.1463
1	1.145	0.3353	-78.08	0.1793
1.25	1.162	0.4226	-70.25	0.2303
1.5	1.181	0.5076	-62.54	0.3058
1.75	1.203	0.5869	-54.92	0.4133
2	1.228	0.6579	-47.48	0.5616

Appendix B

Line Search

In essence, the line search optimization algorithm is used to solve a single dimension minimization problem. In other words, line search is used to solve for an unknown in a highly non-linear equation. Line search is commonly used instead of Newton or Secant methods in problems where derivative information is unavailable or difficult to obtain. In the line search algorithm there is no need for derivative information. Instead, line search algorithms typically search a bracketed interval.

Let $F(x)$ be a highly non-linear equation with respect to x. It is desired to find a value of x such that $F(x) = 0$. In line search optimization, the value of x that minimizes $F(x)$ is sought within a given interval. Consider Fig. 1 below,

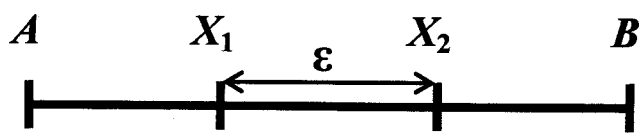


Figure 1 Interval in which the minimization solution is sought.

Here, A and B are the bounds to the search interval, X_1 and X_2 are any two points within the interval and ε represents the desired resolution. The line search algorithm is iterative in nature as it compares the values of $F(X_1)$ and $F(X_2)$ for different X_1 and X_2. When $F(X_1) < F(X_2)$, it indicates that the solution to the minimization problem is between points A and X_2 from Fig. 1. Thus in the next iteration, the search interval can be reduced in size. At each iteration, the search interval is reduced until the values of X_1 and X_2 are closer than the desired resolution. Below is a pseudo code for two-point (dichotomous) line search minimization.

Initialization: Set A as the lower bound and B as the upper bound of the search interval. Set the value of the desired resolution ε.

Step 1: Calculate the value of X_1 and X_2 using

$$X_1 = A + \frac{(B-A)}{2} - \frac{\varepsilon}{2}$$

and

$$X_2 = A + \frac{(B-A)}{2} + \frac{\varepsilon}{2}.$$

Step 2: Calculate $F(X_1)$ and $F(X_2)$.

Step 3: Compare $F(X_1)$ and $F(X_2)$.

-IF $F(X_1) < F(X_2)$ THEN SET $B = X_2$ and GO TO *Step 4*.

-IF $F(X_1) > F(X_2)$ THEN SET $A = X_1$ and GO TO *Step 4*.

-IF $F(X_1) = F(X_2)$ THEN pick new values for X_1 and X_2. Such that $X_1 < X_2$ and where $X_1, X_2 \in [A, B]$. GO TO *Step 4*.

Step 4: IF $F(X_2)$-$F(X_1) < 2*\varepsilon$ THEN STOP, OTHERWISE GO TO *Step 1*.

The value of ε can be adjusted until X_1 and X_2 are sufficiently close. At this point, both X_1 and X_2 will represent the value of x that minimizes $F(x)$. This optimization algorithm is comparatively CPU inexpensive as no derivative information is required. Caution must be taken when selecting the values of A and B. If the solution lies outside the search interval, the algorithm will not converge.