Design of Adaptive Amplifiers with DC Varying Inputs

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Abstract

Design of Adaptive Amplifiers with DC Varying Inputs

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Analog amplifiers are one of the most commonly used building blocks in electronic systems. Emerging circuit technologies create new systems and also new applications for signal amplification. A conventional amplifier operates at a fixed biasing point to transfer signals varying on a fixed DC level with a constant or variable gain. In some new systems, particularly those involving sensors, the DC component of a signal to be amplified can be variable, instead of fixed. The established design procedure is not applicable for such signals.

In this thesis, a design method for adaptive amplifiers is proposed. It is to design an amplifier that can adjust itself automatically to suit the DC level of the input voltage and the amplification gain is variable according to the input DC level. The amplifier is made to perform, from a small signal point view, a linear amplification with a fixed gain, but from a large signal point view, a nonlinear voltage transfer. The nonlinear character of its function makes the amplifier capable of operating with an input voltage of which the DC level can vary in a specified range and providing a gain adapting to the input DC level.

The proposed method has been used to design an amplifier for a voltage signal enhancement in a wide dynamic range current-to-voltage conversion circuit. The designed amplifier has four cascading stages, i.e., three simple common source amplifier stages and one source follower. The units are tuned to perform a nonlinear voltage transfer while keeping a local linearity. These units are combined to implement the characteristics needed for the signal enhancement. The circuit has been simulated and the results demonstrated that it is able to perform the required amplification of the signal varying on different DC levels with an input-dependent gain.

Table of Content

LIST OF FIGURES

LIST OF TABLES

Chapter 1

Introduction

Analog amplifiers may be the most commonly used analog building blocks in electronic circuits, and many other functional circuits are built on the basis of amplifier units. In general, analog amplifiers are considered as linear circuits and are expected to perform a linear signal transfer with a specific gain. With emerging applications and changing device technology, the methods of circuit design need to evolve continuously. There is more and more demand for amplification of a voltage signal of which the DC component cannot be fixed at one level. Moreover, in some applications, a variable gain is required, instead of a constant one. The functions of amplifiers for such applications are not linear any more, and new design methods for such amplifiers need to be developed.

The work presented in this thesis is in the area of analog amplifier design, aiming at widening the range of the DC input and making the gain adaptive to the input level. In this chapter, the motivation of the work is described, and the objective specified. Also the scope and the organization of the thesis are presented.

1.1 Motivation and the objective of the work

Most analog amplifiers are designed to perform a linear amplification. As the devices in circuits are nonlinear, small signal models are used for circuit analysis with the assumption that each of the devices operates at a particular biasing point, at which the characteristics are considered “linear”. In case of a voltage amplifier, if the input voltage level is shifted, driving one of the devices out of its biasing point, the circuit may not perform the designed amplification. In other words, the DC component of the input voltage needs to be at a particular level that matches the biasing point to secure the

normal operation condition. Hence there is almost no room for the input DC level to change. In the design of this kind of amplifiers, the efforts are made to improve the gain, the frequency response, or stabilization of the biasing points, instead of the tolerance to an input DC shift.

In the last couple of years, the technical evolution of electronic systems has created many new needs for signal amplifications. In particular, the development of sensor technology facilitates signal acquisitions from the environment. As digital circuits take many signal processing tasks away from analog circuits, the application of analog amplifiers in sensors has become very important. This research on analog circuit design needs to follow the trend.

A sensor converts a physical variable that may vary over a very wide range to a voltage or current signal. Such a signal can be seen as a combination of a DC component and small signal component. The former usually represents the background level and the latter the detailed information. In many cases, the small signal may not always vary on the same scale at the same DC component. In other words, the DC component of a signal to be amplified may shift. Conventional linear amplifiers described above may not be able to handle such an input signal. Moreover, as the input DC component can change within a range determined by the sensor acquiring the signal, the amplitude of the small signal may have a range of variation that is much wider than that of the conventional fixed-biasing one. In this case, the amplification gain may need to be variable, for example, a higher gain in case that the signal becomes weaker, in order to be able to respond to a wide range of excitations. There are some techniques developed to make the gain adjusted by a control voltage or current. However, it is hard to find an amplifier that functions if the DC component of the input is shifted significantly and also adjust the gain automatically to suit the input. Such an amplifier needs to have some nonlinear characteristics.

The commonly used methods for circuit design and analysis are not suitable for circuits having nonlinear characteristics. The objective of the work presented in this thesis is to develop a method of designing adaptive amplifier circuits having the following features :

1. Its biasing point adjusted automatically to suit the input level that can vary over a wide range.
2. Its amplification gain for the small signal is variable according to the input DC level. However, the gain should be fixed if the signal component of the input varies on a fixed DC level.

As mentioned previously, this kind of amplifier is mainly for sensor applications. They can also be used for other purposes. For example, a variable-gain amplifier can be used to compensate for a signal loss at a particular DC level, or to generate, from a waveform of uniform amplitude, a signal of which the amplitude is background-dependent.

1.2 Scope and organization of the thesis

Contrary to the use of the small signal models for circuit analysis under the condition of a fixed biasing, the design of the adaptive amplifiers should be based on the analysis of the circuit behavior under large signal conditions. The development of the proposed method requires a study on the very basic structures of MOS voltage amplifiers to investigate how the basic elements, such as the parameters of the devices employed, are related to the circuit biasing and signal amplification. Instead of maintaining the circuit biasing at a fixed point to avoid the nonlinear zone, it is important to explore the nonlinearity of these elements to make it possible for the amplifier to operate with its biasing point shifted and gain adjusted by the input. A simple circuit unit can be made to perform a simple signal transfer with a significant tolerance to an input DC level shift. Such a unit can also be tuned for amplification with a variable gain in a simple manner. A voltage amplifier of sophisticate input-dependent gain may be built by appropriately combining these units.

The thesis is organized as follows. In Chapter 2, the basics of analog amplifiers and existing work about variable-gain circuits are presented. Chapter 3 presents the development of the proposed design method. Using an example of voltage amplifier for compensation, the way of determining the characteristics of an adaptive amplifier is

described. Based on the study on the basic configurations of MOS amplifiers, two different approaches to varying the amplification gain and shifting the device biasing according to the input voltage are proposed in this chapter. In Chapter 4, the design of the voltage amplifier for the compensation is described to illustrate how the proposed method can be applied. The simulation results of the designed circuit are presented. And finally, the summary of the work is presented in Chapter 5.

Chapter 2

Background and review of existing work

In this chapter, the different techniques for creating amplifiers with wide dynamic range and adaptive gain are explored. Different methods are used for different tasks and it is important to look at how other people achieved adaptive gain or wide dynamic range in their own amplifier designs. Furthermore, as the designed amplifier will be applied to a specific type of input signal, it is necessary to study to behavior of the wide dynamic range and high sensitivity current to voltage converter shown in [Wang10].

This chapter is separated into four different sections. The first section is an overview of basic amplifier designs. The second is a study of various methods to insure wide dynamic range. The third section is devoted to the various methods for varying gain. As for the final section, it will contain a review of the I-V converter, to make it possible to understand the details of the circuit that cause the particular signal.

2.1 Amplifier basics

As a technology, amplifiers are as old as the semiconductors they are made of. Some of the earliest types of MOSFET voltage amplifiers are the basic common source, common gate and common drain amplifiers, shown in Figure 2.1. These amplifiers have spawned a wide range of different types for modern applications such as cascode, differential, and folded amplifiers [John97]. Novel applications were created for different kinds of tasks such as high frequency power amplifiers for transmitters, high gain current to voltage converters, or transimpedance amplifiers, and low-voltage compact amplifiers. Complex designs were created to achieve things such as constant gain under multiple conditions and programmable amplifiers that operate in many different conditions. It is thus necessary to design a class of amplifiers for our specific requirement and use.

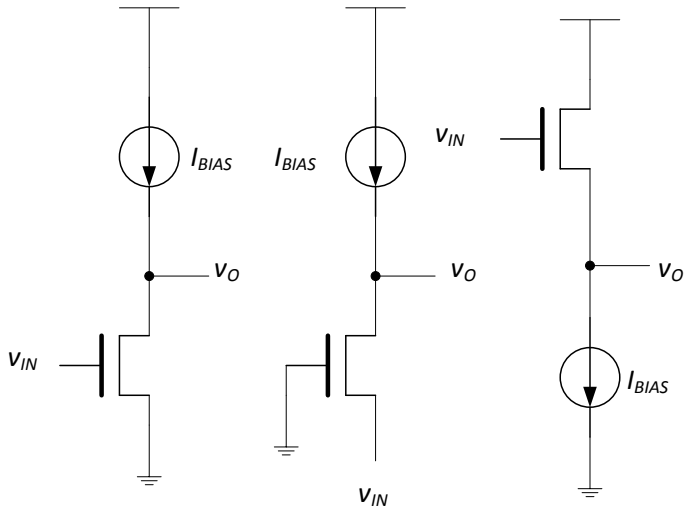


Figure 2.1: Common source, common gate, and common drain amplifier.

The classical operation mode of an amplifier involves a certain set of operating conditions. Amplifiers must have their transistors operate in the saturation region and the biasing current of the amplifier, defined as I_{BIAS}, should be a fixed value. When operating under these conditions the amplifier can be simplified into a linear device described in the small signal model. The small signal model of the common source amplifier is shown in Figure 2.2, the common source amplifier is selected as it is the most popular basic type for low frequency amplification.

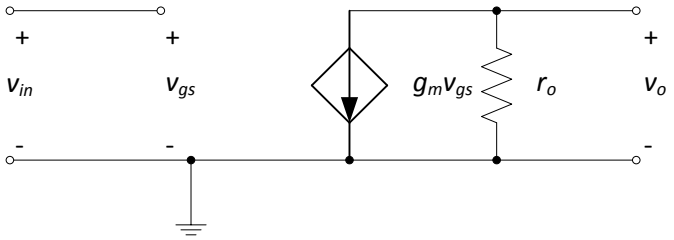


Figure 2.2: Small signal model of the common source amplifier.

In this simplified model there are two circuit elements, the voltage controlled current source (VCCS) and the amplifiers inherent output resistance, r_o. The transconductance of the transistor, g_m, which in the small signal model, serves as a multiplier to the input voltage, is set by the bias current, I_{BIAS} as we can see here from [Sedr04]

$$g_m = \sqrt{2k_n' \frac{W}{L} I_{BIAS}} \quad (1)$$

where k_n' and W/L are fundamental properties of the transistor. The resistance r_o is also controlled by the same current as

$$r_o = {}^{V_A}/_{I_{Bias}}. \quad (2)$$

where V_A is the early voltage of the transistor. Thus, the gain of the amplifier is a fixed value of $-g_m r_o$, and this value of gain is only for a specific bias current. This assumption is flawed when the DC level of V_{GS} or I_{BIAS} varies, and as the objective of this thesis is to design an adaptive amplifier that operates with varying DC level, it is necessary to look beyond the basic small signal model. Alternatively, if we have multiple biasing points for the same amplifier, with a different $-g_m r_o$ value at each level, then we have an amplifier whose gain is controlled by the input DC level.

Conventional amplifier design does not commonly discuss this fact. Modern amplifiers are mostly oriented around higher gain, greater frequency response, or greater linearity. The popular use of differential amplifiers partially shields modern amplifiers from the effect of DC level variation but not enough for the requirements set out in this research. The amplifiers to be designed for this thesis must accept a larger amount of input DC level variation and also have variable gain. Thus it is necessary to look at amplifier designs that achieve these two conditions.

2.2 Amplifiers with a varying bias current

Amplifiers that can accept input signals whose DC level varies, are very important for this research. In differential amplifier designs, the issue of varying input DC level is usually solved through designing the amplifier to have very low common-mode gain, i.e. the gain of the portion of the signal shared by both inputs is very low. This solution however is exclusive to differential amplifiers. As this solution is impossible for a single input signal a different technique must be found.

One method to control for input DC level variation is a negative feedback offset canceller. The principle is to include an element to the circuit that receives the DC output level as its input and corrects the amplifiers input to have the proper bias point such as in [Song00]. The advantage of such a system is that it is automatic, but it carries the risk of causing excessive attenuation at the output if it is not properly designed.

A different solution is to vary the bias current of the amplifier. A dynamic amplifier such as the one in [Host80] uses changing bias current in a clocked system. At the beginning of the clock pulse, the amplifier has maximum current for fast switching then as time advances the bias current is reduced, increasing gain. This principle was later used in [Degr82] where the bias current of the amplifier is made to be dependent on the input signal. In this case the idea is principally applied to reduce power consumption as the bias current switches off when there is no input signal and fully turns on when there is one. In another paper, [Baze91], we are presented with a pair of self-biased amplifiers. These amplifiers, shown in Figure 2.3, use a negative feedback system to change the bias current in order to always maintain the amplifier in the ideal bias point for the input signal. This system is very interesting as it does not require any kind of control signal, which also makes it resistant to process and temperature variations. Unfortunately it also means that the change in biasing cannot be controlled independently, making it impossible to use this particular technique for modifying the gain. Alternatively, if the signal controlling the biasing is controlled by the input signal or something related to it, there is the possibility of modifying the bias with a more complex control which could allow for gain variation.

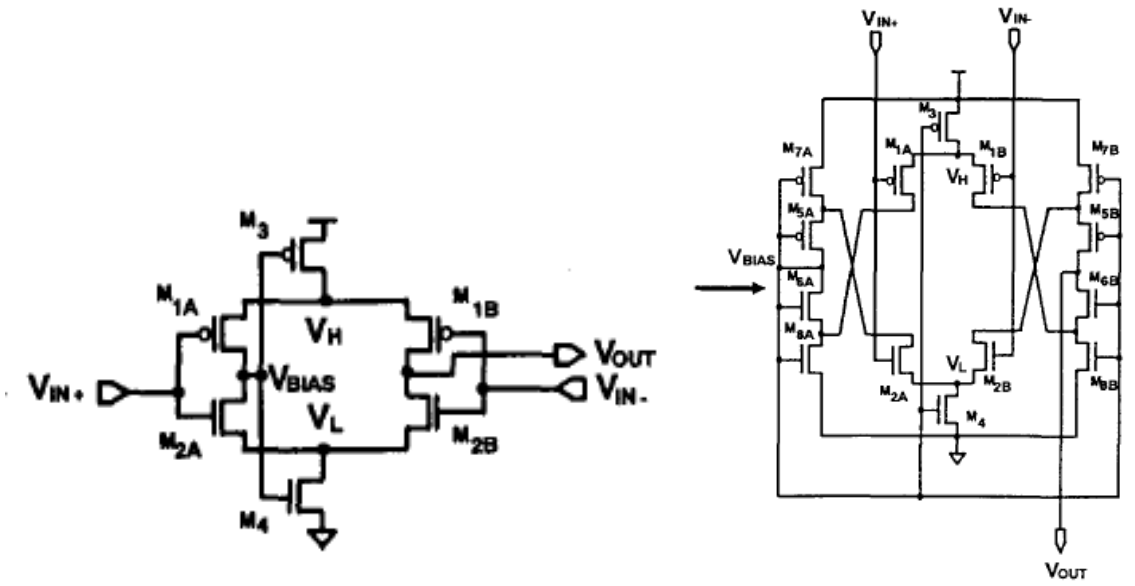


Figure 2.3: Diagram of a complementary self-biased differential amplifier and a very-wide-common-mode-range differential amplifier. Both are taken from [Baze91].

2.3 Variable gain amplifiers

The other objective of this research is to design a variable gain amplifier. Variable gain amplifiers are used in all sorts of fields and technologies such as transmitters, receivers, audio equipment, video equipment, and even cochlear implants as in [Sarp98]. These amplifiers create this variable gain through a wide variety of different methods that will be explained here, however, one thing that they have in common is that they are almost all designed to generate exponential gain change (linear in dB scale) from a linear control voltage.

First of all let us discuss the digitally controlled variable amplifiers. Digital amplifiers can be quite simple, as in [Park12] which has only three distinct gain levels. However, to make it possible to generate the same kind of gain various as is required, with the necessary level of accuracy, would have to be quite large. In this case, digital amplifiers mean amplifiers with components that switch on or off depending on the gain requirement. The other type of digital amplifiers are the sort that have a digitally

generated control signal, for the purpose of this research they are treated as analog amplifiers as their behavior is no different if given a continuous control signal. Two broad methods of digital control are presented here, current multiplication / division, and feedback switching.

A current multiplying or dividing amplifiers has multiple circuit elements that are either turned on or off in order to change the gain. In [Elwa99], a pair of series connected amplifiers are separated by a current division network as shown in Figure 2.4. Thus this current divider operates as a kind of attenuator between the stages allowing the gain of the complete circuit to vary. Alternatively these multiple groups of parallel elements can be integrated into the amplifier itself, in [Parl12] the variable gain amplifier has enough parallel current sources and source resistances to create 64 distinct gain levels, and [Xian11] has three stages of highly variable amplifiers and one fine-tuning stage. Finally, there is [Kang10], which demonstrates not only a parallel group of cascode elements that can be switched on or off, but also switched shunt resistors that are used to attenuate the gain of the amplifier. These circuits have very accurate gain control but require a digital control signal, which would require an A/D converter. Thus it is best to concentrate on analog solutions.

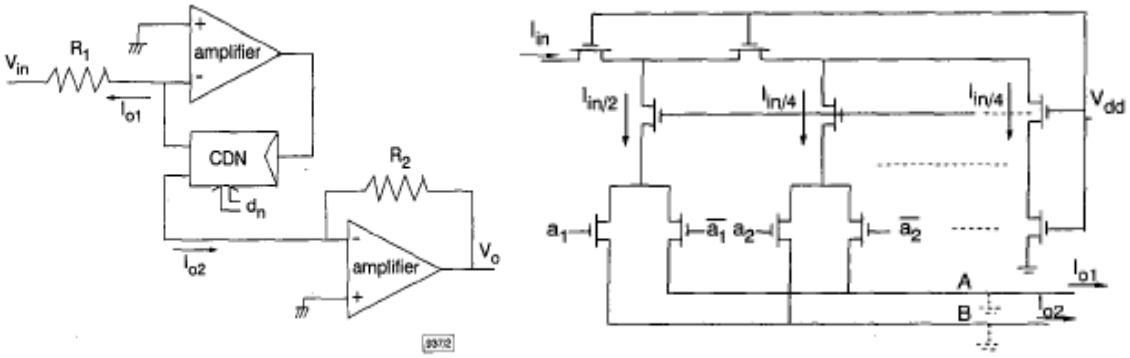


Figure 2.4: digitally controlled VGA and the current division network as shown in [Elwa99]

One analog method to vary an amplifiers gain is to control the bias voltage of the cascode element in a cascode differential amplifier. In [Song00] the individual variable gain amplifiers (VGA) have their gain controlled by the cascode bias as seen in Figure

2.5. Modifying the cascode impedance will vary the output DC level which is why the circuit also incorporates a offset canceller. Alternatively, in [Kim12] the compensation for changing DC level is integrated in the amplifier itself. On the other hand, [Kwon03] modulates the cascode bias, the drain voltage of the amplifying pair, and the source resistance at the same time. This way the output voltage is not affected by the change in gain.

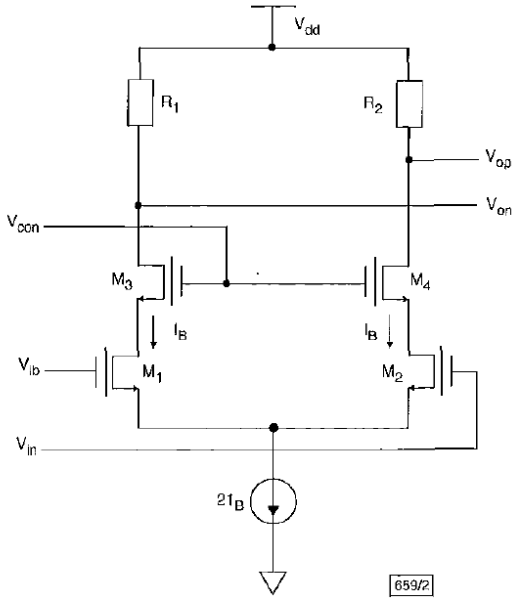


Figure 2.5: Variable gain amplifier cell used in [Song00]

Another alternative method, involves a negative feedback control, where the amplitude of the output of the amplifier is reduced by some form of attenuating element. The design in [Mang00] shows both a basic form such as having a pair of diode connected transistors as shown in Figure 2.6 (a), and the far more advanced feedback amplifier based design shown in Figure 2.6 (b). Though this solution appears to be rather basic, the properties of diode connected transistors causes the amplifier to have its gain vary exponentially based on the input signal. Furthermore, no separate control signal is needed as the control of the feedback element is done directly by the output. There is however a pair of disadvantages to this technique. The immediate problem is that the gain of such an amplifier is somewhat limited as the variability comes from reducing the gain at certain input levels. The other issue is that the exponential change in gain cannot be

controlled, making it impossible to use these amplifiers to generate complex gain variation as it would be required of the amplifier in this thesis.

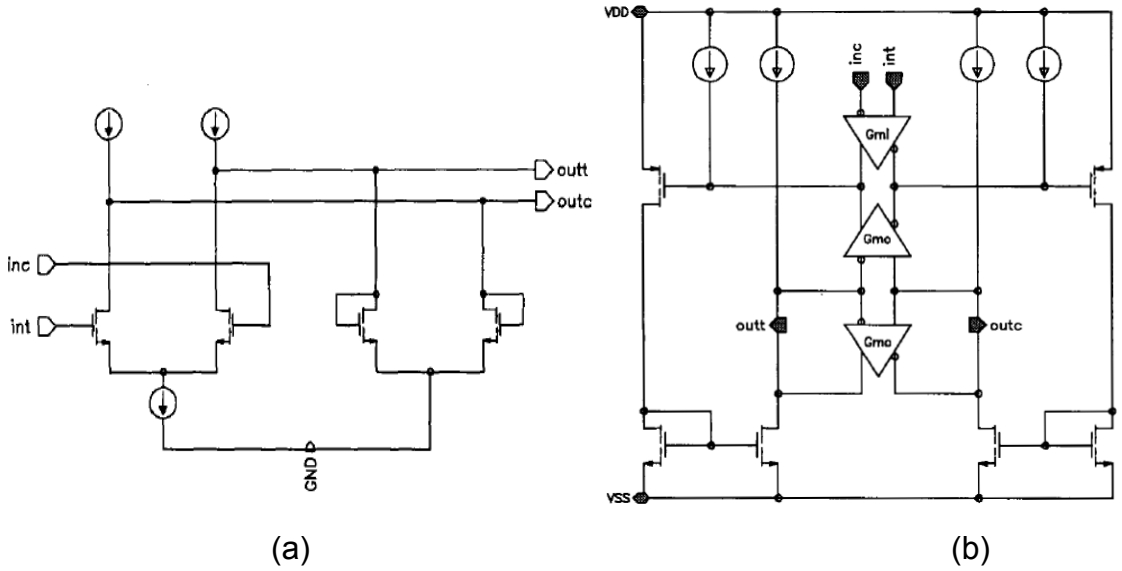


Figure 2.6: Two forms of feedback based variable gain amplifiers, both from [Mang00].

Yet another method to vary the gain is by modifying the bias current of the amplifier. Bias current modification was mentioned previously as a means of giving an amplifier a wide dynamic range. It can also be used to vary the gain. In [Hsie12] this is accomplished by adding a separate branch of current injection to a current-steering amplifier. Alternatively, in [Gaba11] the control voltage modulates the bias current and transconductance of a combiner transistor. A third option is to directly control the voltage of the bias transistors, just like it is done in [Yama02]. In all these cases this technique is used to give the amplifier excellent high frequency response in the GHz range. A different gain variation technique is also found in high bandwidth designs. In [Chen11] the distributed amplifier has its gain varied by modifying the gate bias or the voltage at the source of the amplifying transistor.

The last method for varying gain that is presented here involves varying the source or degeneration resistance. In [Huan98] this is achieved by varying the gate voltage of the amplifiers source resistance. Another option is found in [Yu11] where the

varying source resistance is combined with a signal summing system that further varies the amplifiers gain as we can see in Figure 2.7. This particular technique is very interesting as a source resistance can be incorporated into almost all different kinds of amplifiers, such as for example the basic amplifiers shown in Figure 2.1.

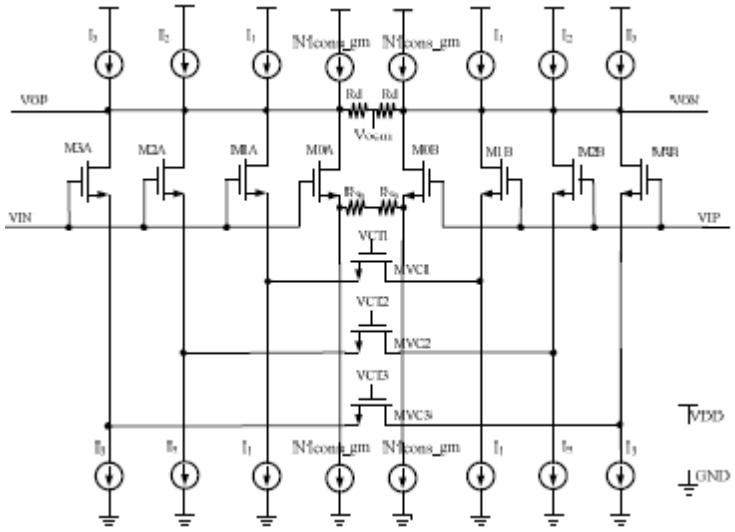


Figure 2.7: Variable source resistance and signal summing amplifier from [Yu11].

Finally there are three particular variable gain amplifiers that should be discussed in a deeper fashion. The first of which is the analog cochlear variable gain amplifier presented in [Sarp98]. The cochlear amplifier is a large device composed of multiple gain stages, for the purpose of this research we will look at only a single stage of the whole adaptive amplifier. The amplifier is composed of three distinct elements. The amplification is performed by a pair of wide-linear-range transconductance amplifiers, In the paper, their primary objective is to serve as a second order filter for the input signal. The offset-adaption circuit (LPF and OCR) is used to correct for DC level error, it is a negative feedback circuit that corrects the amplifiers DC output level. The last element is the Inner hair cell and peak detector (IHC & PD), it generates an output signal which is received by the Tau & Q control element that modifies the bias current of the two amplifiers. In this case this control has no feedback, it is input control, which makes the circuit resistant to instabilities and oscillations. The cochlear circuit is not specifically designed for high gain but its control circuits show the breath of options available to this research work.

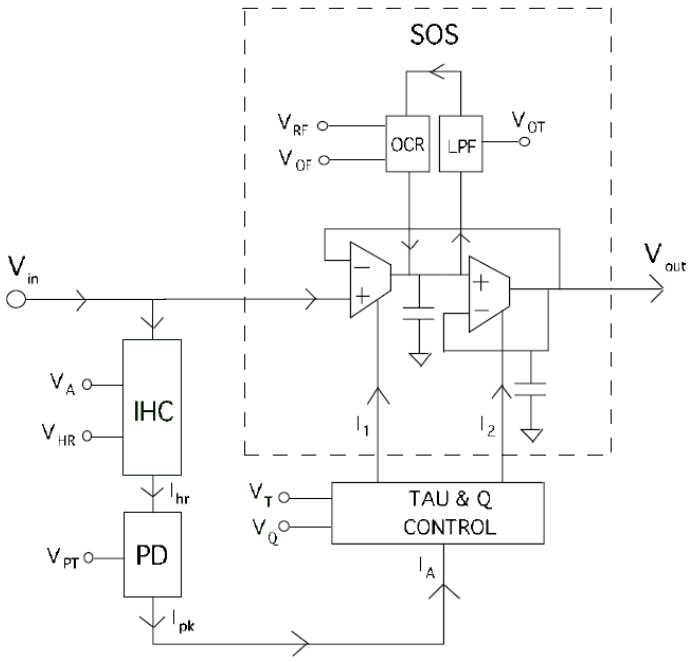


Figure 2.8: Single cochlear amplifier from [Sarp98]

Another paper that warrants a closer investigation is [Rijn96], this wide-range variable-gain is based on a single input with reference voltage and then contains an integrated single to differential converter. It is one of the few papers designed to work with single sided inputs, and also one of the few papers that discusses linear input range variation. The variable gain amplifier is shown in Figure 2.9, in it we can see that the use of a differential amplifier allows for a digitally controlled variable degenerative resistance. The reference voltage input makes it possible for the amplifier to accept a DC level variation equivalent to roughly 30 % of the full DC range (1 V to 2.5 V in a 5 V circuit) and the amplifier. This amplifier would thus be applicable for the same kind of input as the one generated by the I-V converter. Furthermore it is interesting to mention that since this circuit takes a DC varying single input, and outputs a DC stable differential output, it could be combined with any of the other differential variable gain amplifiers in a multiple stage system.

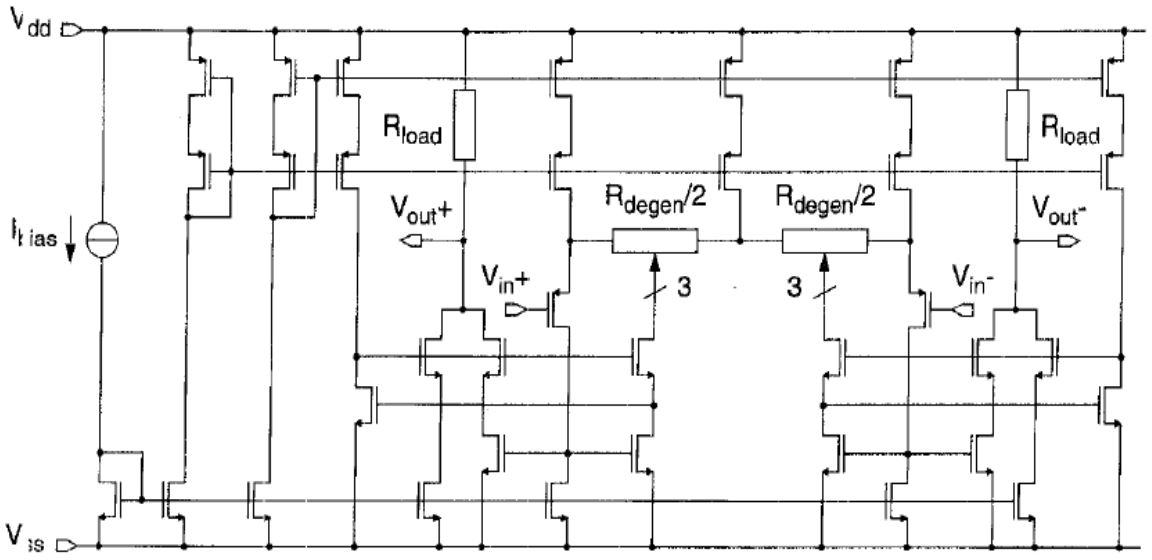


Figure 2.9: Variable gain amplifier found in [Rijn96].

The last variable gain amplifier paper that requires a deeper look is in [Duon06] whose variable gain amplifier can be seen in Figure 2.10. It incorporates variable source resistance and output degeneration to modify the gain. Furthermore, the common-mode feedback circuit corrects the bias current to a level controlled by the reference voltage. Note however that this circuit is not designed to handle DC level variation, it merely has the elements necessary to correct it. The variation in DC level would alter the amplifiers gain, requiring the control signal that modifies the amplifiers gain to take this variation into account.

No matter what technique is used to vary the gain, it must conform both to the requirements of the intended output signal, and to the type of input signal that the amplifier will receive. It is thus essential to study the I-V converter that will serve as the generator of the test input signal in order to select the right kind of gain variation technique.

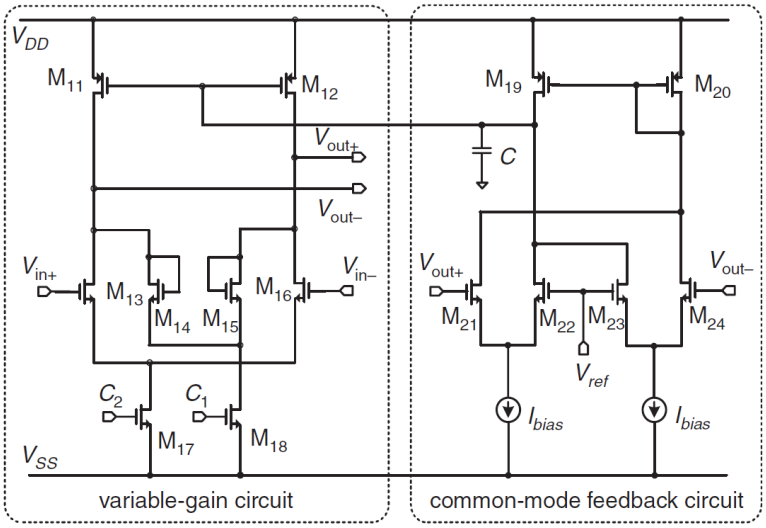


Figure 2.10: Variable gain amplifier as shown in [Duon06]

2.4 Wide-dynamic-range transimpedance amplifier

A transimpedance amplifier is a current to voltage converter. The particular converter shown in [Wang10] is designed for a wide dynamic range coupled with high sensitivity. These two factors are often incompatible with each other, however this circuit contains a method that preserves both these factors. This method is important as it is essential to prevent the output voltage from saturating which would lead to a loss of signal information.

The amplifier is shown in Figure 2.11. Since the input signal is composed of two parts a DC and signal portion that is treated as $i_{IN} = I_{IN} + i_{in}$, the current to voltage converter treats both parts with two separate methods. The first part converts the DC component into a voltage with a nonlinear compression. The second part involves applying a "locally linear" conversion to the signal component of the input current.

The "locally linear" conversion has large gain when the DC input current is small and small gain at the highest part of the circuits operating range. Since the signal variation is always small compared to the DC component (no greater than 20%) and the DC variation is multiple orders of magnitude then we can treat the DC gain as fixed for

any one DC current. As such the gain can be treated as being adaptive, reducing its value as the input current increases. This makes it possible to read the proportional magnitude (percentage of signal current compared to the DC current) of the output voltage signal for a very wide range of input current signals.

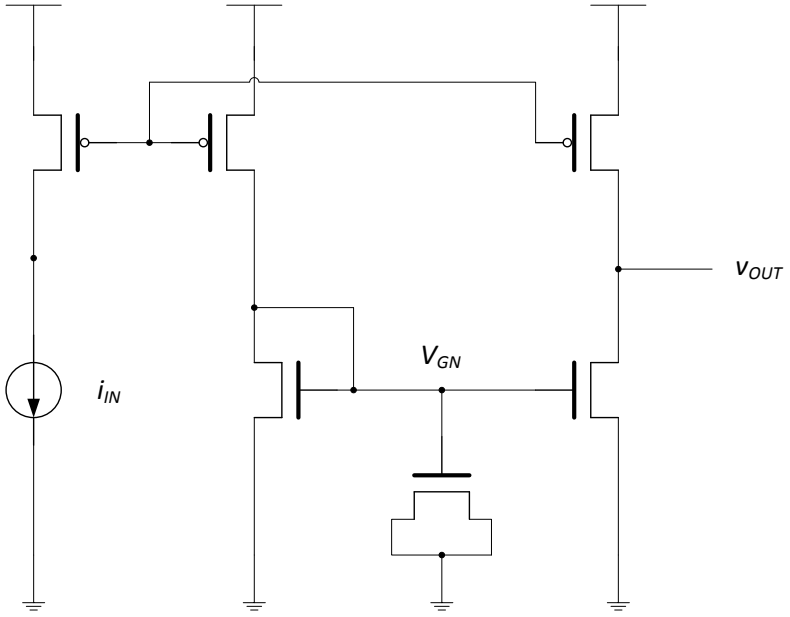


Figure 2.11: Basic I-V converter shown in [Wang10].

To generate the voltage to current conversion it is important to maintain a decent lowpass filtering in the circuit. The necessary condition is a large τ value defined as $\tau >> f_{min}$ and $\tau = C/g_{m1}$. Since the transconductance, gm_1, cannot be controlled easily, this circuit instead maintains a large capacitance to maintain the above condition. The negative consequence however is that this capacitor requires a large allotment of space in the fabricated circuit.

2.5 Summary

In this chapter we have looked at the basic principle of amplification. How the standard small signal model is based on a certain set of requirements such as a fixed bias current and fixed gate voltage level. The type of signal our amplifier is designed for is does not conform to the small signal model.

Thus we have looked at other peoples work in DC level correction and variable gain, such as self-biasing amplifiers, shunt resistors, or variable source resistance among other. Almost all of the presented methods ignore the possibility of varying input DC level and instead concentrate on generating a specific exponential gain according to a linearly changing input signal.

Finally we have looked at the I-V converter for which this class of amplifiers is designed. The I-V converter generates a certain type of output, an output with varying DC level and amplitude. Replacing the capacitor with a much smaller version reduces the converters output signal amplitude to an unacceptable level. Thus it is necessary to design an amplifier to replace this loss.

The amplifier must be designed to operate with a varying input DC level and also generate variable gain. None of the amplifiers presented here are designed for this particular task. Thus it is necessary to design a new sort of variable gain amplifier specifically designed for these requirements. In the next chapter we will do a detailed study of the behavior of the amplifiers input signal and present the methodology to design a wide range adaptive amplifier.

Chapter 3

Design of the adaptive amplifiers with a varying DC input level

As mentioned previously, the objective of the research work presented in this thesis is to develop a method of designing a kind of adaptive amplifier in which the biasing point is shifted automatically to suit a wide range of the input DC levels and the voltage signal gain varies to adapt to the input level in a defined way, contrary to the biasing stability and the signal transfer linearity of conventional amplifiers. Moreover, the circuit operation should be made locally linear, i.e., the output voltage signal amplitude being proportional to the input one if the input DC level is fixed.

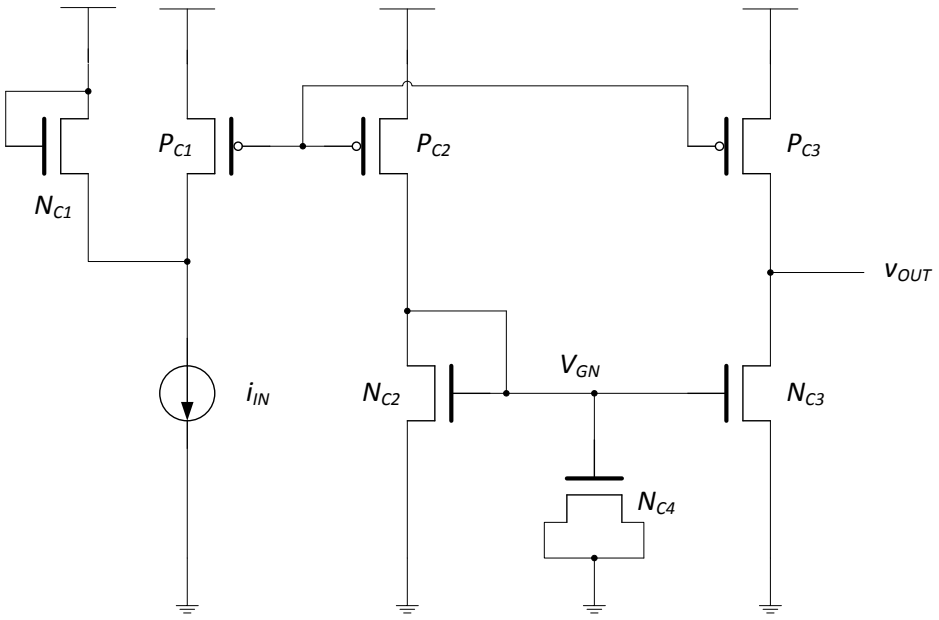
This chapter consists of three sections. In the first section, the critical problems in the design of the wide range adaptive amplifiers are addressed and the challenging issues are shown. To be specific, an example of a wide dynamic range current-to-voltage converter is used to highlight these problems. The second section is dedicated to the presentation of the analysis of the basic amplifiers, in particular the elements related to the amplification gain and possible configuration of wide range adaptive amplifiers. In the third section, the development of the design method is described and the design of the adaptive amplifier that helps to improve the current-to-voltage conversion is presented.

3.1 Need for adaptive amplifiers and the definition of the characteristics of an amplifier.

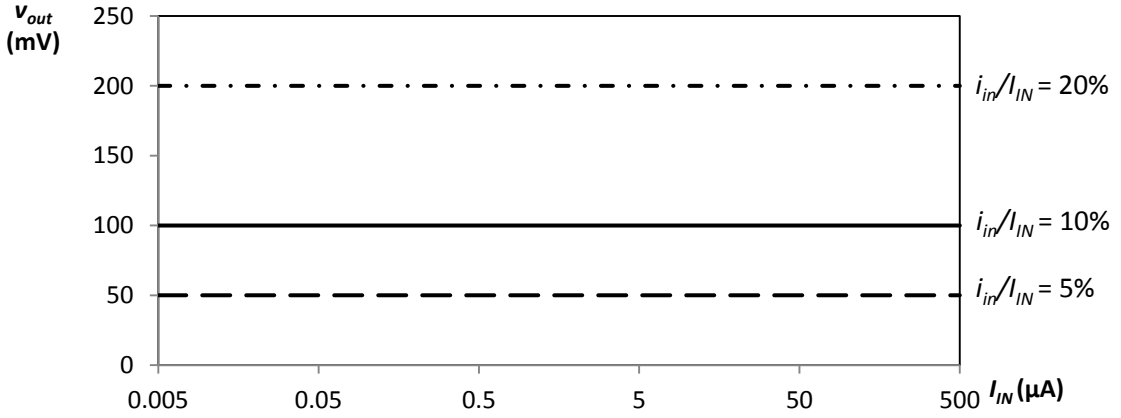
In the design of amplifier circuits, the efforts are usually made to obtain a high amplification gain, good linearity and/or wide frequency response. The research presented in this thesis aims at developing nonconventional amplifiers. It was initially

motivated by the need of an adaptive amplifier to solve the problem of the insufficient amplitude of a voltage signal delivered by the current-to-voltage converter presented in [Wang10]. This serves as a typical case illustrating the need for amplifiers of which the gain varies with the input. The design of this amplifier is presented as an example to show, in a concrete manner, how the proposed method can be applied in the development of this kind of adaptive amplifiers.

As described in Chapter 2, the current-to-voltage converter, as shown in Figure 3.1(a), involves a low pass current filter, consisting of the five devices P_{C2}, P_{C3}, N_{C2}, N_{C3} and N_{C4}, to separate the signal variation component i_{in} from the DC one I_{IN}. The current signal i_{in} is then converted at an adaptive rate into a voltage signal v_{out} and I_{IN} to V_{OUT} with a compression. The range of the conversion is related to the operating range of the low pass filter. The time constant at the node v_{GN}, determined by the capacitance at the node and the input-current-dependent transconductance of N_{C2}, should be large enough with respect to the cycle time of the signal variation to secure a normal filtering operation. In the original version of the converter of [Wang10], a large capacitance given by N_{C4} sized 20x20 μm^2 satisfies the condition in the entire range of the input current, despite that the transconductance of N_{C2} becomes smaller when the input DC level increases. The converter can have a characteristic of output voltage amplitude $|v_{out}|$ versus input DC level I_{IN} very close as that shown in Figure 3.2. The input current is from an optical sensor and the DC level I_{IN} represents the background intensity. Its range is from 5 nA to 0.5 mA, and the amplitude of i_{in} can be anything between 5% to 20% of the DC level on which it varies. The conversion is locally linear, i.e., at the same I_{IN} level, the rate of v_{out}/i_{in} is constant. However, the conversion is globally nonlinear, i.e., the conversion rate changing with the input DC level. For instance, i_{in} = 5 nA at I_{IN} = 50 nA yields $|v_{out}|$ = 100 mV at the conversion rate of v_{out}/i_{in} = 20 mV/nA, whereas i_{in} = 40 μA at I_{IN} = 0.4 mA also yields $|v_{out}|$ = 100 mV at a much small rate of v_{out}/i_{in} = 25 mV/μA. This nonlinearity makes the converter operate over a wide range of the input current. Moreover, the converter is tuned to produce an almost constant output signal voltage amplitude for a given input current ratio i_{in}/I_{IN}. For example, if i_{in}/I_{IN} = 0.1, | $|v_{out}|$ will be 100 mV, no matter that I_{IN} is 5 nA or 5 μA, as shown in Figure 3.1 (b).



(a)



(b)

Figure 3.1 (a) Current-to-voltage converter operating over a very wide range of the input. It involves a low pass current filter, consisting of the five devices P_{C2}, P_{C3}, N_{C2}, N_{C3} and N_{C4}, as shown in [Wang10]. (b) Output signal amplitude v_{out} versus input DC level I_{IN} of the current voltage converter, in case of $|i_{in}|/I_{IN} = 0.05$, 0.1 and 0.2, when the capacitance at V_{GN} is large enough to secure the low pass filtering condition in the entire input current range.

As mentioned above, the correct operating condition of the low pass filtering in the circuit shown in Figure 3.1 (a) is secured by having a large capacitance at the NMOS gate. Such a large capacitance requires, however, a large space allocation in the circuit implementation, which can consequently limit the application of the converter. Reducing the capacitance would reduce the operating range of the converter. The consequence is that the amplitude of the output voltage signal in some part of the operation range becomes too small to be useful due to the poor function of the low pass filter. If the gate size of N_{C4} is reduced from 20x20 μm^2 to 1x1 μm^2, when $|i_{in}|/I_{IN} = 0.1$ the output signal amplitude $|v_{out}|$ will be significantly reduced and the characteristic of $|v_{out}|$ versus I_{IN} is shown in Figure 3.2.

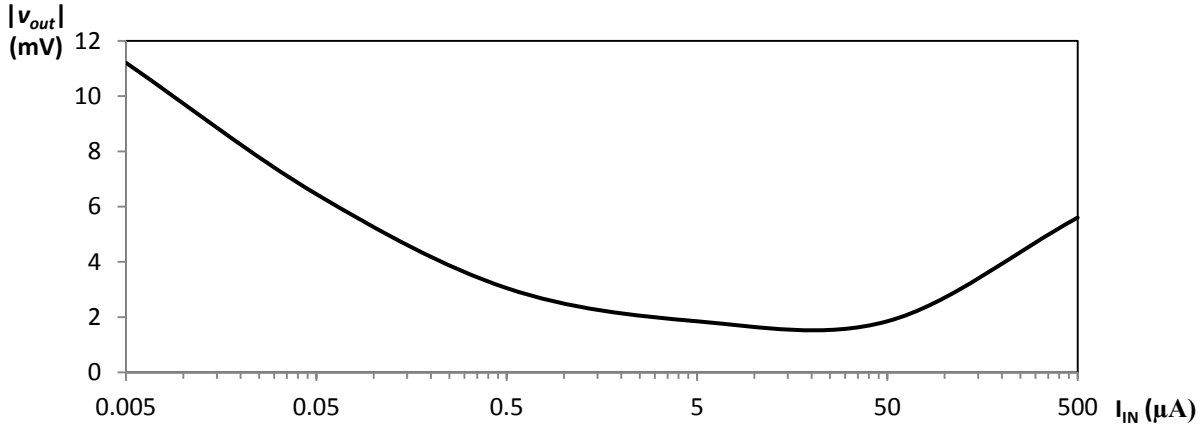


Figure 3.2 Characteristic of the input signal amplitude $|v_{out}|$ versus the input DC current level I_{IN} of the converter shown in Figure 3.1 (a).

To make the converter functional without using a space consuming component, such as a large capacitor, one can place an amplifier to enhance the output voltage, as shown in Figure 3.3. As the reduction of the signal amplitude is not uniform in the input DC current range, as shown in Figure 3.2, to recover the circuit characteristics shown in Figure 3.1 (b), the voltage signal gain of the amplifier needs to be tuned differently by the input DC level. In other words, the amplifier should be designed in such a way that its gain adapts the change of the input level according to a defined characteristic.

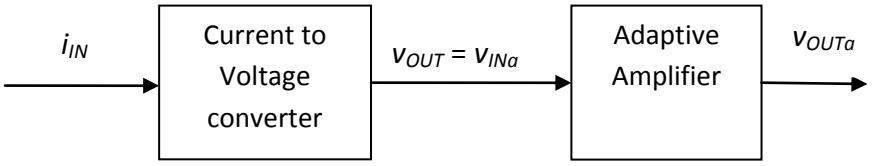


Figure 3.3: Block diagram of the current-voltage converter with an adaptive amplifier incorporated to enhance the voltage amplitude. Note that the output voltage of the converter v_{OUT} is the input of the amplifier v_{INa}.

To characterize the voltage signal amplification gain versus the input DC level V_{INa} of the adaptive amplifier shown in Figure 3.3, one needs first to determine the characteristic of the input signal amplitude $|v_{ina}|$ versus the input DC level V_{INa}, where (v_{ina}, V_{INa}) of the amplifier is (v_{out}, V_{OUT}) of the converter. Figure 3.2 illustrates the characteristic of $|v_{ina}|$ versus I_{IN} of the converter when the transistor N_{C4} is sized 1x1 μm^2. As I_{IN} range of (5 nA, 0.5 mA) is converted in to the DC voltage range of (0.2 V, 0.5 V) in a near-logarithmic scale, the relation between $|v_{ina}|$ and V_{INa} is characterized as shown in Figure 3.4. If the circuit shown in Figure 3.3 tends to have the characteristics similar to those shown in Figure 3.1 (b), the gain of the amplifier should be made input-DC-level dependent as illustrated in Figure 3.5.

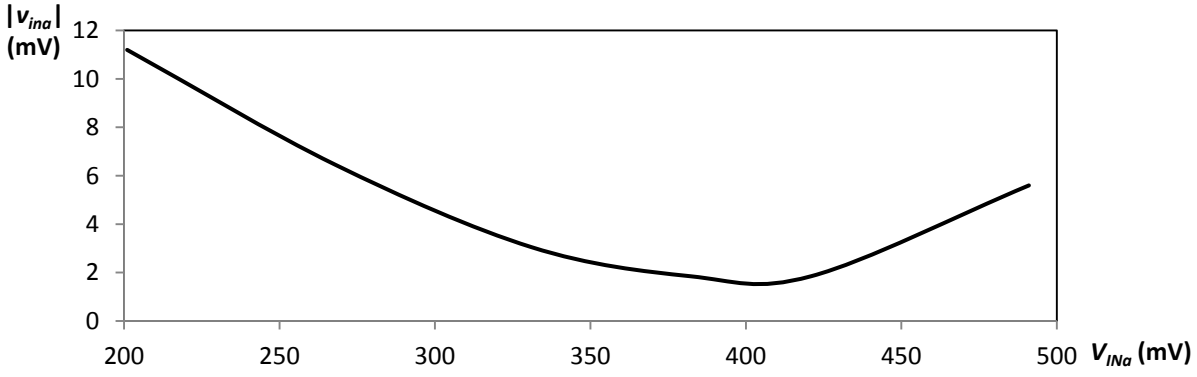


Figure 3.4: Characteristic of the input signal amplitude $|v_{ina}|$ versus the input DC voltage level V_{INa} of the amplifier.

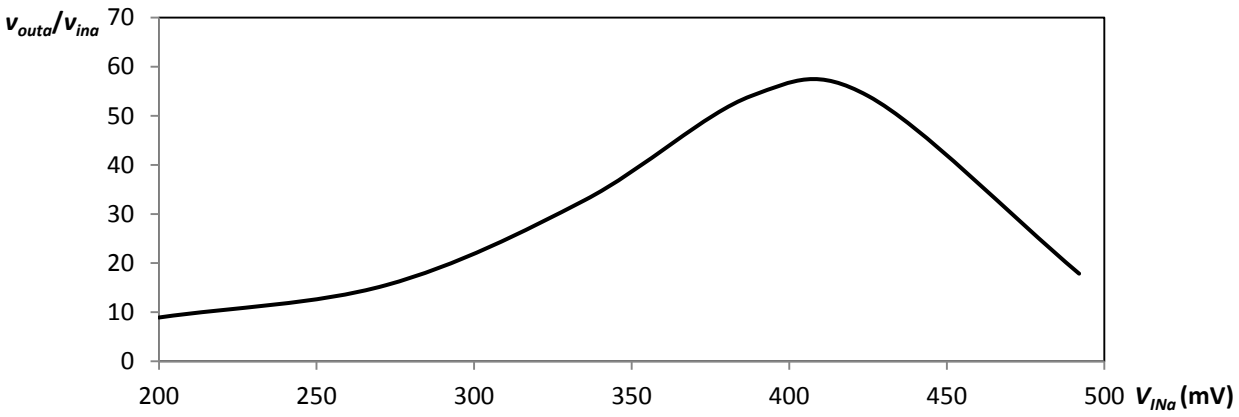


Figure 3.5: Anticipated characteristic of the adaptive amplifier. The gain v_{outa}/v_{ina} is variable according to the DC input voltage V_{INa}.

From the characteristics shown in Figure 3.4 and 3.5 we can see that the amplifier to be designed should have the following characters.

1. The amplifier should be able to operate over a very wide range of V_{INa} to support the wide dynamic range of the converter.
2. It is important to maintain a nonlinear amplification gain over the entire range. As shown in Figure 3.5, the gain is neither a simple increasing nor a decreasing function of V_{INa}. It increases with V_{INa} in the lower segment and decreases in the upper segment of the range.
3. Much like the local linearity in the original converter, there must be a linear amplification at a given V_{INa} level. This makes it possible to maintain the characteristic of v_{outa} versus I_{IN}, similar to the one shown in Figure 3.1 (b).
4. Apart from the critically required characters mentioned above, it should be noted that the design of the amplifier does not aim at a high gain.

Taking the above mentioned characters into consideration, the design of this adaptive amplifier will not fit a conventional model. We need to develop a new design method starting with the basics of amplifier structures. In the following part of the chapter, a study of the basic configurations of the voltage amplifiers and an investigation of the basic elements related to the voltage gain will be presented.

3.2 Variable gain common source amplifiers

As mentioned previously, the amplifier needs to operate over a very wide range of the input voltage level. Moreover, in terms of the voltage amplification, the critical issue is the control of the gain according to the input level, rather than a high amplification gain. Based on all of these factors, the circuit analysis of the amplifier should be on the basis of both large and small signal models, which deviates the design from conventional approaches. It is, therefore, important to look into the basic configurations of MOSFET amplifiers in order to obtain a suitable structure that permits a shift of the bias point and an easy control of the gain.

There are 3 basic configurations for MOSFET amplifiers, namely common source, common drain and common gate amplifiers. A common drain amplifier does not produce a gain higher than unity, while a common base amplifier has a relatively low input resistance and is mainly used for high frequency applications. The most commonly used basic configuration in the design of amplifiers is the common source (CS) amplifier, as shown in Figure 3.6. In this configuration, the PMOS transistor is used as an active load and V_{bias} adjusts the bias current of the amplifier.

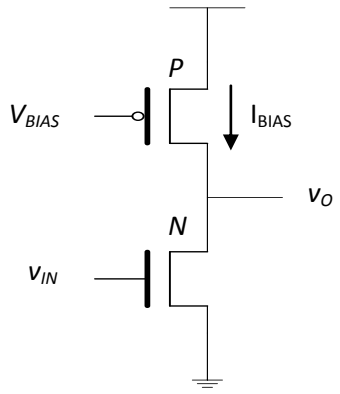


Figure 3.6: Basic NMOS common source amplifier

The circuit shown in Figure 3.6 can perform an amplification of the small signal v_{in} if the two transistors are biased at an appropriate operating point in the saturation region. The bias current is adjusted by V_{BIAS}, the gate voltage of P. If the input DC level

changes, V_{BIAS} must also change so that the operating point of the NMOS transistor will shift accordingly to maintain operation in saturation mode. At a given bias current level I_{bias}, the voltage gain of the amplifier (A_V) is given as

$$A_V = -g_m\left(r_{sdp} \parallel r_{dsn}\right) \tag{5}$$

where g_m is the transconductance of the NMOS transistor, r_{dsn} is its drain-source resistance and r_{dsp} is the source-drain resistance of the PMOS transistor. These three factors depend on the bias current I_{BIAS}. In other words, V_{BIAS} is the only parameter that can be used to adjust I_{BIAS} to maintain both transistors in the saturation mode, and consequently determine the gain.

Figure 3.7 illustrates the voltage transfer characteristics of v_O versus v_{IN} of the circuit shown in Figure 3.6. It is observed that a good voltage amplification, i.e. $dv_O/dv_{IN} >> 1$, requires a particular DC level of the input V_{IN} if V_{BIAS} is fixed. In other words, if the DC level V_{IN} changes, V_{BIAS} needs to be changed to match it. It can also be observed that a decrease of V_{BIAS}, i.e. an increase of I_{BIAS}, causes dv_O/dv_{IN} to decrease, which indicates that V_{BIAS} determines both the operating point and the gain. Hence, the operating point and the gain cannot be adjusted independently by using only the bias current.

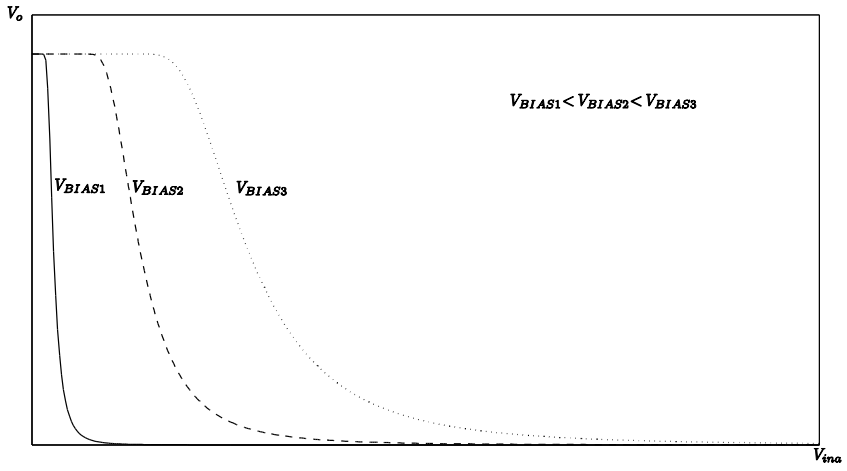
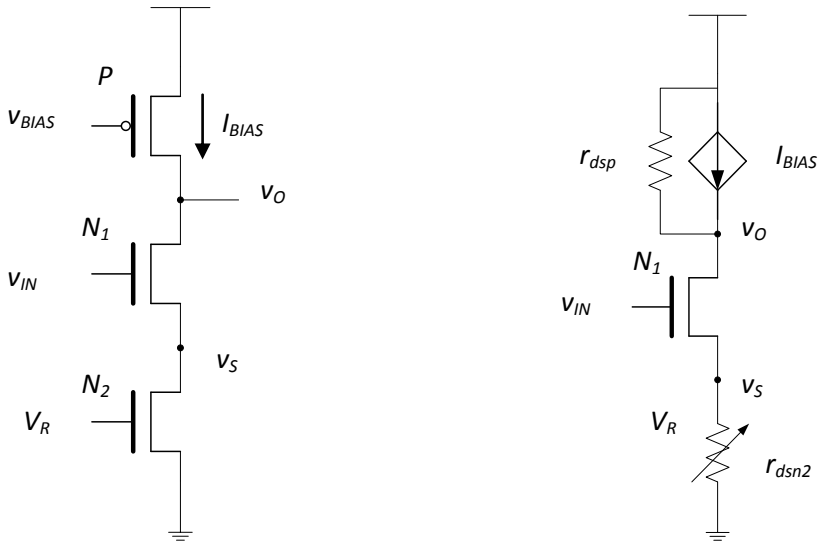


Figure 3.7: Characteristics of the output voltage v_O versus input voltage v_{IN}, with different V_{BIAS} of the CS amplifier shown in Figure 3.6.

As described in Section 3.1, the target application of the adaptive amplifier requires a good control of the gain. In other words, it is necessary to enable a change of the gain in a complex manner depending on the input voltage level. Thus, this simple CS amplifier cannot meet the requirement. We need a configuration that allows the adjustment of more parameters to the gain when the bias current is fixed.

In a common source amplifier with a source resistance such as the one shown in Figure 3.8 (a), the resistance, made of the NMOS transistor N_2 operating in the triode region, makes a negative feedback that reduces the gain in exchange for more control and better linearity. In this configuration, V_{BIAS} controls the bias current, I_{BIAS}, of the amplifier while V_R controls the equivalent drain-source resistance of N_2. The introduction of this resistance alters the characteristics of the amplifier and one needs to see how the adjustment of the voltage V_{BIAS} and V_R can effectively change and determine the characteristics of the amplifier.



(a) (b)

Figure 3.8: (a) Three transistor common source amplifier, N2 serves as a resistor. (b) Equivalent circuit of the amplifier under the condition of a fixed V_{BIAS}.

In the circuit shown in Figure 3.8 (a), at a given I_{BIAS}, the voltage gain A_V is expressed as

$$A_V = -\frac{g_m(r_{sdp} \| r_{dsn1})}{1+g_m r_{dsn2}} \tag{6}$$

where g_m and r_{dsn1}, are the transconductance and the drain-source resistance of N_1 respectively, r_{sdp} the source-drain resistance of the PMOS P, and r_{dsn2} the drain-source resistance of N_2. It is known that A_V is determined at a given biasing point, i.e. a specified set of V_R and V_{BIAS} that suits the input voltage level. For instance, V_{I1}, as shown in Figure 3.9 (a) will require a matched V_{BIAS} and V_R to have $A_V = A_{V1}$. Normally, to obtain a wider linear range of the amplification V_R is put at a level that makes r_{dsn2} larger, at the expense of lower voltage gain, as shown in Figure 3.9 (b). Thus, this configuration provides designers with a trade-off of gain and range, which can be useful in many cases.

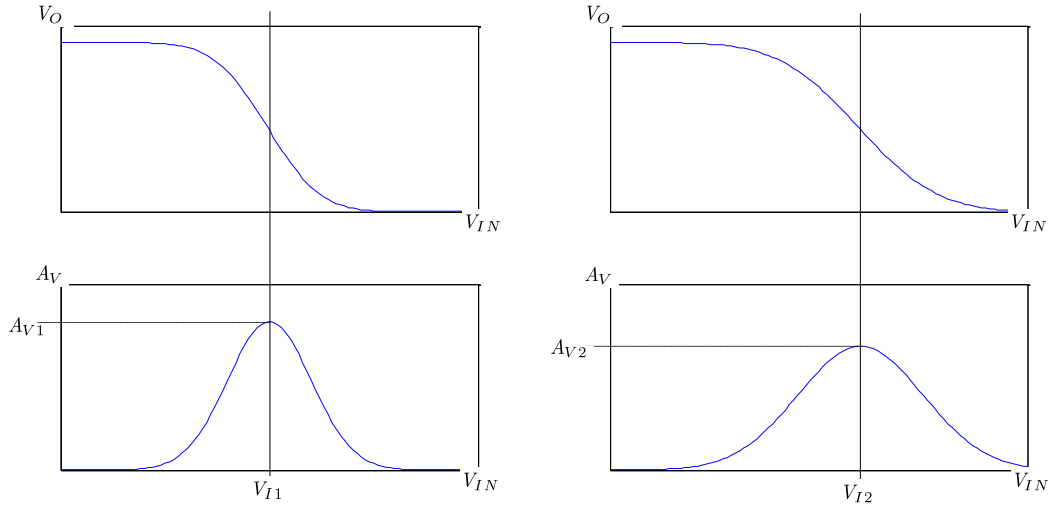


Figure 3.9: characteristics of a common source amplifier with a source resistance, where r_{dsn2} is higher in (b) compared to that in (a).

In this amplifier illustrated in Figure 3.8 there are two control voltages, namely V_{BIAS} and V_R, thus the control of the transistor operation is more flexible. For voltage amplification, the transistors P and N_1 should operate in the saturation region, and N_2 in the triode region. It is important to maintain a low level of V_S, the source voltage of N_1 and the drain voltage of N_2, to satisfy these basic conditions. It should be mentioned that the input level of the amplifier is expected to vary over a wide range. At any of these levels the amplification conditions must be satisfied. If the input level V_{IN} is given and I_{BIAS} is kept stable at an appropriate level, one can vary V_R to adjust the drain-source resistance of N_2 in order to modify the amplification gain to a certain extent.

Under the conditions of amplification, the circuit shown in Figure 3.8 (a) can be equivalent to that illustrates in Figure 3.8 (b). Based on this equivalent circuit, one can analyze the behavior of the circuit with respect to the changes brought by the bias voltages V_{BIAS} and V_R, as well as that of the DC voltage level of the input v_{IN}. In this analysis, the bias current I_{BIAS} is given if V_{BIAS} is fixed. There will then be three scenarios, in each of them we will observe how the device biasing and the effective gain can vary if V_R changes, or V_{IN} changes, or both change.

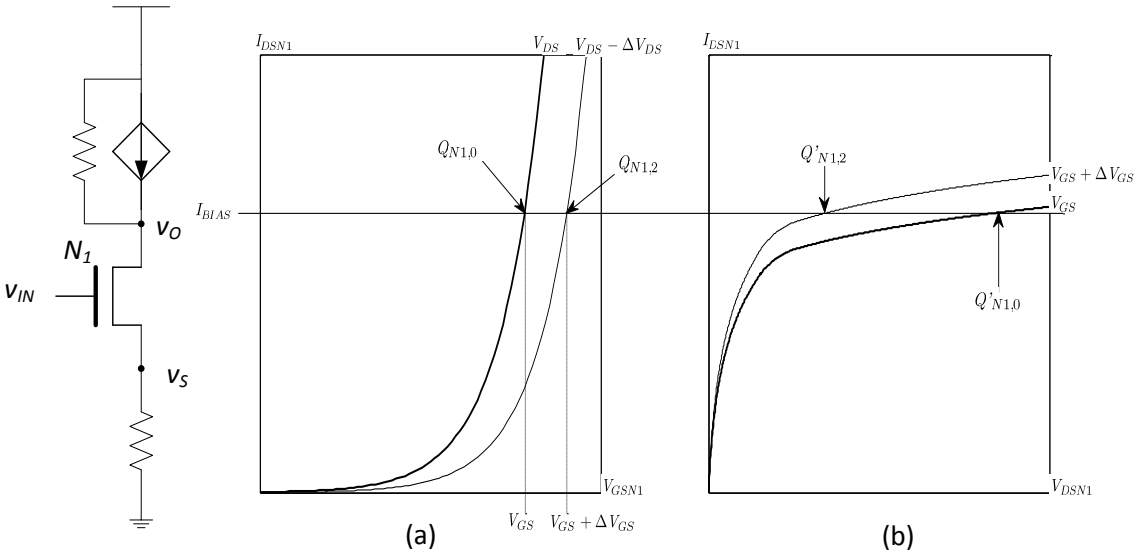


Figure 3.10: Characteristics of the transistors in the CS amplifier and the shift of the operating point if the gate-source voltage of N_1 changes. (a) I_{DS} versus V_{GS}. (b) I_{DS} versus V_{DS}.

In the first scenario, V_R in Figure 3.8 (b) is fixed and thus r_{dsn2} can also be considered fixed. In a conventional common source amplifier, the DC level of the input is assumed to be constant. However, in this design, the DC voltage level V_{IN} can shift very significantly. The analysis concentrates on the effect of a change of the input DC voltage level V_{IN} on the circuit operation. We assume that the initial operating point of N_1 is specified as ($Q_{N1,0}$, $Q'_{N1,0}$) in its characteristics of I_{DS} versus V_{GS} and I_{DS} versus V_{DS}, respectively, as shown in Figure 3.10 (a) and (b). When V_{IN} increases, the operating point of N_1 shifts to ($Q_{N1,2}$ and $Q'_{N1,2}$), while the bias current I_{BIAS} is stable, leading to a visible decrease of V_{DS} and thus reducing the output voltage V_O. In addition, the transconductance g_m and drain-source resistance r_{DSN1} of N_1 will also be modified by the

change in V_{IN}. Thus, an increase of V_{IN} results in a significant decrease of the output level and a modification of the gain. In other words, if V_{IN} is made to decrease, one should expect the DC level of V_O to increase.

In the second scenario V_{BIAS} in Figure 3.8 (b) is fixed, let us observe how the circuit will respond to a change of r_{dsn2} to adjust the characteristics of the amplifier. It should be mentioned that I_{BIAS} is stabilized at a given level and the gate voltage V_{IN} is fixed. One can assume that the initial operating point of N_1 and that of N_2 are $Q_{N1,0}$ and $Q_{N2,0}$, respectively, as shown in Figure 3.11 (a) and (b). If V_R increases by a ΔV_R, r_{dsn2}, given by di_{DSN2}/dv_{DSN2}, will decrease, resulting in a decrease of the drain-source voltage of N_2 and thus lowering V_S. The transistor N_2 will then operate at $Q_{N2,1}$. Consequently the gate-source voltage of N_1 will increase, shifting the operating point of N_1 to $Q_{N1,1}$. As a result, a lower level of V_O and a slight modification of g_m should be expected. As such, in this process, a change in V_R, if the conditions of amplification are kept satisfied, can cause a significant change in r_{dsn2} and a small modification in g_m. Consequently, the voltage amplification gain will be increased while the DC output voltage is visibly shifted to a lower level by the increase in V_R.

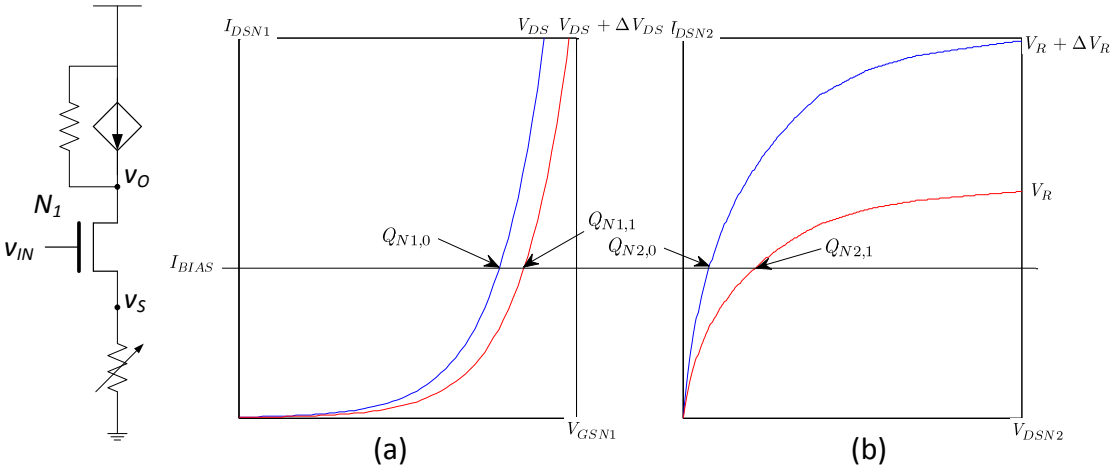


Figure 3.11: Characteristics of the transistors in the CS amplifier and the operating points if the gate-source voltage of N_2 changes (a) i_{DS} versus v_{GS} of N_1, (b) i_{DS} versus v_{DS} of N_2.

In the third scenario, both V_R and the DC level of the input v_{IN} can be changed. As described above, a change in V_R can lead to an adjustment of the voltage gain, accompanied by a shift of the DC level of the output, whereas a change of V_{IN} alone produces a shift of the DC level of the output with a modification of the gain. It is possible in the circuit shown in Figure 3.8, that when V_{IN} changes from one level to another, causing the level of V_O to shift, the bias current can be kept stable and the voltage V_R modified to serve the 2 purposes. The first is to adjust the amplification gain, and the second, meanwhile, to shift the output level in the opposite direction to that caused by the change in V_{IN}. Therefore, this circuit can receive an input voltage, of which the DC level varies significantly, and maintain its bias current with the output DC level stabilized.

Summarizing the above analysis, one can see that the common source configuration shown in Figure 3.8 has the following features, which are not given by the basic CS amplifier consisting of two transistors and are not fully explored in the conventional amplifier designs.

- When the DC level of the input voltage changes significantly, the bias current can still be maintained by a fixed V_{BIAS}.
- It is possible to keep the output DC level stabilized when the input DC level V_{IN} shifts by adjusting V_R.
- V_R is also used to change the amplification gain as it controls the source resistance, r_{dsn2} and consequently the output DC level will be shifted due to the change of V_R.
- It is possible to adjust the gain and to stabilize V_O simultaneously if V_R is changed with the DC level of the input voltage in a “synchronized” manner.

This common source amplifier allows the designers to tackle both input level shifting and variable amplification gain by using the voltages V_{BIAS} and V_R. Ultimately it makes it possible to have an amplifier with both wide range of input level. It is thus an important building block in the design of an adaptive amplifier. In the next section the design of such an amplifier is presented.

3.3 Design of an adaptive amplifier

The objective of the work presented in this thesis is to develop a methodology of designing wide-range adaptive amplifiers. To be more specific, the DC level of the input signal of such an amplifier can shift from one DC level to another, and the amplification gain needs to be variable in a deterministic way, depending on the DC level, which is very different from what a conventional amplifier can do. Because of the particular feature of the input, the amplifier has to be designed with an approach different from conventional ones. Based on the study of the basic configurations presented in Section 3.2, one can see that a common source amplifier with a source resistance provides not only a control of the amplification gain but also a fair tolerance for any shift in the DC input level. It can be used as an important basic unit to perform part of the required task. Combining it with other units, one can constitute an adaptive amplifier described above. Thus, such an amplifier has to have multiple stages. According to the requirement of the gain variation and of the input DC level, the organization of the stages, i.e. the assignment of the tasks to each stage, has to be carefully made on a case by case basis. As we take the adaptive amplifier to be used in the current-voltage converter as a design example, the way of organizing the multiple stages of the amplifier and the design of each stage is presented here.

The targeted adaptive amplifiers are expected to handle their input voltages that may not be within the range of a conventional one. The DC level can be too low or too high to make some transistors operate normally. Also, the amplitude of the signal variation may not be necessarily small, but needs to be amplified in a sophisticated manner to meet the requirement of the output. The input of the amplifier in the design example has its DC level ranged from 0.2 V to 0.5 V, which is far from the normal operating range of a conventional amplifier. Moreover, its input signal variation is about 25 mV when the DC level is 0.25 V and 2 mV at 0.4 V. The required gain, in this case, is strongly non-linear and DC level dependent, as shown in Figure 3.5. Such a sophisticated gain has to be obtained step by step, by multiple stages. Thus it is reasonable to have 2 parts in this adaptive amplifier, namely the conditioning block and the amplification block.

The amplification block will have its stages well tuned so that it will produce the characteristics as shown in Figure 3.5. To facilitate this task it is required to have the DC voltage of its input at an appropriate level to suit its operating range. Moreover it has been demonstrated in Section 3.2 that the input DC level is one of the elements determining the gain. To make the adjustment of the gain in this block more flexible, one would like to have the input DC component not constant, but shifted from the initial range.

The conditioning unit is expected to perform this shift of the voltage level range and a pre-amplification. It can include a shifting unit such as a source follower, and a pre-amplifier stage. The challenge in the design of the conditioning unit is in the pre-amplifier as the amount of the level shift can be relatively easily controlled. The pre-amplifier is expected to help in the implementation of the voltage-level-dependent gain illustrated in Figure 3.5. It should thus have a lower gain when V_{IN} is in the lower segment of its range, and a larger gain in the upper segment. At any given level of V_{IN} within its range, the signal variation needs to be transmitted with a minimum distortion. Thus, the amplifier should be designed to have a wide range of operation, which is possible by sacrificing the gain.

3.3.1 Conditioning block

The conditioning block is to transform the input voltage of the adaptive amplifier to what the amplification block needs, i.e. a DC level change and preliminary amplification of the signal variation. These two operations can normally be performed by a voltage follower and an amplifier. Regarding the specific condition of the input and the requirement of the output of the conditioning block, one can look for an optimal combination of the two functioning units to make the structure as simple as possible.

The given input voltage to the conditioning block has its DC level ranged from 0.2 V to 0.5 V. It can drive the transistors of a PMOS based CS amplifier with a source resistance, as shown in Figure 3.12, to operate normally. This stage can thus serve as a pre-amplifier, if it is made to have its gain vary correctly according to the input DC level.

In this case, the conditioning block will consist of two stages, i.e. a PMOS based CS amplifier succeeded by a source follower to adjust the range of the voltage DC level.

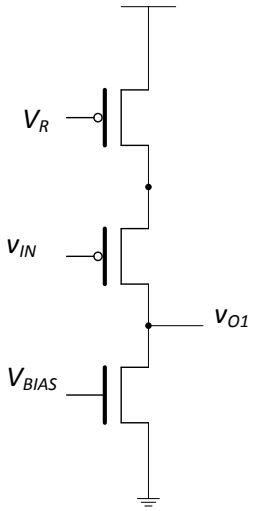


Figure 3.12: First stage of the adaptive amplifier.

Another option for the structure of the conditioning unit is to place a voltage shifter in the first stage so that the range of DC level will be moved up to suit a NMOS based CS amplifier. However, in this case one may need another voltage shifter after the amplifier, as the DC range after amplification may not be in the appropriate region for the succeeding amplification block.

As mentioned previously, a CS amplifier with a source resistance can have its gain variable by adjusting the source resistance. However, if a certain level of amplification is required, it is hardly possible to obtain a characteristic of gain similar to that shown in Figure 3.5, also presented in Figure 3.13 (a). Nevertheless, it is possible to have a voltage transfer, in which the gain of the signal variation is modulated to have a bell-shaped characteristic similar to that shown in Figure 3.13 (b). Such a characteristic can be implemented under the condition that the gain is around unity and the input signal amplitude is very small. In this case, the succeeding amplifier block can be designed to have a characteristic as shown in Figure 3.13 (c), where the gain increases non-linearly with the input DC level, which is feasible with the CS amplifier shown in Section 3.2.

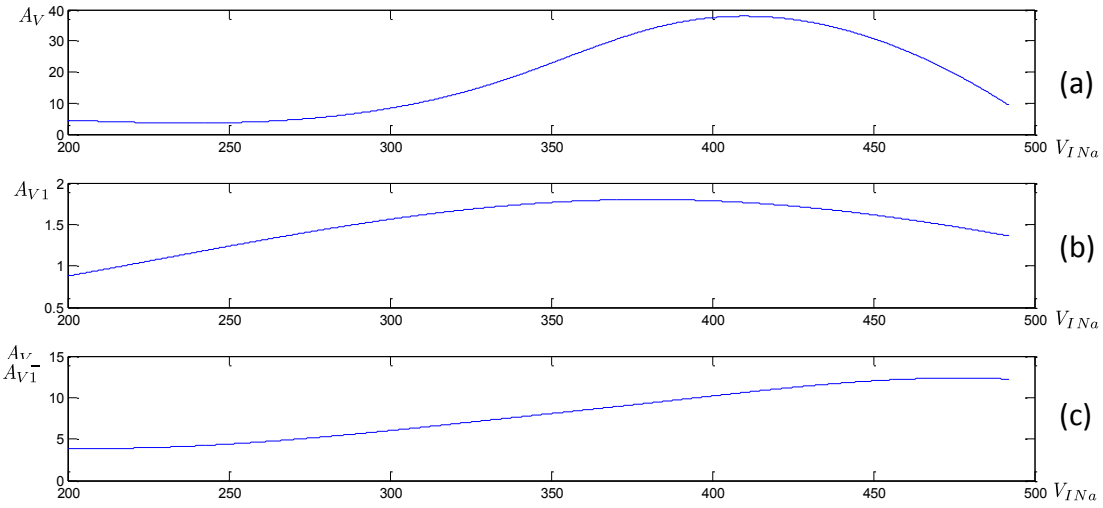


Figure 3.13: (a) Characteristic of the required overall voltage gain, (b) anticipated voltage gain of the pre-amplifier, (c) and that of the amplification block.

The design of the pre-amplifier starts with an investigation of the characteristics of a CS amplifier with a source resistance. If the bias current and V_R are fixed, the characteristic v_O versus v_{IN} is shown in Figure 3.14 (a) and that of the gain $A_V = dv_O/dv_{IN}$ as Figure 3.14 (b). In a normal operation the input DC level is set up at V_{IN0} to have $A_V = A_{Vmax}$. Due to the nonlinearity of the characteristic, if the DC input deviates from V_{IN0}, the gain for the variations will be smaller than A_{Vmax}. However, this nonlinear characteristic can be used to implement a voltage signal transfer with a gain depending on the DC input, provided that the amplifier operates under a certain set of restrictions.

In the pre-amplifier to be designed, i.e. of the configuration shown in Figure 3.12, the DC level of the input is not fixed at a specific point, but can vary between V_{INmin} and V_{INmax}. Thus the pre-amplifier is not operating in a conventional mode. A given level of V_{IN} should result in a particular value of A_V between a predetermined (A_{Vmin}, A_{Vmax}). If the pre-amplifier is adjusted in such a way that it makes $A_V(V_{INmin}) = A_{V1}$, $A_V(V_{IN0}) = A_{V2}$, and $A_V(V_{INmax}) = A_{V3}$, this circuit will perform a voltage transfer characteristic similar to that shown in Figure 3.13(b). Figure 3.15 illustrates the small signal operation of the circuit in the cases where the DC input is at 3 different levels, namely V_{INmin}, V_{IN0} and V_{INmax}. The

shift of the input DC level and the nonlinearity of the amplification are combined to implement the required bell-shaped voltage transfer characteristic.

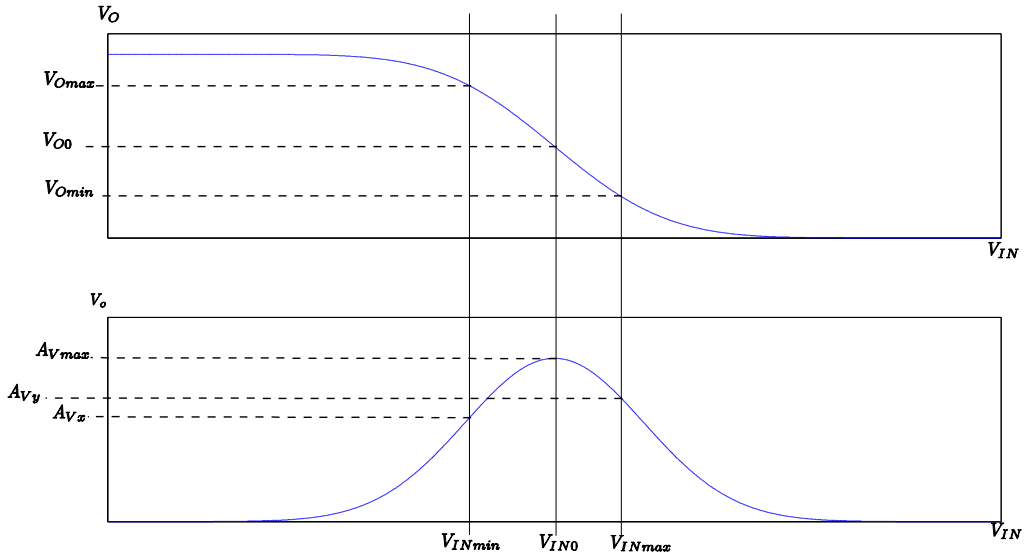


Figure 3.14: Characteristics of the CS amplifier shown in Figure 3.12 when the bias current and source resistance is fixed. (a) v_O versus v_{IN}, (b) Derivative of (a) i.e. dv_O/dv_{IN}.

It should be noted that even though the nonlinear characteristic of the pre-amplifier is used to achieve a gain that varies with the DC input level, it should perform a "linear" transfer of voltage variation if the DC input is at a given level. This "linear" transfer is based on a segment of the nonlinear characteristic that is small enough to be "linearized". To minimize the signal distortion in the "linear" transfer, the pre-amplifier should be designed to operate with restrictions concerning the gain with respect to the amplitude of the input signal variations. One needs to estimate the degree of the signal distortion in order to define the restrictions.

Within the operation range of the amplifier specified in Figure 3.15, it is assumed that the maximum difference of the gain is given by $\Delta A_V = A_{Vmax} - A_{Vx}$. This ΔA_V corresponds to the input DC range of $\Delta V_{IN} = V_{IN0} - V_{INmin}$. The change of the gain per unit voltage, denoted as K_V, can be approximately expressed as

$$K_V = \frac{\Delta A_V / A_{Vavg}}{\Delta V_{IN}} \quad (7)$$

where A_{Vavg} is the average value of (A_{Vmax}, A_{vmin}) and $\Delta A_V/A_{vavg}$ is the variation rate of voltage transfer gain. The rate K_V can be seen in the following two aspects

- It shows the range of the gain of voltage transfer that can be achieved within the given range of the DC input level. To make the amplifier capable of producing a wide range of the gain variation, K_V should be large.
- This rate also gives an indication of the deviation of the gain applied to a small signal varying at a particular DC level. From this point of view, one would minimize K_V to minimize the distortion.

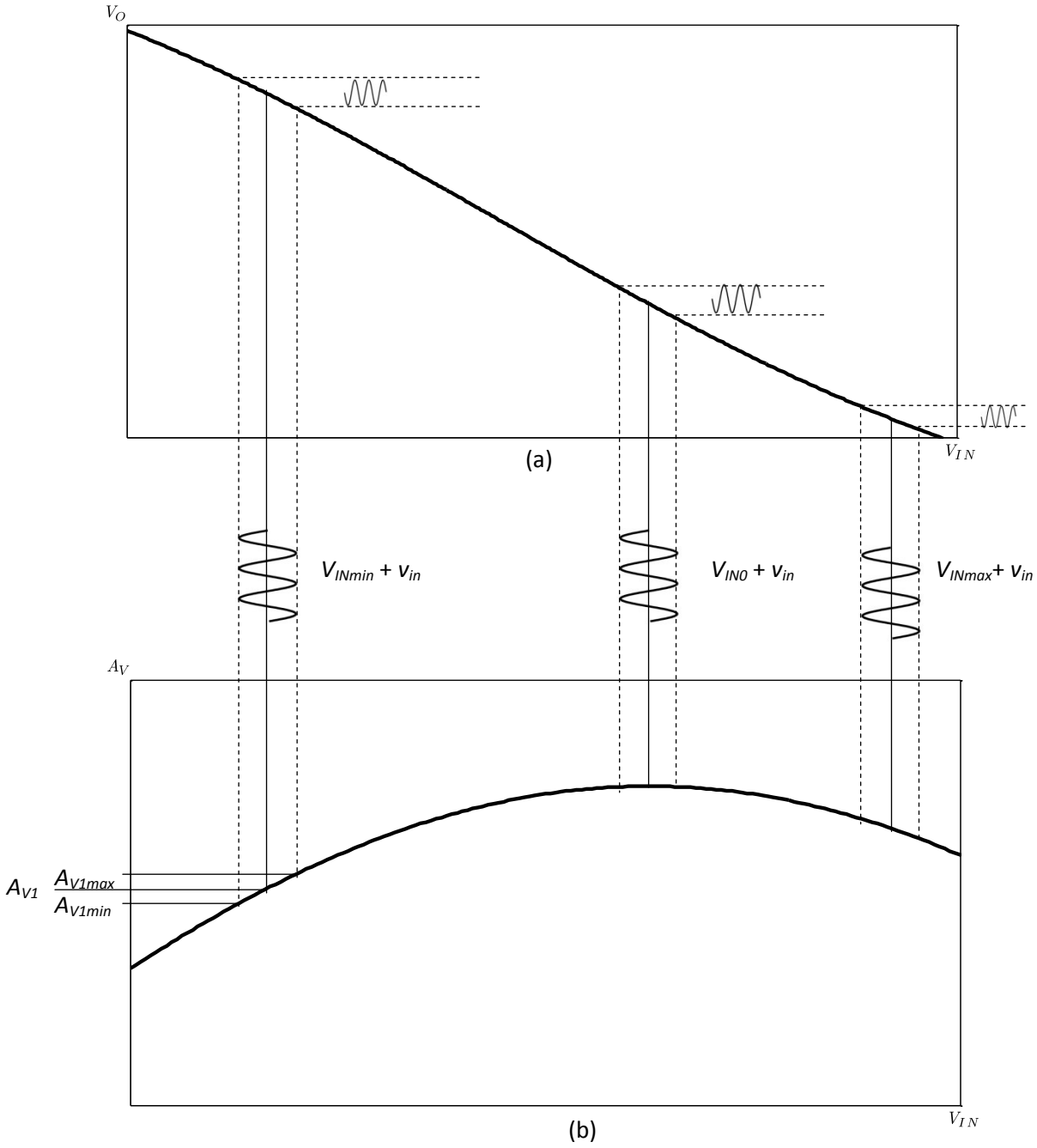


Figure 3.15: Voltage transfer for small signal variation of the CS amplifier shown in Figure 3.12 with a fixed bias current and at different DC input levels ranging from V_{INmin} to V_{INmax}

As K_V represents two opposing characters of the pre-amplifier, one needs to find a good trade-off to balance the range of the gain and the limit of small signal distortion. For a given signal v_{in} the rate of signal distortion can be estimated by

$$K_D = \pm|v_{in}| * \frac{\Delta A_V / A_{Vavg}}{\Delta V_{IN}} \tag{8}$$

In case of ΔV_{IN} = 200 mV, $|v_{in}|$ = 20 mV, and the maximum signal distortion being 5%, the maximum variation rate of $\Delta A_V/A_{vavg}$ will be 0.5. It is to say that the gain will be 0.75 A_{Vavg} if the input signal is varying at the level of V_{INmin}, and it will become 1.25 A_{Vavg} if the DC level is shifted to V_{IN0}. It should also be underlined that this is to secure the condition for a maximum signal distortion of 5%, when a small signal varies at a given level.

It should be noted that if the circuit shown in Figure 3.12 is used for the pre-amplification, the DC input will be in the range from V_{INmin} to V_{INmax}. In this case, the output DC level is expected to change with the input one, as shown in Figure 3.14 (a). The range of the output DC level needs to be examined to see if it suits the requirement of the succeeding Amplification block. Adjusting the DC level can be done with a source follower. Two versions of source follower are shown in Figure 3.16. The NMOS version is used to shift the voltage to a lower level while the PMOS one to an upper level.

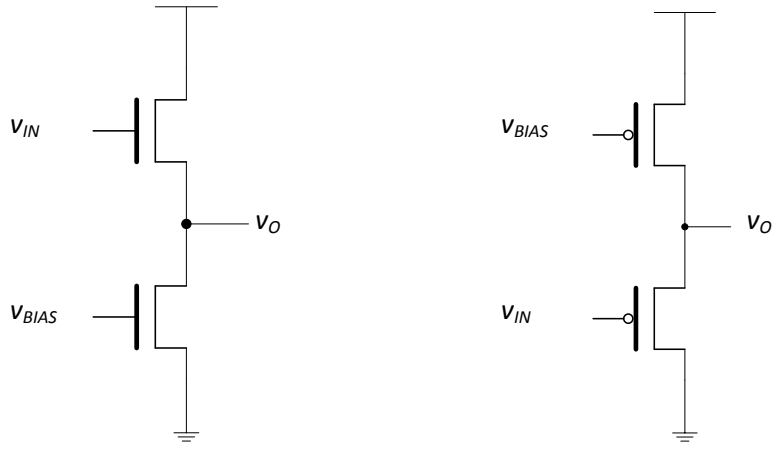


Figure 3.16: Two complementary versions of source follower.

In the design of the conditioning unit, the emphasis is on the pre-amplifier that has a bell shaped small voltage signal transfer characteristic. A method of designing such a circuit has been presented. The conditioning unit will consist of a pre-amplifier and a voltage follower. As the pre-amplifier does not give a significant voltage gain, the signal amplitude will be amplified in the next block. The voltage follower is used in this block to adjust the output DC level of the pre-amplifier to the requirements of the next amplifier block.

3.3.2 Amplification block

The overall voltage gain of the adaptive amplifier is expected to be dependent on the input DC level as specified in Figure 3.5 that is also presented in Figure 3.13 (a). The pre-amplifier, of which the design was presented in Section 3.3.1, is made to perform a transfer of small signal variations in different DC levels with a bell-shaped transfer characteristic close to that of Figure 3.13 (b). However, as the design effort of the pre-amplifier is focused on making the transfer gain variable as what is required, the value of the gain is not much more then unity. The amplification block is expected to perform a voltage amplification as specified in Figure 3.13 (c), i.e. a more significant non-linear gain increase according to the DC input.

From a general point of view, the priority in the amplification block is not a high gain. However, it has some critical issues that are not in a conventional design. It requires a change of the gain in a wide range, i.e. the maximum gain being 3 or 4 times higher than the minimum gain, as we can see in Figure 3.13 (c), which is more than a simple modulation. Also the DC input of the block is not fixed, which can actually be used as one of the elements enabling the implementation of the variable gain.

A CS amplifier with a source resistance, as shown in Figure 3.17, can be used for the amplification, for which the adjustment of the source resistance enables a change of the gain. Figure 3.18 (a) illustrates the voltage transfer characteristics of the circuit shown in Figure 3.17 (a) with different values of V_R, and Figure 3.18 (b), the derivative of the characteristics in (a). The figures demonstrate that if the input DC level is, for example, at

V_{IN1} and $V_R = V_{R1}$, the small voltage variation will be transferred with an amplification gain around 12. If V_{IN} increases to a higher level such as V_{IN2} and V_R is adjusted to a lower level V_{R2}, resulting in a higher source resistance, the voltage signal will be amplified with a lower gain. Hence, if V_R is made to vary with V_{IN}, the gain will be adjusted to increase or decrease. Meanwhile, it is demonstrated in Figure 3.18 (a) that if V_R is adjusted to match each V_{IN} in order that the signal variation at that level of V_{IN} is amplified with maximum gain, i.e. that the input level corresponds to the maximum point of the derivative, then the output DC level will be uniform as long as V_{IN} is in its range.

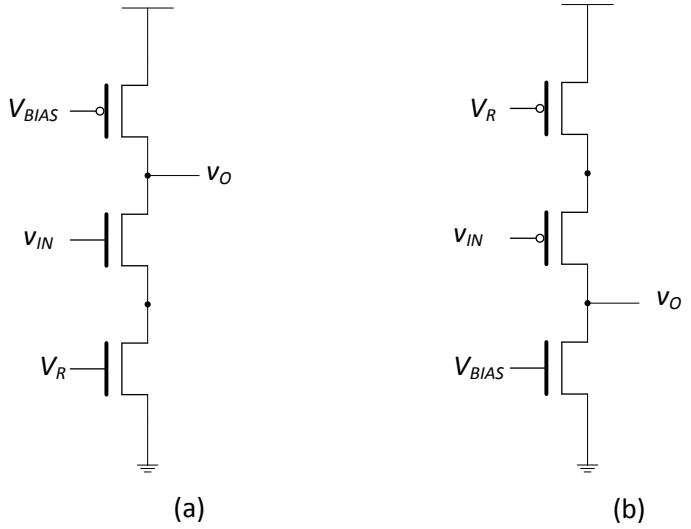


Figure 3.17: (a) Three-transistor common source amplifier. (a) NMOS version, (b) PMOS version.

Summarizing the above description, one can use a CS amplifier with a source resistance to implement a particular voltage amplification with the gain depending on the input DC level. In other words, this kind of amplifier can have an input voltage of which the signal variation can be at any level between V_{INmin} and V_{INmax}. It is important to make V_R varying with V_{IN} to implement this dependency on the input. Also, this kind of amplification will result in a uniformed output DC level. Two complementary versions of CS amplifiers are presented in Figure 3.17. The voltage gain of the NMOS version decreases with an increase of V_{IN}, whereas the PMOS version functions in the opposite way. This gives designers the options to handle different kinds of gain requirements.

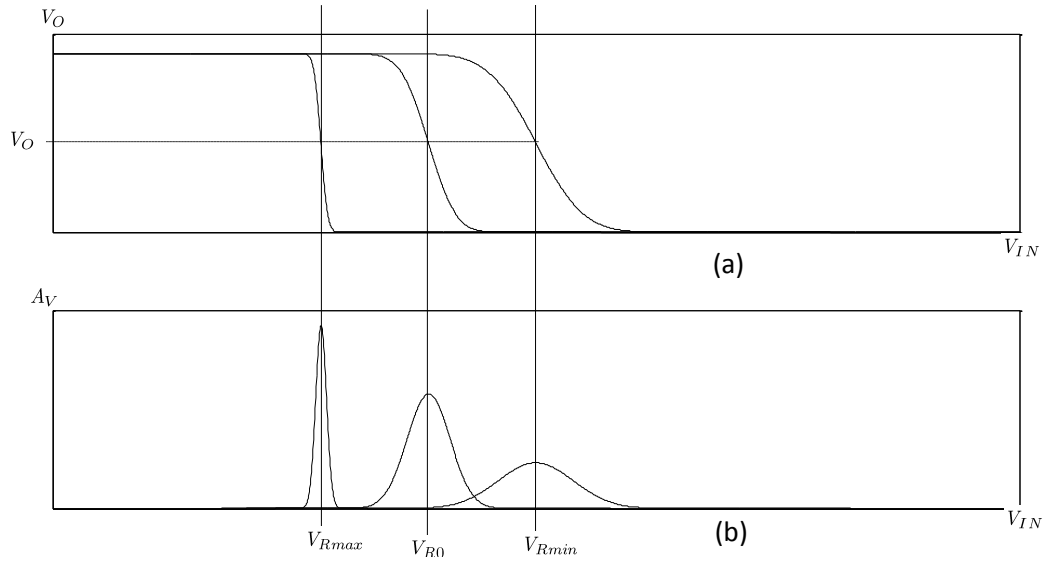


Figure 3.18: Characteristics of the CS amplifier shown in Figure 3.17 (a) when the bias current is fixed and source resistance is variable. (a) v_O versus v_{IN}, (b) Derivative dv_O/dv_{IN} versus V_{IN}.

In order for the amplifier to operate as described above, the control voltage of V_R needs to match V_{IN}. In other words, V_R should have a dependency on V_{IN}. In order to do so, V_R can be generated from V_{IN}, Figure 3.19 illustrates the implementation of this idea by means of a low pass filter. The DC component of v_{IN} is obtained and it is then adjusted so that V_R is the appropriate level to result in the needed variable source resistance within the range of V_{IN}. It should, however, be mentioned that there are different methods to generate V_R based on V_{IN}, or on a voltage signal related to V_{IN}. For example, the DC level of V_{IN} depends on the preceding conditioning block and therefore this voltage can, in some cases, be used to generate V_R.

As described above, a stage of the common source amplifier with a source resistance can be made to implement a variable gain that adapts to the input level. The emphasis of the design of such a single stage is to adjust the gain in such a way that it varies to have a similar profile as that is required. In this case, the gain cannot be very high, therefore, the voltage output may not reach the required amplitude, and another stage of amplification will be needed. This stage can be a conventional amplifier as it receives a voltage signal with a fixed DC level. Thus, the amplification block can have two stages. One provides variable gain and the other, a conventional amplification.

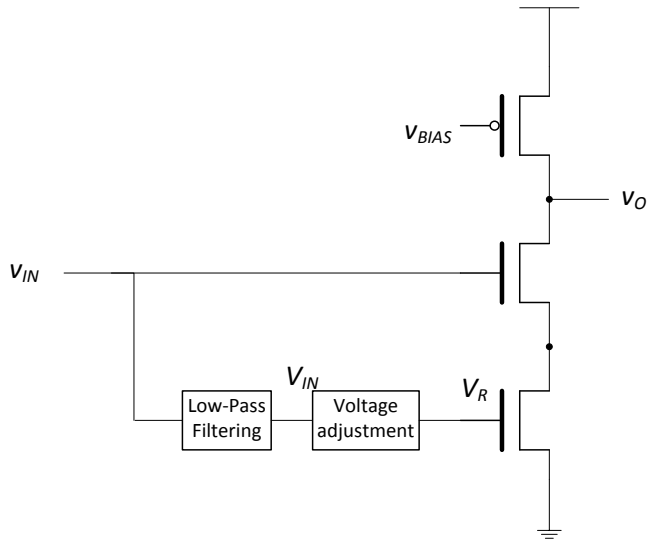


Figure 3.19: Diagram of an implementation of a generation of V_R from V_{IN}.

3.4 Summary

In this chapter the development of a method to design the adaptive amplifiers has been presented. The adaptability of the circuit is of the voltage gain to a large variation of the input DC level. The need for such adaptive amplifiers has been presented. In particular, an example of an amplifier to be incorporated in a wide-range high-sensitivity current-voltage converter is described in detail in order to demonstrate the complexity of the task and the challenges in the design of such amplifiers.

This kind of amplifier operates in a way that is very different from conventional ones, the work of developing a design method has started with a study of the basic configurations of amplifiers. The focus was on the common source amplifier with a source resistance, as its gain can be adjusted by the source resistance. Also, the behaviour of the amplifier with the changing DC input levels has been analysed.

Based on the study of the basic configurations, a scheme of two blocks has been proposed to implement a voltage gain varying nonlinearly with the input DC level in a complex manner. In such an implementation, one needs multiple stages of different nonlinear amplifications. Two methods of designing nonlinear amplifiers have been

proposed. The first one is to explore the nonlinear voltage transfer characteristics of a common source amplifier. As the voltage transfer ratio is input-level-dependent, a range of input DC levels correspond to a segment of the characteristic. The parameters of the amplifier are adjusted to make the ratio corresponding to the different input levels in the segment suit the required input-level-dependency. In this case the voltage transfer may not have any significant gain. The second method is to adjust the source resistance of a common source amplifier by a voltage related to that of the DC level of the input. With this method, the gain can also be made very DC-input-level-dependent in a nonlinear manner, and a large difference between the minimum and maximum gain can be obtained. However, it should be noted that an amplifier designed using either of the methods operates with a "local linearity" i.e. the gain is fixed at any given input DC level.

The amplifiers designed with the method described above can be combined with different building blocks, such as source followers and conventional amplifiers to make varieties of adaptive amplifiers for different applications. In the next chapter, the design of the adaptive amplifier to be used to enhance the voltage signal of the I-V converter is described and the simulation results presented.

Chapter 4

Design of an adaptive amplifier for input-dependent voltage enhancement

In Chapter 3, a design method for adaptive amplifiers is proposed. This chapter presents a specific example of applying the method in order to demonstrate its effectiveness. Specifically, it is the design of an adaptive amplifier for the current-voltage converter mentioned in Section 3.1 is presented.

The amplifier to be designed is for the signal enhancement of the current-to-voltage converter. The input voltage of the amplifier is characterized as shown in Figure 3.4 and the required voltage gain versus input DC level is illustrated in Figure 3.5. The two characteristics are presented in this chapter as Figure 4.1 (a) and (b). In order to implement the required variable gain, the two-block scheme shown in Figure 4.2 is used in the design. The first block is to "pre-amplify" the input voltage signal, and the main objective is, in fact, to apply a voltage transfer, rather than voltage amplification, of which the small signal transfer ratio is characterized to have a similar DC level dependency as that shown in Figure 4.1 (b). The second block is to amplify the voltage signal with a gain variable according to the DC input to reach the required amplitude.

This chapter is organized as follows. The design of the first block is presented in Section 4.1, and Section 4.2 is dedicated to that of the second block. The performance evaluation and analysis of the amplifier is found in Section 4.3.

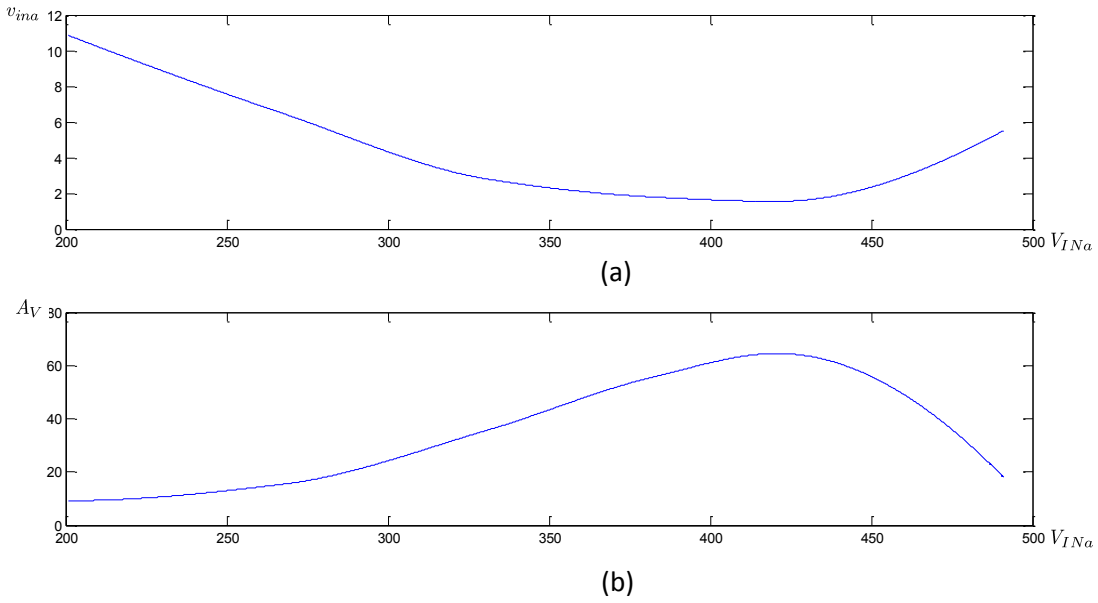


Figure 4.1: (a) Characteristic of the input voltage to the adaptive amplifier. (b) Required gain for the amplifier in order to get the right output.

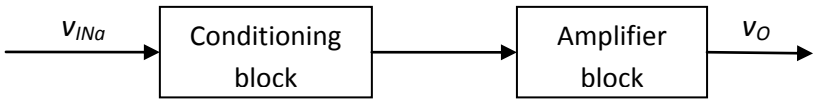


Figure 4.2: Block diagram of the adaptive amplifier used.

4.1 Design of the conditioning block

The input voltage of this block is characterized as shown in Figure 4.1 (a). One can see that its DC level is from 0.2 V to 0.5V, requiring a wide input operating range for the first stage of the block. Also, the overall gain of the amplifier needs to be strongly input-DC-level-dependent, as shown in Figure 4.1 (b). The required maximum gain that is at the input level of 420 mV should be made about 7 times larger than that at 0.2 V, while the gain at the level of 490 mV needs to be much lower than the maximum. This kind of "bell-shaped" characteristic cannot be easily implemented in one step. A "pre-amplifier" in the conditioning block is designed to implement such a bell-shaped voltage signal transfer characteristic, while the amplitude of the transfer ratio is expected to be

modest. The main challenge in the design of this block is to make the characteristic profile as close to that shown in Figure 4.1 (b) as possible while keeping the signal distortion within the limit.

Considering that the Input DC voltage range is from 0.2 to 0.5 volts, one can use the PMOS version of the common source amplifier with a source resistance shown in Figure 4.3 in order to implement the voltage transfer as mentioned in Section 3.3.1. In this design, the limitation of the maximum acceptable distortion and the required profile of gain variation are the most important issue. Thus, the equivalent resistance of P_1 in the pre-amplifier should be large, in order to provide a large feedback to extend the input range, and the gate-source voltage of P_1 should also be large enough for the same purpose. Additionally, the bias current of the circuit should be adjusted to secure that wide input range. To this end, the gate-source voltage of N_1 that serves as a current source should be high enough to drive the transistor in strong inversion mode but not too high keep the device operating in the saturation region. Moreover, the gate length of N_1 should be long enough not to have a significant effect of the channel-length-modulation.

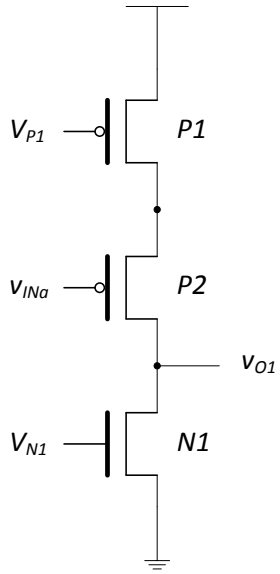


Figure 4.3: Pre-amplification common source amplifier with a source resistance.

In the circuit shown in Figure 4.3, the transconductance of P_2 can be modest as the transfer gain is not a critical issue. However, the gate capacitance of P_2 needs to be

minimized in order to have a good frequency response, particularly in case that the current driving capacity of the previous stage is weak. Therefore, P_2 should be minimum-sized. It should also be noted that, to achieve the needed non-linear characteristic of the voltage transfer, another important issue is that the input DC level at which the maximum transfer gain of the circuit occurs, must match that of the peak gain specified in Figure 4.1 (b). This adds another constraint in the adjustment of the device parameters and the bias voltages. If this matching cannot be obtained, the input voltage would first have to be applied to a voltage shifter to make its DC range shifted to suit the range of the pre-amplifier.

In the circuit design, taking the above mentioned elements into consideration, the transistors of the pre-amplifier, as shown in Figure 4.3, are sized as specified in Table 4.1. The voltage V_{N1} at the gate of N_1 is 0.61 V, which produces a bias current of 4.43 μA, and the voltage of V_{P1} is also 0.61 V.

Table 4.1: Transistor sizing in the circuit shown in Figure 4.3 serving as the first stage of the conditioning block.

Name	Size ratio	Operation mode
P_1	220 nm / 620 nm	Triode
P_2	220 nm / 180 nm	Saturation
N_1	300nm / 360 nm	Saturation

The circuit of the pre-amplifier has been simulated using HSpiceS with the transistor models of a 0.18 μm CMOS technology. The voltage transfer characteristics obtained are shown in Figure 4.4. If the DC input V_{IN} is changed from 0.2 V to 0.5 V, the small signal transfer ratio will first increase from 0.735 to its peak value of 1.168 then decrease to 0.841. The input DC level, at which the transfer ratio is at its maximum point, is 0.38 V, approximately matching the point in the characteristic shown in Figure 4.1 (b). This gives the required "bell-shaped" small signal transfer characteristic. The signal distortion at a given level of V_{IN} is measured with (3-8) and is expressed as follow

$$K_D = \pm|v_{in}|\frac{\Delta A_V / A_{Vavg}}{\Delta V_{IN}} \quad (4\text{-}1)$$

where $\Delta A_V = 1.168 - 0.735$, $A_{Vavg} = (1.168 + 0.735)/2$, $\Delta V_{IN} = 0.385$ V – 0.2 V, and $|v_{in}|$ is the amplitude of the signal variation at a gain level. Considering that the amplitude of the input variation is larger at the lower end of the DC input range then that in the higher end, as shown in Figure 4.1 (a). The worst case scenario occurs at V_{IN} = 0.2 V. If the maximum amplitude at that point is 10.85 mV, the maximum signal distortion will be ±2.67%

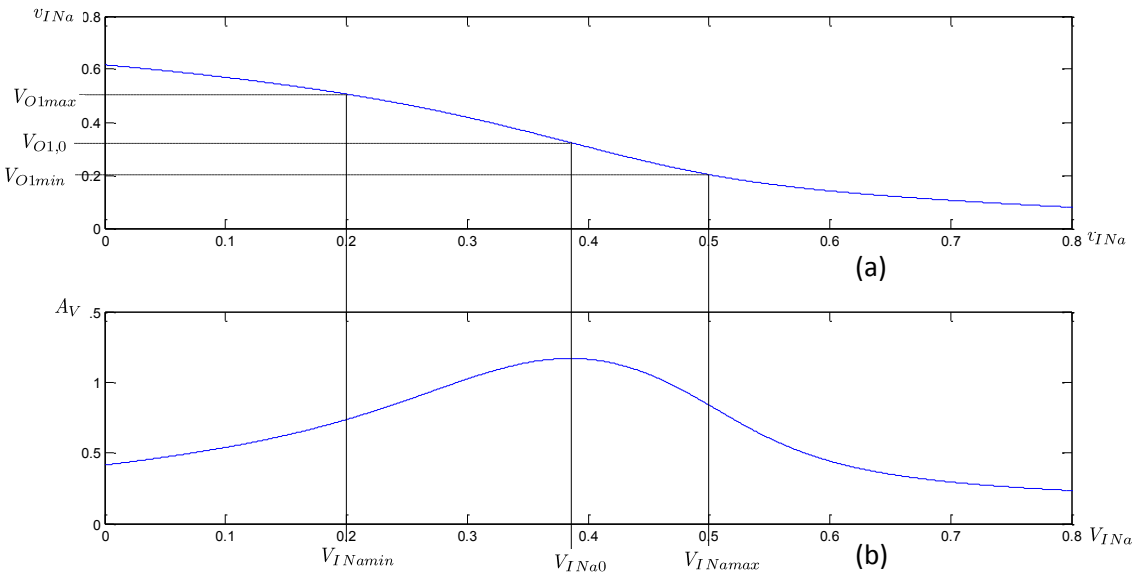


Figure 4.4: Characteristics of the pre amplifier shown in Figure 4.3. (a) v_{OI} versus v_{Ina}. (b) Derivative of (a).

Figure 4.5 illustrates the simulation waveforms of the pre-amplifier. The input voltage, shown in Figure 4.5 (a), is generated by the I-V converter and the output of the pre-amplifier is shown in Figure 4.5 (b). One can see that the amplitude of the input voltage variation is very different from one DC level to another, which is caused by the poor function of the I-V converter. The output waveform shown in Figure 4.4 (b) illustrates that the amplitude at the lower and upper ends of the DC level is smaller than that of the input, while at the mid-level of the input DC is slightly larger. Thus by means of the pre-amplifier, the difference between the maximum and minimum amplitudes is

reduced from 7 times to 4 times. Also, it should be noted that the range of the DC level of the output voltage as shown in Figure 4.5 (b) is from 0.5 V to 0.21 V corresponding to that of the input, i.e. from 0.2 V to 0.5 V.

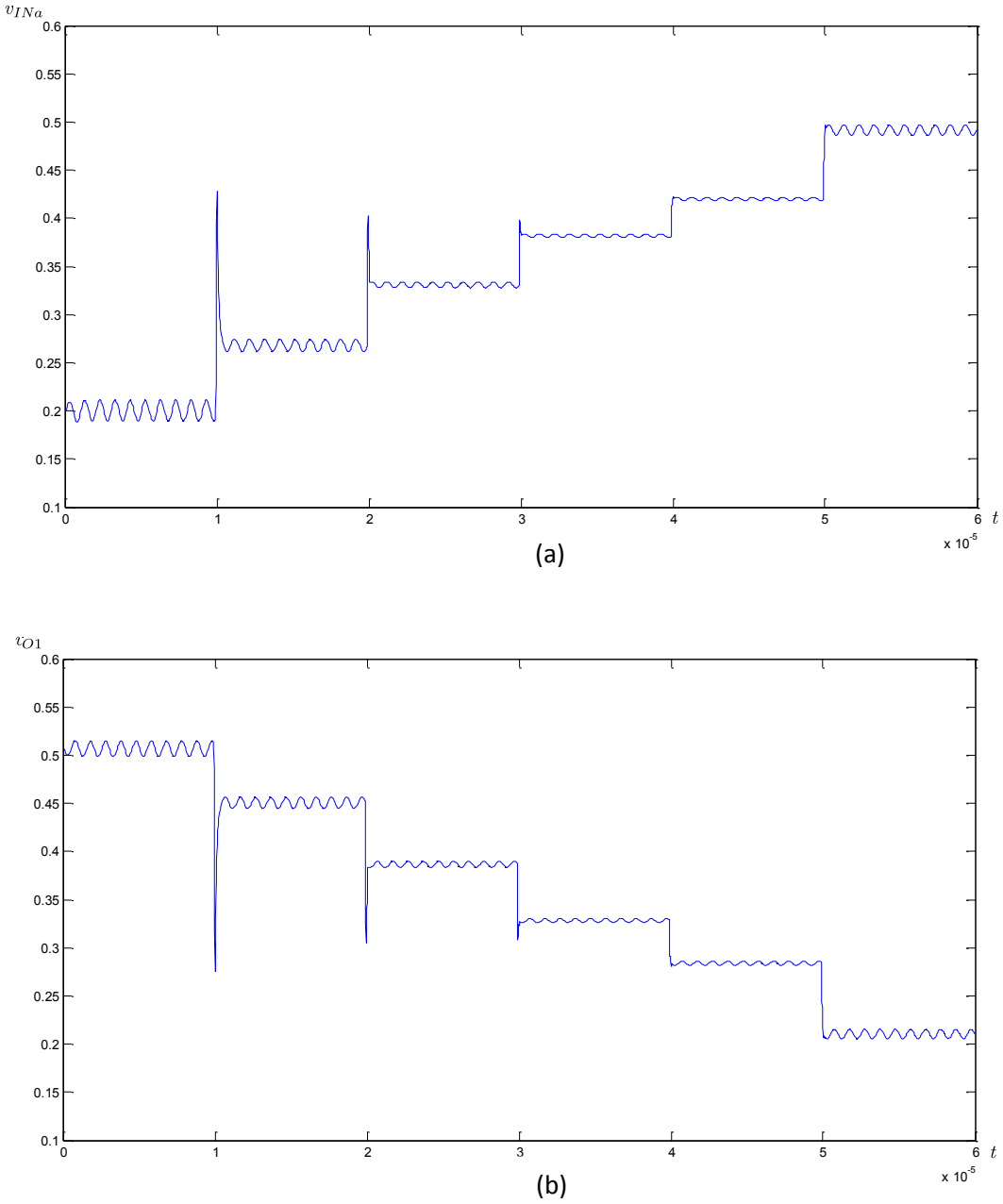


Figure 4.5: (a) Input voltage signal of the pre-amplifier. (b) Output voltage signal of the pre-amplifier.

Even though the voltage transfer performed by the pre-amplifier is not as ideal as one would wish, it does transform the voltage signal to facilitate the operation in the following stages. For a further improvement of the voltage signal, one needs another wide-range voltage amplifier, in which the gain can simply decrease with the input DC level. This can be done by a NMOS version of the common source amplifier with a variable source resistance, as shown in Figure 3.17 (a). This kind of amplifier requires a minimum input DC level that is much higher than 0.21 V shown in Figure 4.5 (b). Thus, a source follower is used to lift the range of the DC voltage of (0.21 V to 0.5 V) to (0.8 V to 1.1 V). The design of the succeeding stages that make the amplification block is presented in the next section.

4.2 Design of the amplification block

The input voltage of the amplification block is shown in Figure 4.6. The objective of the operation in this block is to amplify the signal amplitude in such a way that the gain decreases with the DC input to make the amplitude of the output signal more "uniform", or less strongly DC-level-dependent, about which the details of the requirement are presented in Section 3.1.

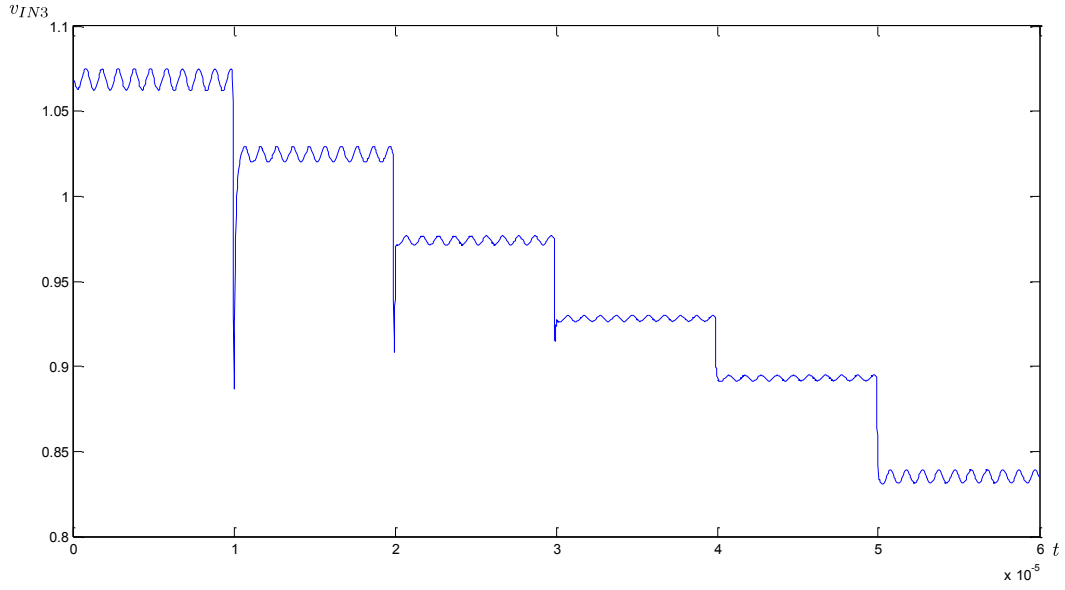


Figure 4.6: Input signal of the amplification block.

An NMOS version of the common source amplifier with a source resistance, as shown in Figure 3.17 (a), is used to be the first stage of the amplification block. The purpose of this first stage is to make the input voltage signal amplified and the DC level uniform. The critical issues in the design are as follows:

1. The gain of the amplifier can be very modest as the emphasis is on the difference between its maximum and minimum values.
2. With a given V_R, the characteristic of dv_{OUT}/dv_{IN} versus the input voltage should be "flat" enough that a small deviation of the level will not result in a significant reduction of the gain, thus ensuring a limited distortion.
3. The transistor serving as the source resistor has its gate voltage V_R adjustable, to implement the variable gain of the amplifier. On one hand the range of the equivalent resistance of the transistor should be wide enough to produce the required range of the gain. On the other hand, this equivalent resistance should not be too sensitive to V_R so that a small shift of the level of V_R will not bring the amplifier out of the biasing point. The gate voltage V_R is generated by a voltage transfer unit in such a way that it is related to the input DC voltage V_{IN}. Reducing the sensitivity of the resistance to V_R facilitates the generation of V_R with a less restrictive requirement of precision. To this end, the single NMOS transistor is replaced by two parallel transistors, namely N_3 and N_4, as shown in Figure 4.7.

Taking all the above issues into consideration, the transistors in the circuit shown in Figure 4.7 are sized as specified in Table 4.2. The transistors P_5 and N_2 have a large ratio of W/L in order to have, at a given V_R, a low sensitivity of the gain to the DC input. When the gate voltage V_{P5} = 1 V, the bias current is 88 μA. The transistors N_3 and N_4 are moderately sized and N_4 has a constant gate voltage V_{N4} of 1 V. With this set of transistor sizing and biasing, the characteristics of this stage are illustrated in Figure 4.8, indicating the feasibility of implementing the required ratio of gain.

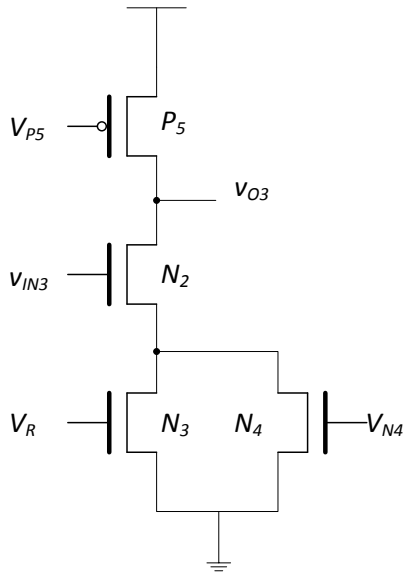


Figure 4.7: First stage of the amplification block

To achieve the objective of minimizing the amplitude difference of the signal variation at different DC levels, V_R is adjusted, by means of an ideal piecewise voltage source to make the first stage produce its output voltage as shown in Figure 4.9 when the input is shown in Figure 4.6. The amplitude difference in the voltage signal is about 2 to 3 times, compared to that in the input voltage, i.e. 4 times. The characteristic V_R versus V_{IN3} required to achieve this variable gain amplification is shown in Figure 4.10.

Table 4.2: Transistor sizing in the circuit shown in Figure 4.7.

Name	Size ratio	Operation mode
P_5	2.2 µm / 180 nm	Saturation
N_2	4.4 µm / 180 nm	Saturation
N_3	220nm / 760 nm	Triode
N_4	260nm / 240 nm	Triode

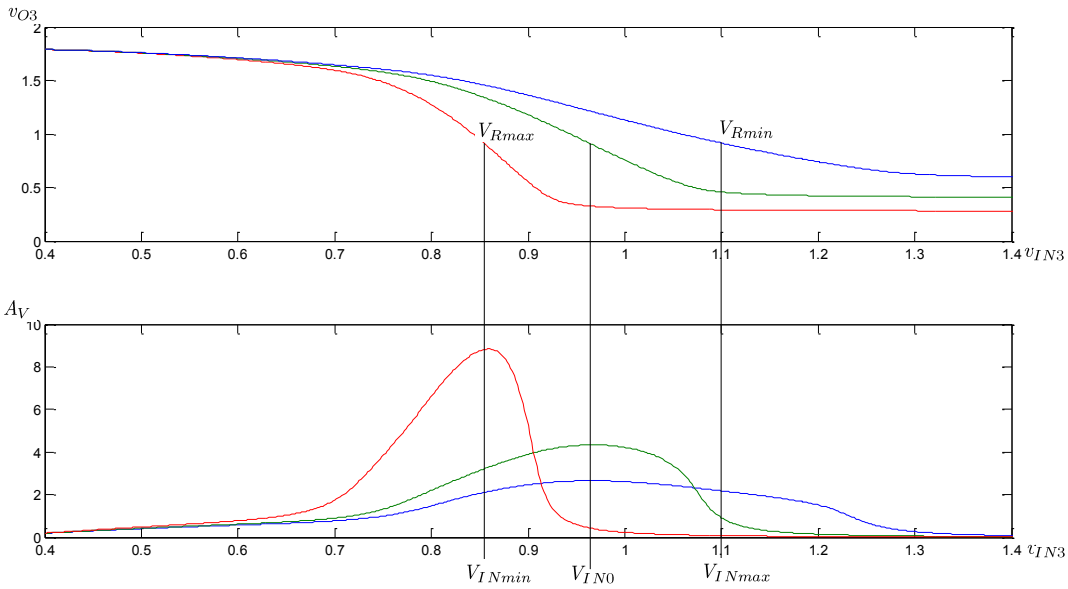


Figure 4.8: Characteristics of the first stage of the amplification block amplifier shown in Figure 4.7. (a) Output v_{O3} versus input v_{IN3} with V_R = 0.85 V, 0.97 V and 1.42 V. (b) Derivatives of (a).

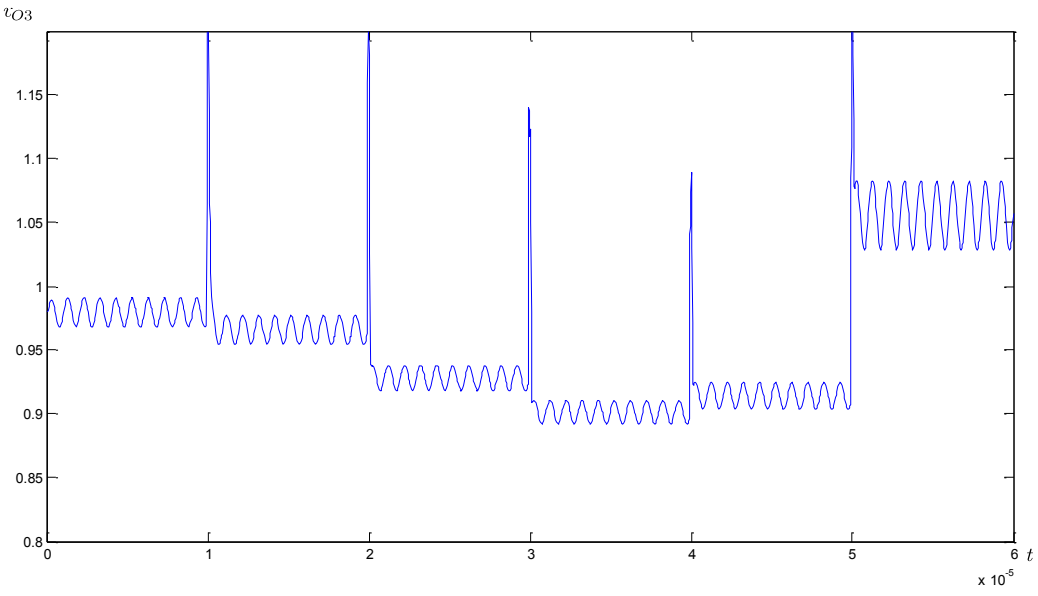


Figure 4.9: Waveform of the output of the variable amplifier, assuming ideal V_R.

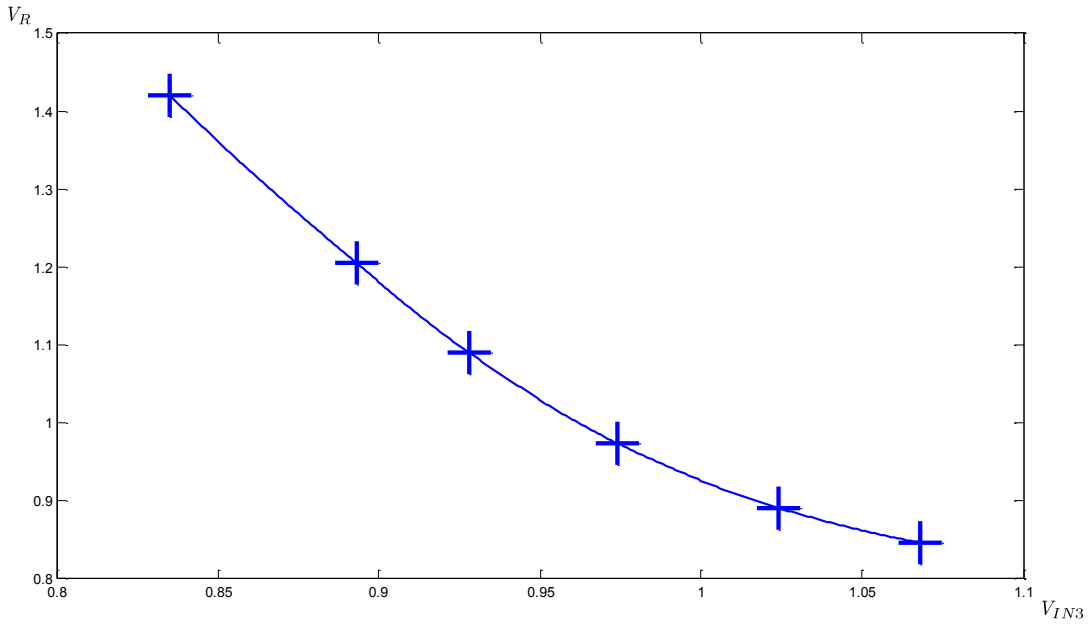


Figure 4.10: Characteristic V_R versus V_{IN3} required to obtain the output voltage shown in Figure 4.11.

Having Characterized V_R for the required variable-gain amplification, one needs to build a voltage transfer unit to produce V_R based on V_{IN3} or a voltage related to it. The voltage V_{IN3} is the DC component of the input and is not available in this circuit. However it is related to V_{Ina}, the DC input of the conditioning block, i.e. the DC component of the output of the I-V converter. The equivalent voltage of the DC component is V_{GN}, found at the common gate node of the transistor N_{C3} and N_{C4} shown in Figure 3.3 (b). The DC voltage V_{GN}, i.e. V_{INa}, is first converted to V_{IN2} by the pre-amplifier and then shifted to be V_{IN3}, Figure 4.11 (a) illustrates the relationship between V_{INa} and V_{IN3}. Based on this relationship, the characteristic of V_R versus V_{INa} is obtained, as shown in Figure 4.11 (b). A circuit unit having a similar characteristic as is illustrated in Figure 4.11 (b) can be used to generate V_R from V_{INa}. The unit designed for this purpose is shown in Figure 4.12.

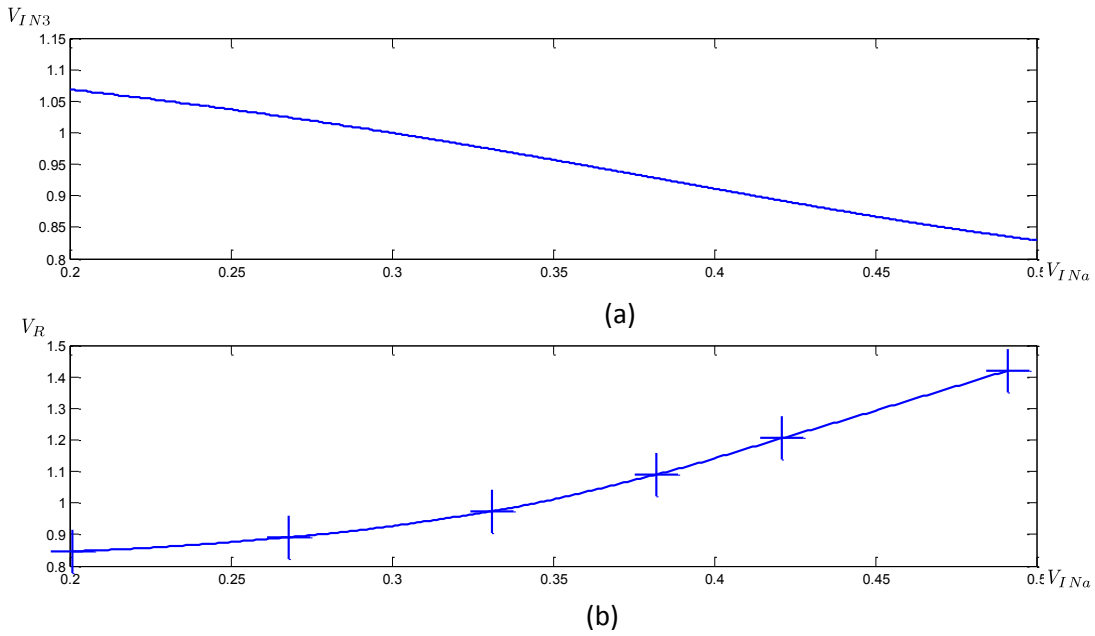


Figure 4.11: (a) Characteristic of V_{IN3} versus V_{Ina}. (b) Characteristic of V_R versus V_{Ina}.

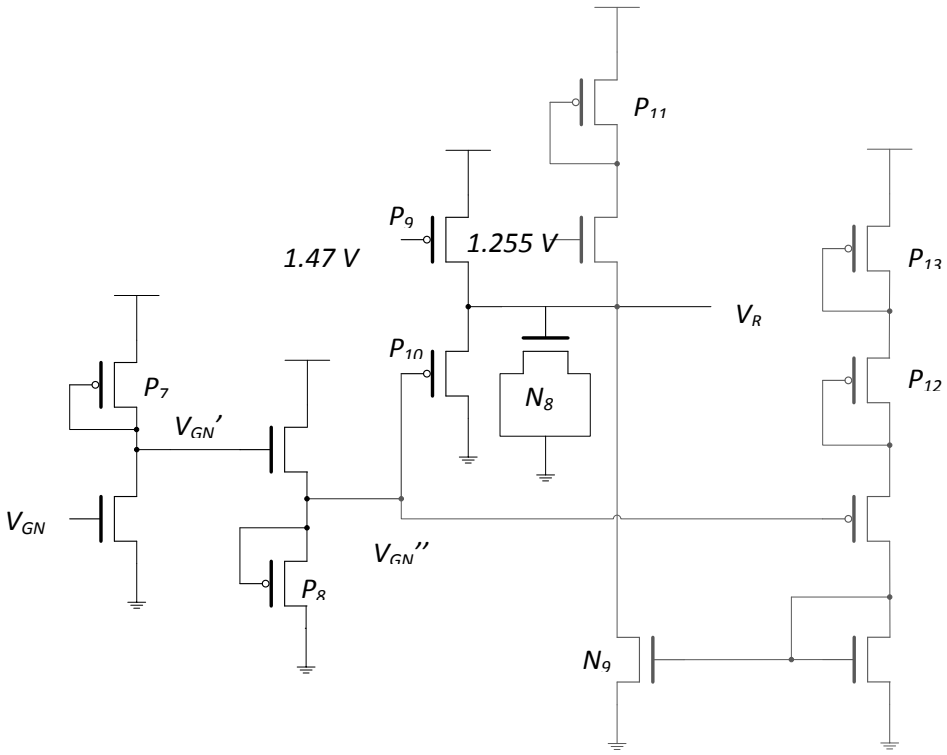


Figure 4.12: Voltage transfer unit that converts V_{INa} into V_R. Transistor sizes are specified in Table 4.3 if not minimum sized.

As V_R needs to increase with V_{Ina}, i.e., $dV_R/dV_{Ina} > 0$, but at a small rate, two inversion stages of two transistors, of which the biasing current is determined by a diode-connected PMOS, are used in the circuit unit shown in Figure 4.12. A stage of voltage shifting is also used to raise the voltage to the required level. The output voltage is fed back to control two additional current sources adjusting the amount of voltage shift in order to fine tune the characteristic of this circuit. With the sizing of the transistors specified in Table 4.3, the characteristic of this unit is shown in Figure 3.13. It is almost superposed with the one shown in Figure 4.11 (b) except in the upper end of the curve. However, this deviation of V_R in the upper side is not critical to the circuit operation, as the source-drain resistance of the transistor controlled by V_R is not sensitive to the variation of V_R at that a high level.

Table 4.3: Size of the transistors shown in Figure 4.12

Name	Size ratio	Name	Size ratio
P_7, P_8	220 nm / 1 μm	N_8	1 μm / 1 μm
P_9, P_{11}, P_{12}, P_{13}	220 nm / 1.8 μm	N_9	220 nm / 720 nm
P_{10}	2.2 μm / 180 nm		

By using the circuit shown in Figure 4.12, the first stage of the amplification has a DC-level-dependent gain that is characterized as shown in Figure 4.14. Its input and output voltage is shown in figure 4.15. We can see that the difference in signal amplitude has been visibly reduced by this stage. Another stage of amplification is needed to further reduce the difference in amplitude. Furthermore, the DC voltage variation of the output is not fixed; the succeeding stage will again be a common source amplifier with a variable source resistance.

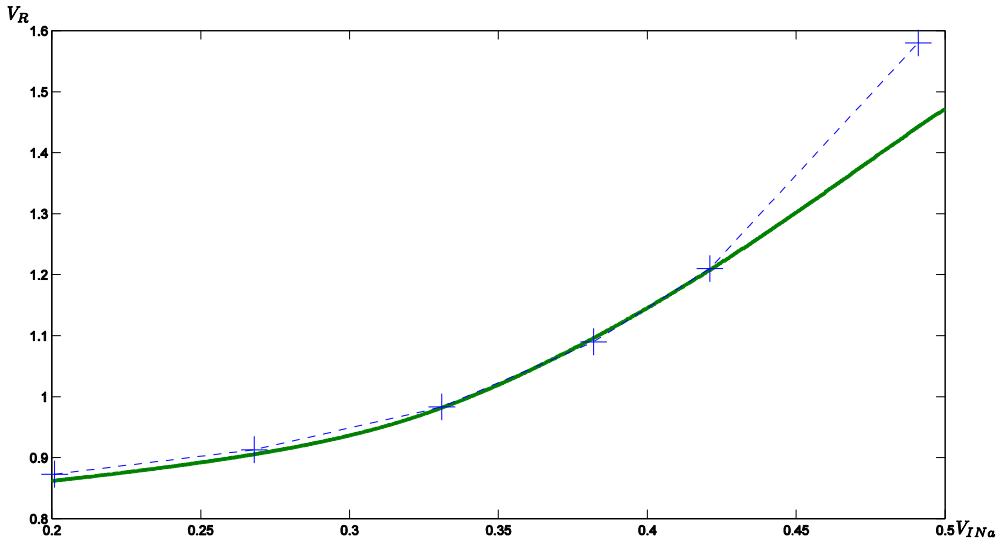


Figure 4.13: Characteristics of V_R versus V_{INa} implemented by the circuit unit shown in Figure 4.12. It is super-imposed with the ideal V_R, shown in Figure 4.11 (b).

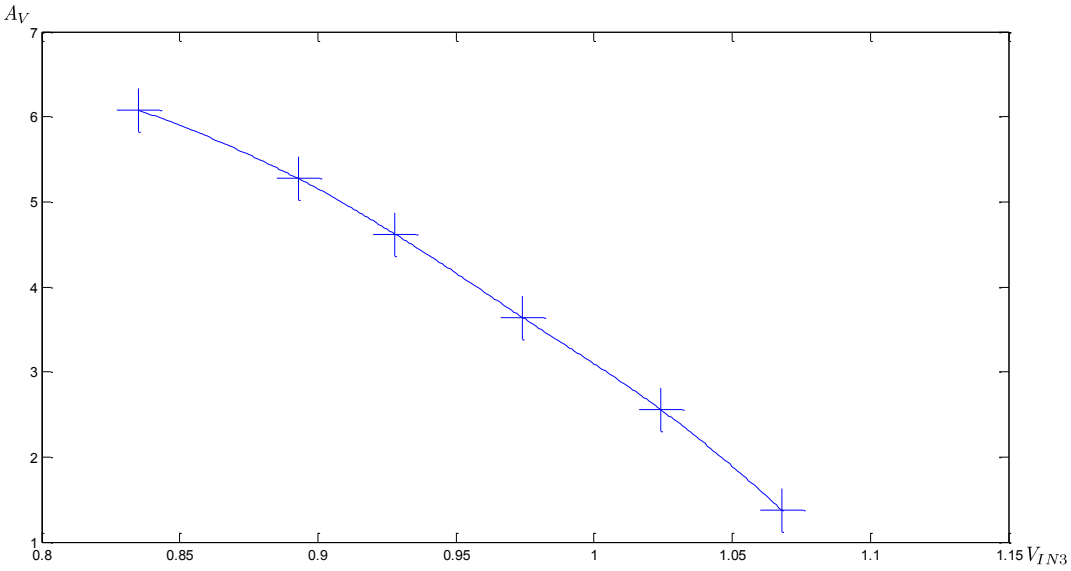


Figure 4.14: Characteristic of the gain versus V_{IN3}.

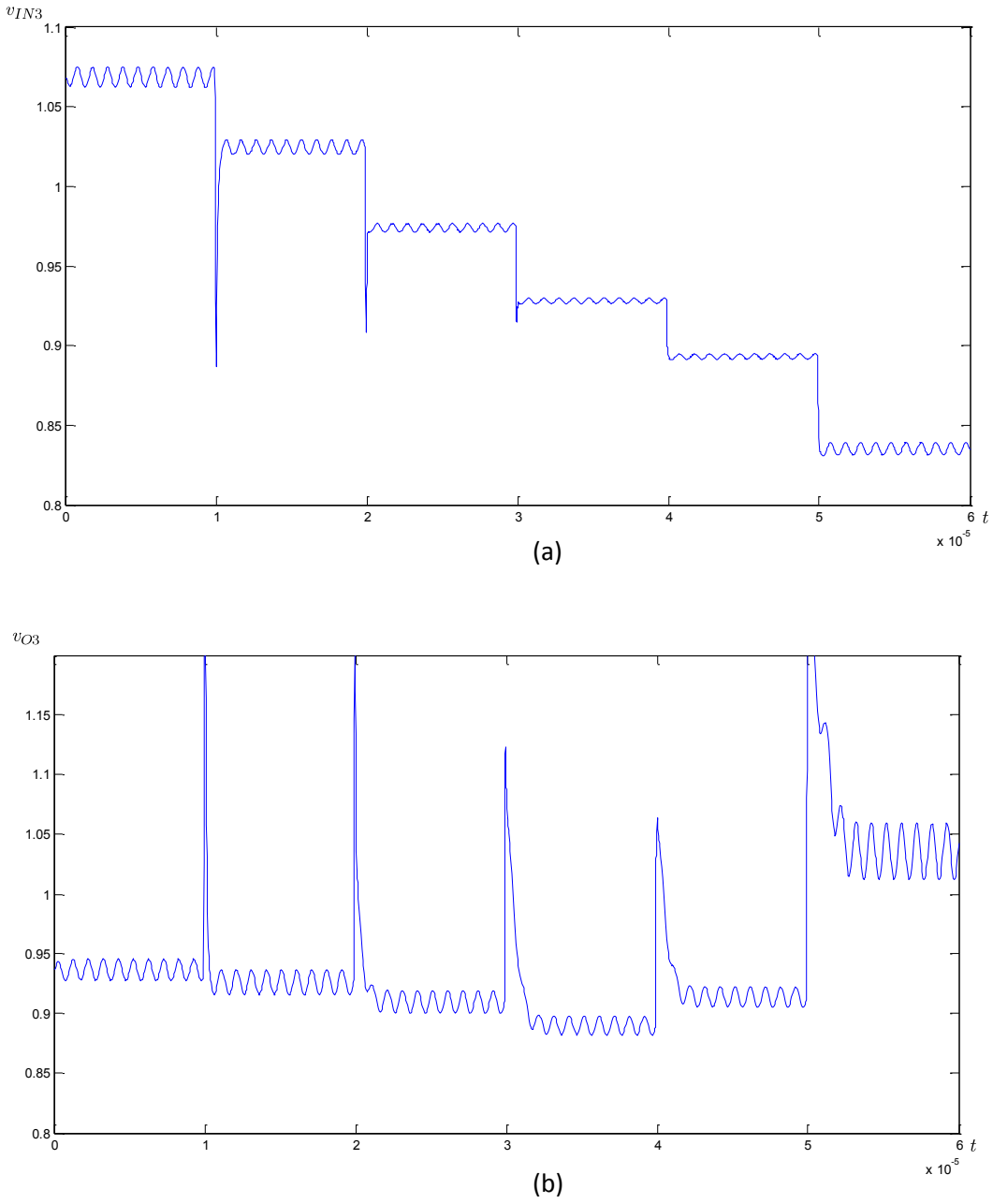


Figure 4.15: Waveform of the input (a) and output (b) of the variable amplifier shown in Figure 4.7, using the generated v_R shown in Figure 4.12.

The second stage of the amplification block is used to further amplify the signal amplitude and reduce the amplitude difference in different DC levels. One can see from the waveform, shown in Figure 4.15 (b), of the voltage v_{O3}, i.e. the input of the second stage, that to make the amplitude uniform, the gain in this stage needs a relatively weaker

variation than that in the preceding one. Also the gain needs to be higher in the lower side of the DC input range, and a NMOS common source amplifier with a source resistance suits this case. Moreover, as shown in Figure 4.15 (b), the DC level of the input varies from 0.9 V to 1.03 V, which is appropriate for the CS amplifier.

The circuit Diagram of the second stage is shown in Figure 4.16. The voltage V_{R2} is used to tune the equivalent resistance of N_6 and N_7 combined to adjust the gain and the DC output level. The parallel connection of N_6 and N_7, with a fixed gate voltage applied to N_7, is to make the equivalent resistance that is related to the circuit biasing less sensitive to the deviation of the level of V_R.

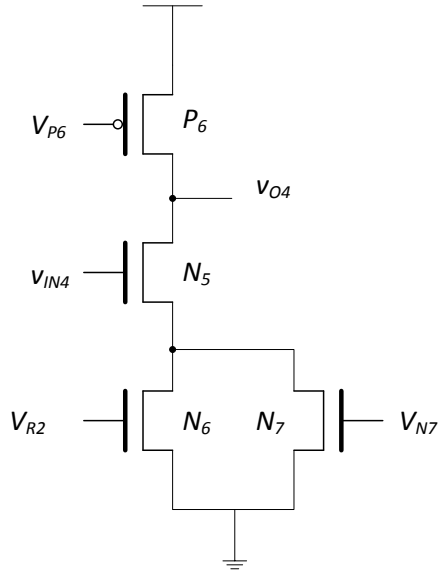


Figure 4.16: Second stage of the amplification block.

In this design, the transistor sizes of the circuit shown in Figure 4.16 are specified in Table 4.4. The voltage V_{P6} is 1 V, resulting in a bias current of 44 μA, and V_{N7} is also 1 V to make N_7 operate in the triode region. Finally, the transistors P_6 and N_5 are narrower than in the preceding stage, to increase the gain.

Table 4.4: Transistor sizing in the circuit shown in Figure 4.15.

Name	Size ratio	Operation mode
P_6	2.2 μm / 360 nm	Saturation
N_5	2.2 μm / 180 nm	Saturation
N_6	220nm / 1.8 μm	Triode
N_7	220nm / 620 nm	Triode

In the circuit shown in Figure 4.16, V_{R2} is used to adjust the combined equivalent resistance of N_6 and N_7 in order to tune the bias of N_5 and the amplification gain when the DC level of V_{IN4} changes, similarly to the way that V_R determines the bias and the gain in the first stage of amplification. The relationship between V_R and V_{INa} is characterized and presented as the dashed curve in Figure 4.17. A voltage transfer unit has been designed to convert V_{INa}, i.e. V_{GN} of the I-V converter, into V_{R2}. The unit is shown in Figure 4.18 and the characteristic of the unit is presented as the solid curve in Figure 4.17. The design of this unit is based on the same principle as that of the first stage. Current sources are used to tune the bias current of the transfer unit. These current sources are controlled by the voltages generated in the unit so that each of the sources is activated in a certain section of the input range in order to adjust the voltage transfer characteristic to what is needed. The detailed sizing of the transistors is presented in Table 4.5.

Employing the voltage level V_{R2} generated by the transfer unit to the amplifier shown in Figure 4.16, one can obtain the output voltage waveform shown in Figure 4.19 (b). In this waveform, the signal variation is large enough to satisfy the minimum amplitude requirement, and the difference in amplitude has been further reduced compared to that of the previous stage. Moreover the DC level is uniformized. The characteristic of the gain versus the input voltage is presented in Figure 4.20, we can see that the variation of the gain in this stage is different from that in the preceding stage, indicating a different nonlinearity of the circuit characteristic.

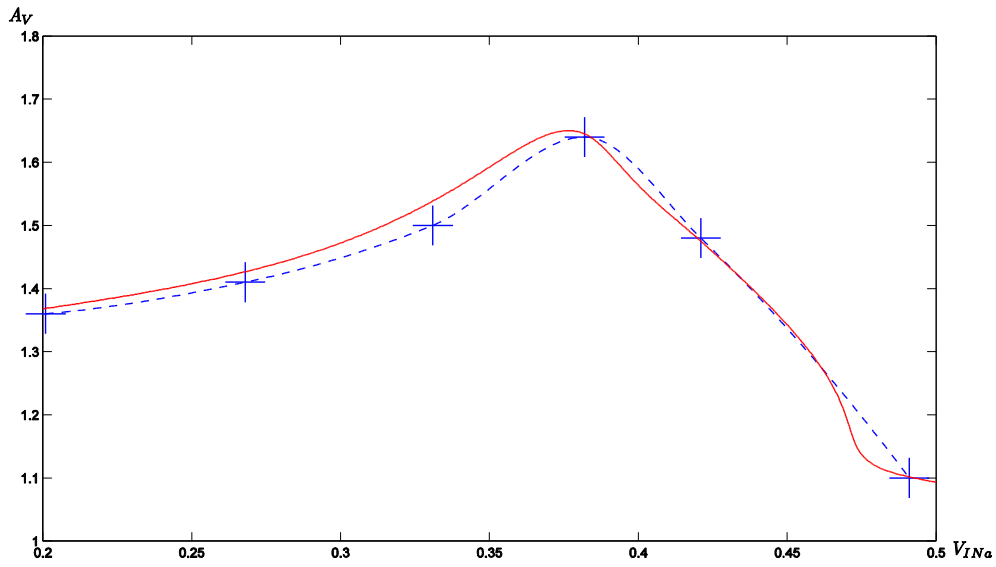


Figure 4.17: Anticipated characteristic of V_{R2} versus V_{INa} (dashed curve), and the characteristic generated by the circuit shown in Figure 4.18.

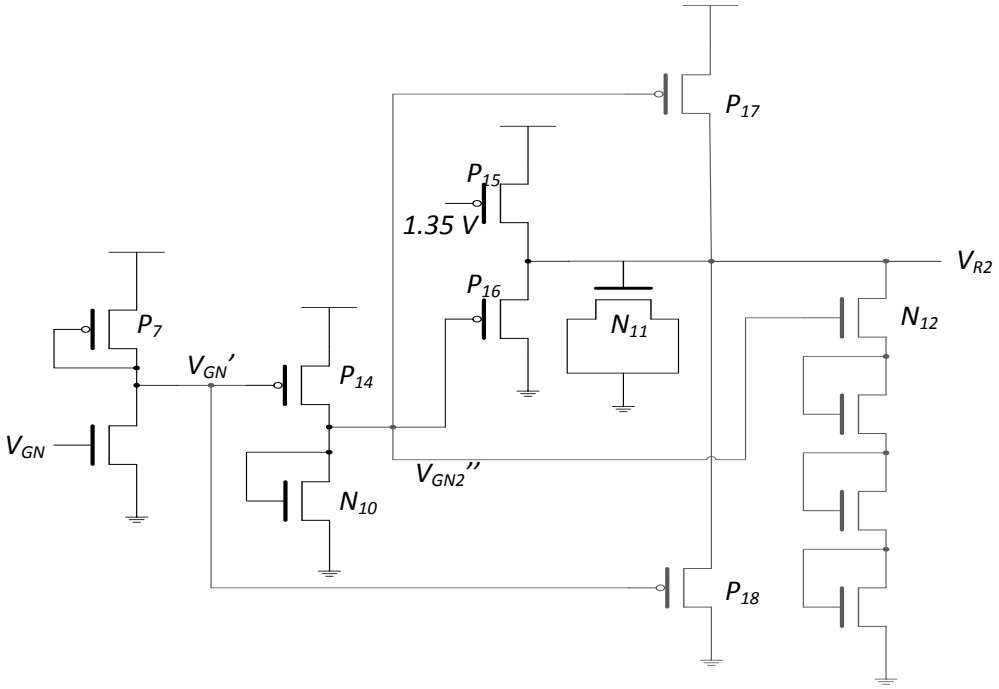
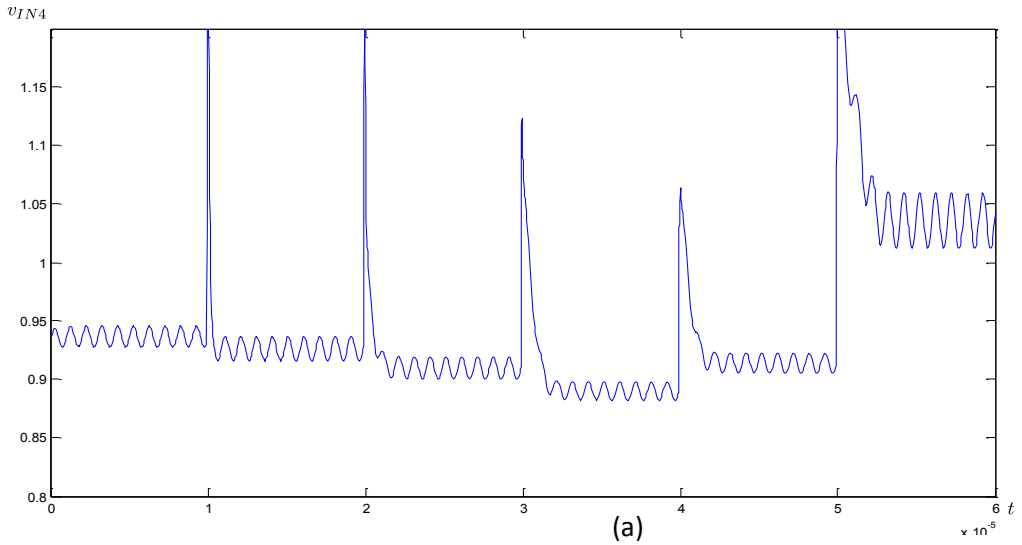


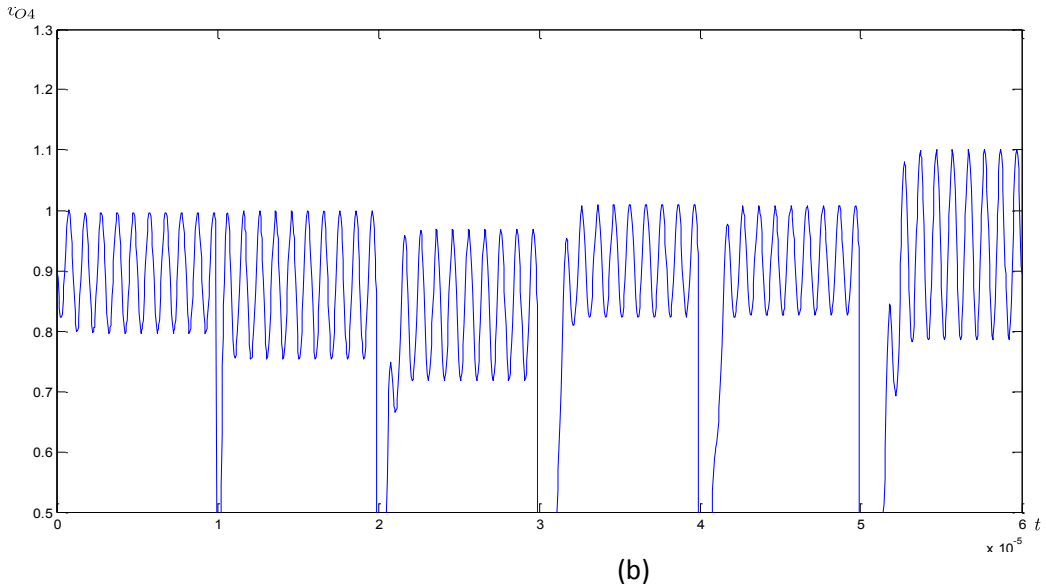
Figure 4.18: Voltage transfer unit that converts V_{GN} into V_{R2}. Transistor sizes are specified in Table 4.5 if not minimum-sized. The first inverter is the same as that shown in Figure 4.12 and thus shared.

Table 4.5: Sizes of the transistors shown in Figure 4.18

Name	Size ratio	Name	Size ratio
P_7	220 nm / 1 µm	N_{10}	220 nm / 1.54 µm
P_{14}	1.1 µm / 180 nm	N_{11}	1 µm / 1 µm
P_{15}, P_{16}, P_{18}	220 nm / 720 nm	N_{12}	220 nm / 1.8 µm
P_{17}	220 nm / 4 µm		



(a)



(b)

Figure 4.19: Input and output voltages of the second stage of the amplification block.

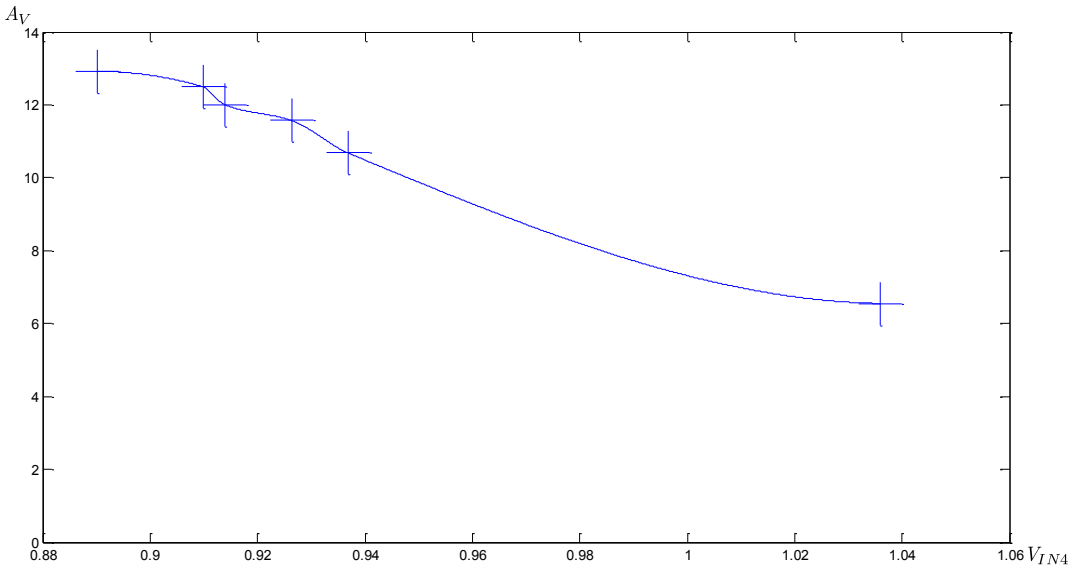


Figure 4.20: Characteristic of the gain of the second amplifier versus V_{IN4}.

Having shown the results of both amplifiers, it is now necessary to discuss the amplification block as a whole. The gain of the amplification block varied from 15 to 50 so that the signal shown in Figure 4.15 (a), which had a variation between the largest and smallest signal of 4, now has a variation of ≈ 1.5 times. Furthermore the DC input level was from 0.83 V to 1.08 V to a DC level of 0.9 V ± 0.05 V. It is now necessary to do a comprehensive analysis of the whole adaptive amplifier, such as its response to different inputs, its frequency response, and a measure of its distortion such as the Total Harmonic Distortion.

4.3 Evaluation of the overall performance of the adaptive amplifier

In this section, the overall performance of the adaptive amplifier is evaluated based on the HSPICE simulation results of the circuit. The specifications measured are of signal ranges, distortions, and frequency response.

Figure 4.21 illustrates the characteristic of the amplification gain versus the input DC level. One can see that the amplifier is able to operate with the input voltage, of which the

DC level can change in a range of 300 mV, and it has the sophisticated dependency of the gain to the input DC level similar to that required shown in Figure 4.1(b).

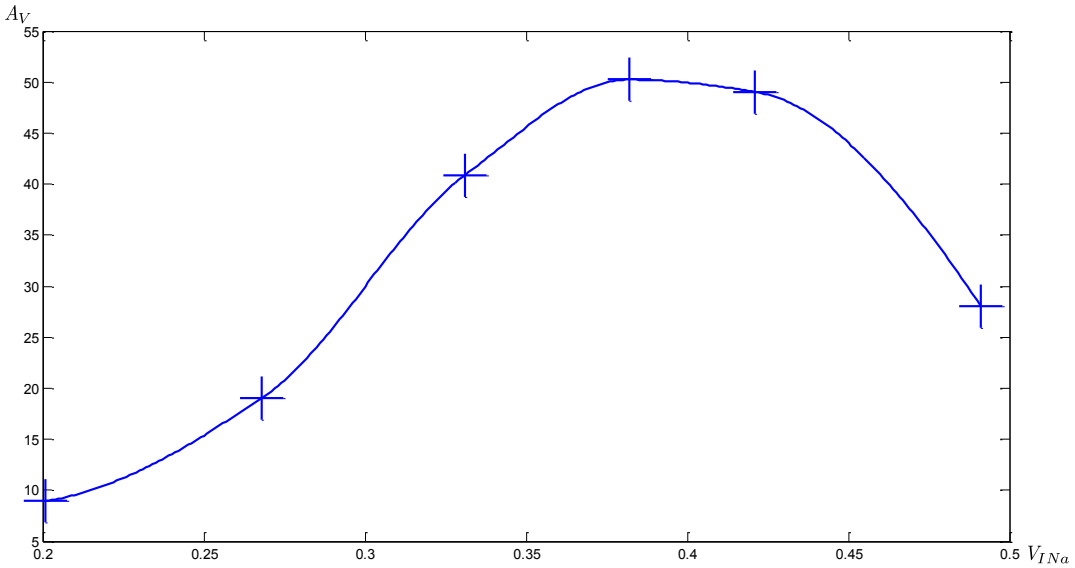


Figure 4.21: Characteristic of the gain versus the input DC level of the adaptive amplifier.

As mentioned previously, the circuit operation should be globally nonlinear and locally "linear". If the input DC level is fixed, the small signal component should be amplified with a fixed gain, and the gain will only change if the DC level is shifted. Table 4.6 shows that, at a given input DC level, e.g., V_{INa} = 0.201, the signal voltage gain A_V does not change much when the amplitude of the small signal v_{ina} doubled or halved. The deviation in the worst case of those shown in the table is less than 5 %. Thus, the local "linear" amplification is implemented in this circuit.

Table 4.6: Voltage gain and signal distortion of the adaptive amplifier

V_{INa} (V)	$\|v_{ina}\|$ (mV)	A_V (V/V)	*THD*
0.201	5.58	9.3	1.33 %
	11.2	8.9	2.65 %
	22.3	9.1	3.82 %
0.268	3.23	19	1.54 %
	6.45	19	2.84 %
	12.9	20	5.36 %
0.331	1.53	41	1.60 %
	3.05	41	2.37 %
	6.10	44	3.57 %
0.382	0.93	50	1.32 %
	1.85	50	1.91 %
	3.70	54	3.56 %
0.421	0.93	48	1.24 %
	1.85	49	1.72 %
	3.70	54	3.66 %
0.491	2.80	28	1.84 %
	5.60	28	1.93 %
	11.2	29	2.47 %

As the circuit is expected to perform a "linear" amplification if the DC level of the input voltage is fixed at a level within its range, one needs to measure the signal distortion in the voltage transfer of the amplifier. The Total Harmonic Distortion (THD) is measured and the result is listed in the right column of Table 4.6. As the nonlinear characteristics of the circuit is used to implement the required gain variation, a smaller $|v_{ina}|$ results in a smaller THD. To avoid a perceptible signal distortion, the amplitude of the input signal variation should be limited.

The frequency response of the amplifier is presented in Figure 4.22. As the circuit is not particularly designed for high frequency application, small-gate MOS transistors are used. Thus, the frequency response looks very modest.

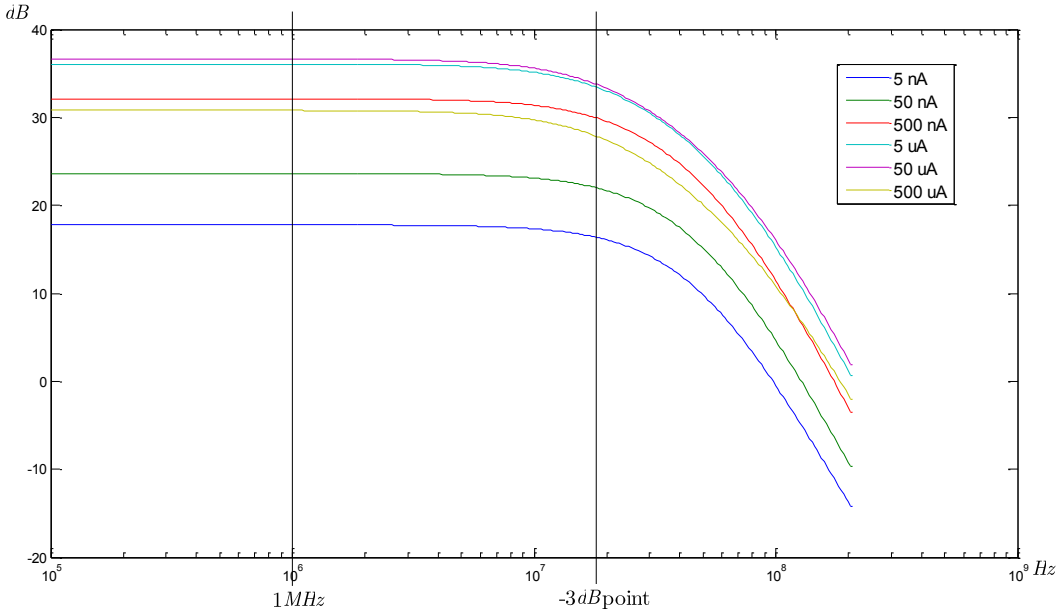


Figure 4.22: Frequency response of the adaptive amplifier obtained with different input DC levels as specified in Table 4.6.

The performance evaluation usually involves a comparison of the results obtained with those produced by the latest development in the topic area. After a comprehensive search, it seems that there are few research papers about amplifiers that can operate with both an input of changing DC level and also feature an input-dependent gain. The circuit presented in [Rijn96] allows the input DC voltage to shift, but it is not designed to have a particularly defined characteristic of the gain and the circuit operation is considered linear. The circuit in [Baze90] is also about input DC shift but does not discuss variable gain, additionally some specifications are not presented in the paper. The amplifier in [Duon06] has a variable gain, but the input DC needs to be fixed for the amplification. Table 4.7 summarizing the available data of the amplifier designs the most relevant found in literature for a comparison. It shows that the adaptive amplifier of this work is the most space-and-power efficient, but it has no advantage in signal distortion and operation

speed. However, it should be mentioned that one of its important features, a sophisticated characteristic of the gain versus the input voltage, does not exist in other amplifiers.

Table 4.7: Comparison of the results of some relevant work

Adaptive amplifier	Tech (μm)	Power (mW)	Frequency	$V_{INmin} \sim V_{INmax}$	$A_{Vmin} \sim A_{Vmax}$	THD	Area
[Rijn96]	0.8	25	15 MHz	0.8~2.5	1~4	0.04%	0.18 mm^2
[Duon06]	0.18	6.7	50 MHz	-	0~63	N.A.	0.34 mm^2
[Baze91]	not available	not available	not available	0.5~4,5	2	not available	not available
This work	0.18	0.2	18.2 MHz	0.2~0.5	8~50	5.36%	11.2 μm^2

4.5 Summary

In this chapter, the design of the adaptive amplifier used to enhance voltage signal in a wide dynamic range current-to-voltage conversion circuit is presented. It is to illustrated how the proposed method presented in Chapter 3 can be applied to design a circuit that can use the change of the input DC level to perform a sophisticated variable-gain amplification, while maintaining a fixed gain if the DC level does not change. The circuit is designed to have 4 cascading stages, and each of them is a very simple basic amplification unit or voltage follower. The amplifier has been simulated and the overall performance evaluated. The results show that the circuit is capable performing the required amplification, i.e., the gain varying according to the input DC voltage in the same complex manner as that required. As expected, it also performs a linear amplification with a fixed DC input. Hence, this amplifier is made to be unique and useful for the defined amplification task.

Chapter 5

Conclusion

Analog amplifiers are widely used in electronic systems and the design of amplifiers has a well established procedure involving the use of small signal circuit models under the condition of a fixed biasing point. The development of electronic systems offers new applications for analog amplifiers, and new signals to be amplified that may not necessarily to have a fixed DC component, which requires an automatic biasing-shift in the amplifier. If the DC level of the input is not fixed, the amplitude of the signal component can vary in a range much wider than that on a fixed DC level. Thus, variable gain may also be needed. Amplifiers that can operate with such inputs may not be linear circuits and the established design procedure is not applicable.

The objective of the work presented in the thesis is to develop a design method for adaptive amplifiers. Such an amplifier can adjust itself automatically to suit the DC level of the input voltage and the amplification gain is variable according to the DC level. To design such an amplifier, one needs to define the characteristics of the circuit according to the given input and the required output. One should expect a great diversity of the characteristics of amplification, as each application has different requirements. Hence, a design method that is applicable for many cases is needed.

The proposed design method is developed based on the analysis of the circuit characteristics under large signal conditions. The basic unit of the adaptive amplifier is a simple common-source amplifier consisting of three MOS transistors and one of the three serves as the source resistor. When the equivalent resistance value of the source resistor varies, both the biasing of the unit and the amplification gain will change. If the resistance is controlled by the DC component of the input voltage, the biasing point and the gain will be DC-input-dependent. A scheme of multi-stage of such basic units is proposed to implement the required characteristics of an adaptive amplifier. Each of the

stages performs a simple nonlinear voltage transfer. The nonlinear characteristic of voltage transfer can be adjusted by changing the source resistance. This change can be done by applying a varying gate-source voltage to the transistor, or by a shift of the drain voltage caused by the DC input shift while the gate-source voltage is fixed. One can implement the required DC-input-dependent voltage amplification by adjusting stage by stage the voltage transfer characteristics of the nonlinear units. The adaptive amplifiers designed with the proposed methods can be applied in sensors for conditioning. They can also be applied for various signal compensations techniques.

The proposed method has been applied to design an adaptive amplifier used for voltage signal compensation in a wide-dynamic-range current-to-voltage conversion circuit. The DC level of the input voltage can shift in a range of hundreds of millivolts, and the required nonlinear characteristic of the gain versus the input DC level is "bell-shaped", i.e. the gain increasing in the lower section of the DC range and decreasing in the upper section. By using four cascading stages, three common source amplifier and one source follower, the required variable gain amplification is implemented. The overall performance of the 4-stage amplifier has been evaluated by HSPICE simulation. The results show that the DC component of the input voltage can change from 200 mV to 500 mV while the amplifier is functional. The maximum gain is 50 when the input DC level is 0.39 V and the minimum gain is 9 when the input DC level is 0.2 V, which is very close to what is required. At a given input DC level, the amplification is nearly linear, i.e. the gain being almost "fixed" with a deviation of less than 5%.

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