A Universal Amplifier Module (UAM) in 0.18 µm CMOS (CMOSP18/TSMC) Technology With Some Applications in Analog Signal Processing

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ABSTRACT

A Universal Amplifier Module (UAM) in 0.18 µm CMOS (CMOSP18/TSMC) Technology With Some Applications in Analog Signal Processing

Md. A. H. Talukder

The amplifiers such as operational amplifier, operational transconductance amplifier, operational transresistance amplifier, current conveyor etc. are the basic building blocks in analog circuits and systems. These important basic amplifiers find wide spread applications in the integration of several electronic systems. However, different analog devices are preferred for different systems. It is difficult to use a single type of device to cater for the needs of different systems with diverse input output impedance environments.

In this thesis work, a Universal Amplifier Module (UAM) is designed and implemented in a modern 0.18µm CMOS (CMOSP18/TSMC) technology and its applications toward realization of second order voltage and current – mode filters are reported. Concepts of network transposition and nullor equivalent of ideal active devices are utilized to realize both voltage and current – mode filters using the same UAM module which is able to provide all the voltage and current mode operations (such as, OP-AMP with VCVS, OTA with VCCS, OTRA with CCVS, and CCCS).

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DEDICATIONS

To My Beloved Parents and brothers for their love, affection, encouragement and inspiration in every step of my life.

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LIST OF SYMBOLS AND ABBREVIATIONS

C	Capacitor
R	Resistor
Q_p	Pole Quality Factor
ω	Frequency in Radians
H(s)	Frequency Domain Transfer Function
AC	Alternating Current
V_{th}	Threshold Voltage of the Transistor
IC	Integrated Circuit
W	Channel Width of the MOS Transistor
L	Channel Length of the MOS Transistor
g_m	AC Transconductance
VDD	Positive Supply Voltage
VSS	Negative Supply Voltage
CMOS	Complementary Metal Oxide Semiconductor
PMOS	Positive-channel Metal Oxide Semiconductor
NMOS	Negative-channel Metal Oxide Semiconductor
MOSFET	MOS Field Effect Transistor
VLSI	Very Large Scale Integration
OP-AMP	Operational Amplifier
OTA	Operational Transconductance Amplifier
OTRA	Operational Transresistance Amplifier
CCII	Second-Generation Current Conveyor

VCVS	Voltage Controlled Voltage Source
CCCS	Current Controlled Current Source
CCVS	Current Controlled Voltage Source
VCCS	Voltage Controlled Current Source
CTF	Current Transfer Function
VTF	Voltage Transfer Function
VMF	Voltage Mode Filter
CMF	Current Mode Filter
TCF	Transconductance Filter
TRF	Transresistance Filter
BPF	Band Pass Filter
ADC	Analog-to-Digital Converter
VCT	voltage to current transducer
CMFB	Common Mode Feedback
RHP	Right Hand Plane

CHAPTER 1

INTRODUCTION

1.1 Basic electronic amplifiers

An amplifier receives a signal at its input and delivers undistorted large signal at its output. Several applications of amplifiers include wireless communications and broadcasting, and in audio equipment of all kinds [1].

Amplifiers can be classified into four basic categories based on the magnitudes of the input and output impedances in comparison with the source and load impedances respectively. These are [1]:

- ►Voltage controlled voltage source amplifier (VCVS),
- ►Voltage controlled current source amplifier (VCCS),
- ►Current controlled voltage source amplifier (CCVS), and
- ►Current controlled current source amplifier (CCCS).

1.1.1 VCVS

It provides an output voltage proportional to the input voltage. The proportionality factor is independent of the magnitudes of source and load resistance. Figure 1.1 shows the Thevenin's equivalent circuit of VCVS amplifier.

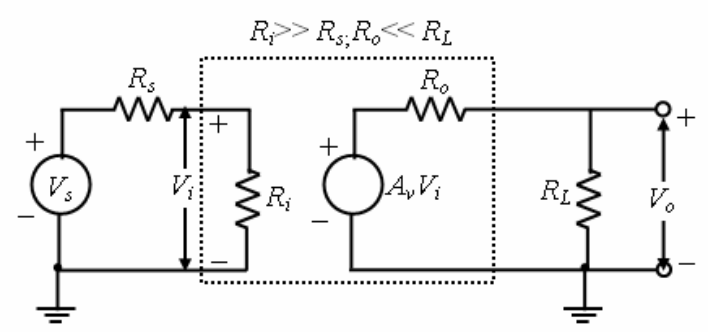

Figure 1.1: Equivalent circuit of VCVS

Here, V_s= source voltage, V_i= amplifier input voltage, V_o= output voltage, R_s= source resistance, R_i= amplifier input resistance, R_o= amplifier output resistance, R_L= external load resistance.

From the input circuit,

$$V_i = \frac{R_i}{R_i + R_s} V_s$$

$$V_i \approx V_s \text{ (if } R_i >> R_s) \tag{1.1}$$

From the output circuit,

$$V_o = \frac{R_L}{R_L + R_o} A_v V_i \tag{1.2}$$

$$V_o \approx A_v V_i \text{ (if } R_o << R_L)$$

$$V_o = A_v V_s \text{ (from equation (1.1))}$$

Hence output voltage is proportional to input voltage.

From equation (1.2),

$$V_o = \frac{R_L}{R_L + R_o} A_v V_i$$

$$V_o = A_v V_i \text{ (with } R_L = \infty)$$

$$A_v = \frac{V_o}{V_i}$$

Hence A_v represents the open-circuit voltage amplification, or voltage gain.

1.1.2 VCCS

It provides an output current proportional to the input voltage. The proportionality factor is independent of the magnitudes of source and load resistance. Figure 1.2 shows a VCCS amplifier, where Thevenin's equivalent circuit is used at input side and Norton's equivalent circuit is used at output side.

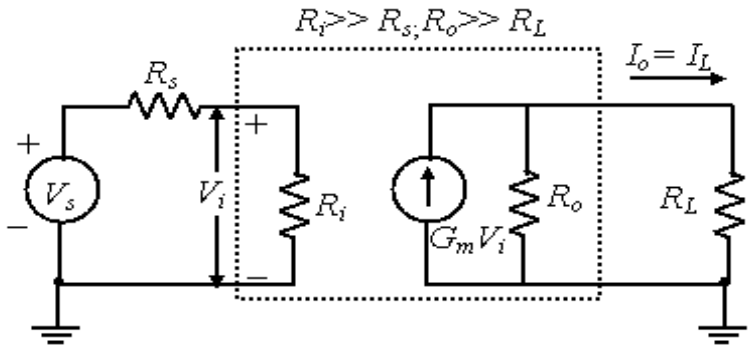

Figure 1.2: Equivalent circuit of VCCS

From the input circuit,

$$V_i = \frac{R_i}{R_i + R_s} V_s$$

$$V_i \approx V_s \text{ (if } R_i >> R_s) \qquad (1.3)$$

From the output circuit,

$$I_o = \frac{R_o}{R_L + R_o} G_m V_i \qquad (1.4)$$

$$I_o \approx G_m V_i \text{ (if } R_o >> R_L)$$

$$I_o = G_m V_s \text{ (from equation (1.3))}$$

Hence output current is proportional to input voltage.

An ideal VCCS amplifier must have infinite input resistance (*i.e.* $R_i = \infty$) and infinite output resistance (*i.e.* $R_o = \infty$). From equation (1.4),

$$I_o = \frac{R_o}{R_L + R_o} A_v V_i$$

$$I_o = G_m V_i \text{ (with } R_L = 0)$$

$$G_m = \frac{I_o}{V_i}$$

Hence G_m represents the short-circuit trans-conductance gain.

1.1.3 CCVS

It provides an output voltage proportional to the input current. The proportionality factor is independent of the magnitudes of the source and load resistance. Figure 1.3 shows a CCVS amplifier where Norton's equivalent circuit is used at input side and Thevenin's equivalent circuit is used at output side.

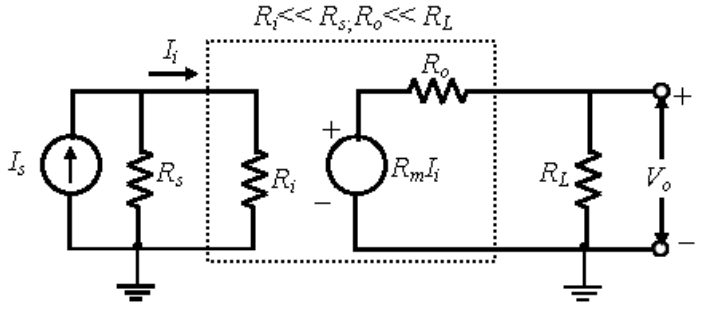

Figure 1.3: Equivalent circuit of CCVS

From the input circuit,

$$I_i = \frac{R_s}{R_i + R_s} I_s$$

$$I_i \approx I_s \text{ (if } R_i << R_s) \tag{1.5}$$

From the output circuit,

$$V_o = \frac{R_L}{R_L + R_o} R_m I_i \tag{1.6}$$

$$V_o \approx R_m I_i \text{ (if } R_o << R_L)$$

$$V_o = R_m I_s \text{ (from equation (1.5))}$$

Hence, output voltage is proportional to input current.

An ideal CCVS amplifier must have zero input resistance (*i.e.* R_i =0) and zero output resistance (*i.e.* R_o = 0). From equation (1.6),

$$V_o = \frac{R_L}{R_L + R_o} R_m I_i$$

$$V_o = R_m I_i \text{ (with } R_L = \infty)$$

$$R_m = \frac{V_o}{I_i}$$

Hence R_m represents the open-circuit trans-resistance gain.

1.1.4 CCCS

It provides an output current proportional to the input current. The proportionality factor is independent of the magnitudes of the source and load resistance. Figure 1.4 shows a Norton's equivalent circuit of a CCCS amplifier.

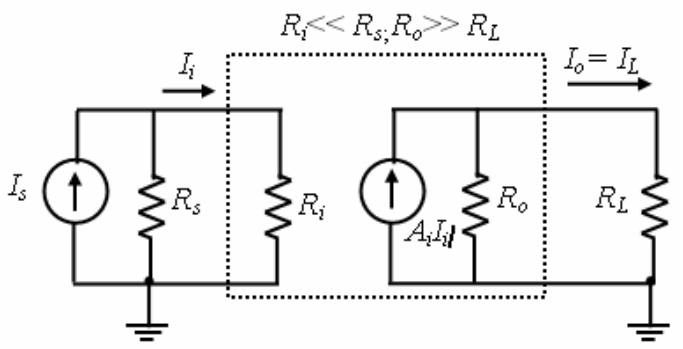

Figure 1.4: Equivalent circuit of CCCS

Here, I_s= source current, I_i= amplifier input current, $I_o = I_L$= output or load current.

From the input circuit,

$$I_i = \frac{R_s}{R_i + R_s} I_s$$

$$I_i \approx I_s \text{ (if } R_i << R_s) \tag{1.7}$$

From the output circuit,

$$I_o = \frac{R_o}{R_L + R_o} A_i I_i \tag{1.8}$$

$$I_o \approx A_i I_i \text{ (if } R_o >> R_L)$$

$$I_o = A_i I_s \text{ (from equation (1.7))}$$

Hence output current is proportional to input current.

An ideal current amplifier must have zero input resistance (*i.e.* R_i =0) and infinite output resistance (*i.e.* $R_o = \infty$). From equation (1.8),

$$I_o = \frac{R_o}{R_L + R_o} A_i I_i$$

$$I_o = A_i I_i \text{ (with } R_L = 0)$$

$$A_i = \frac{I_o}{I_i}$$

Hence A_i represents the short-circuit current gain.

1.2 Practical electronic amplifiers

1.2.1 Operational Amplifier (OP-AMP)

The operational amplifier (OP-AMP) is a fundamental building block in analog integrated circuit design [2-4]. It is a very useful and versatile building block which can provide many nearly ideal signal processing functions such as addition, subtraction, multiplication, integration and so on. Figure 1.5 shows the block diagram of important sub systems of an OP-AMP [5].

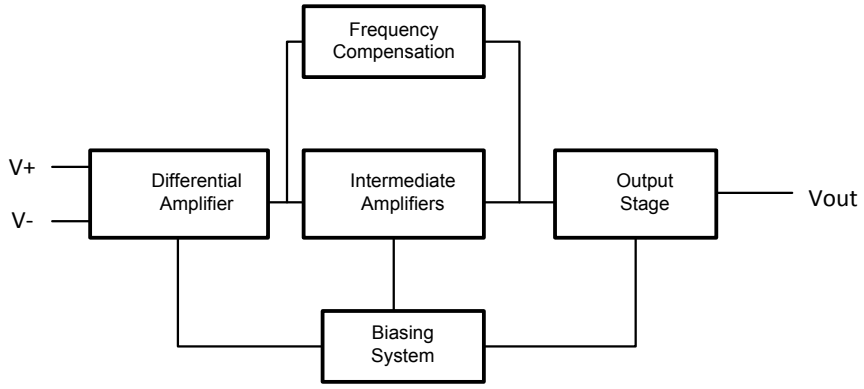

Figure 1.5: Block diagram of an OP-AMP with different sub systems

From the figure, V_+ is the voltage at the non-inverting terminal and V_- is the voltage at the inverting terminal. Ideally the OP-AMP amplifies only the difference in voltage between the two input terminals, which is called the differential input voltage. The output voltage of the OP-AMP is given by the equation,

$$V_{out} = (V_+ - V_-) A_{OL} \tag{1.9}$$

where, A_{OL} is the called as open loop gain of the amplifier. The differential amplifier (DA) is an essential part of OP-AMP. The DA may perform differential to single-ended conversion. DA stage provides most of the open loop gain required of the OP-AMP. High gain at the input may reduce offset and the noise figure. The intermediate stages boost up the gain to expected high level. Intermediate stages may also provide dc level shift so that the nominal dc level at the output of the OP-AMP is nearly equal to zero volt. This facilitates maximum possible swing at the output of the OP-AMP when a signal is applied at the input. The output buffer stage is a power amplifier. If the OP-AMP is required to drive a resistance load or a large capacitive load or a combination of both, the output buffer is used. But if the OP-AMP is required to drive purely capacitive load, the output buffer is not used [5]. With the output buffer, the output resistance of the OP-AMP becomes low which is the characteristic of a voltage source. Hence, the OP-AMP behaves closely like a voltage amplifier (i.e. VCVS). The bias circuit section provides required dc bias current to various sub-systems of the OP-AMP. The compensation sub system provides feedback or feed forward path between different sections of OP-AMP to ensure stability of the OP-AMP in negative feedback connection. Most of the cases, except for building regenerative systems (i.e., oscillatory), an OP-AMP is invariably used with negative feedback between its output and input. Several operational amplifiers are available commercially, such as, LM258, LM358A, LM358, LM2904 (Dual operational amplifier) [28], AU2904 (Low power dual Operational Amplifier), AU2902 (Low power Quad Operational Amplifier) [29] etc.

1.2.2 Operational transconductance amplifier (OTA)

The operational transconductance amplifier (OTA) is basically an operational amplifier (OP-AMP) with no output buffer [5]. Hence an OTA is mainly designed to drive purely capacitive loads. Differential input voltage of OTA produces an output current. Hence it works as a VCCS

[6]. Ideally, the input and output nodes are the high impedance nodes in an OTA. Transconductance (g_m) of an OTA can be controlled by changing the bias voltage or bias current. OTAs can provide single ended output and differential output. Figure 1.6 shows the block diagram of a single ended output OTA [61].

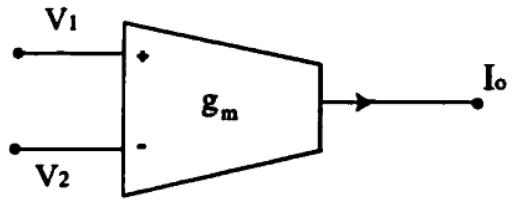

Figure 1.6: Single ended output OTA

The operation of the single ended OTA can be described as the following equation:

$$I_0 = g_m(V_1 - V_2) \tag{1.10}$$

Figure 1.7 shows the block diagram of a differential output OTA.

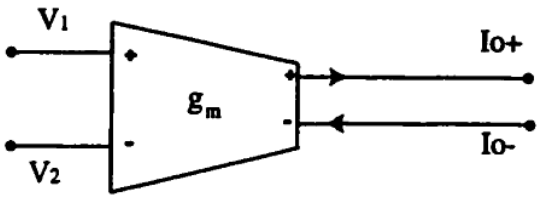

Figure 1.7: Differential output OTA

The operation of the differential output OTA can be described by the following equation:

$$I^{+}{}_0 - I^{-}{}_0 = g_m(V_1 - V_2) \tag{1.11}$$

It is shown from equation (1.11) that, output current which is the difference of two component output currents is proportional to the differential input voltages. Practical OTA may exhibit non-linearity at input differential voltage as low as 20 mV [62]. But in modern devices, such as LM13600, the linearity is maintained up to the differential input level of 80 mV [63].

Now-a-days, OTA has received considerable attention as voltage to current transducer (VCT) due to its versatility and usefulness in many signal processing and filtering applications [7]. Several researchers have contributed toward improvement of the OTA performance in terms of bandwidth [8], linearity, power dissipation [9] and so on. Several commercial OTAs, such as, OPA860 (an OTA and a closed-loop buffer), OPA861 (an OTA), OPA615 (a wide-bandwidth dc restoration circuit that contains an OTA and a switching OTA or SOTA) [10], CA 3080 and LM 13600, LM13700 [11-15] are available for electronic circuits and system design.

1.2.3 Operational Transresistance amplifier (OTRA)

The operational transresistance amplifier (OTRA) has received considerable attention from analog designers due to its applications in current-mode analog integrated circuits [16] – [20]. An OTRA typically can have two low-input-impedance terminals and one low-output-impedance terminal. OTRA is found to have constant bandwidth independent of the gain in most closed-loop configurations [20], whereas a traditional operational amplifier has a bandwidth which is dependent on the closed-loop voltage gain. Figure 1.8 shows the symbol of an OTRA [21].

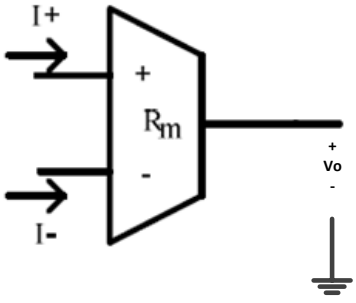

Figure 1.8: Circuit symbol of OTRA

The operation of the OTRA can be described by the following matrix [21]:

$$\begin{bmatrix} V_+ \\ V_- \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_+ \\ I_- \\ I_o \end{bmatrix}$$

Both the input terminals are virtually grounded and the output voltage of the OTRA is the difference of the two input currents multiplied by transresistance R_m. Ideally, the transresistance gain, R_m approaches infinity, hence forcing the input currents to become equal. Several OTRAs are available commercially, such as, ADN2880 (3.2 Gbps, 3.3 V, Low Noise Transimpedance Amplifier) [24], LG1628BXA (Sonet / sdh 2.488 Gbits / s Transimpedance Amplifier) [25], MAX3793 (1Gbps to 4.25Gbps Multi-rate Transimpedance Amplifier with Photocurrent Monitor) [26], OPA380 (Precision, High-Speed Transimpedance Amplifier) [27].

1.2.4 Current Conveyor (CC)

Current Conveyor (CC) is a well-known current signal processing device which was introduced by A. Sedra and K. Smith first [30]. A CC is a four terminal device which can perform several analog signal processing functions when it is arranged in specific circuit configurations with other electronic elements. [31]. Figure 1.9 shows the block diagram of a current conveyor [22].

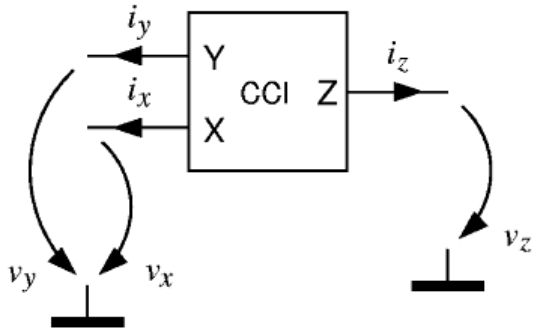

Figure 1.9: Block diagram of a current conveyor (CC)

Current conveyor is capable to convey current between two terminals (X and Z) with very different impedance levels. It has several advantages over traditional OP-AMP, such as CC can provide higher voltage gain over a larger signal bandwidth than corresponding OP-AMP. The operation of a CCI (current conveyor type I) can be represented by the following matrix [22]:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}$$

$$\begin{cases} i_x = i_y = i_z \\ v_x = v_y \end{cases}$$

In case of the second generation current conveyor (CCII), if a voltage is applied at Y terminal, then an equal potential appears on the X terminal. The current in node Y=0. The current I is conveyed to Z terminal such that terminal Z has the characteristics of a current source having value of I, with high output impedance. Voltage of X terminal is set by that of Y terminal and is independent of the current that is being forced into terminal X. Terminal Y exhibits infinite input impedance. The operation of a CCII can be represented by the following matrix [22]:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}$$

$$\begin{cases} i_y = 0 \\ v_x = v_y \\ i_z = \pm i_x \end{cases}$$

1.3 Motivation

Current-mode signal processing has become popular because of its potentials for low-voltage, wide-band operations. Several researchers have reported new active devices, such as current-coveyor, current operational amplifier, and so on with potential applications toward implementation of current-mode filters. Recently, Raut and Swamy have reported that by the applications of the concepts of (i) network transposition, and (ii) nullor equivalence of ideal active devices, an operational amplifier (as a VCVS) can be used to realize both voltage-mode and current-mode filters [37]. Since any ideal active device is equivalent to a nullor [23], both voltage-mode and current-mode filters could be realized by any of the four ideal controlled source representations of an active device, i.e., VCVS, CCCS (current-controlled current-source), VCCS (voltage-controlled current-source), and CCVS (current-controlled voltage source). However, different practical active devices will approach the respective ideal operation characteristic differently, the voltage- or current-mode signal processing quality is likely to differ depending upon which active device is being employed.

It is therefore, felt necessary to implement all the four categories of amplifiers using a modern integrated circuit (IC) technological process and test the quality of signal processing, such as analog filtering, by using each such amplifier. The work in this thesis has been undertaken with this motivation. For the current work we have chosen CMOS technology. The CMOS technology was chosen because of accessibilty and compatibility with main stream digital VLSI circuits. Thus, the thesis presents the implementation of a Universal Amplifier Module (UAM) which can function as any of the four (i.e., VCVS, VCCS, CCVS and CCCS) active devices . The UAM has then been used to realize several second order filtering functions and a comparison of the relative performances has been reported.

1.4 Organization of thesis

With the background as above, the rest of the thesis is organized as follows:

Chapter 2 presents different sub-systems of the proposed Universal Amplifier Module (UAM) with specific reference to their operations, e.g. bias sources, input differential amplifier (DA), level shifting stages, output voltage buffer stage, output current buffer stage and so on. Configuration of the UAM for either voltage-mode or current-mode operation is also presented.

Chapter 3 presents simulation set-ups and results pertaining to the operations of the UAM as the four categories of amplifiers. Different performance parameters are measured by SPICE simulations. The simulations are performed at the schematic level followed by post layout simulations. The layout has been implemented using 0.18 μm CMOS (CMOSP18/TSMC) process.

Chapter 4 presents several signal processing cases with the UAM as active device building block. Some traditional amplifier circuits are implemented using the UAM, such as, inverting amplifier, non-inverting amplifier, ideal integrator, lossy integrator etc. Further, several voltage mode 2^{nd} order band pass filters and current mode filters using the principles of transposed network with the UAM as the active device are illustrated.

Chapter 5 summarizes contributions of this thesis and gives some recommendations for future work related to the Universal Amplifier Module (UAM).

CHAPTER 2

ANALYSIS AND DESIGN OF THE UNIVERSAL AMPLIFIER MODULE (UAM)

2.1 Introduction

This chapter presents the different sub-systems of the proposed Universal Amplifier Module (UAM) with specific reference to their operations, e.g. bias sources, input differential amplifier (DA), intermediate stages, output voltage buffer stage, output current buffer stage and so on. Configuration of the UAM for either voltage-mode or current-mode operations is also presented. A block diagram of the system is shown in figure 2.1.The operations of the various blocks are described below.

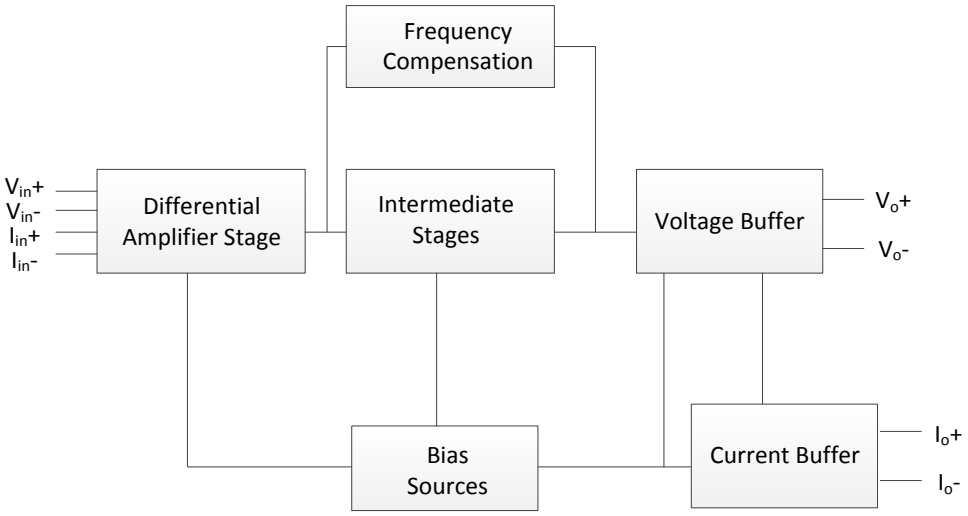

Figure 2.1: Block Diagram of the Universal Amplifier Module (UAM)

2.2 Bias sources

The UAM operates with ±1.3 V DC supply. A simple voltage divider circuit is used to provide different bias voltage levels to the UAM. Figure 2.2 shows the schematic diagram of the bias circuit comprised of transistors M0, M1, M2 & M3. Two bias voltage levels, V_a = 691 mV and V_c = -765 mV required in the UAM are produced by this arrangement.

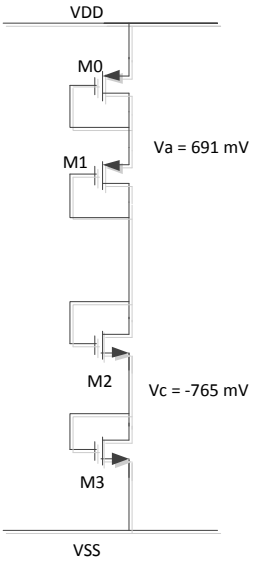

Figure 2.2: Schematic diagram of the bias sources

All transistors are gate – drain connected and operated in saturation region. Using the standard square law formula, drain current for PMOS in saturation region can be written as [64]:

$$I_{SDP} = \frac{1}{2}\mu_p C_{ox}\frac{W_p}{L_p}(V_{SGP} - |V_{tp}|)^2 \quad (2.1)$$

Drain current for NMOS in saturation region can be written as:

$$I_{DSN} = \frac{1}{2}\mu_N C_{ox}\frac{W_N}{L_N}(V_{GSN} - V_{tn})^2 \quad (2.2)$$

Where μ_N and μ_P are the mobility & V_{tn} and V_{tp} are the threshold voltages of NOMS and PMOS transistors respectively. Putting the values of mobility; threshold voltage; C_{ox} (from APPENDIX – F) and bias current $I_D = I_N = 15$ µA in equations (2.1) & (2.2) and choosing $W_p = 20$ µm, $W_n = 10$ µm, $L_n = L_p = 1.2$ µm so that, $V_a = 691$ mV and $V_c = -765$ mV are generated.

2.3 Differential input stages

Figures 2.3(a) & (b) show respectively the schematic diagram of the input differential amplifier (DA) stage of the UAM and its small signal equivalent. Transistors M4, M5, M6, M7 & M12 are included in the DA stage. The circuit is designed for bias current level (approximately) of $I_{DM12} = 70$ µA, so that each branch have bias current level of $I_{DM5} = I_{DM4} = 35$ µA. Now to obtain this level in each branch and solving for $I_{DM5} = I_{DM7}$ (or $I_{DM4} = I_{DM6}$) using the standard square law equation, the transistor size can be chosen as $W_{M12} = 95$ µm, $L_{M12} = 1.2$ µm; $W_{M4} = W_{M5} = 40$ µm, $L_{M4} = L_{M5} = 1.2$ µm and $W_{M6} = W_{M7} = 23.4$ µm, $L_{M6} = L_{M7} = 1.2$ µm. As the module operates both in voltage and current mode, there are provisions for both voltage and current signal inputs. Necessary bias voltage levels are taken from the voltage divider circuit as in figure 2.2.

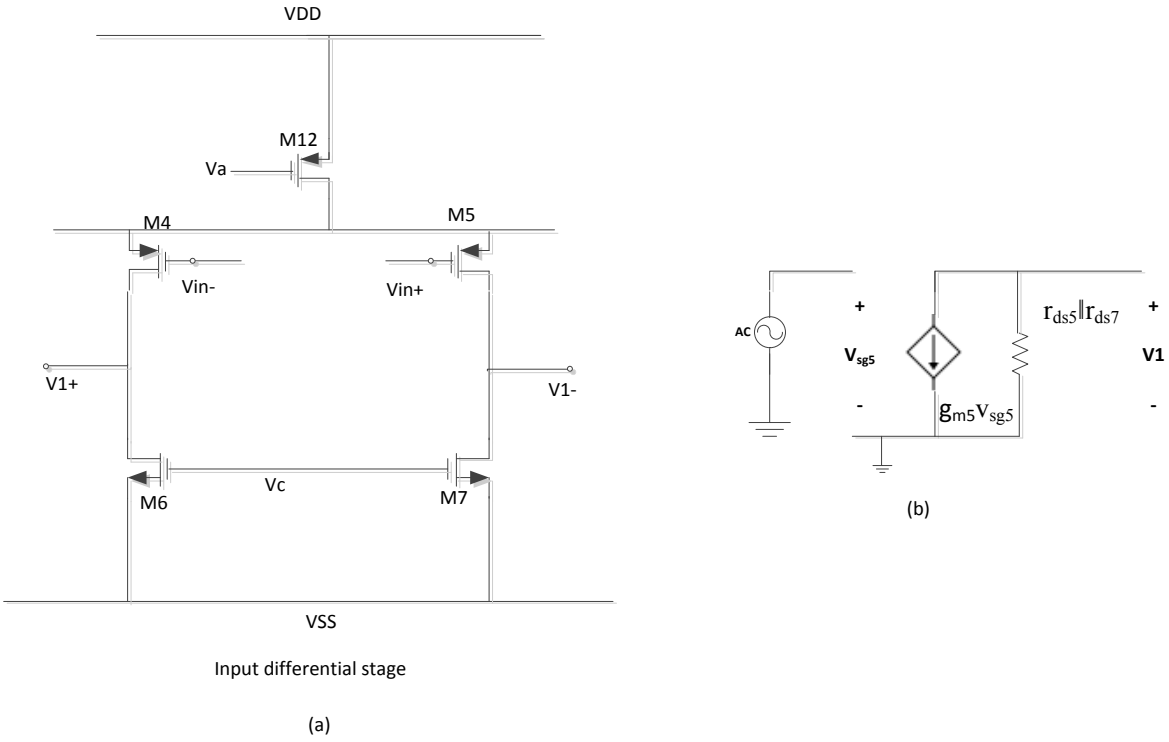

Figure 2.3: (a) Schematic diagram of differential input stage (b) Small signal equivalent model of DA stage

Small signal voltage gain of the differential amplifier stage is,

$$\frac{v_1}{v_{in}} = -g_{m5}\,(r_{ds5} \| r_{ds7}) \qquad (2.3)$$

Using the proper transconductance and resistance values from APPENDIX – F, gain ≈ 56.

Input signal voltage is applied to conventional PMOS differential pairs. For applying current input with the existing configuration for voltage, two complementary gate – drain connected MOS are inserted, output of which is connected with the voltage input leads. Resistance of the gate – drain connected MOS stage is low enough (~200Ω in this case) to apply current input at this node. Current input stage is separated from the voltage input stage by a NMOS switch (S1, S2 in figure 2.4). Hence either voltage or current input stage is selected based on the intended mode of operation, i.e. voltage input stage is selected in case of voltage mode operation and current input

stage is selected in case of current mode operation. Figure 2.4 shows the complete schematic diagram of the input stage for applying current signal.

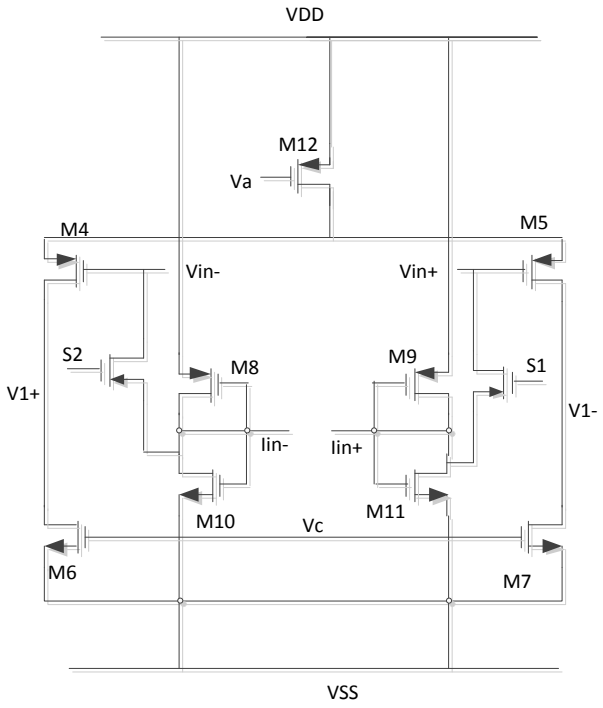

Figure 2.4: Schematic diagram of the input stage of the UAM

2.4 Intermediate stages

Two more stages are added with the differential input stages for boosting up the gains i.e. voltage gain, current gain, transconductance and transresistance gain. These comprise of transistors M13, M15, M17 & M23. Intermediate stages also shift the dc voltage level so that nominal output DC level is nearly equal to zero volts. Simple common-source amplifier configuration is used as gain boosting stages with PMOS loads. Figures 2.5(a) & (b) show respectively the schematic diagram of the intermediate stages and small signal equivalent model. Bias current level of the M13, M15 column of transistors is, $I_{DM13} = I_{DM15} = 56$ µA and output DC level at the drain of M13 (& M15) ≈ -740 mV. Now using the standard square law equation and solving for $I_{PM13} = I_{NM15}$ provides, $W_{PM13} = 70$ µm, $L_{M13} = 1.2$ µm and $W_{NM15} = 11.88$ µm, $L_{NM15} = 1.2$ µm.

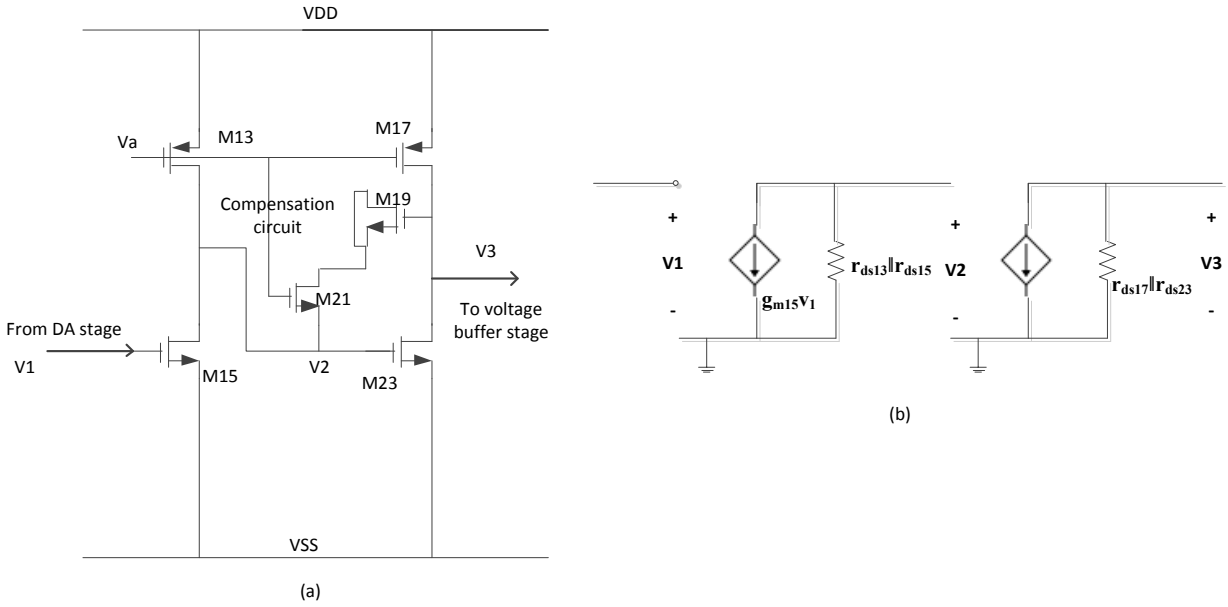

Figure 2.5: (a) Schematic diagram of intermediate stages; (b) Small signal equivalent model

From figure 2.5 (b), small signal gain of the M13, M15 column of transistors can be written as [64],

$$\frac{v_2}{v_1} = -g_{m15}\,(r_{ds13} \| r_{ds15}) \tag{2.4}$$

Similarly small signal gain of the M17, M23 column of transistors can be written as:

$$\frac{v_3}{v_2} = -g_{m23}\,(r_{ds17} \| r_{ds23}) \tag{2.5}$$

Putting the values of appropriate transconductances and resistances (APPENDIX – F) in equations (2.4) and (2.5), gains of these stages become $\frac{V_2}{V_1} \approx 125.11$, and $\frac{V_3}{V_2} \approx 149$ respectively.

2.5 Frequency compensation

A technique using Miller's theorem is used for frequency compensation of this system. Inserting the compensating capacitance, C_c between two gain stages provides the compensated poles at, $P_1 \approx$ -503.8 KHz. Pole frequency is obtained by performing HSPICE simulation using appropriate command (.PZ V(3) Vin; [65]). Formula for the first pole can be expressed as [2]:

$$P_1 = \frac{-1}{g_{mII} R_{II} R_I C_C} \tag{2.6}$$

where, g_{mII} = conductance of M23 = g_{mM23};

R_{II} = equivalent resistance of transistors M17 and M23 = $r_{ds17} \| r_{ds23}$;

R_I = equivalent resistance of transistors M13 and M15 = $r_{ds13} \| r_{ds15}$

and C_c = Compensating capacitance

Putting the value of these parameters from APPENDIX-F, value of the compensating capacitor, C_c can be calculated from equation (2.6) as, C_c = 71.65 fF. A source – drain connected MOS (transistor M19) having W = 13 μm, L = 1.2 μm can be used to produce a capacitor of this value. Fig. 2.5 shows the components for pole and zero compensation between two gain boosting intermediate stages.

As the RHP zero results from the feed forward path through the compensation capacitor, it tends to limit the gain-bandwidth of the system. Hence to eliminate the effect of RHP zero, a nulling resistor, R_z is inserted in series with C_c resulting the compensating zero at [2]:

$$z_1 = \frac{1}{C_C(\frac{1}{g_{m23}} - R_Z)}$$

Considering $z_1 = p_2 = \frac{-g_{mM23}}{C_{II}}$, R_z can be calculated as [2],

$$R_z = \frac{C_C + C_{II}}{C_C} . \frac{1}{g_{mM23}} \quad (2.7)$$

Using C_c = 71.65 fF and value of C_{II} & g_{mM23} (from APPENDIX – F), value of R_z can be calculated rom equation (2.7) as, R_z = 53.11 KΩ. An NMOS (transistor M21) is designed having W = 1 μm, L = 2.25 μm to operate in resistive mode that provides the value of R_z.

2.6 Voltage buffer stage

The final stage in the voltage amplifier system is the common drain buffer stage. Figures 2.6 (a) & (b) show respectively the schematic diagram of the voltage buffer stage of the UAM and its small signal equivalent model. This stage comprises of transistors M25, M27 & M29. The purpose of this stage is to drive resistive load or large capacitive load (or a combination of both) [5]. Voltage buffer stage can provide voltage gain with voltage signal input applied at the input stage for voltage and transresistance gain with current signal input applied at input stage for current.

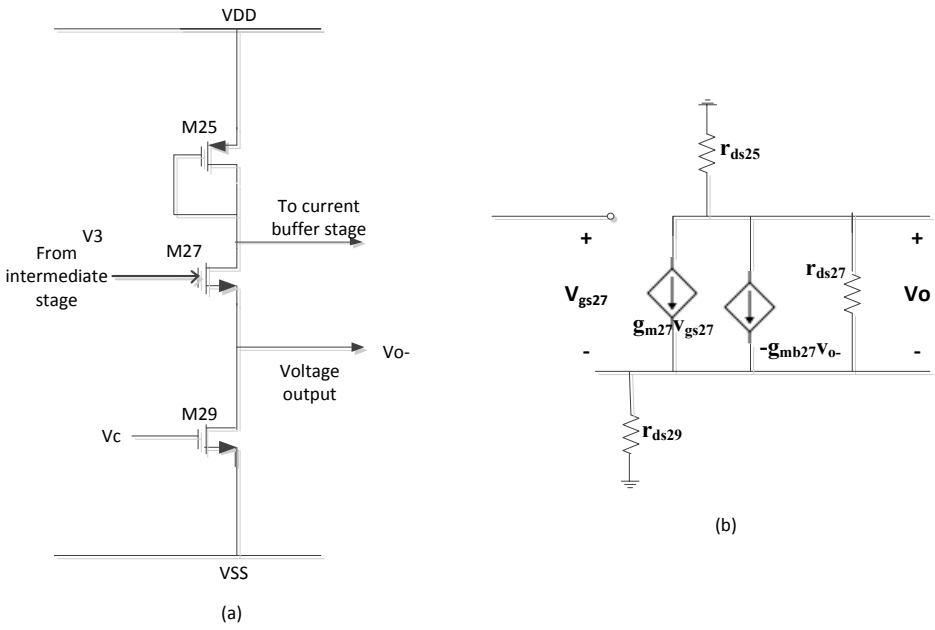

Figure 2.6: (a) Schematic diagram of the voltage buffer stage; (b) Small signal model of the voltage buffer

From figure 2.6 (b), small signal gain of the voltage buffer stage can be written as [64]:

$$\frac{v_o}{v_3} = \frac{g_{m27}R'}{1+(g_{m27}+g_{mb27})R'} \tag{2.8}$$

$$\text{Where, } R' = (r_{ds27}+r_{ds25}) \| r_{ds29} \| \frac{1}{g_{mb27}}$$

Using the appropriate values of parameters from APPENDIX – F, $\frac{v_o}{v_3} = 0.73$

2.7 Current buffer stage

A wideband CMOS transconductor [32] is used as the current buffer stage of the UAM. The purpose of this stage is to provide satisfactory transconductance gain with voltage signal input as well as current gain with current signal input over a wide bandwidth range. Figure 2.7 shows the schematic diagram of the current buffer stage of the UAM comprising transistors M31 – M38.

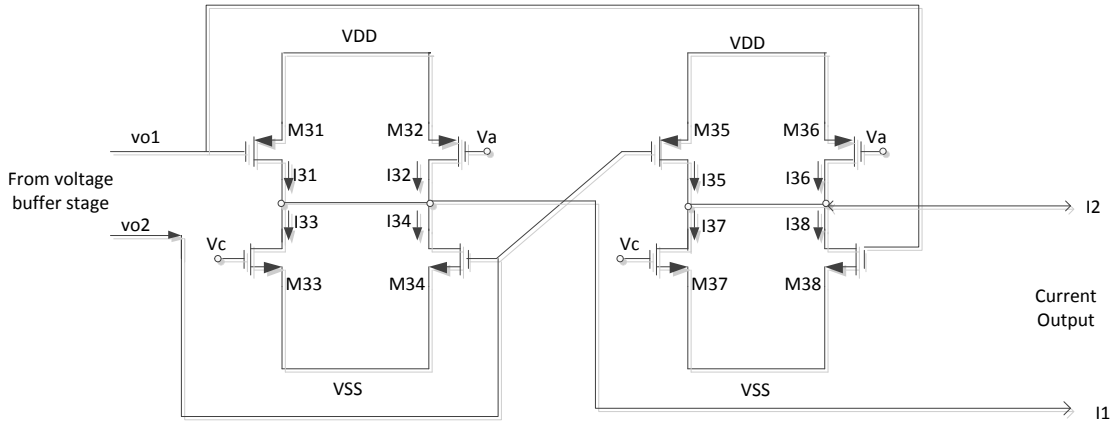

Figure 2.7: Schematic diagram of the current buffer stage of the UAM

From figure 2.7, using the standard square-law model for the transistors in saturation region, we can write the KCL,

$$I_1 = I_{31} + I_{32} - I_{33} - I_{34} \tag{2.9a}$$

$$\text{and } I_2 = I_{35} + I_{36} - I_{37} - I_{38} \tag{2.9b}$$

Hence, the differential output current,

$$I_{out} = I_2 - I_1$$

$$I_{out} = V_{in}\,[2\beta_{31}(V_{DD} - |V_{TP}|) + 2\beta_{34}(V_{SS} + V_{TN})]$$

where, $\beta_{31} = \frac{\mu_p C_{ox}}{2}\frac{W_{31}}{L_{31}}$, $\beta_{34} = \frac{\mu_p C_{ox}}{2}\frac{W_{34}}{L_{34}}$; $|V_{TP}|$ and V_{TN} threshold voltages for PMOS and NMOS respectively. v_{in} is the differential input voltage, i.e. $v_{in} = v_{o1} - v_{o2}$. Here M31-M35, M32-M36, M33-M37 and M34-M38 are considered as matched pairs.

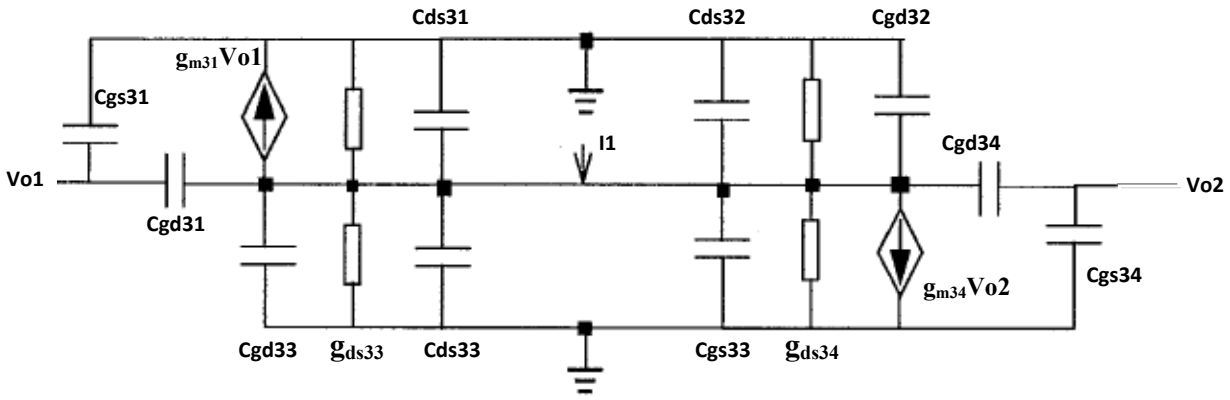

Figure 2.8: Small signal equivalent model of the transconductor

Figure 2.8 shows the small signal equivalent model of the transconductor as shown in figure 2.7. From the figure, equation of output AC current can be written as:

$$-i_1 = g_{m31}v_{o1} + g_{m34}v_{o2} - sC_{gd31}v_{o1} - sC_{gd34}v_{o2} \quad (2.10a)$$

Similarly for the other half circuit,

$$-i_2 = g_{m35}v_{o2} + g_{m38}v_{o1} - sC_{gd35}v_{o2} - sC_{gd38}v_{o1} \quad (2.10b)$$

Differential small signal output current can be calculated as [66],

$$i_{out} = i_2 - i_1$$

$$i_{out} = 2(g_{m38} - g_{m31})\, v_{o1} \quad (2.11)$$

Hence, by putting the transconductance values of M38 & M31 (from APPENDIX – F) and value of v_{o1} from the voltage buffer stage, output AC current can be calculated from equation (2.11) as, i_{out} = - 4.54 A.

2.8 The Universal Amplifier Module (UAM)

Combining all the sub systems i.e. the input differential stages, intermediate stages, compensation circuit, voltage buffer stage and current buffer stage provide the complete schematic diagram of the proposed universal amplifier module (UAM). The complete schematic diagram of the UAM is shown in figure 2.9.

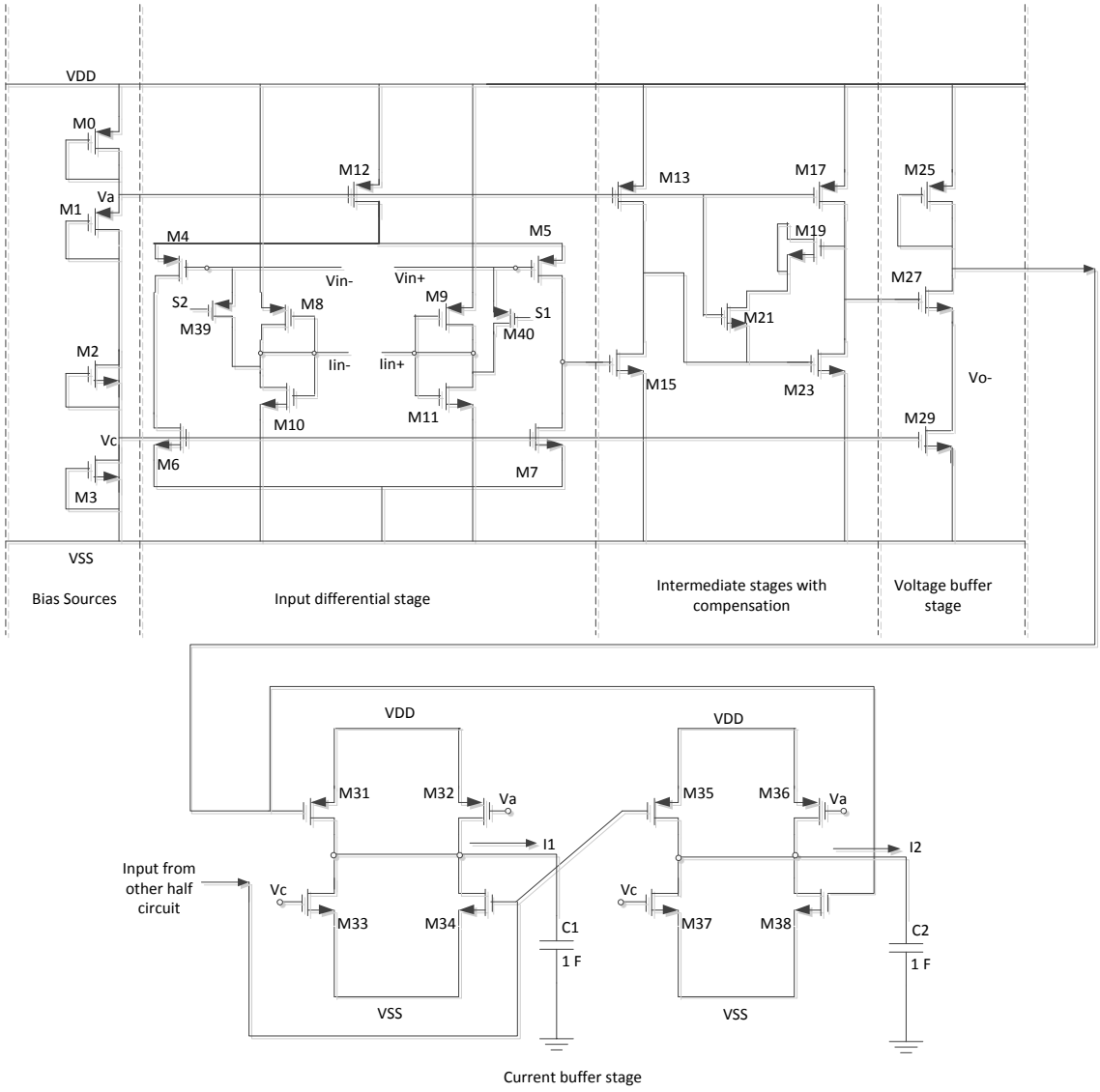

Figure 2.9: Schematic diagram of the half circuit of the universal amplifier module (UAM)

The proposed Universal Amplifier Module (UAM) takes both voltage and current signal input and provides both voltage and current signal output, hence providing all types of voltage and current mode operations i.e., the UAM is capable of providing VCVS, VCCS, CCVS and CCCS operations. Hence the module is named as the universal module.

2.9 Voltage and current – mode operations of the UAM

In this section the operations of the UAM as VCVS, VCCS, CCVS and CCCS are described with some basic formulas and appropriate small signal equivalent circuit models.

2.9.1 Implementation of VCVS using the UAM

Figure 2.10 shows the VCVS implementation of the UAM. 1 V AC is applied across the input differential PMOS transistors. Voltage signal output is taken from the voltage buffer stage. Figure 2.11 shows the small signal equivalent model of the VCVS.

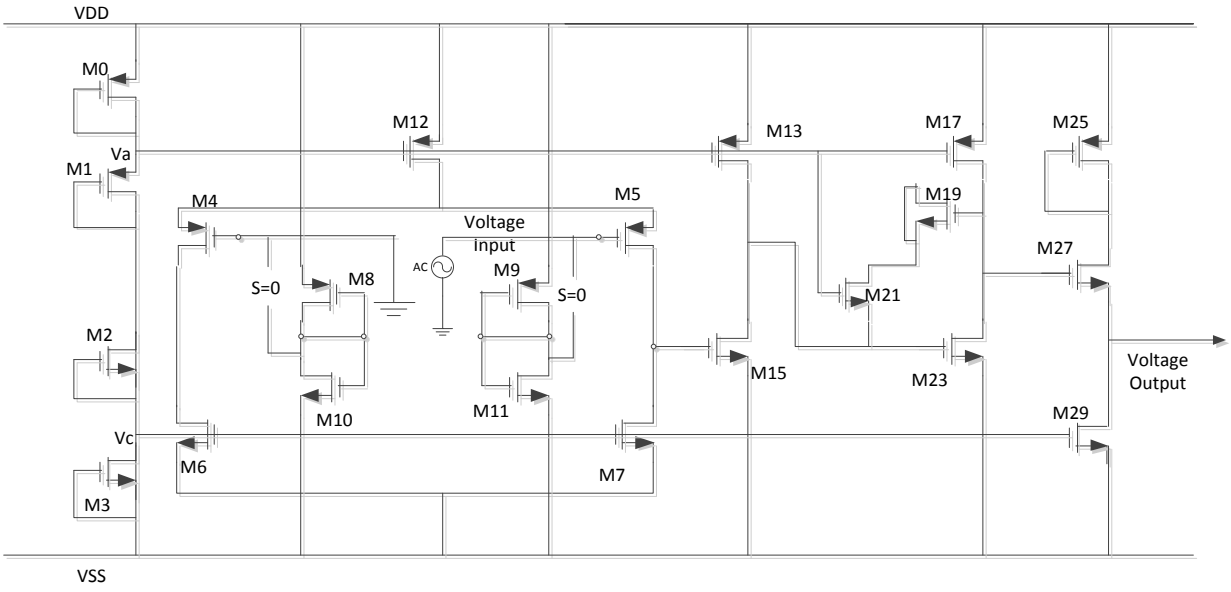

Figure 2.10: Schematic diagram of the half circuit of VCVS implementation of the UAM

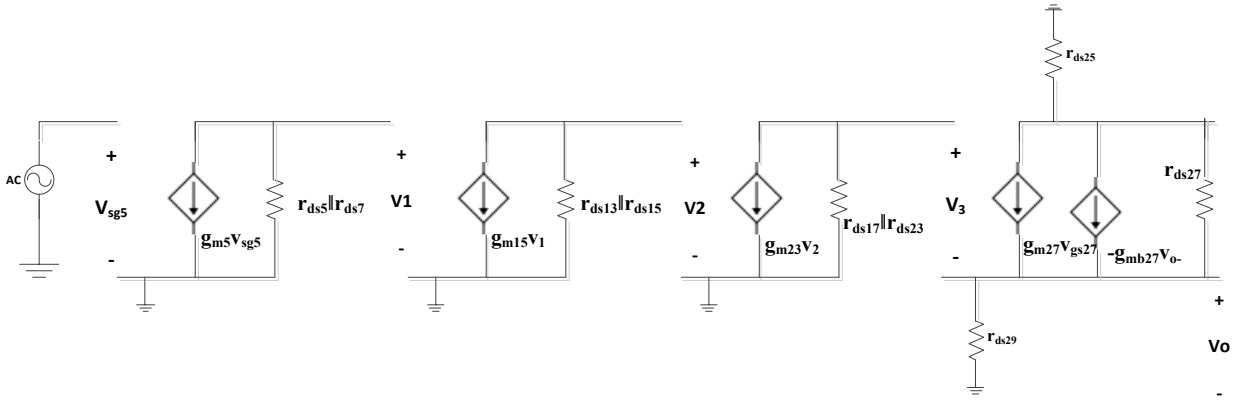

Figure 2.11: Small signal equivalent circuit of the UAM configured as VCVS

From figure 2.11, overall AC gain can be written as:

$$A_v = \frac{v_o}{v_{in}}$$

$$= \frac{v_o}{v_3} \cdot \frac{v_3}{v_2} \cdot \frac{v_2}{v_1} \cdot \frac{v_1}{v_{in}} \qquad (2.12)$$

Now putting the values from equations (2.3), (2.4), (2.5) & (2.8) into equation (2.12),

$$Av = [-g_{m5}\ (r_{ds5} \| r_{ds7})].[-g_{m15}\ (r_{ds13} \| r_{ds15})].[-g_{m23}\ (r_{ds17} \| r_{ds23})].[\ \frac{g_{m27}R'}{1+(g_{m27}+g_{mb27})R'}\ ] \qquad (2.13)$$

Hence, using the appropriate conductance and resistance values from APPENDIX – F, value of overall gain of the VCVS can be calculated from equation (2.13) as, $A_v = 794.33\ K \approx 118\ dB$.

2.9.2 Implementation of CCVS using the UAM

Gate – drain connected stage is added at the input of the same existing VCVS circuit to apply current so that there is a small impedance node at the input. Figure 2.12 shows the schematic diagram of the UAM that works as CCVS (i.e. a trans-resistance device).

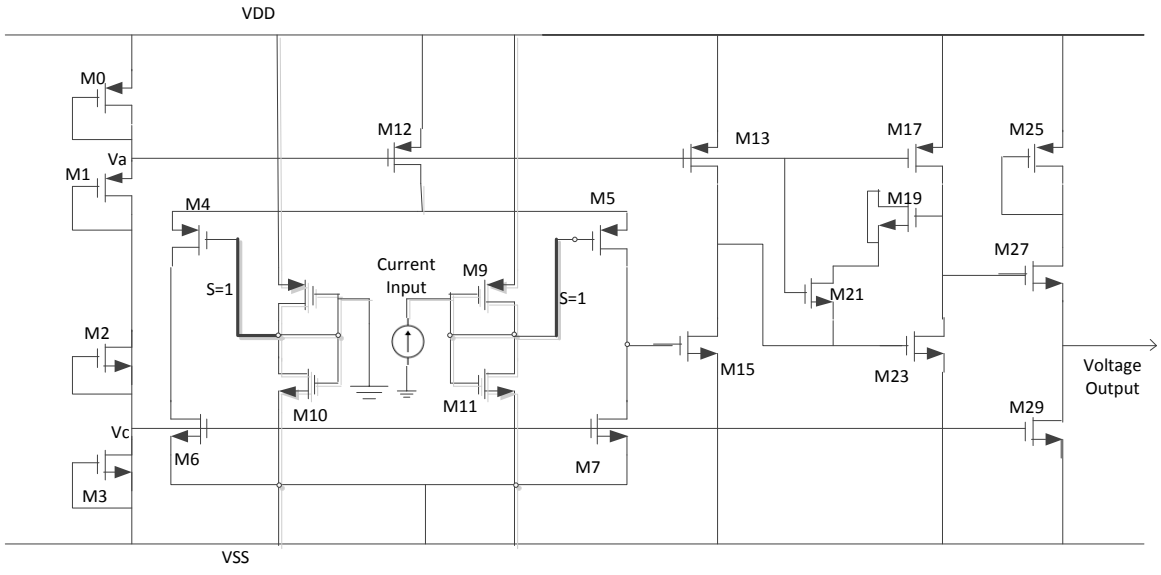

Figure 2.12 Schematic diagram of CCVS implementation of the UAM

Similar small signal equivalent model can be drawn to express the transresistance gain. As, a gate – drain connected stage is added with the existing configuration of VCVS, hence there will

be an additional resistance at the input stage parallel with the input current source. Figure 2.13 shows the small signal equivalent half – circuit of the CCVS system.

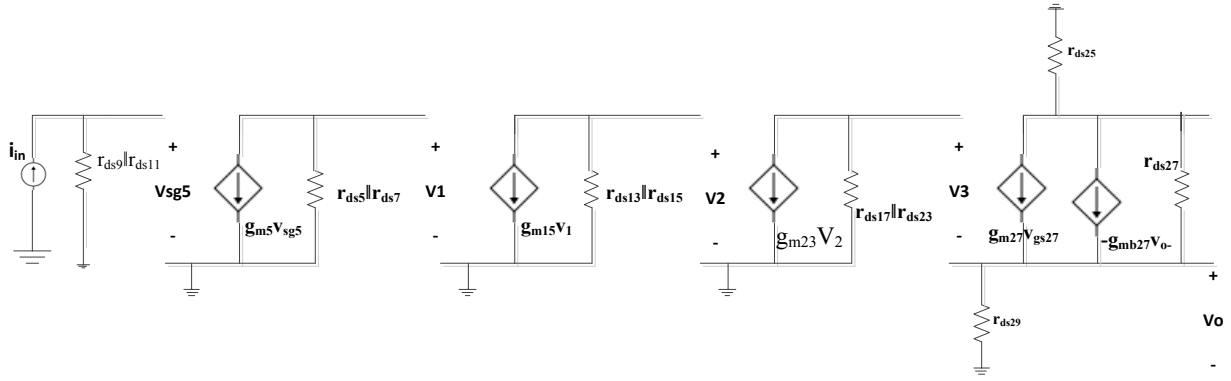

Figure 2.13: Small signal equivalent circuit of CCVS configuration

From figure 2.13, small signal voltage gain of stage 1 is,

$$\frac{v_1}{v_{sg5}} = -g_{m5}\,(r_{ds5} \| r_{ds7}) \tag{2.14}$$

Now overall voltage gain can be calculated as:

$$A_v = \frac{v_o}{v_{sg5}} = \frac{v_o}{v_3} \cdot \frac{v_3}{v_2} \cdot \frac{v_2}{v_1} \cdot \frac{v_1}{v_{sg5}} \tag{2.15}$$

Now v_{gs5} can be written as,

$$v_{sg5} = (r_{ds5} \| r_{ds7})\, i_{in}$$

Putting the value of v_{sg5} into equation (2.15),

$$\frac{v_o}{(r_{ds5} \| r_{ds7})\, i_{in}} = \frac{v_o}{v_3} \cdot \frac{v_3}{v_2} \cdot \frac{v_2}{v_1} \cdot \frac{v_1}{v_{sg5}}$$

Hence, the overall transresistance gain of the CCVS will be,

$$R_m = \frac{v_o}{i_{in}} = \frac{v_o}{v_3} \cdot \frac{v_3}{v_2} \cdot \frac{v_2}{v_1} \cdot \frac{v_1}{v_{sg5}} \, (r_{ds5} \| r_{ds7}) \qquad (2.16)$$

Plugging the values from equations (2.4), (2.5), (2.8) & (2.14) into equation (2.16),

$$R_m = [-g_{m5} \, (r_{ds5} \| r_{ds7})][-g_{m15} \, (r_{ds13} \| r_{ds15})][-g_{m23} \, (r_{ds17} \| r_{ds23})] . \frac{g_{m27} R'}{1 + (g_{m27} + g_{mb27}) R'} (r_{ds5} \| r_{ds7}) \qquad (2.17)$$

Hence, using the values of g_m and r_{ds} of the appropriate transistors from APPENDIX – F, value of overall transresistance gain of the CCVS can be calculated from equation (2.17) as, R_m = 179.27 MΩ ≈ 165.07 dBΩ.

2.9.3 Implementation of VCCS using the UAM

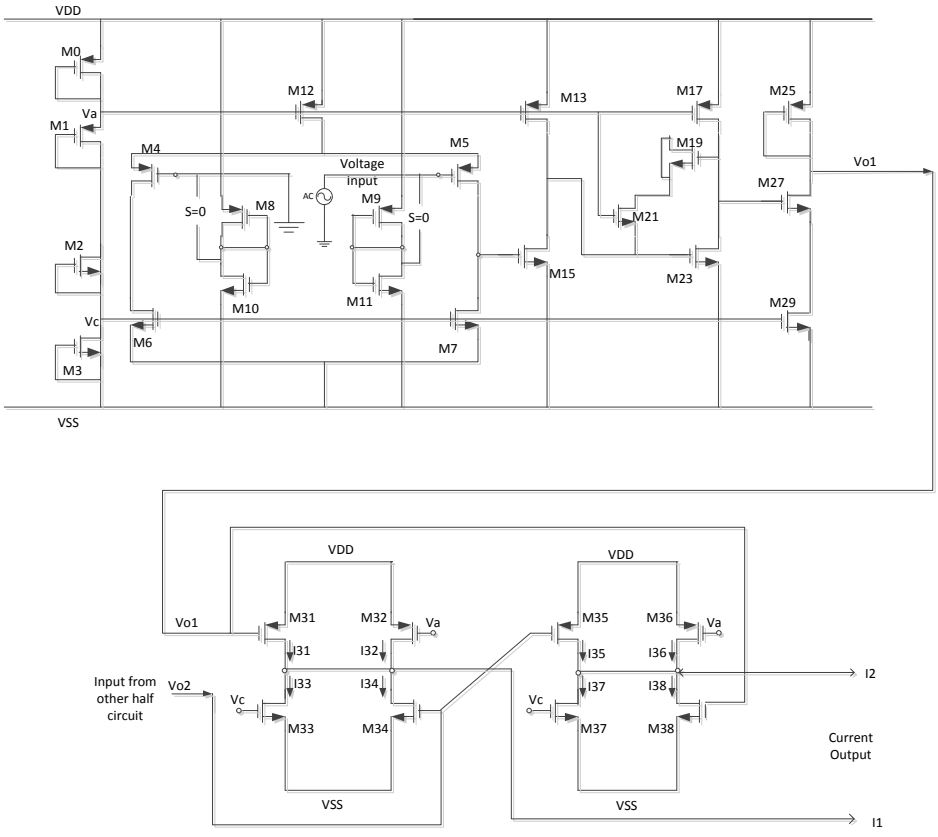

Figure 2.14: Schematic diagram of VCCS implementation of the UAM

Figure 2.14 shows the diagram of the VCCS implementation of the proposed Universal Amplifier Module (UAM). Voltages, v_{o1} & v_{o2} from the output voltage buffer stage of two differential half circuits are fed to the transconductor. The transconductor converts the difference of the voltages (i.e. $v_{o1} - v_{o2}$) into equivalent current.

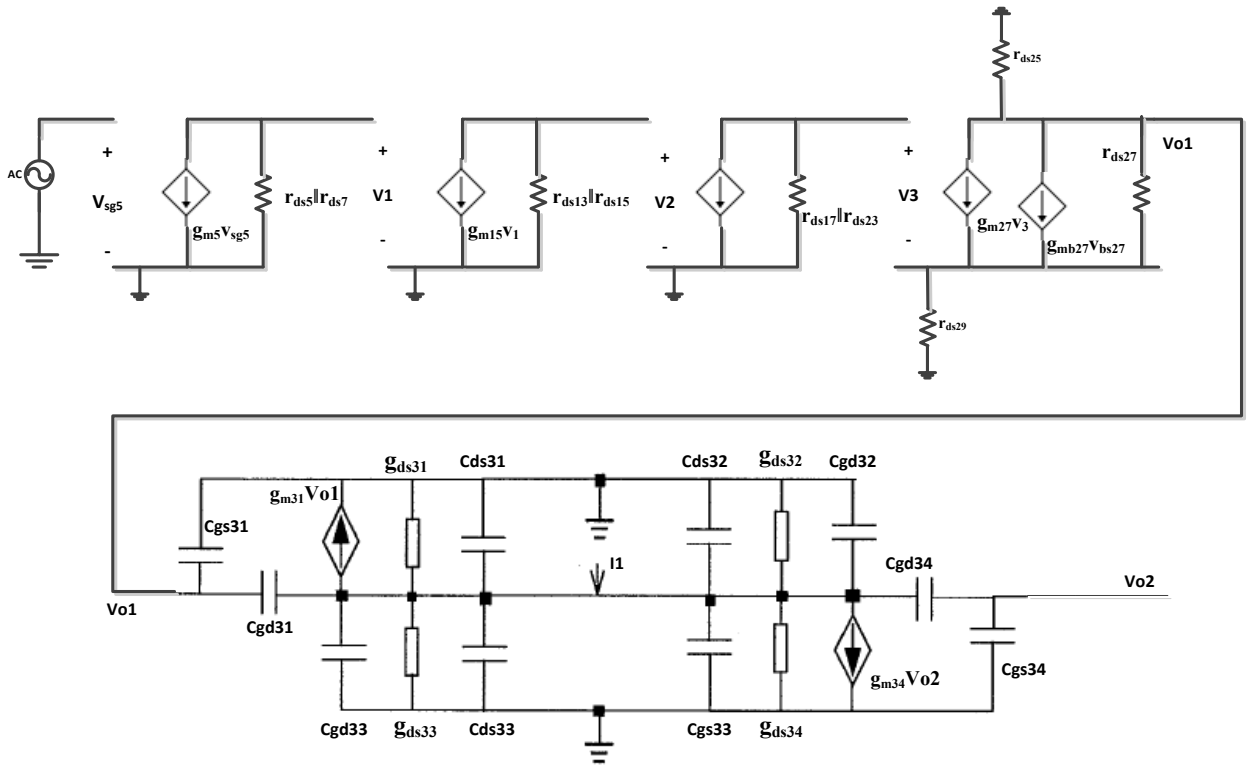

Figure 2.15: Small signal equivalent model of the half circuit of VCCS

Figure 2.15 shows the small signal equivalent model of the half circuit of the VCCS. From the figure, v_{o1} is taken from the drain terminal of M27, hence working as a common-source amplifier with source degeneration. In this case, Small signal gain of this stage is [64],

$$\frac{v_{o1}}{v_3} = - \frac{g_{m27} r_{ds25}}{1 + (g_{m27} + g_{mb27}) r_{ds29}} \tag{2.18}$$

Hence overall gain can be calculated as,

$$\frac{v_{o1}}{v_{in}} = \frac{v_{o1}}{v_3} \cdot \frac{v_3}{v_2} \cdot \frac{v_2}{v_1} \cdot \frac{v_1}{v_{in}} \tag{2.19}$$

Using the values from equation (2.3), (2.4), (2.5) & (2.18) and putting into equation (2.19),

$$\frac{v_{o1}}{v_{in}} = [-\frac{g_{m27} r_{ds25}}{1 + (g_{m27} + g_{mb27}) r_{ds29}}] [-g_{m23} (r_{ds17} \| r_{ds23})].[-g_{m15} (r_{ds13} \| r_{ds15})].[-g_{m5} (r_{ds5} \| r_{ds7})]$$

$$\text{Hence, } v_{o1} = [-\frac{g_{m27} r_{ds25}}{1 + (g_{m27} + g_{mb27}) r_{ds29}}] [-g_{m23} (r_{ds17} \| r_{ds23})].[-g_{m15} (r_{ds13} \| r_{ds15})].$$

$$[-g_{m5} (r_{ds5} \| r_{ds7})] \, v_{in} \tag{2.20}$$

Now from equation (2.11) output AC current is already calculated as:

$$i_{out} = 2(g_{m38} - g_{m31}) \, v_{o1}$$

Putting the value of v_{o1} from equation (2.20),

$$i_{out} = 2(g_{m38} - g_{m31}) \, [-\frac{g_{m27} r_{ds25}}{1 + (g_{m27} + g_{mb27}) r_{ds29}}] .[-g_{m23} (r_{ds17} \| r_{ds23})].$$

$$[-g_{m15} (r_{ds13} \| r_{ds15})].[-g_{m5} (r_{ds5} \| r_{ds7})] \, v_{in}$$

Hence, the overall transconductance gain of the VCCS is,

$$G_m = \frac{i_{out}}{v_{in}} = 2(g_{m38} - g_{m31})[-\frac{g_{m27} r_{ds25}}{1 + (g_{m27} + g_{mb27}) r_{ds29}}] .[-g_{m23} (r_{ds17} \| r_{ds23})].$$

$$[-g_{m15} (r_{ds13} \| r_{ds15})].[-g_{m5} (r_{ds5} \| r_{ds7})] \tag{2.21}$$

So using the appropriate transconductance and resistance values from APPENDIX – F, overall transconductance gain of the CCVS can be calculated from equation (2.21). The value in case of the UAM is, $G_m = 2.296$ A/V ≈ 7.22 dBA/V.

2.9.4 Implementation of CCCS using the UAM

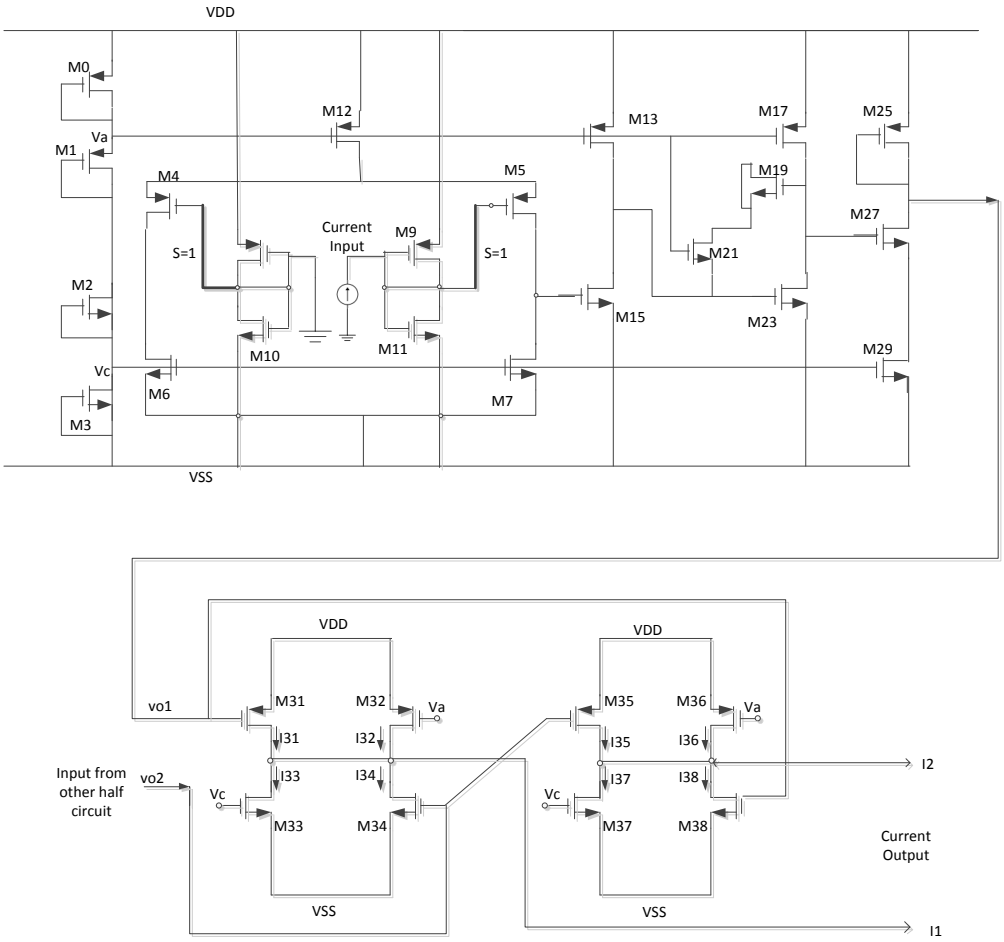

Figure 2.16: Schematic diagram of CCCS implementation of the UAM

Figure 2.16 shows the diagram of the CCCS implementation of the proposed Universal Amplifier Module (UAM). Signal current is applied at the gate – drain connected input stage. This current produces a voltage v_{o1} & v_{o2} at the output voltage buffer stage of two differential half circuits. v_{o1} & v_{o2} are fed to the transconductor which produces current at the current buffer

stage. Similar small signal equivalent model can be drawn for the CCCS circuit. Figure 2.17 shows the half circuit of the AC equivalent model of the circuit as in figure 2.16.

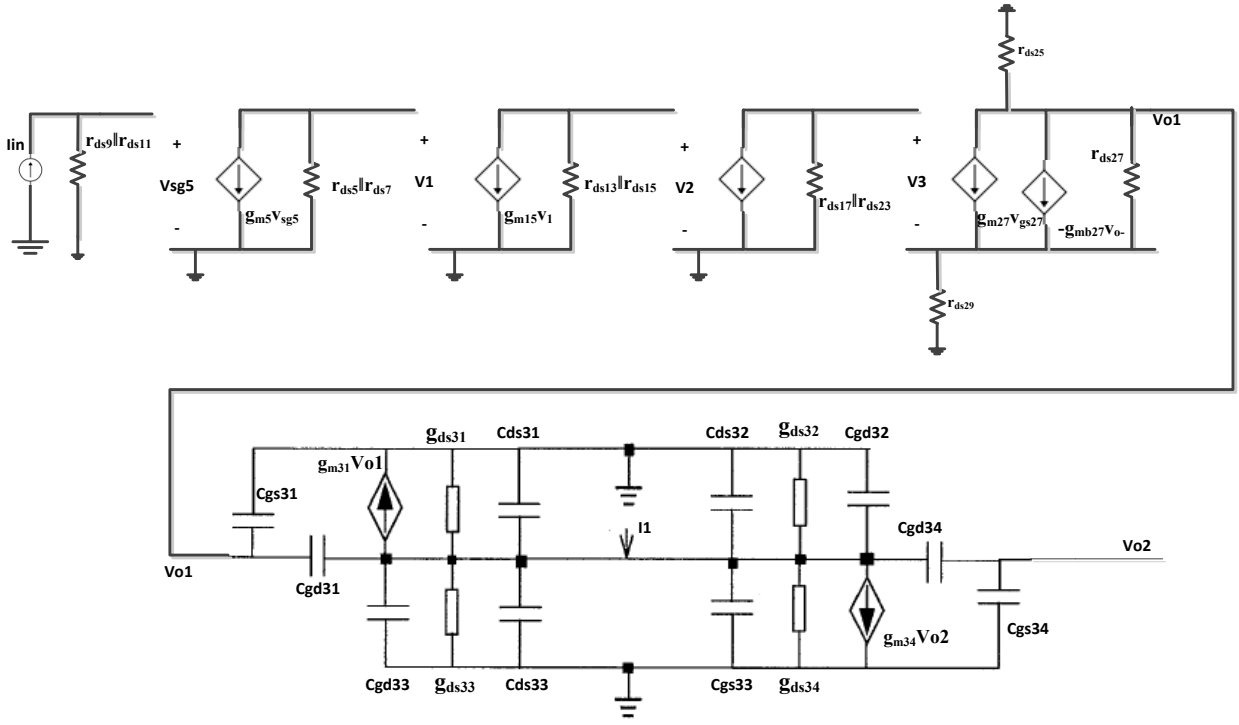

Figure 2.17: Small signal equivalent model of the half circuit of CCCS

From the above figure, we get the voltage gain expression as:

$$\frac{v_{o1}}{v_{sg5}} = \frac{v_o}{v_3} \cdot \frac{v_3}{v_2} \cdot \frac{v_2}{v_1} \cdot \frac{v_1}{v_{sg5}} \tag{2.22}$$

Now using (2.15),

$$\frac{v_{o1}}{v_{sg5}} = [-\frac{g_{m27} r_{ds25}}{1+(g_{m27}+g_{mb27}) r_{ds29}}] [-g_{m23} (r_{ds17}\|r_{ds23})]. [-g_{m15} (r_{ds13}\|r_{ds15})].[-g_{m5} (r_{ds5}\|r_{ds7})]$$

$$\text{Hence, } v_{o1} = [-\frac{g_{m27} r_{ds25}}{1+(g_{m27}+g_{mb27}) r_{ds29}}] .[-g_{m23} (r_{ds17}\|r_{ds23})].[-g_{m15} (r_{ds13}\|r_{ds15})].$$

$$[-g_{m5}\ (r_{ds5} \| r_{ds7})] v_{sg5} \tag{2.23}$$

Now putting the value of $v_{sg5} = (r_{ds5} \| r_{ds7})\ i_{in}$ into equation (2.23),

$$v_{o1} = [-\frac{g_{m27} r_{ds25}}{1 + (g_{m27} + g_{mb27}) r_{ds29}}] .\ [-g_{m23}\ (r_{ds17} \| r_{ds23})].[-g_{m15}\ (r_{ds13} \| r_{ds15})].$$

$$[-g_{m5}\ (r_{ds5} \| r_{ds7})].(r_{ds5} \| r_{ds7})\ i_{in} \tag{2.24}$$

Now from equation (2.11), output AC current,

$$i_{out} = 2(g_{m38} - g_{m31})\ v_{o1}$$

Putting the value of v_{o1} from equation (2.24) implies,

$$i_{out} = 2(g_{m38} - g_{m31}).\ [-\frac{g_{m27} r_{ds25}}{1 + (g_{m27} + g_{mb27}) r_{ds29}}] .\ [-g_{m23}\ (r_{ds17} \| r_{ds23})].[-g_{m15}\ (r_{ds13} \| r_{ds15})].$$

$$[-g_{m5}\ (r_{ds5} \| r_{ds7})].(r_{ds5} \| r_{ds7})\ i_{in}$$

Hence overall current gain of the CCCS circuit will be,

$$A_i = \frac{i_{out}}{i_{in}} = 2(g_{m38} - g_{m31}).\ [-\frac{g_{m27} r_{ds25}}{1 + (g_{m27} + g_{mb27}) r_{ds29}}] .\ [-g_{m23}\ (r_{ds17} \| r_{ds23})].[-g_{m15}\ (r_{ds13} \| r_{ds15})].$$

$$[-g_{m5}\ (r_{ds5} \| r_{ds7})].(r_{ds5} \| r_{ds7}) \tag{2.25}$$

The numerical value of the gain can be calculated from equation (2.25) using transconductance and resistance of appropriate transistors from APPENDIX – F. The value of current gain in this case is, $A_i = 520 \approx 54.32$dB.

2.10 Summary

This chapter introduced different sub-systems of the UAM with their proper functions. The gain expressions for the four different categories of amplifiers (i.e., VCVS, VCCS, CCVS, and CCCS) are produced and the respective numerical values are provided. The theoretical analysis should be validated using suitable simulations and experimental works. In the next chapter, simulations of the UAM are provided to validate the proposed voltage and current mode implementations of the UAM.

CHAPTER 3

CHARACTERIZATION OF THE UAM USING SIMULATIONS

3.1 Introduction

In the previous chapter, the design and analysis aspects corresponding to different sub-systems of the UAM have been presented. The techniques to adopt the UAM for the four basic categories of amplifiers (i.e., VCVS, VCCS, CCVS and CCCS) have been shown as well. Theoretical formulas for the gains of the basic amplifiers and the respective numerical values have been provided.

To validate the theoretical analysis, suitable simulations and experimental works are necessary. This chapter presents simulation results pertaining to the operations of the UAM as the four categories of amplifiers. Different performance parameters are measured by SPICE simulations. The simulations are performed at the schematic level followed by post layout simulations. The layout has been implemented using 0.18 μm CMOS (CMOSP18/TSMC) process.

3.2 Complete Schematic of UAM

Figure 3.1 shows the complete schematic diagram of the proposed Universal Amplifier Module (UAM) in 0.18 µm CMOS (CMOSP18/TSMC) technology.

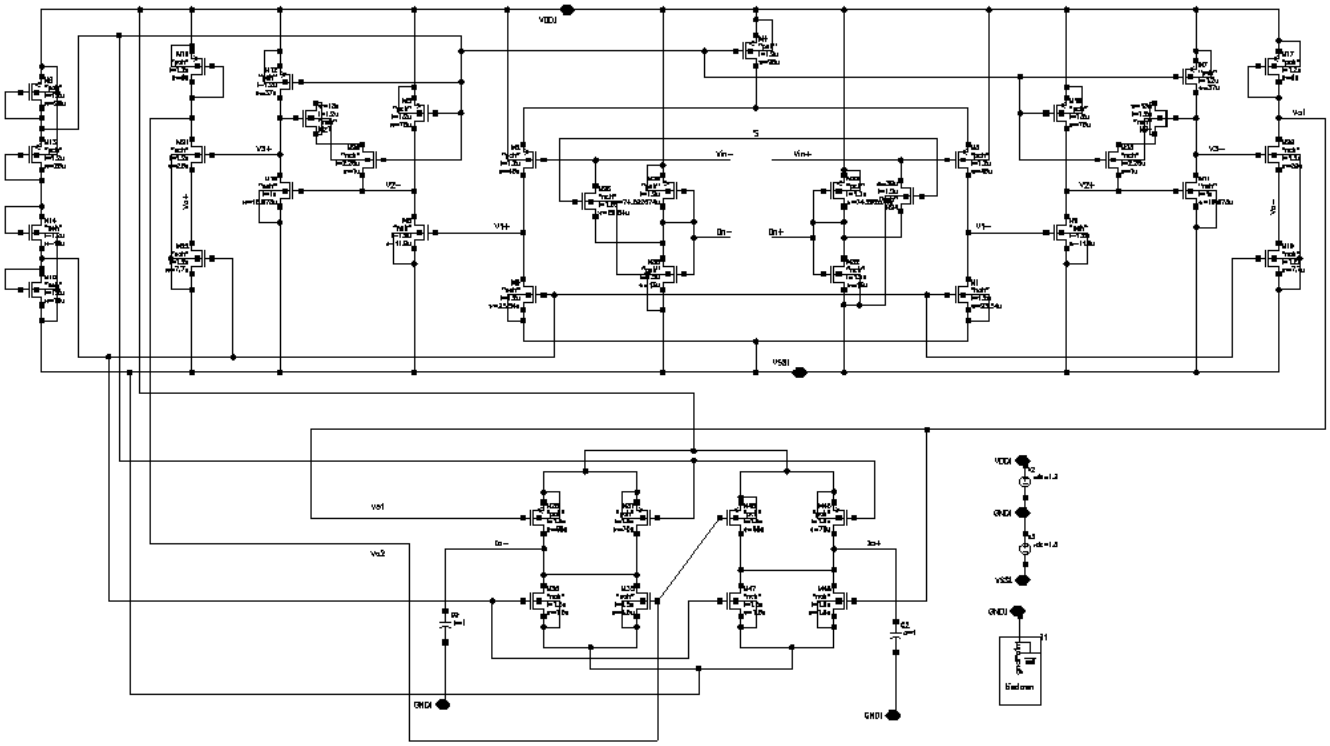

Figure 3.1: Complete schematic diagram of the UAM in 0.18 µm CMOS (CMOSP18/TSMC) technology

The UAM is now capable of providing all the voltage and current mode operations with just a single module. Either voltage or current signal input can be chosen by the switch, S. Two NMOS pass transistors are used as switch (S).

The switch (S) is:

'ON' when V_{gsn} = VDD, i.e. S = 1

and 'OFF' when V_{gsn} = VSS, i.e. S = 0

When the switch is 'ON', then the gate – drain connected transistors M8, M9, M10 & M11 (shown in figure 2.4) are connected across the input differential stages. Hence, there is a low impedance node at the input stages and a signal current can be applied at this node.

When the switch (S) is 'OFF', the gate – drain connected stage is disconnected from the input differential stages. Hence, a voltage signal can be applied to the input of the differential voltage amplifier section (comprising of transistors M4, M5, M6 & M7).

Selection of the switch (S) depends on the intended use of the mode of operations. Hence, S = 0 is set for voltage signal mode of operations, i.e. for VCVS and VCCS operations. On the other hand, S = 1 is set for current signal mode of operations, i.e. for CCVS and CCCS operations.

Voltage signal output is taken from the voltage buffer stage (comprising of transistors M25, M27 and M29 as shown in figure 2.6) which is a low impedance node. The current signal output is taken from the current buffer stage (comprising of transistors M31 – M38 as shown in figure 2.7) which is a high impedance node.

3.3 Dimensions of the transistors

The transistors in the half circuit of the Universal Amplifier Module (UAM), shown in figure 2.9 of chapter 2, have the dimensions presented in Table 3.1.

Table 3.1: Dimensions of the transistors used in UAM

TRANSISTORS	W (µm)	L (µm)
M0, M1, M27	20	1.2
M2, M3	10	1.2
M4, M5	40	1.2
M6, M7	23.4	1.2
M8, M9	74.16	1.2
M10, M11, M19	13	1.2
M12	95	1.2
M13	70	1.2
M15	11.88	1.2
M17	37	1.2
M21	1	2.25
M23	10.08	1
M25	9	1.2
M29	7.7	1.2
M31, M35	65	1.5
M32, M36	70	1.5
M33, M34, M37, M38	1.5	1.5
M39, M40	30	1.2

3.4 Performance parameters measurements

Simulations were done for all the voltage and current mode operations (i.e. VCVS, VCCS, CCVS and CCCS). Due to page limitations, only simulations of VCVS are presented in this section. At the same time, all the voltage and current mode simulation results are given in tabular format. Figure 3.2 shows the UAM as a block representation used for the simulations to measure various performance parameters.

Measurements for VCVS (i.e., operational amplifier, OP-AMP) Configuration:

3.4.1 Open loop frequency response

V_{in} = 1 V AC is applied at the voltage input section. The switch, S is set to OFF mode (i.e., S=0).

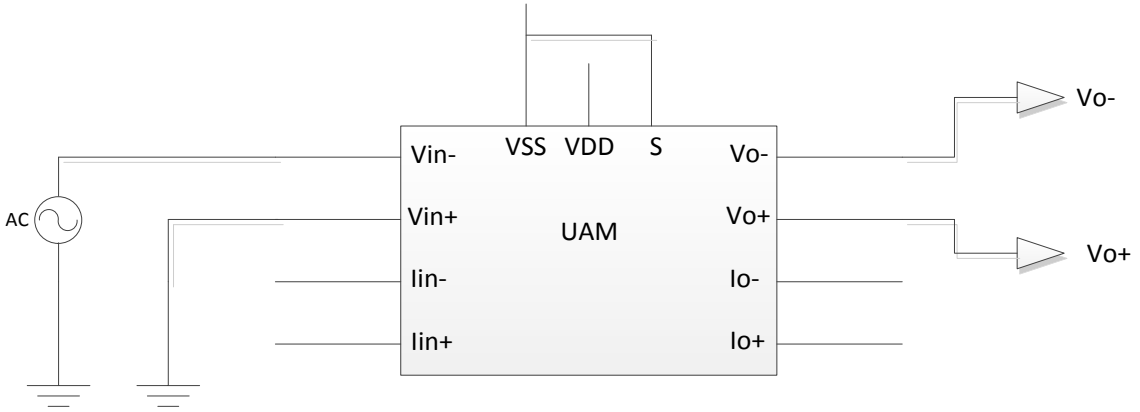

Figure 3.2: Configuration for open loop frequency response

The frequency plot, called as bode plot gives an estimation of open loop voltage gain and phase response. It also shows the occurrence of poles, zeros, unity gain bandwidth, 3dB frequency etc. The phase margin and gain margin of the VCVS can also be calculated from the frequency response. Figure 3.3 shows the magnitude and phase response of the VCVS. From the figure, voltage gain, A_v = 118 dB (for v_{o-}). From the other half circuit it can be shown that, voltage gain is 117.9 dB (for v_{o+}).

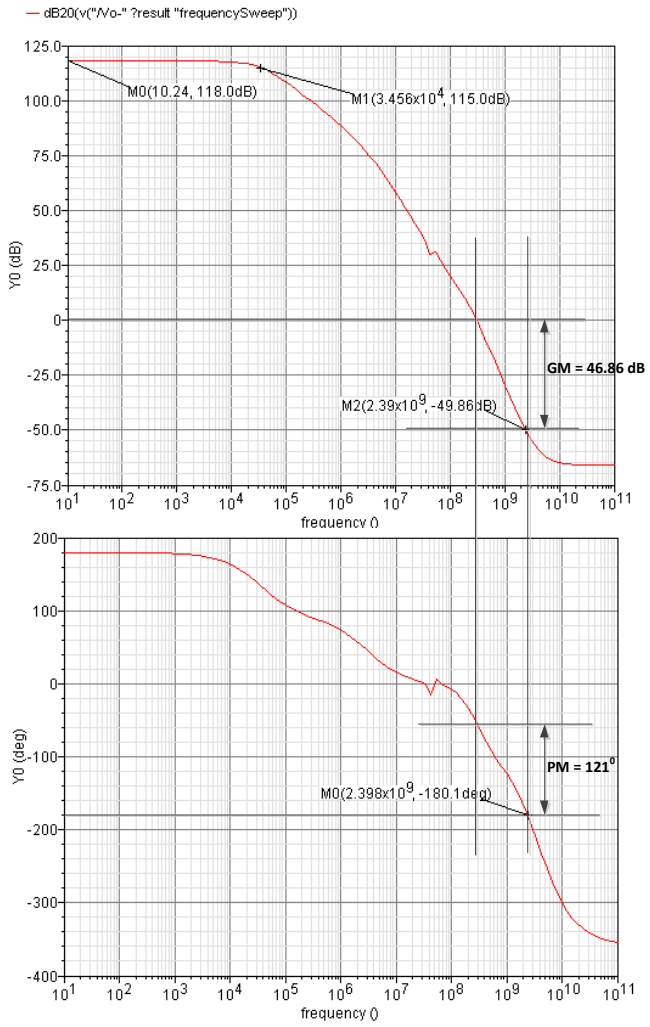

Figure 3.3: Magnitude and phase response of the VCVS

3.4.2 Phase margin and Gain margin

Phase margin and gain margin are the measures of stability of a feedback system. Sometimes only phase margin is used rather than both. Based on the magnitude response of the loop gain, $|A_{OL}\beta|$, phase margin can be defined as the phase difference between $|\angle A_{OL}\beta(w_{0dB})|$ and 180° where w_{0dB} is the frequency at which $|A_{OL}\beta|$ is unity (0 dB). For a stable feedback system, phase margin of 60° is highly desirable as a trade-off between closed-loop stability and settling time in the transient response. Typically, the minimum acceptable phase margin is 45°. Phase margin is

illustrated in figure 3.3. From the figure, phase margin of the VCVS is 121^0 (for v_{o-}). From the other half circuit it can be shown that, phase margin is 56.9^0 (for v_{o+}). On the other hand, gain margin can be calculated as the difference between unity gain (0 dB) and $|A_{OL}\beta(w_{180°})|$ where $w_{180°}$ is the frequency at which the loop gain phase, $\angle A_{OL}\beta$, is -180°. From figure 3.3, gain margin is 49.86 dB (for v_{o-}) and for the other half circuit gain margin is 33.72 dB (for v_{o+}).

3.4.3 Input offset voltage

The differential input offset voltage is defined as the voltage that must be applied between the two input terminals of the op amp to make the differential output (V_{odiff} in fig. 3.4) as zero volts.

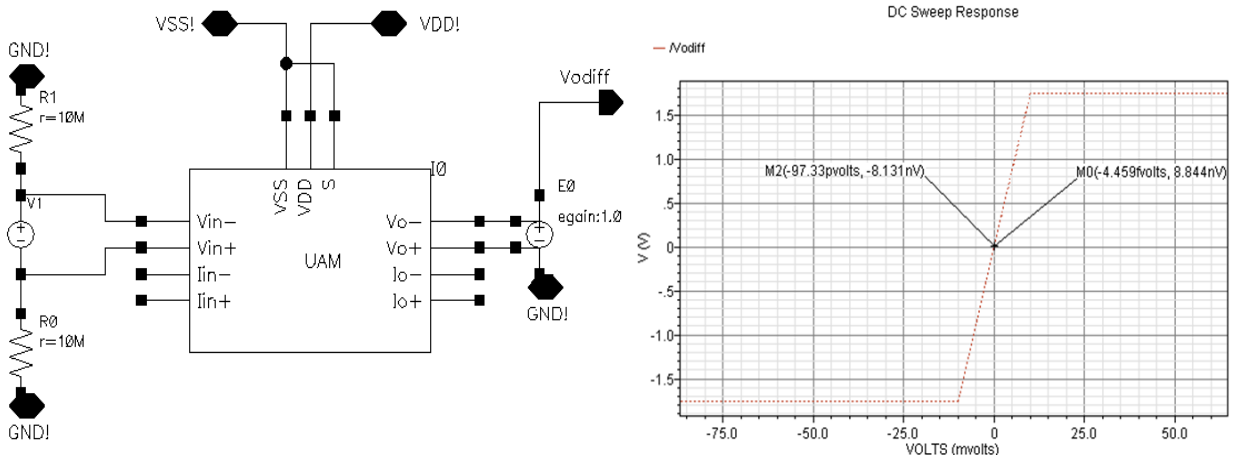

Figure 3.4: (a) Configuration for measuring input offset voltage (b) Simulated result of input offset voltage

Figure 3.4 (a) shows the simulation set-up for measuring input offset voltage of the VCVS. Ideally, input offset of an OP-AMP should be at zero volts. But in practical case, amplifiers exhibit offset which may shift the voltage transfer curve from the origin and in this case, the voltage transfer curve is shifted by 97.33 pV to the negative x-axis. Hence, for this system, the differential input offset voltage of the UMA is -97.33 pV as shown in figure 3.4 (b).

3.4.4 Input common mode range (ICMR)

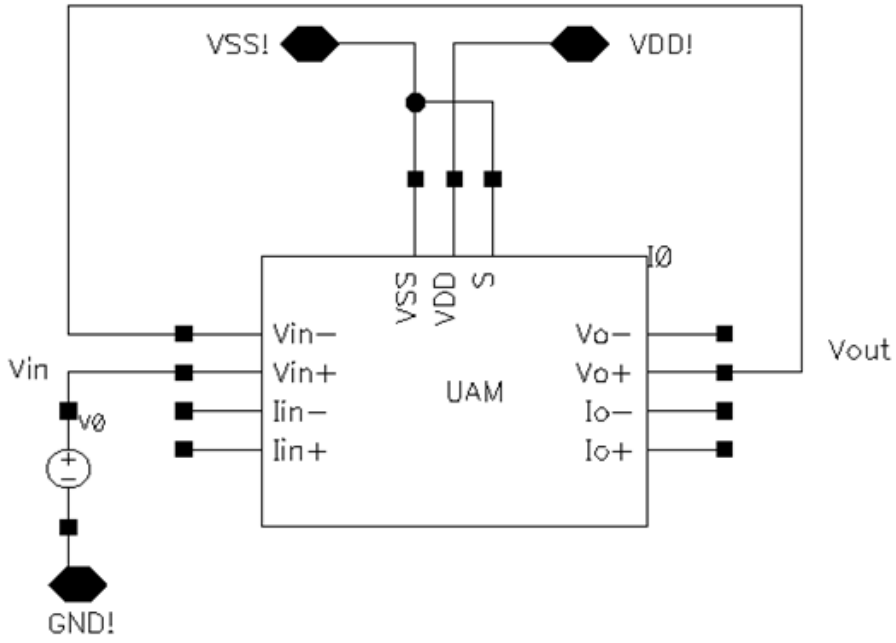

Figure 3.5: Configuration for measuring input common mode range (ICMR)

Figure 3.5 shows the set-up for measuring input common mode range (ICMR) [2]. ICMR is defined as a range of voltages over which the amplifier continues to sense and amplifies the input signal with a constant gain. The OP-AMP is configured in unity gain configuration for measuring or simulating ICMR. A DC voltage sweep is applied at the positive voltage terminal of the VCVS. Figure 3.6 shows the DC sweep response of the system. The linear part of the transfer curve corresponds to the input common mode voltage range of the system. A non-linear characteristics curve may cause distortion in the output signal. From the figure, the input common mode range of the VCVS is ≈ -690 mV ↔ +467.7 mV.

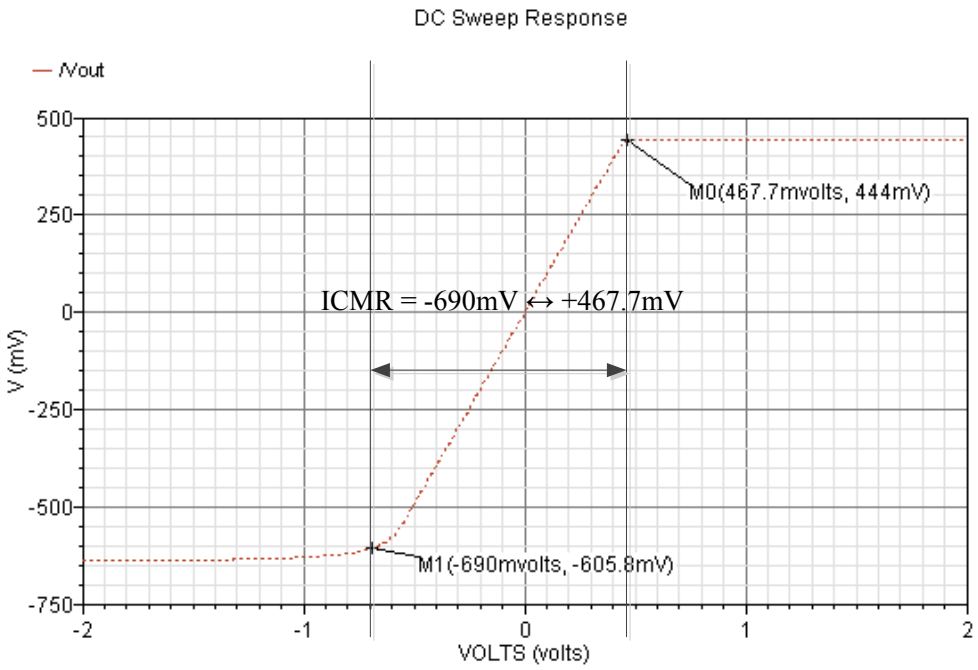

Figure 3.6: Simulated ICMR characteristics

3.4.5 Output voltage swing

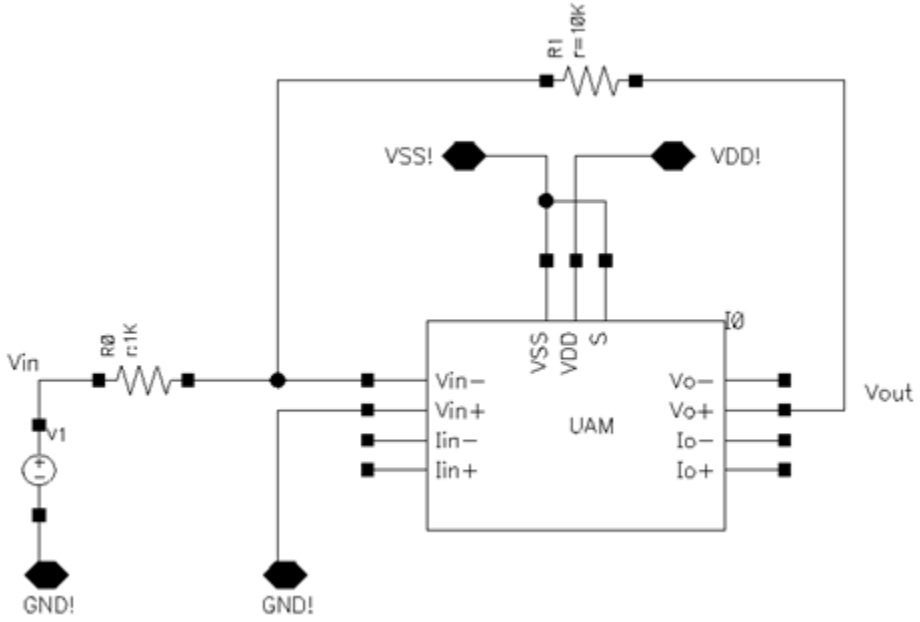

Figure 3.7: Measurement set-up for output voltage swing

The input common mode range (ICMR) is limited by the linearity of the transfer curve in the unity gain configuration. Whereas, if the amplifier is configured as for higher gain, the linear part of the transfer curve corresponds to the output voltage swing [2]. Figure 3.7 shows the configuration for measuring output voltage swing. The amplifier is configured for inverting gain of -10 (R_0 = 1 KΩ, R_1 = 10 KΩ). Figure 3.8 shows the output response. From the figure, output voltage range is ≈ -117.9 mV ↔ +328.5 mV.

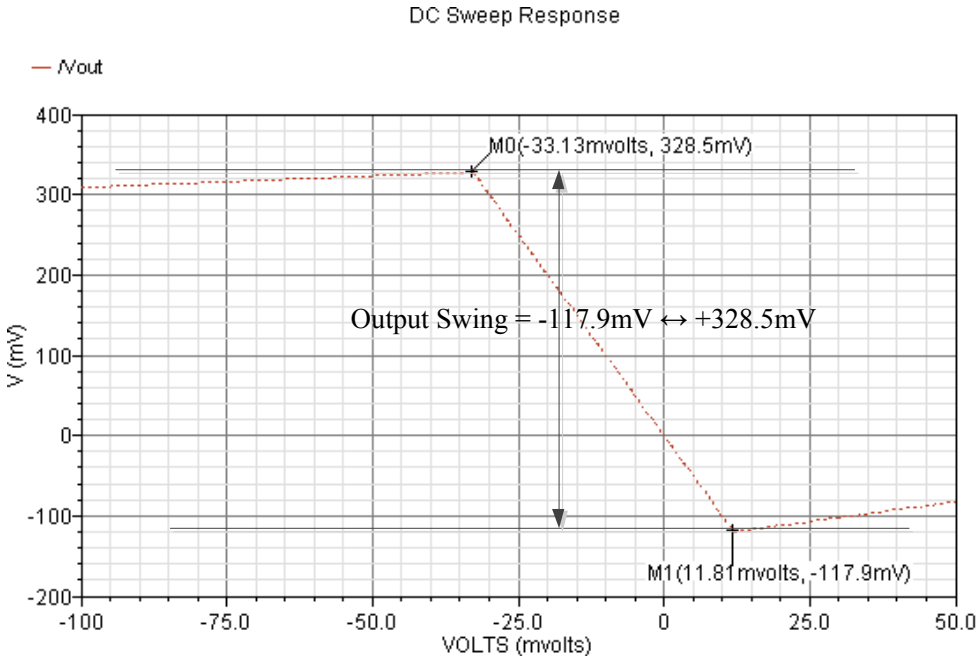

Figure 3.8: Simulated output voltage swing

3.4.6 Output offset voltage

The differential output offset voltage can be measured using the same configuration as shown in figure 3.4. The differential output offset voltage can be defined as the difference between the DC output voltages in ideal condition and DC output voltage of the VCVS when the input voltage is set to some fixed reference voltage. From the transfer curve of 3.4(b), the differential output

voltage was observed as 8.8 nV when the differential input voltage is ≈ 0 V. Hence, the differential output offset voltage of the VCVS is 8.8 nV.

3.4.7 Slew rate measurement

Slew rate is defined as the rate of change of output voltage when a step voltage is applied at the input of the operational amplifier in unity gain configuration. This parameter actually designates the fastness of an OP-AMP with which the output of an OP-AMP can change consequent to a large signal input to the system. This arises because of the limitation on the maximum amount of current that the OP-AMP can deliver to a capacitive load. The limitation originates at the input stage of the OP-AMP.

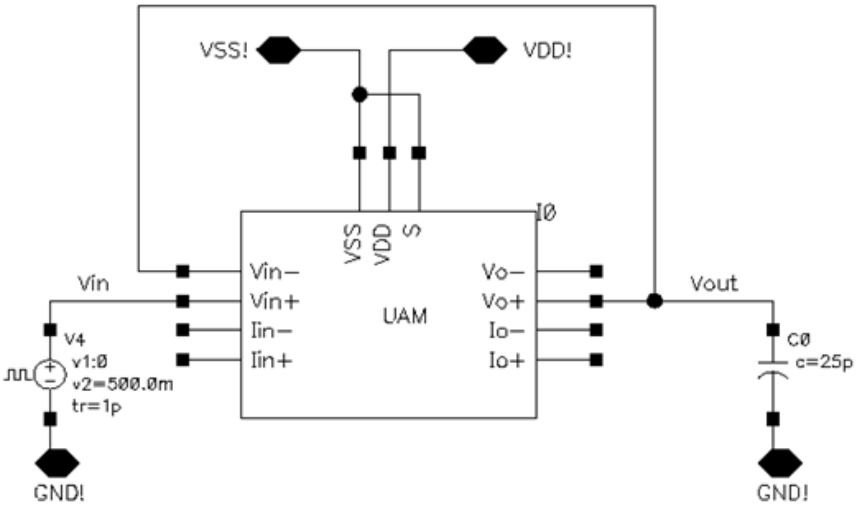

Figure 3.9: Configuration for measuring slew rate

Figure 3.9 shows the configuration for measuring the slew rate of the VCVS. A step input is applied at the input and output is measured as a function of time. The capacitive load could be arising out of parasitic or it could be a physical capacitance. In this case, a load capacitor of C_L = 25 pF is used to simulate the slew rate. Figure 3.10 shows the simulated result of the slew rate measurement. Positive slew rate is measured at the rising edge of the output response. From the

figure, positive slew rate, SR^+ = +2.42 V/µs. On the other hand, negative slew rate is measured at the falling edge of the output. From the figure, SR^- = -0.48 V/µs.

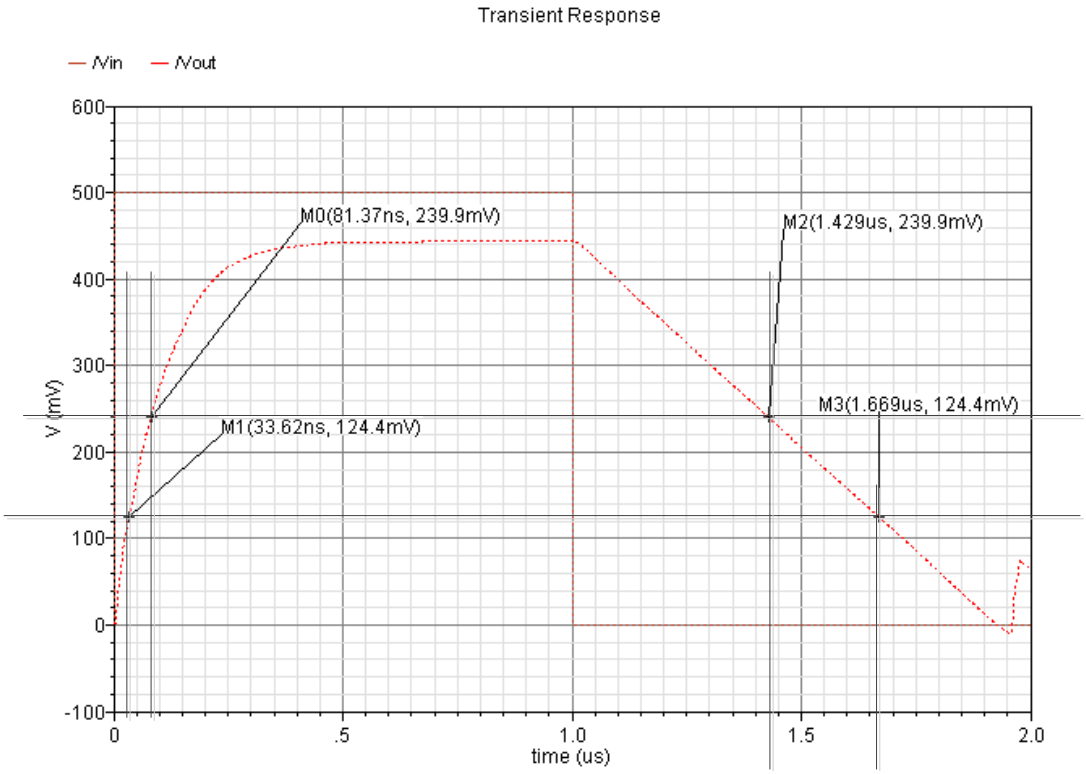

Figure 3.10: Simulated result of slew rate measurement

3.4.8 Common mode rejection ratio (CMRR)

Common mode rejection ratio (CMRR) is defined as the ability of the differential amplifier to reject the common mode signal. It can be measured from the differential mode voltage gain, A_d to the ratio of common mode voltage gain, A_{cd} as [33]:

$$CMRR = \frac{A_d}{A_{Cd}}$$

Figure 3.11 shows the configuration for the measurement of differential CMRR. Differential common mode gain is measured from this set-up as, $A_{cd} = \frac{v_{o+} - v_{o-}}{v_{cm}} = \frac{v_{odiff}}{v_{cm}}$ = -78.79 dB. Hence

CMRR can be calculated by dividing the differential gain (A_d = 122 dB in this case) by differential common mode gain, A_{cd}. Hence, CMRR = 122 dB – (-78.79) dB = 200.79 dB (at low frequency). Figure 3.12 shows the simulated CMRR response which is obtained by differencing the differential mode response (in dB) and common mode response (in dB) i.e. A_d–A_{cd}.

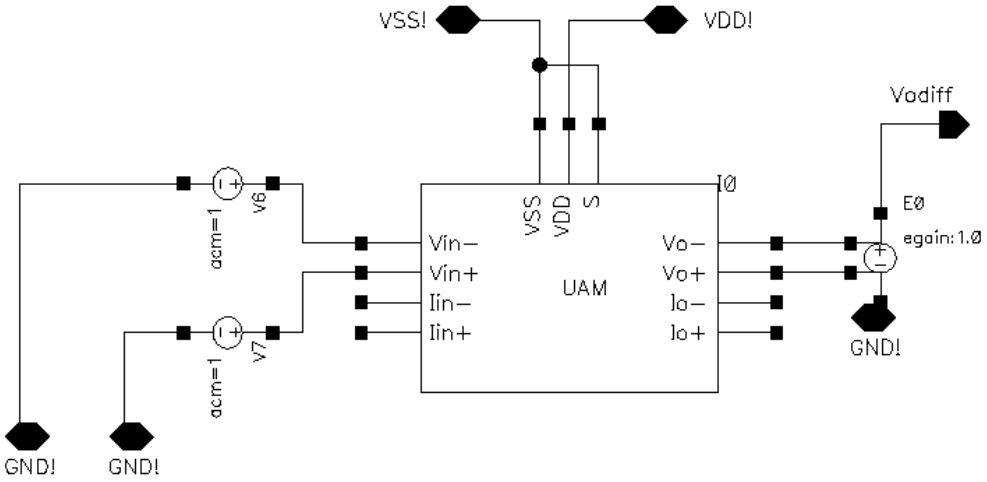

Figure 3.11: Measurement set-up for CMRR

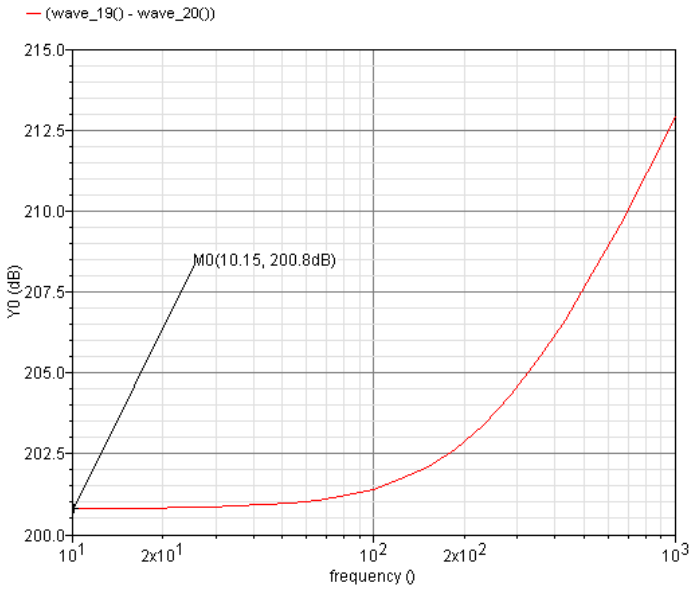

Figure 3.12: Simulated CMRR response

3.4.9 Power supply rejection ratio (PSRR)

Power supply rejection ratio (PSRR) is defined as the ratio of the differential gain of the amplifier to the gain from the power supply ripple that contributes to the output. Power supply ripple actually contributes to the noise at the output of the OP-AMP. Ideally, an OP-AMP should have infinite PSRR, i.e. the output should be unaffected by the power supply ripple voltage. PSRR can be calculated by putting the OP-AMP in the unity-gain configuration with the input shorted [67]. Figure 3.13 shows the configuration for the measurement of PSRR as a function of frequency. In this case, a 1 V sinusoidal signal is inserted in series with VDD for measuring

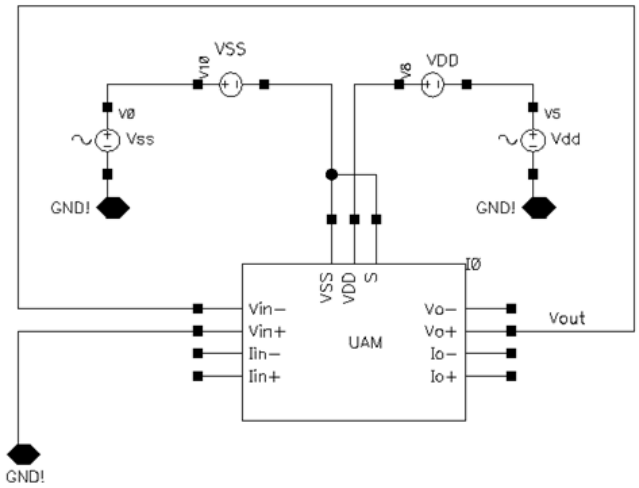

Figure 3.13: Configuration for measuring PSRR [2]

$PSRR^+$ while VSS is maintained at its usual value. On the other hand, for measuring $PSRR^-$, a 1V sinusoidal signal is inserted in series with VSS while VDD is maintained at its usual value. Output is observed at v_{o+}. The PSRR can be calculated from the following equation [2]:

$$\frac{v_{o+}}{v_{dd}} \approx \frac{1}{PSRR^+} or \frac{v_{o+}}{v_{ss}} \approx \frac{1}{PSRR^-}$$

Figure 3.14 shows the simulated frequency response of the PSRR. From the figure, the peak value of $PSRR^+ = PSRR^- = 82.74$ dB @43 KHz. Similar result was obtained for v_{o-}.

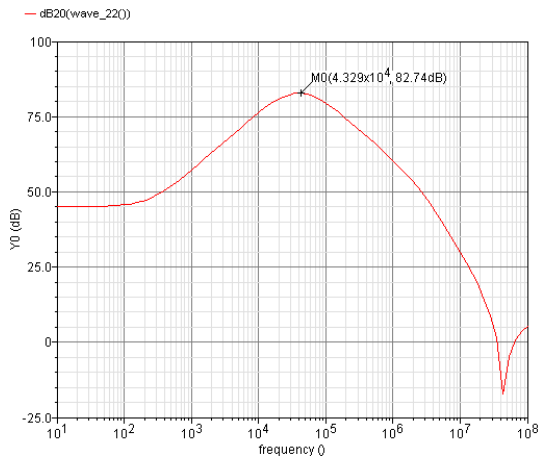

Figure 3.14: Simulated result for PSRR frequency response

3.5 Complete Layout of UAM

The simulations were verified in layout level as well. Figure 3.15 shows the complete layout the Universal Amplifier Module in 0.18 µm CMOS (CMOSP18/TSMC) technology. The pad connections are not shown.

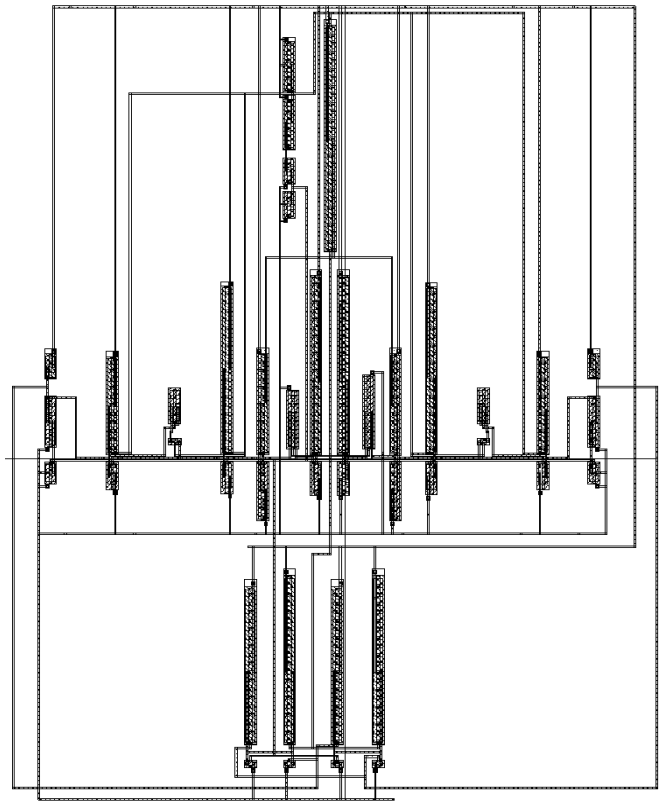

Figure 3.15: Complete layout of the UAM in 0.18 µm CMOS (CMOSP18/TSMC) technology

3.6 Performance parameters for VCCS, CCVS and CCCS

Simulations for performance parameters measurement were also done for other voltage and current mode circuit operations (i.e. VCCS, CCVS and CCCS). The previous section presented the simulation set-ups and results for only VCVS configuration. The simulation set-ups and results for other voltage and current mode implementations (i.e. VCCS, CCVS and CCCS) are provided in APPENDIX – D. All the voltage and current mode simulation results are presented in table 3.2.

Table 3.2: Table for performance parameters measurements

Parameters	Voltage Amplifier (VCVS)	Transconductance Amplifier (VCCS)	Transresistance Amplifier (CCVS)	Current Amplifier (CCCS)
CMOS technology	0.18 µm			
Power Supply	+1.3 V, -1.3 V			
Open loop Gain	117.8 dB	7.22 dBA/V	165.1 dBΩ	54.32 dB
3dBGain bandwidth	26.83 GHz	80.56 KHz	5.97 THz	18.2 MHz
Unity gain bandwidth	272.7 MHz	72.83 KHz	1.28 GHz	8.92 MHz
Phase margin	56.9^0	64.4^0	53.5^0	44.12^0
Gain margin	49.86 dB	68.83dB	88.09 dB	58.76 dB
Input offset	-97.33 pV	-11.14 pV	1.49 µA	-
Input CMR	-690 mV ↔ +467.7 mV	-1.069 V ↔ +1.069 V	-0.4 mA ↔ +10 mA	-10 mA ↔ +53.37 µA
Output swing	-117.9 mV ↔ 328.5 mV	-1.025 µA ↔ -689.1 µA	-252 mV ↔ +1.048 V	-1.054 mA ↔ +947.2 mA
Slew rate+	2.42 V/µs	0.45 V/µs	3.2 V/µs	0.22 V/µs
Slew rate-	-0.48 V/µs	-0.3 V/µs	0.4 V/µs	0.10 V/µs
CMRR	200.79 dB	156.01 dB	78.3 dB	83.17 dB
PSRR	82.74 dB	48.21 dB	84.55 dB	87.93 dB
Output offset	8.8 nV	90 fA	-260.5 µV	-
Output resistance	1.1 KΩ	115.62 KΩ	1.1 KΩ	115.62 KΩ
Input resistance	∞	∞	200 Ω	200 Ω
Power dissipation	7.179 mW	7.179 mW	7.179 mW	7.179 mW

3.7 Common-Mode Feedback (CMFB)

Differential Difference Amplifier (DDA) CMFB circuit is used to provide common – mode feedback [38] for the UAM. The DDA CMFB circuit averages two differential signals and compares that average to a reference common-mode voltage, V_{cm} by using four identical transistors configured into two differential-pair (DP) structures [38]. One of the two transistors in each DP is connected to V_{cm} and the other two transistors are connected to the differential signals that are obtained from the VCVS.

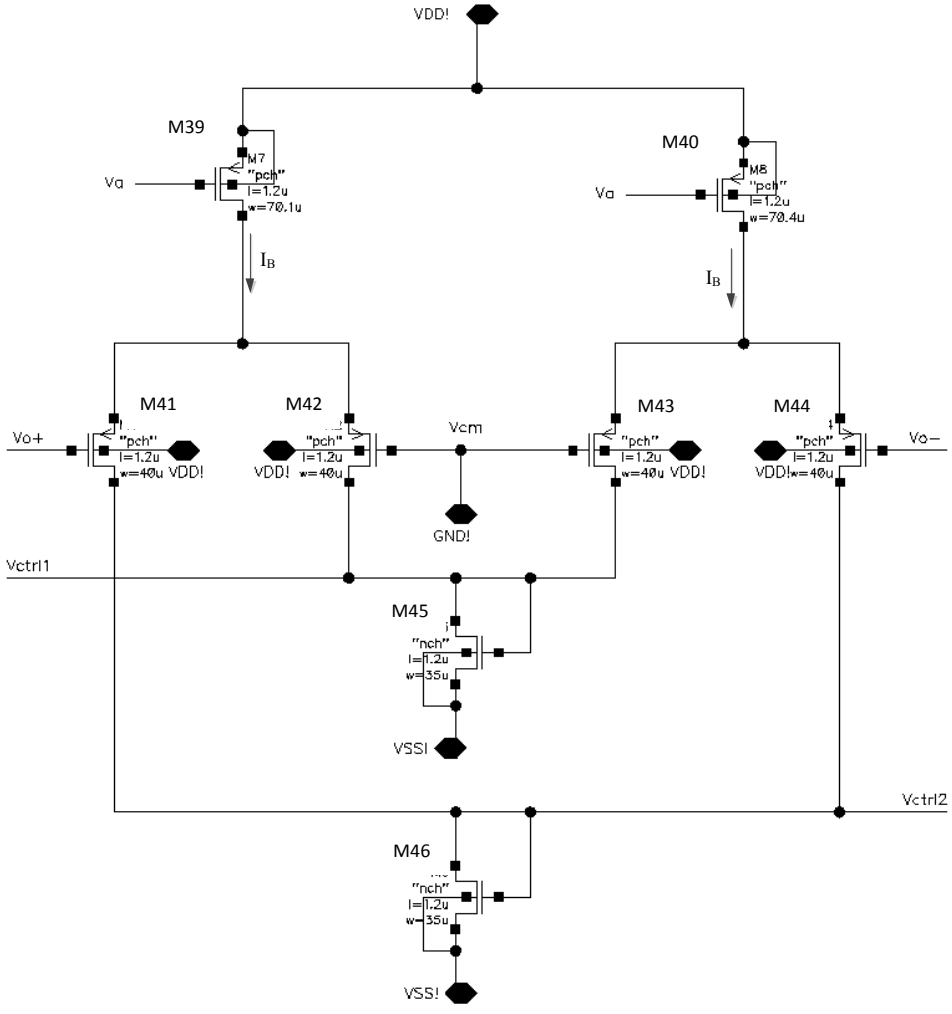

Figure 3.16: Differential Difference Amplifier CMFB circuit [38]

Figure 3.16 shows the differential difference common-mode feedback circuit that is used in this case. Two differential signals are obtained from the VCVS output voltage buffer stages as V_{o+} and V_{o-}. These two differential voltages are compared with V_{cm} which is considered here as '0' volts. Writing the drain current (I_D) equations for transistor M41, M42, M43 and M44,

$$I_{D41} = \frac{I_B}{2} - \Delta I$$
$$I_{D42} = \frac{I_B}{2} + \Delta I$$
$$I_{D43} = \frac{I_B}{2} - \Delta I$$
$$I_{D44} = \frac{I_B}{2} + \Delta I$$

Here, ΔI is large signal current change in I_{D42}. From the above equations it can be seen that,

$$I_{D41} = I_{D43} \text{ and } I_{D42} = I_{D44}$$

Equation of current through M45 can be written as,

$$I_{D45} = I_{D42} + I_{D43}$$
$$I_{D45} = (\frac{I_B}{2} + \Delta I) + (\frac{I_B}{2} - \Delta I)$$
$$I_{D45} = I_B$$

The size of transistor M45 is chosen such that $I_{D45} = I_B$, which implies that the common-mode voltage of the differential output signals (V_{o+} & V_{o-}) equals to V_{cm}. Two control voltages, V_{ctrl1} and V_{ctrl2} are generated which are fed back to two differential voltage buffer stages of the UAM that establish the correct common-mode output currents in the output stage of the UAM to keep the common-mode output voltage at V_{cm}. Figure 3.17 shows the complete diagram of the CMFB implementation with the UAM. Internal circuitry of UAM block is shown in figure 2.9 in section 2.8 of chapter 2. Figure 3.18 shows the output response of the UAM with CMFB.

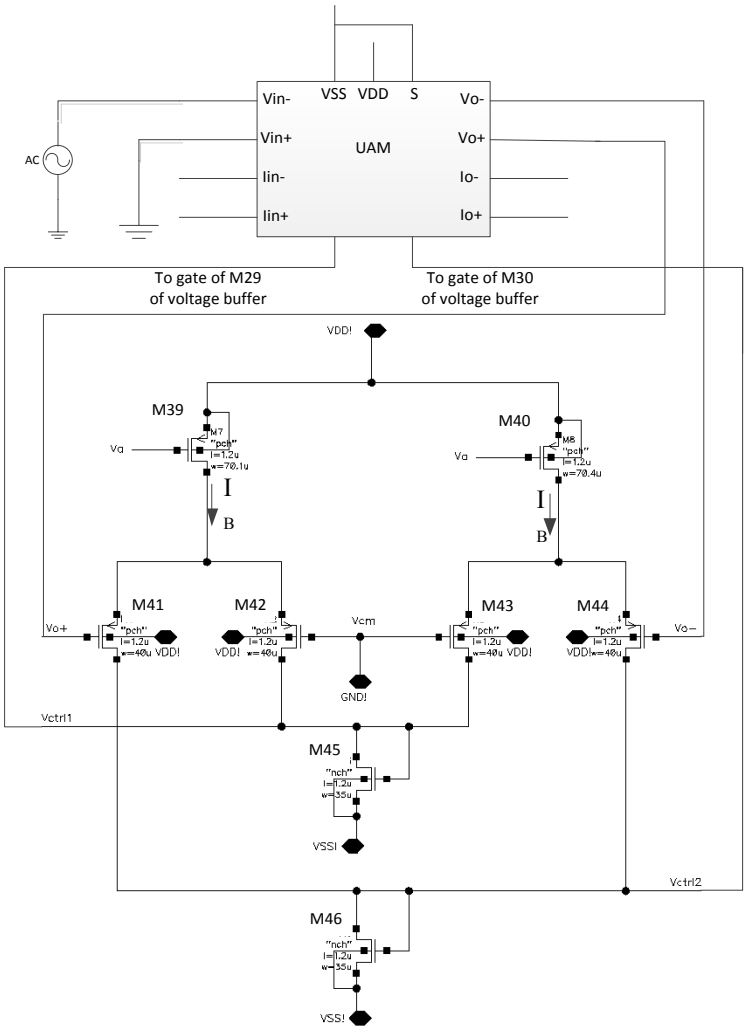

Figure 3.17: Complete diagram of the CMFB implementation with the UAM

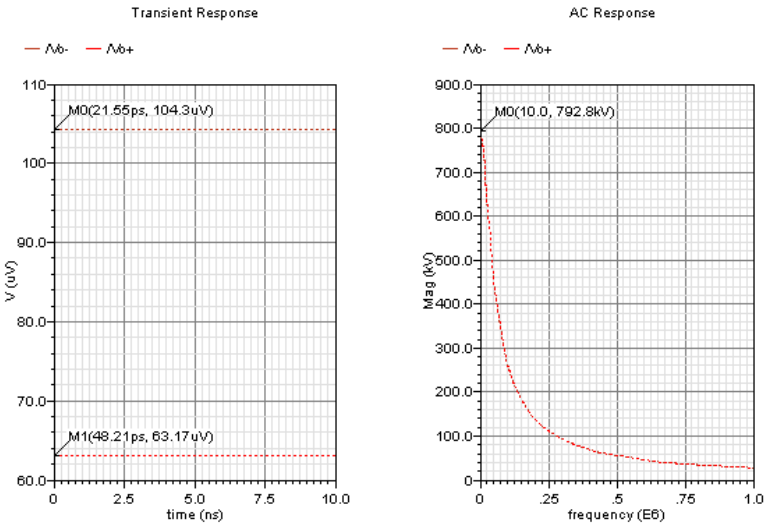

Figure 3.18: Simulated output of the VCVS after using CMFB

3.8 Comparison between the UAM and reported work in the literature

In this section, the performance of the proposed Universal Amplifier Module (UAM) is compared with some works reported in the literatures. We did not find any work oriented toward the UAM concept. There are research works available on operational amplifier, transconductance amplifier, transresistance amplifier, current conveyor separately. In this sense, it is difficult to compare this work with previous works as a whole. Rather, as the proposed UAM can provide all the voltage and current mode operations, different mode of operations can be compared with the similar voltage and current mode devices respectively. Latest reported work on OP-AMP, OTA, OTRA and CCII using this technology in this regard appears to be in 2008.

3.8.1 Comparison between the UAM (operating as OP-AMP) and reported work in literature

Table 3.3: Comparison between UAM (operating as Operational Amplifier) and reported work in literature

Parameters	This UAM as OP-AMP	[47]	[49]	[48]
CMOS technology	0.18 µm	0.8 µm	1.6 µm	1.2 µm
Power Supply	±1.3 V	3 V	1.8 – 7.0 V	3 V
Gain	117.9 dB	95.1 dB	86 dB	113 dB
Gain bandwidth	272.7 MHz	17.5 MHz	4 MHz	5.5 MHz
Phase margin	56.9^0	60^0	67^0	$>45^0$
Input offset	-97.33 pV	-	6 mV	-
Input CMR	-690 mV ↔ +467.7 mV	-	Vss – 0.5 V↔ Vdd – 1.3 V	-
Output swing	-117.9 mV ↔ 328.5 mV	-	Vss + 0.1 V ↔ Vdd – 0.1 V	-
Capacitive load, C_L	25 pF	15	10	10
Slew rate	2.42 V/µs		4 V/µs	
Power dissipation, P	7.179 mW	4.8 mW	9 mW	0.31 mW
Figure of merit ($GBW*C_L/P$)	949.64	54.68	4.44	177.42

3.8.2 Comparison between the UAM (operating as OTA) and reported work in literature

Table 3.4: Comparison between the UAM (operating as OTA) and reported work in literature

Parameters	This UAM as OTA	[50]	[51]	[52]	[53]
CMOS technology	0.18 µm	1.2 µm	0.18 µm	0.35 µm	0.25 µm
Power Supply	±1.3 V	±1.5 V	0.5 V	1.5 V	1.2 V
Gain	7.22 dBA/V	>63 dB*	55 dB*	70.8 dB*	68.5 dB*
Unity gain bandwidth	72.83 KHz	8 MHz	8.72 MHz	330 MHz	165 MHz
Phase margin	64.4^0	60^0	61^0	64.5^0	65^0
Capacitive load, C_L	25 pF	35 pF	10 pF	3 pF	4 pF
Slew rate	0.45 V/µs	10.2 V/µs	1.35 V/µs	300 V/µs	329 V/µs
CMRR	156.01 dB	-	61.9 dB	-	-
Output resistance	115.62 KΩ	-	200 KΩ	-	-
Power dissipation, P	7.179 mW	0.7 mW	77 µW	1.4 mW	5.8 mW

* Indicates voltage gain number

3.8.3 Comparison between the UAM (operating as OTRA) and reported work in literature

Table 3.5: Comparison between the UAM (operating as OTRA) and reported work in literature

Parameters	This UAM as OTRA	[54]	[56]	[55]
CMOS technology	0.18 µm	0.25 µm	0.18 µm	0.25 µm
Power Supply	±1.3 V	±1.5 V	0.8 V	±1.5 V
Gain	165.1 dBΩ	130 dBΩ	158 dBΩ	179.12 dBΩ
Gain bandwidth	5.97 THz	3.16 THz	-	45.2 THz
Phase margin	53.5^0	-	70^0	22.5^0
Input CMR	-0.4 mA ↔ +10 mA	-50 µA ↔ +50 µA	-	-50 µA ↔ +50 µA
PSRR	84.55 dB	90.2 dB	-	-
Input resistance	200 Ω	26.07 KΩ	-	26.07 KΩ
Power dissipation	7.179 mW	0.709 mW	-	0.82 mW

3.8.4 Comparison between the UAM (operating as CCII) and reported work in literature

In this case, the UAM was configured as CCII configuration following the current feedback technique as reported in [35]. Detail CCII implementation of the UAM is discussed in section 4.7 of chapter 4.

Table 3.6: Comparison between the UAM (operating as CCII) and reported work in literature

Parameters	This UAM as CCII	[57]	[58]	[59]
CMOS technology	0.18 µm	0.18 µm	1.2 µm	0.13 µm
Power Supply	±1.3 V	±1.65 V	-2.5 – 2.92	±0.5 V
Gain	22.5 dB	1.01 dB	1.0015 dB	1 dB
3dBGain bandwidth	20.2 MHz	700 MHz	104 MHz	77 MHz
Input CMR	-1 mA ↔ +0 A	-	-100 µA ↔ +100 µA	-
Output resistance	115.62 KΩ	-	-	600 KΩ
Input resistance	200 Ω	0.018 Ω	26 Ω	68Ω
Power dissipation	7.179 mW	3.1 mW	-	1.04 mW

3.9 Post layout simulations

Layout of different sub-systems of the Universal Amplifier Module (UAM) is performed separately and the simulation results are compared with corresponding theoretical values. The layout was done in 0.18 µm CMOS (CMOSP18/TSMC) technology.

3.9.1 Layout of bias sources

Figures 3.19(a) & (b) show respectively the layout of the bias sources and the test block for simulations. Figure 3.20 shows the simulated output of the bias source block. Form the figure, it is observed that, two bias voltages $V_a \approx 691$ mV and $V_c \approx -765$ mV are generated that was designed theoretically in section 2.2 of chapter 2.

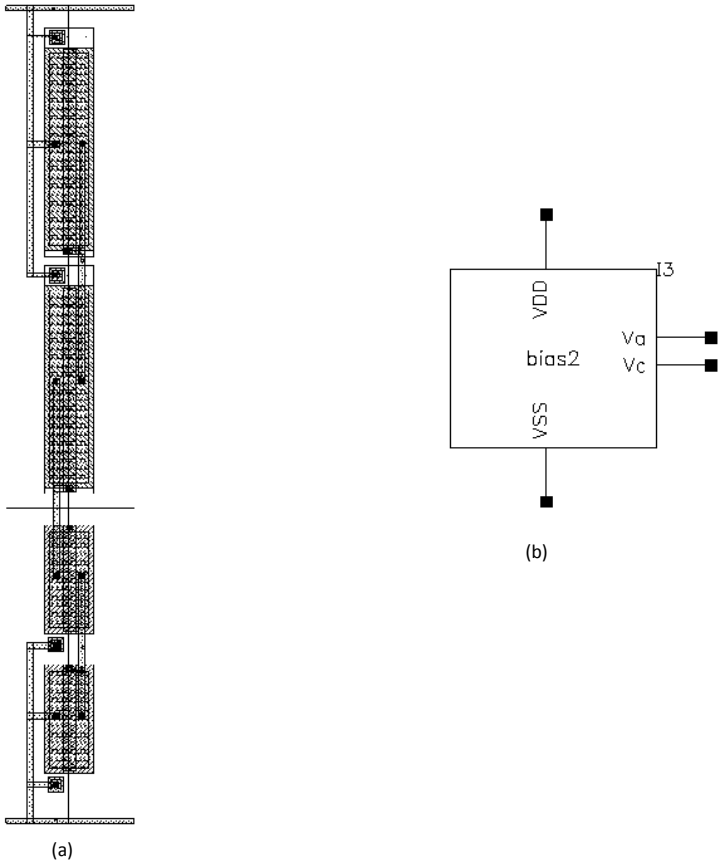

Figure 3.19: (a) Layout of the bias sources; (b) test block of the bias source

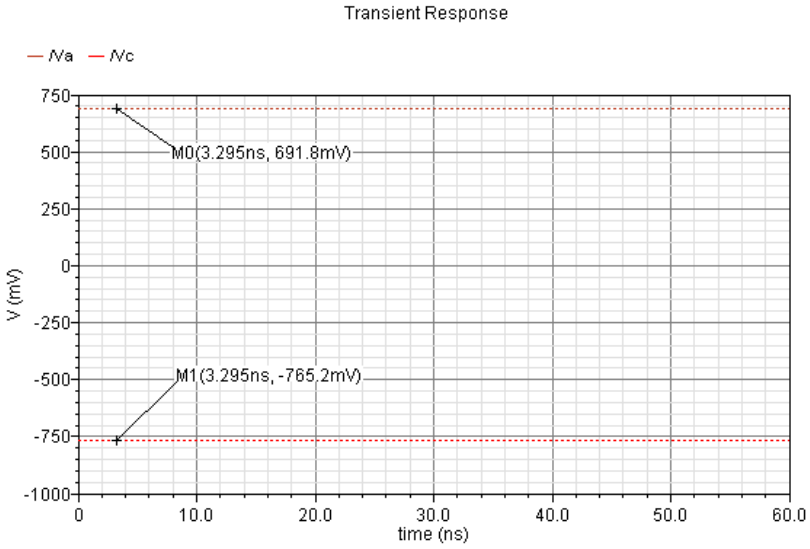

Figure 3.20: Simulated output of the bias source layout block

3.9.2 Layout of input differential amplifier stages

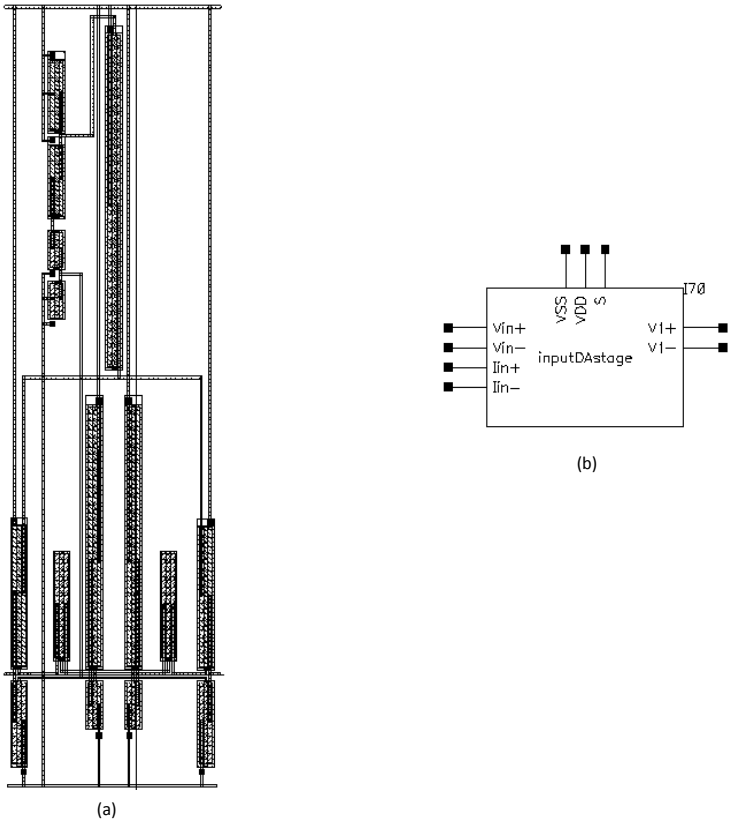

Figure 3.21: (a) Layout of the input differential stages; (b) Test block of the input DA stages

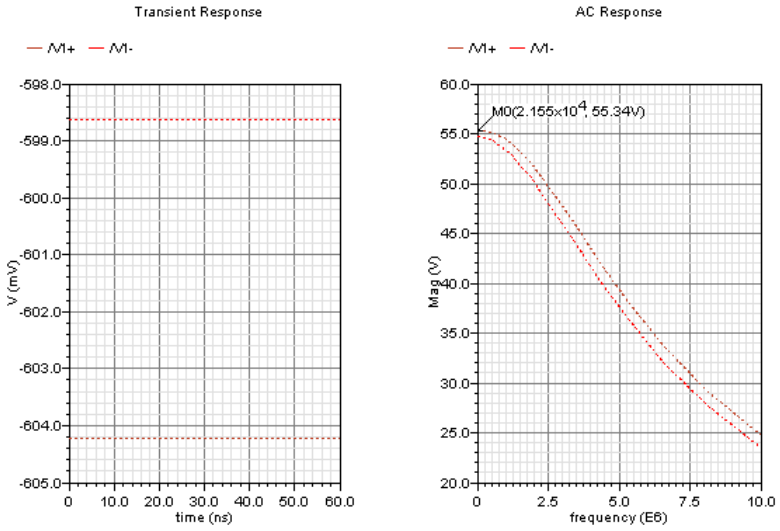

Figure 3.22: Simulated DC level and output AC signal of the input DA stages

Figures 3.21(a) & (b) show respectively the layout of the input differential stages and corresponding test block for simulations. Figure 3.22 shows the simulated output of the input DA stage layout block. From the figure, it is clear that, output signal voltage of this stage is v_1 = 55.34 V, whereas, the theoretical value was 56 V from equation (2.3) in section 2.3, chapter 2.

3.9.3 Layout of intermediate stages

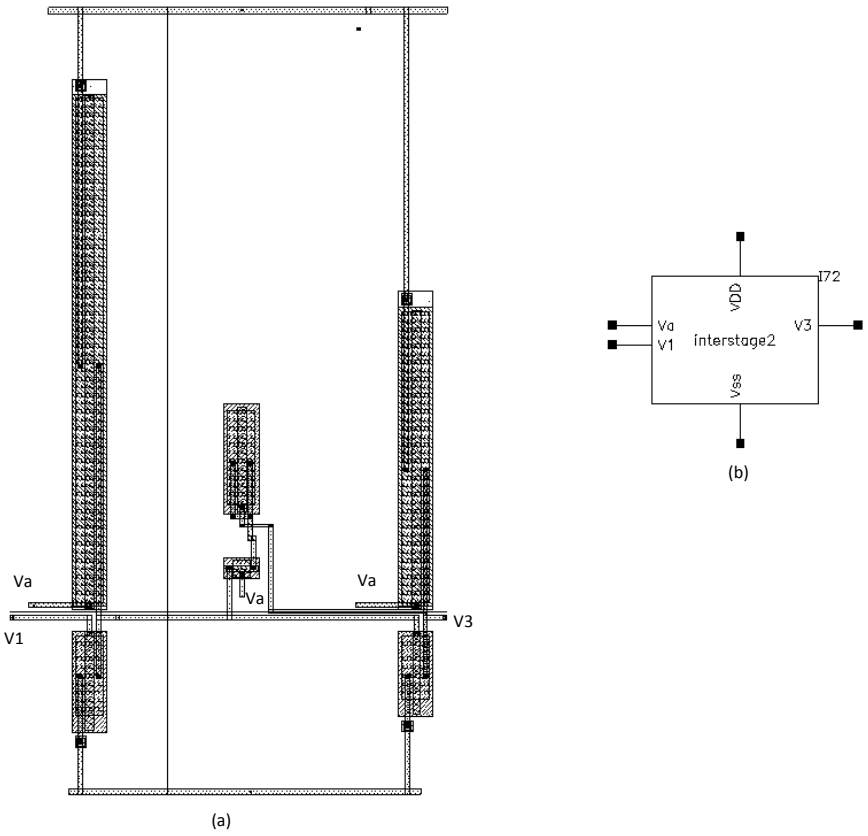

Figure 3.23: (a) Layout of the intermediate stages; (b) Test block of the intermediate stages

Figures 3.23(a) & (b) show respectively the layout of the intermediate stages and the test block for simulations. In the figure, v_1 = Output from input DA stage, V_a = 691 mV, v_3 = Output of the intermediate stages. Figure 3.24 shows the simulated output of the intermediate stage comprising transistors M13 & M15; whereas, figure 3.25 shows the simulated output of the intermediate

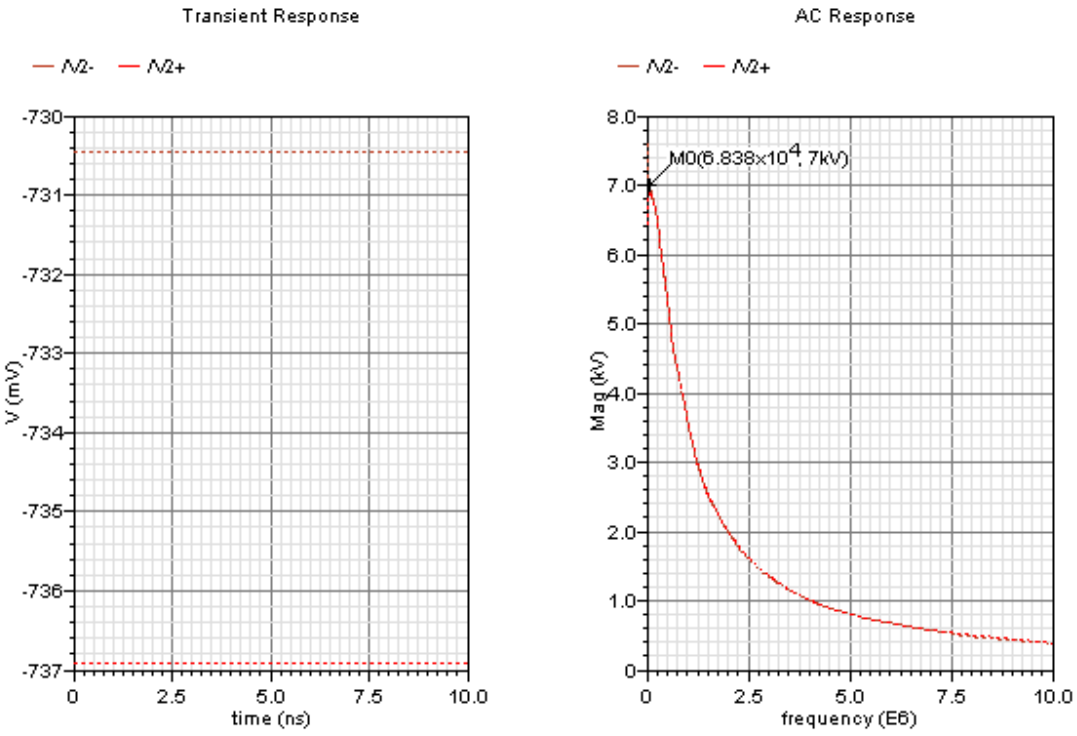

Figure 3.24: Simulated output of the intermediate stage comprising transistors M13 & M15

stage comprising transistors M17 & M23. From the figure, it is observed that, gain of the intermediate stage (comprising transistors M13 & M15) is $\frac{v_2}{v_1} = \frac{7K}{55.34} = 126.5$, whereas the theoretical gain from equation (2.4) was 125.11.

On the other hand, gain of the intermediate stage (comprising transistors M17 & M23) is,

$\frac{v_3}{v_2} = \frac{937.54K}{7K} = 133.93$, whereas theoretical gain of this stage from equation (2.5) was 149.

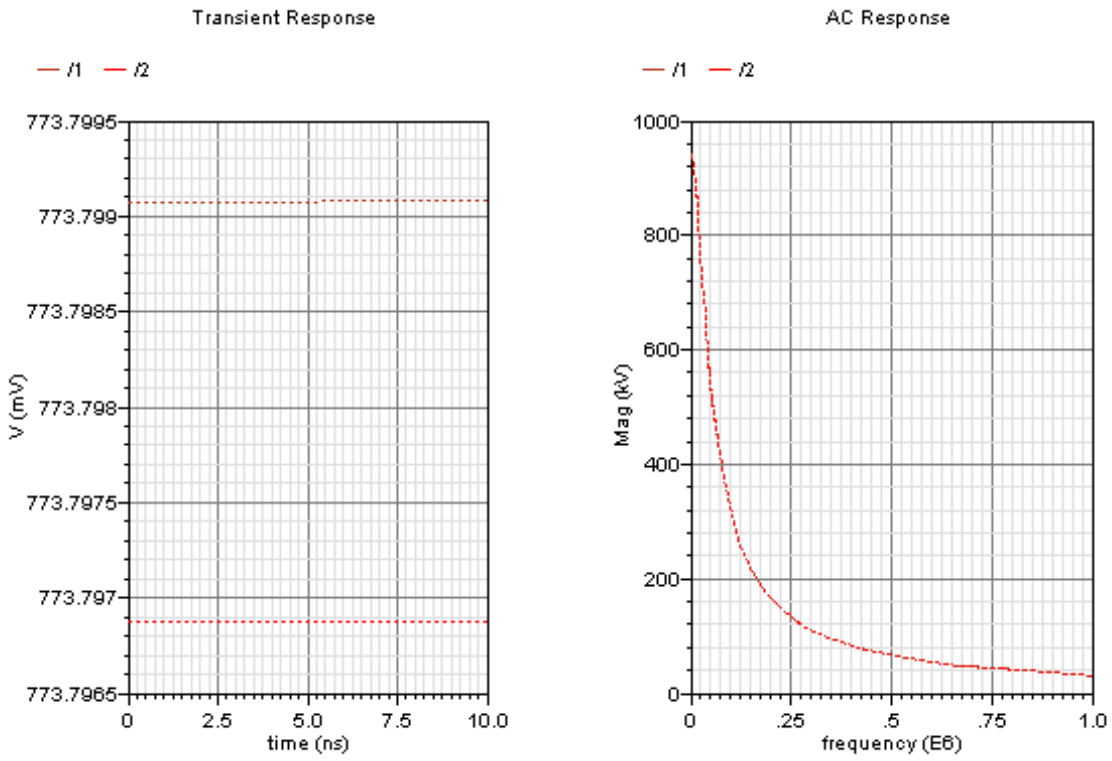

Figure 3.25: Simulated output of the intermediate stage comprising transistors M17 & M23

3.9.4 Layout of voltage buffer stage

Figures 3.26(a) and (b) show respectively the layout of the voltage buffer stage and the test block of the voltage buffer for simulations. Figure 3.27 shows the simulated output of the voltage buffer stage. From the figure, gain of the voltage buffer stage is $\frac{v_o}{v_3} = \frac{790.1K}{937.54K} = 0.84$, whereas theoretical value of the gain from equation (2.8) was 0.73.

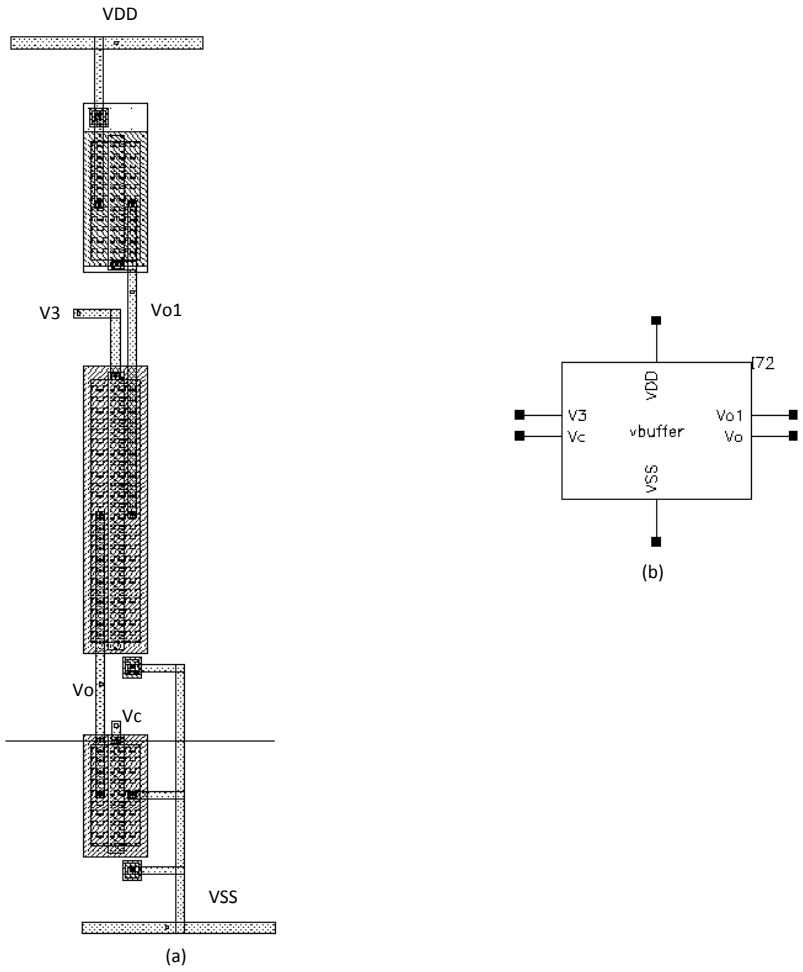

Figure 3.26: (a) Layout of the voltage buffer stage; (b) Test block of the voltage buffer

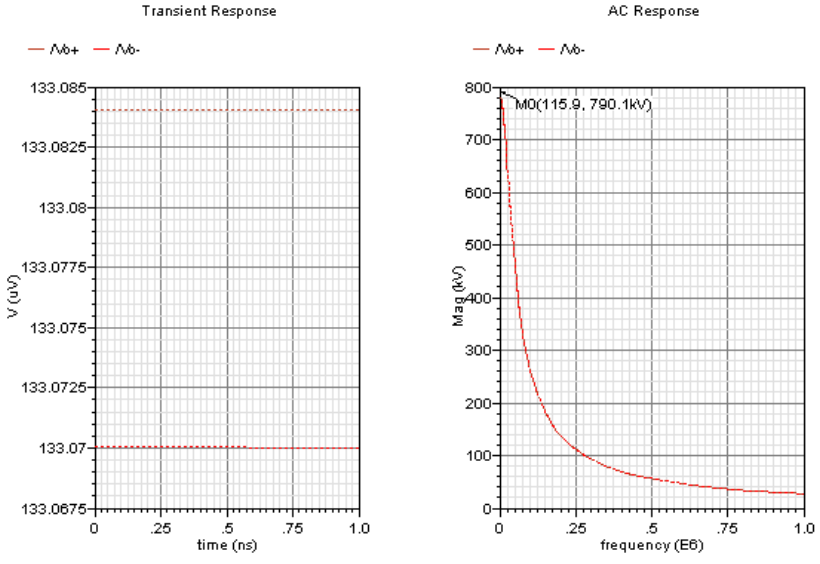

Figure 3.27: Simulated output of the voltage buffer stage

3.9.5 Layout of current buffer stage

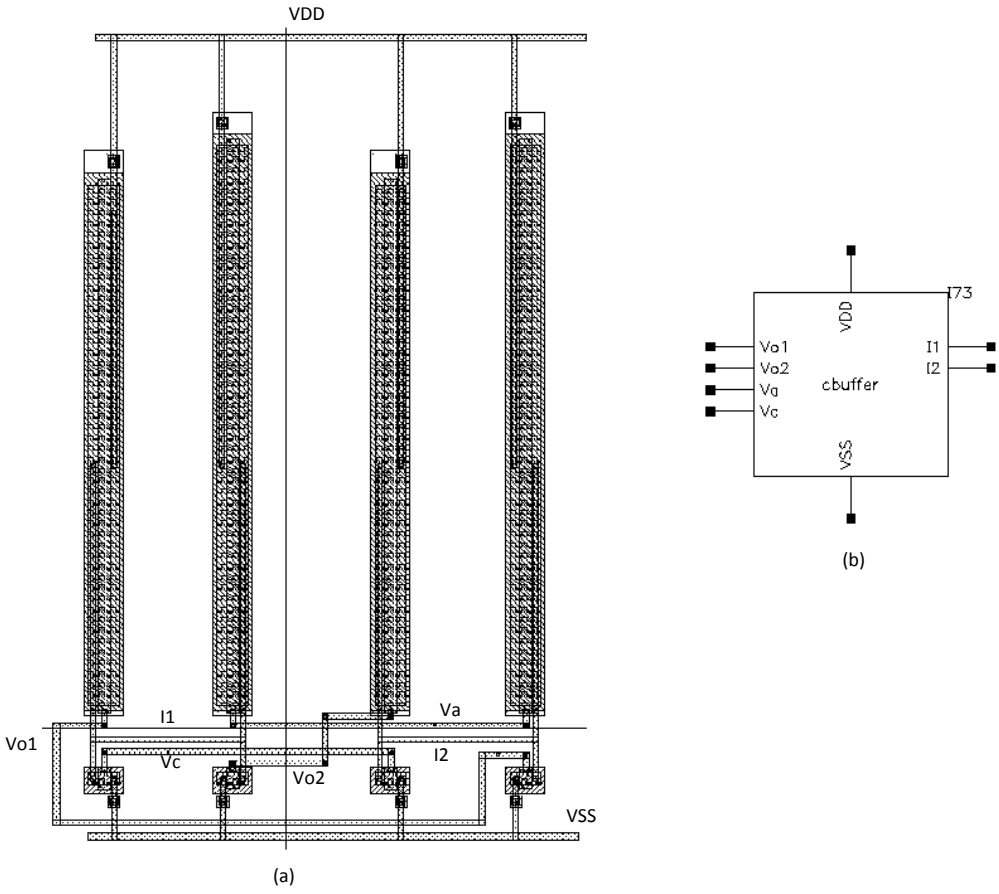

Figure 3.28: (a) Layout of the current buffer stage; (b) Test block of the current buffer

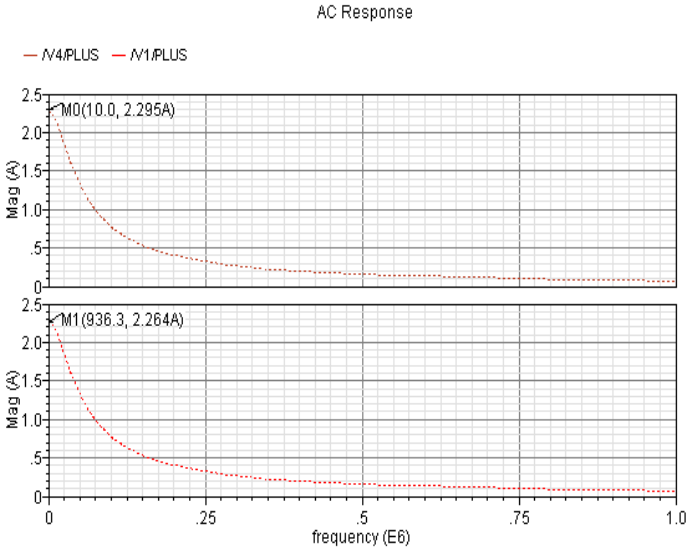

Figure 3.29: Simulated output of the current buffer stage

Figures 3.28(a) & (b) show respectively the layout of the current buffer stage and the test block used for simulations. Output AC current is taken from the i_1, i_2 nodes. Figure 3.29 shows the simulated output of the current buffer stage. From the figure, $i_2 = 2.295 \angle 180^0$ A and $i_1 = 2.264 \angle 0^0$A. Hence output AC current can be calculated as, $i_{out} = i_2 - i_1 = 2.295 \angle 180^0 - 2.264 \angle 0^0 = -2.295 - 2.264 = -4.56$ A, whereas, theoretical value from equation (2.11) was $i_{out} = -4.54$ A.

3.10 Summary

In this chapter, necessary simulation results pertaining to the operations of the UAM as the four categories of basic amplifiers (i.e., VCVS, VCCS, CCVS and CCCS) are presented. The performance parameters are measured by SPICE simulations. The layout has been implemented using 0.18 um CMOS (CMOSP18/TSMC) process. It is now necessary to show the utility of the UAM by implementing different analog electronic circuits. In the next chapter, several signal processing cases are presented with the UAM as the active device building block.

CHAPTER 4

APPLICATION CASES OF THE UAM

4.1 Introduction

This chapter presents several signal processing application cases with the UAM as the active device building block. Some traditional amplifier circuits, such as, inverting amplifier, non-inverting amplifier, ideal integrator, lossy integrator etc. are implemented using the UAM. Further, voltage mode 2nd order band pass filters and current mode filters using the principles of transposed network [37] with the UAM as the active device are illustrated.

4.2 Inverting amplifier implementation

The most basic application of an OP-AMP (as a VCVS) is in realizing an inverting voltage amplifier. This configuration uses negative feedback to stabilize the voltage gain [34]. Due to the negative feedback, the output voltage is 180^0 out of phase with the input. Hence this amount is subtracted from the input voltage and gain is reduced. Formula for the inverting amplifier is:

$$V_{out} = -\frac{R_f}{R_i} V_{in} \Rightarrow \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_i} \Rightarrow A_v = -\frac{R_f}{R_i} \tag{4.1}$$

Figure 4.1 shows the configuration of inverting amplifier implementation using the UAM. The simulations were done for inverting gain of -1 (R_i = 1 KΩ, R_f = 1 KΩ) and -10 (R_i = 1 KΩ, R_f = 10 KΩ).

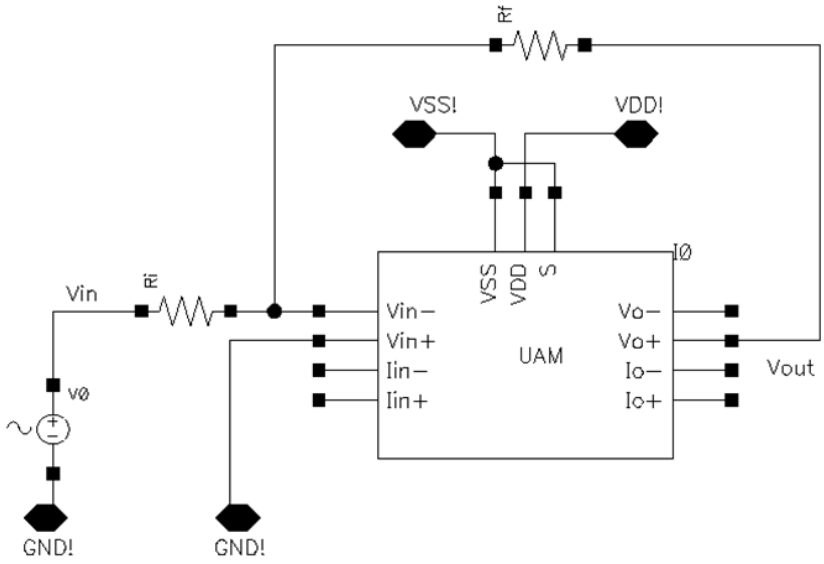

Figure 4.1: Inverting amplifier implementation using the UAM

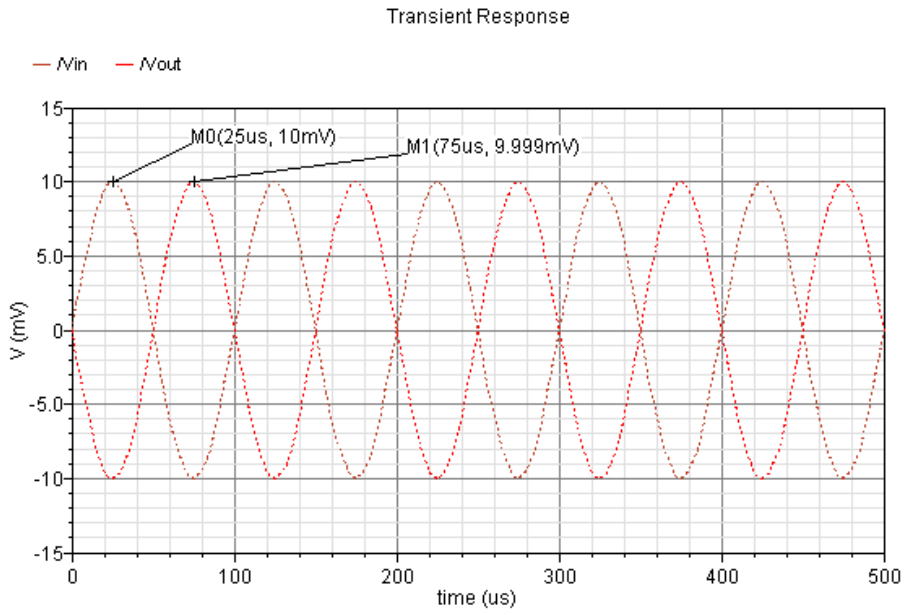

Figure 4.2: Output of the inverting amplifier for gain of -1 (R_i = 1 KΩ, R_f = 1 KΩ)

Figure 4.2 shows the output of the inverting amplifier for the gain of -1. From the simulated output, V_{out} = 9.999 mV and V_{in} = 10 mV. Hence, gain, A_v = - 9.999/10 = -0.9999 ≈ -1.

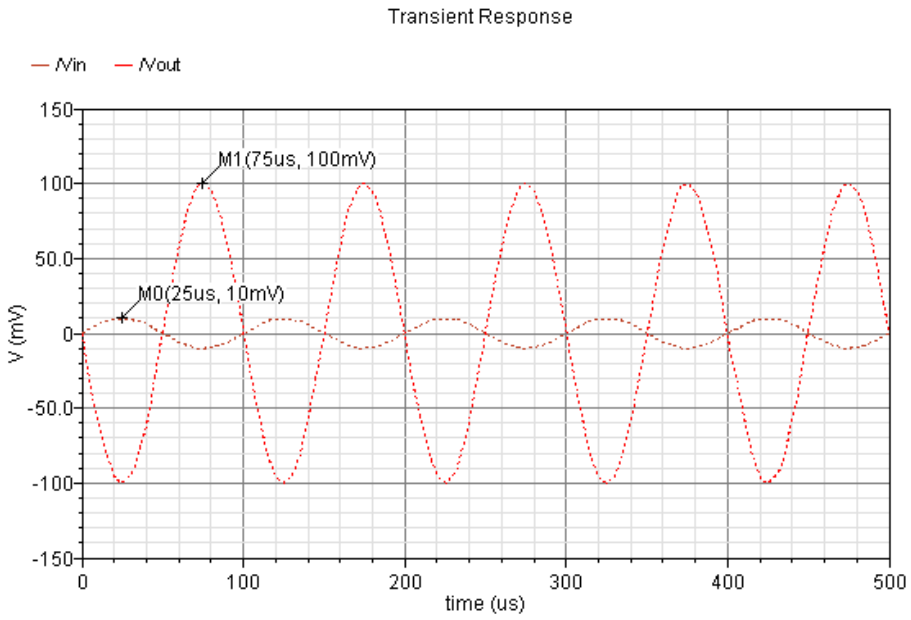

Figure 4.3: Output of the inverting amplifier for gain of -10 (R_i = 1 KΩ, R_f = 10 KΩ)

Figure 4.3 shows the output of the inverting amplifier for gain of -10. From the simulated output it is shown that, V_{out} = 100 mV and V_{in} = 10 mV. Hence, gain, A_v = -100/10 = -10.

4.3 Non-inverting amplifier implementation

In a non-inverting amplifier, the input signal is applied at the positive input terminal of the OP-AMP (as VCVS) and the circuit provides a gain greater than unity. Further, the output voltage signal remains in phase with the input voltage signal, hence, the name non-inverting. The Output voltage and the gain of a non-inverting amplifier can be written as:

$$V_{out} = \left(1 + \frac{R_f}{R_i}\right) V_{in} \Rightarrow \frac{V_{out}}{V_{in}} = \left(1 + \frac{R_f}{R_i}\right) \Rightarrow A_v = \left(1 + \frac{R_f}{R_i}\right) \quad (4.2)$$

Figure 4.4 shows the configuration of non-inverting amplifier implementation using the UAM. Simulations were done for gain of +5 (R_i = 1 KΩ, R_f = 4 KΩ) and +10 (R_i = 1 KΩ, R_f = 9 KΩ).

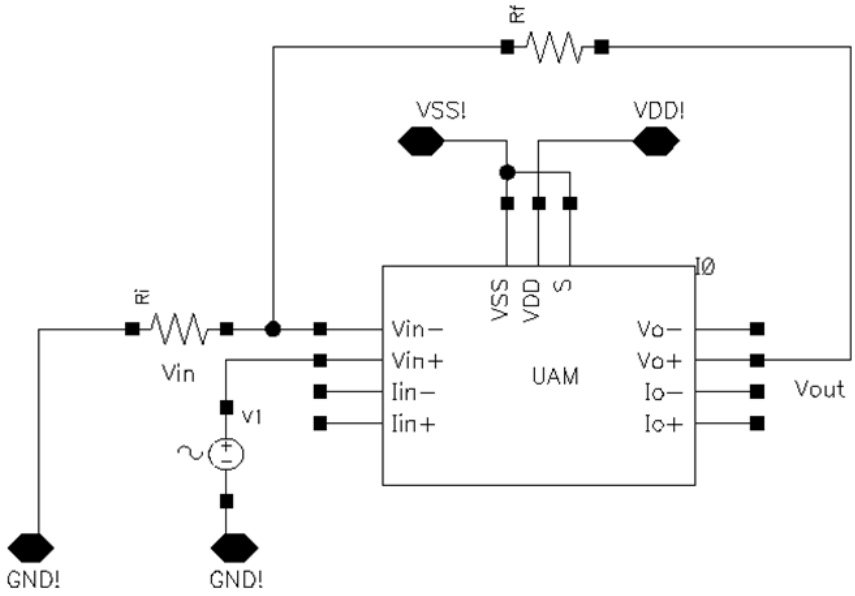

Figure 4.4: Non-inverting amplifier implementation using the UAM

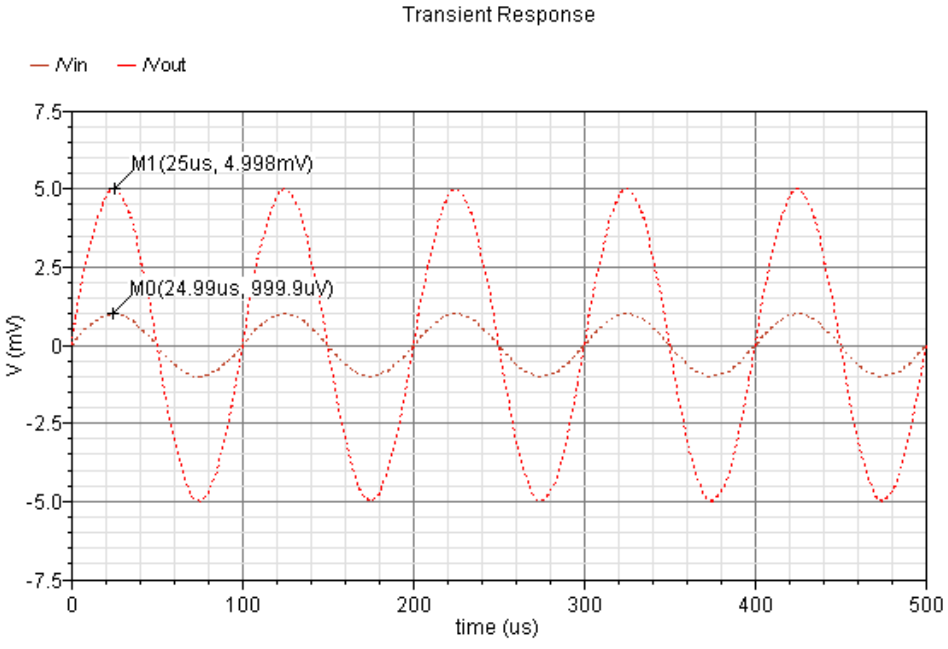

Figure 4.5: Output of the non-inverting amplifier for gain of +5 (R_i = 1 KΩ, R_f = 4 KΩ)

Figure 4.5 shows the output of the non-inverting amplifier for the gain of +5. From the simulated output it is observed that, V_{out} = 4.998 mV and V_{in} = 0.9999 mV. Hence, gain, A_v = 4.998/0.9999 = 4.998 ≈ 5.

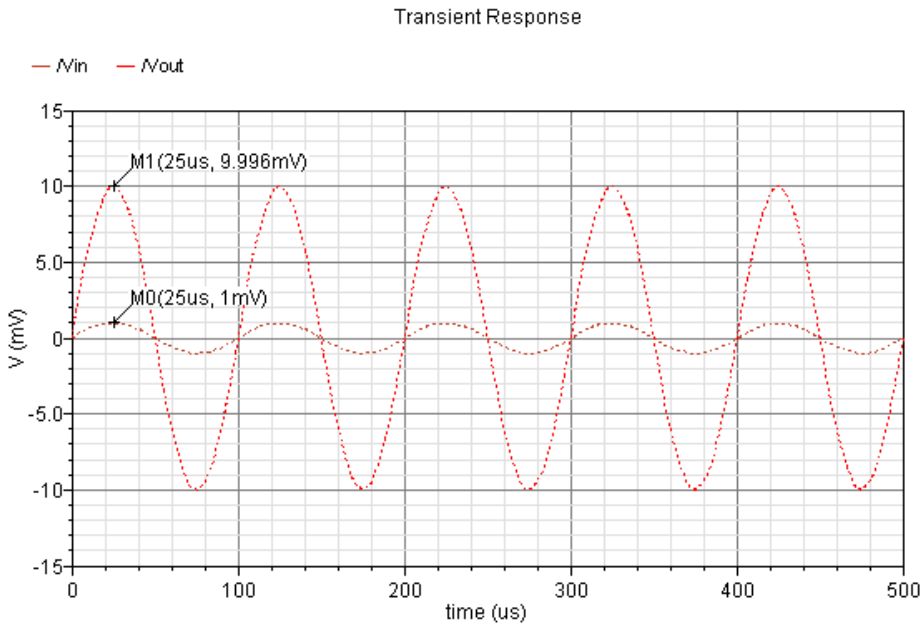

Figure 4.6: Output of the non-inverting amplifier for gain of +10 (R_i = 1 KΩ, R_f = 9 KΩ)

Figure 4.6 shows the output of the non-inverting amplifier for gain of +10. From the simulated output it is observed that, V_{out} = 9.996 mV and V_{in} = 1 mV. Hence, gain, A_v = 9.996/1 = 9.996 ≈10.

4.4 Voltage follower (unity gain buffer) implementation

This is a special type of non-inverting amplifier configuration which provides output voltage that is identical to the input voltage. Hence, it can be used for isolation purpose. In case of voltage follower, equation of output voltage can be written as:

$$V_{out} = V_{in} \tag{4.3}$$

Figure 4.7 shows the set-up for voltage follower implementation using the UAM. Figure 4.8 shows the simulated output of the voltage follower. From the figure it is seen that, for an input voltage, V_{in} = 1 mV, the output voltage is V_{out} = 0.9996 mV ≈ 1 mV ≈ Vin.

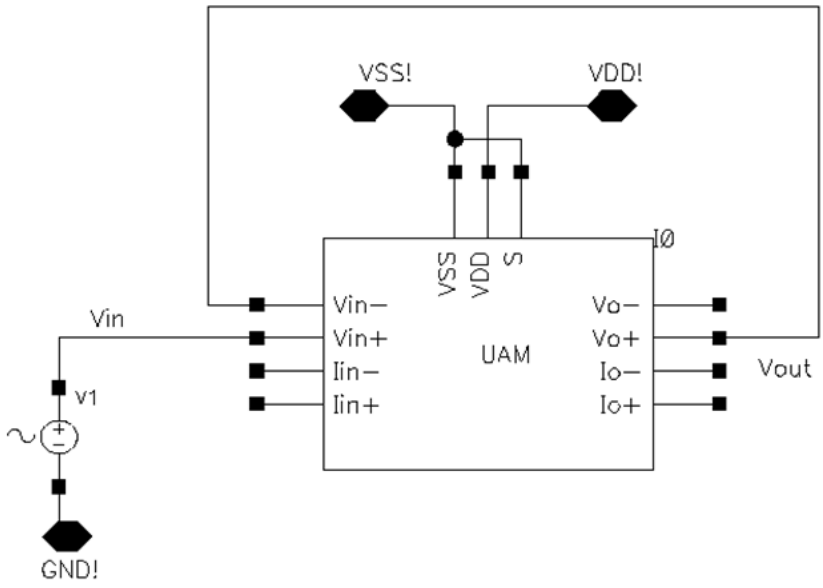

Figure 4.7: Voltage follower implementation using UAM

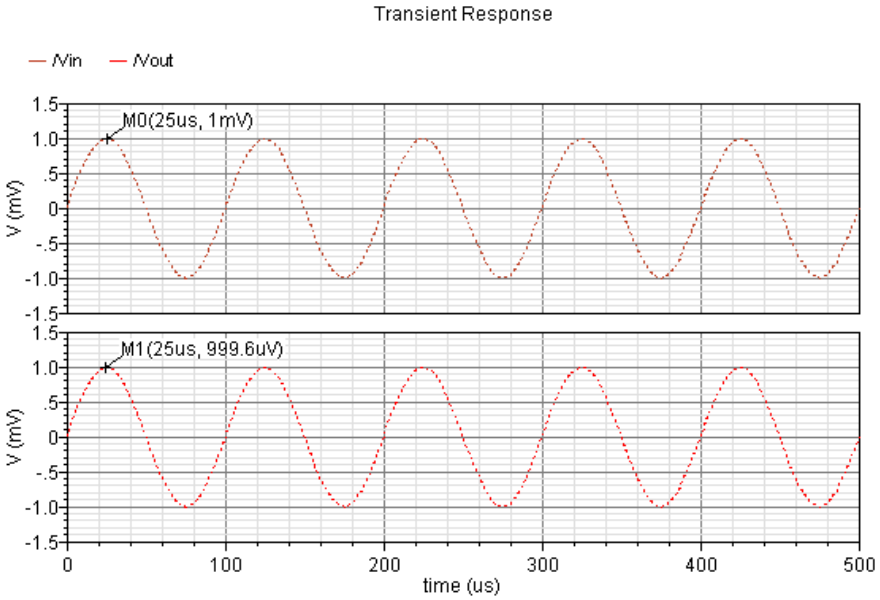

Figure 4.8: Simulated output of the voltage follower

4.5 Ideal inverting integrator implementation

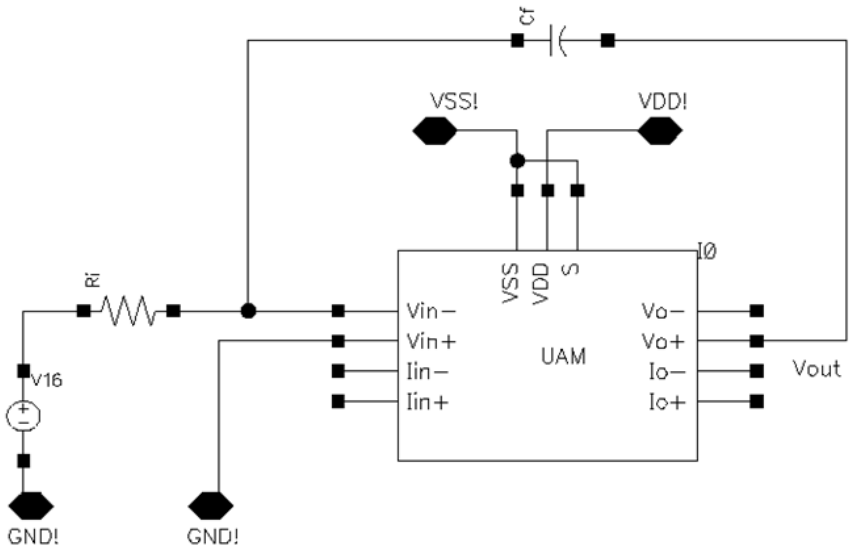

Figure 4.9: Ideal inverting integrator implementation using UAM

Figure 4.9 shows the set-up for implementation of the ideal inverting integrator. R_i and C_f are called the external integrating resistor and capacitor respectively. Frequency domain analysis of the integrator can be done easily and output voltage equation can be written in term of frequency. Output voltage of the integrator is:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-1}{sR_iC_f}$$

where, s = jw and w = angular frequency = $2\pi f$, hence,

$$\frac{V_{out}(jw)}{V_{in}(jw)} = \frac{-1}{jwR_iC_f} \tag{4.4}$$

Therefore, the magnitude and phase response of an ideal integrator can be written as:

$$\text{Magnitude: } \left|\frac{V_{out}}{V_{in}}\right| = \frac{1}{jwR_iC_f} \text{ and phase: } \omega = 180^0 - 90^0 = 90^0 \text{ constant} \tag{4.5}$$

In this design, R_i = 10 KΩ and C_f = 10 nF are used. Hence, expected value of the magnitude @10 Hz is = $\frac{1}{2\pi.10.10K.10n}$ = 159.155 ≈ 44 dB. Figure 4.10 shows the magnitude response of the integrator. From the figure it is observed that, magnitude @10 Hz is = 43.93 dB ≈ 44 dB. Also figure 4.11 shows that phase of the integrator is 90^0.

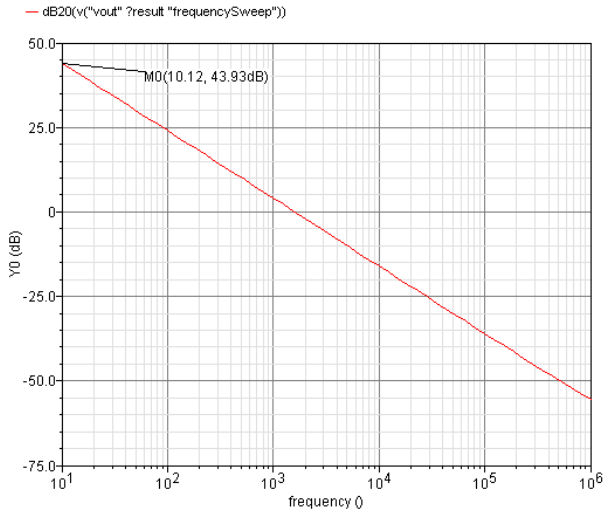

Figure 4.10: Magnitude response of the inverting integrator

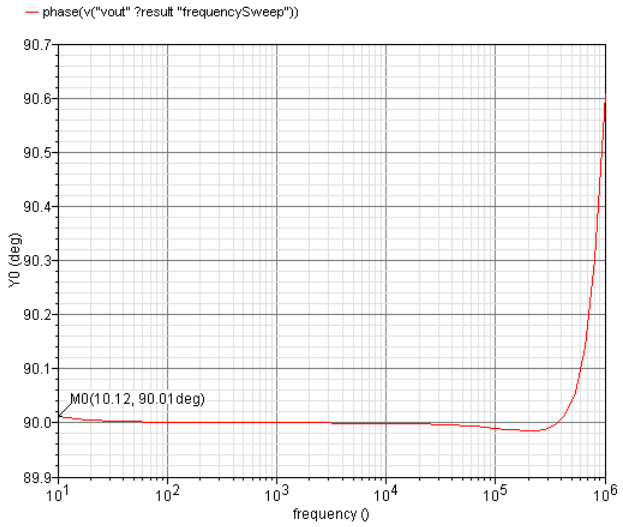

Figure 4.11: Phase response of the inverting integrator

4.6 Lossy integrator implementation

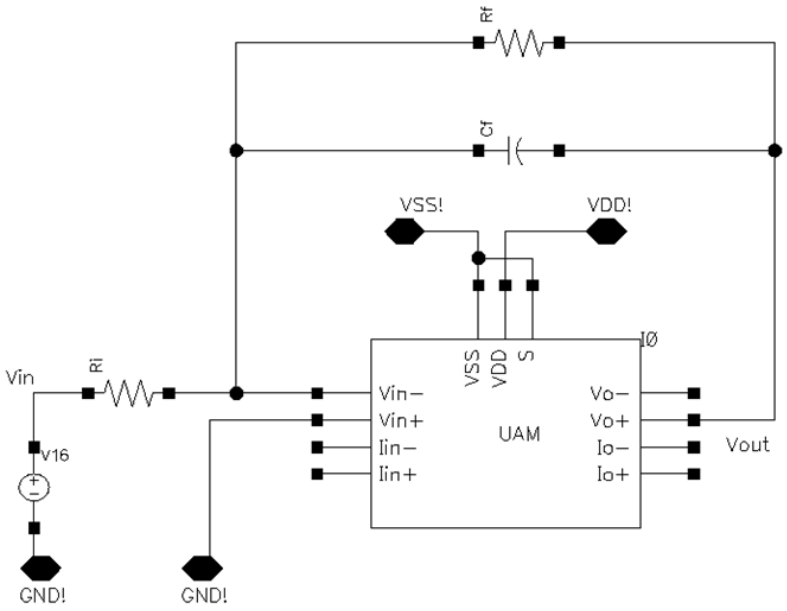

Figure 4.12: Lossy integrator implementation using UAM

Figure 4.12 shows the configuration for lossy integrator implementation. The transfer function of a lossy integrator can be written as:

$$\frac{V_{out}(s)}{V_{in}(s)} = -\left(\frac{R_f}{R_i}\right)\frac{1}{1+sR_fC_f}$$

where, s = jw and w = angular frequency = 2πf, hence,

$$\frac{V_{out}(jw)}{V_{in}(jw)} = -\left(\frac{R_f}{R_i}\right)\frac{1}{1+jwR_fC_f} \quad (4.6)$$

In this design, R_i = 1 KΩ, R_f = 10 KΩ and C_f = 10 nF are used. Hence from above equation, expected value of magnitude of the lossy integrator @10 Hz is = $\left(\frac{10K}{1K}\right)\left(\frac{1}{1+2\pi.10.10K.10n}\right)$ = 9.94 ≈ 19.95 dB ≈ 20 dB. Figure 4.13 and 4.14 show the magnitude and phase response of the

lossy integrator implementation using the UAM as in figure 4.12. From the figures, it is observed that, magnitude @10 Hz is 20 dB and phase ≈ 180^0.

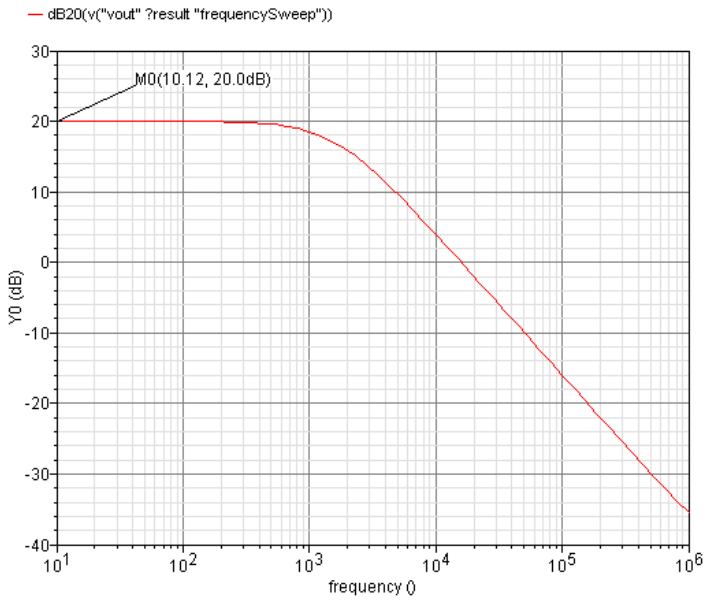

Figure 4.13: Magnitude response of the lossy integrator

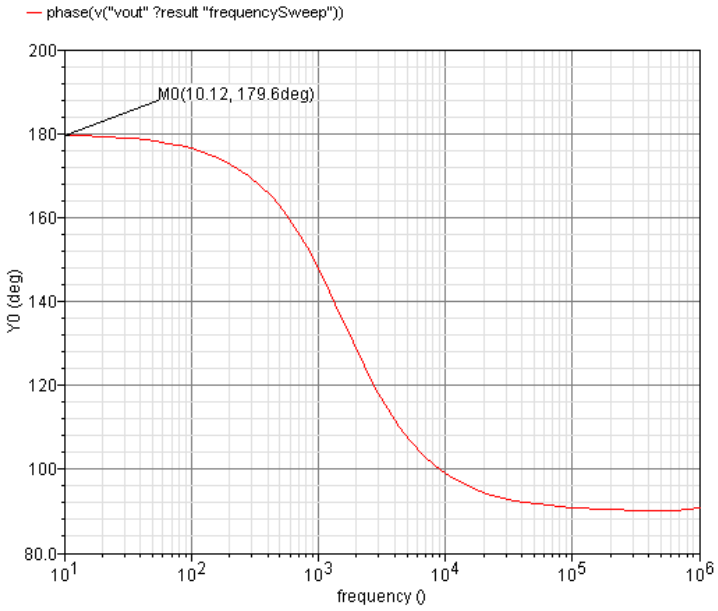

Figure 4.14: Phase response of the lossy integrator

4.7 Current conveyor (CCII) realization using UAM

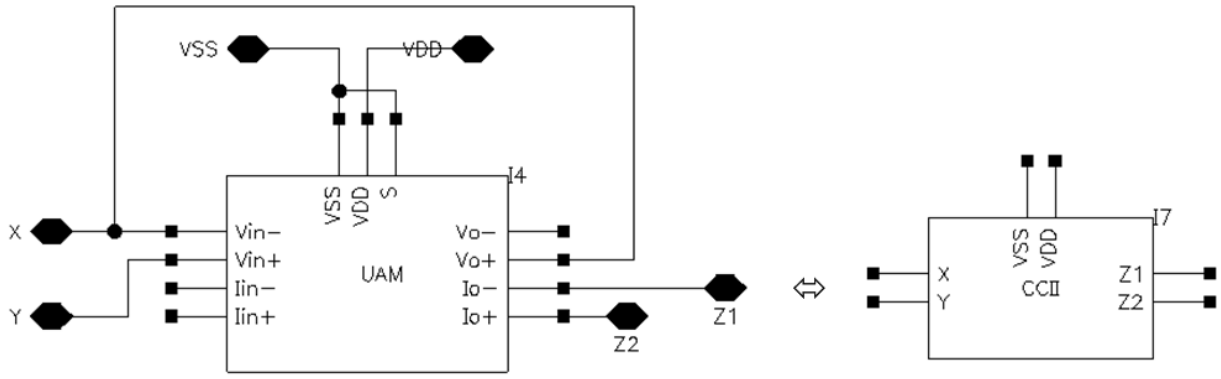

Figure 4.15: CCII implementation using UAM

Figure 4.15 shows the current conveyor (CCII) realization using the UAM. The UAM is operating in VCVS mode (S = 0) and connected in negative feedback configuration [35]. As the UAM already has the output current buffer stage which can provide two differential output currents opposite in phase, above implementation of the UAM can provide both CCII+ and CCII- at the same time.

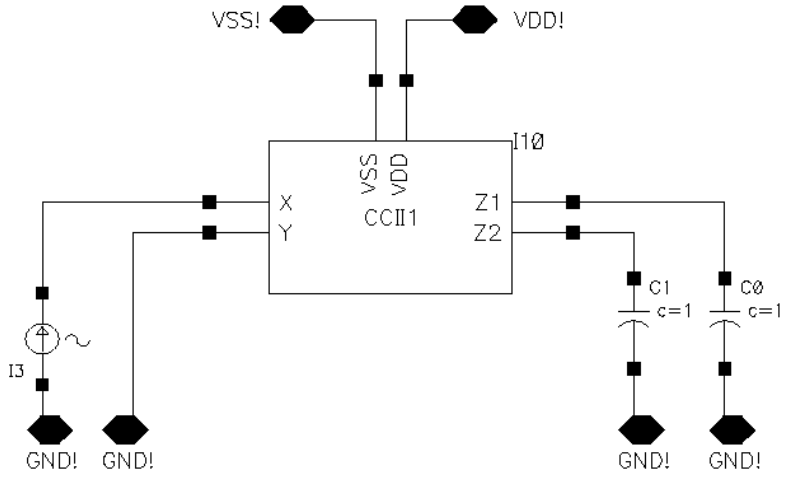

Figure 4.16: CCII simulation set-up

Figure 4.16 shows the set-up for CCII implementation using the UAM. An AC current signal, I_{in} = 1 A is applied at X terminal. The output directly shows the current gain of the CCII. Figure 4.17 shows the simulated output of the CCII where gain of CCII is 22.5 dB. In this case, gain is decreased in comparison with CCCS. This is because the UAM is configured as OP-AMP with feedback from VCVS output to DA input. Hence, buffer voltage is lowered due to decreased level of resistance which produces lower current at the current buffer output stage with compare to CCCS configuration.

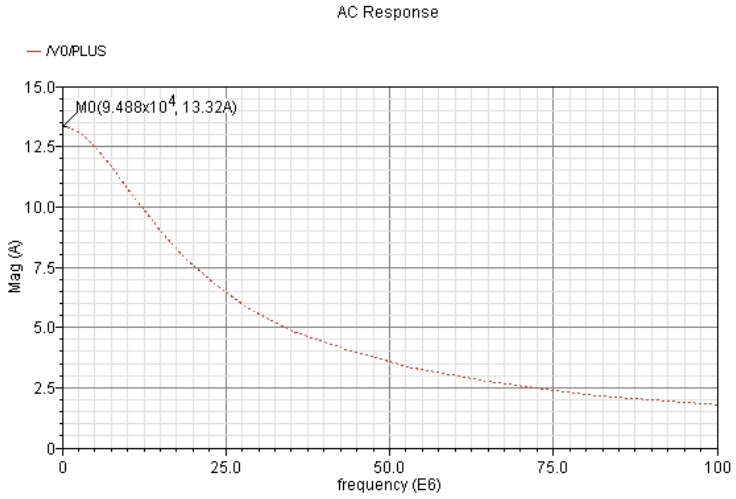

Figure 4.17: Simulated output of the CCII

4.8 Voltage-mode filter (VMF) implementation using three UAM

The proposed Universal Amplifier Module (UAM) was used to implement voltage mode Ackerberg and Mossberg (A & M) 2nd order band pass filter [APPENDIX – A]. The band pass transfer function of the A & M filter can be written as [37]:

$$\frac{V_{o1}}{V_i} = -\frac{s/RC_1}{s^2 + s\frac{1}{R_1C_1} + \frac{r_1}{C_1C_2R_2rr_2}} \qquad (4.7)$$

Comparing equation (4.7) with the standard second order band pass filter transfer function [68]:

$$H(s) = \frac{N(s)}{D(s)} = H_0 \frac{s^2 + (\frac{\omega_z}{Q_z})s + \omega^2{}_z}{s^2 + (\frac{\omega_p}{Q_p})s + \omega^2{}_p} \tag{4.8}$$

we can find:

$$\frac{\omega_p}{Q_p} = \frac{1}{R_1 C_1}$$

Hence, C_1 can be calculated as:

$$C_1 = \frac{Q_p}{\omega_p R_1} = \frac{Q_p}{2\pi f_p R_1} \tag{4.9}$$

$$\text{and, } \omega^2{}_p = \frac{r_1}{C_1 C_2 r r_2 R_2}$$

Hence, C_2 can be calculated as:

$$C_2 = \frac{r_1}{\omega^2{}_p C_1 r r_2 R_2} = \frac{r_1}{(2\pi f_p)^2 C_1 r r_2 R_2} \tag{4.10}$$

Figure 4.18 shows the voltage-mode band pass filter implementation using the UAM.

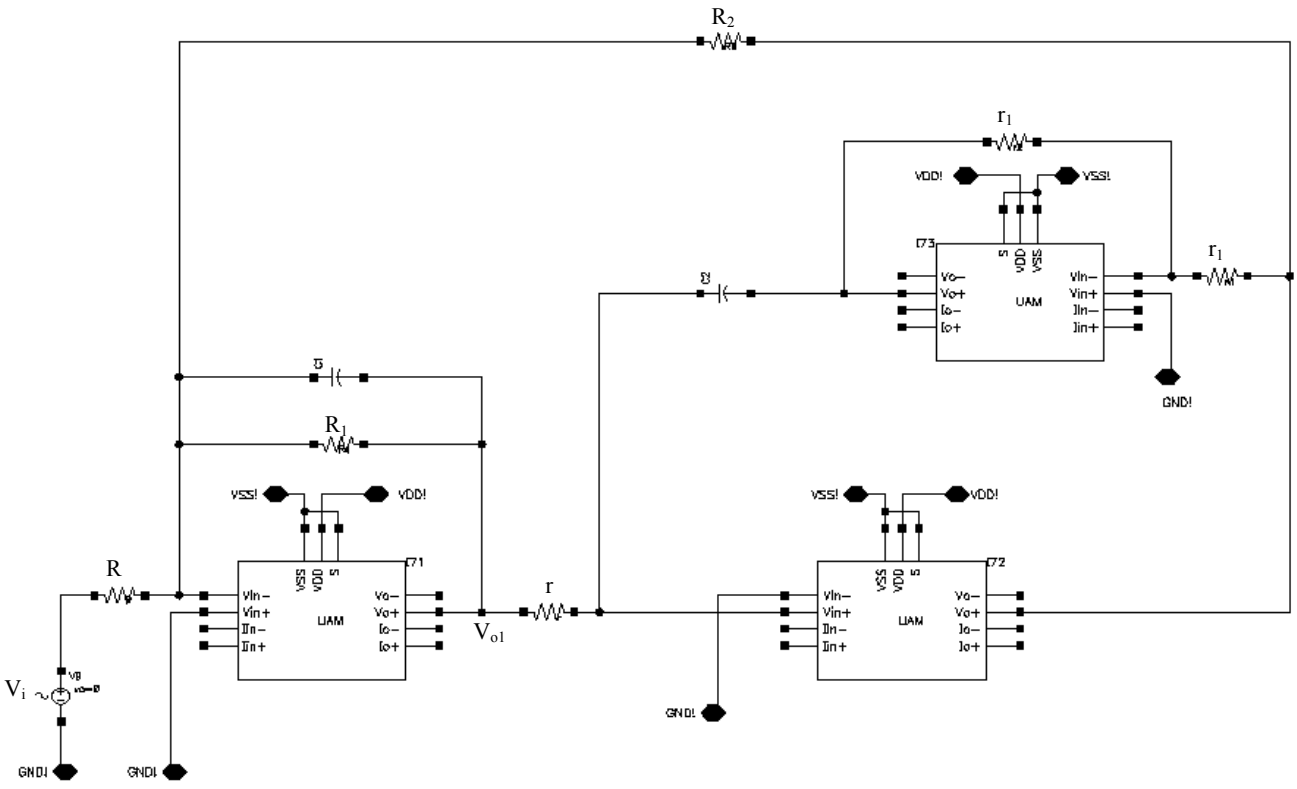

Figure 4.18: Voltage-mode BPF implementation using UAM

Choosing f_p = 10 KHz, Q_p = 2.5, r = r_1 = r_2 = R_1 = R_2 = 1 KΩ.

From equation (4.9) & (4.10), C_1 = 39.7887 nF and C_2 = 6.3662 nF.

Figure 4.19 shows the frequency response of the VMF implementation for f_p = 10 KHz. From the figure it is observed that, center frequency, f_p = 10 KHz which is exactly the same as the designed value of f_p.

Also, $Q_p = \frac{f_p}{\Delta f} = \frac{10K}{12.17K - 8.208K} = \frac{10K}{3.962K} = 2.5$, which is exactly same as the chosen value of Q_p.

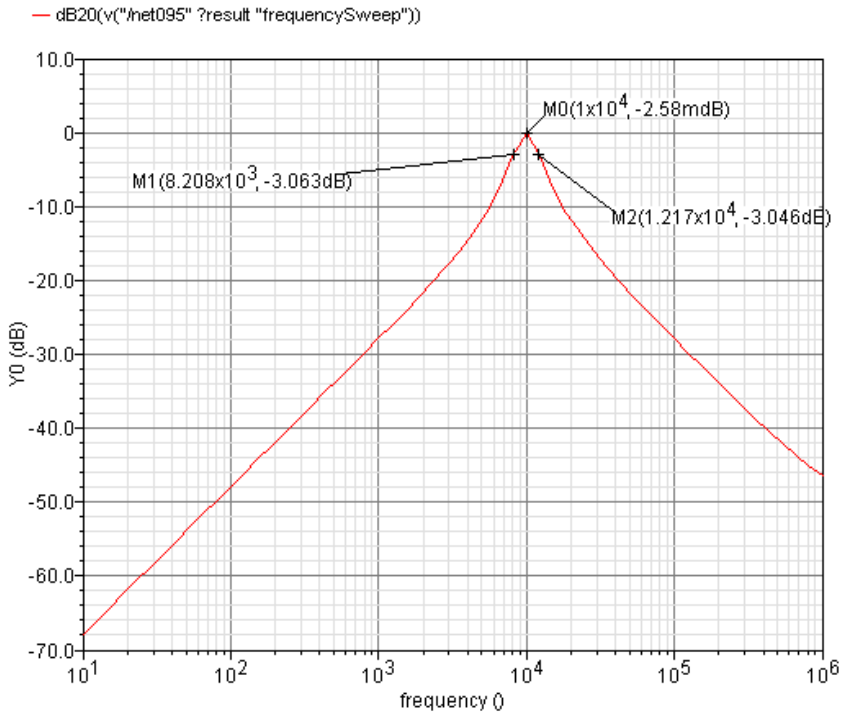

Figure 4.19: Frequency response of the VMF for f_p = 10 KHz

Figure 4.20 shows the frequency response of the VMF for f_p = 1 MHz.

Choosing, $Q_p = 2.5$, $r = r_1 = r_2 = R_1 = R_2 = 1$ KΩ.

From equation (4.9) & (4.10), $C_1 = 0.397887$ nF and $C_2 = 63.662$ pF.

From figure 4.20 it is observed that, center frequency, f_p = 1 MHz which is exactly same as the designed value of f_p.

Also, $Q_p = \frac{f_p}{\Delta f} = \frac{1M}{1.21M - 0.8246M} = \frac{1M}{0.3854M} = 2.59$, which is almost same as the designed value of Q_p.

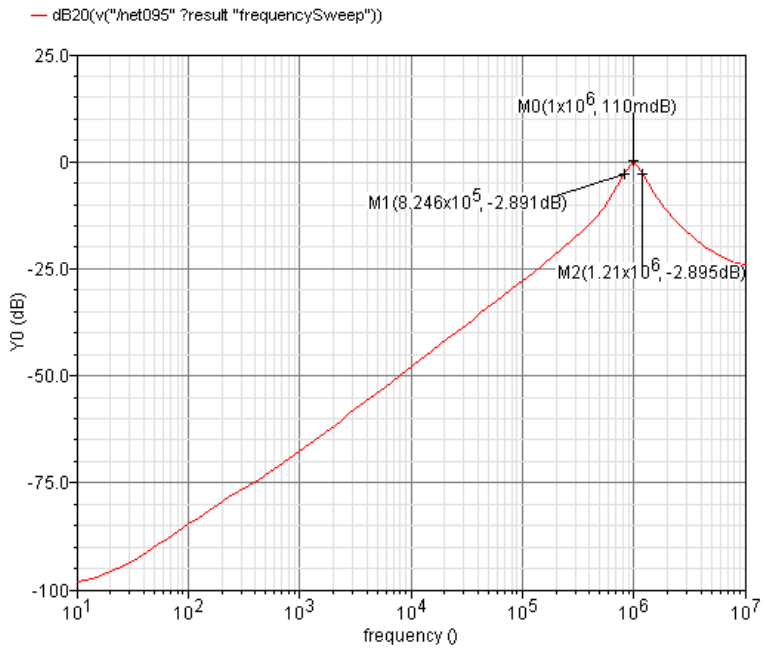

Figure 4.20: Frequency response of the VMF for f_p = 1 MHz

4.9 Transconductance filter (TCF) implementation using three UAM

Figure 4.21 shows the implementation of transconductance-mode band pass filter which is obtained from the voltage mode A & M 2nd order band pass filter of section 4.8. In this case, the voltage signal is applied at the voltage input terminal and the output current signal is measured from the output current buffer stage. Hence the filter may provide transconductance transfer function as:

$$\frac{I_o}{V_i} = -\frac{s/RC_1}{s^2 + s\frac{1}{R_1C_1} + \frac{r_1}{C_1C_2R_2rr_2}} \tag{4.11}$$

Comparing equation (4.11) with standard 2nd order BPF transfer function of equation (4.8), it is shown that equations (4.9) & (4.10) are valid to calculate the values of C_1 & C_2.

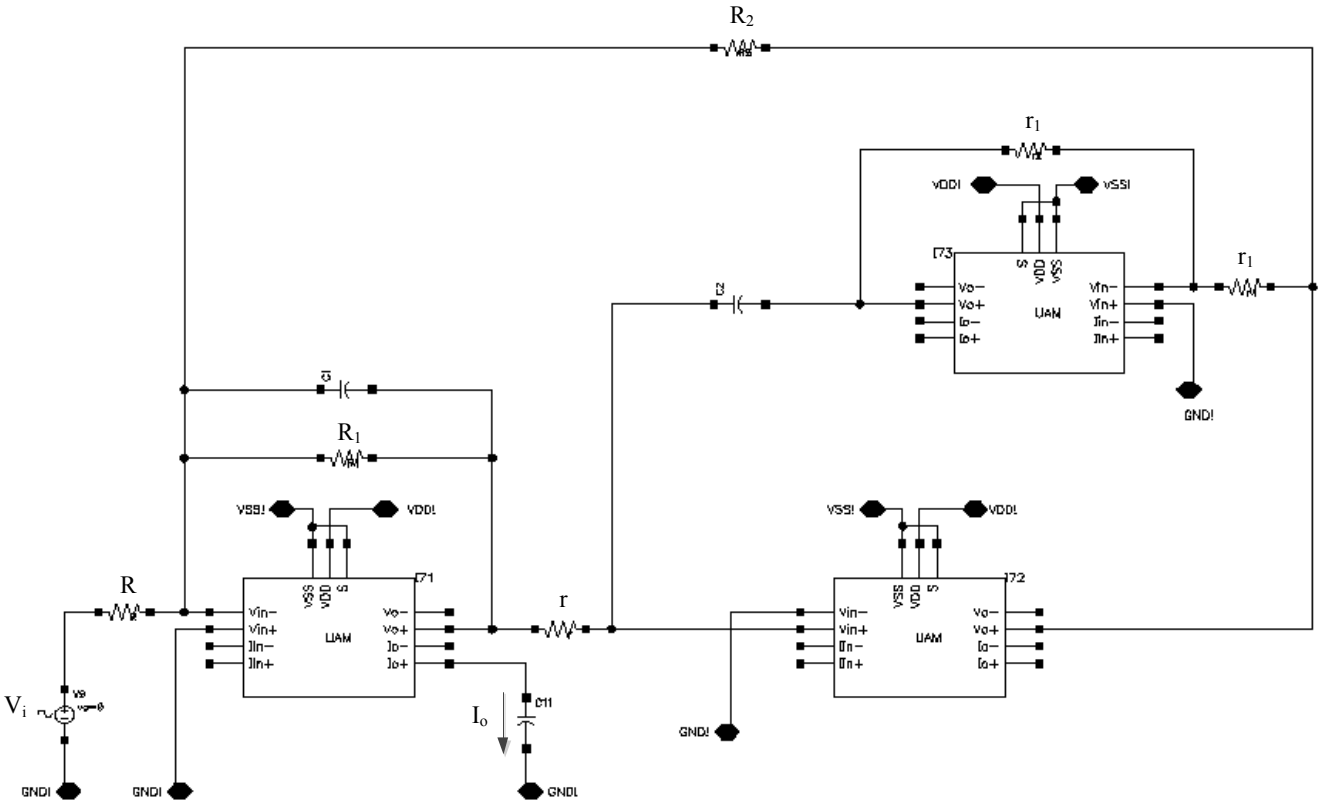

Figure 4.21: Transconductance filter implementation using the UAM

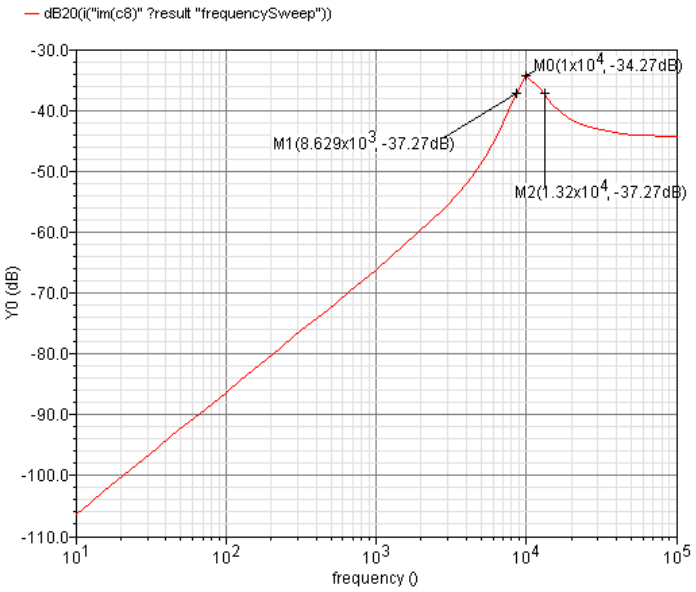

Figure 4.22: Frequency response of the TCF for f_p = 10 KHz

Figure 4.22 shows the frequency response of the TCF for f_p = 10 KHz.

Choosing, Q_p = 2.5, r = r_1 = r_2 = R_1 = R_2 = 1 KΩ.

From equation (4.9) & (4.10), C_1 = 39.7887 nF and C_2 = 6.3662 nF.

From figure 4.22, it is observed that, center frequency, f_p = 10 KHz which is exactly same as the designed value of f_p.

Also, Qp = $\frac{f_p}{\Delta f} = \frac{10K}{13.2K - 8.629K} = \frac{10K}{4.571K}$ = 2.2, which is nearly equal to the chosen value of Q_p.

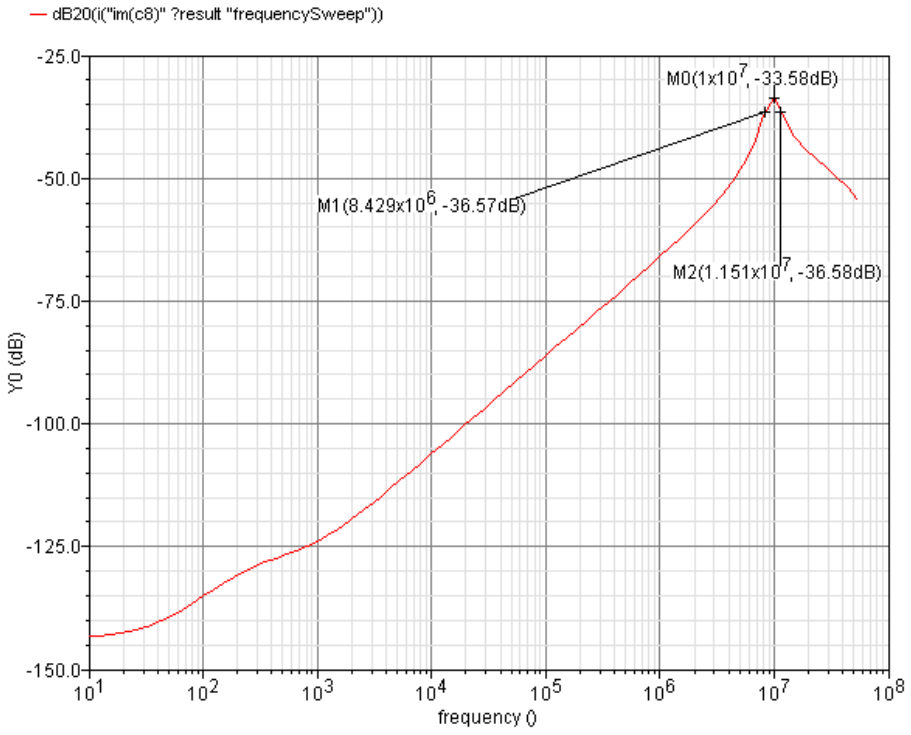

Figure 4.23: Frequency response of the TCF for f_p = 10 MHz

Figure 4.23 shows the frequency response of the TCF for f_p = 10 MHz.

Choosing, Q_p = 2.5, r = r_1 = r_2 = R_1 = R_2 = 1 KΩ.

Using equation (4.9) & (4.10), C_1 = 39.7887 pF and C_2 = 6.3662 pF.

From figure 4.23, it is observed that, center frequency, f_p = 10 MHz which is exactly same as the designed value of f_p.

Again $Q_p = \frac{f_p}{\Delta f} = \frac{10M}{11.51M - 8.429M} = \frac{10M}{3.081M} = 3.2$, which is slightly larger than the designed value of Q_p. The reason is an enhancement of Q_p of the filter when the intended center frequency becomes comparable to the unity gain band-width of the active device (the UAM here) [68].

4.10 Current-mode filter (CMF) implementation using three UAM

Figure 4.24 shows the current-mode A & M filter (CMF) implementation using the UAM. The CMF is obtained directly from the VMF by just reversing the input-output ports of the each VCVS elements in the VMF shown before. This involves application of the principle of transposition [37].

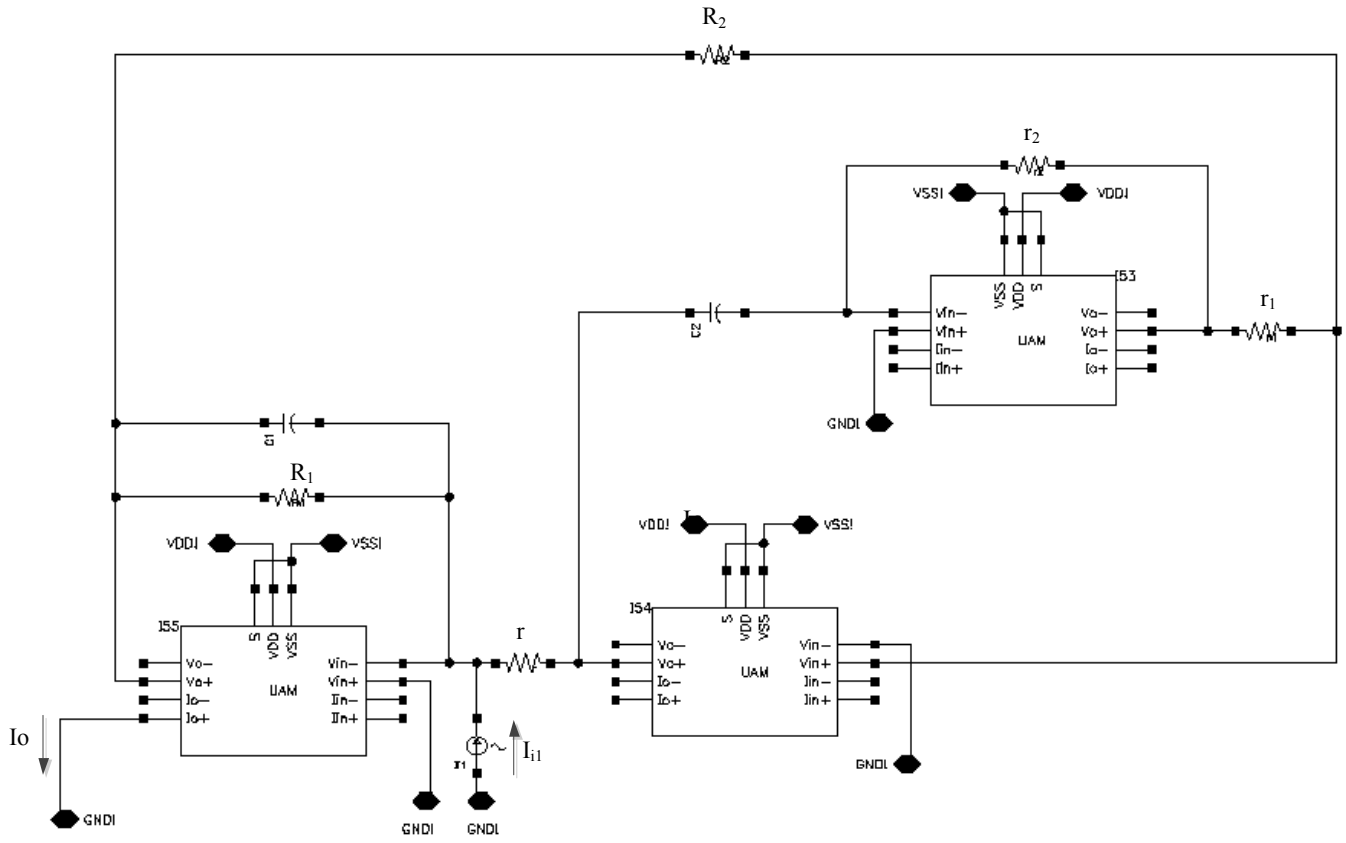

Figure 4.24: Current-mode BPF implementation using UAM

Current transfer function of the CMF as in figure 4.24 can be written as [APPENDIX – A]:

$$\frac{I_o}{I_{i1}} = -\frac{\frac{1}{RC_1}s}{s^2 + \frac{1}{R_1C_1}s + \frac{r_1}{C_1C_2rr_2R_2}} \qquad (4.12)$$

Current mode transfer function of equation (4.12) can be compared with the standard 2nd order filter transfer function of equation (4.8). C_1 and C_2 in this case can also be calculated from equations (4.9) & (4.10). Figure 4.25 shows the frequency response of the CMF for f_p = 10 KHz.

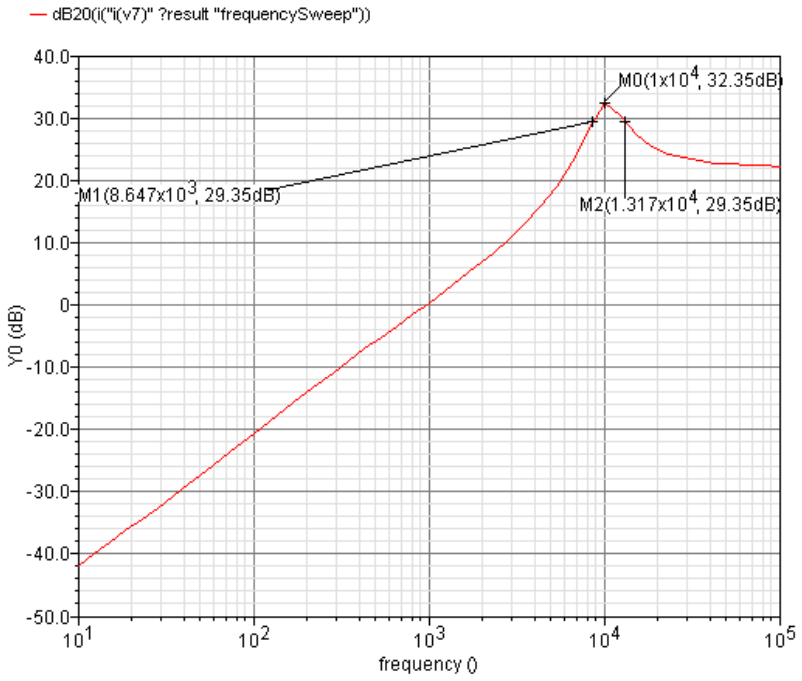

Figure 4.25: Frequency response of the CMF for f_p = 10 KHz

Choosing f_p = 10 KHz, Q_p = 2.5, r = r_1 = r_2 = R_1 = R_2 = 1 KΩ.

From equation (4.9) & (4.10), C_1 = 39.7887 nF and C_2 = 6.3662 nF.

From figure 4.25, it is observed that, center frequency, f_p = 10 KHz which matches with the designed value of 10 KHz.

Also, $Q_p = \frac{f_p}{\Delta f} = \frac{10K}{13.17K - 8.647K} = \frac{10K}{4.523K}$ = 2.2, which is nearly equal to the designed value of Q_p.

Figure 4.26 shows the frequency response of the CMF for f_p = 10 MHz.

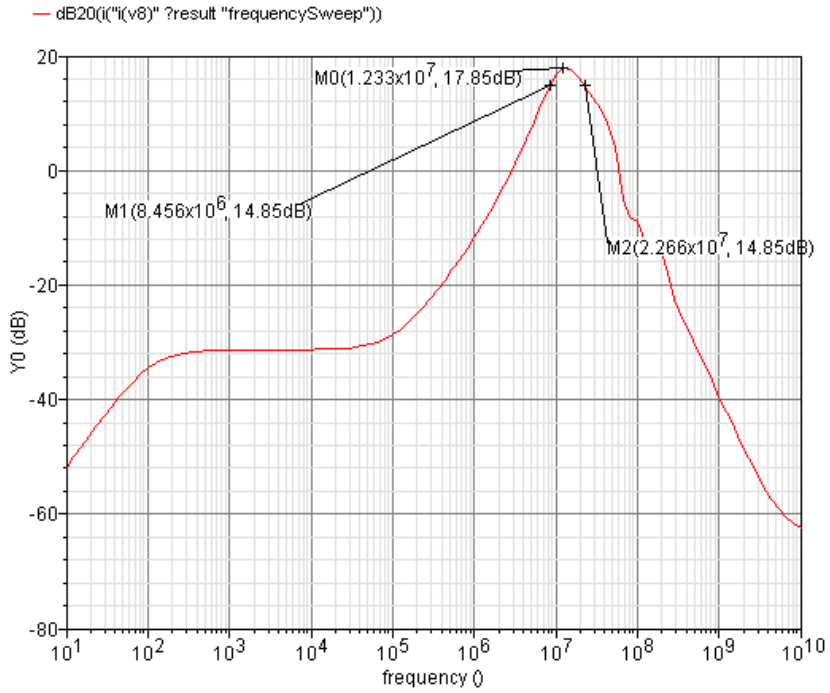

Figure 4.26: Frequency response of the CMF for f_p = 10 MHz

Choosing, $Q_p = 2.5$, $r = r_1 = r_2 = R_1 = R_2 = 1$ KΩ.

From equation (4.9) & (4.10), $C_1 = 39.7887$ pF and $C_2 = 6.3662$ pF.

From figure 4.26, it is observed that, center frequency, $f_p = 12.33$ MHz, which is nearly equal to the designed value of f_p.

Also, $Q_p = \frac{f_p}{\Delta f} = \frac{12.33M}{22.66M - 8.456M} = \frac{12.33M}{14.204M} = 0.9$. The not so ideal response characteristics could be ascribed to the non-ideal performance characteristic of the UAM as a CCCS as opposed to VCVS. This requires further investigation.

4.11 Transresistance filter (TRF) implementation using three UAM

Figure 4.27 shows the transresistance mode band pass filter implementation using the UAM. The same voltage mode to current mode transformation is used of the VCVS device to apply current signal at the input terminal. Final output voltage is taken from the voltage buffer stage.

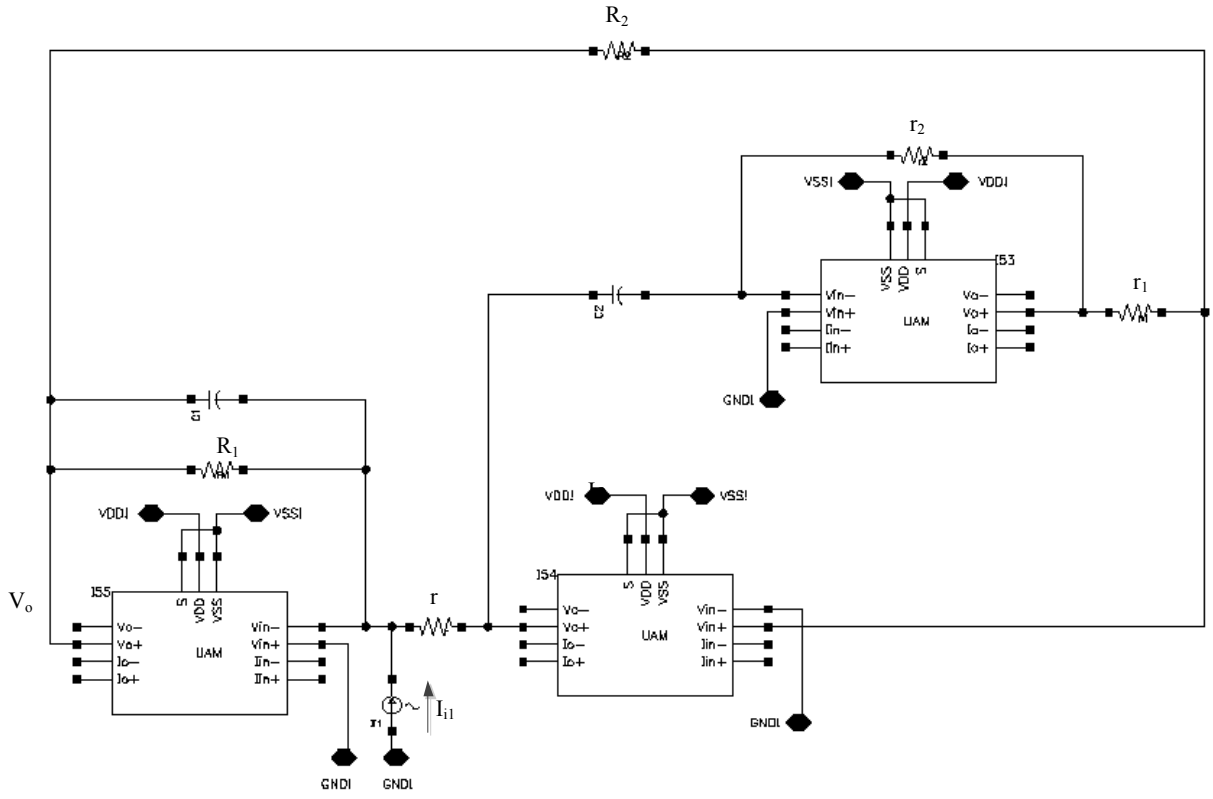

Figure 4.27: Current-mode BPF implementation using UAM

For the transresistance filter (TRF), the transfer function can be written as:

$$\frac{V_o}{I_{i1}} = -\frac{\frac{1}{RC_1}s}{s^2 + \frac{1}{R_1C_1}s + \frac{r_1}{C_1C_2rr_2R_2}} \tag{4.13}$$

Comparing equation (4.13) with the standard 2nd order band pass transfer function:

$$H(s) = \frac{N(s)}{D(s)} = H_0 \frac{s^2 + (\frac{\omega_z}{Q_z})s + \omega^2{}_z}{s^2 + (\frac{\omega_p}{Q_p})s + \omega^2{}_p} \tag{4.14}$$

It can be written that,

$$\frac{\omega_p}{Q_p} = \frac{1}{R_1 C_1}$$

Hence, C_1 can be calculated from the following equation as:

$$C_1 = \frac{Q_p}{\omega_p R_1} = \frac{Q_p}{2\pi f_p R_1} \tag{4.15}$$

$$\text{and, } \omega^2{}_p = \frac{r_1}{C_1 C_2 r r_2 R_2}$$

Hence, C_2 can be calculated from the following equation as:

$$C_2 = \frac{r_1}{\omega^2{}_p C_1 r r_2 R_2} = \frac{r_1}{(2\pi f_p)^2{}_p C_1 r r_2 R_2} \tag{4.16}$$

Figure 4.28 shows the frequency response of the TRF for fp = 1 KHz.

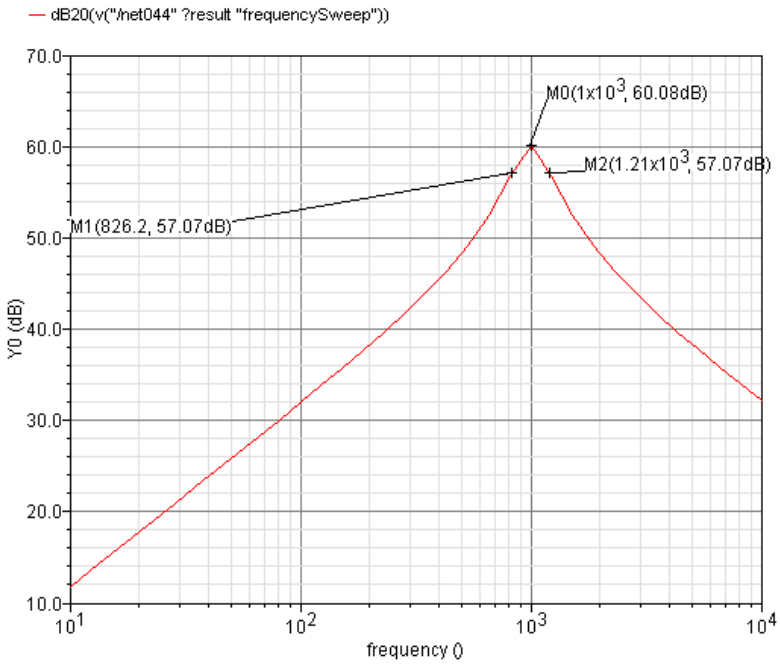

Figure 4.28: Frequency response of the TRF for f_p = 1 KHz

Choosing, $Q_p = 2.5$, $r = r_1 = r_2 = R_1 = R_2 = 1\ K\Omega$.

From equation (4.15) & (4.16), C1 = 397.887 nF and C2 = 63.662 nF.

From figure 4.28, it is observed that, center frequency, f_p = 1 KHz which matches with the designed value of 1 KHz.

Also, $Q_p = \frac{f_p}{\Delta f} = \frac{1K}{1.21K - 0.8262K} = \frac{1K}{0.3838K} = 2.6$, which is almost same as the designed value of Q_p.

Figure 4.29 shows the frequency response of the CMF for f_p = 100 KHz.

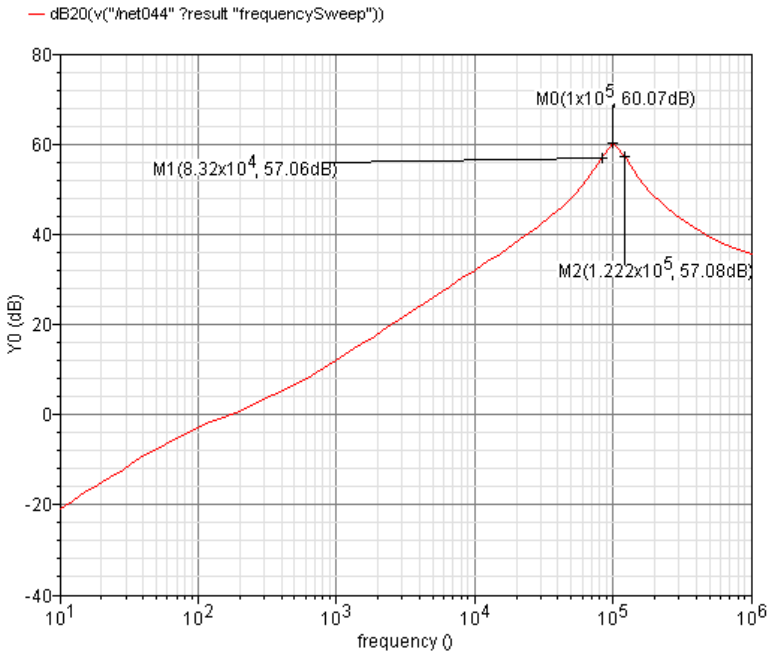

Figure 4.29: Frequency response of the TRF for f_p = 100 KHz

Choosing, $Q_p = 2.5$, $r = r_1 = r_2 = R_1 = R_2 = 1\ K\Omega$.

From equation (4.15) & (4.16), C1 = 3.97887 nF and C2 = 0.63662 nF.

From figure 4.29, it is observed that, center frequency, f_p = 100 KHz which is equal to the designed value of f_p.

Also, $Q_p = \frac{f_p}{\Delta f} = \frac{100K}{122.2K - 83.2K} = \frac{100K}{39K} = 2.5$, which is exactly same as the designed value of Q_p.

4.12 Use of UAM as electronic sensors and actuators

A sensor tells something about its environment. An electronic sensor provides the information about its environment generating an electrical signal. The measured electrical signal generated by the electronic sensor should change according to the change of the things it is measuring. For example, a thermostat controls the heat. It measures the temperature of the environment and converts this to an electrical signal. This signal is then sent down to wires and back to the heater itself. When the signal indicates that it is too cold, then the heater becomes on.

There are lots of electronic sensors in real life which are used to measure heat, light, humidity, sound level, weight etc. Each of these quantities requires different types of sensors. In each case, physical changes are sensed and converted to electrical signals that are sent down to wires or sent over a radio channel etc. Some common types of sensors that are used in practical life can be listed as:

1. Microphones
2. Infrared detectors used in motion sensors
3. Video cameras
4. Hall Effect probes (magnetic field)
5. Remote control devices (such as, TV remote, iTunes remote, BOXEE remote, DVD remote, VLC remote etc.)
6. Photocells etc.

Amplifiers are the essential parts of the sensors which sense the change of voltage/current at their inputs and convert to an amplified level of signals. In the following sections, some possible

examples are included of the proposed Universal Amplifier Module (UAM) for interfacing with electronic sensors and actuators.

4.12.1 UAM for Micro Mechanical Sensors and Actuator Circuitry

In recent year, it has been discovered that, Resonant Micro Electro-Mechanical (MEMS) sensors and actuators can serve as better alternatives to existing macro scale counterparts [39]. These MEMS sensors and actuators are capable of delivering a small form factor, integrated solution. Capacitive-coupled MEMS-based oscillators provide satisfactory phase noise performance that meets GSM requirements [40] – [41]. Moreover, Capacitive-coupled MEMS-based oscillators have become potential candidates to replace bulky discrete crystal oscillators used in RF and microprocessor applications.

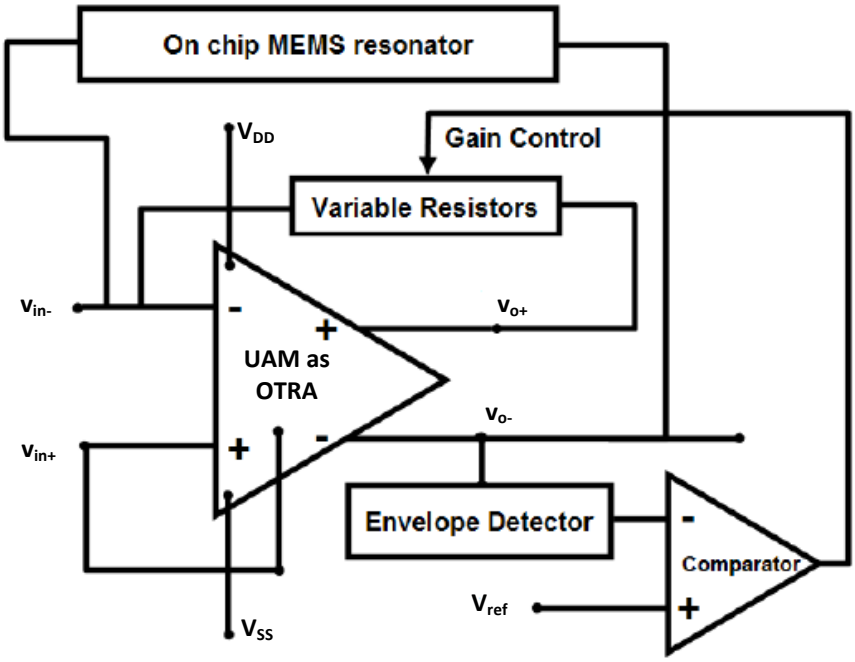

Figure 4.30: Capacitive-coupled MEMS oscillator using the proposed UAM

Fig. 4.30 shows the block diagram of the general topology of a micro mechanical resonator oscillator circuit [42]. A fully differential operational transresistance amplifier (OTRA)

constitutes the core circuit block in the control circuit associated with resonant MEMS sensors and actuators [41], [43]. The Universal Amplifier Module (UAM) reported in this thesis can be used as the core block of the MEMS oscillator shown in figure 4.30. An OTRA interface is preferred because of the large impedance of the MEMS resonator. The OTRA exhibits low input and output impedances (shown in figure 1.3 of chapter 1) which reduces the loading on the MEMS resonators. Hence the resonators have high Q which is necessary for reducing the oscillator phase noise. The UAM reported in this thesis can be very easily configured as an OTRA (section 2.9.2, chapter 2).

It is a great challenge to design appropriate operational amplifiers that combine high DC gain, high unity-gain bandwidth and wide dynamic range [44]. For the OTRA (realized from the UAM), the open loop DC gain of 165.07 dB, unity-gain bandwidth of 1.3 GHz, input resistance of 200 Ω and output resistance of 1.1 KΩ (shown in table 3.2 in section3.6, chapter 3) make the UAM operating as OTRA (CCVS) as a better candidate for the core circuit block for the MEMS oscillator shown in figure 4.30.

In the advanced process technology, the core amplifier needs to deliver required high gain and bandwidth to implement a MEMS oscillator even though the supply voltage and intrinsic gain of the transistors decreases with scaling. It is important that, the amplifier has to maintain high gain in presence of process variations and under all process corners which is a challenge that is really difficult to meet using topologies that are satisfactory on older process technologies. In this sense, though the UAM was designed in 0.18 μm CMOS (CMOSP18/TSMC) technology and the supply voltages scaled down to ±1.3 V, the proposed UAM can provide the gain, bandwidth and

other design parameter values (shown in table 3.2 of chapter 3) good enough to provide a successful core circuit of the MEMS sensors and actuator.

4.12.2 Pressure Transducer to ADC Application using UAM

An important application of an OP-AMP is to convert and condition signals from transducers into signals that are used by some other devices such as analog-to-digital converters (ADCs). Conversion & conditioning of signals are necessary for synchronizing between transducers and the ADC. Because usually the transducer and ADC ranges and offsets are not same. OP-AMP is also useful in signal filtering for compatibility with ADC circuits [45].

The sensor considered here is a pressure transducer SX01 produced by SenSym [45]. It is a solid-state pressure sensor with available full-scale ranges of 1 – 150 psi (7 kPa – 1 MPa). Three pressure measurement types are available: gauge, differential, and absolute. The device evaluated here has a full-scale pressure of 7 kPa. Its cost is low relative to other devices in this range. To operate a bridge transducer, it must be excited by a voltage source. As the accuracy of the measurement signal is affected by the stability of the excitation voltage, a regulated voltage source is necessary. A regulated 5-V supply is considered in this case.

For the design of SX01 pressure transducer, TLV2544 ADC has been used which has an analog input range of 0 – 5 V. The ADC's 0 – 5 V analog-input range and the fact that the power available was a single 5-V supply require a rail-to-rail output device. The OP-AMP must also be able to handle the full input range of the transducer. For these reasons, the TLV2474 was chosen as the OP-AMP [46]. In comparison with the TLV2474 device, the proposed UAM of this report

can be a good alternative in this case. The performance parameters on which the UAM stands up are gain, bandwidth, supply voltage range, input offset voltage, slew rate, CMRR etc.

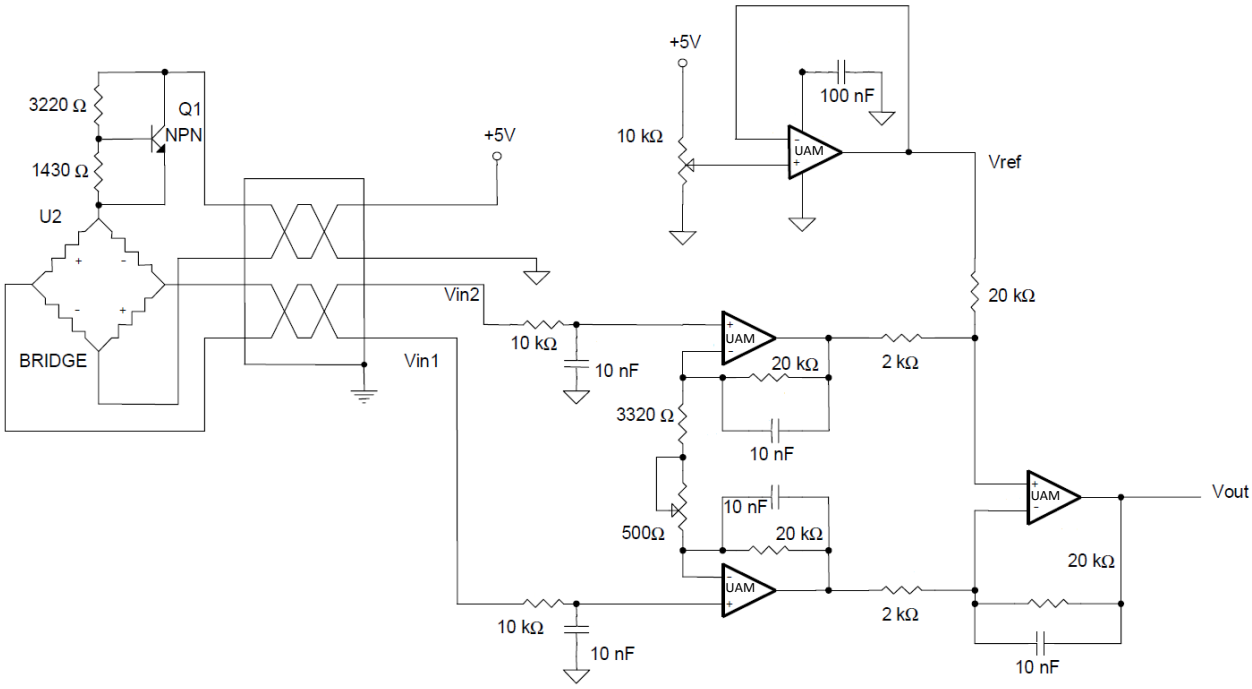

Figure 4.31: OP-AMP circuit for the pressure transducer to ADC application

Figure 4.31 shows the circuit configuration that can be used for pressure transducer to ADC application. The UAM provides interface, converts and conditions signals from transducers into signals that are used by the ADC. A short comparison between the used OP-AMP TLV2474 in the transducer and the proposed UAM of this report is given in table 4.1 below:

Table 4.1: Performance parameters comparison between TLV2474 [46] and the UAM

Parameters	TLV2474	UAM (of this report)
Total supply voltage (Min)	2.7 V	-1.3
Total supply voltage (Max)	6 V	+1.3
Gain bandwidth	2.8 MHz	26.83 GHz
Open loop gain	90 dB	117.8 dB
Slew rate	1.4 V/µs	2.42 V/µs
Input offset voltage	250 µV	-97.33 pV
CMRR	61 dB	200.79 dB

4.13 Summary

In this chapter, some basic signal processing cases with the UAM have been presented. Some traditional amplifier circuits, such as, inverting amplifier, non-inverting amplifier, ideal integrator, lossy integrator etc. have been implemented using the UAM. Moreover, several voltage mode 2^{nd} order band pass filters and current mode filters using the principles of transposed network are illustrated with the UAM as the active device. The next chapter concludes the achievements of this thesis and gives some recommendations for future works related to the Universal Amplifier Module (UAM).

CHAPTER 5

CONCLUSION AND FUTURE WORKS

5.1 Conclusion

In this thesis, a promising Universal Amplifier Module (UAM) has been designed. The UAM offers voltage and current mode operations as voltage amplifier, transconductance amplifier, transresistance amplifier, current amplifier operation etc. depending upon the voltage or current signal applied at the input. The UAM can be used in many applications such as, voltage mode filters, current mode filters, second order universal filter etc. The Universal Amplifier Module (UAM) has been designed both in schematic and layout level using 0.18 μm CMOS (CMOSP18/TSMC) technology. The UAM can function in fully differential (i.e., differential input-differential output) mode. A pair of gate-drain connected MOSFET devices, each connected to one of the differential voltage input terminals via a MOSFET switch, facilitates application of current signals at the input of the system. The switch can be digitally controlled (i.e., ON/OFF operation) to enable the UAM to operate either in the voltage or in the current-mode scenario. The UAM has low impedance voltage buffer and high impedance current buffer

output stages. For VCVS and CCVS modes of operations, the output can be taken off from the voltage buffer output stage, while for CCCS and VCCS modes of operations, the output must be taken off from the current buffer output stage.

The UAM was used to implement some traditional systems, such as, inverting amplifier, non-inverting amplifier, ideal integrator, lossy integrator and so on. To demonstrate the system level implementation capabilities, the UAM has been used to build 2^{nd} order band pass filter (BPF) circuits. Utilizing the principle of transposition, it has been possible to realize both voltage-mode and current-mode filtering functions using the same set of UAM devices.

Conventional amplifiers such as, OP-AMP, OTA, OTRA, CCII etc. separately can provide either voltage or current mode operations. Hence in the sense of universal concept, the proposed UAM could become versatile analog building block that could afford to implementation of multi-mode analog signal processing functions with low power consumption and less substrate area in an integrated circuit environment.

5.2 Recommendations for Future Works

5.2.1 Optimization of the layout

The layout of the UAM was developed segmentally, i.e., by the sub-system of the UAM. While the individual layout modules produced satisfactory results after post layout simulations, the overall layout obtained by connecting together the segmental modules did not provide desired results. It is felt that the parasitic components associated with the layout segments and the interconnection layers could have caused the problem. No optimization procedure was pursued

in creating the segmental layout modules. It is necessary to follow careful layout practice to minimize the effects of the parasitic components so that the overall layout produces successful results.

5.2.2 Chip fabrication and test

In addition to the work presented in this thesis, it is also desirable to complete the whole design process by implementing the proposed design as an integrated circuit (IC). Due to shortage of some essential resources, the array of pads around the core layout was not placed. Hence the layout was not ready to be processed for fabrication. Further work can be undertaken to complete the layout of the UAM with padding and process the work for fabrication as an IC chip via the resources available through the Canadian Microelectronics Corporation (CMC), Canada. This could be followed up by proper test and evaluation.

5.2.3 UAM in other technologies

A family of UAM could be implemented in different technologies such as BiCMOS, BJT, HBT etc., and their potential applications explored for signal processing cases with varied performance requirements.

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APPENDIX – A

A.1 Ackerberg and Mossberg (A & M) biquadratic filters

The A & M filter which can produce both low-pass and band-pass filter responses depending upon the choice of the output signal node is shown in Figure A.1.1. The two voltage transfer functions of the A & M filter are [37]:

$$\frac{V_{o1}}{V_i} = -\frac{s/RC_1}{s^2 + s\frac{1}{R_1C_1} + \frac{r_1}{C_1C_2R_2rr_2}}$$

and

$$\frac{V_{o2}}{V_i} = -\frac{\frac{r_1}{C_1C_2Rrr_2}}{s^2 + s\frac{1}{R_1C_1} + \frac{r_1}{C_1C_2R_2rr_2}}$$

Figure A.1.2 shows the corresponding CM network N_C obtained directly from the VM filter by reversing the input/out ports of each of the VCVS elements in Figure A.1.1. It can easily be shown that the two current transfer functions are given by:

$$\frac{I_o}{I_{i2}} = -\frac{\frac{r_1}{C_1C_2Rrr_2}}{s^2 + \frac{1}{R_1C_1}s + \frac{r_1}{C_1C_2rr_2R_2}} \qquad \text{with } I_{i1}=0$$

and

$$\frac{I_o}{I_{i1}} = -\frac{\frac{1}{RC_1}s}{s^2 + \frac{1}{R_1C_1}s + \frac{r_1}{C_1C_2rr_2R_2}} \qquad \text{with } I_{i2}=0$$

which are, respectively, the same as the VTFs (V_{o1}/V_i) and (V_{o2}/V_i) of the VM filter of Figure A.1.1. Thus, we can obtain a CM filter from a VM filter that employs three-terminal ideal VCVSs by simply reversing the input/output terminals of each of the VCVSs in the latter.

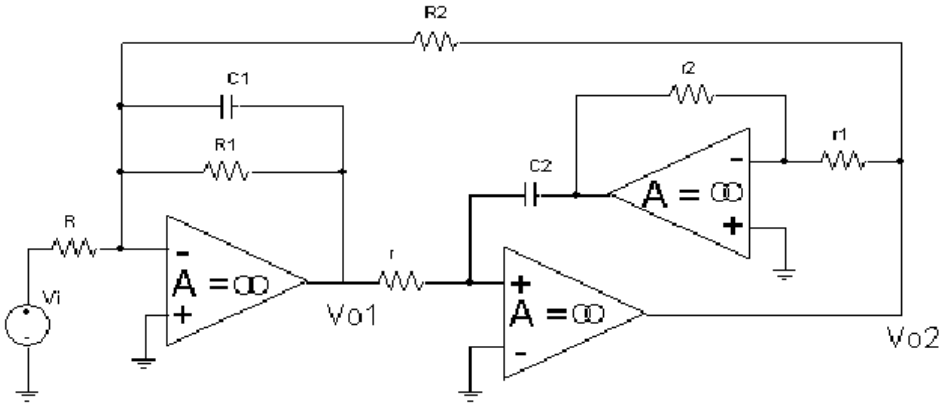

Figure A.1.1: Voltage-mode A & M biquadratic filter

Similarly, we can conclude that if the VM filter consists of only three-terminal CCCS elements, then we can obtain the corresponding CM filter by simply reversing the input/output terminals of the CCCSs in the former.

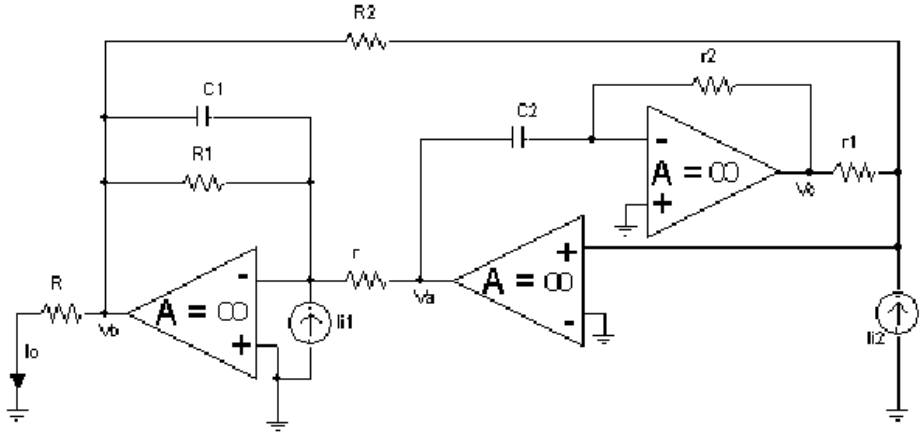

Figure A.1.2: Current-mode A & M biquadratic filter

APPENDIX – B

B.1 The Voltage-Mode A & M Filter

For the VM A & M filter shown in Figure A.1.1, let us assume that each OA has a gain A. Then, the LP and BP voltage transfer functions are given by [37]:

$$\frac{V_{o2}}{V_i} = -\frac{1/rR}{\frac{1}{R_2 r} + \left(\frac{\frac{1}{R}+\frac{1}{R_2}}{A} + \left(1+\frac{1}{A}\right)\left(\frac{1}{R_1}+SC_1\right)\right)\left(\frac{\frac{1}{r}+SC_2}{A} + \frac{\frac{SC_2}{r_1}}{\frac{1}{r_2}+\frac{1/r_2+1/r_1}{A}}\right)}$$

$$\frac{V_{o1}}{V_i} = -\frac{\frac{1}{R}\left(\frac{\frac{1}{r}+SC_2}{A} + \frac{\frac{SC_2}{r_1}}{\frac{1}{r_2}+\frac{1/r_2+1/r_1}{A}}\right)}{\frac{1}{R_2 r} + \left(\frac{\frac{1}{R}+\frac{1}{R_2}}{A} + \left(1+\frac{1}{A}\right)\left(\frac{1}{R_1}+SC_1\right)\right)\left(\frac{\frac{1}{r}+SC_2}{A} + \frac{\frac{SC_2}{r_1}}{\frac{1}{r_2}+\frac{1/r_2+1/r_1}{A}}\right)}$$

To evaluate the performance of the VM filters, we use the one-pole model of the OA,

$$A = A(s) = \frac{A_o}{1+\frac{s}{\omega_b}}$$

where ω_b is the pole frequency. For frequencies $\omega >> \omega_{b,}$ we may assume

$$A = A(s) \approx \frac{A_o \omega_b}{s} \approx \frac{\omega_t}{s}$$

where $\omega_t \approx A_o \omega_b$ is the unity gain bandwidth of the OA. We further assume that

$$R = R_2 = r = r_1 = r_2, \quad C_1 = C_2 = C, \quad R_1 = Q_o R$$

and $$\omega_o << \omega_{t.,}$$

where, ω_o and Q_o are the pole frequency and pole-Q of the filter. With the above assumptions, we get the overall denominator DV(s) to be:

$$D_V(s) = 4\frac{s^5}{\omega_t^3} + \left[\frac{4\omega_o}{Q_o\omega_t^3} + \frac{8\omega_o}{\omega_t^3} + \frac{3}{\omega_t^2}\right]s^4 + \left[\frac{3\omega_o^3}{Q_o\omega_t^2} - \frac{\omega_o^3}{\omega_t^2}\right]s^3 + \left[1 + \frac{2\omega_o^2}{\omega_t^2} + \frac{\omega_o^2}{Q_o\omega_t^2} + \frac{3\omega_o}{\omega_t}\right]s^2 + \left[\frac{\omega_o^2}{Q_o\omega_t} + \frac{\omega_o}{Q_o}\right]s + \omega_o^2$$

Assuming that the actual operating frequency remains close to the pole frequency ω_o, we find the solution following the principle of dominant root search [60]. For this purpose, we use the approximations $s^3 = -\omega_o^2 s$, $s^4 = \omega_o^4$, $s^5 = \omega_o^4 s$ and simplify $D_V(s)$. This leads to:

$$\begin{aligned}
D_V(s) &\approx s\frac{4\omega_o^4}{\omega_t^3} + \left[\frac{4\omega_o}{Q_o\omega_t^3} + \frac{8\omega_o}{\omega_t^3} + \frac{3}{\omega_t^2}\right]\omega_o^4 - s\left[\frac{3\omega_o^3}{Q_o\omega_t^2} - \frac{\omega_o^3}{\omega_t^2}\right] \\
&\quad + s^2\left[1 + \frac{2\omega_o^2}{\omega_t^2} + \frac{\omega_o^2}{Q_o\omega_t^2} + \frac{3\omega_o}{\omega_t}\right] + s\left[\frac{\omega_o^2}{Q_o\omega_t} + \frac{\omega_o}{Q_o}\right] + \omega_o^2 \\
&\approx s^2\left[1 + \frac{2\omega_o^2}{\omega_t^2} + \frac{\omega_o^2}{Q_o\omega_t^2} + \frac{3\omega_o}{\omega_t}\right] + s\frac{\omega_o}{Q_o}\left[1 + \frac{\omega_o}{\omega_t} + \frac{4Q_o\omega_o^3}{\omega_t^3} - \frac{3\omega_o^2}{\omega_t^2} + \frac{Q_o\omega_o^2}{\omega_t^2}\right] \\
&\quad + \omega_o^2\left[1 + \frac{4\omega_o^3}{Q_o\omega_t^3} + \frac{8\omega_o^3}{\omega_t^3} + \frac{3\omega_o^2}{\omega_t^2}\right] \\
&\approx \Delta_v\left[s^2 + s\frac{\omega_o(1+\gamma_v)}{Q_o\Delta_v} + \frac{\omega_o^2(1+\delta_v)}{\Delta_v}\right] \\
&= \Delta_v(s^2 + s\frac{\omega_{oa}}{Q_{oa}} + \omega_{oa}^2)
\end{aligned}$$

where,

$$\Delta_v = 1 + \frac{2\omega_o^2}{\omega_t^2} + \frac{\omega_o^2}{Q_o\omega_t^2} + \frac{3\omega_o}{\omega_t}$$

$$\gamma_v = \frac{\omega_o}{\omega_t} + \frac{4Q_o\omega_o^3}{\omega_t^3} - \frac{3\omega_o^2}{\omega_t^2} + \frac{Q_o\omega_o^2}{\omega_t^2}$$

$$\delta_v = \frac{4\omega_o^3}{Q_o\omega_t^3} + \frac{8\omega_o^3}{\omega_t^3} + \frac{3\omega_o^2}{\omega_t^2}$$

The terms like $(\frac{\omega_o}{\omega_t})^2, (\frac{\omega_o}{\omega_t})^3 \cdots$ can be ignored, and $\frac{1}{(1+x)^n} \approx 1 - nx$ for first-order accuracy, x<<1, where $x = \omega_0/\omega_t$, we get the following expressions for the deviations in the pole-frequency and pole-Q of the VM filter of Figure A.1.1.

$$\sigma_V = \frac{\omega_{oa} - \omega_o}{\omega_o} = \left(\frac{1+\delta_v}{\Delta_v}\right)^{\frac{1}{2}} - 1 \approx -\frac{3\omega_o}{2\omega_t}$$

$$\eta_v = \frac{Q_{oa} - Q_o}{Q_o} = \frac{[\Delta_v(1+\delta_v)]^{\frac{1}{2}}}{(1+\gamma_v)} - 1 \approx \frac{\omega_o}{2\omega_t}$$

where ω_{oa} and Q_{oa} are the realized values.

APPENDIX – C

C.1 The Current-Mode A & M Filter

Figure A.1.2 shows the CM A & M filter. The LP and BP current transfer functions (CTF) are obtained as [37]:

$$\frac{I_o}{I_{i2}} = -\frac{1/rR}{\frac{1}{R_2 r} + \left(\frac{1}{Ar} + \left(1+\frac{1}{A}\right)\left(\frac{1}{R_1} + SC_1\right)\right)\left(\frac{\frac{1}{R_2}+\frac{1}{r_1}}{A} + \frac{\frac{SC_2}{r_1}}{\frac{1}{r_2}+\frac{1/r_2+SC_2}{A}}\right)}$$

and

$$\frac{I_o}{I_{i1}} = -\frac{\frac{1}{R}\left(\frac{\frac{1}{R_2}+\frac{1}{r_1}}{A} + \frac{\frac{SC_2}{r_1}}{\frac{1}{r_2}+\frac{1/r_2+SC_2}{A}}\right)}{\frac{1}{R_2 r} + \left(\frac{1}{Ar} + \left(1+\frac{1}{A}\right)\left(\frac{1}{R_1} + SC_1\right)\right)\left(\frac{\frac{1}{R_2}+\frac{1}{r_1}}{A} + \frac{\frac{SC_2}{r_1}}{\frac{1}{r_2}+\frac{1/r_2+SC_2}{A}}\right)}$$

With the same assumptions as the VM filter in Section B.1, we get denominator $D_I(s)$ to be

$$D_I(s) = 2\frac{s^5}{\omega_t^3} + \left[\frac{2\omega_o}{Q_o\omega_t^3} + \frac{4\omega_o}{\omega_t^3} + \frac{2}{\omega_t^2}\right]s^4 + \left[\frac{2\omega_o^4}{Q_o\omega_t^3} + \frac{2\omega_o^4}{\omega_t^3} + \frac{2\omega_o^3}{Q_o\omega_t^2} + \frac{4\omega_o^3}{\omega_t^2} + \frac{\omega_o^2}{\omega_t}\right]s^3$$
$$+ \left[1 + \frac{\omega_o}{Q_o\omega_t} + \frac{2\omega_o^2}{\omega_t^2} + \frac{4\omega_o^2}{Q_o\omega_t^2} + \frac{4\omega_o}{\omega_t}\right]s^2 + \left[\frac{\omega_o}{Q_o} + \frac{\omega_o^2}{\omega_t} + \frac{2\omega_o^2}{Q_o\omega_t}\right]s + \omega_o^2$$

We approximate $s^3 = -\omega_o^2 s$, $s^4 = \omega_o^4$, $s^5 = \omega_o^4 s$ and simplify $D_I(s)$. This leads to

$$D_V(s) \approx s\frac{4\omega_o^4}{\omega_t^3} + \left[\frac{4\omega_o}{Q_o\omega_t^3} + \frac{8\omega_o}{\omega_t^3} + \frac{3}{\omega_t^2}\right]\omega_o^4 - s\left[\frac{3\omega_o^3}{Q_o\omega_t^2} - \frac{\omega_o^3}{\omega_t^2}\right]$$
$$+ s^2\left[1 + \frac{2\omega_o^2}{\omega_t^2} + \frac{\omega_o^2}{Q_o\omega_t^2} + \frac{3\omega_o}{\omega_t}\right] + s\left[\frac{\omega_o^2}{Q_o\omega_t} + \frac{\omega_o}{Q_o}\right] + \omega_o^2$$
$$\approx s^2\left[1 + \frac{2\omega_o^2}{\omega_t^2} + \frac{\omega_o^2}{Q_o\omega_t^2} + \frac{3\omega_o}{\omega_t}\right] + s\frac{\omega_o}{Q_o}\left[1 + \frac{\omega_o}{\omega_t} + \frac{4Q_o\omega_o^3}{\omega_t^3} - \frac{3\omega_o^2}{\omega_t^2} + \frac{Q_o\omega_o^2}{\omega_t^2}\right]$$
$$+ \omega_o^2\left[1 + \frac{4\omega_o^3}{Q_o\omega_t^3} + \frac{8\omega_o^3}{\omega_t^3} + \frac{3\omega_o^2}{\omega_t^2}\right]$$

$$\approx \Delta_I\left[s^2 + s\frac{\omega_o(1+\gamma_I)}{Q_o\Delta_I} + \frac{\omega_o^2(1+\delta_I)}{\Delta_I}\right]$$
$$= \Delta_I(s^2 + s\frac{\omega_{oa}}{Q_{oa}} + \omega_{oa}^2)$$

where,

$$\Delta_I = 1 + \frac{\omega_o}{Q_o\omega_t} + \frac{2\omega_o^2}{\omega_t^2} + \frac{4\omega_o^2}{Q_o\omega_t^2} + \frac{4\omega_o}{\omega_t}$$

$$\gamma_I = \frac{2\omega_o}{\omega_t} - \frac{2\omega_o^3}{\omega_t^3} - \frac{2\omega_o^2}{\omega_t^2} - \frac{4Q_o\omega_o^2}{\omega_t^2}$$

$$\delta_I = \frac{2\omega_o^3}{Q_o\omega_t^3} + \frac{4\omega_o^3}{\omega_t^3} + \frac{2\omega_o^2}{\omega_t^2}$$

Again, Using the assumption that terms like $(\frac{\omega_o}{\omega_t})^2, (\frac{\omega_o}{\omega_t})^3 \ldots$ can be ignored, and that $\frac{1}{(1+x)^n} \approx 1 - nx, x << 1,$ where $x = \omega_0/\omega_t$, we get the following expressions for the deviations in the pole-frequency and pole-Q of the CM filter of Figure A.1.2.

$$\sigma_I = \frac{\omega_{oa} - \omega_o}{\omega_o} = \left(\frac{1+\delta_I}{\Delta_I}\right)^{\frac{1}{2}} - 1 \approx -(\frac{2\omega_o}{\omega_t} + \frac{\omega_o}{2Q_o\omega_t})$$

and

$$\eta_I = \frac{Q_{oa} - Q_o}{Q_o} = \frac{[\Delta_I(1+\delta_I)]^{\frac{1}{2}}}{(1+\gamma_I)} - 1 \approx \frac{\omega_o}{2Q_o\omega_t}$$

where ω_{oa} and Q_{oa} are the realized values.

APPENDIX – D

D.1 Simulation set-up for CCVS

D.1.1 Open loop frequency response

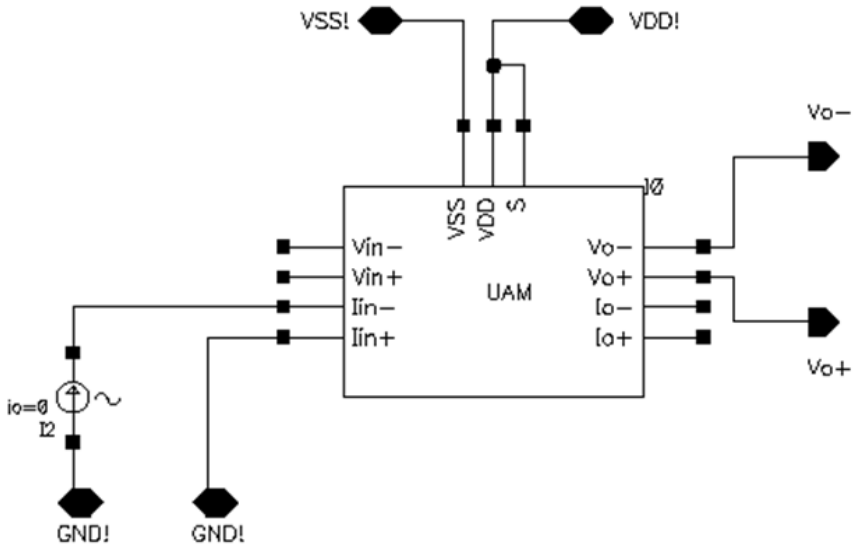

Figure D.1.1: Configuration for open loop frequency response of the CCVS

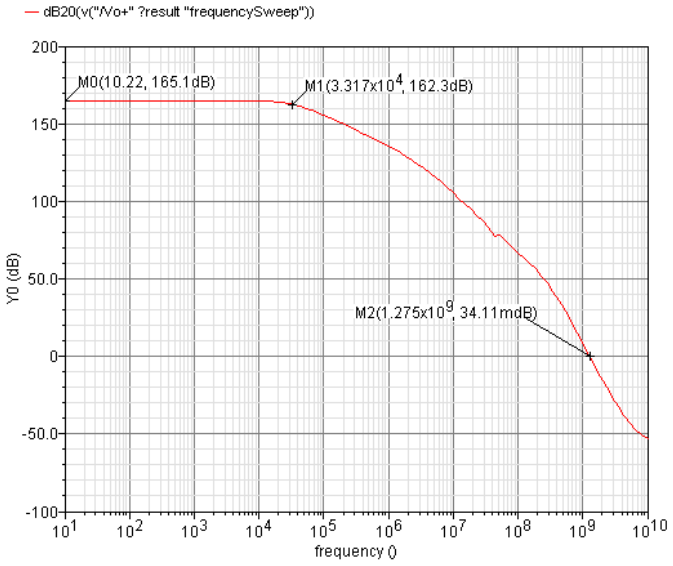

Figure D.1.2: Magnitude response of the CCVS

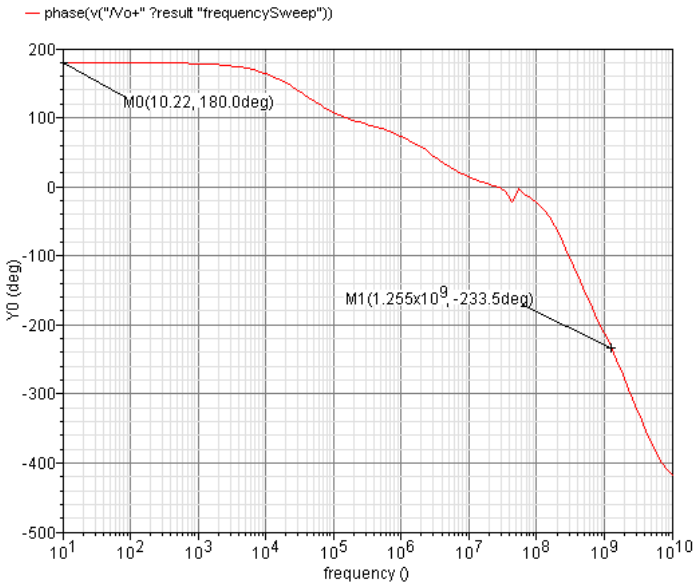

Figure D.1.3: Phase response of the CCVS

D.1.2 Input common mode range (ICMR)

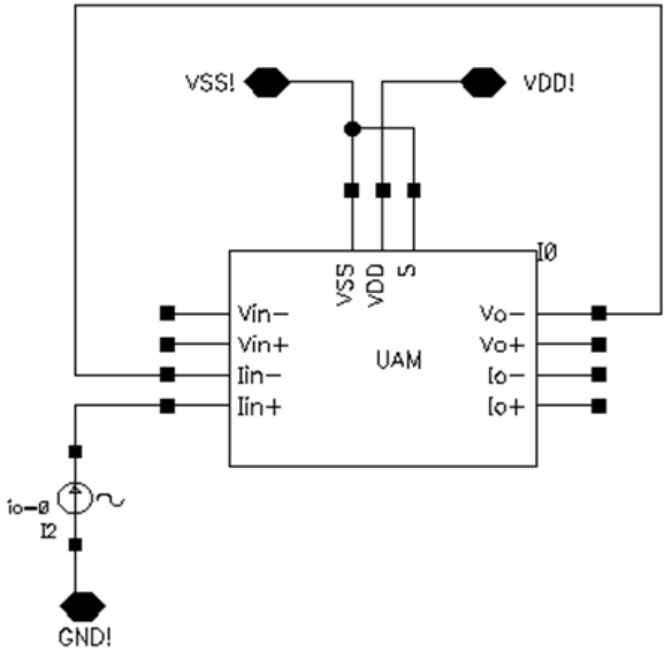

Figure D.1.4: Configuration for measuring input common mode range of the CCVS

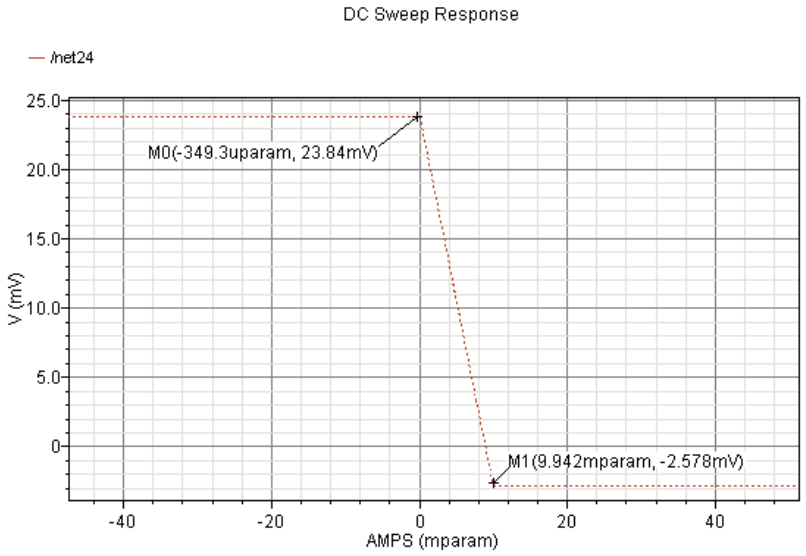

Figure D.1.5: Simulated ICMR characteristics of the CCVS

D.1.3 Input and output offset voltage

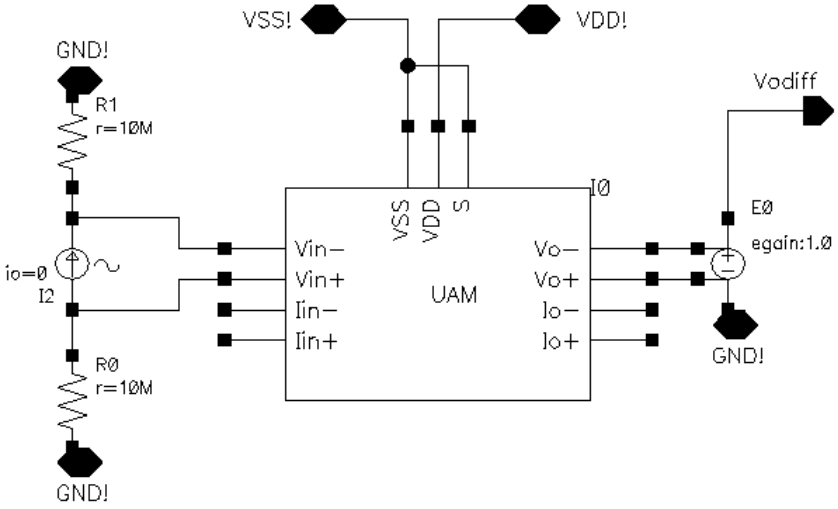

Figure D.1.6: Configuration for measuring input offset of the CCVS

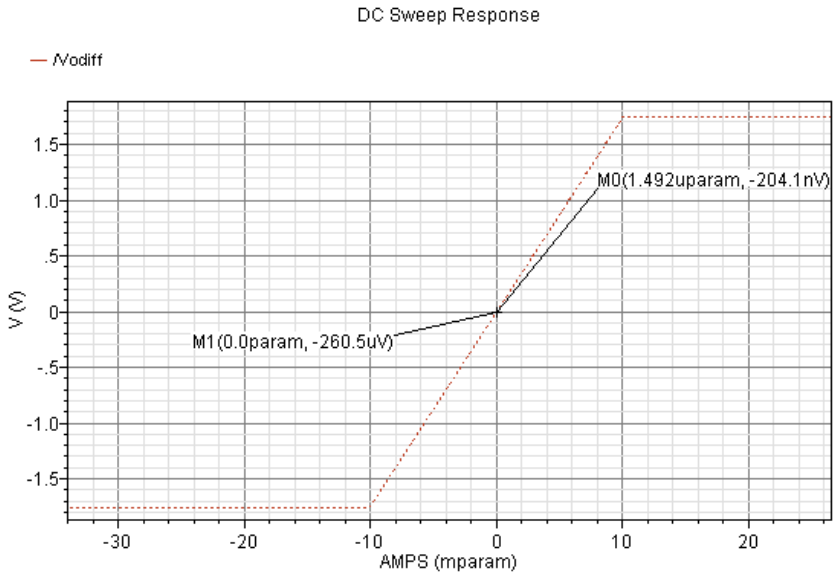

Figure D.1.7: Simulated input offset voltage of the CCVS

D.1.4 Output voltage swing

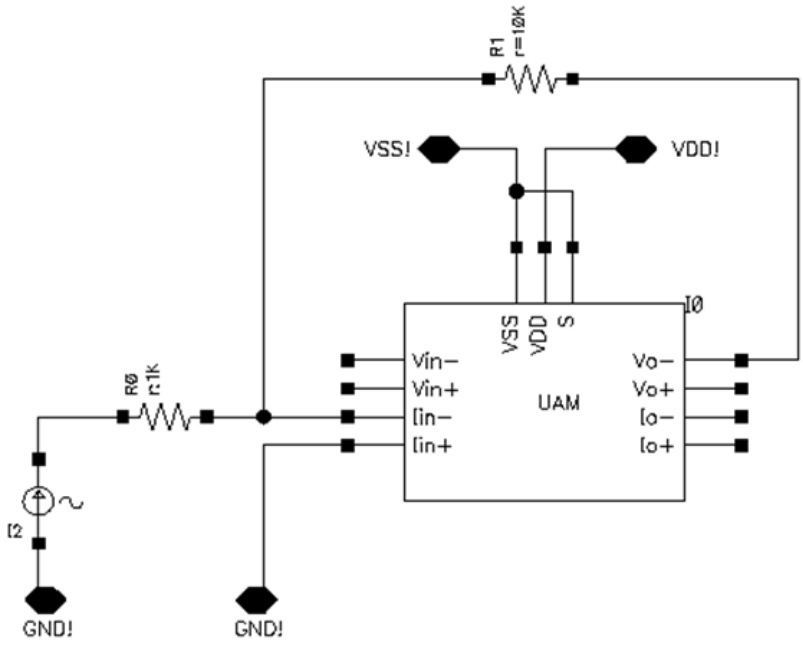

Figure D.1.8: Measurement set-up for output voltage swing of the CCVS

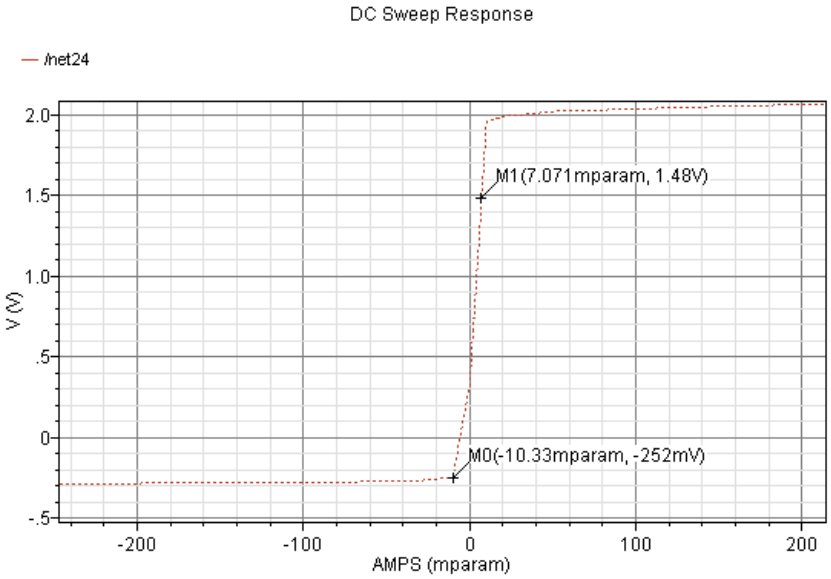

Figure D.1.9: Simulated output voltage swing of the CCVS

D.2 Simulation set-up for CCCS

D.2.1 Open loop frequency response

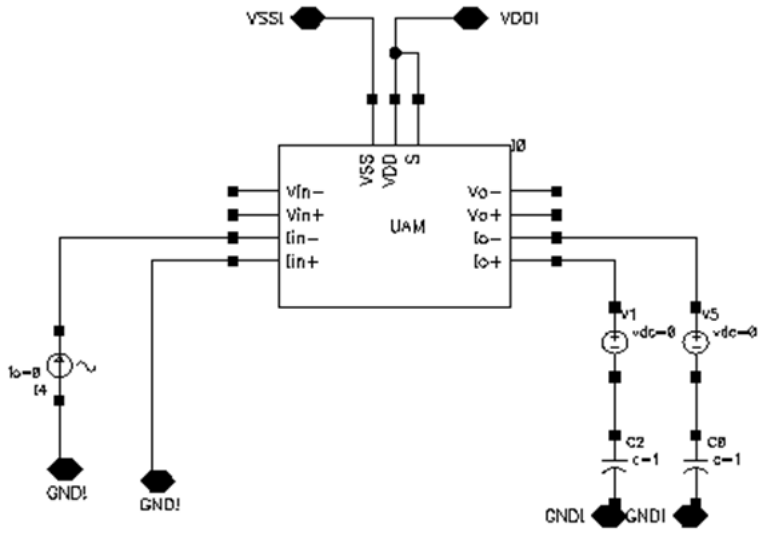

Figure D.2.1: Configuration for open loop frequency response of the CCCS

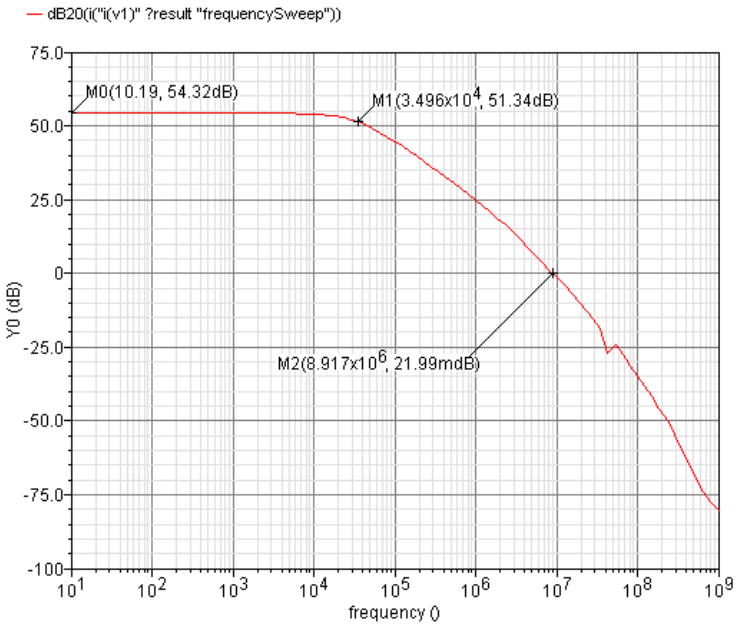

Figure D.2.2: Frequency response of the CCCS

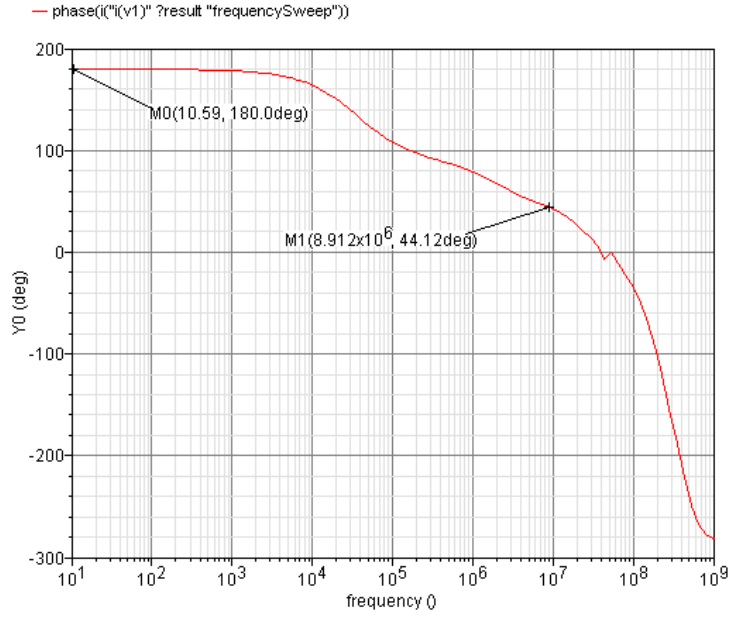

Figure D.2.3: Phase response of the CCCS

D.2.2 Input common mode range (ICMR)

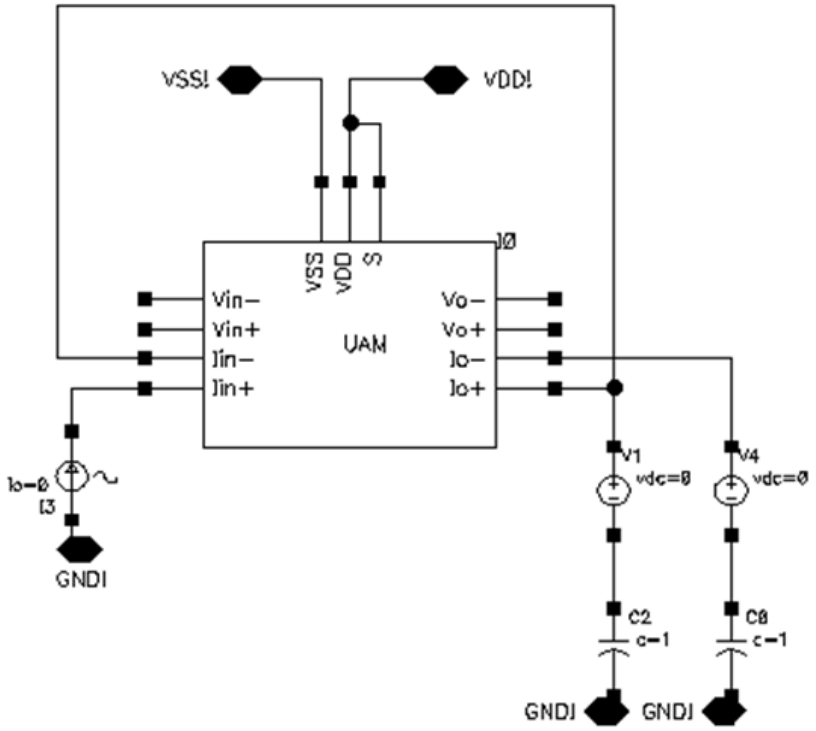

Figure D.2.4: Configuration for measuring input common mode range of the CCCS

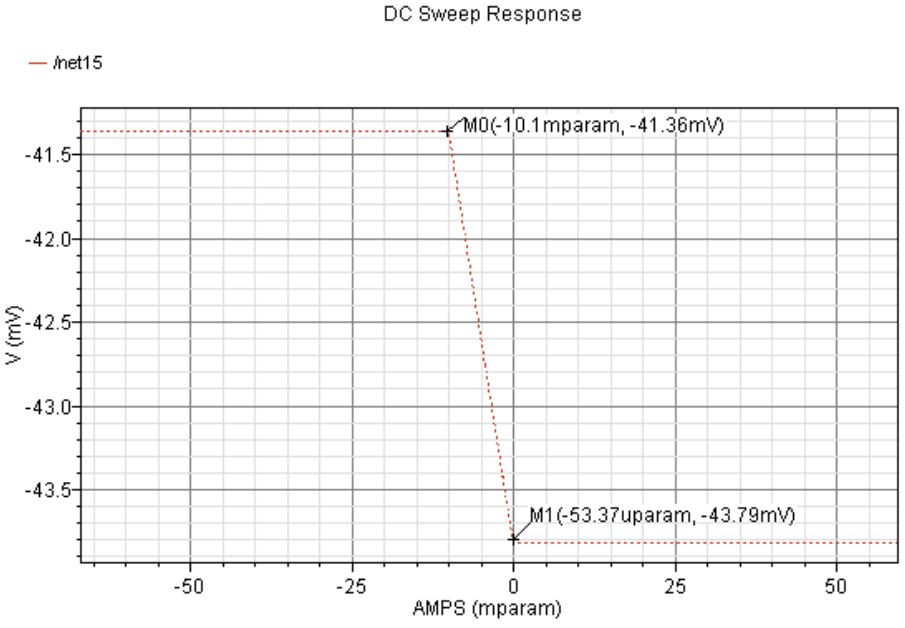

Figure D.2.5: Simulated ICMR characteristics of the CCCS

D.2.3 Output voltage swing

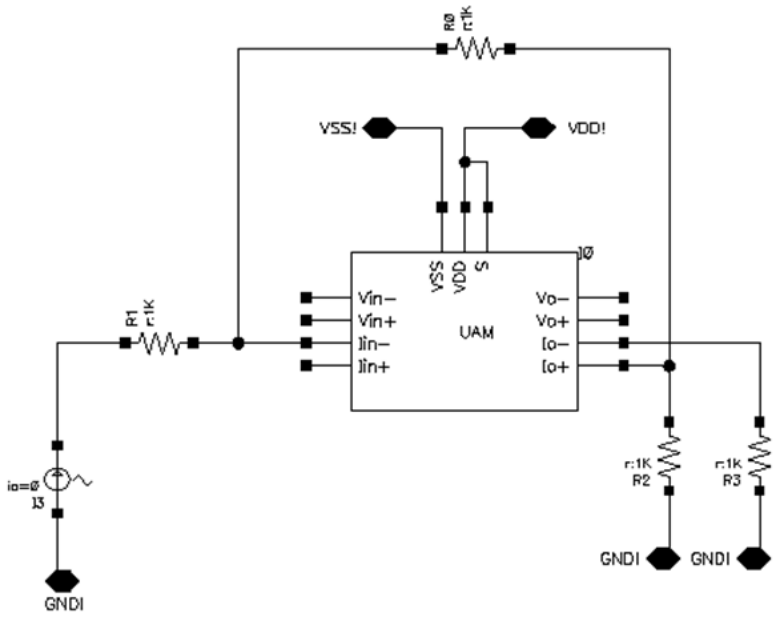

Figure D.2.6: Measurement set-up for output swing of the CCCS with R_L = 1 KΩ

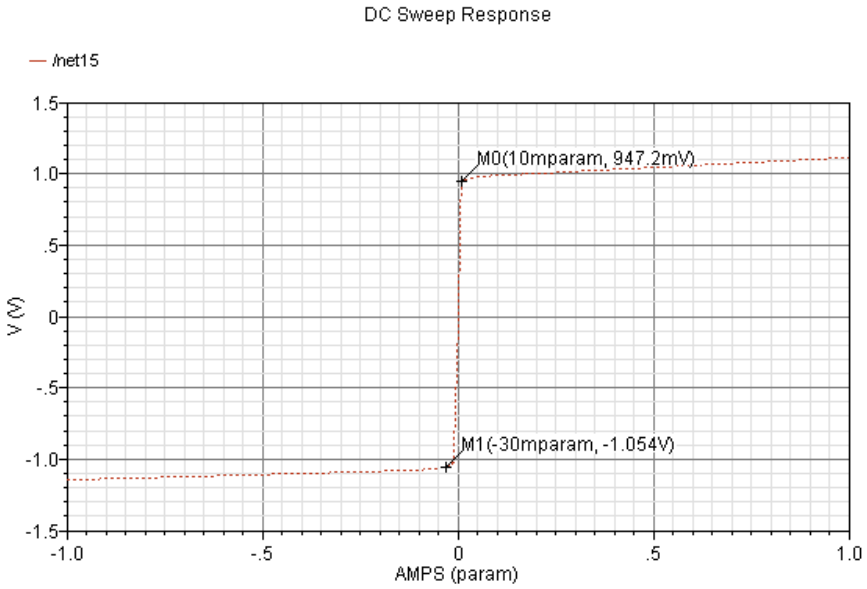

Figure D.2.7: Simulated output swing of the CCCS

D.3 Simulation set-up for VCCS

D.3.1 Open loop frequency response

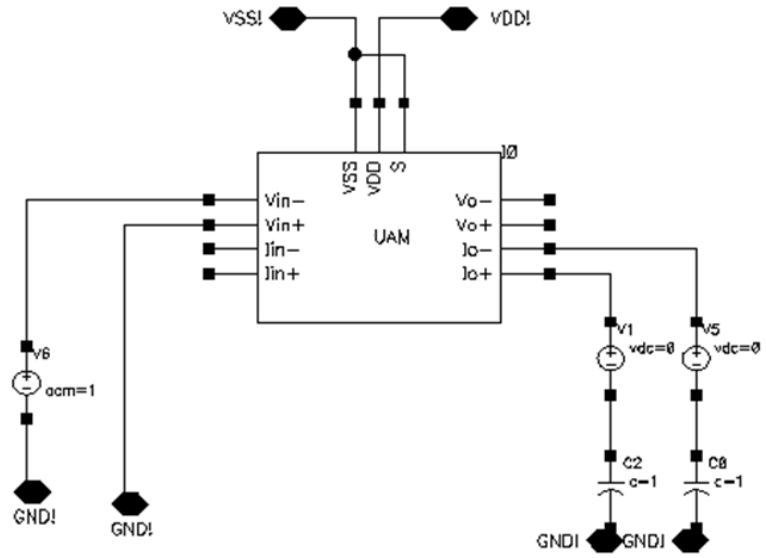

Figure D.3.1: Configuration for open loop frequency response of the VCCS

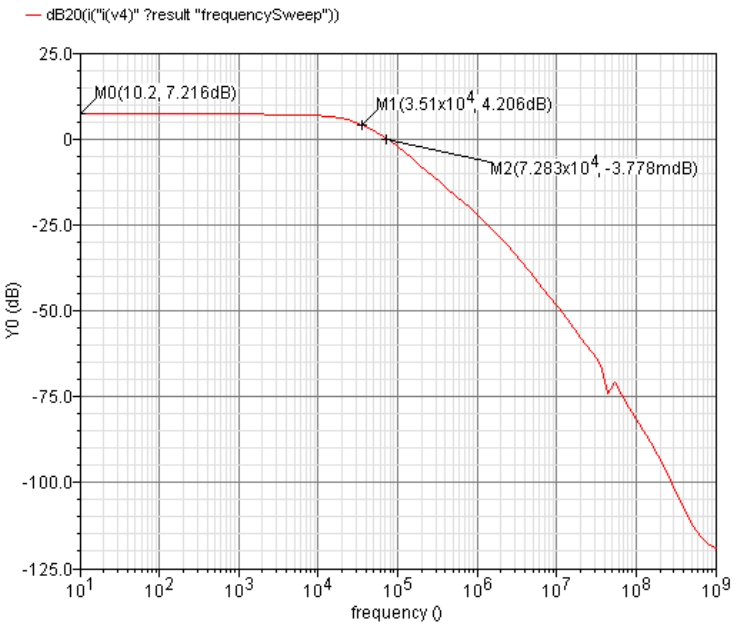

Figure D.3.2: Magnitude response of the VCCS

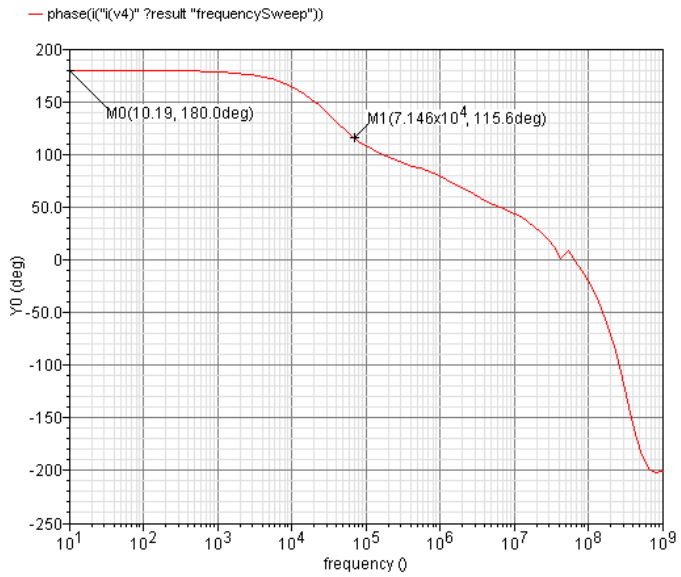

Figure D.3.3: Phase response of the VCCS

D.3.2 Input and output offset voltage

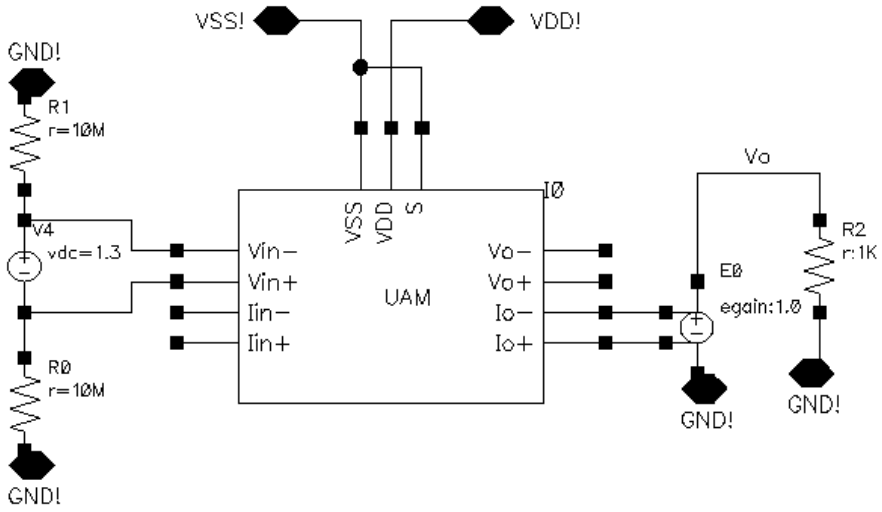

Figure D.3.4: Configuration for measuring input offset of the VCCS with R_L = 1 KΩ

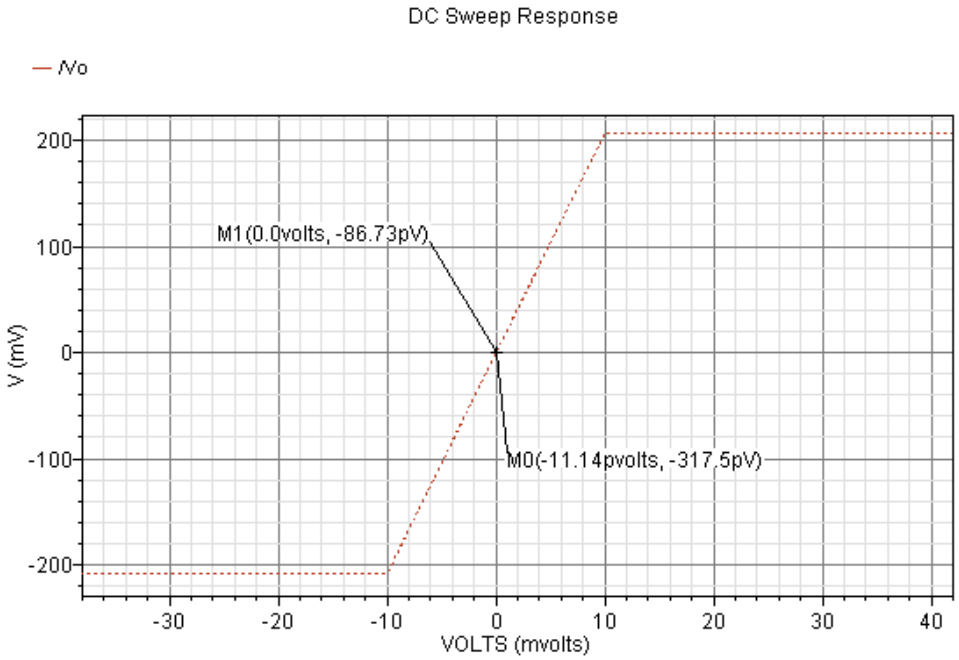

Figure D.3.5: Simulated input offset of the VCCS

APPENDIX – E

E.1 SPICE file for the NETLIST of the Universal Amplifier Module

```
* # FILE NAME:
/NFS/THESIS/M/M_TALUKD/SIMULATION/MYUAMCKT/HSPICES/SCHEMATIC/
* NETLIST/MYUAMCKT.C.RAW
* NETLIST OUTPUT FOR HSPICES.
* GENERATED ON AUG 2 02:17:17 2011

* GLOBAL NET DEFINITIONS
.GLOBAL VDD! VSS! GND!
* FILE NAME: NEWUAM2_MYUAMCKT_SCHEMATIC.S.
* SUBCIRCUIT FOR CELL: MYUAMCKT.
* GENERATED FOR: HSPICES.
* GENERATED ON AUG  2 02:17:17 2011.

C0 NET0225 GND!  1.0 M=1.0
C2 NET0227 GND!  1.0 M=1.0
V5 NET0307 GND!  AC 1.0
V2 VDD! GND!  1.3
V3 GND! VSS!  1.3
V1 NET0343 NET0227  0.0
V4 NET0335 NET0225  0.0
XI1 GND! TIEDOWN_G1

M12 NET0317 NET0261 VDD! VDD!  PCH  L=1.2E-6 W=37E-6 AD=+1.77600000E-11
+AS=+1.77600000E-11 PD=+7.49600000E-05 PS=+7.49600000E-05 NRD=+7.29729730E-03
+NRS=+7.29729730E-03 M=1.0
M17 NET171 NET171 VDD! VDD!  PCH  L=1.2E-6 W=9E-6 AD=+4.32000000E-12
+AS=+4.32000000E-12 PD=+1.89600000E-05 PS=+1.89600000E-05 NRD=+3.00000000E-02
+NRS=+3.00000000E-02 M=1.0
M7 NET0321 NET0261 VDD! VDD!  PCH  L=1.2E-6 W=37E-6 AD=+1.77600000E-11
+AS=+1.77600000E-11 PD=+7.49600000E-05 PS=+7.49600000E-05 NRD=+7.29729730E-03
+NRS=+7.29729730E-03 M=1.0
M18 NET233 NET233 VDD! VDD!  PCH  L=1.2E-6 W=9E-6 AD=+4.32000000E-12
+AS=+4.32000000E-12 PD=+1.89600000E-05 PS=+1.89600000E-05 NRD=+3.00000000E-02
+NRS=+3.00000000E-02 M=1.0
M33 NET0389 NET0389 VDD! VDD!  PCH  L=1.2E-6 W=74.202674E-6 AD=+3.56172835E-
11
+AS=+3.56172835E-11 PD=+1.49365348E-04 PS=+1.49365348E-04 NRD=+3.63868289E-03
+NRS=+3.63868289E-03 M=1.0
```

M29 NET0342 NET0342 VDD! VDD! PCH L=1.2E-6 W=74.202674E-6 AD=+3.56172835E-11
+AS=+3.56172835E-11 PD=+1.49365348E-04 PS=+1.49365348E-04 NRD=+3.63868289E-03
+NRS=+3.63868289E-03 M=1.0
M26 NET0335 NET171 VDD! VDD! PCH L=1.5E-6 W=65E-6 AD=+3.12000000E-11
+AS=+3.12000000E-11 PD=+1.30960000E-04 PS=+1.30960000E-04 NRD=+4.15384615E-03
+NRS=+4.15384615E-03 M=1.0
M31 NET0335 NET0261 VDD! VDD! PCH L=1.5E-6 W=70E-6 AD=+3.36000000E-11
+AS=+3.36000000E-11 PD=+1.40960000E-04 PS=+1.40960000E-04 NRD=+3.85714286E-03
+NRS=+3.85714286E-03 M=1.0
M46 NET0343 NET0261 VDD! VDD! PCH L=1.5E-6 W=70E-6 AD=+3.36000000E-11
+AS=+3.36000000E-11 PD=+1.40960000E-04 PS=+1.40960000E-04 NRD=+3.85714286E-03
+NRS=+3.85714286E-03 M=1.0
M45 NET0343 NET233 VDD! VDD! PCH L=1.5E-6 W=65E-6 AD=+3.12000000E-11
+AS=+3.12000000E-11 PD=+1.30960000E-04 PS=+1.30960000E-04 NRD=+4.15384615E-03
+NRS=+4.15384615E-03 M=1.0
M8 NET0261 NET0261 VDD! VDD! PCH L=1.2E-6 W=20E-6 AD=+9.60000000E-12
+AS=+9.60000000E-12 PD=+4.09600000E-05 PS=+4.09600000E-05 NRD=+1.35000000E-02
+NRS=+1.35000000E-02 M=1.0
M3 NET0355 NET0307 NET216 VDD! PCH L=1.2E-6 W=40E-6 AD=+1.92000000E-11
+AS=+1.92000000E-11 PD=+8.09600000E-05 PS=+8.09600000E-05 NRD=+6.75000000E-03
+NRS=+6.75000000E-03 M=1.0
M5 NET0325 NET0261 VDD! VDD! PCH L=1.2E-6 W=70E-6 AD=+3.36000000E-11
+AS=+3.36000000E-11 PD=+1.40960000E-04 PS=+1.40960000E-04 NRD=+3.85714286E-03
+NRS=+3.85714286E-03 M=1.0
M13 NET259 NET259 NET0261 VDD! PCH L=1.2E-6 W=20E-6 AD=+9.60000000E-12
+AS=+9.60000000E-12 PD=+4.09600000E-05 PS=+4.09600000E-05 NRD=+1.35000000E-02
+NRS=+1.35000000E-02 M=1.0
M10 NET0371 NET0261 VDD! VDD! PCH L=1.2E-6 W=70E-6 AD=+3.36000000E-11
+AS=+3.36000000E-11 PD=+1.40960000E-04 PS=+1.40960000E-04 NRD=+3.85714286E-03
+NRS=+3.85714286E-03 M=1.0
M4 NET216 NET0261 VDD! VDD! PCH L=1.2E-6 W=95E-6 AD=+4.56000000E-11
+AS=+4.56000000E-11 PD=+1.90960000E-04 PS=+1.90960000E-04 NRD=+2.84210526E-03
+NRS=+2.84210526E-03 M=1.0
M2 NET0369 GND! NET216 VDD! PCH L=1.2E-6 W=40E-6 AD=+1.92000000E-11
+AS=+1.92000000E-11 PD=+8.09600000E-05 PS=+8.09600000E-05 NRD=+6.75000000E-03
+NRS=+6.75000000E-03 M=1.0
M11 NET0321 NET0371 VSS! VSS! NCH L=1E-6 W=10.073E-6 AD=+4.83504000E-12
+AS=+4.83504000E-12 PD=+2.11060000E-05 PS=+2.11060000E-05 NRD=+2.68043284E-02
+NRS=+2.68043284E-02 M=1.0
M19 1 NET0349 VSS! VSS! NCH L=1.2E-6 W=7.7E-6 AD=+3.69600000E-12
+AS=+3.69600000E-12 PD=+1.63600000E-05 PS=+1.63600000E-05 NRD=+3.50649351E-02
+NRS=+3.50649351E-02 M=1.0
M20 NET171 NET0321 1 VSS! NCH L=1.2E-6 W=20E-6 AD=+9.60000000E-12
+AS=+9.60000000E-12 PD=+4.09600000E-05 PS=+4.09600000E-05 NRD=+1.35000000E-02
+NRS=+1.35000000E-02 M=1.0

M21 NET233 NET0317 2 VSS! NCH L=1.2E-6 W=20E-6 AD=+9.60000000E-12
+AS=+9.60000000E-12 PD=+4.09600000E-05 PS=+4.09600000E-05 NRD=+1.35000000E-02
+NRS=+1.35000000E-02 M=1.0
M34 NET0211 NET0321 NET0211 NET0379 NCH L=1.2E-6 W=13E-6 AD=+6.24000000E-
12
+AS=+6.24000000E-12 PD=+2.69600000E-05 PS=+2.69600000E-05 NRD=+2.07692308E-02
+NRS=+2.07692308E-02 M=1.0
M16 NET0317 NET0325 VSS! VSS! NCH L=1E-6 W=10.073E-6 AD=+4.83504000E-12
+AS=+4.83504000E-12 PD=+2.11060000E-05 PS=+2.11060000E-05 NRD=+2.68043284E-02
+NRS=+2.68043284E-02 M=1.0
M22 2 NET0349 VSS! VSS! NCH L=1.2E-6 W=7.7E-6 AD=+3.69600000E-12
+AS=+3.69600000E-12 PD=+1.63600000E-05 PS=+1.63600000E-05 NRD=+3.50649351E-02
+NRS=+3.50649351E-02 M=1.0
M25 GND! VSS! NET0342 VSS! NCH L=1.2E-6 W=23.54E-6 AD=+1.12992000E-11
+AS=+1.12992000E-11 PD=+4.80400000E-05 PS=+4.80400000E-05 NRD=+1.14698386E-02
+NRS=+1.14698386E-02 M=1.0
M36 NET0335 NET0349 VSS! VSS! NCH L=1.5E-6 W=1.5E-6 AD=+7.20000000E-13
+AS=+7.20000000E-13 PD=+3.96000000E-06 PS=+3.96000000E-06 NRD=+1.80000000E-01
+NRS=+1.80000000E-01 M=1.0
M35 NET0335 NET233 VSS! VSS! NCH L=1.5E-6 W=1.5E-6 AD=+7.20000000E-13
+AS=+7.20000000E-13 PD=+3.96000000E-06 PS=+3.96000000E-06 NRD=+1.80000000E-01
+NRS=+1.80000000E-01 M=1.0
M47 NET0343 NET0349 VSS! VSS! NCH L=1.5E-6 W=1.5E-6 AD=+7.20000000E-13
+AS=+7.20000000E-13 PD=+3.96000000E-06 PS=+3.96000000E-06 NRD=+1.80000000E-01
+NRS=+1.80000000E-01 M=1.0
M48 NET0343 NET171 VSS! VSS! NCH L=1.5E-6 W=1.5E-6 AD=+7.20000000E-13
+AS=+7.20000000E-13 PD=+3.96000000E-06 PS=+3.96000000E-06 NRD=+1.80000000E-01
+NRS=+1.80000000E-01 M=1.0
M0 NET0369 NET0349 VSS! VSS! NCH L=1.2E-6 W=23.54E-6 AD=+1.12992000E-11
+AS=+1.12992000E-11 PD=+4.80400000E-05 PS=+4.80400000E-05 NRD=+1.14698386E-02
+NRS=+1.14698386E-02 M=1.0
M1 NET0355 NET0349 VSS! VSS! NCH L=1.2E-6 W=23.54E-6 AD=+1.12992000E-11
+AS=+1.12992000E-11 PD=+4.80400000E-05 PS=+4.80400000E-05 NRD=+1.14698386E-02
+NRS=+1.14698386E-02 M=1.0
M14 NET259 NET259 NET0349 VSS! NCH L=1.2E-6 W=10E-6 AD=+4.80000000E-12
+AS=+4.80000000E-12 PD=+2.09600000E-05 PS=+2.09600000E-05 NRD=+2.70000000E-02
+NRS=+2.70000000E-02 M=1.0
M15 NET0349 NET0349 VSS! VSS! NCH L=1.2E-6 W=10E-6 AD=+4.80000000E-12
+AS=+4.80000000E-12 PD=+2.09600000E-05 PS=+2.09600000E-05 NRD=+2.70000000E-02
+NRS=+2.70000000E-02 M=1.0
M6 NET0325 NET0369 VSS! VSS! NCH L=1.2E-6 W=11.9E-6 AD=+5.71200000E-12
+AS=+5.71200000E-12 PD=+2.47600000E-05 PS=+2.47600000E-05 NRD=+2.26890756E-02
+NRS=+2.26890756E-02 M=1.0
M9 NET0371 NET0355 VSS! VSS! NCH L=1.2E-6 W=11.9E-6 AD=+5.71200000E-12
+AS=+5.71200000E-12 PD=+2.47600000E-05 PS=+2.47600000E-05 NRD=+2.26890756E-02
+NRS=+2.26890756E-02 M=1.0

```
M23 NET0211 NET0261 NET0371 NET0379  NCH  L=2.26E-6 W=1E-6 AD=+4.80000000E-
13
+AS=+4.80000000E-13 PD=+2.96000000E-06 PS=+2.96000000E-06 NRD=+2.70000000E-01
+NRS=+2.70000000E-01 M=1.0
M27 NET0203 NET0317 NET0203 NET0383  NCH  L=1.2E-6 W=13E-6 AD=+6.24000000E-
12
+AS=+6.24000000E-12 PD=+2.69600000E-05 PS=+2.69600000E-05 NRD=+2.07692308E-02
+NRS=+2.07692308E-02 M=1.0
M24 NET0389 VSS! NET0307 VSS!  NCH  L=1.2E-6 W=30E-6 AD=+1.44000000E-11
+AS=+1.44000000E-11 PD=+6.09600000E-05 PS=+6.09600000E-05 NRD=+9.00000000E-03
+NRS=+9.00000000E-03 M=1.0
M32 NET0389 NET0389 VSS! VSS!  NCH  L=1.2E-6 W=13E-6 AD=+6.24000000E-12
+AS=+6.24000000E-12 PD=+2.69600000E-05 PS=+2.69600000E-05 NRD=+2.07692308E-02
+NRS=+2.07692308E-02 M=1.0
M28 NET0203 NET0261 NET0325 NET0383  NCH  L=2.26E-6 W=1E-6 AD=+4.80000000E-
13
+AS=+4.80000000E-13 PD=+2.96000000E-06 PS=+2.96000000E-06 NRD=+2.70000000E-01
+NRS=+2.70000000E-01 M=1.0
M30 NET0342 NET0342 VSS! VSS!  NCH  L=1.2E-6 W=13E-6 AD=+6.24000000E-12
+AS=+6.24000000E-12 PD=+2.69600000E-05 PS=+2.69600000E-05 NRD=+2.07692308E-02
+NRS=+2.07692308E-02 M=1.0


* FILE NAME: CMOSP18_TIEDOWN_SCHEMATIC.S.
* SUBCIRCUIT FOR CELL: TIEDOWN.
* GENERATED FOR: HSPICES.
* GENERATED ON AUG  2 02:17:17 2011.

* TERMINAL MAPPING: GNDPOINT = GNDPOINT
.SUBCKT TIEDOWN_G1 GNDPOINT
R3 0 GNDPOINT  1.0


* END OF SUBCIRCUIT DEFINITION.
.ENDS TIEDOWN_G1

 * INCLUDE FILES

* END OF NETLIST
.AC DEC       11.0000       10.0000      1.000000E+06
.TEMP    25.0000
.OP
.save
.OPTION  INGOLD=2 ARTIST=2 PSF=2
+       PROBE=0
.END
```

APPENDIX – F

F.1 SPICE file for the output listing file of the Universal Amplifier Module

This is the /encs/bin/hspice wrapper script

adding to existing value of LM_LICENSE_FILE
SNPSLMD_LICENSE_FILE is set to /encs/Share/synopsys/license.dat
LM_LICENSE_FILE is set to /encs/Share/synopsys/license.dat:5280@license-cadence.encs.concordia.ca

Using: /bin/time /CMC/tools/meta/sparcOS5/hspice netlist_vcvs.sp
****** HSPICE -- C-2009.03-SP1 32-BIT (May 25 2009) sunos ******
Copyright (C) 2009 Synopsys, Inc. All Rights Reserved.
Unpublished-rights reserved under US copyright laws.
This program is protected by law and is subject to the
terms and conditions of the license agreement from Synopsys.
Use of this program is your acceptance to be bound by the
license agreement. HSPICE is the trademark of Synopsys, Inc.
Input File: netlist_vcvs.sp
lic:
lic: FLEXlm: v8.5b
lic: USER: m_talukd HOSTNAME: victoria.ece.concordia.ca
lic: HOSTID: 832fa025 PID: 10433
lic: Using FLEXlm license file:
lic: 1702@license-synopsys.encs.concordia.ca
lic: Checkout 1 hspice
lic: License/Maintenance for hspice will expire on 31-may-2012/2011.03
lic: FLOATING license(s) on SERVER license-synopsys.encs.concordia.ca
lic:
Init: read install configuration file: /CMC/tools/meta/meta.cfg
Init: hspice initialization file: /CMC/tools/meta/hspice.ini
.option runlvl

warning ic file for .op will not be created since .save exists

lic: Using FLEXlm license file:
lic: 1702@license-synopsys.encs.concordia.ca
lic: Checkout 1 cdsaawaves
lic: License/Maintenance for cdsaawaves will expire on 31-may-2012/2011.03
lic: FLOATING license(s) on SERVER license-synopsys.encs.concordia.ca
lic:
1****** HSPICE -- C-2009.03-SP1 32-BIT (May 25 2009) sunos ******
******

```
* # file name: /nfs/thesis/m/m_talukd/simulation/myuamckt/hspices/schematic/

 ******  circuit name directory
 circuit number to circuit name directory
  number circuitname                  definition        multiplier
       0 main circuit
       1 xi1.                         tiedown_g1        1.00
  **warning** (netlist_vcvs.sp:155) both nodes of resistor xi1^r3 defined in subckt tiedown_g1
are connected together
  **warning** (netlist_vcvs.sp:14) in element=c0 defined in subckt 0                  capacitance =
1.00     >= 0.1 farad, please verify it.
 ******************************************************************************
 ***        model parameters  model name:   0:pch.2    model type:pmos    ***
 ******************************************************************************

   *** general parameters ***
    deriv=   0.

   ***  level 49  model parameters  ***

      hspver=    2006.03            level=           49
     version=       3.24          paramchk=         0
      apwarn=          1             lite=           0
      vgslim=          0          binUnit=           2
      capMod=          3            xpart=           1
      mobMod=          1           nqsMod=           0
      stiMod=          0              elm=           5
      sfvtflag=        0              tox=   4.08e-09 meter
         xj=    1.7e-07 meter       binflag=         0
        lmin=    1.2e-06 meter         lmax=      1e-05 meter
        wmin=      1e-05 meter         wmax=0.000900001 meter
        lref=         0 meter         wref=         0 meter
        lint=    1.5e-08 meter         wint=      5e-09 meter
       lmult=          1             wmult=         1
            ll=         0               lln=        -1
           lw=          0              lwn=         1
          lwl=          0               wl=         0
          wln=          1               ww=          0
          wwn=          1               wwl=         0
          dwg=          0 m/V             dwb=         0 m/V^1/2
           xl=     -2e-08               xw=          0
           a0=    1.03857               ags=       0.02 V^-1
           b0=          0 meter          b1=          0 meter
        keta=  0.0268378 V^-1           voff=    -0.1274 V
       ngate=          0 cm^-3          vbx=          0 V
        vbm=         -3 V               xt=   1.55e-07 meter
```

vth0= -0.435987 V nch= 3.9e+17 cm^-3
nsub= 6e+16 cm^-3 nlx= 0 meter
gamma1= 0 V^-1/2 gamma2= 0 V^-1/2
k1= 0.535645 V^1/2 k2= 0.035584
k3= 0 k3b= 0 V^-1
w0= 0 meter dvt0= 0
dvt1= 0 dvt2= 0 V^-1
dvt0w= 0 meter^-1 dvt1w= 0 meter^-1
dvt2w= 0 V^-1 dsub= 0
eta0= 5e-05 etab= -5e-05 V^-1
u0= 0.0109952 m^2/V/sec ua=8.62531e-10 m/V
ub= 6.402e-19 (m/V)^2 uc=-8.85514e-11 V^-1
vsat= 151307 m/sec a1= 0 v^-1
a2= 0.4 delta= 0.01 V
rdsw= 530 ohm-um prwg= 0 V^-1
prwb= 0 V^-1/2 wr= 1
pclm= 0.573864 pdiblc1= 1e-06
pdiblc2=0.000477273 pdiblcb= 0.01 V^-1
pscbe1=1.80398e+08 V/m pscbe2= 5e-07 V/m
drout= 0 pvag= 0
nfactor= 1 cdsc= 0 f/m^2
cdscb= 0 f/V/m^2 cdscd= 0 f/V/m^2
cit= -0.0001 f/m^2 alpha0= 0 m/V
beta0= 22.6783 V dlc= 2e-09 meter
dwc= 5e-09 meter clc= 1e-07 meter
cle= 0.6 cgso= 3.28e-10 f/m
cgdo= 3.28e-10 f/m cgbo=8.46356e-11 f/m
cgsl= 0 f/m cgdl= 0 f/m
ckappa= 0.6 cf= 0 f/m
acde= 1 m/V moin= 15 V^1/2
toxm= 4.08e-09 m dtoxcv= 0 m
vfb (not used) alpha1= 6.87305 1/V
ijth= 0.1 A noff= 1
voffcv= 0 tcj= 0.0009739 1/K
tcjsw=0.000413072 1/K tcjswg=0.000413072 1/K
tpb= 0.00157203 V/K tpbsw= 0.00157203 V/K
tpbswg= 0.00157203 V/K llc= -0.039
lwc= 0 lwlc= 0
wlc= 0 wwc= 0
wwlc= 0 tnom= 298.15 K
kt1= -0.229588 V kt1l= 0
kt2= -0.0240311 ute= -0.838555
ua1= 1.224e-09 m/V ub1=-1.39771e-18 (m/V)^2
uc1=-6.69492e-12 m/V^2 at= 10000 m/s
prt= 0
using Berkeley noise model noiMod= 2

```
      noia=    9.5e+18              noib=     100000
      noic=    1.4e-12               em=      3e+07
        ef=      1.064              af=         1
        kf=          0           gdsnoi=-1.23457e-29
      using Berkeley diodes         using ACM
      acm=         12              hdif=     2e-07 meter
      ldif=     9e-08 meter           js=   2.5e-07 amp/m^2
      jsw=   1.2e-12 amp/m            xti=         3
        nj=        1               cj=  0.001121 f/m^2
        mj=    0.4476               pb=  0.895226 V
     cjsw= 2.481e-10 f/m            mjsw=  0.368362
      php (not used)               pbsw=  0.895226 V
    cjgate (not used)              cjswg= 4.221e-10 f/m
     mjswg=  0.368362               pbswg=  0.895226 V
       la0=7.54812e-08             lketa=-2.04627e-09
     lvoff=-1.90913e-09              lvth0=-2.48141e-08
       lk1=1.87836e-08               lk2=-5.48717e-09
     leta0=      3e-14             lu0=-1.29397e-09
       lua=-3.90411e-16               lub=4.50063e-25
       luc=1.98736e-17             lvsat= -0.0130028
    lpclm=2.60057e-07            lpdiblc2=5.20114e-09
   lpscbe1=    195.043              lkt1=-1.53332e-08
      lkt2=-3.07259e-09               lute=9.62097e-08
      lub1=4.80233e-26               luc1=2.08975e-17
     peta0=      3e-21
*******************************************************************************
***       model parameters  model name:   0:pch.6    model type:pmos   ***
*******************************************************************************

  *** general parameters ***
  deriv=   0.

  ***  level 49  model parameters  ***

    hspver=    2006.03              level=         49
   version=       3.24           paramchk=          0
    apwarn=          1              lite=          0
    vgslim=          0            binUnit=          2
    capMod=          3              xpart=          1
    mobMod=          1             nqsMod=          0
    stiMod=          0               elm=          5
  sfvtflag=          0              tox=   4.08e-09 meter
        xj=    1.7e-07 meter       binflag=          0
      lmin=    1.2e-06 meter         lmax=      1e-05 meter
      wmin=    1.2e-06 meter         wmax=      1e-05 meter
      lref=          0 meter         wref=          0 meter
```

lint= 1.5e-08 meter wint= 5e-09 meter
lmult= 1 wmult= 1
ll= 0 lln= -1
lw= 0 lwn= 1
lwl= 0 wl= 0
wln= 1 ww= 0
wwn= 1 wwl= 0
dwg= 0 m/V dwb= 0 m/V^1/2
xl= -2e-08 xw= 0
a0= 1.04404 ags= 0.02 V^-1
b0= 0 meter b1= 0 meter
keta= 0.0261287 V^-1 voff= -0.127341 V
ngate= 0 cm^-3 vbx= 0 V
vbm= -3 V xt= 1.55e-07 meter
vth0= -0.437329 V nch= 3.9e+17 cm^-3
nsub= 6e+16 cm^-3 nlx= 0 meter
gamma1= 0 V^-1/2 gamma2= 0 V^-1/2
k1= 0.534458 V^1/2 k2= 0.0361579
k3= 0 k3b= 0 V^-1
w0= 0 meter dvt0= 0
dvt1= 0 dvt2= 0 V^-1
dvt0w= 0 meter^-1 dvt1w= 0 meter^-1
dvt2w= 0 V^-1 dsub= 0
eta0= 5e-05 etab= -5e-05 V^-1
u0= 0.0111214 m^2/V/sec ua=8.45286e-10 m/V
ub= 7.084e-19 (m/V)^2 uc=-8.04939e-11 V^-1
vsat= 151307 m/sec a1= 0 v^-1
a2= 0.4 delta= 0.01 V
rdsw= 530 ohm-um prwg= 0 V^-1
prwb= 0 V^-1/2 wr= 1
pclm= 0.573864 pdiblc1= 1e-06
pdiblc2=0.000477273 pdiblcb= 0.01 V^-1
pscbe1=1.80398e+08 V/m pscbe2= 5e-07 V/m
drout= 0 pvag= 0
nfactor= 1 cdsc= 0 f/m^2
cdscb= 0 f/V/m^2 cdscd= 0 f/V/m^2
cit= -0.0001 f/m^2 alpha0= 0 m/V
beta0= 22.6783 V dlc= 2e-09 meter
dwc= 5e-09 meter clc= 1e-07 meter
cle= 0.6 cgso= 3.28e-10 f/m
cgdo= 3.28e-10 f/m cgbo=8.46356e-11 f/m
cgsl= 0 f/m cgdl= 0 f/m
ckappa= 0.6 cf= 0 f/m
acde= 1 m/V moin= 15 V^1/2
toxm= 4.08e-09 m dtoxcv= 0 m
vfb (not used) alpha1= 6.87305 1/V

ijth= 0.1 A noff= 1
voffcv= 0 tcj= 0.0009739 1/K
tcjsw=0.000413072 1/K tcjswg=0.000413072 1/K
tpb= 0.00157203 V/K tpbsw= 0.00157203 V/K
tpbswg= 0.00157203 V/K llc= -0.039
lwc= 0 lwlc= 0
wlc= 0 wwc= 0
wwlc= 0 tnom= 298.15 K
kt1= -0.230315 V kt1l= 0
kt2= -0.0241558 ute= -0.84921
ua1= 1.224e-09 m/V ub1=-1.40527e-18 (m/V)^2
uc1=-9.47004e-12 m/V^2 at= 10000 m/s
prt= 0
using Berkeley noise model noiMod= 2
noia= 9.5e+18 noib= 100000
noic= 1.4e-12 em= 3e+07
ef= 1.064 af= 1
kf= 0 gdsnoi=-1.23457e-29
using Berkeley diodes using ACM
acm= 12 hdif= 2e-07 meter
ldif= 9e-08 meter js= 2.5e-07 amp/m^2
jsw= 1.2e-12 amp/m xti= 3
nj= 1 cj= 0.001121 f/m^2
mj= 0.4476 pb= 0.895226 V
cjsw= 2.481e-10 f/m mjsw= 0.368362
php (not used) pbsw= 0.895226 V
cjgate (not used) cjswg= 4.221e-10 f/m
mjswg= 0.368362 pbswg= 0.895226 V
la0=6.87813e-08 lketa=-1.26627e-09
lvoff=-1.46836e-09 lvth0=-2.42799e-08
lk1=1.81844e-08 lk2=-5.28064e-09
leta0= 3e-14 lu0=-1.30552e-09
lua=-3.93561e-16 lub=4.21946e-25
luc=1.88832e-17 lvsat= -0.0130028
lpclm=2.60057e-07 lpdiblc2=5.20114e-09
lpscbe1= 195.043 lkt1=-1.63009e-08
lkt2=-3.31284e-09 lute= 9.6645e-08
lub1=5.44273e-26 luc1= 1.8277e-17
wa0=-5.45988e-08 wketa=7.08436e-09
wvoff=-5.87989e-10 wvth0=1.34068e-08
wk1=1.18551e-08 wk2=-5.73278e-09
wu0=-1.26108e-09 wua=1.72276e-16
wub=-6.81325e-25 wuc=-8.04953e-17
wkt1=7.25675e-09 wkt2=1.24568e-09
wute=1.06441e-07 wub1=7.55269e-26
wuc1=2.77234e-17 pa0=6.69322e-14

```
    pketa=-7.79217e-15             pvoff=-4.40328e-15
    pvth0=-5.33647e-15               pk1=5.98624e-15
     pk2=-2.06331e-15              peta0=      3e-21
     pu0=1.15432e-16               pua=3.14656e-23
     pub=2.80886e-31               puc= 9.8941e-24
    pkt1= 9.6667e-15              pkt2=2.40007e-15
     pute=-4.3481e-15              pub1=-6.39762e-32
     puc1= 2.6179e-23
*****************************************************************************
***       model parameters  model name:   0:nch.3    model type:nmos   ***
*****************************************************************************

 *** general parameters ***
  deriv=   0.

 ***  level 49  model parameters  ***

   hspver=    2006.03             level=         49
  version=       3.24           paramchk=          0
   apwarn=          1              lite=          0
   vgslim=          0           binUnit=          2
   capMod=          3              xpart=          1
   mobMod=          1              nqsMod=          0
   stiMod=          0               elm=          5
 sfvtflag=          0               tox=   4.08e-09 meter
       xj=    1.6e-07 meter       binflag=          0
     lmin=      5e-07 meter         lmax=    1.2e-06 meter
     wmin=      1e-05 meter         wmax=0.000900001 meter
     lref=          0 meter         wref=          0 meter
     lint=      1e-08 meter         wint=      3e-09 meter
    lmult=          1              wmult=          1
       ll=          0               lln=         -1
       lw=          0               lwn=          1
      lwl=          0                wl=          0
      wln=          1               ww=          0
      wwn=          1               wwl=          0
      dwg=          0 m/V           dwb=          0 m/V^1/2
       xl=     -2e-08               xw=          0
       a0=  -0.291157               ags=  0.0462474 V^-1
       b0=          0 meter         b1=          0 meter
    keta= -0.0159275 V^-1          voff=  -0.162119 V
   ngate=          0 cm^-3          vbx=          0 V
     vbm=         -3 V              xt=   1.55e-07 meter
    vth0=   0.479324 V              nch=    3.9e+17 cm^-3
    nsub=      6e+16 cm^-3          nlx=          0 meter
  gamma1=          0 V^-1/2       gamma2=          0 V^-1/2
```

k1= 0.531805 V^1/2 k2= 0.00486491
k3= 0 k3b= 0 V^-1
w0= 0 meter dvt0= 0
dvt1= 0 dvt2= 0 V^-1
dvt0w= 0 meter^-1 dvt1w= 0 meter^-1
dvt2w= 0 V^-1 dsub= 0
eta0=1.71429e-05 etab=-1.71429e-05 V^-1
u0= 0.0438136 m^2/V/sec ua=-1.03475e-09 m/V
ub=3.01008e-18 (m/V)^2 uc=1.46789e-10 V^-1
vsat= 85658.6 m/sec a1= 0 v^-1
a2= 0.99 delta= 0.01 V
rdsw= 170 ohm-um prwg= 0 V^-1
prwb= 0 V^-1/2 wr= 1
pclm= 0.868717 pdiblc1= 1e-06
pdiblc2= 0.00168476 pdiblcb= 0.01 V^-1
pscbe1= 4e+08 V/m pscbe2= 1e-06 V/m
drout= 0 pvag= 0
nfactor= 1 cdsc= 0 f/m^2
cdscb= 0 f/V/m^2 cdscd= 0 f/V/m^2
cit=-0.000157886 f/m^2 alpha0= 0 m/V
beta0= 11.5926 V dlc= 3e-09 meter
dwc= 3e-09 meter clc= 1e-07 meter
cle= 0.6 cgso= 3.665e-10 f/m
cgdo= 3.665e-10 f/m cgbo=5.07814e-11 f/m
cgsl= 0 f/m cgdl= 0 f/m
ckappa= 0.6 cf= 0 f/m
acde= 1 m/V moin= 15 V^1/2
toxm= 4.08e-09 m dtoxcv= 0 m
vfb (not used) alpha1= 0.448151 1/V
ijth= 0.1 A noff= 1
voffcv= 0 tcj= 0.00104029 1/K
tcjsw=0.000645489 1/K tcjswg=0.000645489 1/K
tpb= 0.00155431 V/K tpbsw= 0.00155431 V/K
tpbswg= 0.00155431 V/K llc= -0.039
lwc= 0 lwlc= 0
wlc= 0 wwc= 0
wwlc= 0 tnom= 298.15 K
kt1= -0.229028 V kt1l= 0
kt2= -0.0316119 ute= -1.35047
ua1=1.22662e-09 m/V ub1=-8.57439e-20 (m/V)^2
uc1=6.78868e-11 m/V^2 at= 20000 m/s
prt= 0
using Berkeley noise model noiMod= 2
noia= 2e+19 noib= 12000
noic= 2.5e-13 em= 3e+07
ef= 0.874 af= 1

```
       kf=          0             gdsnoi=-1.23457e-29
      using Berkeley diodes          using ACM
      acm=         12              hdif=     2e-07 meter
     ldif=     9e-08 meter           js=   3.5e-07 amp/m^2
      jsw=  1.45e-12 amp/m           xti=         3
       nj=         1              cj=0.00100027 f/m^2
       mj=  0.359526                pb=  0.688268 V
     cjsw=2.04055e-10 f/m            mjsw=  0.200388
      php (not used)               pbsw=  0.688268 V
    cjgate (not used)              cjswg=3.34055e-10 f/m
    mjswg=   0.43879               pbswg=  0.688268 V
      la0=4.58143e-07              lags=-3.0447e-08
    lketa=-8.95403e-09             lvoff=1.57353e-08
    lvth0=3.94276e-09              lk1=-7.21425e-09
      lk2=1.70315e-09              leta0=3.81318e-11
    letab=-3.81143e-11             lu0=1.04061e-09
      lua=7.98297e-17              lub=-1.56309e-25
      luc=-9.6699e-18              lvsat=-0.000762286
    lpclm=1.52457e-07              lpdiblc2=1.52568e-09
     lcit=3.02627e-10              lkt1=5.78268e-09
     lkt2=1.55708e-09              lute=-2.66305e-07
     lua1=-3.04467e-18             lub1=-1.20042e-24
     luc1=-6.51727e-17             peta0=    7.5e-21
*******************************************************************************
***       model parameters  model name:   0:nch.6    model type:nmos   ***
*******************************************************************************

 *** general parameters ***
  deriv=   0.

 ***  level 49  model parameters  ***

   hspver=    2006.03              level=         49
  version=       3.24            paramchk=          0
   apwarn=          1              lite=          0
   vgslim=          0            binUnit=          2
   capMod=          3              xpart=          1
   mobMod=          1              nqsMod=          0
   stiMod=          0              elm=          5
 sfvtflag=          0              tox=   4.08e-09 meter
       xj=    1.6e-07 meter       binflag=          0
     lmin=    1.2e-06 meter         lmax=      1e-05 meter
     wmin=    1.2e-06 meter         wmax=      1e-05 meter
     lref=          0 meter         wref=          0 meter
     lint=      1e-08 meter         wint=      3e-09 meter
    lmult=          1              wmult=          1
```

ll= 0 lln= -1
lw= 0 lwn= 1
lwl= 0 wl= 0
wln= 1 ww= 0
wwn= 1 wwl= 0
dwg= 0 m/V dwb= 0 m/V^1/2
xl= -2e-08 xw= 0
a0= 0.40626 ags= 0.02 V^-1
b0= 0 meter b1= 0 meter
keta= 0.0148948 V^-1 voff= -0.139582 V
ngate= 0 cm^-3 vbx= 0 V
vbm= -3 V xt= 1.55e-07 meter
vth0= 0.430392 V nch= 3.9e+17 cm^-3
nsub= 6e+16 cm^-3 nlx= 0 meter
gamma1= 0 V^-1/2 gamma2= 0 V^-1/2
k1= 0.508509 V^1/2 k2= 0.0173102
k3= 0 k3b= 0 V^-1
w0= 0 meter dvt0= 0
dvt1= 0 dvt2= 0 V^-1
dvt0w= 0 meter^-1 dvt1w= 0 meter^-1
dvt2w= 0 V^-1 dsub= 0
eta0= 5e-05 etab= -5e-05 V^-1
u0= 0.0427303 m^2/V/sec ua=-5.37713e-10 m/V
ub=2.25379e-18 (m/V)^2 uc=1.06578e-10 V^-1
vsat= 90678 m/sec a1= 0 v^-1
a2= 0.99 delta= 0.01 V
rdsw= 170 ohm-um prwg= 0 V^-1
prwb= 0 V^-1/2 wr= 1
pclm= 0.775529 pdiblc1= 1e-06
pdiblc2=0.000396818 pdiblcb= 0.01 V^-1
pscbe1=1.73636e+08 V/m pscbe2= 1e-06 V/m
drout= 0 pvag= 0
nfactor= 1 cdsc= 0 f/m^2
cdscb= 0 f/V/m^2 cdscd= 0 f/V/m^2
cit=-0.000126759 f/m^2 alpha0= 0 m/V
beta0= 11.5926 V dlc= 3e-09 meter
dwc= 3e-09 meter clc= 1e-07 meter
cle= 0.6 cgso= 3.665e-10 f/m
cgdo= 3.665e-10 f/m cgbo=5.07814e-11 f/m
cgsl= 0 f/m cgdl= 0 f/m
ckappa= 0.6 cf= 0 f/m
acde= 1 m/V moin= 15 V^1/2
toxm= 4.08e-09 m dtoxcv= 0 m
vfb (not used) alpha1= 0.448151 1/V
ijth= 0.1 A noff= 1
voffcv= 0 tcj= 0.00104029 1/K

tcjsw=0.000645489 1/K tcjswg=0.000645489 1/K
tpb= 0.00155431 V/K tpbsw= 0.00155431 V/K
tpbswg= 0.00155431 V/K llc= -0.039
lwc= 0 lwlc= 0
wlc= 0 wwc= 0
wwlc= 0 tnom= 298.15 K
kt1= -0.223178 V kt1l= 0
kt2= -0.0304697 ute= -1.58095
ua1= 1.224e-09 m/V ub1=-1.06431e-18 (m/V)^2
uc1=2.49678e-11 m/V^2 at= 20000 m/s
prt= 0
using Berkeley noise model noiMod= 2
noia= 2e+19 noib= 12000
noic= 2.5e-13 em= 3e+07
ef= 0.874 af= 1
kf= 0 gdsnoi=-1.23457e-29
using Berkeley diodes using ACM
acm= 12 hdif= 2e-07 meter
ldif= 9e-08 meter js= 3.5e-07 amp/m^2
jsw= 1.45e-12 amp/m xti= 3
nj= 1 cj=0.00100027 f/m^2
mj= 0.359526 pb= 0.688268 V
cjsw=2.04055e-10 f/m mjsw= 0.200388
php (not used) pbsw= 0.688268 V
cjgate (not used) cjswg=3.34055e-10 f/m
mjswg= 0.43879 pbswg= 0.688268 V
la0=-3.58899e-07 lketa=-4.51899e-08
lvoff=-1.08061e-08 lvth0=6.07061e-08
lk1=1.71616e-08 lk2=-1.21386e-08
leta0= 1.75e-14 lu0=3.04409e-09
lua=-5.0678e-16 lub=7.88254e-25
luc=3.98429e-17 lvsat=-0.00675303
lpclm=2.43734e-07 lpdiblc2=3.01969e-09
lpscbe1= 262.582 lcit=2.66521e-10
lkt1=-4.67462e-10 lkt2=4.08732e-10
lute=5.65415e-09 lub1=-4.13336e-26
luc1=-7.34375e-18 wa0=-1.07861e-08
wketa=-1.29242e-08 wvoff=5.54854e-10
wvth0= 7.8115e-10 wk1=4.22165e-08
wk2=-1.39575e-08 wu0=-8.56866e-09
wua=-2.7926e-16 wub=-1.42821e-25
wuc=-1.7297e-17 wvsat=-0.000191046
wpclm=-1.91037e-08 wkt1=-8.68815e-09
wkt2=2.03928e-09 wute=9.53953e-09
wub1=-5.66354e-25 wuc1=-1.33238e-16
pa0=9.28455e-14 pketa= 1.9809e-14

```
     pvoff=3.34524e-15              pvth0=-9.31688e-16
       pk1=-2.25142e-14               pk2=1.02462e-14
     peta0=    7.5e-21              pu0=2.47569e-15
       pua=4.24334e-22                pub=-5.06556e-31
       puc=-8.58813e-24             pvsat=1.90272e-09
     ppclm=1.90272e-13                pkt1=4.71091e-15
      pkt2=-4.13038e-15               pute=-5.70817e-14
      pub1=4.17613e-31               puc1=7.41758e-23
*************************************************************************
***       model parameters  model name:   0:nch.2    model type:nmos   ***
*************************************************************************

 *** general parameters ***
  deriv=   0.

 ***  level 49  model parameters  ***

    hspver=    2006.03             level=         49
   version=       3.24           paramchk=          0
    apwarn=          1              lite=          0
    vgslim=          0           binUnit=          2
    capMod=          3              xpart=          1
    mobMod=          1              nqsMod=          0
    stiMod=          0               elm=          5
  sfvtflag=          0               tox=   4.08e-09 meter
        xj=    1.6e-07 meter       binflag=          0
      lmin=    1.2e-06 meter         lmax=      1e-05 meter
      wmin=      1e-05 meter         wmax=0.000900001 meter
      lref=          0 meter         wref=          0 meter
      lint=      1e-08 meter         wint=      3e-09 meter
     lmult=          1              wmult=          1
        ll=          0               lln=         -1
        lw=          0               lwn=          1
       lwl=          0                wl=          0
       wln=          1                ww=          0
       wwn=          1               wwl=          0
       dwg=          0 m/V            dwb=          0 m/V^1/2
        xl=     -2e-08                xw=          0
        a0=   0.405181                ags=       0.02 V^-1
        b0=          0 meter          b1=          0 meter
     keta=  0.0136016 V^-1           voff=  -0.139527 V
    ngate=          0 cm^-3          vbx=          0 V
      vbm=         -3 V              xt=   1.55e-07 meter
     vth0=    0.43047 V              nch=    3.9e+17 cm^-3
     nsub=      6e+16 cm^-3           nlx=          0 meter
   gamma1=          0 V^-1/2        gamma2=          0 V^-1/2
```

k1= 0.512733 V^1/2 k2= 0.0159136
k3= 0 k3b= 0 V^-1
w0= 0 meter dvt0= 0
dvt1= 0 dvt2= 0 V^-1
dvt0w= 0 meter^-1 dvt1w= 0 meter^-1
dvt2w= 0 V^-1 dsub= 0
eta0= 5e-05 etab= -5e-05 V^-1
u0= 0.0418729 m^2/V/sec ua=-5.65655e-10 m/V
ub= 2.2395e-18 (m/V)^2 uc=1.04847e-10 V^-1
vsat= 90658.9 m/sec a1= 0 v^-1
a2= 0.99 delta= 0.01 V
rdsw= 170 ohm-um prwg= 0 V^-1
prwb= 0 V^-1/2 wr= 1
pclm= 0.773617 pdiblc1= 1e-06
pdiblc2=0.000396818 pdiblcb= 0.01 V^-1
pscbe1=1.73636e+08 V/m pscbe2= 1e-06 V/m
drout= 0 pvag= 0
nfactor= 1 cdsc= 0 f/m^2
cdscb= 0 f/V/m^2 cdscd= 0 f/V/m^2
cit=-0.000126759 f/m^2 alpha0= 0 m/V
beta0= 11.5926 V dlc= 3e-09 meter
dwc= 3e-09 meter clc= 1e-07 meter
cle= 0.6 cgso= 3.665e-10 f/m
cgdo= 3.665e-10 f/m cgbo=5.07814e-11 f/m
cgsl= 0 f/m cgdl= 0 f/m
ckappa= 0.6 cf= 0 f/m
acde= 1 m/V moin= 15 V^1/2
toxm= 4.08e-09 m dtoxcv= 0 m
vfb (not used) alpha1= 0.448151 1/V
ijth= 0.1 A noff= 1
voffcv= 0 tcj= 0.00104029 1/K
tcjsw=0.000645489 1/K tcjswg=0.000645489 1/K
tpb= 0.00155431 V/K tpbsw= 0.00155431 V/K
tpbswg= 0.00155431 V/K llc= -0.039
lwc= 0 lwlc= 0
wlc= 0 wwc= 0
wwlc= 0 tnom= 298.15 K
kt1= -0.224047 V kt1l= 0
kt2= -0.0302657 ute= -1.57999
ua1= 1.224e-09 m/V ub1=-1.12098e-18 (m/V)^2
uc1= 1.1636e-11 m/V^2 at= 20000 m/s
prt= 0
using Berkeley noise model noiMod= 2
noia= 2e+19 noib= 12000
noic= 2.5e-13 em= 3e+07
ef= 0.874 af= 1

```
       kf=         0            gdsnoi=-1.23457e-29
      using Berkeley diodes         using ACM
      acm=        12              hdif=     2e-07 meter
     ldif=     9e-08 meter           js=   3.5e-07 amp/m^2
      jsw=  1.45e-12 amp/m          xti=        3
       nj=        1              cj=0.00100027 f/m^2
       mj=  0.359526               pb=  0.688268 V
     cjsw=2.04055e-10 f/m           mjsw=  0.200388
      php (not used)              pbsw=  0.688268 V
    cjgate (not used)             cjswg=3.34055e-10 f/m
     mjswg=   0.43879             pbswg=  0.688268 V
      la0=-3.49609e-07             lketa=-4.32078e-08
     lvoff=-1.04713e-08            lvth0=6.06129e-08
      lk1=1.49088e-08              lk2=-1.11134e-08
     leta0=   1.75e-14            lu0=3.29181e-09
      lua=-4.64322e-16              lub=7.37568e-25
      luc=3.89836e-17             lvsat=-0.00656264
    lpclm=2.62773e-07           lpdiblc2=3.01969e-09
   lpscbe1=    262.582            lcit=2.66521e-10
     lkt2=-4.55349e-12             lute=-5.74395e-11
     lub1=4.52732e-28              luc1=7.82777e-20
     peta0=    7.5e-21
*******************************************************************************
***       model parameters  model name:   0:nch.10   model type:nmos   ***
*******************************************************************************

 *** general parameters ***
  deriv=   0.

 ***  level 49  model parameters  ***

    hspver=    2006.03             level=        49
   version=       3.24           paramchk=         0
    apwarn=          1              lite=         0
    vgslim=          0            binUnit=         2
    capMod=          3              xpart=         1
    mobMod=          1             nqsMod=         0
    stiMod=          0               elm=         5
  sfvtflag=          0              tox=   4.08e-09 meter
        xj=    1.6e-07 meter       binflag=         0
      lmin=    1.2e-06 meter         lmax=      1e-05 meter
      wmin=      5e-07 meter         wmax=    1.2e-06 meter
      lref=          0 meter         wref=          0 meter
      lint=      1e-08 meter          wint=      3e-09 meter
     lmult=          1             wmult=         1
       ll=          0              lln=        -1
```

lw= 0 lwn= 1
lwl= 0 wl= 0
wln= 1 ww= 0
wwn= 1 wwl= 0
dwg= 0 m/V dwb= 0 m/V^1/2
xl= -2e-08 xw= 0
a0= 0.324591 ags= 0.02 V^-1
b0= 0 meter b1= 0 meter
keta= 0.00382927 V^-1 voff= -0.138834 V
ngate= 0 cm^-3 vbx= 0 V
vbm= -3 V xt= 1.55e-07 meter
vth0= 0.434015 V nch= 3.9e+17 cm^-3
nsub= 6e+16 cm^-3 nlx= 0 meter
gamma1= 0 V^-1/2 gamma2= 0 V^-1/2
k1= 0.560017 V^1/2 k2= 0.00168545
k3= 0 k3b= 0 V^-1
w0= 0 meter dvt0= 0
dvt1= 0 dvt2= 0 V^-1
dvt0w= 0 meter^-1 dvt1w= 0 meter^-1
dvt2w= 0 V^-1 dsub= 0
eta0= 5e-05 etab= -5e-05 V^-1
u0= 0.0348277 m^2/V/sec ua=-8.8744e-10 m/V
ub=2.25846e-18 (m/V)^2 uc=1.03158e-10 V^-1
vsat= 90622.6 m/sec a1= 0 v^-1
a2= 0.99 delta= 0.01 V
rdsw= 170 ohm-um prwg= 0 V^-1
prwb= 0 V^-1/2 wr= 1
pclm= 0.769987 pdiblc1= 1e-06
pdiblc2=0.000396819 pdiblcb= 0.01 V^-1
pscbe1=1.73636e+08 V/m pscbe2= 1e-06 V/m
drout= 0 pvag= 0
nfactor= 1 cdsc= 0 f/m^2
cdscb= 0 f/V/m^2 cdscd= 0 f/V/m^2
cit=-0.000126723 f/m^2 alpha0= 0 m/V
beta0= 11.5926 V dlc= 3e-09 meter
dwc= 3e-09 meter clc= 1e-07 meter
cle= 0.6 cgso= 3.665e-10 f/m
cgdo= 3.665e-10 f/m cgbo=5.07814e-11 f/m
cgsl= 0 f/m cgdl= 0 f/m
ckappa= 0.6 cf= 0 f/m
acde= 1 m/V moin= 15 V^1/2
toxm= 4.08e-09 m dtoxcv= 0 m
vfb (not used) alpha1= 0.448151 1/V
ijth= 0.1 A noff= 1
voffcv= 0 tcj= 0.00104029 1/K
tcjsw=0.000645489 1/K tcjswg=0.000645489 1/K

tpb= 0.00155431 V/K tpbsw= 0.00155431 V/K
tpbswg= 0.00155431 V/K llc= -0.039
lwc= 0 lwlc= 0
wlc= 0 wwc= 0
wwlc= 0 tnom= 298.15 K
kt1= -0.231009 V kt1l= 0
kt2= -0.0286887 ute= -1.60809
ua1= 1.224e-09 m/V ub1=-1.53381e-18 (m/V)^2
uc1=-7.31641e-11 m/V^2 at= 20000 m/s
prt= 0
using Berkeley noise model noiMod= 2
noia= 2e+19 noib= 12000
noic= 2.5e-13 em= 3e+07
ef= 0.874 af= 1
kf= 0 gdsnoi=-1.23457e-29
using Berkeley diodes using ACM
acm= 12 hdif= 2e-07 meter
ldif= 9e-08 meter js= 3.5e-07 amp/m^2
jsw= 1.45e-12 amp/m xti= 3
nj= 1 cj=0.00100027 f/m^2
mj= 0.359526 pb= 0.688268 V
cjsw=2.04055e-10 f/m mjsw= 0.200388
php (not used) pbsw= 0.688268 V
cjgate (not used) cjswg=3.34055e-10 f/m
mjswg= 0.43879 pbswg= 0.688268 V
la0=-1.97254e-07 lketa=-2.80272e-08
lvoff=-3.60222e-09 lvth0=6.59205e-08
lk1=1.05124e-08 lk2=-5.41005e-09
leta0= 1.75e-14 lu0=3.70575e-09
lua=-1.91245e-16 lub=4.11704e-25
luc=4.03882e-17 lvsat= -0.0062011
lpclm=2.98928e-07 lpdiblc2=3.01969e-09
lpscbe1= 262.582 lcit= 2.6616e-10
lkt1=-3.08281e-09 lkt2=-3.86688e-09
lute=-1.21905e-08 lub1=3.24336e-25
luc1=4.34149e-17 wa0=8.67267e-08
wketa=2.88033e-10 wvoff=-3.38845e-10
wvth0=-3.54447e-09 wk1=-1.92839e-08
wk2=4.69852e-09 wu0=8.67053e-10
wua=1.38314e-16 wub=-1.48399e-25
wuc=-1.32136e-17 wvsat=-0.000124879
wpclm=-1.24872e-08 wcit=-4.31737e-14
wkt1=6.62534e-10 wkt2=-8.72568e-11
wute= 4.1952e-08 wub1=-5.7683e-27
wuc1=-1.6069e-17 pa0=-1.00159e-13
pketa=-6.8318e-16 pvoff=-5.25613e-15

```
      pvth0=-7.15767e-15          pk1=-1.45749e-14
       pk2=2.21228e-15          peta0=    7.5e-21
       pu0=1.68567e-15           pua=4.75847e-23
       pub=-5.69553e-32          puc=-9.23919e-24
      pvsat=1.24373e-09         ppclm=1.24372e-13
       pcit=4.30275e-19         pkt1=7.83364e-15
       pkt2=9.74704e-16          pute=-3.57751e-14
       pub1=-1.89964e-32         puc1=  1.357e-23


**********************************************************************
****** option summary
******
runlvl  = 3         bypass  = 2
1****** HSPICE -- C-2009.03-SP1 32-BIT (May 25 2009) sunos ******
******
* # file name: /nfs/thesis/m/m_talukd/simulation/myuamckt/hspices/schematic/

 ******  operating point information tnom=  25.000 temp=  25.000 *****
***** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:1       = 1.138e-04 0:2       = 1.138e-04 0:net0203 =-7.396e-01
+0:net0211 =-7.396e-01 0:net0225 =-8.975e-01 0:net0227 =-8.975e-01
+0:net0261 = 6.918e-01 0:net0307 =   0.      0:net0317 = 7.738e-01
+0:net0321 = 7.738e-01 0:net0325 =-7.396e-01 0:net0335 =-8.975e-01
+0:net0342 =-1.080e-09 0:net0343 =-8.975e-01 0:net0349 =-7.652e-01
+0:net0355 =-6.769e-01 0:net0369 =-6.769e-01 0:net0371 =-7.396e-01
+0:net0379 =-7.396e-01 0:net0383 =-7.396e-01 0:net0389 =-1.080e-09
+0:net171  = 6.296e-01 0:net216  = 7.776e-01 0:net233  = 6.296e-01
+0:net259  =-9.456e-02 0:vdd!    = 1.300e+00 0:vss!    =-1.300e+00


****  voltage sources

subckt
element  0:v5       0:v2       0:v3       0:v1       0:v4
 volts      0.       1.300e+00  1.300e+00    0.         0.
 current -1.300e-12 -2.761e-03 -2.761e-03    0.         0.
 power      0.       3.589e-03  3.589e-03    0.         0.

    total voltage source power dissipation=  7.179e-03       watts
```

**** mosfets

subckt						
element	0:m18	0:m25	0:m17	0:m26	0:m9	0:m8
model	0:pch.2	0:pch.6	0:pch.2	0:pch.6	0:pch.2	0:pch.2
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	-2.792e-05	-1.204e-05	-2.792e-05	-1.204e-05	-1.119e-03	-1.119e-03
ibs	5.389e-21	2.412e-21	5.389e-21	2.412e-21	2.146e-19	2.146e-19
ibd	9.451e-17	2.390e-17	9.451e-17	2.390e-17	1.965e-16	1.965e-16
vgs	-6.082e-01	-6.704e-01	-6.082e-01	-6.704e-01	-1.300e+00	-1.300e+00
vds	-5.262e-01	-6.704e-01	-5.262e-01	-6.704e-01	-1.300e+00	-1.300e+00
vbs	0.	0.	0.	0.	0.	0.
vth	-4.574e-01	-4.573e-01	-4.574e-01	-4.573e-01	-4.573e-01	-4.573e-01
vdsat	-1.591e-01	-2.052e-01	-1.591e-01	-2.052e-01	-6.760e-01	-6.760e-01
vod	-1.508e-01	-2.131e-01	-1.508e-01	-2.131e-01	-8.427e-01	-8.427e-01
beta	2.225e-03	5.329e-04	2.225e-03	5.329e-04	3.804e-03	3.804e-03
gam eff	4.939e-01	4.943e-01	4.939e-01	4.943e-01	4.939e-01	4.939e-01
gm	2.909e-04	9.626e-05	2.909e-04	9.626e-05	2.259e-03	2.259e-03
gds	1.396e-06	4.829e-07	1.396e-06	4.829e-07	2.301e-05	2.301e-05
gmb	9.563e-05	3.181e-05	9.563e-05	3.181e-05	8.151e-04	8.151e-04
cdtot	4.978e-14	1.189e-14	4.978e-14	1.189e-14	8.774e-14	8.774e-14
cgtot	2.878e-13	7.166e-14	2.878e-13	7.166e-14	6.285e-13	6.285e-13
cstot	3.492e-13	8.706e-14	3.492e-13	8.706e-14	7.590e-13	7.590e-13
cbtot	1.711e-13	4.147e-14	1.711e-13	4.147e-14	3.158e-13	3.158e-13
cgs	2.581e-13	6.499e-14	2.581e-13	6.499e-14	5.956e-13	5.956e-13
cgd	1.224e-14	2.967e-15	1.224e-14	2.967e-15	2.457e-14	2.457e-14

subckt						
element	0:m31	0:m32	0:m36	0:m35	0:m0	0:m5
model	0:pch.2	0:pch.2	0:pch.2	0:pch.2	0:pch.2	0:pch.2
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	-7.512e-05	-4.663e-05	-4.663e-05	-7.512e-05	-1.515e-05	-3.584e-05
ibs	1.442e-20	8.948e-21	8.948e-21	1.442e-20	2.954e-21	1.020e-16
ibd	1.153e-08	9.468e-09	9.468e-09	1.153e-08	5.163e-17	6.119e-12
vgs	-6.704e-01	-6.082e-01	-6.082e-01	-6.704e-01	-6.082e-01	-7.776e-01
vds	-2.197e+00	-2.197e+00	-2.197e+00	-2.197e+00	-6.082e-01	-1.454e+00
vbs	0.	0.	0.	0.	0.	5.224e-01
vth	-4.526e-01	-4.526e-01	-4.526e-01	-4.526e-01	-4.574e-01	-6.087e-01
vdsat	-2.088e-01	-1.625e-01	-1.625e-01	-2.088e-01	-1.591e-01	-1.786e-01
vod	-2.178e-01	-1.556e-01	-1.556e-01	-2.178e-01	-1.508e-01	-1.689e-01
beta	3.102e-03	3.385e-03	3.385e-03	3.102e-03	1.202e-03	2.217e-03
gam eff	4.887e-01	4.887e-01	4.887e-01	4.887e-01	4.939e-01	4.788e-01
gm	5.847e-04	4.706e-04	4.706e-04	5.847e-04	1.578e-04	3.423e-04
gds	1.956e-06	1.447e-06	1.447e-06	1.956e-06	6.946e-07	1.228e-06
gmb	1.930e-04	1.546e-04	1.546e-04	1.930e-04	5.186e-05	9.378e-05
cdtot	6.915e-14	7.446e-14	7.446e-14	6.915e-14	2.648e-14	4.351e-14

cgtot	6.352e-13	6.687e-13	6.687e-13	6.352e-13	1.555e-13	3.112e-13
cstot	7.629e-13	8.032e-13	8.032e-13	7.629e-13	1.889e-13	3.601e-13
cbtot	3.204e-13	3.468e-13	3.468e-13	3.204e-13	9.225e-14	1.470e-13
cgs	5.809e-13	6.044e-13	6.044e-13	5.809e-13	1.394e-13	2.855e-13
cgd	2.123e-14	2.286e-14	2.286e-14	2.123e-14	6.585e-15	1.307e-14

subckt

element	0:m14	0:m1	0:m13	0:m12	0:m4	0:m23
model	0:pch.2	0:pch.2	0:pch.2	0:pch.2	0:pch.2	0:nch.3
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	-5.599e-05	-1.515e-05	-5.599e-05	-7.167e-05	-3.584e-05	2.785e-05
ibs	1.075e-20	5.155e-17	1.075e-20	1.373e-20	1.020e-16	-6.381e-21
ibd	4.208e-09	5.166e-17	4.208e-09	2.409e-16	6.119e-12	-6.222e-08
vgs	-6.082e-01	-7.863e-01	-6.082e-01	-6.082e-01	-7.776e-01	5.604e-01
vds	-2.039e+00	-7.863e-01	-2.039e+00	-5.224e-01	-1.454e+00	2.073e+00
vbs	0.	6.082e-01	0.	0.	5.224e-01	0.
vth	-4.571e-01	-6.312e-01	-4.571e-01	-4.574e-01	-6.087e-01	4.830e-01
vdsat	-1.593e-01	-1.688e-01	-1.593e-01	-1.591e-01	-1.786e-01	1.312e-01
vod	-1.511e-01	-1.552e-01	-1.511e-01	-1.508e-01	-1.689e-01	7.741e-02
beta	4.210e-03	1.098e-03	4.210e-03	5.713e-03	2.217e-03	4.219e-03
gam eff	4.939e-01	4.766e-01	4.939e-01	4.939e-01	4.788e-01	5.118e-01
gm	5.750e-04	1.547e-04	5.750e-04	7.470e-04	3.423e-04	3.785e-04
gds	2.017e-06	6.109e-07	2.017e-06	3.603e-06	1.228e-06	1.144e-06
gmb	1.891e-04	4.128e-05	1.891e-04	2.455e-04	9.378e-05	1.082e-04
cdtot	7.555e-14	2.333e-14	7.555e-14	1.276e-13	4.351e-14	1.016e-14
cgtot	5.440e-13	1.546e-13	5.440e-13	7.389e-13	3.112e-13	5.836e-14
cstot	6.610e-13	1.778e-13	6.610e-13	8.963e-13	3.601e-13	7.074e-14
cbtot	3.053e-13	7.366e-14	3.053e-13	4.385e-13	1.470e-13	3.676e-14
cgs	4.879e-13	1.418e-13	4.879e-13	6.628e-13	2.855e-13	4.738e-14
cgd	2.288e-14	6.554e-15	2.288e-14	3.144e-14	1.307e-14	3.682e-15

subckt

element	0:m29	0:m27	0:m28	0:m19	0:m24	0:m30
model	0:nch.6	0:nch.2	0:nch.2	0:nch.2	0:nch.3	0:nch.6
region	Saturati	Saturati	Saturati	Linear	Saturati	Saturati
id	1.204e-05	1.204e-05	1.204e-05	0.	2.785e-05	1.204e-05
ibs	-2.795e-21	-6.275e-17	-6.275e-17	-2.387e-27	-6.381e-21	-2.795e-21
ibd	-3.572e-10	-1.528e-15	-1.528e-15	-2.387e-27	-6.222e-08	-3.572e-10
vgs	5.348e-01	7.737e-01	7.737e-01	1.513e+00	5.604e-01	5.348e-01
vds	1.300e+00	6.295e-01	6.295e-01	0.	2.073e+00	1.300e+00
vbs	0.	-1.300e+00	-1.300e+00	-1.486e-12	0.	0.
vth	4.824e-01	7.730e-01	7.730e-01	4.827e-01	4.830e-01	4.824e-01
vdsat	1.171e-01	8.973e-02	8.973e-02	8.847e-01	1.312e-01	1.171e-01
vod	5.234e-02	7.147e-04	7.147e-04	1.030e+00	7.741e-02	5.234e-02
beta	2.659e-03	6.597e-03	6.597e-03	3.487e-03	4.219e-03	2.659e-03
gam eff	5.146e-01	5.069e-01	5.069e-01	5.137e-01	5.118e-01	5.146e-01

gm	1.826e-04	2.225e-04	2.225e-04	0.	3.785e-04	1.826e-04
gds	5.225e-07	7.697e-07	7.697e-07	0.	1.144e-06	5.225e-07
gmb	5.256e-05	4.143e-05	4.143e-05	0.	1.082e-04	5.256e-05
cdtot	8.389e-15	2.027e-14	2.027e-14	1.398e-13	1.016e-14	8.389e-15
cgtot	4.858e-14	8.810e-14	8.810e-14	1.393e-13	5.836e-14	4.858e-14
cstot	5.759e-14	8.656e-14	8.656e-14	1.414e-13	7.074e-14	5.759e-14
cbtot	3.197e-14	5.669e-14	5.669e-14	6.026e-14	3.676e-14	3.197e-14
cgs	3.781e-14	6.139e-14	6.139e-14	7.211e-14	4.738e-14	3.781e-14
cgd	2.814e-15	7.318e-15	7.318e-15	6.969e-14	3.682e-15	2.814e-15

subckt

element	0:m39	0:m33	0:m34	0:m37	0:m38	0:m6
model	0:nch.2	0:nch.6	0:nch.6	0:nch.6	0:nch.6	0:nch.2
region	Cutoff	Saturati	Linear	Saturati	Linear	Saturati
id	0.	1.843e-06	1.199e-04	1.843e-06	1.199e-04	3.584e-05
ibs	-7.361e-17	-5.262e-22	-3.415e-20	-5.262e-22	-3.415e-20	-8.008e-21
ibd	-7.361e-17	-5.994e-18	-5.994e-18	-5.994e-18	-5.994e-18	-1.089e-15
vgs	-1.300e+00	5.348e-01	1.929e+00	5.348e-01	1.929e+00	5.348e-01
vds	1.080e-09	4.025e-01	4.025e-01	4.025e-01	4.025e-01	6.231e-01
vbs	-1.300e+00	0.	0.	0.	0.	0.
vth	7.732e-01	4.720e-01	4.720e-01	4.720e-01	4.720e-01	4.826e-01
vdsat	5.153e-02	1.221e-01	1.231e+00	1.221e-01	1.231e+00	1.171e-01
vod	-2.073e+00	6.279e-02	1.457e+00	6.279e-02	1.457e+00	5.218e-02
beta	7.844e-03	3.725e-04	2.603e-04	3.725e-04	2.603e-04	8.165e-03
gam eff	5.069e-01	5.300e-01	5.300e-01	5.300e-01	5.300e-01	5.137e-01
gm	0.	2.747e-05	5.169e-05	2.747e-05	5.169e-05	5.479e-04
gds	0.	1.089e-07	2.380e-04	1.089e-07	2.380e-04	1.884e-06
gmb	0.	7.985e-06	3.214e-05	7.985e-06	3.214e-05	1.576e-04
cdtot	2.532e-14	2.038e-15	1.656e-14	2.038e-15	1.656e-14	2.795e-14
cgtot	7.706e-14	1.210e-14	1.978e-14	1.210e-14	1.978e-14	1.484e-13
cstot	2.532e-14	1.439e-14	1.959e-14	1.439e-14	1.959e-14	1.755e-13
cbtot	9.320e-14	7.856e-15	7.984e-15	7.856e-15	7.984e-15	9.943e-14
cgs	8.627e-15	9.631e-15	1.174e-14	9.631e-15	1.174e-14	1.156e-13
cgd	8.625e-15	5.533e-16	8.300e-15	5.533e-16	8.300e-15	8.627e-15

subckt

element	0:m7	0:m2	0:m3	0:m16	0:m15	0:m21
model	0:nch.2	0:nch.2	0:nch.2	0:nch.2	0:nch.2	0:nch.10
region	Saturati	Saturati	Saturati	Saturati	Saturati	Linear
id	3.584e-05	1.515e-05	1.515e-05	5.600e-05	5.600e-05	7.301e-16
ibs	-8.008e-21	-3.207e-17	-3.471e-21	-1.274e-20	-1.274e-20	7.743e-28
ibd	-1.089e-15	-3.061e-15	-3.509e-17	-3.850e-17	-3.850e-17	-2.577e-28
vgs	5.348e-01	6.707e-01	5.348e-01	6.231e-01	6.231e-01	1.431e+00
vds	6.231e-01	6.707e-01	5.348e-01	5.604e-01	5.604e-01	5.948e-12
vbs	0.	-5.348e-01	0.	0.	0.	4.462e-12
vth	4.826e-01	6.176e-01	4.826e-01	4.826e-01	4.826e-01	4.569e-01

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 vdsat     1.171e-01  1.191e-01  1.171e-01  1.836e-01  1.836e-01  8.830e-01
 vod       5.218e-02  5.306e-02  5.216e-02  1.405e-01  1.405e-01  9.745e-01
 beta      8.165e-03  3.389e-03  3.467e-03  4.084e-03  4.084e-03  1.302e-04
 gam eff   5.137e-01  5.105e-01  5.137e-01  5.137e-01  5.137e-01  5.294e-01
 gm        5.479e-04  2.331e-04  2.317e-04  5.890e-04  5.890e-04  5.377e-16
 gds       1.884e-06  7.768e-07  8.625e-07  2.691e-06  2.691e-06  1.228e-04
 gmb       1.576e-04  5.341e-05  6.666e-05  1.691e-04  1.691e-04  2.432e-16
 cdtot     2.795e-14  1.098e-14  1.218e-14  1.445e-14  1.445e-14  1.903e-14
 cgtot     1.484e-13  6.271e-14  6.307e-14  8.683e-14  8.683e-14  1.970e-14
 cstot     1.755e-13  7.115e-14  7.463e-14  1.066e-13  1.066e-13  1.946e-14
 cbtot     9.943e-14  3.467e-14  4.268e-14  5.103e-14  5.103e-14  7.518e-15
 cgs       1.156e-13  5.110e-14  4.910e-14  7.364e-14  7.364e-14  1.013e-14
 cgd       8.627e-15  3.660e-15  3.668e-15  4.395e-15  4.395e-15  9.803e-15

subckt
element  0:m20      0:m40      0:m11      0:m22      0:m10
model    0:nch.2    0:nch.2    0:nch.2    0:nch.10   0:nch.2
region      Linear     Cutoff   Saturati     Linear   Saturati
 id              0.         0.      1.119e-03  7.006e-16  1.119e-03
 ibs    -2.291e-27 -9.343e-17 -2.532e-19  7.430e-28 -2.532e-19
 ibd    -2.291e-27 -9.343e-17 -7.593e-13 -2.473e-28 -7.593e-13
 vgs     1.513e+00 -1.300e+00  1.300e+00  1.431e+00  1.300e+00
 vds            0.  -1.080e-09   1.300e+00  5.707e-12  1.300e+00
 vbs    -1.426e-12 -1.300e+00        0.        4.281e-12         0.
 vth      4.827e-01  7.732e-01  4.825e-01  4.569e-01  4.825e-01
 vdsat    8.847e-01  5.153e-02  7.256e-01  8.830e-01  7.256e-01
 vod     1.030e+00 -2.073e+00  8.175e-01  9.745e-01  8.175e-01
 beta     3.487e-03  9.997e-03  3.762e-03  1.302e-04  3.762e-03
 gam eff  5.137e-01  5.069e-01  5.137e-01  5.294e-01  5.137e-01
 gm             0.         0.      2.104e-03  5.160e-16  2.104e-03
 gds            0.         0.      2.194e-05  1.228e-04  2.194e-05
 gmb            0.         0.      6.942e-04  2.334e-16  6.942e-04
 cdtot     1.398e-13  3.223e-14  1.424e-14  1.903e-14  1.424e-14
 cgtot     1.393e-13  9.819e-14  1.040e-13  1.970e-14  1.040e-13
 cstot     1.414e-13  3.223e-14  1.274e-13  1.946e-14  1.274e-13
 cbtot     6.026e-14  1.187e-13  5.279e-14  7.518e-15  5.279e-14
 cgs       7.211e-14  1.099e-14  9.293e-14  1.013e-14  9.293e-14
 cgd       6.969e-14  1.100e-14  4.847e-15  9.803e-15  4.847e-15

        ***** job concluded
1****** HSPICE -- C-2009.03-SP1 32-BIT (May 25 2009) sunos ******
******
* # file name: /nfs/thesis/m/m_talukd/simulation/myuamckt/hspices/schematic/

 ******  job statistics summary tnom=  25.000 temp=  25.000 *****
```

```
******  HSPICE Threads Information  ******
Command Line Threads Count              :     1
Available CPU Count                     :     2
Actual Model Evaluation(Load) Threads Count :     1
Actual Solver Threads Count             :     1


******  Circuit Statistics  ******
# nodes      =     110 # elements   =      48
# resistors   =       0 # capacitors =       2 # inductors   =       0
# mutual_inds =       0 # vccs       =       0 # vcvs        =       0
# cccs        =       0 # ccvs       =       0 # volt_srcs   =       5
# curr_srcs   =       0 # diodes     =       0 # bjts        =       0
# jfets       =       0 # mosfets    =      41 # U elements  =       0
# T elements  =       0 # W elements =       0 # B elements  =       0
# S elements  =       0 # P elements =       0 # va device   =       0


******  Runtime Statistics (seconds)  ******

analysis          time    # points   tot. iter  conv.iter
op point          0.03           1          38
ac analysis       0.01          56          56
readin            1.27
errchk            0.09
setup             0.01
output            0.00


        total memory used          834  kbytes
        total cpu time            1.42 seconds
        total elapsed time        1.77 seconds
        job started at     02:19:29 08/02/2011
        job ended   at     02:19:31 08/02/2011


 Init: hspice initialization file: /CMC/tools/meta/hspice.ini
 lic: Release cdsaawaves token(s)
 lic: Release hspice token(s)

End of /encs/bin/wrapper script.
```