High-speed Energy-efficient Soft Error Tolerant Flip-flops

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Abstract

High-speed Energy-efficient Soft Error Tolerant Flip-flops

Riadul Islam

Single event upset (SEU) or soft error caused by alpha particles and cosmic neutrons has emerged as a key reliability concern in nanoscale CMOS technologies. The decrease in signal charge due to the reduction of the operating voltage and node capacitance primarily increases the soft error rate (SER) in integrated circuits. The situation is aggravated by the increasing number of memory elements (e.g., flip-flops) on chip, the lack of inherent error masking mechanisms in these elements, and the below-nominal voltage operation for reducing the power consumption. In fact, limiting the power consumption is critical to enhance the battery life of portable electronic devices. In this thesis, I present several soft error tolerant flip-flops that offer high speed while consuming low power either inherently or through low-energy clocking scheme.

The proposed soft error tolerant flip-flops can be divided into two major categories: i) flip-flops with square-wave clock and ii) flip-flops with energy recovery sinusoidal clock, which is very attractive to significantly lower the clock power consumption. The two square-wave clock based proposed flip-flops are: a true single phase clock (TSPC) DICE flip-flop and a clocked precharge soft error robust flip-flop. These flip-flops use fewer transistors and offer as much as 35% lower power-delay-product (PDP) than existing soft error robust pulsed DICE flip-flop. The energy recovery clock based

proposed flip-flops are: a soft clock edge SEU hardened (SCESH) flip-flop, C^2-DICE flip-flop, a conditional pass Quatro (CPQ) flip-flop, and two energy recovery TSPC flip-flops. These flip-flops exhibit lower PDP ranging from 30% to 69% when compared to the pulsed DICE flip-flop and the single-ended conditional capturing energy recovery (SCCER) flip-flop. Thus, the proposed flip-flops provide a wide range of power and delay choices and as such can be used in a variety of low-power or high performance applications including high-end microprocessors, low-power system-on-chips (SOCs), and implantable medical devices.

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Contents

List of Figures

List of Tables

Chapter 1 Introduction

As the complementary metal-oxide-semiconductor (CMOS) technology continues to scale in the sub-45nm regime, ensuring reliability of integrated circuits is becoming more difficult than ever before. Particularly, due to the reduction of the node capacitance and the operating voltage, the signal charge representing a logic state has become too small. As a result, noise sources, such as electromagnetic interference, chip- and board-level signal coupling, radiation-induced voltage transients, etc. can easily corrupt the data. In a well designed system, radiation-induced voltage transients appear to be the major threat to the data integrity. The threat is accentuated by the increasing number of memory elements (e.g., flip-flops) on chip, the lack of inherent error tolerance in these elements, and the operation at lower voltages than the nominal for reducing the power consumption.

The radiation that affects the integrated circuits primarily consists of high energy neutrons and alpha particles, which come from intergalactic cosmic rays and chip packaging materials, respectively [1]. These particles interact with the silicon substrate and indirectly or directly generates unwanted charge i.e., electron-hole pairs (EHP) in the substrate [2], [3]. When collected at a sensitive node, which is primarily a reverse biased p-n junction, the unwanted charge generates a voltage transient at the node. The transient is referred to as a single event transient (SET). If the SET is large enough, it can flip the logic state ('0' to '1' or vice versa) at the node. When the flipped state is captured by a memory element, such as a flip-flop, it is referred to as a single event upset (SEU). Since an SEU does not permanently damage a device and can be cleared by resetting the

system, it is called a "soft error". With CMOS technology scaling the soft error rate in logic circuits is exponentially increasing [3].

1.1 Sources of Soft Errors

The three primary sources of radiation induced soft error in semiconductor devices are: i) alpha particles, ii) high-energy neutrons from cosmic radiation , and iii) the interaction of cosmic ray thermal neutrons and ^{10}B in devices containing borophosphosilicate glass (BPSG) [1]. The third particle source is no longer a concern below 0.25μm technology, where the BPSG has been eliminated from the fabrication process.

An alpha particle is a doubly ionized helium atom ($^4He^2$) that is emitted from radioactive materials like Uranium (^{238}U), Thorium (^{232}Th), and lead (^{210}Pb). Trace amount of these materials can be found in chip package materials, primarily in solder balls [4]. Alpha particles typically have energies in the order of 1 – 9 MeV while only 3.6 eV of energy generates 1 EHP in silicon [5]. Accordingly, an alpha particle of 1 MeV energy can generate approximately 44.5 fC of charge, which can easily flip the logic state in a latch.

There are three commonly employed techniques that can reduce the alpha particle induced soft errors [1]. The first technique, which is very expensive, is to use extremely pure materials with very low alpha emission rate. The second technique is to spatially separate sensitive circuits from alpha emitting packaging components. However, this technique does not appear to be a viable solution in present SOCs, where majority of the chip area is consumed by memory elements. The last technique is to shield the high alpha
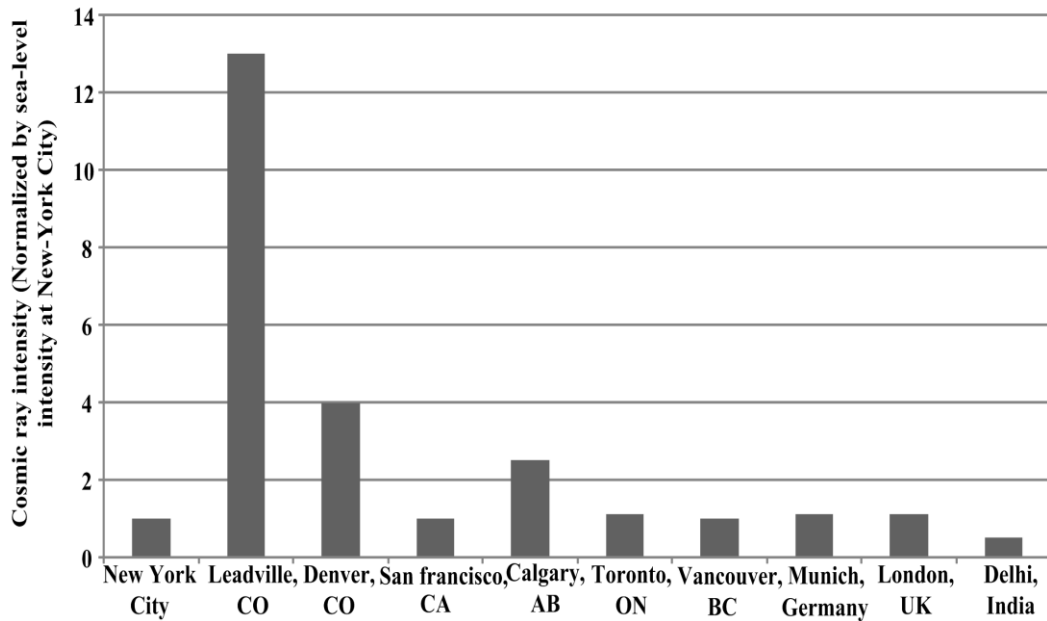
Figure 1.1: Cosmic ray intensity at different cities in the world [4].

emitting materials using a thin polyimide coating over the chip. This technique is not suitable for flip-chip packages where solder balls need to be electrically connected to the metal of the bond pad.

The second dominant source of soft error is the high energy neutrons that come from the galactic cosmic rays. The flux (number of neutrons per unit area per second) of cosmic neutrons is a function of neutrons energy and the altitude. Higher the altitude, higher is the neutron flux. As a result, cosmic ray intensities vary in different cities of the world as shown in Figure 1.1 [4], causing a variation in the SER of the same device in different cities.

A cosmic neutron generates charge in silicon by colliding with a silicon nucleus. The high kinetic energy of the neutron knocks the silicon from the lattice and the silicon nucleus breaks into smaller fragments, each of which generates charge. The resulting

charge density per distance traveled (25-150 fC/μm) is significantly higher than that for alpha particles (16 fC/μm) [1].

Unlike alpha particles, the cosmic neutron flux cannot be reduced significantly at the chip level with traditional techniques. Concrete has been shown to shield the cosmic radiation at a rate of only ~1.4x per foot of concrete thickness [6]. Thus, little can be done to protect commonly used integrated circuits from cosmic radiation. The resulting soft errors must therefore be dealt with by process, circuit, or architecture level mitigation techniques.

1.2 Basic Mechanism of Soft Error

The soft error in semi-conductor devices can be described with reference to Figure 1.2 [3]. Figure 1.2(a) shows the onset of the ionization event, where a cylindrical charge column of submicron radius is generated as the energetic particle pass through or near a p-n junction. The amount of generated charge depends on the particle's linear energy transfer (LET), which is a measure of energy loss per unit length.

The generated charge is rapidly collected at the p-n junction - electrons drift to the higher potential n-diffusion and holes drift to the lower potential p-substrate (see Figure 1.2(b)). A notable feature of this phase is the formation of a funnel through the distortion of the depletion region [7]. The funnel enhances the charge collection (primarily by drift) by extending the depletion region deeper into the substrate. This rapid charge collection phase is completed within a nanosecond and followed by a diffusion phase (see Figure 1.2(c)). Charge collection through the diffusion continues until all excess carriers have
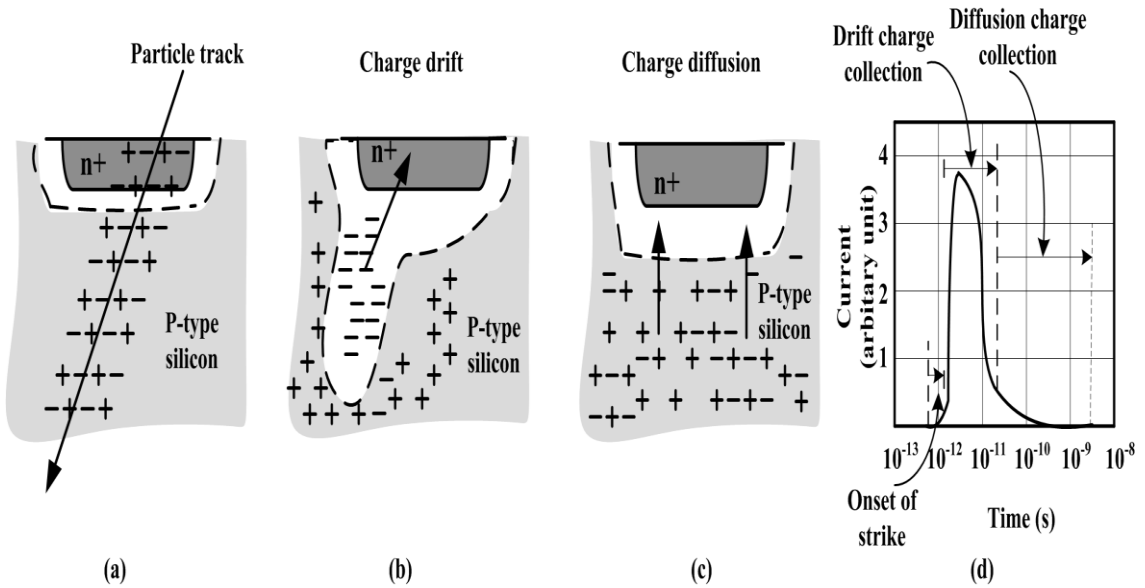
Figure 1.2: Charge generation and collection phases in a reverse-biased p-n junction and the resultant current pulse caused by the passage of a high-energy ion [3].

been collected, recombined, or diffused away from the junction area. The diffusion phase lasts from hundreds of picoseconds to nanoseconds.

The above charge generation and collection phases result in a current pulse, which is shown in Figure 1.2(d). The current pulse generates a voltage transient or single event transient (SET) at the circuit node connected to the junction. The amplitude and duration of the SET depends on the amount of collected charge (Q_{coll}), which again depends on a complex combination of the size of the device, biasing of circuit nodes, substrate doping, the type of the particle, its energy, its trajectory, the initial position of the event within the device, and the logic state of the device. When Q_{coll} exceeds the critical charge (Q_{crit}), which is defined as the minimum charge required to change the logic state in a memory element, a soft error occur.
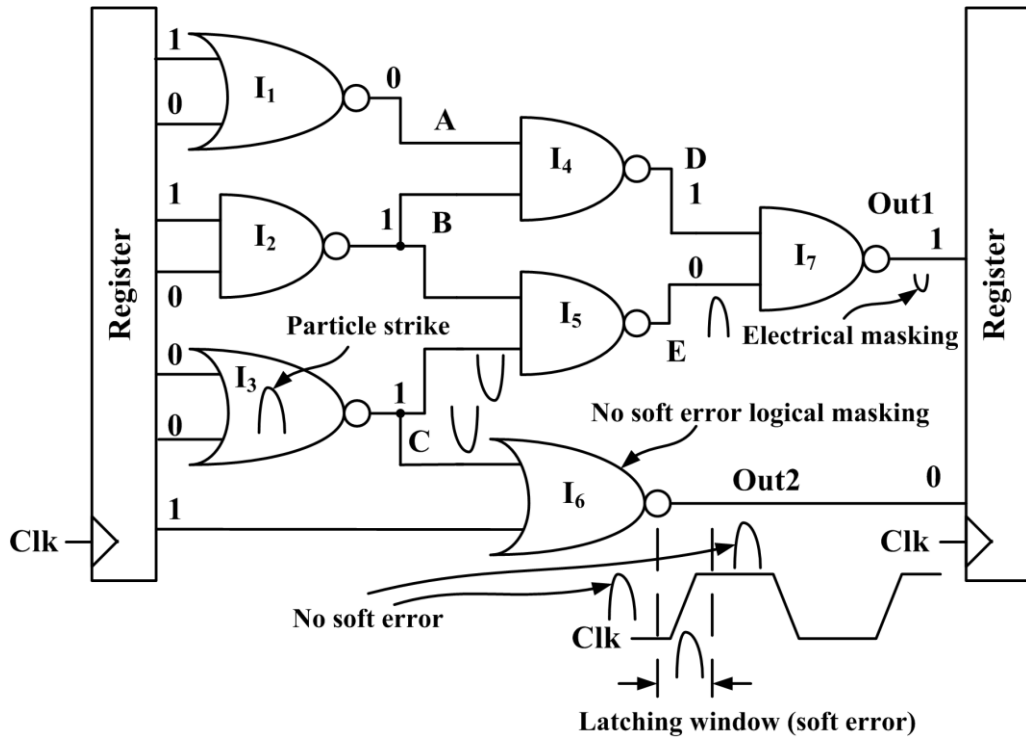
Figure 1.3: An example of the soft error in combinational circuits.

1.3 Soft Error in Combinational Logic

An SET may propagate through the combinational stages and eventually be latched by a memory element (latch, flip-flop, etc.) to cause a soft error. However, in combinational circuits, there are three inherent masking mechanisms that prevent the propagation of any given pulse along a path towards the input of a memory element [8]. These masking mechanisms are logical masking, electrical masking, and latching window masking, which can be described with reference to the NAND-NOR based circuit shown in Figure 1.3. Assuming a particle strike causes a negative pulse at node C. The pulse at node C does not cause any change at the output (Out2) of the NOR gate I_6. This is because the other input of I_6 is '1' and it held, according to the principle of a NOR gate, the output is logic 0. This is referred to as the logical masking. On the other hand, due to

6

the limited bandwidth of CMOS circuits, an SET can get attenuated as it advances through the gates and eventually becomes negligible when it reaches the latch or register (Out1 in Figure 1.3). This phenomenon is called the electrical masking. Finally, the latching window masking means that if an SET occurs outside the clock latching window, it will not be latch by the register and no soft error will error.

1.4 Soft Error in Memory Elements

Due to the increasing number of memory circuits in SOCs and the lack of inherent error masking mechanisms, soft error rate (SER) in memories is becoming a critical reliability concern. If a soft error occurs at a memory cell, the erroneous values remain stored until the data value is re-written.

1.4.1. Soft Error in DRAM and SRAM

A typical dynamic random access memory (DRAM) cell has one sensitive node (node C at Figure 1.4(a)) that is susceptible to particle induced soft errors. If the amount of collected charge is large enough at this node, it can corrupt the stored logic of the cell. However, with 3D trench capacitor, the Q_{crit} in DRAM bit-cell dominate the Q_{coll} and the bit-level SER is reduced. However, as the density of bits in DRAM is growing, the system-level SER in DRAM is remaining constant [3].

Unlike DRAM cell, static random access memory (SRAM) cell uses two cross coupled inverters to store data (see Figure 1.4(b)). The cross coupled inverters strongly drives each other to keep the data bit and its complement as long as the power is ON. An SRAM cell has two sensitive nodes (node A and node B in Figure 1.4(b)) that are
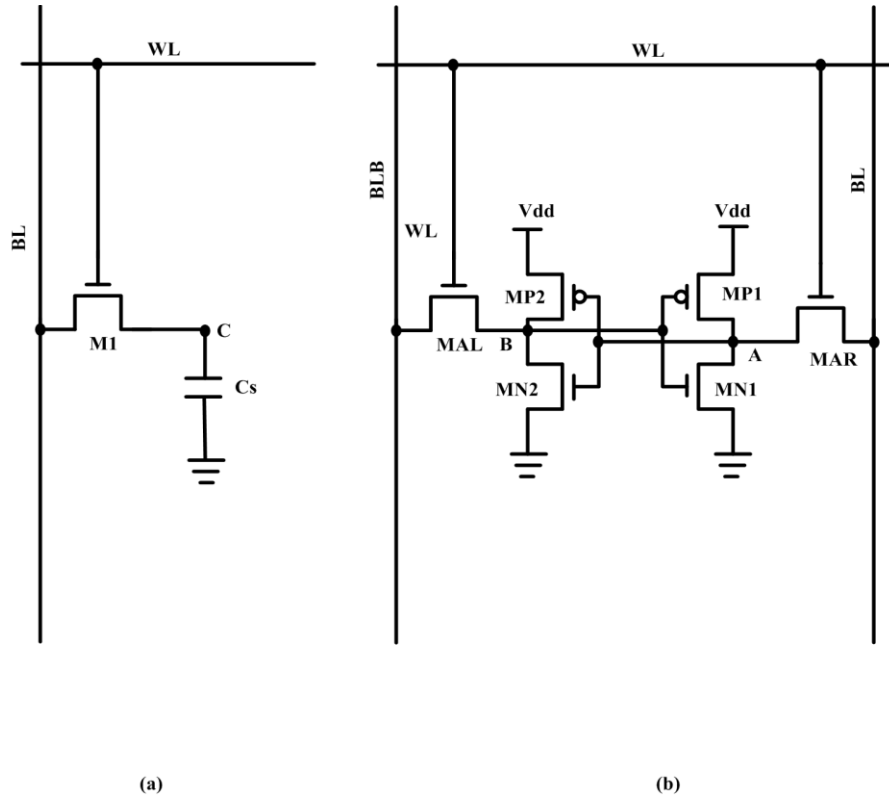
Figure 1.4: a) Schematic of a standard one transistor DRAM cell and b) a standard six-transistor SRAM cell. WL: word line, BL: bit line, BLB: complementary bit line.

susceptible to soft errors. The sensitivity of these nodes (e.g., critical charge Q_{crit}) depends on the charge ($Q_{node}=C_{node}*V$) of these nodes and the driving capability of the transistors that are connected to these nodes and are ON. With technology scaling, SRAM bit Q_{crit} and Q_{coll} are both decreasing, causing a constant bit-level soft error rate. Since the number of bits in SRAM is exponentially increasing, the system level SER in SRAM is also exponentially growing [3]. An effective and the most popular technique to deal with this problem in SRAM (and also in DRAM) is to use the error correction codes (ECC).
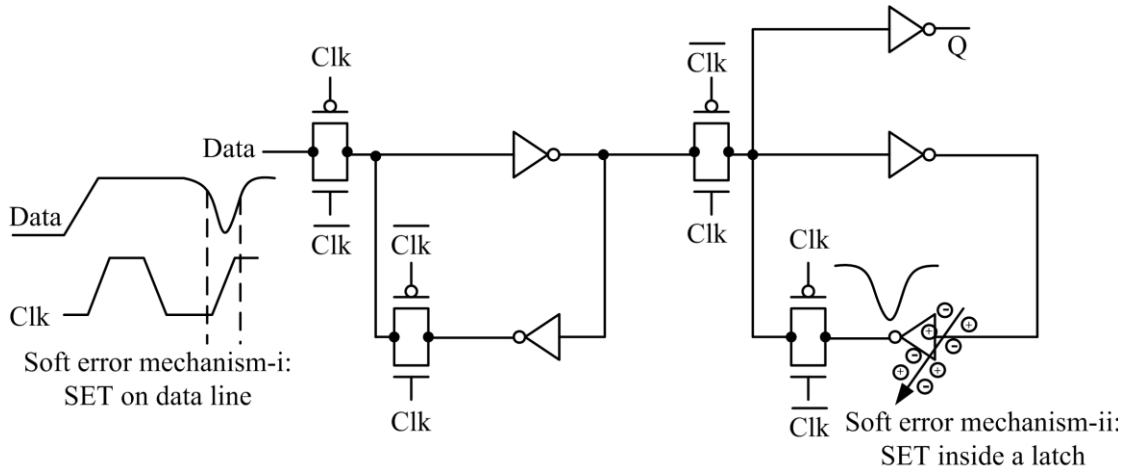
Figure 1.5: SEU mechanisms in a typical master-slave D flip-flop.

1.4.2. Soft Error in Flip-flops

Soft errors in flip-flops are caused in a manner that is similar to upsets in SRAM bit cells: the collection of particle-induced charges results in a bit flip if Q_{coll} exceeds Q_{crit}. Typically, a flip-flop experiences a particle-induced SET through two possible mechanisms: i) by latching an SET arriving at the input data line during the latching window of the clock and ii) by having an SET at a sensitive node of the latch inside the flip-flop. Figure 1.5 illustrates these two mechanisms for a conventional master-slave D flip-flop. In the first mechanism, since the SET cannot be distinguished from the data, managing the resulting SEU is very difficult and incurs unacceptable performance penalty. In contrast, for protecting from the second SEU mechanism, the flip-flop can be made robust by applying circuit techniques while satisfying the required performance metrics.

Unlike the memory arrays (e.g., SRAM), the irregular distribution of flip-flops across the chip makes it difficult to protect them using the parity check or ECC. Instead, the protection techniques involve either the redundancy or the circuit hardening by design

9
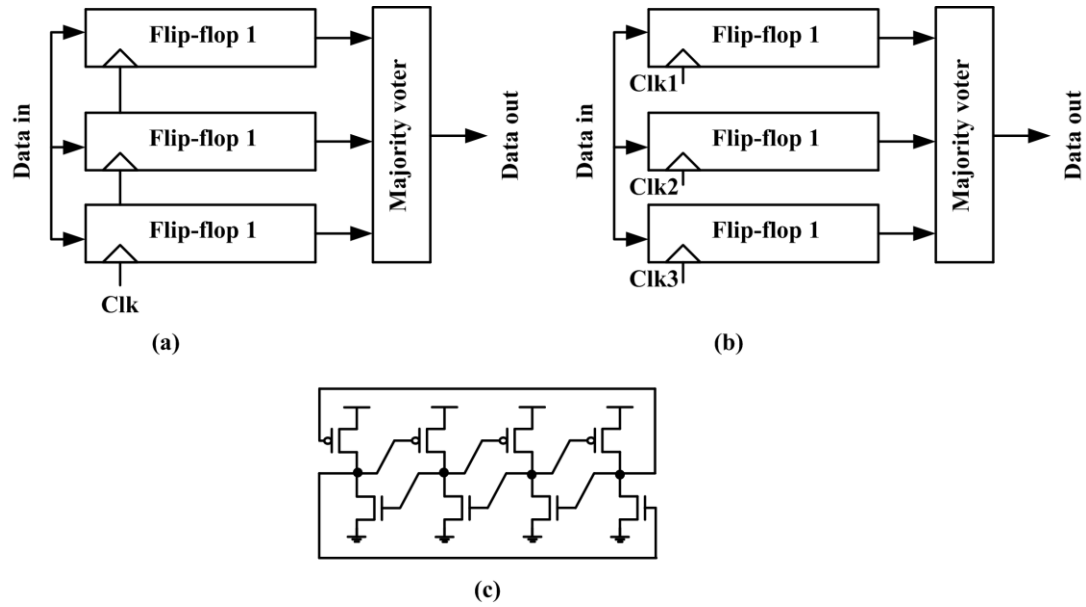
Figure 1.6: a) Spatial and b) temporal redundancy schemes, and c) the SEU robust DICE latch for HBD schemes.

(HBD). Redundancy can again be spatial or temporal. The most commonly used spatial redundancy method is the triple modular redundancy (TMR) [9]. TMR replicates the hardware, such as a flip-flop three times and applies majority voting to extract the correct data in the case of an SEU (see Figure 1.6(a)). While this technique corrects an SEU in any latch inside the replicated flip-flops (mechanism-ii of Figure 1.5), the technique fails to detect and correct an SEU caused by an SET on the data line (mechanism-i of Figure 1.5). The temporal redundancy technique, on the other hand, samples the data at different times (Clk1, Clk2, and Clk3 in Figure 1.6(b)) with an interval greater than the pulse width of the SET. Then it stores the sampled values in different latches and uses majority voting to determine the correct data [10]. This technique can detect and correct a SEU for an SET on the data line. In addition, since it involves majority voting of replicated latches, it can correct a SEU occurred inside any of the latches. However, both of these redundancy techniques incur large area and power penalties (~3x for TMR) in the

replicated circuits and performance penalty in the sampling and/or voter circuit. In contrast, HBD techniques employ SEU immune latches instead of replicating the hardware. In the event of an SET at any of the sensitive nodes, these latches prevent flipping of the data stored in the flip-flops [11]-[16].

The most commonly used HBD flip-flops are based on the eight transistor (8T) dual interlocked cell (DICE) shown in Figure 1.6(c) [13]. The cell stores the complementary logic ('1' and '0') as a combination of four node voltages, two nodes holding the original data and two nodes the complement of the data. The cell efficiently tolerates a single node SET and widely used as storage cell for designing soft error tolerant flip-flops and latches. However, it often incurs large area and power consumption.

1.5 Low Power Techniques and Soft Error

In order to reduce power consumption and increase the battery life of portable devices, different low power techniques are employed. Most commonly, low-voltage operation, use of sleep transistors to shut down inactive circuit parts, and applying virtual ground/supply control on active non-operating circuits to minimize the leakage power [17]-[18]. However, these techniques typically reduce the Q_{crit} of latches and flip-flops, making them more susceptible to soft errors. In fact, reduction in operating voltage linearly reduces Q_{crit}, which exponentially increases the SER [8], [4].

Another emerging technique to reduce the overall chip power consumption is to use the resonant energy recovery clocking [19]. In high performance applications, clock power can be as much as 40% of the total chip power consumption [20]. Accordingly, in order to reduce the clock power, the resonant energy recovery clocking uses the

capacitance of the clock distribution network with an on-chip inductor to form an LC network that generates a sinusoidal clock. The sinusoidal clock recycles the energy between the charging and discharging phases and takes little energy from the battery. Thus, energy recovery clock-based flip-flop design is very promising for realizing low power digital systems. However, in order to make these systems robust against soft errors and the associated malfunction, the flip-flops need to be soft error tolerant.

1.6 Motivation and Thesis Outline

Given the fact that the integrated circuits in today's nanoscale technologies are highly susceptible to soft errors and low power operation is the key to extending the life of battery operated devices, devising soft error tolerant integrated circuits having the minimal power penalty or the compatibility with low-power techniques is critical. In this thesis, I propose several high speed and power efficient soft error tolerant flip-flops. Two of the flip-flops operate with conventional square-wave clock while the others operate with the energy recovery sinusoidal clock. To the best of my knowledge, no soft error tolerant flip-flop with energy recovery clocking has been reported to date.

The thesis is organized as follows. Chapter 2 analyses variety of soft error robust and energy recovery flip-flops reported in the literature. Chapter 3 presents the schematic and operating principles of the proposed soft error tolerant flip-flops. Chapter 4 discusses the implementation of the flip-flops and compares their performance with recently reported soft error tolerant flip-flops. Chapter 5 outlines the future directions of this work and draws the conclusion.

Chapter 2 Review of Soft Error Robust and Energy Recovery Flip-flops

The traditional flip-flops are designed with typical square clock signal. With the rising edge (or falling edge) of the square clock, the data is written in the storage cell and output is changed depending on the data signal. Again this kind of flip-flop can utilize two edges (rising and falling) of the clock signal, which is for each rising and falling edge, the data will be latched to the output named dual edge trigger flip-flop. On the other hand, flip-flops can utilize sinusoidal clock instead of traditional square signal. Where, data is latched to the output with the rising or falling edge of the sinusoidal clock. Primarily, the advantage of using sinusoidal clock over square clock comes from the energy recovery of the associated flip-flops input clock and the clock distribution network.

2.1 Soft Error Robust Flip-flops

By soft error robust flip-flops, we primarily mean the hardening by design (HBD) flip-flops. The most commonly used HBD flip-flops are based on static DICE cell [13]. The four nodes of the DICE cell holds data in its two nodes and the complement of data in other two nodes, storing a logic '1' or a logic '0'. Each storage node connects to one NMOS and one PMOS, when the state of any node is changed by a SET, and the MOSFET connects to the corresponding node help restore the correct value of the affected node. Typically, DICE-based flip-flops use a single DICE [12] and two DICE as master-slave configuration, such depicted in [15]. The flip-flop proposed by *Kruger et.*
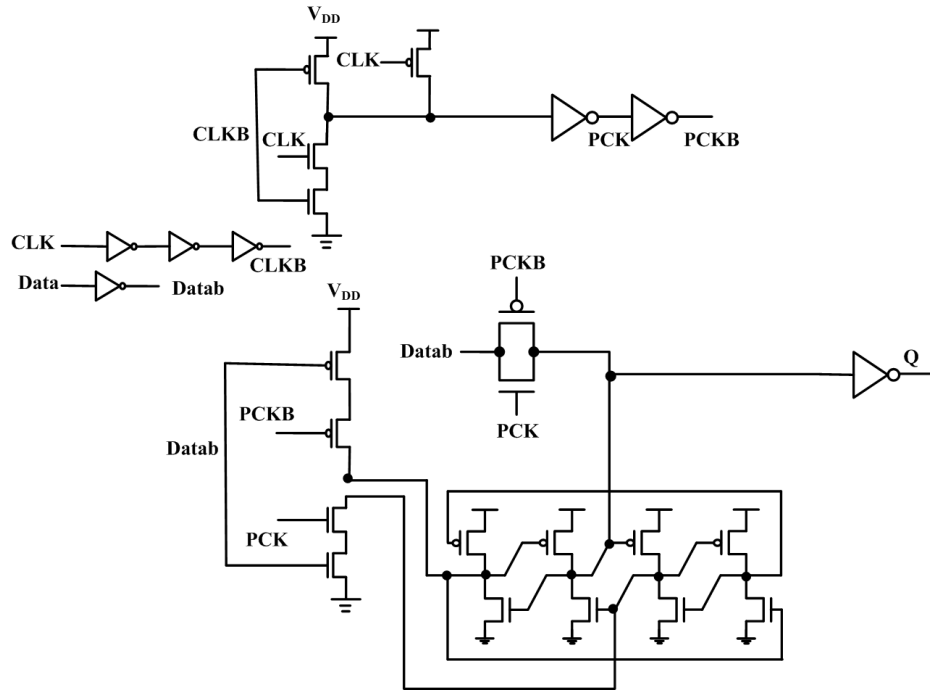
Figure 2.1: Pulsed DICE flip-flop reported in [12].

al. is based on DICE cell (see Figure 2.1) [12]. Its input section generates pulse signals

PCK and PCKB in Figure 2.1. With the rising edge of the PCK signal in transmission

gate, the data are written into the DICE. We refer this flip-flop as pulsed DICE. The

pulsed DICE flip-flop does not have any sizing constraints inside the DICE cell; however

consume higher power, particularly at low data activity. This is due to the fact, at low

data activity the pulse generator circuit is active, resulting power consumptions

irrespective of data transition.

Figure 2.2 shows the Delay-filter DICE flip-flop with preset and clear reported in

[14]. This flip-flop utilized a delay-filter at the input stage. The data and a delayed

version of data are used in a C-element to mask the data line SET. It should be note that

the data delay in the C-element is equal to the time interval of a typical SET period. This
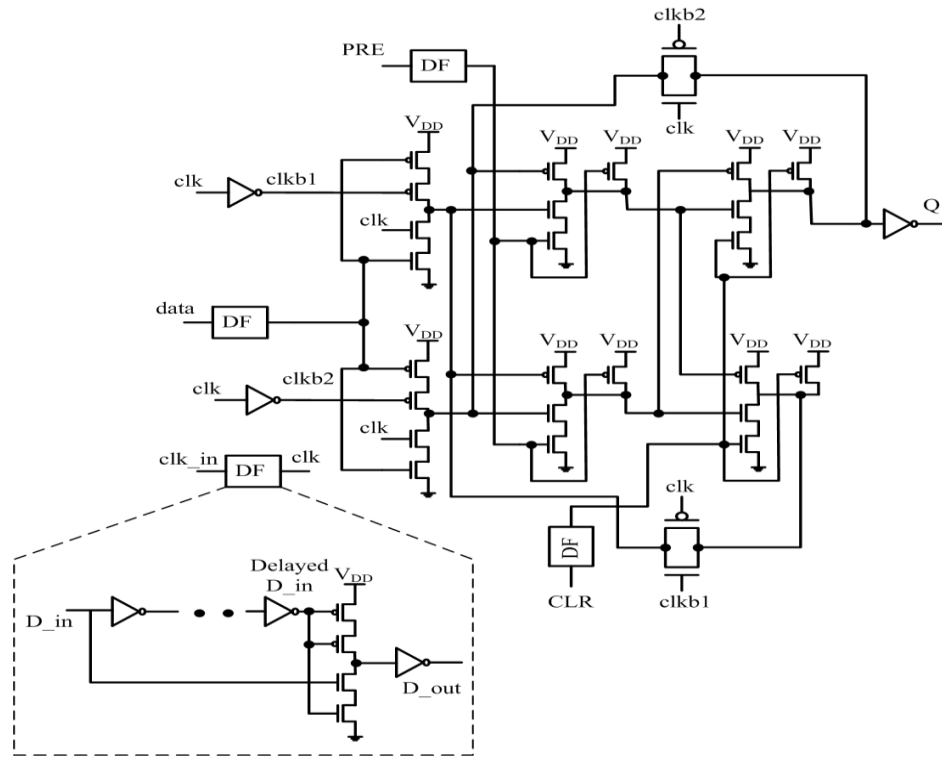
Figure 2.2: Delay-filtered DICE flip-flop reported in [14].

flip-flop can efficiently mask a data line SET; however, require large area, has large clock-to-Q delay and consumes more power even at a low data activity.

Wang et. al. reported a master-slave DICE flip-flop in [15], schematic of this flip-flop is shown in Figure 2.3. Similar to Delay-filter DICE flip-flop [14], it uses the clock signal and the complement of clock signal at the input clocked stage to conditionally write data at the DICE cell. This flip-flop has high Clock-to-Q delay and requires large area to implement. This flip-flop consumes a high power at high data activities; however, consumes a very low power at a low data activity.

Most of the DICE based flip-flop cannot mask an SET of internal node propagating to the output node. A C-element based SEU hardened dual data rate flip-flop proposed in

15
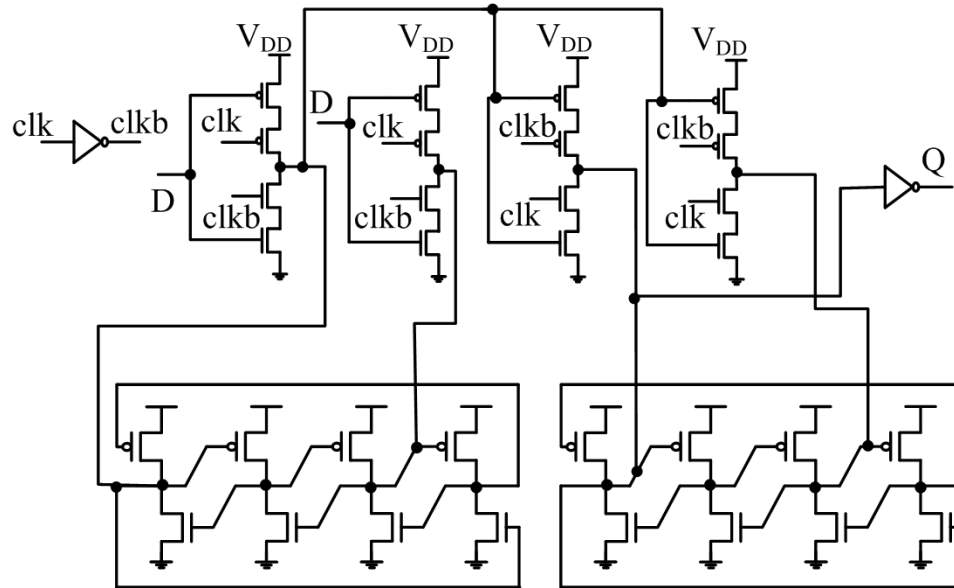
Figure 2.3: Master-slave DICE flip-flop without preset and clear [15].

[21] can efficiently serve this purpose. However, this flip-flop suffers from significant performance penalty. The dual data rate flip-flop requires large silicon area (approximately double the number of transistor than those of traditional designs) and consequently consumes more power. Thus soft error tolerant flip-flops with minimal power and high performance are of significant interest in order to meet overall power budget and reliability of microprocessor and SOCs.

2.2 Energy Recovery Flip-flops

Typically energy recovery flip-flop uses sinusoidal clock instead of conventional square wave clock to conditionally write data at the storage element. A four-phase transmission-gate (FPTG) energy recovery flip-flop was presented in [22]. It is similar to the conventional transmission-gate flip-flop (TGFF) [23], except that it uses four-transistor pass-gates designed to conduct during a short fraction of the clock period. The FPTG is a master-slave flip-flop uses four-phase sinusoidal energy recovery clock. This
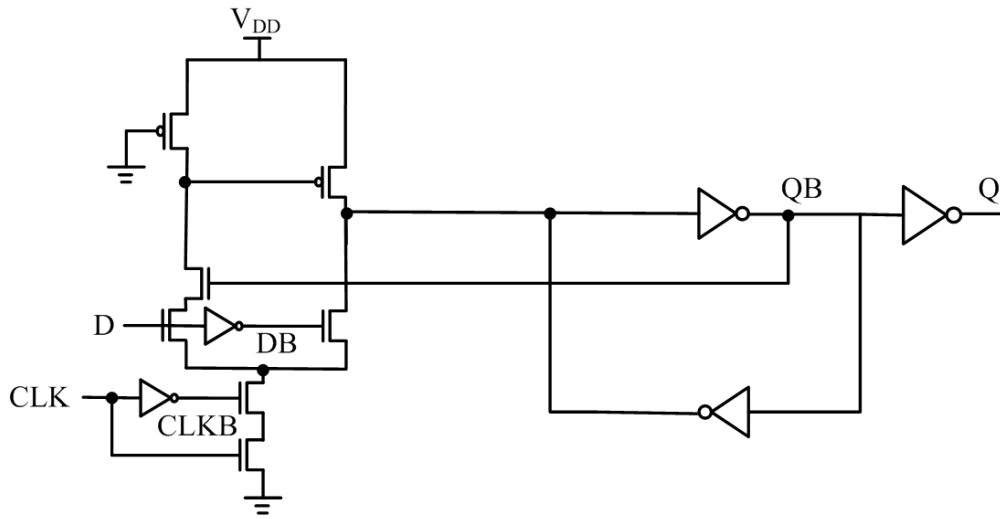
Figure 2.4: SCCER flip-flop reported in [24].

flip-flop has large data to output delay and the transmission gate MOSFETs are large, which consequently increase power consumption. In addition, the use of 4-phase clock increases clock distribution network complexity. The Sense amplifier energy recovery (SAER) flip-flop proposed in [24] consumes more power due to overlap between evaluation and precharge phases and its internal nodes are charging and discharging at every clock cycle regardless of any data activity. The static differential energy recovery (SDER) is a static pulsed flip-flop has very small Clock-to-Q ($t_{C\text{-}Q}$) delay and also eliminates the latter problem of SAER but consumes more power at high data activity [24]. SDER consumes a significant amount of power in its data input. The Single-ended conditional capturing energy recovery (SCCER) flip-flop [24] is very high-performance in terms of delay, however consumes large power at high data activity due to the stack MOSFETs at input stage (see Figure 2.4). Moreover, SCCER flip-flop uses one always 'ON' PMOS at the input stage to reduce charge sharing, which again produces high short-circuit current with sinusoidal resonant clock. The dual-edge triggered sense

amplifier flip-flop [25] and dual-edge triggered pulsed energy recovery flip-flops proposed in [26] uses chain of inverters to generate pulse signal. These flip-flops consume more power due to increasing number of transistors and the charging-discharging of internal node, particularly at low data activities. While these energy recovery flip-flops may offer a lower-power solution in comparison with traditional square-wave clock flip-flops, the energy recovery flip-flops are not soft error robust. Therefore, in order to achieve a low-power clocking scheme without compromising the reliability, designing soft error tolerant energy recovery flip-flops is critical.

Chapter 3 Proposed Soft Error Robust Flip-flops

This chapter presents the proposed soft error robust flip-flops with their circuit constructions and transient simulations. The flip-flops are categorized into two groups: i) flip-flops with square wave clock, and ii) flip-flops with energy recovery clock.

3.1 Proposed Flip-flops with Square-wave Clock

3.1.1. A True Single Phase Clock (TSPC) Soft Error Robust Flip-flop

The first proposed flip-flop is a DICE-based true single phase clock (TSPC) flip-flop. Figure 3.1 shows the proposed flip-flop. The true single phase architecture limits the effect of the negative bias temperature instability (NBTI). NBTI is a MOS degradation mechanism that increases PMOS threshold voltage over time due to the diffusion of hydrogen in the gate dielectric of 'ON' PMOS. Since the PMOS transistors in a TSPC input stage are 'OFF' for more than half of their lifecycle, the NBTI effect on those transistors and hence on the setup and hold time of the flip-flop is minimal. The proposed flip-flop consists of a TSPC input stage, the SEU hardened DICE latch, and a C-element output stage. An equalizer transistor M18 works in conjunction with the input stage to enable writing into the DICE latch at the rising edge of the clock (*clk*). For a stored data value of '1' in the flip-flop, the voltages at internal nodes X_0, X_1, X_2, and X_3 are '1', '0',
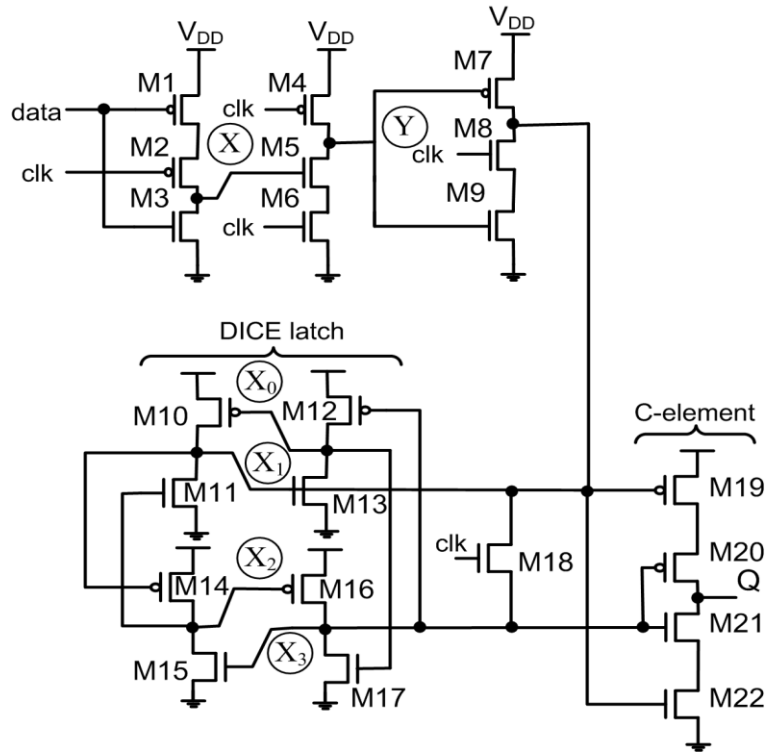
Figure 3.1: TSPC DICE soft error robust flip-flop.

'1', and '0', respectively. For a stored data value of '0', the node voltages are the opposite.

The operation of the flip-flop can be described with reference to Figure 3.1 and Figure 3.2. When clk='0', node X is precharged to the complement of the data while node Y is precharged to '1'. Consequently, M7 and M8 are OFF, leaving node X_1 at a logic value determined by the previous value stored in the DICE latch. When clk becomes '1', the data are written into the DICE latch in two ways. If the data is '1' and clk='1', node X is '0' and node Y remains at '1' (see Figure 3.2), which pull down node X_1 and turn ON M18. A low-impedance path through M18 then pulls down node X_3, changing the voltages at nodes X_0 and X_2 from '0' to '1'. Since nodes X_1 and X_3 are both '0', output
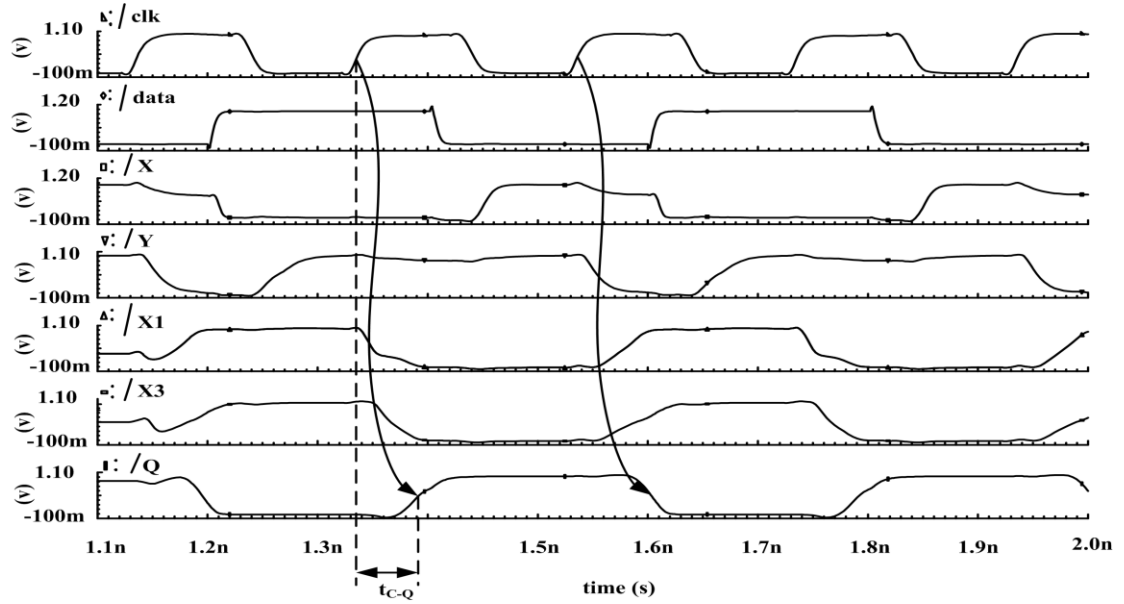
Figure 3.2: Simulation waveforms of the TSPC DICE flip-flop.

node Q is pulled up to '1', which is the same as the input data. On the other hand, if the data is '0' and clk='1', node X is '1' and node Y is pulled down to '0'. This pulls up node X_1 through M7 if node X_1 (and hence node X_3) was previously holding '0'. Subsequently, node X_3 is also pulled up through M18 and M16, updating nodes X_0 and X_2.

The pull-up of the node X_3 potential using the equalizer M18, requires M18 and M7 to be large enough to quickly overpower M17, which is driven by node X_0. In addition, M13 and M15 are made slightly larger than the minimum sized M11 and M17 in order to make the writing process faster. Here, the DICE latch is written by driving both nodes X_1 and X_3 to the same potential. In contrast, it is assumed that an SET can affect only one node of the DICE latch, thus failing to upset it. In order to validate this assumption in the implemented design, similar potential nodes (nodes X_1 and X_3 or nodes X_0 and X_2) were placed as far as possible in the layout. Such layout minimizes
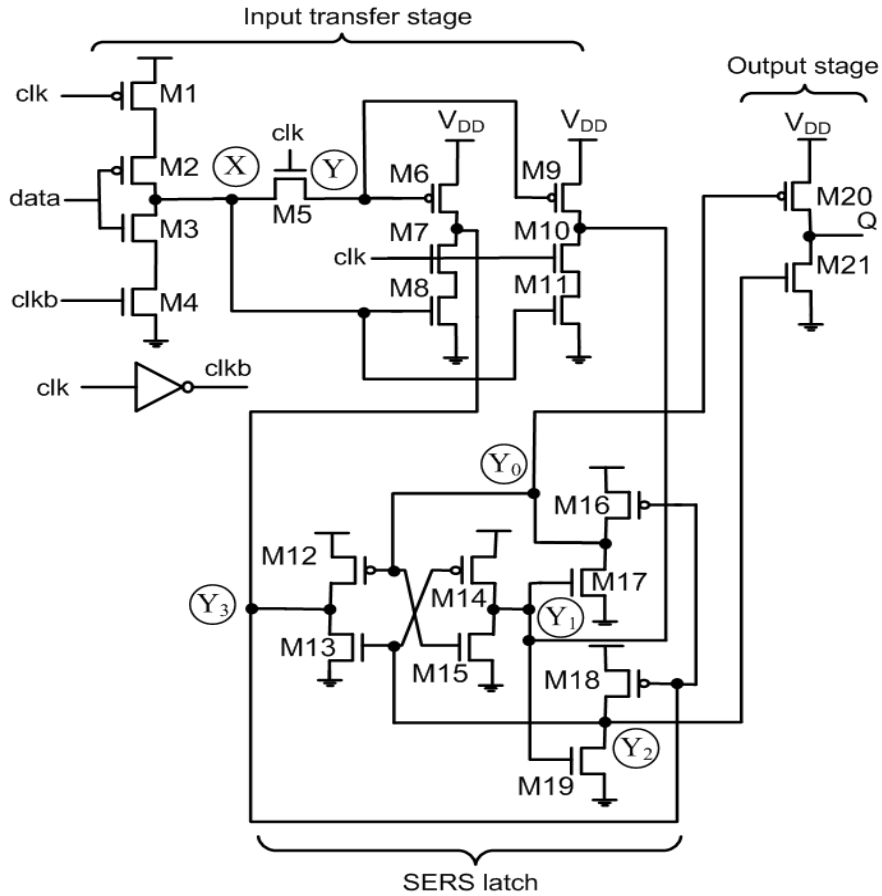
Figure 3.3: Clocked prechrage soft error robust flip-flop.

neighbouring nodes charge sharing, which can potentially upset the DICE latch in nanometric technologies [27]-[28].

3.1.2. Clocked Precharge Soft Error Robust Flip-flop

The proposed clocked precharge soft error robust (CPSER) flip-flop is shown in Figure 3.3. It has a clocked input transfer unit, a soft error robust storage (SERS) latch, and an output buffer. The input transfer unit has a clocked transistor stack that conditionally passes the data and its complement to the latch. Similar to the DICE latch, SERS latch has four storage nodes, Y_0, Y_1, Y_2, and Y_3, where Y_1 and Y_3 nodes store the
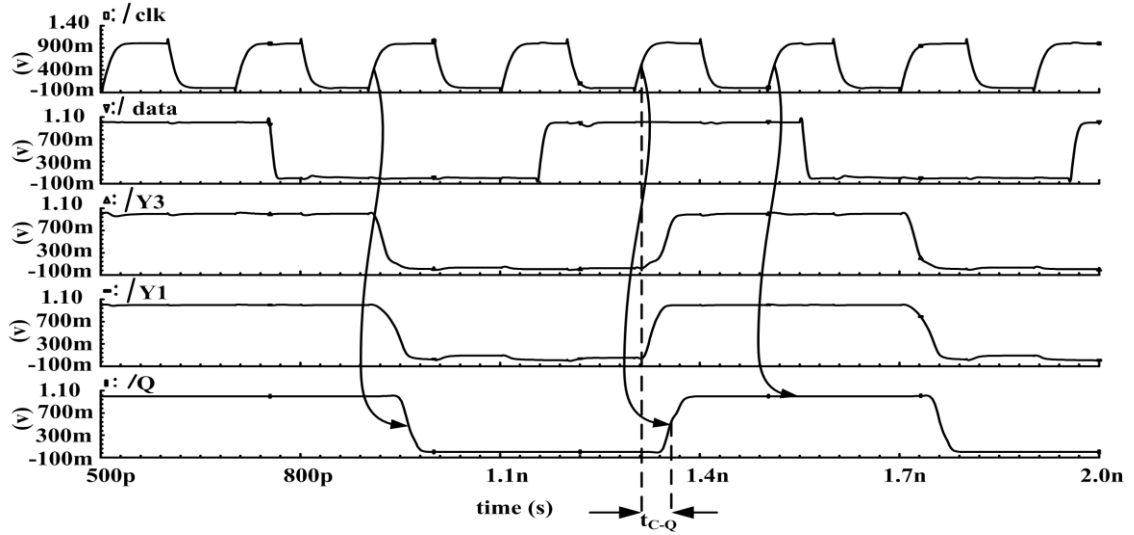
Figure 3.4: Simulation waveforms of the CPSER flip-flop.

data while Y_0 and Y_2 nodes store the compliment of data. Each of these four nodes is driven by one NMOS and one PMOS transistor. However, unlike the DICE latch, PMOS pair M16 and M18 has a common gate Y_3 while NMOS pair M17 and M19 has a common gate Y_1. This arrangement makes writing into the SERS cell easier through the input transfer unit. On the other hand, the SERS cell prevents unintentional flipping of data by an SET.

The operation of the (CPSER) flip-flop can be described with reference to Figure 3.3 and Figure 3.4. When the clock (*clk*) signal is '0' and *clkb* is '1' (M1 and M4 turns ON), depending on the data signal (high or low), the complement of data is passed to node X in two ways. If node X is low, with the rising edge of *clk* signal node Y discharges through NMOS M5. As a result, PMOS M6 and M9 turns ON to charge up node Y_3 and node Y_1, writing '1' data at SERS cell. In contrast, if node X is high (data is low), node Y_1 and node Y_3 are pulled down to V_{SS} by M7-M8 and M10-M11 pull-down pairs at rising edge of *clk*, thus writing '0' data at the SERS cell. In each case, the node X

23

signal requires to be stable before the rising edge of the c*lk* signal. This result in a positive setup time (see Figure 3.5).

In order to reliably write into the SERS latch, a careful design of the transfer unit is necessary. In particular, the effective resistances of the NMOS stack at the transfer unit have to be lower than those of the PMOS transistors driving node Y_1 and Y_3. In particular, the effective resistance of transistor pairs M7-M8 and M10-M11 requires to be lower than that of single PMOS M12 and M14, respectively. On the other hand, the effective resistance of single PMOS transistor M6 and M9 requires to be lower than that of single NMOS M13 and M15, respectively in the SERS latch.

In order to reduce the power and delay of the CPSER flip-flop, the sizing of the transistor stack M6-M8 is made different from the stack M9-M11. In particular, the size of M9 is larger than M6. This is because, M9 pulls up node Y1 and if Y1 is pulled up faster, it will quickly turn on the two NMOS transistors M17 and M19, reducing the write time into the SERS latch. Consequently, the clock to output (C-Q) delay decreases. On the other hand, M6 is used to just pull up Y3 and turn off two PMOS transistors M16 and M18. Similarly, the size of M7-M8 is larger than the size of M10-M11. Such design enables significant power saving without degrading flip-flop performance.

The 2-input output buffer is driven by the storage node Y_0 and Y_2, which hold the same logic value. If any one of these nodes is affected by an SET, the SET can propagate to the output (Q). A sufficient large SET at node Y_0 (or at node Y_2) has the potential to change the output. Similar to TSPC DICE flip-flop a C-element output buffer can eliminate this problem; however, it will increase the transistor count, power, and delay.
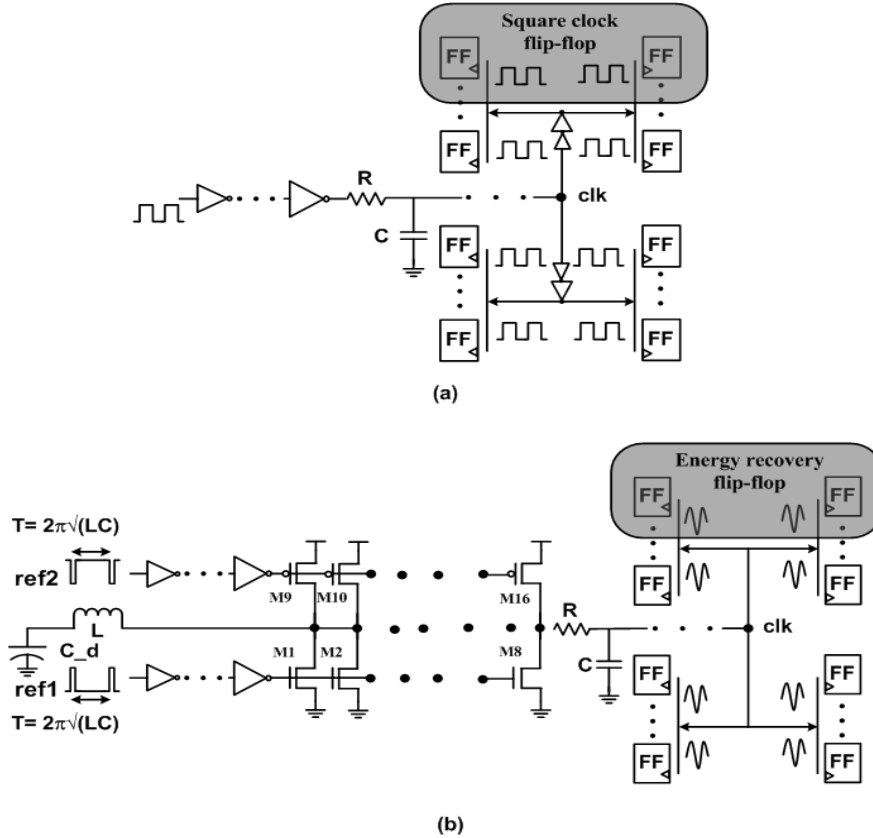
Figure 3.5: a) Traditional clocking scheme and b) resonant energy recovery clocking scheme (*R* and *C* represent the resistance and capacitance of clock network).

3.2 Proposed Flip-flops with Energy Recovery Clock

3.2.1. Energy Recovery Clocking

Unlike the traditional square wave clock (see Figure 3.5(a)), the energy recovery clock generator is a single-phase resonant clock generator [24], [29], the frequency of oscillation of which is given by:

$$f = \frac{1}{2\pi\sqrt{L(\frac{C \times C\_d}{C + C\_d})}},$$ (3.1)

where C is the total capacitance of the clock network including gate capacitances associated with clock inputs of all flip-flops, C_d is the input decoupling capacitance [25], and L is the lumped on-chip inductor. To sustain the oscillation, the clock generator needs to compensate for the loss in the network. This can be achieved by pulling down the clock signal to ground by the equal sized NMOS transistors (M1-M8) in Figure 3.5(b) when the clock signal reaches its minimum. The equal sized PMOS transistors (M9-M16) can be added (see Figure 3.5(b)) to make the clock generator robust against process-voltage-temperature (PVT) variations. In order to eliminate the short-circuit current, the gate control signals of these PMOS and NMOS transistors are $180°$ out of phase. By variation in the pulse width of the reference signals (ref1 and ref2 of Figure 3.5(b)) and the size of the driver transistors, the amplitude of the generated *clk* signal can be controlled. Since in a specific network, the capacitance C is fixed, the inductance L is tuned to achieve different frequencies ranging from 5GHz to 1GHz using the Eq. (3.1). The energy recovery clock can be at the global level with local or sector square-wave clock buffers [29] or at both global and local levels without any local buffers [24]. The proposed flip-flops are intended for the latter scheme, which is more power efficient.

3.2.2. Soft Error Robust Flip-flop with Energy Recovery Clock

The previous sub-section presented energy recovery clocking scheme for flip-flops. In the subsequent sections, the thesis will present a variety of high performance soft error tolerant flip-flops that work with the energy recovery clock in order to reduce both the SER and the clock power of the chip. By working with the energy recovery clock, the flip-flop enables recovering energy from the gate capacitances associated with its clock inputs and eliminates the need for local buffers, which would have been required for a
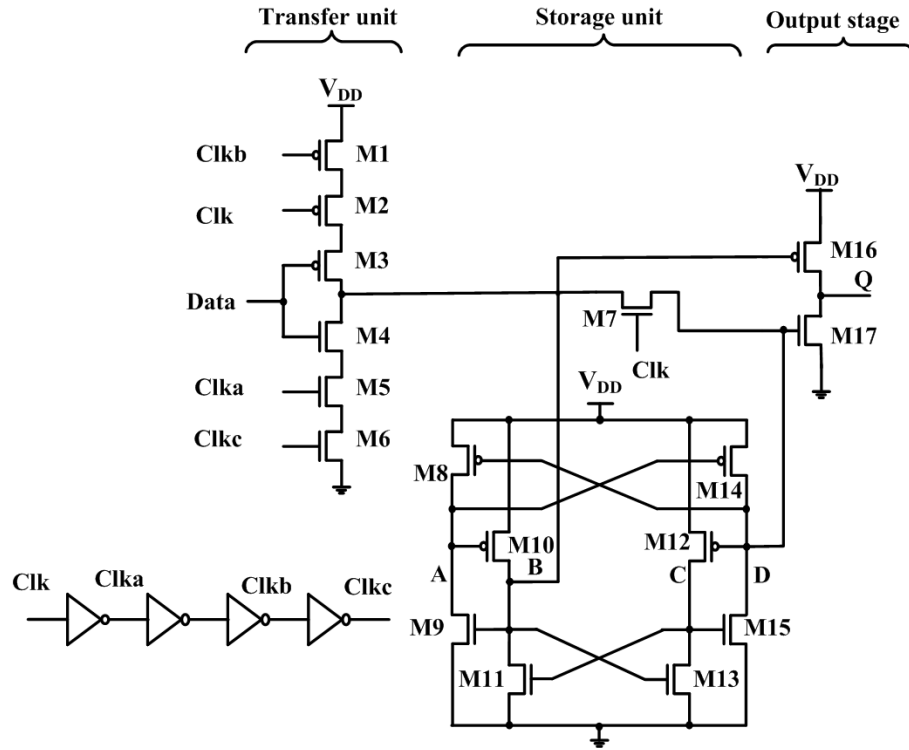
Figure 3.6: Soft clock edge SEU hardened (SCESH) energy recovery flip-flop.

square-wave clock. The flip-flops are based on eight transistor soft error robust storage cell and unique input and output stages.

3.3 Soft Clock Edge SEU Hardened (SCESH) Energy Recovery Flip-flop

The proposed soft clock edge SEU hardened (SCESH) energy recovery flip-flop is shown in Figure 3.6. It has an input transfer unit, a soft error robust Quatro latch [30], and a two-input output buffer. The input transfer unit has a clocked transistor stack that provides a narrow time window to pass the data and its complement to the latch, thus having a soft clock edge. Similar to the DICE latch, Quatro latch has four storage nodes,
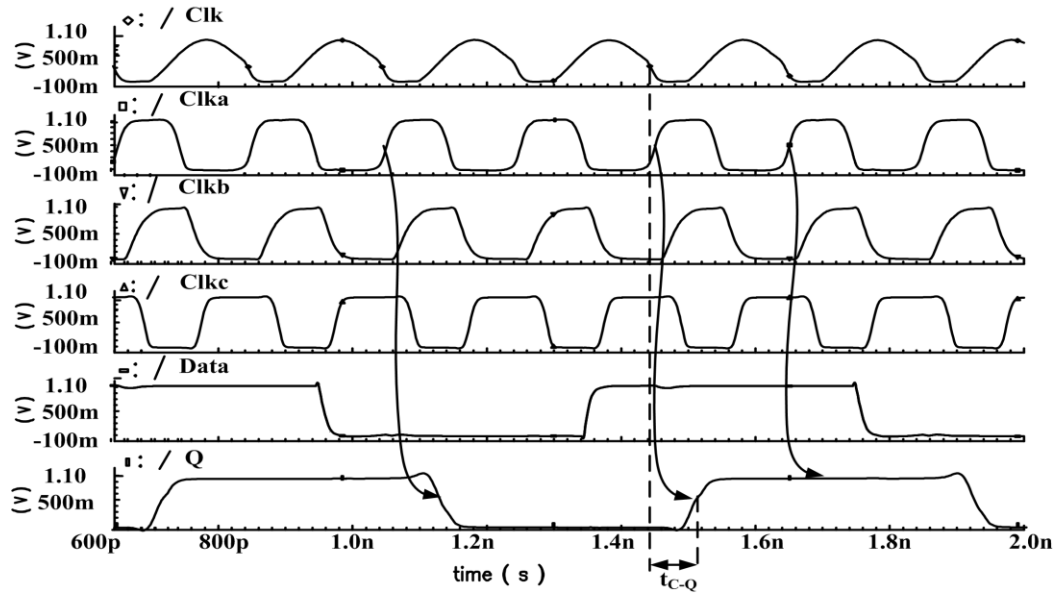
Figure 3.7: Simulation waveforms of the SCESH flip-flop.

A, B, C, and D. Here, B and D nodes store the complement of the data while A and C nodes store data acting as redundant storage nodes. Each of these four nodes is driven by one NMOS and one PMOS transistor. Unlike an inverter, the gates of these NMOS and PMOS transistors are connected to two different nodes. Since an SET can momentarily pull up (down) a node voltage, it will be restored by the corresponding NMOS (PMOS) connected to that node and driven by an unaffected node. Thus similar to SERS and DICE latch, Quatro latch provides excellent soft error immunity.

The operation of the proposed flip-flop can be described with reference to Figure 3.6 and Figure 3.7. There is a three-inverter delay between *Clka* and *Clkc*, generating a narrow time window at the transfer unit to pass logic '1' data to the output. Similarly, three-inverter delay between *Clk* and *Clkb* allows the time window to pass logic '0' data to the output. In each case, the data signal requires to be stable before the rising edge of

28
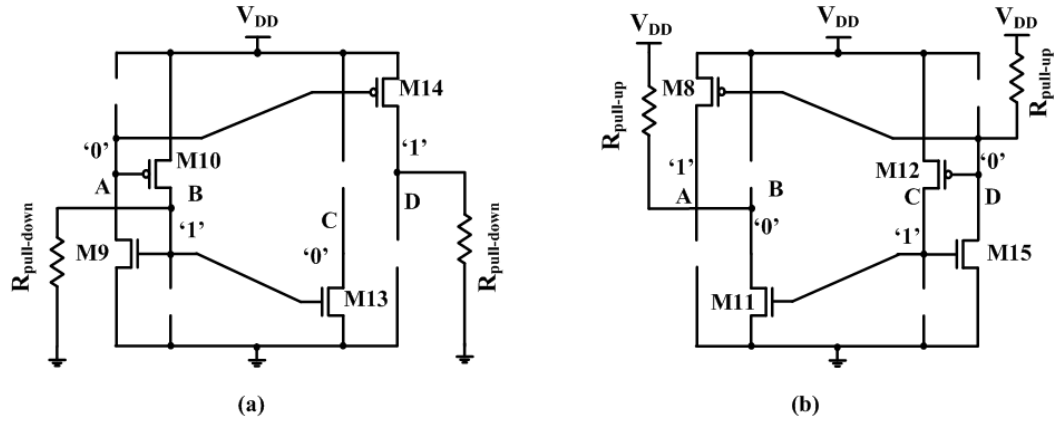
Figure 3.8: Quatro latch at the beginning of a) writing '0' and b) writing '1', for SCESH flip-flop.

the *Clka* signal. This makes the flip-flop trigger at the negative or falling edge of the sinusoidal clock (*Clk*) signal and exhibit a negative setup time.

A careful design of the transfer unit in the SCESH flip-flop is required in order to reliably write into the Quatro latch. For writing '0', the effective resistances of the NMOS stack ($R_{pull-down}$ of node B and D) in the transfer unit have to be smaller than the ON resistance of the transistor M10 or M14 (see Figure 3.8(a)). Similarly, in order to write '1', the effective resistances of the PMOS stack ($R_{pull-up}$ of node B and D) in the transfer unit have to be smaller than the ON resistance of the transistor M11 or M15 (see Figure 3.8(b)). An equalizing transistor M7 is used to work in conjunction with the input transfer unit to write data into the Quatro latch. In fact, in order to write into the Quatro latch, two nodes having the same logic value (nodes storing '1' or nodes storing '0') need to be driven to the new value. Driving only one of the nodes of the Quatro latch to logic '0' or '1' cannot write into the cell. Therefore, the key assumption behind the soft error immunity of the Quatro latch is that an SET can affect only one node in a given strike. In order to validate this assumption, two similar potential nodes (A and C or B and D) are

placed as far as possible in the layout. However, due to the small geometry of the transistors in the nanoscale technology, an SET can affect multiple nodes by causing charge sharing among the neighbouring nodes. Accordingly, this thesis investigate the robustness of the proposed flip-flop to multiple node SETs.

Similar to CPSER flip-flop, the two-input based output buffer transfers the stored data from the Quatro latch to the output. Since the inputs of the buffer (B and D) are of the same potential, they reliably transfer the data to the output. However, if an SET occurs at one of the inputs (B or D), it may selectively propagate to the output depending on the type of the SET (0→1 or 1→0). Replacing the output buffer with a C-element (like the TSPC DICE flip-flop) can filter all single SET at B or at D irrespective of their types.

3.4 Conditional Pass Quatro (CPQ) Flip-flop

The proposed energy recovery Conditional Pass Quatro (CPQ) flip-flop is shown in Figure 3.9. It consists of three stages, namely an input transfer unit with a delay element, a soft error robust Quatro latch, and an output stage. The delay element opens a small transparent window between clock (*Clk*) and its delayed complement (*Clkb*) signal to pass the data and its complement to write the data to the Quatro latch. An equalizer transistor M7 works in conjunction with the input stage to enable writing into the Quatro latch at the rising edge of the *Clk* signal. For a stored data value of '1' in the flip-flop, the voltage at internal nodes A, B, C, and D are '0', '1', '0', and '1', respectively. For a stored value of '0' the node voltage are opposite. Like the flip-flops in previous sub-
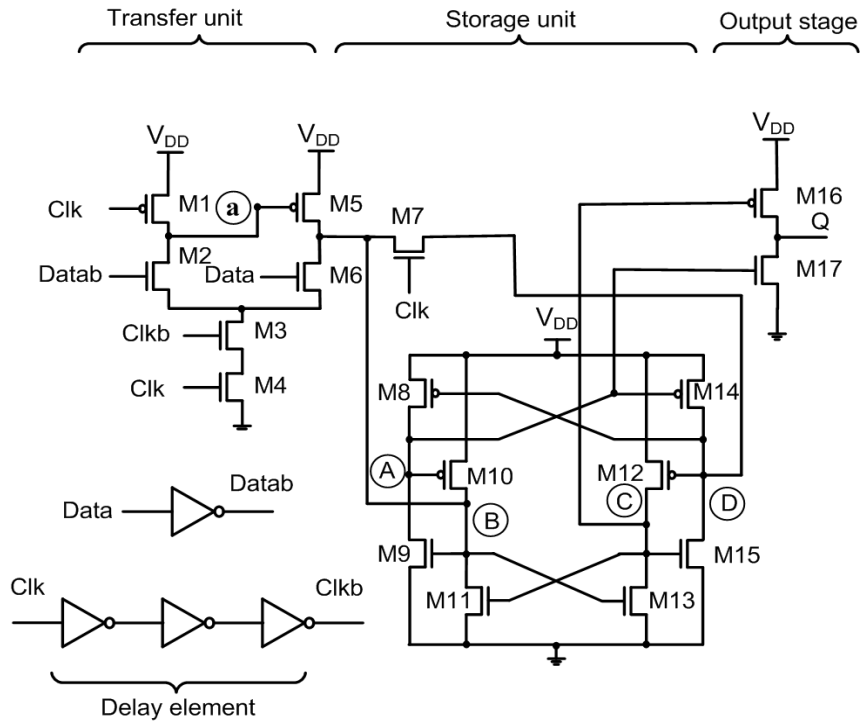
Figure 3.9: Proposed Conditional Pass Quatro flip-flop.

sections, the output stage consists of a two-input inverter buffer that masks the SET to propagate to the output.

The operation of the flip-flop can be described with reference to Figure 3.9 and Figure 3.10. There is three minimum sized inverter delay between Clk and Clkb signals, generating a narrow time window at the transfer unit to pass logic '1', or '0' data to the output. In each case, data signal requires to stable before the falling edge of the *Clkb* signal. This makes the flip-flop trigger at positive or rising edge of the sinusoidal *Clk* signal and may exhibit a negative setup time.

In order to reliably write into the Quatro latch, the current drive capability of the input transfer unit requires to-be large enough to overpower the latch. The sizing of M1 and M5 is critical to minimize charge sharing and proper functionality of the flip-flop.
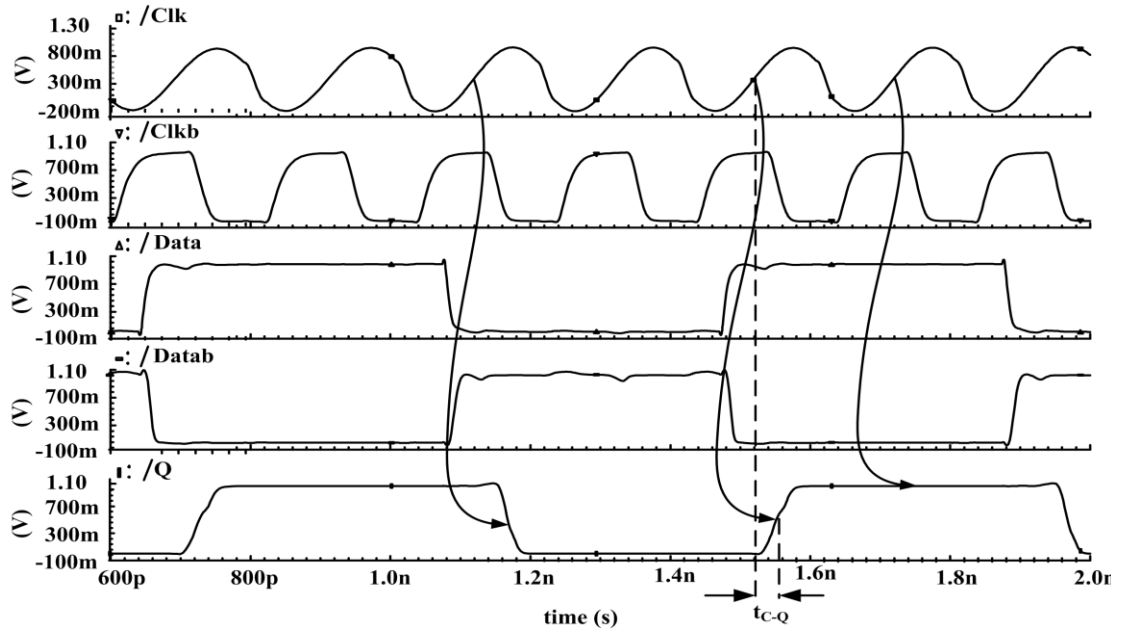
Figure 3.10: Simulation waveforms of the CPQ flip-flop.

The problem associated with the CPQ flip-flop input stage arises particularly at low data activity. For example, if the data signal are low for a long time, node 'a' will charge and discharge at every clock cycle. In order to reduce this problem, the length of M1 was increased up to 3x of minimum length of the technology, which increases the resistance between node 'V_{DD}' and node 'a'. The small clocked equalizing transistor M7 provides input transfer unit to access at two nodes of the latch, which is mandatory to write data in the Quatro latch.

3.5 Energy Recovery C²-DICE Flip-flop

Figure 3.11 shows the proposed soft error robust C²-DICE energy recovery flip-flop, which is based on the standard clocked CMOS (C²MOS) input transfer unit and the DICE latch. When the clock (*Clk*) signal is low, the first stage of the transfer unit is active. This unit acts as an inverter by paasing the inverted version of data to the node X,
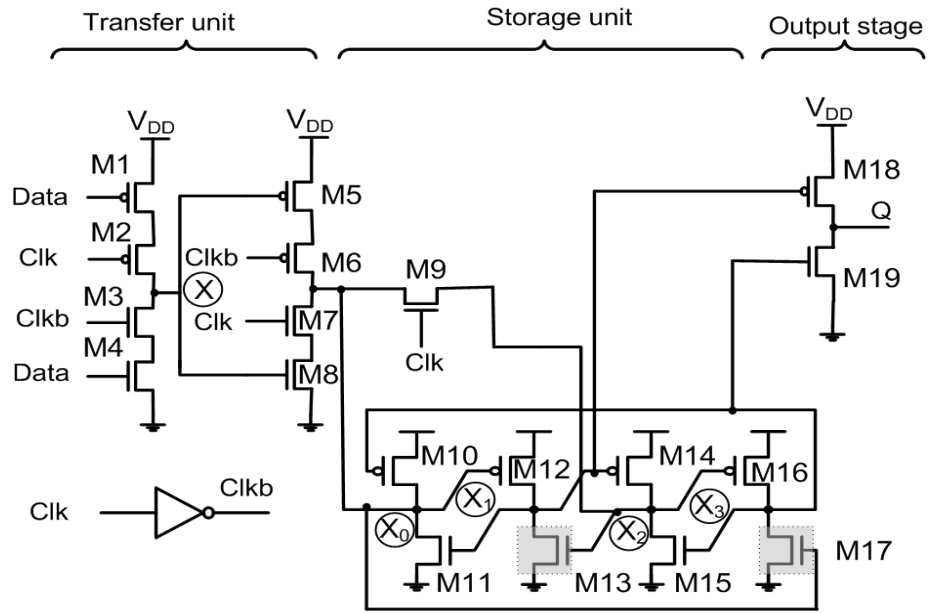
Figure 3.11 : Energy recovery C^2-DICE flip-flop.

leaving the second stage in hold mode. When the *Clk* signal is high, the first stage goes to

the hold mode (M2-M3, off) and the second stage becomes active. The value stored in

node X propagates to the output node through second stage, which acts as an inverter.

The overall circuit operates similar to a master-slave D flip-flop. Figure 3.12 presents the

simulation waveforms of the energy recovery C^2-DICE flip-flop.

Unlike master-slave D flip-flop, the storage nodes of the C^2-DICE flip-flop are

insensitive to the overlap of *Clk* and *Clkb* signal. When *Clk-Clkb* has 0-0 overlap input

register stage can be redrawn as Figure 3.13(a). In this figure, both M1 and M2 of master

stage are ON during this overlap period. In order to operate correctly as edge triggered

flip-flop, none of the new data sampled during overlap window should propagate to the

node X_0. Thus, new data are sampled on node X can make a 0-to-1 transition during

overlap period. Since NMOS devices M5 and M7 are turn OFF, this data cannot

propagate to the output of the second stage (node X_0), making the storage node

33
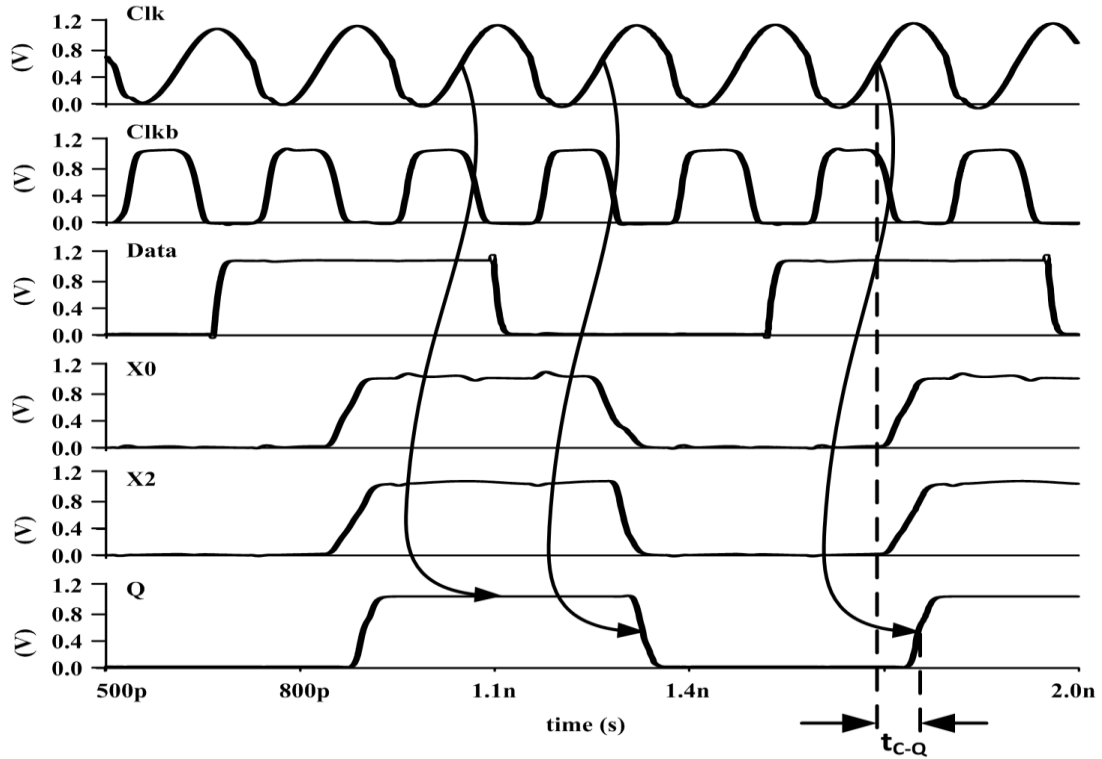
Figure 3.12: Simulation waveforms of energy recovery C2-DICE flip-flop.

unaffected by input change (see Figure 3.13(a)). At the end of the overlap period, *Clkb* = '1' and both M6 and M7 turn OFF, putting the second stage in the hold mode. Thus, any data sampled at the falling edge of the clock is not propagating to the node X_0.

Similarly, when *Clk-Clkb* has a 1-1 overlap, the NMOS devices M3 and M7 are turned ON (see Figure 3.13(b)). If the new data goes high, there will be a 1-to-0 transition at node X. However, it cannot propagate to X_0, as the PMOS device M6 is OFF (see Figure 3.13(b)). At the end of the overlap period, *Clkb* = '0' and M3 turns OFF, putting the first stage in the hold mode. However, it turns on M6 and unexpectedly the '0' at X_0 can propagate to the output. This problem is solved by imposing extra hold time in the input data. The data should not change at the overlap period [31].

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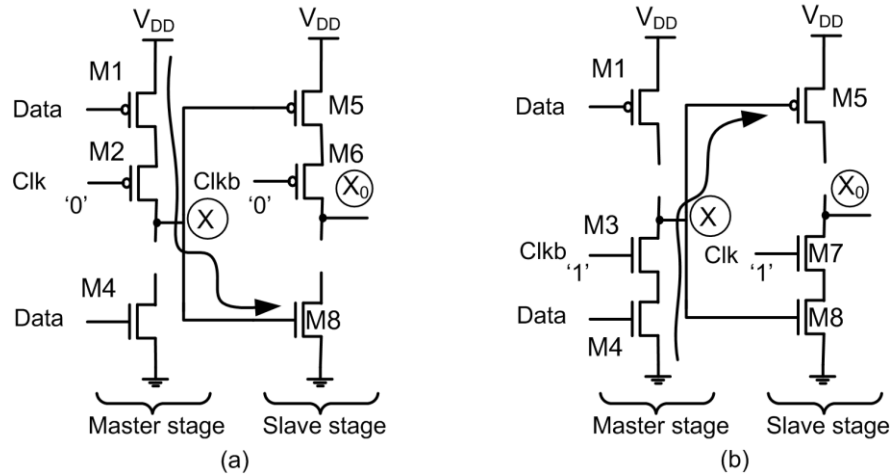
Figure 3.13: Overlap periods of energy recovery C^2-DICE flip-flop input stage [31].

Unlike the CPQ flip-flop, the C^2-DICE flip-flop has positive setup time, however, it triggers at the positive or rising edge of the sinusoidal *Clk* signal. Similar to CPQ flip-flop, the C^2-DICE flip-flop also utilizes an equalizing transistor M9 to access the two storage nodes of the DICE latch. The pull-up of the node X_2 potential using the equalizer M9 requires M5, M6 and M9 to be large enough to quickly overpower M15 which is driven by node X_3. In addition, M13 and M17 are made slightly larger than M11 and M15 in order to facilitate the writing process faster.

3.6 TSPC Energy Recovery Flip-flop

The proposed true single phase clock energy recovery (TSPCER) SEU hardened flip-flop is shows in Figure 3.14. The flip-flop consists of an improved true single phase clock input stage, a soft error robust Quatro latch, and a two-input output buffer. The operation of the flip-flop can be described with reference to Figure 3.14 and Figure 3.15. When the *Clk* signal is '0', node X is precharged to the complement of data while node Y is precharged to high '1'. Accordingly, M7 and M8 are OFF, leaving node B at a logic
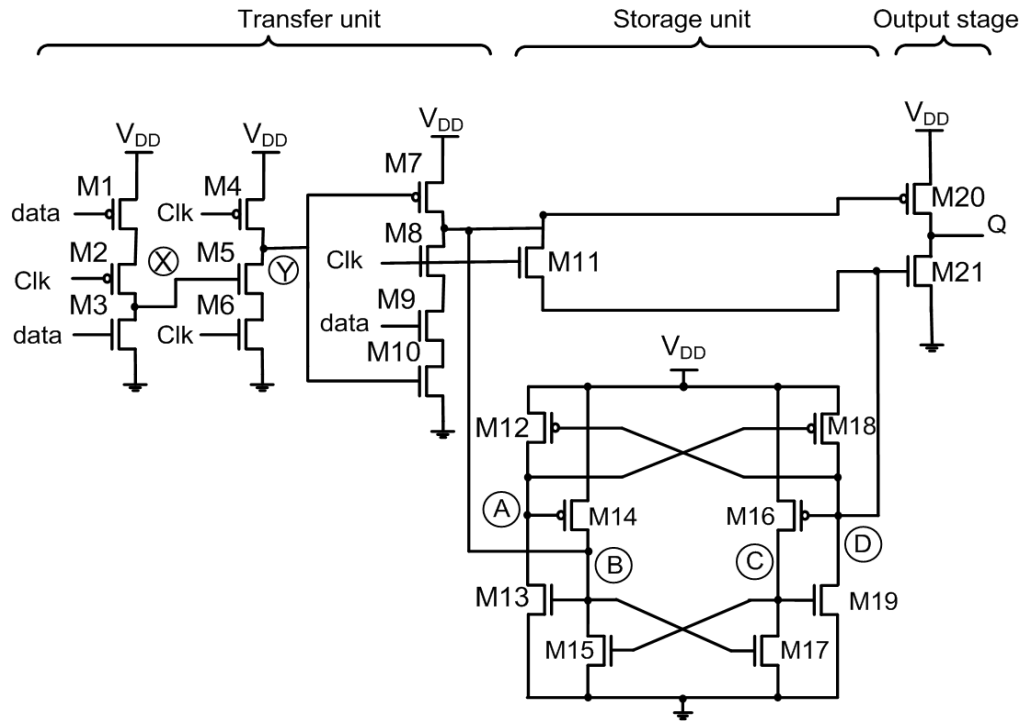
Figure 3.14: TSPC energy recovery Flip-flop.

value determined by the Quatro latch. When *Clk* becomes '1', the data is written into the Quatro latch in two ways. If the data is '1', node X becomes '0' and M8 turns on. Consequently, at the rising edge of *Clk* signal, node B is pulled down to '0'. A low impedance path through M11 then pulls down node D (see Figure 3.15), changing the voltage at nodes A and C from '0' to '1'. Since node B is '0', output node 'Q' is pulled up to '1'. On the other hand, when the data is '0' and *Clk* = '0', node X is precharged to '1'and with the rising edge of *Clk* signal, node Y is pulled down to '0'. This pulls up node B and with the help of M11 node D is pulled up. The pull up of node D potential using the equalizer M11 requires M7 and M11 to be large enough to quickly overpower M19, which is driven by node C.
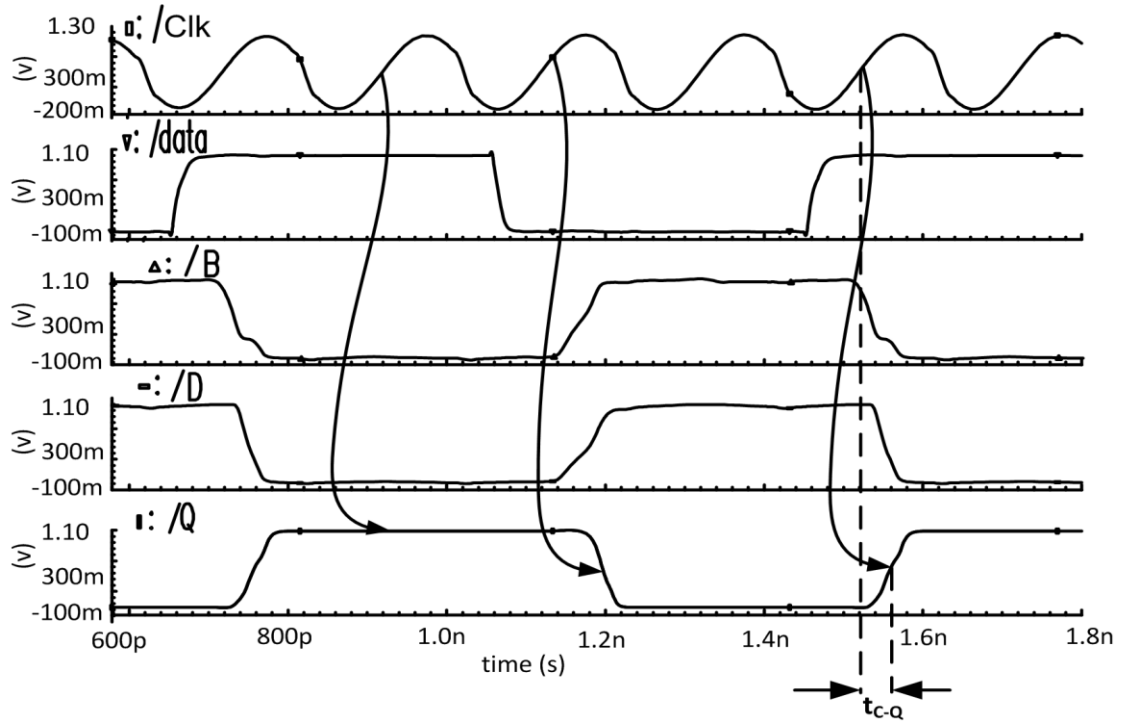
Figure 3.15: Simulation waveforms of TSPC energy recovery flip-flop.

The problem associate with the traditional TSPC register is when the data is low and at low data switching activity glitches may appear at the output node. The purpose of M9 is to reduce the internal nodes charging-discharging and completely remove glitches from output. Figure 3.16(a) shows the traditional TSPC register and the simulation waveform of that register with glitches. The improved TSPC register and its simulation waveforms are shown in Figure 3.16(b).
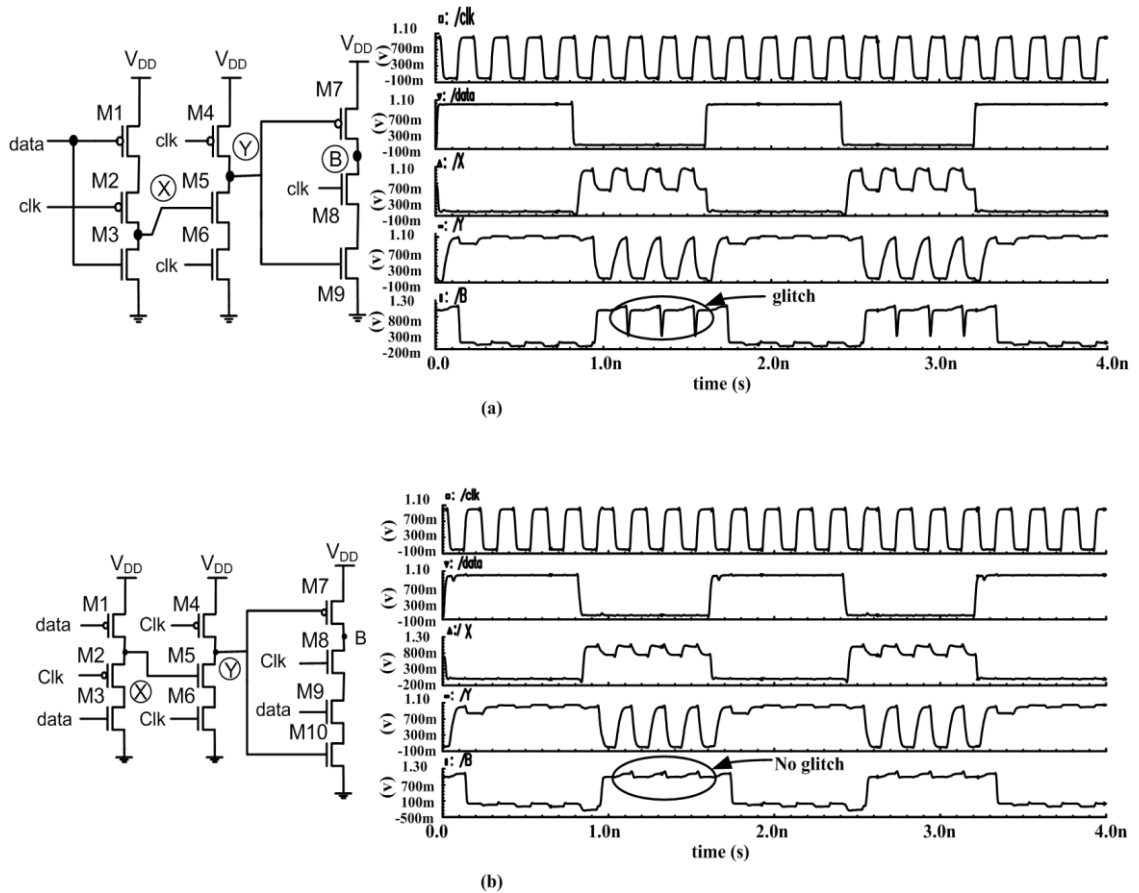
Figure 3.16: a) Traditional TSPC register with glitch and b) proposed TSPC register without glitch.

3.7 An Alternate TSPC Energy Recovery (ATSPCER) Flip-flop

The proposed alternate TSPC energy recovery (ATSPCER) flip-flop is shown in Figure 3.17. It has an input transfer unit, a soft error robust DICE latch, and a two-input output buffer. The input transfer unit has a clocked transistor stack that provides a narrow time window to pass the data and its complement to the latch.
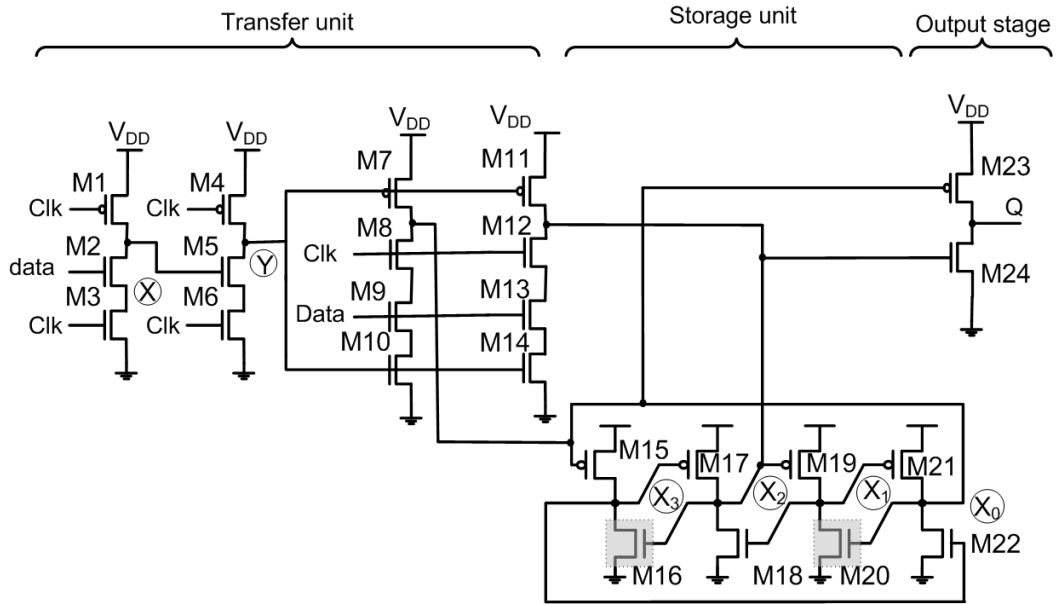
Figure 3.17: An alternate TSPC energy recovery flip-flop.

The operation of the proposed flip-flop can be described with reference to Figure 3.17 and Figure 3.18. When the clock (Clk) is '0' the nodes X and Y precharged to '1'. Consequently, M3, M6, M8, M11 and M12 are OFF, leaving nodes X_0 and X_2 at a logic value determined by the DICE latch. When the Clk is '1', the data are written into the DICE latch in two ways. If the data and Clk are '1', node X is '0' and Y remains at '1' which pulls down the nodes X_0 and X_2 (see Figure 3.18), updating the DICE latch value and driving output Q to '1'. On the other hand, if the *data* is '0' and Clk is '1', node X is '1' and node Y is pull down to '0'. This turned on M7 and M11 to pull up nodes X_0 and X_2, resulting low '0' output. Figure 3.18 clarifies that the proposed flip-flop has no glitches at the output at low data activity. Due to the large rise time of sinusoidal clock, the flip-flop can have a negative setup time.
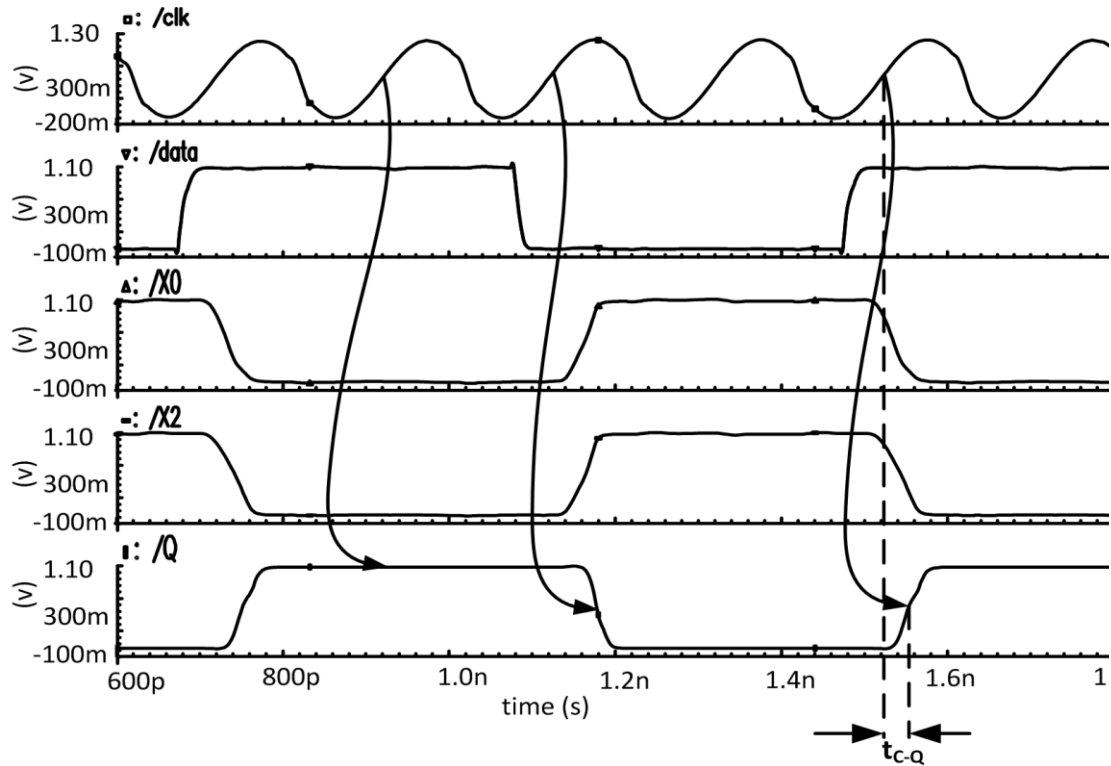
Figure 3.18: Simulation waveforms of ATSPCER flip-flop.

In order to reliably write into the DICE latch, a careful design of the transfer unit is required. In particular, M7 and M11 should be large enough to quickly overpower M22 and M18, respectively. In addition, M16 and M20 are made slightly larger than minimum sized M18 and M22 in order to facilitate writing process faster. In fact, by driving both nodes X_0 and X_2 to the same potential, I wrote into the DICE latch. Thus a particle strikes at single node failing to upset it. The two-input output buffer is driven by the storage node X_0 and X_2, which hold the same logic value.

Chapter 4 Performance Comparison of Proposed Flip-flops

This chapter compares the layout area and performance of the proposed flip-flops with recently reported competing flip-flops.

4.1 Area and Power Consumption

In order to have a fair comparison, I have designed and laid out the proposed TSPC DICE flip-flop, CPSER flip-flop, SCESH flip-flop, CPQ flip-flop, C^2-DICE flip-flop, TSPCER flip-flop, ATSPCER flip-flop along with a conventional master-slave D flip-flop (MS DFF), a master-slave DICE flip-flop without preset and clear [15], a pulsed DICE flip-flop [12], a Quatro impulse flip-flop [16], and a SCCER flip-flop [24], in a commercial 65nm CMOS technology. The layout areas of these flip-flops are listed in Table 4.1, which shows that the proposed flip-flops consume less area than the competing recently reported soft error robust flip-flops. Among the proposed flip-flops, the CPSER flip-flop requires lowest area, while SCESH flip-flop requires highest area. The proposed C^2-DICE flip-flop consumes comparable area to the SCCER flip-flop. The CPSER flip-flop requires 39% and 25% less area than those of MS DICE and pulsed DICE flip-flop, respectively. The performance of the flip-flops are then evaluated using post layout simulation at a clock frequency ranging from 5 GHz to 1 GHz and a supply voltage of 1 V. The layout of the proposed square clock flip-flops are shown in Figure 4.1. The layout of the resonant energy recovery flip-flops are presented in Figure 4.2 and Figure 4.3.

Table 4.1. Comparison of area in (μm^2).

Types of Flip-flop	Number of Transistors	Layout Area (μm^2)
MS DFF	22	12.75
MS DICE	36	23.09
Pulsed DICE	32	18.83
Quatro Impulse	28	18.20
SCCER	17	15.60
TSPC DICE	22	17.82
CPSER	23	14.12
SCESH	25	19.88
CPQ	25	18.51
C^2-DICE	21	15.72
TSPCER	21	16.49
ATSPCER	24	16.89

(a)

(b)
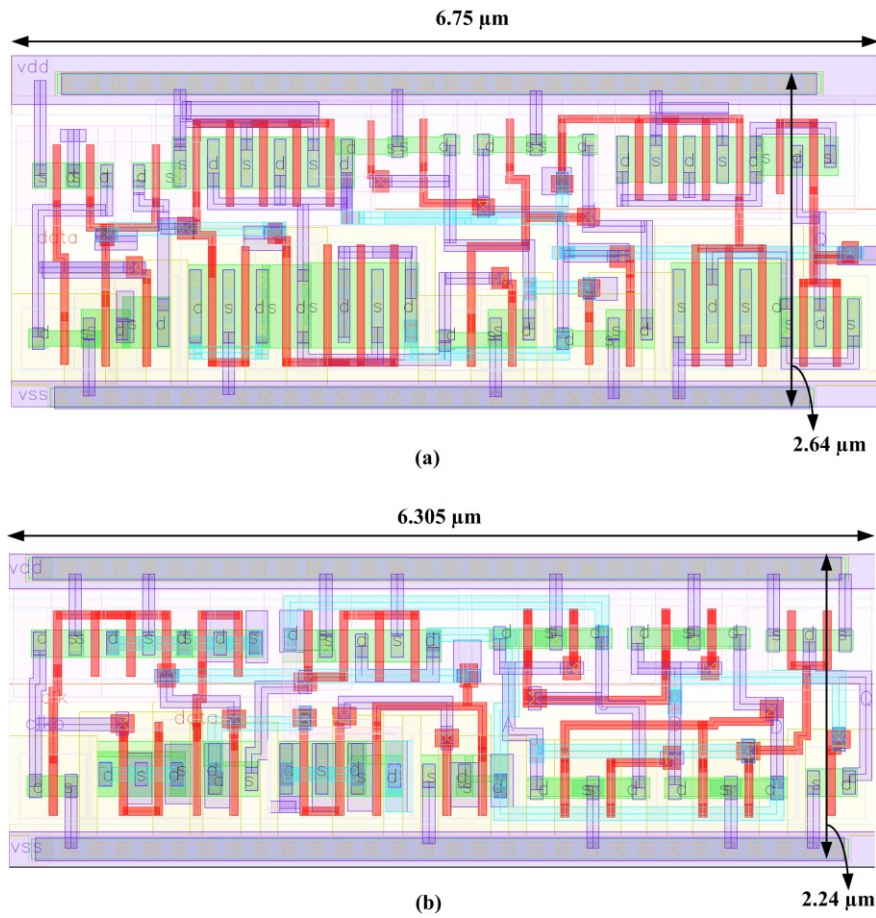
Figure 4.1: Layout of a) TSPC DICE flip-flop and b) CPSER flip-flop.

42
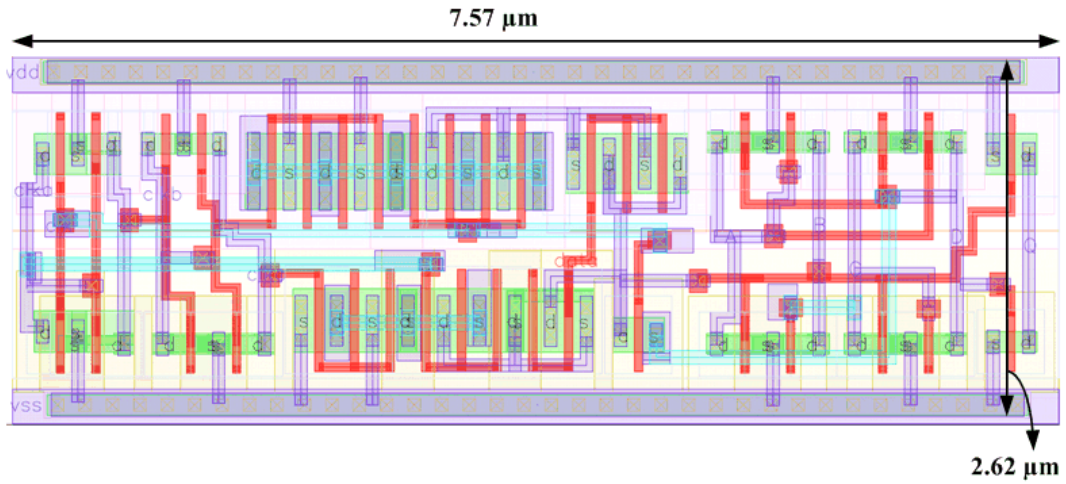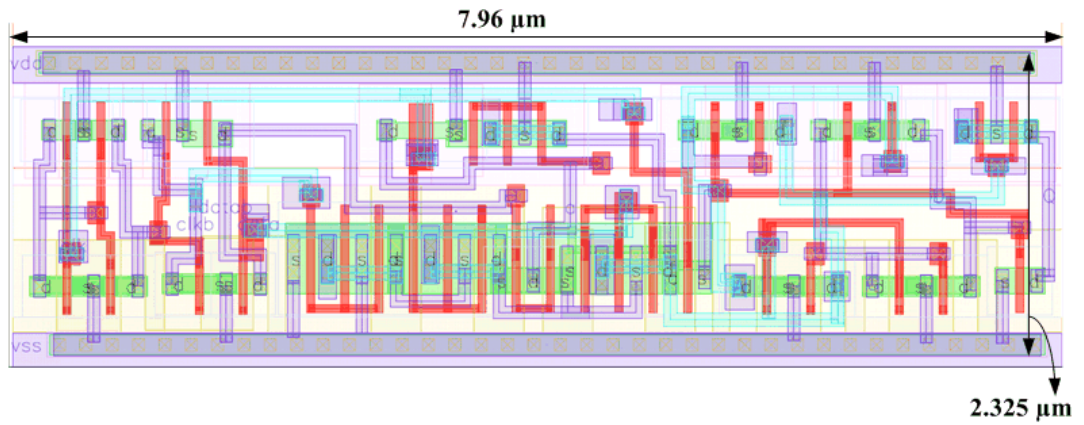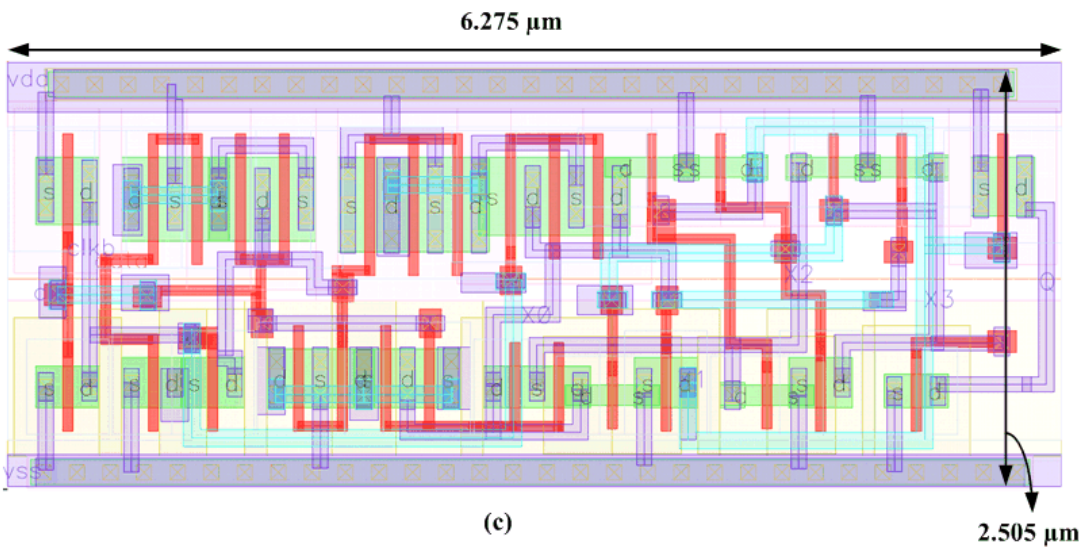
Figure 4.2: The layout of a) SCESH flip-flop, b) CPQ flip-flop, and c) C2-DICE flip-flop.
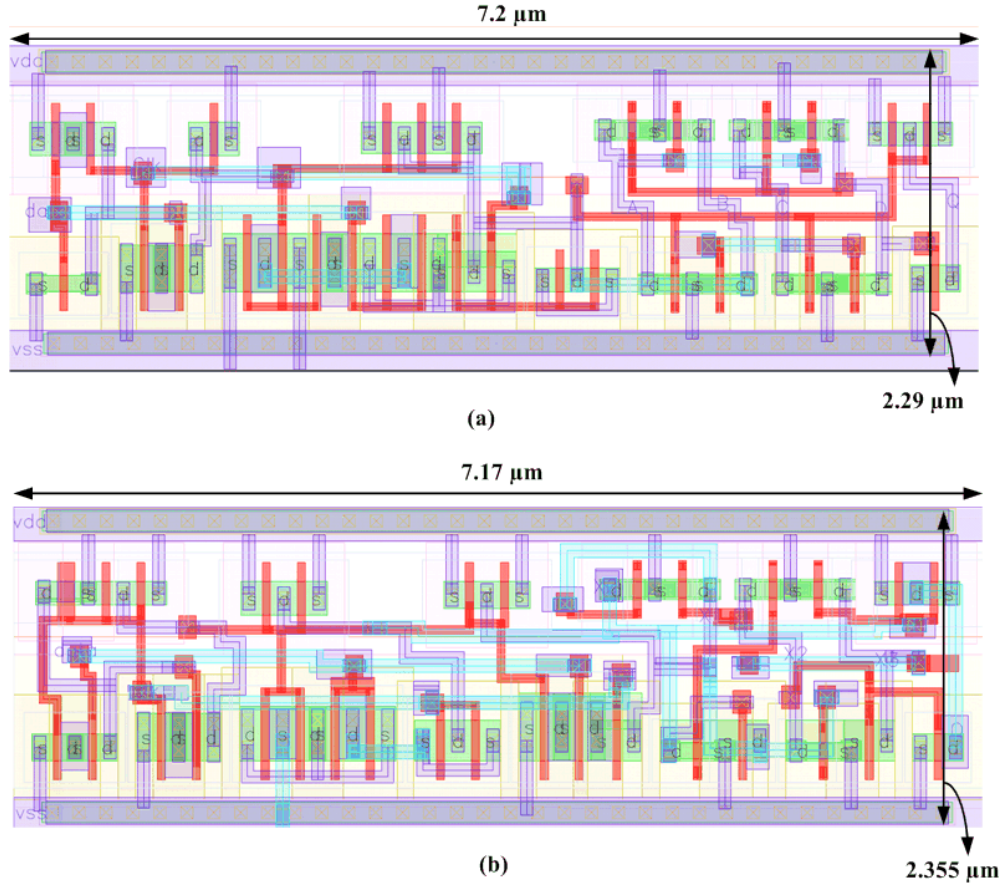
Figure 4.3: The layout of proposed a) TSPCER flip-flop and b) ATSPCER flip-flop.

In order to determine the power consumption of the flip-flops, I determined the input clock loading (P_{Clk}), data loading (P_{Data}), and internal power (P_{Int}) of the each flip-flop at different data activity. Figure 4.4(a) and Figure 4.4(b) present the test bench to determine each component of power for square clock flip-flop and sinusoidal clock flip-flop, respectively. The total power (P_T) consumption of the each flip-flop then calculated by adding the individual components: $P_T = P_{Clk} + P_{Data} + P_{Int}$ and listed in Table 4.2 at 5 GHz clock frequency. It is apparent from the Table 4.2; the proposed flip-flops consume less power than the other DICE based flip-flops. Furthermore, proposed flip-flops consume less power than energy recovery flip-flops SCCER, and SDER flip-flop. In
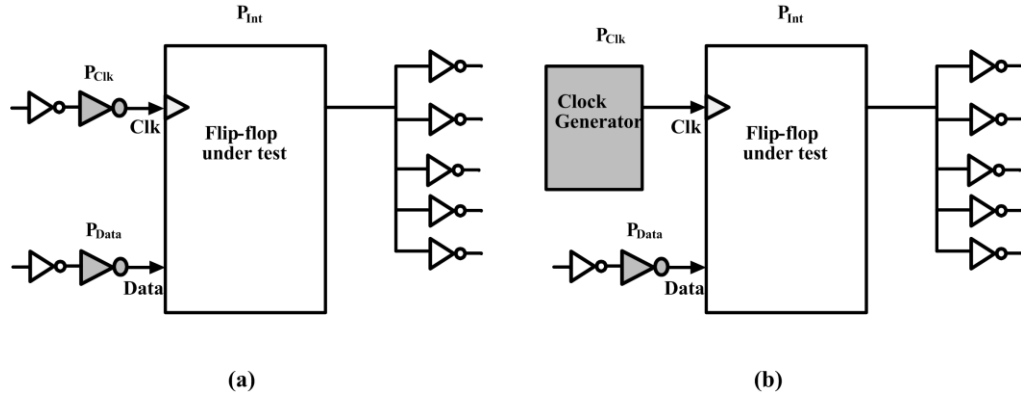
Figure 4.4: The test bench to determine each component of power for a) square clock flip-flop and b) sinusoidal clock flip-flop.

Table 4.2: Comparison of power consumption at 5 GHz clock frequency.

Flip-Flop Categories	Clock power (P_{Clk})	Data Activity (100%) Power (µw)			Data Activity (50%) Power (µw)			Data Activity (25%) Power (µw)			Data Activity (12.5%) Power (µw)		
		P_{Int}	P_{Data}	P_{FFT}	P_{Int}	P_{Data}	P_{FFT}	P_{Int}	P_{Data}	P_{FFT}	P_{Int}	P_{Data}	P_{FFT}
DFF MS	11.5	33.75	4.9	50.15	20.44	2.35	34.3	13.75	1.1	26.35	10.5	0.43	22.4
MS DICE	13.7	133	6.2	153	67.5	3.12	84.3	39	1.6	51.3	24.5	0.4	38.6
Pulsed DICE	8	75	3.1	86.1	58	1.6	67.6	49	0.8	57.8	37	0.2	45.2
Quatro Impulse	10.4	78	5	93.4	54	2.9	67.3	39	1.44	50.84	26	0.33	36.7
SDER	7	79	47.6	133.6	48	24.2	79.2	33	12	52	25.3	6.2	38.5
SCCER	9.15	67.5	9.3	86	38	4.7	52	23.4	2.4	35	16.5	1.23	27.0
TSPC DICE	16.9	74.6	2.5	94	48.6	1.26	66.8	35.6	0.63	53.1	29	0.32	46.2
CPSER	13.75	66.6	4.3	84.7	42.9	2.6	59.3	27	1.3	42	18.1	0.66	32.5
SCESH	7.8	82.6	7.0	97.4	60.9	3.7	72.4	50	1.9	59.7	44.9	0.92	53.6
CPQ	5.4	69.5	6.6	81.5	47.6	3.3	56.3	36.3	1.6	43.3	33.75	0.8	37.0
C^2-DICE	4.5	72.3	4.7	81.5	43.4	2.4	50.3	28.3	1.2	34	20.7	0.6	25.8
TSPCER	3.7	55.4	5.9	65	31.4	3	38.1	19.3	1.5	24.5	13.2	0.8	17.7
ATSPCER	5.2	55.4	5.1	65.7	34.1	2.6	41.9	23.4	1.3	29.9	18.1	0.7	24.0

addition, at low data switching activity, the power consumption of C^2-DICE is comparable to master-slave D flip-flop, while proposed TSPCER consumes 21% less power than that of DFF MS, at 12.5% data switching activity. The proposed CPQ and C^2-
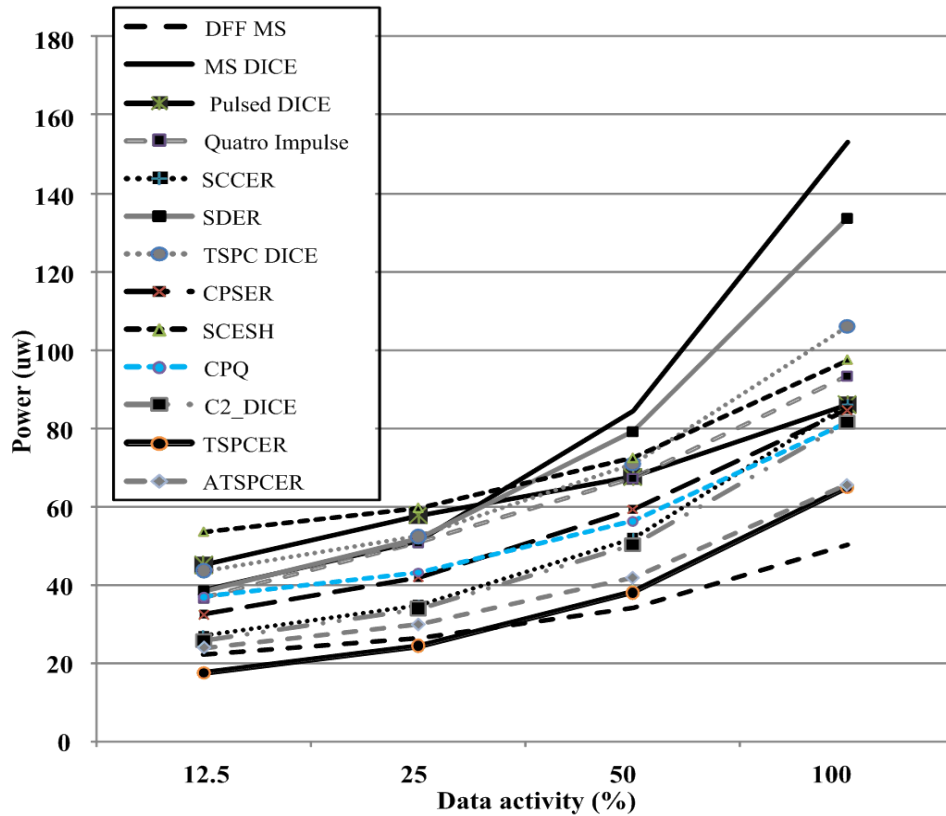
Figure 4.5: Power versus data switching activity at 5 GHz.

DICE flip-flops consume comparable power at high data activity. However with the decrease of data activity, the rate of reduction of power consumption of C^2-DICE is much higher than the CPQ flip-flop (see Figure 4.5). From 25% to lower data switching activity, the proposed TSPCER flip-flop consumes less power than rest of the competing flip-flops. Moreover, at 100% data switching activity TSPCER flip-flop consume 25% and 24% lower power than those of pulsed DICE and SCCER flip-flop, respectively. At 12.5% data switching activity, the TSPCER flip-flop consume 54% and 61% lower power when compared with MS DICE flip-flop and pulsed DICE flip-flop, respectively (see Table 4.2).
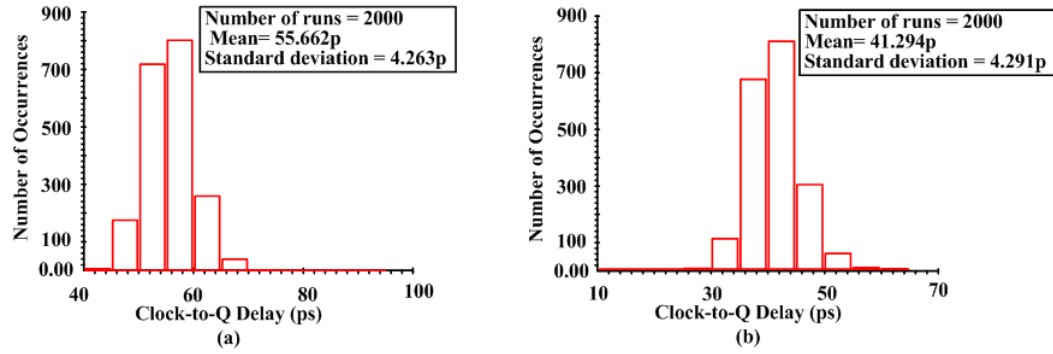
Figure 4.6: Monte-Carlo simulations of C-Q delay of the a) TSPC DICE flip-flop and b) CPSER flip-flop.

Table 4.3: Comparison of setup and hold time.

Types of flip-flop	Set up time (ps)	Hold time (ps)
MS DFF	16.7	-6
Pulsed DICE	22	23.8
SCCER	8	12
TSPC DICE	17	20
CPSER	28	7
SCESH	-35	57
CPQ	-1	3
C^2-DICE	25	34
TSPCER	21	36
ATSPCER	-2.5	28

4.2 Speed Performance

4.2.1. Delay

The Clock-to-Q (t_{C-Q}) delays of the flip-flops are measured under relaxed timing condition, which means that I made the data stable sufficiently before the arrival of the clock edge. The distribution of the C-Q delays of the square clock soft error robust flip-flops (TSPC DICE flip-flop and CPSER flip-flop) and sinusoidal clock soft error robust flip-flops (SCESH flip-flop, CPQ flip-flop, C^2-DICE flip-flop, TSPCER flip-flop, and ATSPCER flip-flop) are shown in Figure 4.6 and Figure 4.7, respectively with 2000
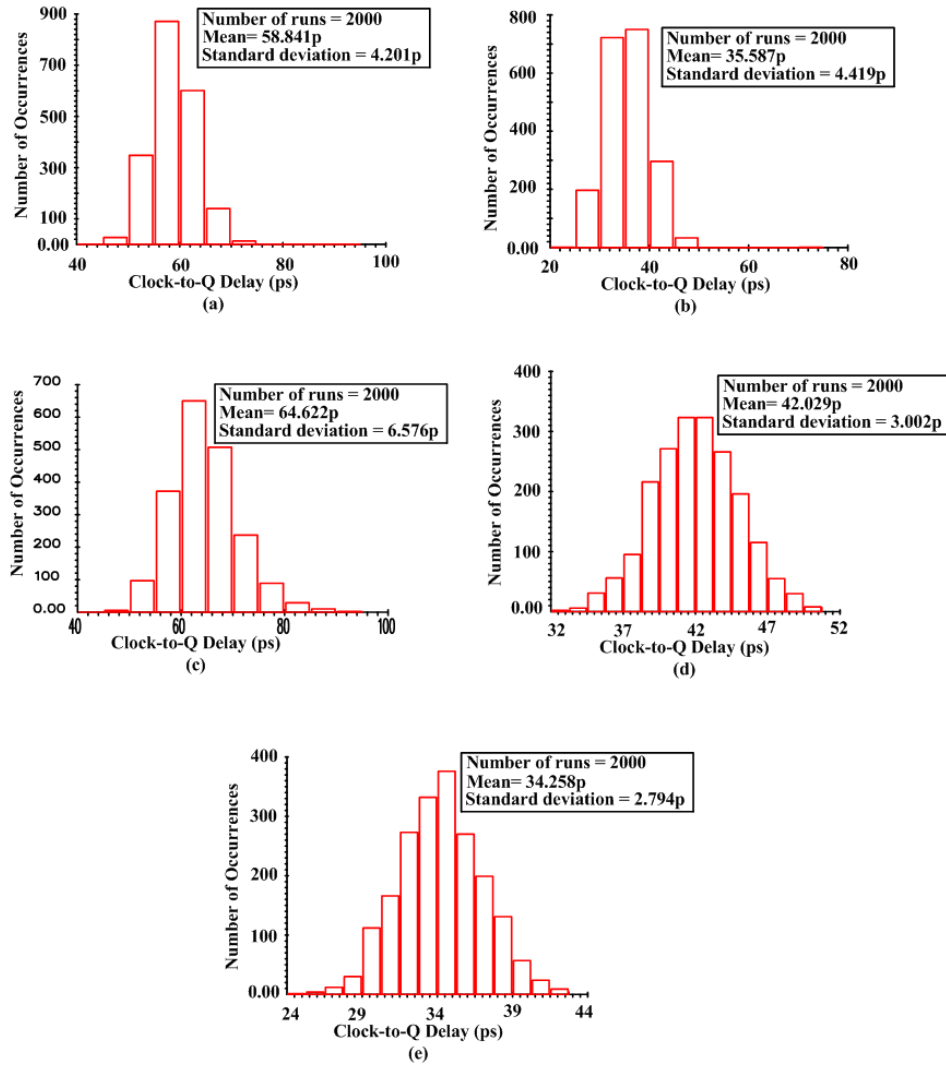
Figure 4.7: Monte-Carlo simulations of C-Q delay of the a) SCESH flip-flop, b) CPQ flip-flop, c) C2-DICE flip-flop, d) TSPCER flip-flop, and e) ATSPCER flip-flop.

Monte-Carlo runs under varying process and mismatch conditions at 27 ℃. Five minimum sized inverters were used as the flip-flop load and the operating frequency was 5 GHz. Then, the setup time (t_{su}) and the hold time (t_h) are determined. We define t_{su} as the point where t_{C-Q} is 20% higher than the nominal t_{C-Q}. Accordingly, we move the data transition edge closer to the clock rising edge until the C-Q delay reaches 1.2t_{C-Q}. Similarly, we measure the hold time of the flip-flop by moving the data edge closer to the

Table 4.4: Comparison of delay.

Types of flip-flop	C-Q Delay $t_{C\text{-}Q}$ (ps)	D-Q Delay $t_{D\text{-}Q}$ (ps)
MS DFF	32.0	48.7
MS DICE	73.3	85.3
Pulsed DICE	57.0	79.0
SCCER	41.3	49.3
TSPC DICE	55.0	72.0
CPSER	43.4	71.4
SCESH	59.0	24.0
CPQ	35.1	34.1
C^2-DICE	63.8	88.8
TSPCER	41.9	62.9
ATSPCER	34.0	31.5

clock edge from the opposite direction until the C-Q delay reaches $1.2t_{C\text{-}Q}$. The comparison of setup time and hold time for the flip-flops are shown in Table 4.3. Once $t_{C\text{-}Q}$ and t_{su} are known, the data to output delay ($t_{D\text{-}Q}$) is simply the summation of nominal $t_{C\text{-}Q}$ and t_{su}. The maximum $t_{D\text{-}Q}$ delay of the flip-flops is extracted for both low-to-high and high-to-low data transitions. Table 4.4 presents the maximum $t_{C\text{-}Q}$ and $t_{D\text{-}Q}$ of the flip-flops. Clearly, proposed flip-flops have much lower $t_{C\text{-}Q}$ and $t_{D\text{-}Q}$ delay than the competing flip-flops. The CPQ and ATSPCER flip-flops have comparable $t_{C\text{-}Q}$ delay to that of MS DFF. The CPSER has 24% lower $t_{C\text{-}Q}$ than that of pulsed DICE and ATSPCER flip-flops has 40% and 18% lower $t_{C\text{-}Q}$ than those of pulsed DICE and SCCER flip-flops, respectively. The TSPCER flip-flop has 43% and 26% lower $t_{C\text{-}Q}$ than those of MS DICE flip-flop and pulsed DICE flip-flop, respectively. The SCESH flip-flop has the lowest $t_{D\text{-}Q}$ delay when compared to all the competing flip-flops. It has 51% and 70% lower $t_{D\text{-}Q}$ delay when compared to SCCER and pulsed DICE flip-flop, respectively.

Due to the variation of rise-fall time of the sinusoidal clock signal, the C-Q delays of the energy recovery flip-flops are different at different frequency. However traditional
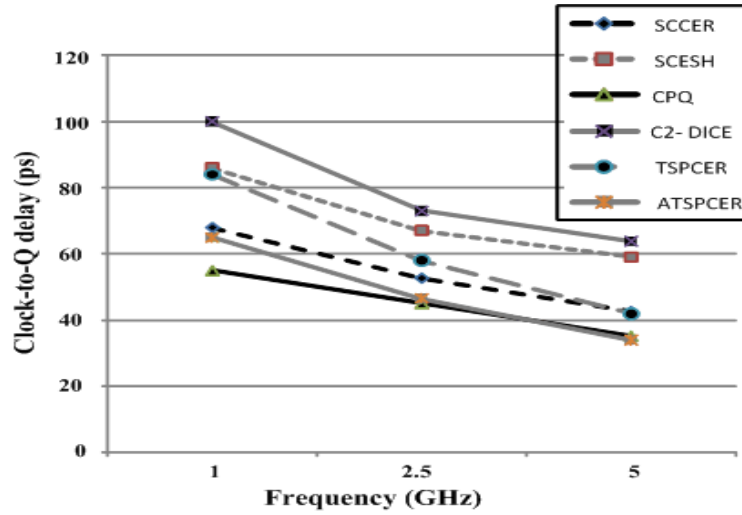
Figure 4.8: Delay versus frequency of proposed energy recovery flip-flops with reference to SCCER flip-flop.

square clock flip-flop has constant C-Q delay with the variation of frequency. The variation of C-Q delay of the proposed flip-flops in reference to high performance SCCER flip-flop is shows in Figure 4.8.

4.2.2. Power-Delay Product

Power-delay product (PDP) is a measure of performance for circuit components. In digital circuits, there is always a compromise between power and delay. If we try to reduce the delay of a specific circuit, we may need to increase the sizes of the MOSFETs. Thus, it increases the power consumption of that circuit. The lower PDP means that the power is better translated into speed of operation. In order to make the performance comparison of the proposed flip-flops with the competing flip-flops, I measured the PDP of each flip-flop. Figure 4.9 presents the power and t_{D-Q} delay product of the flip-flops at 25% data activity. It is evident that the PDP of the proposed CPQ flip-flop is much lower than that of DICE-based and energy recovery flip-flops, even its PDP is comparable to
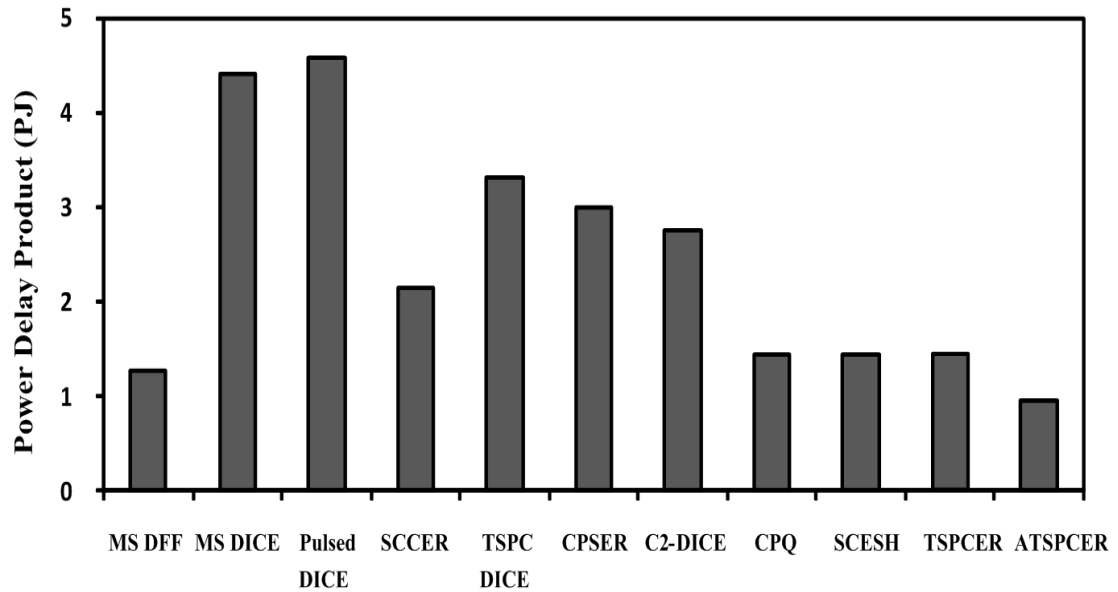
Figure 4.9: Power-delay (D-Q) product of different flip-flops at 25% data activity at 5 GHz.

MS DFF at this particular data activity. At 100% data activity, the proposed CPQ flip-flop exhibits 58% lower PDP than that of pulsed DICE and 42% lower PDP than that of SCCER flip-flop. At 25% data activity the proposed C^2-DICE flip-flop illustrates 40% lower PDP than that of pulsed DICE flip-flop and 38% lower PDP than that of MS DICE flip-flop. The CPSER flip-flop shows 34% and 35% lower PDP when compared to pulsed DICE flip-flop at 25% and 12.5% data switching activity, respectively. The proposed TSPCER flip-flop exhibits lower PDP compare to competing soft error robust and energy recovery flip-flops. At 12.5% data switching activity TSPCER demonstrates 69% lower PDP than that of pulsed DICE flip-flop and 30% lower PDP than that of SCCER flip-flop. The ATSPCER flip-flop has lower PDP than all the competing flip-flops from 100% to 0% data switching activity. The ATSPCER flip-flop exhibits 79% lower PDP than that of pulsed DICE flip-flop and 56% lower PDP than that of SCCER flip-flop, at 25% data
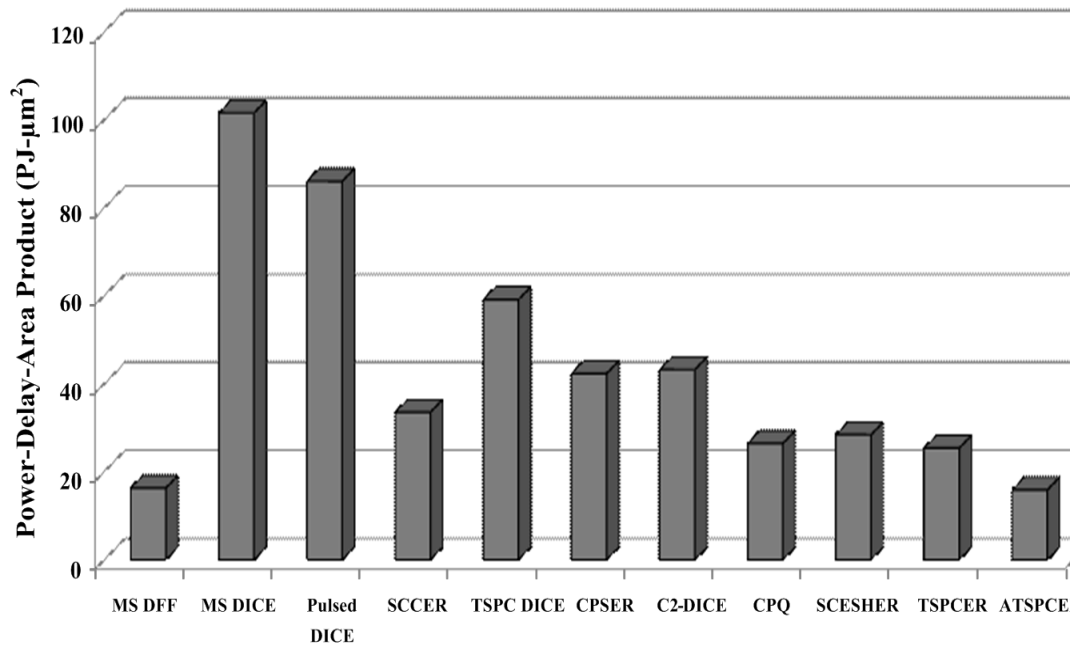
Figure 4.10: Power-delay-area product (PDAP) of different flip-flops at 25% data activity at 5 GHz.

switching activity. Thus, ATSPCER flip-flop is favourable than the competing flip-flops for all the applications independent of data switching activity. On the other hand, square clock flip-flop CPSER is attractive for low data switching activity applications.

4.2.3. Power-Delay-Area Product

In order to measure the overall performance of the flip-flops, the power-delay (t_{D-Q})-area product (PDAP) was also measured under the scope of this thesis. The PDAP has the unit of joule-μm^2. Figure 4.10 presents the PDAP of the proposed flip-flops comparing with the competing flip-flops at 25% data switching activity. The square clock flip-flop CPSH has 51% lower PDAP than that of pulsed DICE flip-flop and 57% lower PDAP than that of MS DICE flip-flop at this particular data switching activity. The
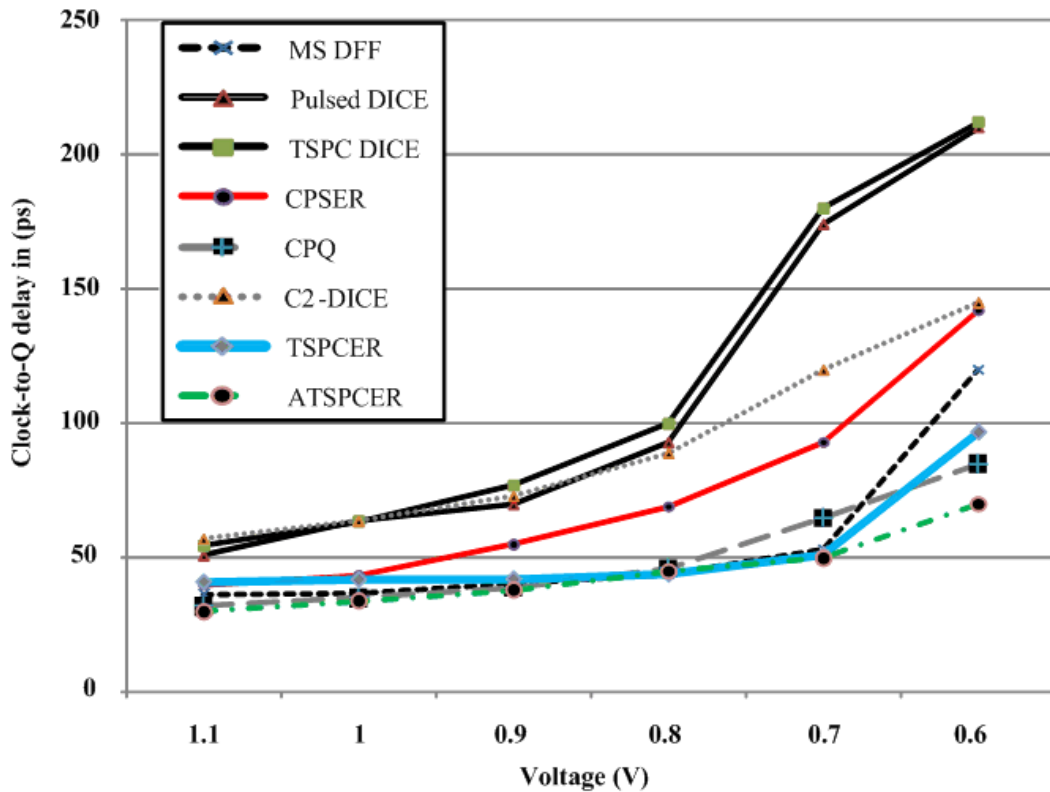
Figure 4.11: Effect of supply voltage variation on C-Q delay.

sinusoidal clock flip-flop ATSPCER has 82% and 53% lower PDAP than those of pulsed DICE and SCCER flip-flop, respectively.

4.3 Effect of Voltage and Temperature Variations

Systematic and random variations in process, supply voltage, and temperature (PVT) are posing a major challenge in the nanoscale CMOS technology. Since we already have presented the effects of process and mismatch variation in C-Q delay using Monte-Carlo simulation, in this section we will only consider the effects of voltage and temperature variation on proposed flip-flop.
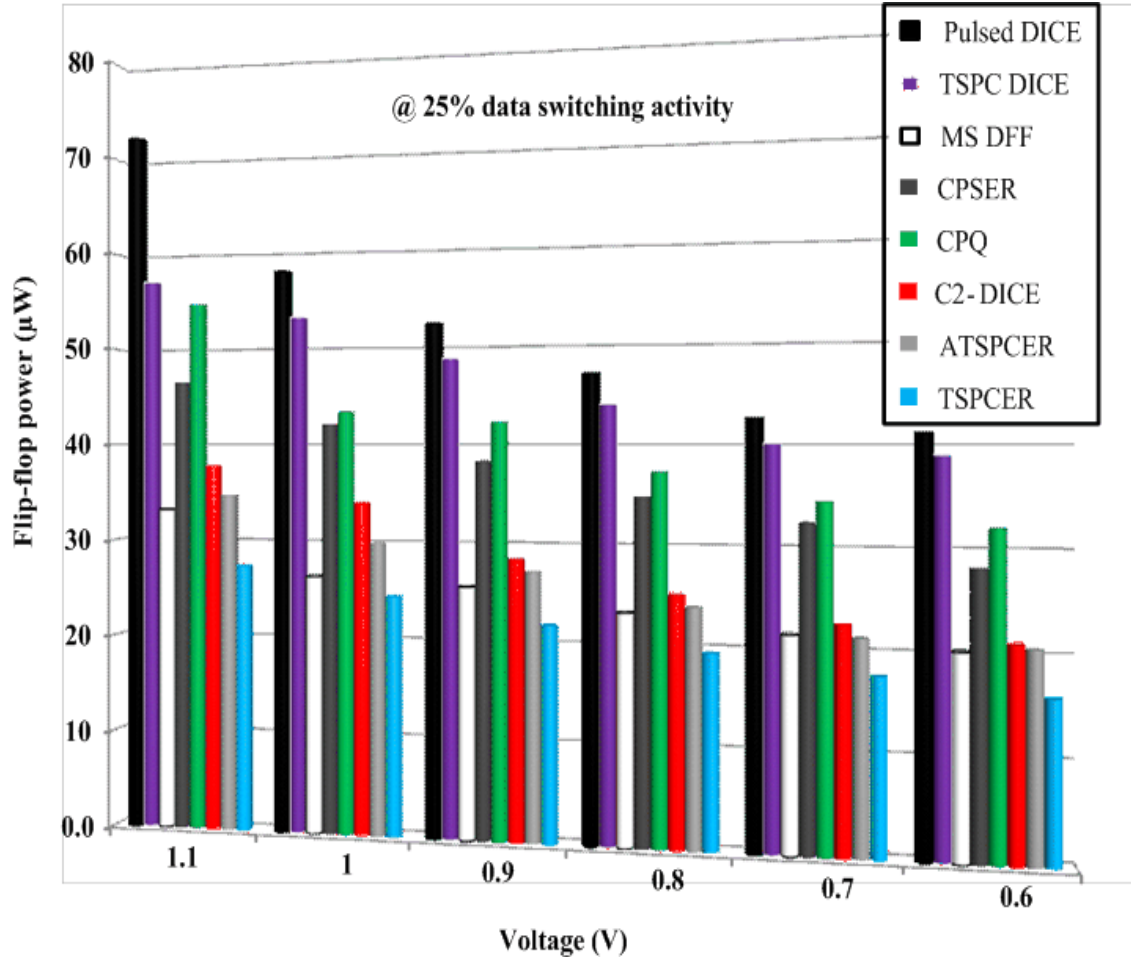
Figure 4.12: Effect of supply voltage variation on flip-flops total power at 5 GHz.

A. Voltage Variation

As mentioned earlier, scaling down the voltage is a common technique to reduce the power consumption. A wide range of voltage variation (from 1.1V to 0.6V) has been considered to present the effect of voltage variation on power consumption and on the C-Q delay of the flip-flops. Figure 4.11 presents the effect of voltage variation on $t_{C\text{-}Q}$ of the proposed flip-flops comparing with the competing flip-flops. Due to the large stack
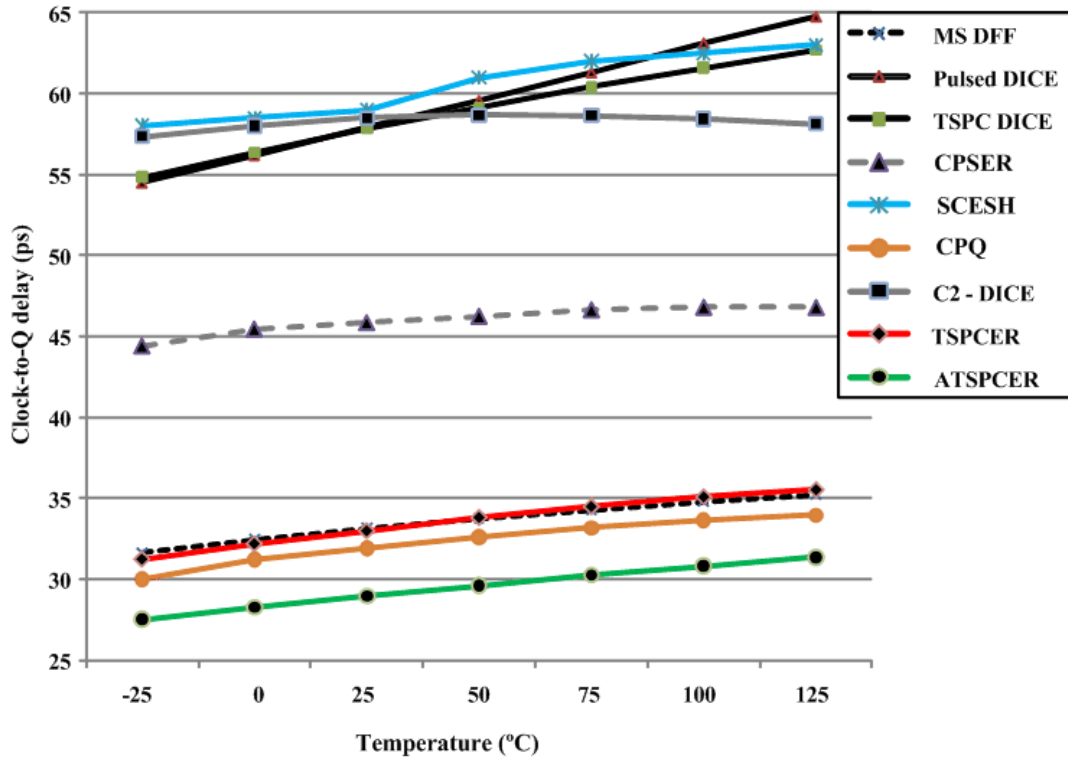
Figure 4.13: Temperature variation effect on Clock-to-Q delay.

MOSFETs of SCESH flip-flop, it cannot work below 0.7V for the current technology and requires special care on designing input section to work at low voltages. Thus, we eliminate SCESH flip-flop for this experiment. In addition, since MS DICE flip-flop incur significantly large area and delay penalties, I exclude it in this analysis. Results show that, proposed ATSPCER flip-flop has lowest C-Q delay variation compare to those of other competing flip-flops.

The total power consumption (P_{FFT}) of each flip-flop is measured using a wide range of voltage variation (from 1.1V to 0.6V). Figure 4.12 shows the effect of voltage variation on total power consumption of each flip-flop. Here, the values are based on 25% data activity, which is considered to be reasonable for typical applications. As evident from Figure 4.12, with the scaling of supply voltage, all the flip-flops power

55

consumption reduces at the expense of delay. At 0.6V supply, the proposed TSPCER flip-flop consumes 61% and 21% lower power when compared to pulsed DICE flip-flop and MS DFF, respectively.

B. Temperature Variation

A wide range of temperature variations from -25 ºC to 125 ºC in steps of 25 ºC was adopted here to investigate the temperature effect on the clock-to-Q delay of each flip-flop. Figure 4.13 presents the result of this experiment. Clearly, the flip-flops are working perfectly with the temperature variation with very small variation on C-Q delay. The Figure 4.13 shows that with increase of temperature the C-Q delay of all the flip-flops also increasing.

4.4 Soft Error Tolerance

The soft error tolerance of the proposed flip-flops is verified using SPICE simulation. As mentioned earlier the proposed flip-flops cannot detect and correct SETs at the data line. However the flip-flops are robust against particle induced SETs by using soft error robust storage cells (e.g., DICE, SERS and Quatro latch).

4.4.1. Single Node Charge Collection

In this thesis, I have presented soft error robust flip-flops based on three storage cells. It is necessary to verify the robustness of these cells (DICE, Quatro, and SERS) against soft errors.

Figure 4.14: Response of the proposed TSPC DICE flip-flop to a) an SET at a single node and b) simultaneous SETs at neighbouring nodes.

The soft error immunity of the proposed flip-flops is verified by injecting an exponential current pulse at a test node to mimic a particle-induced SET. Results show that all nodes (X_0, X_1, X_3, and X_4 of Figure 3.1) or (Y_0, Y_1, Y_3, and Y_4 of Figure 3.3) or (A, B, C, and D of Figure 3.6) are capable of recovering from (1-to-0) or (0-to-1) SETs. Figure 4.14(a) presents such recovery of a DICE based flip-flop (TSPC DICE) at node X_2 (0-to-1) and node X_3 (1-to-0) for SETs at two different time instant. As apparent, the data stored at the cell is unchanged and the output (Q) is not at all disturbed during each SET. The latter property of the flip-flop is very advantageous as it masks the SETs to propagate from the storage cell to the output, which may be driving the next stage in a pipeline network.
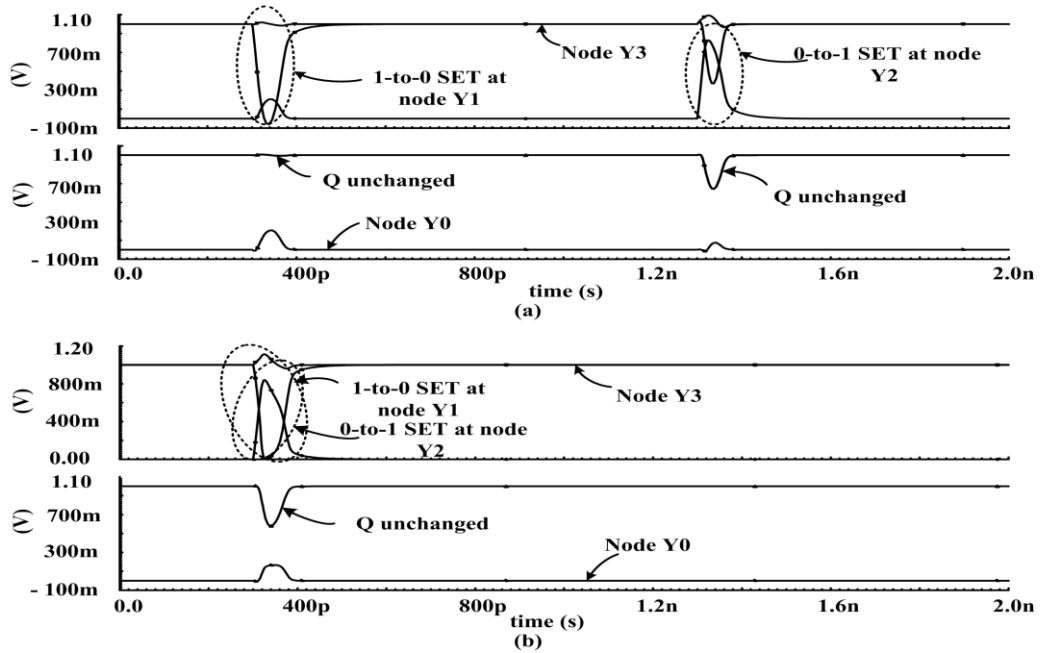
Figure 4.15: Response of the proposed CPSER flip-flop to a) an SET at a single node and b) simultaneous SETs at neighbouring nodes.

Figure 4.15(a) presents the soft error immunity of SERS cell based CPSER flip-flop at node Y_1 (1-to-0) SET and at node Y_2 (0-to-1) SET. It is evident that the storage data is unchanged for single node particle induced SET. The two-input output inverter can masks the propagation of any SET transient during the SET period, however a sufficiently large particle induced SET at node Y_0 or Y_2 can propagate to the output.

Figure 4.16(a) illustrates such recoveries of Quatro cell based SCESH flip-flop at node A and node B for SETs at two different time instants. The structure of Quatro latch provides a 0-to-1 SETs, nodes A and D are able to recover while node B or C has the potential to flip the Quatro latch for a sufficiently large 0-to-1 SET. However, the critical charge, i.e., the charge required to cause a flip for such a case is very large, meaning a
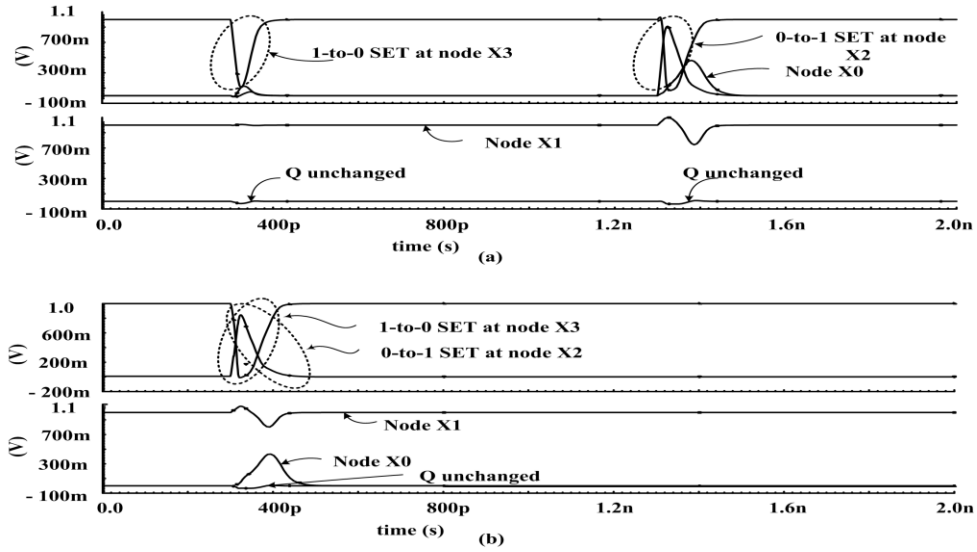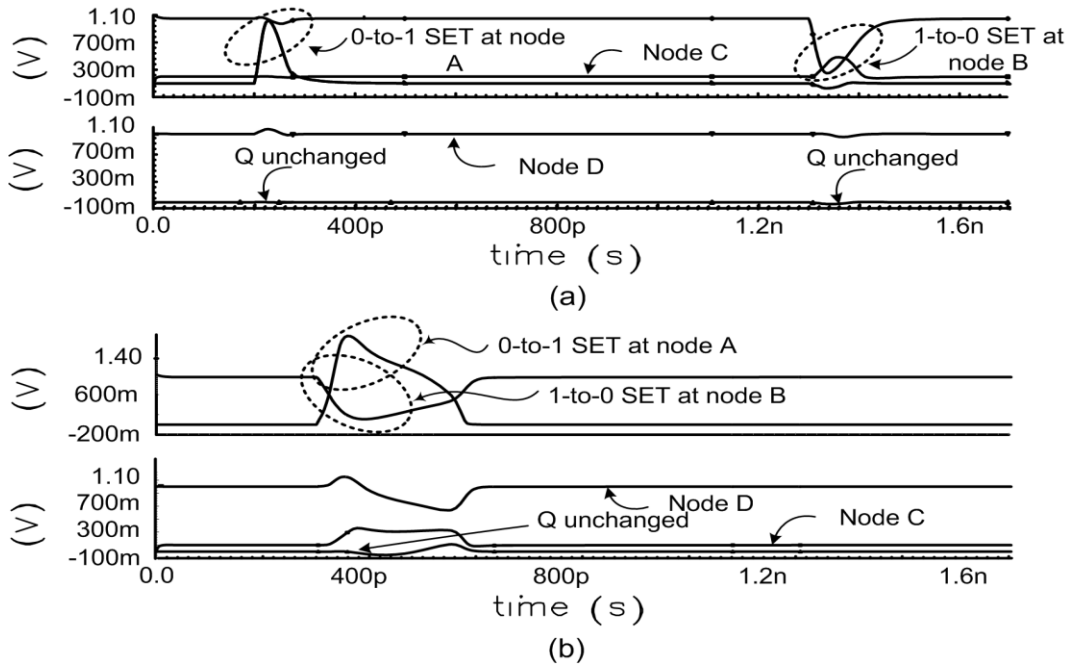
Figure 4.16: Response of the proposed SCESH flip-flop to a) an SET at a single node and b) simultaneous SETs at neighbouring nodes.

very high energy neutron is required to cause the upset [30]. Since the ground level neutron flux exponentially decreases with increasing energy, the upset probability is very low.

4.4.2. Multiple Node Charge Sharing

Following some promising results of the proposed flip-flops against single-node SET, I tested the robustness for multiple node SETs by injecting exponential current pulses at the two storage nodes of the flip-flops at the same time instant. This test is critical as sharing of collected charge among neighbouring nodes are increasing in nanoscale CMOS technologies where larger number of nodes are being closely packed. Figure 4.14(b), Figure 4.15(b), and Figure 4.16(b) are the evidences of the proposed flip-flops to be robust against double node SETs. Typically, the ground level radiation can

59
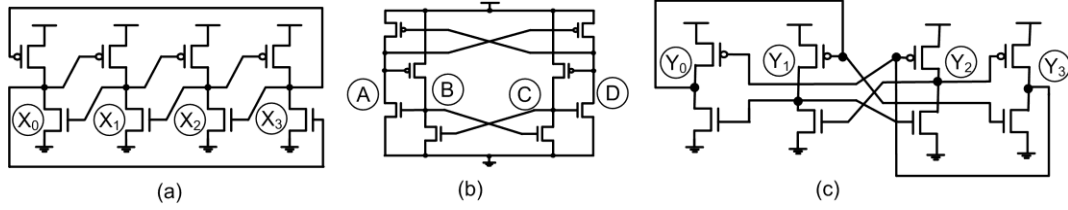
Figure 4.17: Soft error tolerant latches: a) DICE, b) Quatro and c) SERS.

Table 4.5: Critical charge of DICE, Quatro, and SERS latches for double node SET.

Stored data	SET affected node			Critical charge (fC)		
	DICE	Quatro	SERS	DICE	Quatro	SERS
(0,0)	X_0, X_2	A, C	Y_0, Y_2	5.73, 5.73	5.71, 5.71	5.74, 5.74
(1,1)	X_0, X_2	A, C	Y_0, Y_2	3.14, 3.14	3.15, 3.15	3.15, 3.15
(0,0)	X_1, X_3	B, D	Y_1, Y_3	5.73, 5.73	5.71, 5.71	5.7, 5.7
(1,1)	X_1, X_3	B, D	Y_1, Y_3	3.14, 3.14	3.15, 3.15	3.14, 3.14
(1,0)	X_2, X_3	C,D	Y_2, Y_3	No flip	No flip	No flip
(0,1)	X_2, X_3	C,D	Y_2, Y_3	2.22, 2.22	3.96, 3.96	3.33, 3.33
(1,0)	X_1, X_2	B,C	Y_1, Y_2	No flip	2.64, 2.64	No flip
(0,1)	X_1, X_2	B,C	Y_1, Y_2	2.22, 2.22	2.64, 2.64	2.61, 2.61

deposit charge in silicon within a few microns around the point of strike. As a result, two neighbouring nodes of the Quatro or DICE latch or SERS can potentially share the deposited charge and work in tandem to upset the stored logic value. Sheshadri and colleagues presented a technique to identifying the critical nodes in DICE latch depending on the driving transistors connected to those nodes and the structure of DICE latch [32]. The basic idea behind that is the charge sharing between similar potential nodes to cause upset in DICE latch. In order to mimic the charge sharing scenario, I simultaneously injected current at two nodes of the DICE, Quatro, and SERS latches (see Figure 4.17) and determined the injected charge that causes an upset. Table 4.5 lists the critical charge thus obtained for a variety of node combinations. Clearly, for charge sharing among two similar logic storing nodes (e.g., X_0 and X_2 or X_1 and X_3 in DICE, A

and C or B and D in Quatro latch, and Y_0 and Y_2 or Y_1 and Y_3 in SERS), the storage latches have similar sensitivity to an SET. In case of two opposite logic storing nodes (e.g., X_2 and X_3 or X_1 and X_2 in DICE, C and D or B and C in Quatro latch, and Y_2 and Y_3 or Y_1 and Y_2 in SERS), the Quatro and SERS latch has higher critical charge compared to DICE which implies a lower SER. Moreover the latter two cases, where in each condition Quatro latch has critical chare suggest that we can differentially write data into a Quatro latch. While this characteristics is absent in DICE and SERS latch (see Table 4.5), makes DICE and SERS latch more attractive than Quatro latch in terms of SER depending on the opposite node charge sharing.

4.5 Power Consumption with Clock Tree

Energy recovery clocking is demonstrated by integrating 1024 proposed soft error robust energy recovery flip-flops distributed across an area of 1mm × 1mm and clocked them by a single-phase sinusoidal clock through an H-tree clocking network. The area was chosen by evenly grouping the proposed flip-flops into registers of 16 flip-flops. In order to easily control the data switching activity, a common data input is used for all the flip-flops. Figure 4.18(a) shows the layout geometry of the clock distribution in a square shaped balanced H-tree. In order to reduce capacitance, metal-5 layer is used, which has the lowest parasitic capacitance to the substrate. Table 4.6 presents a detailed description of the wire lengths and widths of the clock distribution in a square shaped balanced H-tree as shown in Figure 4.18.
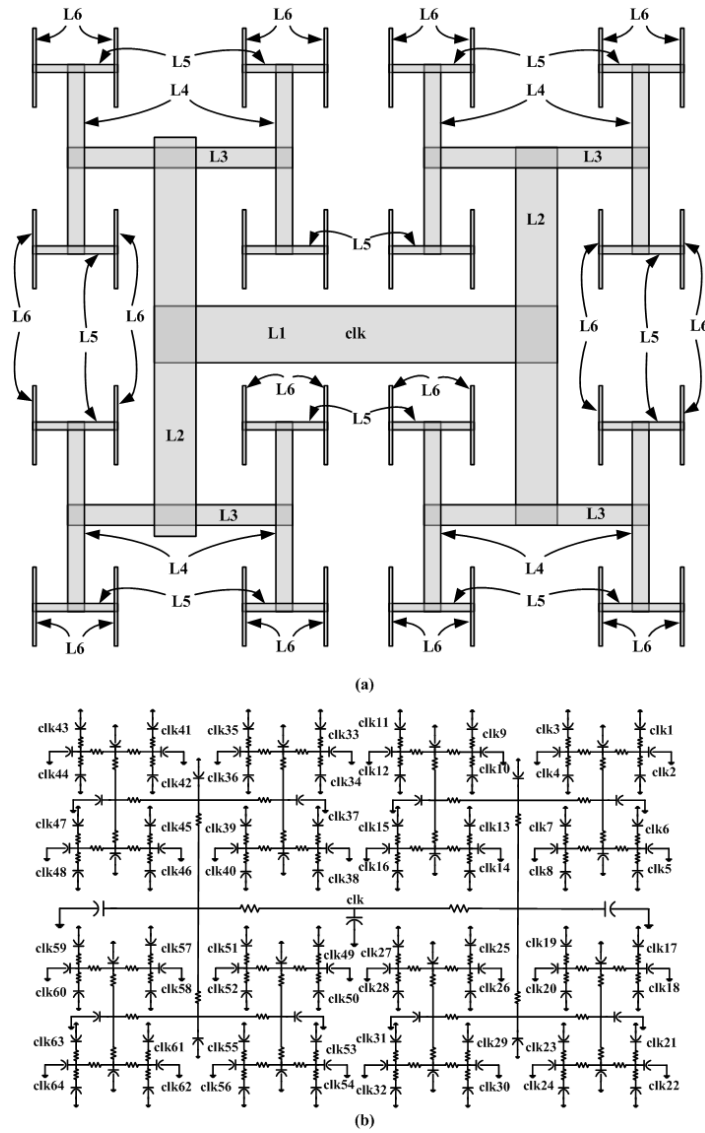
Figure 4.18: a) H-tree structure and b) Distributed resistance-capacitance (RC) model
of clock-tree.

Technology parameters are used to estimate the capacitance and resistance of each

wire. A lumped 3-segment π-type resistance-capacitance (RC) model was used for each

wire of the clock-tree and then connected together to make a distributed RC model of the

clock tree [33]. The energy recovery clock generator (see Figure 3.5(b)) drives the source

node of the clock-tree (node clk in Figure 4.18), and each final node of the clock-tree

clk1 to clk64 is connected to the 16-bit registers. Figure 4.19 shows the simulation

Table 4.6: H-tree parameters.

Wire name	No. of wire	Width (μm)	Length (μm)
L1	1	12.8	560
L2	2	6.4	560
L3	4	3.2	280
L4	8	1.6	280
L5	16	0.8	140
L6	32	0.4	140
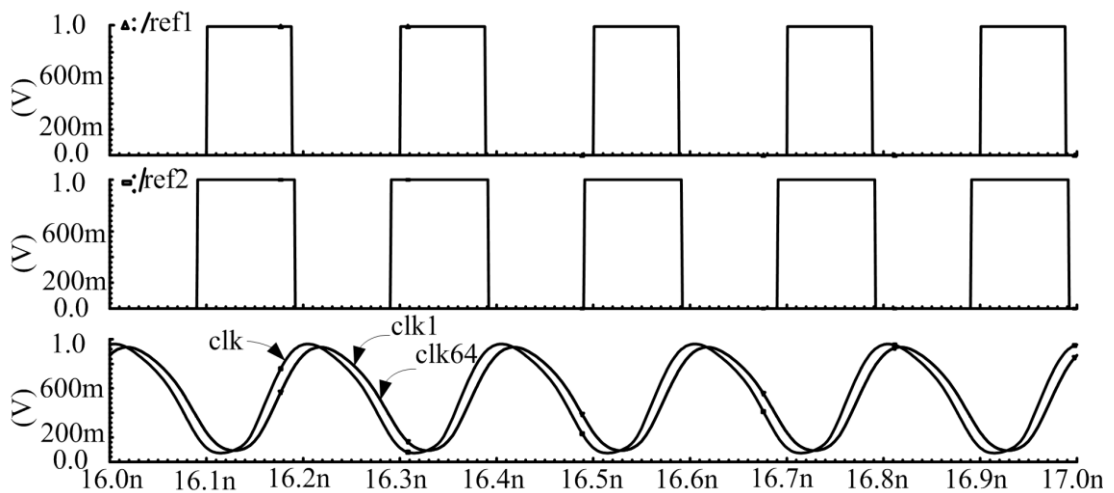
Figure 4.19: Simulation waveforms of generated energy recovery clock signal with 1024 flip-flops as clock load.

waveforms of the resonant clock generator with 1024 flip-flops as clock distribution network load.

In order to compare with the square wave clocking, I distributed two square wave flip-flops in the same area and clocked them through a square wave signal (see Figure 3.5(a)). Since proposed flip-flops are soft-error robust, I chose one recently proposed DICE based flip-flops (Pulsed DICE [12]) with a conventional master-slave D flip-flop as the reference. A chain of progressively sized inverter used for square wave clocking. A total number of 84 inverters were used within the square-wave clock distribution
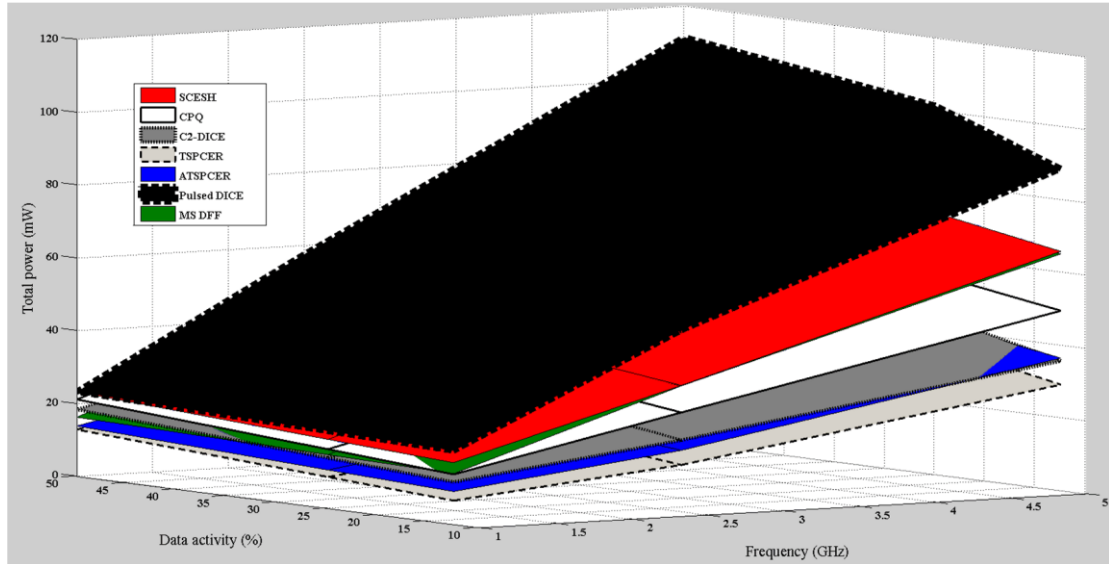
Figure 4.20: Total power versus data switching activity versus frequency.

network. The whole system of clock buffers, clock H-tree, and flip-flops was simulated under frequencies ranging from 5GHz to 1 GHz at different data switching activities. Figure 4.20 depicts the result of this experiment. The system power is plotted versus data switching activity and frequency for the systems with different flip-flops. Among all the flip-flops, the proposed flip-flop systems show lower power consumption for all data switching activities and frequencies. Among all the flip-flop system, the pulsed DICE system consumed highest power at all the data switching activity and frequency. The proposed SCESH flip-flop consumed highest power and proposed TSPCER flip-flop consumed lowest power when compared to other proposed soft error robust energy recovery flip-flops. The SCESH flip-flop system consumed comparable power to that of MS DFF while CPQ flip-flop system, C^2-DICE flip-flop system, TSPCER flip-flop system, and ATSPCER flip-flop system consumed much lower power than those of the competing square clock flip-flops.

Table 4.7: Power consumption comparison of different flip-flop system at different frequency and data switching activity in mW.

Types of flip-flop	Frequency (GHz)	CDN Power	50% data activity		25% data activity		12.5% data activity	
			Flip-flops power	Total power	Flip-flops power	Total power	Flip-flops power	Total power
MS DFF	5	42.10	35.10	77.2	27.0	69.10	22.9	65.0
Pulsed DICE		42.10	69.20	111.3	59.2	101.3	46.3	88.4
SCESH		10.80	74.10	84.9	61.1	71.90	54.9	65.7
CPQ		11.95	57.65	69.6	43.0	54.95	37.4	49.4
C^2-DICE		12.20	48.10	60.3	31.7	43.90	23.4	35.6
ATSPCER		11.80	42.90	54.7	30.6	42.40	24.6	36.4
TSPCER		11.00	39.00	50.0	25.1	36.10	18.1	29.1
MS DFF	2.5	22.75	17.7	40.5	13.9	36.7	11.8	34.6
Pulsed DICE		22.75	34.8	57.6	29.7	52.5	27.1	49.9
SCESH		3.70	44.0	47.7	35.4	39.1	31.0	34.7
CPQ		3.14	38.8	41.9	28.7	31.8	24.2	27.3
C^2-DICE		3.01	31.0	34.0	21.7	24.7	16.7	19.7
ATSPCER		3.08	42.2	27.3	17.3	20.4	13.8	16.9
TSPCER		2.80	21.8	24.6	14.0	16.8	10.1	12.9
MS DFF	1	9.20	7.1	16.3	5.60	14.8	4.80	14.0
Pulsed DICE		9.20	14.1	23.3	12.1	21.3	11.1	20.3
SCESH		1.10	22.0	23.3	17.9	19.0	15.9	17.0
CPQ		1.00	20.2	21.2	15.3	16.3	12.8	13.8
C^2-DICE		0.67	17.7	18.4	12.9	13.6	11.1	11.8
ATSPCER		0.90	13.0	13.9	9.70	10.6	8.20	9.10
TSPCER		0.65	12.1	12.8	7.90	8.60	5.80	6.50

Table 4.7 shows the power breakdown of the systems with different flip-flops at different data switching activity and at 5GHz, 2.5GHz, and 1GHz clock frequency. The total power is broken down into two components: clock distribution network (CDN) power including clock generator power and flip-flops power. A careful observation of the Table 4.7 reflects that the rate of power reduction of proposed C^2-DICE, TSPCER, and ATSPCER flip-flops is much higher than that of existing and other proposed flip-flops with reduction of the data switching activity.
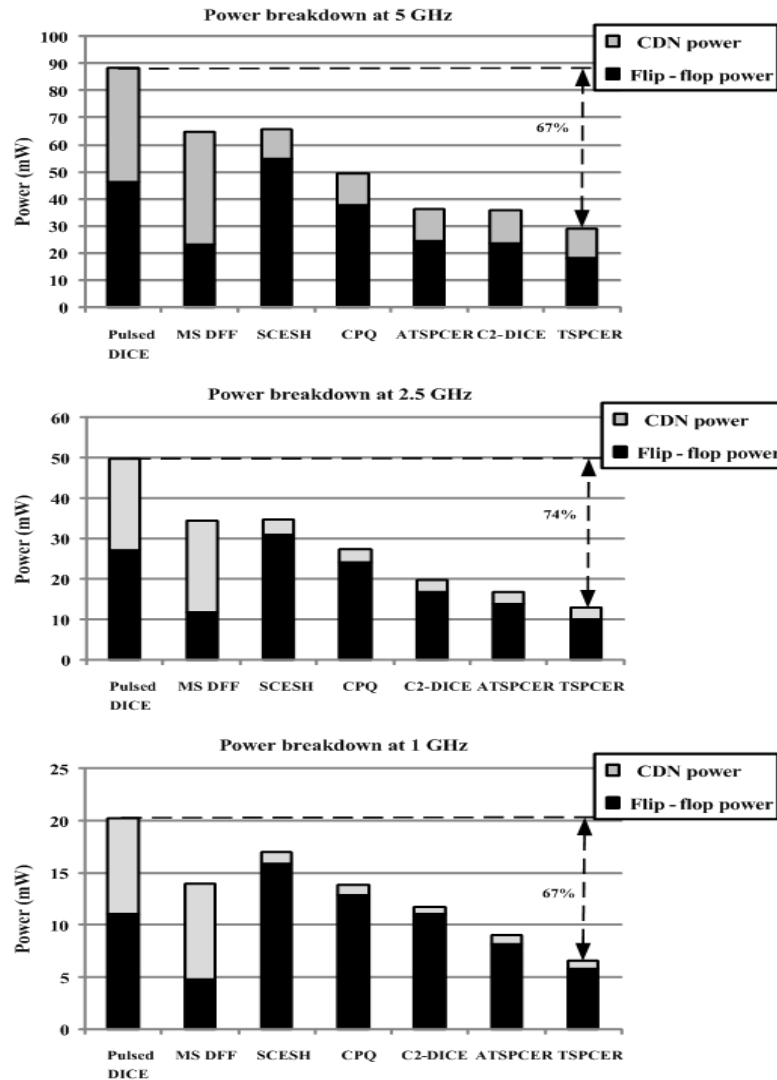
Figure 4.21: Power breakdown at 12.5% data switching activity.

In comparison to pulsed DICE system, the C^2- DICE system shows power saving of 47% at 50% data switching activity and the TSPCER system exhibits 56% power saving at this particular data switching activity and at clock frequency of 5 GHz. Moreover at 25% and 12.5% data switching activity the proposed C^2-DICE system demonstrates 57% and 60% power saving when compared to Pulsed DICE system, respectively. At 5 GHz clock frequency TSPCER system shows 67% power saving compare to that of Pulsed DICE system (see Figure 4.21), at 12.5% data switching activity. At 2.5GHz clock

frequency the CPQ flip-flop system and TSPCER system shows 27% and 57% power saving as compared to that of pulsed DICE system at 50% data switching activity, respectively (see Table 4.7). The TSPCER system exhibits 63% and 74% power saving when compared to those of MS DFF system and pulsed DICE system, respectively at 2.5 GHz clock frequency and 12.5 % data switching activity (see Figure 4.21). As compared to Pulsed DICE system, the C^2-DICE system shows power saving of 53% and 61% at 25% and 12.5% data switching activity, respectively at 2.5 GHz clock frequency (see Table 4.7). When compared to pulsed DICE system at 1GHz clock frequency, the proposed ATSPCER system exhibits as much as 55% power saving at 12.5% data switching activity and TSPCER system shows 67% power saving, at this particular data switching activity (see Figure 4.21).

Chapter 5 Conclusion

5.1 Contribution to the Field

Soft error tolerance of microprocessors or SOCs in current sub-45nm technologies is very critical. However, the soft error resilience need to be achieved without adversely affecting the other design parameters such as power, performance (e.g., delay), and area or cost.

This thesis has presented seven high performance soft error robust flip-flops and precisely measured the performance of each flip-flop. The flip-flops were designed and implemented based on circuit techniques to achieve a low power with the minimum performance degradation. Comparison was made between the designed and recently reported high performance flip-flops in terms of their area, power, delay, and soft error tolerance. The soft error tolerance was investigated based on the multiple-node charge sharing, which is a growing concern in nanoscale technologies. The proposed flip-flops exhibit excellent power-delay performance and soft error robustness compared to existing soft error robust flip-flops and energy recovery flip-flops. To the best of my knowledge, this thesis is the first report on the soft error robust energy recovery flip-flops. As the energy recovery resonant clocking significantly saves the clock power, which can be as much as 40% of the total power of a high performance chip, the proposed flip-flops will enable reducing the total power consumption while achieving the soft error robustness. In fact, based on the power and performance of the proposed flip-flops, the flip-flops can provide i) soft error immunity and low performance and power penalty in high-end microprocessors where performance and reliability are the main figures of merit, ii) soft

error immunity to power constrained, mission-critical SOCs, and iii) soft error immunity to ultra low-power implantable medical devices like the implantable cardioverter-defibrillator (ICD).

5.2 Future Work

The proposed flip-flops were tested and compared based on schematic design and post-layout simulations only. So, the first step as the future work would be to implement the proposed flip-flops in a test chip and get a more accurate estimation of their performance. Given the test chip fabrication schedule of Canadian microelectronics corporation (CMC) and the time limitations of my degree program, I have not been able to design and tape out a test chip. However, doing the layout and post-layout simulations constitute the major part of a test chip design and I have of completed that part in this thesis.

Other than test chip implementation, a number of techniques can be adopted to enhance the applicability and reliability of the proposed flip-flops and devise new flip-flops with competing capabilities. For example, a new architecture can be considered for the flip-flops to reduce internal switching activity at test mode. A built-in self-test methodology can be adopted for the TSPC architecture, which offers the possibility to test the chip internally without going through the input-output ports [34].

Clock gating technique is an attractive technique for low power applications to reduce the power consumption in the standby mode. Clock gating technique can be adopted to develop modified architectures of the flip-flops. Then the power consumption of the whole network with and without clock gating technique can be measured with area

and performance overhead. In addition, the complexities of clock gating signal routing in the clock distribution network for resonant clocking scheme can be measured.

Dual edge triggered flip-flops, where data are latched at both rising and falling edges of the clock, are often very useful for some applications to double the data rate without increasing the clock frequency. This enables low power operation while having a very high data rate. Accordingly, dual edge triggered soft error robust flip-flop can be a very interesting topic to be explored.

The proposed flip-flops are based on storage cells which are robust against single node SET and exhibits excellent soft error immunity for single node SET. However, the affected area of ground level radiation SETs is large enough to share charge at two neighbouring nodes resulting data upset at the storage cell. A soft error robust storage cell with double node SET protection can be a future work to be conducted.

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List of Abbreviations

ATSPCER: Alternate true single phase clock energy recovery

BPSG: Borophosphosilicate glass

C^2MOS: Clocked CMOS

CDN: Clock distribution network

CMC: Canadian microelectronics corporation

CMOS: Complementary metal-oxide-semiconductor

CPQ: Conditional pass Quatro

CPSER: Clocked precharge soft error robust

DICE: Dual interlocked cell

DRAM: Dynamic random access memory

ECC: Error correction codes

EHP: Electron-hole pairs

FPTG: Four-phase transmission-gate

HBD: Hardening by design

ICD: Cardioverter-defibrillator

LET: Linear energy transfer

MS DFF: Master-slave D flip-flop

NBTI: Negative bias temperature instability

PDP: Power-delay product

PDAP: Power-delay-area product

PVT: Process-voltage-temperature

RC: Resistance-capacitance

SAER: Sense amplifier energy recovery

SCCER: Single-ended conditional capturing energy recovery

SCESH: Soft clock edge SEU hardened

SDER: Static differential energy recovery

SER: Soft error rate

SERS: Soft error robust storage

SET: Single event transient

SEU: Single event upset

SOC: System-on-chip

SRAM: Static random access memory

TGFF: Transmission-gate flip-flop

TMR: Triple modular redundancy

TSPC: True single phase clock

TSPCER: True single phase clock energy recovery