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Design and modeling of a completely CMOS Compatible RF Varactor and a MUMPs Varactor

Hong Qu

A Thesis
In
The Department
Of
Electrical and Computer Engineering

Presented in Partial Fulfillment of the Requirements for the Degree of
Master of Applied Science at Concordia University
Montreal, Quebec, Canada

March 2005

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Abstract

Design and modeling of a completely CMOS Compatible RF Varactor and a MUMPs Varactor

Hong Qu

Micro electro mechanical system (MEMS) technology has shown its bright future in many different fields, especially in space and radio frequency (RF) systems. In wireless communication systems, passive elements including tunable capacitors and inductors often need a high quality factor and high self-resonant frequency. High-quality tunable capacitors and inductors can lead to improved power or figure of merit in low noise amplifiers, low insertion loss in band-pass filters, and better phase noise and power in voltage-controlled oscillators (VCOs).

By using MEMS technology, we can greatly shrink the cost and the footprint of RF circuits since all the off-chip components such as inductors and capacitors can be fabricated and integrated into a whole single chip at one time. Our research is directed by the purpose of developing more powerful RF components.

The goal of this project is to build a completely on-chip IC-compatible, high-Q variable capacitor using vertical electro-thermal actuators. The variable capacitor has been accomplished through building an all-Polysilicon microstructure. The fabrication procedure is fully compatible with a standard IC integration. The research results presented at the figure1 shows an SEM of the top-view of a fabricated capacitor with a nominal capacitance value of 1900 fF.

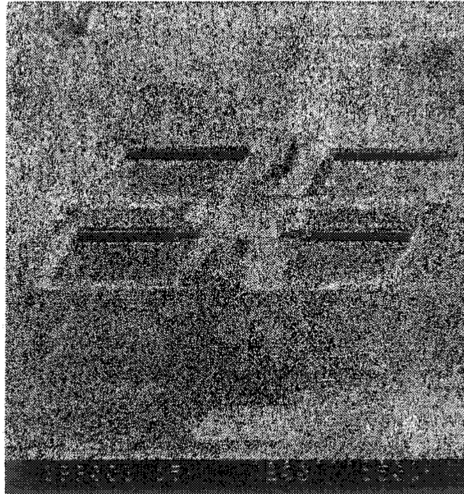

Figure1: Varactor

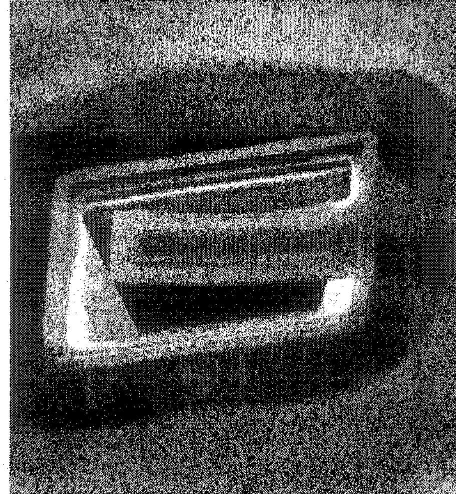

Figure2: Beam

The device consists of a thin polysilicon plate (90 um x 90 um) suspended in air nominally 0.037um above a bottom polysilicon layer by two mechanical springs. Figure2 shows the suspended beam. The high quality factor (Q) of the capacitor even at high frequencies, a key parameter to meet low phase noise requirements of high-performance communication systems, such as cellular telephony.

ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to my thesis supervisor, Dr. Mojtaba Kahrizi, for his continued help, guidance and encouragement during the course of this work. The hours of discussion and consultation with him had been the best times during my studies in Concordia University.

My sincere thanks go to Siamak Fouladi. I can not make this without his help at the beginning stages of this work.

I am grateful for the support of Jun Chen during the post processing of my device. Thanks for his good advice in many details; this saves me a lot of time and energy.

I express my thanks to Neal Lemaire, Vito Loguidice in Mcgill nanolab and Mr.Shailesh Prasad who helped me in the material and instructions in the device postprocessing.

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Chapter 1

Background

1.1 Introduction to MEMS

With the advent of integrated circuit (IC) fabrication technology in the 1960s, human being's ability to make physically small objects received a big progress. Since the circuits still perform the same function when they are scaled down by factors, competition occurred to develop ways of integrating more and more circuits on a semiconductor wafer. From the economic side, that is beneficial since the greater the number of circuits, the greater the profits. Such an exemplary success in mass production as appeared in IC industry has been achieved, and researchers are motivated to apply the concepts of integrated electronics manufacturing to mechanics, optics and fluidics with the hope of acquiring the same improvements in performance and cost effectiveness experienced by the semiconductor industry.

That resulted in the advent of MEMS technologies. MEMs is the acronym for MicroElectroMechanical Systems. In Europe, it is also called Microsystems.

By now, there is still no generally accepted definition for MEMS. Some researchers depict it as the integration of miniaturized sensors, actuators and signal processing units, enabling the whole system to sense, decide and react [1]. Other MEMS engineers consider a typical MEMS device as follows:

• A device that consists of a micro machine and microelectronics, where the micro machines are controlled by microelectronics. Quite often, micro

sensors are involved in the control system by providing signals to the microelectronics.

• A device that is fabricated using micromaching technology and an integrated circuit (IC) process, i.e., technologies of batch fabrication.

• A device that is integratedly born, without individual assembly steps for the main parts of the device except for the steps required for packaging.

More generally speaking, MEMS is simultaneously a toolbox, a physical product and a methodology all in one [2]. As the name implies, "Micro" establishes the size definition, "Electro" intimates that either electricity or electronics is involved or "mechanical" infers that some moving parts should be included. From the physical point view, MEMS is usually the integration of mechanical elements and electronics on a common silicon wafer using micro fabrication technologies. The electronics can be fabricated by IC process sequence (e.g., CMOS) and the mechanical elements are constructed by micromachining methods that are compatible with the IC fabrication process. Figure 1.1 depicts MEMS characteristics. The sensors

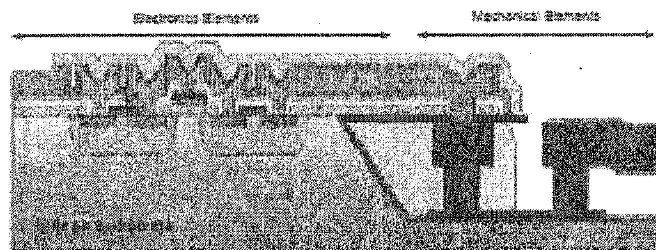


Figure 1.1: The schematic view of MEMS chip [31]

And Electronics Elements Mechanical Elements actuators can be made of mechanical elements, and signal processing and control units can be built by using electronics circuits. So, the whole system can be integrated on a single chip without any extra assembly process.

The motivation for integrating the whole system on a single chip is miniaturization and parallel processing which leads to inexpensive fabrication in large quantities. It also has the ability to make devices with the functions that cannot be realized with traditional technologies.

In the beginning of 1990s, MEMS emerged with the development of IC fabrication processes, in which sensors, actuators and control functions are fabricated on the same silicon chip [3]. With the strong financial support from both governments and industries, MEMS research has achieved remarkable progress. MEMS technology has proven its outstanding and revolutionary capability in many different fields. There are numerous MEMS applications that have been commercialized such as micro accelerometers, micro sensors, inkjet printer head, micro mirrors for projection, etc.

In addition to these less-integrated MEMS devices, more complicated MEMS applications also have been proposed and demonstrated for their concepts and possibilities in such varied fields as biomedical, chemical analysis, micro fluidics, data storage, display, optics wireless communications etc[4]. With more and more energy and effort injected, some new branches of MEMS technologies have appeared such as microoptoelectromechanical systems (MOEMS) and micro total analysis systems (μTAS) because of their potential applications' market. MEMS technologies do face a lot of challenges.

First of all, from the design point view, MEMS computer aided design (CAD) software packages are still very time consuming and not powerful enough to include all the real factors that affect the operation of MEMS devices at one time. The complexity of MEMS design is also a big issue for MEMS designers. Typical MEMS devices, even simple ones, manipulate

energy in several physics domains. That requires that the MEMS designer must understand and find ways to control complex interactions between these domains. Secondly, in the fabrication side view, the cost issue for a state-of-the-art silicon foundry is also a barrier most MEMS designers have to face. High initial investment limits the speed of the MEMS development. Packaging can also affect the performance of MEMS devices and becomes one of the most fundamental problems in MEMS research. Due to the diversity of MEMS devices, each new MEMS device almost needs a totally new and particular packaging method.

1.2 Micromaching Technique

The motivation for micromachining MEMS devices is the same as for integrated circuits: micro fabrication allows miniaturization and parallel processing which leads to inexpensive fabrication in large quantities. This can be used to make cheap products, large arrays, integrated systems and devices with the functions that cannot be realized with traditional technologies.

Micromachining is the set of design and fabrication tools that precisely machine and form structures and elements at a scale well below the limits of human perceptive capability the micro scale. Micromachining is the underlying foundation of MEMS fabrication, and a key factor for MEMS processes. In general, micromachining is such a process that selectively etches away parts of the silicon wafer or adds new structural layers to form the mechanical and electromechanical devices.

The well-established integrated circuit (IC) industry played an important role in fostering an environment suitable for the development and growth of

micromachining technologies. Many tools and processes used in the design and micromachining of MEMS products are borrowed from the IC technology.

Bulk and surface micromachining are two basic and major micro-machining techniques. Wafer bonding can be used as the post process of bulk micromachining. LIGA has been used in high-aspect ratio applications. In some special applications, the substrate is required to have some particular properties which silicon does not have. The flip chip technique is applied to solve this problem. The goal of this section is to briefly introduce these basic micromachining techniques.

1.2.1 Bulk micromachining

The bulk micromachining technique is one of the most popular micromachining techniques. The term bulk micromachining comes from the fact that this type of micromachining is used to realize micromechanical structures within the bulk of a single crystal silicon wafer by selectively Removing ('etching') wafer material. Bulk micromachining allows selective removal of significant amounts of silicon from a substrate to form three dimensional mechanical structures such as membranes, trench holes and so on (Figure 1.2).

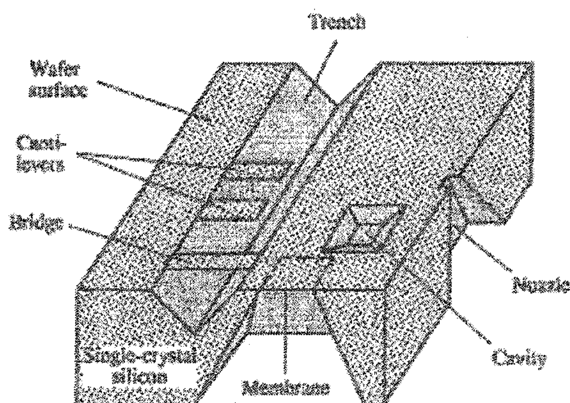


Figure 1.2: Various Bulk-micromachining Structures [30]

The crystal orientation of the wafer plays a decisive role. Different etchants such as solutions of potassium hydroxide (KOH), TMAH have different etching rates in different crystal orientations of silicon [5]. A high aspect ratio can also be reached for micromechanical components that can be formed directly from the silicon wafer.

Although bulk micromachining is a mature technique, it has some fundamental limitations. For instance, the wafer's crystallographic planes determine the maximum obtainable aspect ratios. The higher aspect ratios can requires larger sizes as compared with other micromachining techniques. Also, it is difficult to get complex structures from bulk micromachining. One Approach to solve this problem is the wafer bonding technique.

1.2.2 Surface micromachining

Unlike bulk micromachining, surface micromachining does not remove material from the bulk silicon, but constructs structures on the surface of the silicon wafer by adding ("depositing") thin films. A thin film is deposited wherever either an open area or a free-standing mechanical structure is desired, is called a sacrificial layer. The thin film, out of which the free-standing structure is made, is called the structure layer. Finally the given mechanical structure is defined through removing the sacrificial layer and releasing the structure layer (Figure 1.3).

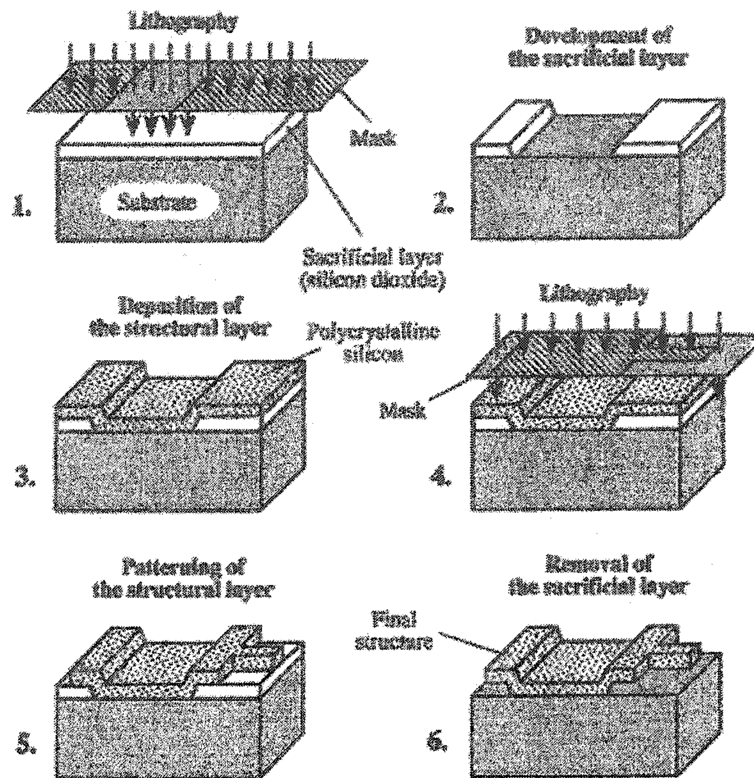


Figure 1.3: Processing steps of typical surface micromachining. [30]

Surface micromachining requires a compatible set of structural materials, sacrificial materials and chemical ethants. First of all, these materials have to be suitable for the application. Then, for the structure materials, they must have good mechanical properties such as high yield and fracture stress, minimal creep and fatigue, also good wear resistance. The sacrificial materials also need good mechanical properties in order to prevent the devices from the fabrication process. The etchants have to have excellent etch selectivity, which means they have to etch the sacrificial materials quickly without affecting the structure materials.

The dimensions of surface micro machined structures can be several orders of magnitude smaller than bulk micro machined structures. The surface micro machined devices are also very easy to integrate in IC circuits since the

IC circuits are also made of the silicon wafer. As its name implies, surface micro machined devices are usually planar structures. The assembly Process has to be added to build three dimensional devices.

1.2.3 Flip Chip Technique

Traditionally, flip chip technology is defined as mounting the chip to a substrate with any kind of interconnect materials and methods (e.g., flux less solder bumps, tape-automated bonding (TAB), wire interconnects, conductive polymers, anisotropic conductive adhesives, metallurgy bumps, compliant bumps, and pressure contacts), as long as the chip surface (active area) is facing the substrate [6]. Flip chip components are predominantly semiconductor devices; however, with the development of flip chip technology, MEMS devices are also beginning to be used in flip chip form. The boom in flip chip technologies results not only from flip chip's advantages in size, performance, flexibility, reliability and cost over other technologies, but also from the widening availability of flip chip materials, equipment and devices. Using flip chip technologies in MEMS devices, performances can be greatly improved because of the following advantages:

• Smallest size: eliminating the packages and bond wires reduces the required area.

• Highest electrical performance: eliminating bond wires reduces the delaying inductance and capacitance of the connection. (The inductance of a single solder bump is less than 0.05nH, compared to 1nH for a 125-um-long and 25-um-diameter wire.

• Greatest I/O density: unlike wire bonding which requires that bond pads are positioned on the periphery of the die to avoid crossing wires, flip chip allows the placement of bond pads over the entire die.

• Most rugged: flip chips are mechanically the most rugged interconnection method because they are solid little blocks of cured epoxy when completed with an adhesive under fill. Besides these general properties,

Flip chip technologies are attractive to the MEMS industry because of their abilities to integrate a system on a chip through packaging a number of different dies on a single substrate. One of the most attractive features of anyMEMS fabrication service is the number of structural layers available to MEMS designers. Most MEMS fabrication processes have a limited number of structure layers because of time and cost issues. The more structure layers the process has, the longer time and more expensive the process needs. One of the most popular MEMS commercial foundries, Muti-User MEMS Processes (MUMPs), is only a three layers surface micromachining polysilicon process [7]. It is the bottleneck for MEMS designers to design more complex structures. As one solution, flip chip technologies can give designers more room and more releasable layers to construct their designs.

Flip chip technologies also can transfer MEMS devices to other substrates. This technique can be used to produce highly advanced micromechanical systems that are better suited to radio frequency (RF), microwave, or optical applications where specific material properties or additional structural layers are fatal [8]. Figure 1.4 illustrates the flip chip technique.

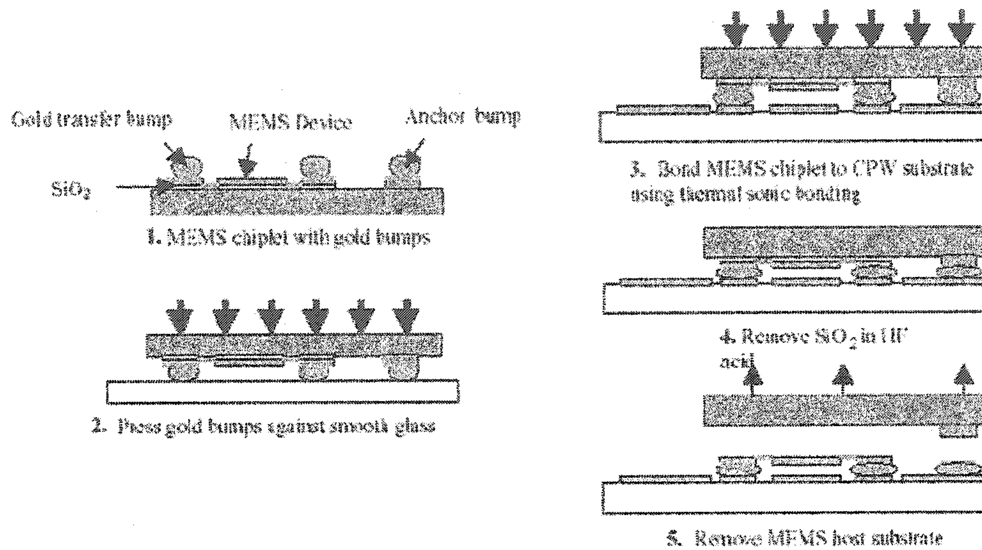


Figure 1.4: The schematic diagram of flip chip process [29]

The process starts with an unreleased MEMS device; gold transfer bumps are placed on all the transfer pads and one anchor pad. The transfer pads are only connected to the host substrate with the sacrificial SiO_2 layer. When the SiO_2 layer is dissolved in hydrofluoric acid (HF), the transfer pads and thus the MEMS devices are completely disconnected from the host substrate. Because of permanent connection to the host substrate, the anchor not only prevents the substrate from contacting the device after release, but also suspends the substrate to act as a shield during the release and drying process. Before bonding the MEMS devices to other substrates, the gold bumps on the MEMS host substrate are pressed against a smooth glass substrate. This pressing step is required to flatten any trailing wires from the top of the bump left by the wire-bonding machine.

In addition, pressing the bumps provides better planarity across the bumps during the actual bonding. Then the entire structure is flip chip bonded to a target substrate. The silicon substrate is anchored at an anchor bump.

Once released, the substrate can be removed sagely by using clamps to break the anchor without damage to the device. After bonding and releasing, the flip chip devices are rinsed in methanol to displace the HF in order to prevent HF further etching from within the devices. After several minutes in a methanol rinse, the devices are super-critically dried in a special drying chamber that uses liquid CO_2 to displace the methanol. Without this step, the evaporating methanol would pull devices downward into contact with the substrate and destroy the devices. After these steps, the MEMS device is transferred to another substrate successfully.

Chapter 2

Introduction

In a large number of RF applications, the many discrete, board-level components significantly increase assembly cost and overall size, as well as limiting performance. Thus integrated passive components would be desirable [9]. It is well recognized that RF-MEMS variable capacitor (varactor) have been shown to exhibit superior performance compared to FET and diode varactors; however most of these devices have been built using highly special processing techniques incompatible with integrated circuit fabrication. As a result, the implementation of RF MEMS devices into products has remained elusive.

In this paper, we will present new CMOS-compatible variable capacitors. Previous designs use separately fabricated CMOS electronics for potential applications like VCOs or tunable filters [10] [11] [12], as the capacitors are not CMOS compatible. For our designs, the structures are made using the CMOS interconnect stack and released with mask CMOS micro machining process. A key advantage of this approach is the CMOS electronics for VCOs and other possible applications can be integrated on the same chip, thereby eliminating losses coming from interconnects between chips.

2.1 Why CMOS35?

This technology, manufactured by TSMC and provided through CMC, is a 0.35-micron dual poly, four metal layers, polycide CMOS process. The recommended nominal supply voltage is 3.3 volts. The technology is suitable for designs in the following areas: analog, low power, RF, high-speed digital, MEMS.

The technology enables users to develop fully suspended **MEMS devices** using single crystal silicon with metal electrodes. The CMOS based MEMS devices can be completely integrated with all kinds of CMOS integrated circuits as figure 2.1. The advantages are listed as followed:

1: Improve the implementation of RF MEMS devices into product by Simplify the packaging, decrease the loss through connection.

2: Improve the performance of the RF integrated circuits dramatically.

3: CMOS35 is a well-known low cost IC fabrication process compared With cmosp28, cmosp9 and so on.

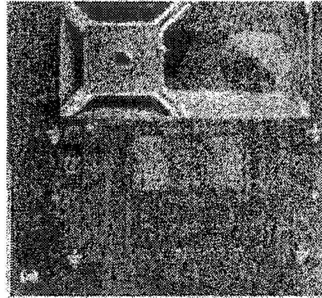


Figure2.1 a CMOSP35 fabricated MEMS varactor integrated with IC. [37]

2.2 CMOSP35 Micromachining

In this part the basic design rules and specifications for the 0.35um TSMC, CMOSP35 technology are discussed and then a simple MEMS design based on this technology and the required CMOS post-processing steps are

presented. The design rules found in document TA-2098-4003 provided by CMC are for a four metal and dual poly process, which we are using for MEMS device fabrication. [13]

2.2.1 CMOSP35 MEMS related Specification

In MEMS applications for the areas which we want to do the post-processing (substrate etching), in order to release the structure, it is compulsory to use 'Active' layer for the layout. Otherwise the thick field oxide layer will not be removed. Figure 2.2 shows the difference between two layouts. There is a metal beam and we want to release it, for the right hand side layout which the active layer has not been used, there is thick field oxide layer and so it's very difficult to do the substrate etching. In this case first we have to do an HF oxide etching and then after removing the black oxide layer it's possible to do the TMAH etching, but the first HF etching will result in damages to the metal layers used in the device structure and also the contact pads.

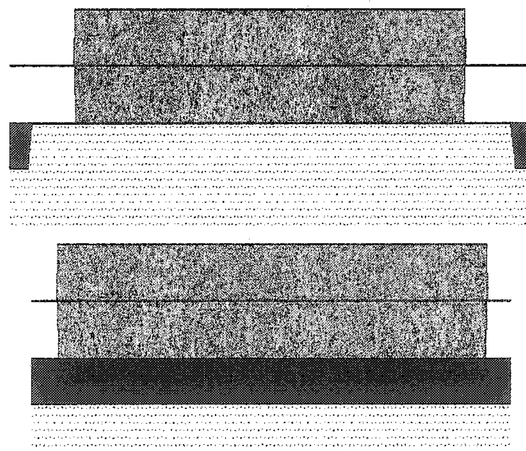


Figure 2.2 Different layouts a) with active layer and b) without the active layer, black color shows the field oxide layer on the substrate [32]

Poly-1 and Poly-2:

The first poly layer has a thickness of 0.275u and is used as the gate for MOS transistors, but it can be also used as a structural layer in MEMS devices. If poly-2 is used as a structural layer then there would be an extra oxide layer between poly-2 and substrate, thin oxide or thick oxide with a thickness of 0.05u or 0.25u, respectively. The minimum density of poly-2 layer shouldn't be less than 24%. This density is calculated as: (Total poly layout area/Chip area). TSMC suggests adding dummy poly patterns for those with poly densities less than 24%. Dummy poly patterns must be added on field oxide area and distributed over chip as uniformly as possible.

The second poly layer, poly-2, is 0.28u thick and usually, in double poly CMOS processes, is used to form capacitors. The top plate of this capacitor is poly-2 and the bottom plate is poly-2, the dielectric between these two plates is an oxide layer with a thickness of 370A.

Contact:

The contact layer is used to etch the oxide layer under Metal-2 and so provides a window to connect Metal-2 to the active region on the substrate. Also using the contact layer it's possible to make a connection between the Metal-2 and Poly layers, but as a design rule, poly contact on active regions is forbidden. It means that if both active and poly layers exist under the Metal-2 layer then the contact window will result in a connection between Metal-2 and active region however it violates the design rule. Figure 2.3, right hand side,

shows the contact between Metal-2 and poly and the left side picture shows the contact between Metal-2 and active layer.

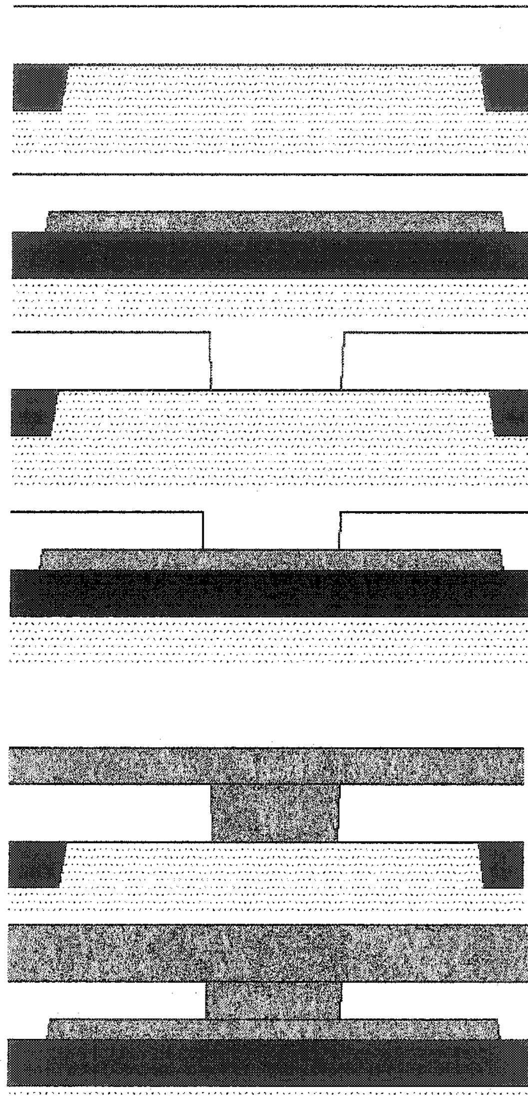


Figure 2.3 contact window for Metal-2[32]

If we use a contact layer without any Metal-2 layer on top of it then the oxide layer between the Metal-2 and Poly or active layer will be removed and it's necessary for the areas which we want to do the substrate etching. The thickness for this oxide layer is 0.428μm.

Metal and via layers:

The most important structural layers for MEMS devices are the metal layers. There are totally four metal layers for this technology separated by silicon-oxide layers between them. The first metal layer, Metal-2, is 0.665u thick. Table 2.1 shows the thickness for the other metal layers and the oxide layers between them.

Layer	Metal-2	Oxide	Metal-2	Oxide
Thickness	6650A	20000A	6400A	20000A

Table 2.1 Thickness of metal layers in TSMC CMOSP35 technology

Via provides a window to connect two metal layers and like the contact window if we use via between two metal layers without the top metal layer, as shown in figure 4, it's possible to etch the oxide layer between the metals. The last metal layer, Metal-4 and the first one, Metal-2, are separated with a thick oxide layer with a total thickness of 3u and by using via-2, via-2, and via-3 with together we can remove this thick oxide layer on the substrate regions where we want to do the TMAH etching.

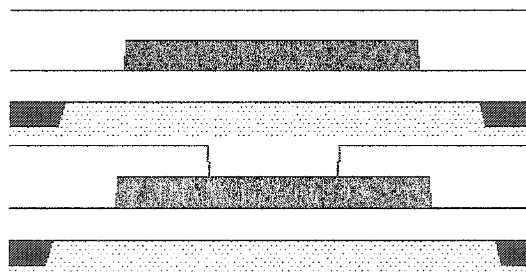


Figure2.4 Via without Metal-2 layer results in oxide etching between Metal-2 and Metal-2[32]

For all metal layers the density of metal area should be larger than 30%. This density is calculated as: Total metal layout area/Chip area. Dummy pattern is required for those with metal density less than 30%. A dummy metal example which TSMC recommends is 5u*2u pads with spacing of 2u.

Pad:

The final masking step is the pad opening. The passivation window provides an opening through the final protecting glass and silicon-nitride layers which cover all the chip area. There are three protecting over glass layers on top of the chip, Silicon-oxy-nitride, spin-on-glass and silicon-nitride respectively, the last layer is silicon-nitride. Table 4 shows the thickness of these layers.

Layer	Silicon-oxy-nitride	Spin-on-glass	Silicon-nitride
Thickness	2500A	3000A	20000A

Table 2.2 Thickness of over glass layers

It is necessary to use the passivation window on top of the pads in order to connect the wires and to do the bonding. For MEMS applications this window should be located on the areas which are going to be etched during the post-processing. Figure below shows an over glass window on top of a pad.

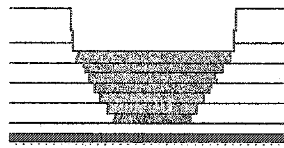


Figure 2.5 Passivation window [32]

There are some points which are not clear about this technology yet. The first one is the exact thickness of thin oxide, thick oxide and field oxide layers. The values reported here are for the TSMC 0.25um CMOS

technology. The other problem relates to via and contact windows. As mentioned before for example by using a via we can remove the oxide layer between two different metal layers, but if we follow the masking steps shown in figure 6 it seems that if we don't use the top metal layer, still there is a deposited metal layer, and the oxide between the top and bottom metal layers is not removed completely. In order to minimize the problems related to post-processing, we need to remove the oxide layers completely and make an open window on the substrate areas which should be etched.

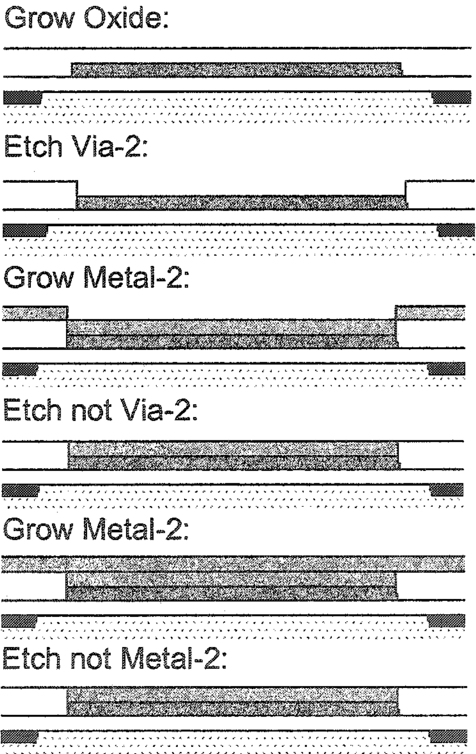


Figure 2.6 not complete etching of oxide layer between Metal-2 and Metal-2 layers [32]

Figure 2.7 shows the same problem. After using all via layers and contact window, between Metal-2 and active region, still there are some metal

and oxide layers under the passivation window and so we can not do the post-processing without using HF to remove the remained oxide layers.

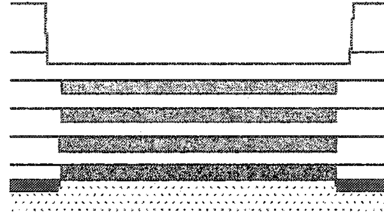


Figure 2.7 remaining metal and oxide layers on top of the substrate areas which should be etched [32]

2.2.2 CMOSP35 MEMS example

CMOS-MEMS Example:

This is a simple example of a MEMS device using CMOSP35 technology. The different layers which will be used in this technology are shown in table 5 along with the corresponding GDSII numbers.

Name	Render	GDSII	Name	Render	GDSII
active		11	metal2		18
poly1		13	via23		27
poly2		14	metal3		28
contact		15	via34		29
metal1		16	metal4		31
via12		17	pad		19

Table 2.3 layers which are used in MEMS devices

Figure 2.8 shows the layout for a MEMS cantilever beam, the structural part of the beam consists of Metal-1, Metal-2, Metal-3 and Metal-4 layers combined with each other. The red squares are the dummy poly-2 cells to increase the density, as mentioned before this density shouldn't be less

than 24%. The other green squares are dummy cells which are consisted of all the metal layers on top of each other. [32]

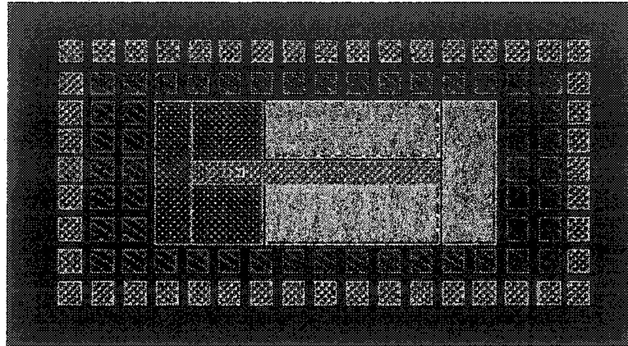


Figure 2.8 MEMS cantilever beam layout

The beam is connected to the support by three via windows, via12, via23, and via34 as shown in figure 2.8. Figure 2.8 shows the details of the layers used for each part of the device, for example the area which we want to do the TMAH is covered with these layers from top to down:

Pad: To make an opening on the over glass layer.

Via34: To etch the oxide between Metal-4 and Metal-3.

Via23: To etch the oxide between Metal-3 and Metal-2.

Via12: To etch the oxide between Metal-2 and Metal-2.

Contact: To etch the thin oxide and thick oxide layers.

Active: To etch the field oxide layer on the substrate.

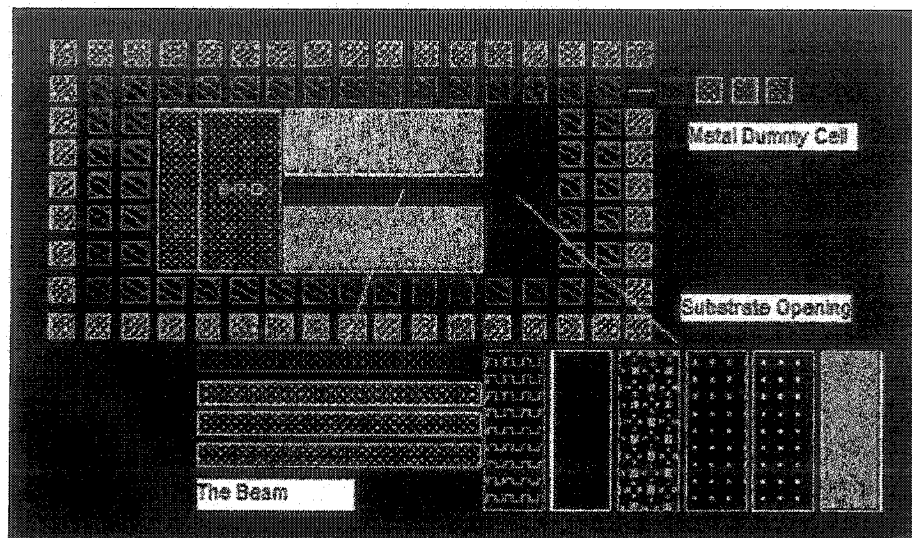


Figure 2.9 detailed view of layers used for different parts of the device

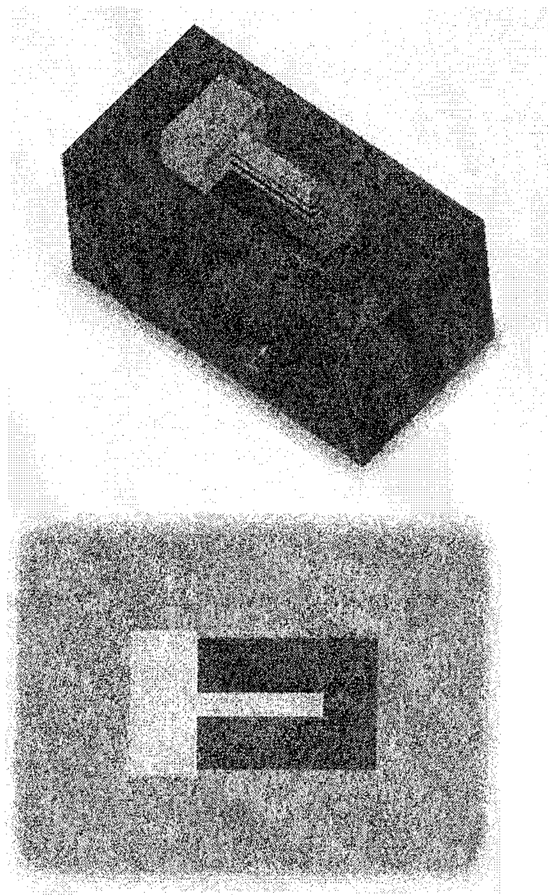


Figure 2.10 the 3-D view and top view of the MEMS cantilever beam [32]

2.3 MUMPS technology introduction

The Multi-user MEMS processes or MUMPs is a three-layer polysilicon surface micromachining process derived from work performed at the Berkeley Sensors and Actuators Center (BSAC) at the University of California in the late 80's and early 90's. It is a commercial program that provides the international industrial, governmental and academic communities with cost effective, proof-of concept surface micromachining fabrication [14]. This process has the general features of a standard surface micromachining process as follows:

- Polysilicon is used as the structure material,
- Deposited silicon oxide is used as the sacrificial layer,
- Silicon nitride is used as electrical isolation between the polysilicon and the substrate,
- Metal (usually gold) is the top layer of the device and can be used as conductive layer.

Figure 2.11 shows the cross section of an electrostatic motor fabricated by the MUMPs process. This device includes all the layers that are available in the MUMPs process. In order

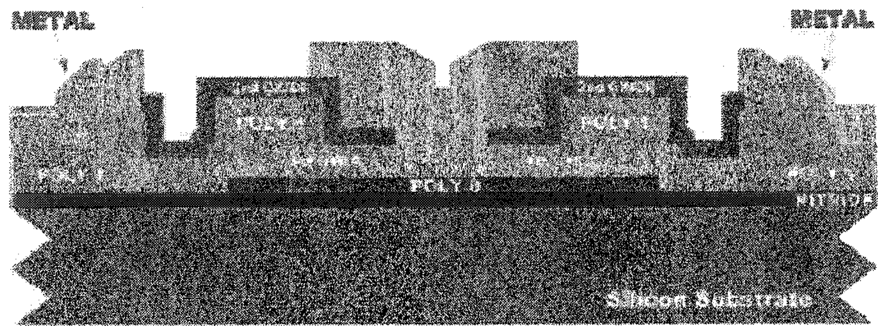


Figure 2.11 Cross section of MEMS motor fabricated by MUMPs [28]

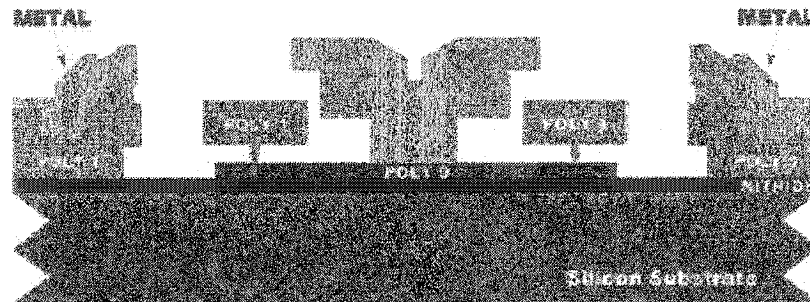
To make the process as general as possible, MUMPs process defines all the layers' thickness and their functions.

All MEMS designers have to follow these definitions and design rules. These definitions and design rules limit the designers to design more complex devices, but they make it possible for many different designs to be put on a single silicon wafer in one single fabrication process. Also, the standardization of the fabrication process reduces the fabrication cost and lets more and more designers submit their designs. In this thesis, all the actuators are designed by the following MUMPs design rules. Table 2.4 shows the main limitations of MUMPs process and a brief introduction of each layer's function.

Material Layer	Thickness	Lithography level name	Function
Silicon Nitride	0.6um		Insulator
Poly0	0.5um	Poly0 and hole0	Conductive layer
First oxide	2.0um	Dimple	Release friction
First oxide	2.0um	Anchor1	Fix poly1 on substrate
Poly1	2.0um	Poly1 and hole1	Structure layer
Second oxide	0.75um	Poly1-poly2-via	Connection with poly1 and poly2
Second oxide	0.75um	Anchor2	Fix poly1 on substrate
Poly2	1.5um	Poly2 and hole2	Structure layer
metal	0.5um	Metal and metal hole	Conductive layer

Table 2.4: MUMPs process layers and their Properties

Figure 2.12 shows a device after sacrificial oxide release.



2.12 Cross section of MEMS motor after releasing process [28]

2.4 Motivation for the study of MUMPs

PolyMUMPs is a process designed specially for MEMS devices. It has a nitride layer as electrical isolation layer, a poly1 layer as ground layer. There is another two poly layers act as the structure layers and there is gold layer on top of the second poly layer to increase the reflectivity and electrical property. The main advantages of PolyMUMPs are as follows:

- Designed to be as general as possible, and to be capable of supporting many different designs on a single silicon wafer
- Not optimized with the purpose of fabricating any one specific device
- Poly-silicon is used as the structural material, deposited oxide (PSG) is used as the sacrificial layer, and silicon nitride is used as electrical isolation
- The thickness of the structural and sacrificial layers were chosen to suit most users
- The TMAH does not etch the polylayers, which made the substrate etching much more easily.

Chapter 3

Review of Various varactors for RF application

Varactor is a capacitor capable of changing its capacitance through external voltage source. Varactor is formulated by the parallel plate capacitor while neglecting the fringing fields.

$C=\varepsilon_0\varepsilon A/d$

Here d is the gap between the plates, A is the overlapping area of the parallel plates, ε is the relative dielectric constant of the medium between the plates, ε_0 is the electric permittivity of vacuum.

Varactors have four main parameters which are tuning ratio (Cmax/Cmin), quality factor (Q), CV characteristic, self resonance frequency. The Quality factor and tuning range are most important parameters.

The Quality factor is defined as:

$$Q=\frac{2\pi(E_{\max,c}-E_{\min,l})}{E_{dis}}$$

$E_{max,c}$ is the maximum energy the capacity can store

$E_{max,l}$ is the maximum energy the inductor can store

E_{dis} is the dissipated energy per cycle.

Q is a measure of loss, which is the less, the better. This means we need large Q .if we have an ideal capacitor and a resistor in series, then its quality factor is

$Q=\frac{1}{RWC}$, here R is the resistance; W is the signal angular .frequency. C is the capacitance.

3.1 MEMS Varactors

MEMs varactors exhibit great chances in improving the quality factor and tuning range ratio. MEMS varactors can be made by polysilicon and metal.

3.1.1 Varactors based on variation of the dielectric

The function principle is realized by a dielectric slab, which is suspended between two capacitor plates (figure3.1) the slab is anchored to the substrate outside the two plates by spring structures and the dielectric is free to move. The dielectric can move to change either the overlap between it and the two plates or the fringing field between them. In the former case, When a DC bias is applied between the two plates, the charges on the capacitor plates exert an electrostatic force on the induced charges in the dielectric to pull the dielectric into the gap. The author also point out that the vertical motion of the dielectric offers a respectable amount of capacitance change as well (Table3.1). Tuning in this mode is due to fringing fields between the asymmetrical metal to dielectric gaps. [15]

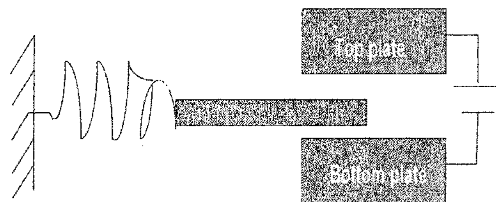


Figure 3.1 Varactor based on the variation of the dielectric

Working mode	C_{max}/C_{min}	Q_{min} (at 2Ghz)
Horizontal	1.077	146
Vertical	1.4	109

Table 3.1Main characteristics of the varactor with Variable Dielectric in two working modes

3.1.2 Varactors based on variation of the overlapping area

This varactor is represented by the comb drive varactors (figure3.2). One of the comb is fixed whereas the other can move towards it and back [16] or parallel to it (up and down) [17].As the movable fingers changes its position, the overlapping area of the capacitor changes and the capacitance changes too.

Most of these kinds of varactors are made of polysilicon. The resistance of polysilion is comparably large and so the loss is large. This results the quality factor is not very large (Table 3.2).If the comb is made by metal, it can cause higher quality factor. However, to produce metallic comb-drive varactors, one needs LIGA or a similar high aspect ration lithography method which is quite expensive because vertical structure dimensions are larger than horizontal ones.

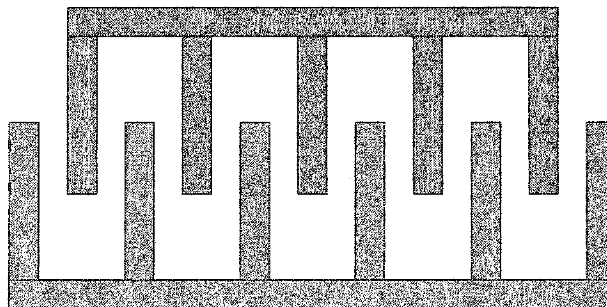


Figure3.2 Comb drive varactors made by polysilicon

Varactor type	Cmax/Cmin	Q(at 2Ghz)
Comb drive(vertical)	3	9
Comb drive(parallel)	1.1	4

Table 3.2 Main parameters of comb drive varactors

3.1.3 Varactors based on variation of the gap

This kind of varactor usually has one movable plate supported by the spring beam. One kind of varactor has one or more electrode which can also act as another capacitor plate. When we add voltage between the plate and

the electrode, the movable plate starts to move toward the electrode. During this, the electrostatic force and the restoring mechanical force are in equilibrium.

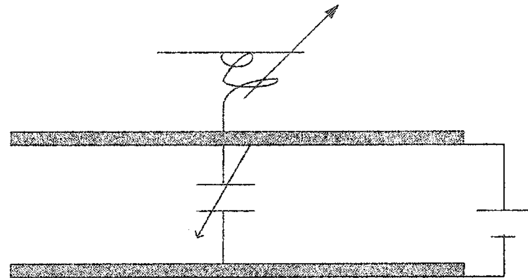


Figure 3.3 Varactor based on variation of the gap

This equilibrium exists only if the distance between the plate and the electrode is larger than the 2/3 of the initial gap. Once the distance is smaller than this (we call the voltage now is V_{th1}), the plate and electrode reach together. Now we reduce the voltage but the plate still stay with the electrode until the voltage reaches another value which we call V_{th2}). The capacitance can only continually change while the voltage is smaller than V_{th1} or bigger than V_{th2}. The tuning range of this capacitor is at most can reach 1.5 in theory.

Another kind of driving principle is by electro thermal actuator (SEM picture). This kind of actuator can move up and down as long as in the limit of mechanics and the two plates do not stick together because of the short distance. The quality factor is also greatly increased by the removal of the substrate beneath of the capacitor.

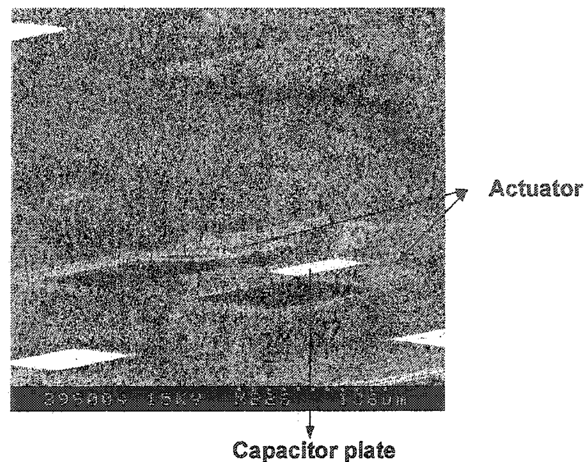


Figure 3.4 Capacitor with electro thermal actuator (SEM)

3.2 Actuators

A micro actuator is the key device for the MEMS to perform physical functions. They can drive the capacitor to the desired value for the Voltage controlled oscillators. They can drive micro mirrors as a scanner or a switch; they also can actuate micro pumps for micro fluidic systems. The most popular actuation principles nowadays are electrostatic force, electro thermal expansion, piezoelectric force which has been used to design various structures for specific applications. This result in the fact that more and more different, powerful and fancy micro actuators have been designed, fabricated, and applied [18].

3.2.1 Thermal actuators

Thermal actuation has been extensively employed in MEMS. It includes a broad spectrum of principles such as thermal pneumatic, shape memory alloy (SMA) effect, bimetal effect, mechanical thermal expansion, etc.

[19]. The thermal pneumatic micro actuator uses thermal expansion of a gas or liquid or the phase change between liquid and gas to create the actuation.

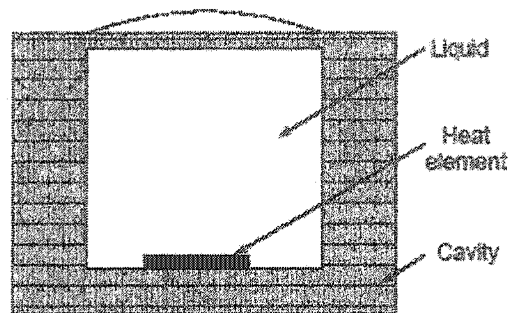


Figure 3.5: The schematic diagram of thermal pneumatic micro actuator

As shown in Figure 3.5, a thermal pneumatic actuator is made of a cavity that contains a volume of fluid with a thin membrane as one wall. Current passed through a heating resistor causes the liquid in the cavity to expand and deform the membrane.

Shape memory alloy effect occurs in some alloys in which a reversible thermal mechanical transformation of the atomic structure of the metal happens at a certain temperature. At low temperature, the SMA is kept at the desired deformed shape. When the temperature rises above a threshold value, the deformed SMA is transformed back to the original shape.

Thermal bimetallic micro actuator consists of two different materials that are layered together. Figure 3.6 shows a cantilever bimetallic structure.

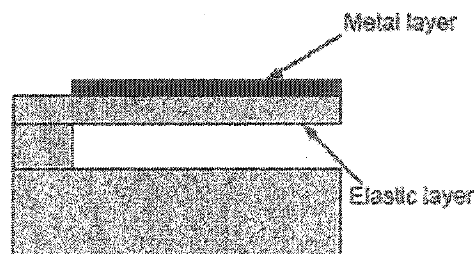


Figure 3.6: The thermal bimetallic micro actuator with the cantilever prototype

When it is heated, a deflection is generated by the different thermal expansion between the two materials. The more different the two materials' thermal expansion coefficients, the more deflection are generated.

The principle of the mechanical thermal expansion micro actuator is similar to that of the bimetallic micro actuator. The only difference is that the mechanical thermal expansion micro actuators are made of the same material.

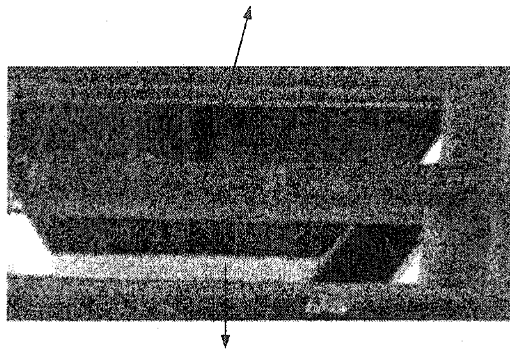


Figure 3.7 two layer polysilicon thermal actuators

The operation procedure of mechanical thermal expansion micro actuators will be explained in detail in Chapter4 and 5.

Thermal actuators can generate relatively large force and displacement at low actuating voltage. The deflection can linearly increase as the control voltage is increased within a large range. Mechanical thermal expansion actuator and bimetallic actuator also can be integrated in a chip easily.

3.2.2 Electrostatic actuators

For a simple parallel-plate style electrostatic micro actuator, the electrostatic force is created by applying the voltage across the two plates. The schematic diagram of this kind of electrostatic micro actuator is shown in

Figure 3.8. Usually the two plates are separate by dielectric material such as air.

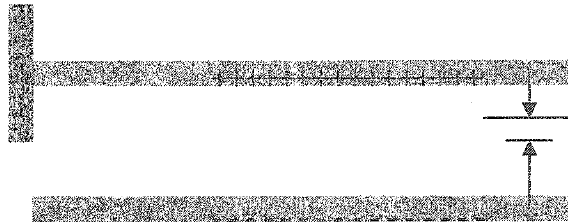


Figure 3.8: The schematic diagram of electrostatic micro actuator

The force generated by applying a voltage can be given by

$$F = V^2 \frac{\partial U}{2\partial d}$$

where F is the electrostatic force, V is the applying voltage, d is the distance between the two plates, U is the energy stored in the two-plate capacitor, which can be obtained by $U=CV^2/2$, C is the capacitance.

The electrostatic micro actuator is one of the most popular micro actuators in MEMS applications. The well-known electrostatic micro actuators include comb-drive micro actuators [20], and wobble micro motors [21]. Figure 3.9 shows scanning electron microscope (SEM) pictures of these two electrostatic micro actuators.

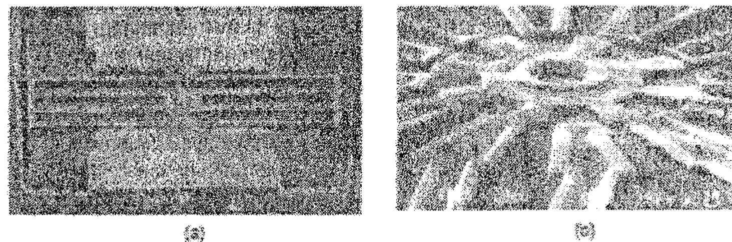


Figure 3.9: (a) Comb-drive electrostatic micro actuator. [2]
(b) Electrostatic micro motor

From the fabrication point of view, the electrostatic micro actuator can be easily integrated on a chip because all fabrication processes are

compatible with traditional IC fabrication. Since there is no current consumption during actuation, the electrostatic micro actuator consumes no power. But in order to have a large deflection or force, high actuating voltage is needed. Also, hysteresis makes the electrostatic micro actuator hard to control.

3.2.3 Other actuators

Other actuators such as magnetic actuators and piezoelectric actuators have also been developed for some special applications [22], [23]. Micro actuators are often fabricated by electroplating techniques, using nickel or its compositions. Since nickel is a ferromagnetic material, it can be used in actuators by using the electromagnetic effect.

The principle of the piezoelectric actuator is based on the inverse piezoelectric effect. When a voltage is applied to an asymmetric crystal lattice, the material will be deformed in a certain direction. Although these two actuators can provide large forces, the fabrication process needs to be further developed.

Chapter 4

A completely CMOS compatible RF Varactor and MUMPS Varactor

4.1 CMOS varactor design and analysis

Several discrete, board level, high performance MEMS capacitors are studied, fabricated and reported in the literature. However, the cost by assembly and packaging has been always an issue [24][25]. This project aimed to build an IC compatible RF capacitor, fabricated using TSMC CMOSP35 technology.

The capacitor and actuator are fabricated by the two poly layer in CMOSP35.The electro thermal actuator connected with the poly2 layer can move up while the actuator connected with the poly1 layer can move downward.

The plate area are designed as 90um*90um and 200um*200um to increase the nominal capacitance.

Following is the layout of the capacitors and actuators fabricated by TSMC CMOSP35 technology.

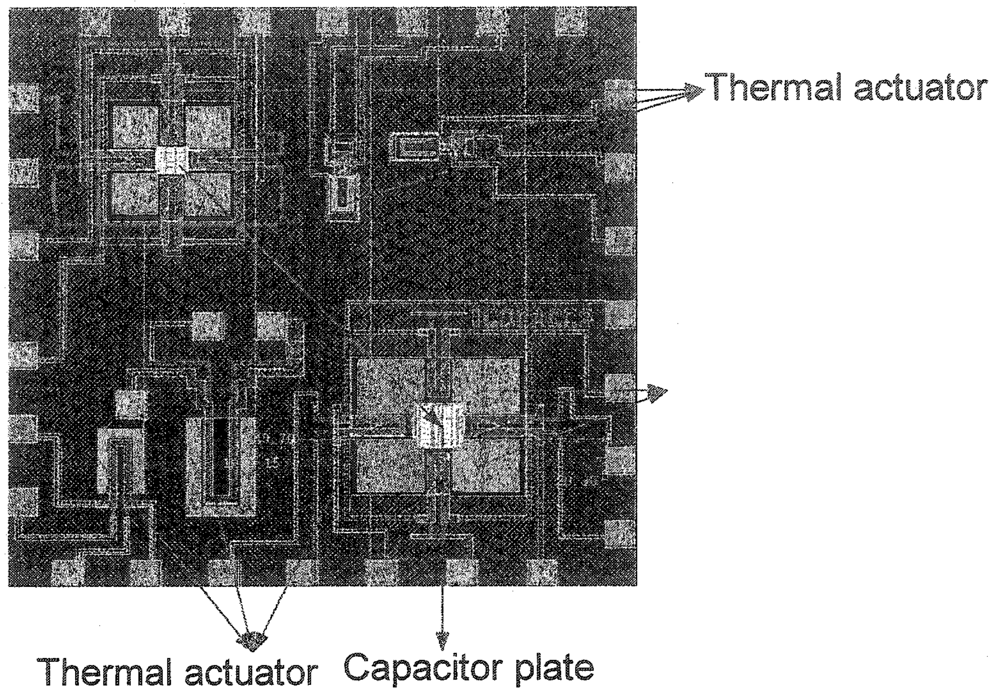


Figure 4.1 top view of the Layout of varactor and actuator

Poly1 thickness Hp1	0.275um
Poly2 thickness Hp2	0.18 um
Oxide	370A
Ls2	37um
W2	24um
Ll2	210um
W1	8um
L1	276um
Le	22um

Table 4.1 Actuator Model parameters

There is a layer of silicon oxide between the two poly layers. When adding voltage between the two pads connected with poly1, the current in poly1 layer will make it expand. The beam will bend up because the difference of the two polylayers expansion. While adding voltage between the pads of poly2, the beam will move downward.

The top plate of the capacitor is made of poly2 while the bottom layer is made of poly1 layer. The capacitance is changeable linearly by the

continuing change of the gap between the two plates. The top plate can move up while the bottom plate can move down, this greatly increased the tuning range of the capacitor. The quality factor (measure of loss) is also increased because of the substrate under the capacitor plate and the actuators are etched away. The loss through the substrate is almost zero.

Through metal layers, this capacitor can be directly connected with the IC integrated circuits.

In the following discussions convection means heat losses through air to the substrate, radiation means heat dissipation through radiation to the ambient environment, and conduction means heat loss through conduction to the anchors.

Analyzation:

Table 4.2 Model parameters

Resistance of Poly2 ρ_0	20	Ohm.um
Resistance of Poly1	10	Ohm.um
Thermal conduction of air	$0.026*10^{-6}$	$w.um^{-1}C^{-1}$
Thermal conduction of poly	$41*10^{-6}$	$w.um^{-1}C^{-1}$
Young's modulus	$169*10^{9}$	Pa
Poisson's ratio	0.22	
Thermal conduction of sio_2	$1.4*10^{-6}$	$w.um^{-1}C^{-1}$
Substrate temprature	27°C	

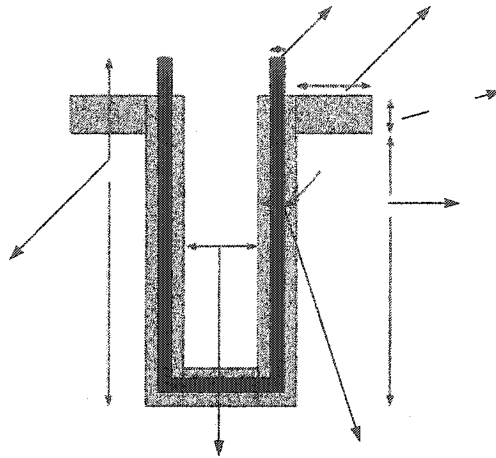


Figure 4.2 Top views of the thermal vertical actuators.

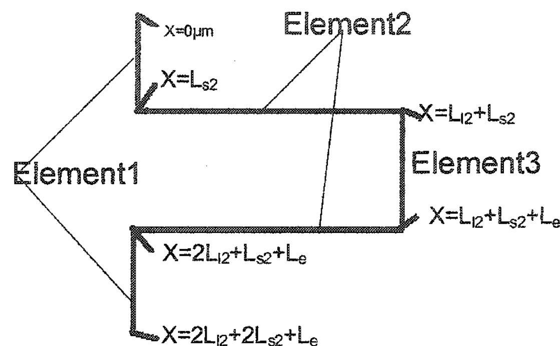


Figure 4.3 simplified one-dimensional coordinate system for the actuator

Element1, Element2, Element3 represents the two short beamL_{s2}, two long beam L_{l2} and the middle connection part of the two long beams for the relative layer.

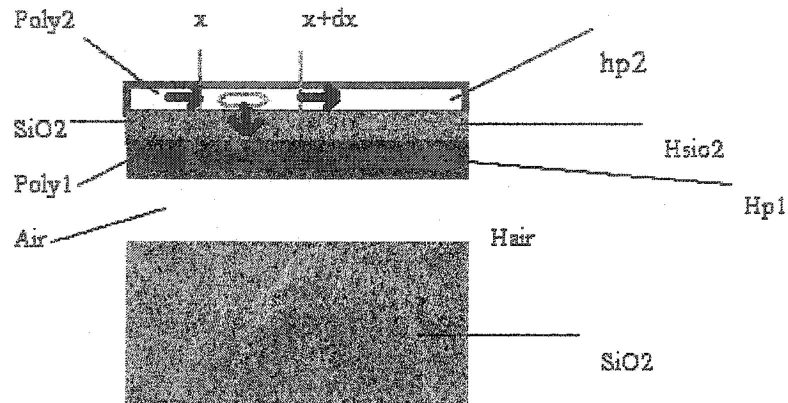


Figure 4.4 Cross section diagram of the actuator for thermal analysis

As shown in figure 4.4, the heat flow equation is derived by examining a differential element of the micro beam of width w_2, thickness h_{p2} and length d_x. Under steady state conditions, resistive heating power generated in the element is equal to heat conduction and convection out of the element. Here the heat loss through radiation is neglected based on the previous analyses using finite element. [34]

$$-K_p W_2 H_{p2} (\frac{d_T}{d_X})_x + J^2 \rho W_2 H_{p2} \Delta x = -K_p W_2 H_{p2} (\frac{d_T}{d_x})_{x+\Delta x} + S \Delta x W_2 \frac{T - T_s}{R_T} \quad \textbf{(1)}$$

Here ρ is the receptivity of the polysilicon. Usually, the resistivity is related to the temperature of the polysilicon, here assumes the resistivity is linearly changeable with the temperature with the coefficient of ξ.

$\rho = \rho_0[1+ \xi(T-T_s)]$

T_s: Substrate temperature, which we set 300K.

T is the operating temperature

K_p is the polysilicon thermal conductivity

J is the current density which equals to J=$\frac{V}{\rho L}$, V is the voltage applied to the two pads of the layer; the L is the length of the layer.

S is the shape factor that accounts for the impact of the shape of the element on heat conduction to the substrate, it equals to

$$S=\frac{H_{p2}}{W_2}\left[\frac{2(H_{SiO2}+H_{poly1}+H_{air})}{H_{p2}}+1\right]+1$$

The shape factor represents the ratio of heat loss from the sides and the bottom of the beam to the heat loss from the bottom of the beam only.

Here H_{p2}, H_{sio2}, H_{poly1}, H_{air} are the thickness of poly2 layer, SiO_2 between two poly layers, Poly1 layer, and the air separately.

R_T is thermal resistance between the polysilicon micro beam and the substrate if the micro beam is wide enough. R_T is given by

$$R_T=\frac{H_{siO_2}}{K_{SiO_2}}+\frac{H_{p1}}{K_p}+\frac{H_{air}}{K_{air}}$$

Here K_{sio2}, K_p and K_{air} are thermal conductivity of SiO_2, Polylayer and air separately.

Taking the limit as $\Delta x \to 0$ for equation (1) produces the following second-order differential equation.

$$Kp\frac{d^2{}_T}{d_X{}^2}+J^2\rho=\frac{S(T-T_s)}{R_T}Htp_2 \quad \textbf{(2)}$$

Solving equation (2) for the three element, the temperature distribution were obtained as follows, respectfully

$$T_1=T_s+\frac{B_1}{A_1^2}+C_1e^{A_1x}+C_2e^{-A_1x} \quad (3)$$

$$T_2= T_s+\frac{B_2}{A_2^2}+C_3e^{A_2x}+C_4e^{-A_2x} \quad (4)$$

$$T_3= T_s+\frac{B_3}{A_3^2}+C_5e^{A_3x}+C_6e^{-A_3x} \quad (5)$$

Here T_1, T2 and T_3 represent the temperature distribution for element1, element2 and element3 separately. C $_{(1\text{-}6)}$ is the constants to be obtained.

$$B_1=\frac{V_{s2}}{L_{s2}^2\rho_0K_p}$$

$$A_1=\frac{S}{K_pR_TT_{p2}}+B_1\xi$$

$$V_{s2}=\frac{V}{2(L_{s2}+L_{l2}+L_e)}L_{s2}$$

Here V_{s2}, V_{l2}, V_e represent the active voltage on Element1,2 and 3.

For R_T and S, it is all the same for the three elements.

$$B_2=\frac{V_{l2}}{L_{l2}^2\rho_0K_p}$$

$$A_2=\frac{S}{K_pR_TT_{p2}}+B_2\xi$$

$$V_{l2}=\frac{V}{2(L_{s2}+L_{l2}+L_e)}L_{l2}$$

$$B_3=\frac{Ve}{L_e^2\rho_0K_p}$$

$$A_3=\frac{S}{K_pR_TT_{p2}}+B_3\xi$$

$$Ve=\frac{V}{2(L_{s2}+L_{l2}+L_e)}L_e$$

R_T=3.8*$e^8\Omega$ (Thermal resistance)

S=1.86(The shape factor)

For equation $T_1=T_s+\frac{B_1}{A_1{}^2}+C_1e^{A_1x}+C_2e^{-A_1x}$, if we add 4 volt

between the two pads connected with Poly2 layers

B_1=6.9e-2

V_{s2}=0.28V

$A_1{}^2$=4.28e-2

A_1=0.2

$T_1=T_s+1.63+C_1e^{0.2x}+C_2e^{-0.2x}$

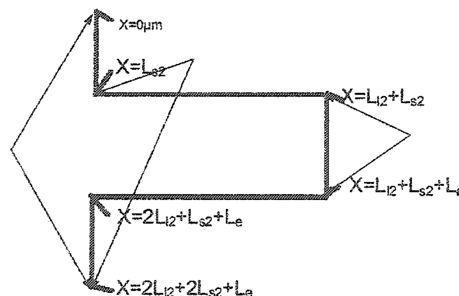
Similarly, T2 and T_3 were got as follows:

$T_2=T_s+0.875+C_3e^{0.3x}+C_4e^{-0.3x}$

$T_3=T_s+0.854+C_5e^{0.9x}+C_6e^{-0.9x}$

For C ($_{1\text{-}6}$) we need at least 6 boundary conditions of temperature distribution to solve the equations of (3) (4) (5). As the structure of our thermal actuator is symmetrical, the temperature distribution of the actuator should be symmetrical too.

Therefore, the temperatures of both ends of short beam are equal to T_{n1}(T_{n1}=Ts) and T_{n2}. The temperatures of both ends of Le are equal to T_{n3}.



4.5 The boundary conditions of temperature continuity

Substituting all the boundary conditions into equations (3)(4)(5), the following equations are obtained

$$\overline{AC} = \overline{B} \qquad \textbf{(6)}$$

Here

$$\overline{A} = \begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ e^{A_1 L_s 2} & e^{-A_1 L_s 2} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 0 & -1 & 0 \\ 0 & 0 & e^{A_2 L_l 2} & e^{-A_2 L_l 2} & 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 & 1 & 1 & 0 & -1 \\ 0 & 0 & 0 & 0 & e^{A_3 L_e} & e^{-A_3 L_e} & 0 & -1 \\ A_1 e^{A_1 L_s 2} & -A_1 e^{-A_1 L_s 2} & -A_2 & A_2 & 0 & 0 & 0 & 0 \\ 0 & 0 & \lambda e^{A2 L_l 2} & -\lambda e^{-A2 L_l 2} & e^{A3 L_l 2} & -e^{A3 L_l 2} & 0 & \dfrac{R}{K_p W_2 H_{p1} A_3} \end{bmatrix}$$

$$\overline{B} = \begin{bmatrix} -\dfrac{B_1^2}{A_1^{\,2}} \\ -Ts - \dfrac{B_1^2}{A_1^{\,2}} \\ -Ts - \dfrac{B_2^2}{A_2^{\,2}} \\ -Ts - \dfrac{B_2^2}{A_2^{\,2}} \\ -Ts - \dfrac{B_3^2}{A_3^{\,2}} \\ -Ts - \dfrac{B_3^2}{A_3^{\,2}} \\ 0 \\ \dfrac{-RTs}{KpW_2 H_{p1} A_3} \end{bmatrix}$$

$$\overline{C} = \begin{bmatrix} C_1 \\ C_2 \\ C_3 \\ C_4 \\ C_5 \\ C_6 \\ T_{n2} \\ T_{n3} \end{bmatrix}$$

Here λ is equal to $W_2H_{p2}A_2/W1H_{p1}A_3$; R is the thermal resistance of the bottom layer of the U-shape vertical thermal actuator.

Finally, the temperature distribution was got as follows:

For x=0μm and x=210*2+37*2+22=516 T=300K

For x=37μm and x=479μm T=550K

For x=247μm and x=269μm T=580K

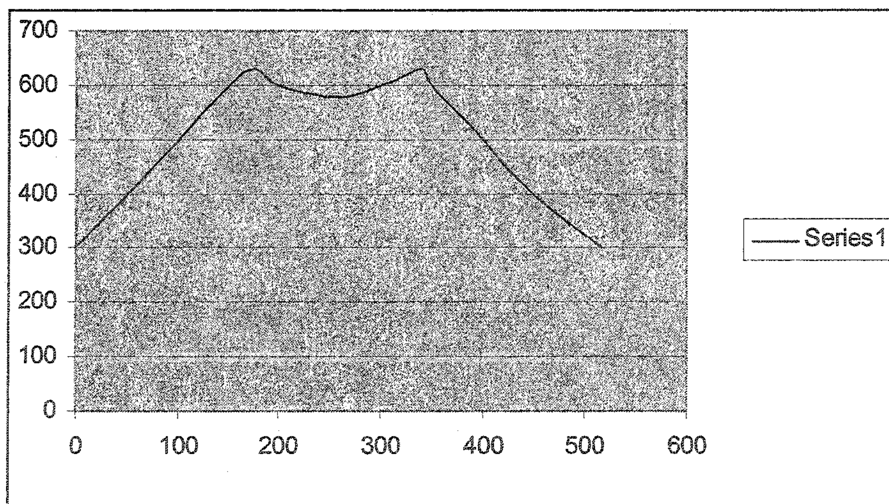


Figure 4.6 the temperature distribution along the actuator beam. (X: the position along the beam (μm), Y: The temperature (K)

4.2 Mechanical analysis

4.2.1 Analytical solution

The linear thermal expansions of the top and bottom layers are the Inputs of the mechanical analysis of the thermal actuator. Based on Equation (4), the thermal expansion of the poly2 layer could be obtained From

$$\Delta L_{12} = \alpha \int_0^{L_{l2}} (T - Ts)dx = \alpha[\frac{B_2}{A_2^2} L_{l2} + \frac{C_3}{A_2}(e^{A_2 L_{l2}} - 1) - \frac{C_4}{A_2}(e^{-A_2 L_{l2}} - 1)] \quad \textbf{(7)}$$

Here the parameters definitions are similar as those in section 4.1.Also, The expansion of element1 and element3 are neglected compared with element2. The thermal expansion of the bottom layer because of the heating of the top layer is similar as

$$\Delta L_{11} = \alpha \int_0^{L_{l1}} (T - Ts)dx = \frac{1}{2}\alpha(T_{n3} - T_s)L_{l1} \quad \textbf{(8)}$$

Here the T_{n3} is the tip temperature of the poly2 layer.

Since the actuator is symmetrical, it can be simplified to figure 4.8. In this Model, element1 is treated as a tortional spring, because when the tip of the vertical thermal actuator bends downward or upward, the long beam rotates about element1.

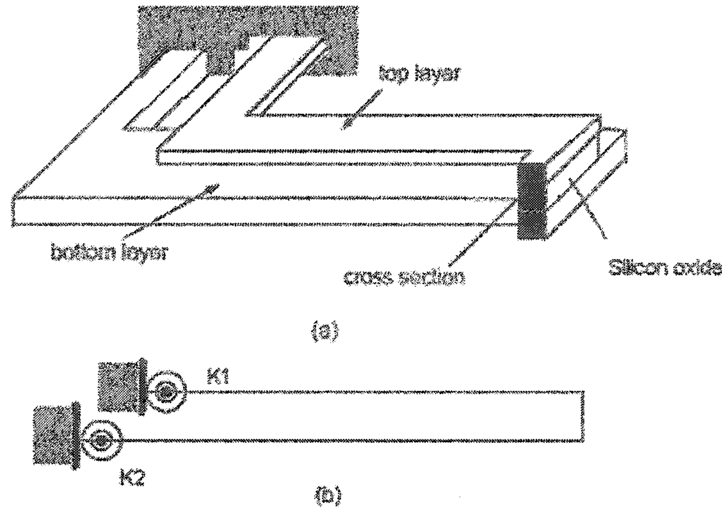


Figure 4.7 (a) the schematic 3D views of the actuator. (b) Four bar Linkage representing for the U-shaped actuator [35]

The deflection of the actuator could be calculated by the following equations. Because the base of the plane rigid frame shown in figure 4.7(b) is hinged And two force components (F_1 and F_2) are calculated by solving equation (9)

$$\begin{bmatrix} f_{11} & f_{12} \\ f_{21} & f_{22} \end{bmatrix}\begin{bmatrix} F_1 \\ F_2 \end{bmatrix}=\begin{bmatrix} \Delta L_{l1}-\Delta L_{l2} \\ 0 \end{bmatrix} \quad \textbf{(9)}$$

Here fij represents the flexibility coefficients, and they can obtained by

$$f_{11}=\frac{L_{l2}^{3}}{3EI_2}+\frac{L_{l2}^{2}L_g}{EI_g}+\frac{L_{l2}^{2}L_{l1}}{EI_1}-\frac{Ll_1^{3}}{3EI_1}$$

$$f_{12}=\frac{L_{l1}^{2}L_g}{2EI_1}-\frac{L_{l2}L_gL_{l1}}{EI_1}-\frac{2L_g^{2}L_{l2}}{3EI_g}$$

$$f12=f21$$

$$f22=\frac{L_g^{3}}{2EI_g}+\frac{L_g2L_{l1}}{EI_1}$$

here E is the Young's modulus of polysilicon, I_1, I_2 and I_g are the moment of inertia for the top and bottom layer long beams and the silicon oxide layer between them. Once the two force components are achieved, the deflection of

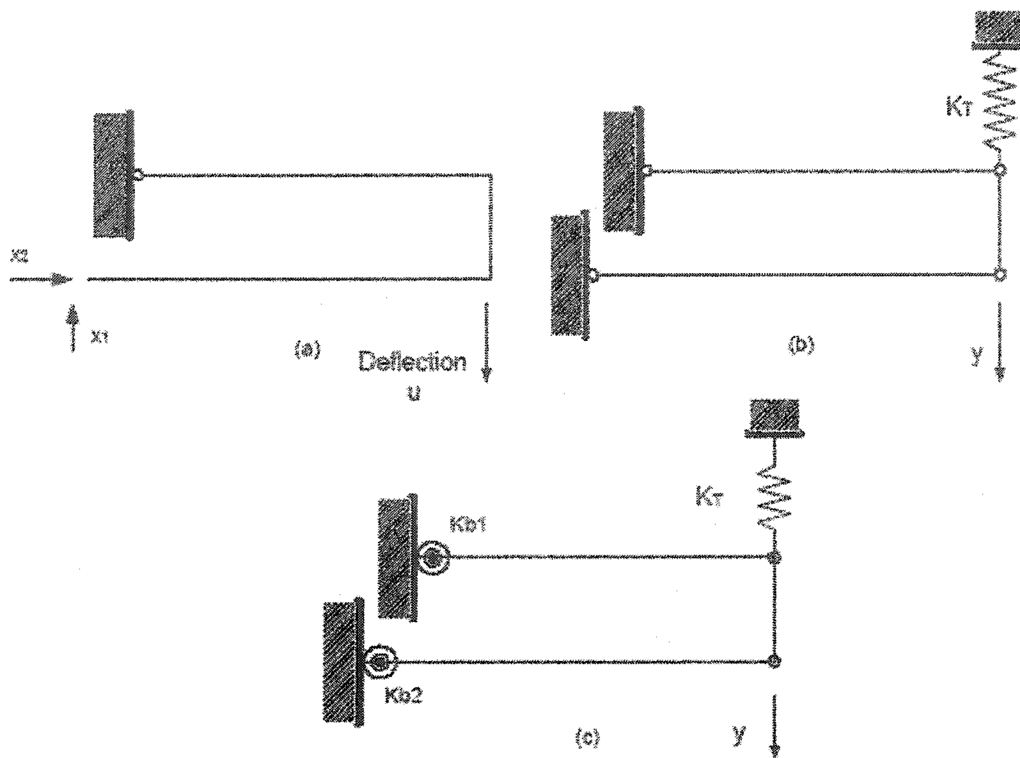
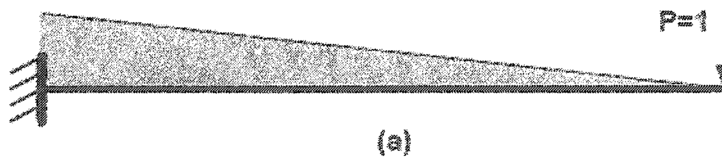
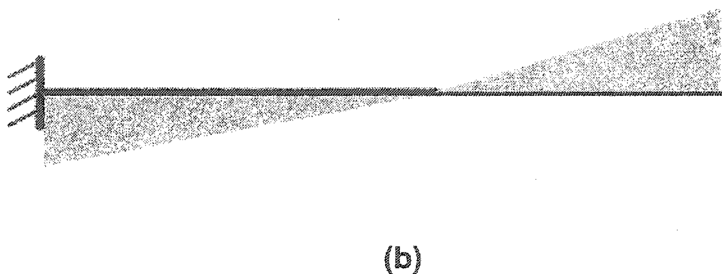


Figure 4.8 (a) The hinged rigid frame for mechanical analysis, (b) schematic of the spring coefficient analysis in y direction. (c) Schematic of the deflection of the actuator[35]

the end of the rigid frame without torsional spring can still be calculated by using the virtual work method. The bending moment due to the virtual force as a function of the position of the top layer long beam is given by





(b)

Figure 4.9(a) the bending moment of the top layer long beam due to the virtual force, (b) The bending moment of the top layer long beam due to the thermal expansion [35]

$\overline{M} = L_{l1} - x$ **(10)**

The bending moment due to the thermal expansion is shown in figure 4.9(b).

$T = F_1 x + F_1(L_{l2} - L_{l1}) - F_2 L_g$ **(11)**

According to the virtual work method, the deflection of the hinged rigid frame without the torsional springs (Figure 4-8 (a)) can be found as

$$s = \frac{1}{EI_1}\int_0^{L_{l1}} M\overline{M}dx = \frac{1}{EI_1}(-\frac{1}{3}F_1 L_{l1}^3 + \frac{1}{2}F_1 L_{l1}^2 L_{l2} - \frac{1}{2}F_2 L_{l1}^2 L_g) \quad \textbf{(12)}$$

In order to find the stiffness coefficient KT in Figure 4-8 (b), three deflections are assigned to the hinged rigid frame structure (Figure 4-10).By using the force method, the stiffness matrix

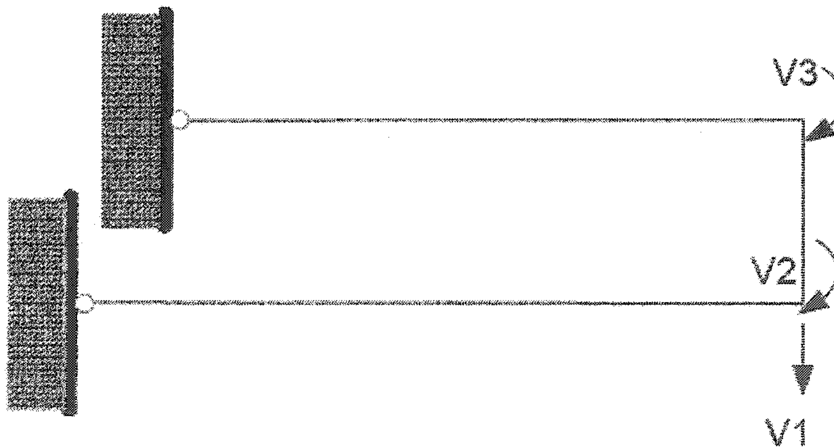


Figure 4.10 The hinged rigid frame with three deflection directions [35]

of the structure in Figure 4-11 can be obtained

$$\begin{bmatrix} K_{11} & K_{12} & K_{13} \\ K_{21} & K_{22} & K_{23} \\ K_{31} & K_{32} & K_{33} \end{bmatrix} \begin{bmatrix} \Delta_1 \\ \Delta_2 \\ \Delta_3 \end{bmatrix} = \begin{bmatrix} G_1 \\ G_2 \\ G_3 \end{bmatrix} \quad \textbf{(13)}$$

where kij is the stiffness coefficient. The definition of a stiffness coefficient is analogous to the definition of the flexibility coefficient: a typical coefficient kij represents the force at i due to a unit displacement applied at j[36]. Δi is the deflection in i direction and Gi is the force at i direction. The stiffness coefficient kij can be given by

$$K_{11} = \frac{3EI_2}{L_{l2}^{\ 3}} + \frac{3EI_1}{L_{l1}^{\ 3}}$$

$$K_{21} = \frac{3EI_2}{L_{l2}^{\ 2}}$$

$$K_{31} = \frac{3EI_1}{L_{l1}^{\ 2}}$$

$$K_{21} = K_{12}$$

$$K_{22} = \frac{3EI_2}{L_{l2}} + \frac{4EI_g}{L_g}$$

$$K_{32} = \frac{3EI_g}{L_g}$$

$$K_{31} = K_{13}$$

$$K_{23} = L_{32}$$

$$K_{33} = \frac{3EI_1}{L_{l1}} + \frac{4EI_g}{L_g}$$

Let G2 and G3 equal to zero, the stiffness coefficient in the direction of V1 can be found from equation (13).

$$\mathrm{K_T} = K_{11} + \frac{K_{23}K_{31} - K_{33}K_{21}}{K_{22}K_{33} - K_{23}K_{32}} K_{12} + \frac{K_{32}K_{21} - K_{22}K_{31}}{K_{22}K_{33} - K_{23}K_{32}} K_{13} \quad \textbf{(14)}$$

where K_T is the stiffness coefficient of the hinged frame in the direction of V1.

Figure 4-11 shows the steps of how to find the final deflection of the U-shape vertical thermal actuator. In Figure 4-11 (a), the thermal expansion can generate the deflection u at the tip of the actuator; it can be treated as an equivalent force G acting at the tip and generates the same deflection. Hence, the value of force G is μkT. When the two torsional springs are added to the structure shown in Figure 4-11 (b),

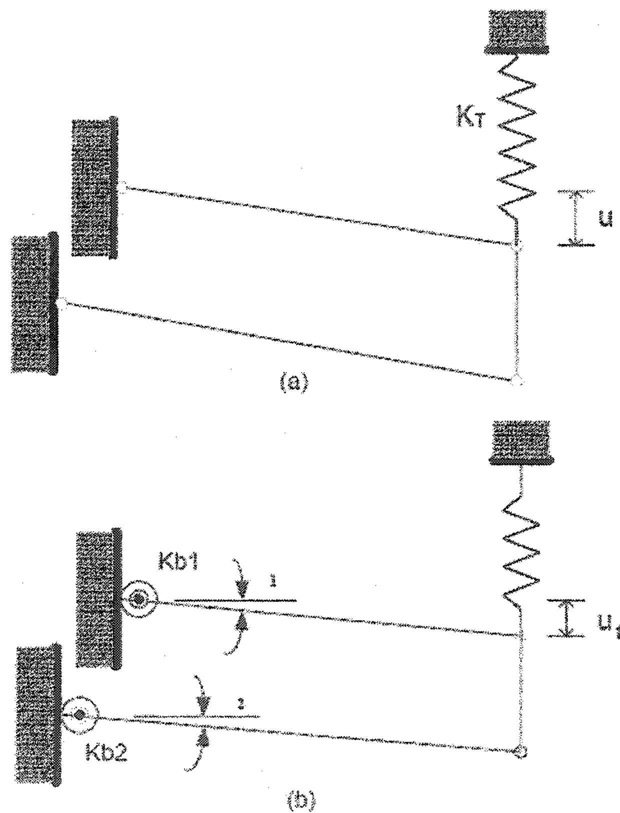


Figure 4-11: (a) the deflection without torsional springs. (b) the deflection with two torsional springs

the final deflection of the U-shape vertical thermal actuator can be obtained from

$$u_f = \frac{K_T}{K_T + \frac{K_{b1}}{L_{l1}^{\ 2}} + \frac{K_{b2}}{L_{l2}^{\ 2}}} u$$

where K_{b1} and K_{b2} are the torsional spring coefficients of the top and bottom layer short bars respectively.

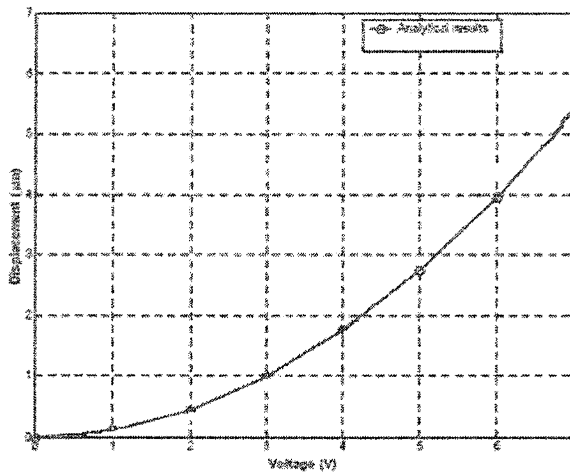


Figure4.12 Deflection of the tip of the U-shaped vertical thermal actuator as a function of input voltage

4.3 MUMPS device fabrication and specification

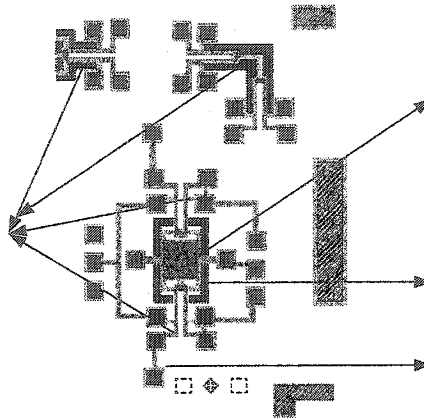


Figure 4.13 PolyMUMPs capacitor and actuator Layout

This is the layout of the capacitor designed using the PolyMUMPs technology. The poly1 and poly2 layers were used as the structure layers of the varactor, which are the part of blue color. The size is 210μm*210μm. The black area surrounded the plate are open area that is designed to reach the silicon substrate so later the substrate could be etched away by the TMAH.

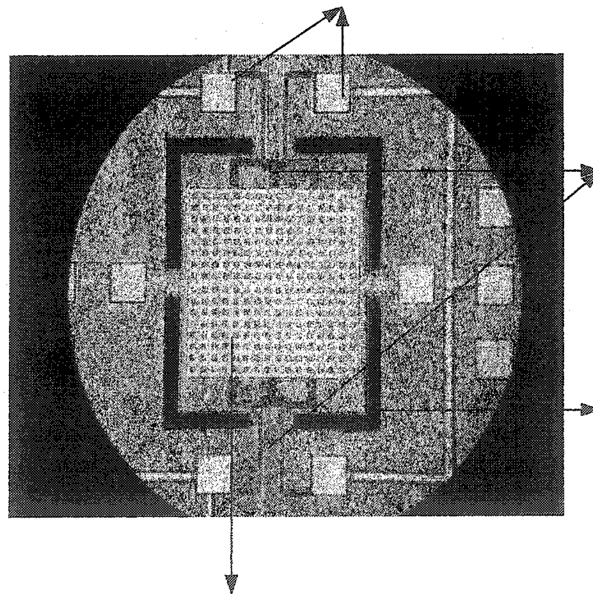


Figure 4.14 Released PolyMUMPs designed varactor

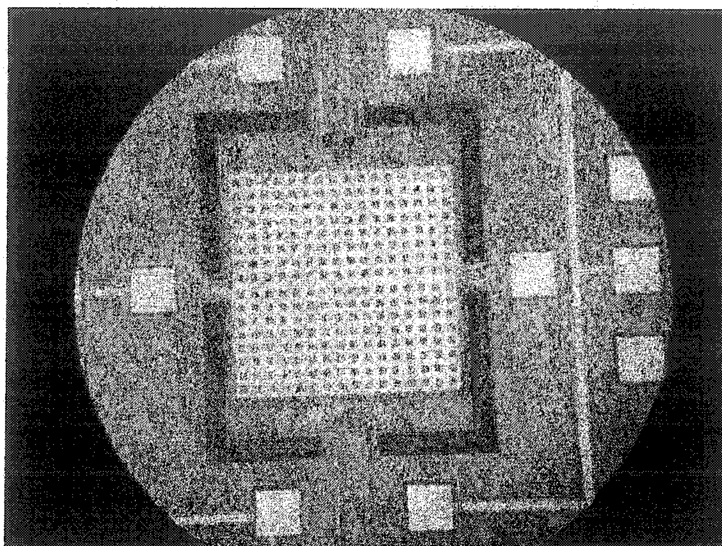
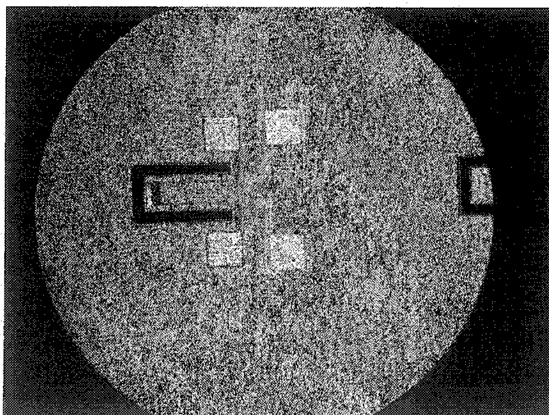


Figure 4.15 varactor before HF release

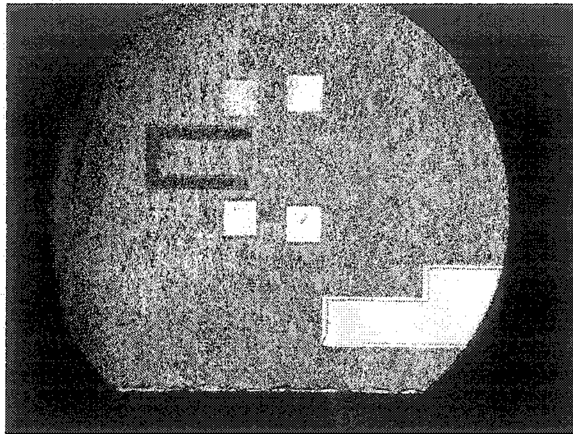
Figure 4.14 is the picture of released device before the TMAH. Figure 4.15 is the picture of the device before HF release.

The red actuator is composed of Poly1 layer that could move up and down.

Figure 4.16 is the electro thermal actuator.



(a) After the release



(b) Before the release

Figure4.16 electro thermal actuator before and after HF release

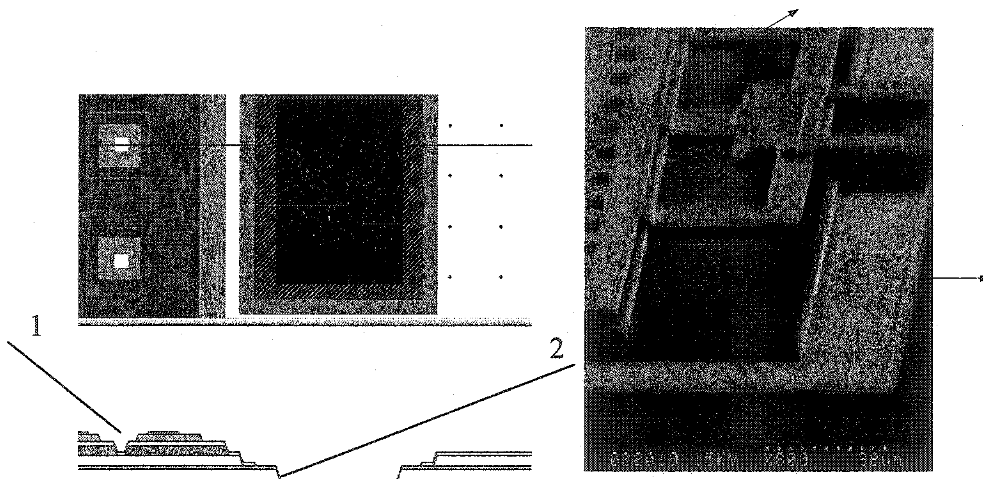


Figure 4.17 Cross-Section of the capacitor plate and open area

Figure 4.17 shows the detail design for the open area that is number 2. From experiment, the polysilicon in MUMPS design is not etchable in TMAH so we can put the device in the TMAH as long as it needs to etch the silicon under the actuator and capacitor.

From figure 4.17, HF can etch the silicon oxide between the poly1 and poly2 layer and also the silicon oxide under poly1 layer through the small open area. The two plates of the varactor can be released by the HF etching.

From figure as follows, the capacitor plate is composed of poly1 and poly2. The poly1 layer is non-movable. The red is poly1 and the grey is poly2 layer. The black on top of the poly2 layer is gold. The gold and poly layers are opened as figure 4.18 shows and the silicon oxide between the poly layers and the oxide under the poly1 layer can be etched away by the HF.

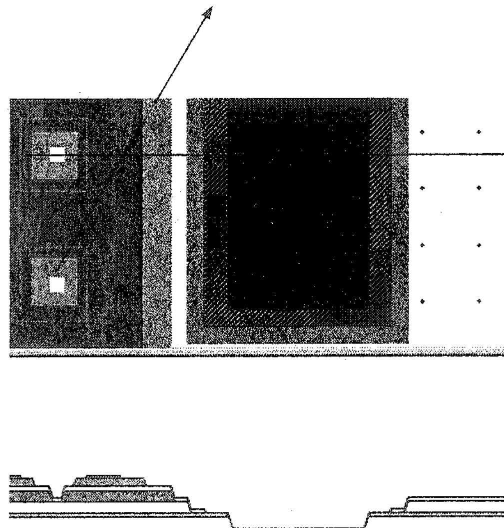


Figure 4.18 Cross section of the designed capacitor plate.

Figure 4.19 is the layout of the capacitor for the flip chip application.

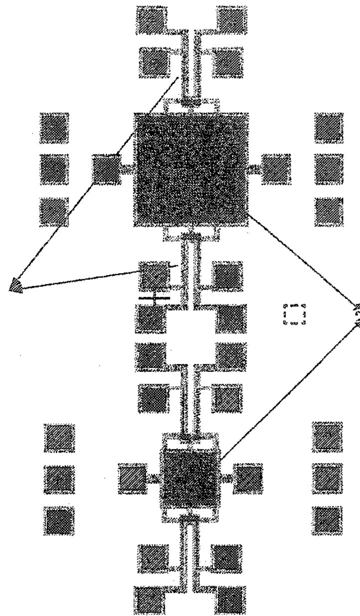


Figure 4.19 Layout of the capacitor for the flip chip application.

These two capacitors are specially designed for the flip chip. The pad and the capacitor are designed so there is a layer of silicon oxide under all the structure layers. This is how the device can be flip chipped to another substrate and after that the substrate under the device can be etched away by HF. The cross section of the design is as figure 4.20.

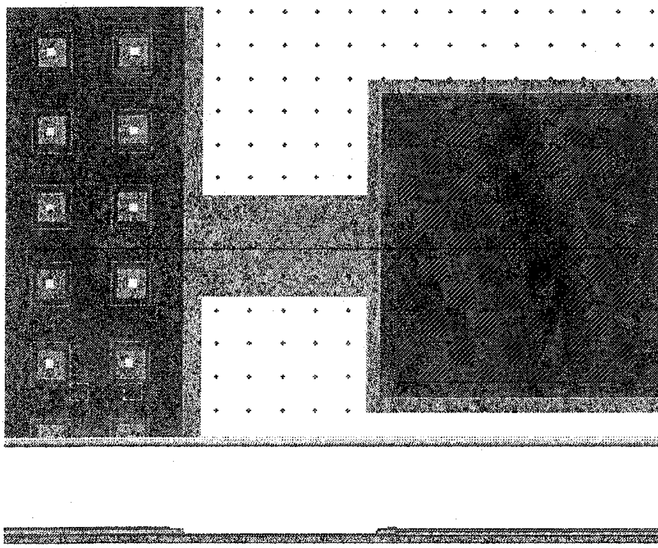


Figure 4.20 Cross section of the capacitor for flip chip

4.4 Simulation result for the PolyMUMPs actuator

The simulation is done by ANSYS software for the PolyMUMPs designed actuator. ANSYS is a general-purpose finite element-modeling package for numerically solving a wide variety of mechanical problems. These problems include: static/dynamic structural analysis (both linear and non-linear), heat transfer and fluid problems. The thermal actuator works on the basis of a differential thermal expansion between different layers composed of the same material. The required analysis is a coupled-field multiphysics analysis that accounts for the interaction (coupling) between thermal, electric, and structural fields.

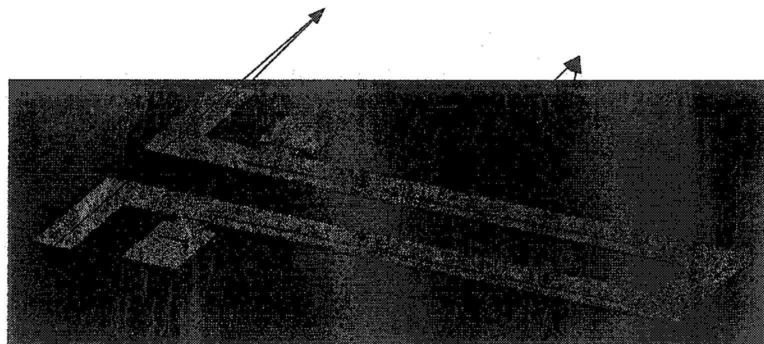


Figure 4.21 Thermal actuator

A potential difference applied across the electrical connection pads induces a current to flow through the beam. The current flow and the resistivity of the polysilicon produce Joule heating (I^2R) in the beam. The Joule heating causes the beam to heat up. Temperatures in the range of 300 - 883K are generated. These temperatures produce thermal expansion and thermally induced deflections.

One of the polysilicon layers is heated and expanded. The difference of expansion of the two layers causes the deformation of the actuator. The maximum deformation occurs at the actuator tip. The amount of tip deflection (or force applied if the tip is restrained) is a direct function of the applied potential difference. Therefore, the amount of tip deflection (or applied force) can be accurately calibrated as a function of applied voltage.

These thermal actuators are used to move micro devices, such as ratchets and gear trains. Arrays of thermal actuators can be connected together at their blade tips to multiply the effective force.

The main objective of the analysis is to compute the tip deflection for an applied potential difference across the electrical connection pads. Additional objectives are to:

- Obtain temperature, voltage, and displacement plots
- Animate displacement results
- Determine total current and heat flow.

4.4.1 Summary of Steps

1. Import GDS file.
2. Define material properties and specification.

Poly1 thickness H_{p1}	2.0μm
Poly2 thickness H_{p2}	1.5μm
Oxide	0.75μm
L_{s2}(length of the short beam)	54μm
W_2 (width of the short beam)	24μm
L_{l2}(length of the long beam)	143μm
W_1(width of the long beam)	8μm
L_e(length of the middle connection)	93μm

Resistance of Poly2 ρ_0	20	Ohm.um
Resistance of Poly1	10	Ohm.um
Thermal conduction of air	$0.026*10^{-6}$	$w.um^{-1}C^{-1}$
Thermal conduction of poly	$41*10^{-6}$	$w.um^{-1}C^{-1}$
Young's modulus	$169*10^{9}$	Pa
Poisson's ratio	0.22	
Thermal conduction of sio_2	$1.4*10^{-6}$	$w.um^{-1}C^{-1}$
Substrate temprature	27°C	

Table 4.3 Model parameters for the simulation

3. Mesh the model.
4. Apply boundary conditions to electrical connection pads for poly2 Layers.
5. Solve the solution.
6. Plot temperature results.
7. Plot voltage results.
8. Plot displacement results.
9. List total heat flow and current.

In all finite element models the domain (the solid in solid mechanics problems) is divided into a finite number of elements (Procedure called meshing). These elements are connected at points called nodes. In solids models, displacements in each element are directly related to the nodal displacements. The nodal displacements are then related to the strains and the stresses in the elements. The finite element method tries to choose the nodal displacements so that the stresses are in equilibrium (approximately) with the applied loads. The nodal displacements must also be consistent with any constraints on the motion of the structure.

The meshing results about 16450 finite elements, which counts about the accuracy of the simulation result.

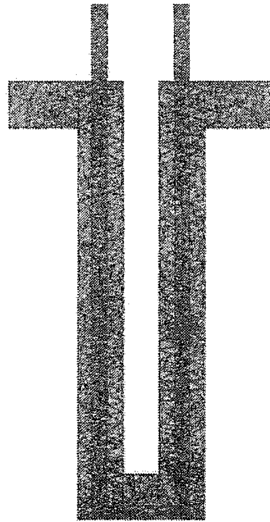


Figure 4.22 meshing of the actuator

Apply load, which is 4 volt between the two pads of the poly2 Layer and the voltage distribution along the beam are got. The red end Is 4 volt while the blue part is ground (0 volt).

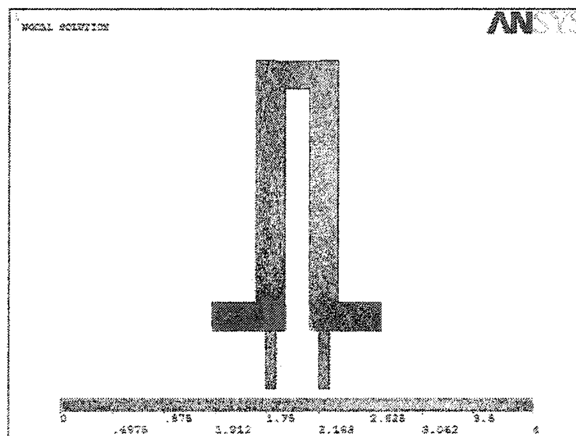


Figure4.23 Voltage distribution along Poly2 layer (0 to 4)

The current in the poly2 layer generate heating and the temperature distribution is got as figure 4.24. The structure of the

beam is symmetrical and so the temperature is also symmetrical. The highest temperature is in the middle of long beam of the poly2 layer.

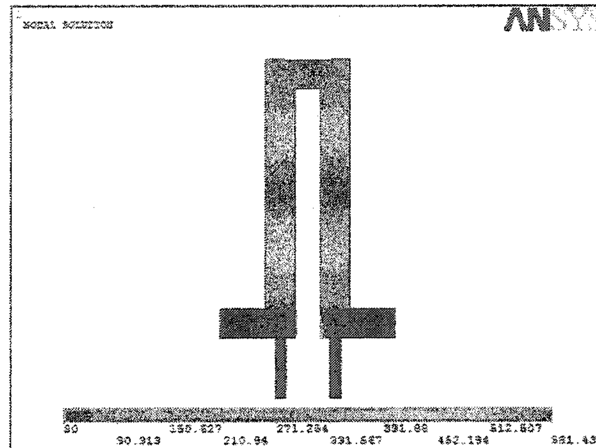


Figure 4.24 Temperature distribution (°C)

The highest temperature is around the middle of the long beam of Poly2 layer that is around 581.5°C.

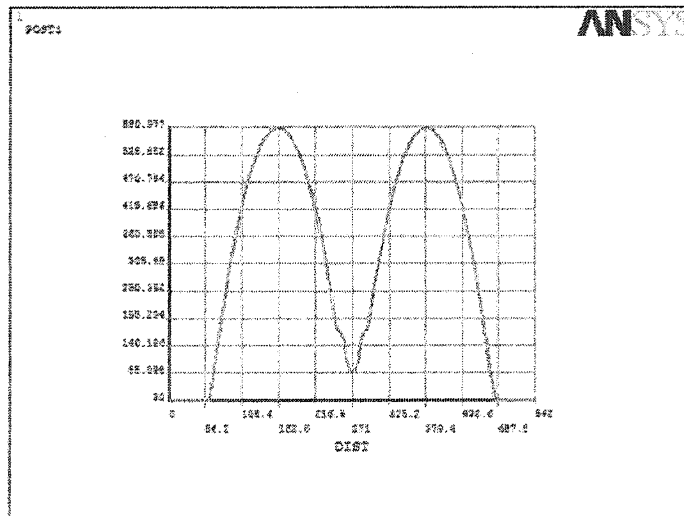
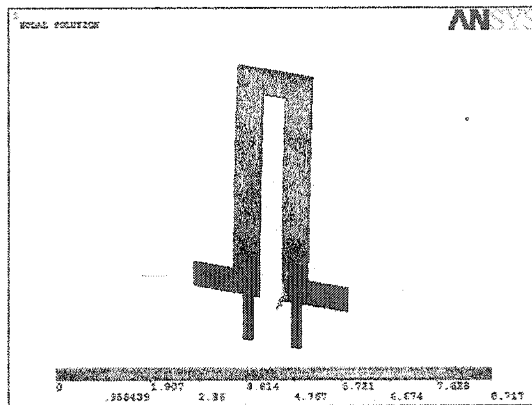
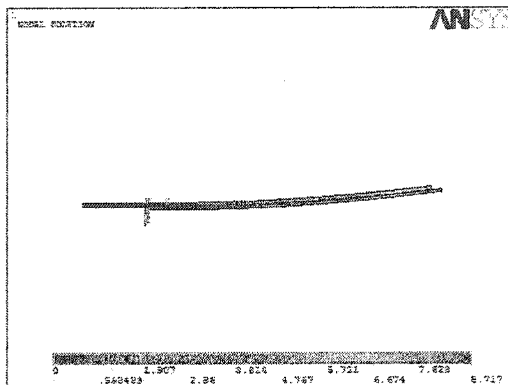


Figure 4.25 Temperature distributions along Poly2 layer

The total length of the beam is 542μm and the lowest temperature is 30°C and the temperature is symmetrically distributed along the beam and it increase first and then decrease to about 85°C which is in the middle of the connection part of the two long beam of poly2 layer.





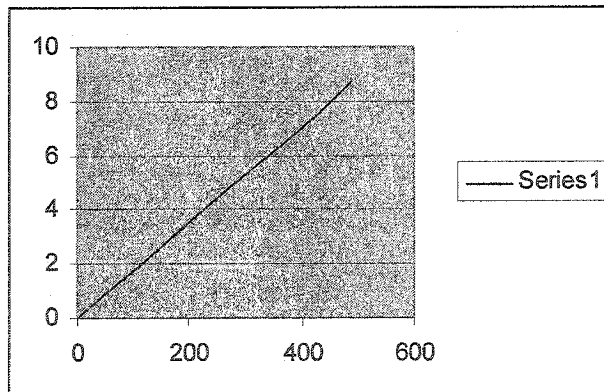


Figure 4.26 Displacement on the z direction of the actuator (X: Different Position of the beam Unit: μm Y: Displacement along the z direction Unit: μm)

An almost linearly relationship of the displacement was got along the beam. The tip deformed around 8 μm. This result was got without connected with the capacitor plate that is why a big displacement was got.

Chapter 5

Experiment Result

5.1 Device preparation for etching

Material and facility: Arch 6501 Photo resist and developer Arch6512

Quintal 162-47(Aligner and UV exposure)

HF: 49%

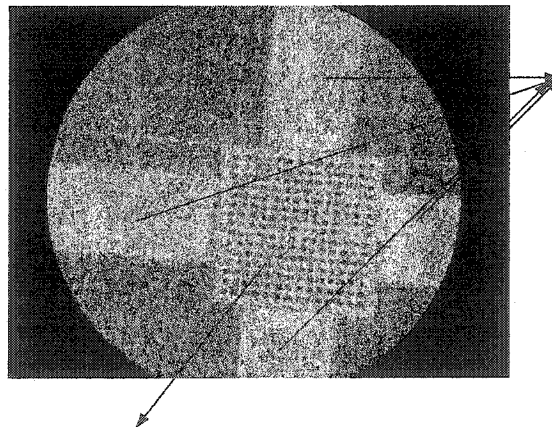
NH4F:40%

Spinner

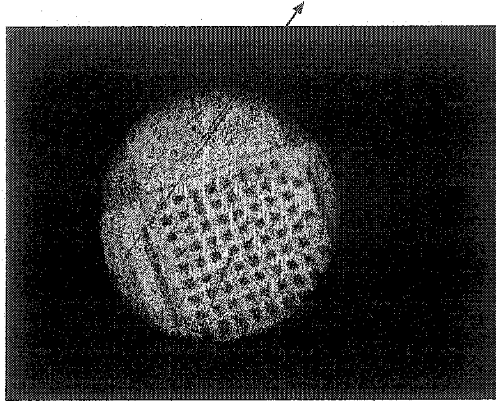
CMOSP35 technology fabricated device: CACDCCS

Procedure:

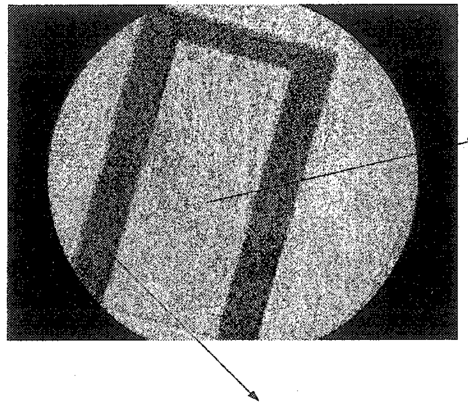
1. Wash the die by De-Ionization water and dry by nitrogen gas; put the die in the oven around 200 ±5°C for about 30minutes, to prepare the surface of the die for photo resist application. This operation promotes adhesion of the photo resist by evaporation any moisture present on the surface of the die.



5.1 (a) Capacitor with actuator before experiment



(b)Capacitor Plate and actuaor



(c)Thermo actuator

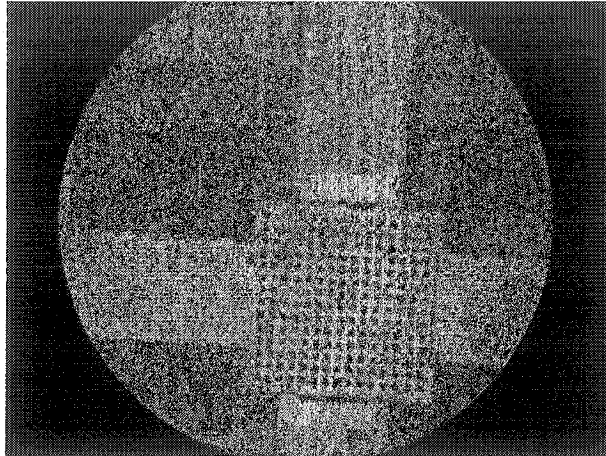
Figure 5.1 Device under microscope before experiment

2. Spinning the positive photo resist onto the die

First, glue (using wax) the die to a thin glass (cleaned using nitrogen gas) for the spinning. Align the die onto chuck so as to have the center of gravity at the midpoint of the chuck.

Drop three drops of photo resist on top of the die for 12 seconds while set the velocity of the spinner at 4150RPM.

3. Soft bake for 1minute at 90°C



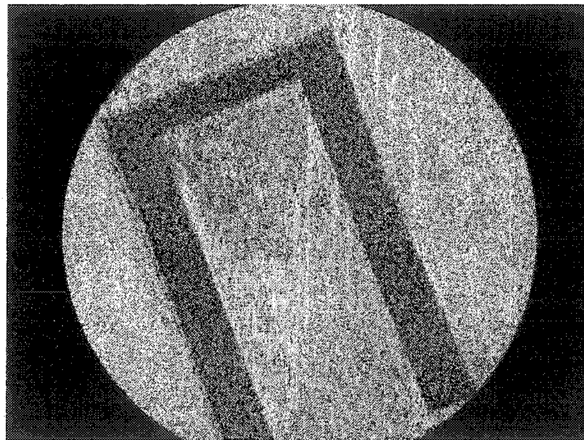


Figure 5.2 Device after a layer of Photo resist

After the photo resist, the whole die exhibit a color of soft pink on it. This makes it easier to see if the part of developed photo resist for the etching area is well done or not.

4: Photolithography

The die is exposed by the UV light for 20 seconds properly (Quintel 162-47) corporation.

5: Put the die in the developer for 1.5 minutes, the rinse by the DI water, if not properly developed, repeat the developer for another 1 minute.

5: Hard bake

Put the device in the oven for 3 to 5 minutes while set the oven at 125°C. Now the device is ready for the isotropic etching.

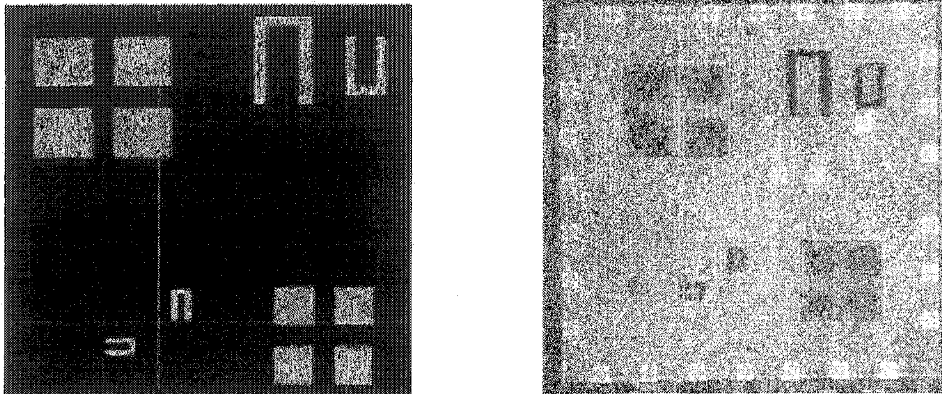


Figure 5.3 the mask used during the photolithography compared with the die

The mask is designed so the actuator and capacitor plate are protected by the photo resist during the HF etching. All the black area in the right figure is exposed to the HF etching. The silicon oxide is kept surrounded the plate and actuator. The polysilicon can be protected later from the TMAH etching.

5.2 Isotropic etching by HF

Purpose: To remove the areas of silicon dioxide unprotected by Photo resist and thereby expose the silicon underneath. [26]

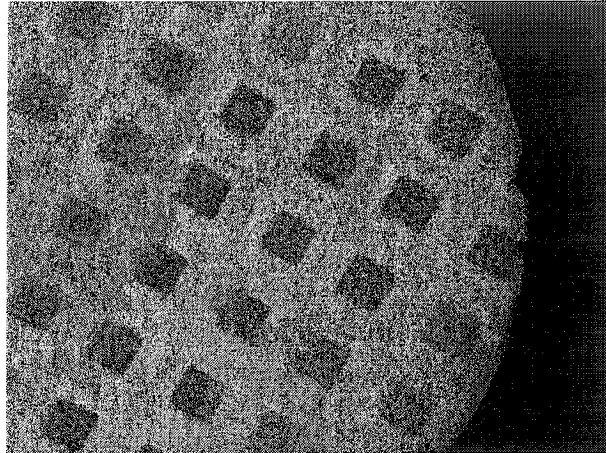
Preparation and Precaution:

1. HF etching should be started within 30 minutes of the completion of Hard bake.
2. Prepare a fresh Buffered Oxide Etch (BOE) solution (6 parts 40% NH4F And 2 parts 49% HF)

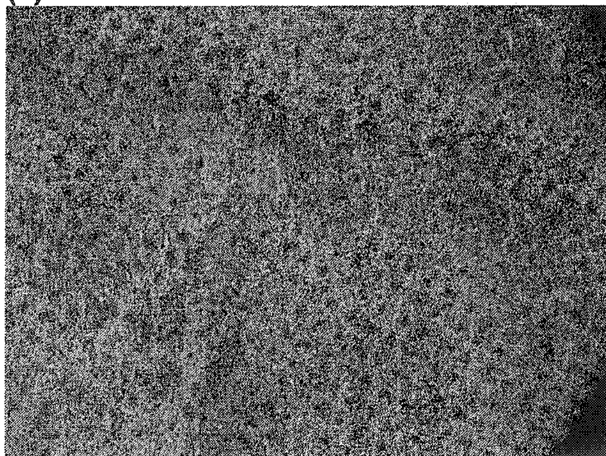
   2.1 Always use plastic beakers and graduated cylinders for enchants

Containing HF because HF etches glass!

2.2 Add HF into NH4F instead of NH4F into HF.



(a) The Plate area



(b) The open area

Figure 5.4 the sample was etched in BHF for Nine minutes.

The small open area in the open area was still clear. This

Means that the device is not ready for TMAH etching yet.

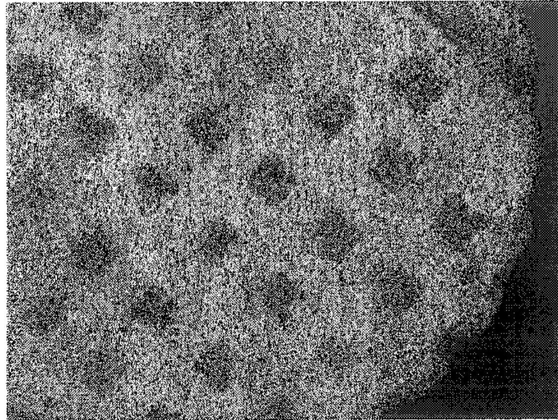


Figure 5.5: The sample was etched about 5 minutes in 6:1 BHF.

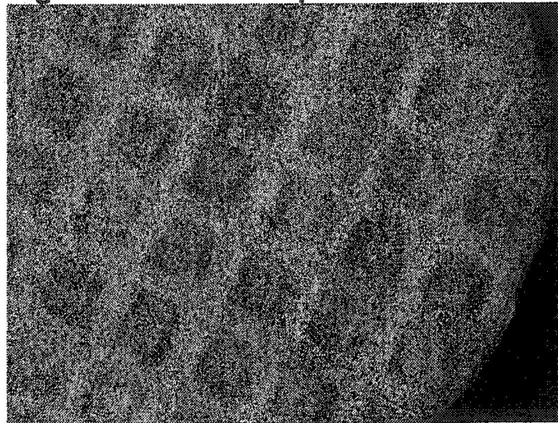
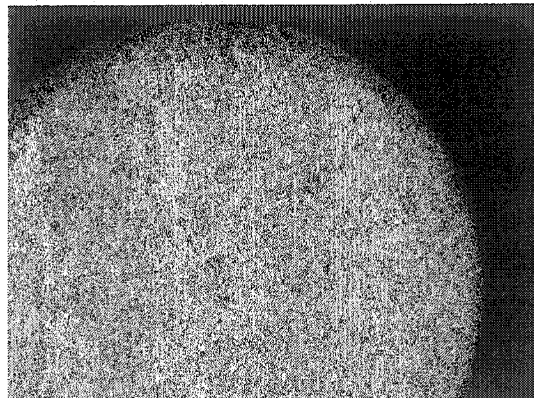


Figure 5.6 the device was in the BHF for about 8.5 minutes

Here the pictures showed the color changes in the area of the varactor plate area.



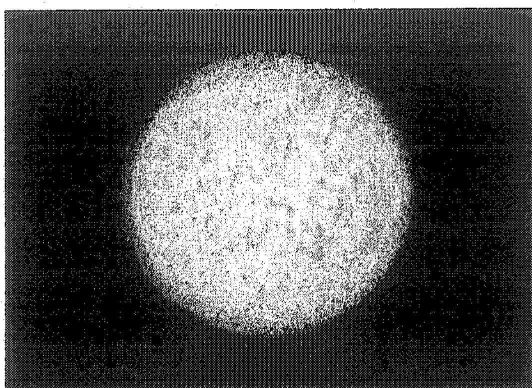


Figure 5.7 the device was etched 14.5 minutes in 6:1 BHF

Now the open area is ready for the TMAH etching.

One picture of the whole capacitor is here after the HF etching, the work was not continued before the TMAH to keep a little bit oxide to protect the varactor plate - Polysilicon.

Together, the die was in the 3:1 BHF for about 9 minutes, 6:1 BHF for 14.5 minutes.

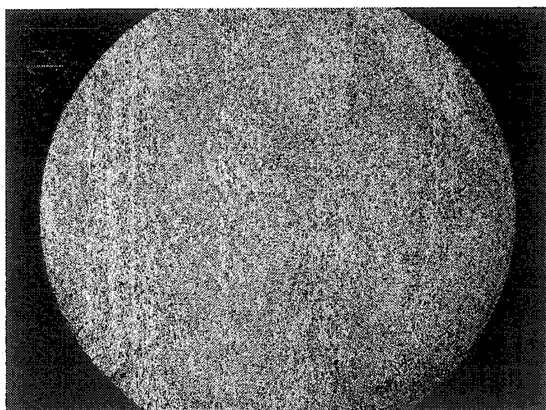
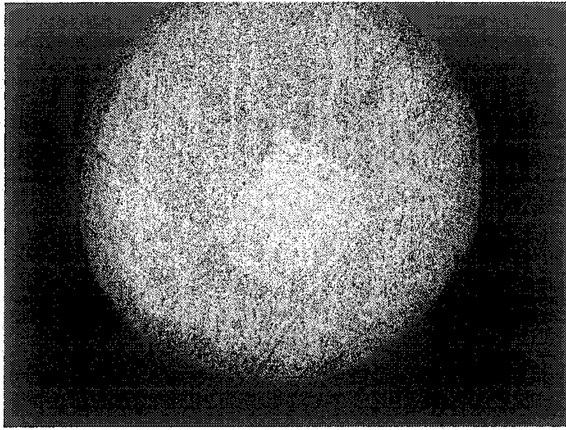


Figure 5.8 a whole varactor picture after the HF etching.

5.3 Anisotropic etching by TMAH

1: The die was put in the BHF (6:1) for 30 seconds, right after this; it was put in the TMAH for 1.5 hour at 30 degrees.



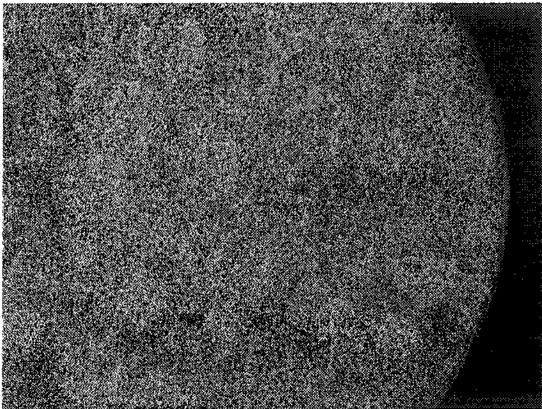
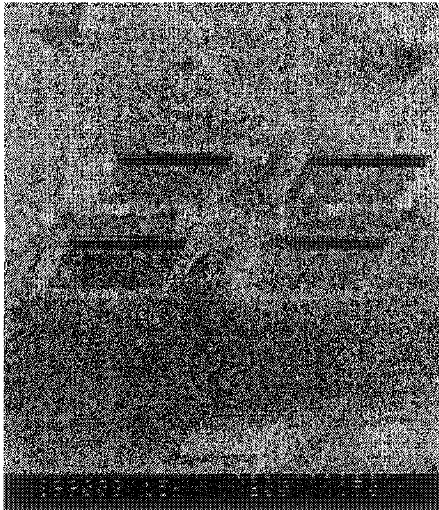


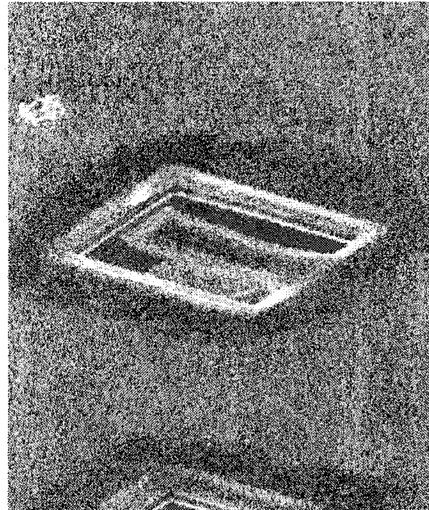
Figure 5.9 Device after put in the TMAH at 30°C for 1.5 hour

Another 2 hours 60 degrees in TMAH. Pictures in SEM, the silicon in (100) direction are etched around 5 to 7 um while it seems stop in the (111) direction under the beam.

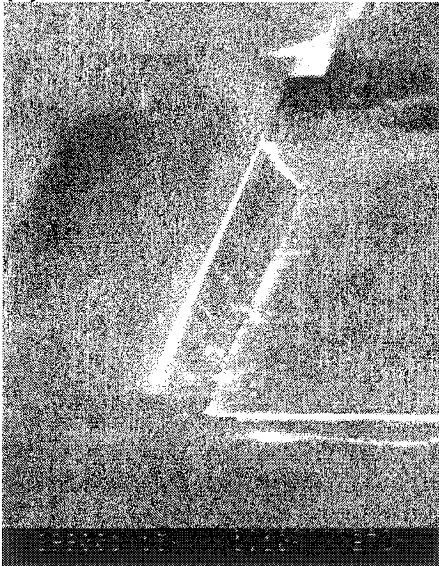
Poly2 layer is etched away and silicon oxide and poly1 still exist since there is oxide around poly 1 layer. (Next time, the sample should be put in the TMAH earlier when there was enough protection for the poly2 layer.



(a) The capacitor



(b) The part released actuator beam



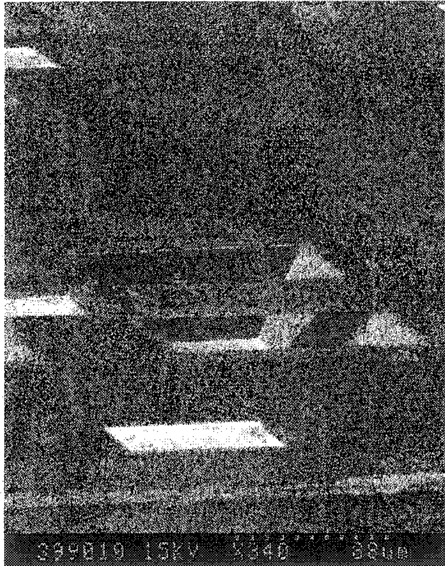
(c) The corner of the capacitor

(d) Part released varactor

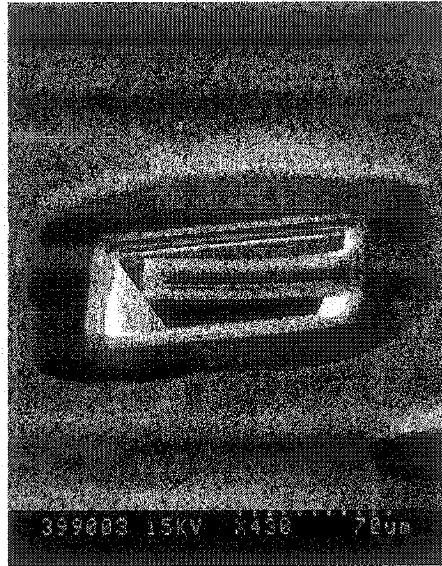
Figure 5.10 Device SEM picture after first step release

As now, the separately designed actuator is almost released while the Silicon under the beam of the actuator of the varactor is stopped under the beam with (111) plane. At the same time, a corner of the varactor is also released.

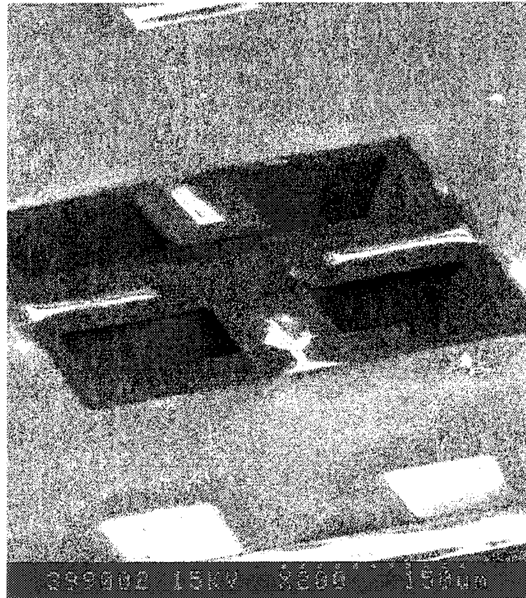
Another 2 hours in the TMAH, the beam is released.



(a)Released varactor beam



(b) completely released actuator



(c) varactor with two beam released

Figure 5.11 SEM pictures of finally release devices

5.4 Problems and remedies during etching

1. The die is too tiny (2000µm*2000µm) which makes it impossible to be put on the spinner directly. It is also very easy to lose the die if dealing with the device by tweezers for the drying procedure while using the nitrogen gas.

To solve this problem, we glued the die to a piece of thin glass by positive photo resist. The wax can stay for the hard bake that is around 125 degrees and the HF Etching. The wax does not react with developer and HF. That makes it an ideal epoxy for this purpose.

2: The only actuators that are successfully released are the actuators on the upper right corner of figure 5.3. The total etch time in the TMAH are around 10 hours at 60 degree (while the standard temperature is 90 degrees for silicon etching). The polysilicon can stay within this temperature and etching time limit.

3: It is hard to know the etching velocity since there are so many tiny holes, which are originally designed to make the HF etching faster. But this turned out to slow the etching because the holes are filled with photo resist which is not solvable in the HF solution.

4. To help with the protection of the circuit during the HF etching, the die is put in the oven for hard bake that is supposed to be 3 to 5 minutes. But the photo resist will be lift up after long time etching in the HF.

For this reason we kept the die stay in the oven for about 10 minutes, which helped the photo, resist stay in HF longer.

5. The etching stops in the <111> direction of the wafer which makes it hard to release the capacitor plate. To solve this problem, we need to have another open area on the beam near the capacitor plate to expose the <114> and <113> direction to the TMAH to etch the silicon and releases the structure completely.

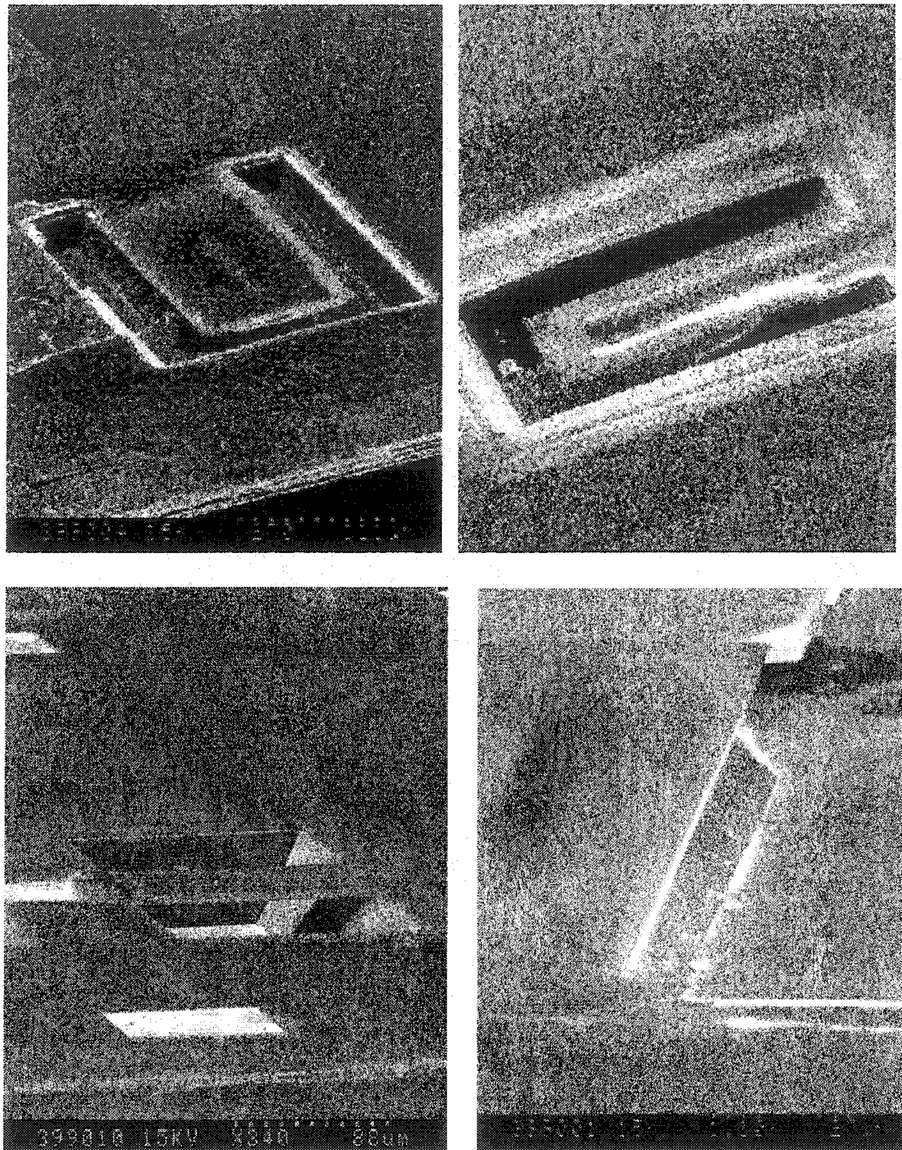


Figure 5.12 Released beams of the varactor and part of its plate area.

5.5 The test facility for the released actuator.

The test facility is composed of a micromanipulator with microscope, DC power supply, and RMS multimeter as figure 5.13

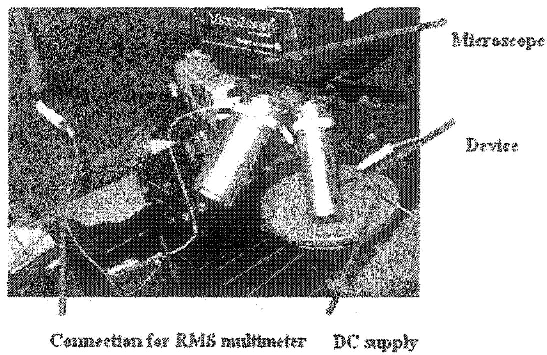


Figure 5.13 Test equipment

5.6 Test result

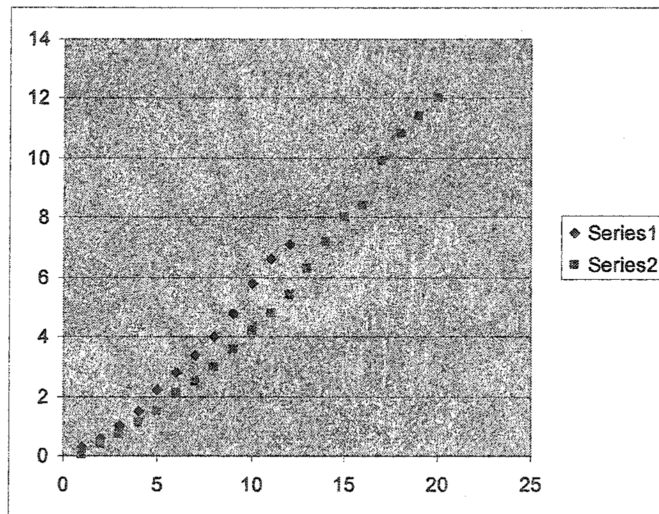


Figure 5.14 Voltage and current relationship (V, mA)

The X direction is voltage that is from zero to about 20 volt while the Y direction is the current; the unit for the current is mille ampere. The resistivity for the actuator beam is around 2500Ω.

Chapter 6

6.1 Conclusions

To realize a completely CMOS technology compatible RF device (mature process for IC) to reduce the cost of assembly and packaging; we tried to fabricate a capacitor using the two layer of polysilicon. The capacitor is actuated by vertical electrothemal actuators, which can move up and down in two directions. The actuators are successfully released; the substrate under it was completely etched away by timing the etching time in TMAH. The actuator is tested and the voltage and current relationship was obtained.

There are a few modifications are needed to be done in order to complete the device fabrication.

1) The open areas to etch silicon under the membrane should be redesigned or use the XeF2 isotropic etching to help the etching of silicon under the capacitor plate.

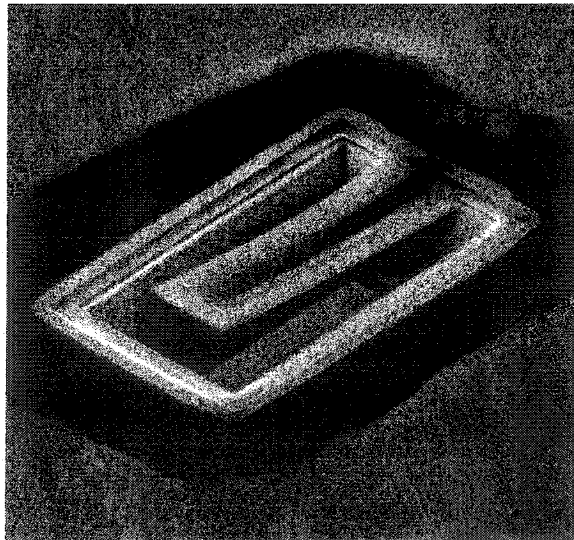


Figure 6.1 a properly released electro thermal actuator

To get the actuator properly released before damaging of the beam of the actuators.

2) How to control precisely the post processing to get the same predefined deformation.

3) There are constraints in the design for the opening of the cavity, which is limited by the design rules. This greatly slows down the SiO_2 etching before put TMAH etching. This happened because CMOS Is not a process designed for MEMS devices. This is important because long time in the HF destroy the positive photo resist and makes it difficult to control the silicon oxide, which we want to keep during the TMAH etching.

6.2 Contributions

This is the first tunable capacitor fabricated by the Polysilicon layers using cmos35 technology. The electro thermal actuator works by the expansion of one of the polysilicon layers(poly1 or poly2). The two actuators are connected together by the silicon oxide which also works as the thermal insulator.

To our best knowledge, it is the first time that electro thermal actuators can move up and down which are connected together by the silicon oxide layer.

This helps the research of RF IC system fabricated completely on a chip without further assembly and packaging.

6.3 Suggestions for future works

I believe that successfully fabricated CMOS process compatible capacitor can realize low packaging cost and superior performance. It always deserves more attention to study the design, fabrication and post processing.

In many RF applications, many discrete, board level components significantly increase assembly cost and overall size, as well as limiting performance.

Now, many researchers are focused on the development of the MEMS technology to achieve universal access to information to realize the seamless, efficient, secure and cost-effective connectivity for information appliances operation within and among the various spheres of consumer activities: (1) the home and office (2) the ground fixed/mobile platform, and (3) the space platform.

One of the important factors is the realization of the high- quality factor, large tuning range varactors.

Another way is to employ the flip chip technology. The device is fabricated by MUMPs which is designed specially for MEMS devices. PolyMUMPs is an extremely flexible process allowing for many types of users and design ideas. The process consists of a non-patternable nitride isolation layer, a polysilicon ground (plane) layer, two structural polysilicon layers, two oxide release layers, and one metal layer for electrical connection and reflectivity enhancement.

Flip chip describes the method of electrically connecting the die to the package carrier. The package carrier, either substrate or lead frame, then provides the connection from the die to the exterior of the package. In "standard" packaging, the interconnection between the die and the carrier is made using wire. The die is attached to the carrier face up, and then a wire is bonded first to the die, then looped and bonded to the carrier. Wires are typically 1-5 mm in length, and 25-35 μm in diameter. In contrast, the interconnection between the die and carrier in flip chip packaging is made

through a conductive "bump" that is placed directly on the die surface. The bumped die is then "flipped over" and placed face down, with the bumps connecting to the carrier directly. A bump is typically 70-100 µm high, and 100-125 µm in diameter.

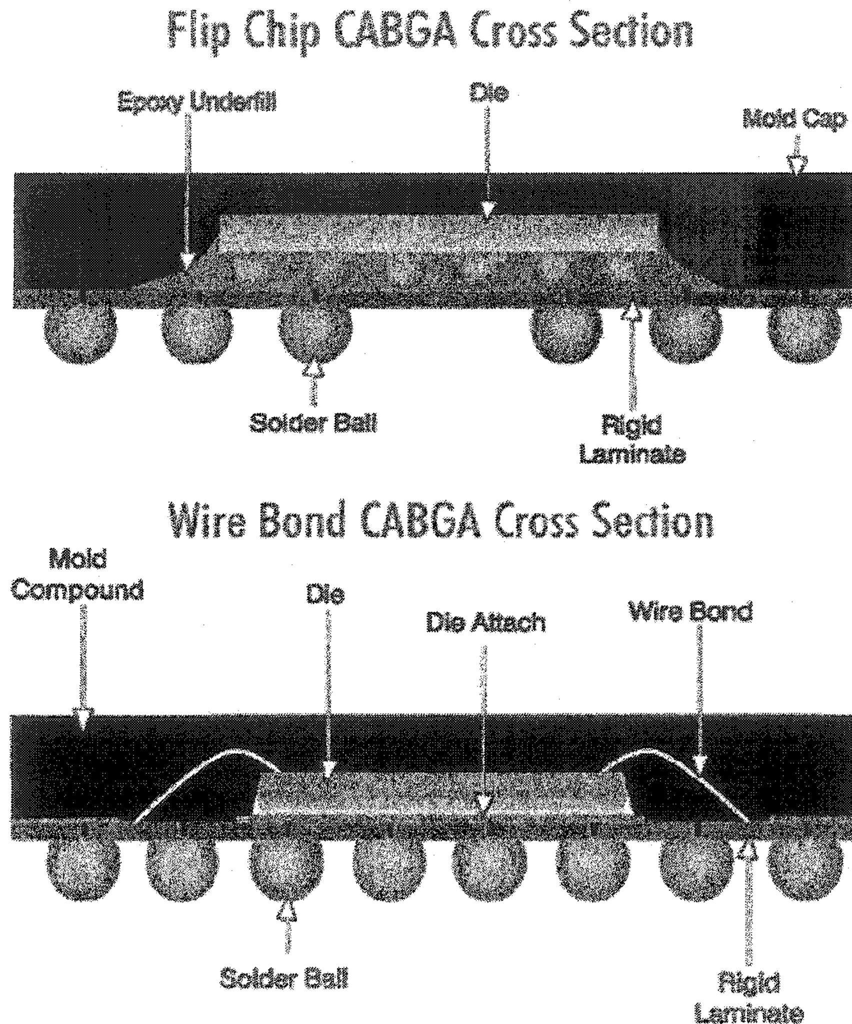


Figure 6.2 Wire bonding and flip chip bonding

Flip chip is a great way to integrate MEMS device with IC die compared with wiring bonding technology. The loss through wire is greatly decreased and the device is even securer than wire bonding.

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E-mail: jjyao@rsc.rockwell.com