Fin and Island Isolation of AlGaN/GaN HFETs and Temperature-dependent Modeling of Drain Current Characteristics of AlGaN/GaN HFETs

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ABSTRACT

Fin and Island Isolation of AlGaN/GaN HFETs and Temperature-dependent Modeling of Drain Current Characteristics of AlGaN/GaN HFETs

Bandar AlOtaibi

Over the past two decades AlGaN/GaN Heterostructure Field Effect Transistors (HFETs) have been the target of many studies on their suitability for high-power and high-temperature applications. Due to the sizable inherent polarization effects, present in these heterostructure-based devices, the built-in sheet charge density at the AlGaN/GaN heterointerface is remarkably high, which makes these devices fall into the category of the depletion-mode field effect transistors. Despite the suitability of this wide-bandgap material system for switching power applications, the depletion-mode character of these HFETs has been acting as an obstacle against the adoption of AlGaN/GaN HFETs to these applications. As a result, a vibrant research on the development of techniques capable of reliably changing the depletion-mode character of AlGaN/GaN HFETs into an enhancement-mode character is currently being pursued by many investigators. Towards this end, the proposed approach of this thesis has been based on modifying the piezoelectric component of the polarization sheet charge density through studying its correlation with the size of the isolation mesa.

The impact of the size of the isolation-mesa on the sweeping- and pulsed-mode drain current-voltage characteristics of AlGaN/GaN HFETs has been studied. Investigations reveal that while by implementing AlGaN/GaN HFETs on array of islands or mesas of smaller dimensions, rather than one continuous-mesa, same values for the maximum drain current level can be maintained, pinch-off voltage can be made less negative. Also,

it is shown that the maximum gate transconductance is improved by island-type isolation. In addition, it is shown that the proportionally larger surface area available for power dissipation in fin- and island-isolated HFETs can reduce the impact of self-heating on AlGaN/GaN HFETs.

Modeling the drain current of AlGaN/GaN HFETs at high-temperature ambient was also another objective of this thesis. A Monte Carlo-based temperature-dependent mobility model, with incorporation of steady-state velocity overshoot, is employed in modeling the drain current-voltage characteristics of AlGaN/GaN HFETs at 300, 400, and 500K. One of the major merits of this model is that it employs a very small set of fitting parameters. The model takes into account the temperature-dependence of the electron transport through the gated-channel of an AlGaN/GaN HFET and also its access regions. This model is validated with regards to the experimentally measured drain current characteristics. Results confirm that the temperature dependency of the drift electron velocity is the cause of the degradation of drain current at elevated temperatures.

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Chapter 1

Introduction

1.1 Material properties of III-Nitride

III-Nitride semiconductors (i.e. InN, GaN, AlN, and their ternary alloys) are promising candidates for many high-power, high-frequency, and high-temperature electronic applications [1-2]. This is a consequence of their wide bandgap, large peak value of the electron drift-velocity, the very wide steady-state overshoot in the drift-velocity versus electric-field (i.e. v_d-E) characteristics, and high breakdown electric-field. Additionally, the widely tuneable bandgap of ternary III-Nitride alloys can cover a very broad range of absorption and emission characteristic wave-lengths from infrared to the ultraviolet, which make them superb choices for electronic and optoelectronic devices (e.g. light emitting diodes, laser diodes, and photo detectors) [3].

Due to the polar nature of III-Nitride heterostructures, two-dimensional channels of extremely high carrier concentrations (i.e. of the order of 10^{13} cm^{-2}) are formed at the III-Nitride heterointerfaces, without the need for any intentional doping [4]. The drift-velocity versus electric-field characteristics of GaN, not unlike other III-V semiconductors, is shown to possess an overshoot at moderate values of electric-field and a saturating characteristic at higher electric-fields. However, this overshoot pattern is remarkably wider and taller than that of the other III-V semiconductors of interest. The large peak electron velocity, wide velocity overshoot, and thermal stability of GaN have favoured GaN over GaAs, especially at lower microwave frequency and higher power applications [4-5]. Figure 1.1 shows a comparison of electron drift-velocity versus electric-field characteristics of GaN with three other major semiconductors (i.e. Si, GaAs, and SiC) [6].

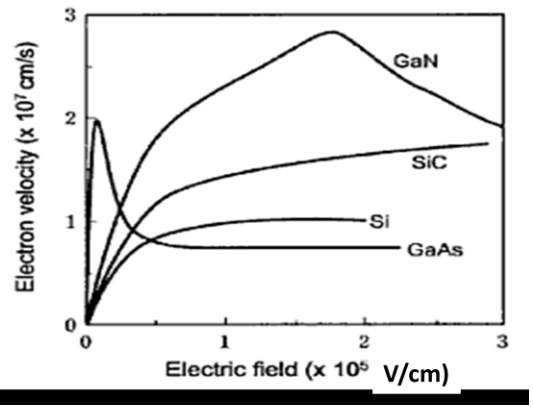


Figure 1.1: Electron drift transport characteristics of Si, SiC, GaAs, and GaN [6].

Among the major semiconductors presented in Figure 1.1, GaN has the widest energy bandgap and the highest breakdown electric-field. This makes this semiconductor very suitable for the channel of high voltage FETs. Table 1.1 compares the bandgap energy, electron mobility (μ_n), breakdown field (E_b), and electron saturation velocity (v_{sat}) of GaN to these other major semiconductors. Although GaN has a considerably lower electron mobility than GaAs, its higher and wider steady-state velocity overshoot and higher saturation velocity serve as compensating factors towards providing competitive current density and power gain at moderate frequencies.

Table 1.1: Comparison of material properties between GaN, Si, GaAs, and SiC at 300K [7].

Material	**Si**	**GaAs**	**4H-SiC**	**GaN**
E_g (eV)	1.1	1.42	3.26	3.39
μ_n (cm^2/Vs)	1350	8500	700	900
E_b (10^6 V/cm)	0.3	0.4	3	3.3
v_{sat} (10^7 cm/s)	1.0	2.0	2.0	2.5

1.2 Spontaneous polarization in GaN

III-Nitride semiconductors can be grown in two different crystalline forms: Zinc blende (Zb) and Wurtzite (Wz) [5]. The Wurtzite structure, which has a hexagonal unit cell, is the most studied form of III-Nitrides. This is due to the extraordinary polar properties of III-Nitrides in this crystalline form. Due to the non-centrosymmetric nature of these Wurtzite crystals, a very large spontaneous polarization is built into the as grown crystal. The value of the spontaneous polarization of GaN is in the order of 3MV/cm [8].

Improvement of such a large component of the spontaneous polarization in the Wurtzite crystals of III-Nitrides is observed along the material order of GaN to InN, and to AlN [8].

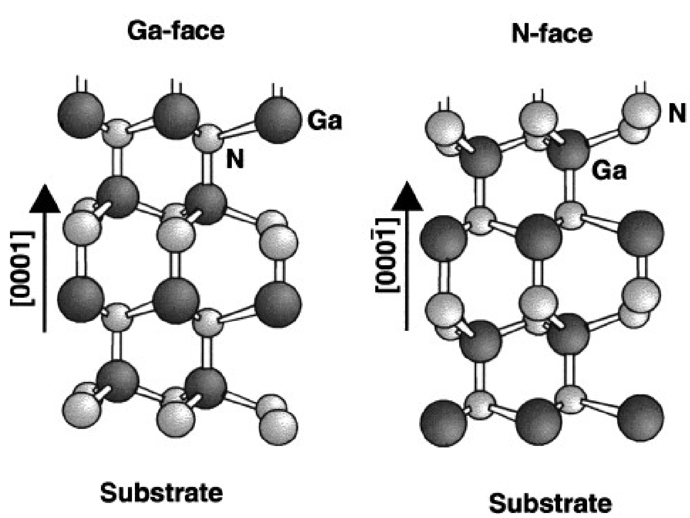


Figure 1.2: A stick-and-ball diagram of hexagonal crystalline structure of GaN in Ga-face and N-face [4].

The growth technique of GaN has been found to bear the possibly of determining the direction of the aforementioned spontaneous polarization vector [4]. This direction is dependent on the face of the grown crystal. Due to the lack of lattice-matched substrates, III-Nitrides are often grown on c-plane Sapphire or SiC substrates. The crystal can either be grown in metallic-face (which is also known as Ga-face) or N-face. As shown in Figure 1.2, the face of the crystal is determined by the type of the atoms of which the topmost layer of the grown crystal is composed. Using the MOVPE (Metal Organic Vapor Phase Epitaxy) growth technique, the Ga-face is observed to be the dominant face [4]. The direction of the spontaneous polarization vector of Ga-face III-Nitride crystals points toward the substrate, while perpendicular to it. In the N-face crystals, spontaneous polarization vector points toward the surface [4].

1.3 AlGaN/GaN Heterostructure Field Effect Transistor (HFET)

In HFETs, the barrier layer, which separates the gate electrode from the channel, is often composed of a wide-bandgap semiconductor (i.e. AlGaN in the case of AlGaN/GaN HFET). The conduction band bending at the heterointerface between the wide-bandgap barrier layer, and the smaller bandgap channel layer results in the formation of a two dimensional electron gas (i.e. 2DEG) at the triangular quantum well, created at the channel-side of the interface (i.e. GaN-side). This is illustrated in Figure 1.3. In this figure, E_1 and E_2 represent the first and second subbands of the triangular quantum well. The flow-path of the drain current of a properly designed HFET is restricted to this quantum well.

In non-polar HFETs, the 2DEG is formed by the transfer of electrons from the intentionally doped barrier to the triangular quantum well. In contrast, the 2DEG of polar

III-Nitride HFETs is formed dominantly due to the polar nature of the AlGaN/GaN heterointerface. The induction of the polarization charge at this heterointerface is partly the result of the mismatch of the spontaneous polarization of the barrier and the channel layer. These two layers despite the uniqueness of the direction of their polarization vectors have different values of polarization. As a result of the polarization imbalance at the heterointerface, formation of the 2DEG at the GaN-side of the heterointerface will become necessary [9-10]. This polar 2DEG is observed to form even in the absence of intentional doping of the barrier.

In addition to the polarization induced at the heterointerface by the discontinuity of the spontaneous polarization of GaN and AlGaN, the lattice mismatch of the barrier and the channel layer is the cause of another polarization component. Due to the smaller value of the lateral lattice constant of AlGaN in comparison to GaN, pseudomorphic growth of AlGaN on top of GaN results in induction of tensile strain at the AlGaN/GaN heterointerface. As a result of this induced strain and existence of large off-diagonal elements in the strain tensor of III-Nitrides, piezoelectric polarization to the extent comparable to the spontaneous polarization, and of the same direction, will be formed at the AlGaN/GaN heterointerface [4]. This is shown in Figure 1.4. The combined impact of the piezoelectric effect and the spontaneous polarization results in formation of 2DEG with densities exceeding 10^{13} cm^{-2}.

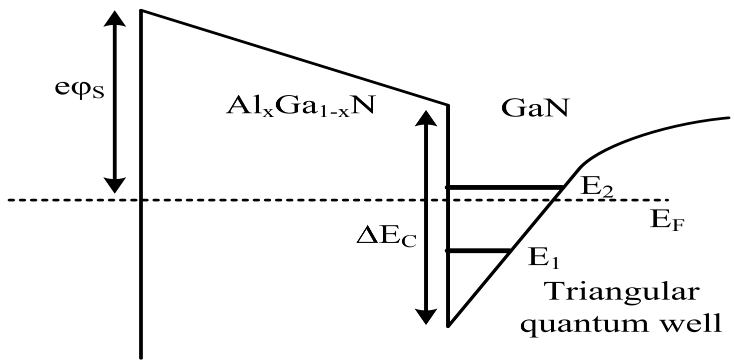


Figure 1.3: Schematic drawing of the conduction band structure of AlGaN/GaN HFET. $e\varphi_s$ is the Schottky barrier height at the metal-AlGaN interface and ΔE_c is the conduction band discontinuity at the AlGaN/GaN heterointerface.

In HFETs, the source and drain electrodes are directly connected to the 2DEG via alloyed Ohmic contacts. The Ohmic contacts are often formed by rapid thermal annealing of a stack of different electron-beam evaporated metals (e.g. Ti/Al/Ti/Au), to ensure Ohmic access to the 2DEG channel. The Schottky gate electrode is located on top of the barrier, between the source and the drain electrodes, to modulate the current passing through the heterointerface. Figure 1.5 shows a simple schematic structure of an AlGaN/GaN HFET. In order to extend the breakdown voltage of HFETs, source and drain electrodes are defined with an offset with regards to the gate. As a result, the channel of an HFET is composed of two access regions (for which the surface of the barrier layer is exposed to air) and a gated HFET (for which the barrier surface is covered by the gate metal). As shown in Figure 1.5, in order to increase the electron mobility at the heterointerface, a very thin layer of AlN is often sandwiched between the GaN channel and the AlGaN barrier-layer. Thus, the remote electron scattering caused by the ionized impurities of the barrier-layer will be eliminated [5].

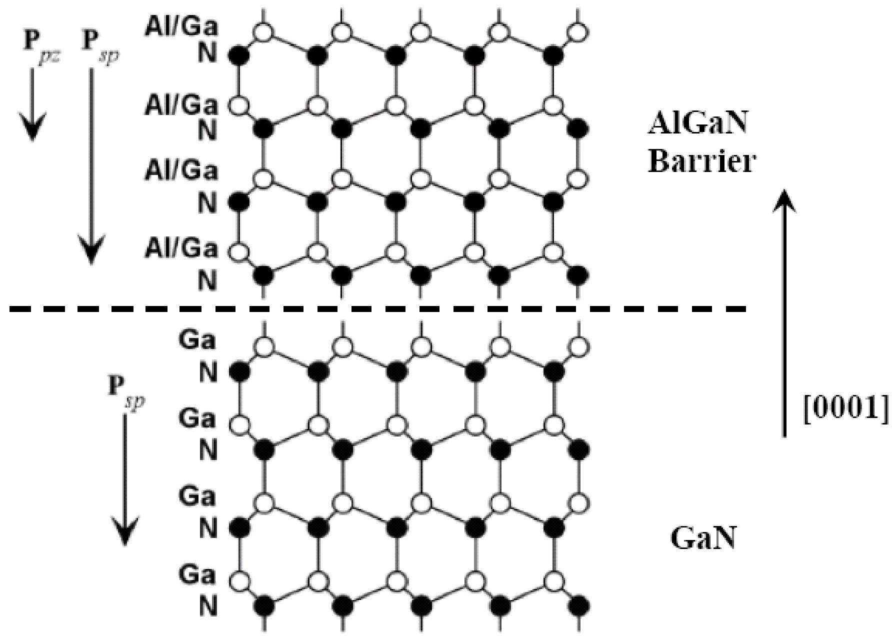


Figure 1.4: Spontaneous and piezoelectric polarization in AlGaN/GaN HFET [11]. $\mathbf{P}_{sp}$ and $\mathbf{P}_{pz}$ stand for spontaneous and piezoelectric polarization vectors, respectively.

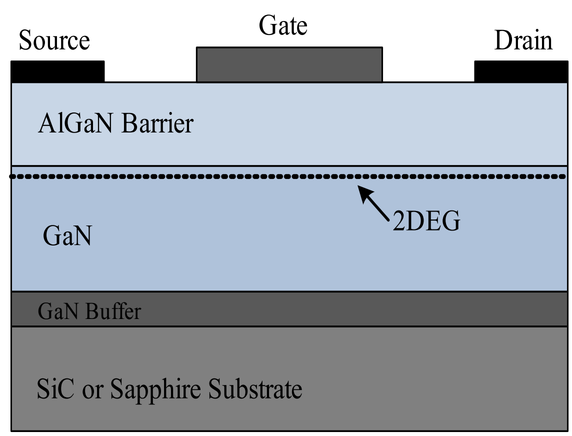


Figure 1.5: Schematic drawing of the basic structure of an AlGaN/GaN HFET.

1.3.1 Polarization engineering in AlGaN/GaN HFET

As it was mentioned earlier, the concentration of the induced 2DEG to the triangular quantum well of AlGaN/GaN HFET is dominantly controlled by the piezoelectric effect and the mismatch in the spontaneous polarization of AlGaN and GaN. As result, engineering these components of inherent polarization are the dominant factors in controlling the 2DEG concentration and current-drive of AlGaN/GaN HFETs. These factors are also invaluable in exerting control over the threshold voltage of AlGaN/GaN HFETs.

Due to the large values of 2DEG densities induced to the polar AlGaN/GaN heterointerfaces, the threshold-voltage of these devices is often negative, resulting in realization of depletion-mode (or, normally-on) FETs. However, in many applications the presence of normally-on devices results in insupportable energy expenditure in the standby mode. As a result, an ongoing research is being pursued in terms of producing Enhancement-mode (or, normally-off) AlGaN/GaN HFETs with positive values of threshold voltage, or even devices of less-negative values of threshold-voltage.

As a result of the dominance of the polarization fields in defining the 2DEG concentration of AlGaN/GaN HFETs, the required level of control exerted towards positive-shifting of the threshold-voltage is expected to be realizable by means of engineering the polarization. While both spontaneous and piezoelectric polarizations can be reduced by reducing the Al-composition of the AlGaN barrier (and essentially bringing the material properties of the channel and the barrier layer more towards one another), such an HFET design will heavily suffer in terms of the gate leakage current through the low Al-composition $Al_xGa_{1-x}N$ barrier layer. As a result, other avenues of engineering the polarization are pursued in Chapter 2 of this thesis.

1.3.2 Performance of AlGaN/GaN HFETs in high-temperature ambient

The low generation rate of thermally-induced carriers and the high thermal conductivity of GaN and AlGaN, turn AlGaN/GaN HFETs to suitable transistors for high-temperature applications (e.g. in automotive, aircraft, and aerospace applications) [12-15]. It should also be mentioned that AlGaN/GaN HFETs have shown considerable thermal stability. In addition, it is known that the steady-state velocity overshoot and the saturation electron drift velocity of GaN are less affected by the temperature increase in comparison with GaAs [16]. Adding to these suitable material characteristics, the recent developments of techniques of Ohmic contact formation and surface treatments of AlGaN/GaN HFETs have also led to substantial improvements in the high-temperature reliability of these contacts [17-18].

AlGaN/GaN HFETs fabricated on SiC substrates show greater potential in terms of thermal stability, due to the high thermal conductivity of SiC [19]. It is shown that low-field electron mobility of the 2DEG is enhanced by the higher thermal conductivity of the Si substrate in comparison to Sapphire (which is the other widely used substrate in AlGaN/GaN technology) [20].

The aforementioned factors lead to the popularity of AlGaN/GaN HFETs for high-temperature applications. In addition, AlGaN/GaN HFETs fabricated on SiC substrates can be integrated on-chip with the other high-temperature integrated systems. As a result, developing a model for predicting the temperature dependency of the drain current-voltage (i.e. I_D-V_D) characteristics of these devices is of prime importance in improvising better device design strategies. This is done in Chapter 3.

1.4 Overview of thesis

In Chapter 2 of the thesis a novel design strategy based on engineering the piezoelectric polarization at the AlGaN/GaN heterointerface is proposed and experimentally investigated. Preliminary results of this investigation show that the proposed strain engineering technique, which is based on the application of small size isolation mesas to the fabrication of AlGaN/GaN HFETs, bears the possibility of positive shifting the value of the threshold-voltage.

In Chapter 3, a manageable analytical model for modeling the drain current-voltage characteristics of AlGaN/GN HFETs at elevated temperatures is proposed and validated with regards to the experimentally measured characteristics.

Chapter 4 includes the conclusions of this work and draws a few suggested directions for the future work in this area.

Chapter 2

Fin and Island Isolation of AlGaN/GaN HFETs*

2.1 Abstract

Traditionally AlGaN/GaN HFETs are fabricated on mesas, etched well into the heterojunctions, to avoid the crosstalk between neighboring devices fabricated on the same chip. In here, for the first time, effect of the size-variation of the isolation mesas of AlGaN/GaN HFETs on their drain current characteristics is studied. In this study, the isolation mesas of the fabricated devices include three varieties: narrow mesas (i.e. 16x40 μm^2 fins), array of very small size mesas (i.e. 16x7 μm^2 islands), and traditionally-sized mesas (i.e. 100x100 μm^2). AlGaN/GaN HFETs of the aforementioned isolation-mesa sizes are investigated in terms of their DC and pulsed measurement characteristics. Results show a correlation between the pinch-off voltage and the size of the isolation mesa. The pinch-off voltage is observed to become less negative by the reduction of the size of the individual mesas. All of the fabricated devices have peak extrinsic gate transconductance values greater than 220 mS/mm. The

* Based on a paper published in May 2011 issue of the IEEE Transaction on Electron Devices.

island-isolated HFETs show merits in terms of relatively higher gate transconductance and less thermal effect.

2.2 Introduction

The natural crystalline form of III-Nitrides is the hexagonal crystal structure of Wurtzite. Wurtzite structure is the crystalline form with the highest degree of symmetry in correlation with the formation of spontaneous polarization. It is observed that the increase in Wurtzite crystal non-ideality from GaN to AlN reflects itself through an increase in the spontaneous polarization [21]. Also, for this crystalline type, the piezoelectric tensor possesses three sizable non-vanishing independent components. These two polarization components of almost identical strength (i.e. in the order of 2-3 MV/cm) are the main sources of two dimensional electron gas (2DEG) formation associated with the divergence of the polarization in space [4].

The spontaneous polarization is dictated through the difference in crystalline non-ideality of the channel and the barrier layer and as a result engineering its value is restricted by the conduction-band discontinuity requirement of HFETs. However, engineering of the piezoelectric polarization term provides an available venue for charge control.

Due to the importance of the role of piezoelectric polarization in determining the 2DEG concentration of polar AlGaN/GaN HFETs, selective engineering of the piezoelectric polarization is for the first time studied. This is done through investigating the impact of the size of the isolation mesa on the DC characteristics.

2.3 Fabrication techniques for enhancement-mode AlGaN/GaN HFETs

In the depletion-mode n-type FETs, the drain-current has a finite value when the gate-source voltage is zero. As a result, for turning these devices off a negative voltage should be applied between the gate and source electrodes. On the contrary, for an n-type enhancement-mode FET, the flow of current occurs only when a positive gate-source voltage is applied. In order to avoid any unnecessary power consumption in the standby mode, enhancement-mode devices are often preferred in switching circuits. Since AlGaN/GaN HFETs are good candidates for high-voltage applications, developing normally-off AlGaN/GaN HFETs for high-voltage switching applications is extremely appealing.

However, as it was discussed in Chapter 1, AlGaN/GaN HFETs due to their extremely high values of sheet charge density fall into the depletion-mode category. Over the years a few techniques have been proposed for the conversion of this depletion-mode characteristic into an enhancement-mode characteristic. A few of these techniques including "gate-recess" and "fluorine-ion bombardment" are briefly reviewed in this section.

The "gate-recess" technique of realization of enhancement-mode AlGaN/GaN HFETs relies on the partial removal of the thickness of the barrier under the gate electrode. This thinning of the barrier essentially results in depletion of the 2DEG concentration due to the charge depleting effect of the Schottky gate. A few of the important unwanted side-effects of this process are the damage of the dry etching to the surface of the mesa and also the increase in the gate-leakage through the thinned barrier [22-23].

Employing fluorine-based reactive ion etching (RIE) for “implanting fluorine ions” into the barrier is the other major technique for the fabrication of enhancement-mode AlGaN/GaN HFETs [24]. The implanted negatively charged fluorine ion concentration in the AlGaN barrier serves to deplete the channel from the polar 2DEG and as a result causes a positive shift in the pinch-off voltage. However, the resulting surface damage of this bombardment process and also the chance for redistribution of these ions under high electric-field and high-temperature operation conditions indicate reliability concerns for this fabrication technique.

Also a less popular solution for realization of enhancement-mode AlGaN/GaN HFETs relies on the incorporation of a p-type GaN cap layer, sandwiched between the gate electrode and the AlGaN barrier [25]. In this technique, the positive shift achieved in pinch-off voltage of AlGaN/GaN HFETs is the result of the formation of the depletion region of the pn-junction under the gate electrode. The difficulty of achieving p-type doping of GaN is one of the major hassles of this fabrication technique. These AlGaN/GaN HFETs are also indicating large values of gate leakage current.

In this study and for the first time, a different avenue has been taken to obtain a positive shift in the pinch-off voltage of AlGaN/GaN HFETs by the means of strain-engineering. This technique seems to have the capacity of offering normally-on and normally-off AlGaN/GaN HFETs on the same chip without exposing the active area of the sample to any type of reactive ion etching.

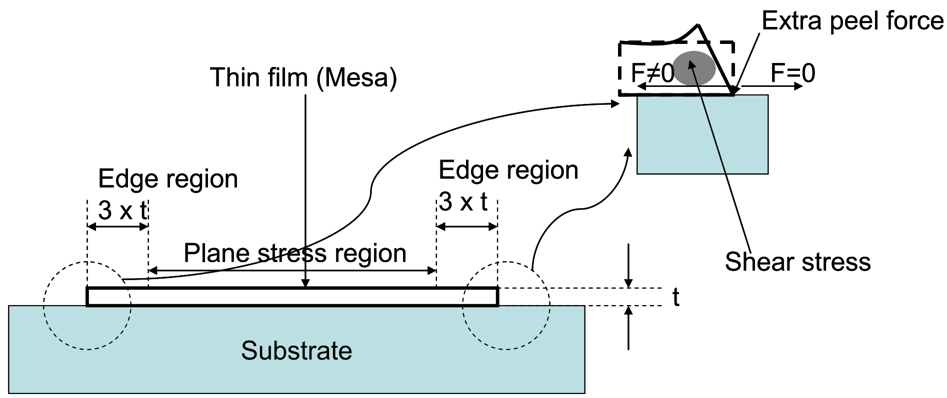


Figure 2.1: Formation of peel forces at the edges of a tensile strained thin film.

It is typically established that the pseudomorphic growth of a crystalline thin film on a thick substrate of a different lattice constant and/or a different thermal expansion coefficient introduces some in-plane strain. In regions apart from the edge by a distance in the order of three times the film thickness almost all the stress lies in-plane, while a smaller in-plane stress is developed at the edge regions [26]. The edge regions possess a complex distribution of shear stress, which is due to transition from the free side to the side with in-plane stress. The discontinuity of the stress at the heterojunction around the edge region, through a phenomenon known as “stress concentration”, leads to an extra force component called “peel force” (Figure 2.1) [26]. The existence of the peel forces and the reduced in-plane strain at the edge regions are expected to reduce the piezoelectric polarization at these parts. This effect has already been investigated in other technologies including SiGe [27-32]. In those material systems, experimental results and theoretical calculations demonstrate that the reduction in mesa size can substantially reduce the built-in strain and depending on the proportion of mesa's vertical and lateral dimensions, this effect can be appreciable even at the center of the epilayer [28].

2.4 Experimental results and discussion

2.4.1 Device structure and characterization

Devices have been fabricated on an AlGaN/GaN HFET structure of Al-composition of 0.3, grown on SiC substrate. The thickness of AlGaN barrier is 20 nm and a 1 nm AlN spacer layer has been sandwiched between this layer and the channel. The thickness of the unintentionally doped GaN channel layer is 200 nm, which was grown on a stack of 2 μm carbon-doped GaN isolation layer and a 20 nm thick AlN nucleation layer (Figure 2.2). Mesa isolation was performed by the use of chlorine-based reactive ion etching. The height of the isolation features is about 300 nm.

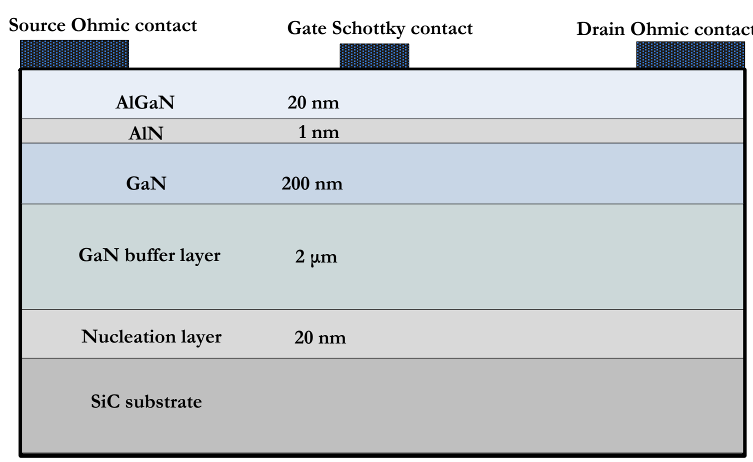


Figure 2.2: Schematic cross-section of the fabricated AlGaN/GaN HFETs.

Device fabrication was carried out by CMC. Device design according to the process flow of this foundry has been performed as part of this project. The process-flow of the device fabrication starts with mesa isolation of 300 nm height, Ohmic contact deposition, and rapid thermal annealing. Following these steps, interconnect deposition, and gate-electrode deposition are carried out in this order. After this step, devices have been passivated by a SiN film. Finally, openings through this dielectric layer have been created for electrical access to the drain-, source-, and gate-pads.

Three types of two-finger HFETs, with different sizes of isolation mesa, have been fabricated side by side one another. The first category of devices were fabricated on mesas of size 100x100 μm^2, the second group of devices were fabricated on long small size mesas of size 16x40 μm^2, referred to as fin (Figure 2.3), and the third category of devices were fabricated on islands of size 16x7 μm^2 (Figure 2.4). As for the island type devices, in order to maintain same value of current-drive an array of islands have been connected together. Figure 2.5 shows micrographs of fin- and island-isolated HFETs. All the explored devices have a gate length of 1 μm, gate-drain spacing of 2 μm, and gate-source spacing of 1.1 μm. The Hall electron mobility of this sample was reported to be about 1000 $cm^2/V.s$ and the 2DEG electron concentration is about 1.7×10^{13} cm^{-2}.

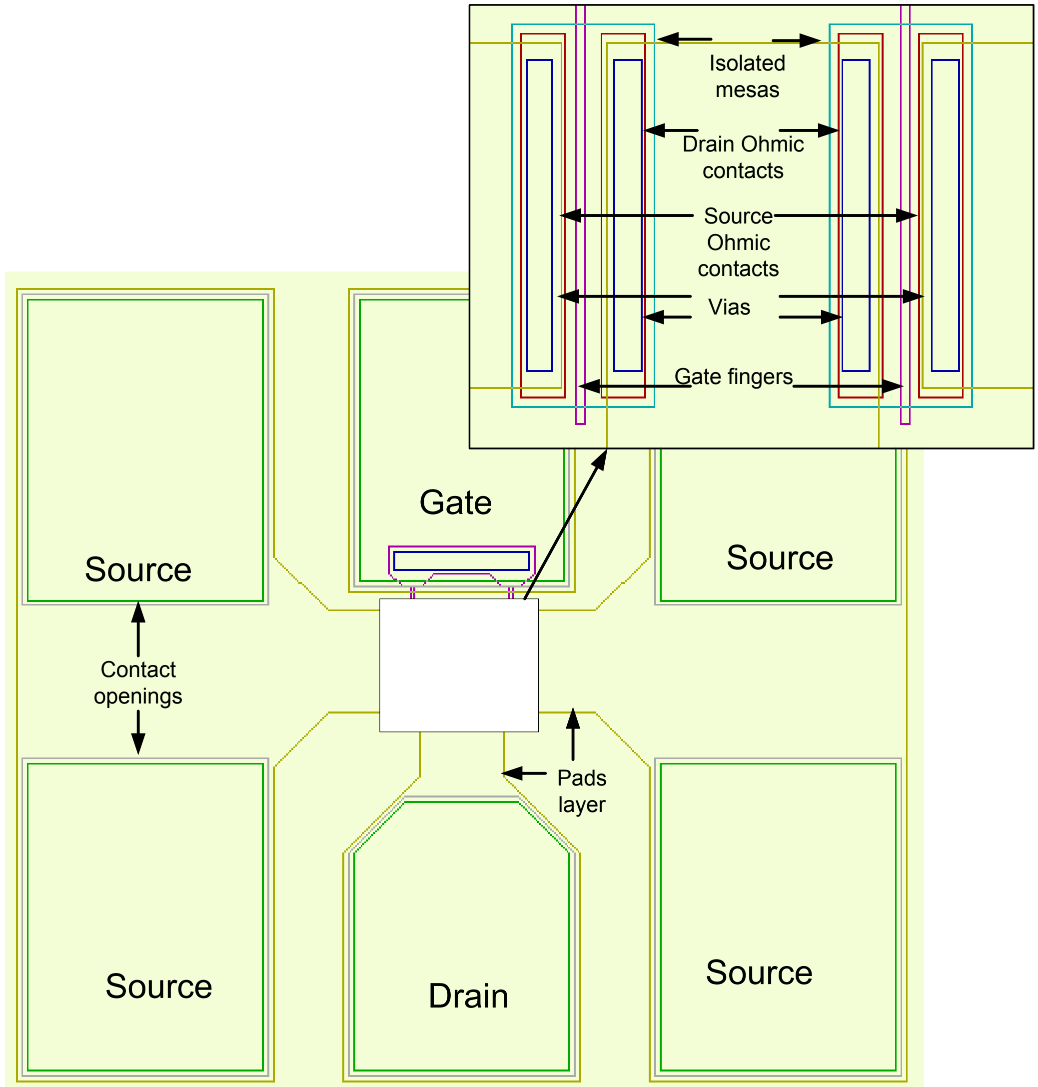


Figure 2.3: Device layout of a two-finger fin-isolated AlGaN/GaN HFET with micro-strip interconnects.

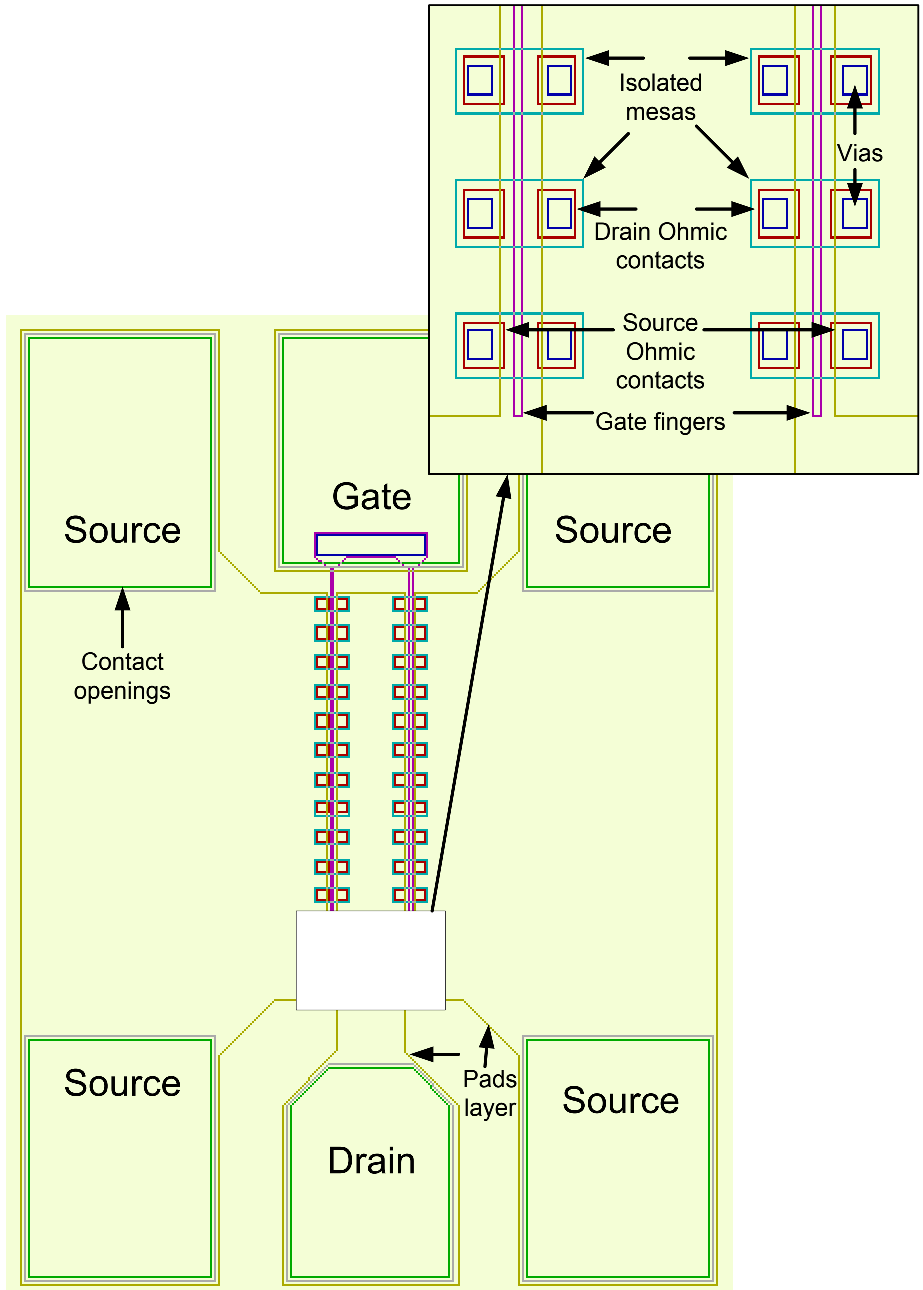
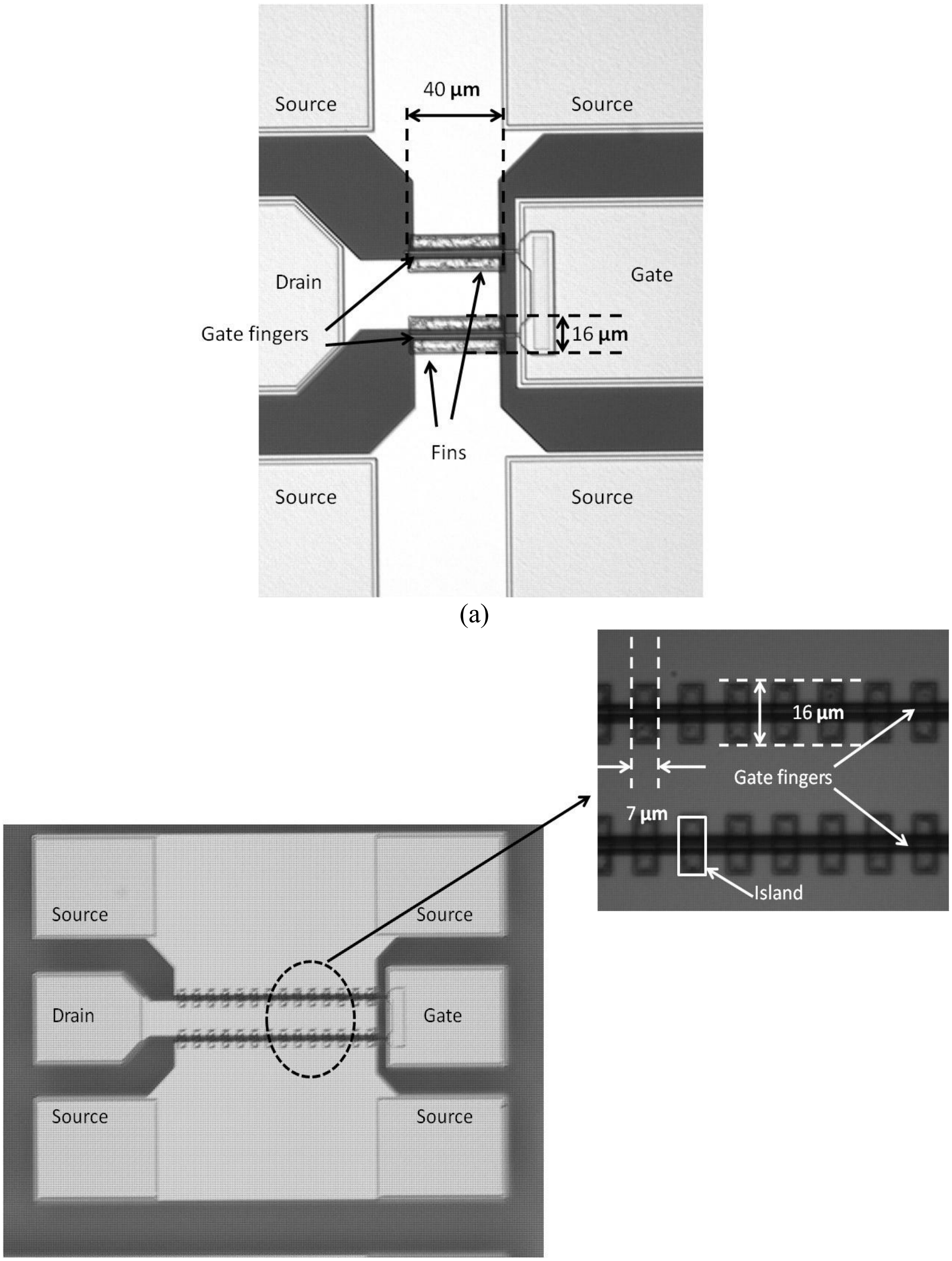


Figure 2.4: Device layout of a two-finger island-isolated AlGaN/GaN HFET with micro-strip interconnects.



(b)

Figure 2.5: Micrographs of the fin-isolated HFET (a), and the island-isolated HFET (b).

2.4.2 Discussion

A Keithley semiconductor parameter analyzer was used for the measurements reported in this section. Measurement results of Figure 2.6 illustrate that the pinch-off voltage becomes less negative as the size of the mesa is reduced from 100x100 μm^2 to 16x40 μm^2, and to 16x7 μm^2. The maximum value of extrinsic gate-transconductance per unit-width of the transistors remains almost the same for mesa- and fin-isolated device types. However, wrapping the gate electrode on two sides of the islands is observed to have increased the gate-transconductance of the island-isolated devices with respect to the other two device types.

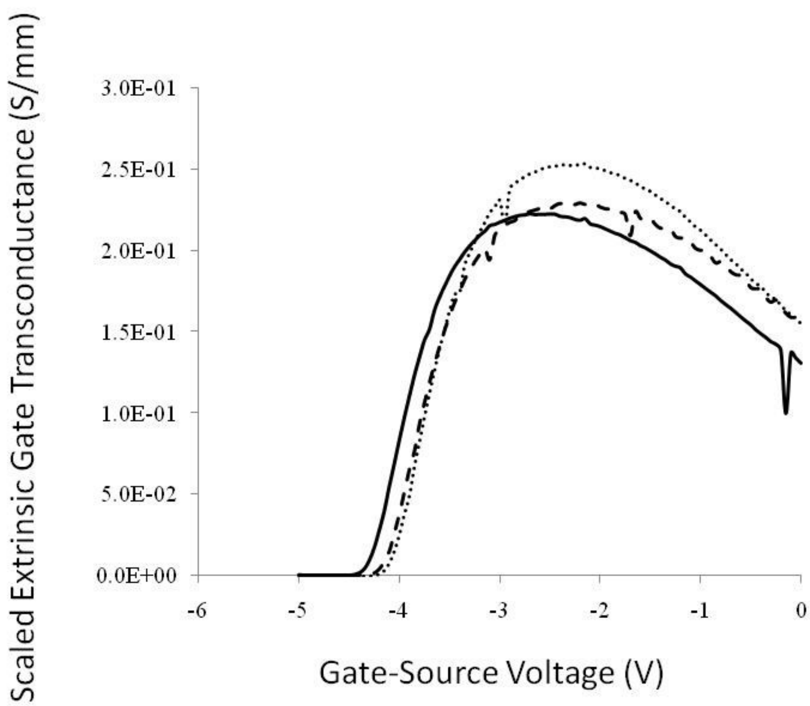


Figure 2.6: Scaled extrinsic gate transconductance versus gate-source voltage for mesa- (continuous), fin- (dashed), and island-isolated (dotted) devices. V_{DS} is equal to 5V.

Scatter plots of the pinch-off voltages of 15 devices from each of the three device categories is presented in Figure 2.7. These devices have been chosen from different areas of the wafer. The largely overlapping scatter plots of the pinch-off voltages of the island- and fin-isolated HFETs, rule out the presence of a fundamental difference between these values. However, Figure 2.7 clearly shows that a fundamental difference between the pinch-off mechanism of the mesa-isolated devices and the other two device types is present. As a result of the non-overlapping scatter plots, this difference cannot be explained by the statistical variation of the pinch-off voltage across the sample.

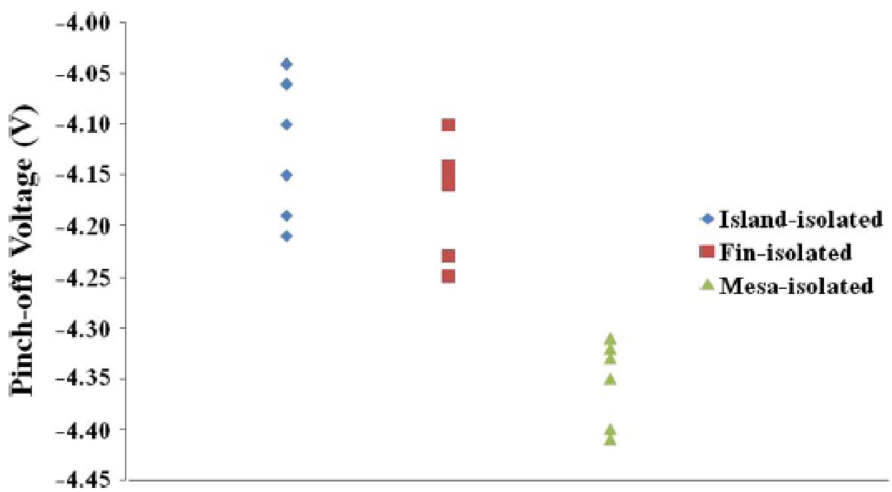


Figure 2.7: Scatter plot of the variation of the pinch-off voltage among the three categories of devices.

Figure 2.8 shows the I_D-V_D and I_G-V_D characteristics of three typical devices (one from each category). The knee voltage and the drain-current density remains almost the same for all three types of devices. Figure 2.8 also indicates that among the three device varieties the mesa-isolated HFET demonstrates the most thermal effect. This is observed through the reduction of drain-current at higher drain-voltages for less negative gate-source voltages. Confirming this observation, the pulsed I/V measurements of mesa-isolated HFETs show a higher output resistance in the saturation operation regime of these devices in the aforementioned bias range. This is due to the presence of proportionally larger surface area for power dissipation in fin- and island-isolated devices, in comparison to the mesa-isolated HFETs of the same gate-width.

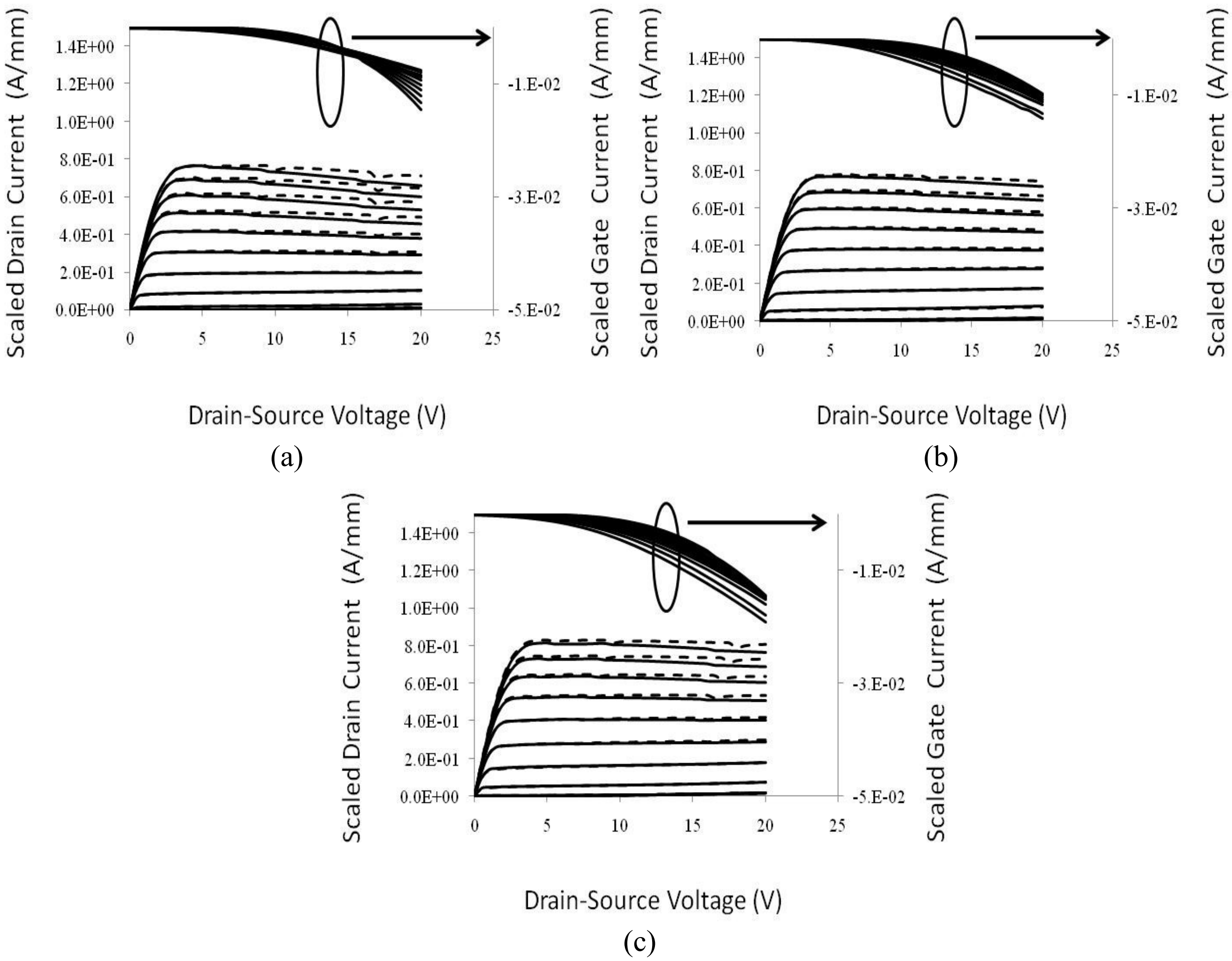


Figure 2.8: Scaled drain- and gate-current versus drain-source voltage, for a typical mesa-isolated HFET (a), fin-isolated HFET (b), and island-isolated HFET (c). On all these figures pulsed drain current values are indicated in dashed lines. V_{GS} is changed from -5 to 0 V, in steps of 0.5 V.

With further reduction of the size of the isolation mesa and the use of compliant substrate schemes in heterostructure growth, it is believed that the observed trends can be further enhanced. The compliant substrate is predicted to act as a decoupling mechanism between the induced strain on the channel GaN layer by the substrate and the barrier layer. This has been theoretically shown to be able to further enhance the relaxation of strain through lateral definition of mesa [28]. This type of polarization engineering is expected to be able to considerably shift the pinch-off voltage of AlGaN/GaN HFETs as the size of isolation mesa reduces to the order of six-times the mesa height [27-32]. To maintain the same current-drive, these devices can be fabricated through employing a large number of islands rather than one single mesa. The minimum size of the islands reported in here has been defined by the constraints of the foundry.

2.5 Conclusion

Two new types of isolation structures for AlGaN/GaN HFETs were introduced: fin- and island-isolation. A correlation between the size of the isolation feature and the pinch-off voltage of AlGaN/GaN HFETs was observed. These results indicate a positive shift in the pinch-off voltage with the reduction of the size of the isolation feature. For the island-isolated AlGaN/GaN HFETs, the gate transconductance is observed to be relatively higher. Also, it is observed that island-isolation results in better thermal behavior of the HFET.

Chapter 3

Investigation of the Impact of Temperature Dependency of Drift Transport Characteristics on the Drain Current of AlGaN/GaN HEFTs

3.1 Abstract

A Monte Carlo-based temperature dependent mobility model, with incorporation of steady-state velocity overshoot, is employed in modeling the drain current-voltage characteristics of AlGaN/GaN HFETs at 300, 400, and 500K. One of the major merits of this model is that it employs a very small set of fitting parameters. The modeled drain current-voltage characteristics have been successfully matched to the experimental characteristics at the aforementioned temperatures. While a brief measurement at these temperatures is believed to be of no meaningful consequence on the quality of the metal-semiconductor contacts, this matching confirms that the temperature dependency of the drift electron velocity is the culprit of degradation of drain current at elevated temperatures.

3.2 Introduction

Over the past decade, AlGaN/GaN HFETs have drawn much attention, due to their great potentials for high power, high frequency, and high temperature applications [2], [15]. The wide bandgap, large peak value of the electron drift-velocity, the very wide steady-state overshoot in the drift-velocity versus electric-field (i.e. v_d-E) characteristics of GaN, in addition to the unprecedented values of polar sheet-carrier concentrations (i.e. of the order of 10^{13} cm^{-2}) at the pseudomorphically grown AlGaN/GaN heterointerfaces, turn these devices into great choices for high power microwave signal amplification [33].

The recent major advances in epitaxial growth [34-35], Ohmic contact formation [17-18], and other device fabrication steps of III-Nitride HFETs have led to an increasing need for modeling the behavior of these novel devices [12], [36-40]. In such an endeavor, the particular attributes of transport through these 2DEG channels ought to be fully included in modeling. Due to the suitability of these devices for high temperature applications, developing a model for predicting the temperature dependency of the drain current-voltage (i.e. I_D-V_D) characteristics is of prime importance.

In the present work, by incorporation of the temperature dependency of the v_d-E characteristics of the 2DEG channel of AlGaN/GaN HFETs, a previously proposed analytically-manageable drift-diffusion –based model of AlGaN/GaN HFETs (i.e. [40]) has been modified to predict the temperature variation of I_D-V_D characteristics. The aforementioned temperature variations of the electron drift transport characteristics of these channels, in line with the predictions of Bhapkar *et al.* [41], are provided by a commercial Monte Carlo-based simulator (i.e. MOCASIM, [42]). The analytical v_d-E expression, required in the device model, has been constrained for yielding the maximum similarity to the Monte Carlo–based predictions, at each temperature. Even though the model has a few fitting parameters, the physical significance of each parameter has been reserved and studied. In addition, in this revision of the work of Loghmany *et al.* [40], the potential drop along the source-access and drain-access regions of the 2DEG channel are more accurately incorporated. These distinctions are indicated in section 3.4.3.

3.3 Temperature dependency of v_d-E characteristics

In obtaining the temperature dependent v_d-E characteristics from MOCASIM, only two of the material parameters of GaN are corrected to match the values referred to in the work of Bhapkar *et al.* [41] and O'Leary *et al.* [16]. These two parameters are the acoustic deformation potential and polar optical phonon energy, for which values of 8.3 eV and 91.2 meV are introduced to MOCASIM (from [41] and [16]), respectively. All of the important scattering mechanisms governing the high-temperature drift transport characteristics through the polar 2DEG channel of the AlGaN/GaN HFETs, including phonon scattering, polar optical phonon scattering, acoustic phonon scattering, ionized impurity scattering, intervalley scattering, and piezoelectric scattering are taken into account by the simulator.

The resulting v_d-E characteristics at 300, 400, and 500K are illustrated in Figure 3.1. In order to substantiate the validity of the predictions of this simulator, these characteristics are compared to a variety of Monte Carlo-based simulations reviewed in the recently published work of Yang *et al.* [43]. Over the same temperature range, this compilation presents identical drift transport characteristics.

The drain current of AlGaN/GaN HFET is the result of electron transport through the 2DEG channel. The two-dimensional confinement nature and the degeneracy of electron population at the heterointerface make the two-dimensional transport of electrons distinguishable from the three-dimensional electron transport through the bulk GaN. However, in support of the application of Monte Carlo-based simulations of v_d-E characteristics, obtained for electron transport in bulk GaN, it should be mentioned that while a meaningful difference is only observed at low electric-fields such an improvement in low-field electron mobility of 2DEG channel is usually compensated for by the degrading effect of interface scattering [44-45]. While such a scattering mechanism impact the electron transport through the 2DEG channels, such an effect is not considered in the simulator. As a result, the adoption of the v_d-E characteristics is sufficiently accurate.

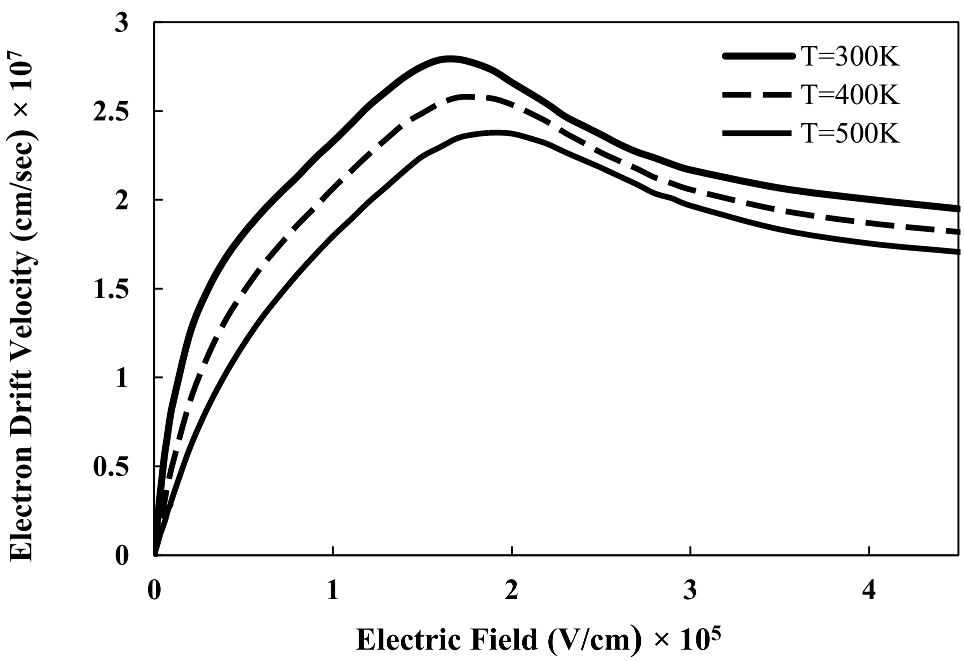


Figure 3.1: Electron drift transport characteristics of GaN at 300, 400, and 500K from MOCASIM.

In order to be able to feed these temperature variable characteristics into the HFET model of Loghmany *et al.* [40] parameters of the analytical mobility model used in that work are tuned for producing the best matched v_d-E characteristics to the Monte Carlo-based drift transport characteristics of Figure 3.1. The aforementioned analytical mobility model is presented as:

$$\nu(E) = \frac{\mu_0 E + \mu_1 E\left(\frac{E}{E_0}\right)^{\alpha} + \nu_{sat}\left(\frac{E}{E_1}\right)^{\beta}}{1 + \left(\frac{E}{E_0}\right)^{\alpha} + \left(\frac{E}{E_1}\right)^{\beta}} \tag{3.1}$$

For best matching to the room-temperature data presented in Figure 3.1, the values of the parameters of (3.1) are extracted using the least mean-square fitting technique. The room-temperature values of these parameters are tabulated in Table 3.1.

Table 3.1: Model parameters of (3.1) at 300K.

Parameter	Description	Value
μ_0	Low-field mobility	1113 $cm^2/(V.s)$
μ_1	High field mobility	128 $cm^2/(V.s)$
E_0	Low electric-field	2.06×10^4 V/cm
E_1	High electric-field	12.79×10^4 V/cm
ν_{sat}	Saturation velocity	1.94×10^7 cm/s
α	Power index	1.33
β	Power index	7.10

The temperature-variations of the first five entries of Table (3.1) were found to follow a power law, as the temperature increases. These variations with reference to parameter values at room-temperature are given by:

$$\mu_0(T) = (\frac{T}{300})^{\alpha_1} \times \mu_0(T = 300K) \tag{3.2}$$

$$\mu_1(T) = (\frac{T}{300})^{\alpha_2} \times \mu_1(T = 300K) \tag{3.3}$$

$$v_{sat}(T) = (\frac{T}{300})^{\alpha_3} \times v_{sat}(\mathrm{T = 300K}) \tag{3.4}$$

$$E_0(T) = (\frac{T}{300})^{\alpha_4} \times E_0(\mathrm{T = 300K}) \tag{3.5}$$

$$E_1(T) = (\frac{T}{300})^{\alpha_5} \times E_1(\mathrm{T = 300K}) \tag{3.6}$$

The least-mean-square –obtained values of α_1, α_2, α_3, α_4, and α_5 are -1.63, -0.06, 0.26, 0.4, and 0.18, respectively. Values of the power indices of (3.1) have been assumed to be temperature independent. It is physically illustrative that among these values α_1 explicitly agrees with the trend of the temperature-variation of low-field electron mobility at high temperatures [20], [46]. Figure 3.2 illustrates the matching of these analytical expressions with the Monte Carlo-based trends (previously shown in Figure 3.1).

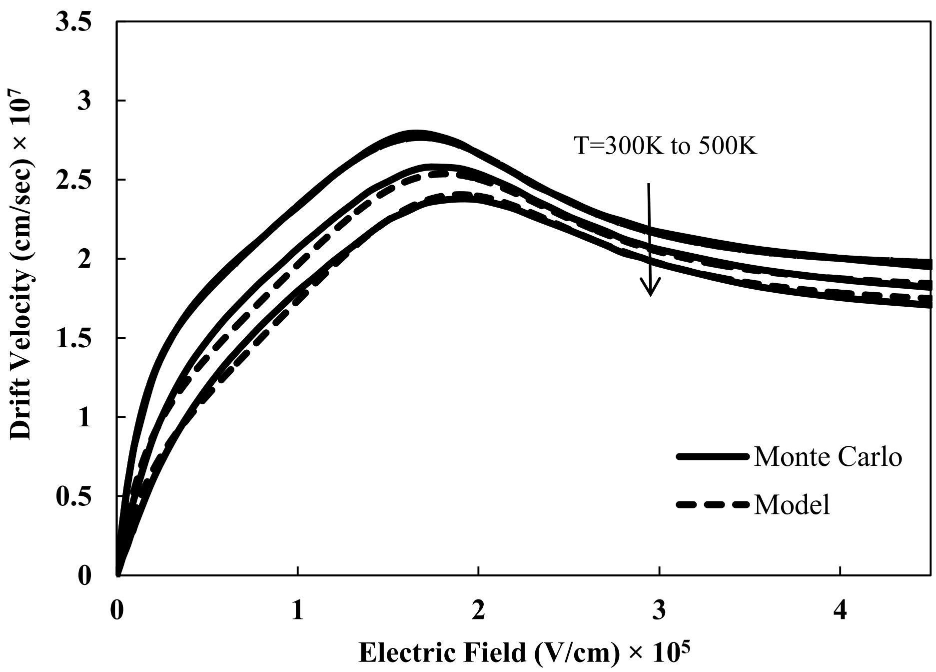


Figure 3.2: Matching of the electron drift transport characteristics shown by the analytical expression (3.1) with the Mont Carlo-based characteristics of Figure 3.1 at 300, 400, and 500K.

3.4 Drain current modeling of AlGaN/GaN HFETs

According to the model of Loghmany *et al.* the channel of a non self-aligned AlGaN/GaN HFET is broken into a combination of three regions: an ungated HFET representative of the source-access region, a gated HFET located under the gate electrode, and an ungated HFET representative of the drain-access region [40]. These regions are identified in Figure 3.3. While due to the special form of the electric-field variation of HFETs along the channel, in the first part of the channel electric-field values are small, at high drain-source voltages (at the drain-side of the gated channel and in its vicinity in the ungated drain-access region) electron drift velocity will go through the velocity overshoot and eventual saturation [40]. In this model, the part of the channel with electric-field values below the corresponding value to the peak electron drift velocity is referred to as linear, while the regime of operation in the rest of the channel is referred to as saturation.

3.4.1 Linear Regime

Assuming the mobility model expressed by (3.1), under the linear regime of operation Loghmany *et al.* have presented the variation of channel-potential (i.e. V(x)) according to the following differential equation [40]:

$$C_{CH}\left(V_{GT}-V(x)\right)\left(\mu_1\frac{-dV(x)}{dx}\left(\frac{\frac{-dV(x)}{dx}}{E_0}\right)^{\alpha}+v_{sat}\left(\frac{\frac{-dV(x)}{dx}}{E_1}\right)^{\beta}+\mu_0\frac{-dV(x)}{dx}\right)$$
$$-J\left(\left(\frac{\frac{-dV(x)}{dx}}{E_0}\right)^{\alpha}+\left(\frac{\frac{-dV(x)}{dx}}{E_1}\right)^{\beta}+1\right)=0 \tag{3.7}$$

In this equation V_T is the threshold voltage, V_{GT} is defined by V_G-V_T, J is the current density per unit-width of the transistor, and C_{CH} is the gate capacitance calculated in terms of dielectric constant of AlGaN (i.e. ε_{AlGaN}), AlGaN thickness (i.e. d), and effective thickness of the 2DEG (i.e. Δd):

$$C_{CH}=\frac{\varepsilon_0\varepsilon_{AlGaN}}{d+\Delta d} \tag{3.8}$$

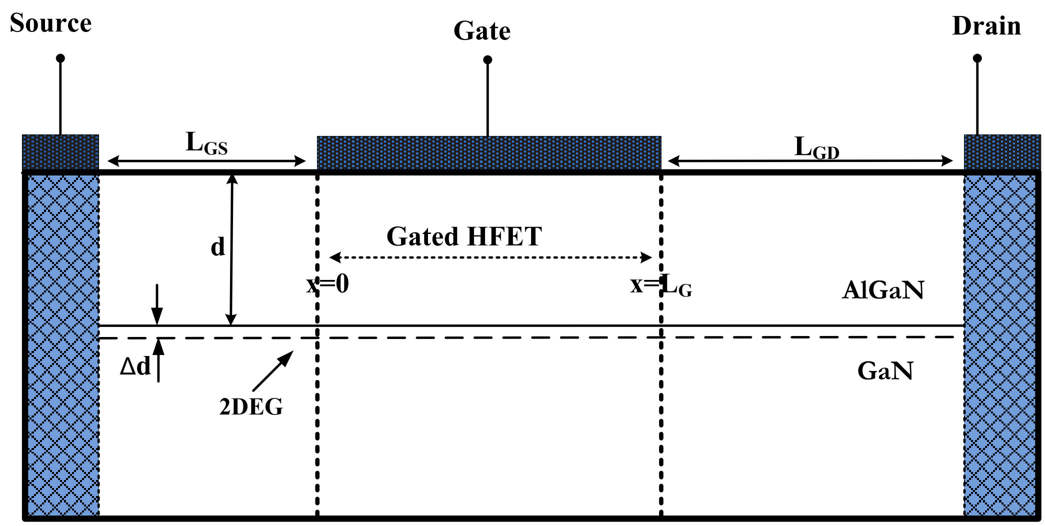


Figure 3.3: Basic schematic structure of an AlGaN/GaN HFET. L_{GS} and L_{GD} represent the length of the ungated HFETs of the source-access and drain-access regions, respectively.

The solution to (3.7) can be obtained by using the backward differentiation method, with the initial value of the voltage at the source edge of the gate (i.e. V(x=0)) calculated for each value of the current density according to the potential drop across the series combination of the source-access region resistance and the source contact resistance.

3.4.2 Saturation Regime

As the electric-field along the channel exceeds the value corresponding to the maximum electron drift velocity (i.e. $E_{v\text{-}max}$), reduction of the drift velocity and also growing significance of the lateral electric-field in calculation of 2DEG carrier density render the drift-only transport formalism, applied to the linear part of the channel, inadequate. Loghmany *et al.* [40], following the footsteps of Grebene *et al.* [47], have investigated the potential drop along this region by considering the steady-state drift velocity overshoot of the electrons in the AlGaN/GaN HFET channel (Figure 3.1) in conjunction with the application of the Gauss' law. The Gaussian box extended throughout this region is indicated in Figure 3.4. This model indicates the development of a non-zero gradient in the electron concentration of this part of the channel. As a result, in applying the current-continuity and continuity of the electric-field along the channel, for each point along this part of the channel the diffusion current density (i.e. J_{Diff}) should be calculated and deducted from the total current density to achieve the drift current component [40].

The resulting expressions for the calculation of the effective threshold voltage (i.e. $V_T(x')$) and the component of the electric-field along the length of the channel under saturation, are given by [40]:

$$V_T(x') = V_G - V(x') - \frac{J_{D(x')}}{C_{CH} \times v(x')} \tag{3.9}$$

$$\frac{\partial E_x(x')}{\partial x'} = -\frac{C_{CH}}{\varepsilon_{GaN} Y_j}\big(V_T - V_T(x')\big) \tag{3.10}$$

where J_D is the drift current density, which is the difference between the total current density (i.e. J) and the diffusion current density. The effective threshold voltage and its gradient are in turn used in calculation of the diffusion current. It has been shown that the assumption of a slightly varying channel-potential along this part of the channel (i.e. V(x')) can easily lead these recursive equations to convergence.

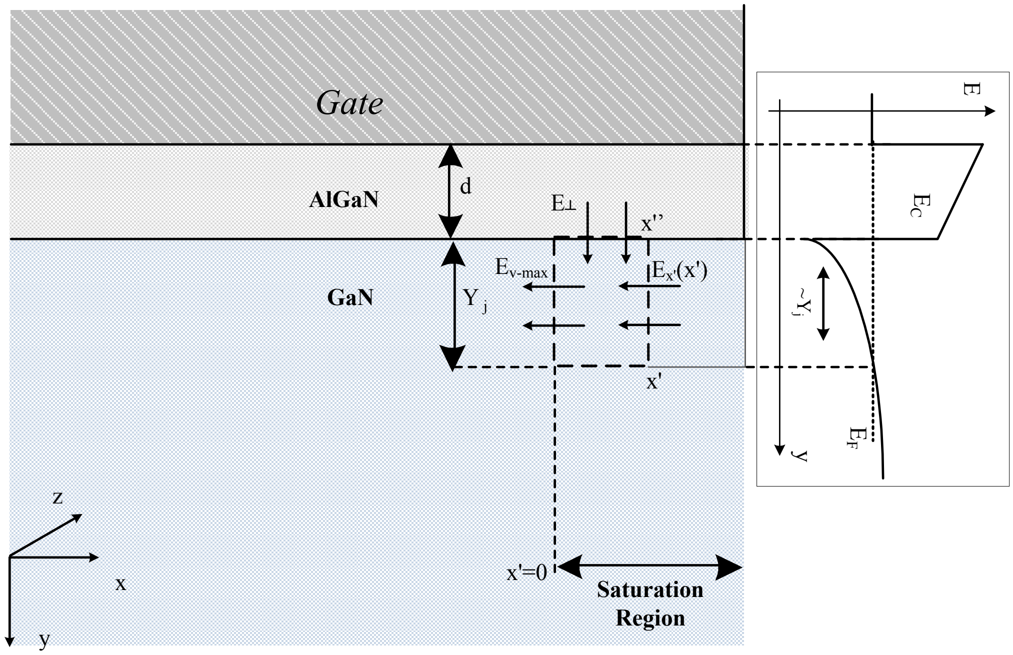


Figure 3.4: Schematic illustration of the boundaries of the Gaussian box formed in the saturation region. The conduction band edge of AlGaN/GaN heterointerface is shown in the inset.

According to this model, for each value of the current density the potential drop along the length of the channel is calculated by adding up the potential drop along the channels of the two ungated HFETs of source- and drain-access regions and the channel of the gated HFET (Figure 3.3). While, the moderate electric-field of the source access-region deems the consideration of a 2DEG sheet resistance sufficient for studying this part of the channel, in the drain access-region the ungated HFET should be investigated as a channel prone to saturation. As a result, the model explained in sections 3.4.1 and 3.4.2, with a few modifications, is applied to this part of the channel. These modifications include the mathematical consideration of a uniform surface potential, calculated through establishing the current-continuity and continuity of electric-field at the boundary of the gated and the ungated HFET [40].

Considering the absence of a blocking Schottky contact at the surface of the AlGaN barrier of an ungated HFET, it is evident that the channel will preserve its linear characteristics up to relatively higher drain-source voltages [48-49]. This fact contributes to lowering the potential drop along the drain-access region. This is caused by the mandate of the current-continuity that under the linear regime of operation the electrons in the more populated 2DEG channel of the ungated HFET should drift more slowly than in the neighbouring gated HFET. As a result, the electric-field of this part of the channel is forced to maintain a lower strength (Figure 3.1). Supporting this observation of the deferred saturation, in this implementation of the model presented in [40], choosing an appropriate threshold voltage for the channel of the drain-access region under the linear regime of operation has resulted in a more accurate prediction of the device knee voltage. This very important improvement in the prediction power of the model is presented in section 3.5 with regards to the experimental I_D-V_D characteristics.

3.4.3 Temperature variations of the channel potential

In modeling the temperature variations of the I_D-V_D characteristics of AlGaN/GaN HFETs, the temperature-dependent drift transport model presented in section 3.3 has been applied to the device model of sections 3.4.1 and 3.4.2. In this implementation, attention has been paid to the thermal characteristics of sheet resistance in the access regions. This has been observed to be able to improve the predicting power of the model in comparison to the other temperature-dependent models of AlGaN/GaN HFETs [50-54]. For the source-access region this variation is quite accurately predicted in terms of the power-law variation of the low-field electron mobility (i.e. (3.2)) [20].

For the temperature range of interest of this study (i.e. 300-500K) a change in the quality of Ohmic and Schottky contacts to the AlGaN/GaN HFET has not been predicted. As a result these effects are not considered. This assumption is substantiated by the experimental observations provided in section 3.5. These include the absence of a temperature-dependent variation of the threshold voltage of the device and also optical evaluation of the contacts before and after the high-temperature tests (Figure 3.5). It has also been observed that the high-temperature tests leave no considerable permanent degradation in the I_D-V_D characteristics.

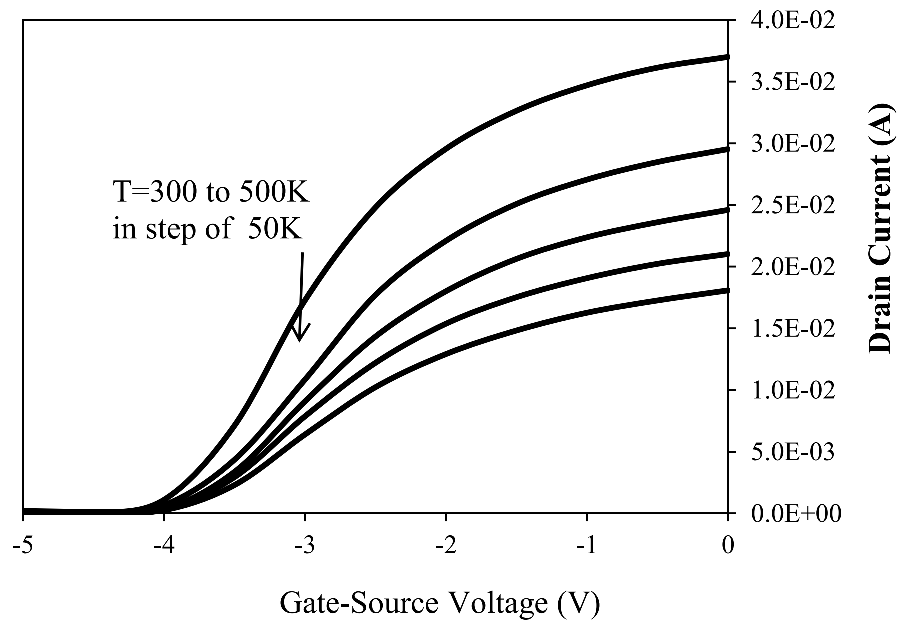


Figure 3.5: I_D-V_G characteristics when V_D=1V at T=300 through 500K, in step of 50K.

3.5 Experimental background and discussions

The temperature dependent model, presented in section 3.4, has been assessed versus the experimentally measured I_D-V_D characteristics of a number of AlGaN/GaN HFET, measured at temperatures of 300, 400, and 500K. The device characteristics used in these evaluations have been typical characteristics of the device behaviors observed across the wafer.

The HFET epitaxial layers of the devices explored in this study have been grown on a SiC substrate. Details of the layer structure are shown in Figure 2.2. To review these details it should be mentioned that this structure is composed of a 20 nm -thick AlGaN barrier of thirty percent Al-composition, a 1 nm -thick AlN spacer layer sandwiched between the AlGaN barrier and GaN channel, and a GaN channel layer. The thickness of the unintentionally-doped GaN channel layer is 200 nm. Device fabrication was carried out by CMC. Device design has been performed according to the process flow of this foundry, which has been explained in Chapter 2.

Absence of frequency dispersion in the drain current and gate-transconductance of the measured devices and high values of gate-transconductance (i.e. of the order of 250 mS/mm), and drain current density (i.e. of the order of 1 A/mm) of these devices are indicative of good quality of surface passivation and processing [55]. A strong saturating characteristic of the drain current is also observed. As a result, conclusions drawn from the modeling of the I_D-V_D characteristics of these devices fairly assess the high-temperature transport problem of AlGaN/GaN HFETs.

The device layout is shown in Figure 3.6, whereas the vertical and horizontal device dimensions are tabulated in Table 3.2. Also in this table, the parameters adopted in the application of the model, presented in section 3.4, to these devices are summarized.

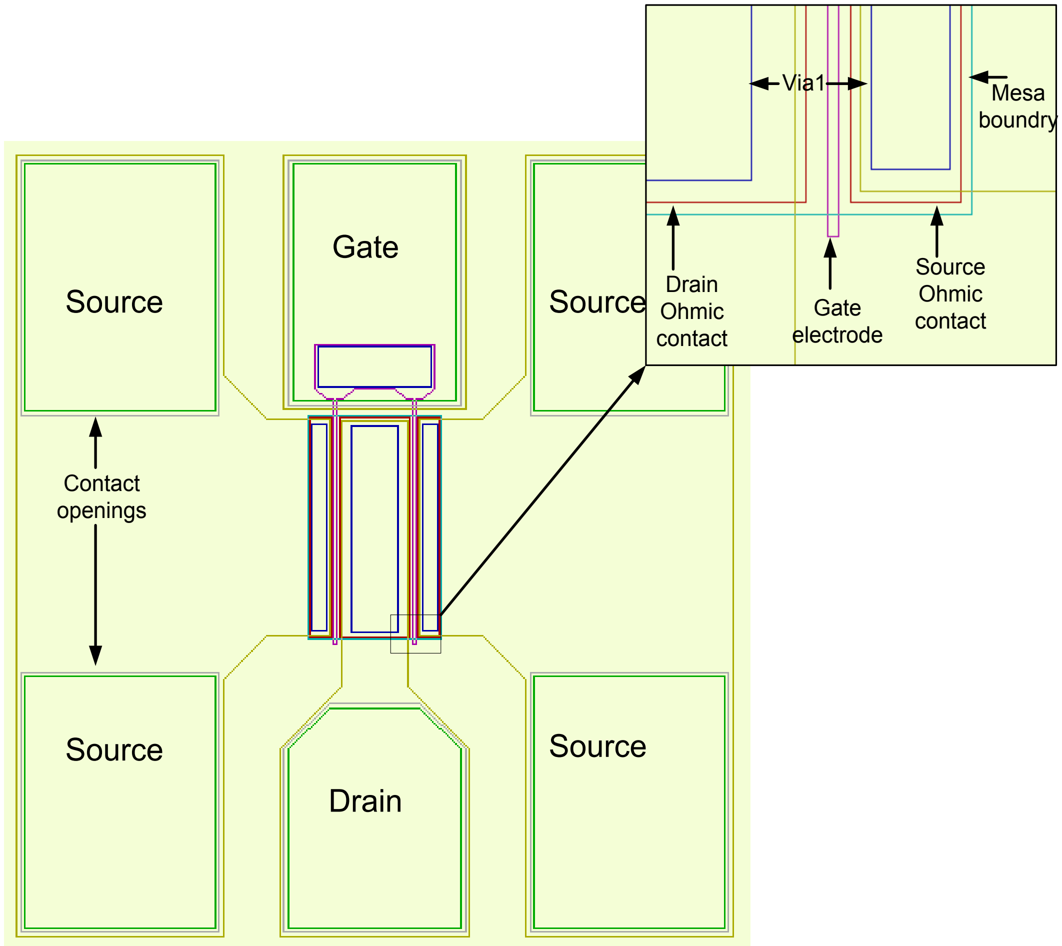


Figure 3.6: Device layout of a two-finger AlGaN/GaN HFET with micro-strip interconnects.

Table 3.2: Device parameters and parameters used in the model.

Symbol	Description	Value
L_G	Gate Length	1 µm
L_{GD}	Drain-access region length	2 µm
L_{GS}	Source-access region length	1.1 µm
W	Channel width	100 µm
R_{CS} and R_{CD}	Source and drain contact resistivity	0.73 Ohm.mm (provided by the foundry)
R_{sh}	Channel sheet resistance	262 Ohm/sq
d	Barrier thickness	21 nm
Δd	2DEG thickness	2 nm
V_T	Threshold voltage	-4.1 V

3.5.1 Assessment of the temperature-dependent device model

In all the measurements reported in here, a Keithley semiconductor parameter analyzer was used. Measurements were done in the pulsed-mode with short pulses of small duty-cycle to avoid self-heating. Figure 3.7 illustrates the agreement between the experimentally-measured and modeled room-temperature I_D-V_D characteristics of the AlGaN/GaN HFET reported earlier in this section. The superb match between these two characteristics is indicative of the importance of the correct assessment of the deferred saturation of the ungated drain-access region (indicated in section 3.4.2). The model explained in section 3.4 has been implemented numerically with the use of the finite difference technique. Modeling has been performed for the gate voltages not too close to the threshold voltage. The reason for that is that the model presented in section 3.4 assumes zero leakage through the substrate and as a result it is not capable of correctly reproducing the I_D-V_D characteristics close to the threshold voltage [40].

The convergence of the electric-field, channel potential, effective threshold voltage, electron linear mobility, electron drift velocity, sheet-charge density, drift-, and diffusion-current density, in the saturation region of the gated HFET for one value of current-density and gate-voltage are shown in Figure 3.8 (a)-(h), respectively. The one percent convergence criterion has been used in this modeling.

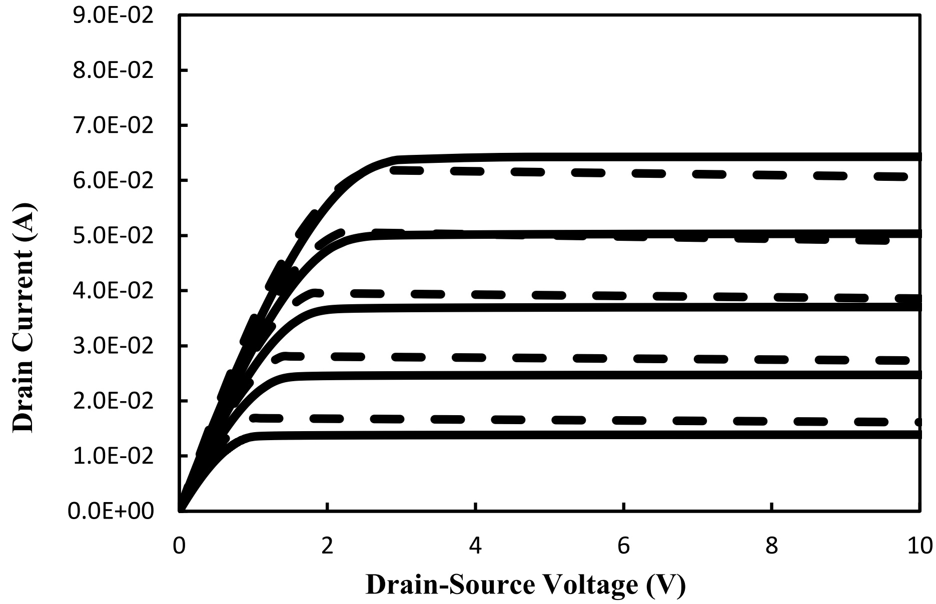


Figure 3.7: I_D-V_D characteristics based on model (solid line) and experimental results (dashed line) at T=300K for V_G=-3 to -1V, in step of 0.5V.

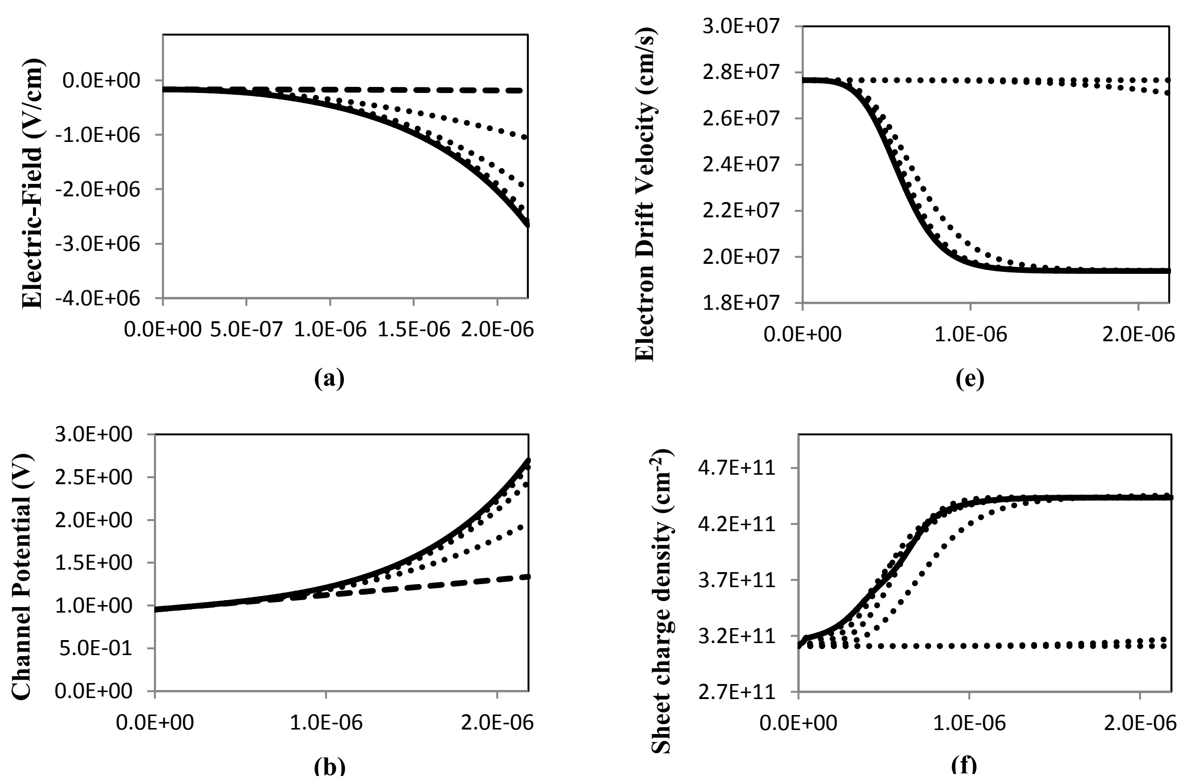


Figure 3.8: Continued on the next page.

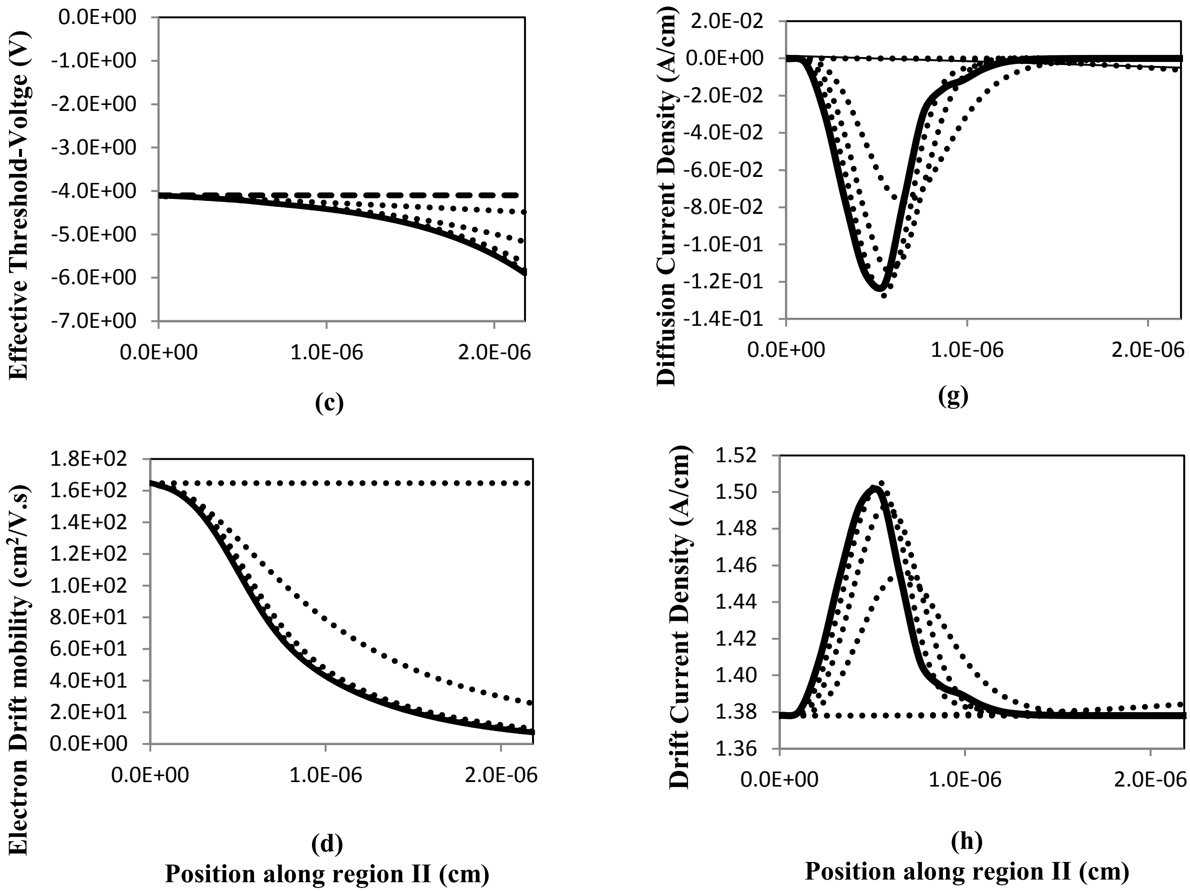
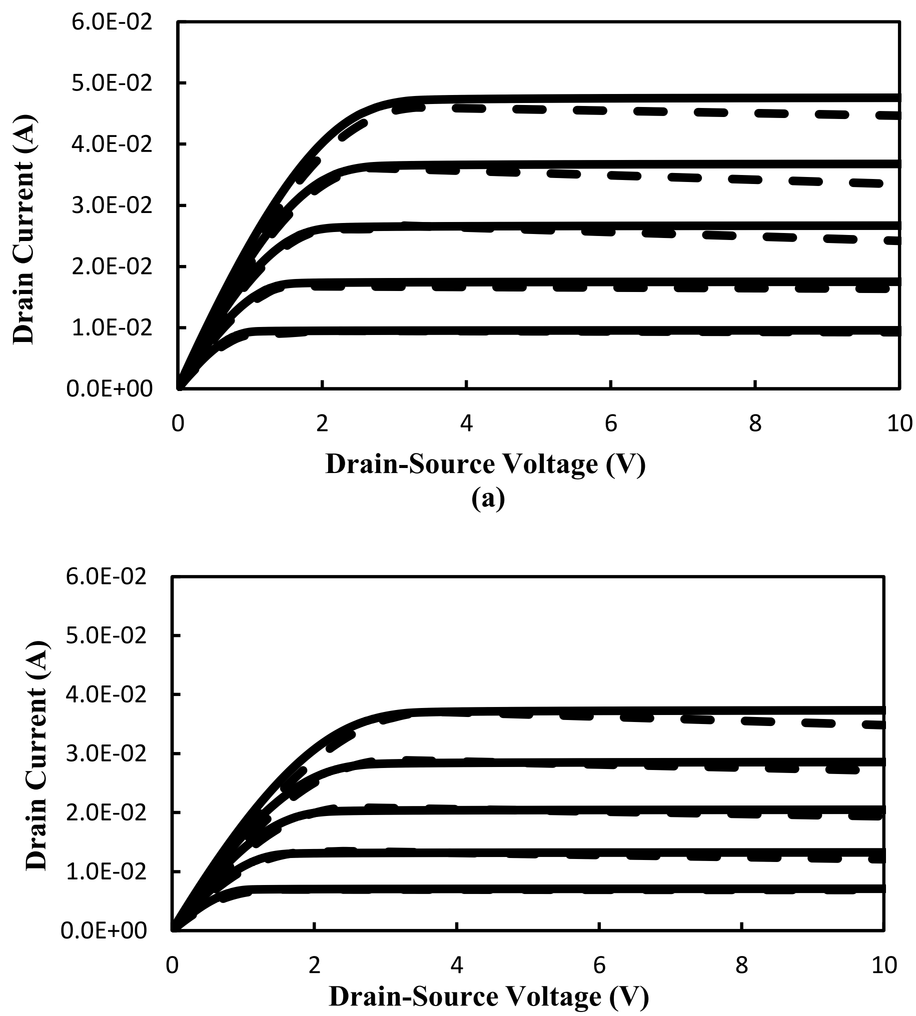


Figure 3.8: Convergence of electric-field (a), channel-potential distribution (b), effective threshold-voltage (c), linear electron mobility (d), electron drift velocity (e), sheet charge density distribution (f), diffusion current density (g), and drift current density (h) at V_G=-3 V and current density equal to 1.378 A/cm at T=300K, where final results are shown in solid line, initial guesses for electric-field, channel potential, and effective threshold-voltage is shown in dashed lines, and iterations are shown in dotted lines.

Figures 3.9(a) and (b) illustrate the superb match between the modeled and the experimentally measured I_D-V_D characteristics at 400 and 500K, respectively. The on-chip high temperature measurements have been performed using the enclosed chamber of an MMR probe station. Samples were kept at the measurement temperature long-enough to reach the steady-state condition. In obtaining the modeled characteristics, the temperature variation of the transport in all three regions of gated-channel, source-, and drain-access are considered, as outlined in section 3.4.

In order to demonstrate the importance of considering the temperature-dependency of transport in the access regions, Figure 3.10 depicts the modeled drain characteristics versus the experimental data with only considering the temperature-dependency of transport in the gated-channel. The degradation in prediction of the knee-voltage and the saturation characteristics are clearly indicative of the importance of studying the temperature variation of the sheet resistance in the access region.



(a)

6.0E-02
5.0E-02
4.0E-02
3.0E-02
2.0E-02
1.0E-02
0.0E+00
Drain Current (A)
0
2
4
6
8
10
Drain-Source Voltage (V)

(b)

Figure 3.9: I_D-V_D characteristics based on model (solid line) and experimental results (dashed line) at T=400 (a), and 500K (b), for V_G=-3 to -1V in step of 0.5V. The temperature variation of the sheet resistance in the access region is fully considered.

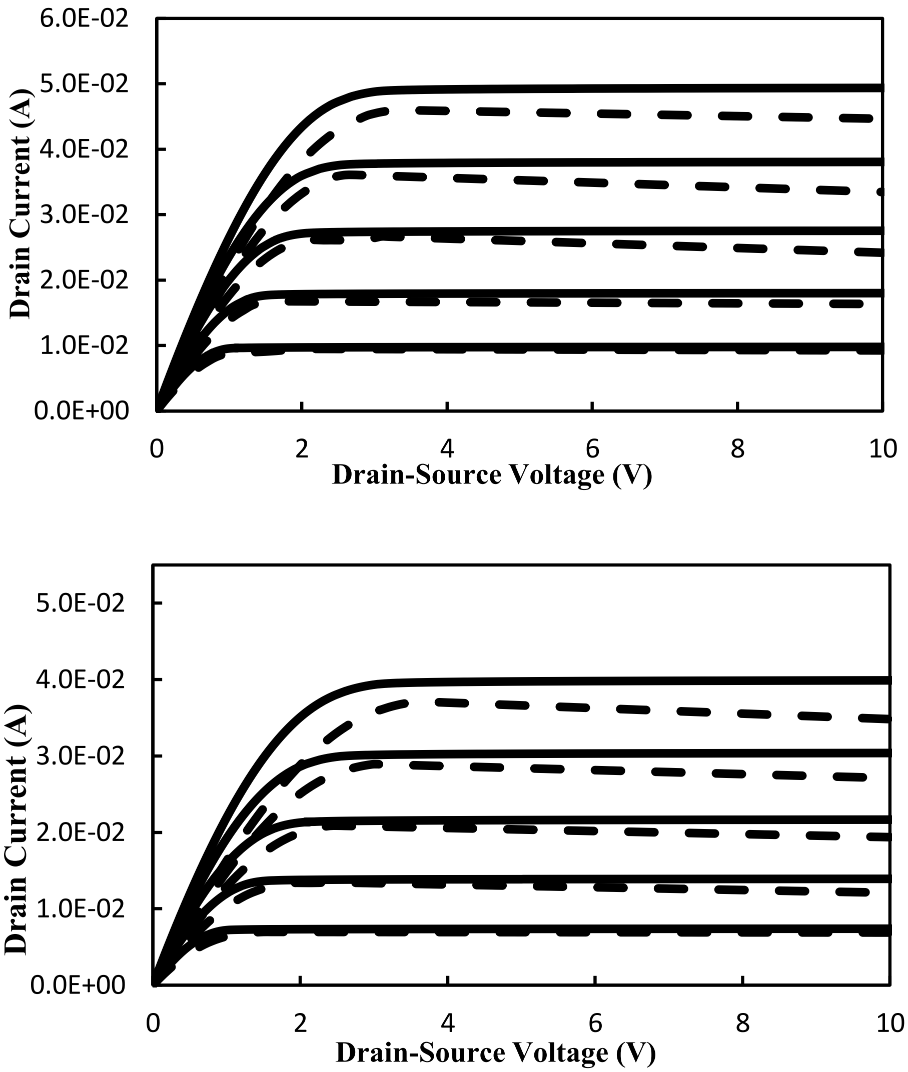


Figure 3.10: I_D-V_D characteristics based on model (solid line) and experimental results (dashed line) at T=400 (a), and 500K (b), for V_G=-3 to -1V in step of 0.5V. The temperature variation of the sheet resistance in the access region is not considered.

3.5.2 Role of the accurate modeling of high-field drift-velocity in high-temperature device modeling

Many of the existing device models, while paying attention to the low-field electron mobility of the AlGaN/GaN channel, approximate the high-field electron drift velocity in terms of a purely-saturating v_d-E characteristic [36]. In order to assess the degree of accuracy of this assumption at higher temperatures, in this part two different mobility models with different degrees of accuracy in following the temperature-dependent v_d-E characteristics resulted from MOCASIM simulations are investigated:

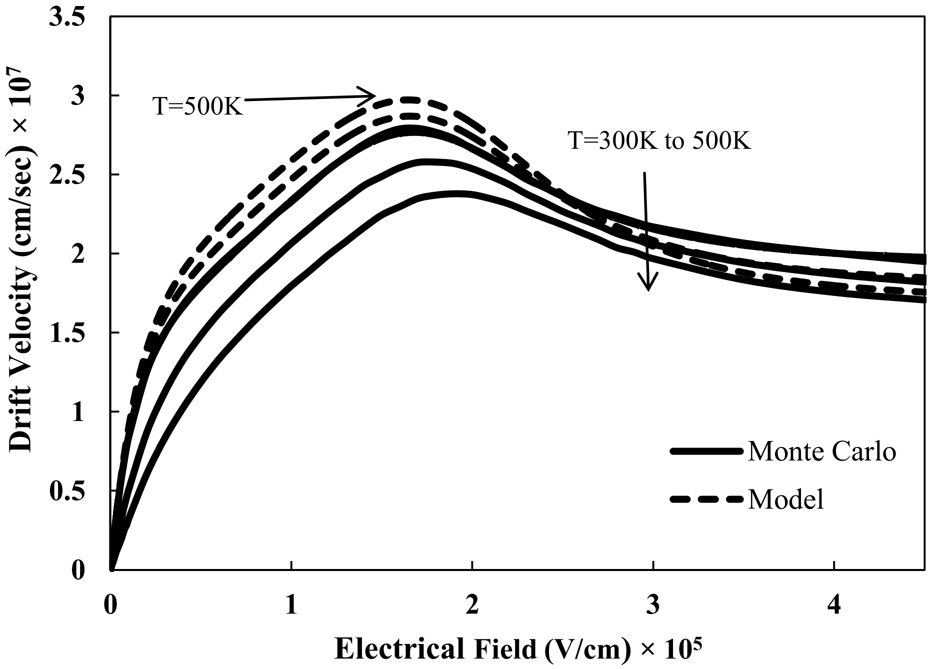
Transport model (1): In this model the low-field electron mobility (i.e. μ_0) is assumed to be temperature independent, while the temperature dependency of the other parameters of (3.1) are assessed for yield maximum similarity to the Monte Carlo-based transport characteristics at high electric-fields.

Transport model (2): In this model, only the temperature variation of the low-field mobility (i.e. μ_0) is considered in order to yield maximum similarity to the Monte Carlo-based transport characteristics at low to moderate electric-fields, while other parameters of (3.1) are assumed temperature independent.

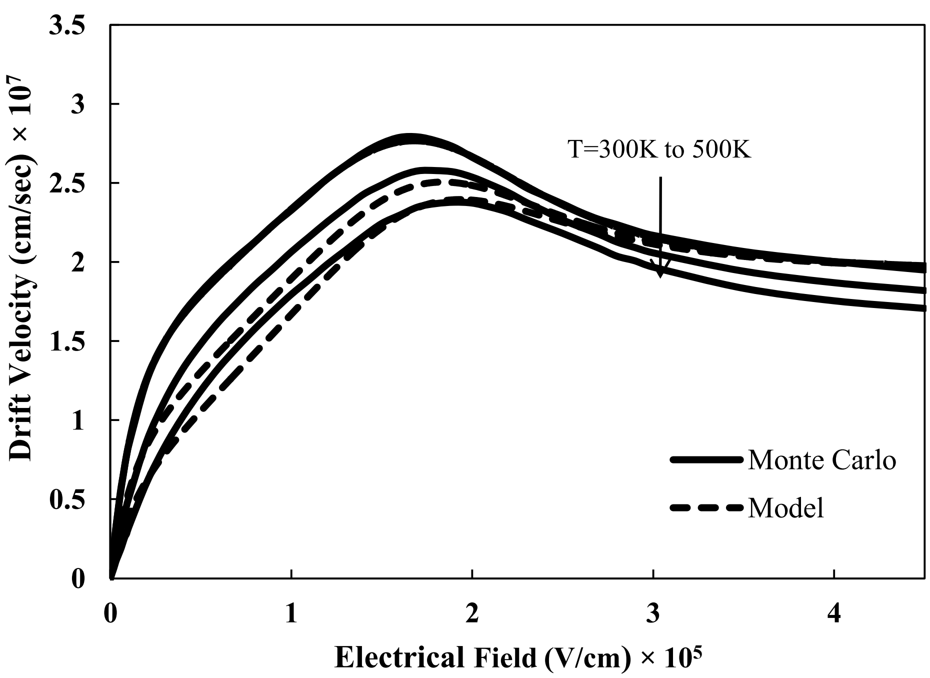
Figures 3.11(a) and (b) depict the predictions of the first and the second model in comparison to the MOCASIM-calculated characteristics, which were also shown in Figure 3.1, respectively.

The adoption of the transport models (1) and (2), to the device model of section 3.4, result in the I_D-V_D characteristics shown in Figures 3.12 and 3.13, respectively. As shown in these figures, for temperatures of 400 and 500K, the inaccuracy inherent to the transport model (1) leaves a much more pronounced impact on the predicting power of the analytical device model. The inherent inaccuracy of the transport model (2) in following the high electric-field transport is observed to merely result in the slightly erroneous calculation of the knee voltage.

These observations confirm that maintaining the accuracy in modelling of low-field electron mobility and steady-state overshoot of drift velocity are much more important in producing an accurate model, than the accuracy in correctly following the saturation velocity. In order to study the degree of this approximation as the temperature is raised, the difference in the value of current density at the onset of deviation of drift velocity from $\mu_0 E$ (referred to in here as onset of saturation) with the value of saturated current density is studied. These values at temperatures of 300, 400, and 500K for a few gate-voltages are tabulated in Tables 3.3, 3.4, and 3.5, respectively. As shown in these tables, with the elevation in temperature especially at gate voltages farther away from threshold, the current density at the onset of saturation region becomes proportionally less important in calculation of the current-drive in saturation. As a result, for these conditions purely maintaining the accuracy of the value of the low-filed electron mobility, which is the dominant factor under the linear regime of operation, would be less acceptable.



(a)



(b)

Figure 3.11: Matching of the electron drift transport characteristics shown by the analytical expression (3.1) with the Mont Carlo-based characteristics of Figure 3.1 at 300, 400, and 500K, according to the transport model (1) and (2), respectively shown in (a) and (b).

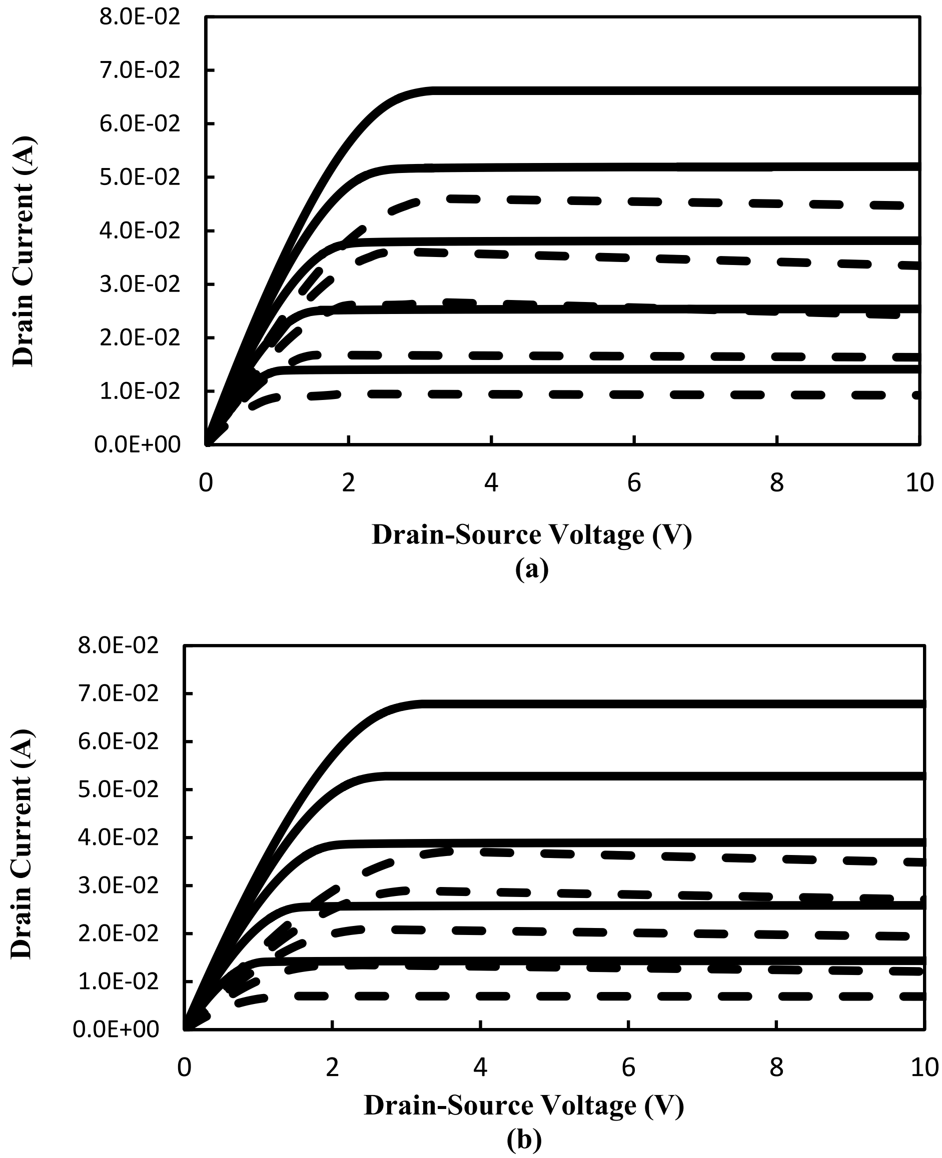


Figure 3.12: I_D-V_D characteristics based on the transport model (1) (solid line) and experimental results (dashed line) at T=400 (a), and 500K (b), for V_G=-3 to -1V in step of 0.5V.

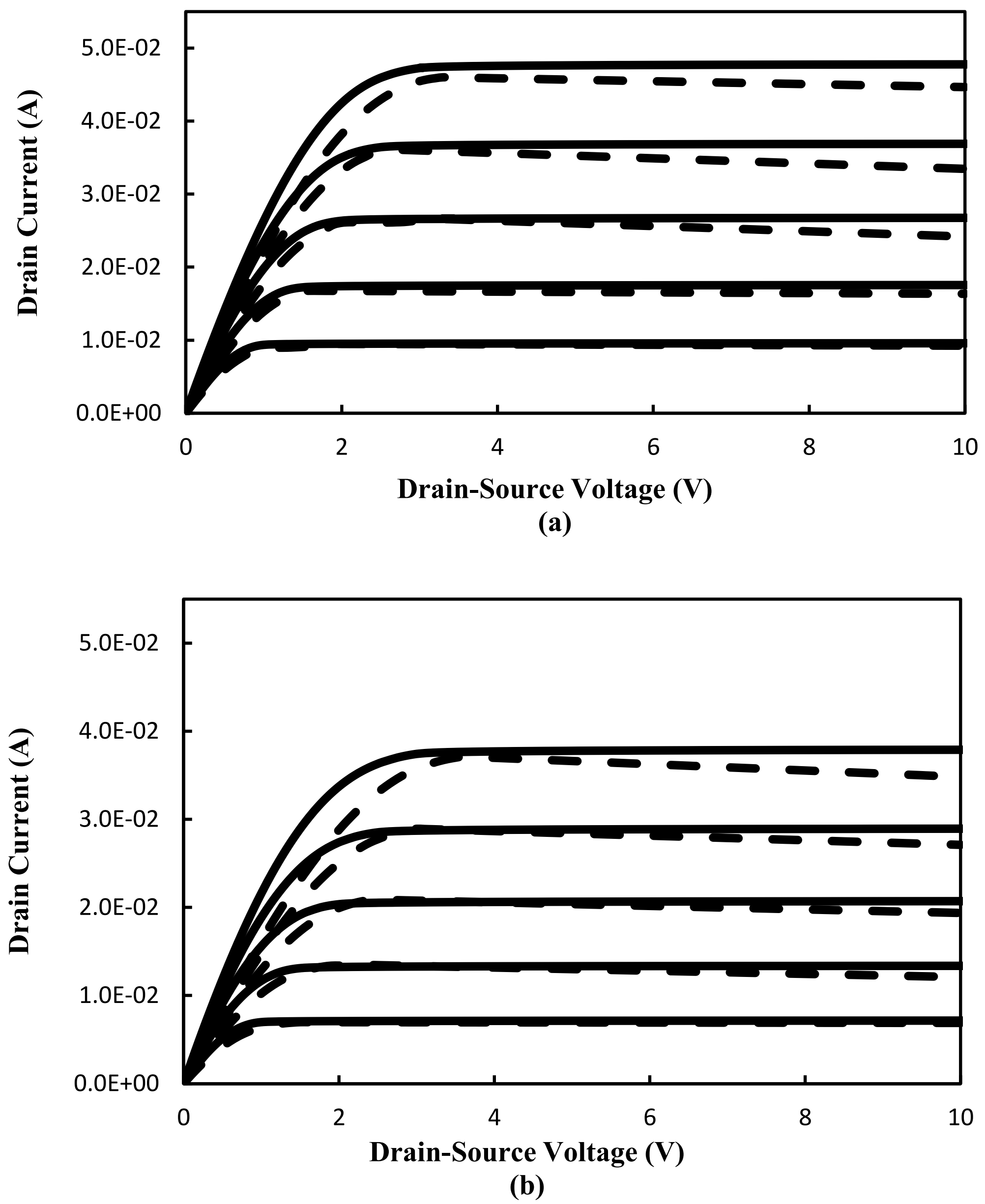


Figure 3.13: I_D-V_D characteristics based on the transport model (2) (solid line) and experimental results (dashed line) at T=400 (a), and 500K (b), for V_G=-3 to -1V in step of 0.5V.

Table 3.3: Current density at the onset of saturation and saturation current density at 300K.

V_G (V)	Current density at the onset of saturation (A/cm)	Saturation current density (A/cm)	Percentage of the saturation current density at the onset saturation
-3	1.317	1.361	96.7
-2.5	2.323	2.441	95.1
-2	3.435	3.663	93.7
-1.5	4.615	4.987	92.5
-1	5.840	6.389	91.4

Table 3.4: Current density at the onset of saturation and saturation current density at 400K.

V_G	Current density at the onset of saturation (A/cm)	Saturation current density (A/cm)	Percentage of the saturation current density at the onset saturation
-3	0.9	0.939	95.8
-2.5	1.615	1.725	93.6
-2	2.412	2.634	91.5
-1.5	3.264	3.634	89.8
-1	4.150	4.71	88.1

Table 3.5: Current density at the onset of saturation and saturation current density at 500K.

V_G (V)	Current density at the onset of saturation (A/cm)	Saturation current density (A/cm)	Percentage of the saturation current density at the onset saturation
-3	0.664	0.698	95.1
-2.5	1.206	1.305	92.4
-2	1.815	2.020	89.8
-1.5	2.467	2.820	87.5
-1	3.149	3.688	85.3

3.6 Conclusions

A capable analytical framework with manageable degree of computational difficulty is proposed for modeling the high-temperature drain current-voltage characteristics of AlGaN/GaN HFETs. The model takes into account the temperature-dependence of transport through the gated-channel of an AlGaN/GaN HFET and also its access regions. This model is validated with regards to the experimentally measured drain current characteristics. In light of this work, it is shown that maintaining a high degree of accuracy in the incorporated transport model into the analytical models developed for modeling the drain-current behavior of AlGaN/GaN HFETs becomes more important with the increase of device operation temperature. In this work, self-heating and non steady-state transport and thermal effects have not been considered. This is a condition suitable for relatively -long-channel devices operating under the low duty-cycle pulsed operation mode.

Chapter 4

Conclusion and Future Work

One goal of this thesis was to pursue on a different approach (through strain-relief) to open a new avenue for fabrication and design of enhancement-mode AlGaN/GaN HFETs, side by side the high current-density depletion-mode AlGaN/GaN HFETs. This is beneficial to applications such as direct connected transistor logic (DCTL). Experimental results, although unsuccessful in achieving enhancement-mode operation, are encouraging in terms of positive shifting of the threshold voltage. This achievement is the first indication of the possibility of exerting control over the threshold voltage of AlGaN/GaN HFETs through the definition of mesa geometry.

In chapter 2, the impact of the size of the isolation-mesa on the sweeping- and pulsed-mode drain current-voltage characteristics of AlGaN/GaN HFETs has been studied. Investigations reveal that while by implementing AlGaN/GaN HFETs on array of islands or mesas of smaller dimensions, rather than one continuous-mesa, same values for the maximum drain current level can be maintained, pinch-off voltage can be made less negative. Also, the maximum gate transconductance will be improved by island-type isolation. It is also observed that the proportionally larger surface area for power dissipation in fin- and island-isolated HFETs can reduce the impact of heating on AlGaN/GaN HFETs.

Due to the fabrication constraints of the foundry, the minimum size of the isolated mesas reported in this work was limited. Further driving-down the size of the isolation-mesas of AlGaN/GaN HFETs is extremely important in further studying the correlation between the positive shift in pinch-off voltage and the mesa geometry.

Modeling the drain current of AlGaN/GaN HFETs at high temperature ambient was the other objective of this thesis, since high temperature ambient is a probable environment for these high-power devices, such a model is extremely beneficial in providing guidelines for device design in this technology.

In chapter 3, an adequate analytical framework is proposed for modeling the high-temperature drain current-voltage characteristics of AlGaN/GaN HFETs. The model takes into account the temperature-dependence of transport through the gated-channel of an AlGaN/GaN HFET and also its access regions. This model is validated with regards to the experimentally measured drain current characteristics. In light of this work, it is shown that maintaining a high degree of accuracy in the incorporated transport model (into the analytical models developed for modeling the drain-current behavior of AlGaN/GaN HFETs) becomes more important with the increase of device operation temperature.

As future works in these two areas the following are suggested:

- Experimental strain analysis and characterization of the small isolated mesas of AlGaN/GaN epilayer.
- Experimentation of strain-relief on epilayers grown on compliant diaphragms.
- Theoretical study of the proposed strain-relief strategy.

- Incorporation of self-heating, gate- and substrate leakage, and non steady-state transport in the presented analytical model.

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