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Bulk and Epitaxial Growth and Characteristics of GaAs and $Pb_{1-x}Gd_xTe$

Jean-Marie Lacroix

A Thesis

in

The Department

of

Electrical Engineering

Presented in Partial Fulfillment of the Requirements
for the Degree of Master of Engineering at
Concordia University
Montréal, Québec, Canada

August 1988

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ABSTRACT

Bulk and Epitaxial Growth and Characteristics

of

GaAs and $Pb_{1-x}Gd_xTe$

Jean-Marie Lacroix

The growth of bulk and epitaxial GaAs and $Pb_{1-x}Gd_xTe$ and their characteristics were studied. The doping mechanism of GaAs epitaxial layers grown using the Close-Spaced Vapor Transport (CSVT) was investigated. A CSVT system for the growth of up to 2 inch diameter epitaxial layers was constructed. Investigation of the doping mechanism was made by varying the growth temperatures from 720°C to 880°C, changing the spacer from fused silica to graphite and changing the source from semi-insulating GaAs to Si doped and Zn doped GaAs sources. Silicon coming from the fused silica spacer was found to be one of the major impurities influencing the electrical characteristics of the epitaxial layers. The inhibition of a deep level, present in the epitaxial layers, by shallow donors was confirmed by the n_{300}/n_{77} vs. n_{300} plot and Shockley curves using a multilevel model.

Epitaxial growth of $Pb_{1-x}Gd_xTe$ on KBr substrates was attempted. Epitaxial

layers were obtained but no electrical characterization could be made due to the inhomogeneous epitaxial surfaces and poor electrical contact adherence.

Growth of bulk $Pb_{1-x}Gd_xTe$ crystals with x=0, 1 and 5% was made using a modified Bridgman method. P and N type crystals, with large single crystal grain sizes, were obtained depending on the synthesis temperature. The mobilities obtained, lower than the ones reported for PbTe, were explained by the degree of compensation due to Te or Pb vacancies. The higher mobilities of the PbTe containing gadolinium ions were explained by three theoretical discussions which relate the abnormally high mobilities to the electron spin of the magnetic ions.

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1.0 INTRODUCTION

Gallium arsenide and lead gadolinium telluride are semiconductors which exhibit interesting properties in view of applications in the new technologies. The development of optical fibers for telecommunications has lead to a need for new optoelectronic devices, such as lasers and light emitting diodes, which operate at various frequencies. In the development of solar energy, GaAs solar cells are surpassing Si solar cells due to their higher efficiency and higher optical absorption. The ever increasing speed and data handling capacity required for new computers necessitates faster and more powerful semiconductor devices. Elemental semiconductors such as Si and Ge cannot fulfill the demanding requirements of these new technologies. Hence, new compound semiconductors are being developed to suit these needs.

The aim of this research was to grow and characterize bulk and epitaxial GaAs and $Pb_{1-x}Gd_xTe$. GaAs is better suited than Si in applications where superior performances are required. Such applications include solar cells, high frequency devices and optoelectronic devices such as solid state lasers and infrared detectors. Compared to the Si-based microelectronic devices, GaAs circuits operate at a much faster speed and with lower dissipation of energy (1). A drawback of this technology relates to the fact that GaAs is still more costly to fabricate than Si.

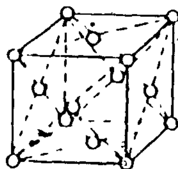
Semimagnetic semiconductors such as $Pb_{1-x}Gd_xTe$ are obtained by partially replacing one of the elements in the semiconductor, in this case PbTe, with a rare earth element capable of forming magnetic ions, in this case Gd. In the case of crystals with 1% gadolinium content, the electrical properties of lead telluride are altered in such a way as to increase the mobility of the free charge carriers. Mobilities of 10^7

$cm^2V^{-1}s^{-1}$ at 4.2 K have been reported (2). This makes it a good competitor to super lattices which are quite costly to fabricate. Lead telluride is presently used for infrared emitters and detectors.

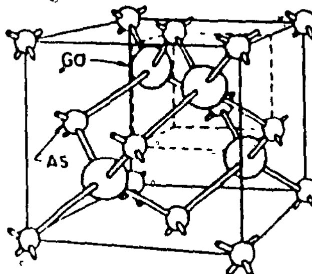
1.1 Electrical properties of GaAs and PbTe

Gallium Arsenide is a III-V compound semiconductor. It crystallizes in the zincblende structure, which consists of two equivalent interpenetrating face-centered cubic lattices, one containing Ga atoms and the other As atoms (3). Lead telluride is a IV-VI compound semiconductor and it crystallizes in the face-centered cubic rock-salt structure (Fig. 1).

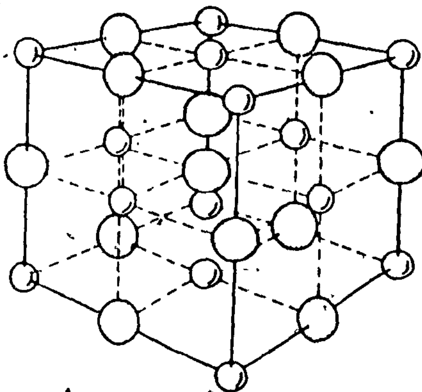
The electronic band structure of semiconductors determines their electrical properties. The improved performances in the semiconductors studied are mainly due to the direct band to band transition and higher mobility. The advantages of GaAs over Si can be illustrated by examining their respective band structures. Figure 2 shows the energy band structure of Si, GaAs and PbTe. In the perfect intrinsic crystal at low temperature, the electron states below the zero energy reference level are filled and those above the bandgap energy are empty conduction band states. When the temperature is raised or impurity dopants are added, vacant states (holes) are generated at the highest valence band states and the lowest conduction band states become occupied (4). The valence band maximum occurs at the Γ direction in the Brillouin zone for both Si and GaAs. The minimum energy level in the conduction band occurs at Γ for GaAs but at X for Si. Hence GaAs is called a direct bandgap semiconductor and Si called an indirect bandgap semiconductor. PbTe has a direct bandgap since the conduction band minimum and valence band maximum both occur at L. The effect of a direct bandgap compared to an indirect bandgap on the optical properties of the semiconductors is an increase in the absorption coefficient for a given photon energy.



Face-centered cubic (5)

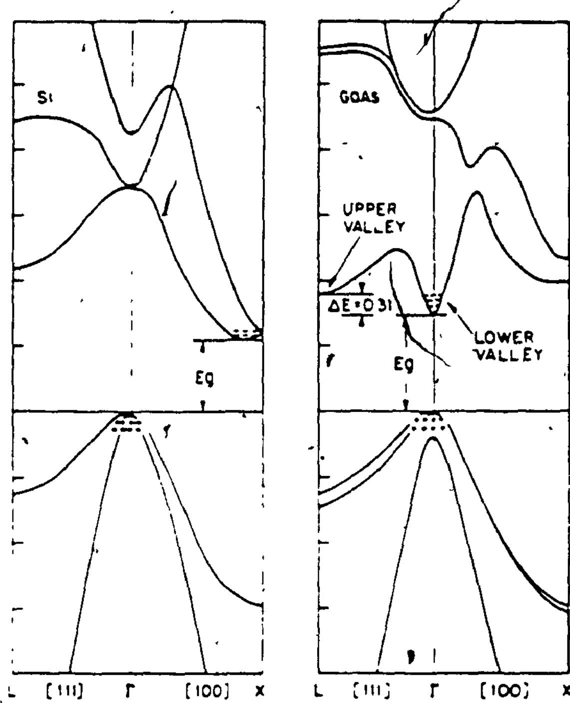


Zincblende (5)

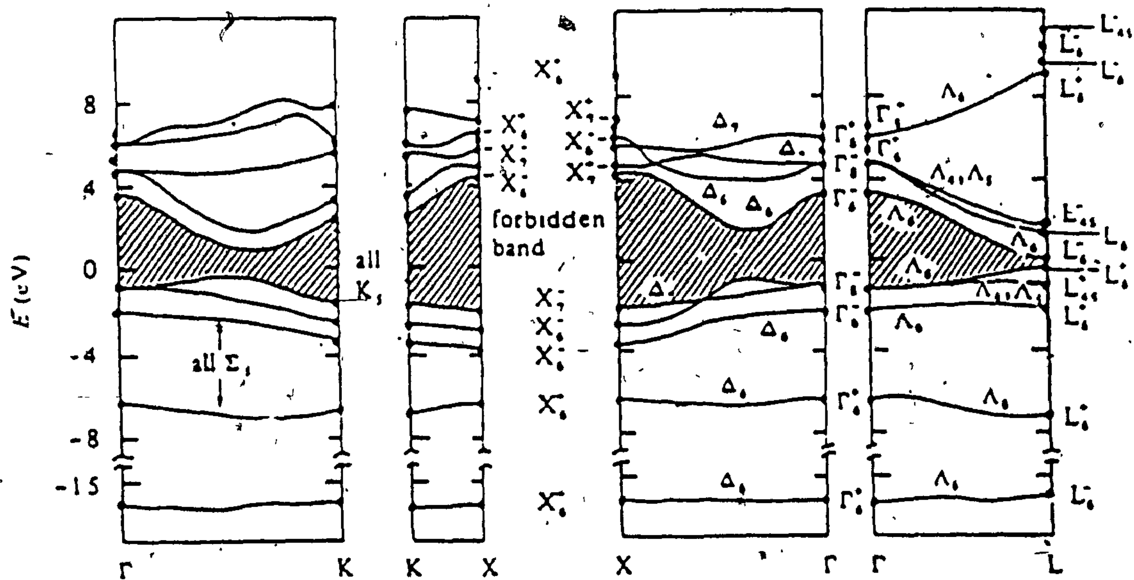


Rock-salt (6)

Fig. 1 Crystal structures



Si GaAs (7)



PbTe (8)

Fig. 2 Energy band structures

This results in more efficient optoelectronic devices.

The differences in the energy band structures of GaAs, Si and PbTe lead to differences in their electrical properties. As seen in APPENDIX A, GaAs has a larger bandgap than Si. Hence, at a certain temperature, the thermal generation of carriers is less probable in GaAs than in Si. This characteristic leeds to more highly insulating materials and a greater operating temperature range for devices made of GaAs. The low field electron mobility is much higher in GaAs than in Si due to the curvature of the conduction band minimum. Hence faster electronic devices can be achieved in GaAs (9). PbTe, on the other hand, is a narrow bandgap material which nevertheless makes it ideal for medium infrared detectors and emitters. PbTe diode lasers have been fabricated (10, 11).

The wavelength corresponding to the incident light absorbed by a given intrinsic semiconductor can be calculated for a band to band transition in the following way:

$$\lambda = hc/E_g \qquad \text{i.e. } \lambda\ (\mu m) = 1.24/(E_g\ (eV))$$

h : Plank's constant (4.14×10^{-15} eV-sec)

c : Speed of light (2.998×10^{8} m/sec)

E_g : bandgap energy

λ : wavelength of incident light

Table 1 lists the different operating wavelengths for intrinsic GaAs, Si and PbTe semiconductors at 300 K for band to band transitions. Figure 3 shows a chart of the electromagnetic spectrum.

TABLE I: Operating wavelengths

Semiconductor	bandgap	wavelength	spectrum region
GaAs	1.424eV	0.871μm	near infrared
Si	1.12eV	1.107μm	near infrared
PbTe	0.3eV	4.133μm	medium infrared

Impurity levels in the forbidden energy band of a semiconductor alter its electrical properties. Figure 4 shows the various ionization energies of impurities in GaAs. The levels below the gap center are acceptors and the levels above are donors except when otherwise specified by D for donor or A for acceptor. The type of semiconductor and the free carrier concentration can be determined from the neutrality condition using a graphical method developed by Shockley (12). GaAs can be either semiconducting or semi-insulating depending on the degree of doping and the nature of the dopant involved. Resistivities can range from less than 10^{-4} ohm-cm to as high as 10^{8} ohm-cm (13). High resistivity GaAs used as substrates allow the fabrication of integrated circuits without the need of p-n junction isolations between devices as is required in the silicon technology. These isolation junctions introduce parasitic capacitances and excess leakage currents (14).

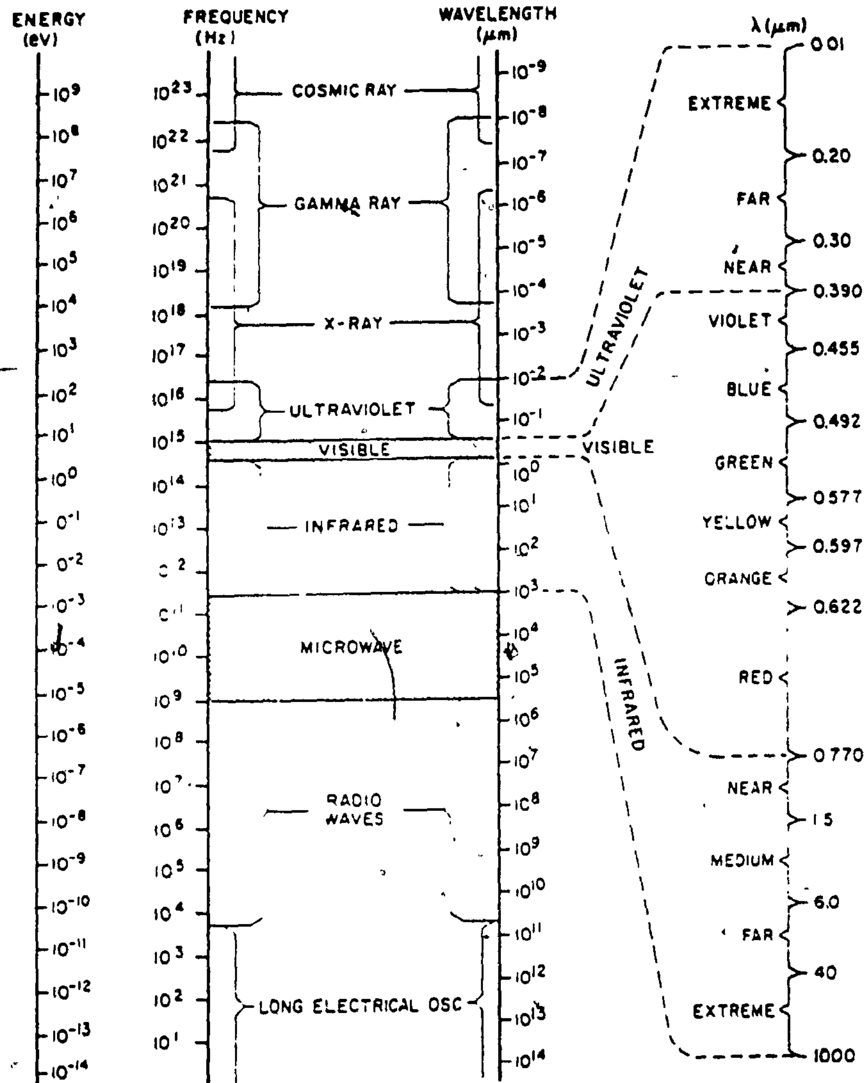


Fig. 3 Electromagnetic spectrum (15)

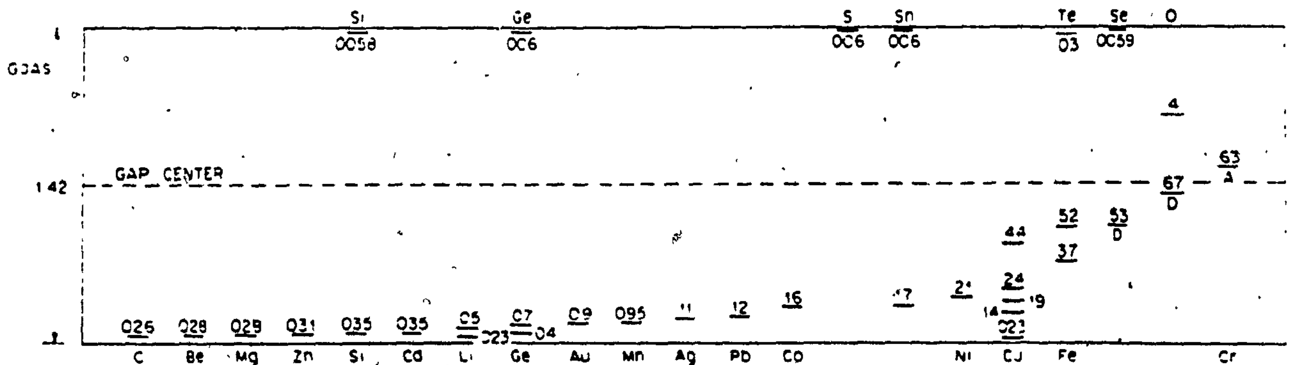


Fig. 4 Impurity levels in GaAs (16)

1.2 Bulk growth

The purpose of bulk growth is to obtain large diameter single crystals of the semiconductor material with controlled composition, controlled doping and minimum concentration of defects. There are various methods for growing bulk semiconductor materials from the melt. Some of these techniques include Bridgman (horizontal or vertical), zone melting and the Czocharlski technique. The Bridgman method, whether vertical or horizontal, consists of a furnace with two temperature zones: one held at the melting point of the material and the other held at a much lower temperature to create a temperature gradient in order to slowly solidify the melt. The molten material is slowly taken out of the hot zone and pulled into the cooler zone. This creates a solid-liquid interface which is moved slowly along the boat containing the material. If the growth rate is slow enough and (or) a seed crystal is introduced, the material will solidify into a single crystal.

Zone melting is similar to the Bridgman method except that there are two solid-liquid interfaces. Only a narrow zone of the material is melted at a time. Hence a three zone furnace is required for this type of growth.

Czochralski growth consists of vertically pulling the crystal from the melt. A seed crystal attached to a rod is lowered into the melt and when equilibrium conditions have been achieved the seed is slowly raised. This method is widely used to grow silicon.

Depending on the physical nature of the semiconductor being grown, these growth methods can be modified to accommodate peculiarities of certain semiconductors. Semicondutors in which one of the elements is volatile is such a case.

1.3 Epitaxial growth

There are three main epitaxial deposition techniques for the growth of thin semiconductor layers. These are liquid phase epitaxy (LPE), molecular beam epitaxy (MBE) and vapor phase epitaxy (VPE). Some of the advantages and disadvantages of these techniques will briefly be discussed.

The advantages of the LPE method are the simple and inexpensive apparatus involved and the high purity of the epitaxial layers produced. On the other hand LPE layers have a very poor surface morphology and the control of thin layers is very difficult (17).

MBE provides a precise control of the epitaxial layer thickness and doping. The resulting layers have an excellent surface morphology. Such a method is used in the fabrication of superlattices. The disadvantages of this method, though, is the sophisticated equipment required and the related high costs.

Some of the weaknesses of LPE are avoided in VPE. A more precise control of the layer thickness can be achieved using VPE. Also a good surface morphology can be obtained (17). A drawback of this method is that it uses toxic gases as the transporting agents. The Close-Spaced Vapor Transport (CSVT) technique used in this study is a modified VPE method which does not have the toxic gases drawback. The CSVT technique was first introduced by an RCA team in 1963 (18). This technique has been used to successfully grow semiconductor films such as Ge (19), Si (20), CdS (21), CdSe (22), CdTe (23), ZnSe (24), HgCdTe (25), $CuInS_2$ (26) and GaAs (27).

1.4 Objectives

Bulk and epitaxial growth of GaAs and $Pb_{1-x}Gd_xTe$ is reported. Bulk GaAs grown using a heat pipe assisted zone melter has been reported previously (28). Crystals of $Pb_{1-x}Gd_xTe$ with nominal Gd concentrations of 0, 1 and 5 % were synthesized using a modified Bridgman method in this investigation.

A CSVT system capable of handling two inch diameter GaAs slices for the epitaxy of GaAs on GaAs and GaAs on Ge was built. The homoepitaxy of semiconducting GaAs on semi-insulating GaAs for large surfaces could prove to be a simple and inexpensive method of obtaining good quality epitaxial layers for the fabrication of GaAs integrated circuits. On the other hand the heteroepitaxy of SC GaAs on Ge is in view of the fabrication of cost effective large surface GaAs solar cells. The CSVT system was tested using small samples of GaAs to gain an understanding and control of the doping mechanism. CSVT of $Pb_{1-x}Gd_xTe$ on KBr substrates was attempted in view of making infrared detectors.

Transport properties measurements were made using Hall effect and deep level transient spectroscopy to characterize the bulk and epitaxial samples prepared in this work.

2.0 EXPERIMENTAL

2.1 Growth of bulk $Pb_{1-x}Gd_xTe$

The $Pb_{1-x}Gd_xTe$ crystals were grown using a modified version of the horizontal Bridgman technique. The horizontal Bridgman method consists of passing the molten semiconductor material through a cooler zone such that solidification occurs along a particular crystal direction. The method used in this research which gave best results consisted of subliming the semiconductor material in the hot zone and condensing or solidifying it in the cooler zone.

2.1.1 Furnace design

A three zone platinum wire furnace on a moving platform was used for the crystal growth. The furnace was a Marshall Platinum-Rhodium High Temperature Tubular Furnace. The heating elements were made of platinum with 20 % rhodium and were capable of attaining temperatures of 1425°C.

Three zones could be controlled in the furnace. Further each zone had a series of taps on the windings to locally shunt sections of the zone. This allowed a considerable adjustment of temperature over the length of the zone. The center zone was controlled using a Barber Colman model 277 P temperature controller. The two external zones were adjusted using variacs (Fig. 5). These three zones were operated to obtain a two zone temperature profile. The hot end of the furnace was closed using a piece of asbestos sheet to minimize the heat loss at that extremity. The temperature of the hot zone was set around the melting temperature of PbTe while the temperature of the cooler zone was adjusted to obtain a temperature gradient in the furnace (Fig. 6).

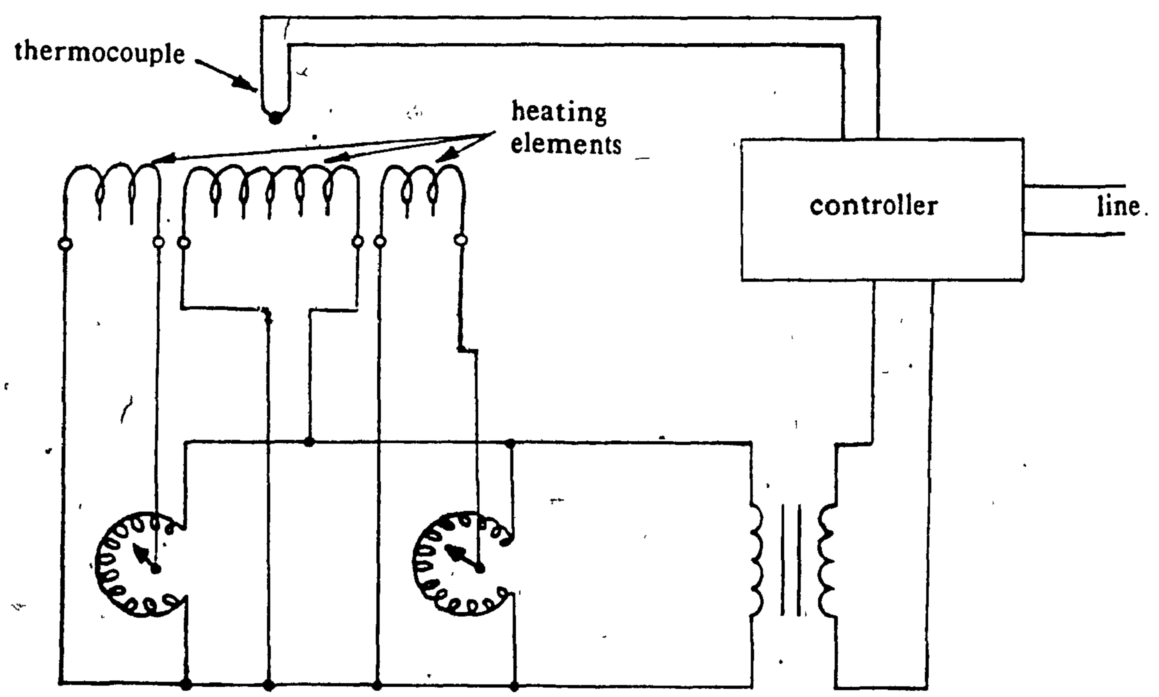


Fig. 5 Electric circuit of the furnace for the $Pb_{1-x}Gd_xTe$ synthesis.

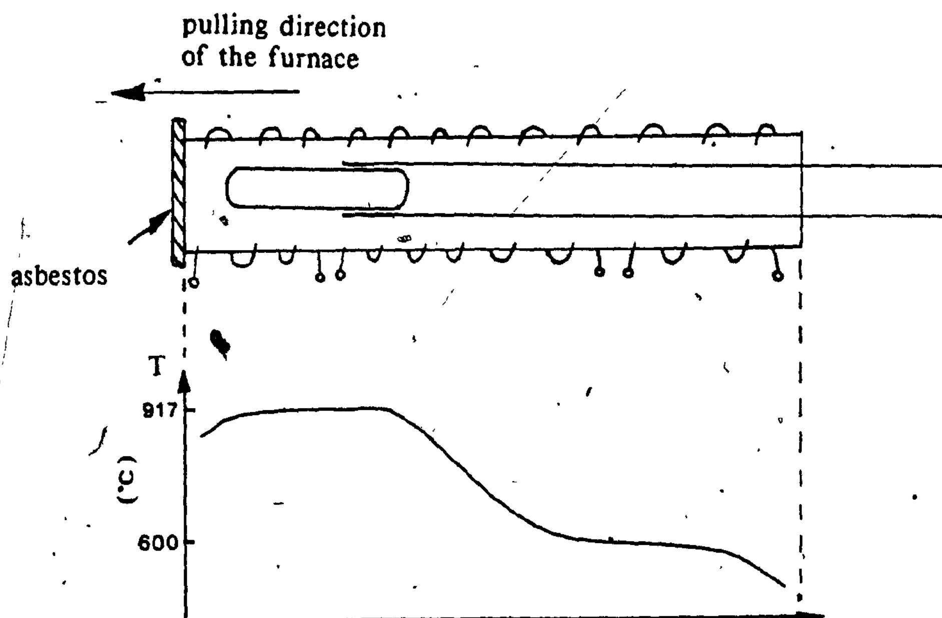


Fig. 6 Furnace temperature profile

Horizontal movement of the furnace was achieved by pulling the furnace platform using a stepping motor. Furnace movements could be made using the reducing gear assembly and infinite screw attached to the platform. The motor used was a Hurst series AS direct drive stepping motor controlled using the Hurst Stepping Motor Controller. The speed of the motor could be controlled using a potentiometer which was added on the control box. Figure 7 shows the circuit for the control of the stepping motor.

2.1.2 Crystal preparation

Crystals of $Pb_{1-x}Gd_xTe$ were synthesized from the basic elements. Stoichiometric amounts of lead (Alpha Products 99.9999%), gadolinium (Alfa Products 99.9%) and tellurium (Noranda high purity grade) were weighed with an accuracy of 0.01 gm. Typical charges weighed 25 gm. Table 2 shows some physical properties of these elements.

TABLE 2: Properties of Pb, Gd and Te

Element	Melting Point	Atomic Weight
Pb	327°C	207.2 gm/mole
Gd	1311°C	157.25 gm/mole
Te	449°C	127.60 gm/mole

The stoichiometric amounts of lead, gadolinium and tellurium were calculated using the following steps.

a) Estimation of the weight of the charge, W (depending on the volume of the fused silica ampule).

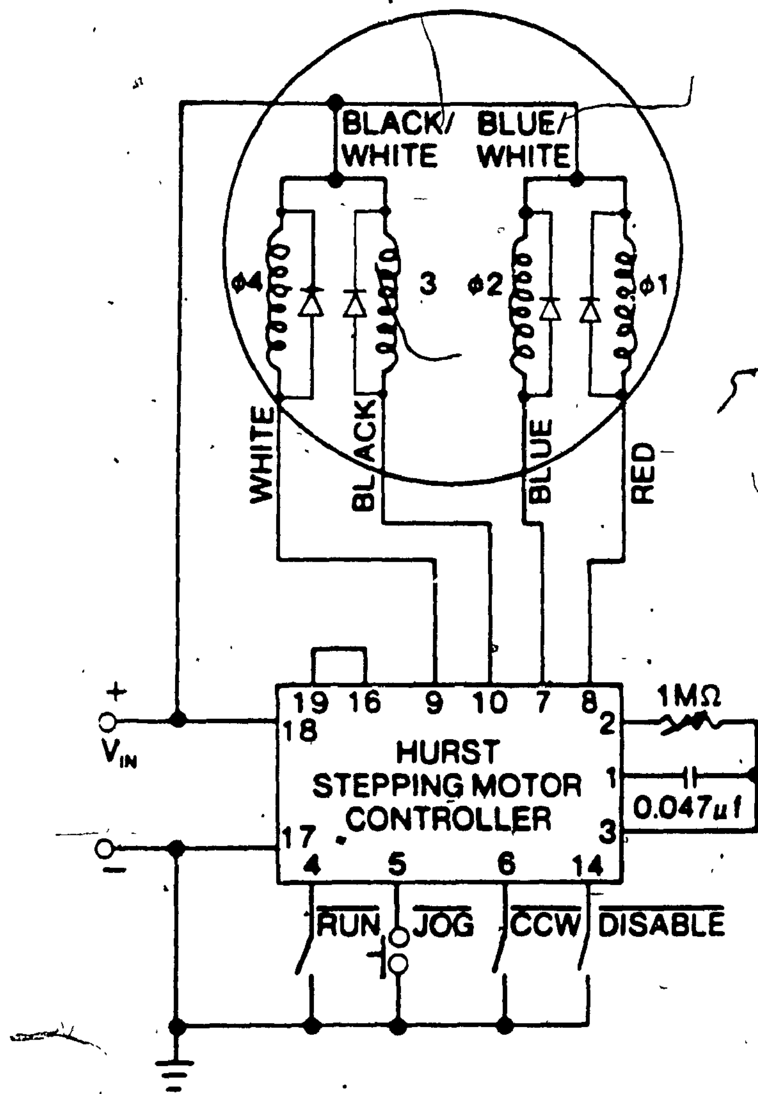


Fig. 7 Stepping motor control

b) Calculation of the required number of moles, M.

$$M = W / ((1-x)207.2 + (x)157.25 + 127.60)$$

(where 207.2, 157.25 and 127.60 are the atomic weights of Pb, Gd and Te respectively).

c) Calculation of the weight of each element is shown in table 3.

TABLE 3: Synthesis Charge Calculation

Element	Amount for the Charge
Pb	M(1-x)207.2
Gd	M(x)157.25
Te	M127.60

The ampules for the synthesis were made of fused silica. The dimensions of these were i.d. 30 mm, o.d. 36 mm and length of 20 cm approximately. They were degreased three times in each of the following solvents: 1-1-1 trichloroethane, acetone and methanol. Subsequently the ampules were etched in a solution of HNO_3:HF:H_2O (1:1:10) for 10 minutes. They were finally rinsed in distilled water and dried in an oven. The ampules containing the elements for the synthesis were rinsed three times with ultra high purity nitrogen and were then sealed under a vacuum of 10^{-5} torr.

2.1.3 Growth conditions

The ampules, supported by a vibration free post, were placed in the hot zone for a period of time varying from 48 hours to 96 hours. The traveling furnace was then pulled at a rate of approximately 6.3 mm/hour. For different syntheses, the temperature of the hot zone was varied around the melting point of lead telluride

(917°C). The variations in the hot zone plateau temperature over the length of the sample was approximately 2°C.

2.2 Epitaxial growth

The CSVT technique can be used for the epitaxial growth of any solid which can react reversibly with a gas. This technique has the advantage of working under atmospheric pressure, using moderate temperature and it can be scaled up (29). The source and substrate are separated by a fraction of a millimeter using a spacer such as fused silica or graphite. The transporting agent is water vapor which is brought into the reaction chamber by a gas via a water saturator. The source and substrate are heated such that the chemical transport from the source to the substrate can be achieved. This is accomplished by establishing a temperature difference, ΔT, between the source and substrate such that the source temperature is greater than the substrate temperature. The close-spacing of the source and substrate ($\simeq$0.3 mm), which is in the range of the mean free path of the reacting species, has many advantages. The reaction is limited at the two surfaces only. This minimizes any side reaction in the gas phase between the source and the substrate. This is similar to the condition of low pressure chemical vapor deposition without the requirement of low pressure. The epitaxial growth is also fast and efficient and is independent of gas flow rates and reactor geometry.

The general characteristics of a CSVT system are as follows. A fused silica reaction chamber with gas inlet and outlet allows the gaseous transporting agent to circulate inside the reactor. The gas inlet is brought near the source and substrate were the mass transport occurs. The source and substrate are placed between graphite blocks which are supported inside the reactor. The graphite blocks act as heat susceptors to homogenize the temperature at the source and substrate. The temperature is monitored

using thermocouples. Finally a heating system provides the necessary energy for the reaction to occur.

The CSVT system designed in this research was based on previous work by D. Coté (29). Coté's system could only handle samples of diameter up to one inch. Hence the design was scaled up to accommodate two inch diameter samples. This required redesigning the reaction chamber as well as the heating system.

2.2.1 Reaction chamber design

The reaction chamber was made entirely of fused silica. The main body of the reactor was made of a square tube of dimensions 6.8 cm by 6.8 cm by 40 cm in length and of wall thickness 2.5 mm. A square tube was used instead of a standard circular tube for the main body to obtain a maximum temperature uniformity inside the reactor. One end of the square tube was closed and the other end was sealed to the male end of a round taper joint of dimensions 58 mm by 70 mm. Figure 8 shows the main body of the reaction chamber.

The inside assembly was made of a heavy walled tube with the following dimensions: inside diameter (i.d.) 30 mm and outside diameter (o.d.) 33.5 mm. One end of this tube was attached to the female end of the taper joint. The other end was closed and two smaller tubes (i.d. 4 mm, o.d. 6 mm), to enclose thermocouples, extended from the end. A rod 11.5 mm in diameter was also attached to this end of the tube to support the graphite blocks. The gas inlet was formed using 4 by 6 mm tubing. The gas inlet tube was brought to the graphite blocks where 10 holes, spaced 15 mm apart, allowed gases to flow between the blocks. The gas outlet was simply a 4 by 6 mm tube extending from the taper joint to the exterior. Figure 9 shows the inside assembly.

The graphite heat susceptors shown in figure 10 were made of Densified Semiconductor grade graphite from Union Carbide. Holes were machined into the blocks to allow the thermocouples to measure the graphite temperature. The dimensions of the blocks are approximately 5 cm by 10 cm by .5 cm (not including the section for the thermocouple.)

2.2.2 Gas system

The gases necessary for the reaction are nitrogen, hydrogen and water vapor. Ultra high purity nitrogen is used for purging the system before and after the epitaxial growth. Ultra high purity hydrogen is used as the carrier gas to bring water vapor into the reaction chamber.

A diagram of the gas system is shown in figure 11. The entire system was built out of 1/4 inch stainless steel tubing and mounted on an aluminum panel. The water saturator was filled with triply distilled water and was placed in an ice bath to obtain the optimal water vapor pressure of 609 Pascals (29). Both the N_2 and H_2 gases were passed through Oxisorb absorbers allowing less than 0.1 ppm of oxygen to go through. The hydrogen was further purified using a palladium diffusion purifier insuring less than 0.05 ppm of oxygen.

2.2.3 Furnace design

Typical furnace requirements for the epitaxial deposition of GaAs is a source temperature of 800°C and substrate temperature of 750°C. Lower temperatures were used for the $Pb_{1-x}Gd_xTe$ epitaxy. To provide the necessary heat, four 1100 watts silicon carbide heating elements spaced two inches apart were used. These were held in position on a moving platform using insulating firebricks. The insulating firebricks also formed the furnace chamber and provided the required

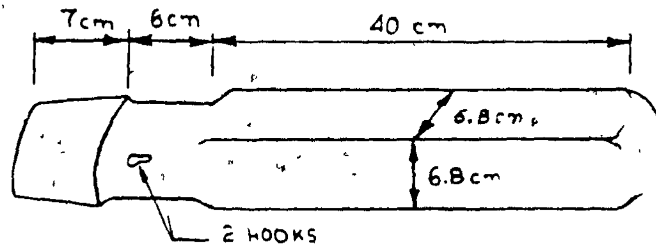


Fig. 8 Reaction chamber main body

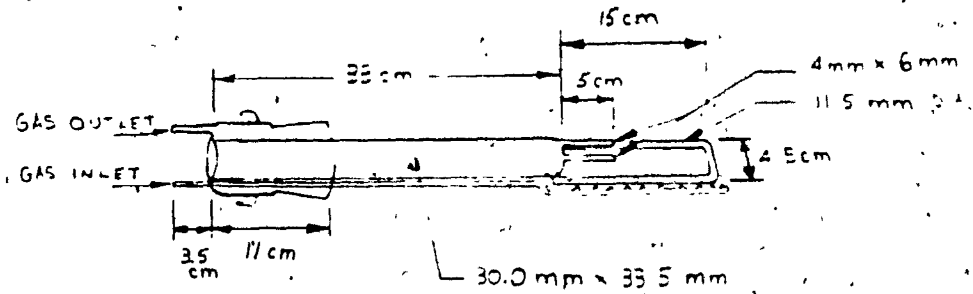


Fig. 9 Inside assembly

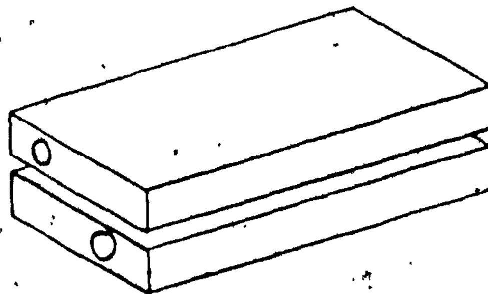


Fig 10 Graphite blocks

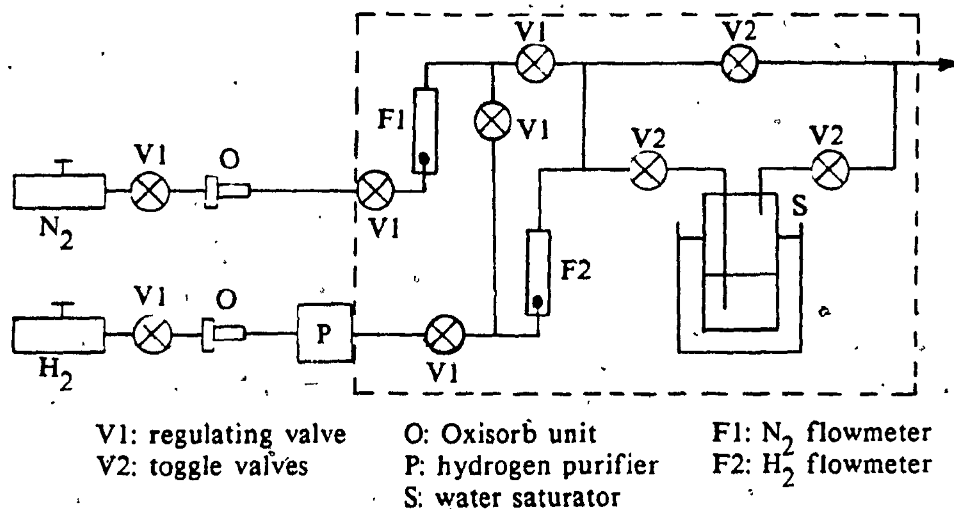


Fig. 11 Gas system

temperature gradient between the source and the substrate. Further control of the temperature gradient was achieved by controlling the flow of air on the top surface of the reactor. A temperature controller was used as the controlling unit of a power controller which drove step down transformers for the heating elements.

2.2.3.1 Temperature controller

The temperature controller was a Barber Coleman model 543 Precision Digital Set Point Controller. Its input was a chromel-alumel thermocouple which was positioned inside the reactor to monitor the temperature of the source.. Its output was a 2-12 mA constant current. The setpoint was adjusted ny means of a 10 turn potentiometer with a readout on a four digit indicator. The control modes were the gain, integral and derivative actions.

2.2.3.2 Power controller

The power controller used was a Barber Coleman series 621 Power Controller. The output dc current, from the temperature controller, was used as the input to the power controller. This dc current controlled the conduction angle of the SCR's in the power controller. Hence the power delivered to the load is proportional to the output of the temperature controller. The ratings of the power controller used are given in table 4.

TABLE 4: Power Controller Ratings

Line voltage	208 V
KVA rating	5.8 KVA
Maximum load amp at 130 °F	28 A

2.2.3.3 Heating elements

Four Globar type SG silicon carbide resistance heating elements from Carborundum Co. were used. These are designed to operate at temperatures up to 1650°C in an air atmosphere. Their resistance to oxidation is excellent and the change in electrical resistance with use is slow and uniform from element to element. Hence great temperature uniformity and stability can be achieved with these elements. The elements used in this design were 25 inches long and had a diameter of 3/4 of an inch. The ends of the heating elements were metalized with aluminum to provide a low resistance path for the terminal connectors.

2.2.3.4 Electric circuit

The electric circuit was designed to accommodate the power requirements of the silicon carbide heating elements. Each element was capable of providing 1100 W of power (APPENDIX B). The required voltage and current of the elements was 40 V and 28 A respectively. Step down transformers were used to bring down the 208 V line voltage to 40 V. The electric circuit is shown in figure 12. Table 5 gives the specifications of the transformers.

TABLE 5: Transformer Specifications

T_1: Hammond class F type: H

primary: 208 V

secondary: 40 V

KVA: 2.4

T_2: General Radio Co. type: 50-A 115 V

KVA: 5

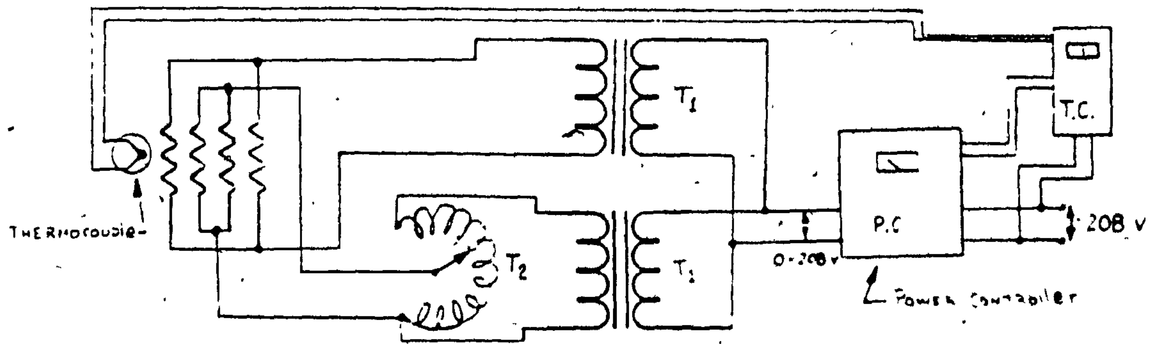


Fig. 12 Electric circuit of the CSVT system

2.2.3.5 Furnace chamber

The furnace chamber consisted of four heating elements held in place using insulating firebricks. The minimum distances, according to specifications, were used between furnace wall and heating elements as well as between heating elements themselves. The arrangement of the heating elements in the furnace is shown in figure 13. Figure 14 shows the complete furnace with an open region to allow room for the reactor.

The temperature uniformity over the length of the graphite blocks was adjusted using the variac on the center elements. A region more than 2 inches in length with a temperature variation of 4°C was obtained (Fig. 15). There was no variations in temperature in the direction parallel to the heating elements over the width of the graphite blocks.

2.2.4 GaAs epitaxial samples

The CSVT system designed was tested using 1 cm^2 GaAs samples. The source and substrate samples were cut from 0.5 mm thick, (100) oriented, undoped semi-insulating (SI) and semiconducting (SC) GaAs wafers, polished on one side, purchased from M/A Com Laser Diode Inc. The resistivity of SI GaAs was in the range of 10^7-10^8 ohm-cm. Si doped wafers had N type carrier concentrations of 1.0-2.0x10^{18} cm^{-3}. Zn doped wafers had P type carrier concentrations of .39-1.0x10^{19} cm^{-3}. The GaAs samples were degreased in hot trichloroethane, hot acetone, hot methanol for 5 minutes and rinsed in distilled water. They were then etched in $NH_4OH:H_2O:H_2O_2$ (6:150:1) for about two minutes which removed approximately a 0.3μm thick layer of GaAs. This etch was preferred to the more common H_2SO_4: H_2O_2:H_2O (5:1:1) solution due to the lower etch rate of the former. The samples were finally rinsed in distilled water and dried with N_2 gas.

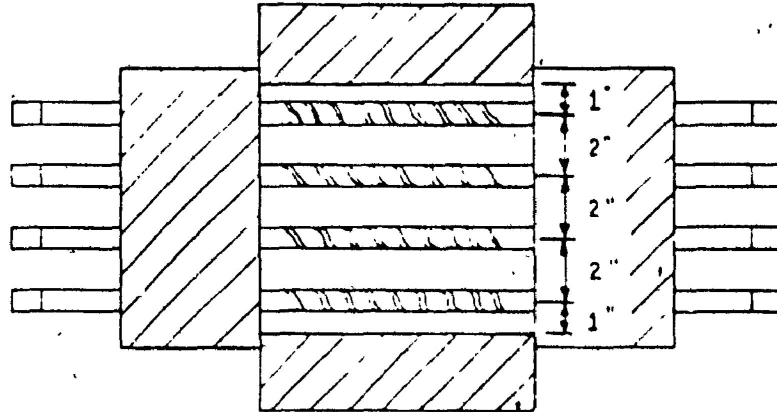


Fig. 13 Position of the heating elements in the furnace

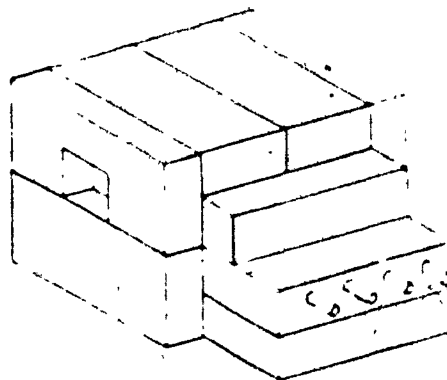


Fig. 14 Furnace chamber

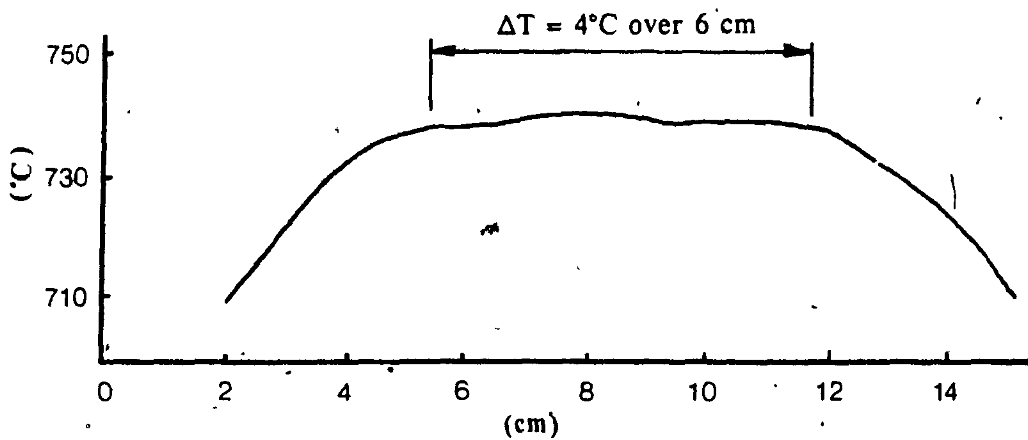


Fig. 15 Temperature variation along the graphite blocks.

2.2.5 $Pb_{1-x}Gd_xTe$ epitaxial samples

Slices of $Pb_{1-x}Gd_xTe$ with 5% Gd were cut from the bulk crystals. These were lapped and polished using 0.3μm alumina powder to a thickness of 1 to 1.5 mm. The substrates used were oriented (100) single crystals of KBr. KBr is a suitable substrate material for the epitaxy of $Pb_{1-x}Gd_xTe$ since its lattice constant is close to that of PbTe, 6.46 Å. Other substrates could have been used as seen in table 6.

TABLE 6: Substrates for $Pb_{1-x}Gd_xTe$ epitaxy.

Material	Structure	Lattice constant	Melting point
KBr	rock-salt	6.58 Å	1007 K
KCl	"	6.29 Å	1043 K
KI	"	7.052 Å	954 K
BaF_2	"	6.184 Å	1628 K
PbTe	"	6.46 Å	1190 K

The $Pb_{1-x}Gd_xTe$ samples were degreased in refluxing acetone for 20 minutes and chemically polished using a brome methanol solution. The KBr substrates were polished using 0.3μm alumina powder and degreased in acetone.

2.2.6 Epitaxial conditions

The spacers used were made of fused silica or graphite. The dimensions were 1cm by 1 cm and 0.3 mm in thickness with a hole, located in the center, of approximately 0.6 cm in diameter. The spacers were cleaned using the same procedure as for the GaAs sources and substrates.

Prior to the depositions the reactor was degassed at approximately 800°C for 1 hour under dry H_2 gas at a flow rate of 500 cc/min.

The samples were first introduced in the open reactor. The source, facing up, was placed on the bottom graphite block. The spacer was positioned over the source and the substrate, facing down, was placed on top of the spacer. The top graphite block was then positioned over the samples and the reactor was closed (Fig. 16).

Nitrogen was circulated in the reactor at a flow rate of 500 cc/min for 20 minutes. Dry hydrogen was then introduced for 10 minutes at a flow rate of 350 cc/min. The pre-heated furnace was then placed under the reactor and wet hydrogen was circulated by passing the hydrogen gas through the bubbler. For GaAs, typical source temperatures of 850°C were obtained within 15 minutes. For $Pb_{1-x}Gd_xTe$, typical substrate temperatures of 650°C were used. Once the temperature was reached a 30 minute deposition was made. A ΔT of 20 to 40°C was maintained during the deposition. Once the reaction time was over, dry hydrogen was circulated through the system for 10 minutes. Finally nitrogen was circulated in the reactor until the sample temperature was near room temperature.

2.3 Transport properties measurements

2.3.1 Ohmic contacts on GaAs

Ohmic contacts were made by soldering small pieces of indium on the samples using a fine tip soldering iron. The samples were then annealed at 500°C for 1 1/2 minutes under a hydrogen atmosphere. The ohmic behavior of the contacts was verified on a curve tracer.

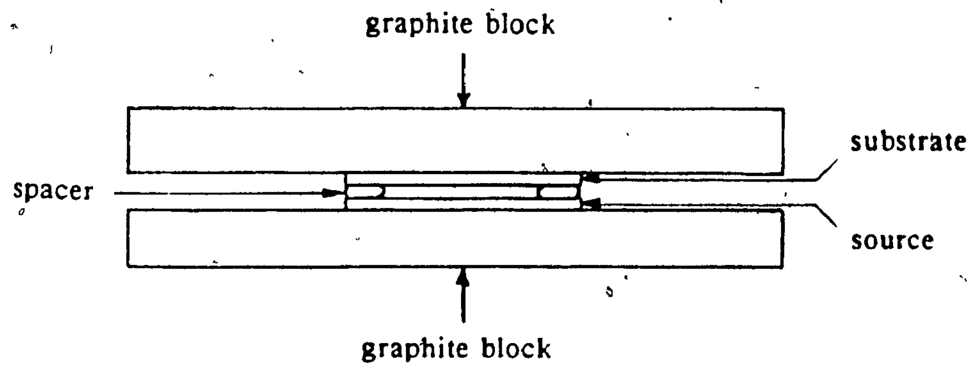


Fig. 16 Position of the samples for the epitaxy

2.3.2 Ohmic contacts on $Pb_{1-x}Gd_xTe$

Contacts were made on the samples using indium. The indium was applied using a fine tip soldering iron. The ohmic contacts were verified on a curve tracer.

2.3.3 Hall effect on bulk samples

Hall effect measurements were made on the bulk crystals to determine the type, concentration and mobility of the majority carriers. $Pb_{1-x}Gd_xTe$ samples were cut using a wire saw into parallelepiped specimens according to the ASTM F76-84 standard (30). The dimensions of the samples were on average 1 by 2 by 10 mm. They were polished using 27 μm alumina abrasive power on a glass plate to achieve the required tolerances. The samples were then etched in H_2O_2:KOH:Ethylene Glycol (1:5:5) for 30 minutes followed by a rinse in distilled water. The dimension of the samples were measured to an accuracy of 0.01 mm using a traveling microscope. Figure 17 shows a typical bulk sample.

A computerized system for Hall effect was set up to perform automatic measurements as a function of temperature. The equipment consisted of an IBM PC compatible computer with an IEEE 488 interface and a 10 Mbyte hard disk, a 5 KGauss magnet, a cryogenic dewar, a scanner, a current source and a voltmeter. Measurement sequencing was made according to the ASTM F76-84 standard (30). Programming of the instruments was made in basic. A flowchart of the program is shown in figure 18. APPENDIX C contains a listing of the program.

The samples were cooled to liquid helium and measurements were initiated. For every 5 degree increase in temperature a new measurement is made. The data acquired and stored on the hard disk consisted of the measurement number, temperature, current through the sample, resistivity, hall coefficient, carrier

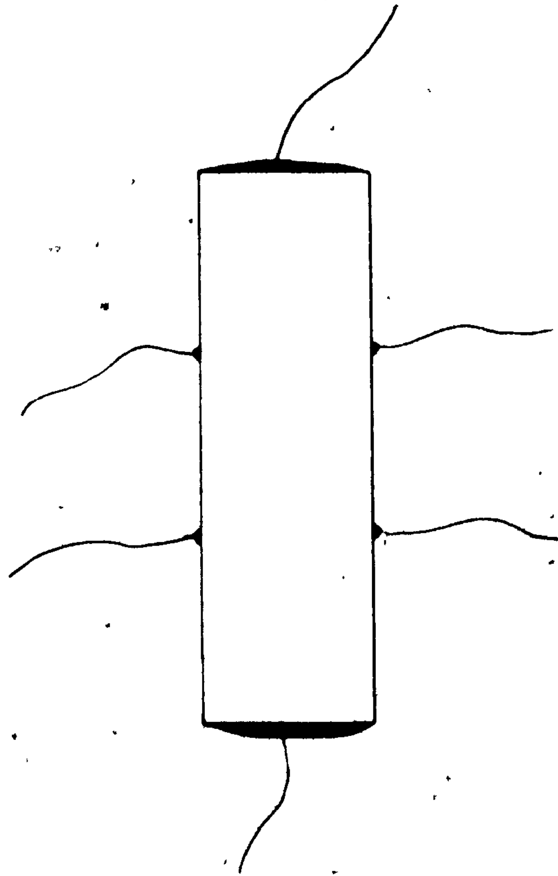


Fig 17 Bulk sample for Hall effect

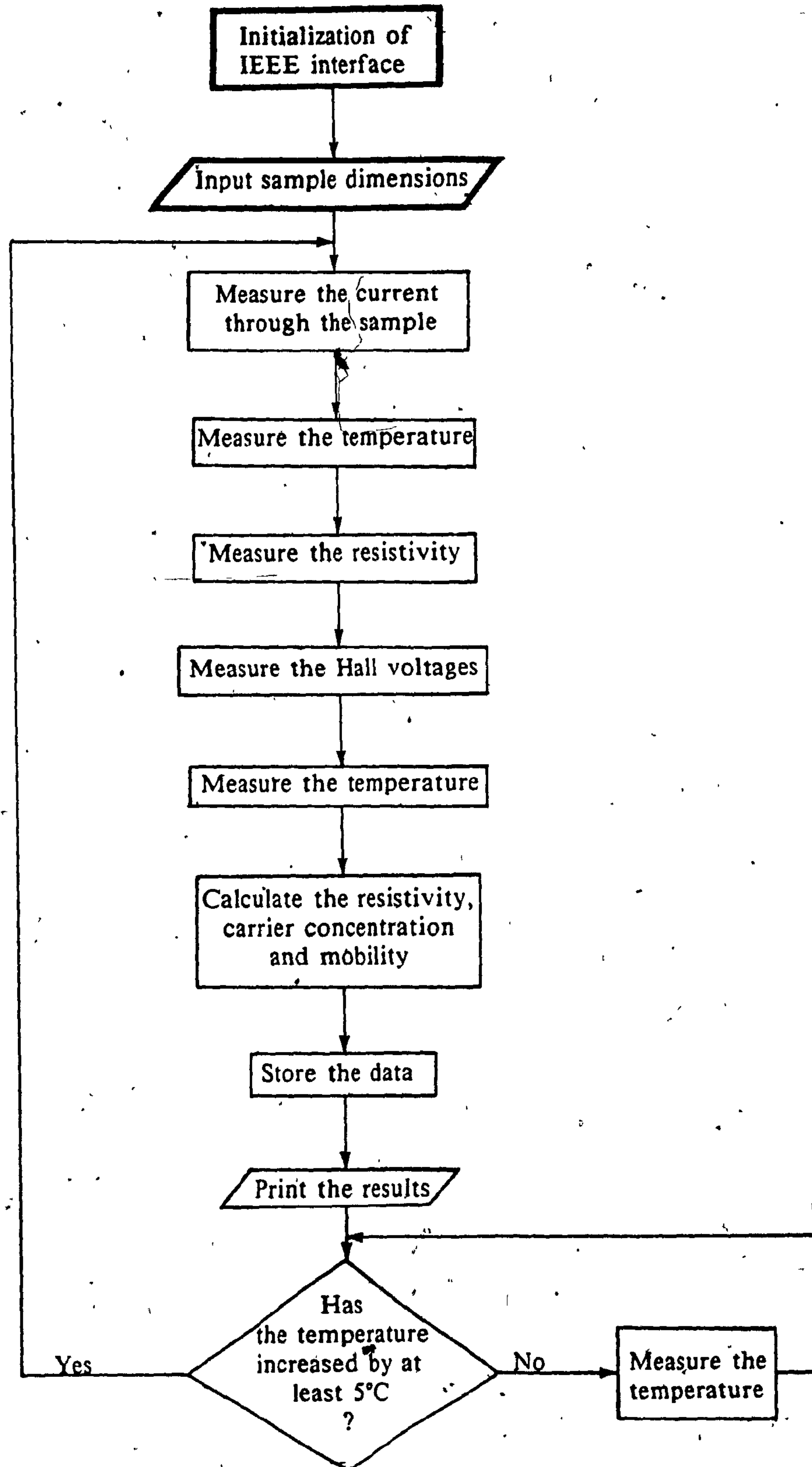


Fig. 18 Flowchart of the Hall effect program for bulk samples

concentration, mobility and magnetic field. Temperature measurements were made using a platinum resistance thermometer. The variations in the measured resistance of the platinum sensor were converted to temperature values using a calibration formula in the program. The conversion formula used in the program was:

$$T = (R2-A)/B$$

where T is the calculated temperature, R2 is the measured resistance and A and B are constant coefficients. Magnetic field measurements were made using a calibrated GaAs sensor. The Hall effect data was saved on the hard disk for later retrieval to plot graphs and to perform further analysis.

2.3.4 Hall effect on epitaxial samples

The Van der Pauw method (31) was used according to the ASTM F76-84 standard method for measuring hall mobility and coefficient for thin semiconductor layers (30). This method can be applied to lamellar samples of arbitrary shape given that the following conditions hold:

a) the contacts are at the circumference of the sample,

b) the contacts are sufficiently small,

c) the sample is homogeneous in thickness,

d) the sample does not have isolated holes.

The data compiled was analyzed using the electronic spreadsheet LOTUS 123 to calculate the resistivity, carrier concentration and mobility. The measured currents, voltages and magnetic field for a given sample under test were entered in specific columns of the spreadsheet. Formulas for the computation of the carrier concentration and mobility were also entered and the results were shown in the corresponding columns.

2.3.5 Deep Level Transient Spectroscopy

Deep Level Transient Spectroscopy (DLTS) is a measurement technique used to evaluate the ionization energies and the concentration of deep levels in semiconductors. This technique requires a P-N junction or Schottky diode for the measurement.

Impurities or defect structures in a semiconductor crystal introduce energy levels within the bandgap. These energy levels can be classified as shallow or deep depending on their ionization energies. A shallow level is located near either the conduction band (donor level) or the valence band (acceptor level). Shallow levels require very low thermal energies to become ionized. Deep levels, on the other hand, are located near the center of the bandgap and require higher thermal energies to become ionized. As an example, Si is a shallow donor in GaAs; its ionization energy is approximately 0.002 eV and at 77 K it is completely ionized. The EL_2 defect structure in GaAs (As atoms in the Ga atom position, As_{Ga}) is a deep donor level whose ionization energy is approximately 0.76 eV and which becomes ionized around 350 K.

The DLTS technique uses the change in capacitance of the biased junction due to an electrical stimulation as a basis for the measurement. Capacitance transients are measured as a function of temperature. As the temperature increases, more levels become ionized. These ionized levels modify the aspect of the capacitance transient since more free carriers are generated. From these changing capacitance transients, the concentration and energy levels of the impurities or defect structures can be calculated (32).

3.0 RESULTS AND DISCUSSION

3.1 GaAs results

The doping mechanisms of the epitaxial growth of GaAs on semi-insulating GaAs substrates were investigated. To accomplish this task, the following growth parameters were studied.

- The temperature difference, ΔT, between the source and substrate, during the heating up time and during the deposition was compared to the quality of the epitaxial surface finish.
- The substrate temperature, T_{sub}, was varied from 720°C to 880°C to see the evolution of the carrier concentration and mobility with the substrate deposition temperature.
- The spacer was changed from fused silica to graphite to see if the doping mechanism was influenced by the spacer material.
- The source material was changed from SI GaAs to Zn doped GaAs and Si doped GaAs to see the effect on the carrier concentration and mobility.

Other parameters such as the partial pressure of H_2O and the spacer thickness have been investigated previously (29).

Epitaxial depositions of GaAs with mirror smooth surface finishes were obtained reproducibly. Such mirror smooth finishes of CSVT grown GaAs layers on (100) oriented GaAs substrates have been oriented using x-ray diffraction (29). It was reported that these layers were also oriented in the (100) direction. Mirror finishes could be obtained by controlling the temperature gradient between the source and the

substrate during the temperature rise in the reactor. From the data compiled it could be seen that ΔT during the temperature rise (ΔT_{rise}) must be greater than ΔT during the deposition (ΔT_{dep}) to achieve mirror finishes. The collected data is shown in table 7.

TABLE 7: Influence of ΔT on the Surface Finish of the Epitaxial Depositions

Substrate Temp (°C)	ΔT_{rise} (°C)	ΔT_{dep} (°C)	Mirror finish
730	40	74	no
"	58	30	yes
"	73	74	no
750	40	52	no
"	65	50	yes
"	40	40	no
770	40	30	yes
"	40	70	no
800	55	34	yes
"	40	40	no

Hall effect measurements were made on the epitaxial layers. Figure 19 shows the free carrier concentration (n) and mobility (μ) at 300 K versus the substrate temperature. Figure 20 shows n and μ at 77 K versus substrate temperature. All of these depositions were N type. This investigation was made using semi-insulating sources and substrates, a fused silica spacer and a ΔT_{dep} of 30°C.

Figure 21 shows the Hall mobility versus impurity concentration at 300 K. The theoretical curve for bulk GaAs drift mobilities was also plotted. The Hall mobilities

are larger than the drift mobilities by a factor between 1 and 2 depending on the scattering mechanisms. The experimental data for the CSVT epitaxial GaAs agrees relatively well with the theoretical data for bulk GaAs.

To verify the presence of deep levels in these depositions, such as the EL_2 which is present in most bulk and epitaxial grown GaAs, a simple graphical plot was made. The presence of the EL_2 deep level and the absence of EL_2 in bulk GaAs was shown by Lagowski (33) using a graphical plot of the ratio of n at 300 K (n_{300}) to n at 77 K (n_{77}) versus n_{300}. His data was plotted in figure 22 along with the CSVT experimental data for undoped SI GaAs sources on undoped SI GaAs substrates using a fused silica spacer. At 77 K only the shallow levels are ionized and contribute to the total free charge carrier concentration. If there is no EL_2 or other deep levels, the total free charge carrier concentration at 300 K will be the same as at 77 K since no other level will be ionized. On the other hand if there is the EL_2, then at 300 K, in addition to the ionized shallow levels, the arsenic vacancies, V_{As}, associated with the EL_2, become ionized. Hence n_{77} should be less than n_{300} if the EL_2 deep level is present.

The source of shallow donors in the epitaxial layers is still under investigation. However, since the source and substrate were both undoped SI GaAs, the shallow donor impurities could not have come from there. Two possible sources for the shallow donor impurities are Si from the fused silica reactor or the fused silica spacer. The fused silica reactor as a source of Si impurities has been reported (34). Hence the fused silica spacer as an additional source of the shallow impurities was investigated. The fused silica spacer was changed to a graphite spacer of the same dimensions. The results are shown in table 8.

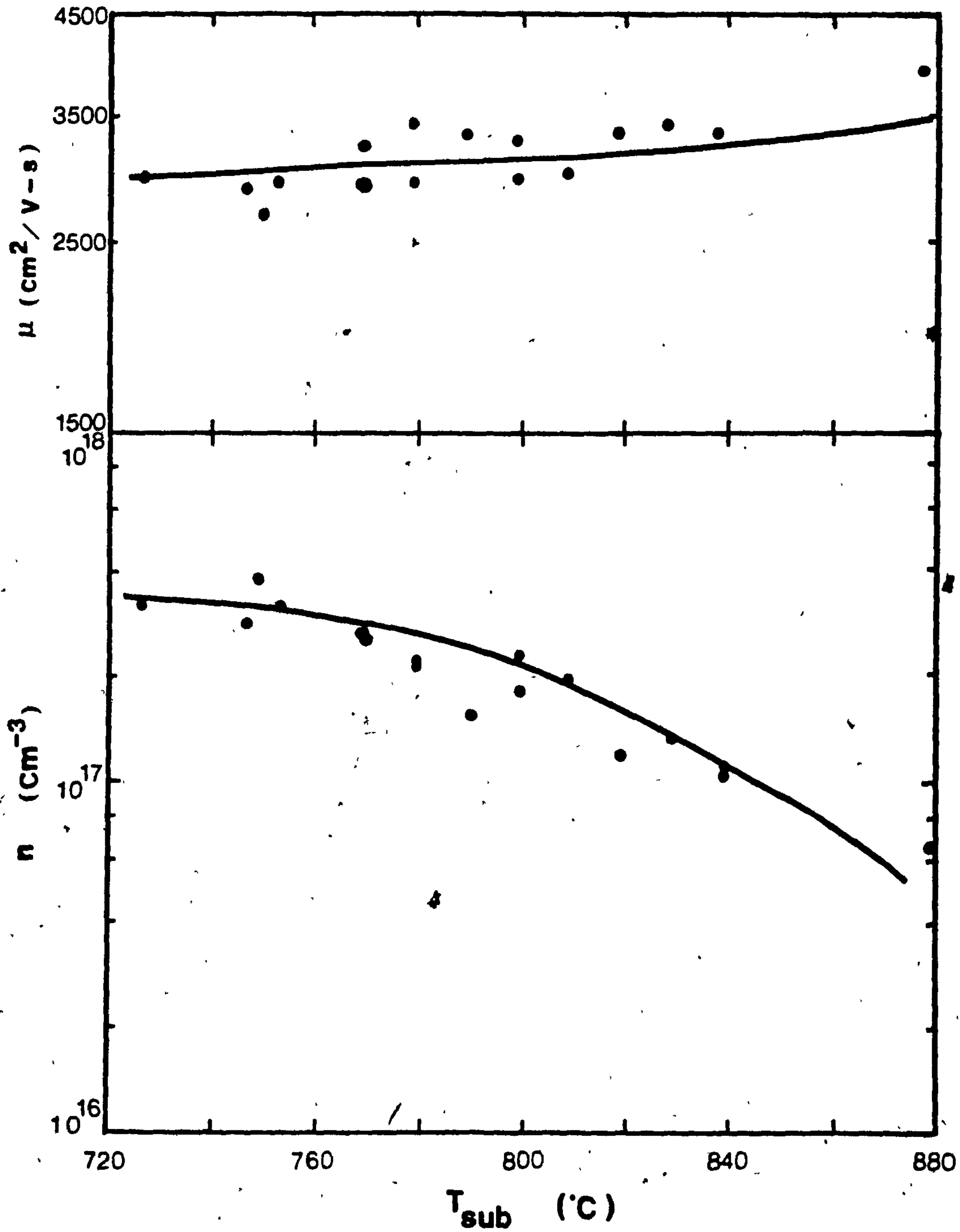


Fig. 19 n and μ at 300 K versus substrate temperature for undoped SI GaAs sources and substrates and using a quartz spacer.

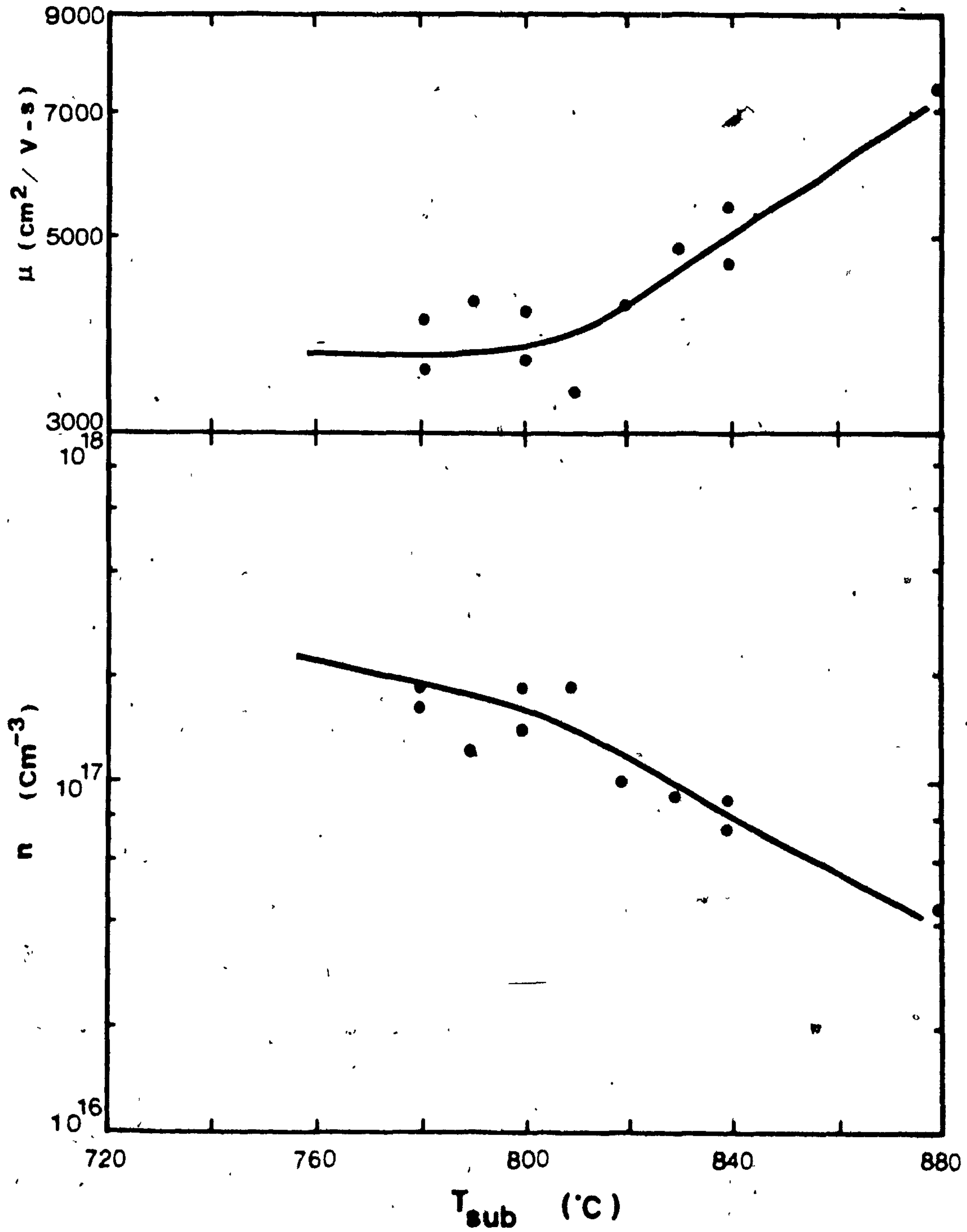


Fig. 20 n and μ at 77 K versus substrate temperature

for undoped SI GaAs sources and substrates and using a quartz spacer

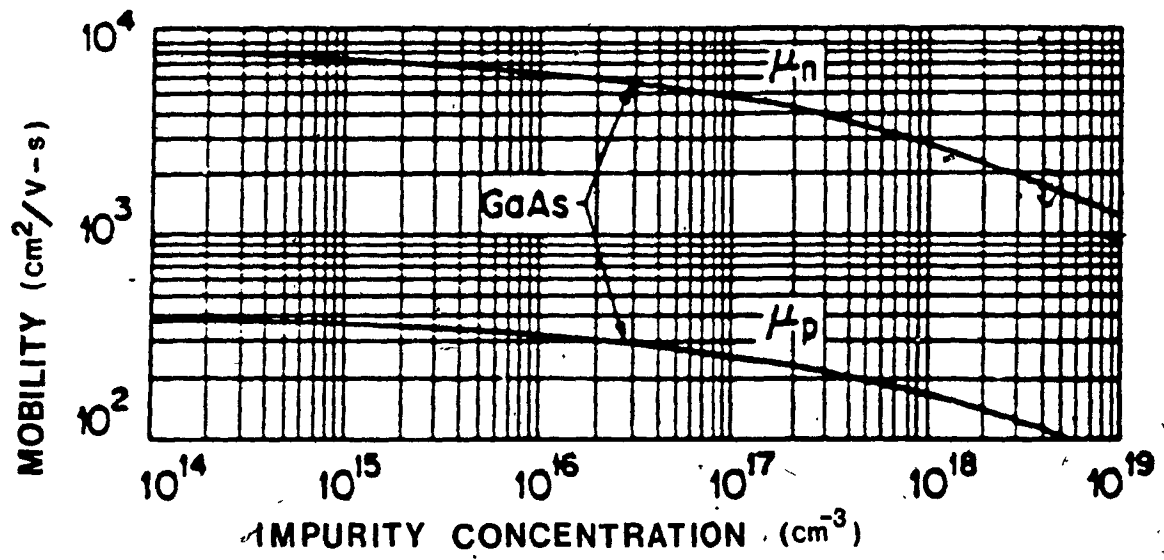


Fig. 21 μ versus n at 300 K (35)

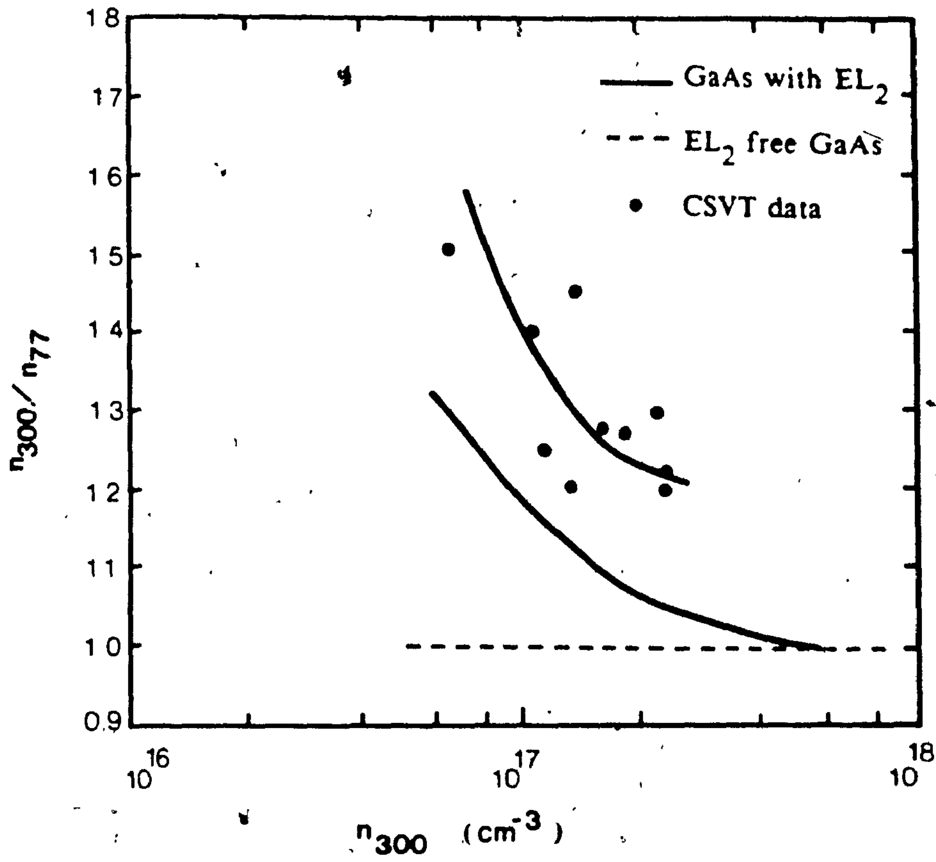


Fig. 22 n_{300}/n_{77} vs. n_{300}

TABLE 8: Fused silica versus graphite spacer

Source	Quartz spacer		Graphite spacer	
temperature	n (cm^{-3})	μ (cm^2/V-s)	n (cm^{-3})	μ (cm^2/V-s)
750°C	3.3×10^{17}	2980	3.4×10^{16}	3300
800°C	2.3×10^{17}	2940	6.1×10^{16}	3030
840°C	1.1×10^{17}	3290	8.6×10^{16}	3070

To further understand the doping mechanism, the undoped SI GaAs sources were replaced by Zn doped GaAs sources. The carrier concentrations and mobilities measured in these epitaxial layers are listed in table 9.

TABLE 9: Characteristics of GaAs epitaxial layers using Zn doped sources

Subs. temp.	n (cm^{-3})	μ (cm^2/V-s)
808°C	6.2×10^{15}	1980
808°C	8.5×10^{15}	2800
820°C	5.4×10^{15}	2600

Although Zn is a shallow acceptor in GaAs (Fig. 4), the epitaxial layers were n type. Even though the carrier concentrations were low, the mobilities were not as high as expected. This indicates a certain degree of compensation or the result of parasitic side reactions.

Si doped sources were also used in the investigation. Unfortunately no ohmic contacts could be obtained on the epitaxial layers. Hence no electrical characterization could be made.

3.2 GaAs discussion

The decrease in carrier concentration, increase in mobility and increase in deep level concentration as the substrate temperature increased (Fig. 15) is similar to the results obtained by many authors (36, 37, 38, 39) where the As/Ga ratio was the parameter varied. This corrolation between the decrease in carrier concentration, increase in mobility and increase in deep level concentration was attributed to the inhibition of a deep level by a shallow donor level. Lagowski et al (40) have reported the annhilation of the 0.82 eV main electron trap in GaAs by shallow donors. These shallow donors were identified as Si, Se or Te. In the case of the CSVT system, Si would be a good candidate since the spacer and the reactor are made of fused silica and no Se or Te are present in any material forming the reactor. Mimiya-Arroyo (34) has attributed the source of shallow donors, in his CSVT system, to Si coming from the fused silica reactor.

The investigation of the spacer as an additional source of shallow donors has proved to be correct. As was shown in table 8, the carrier concentration of the epitaxial layers grown using a graphite spacer were significantly less than those grown using a fused silica spacer. It seems that the additional source of shallow donors could be attributed to Si which could come from the spacer.

For carrier concentrations less than 10^{17} cm^{-3}, which corresponds to substrate temperatures greater than 800°C, the evolution of the deep levels starts to increase rapidly. This was shown in figure 22. The threshold carrier concentration value of 10^{17} cm^{-3} was also exhibited for the annhilation of the EL_2 deep level by shallow donors reported by Lagowski (40). The CSVT epitaxial layers contained deep levels in concentrations greater than the ones reported by Lagowski for the EL_2. Hence the layers contained at least one other deep level other than the EL_2 to account for the

higher deep level concentration. DLTS investigations are under way to confirm and identify the presence and concentration of these deep levels.

The compensation mechanism exhibited by the decrease in carrier concentration with increasing substrate temperature and shown in the n_{300}/n_{77} versus n_{300} plot could explain the N type character of the layers grown using Zn doped (P type) GaAs sources. These layers had low carrier concentrations ($\simeq 10^{15}$ cm^{-3}) with anormally low mobilities (<3000 cm^2/V-s).

To further support the compensation mechanism occurring, a multilevel model based on the Shockley curves and the neutrality condition was used (41). The EL_2 level was used to model the deep level present in the epitaxial layers since it is the most common deep level found in GaAs grown using various methods. The EL_2 deep level is an antisite defect (As_{Ga}) which occurs along with an arsenic vacancy (V_{As}) (42). This structure is called the EL_2 complex. A gallium vacancy (V_{Ga}) filled by an arsenic atom, As_{Ga}, results in 4 covalent bonds and two excess electrons. These two excess electrons form the divalent donor behavior of the EL_2 deep level center. Associated to the antisite is the monovalent shallow donor level, V_{As}, whose concentration is the same as the antisite.

To account for the EL_2 formation in the epitaxial layers, the maximum initial V_{Ga} concentration, which is related to the phase extent of GaAs, was taken to be N_1 = $3x10^{17}$ cm^{-3}. A shallow donor, in this case Si, with variable concentration N_{d1} and activation energy of 0.002eV was included (43). These shallow donors preferentially occupy gallium vacancies. Hence the V_{Ga} concentration available for the formation of antisites is N_1-N_{d1}. Assuming that only a fraction, f, of the unfilled gallium vacancies forms antisites, then the EL_2 concentration is $N_{d2} = f(N_1-N_{d1})$ with an activation

energy of 0.76 eV. The arsenic vacancy concentration is also N_{d2} but its activation energy was taken as 0.025 eV (42). The remaining V_{Ga} left unoccupied are assumed to be deep acceptors and they can be used to compensate the donors. The V_{Ga} concentration is given by $N_{a1} = N_1 - (N_{d1}+N_{d2})$ and its activation energy is 0.25 eV (44). Table 10 summarizes the impurities and defects associated with the multilevel model.

TABLE 10: Multilevel Model Parameters

Impurity or defect	Nature	Concentration	Activation energy
Si	shallow donor	N_{d1}	0.0002 eV
As_{Ga}	deep donor	$N_{d2}=f(N_1-N_{d1})$	0.76 eV
V_{As}	shallow donor	N_{d2}	0.025 eV
V_{Ga}	deep acceptor	$N_{a1}=N_1-(N_{d2}+N_{d3})$	0.25 eV

The fermi level can be determined from the neutrality condition:

$$n + \Sigma N_{a_j}^- = p + \Sigma N_{d_j}^+$$

Where n is the free electron concentration, p is the free hole concentration, $N_{a_j}^-$ is the ionized acceptor concentration and $N_{d_j}^+$ is the ionized donor concentration. The fermi energy is then used as the running index in the computations. When the neutrality condition is satisfied, the fermi level is equal to the fermi energy. The parameters of the neutrality condition are given by the following expressions.

$$n = 2\left(\frac{2\pi m_e kT}{h^2}\right)^{3/2} \exp\left(-\frac{E_g - E_f}{kT}\right)$$

$$p = 2\left(\frac{2\pi m_h kT}{h^2}\right)^{3/2} \exp\left(-\frac{E_f}{kT}\right)$$

$$N_{d_j}^{+} = N_d\left(1 + \frac{1}{g}\exp\frac{E_{d_j} + E_f - E_g}{kT}\right)^{-1}$$

$$N_{a_j}^{-} = N_a\left(1 + g\exp\frac{E_{a_j} - E_f}{kT}\right)^{-1}$$

$$E_g(T) = 1.522 - \frac{5.8\times10^{-4}\,T^2}{T + 300}$$

Where,

$m_e = 0.069m_o$, (density of state effective mass of the electrons)

$m_h = 0.58m_o$, (density of state effective mass of the holes)

$m_o = 0.91095\times10^{-30}$kg, (electron rest mass)

$k = 8.6174\times10^{-5}$eV/K, (Boltzmann constant)

T = absolute temperature

$h = 4.1357\times10^{-15}$eV-s, (Planck constant)

E_f = fermi energy

E_g = bandgap

g = 2, (degeneracy factor)

E_{a_j} = activation energy of the acceptors

E_{d_j} = activation energy of the donors

Taking $N_1=3\times10^{17}$ cm^{-3}, f=0.15, the Si concentration was varied from 3 to 1.5 $\times10^{17}$ cm^{-3}. APPENDIX D shows the different curves obtained. As the Si concentration is decreased, the evolution of the deep levels becomes noticeable for values of $N_{d1}<2\times10^{17}$ cm^{-3}. This is in agreement with the results obtained where the inhibition of the deep level by a shallow donor level was noticed for values of $n > 10^{17}$

cm^{-3}. From the model it was seen that n decreases rapidly as the EL_2 concentration increases.

The process by which Si doping of the epitaxial layer diminishes as the substrate temperature increases is yet unexplained. This phenomena could be related to the increased formation of side reactions involving SiO and Ga_2O at the more elevated temperatures. Reactions of Ga with quartz have been reported (45) and these might help in explaining the observed phenomena. Investigation of this doping mechanism is under way.

3.3 $Pb_{1-x}Gd_xTe$ results

Large diameter bulk crystals were synthesized. The crystallinity of the crystals was investigated as the synthesis temperature was varied. Composition analyses were made to see if the gadolinium was incorporated in the host semiconductor. Finally Hall effect was made on samples of the crystals to determine the type, concentration and mobility of the free charge carriers. Annealing experiments were attempted to improve the low temperature mobilities of the crystals. Epitaxial $Pb_{1-x}Gd_xTe$ on KBr substrates by CSVT was attempted and the results were presented.

The bulk crystals had different crystallinity depending on the synthesis temperature. The crystals grown at the highest hot zone temperature exhibited the largest single crystal grain size or best crystallinity. Most crystals had a uniform shiny texture. Some black deposits were left at the bottom of the ampules after each synthesis. The black, ash like, material had the shape of the gadolinium chips which were used in the synthesis.

An atomic absorption analysis on a sample of $Pb_{1-x}Gd_xTe$ with 1% nominal gadolinium content was made to determine the weight percentage of lead and tellurium

in the sample. The results are shown in table 11.

TABLE 11: Atomic absorption analysis results

	Percentage by weight				Mole fraction
Material	Pb	Te	Unknown	Total	of Pb/Te
Crystal	62.58%	35.35%	2.07%	100.00%	1.09
Black deposit	0%	37.20%	62.80%	100.00%	0

From this analysis a quantitative result of the gadolinium content could not be obtained due to a lack of a gadolinium standard. It can be deduced that the black deposit is a tellurium compound without any lead. It can be said, within experimental error, that there is a slight excess lead in the crystal since the nominal mole fraction of Pb/Te should have been .99. Finally the possibility of gadolinium being present in the crystal exists due to the 2.07% by weight of unknown material.

Further analysis was made using a scanning electron microscope. This revealed the presence of gadolinium in the crystal but in quantities not measurable. Qualitatively it could be seen that there was more gadolinium in the black deposit than in the crystal due to the increased gadolinium peak intensity on the spectrum for the black region.

From these two analyses it could be deduced that the crystals contained gadolinium but in quantities less than the nominal amounts.

Hall effect was made on the bulk $Pb_{1-x}Gd_xTe$ samples. The results are listed in table 12. Crystal No.6 exhibited the highest mobilities at 300 K and 77 K. A complete temperature scan from liquid helium to room temperature was made to find the

maximum mobilities in this crystal. Figure 23 shows the mobility versus temperature relationship for crystal No. 6.

The $Pb_{1-x}Gd_xTe$ epitaxial depositions obtained had inhomogeneous surfaces. The cubic form of the depositions indicate that the growth is epitaxial in the (100) direction. Secondary Ion Mass Spectroscopy analysis made at INSA in Rennes, France, revealed the presence of gadolinium in the deposition but not in a measurable quantity. No electrical characterization of the depositions could be made since contacts on the layers did not adhere properly.

TABLE 12: Bulk Crystal Properties

Crystal		Synthesis	300 K			77 K		
Gd%	No.	Temperature	Type	n (cm^{-3})	μ(cm^2/V-s)	Type	n (cm^{-3})	μ(cm^2/V-s)
5%	1	923°C	P	2.9×10^{18}	600	N	9.5×10^{16}	5000
5%	2	940°C	P	1.2×10^{18}	700	-	-	-
0%	1	928°C	P	1.4×10^{18}	800	P	1.8×10^{18}	3900
1%	A	925°C	N	4.1×10^{17}	1190	N	3.8×10^{17}	31900
1%	B	915°C	N	1.0×10^{18}	1170	N	1.0×10^{18}	26100
1%	3	910°C	N	1.5×10^{18}	800	-	-	-
1%	4	923°C	P	1.3×10^{18}	770	P	1.7×10^{18}	17600
1%	6	907°C	N	4.7×10^{17}	1200	N	5.4×10^{17}	35000
1%	7	902°C	N	5.0×10^{17}	900	N	4.3×10^{17}	22000
1%	8	916°C	P	-	-	-	-	-
1%	9	905°C	N	-	-	-	-	-
1%	10	926°C	P	-	-	-	-	-

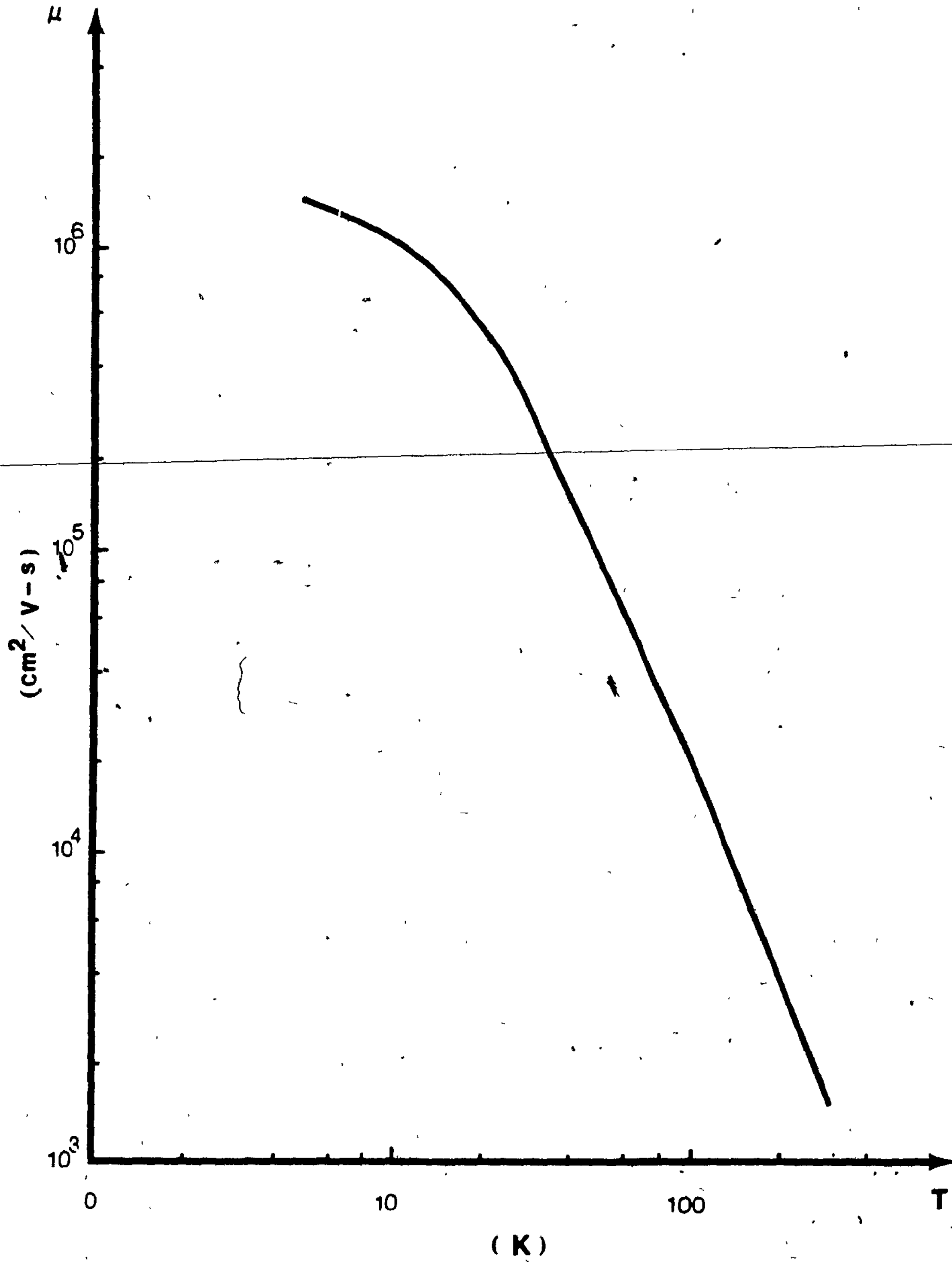


Fig. 23 Mobility versus temperature for $Pb_{.99}Gd_{.01}Te$ crystal No. 6

3.4 $Pb_{1-x}Gd_xTe$ discussion

The temperature dependence of the mobility in the range of 77 K to 300 K for bulk sample No.6 followed the $T^{-5/2}$ law which is characteristic of acoustical phonon scattering (46). This is very close to the $T^{-3/2}$ law for lattice scattering. At low temperatures (4 K) it is well known that the mobility follows the $T^{3/2}$ law characteristic of impurity scattering which usually dominates. In the intermediate temperature range optical phonon scattering influences the total scattering mechanism (47). Crystal no.6 at 4 K had a free carrier concentration of the order of 5.5×10^{17} cm^{-3}. Thus the effect of impurity scattering should have been seen. The large dielectric constant of $Pb_{1-x}Gd_xTe$ crystals (x=.01), ϵ=450 (48), might serve to shield out the electric field of the ionized impurities and defects. Consequently, the impurity scattering occurs only at very low temperatures which might explain the departure from the $T^{-5/2}$ law. The result is an increase in mobility with a decrease in temperature.

The highest mobility obtained was less than the 10^7 cm^2/V-s mobility record reported at 4.2 K. This was thought to be due to the native defects which arise from being slightly off stoichiometric composition. The low temperature mobility would then be controlled by the degree of ionized defect scattering. The various low temperature mobilities can be explained by the degree of compensation due to the native defects (49).

From the PbTe phase diagram (Fig. 24) it can be seen that slight variations in the synthesis temperature have great effects on the stoichiometric composition of the crystals. Crystals grown at slightly lower temperatures than 917°C are rich in Pb This creates Te vacancies which are doubly ionized donors at all temperatures (49) Conversely, a synthesis at a slightly higher temperature will form Pb vacancies which are doubly ionized acceptors at all temperatures

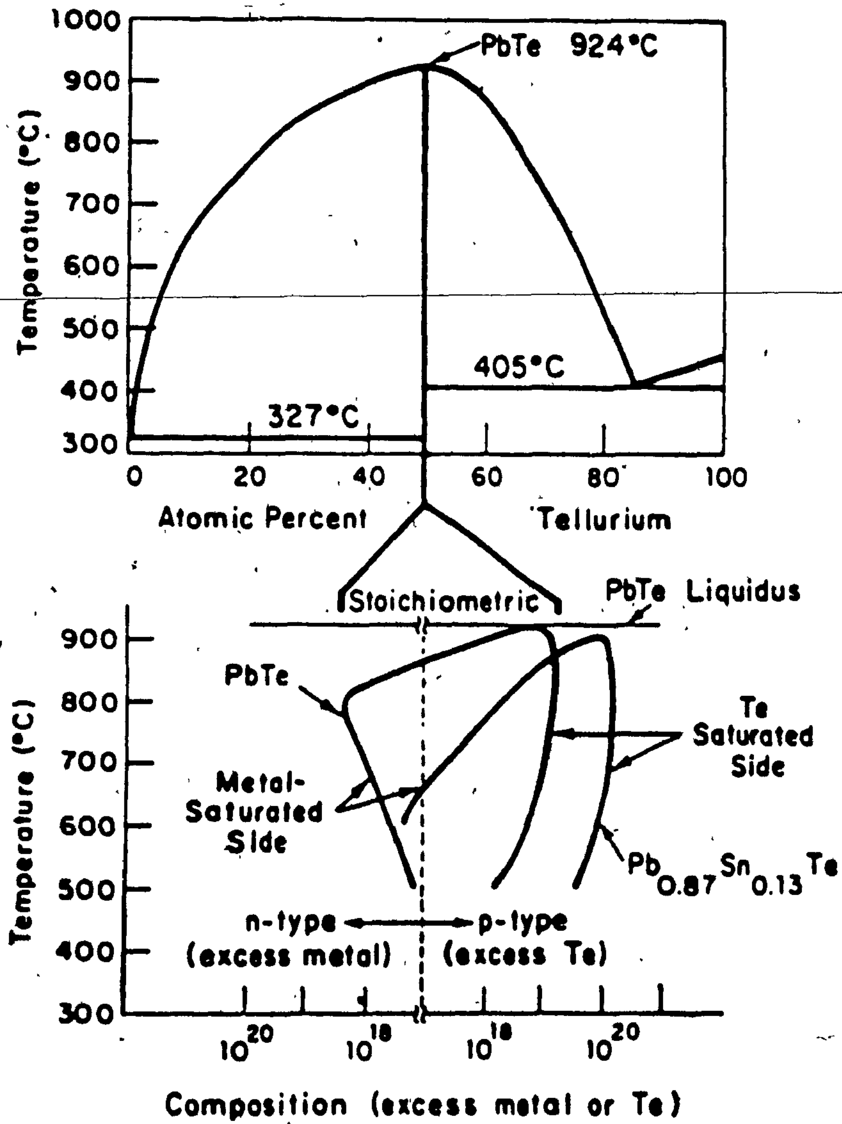


Fig. 24 PbTe phase diagram (50)

The relatively high concentration of vacancies due to slight variations in the synthesis temperatures gives rise to the P or N type character of the crystal. These vacancies are at the origin of the lower mobilities than the ones reported.

To improve the low temperature mobilities, annealing experiments were performed. Attemps were made to re-establish the stoichiometric composition by annealing the N type samples in an excess Te vapor pressure for about 24 hours. Annealing temperatures of 650°C were used. The annealed samples did not exhibit the improved mobility as the ones reported (51, 52). The excess Te coated the samples such that the contacts made on the sample were on the coated layer and not on the semiconductor itself. Hence, the measured carrier concentration and mobility had large percentage errors in them.

The higher mobility of $Pb_{1-x}Gd_xTe$ crystals compared to PbTe, given the stoichiometric composition and hence minimum compensation, is related to the rare earth magnetic ions present in the host lattice. There are three theoretical discussions which can be of value to explain the higher mobility which is related to the spins of the magnetic gadolinium ions. Mobilities related only to the screening of the ionized impurities at low temperatures are comparable to the ones reported for superlattices. The additional effect of magnetic ions in the semiconductor results in mobilities higher than the ones reported in superlattices. The electrons and holes in $Pb_{1-x}Gd_xTe$ both exhibit these high mobilities. Hence, this makes it very interesting for fast CMOS devices.

Gadolinium atoms incorporated in substitutional positions of the lattice form Gd^{3+} ions which participate in the formation of semiconducting sp^3 hybrid bonds and act as donors. The electron shell responsible for the magnetic moment is the $4f^7$ one. The 4f

shell lies deep inside the rare-earth ions. Consequently, the spin-orbit interaction is a dominant phenomenon (2).

Due to the magnetic nature of the gadolinium atoms, the actual field acting on an electron, during a Hall effect measurement, differs from the applied external field. This gives rise to an additional contribution to the Hall potential which is called anomalous Hall effect (53). The origin of this effect is caused by the spin-orbital interaction. The Hamiltonian describing this interaction consists of two terms. The first corresponds to the interaction of the orbit of an electron with its own spin, and the second corresponds to the spins of all other electrons. The second term corresponds to the Lorentz force acting on a conduction electron because its spin located at a point g, being a magnetic dipole, sets up at point r a magnetic field,

$$H_g(\mathbf{r}) = -2\mu_B \nabla' \{[\mathbf{S}_g \cdot (\mathbf{r} - \mathbf{g})] / | \mathbf{r} - \mathbf{g} |^3\} \quad (54)$$

This effect can be interpreted as electron scattering. This scattering probability is anisotropic: the frequency of electron transitions to states with a definite direction of the momentum becomes greater than that of transitions to states with an opposite direction of the momentum.

The role of anomalous Hall effect increases with the growth of the mean electron kinetic energy. It can be suggested that the electrons in PbTe might have large kinetic energies related to the high mobilities at low temperature. This would then favor large anomalous Hall effect when gadolinium atoms are introduced, explaining the higher mobility than for PbTe. Also the anomalous Hall effect has been argued to be favorable in narrow-band semiconductors, making $Pb_{1-x}Gd_xTe$ a good candidate to exhibit this effect (53).

On the other hand, Mycielski (55) discusses the formation of a superlattice of ionized resonant donors or acceptors in semimagnetic semiconductors to explain their abnormally high mobilities. These high mobilities can be interpreted by taking into account the correlation of the position of the ionized donors due to their mutual Coulomb interaction. If a small fraction of the total number of impurities is ionized then the screened Coulomb interaction between the ionized impurities, at low temperatures will induce a correlation of their position resulting in a tendency to be rather distant from each other. This leads to a kind of "crystallization" (ie. formation of a superlattice of ionized donors.) This results in abnormally high carrier mobilities at low temperature.

This treatement was used to explain the measured electron mobilities in HgFeSe (56, 57). It is expected that this treatement can also be applied to other semimagnetic semiconductors such as $Pb_{1-x}Gd_xTe$.

Finally Kondo (58) explains anomalous scattering due to s-d interactions. It was found that small traces of magnetic impurities caused a resistance minimum and this is related to the spin flip interactions of the electrons.

4.0 CONCLUSION

The doping mechanism of GaAs epitaxial layers by CSVT has been investigated. Good quality surfaces were obtained reproducibly. The investigation consisted of finding the influence of certain deposition parameters on the electrical characteristics, such as the free charge carrier concentration and mobility, of the epitaxial layers. The substrate temperature was varied from 720°C to 880°C. The spacer was changed from fused silica to graphite and finally different GaAs sources were used for the reaction. These investigations have all lead to the conclusion that there is a shallow donor in the epitaxial layers which is suspected to be Si coming from the fused silica spacer. A deep level is also present in the epitaxial layers but its nature is yet to be found. A definite evolution of the deep levels and degree of compensation was observed as the parameters under investigation were varied. The compensation mechanism explaining the rather low mobilities at lower carrier concentrations was verified using the multilevel model and Shockley curves.

Further investigation of the doping mechanism could be made by performing DLTS measurements on the samples of this study to correlate all the data in view of controlling the doping of the GaAs epitaxial layers. From there, large area depositions could be attempted for the fabrication of circuits on low cost good quality GaAs epitaxial layers.

The $Pb_{1-x}Gd_xTe$ deposited layers were epitaxial but with inhomogeneous surfaces. A growth rate slightly lower during the epitaxy might solve the inhomogeneous surface problem. Lower growth rates could be achieved by increasing the spacer thickness (29).

The bulk $Pb_{1-x}Gd_xTe$ crystals synthesized had good crystallinity but slightly lower mobilities than expected. This was explained by a certain degree of compensation due to the slight off-stoichiometric composition. Also the low temperature mobilities, expected to be higher than for PbTe, were explained using the spin-orbit interaction of the magnetic gadolinim ions. These very high mobilities at low temperature are larger than the ones reported for the costly superlattice structures. Hence $Pb_{1-x}Gd_xTe$ devices could prove to be good competitors to superlattices at cryogenic temperatures

APPENDIX A: Properties of GaAs, Si and PbTe (300 K)

Property	GaAs	Si	PbTe
Melting point (C)	1238 (59)	1410 (60)	917 (61)
Density (gm/cm^3)	5.32 (62)	2.34 (60)	8.164 (61)
Crystal structure	Zincblende (62)	Diamond (62)	Rock-salt (63)
Energy gap (eV) (300 K)	1.424 (62)	1.12 (62)	0.3 (64)
Transition	Direct (64)	Indirect (64)	Direct (64)
Intrinsic carrier concentration (cm^{-3})	1.79×10^6 (62)	1.45×10^{10} (62)	-
Intrinsic resistivity (ohm-cm)	10^8 (62)	2.3×10^5 (62)	-
Lattice constant (Å)	5.6533 (62)	5.43095 (62)	6.46 (63)
Mobility (drift) ($cm^2 v^{-1} s^{-1}$)			
electrons	8500 (65)	1500 (65)	6000 (64)
holes	400 (65)	450 (65)	4000 (64)

APPENDIX B: Electrical requirements for Globar heating elements

The Globar type SG silicon carbide electric heating elements have positive resistance characteristics above 649°C as shown in figure 25. For calculation purposes, a nominal value of the resistance is taken at 1960°F (1071°C).

The recommended watt loading curve of SG type Globar elements is shown in figure 26. The total radiating surface area of the elements can be calculated using the following expression:

$$S = 2\pi rhn$$

Where,

r: is the radius of the heating elements (0.375 inch),

h: height of the spiral strip (0.75 inch),

n: number of turns of the spiral strip (7.25).

Hence S= 12.81 inches^2.

The recommended watt loading for a chamber temperature of 800°C (1472°F) is 70 W/in^2. Hence the recommemded power per heating element is 897 W.

The electrical requirements for one element can then be calculated. Using the nominal resistance value, given in the heating element specifications, as 1.4 ohms, the voltage and current necessary can be found.

V = 35 volts I = 25 amps.

A slightly higher voltage was used since only 40 V transformers were available. Hence,

V = 40 volts, I = 28 amps and W = 1120 watts.

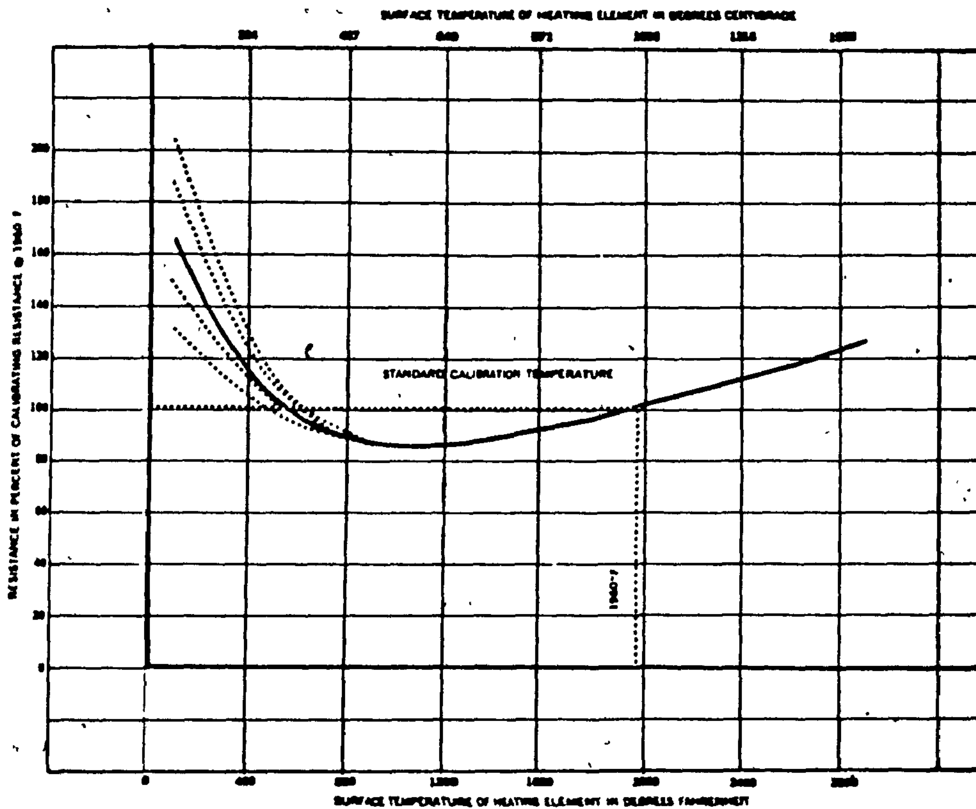


Fig. 25 Resistance temperature characteristics (66)

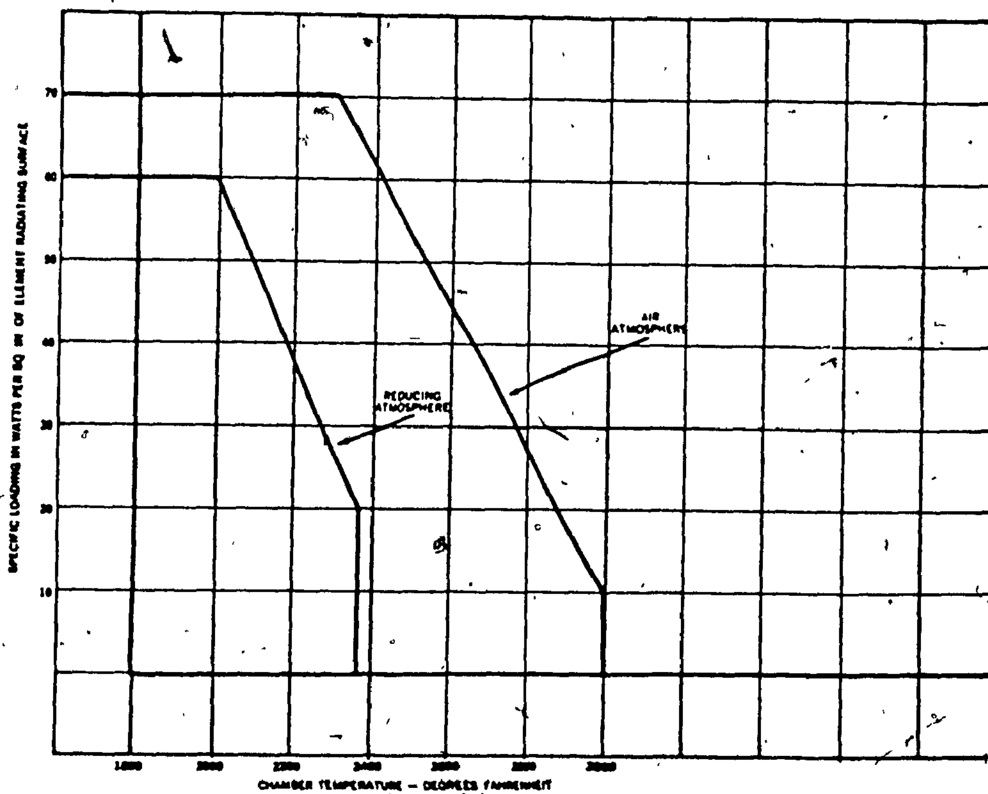


Fig. 26 Recommended watt loading (66)

APPENDIX C: Hall effect program for bulk samples

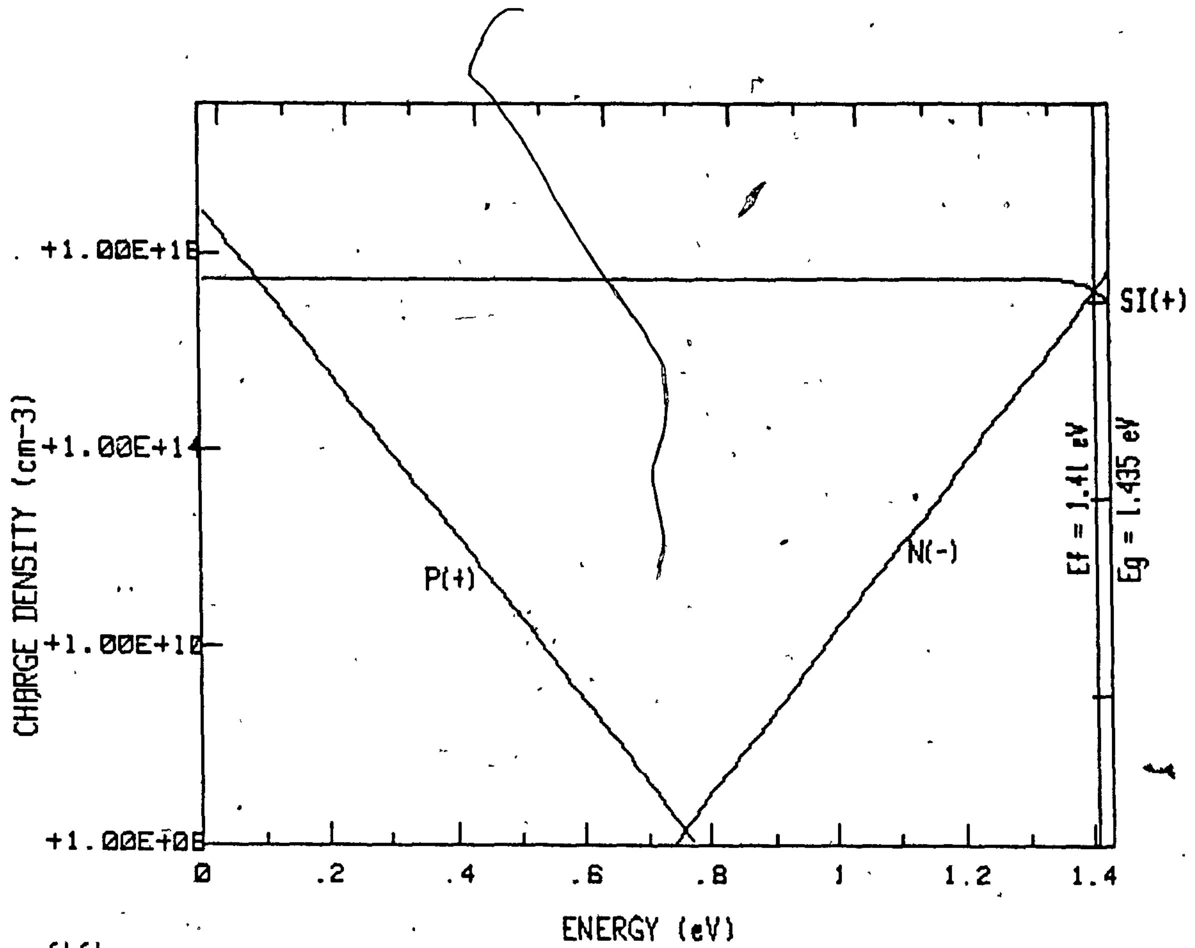
```
10 '            PROGRAMME "AUCAR6" POUR DES MESURES A 6 CONTACTS
20 '
30 CLEAR
40 DEF SEG=&HC400              ' Adresse en mémoire des routines de l'interface
50 INITIALIZE=0 : SEND=9 : ENTER=21        ' Offset des routines
60 SCANNER%=9 : VOLTMETRE%=22              ' Adresse des instruments
70 '
80 '— Initialization de l'interface IEEE-488
90 '
100 IEEE488%    = 21            ' Adresse de l'interface IEEE-488
110 CONTROLLER% = 0             ' Défini l'interface comme contrôlleur du système
120 CALL INITIALIZE (IEEE488%,CONTROLLER%)
130 '
140 KEY OFF : CLS
150 D$="C:\HDATA\" : DELAI=10 : M=10  : L=6 : DIM U(14), T(8)
160 LOCATE 1,20 : PRINT "EFFET HALL POUR 6 CONTACTS"
170 LOCATE 2,1 : INPUT "Nom du fichier (max. 8 car.): ",F$
180 OPEN D$+F$+".DAT" AS #1 LEN=8
190 FIELD #1,8 AS V$
200 W$=MKD$(L)
210 LSET V$=W$
220 PUT #1,1
230 CLOSE #1
240 LOCATE 3,1 : INPUT "Nom de l'échantillon: ",N$
250 LOCATE 4,1 : INPUT "Epaisseur: (mm) ",E1
260 LOCATE 4,28 : INPUT "Largeur: (mm) ",E2
270 LOCATE 5,1 : INPUT "Distance entre les contacts: (mm) ",E3
280 LOCATE 7,1 : INPUT "Voulez-vous un copie sur papier (O/N)";P$
290 LOCATE 7,1 : PRINT "
300 OPEN D$+F$+".NOM" FOR OUTPUT AS #2
310 PRINT #2,F$;N$;E1;E2;E3
320 CLOSE #2
330 IF P$<>"O" AND P$<>"o" THEN 500
340     LOCATE 8,1 : INPUT "Voulez-vous imprimez le titre (O/N)";Q$
350     LOCATE 8,1 : PRINT "
360     IF Q$<>"O" AND Q$<>"o" THEN LPRINT CHR$(27)+"!"+CHR$(4) : WIDTH LPRINT 132 : GOTO 500
370     LPRINT
380     LPRINT CHR$(27)+"!"+CHR$(8)
390     LPRINT "                              EFFET HALL"
400     LPRINT CHR$(27)+CHR$(64)
410     LPRINT CHR$(27)+"x"+CHR$(1)
420     LPRINT USING "Nom du fichier: \        \                    Dimension: épaisseur= #.## (mm)";F$;E1
430     LPRINT USING "Nom de l'échantillon: \              \                  largeur= #.## (mm)";N$;E2
440     LPRINT USING "Date (m-j-a): \      \     Heure: \        \             dist.= #.## (mm)";DATE$;TIME$;E3
450     LPRINT CHR$(27)+CHR$(64) : LPRINT CHR$(27)+"!"+CHR$(4)
460     WIDTH LPRINT 132
470     LPRINT "No. de  TEMP       I          Res1  /  Res2              Rh1  /  Rh2              Mob1  /  Mob2          Pop1  /  P
op2      Champ"
480     LPRINT "mes.    (K)       (mA)         (ohm-cm)                  (cm3/C)                  (cm2v-1s-1)              (cm-3)
        (gauss)"
490     LPRINT "——————————————————————————————————————————————————————————————————————————————————————————————————————————————
——————————————"
500 LOCATE 6,1 : INPUT "Numéro de mesure: ",D
510 WHILE D<>70 OR T<300    '———————— DEBUT DE LA BOUCLE DE MESURE ————————
520   LOCATE 7,1 : FOR S=1 TO 15 : PRINT : NEXT S
530   GOSUB 1050                        ' Mesure du courant
540   LOCATE 8,1 : PRINT USING  "COURANT : ###.##  (mA)";Y
550   GOSUB 1180                        ' Mesure de température
560   T1=T
570   LOCATE 10,1 : PRINT USING "TEMPERATURE AVANT: ###.## (K)";T1
```

```
580  GOSUB 1330                          ' Mesure de résistivité
590  GOSUB 1540                          ' Mesure d'effet Hall
600  GOSUB 1180                          ' Mesure de température
610  T2=T
620  LOCATE 10,40 : PRINT USING "TEMPERATURE APRES: ###.## (K)";T2
630  T(1)=(T1+T2)/2
640  T(2)=(U(1)-U(2))*E1*E2*50/(E3*Y)
650  T(3)=(U(3)-U(4))*E1*E2*50/(E3*Y)
660  T(4)=((U(5)-U(6))/U(14)+(U(10)-U(11))/U(9))*E1*1E+10/(4*Y)
670  T(5)=((U(7)-U(8))/U(14)+(U(12)-U(13))/U(9))*E1*1E+10/(4*Y)
680  T(6)=U(9)
690  T(7)=U(14)
700  T(8)=Y
710  LOCATE 14,1 : PRINT USING "TEMPERATURE MOYENNE: ###.## (K)";T(1)
720  LOCATE 14,40 : PRINT USING "MESURE No.: ##";D
730  LOCATE 15,1 : PRINT USING "RESIST.1     : ##.##^^^^ (ohm cm)";T(2)
740  LOCATE 16,1 : PRINT USING "RESIST.2     : ##.##^^^^ (ohm cm)";T(3)
750  LOCATE 15,40 : PRINT USING "COEFF HALL.1 : ##.##^^^^ (cm3/C)";T(4)
760  LOCATE 16,40 : PRINT USING "COEFF HALL.2 : ##.##^^^^ (cm3/C)";T(5)
770  LOCATE 17,1 : PRINT USING "MOBIL.1      : ##.##^^^^ (cm2/Vs)";T(4)/T(2)
780  LOCATE 18,1 : PRINT USING "MOBIL.2      : ##.##^^^^ (cm2/Vs)";T(5)/T(3)
790  LOCATE 17,40 : PRINT USING "POP.1        : ##.###^^^^ (cm-3)";1/(1.6E-19*T(4))
800  LOCATE 18,40 : PRINT USING "POP.2        : ##.###^^^^ (cm-3)";1/(1.6E-19*T(5))
810  OPEN D$+F$+".DAT" AS #1 LEN=8
820  FIELD #1,8 AS V$
830  W$=MKD$(D) : LSET V$=W$ : PUT #1,2
840  FOR I=1 TO 8
850     W$=MKD$(T(I))
860     LSET V$=W$
870     PUT #1,2+(D-1)*8+I
880  NEXT I
890  CLOSE #1
900 IF P$="O" OR P$="o" THEN LPRINT USING "###    ###.##   ###.##     ##.##^^^^ ##.##^^^^     ##.##^^^^ ##.##^^^^      ##.##^^^^ #
#.##^^^^     ##.##^^^^ ##.##^^^^";D;T(1);Y;T(2);T(3);T(4);T(5);T(4)/T(2);T(5)/T(3);1/(1.6E-19*T(4));1/(1.6E-19*T(5));
910 IF P$="O" OR P$="o" THEN LPRINT USING "  #####";(ABS(T(6))+ABS(T(7)))/2
920  '-- Attendre une variation de température d'au moins 5°
930  LOCATE 23,30 : PRINT "TEMPERATURE:        (K)"
940  WHILE T<T1+5
950     GOSUB 1180                ' Sous-programme TEMPERATURE
960     LOCATE 23,43 : PRINT USING "###.##";T
970     FOR Q=1 TO 2000 : NEXT Q
980  WEND
990  D=D+1
1000 WEND     '   - - - FIN DE LA BOUCLE DE MESURE - - -
1010 PRINT "FIN"
1020 LPRINT CHR$(27)+CHR$(64)
1030 END
1040 '**********************************************************************
1050 '-- Sous-programme COURANT
1060 '
1070 S$="C101204E"
1080 CALL SEND (SCANNER%,S$,STATUS%)
1090 S$="R5F0T1M1"
1100 CALL SEND (VOLTMETRE%,S$,STATUS%)
1110 FOR Q=1 TO DELAI : NEXT Q
1120 R$=SPACE$(30)
1130 CALL ENTER (R$,LENGTH%,VOLTMETRE%,STATUS%)
1140 Y=VAL(MID$(R$,5,14))
1150 Y=1000*Y/1.1
1160 RETURN
```

```
1170 '**************************************************************************
1180 '-- Sous-programme TEMPERATURE
1190 '
1200 S$="C170BE"
1210 CALL SEND (SCANNER%,S$,STATUS%)
1220 S$="R5F1T1M1"
1230 CALL SEND (VOLTMETRE%,S$,STATUS%)
1240 FOR Q=1 TO DELAI : NEXT Q
1250 R$=SPACE$(30)
1260 CALL ENTER (R$,LENGTH%,VOLTMETRE%,STATUS%)
1270 R1=VAL(MID$(R$,5,14))
1280 R2=1000*R1
1290 IF R2>248.79 THEN A=219.0448 : B=.2406                    ELSE A=219.9382 : B=.229994
1300 T=(R2-A)/B
1310 RETURN
1320 '**************************************************************************
1330 '-- Sous-programme RESIS
1340 '
1350 FOR I=1 TO 2
1360   FOR J=1 TO 2
1370     S$="C12"+STR$(9+J)+"0"+STR$(I-1)+"E"
1380     CALL SEND (SCANNER%,S$,STATUS%)
1390     Z=0
1400     FOR K=1 TO 5
1410       S$="R6F0T1M1"
1420       CALL SEND (VOLTMETRE%,S$,STATUS%)
1430       R$=SPACE$(30)
1440       FOR Q=1 TO DELAI : NEXT Q
1450       CALL ENTER (R$,LENGTH%,VOLTMETRE%,STATUS%)
1460       X=VAL(MID$(R$,5,14))
1470       Z=Z+X
1480     NEXT K
1490     IF I=2 THEN U(I+J)=Z/5                                  ELSE U(I+J-1)=Z/5
1500   NEXT J
1510 NEXT I
1520 RETURN
1530 '**************************************************************************
1540 '-- Sous-programme HALL
1550 '
1560 FOR M=5 TO 10 STEP 5
1570   S$="1,15,09E"
1580   CALL SEND (SCANNER%,S$,STATUS%)
1590   FOR Q=1 TO 30000 : NEXT Q
1600   Z=0
1610   S$="R4F0T1M1"
1620   CALL SEND (VOLTMETRE%,S$,STATUS%)
1630   R$=SPACE$(30)
1640   FOR K=1 TO M
1650     CALL ENTER (R$,LENGTH%,VOLTMETRE%,STATUS%)
1660     A=VAL(MID$(R$,5,14))
1670     Z=Z+A
1680   NEXT K
1690   H=Z/M*(-126702.4)-348
1700   IF H<0 THEN LOCATE 12,1 : PRINT USING "CHAMP INVERSE: ##### Gauss";H : U(9)=H        ELSE LOCATE 12,40 : PRINT USING "CHAMP
 DIRECT: ##### Gauss";H :U(14)=H
1710   FOR I=1 TO 2
1720     FOR J=1 TO 2
1730      S$="1,15E"
1740       CALL SEND (SCANNER%,S$,STATUS%)
1750       S$="12"+STR$(9+J)+"0"+STR$(I+1)+"E"
1760       CALL SEND (SCANNER%,S$,STATUS%)
```

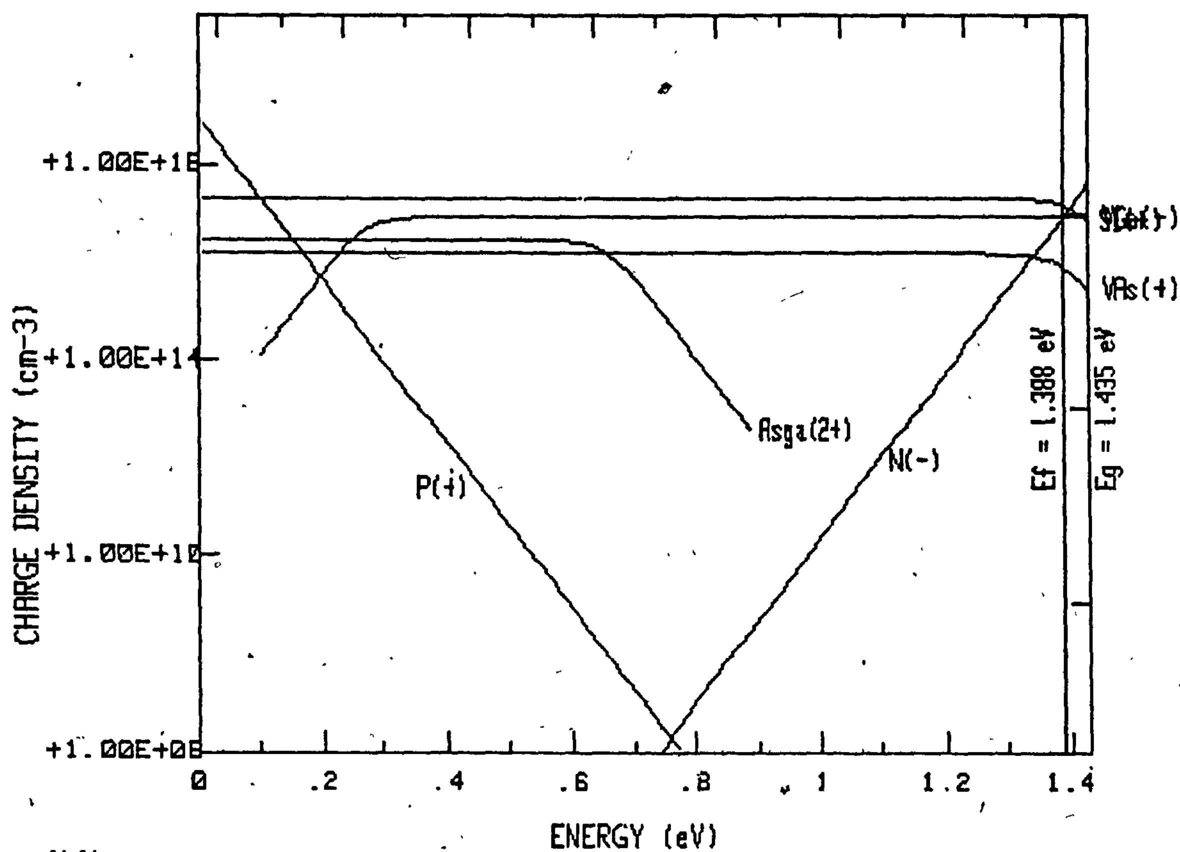
```
1770        S$="R6FOT1M1"
1780        CALL SEND (VOLTMETRE%,S$,STATUS%)
1790        FOR D=1 TO DELAI : NEXT D
1800        Z=0
1810        FOR K=1 TO M
1820          R$=SPACE$(30)
1830          CALL ENTER (R$,LENGTH%,VOLTMETRE%,STATUS%)
1840          X=VAL(MID$(R$,5,14))
1850          Z=Z+X
1860        NEXT K
1870        IF I=1 THEN U(J-1+N)=Z/M                              ELSE U(J+1+N)=Z/M
1880      NEXT J
1890    NEXT I
1900    S$="C1619E"
1910    CALL SEND (SCANNER%,S$,STATUS%)
1920    FOR D=1 TO 15000 : NEXT D
1930 NEXT N
1940 RETURN
1950 '$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
```

APPENDIX D: Shockley curves



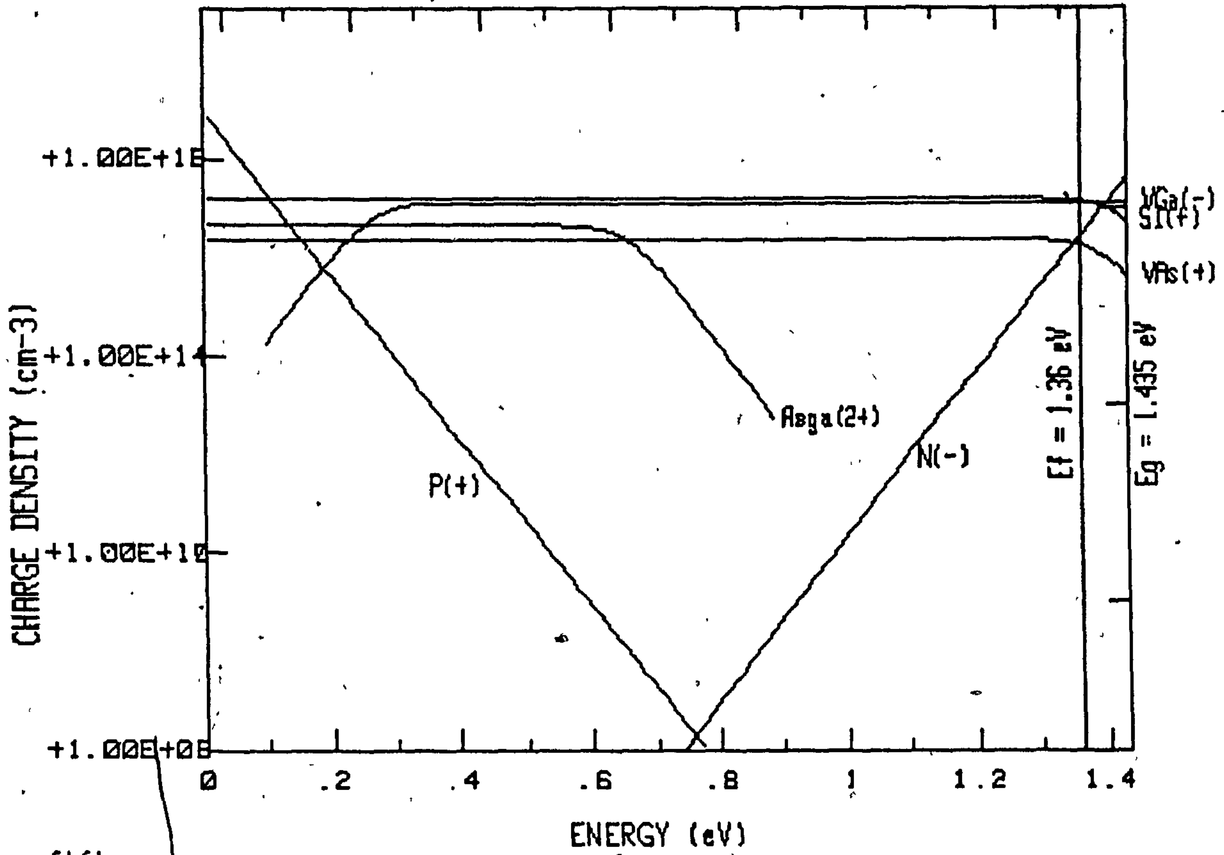
Sample name	X
Si+	1.65E+17 cm-3
S+	0 cm-3
Asga++	0 cm-3
VAs+	0 cm-3
VGa-	0 cm-3
N-	1.69E+17 cm-3
P+	2.03E-5 cm-3

Resistivity	.00429 ohms.cm
Hall coefficient	-36.9 cm3/C
Fermi Level	1.41 eV
Type	N



Sample name	:	X
Si+	:	1.48E+17 cm-3
S+	:	0 cm-3
Asga++	:	15800 cm-3
VAs+	:	8.09E+15 cm-3
VGa-	:	8.5E+16 cm-3
N-	:	7.22E+16 cm-3
P+	:	4.77E-5 cm-3

Resistivity	:	.01 ohms.cm
Hall coefficient	:	-86.4 cm3/C
Fermi Level	:	1.388 eV
Type	:	N



Sample name : X
Si+ : 1.34E+17 cm-3
S+ : 0 cm-3
Asga++ : 69900 cm-3
VAs+ : 1.75E+16 cm-3
VGa- : 1.28E+17 cm-3
N- : 2.45E+16 cm-3
P+ : .000141 cm-3

Resistivity : .0297 ohms.cm
Hall coefficient : -255 cm3/C
Fermi Level : 1.36 eV
Type : N

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