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ZERO VOLTAGE SWITCHING PULSE WIDTH MODULATED INVERTER TOPOLOGIES

VASSILIOS G. AGELIDIS

A Thesis

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ABSTRACT

ZERO VOLTAGE SWITCHING PULSE WIDTH MODULATED INVERTER TOPOLOGIES

VASSILIOS G. AGELIDIS

Among the significant issues in static power converters are high switching frequency and high efficiency. However, switching losses usually limit switching frequencies. Historically, the size and the performance of the static power converters have been closely related to the performance of the semiconductor devices. Furthermore, in the past, any increase in converter switching frequency has almost always been obtained by advances in power semiconductor technology. More recently further improvements have been achieved through the use of appropriate dissipative snubber networks. However, this solution only partially solved the problems of switching losses.

Recent advances, in what are referred to as *soft switching* converter topologies, promise improved semiconductor utilization and substantially higher switching frequencies. The new developments in this area are extensively addressed in this thesis. Moreover, novel *soft switching techniques*, namely zero voltage switching (ZVS) converter topologies for single-phase and three-phase pulse width modulated (PWM) converters are proposed. The most important advantage of these topologies is that they combine features of resonant mode and standard PWM converter. The principles of operation of these topologies are discussed. A detailed design oriented analysis is provided. Simulated results are presented and verified experimentally on laboratory prototypes to establish the feasibility and effectiveness of the proposed converter topologies.

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LIST OF CONTENTS

CHAPTER 3

AN IMPROVED LOW-FREQUENCY HIGH-POWER SINGLE-PHASE FULL-BRIDGE PWM CONVERTER TOPOLOGY

LIST OF FIGURES

LIST OF TABLES

LIST OF ACRONYMS

AC	Alternating Current
ACRLI	Actively Clamped Resonant dc Link Inverter
BJT	Bipolar Junction Transistor
CMSRC	Clamped-Mode Series Resonant Converter
DC	Direct Current
DWM	Discrete Width Modulation
DPM	Discrete Pulse Modulation
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
ESL	Equivalent Series Inductance
GTO	Gate Turn-Off Thyristor
HIPWM	Harmonic Injection Pulse Width Modulation
IGBT	Insulated Gate Bipolar Transistor
JFET	Junction Field Effect Transistor
kW	kilo Watt
MI	Modulation Index
MCT	MOS Controlled Thyristor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
ms	mili seconds
mH	mili Henry
PWM	Pulse Width Modulation

PORC	Parallel Output Series Resonant Converter
RDCLI	Resonant DC Link Inverter
RFI	Radio Frequency Interference
RMS	Root Mean Square
SRC	Series Resonant Converter
Si-Thy	Static Induction Thyristor
SOAR	Safe Operating Area
SMR	Switch Mode Rectifier
SCR	Silicon Controlled Rectifier
SRDCLI	Synchronized resonant DC Link Inverter
SMPS	Switch Mode Power Supply
TM	Topological Modes
UPS	Unninterruptible Power Supply
VVI	Variable Voltage Inverter
VSI	Voltage Source Inverter
VA	Volt-Ampere
ZCS-QRC	Zero Current Switching Quasi Resonant Converter
ZVS	Zero Voltage Switching
ZCS	Zero Current Switching
μP	microProcesssor
μH	micro Henry
μF	micro Farad
μs	micro seconds
ΣΔM	Sigma Delta Modulator

LIST OF PRINCIPAL SYMBOLS

C_1	snubber capacitor
C_S	value of the snubber capacitor
d	converter duty cycle
d_{MIN}	minimum duty cycle
f_O	inverter fundamental output frequency
f_{SW}	converter switching frequency
G_1	switch S_1 gating signal
G_{AC}	AC gain of the PWM technique
i_{Ls}	instantaneous current through L_S
I_O	load current
I_{max}	maximum value of current through L_S
I_{ow}	worst value of i_{Ls}
$I_{Ls,RMS}$	RMS current through L_S
$I_{CC,MAX}$	maximum current through C_C
$I_{AUX,RMS}$	RMS current through auxiliary switch
$I_{AUX,AVG}$	average current through auxiliary switch
$I_{AUX,MAX}$	maximum current through auxiliary switch
$I_{SW,RMS}$	RMS current through converter main switch
$I_{SW,AVG}$	average current through converter main switch
$I_{PRI,RMS}$	RMS current of transformer primary winding
$I_{PRI,MAX}$	maximum current of transformer primary winding

$I_{D,RMS}$	RMS current through a rectifier diode
$I_{D,AVG}$	average current through a rectifier diode
$I_{D,MAX}$	maximum current through a rectifier diode
I_A	line current in the three-phase inverter
I_B	line current in the three-phase inverter
I_C	line current in the three-phase inverter
I_{L1}	current through L_S
I_{L2}	current through L_S
$I_{L,RMS}$	RMS inverter line current
I_{Rs}	current through R_S
K	overvoltage factor
L_S	snubber inductor
P_{OUT}	converter rated output power
P_{Rs}	power dissipation in the snubber resistor R_S
R_S	snubber resistor
S_1	inverter main switch
S_O	auxiliary switch
t_{dead}	dead time of the converter (free-wheeling mode)
t_1	time instant
$t_{ON,So}$	on-time of the auxiliary switch
V_{IN}	dc input power supply
V_{INMAX}	maximum dc input power supply
V_{INMIN}	minimum dc input power supply
V_{CC}	voltage of storage-clamp capacitor C_C

$I_{D,RMS}$	RMS current through a rectifier diode
$I_{D,AVG}$	average current through a rectifier diode
$I_{D,MAX}$	maximum current through a rectifier diode
I_A	line current in the three-phase inverter
I_B	line current in the three-phase inverter
I_C	line current in the three-phase inverter
I_{L1}	current through L_S
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L_S	snubber inductor
P_{OUT}	converter rated output power
P_{Rs}	power dissipation in the snubber resistor R_S
R_S	snubber resistor
S_I	inverter main switch
S_O	auxiliary switch
t_{dead}	dead time of the converter (free-wheeling mode)
t_1	time instant
$t_{ON,So}$	on-time of the auxiliary switch
V_{IN}	dc input power supply
V_{INMAX}	maximum dc input power supply
V_{INMIN}	minimum dc iput power supply
V_{CC}	voltage of storage-clamp capacitor C_C

V_{CI}	voltage across snubber capacitor C_I
V_{OUT}	converter output voltage
$V_{Ls,MAX}$	maximum voltage across L_S
$V_{CC,MAX}$	maximum voltage across C_C
$V_{AUX,MAX}$	maximum voltage across auxiliary switch
$V_{SW,MAX}$	maximum voltage across converter main switch
$V_{PRI,RMS}$	RMS voltage of transformer primary winding
$V_{PRI,MAX}$	maximum voltage of transformer primary winding
$V_{D,MAX}$	maximum reverse voltage across a rectifier diode
V_{AB}	normalized inverter line-to-line voltage
V_{BC}	normalized inverter line-to-line voltage
V_{CA}	normalized inverter line-to-line voltage
$V_{L\text{-}L}$	fundamental component of the line-to-line output inverter voltage
$V_{L\text{-}L,RMS}$	RMS value of the inverter line-to-line voltage
y	analytical expression for the reference waveform of the HIPWM technique
W_{CI}	capacitor energy
W_{IN}	energy that enters C_C
W_{OUT}	energy that leaves C_C
ΔV_{CC}	difference in voltage across C_C
η	efficiency
ω_r	resonant frequency

CHAPTER 1

INTRODUCTION

1.1 Introduction

In power electronic technology, static converters can be viewed as power conditioners which employ semiconductor devices to convert or control energy. Specifically, they enable the energy flow between different systems to be controlled.

When ac and dc systems are coupled, the basic functions that can be realized are as follows:

- rectification, the conversion of ac into dc (i.e. diode or controlled rectifiers,etc.);
- inversion, the conversion of dc to ac (i.e. ac variable speed drives, unninteruptible power supply (UPS) systems, etc.);
- dc conversion, the conversion of dc of a given voltage and polarity into that of another voltage and where applicable, reversed polarity (i.e. dc power supplies, dc variable speed drives, etc.);
- ac conversion, the conversion of ac of a given voltage, frequency, and number of phases into that of another voltage, frequency, and where applicable number of phases (i.e. cycloconverters, ac power controllers, etc.).

Power semiconductor devices are employed to realize the numerous static power converters which perform the previously mentioned functions. A brief discussion of the various semiconductor devices and their essential characteristics is provided in the following section.

1.2 Power semiconductor devices

Power semiconductor devices perform the on-off action which is the basic operation in static power converters. The beginning of the power electronics technology is usually associated with the development of the thyristor (Silicon Controlled Rectifier - SCR) in the laboratories of the General Electric Company in 1957 [1],[2],[3],[4]. Since then, the thyristor has undergone much development. It has not only been improved to become the high-speed thyristor but has also been diversified into various kinds, such as Triac, Gate Turn-Off thyristor (GTO), etc. The high-voltage/high-current capability and the high short-time current-carrying capability ensure that the thyristor is an indispensable part of power electronic converters, especially at high power levels. The GTO, with capability of switching at higher voltages and currents, deserves a special mention since high power converters employing self-commutated devices can be realized. GTO's, as compared with thyristors, reduce the size of static power converters, since all the necessary and complicated networks for the commutation of the thyristors are eliminated.

One important achievement has also been the development and continuing improvement of the Bipolar Junction Transistor's (BJT's) power ratings during the 1980's. The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has been also developed which provides higher speeds and larger safe operating area (SOAR) than the BJT's. Other advances have been the reduction of the on-resistance of the power MOSFET's and increase in their power ratings during the last decade.

Hybrid devices comprised of bipolar and MOS devices such as the Insulated Gate Bipolar Transistor (IGBT), have also been fabricated which are suitable for higher voltages and currents than MOSFET's and are also capable of switching at higher frequencies than BJT's. Additionally, MOS controlled thyristors (MCT), comprised of a MOSFET and a

thyristor, have been developed. These devices are also expected to have high voltage and current capability.

One of the most important problems in static power converters is addressed in the following section.

1.3 Losses in power semiconductor devices

The ever increasing development of self-commutated switching devices has led to increased use of transistors (BJT's, JFET's, MOSFET's, IGBT's, etc.) in many industrial applications related to power electronic technology. However, proper use of these devices requires determination of semiconductor losses since adequate cooling means have to be provided to keep the device temperature within rated values.

Generally, the semiconductor losses are grouped into three categories [5]:

i) conduction losses

- on-state losses
- dynamic saturation losses

ii) switching losses

- turn-on losses
- turn-off losses

iii) off-state losses.

The relative magnitudes of the conduction and switching losses are greatly dependent on the type of the converter (i.e. resonant, quasi-resonant, PWM, etc.), the operating frequency, the type of the load (linear or nonlinear, resistive or inductive), and certain characteristics of the switch itself (i.e. turn-on time, turn-off time, etc.). Off-state losses are generally a very small portion of the total losses and are considered negligible.

The most vital issues in power electronics technology are addressed in the following section.

1.4 Significant issues in power converter technology

In all areas of power electronics, the most significant issues and research interests concerning the static power converters are as follows:

- the improvement of efficiency,
- the reduction of size, weight, and cost,
- fast transient response,
- better input/output spectral characteristics,
- minimization or elimination of acoustic noise and electromagnetic interference (EMI), and
- wide range control of output voltage, current or frequency.

Higher switching frequencies are an essential requirement for achieving all the previously mentioned performance improvements. However, switching losses limit the switching frequencies.

Historically, the size and the performance of the static power converters have been closely related to the performance of the semiconductor devices [2]. In the past, any increase in converter switching frequency has almost always been obtained by advances in power semiconductor technology [4]. Further improvements have been achieved by the use of appropriate lossy snubber networks [6]. However, employing snubber networks only partially solved the problems associated with switching losses. Therefore, development of topologies which employ low loss snubber subcircuits is an important goal, since these converters can operate at higher frequencies without introducing the problems associated

with the switching losses.

Over the last decades, the different approaches dealing with switching losses are critically discussed in the following sections.

1.5 Literature review

Depending upon the application, there are several ways of dealing with switching losses in static power converters. In this section, previous research work, related to various approaches towards alleviating semiconductor devices from switching losses, is reviewed.

1.5.1 Converter snubber networks

Snubber networks are a primitive way to minimize switching losses in pulse width modulated (PWM) converters. In general, snubber networks are converter subcircuits used for the reduction of switching losses of power semiconductor devices [6]. The turn-on and turn-off networks are placed in series/parallel to power switching devices, respectively. For instance, one major purpose of using such networks, especially for power BJT's and GTO's, is to keep the power device within its safe operating area (SOAR).

Two different types of snubber subcircuits can be defined:

- dissipative
- nondissipative (low loss snubbers)

The basic difference between the dissipative and the nondissipative snubber subcircuits is as follows:

- in dissipative snubber networks, the energy stored in the reactive elements (limiting *di/dt* inductor and limiting *dv/dt* capacitor) is dissipated in resistors and converted into heat [7]. This type is certainly not the best choice to achieve high switching

frequencies and/or high power levels.

- in nondissipative (low loss) snubber networks, there are no fundamental losses. In this case, losses are only caused by nonideal device properties, such as conduction and transient switching losses of the switching devices contained in the snubber networks.

It is certainly possible and sometimes advantageous, depending upon the application, to combine dissipative turn-on networks with nondissipative turn-off networks and vice versa [6]. The specific topologies of the snubber subcircuits can vary considerably depending upon the switching characteristics of the components being protected. For instance, the turn-off snubber for a thyristor is primarily intended to control and limit the rate of rise of voltage across the semiconductor device during turn-off. The need to limit that rate (dv/dt) is based on the thyristor's ability to commutate the current in a certain time interval which is usually given in the manufacture's data sheets. The design and the operation of the snubber networks for converters employing thyristors are well documented in the technical literature and they are not the object of this thesis [8],[9].

For the modern semiconductor devices such as power BJT's, JFET's, MOSFET's, IGBT's, and GTO's, snubber subcircuits are also employed in PWM converters. Fig. 1-1 shows the conventional dissipative snubber networks. Specifically, the turn-on snubber (R_S - L_S) to control the rise rate of the switch current during turn-on and the turn-off snubber (R_S - C_S) to control the rise rate of the switch voltage during turn-off are shown. The polarized snubber networks (turn-on/turn-off) are included. The combined polarized complete turn-on/turn-off snubber network is also depicted. The transistor S in each case is the respective semiconductor device that is being protected by the passive snubber components R_S, L_S, C_S and D_S.

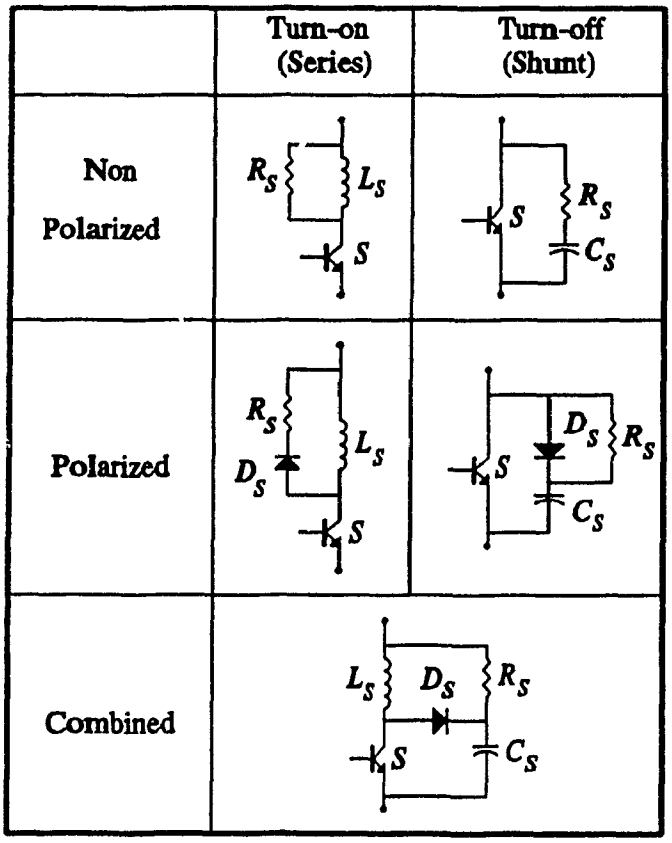

Figure 1-1: Conventional dissipative snubber subcircuits.

With the use of a combined snubber subcircuit (Fig. 1-1), the interaction between the semiconductor device and the snubber subcircuit is as follows:

- During turn-on the voltage fall is a linear time function completely dictated by the switch characteristics, while the current rise is dictated by the series snubber inductor L_S .
- During turn-off, the current fall is a linear time function completely determined by the switch characteristics, while the voltage rise is determined by the shunt snubber capacitor C_S .

The operation of the combined snubber network (Fig. 1-1) is described as follows:

After switch turn-on, the snubber capacitor C_S discharges via the semiconductor device through the C_S - R_S - L_S loop. The discharge current is superimposed on the load current. The snubber capacitor C_S voltage reaches zero afterwards, at which moment the snubber polarizing diode D_S begins to conduct and the remaining overcurrent in the inductor L_S decays exponentially through the L_S - R_S loop. Respectively, after switch turn-off, the series snubber inductor L_S begins to discharge and the snubber diode D_S conducts thus connecting C_S in parallel with the semiconductor device. The discharge voltage of the inductor is superimposed over the input voltage already present across the switch. The discharge network consists of the parallel branch L_S - C_S - R_S. The inductor current reaches zero afterwards at which moment the snubber polarizing diode D_S blocks and the remaining overvoltage decays exponentially through the C_S - R_S loop.

The advantages of the conventional dissipative snubber networks can be summarized as follows:

- transfer of the switching losses from the semiconductor device to an external resistor;
- suppression of high voltage transients;
- control of the rise rate of the current during turn-on and the rise rate of the voltage during turn-off;
- reduction of the generated noise and the electromagnetic interference (EMI);
- avoidance of the secondary breakdown in transistor (BJT) converters.

On the other hand, the following disadvantages associated with these snubber networks can be identified:

- the energy stored in the reactive elements is dissipated in external resistors, thus

decreasing converter efficiency as the switching frequency increases;

- overvoltages can still occur as a result of resonances between snubber or stray inductors and snubber or parasitic capacitors;
- extra components are required, thus increasing power circuit complexity;
- the power losses also complicate the thermal layout and the heat sink design thus leading to an increase in cost.

The operation of the conventional dissipative snubbers at high frequencies and high power levels becomes extremely critical since the dissipated energy increases as a function of the switching frequency.

A thorough analysis by W. McMurray provides an optimization technique that can be employed to design a conventional dissipative *R-L-C* network for a specific application [10]. The results presented show that certain values of snubber capacitor and inductor will minimize the total switching losses, including losses in the device and the eventual dissipation of energy stored in the snubber elements. However, as stated earlier, these passive snubber subcircuits only partially solved the problems associated with the switching losses. Diverting the losses from an active switching device to an external resistor is a primitive solution resulting in a low converter efficiency. Moreover, adequate cooling means have to be provided for the dissipating resistors, increasing converter size, weight and cost.

At higher power levels and switching frequencies, it is more desirable to rather use nondissipative (low loss) snubber networks. An analysis and optimization technique for nondissipative snubber networks has been done by Charl G. Steyn [11]. The paper only treats the single storage element for turn-on (inductor) and turn-off (capacitor) separately and independently of each other. It provides only mathematical information for designing an optimum snubber since no specific subcircuit for energy recovery is addressed.

1.5.2 Improved snubber networks

The snubber subcircuits previously presented (Fig. 1-1) can be used for each switching device separately. However, it is more efficient to combine components and to use for instance one reactive element (inductor/capacitor) for both switches of a PWM converter leg. There are various snubber subcircuits that improve the overall component count by reducing the number of snubber elements.

A snubber subcircuit suitable for BJT-inverter topology using a minimum number of components is proposed in [12]. The snubber components are designed in such a way that maximum ratings associated with semiconductor devices are not exceeded. Modifications have been discussed in cases that power MOSFET's are used as switching devices. However, all the energy associated with the snubber subcircuits is dissipated in passive components which makes this solution unattractive for high frequency high power converters.

Some snubber networks for PWM bridge converters with BJT's or GTO's have been proposed and analyzed by T. M. Undeland [13]. They are simple and give less extra stresses than the conventional configurations (Fig. 1-1). Most of the turn-on and turn-off losses in the semiconductor devices are removed and dissipated in a single snubber resistor, therefore loss recovery can be easily done if desired. A common inductor is used to protect all converter diodes and switches during switching turn-on. Similarly, only one snubber capacitor is used for each pair of switches of a converter phase-leg. However, this paper does not include any way of recovering the losses associated with snubber elements.

An improved snubber configuration for both BJT's and GTO's PWM inverters has been also analyzed by T. M. Undeland [14]. It is a complete turn-on/turn-off snubber network that has the advantages of conventional snubbers, and in addition:

- it has fewer components;
- it introduces lower additional stresses;
- the snubber diodes do not cause any difficulties associated with reverse recovery;
- all the losses are dissipated in one resistor, therefore loss recovery can be easily done, if desired.

As stated earlier, the snubber is suitable for both GTO's and BJT's, but the size of the snubber components may differ for different applications. A three-phase inverter with the same snubber has been also discussed in this paper. However, this paper does not propose any solution to recover the losses associated with the snubber components.

Another snubber configuration based on that proposed in [14] has been further investigated in [15] for PWM-VSI with IGBT's. However, in this paper the inductors as well as the dissipating resistors are split to reduce EMI but loss recovery is not considered at all. Some proposed arrangements include an increased number of components making the power circuit layout more complex.

Based on the snubber configuration proposed in [14], an improved snubber with energy recovery by simple passive network is proposed by J. Matthias [16]. This configuration is suitable for high power and low switching frequency applications using GTO's. In this case, a substantial part of the snubber energy can be recovered by a secondary winding on the turn-on snubber inductor, reducing the total snubber losses to less than one third compared with a conventional snubber. However, the energy recovery subcircuit is complicated making the solution unattractive.

A snubber network suitable for a phase-leg of a voltage source GTO or BJT inverter is proposed and analyzed by W. McMurray [17]. This arrangement reduces the size of the reactive components as well as their number. It also provides efficient means of recovering

a substantial part of the energy trapped in the snubber elements, since the discharge resistor may be replaced by a transformer which conserves trapped energy in both the series (inductor) and shunt (capacitor) reactive components. However, the proposed solution to recover the snubber energy is complicated.

Another snubber circuit for high power GTO inverter which is composed of only passive elements is proposed in [18]. Ideally, no losses occur due to snubber components since the configuration completely recovers the trapped energy of the turn-on and turn-off snubber elements. The overall converter efficiency is increased, which is especially preferred for high power applications. However, the proposed power circuit layout is cumbersome.

A snubber configuration using active switching devices for energy recovery is proposed for PWM transistor inverters [19]. The requirement of being basically a lossless network is fulfilled. However, the complexity of the circuit is high and it can be added that the snubber network itself becomes another power converter topology.

Active way of protecting power transistors and eliminating the necessary snubber subcircuits is also proposed in [20]. Feedback methods are studied to achieve a faster, lighter and integrable solution. The detection of an overvoltage when the device turns-off activates a negative feedback path and drives the device back into conduction in such a way that the overvoltage originated by the inductor current discontinuity is kept constant at a predefined level. With this approach, the current carried by the transistor is decreased in a controlled way, during turn-off, and the voltage does not exceed a certain limit. Similar active drive techniques for power transistor are also discussed in [21]. However, this method deals with protecting the semiconductor device from overvoltages only. Moreover, all the energy associated with switching turn-off is dissipated inside the transistor, since the device is driven back to conduction till the overvoltage is not detected, therefore increasing

semiconductor losses.

1.5.3 *Soft switching* converters

The switch stresses, as discussed in previous sections, can be reduced by connecting simple dissipative snubber subcircuits in series and parallel with the switches in the switch mode converters (Fig. 1-1). However, these dissipative snubbers shift the switching power losses from the active device to the snubber elements, and therefore do not provide a significant reduction in the overall switching power losses.

In contrast to dissipative snubbers in switch-mode converters, the combination of proper converter topologies and switching strategies can overcome the problems of switching stresses, switching power losses, and the EMI by turning on and turning off each of the converter switches when either the switch voltage or the switch current is zero. Ideally, both the switch voltage and current should be zero when the switching transition occurs.

The converter topologies that can provide an automatic and lossless resetting of the snubber components through inherent converter operation are referred to as *soft switching* converters. Such topologies are very attractive at high-power levels when high-frequency operation is to be achieved concurrently, since they allow an oversizing of the snubber subcircuit without introducing the normal penalty of the trapped energy which needs to be dissipated.

Generally, *soft switching* topologies are divided into the following two types:

- zero current switching (ZCS) which refers to device turn-on and turn-off occurring with nearly no current in the switch.
- zero voltage switching (ZVS) which refers to device turn-on and turn-off occurring with almost no voltage across the device.

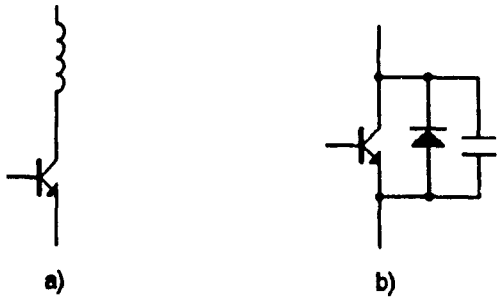

Figure 1-2: *Soft switching* elements.

a) Zero current switching during turn-on only.

b) Zero voltage switching during turn-off only.

Fig. 1-2 shows the two types of devices that experience zero current switching during turn-on only and zero voltage switching during turn-off only respectively. The snubber subcircuits associated with zero current switching are purely inductive. The snubber subcircuits associated with zero voltage switching are purely capacitive and the device turn-on must occur with the antiparallel diode conducting.

The main advantages gained by using *soft switching* elements are as follows:

- very low switching losses and stresses;
- improved converter reliability;
- recirculation of the energy associated with snubber elements, therefore improved overall system efficiency;
- reduced need for cooling means;
- achievement of higher switching frequencies.

Some of these converter topologies which experience zero-voltage and/or zero-current switching, are presented in Chapter 2.

1.6 Scope and contributions

The scope and objective of this thesis is to present, analyze and verify experimentally *soft switching*, namely zero voltage switching pulse width modulated inverter topologies. In particular, the principal contributions of this thesis are as follows:

- The analysis, design and experimental verification of a single-phase full-bridge high-power low-frequency PWM converter topology employing a low loss snubber network (Chapter 3).
- A simple energy recovery subcircuit to improve the efficiency of the same topology is investigated (Chapter 3).
- The analysis, design and experimental validation of a zero voltage switching PWM converter topology using a lossless dc bus commutating subcircuit (Chapter 4).
- A three-phase zero voltage switching pulse width modulated voltage source inverter topology is presented (Chapter 5).

1.7 Summary of the thesis

The contents of the thesis have been organized as follows:

Chapter 2 presents the most widely used converter topologies for dc-dc and dc-ac energy conversion. The *hard switching* topologies (mainly PWM converters) and the *soft switching* ones (i.e. resonant, quasi-resonant, etc.) are presented. The advantages and the drawbacks of these converters are critically discussed.

In Chapter 3, a low loss snubber network for high-power low-frequency single-phase full-bridge PWM converter first is considered. A modified lossless snubber network for the same type of converter is proposed. The main advantage of the converter under consideration is that, at least, theoretically, no energy associated with the snubber reactive

elements is lost. Detailed analysis and design procedures for both power converter topologies are included. Experimental results are presented to verify the principles of operation of the proposed topology.

In Chapter 4, a zero voltage switching (ZVS) high-frequency medium-power single-phase full-bridge PWM converter topology is proposed. The inverter purely capacitive snubber provides nearly zero switching losses during turn-off. The active dc bus subcircuit provides almost zero switching losses during turn-on, by forcing the respective switch antiparallel diodes to conduct prior to main switch turn-on. Converter analysis and design procedure are included. Experimental results are presented to verify the feasibility of the proposed converter topology.

In Chapter 5, a three-phase ZVS PWM VSI topology is studied. The main advantage of the proposed scheme is that the dc bus commutating circuit is synchronized with an appropriate PWM technique. Both the power inverter topology and the modulation technique minimize switching losses thus improving the overall system performance. Detailed description of the modulation strategy and the principles of operation of the inverter are presented. It is also shown that the modulation strategy is optimum for the proposed inverter topology.

Finally, Chapter 6 contains a summary and conclusions of the thesis as well as suggestions for future work.

CHAPTER 2

DC-DC & DC-AC CONVERTER TOPOLOGIES

2.1 Introduction

The three major application areas of power converter technology using self-commutated devices are as follows:

- dc-dc converters,

- dc-ac inverters, and

- ac-dc converters such as pulse width modulated rectifiers.

There exist numerous converter topologies, depending upon the power level, to accomplish the desired conversion functions.

In this chapter, first the conventional PWM dc-dc topologies are presented [22],[23],[24]. Thereafter, converter topologies referred to as *soft switching* topologies such as resonant, quasi-resonant, multi-resonant, and other *soft switching* topologies are also considered. The six-switch three-phase PWM converter, which is widely used for dc-ac energy conversion, is then discussed. Since 1986, significant new developments have been made in the area of power electronic inverter topologies, especially for high power applications. For these new converter topologies attempt has been made to substantially eliminate the semiconductor switching losses. Converters with these properties allow the semiconductor devices to be operated at increased switching frequencies which are then only limited by the device intrinsic delay times rather than its thermal characteristics. Consequently, power electronic converters can be designed which attain higher efficiencies

and bandwidth and which achieve higher power densities. The various *soft switching* three-phase inverter topologies are critically presented in the following sections.

2.2 *Hard switching* PWM dc-dc converter topologies

Most dc-dc applications require single quadrant operation, unipolar voltage and current and unidirectional power flow. The most widely used converter topologies may be classified as *hard switching* pulse width modulated converters. These topologies are referred to as *hard switching* topologies because the switching trajectory of the semiconductor devices results in device stresses. Specifically, with *hard switching*, the power device experiences simultaneously high voltages and currents during turn-on and turn-off leading to high switching losses. The reverse recovery of the free-wheeling diode in a converter phase leg may cause current spikes and EMI. A simple and rugged way of improving semiconductor switching trajectory is by employing snubber networks. These snubber networks have been discussed briefly in Chapter 1.

Most dc-dc converters are derived from the three single quadrant topologies, namely, the buck, the boost and the buck-boost converters [23]. These basic converter topologies are shown in Fig. 2-1. For dc-dc power applications such as the off-line switch mode power supplies (SMPS), there exist a need for high frequency isolation using a transformer. Such static power converters requiring galvanic isolation, include the flyback and forward converters for low power applications (Fig. 2-2), the dual forward and half bridge converters for moderate power applications (Fig. 2-3) and lastly the full bridge converter for high power applications (Fig. 2-4). The advantages and the problems of the *hard switching* PWM dc-dc converters are discussed in the following sections.

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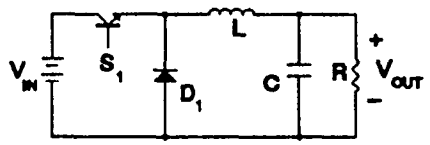

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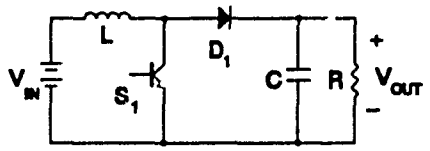

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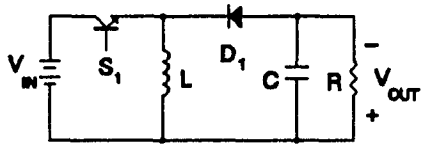
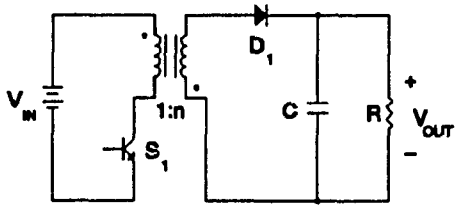


Figure 2-1: a) Buck switching converter.

b) Boost switching converter.

c) Buck-Boost switching converter.

a)



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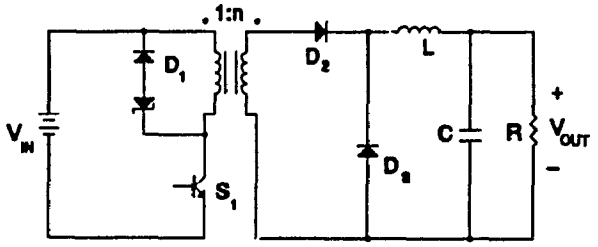


Figure 2-2: a) Flyback switching converter.

b) Forward switching converter.

a)

b)

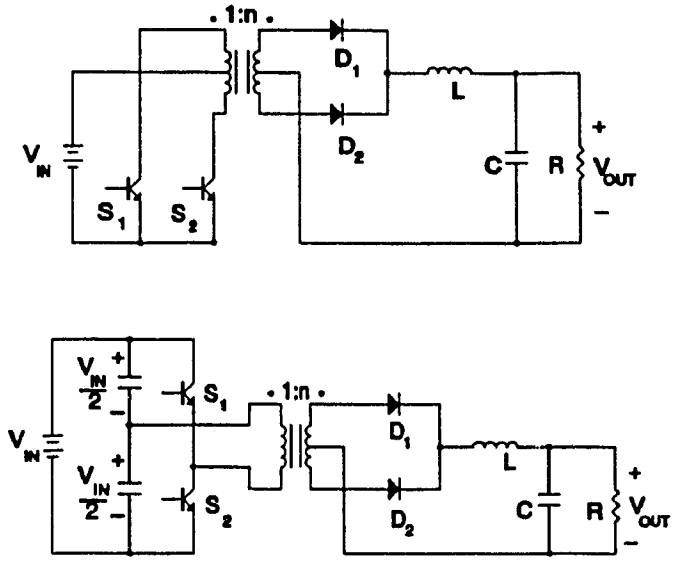


Figure 2-3: Isolated medium power converter topologies

a) Dual forward switching converter.

b) Half-bridge switching converter.

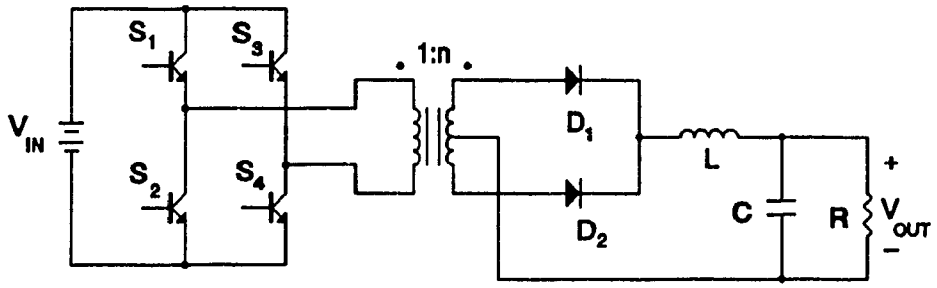


Figure 2-4: Full-bridge switching converter.

2.2.1 Advantages of PWM converters

PWM converters still represent the dominant technology in use by industry today. The reason being that they offer a great deal of advantages which can be summarized as follows:

- simple and rugged power circuit;
- voltage/current control techniques are simple as well;
- low cost;
- minimum VA ratings of semiconductor devices.

Although PWM converters provide a simple solution, they have a numbe. of undesired features. The next section addresses the most serious drawbacks of the PWM converters.

2.2.2 Drawbacks of PWM converters

Most PWM converters operate at low and medium frequency. The reason being that PWM converters need to switch rapidly to minimize switching losses. However, the fast rising edges in the switching waveforms generate a lot of EMI. Both switching losses and EMI tend to increase according to switching frequency. Any attempt to improve converter efficiency by switching faster also increases the level of generated EMI.

The above mentioned problems can be overcome to a certain extend by selecting converter components very carefully. Nevertheless, energy stored in the parasitic inductances is still a significant issue. Therefore, effective snubber networks such as the conventional ones presented in Chapter 1 are required.

Additional problems of the PWM converters at low and medium power levels operating at high switching frequencies are as follows:

- more drive power is required, especially for MOSFET's, which are used to realize high frequency energy conversion;
- equivalent series resistance of capacitors and parasitic effects of magnetic components become significant limiting factors;
- the layout of the power circuit becomes particularly critical to the performance of the converter.

Parasitic elements also create problems. Some of the most important parasitics are the stored charge in the diodes and other semiconductor devices such as MOSFET's, the stray inductance of even short wire connections and the stray capacitance associated with circuit elements.

Generally, limitations in any power converter topology are introduced by the following parameters:

- peak semiconductor voltage and current;
- peak capacitor voltage;
- RMS current in all components;
- size, weight and cost of passive filter components;
- overall circuit efficiency;
- controllability;
- fault tolerance;
- electromagnetic interference.

During the last two decades, a lot of research work has been done towards achieving higher switching frequencies. This work has produced topologies known as *soft switching* topologies and some of them are presented in the following sections.

2.3 *Soft switching* dc-dc converters

Although the area of *soft switching* converters is new, it is very broad. An attempt has been made in the following sections to present only the basic topologies of such dc-dc converter topologies.

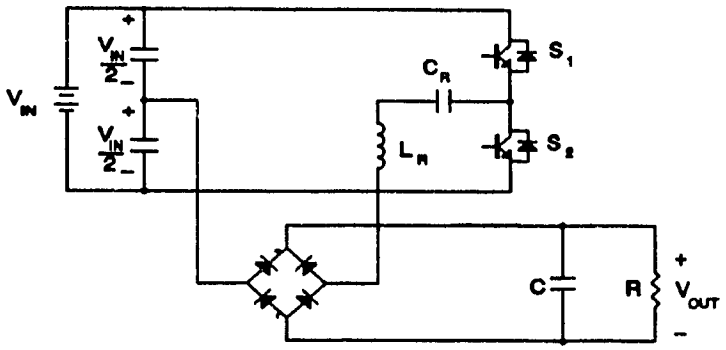
2.3.1 Resonant dc-dc converters

Historically, prior to the availability of self-commutated switches with appreciable voltage- and current-handling capability, the switch-mode converters consisted of thyristors (currently thyristors are employed only at very high power levels). Each thyristor in such a converter required a current-commutation subcircuit, which consisted of an *L-C* resonant circuit plus other auxiliary thyristors and diodes, which turned the main thyristor off by forcing the current through it to go to zero.

A need to increase switching frequencies resulted in replacing the thyristors with self-commutated switches and a simple *L-C* resonant circuit was used to shape the switch voltage and current in order to yield zero-voltage and/or zero-current switching.

The series resonant converter is one of the earlier resonant dc-dc converters, proposed in the technical literature, that provides zero current switching [25]. The circuit proposed in this paper is mainly suitable for high power applications employing thyristors as switching devices. Switch mode power supplies (SMPS) employing series or parallel resonant tank have been also proposed in the literature. Although the series resonant topology is more suitable for high power applications, the parallel output series resonant converter (POSR) provides better characteristics for SMPS systems [26]. The respective converter topologies are shown in Fig. 2-5. If the circuit operates below the L_R - C_R tank resonant frequency, it allows natural commutation of these devices, providing zero current

a)



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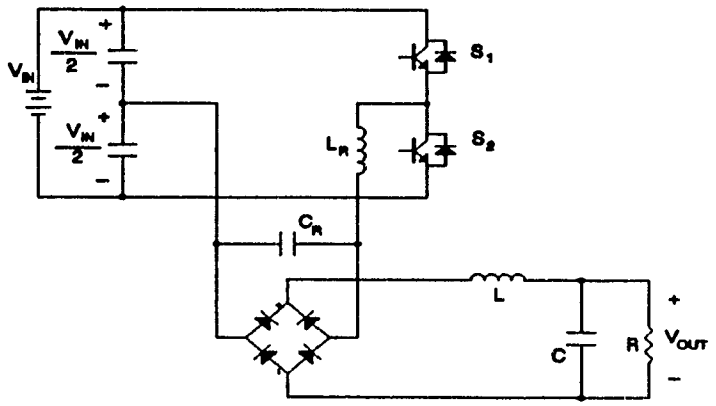


Figure 2-5: Resonant dc-dc converter topologies.

a) Half-bridge series resonant converter.

b) Half-bridge parallel output series resonant converter.

switching in all power devices. It is further shown in [26] that if the switching devices are force-commutated elements such as MOSFET's or BJT's switches, operation of the circuit above the resonant frequency of the L_R - C_R tank can be obtained. Moreover, zero voltage switching for all devices is achieved. Another zero voltage switching resonant mode dc-dc converter is also proposed in [27].

2.3.1.a Advantages of resonant dc-dc converters

The primary objective in selecting resonant mode operation is the reduction of device switching losses. Both ZCS and ZVS topologies attempt to minimize switching losses through the use of low loss snubbers.

The advantages of the resonant dc-dc topologies can be summarized as follows:

- low *di/dt* stress on components due to the non-rectangular waveforms;
- low level of generated EMI;
- improved efficiency since they provide nearly zero switching losses (switching is done either at zero current or zero voltage);
- parasitic elements can be utilized as part of the power processing circuit;
- fast transient response due to higher switching frequencies attained.

2.3.1.b Drawbacks of resonant dc-dc converters

The most serious problems that can be identified for the various resonant converter topologies are as follows:

- generally, both kind of topologies, namely, ZCS and ZVS require a wide range of frequency control, thus making the optimization of the filter components and design of output transformer and EMI filters difficult;
- high RMS currents which result in high conduction losses;
- the use of a resonant mechanism to transfer power from the source to the load implies the use of an underdamped *L-C* circuit with substantial circulating energy trapped in these elements;
- significantly higher VA ratings, compared with the output power, for the devices and other circuit components are required, resulting in inefficient utilization of

device capabilities;

- high control circuit complexity since the switching of the semiconductor devices must be done either at zero current or zero voltage.

The above mentioned problems make these topologies unattractive for medium and high-power high-frequency industrial applications.

2.3.1.c Comparison between ZCS and ZVS

In ZCS converters, the current produced by *L-C* resonance flows through the switch, thus causing it to turn-on and off at zero current. In ZVS converters, the resonant capacitor produces a zero voltage across the switch at which instant the switch can be turned on or off. Both of these techniques require a variable frequency control to regulate the output voltage.

The ZCS topologies are limited in frequencies achievable by the reverse recovery phenomena associated with the antiparallel diode of the main switching device. Moreover, high peak currents during reverse recovery process of the antiparallel diodes contribute high switching losses and high voltage spikes.

On the other hand, ZVS topologies require that the antiparallel diode is conducting prior to the main switch turn-on. By synchronizing the turn-on instant with antiparallel diode conduction, also eliminates the snubber dump phenomenon which normally occurs during main device turn-on and thus allowing the use of purely capacitive snubber elements.

It has been shown that zero voltage switching as opposed to zero current switching is more appropriate control strategy for high-frequency resonant mode converters [27],[28]. This has to do with the internal capacitors of the switch. Specifically, with the turn-on at zero current but at a finite voltage, the charge on the internal capacitors is dissipated in the

switch. This loss becomes significant at very high switching frequencies. However, no such loss occurs if the switch turns on at a zero voltage. In the ZCS, the switch is required to conduct a peak current that is higher than the load current. In the ZVS the switch is required to withstand a forward voltage that is higher than the input supply voltage. This results in a very large rating of the switch for both type of converters.

2.3.2 Quasi-resonant dc-dc converters

To overcome the problems associated with the resonant topologies, quasi-resonant converters such as the zero-current-switching quasi-resonant converter (ZCS-QRC) have been developed [28]. The respective circuit is shown in Fig. 2-6. Different quasi-resonant converters that experience ZVS or ZCS are also discussed in the technical literature [29].

Although these circuits provide improved characteristics compared with the resonant converters, various problems can be also identified. Peak voltage stress associated especially with the ZVS topologies is the most serious problem of the "family" of the quasi-resonant converters. Reverse diode recovery causes voltage spikes and finally the need to limit the voltage stresses restrict the operating range of the quasi-resonant converters.

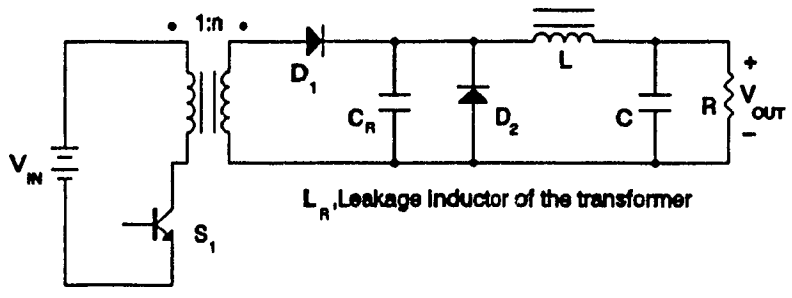


Figure 2-6: The ZCS-quasi resonant converter.

2.3.3 Multi-resonant dc-dc converters

Another promising development has been the recently proposed multi-resonant converter [30]. The ZVS quasi-resonant topology is extended to incorporate the additional parasitic elements associated with the free-wheeling diode. The frequency range is reduced therefore the optimization of the filter components becomes easier. However, the high component stresses make it impractical at high-power or high-voltage applications.

2.3.4 Other *soft switching* dc-dc converters

For high-power multi-quadrant applications, dual bridge topologies such as the circuit shown in Fig. 2-7 can be used [31]. These topologies feature minimal device ratings for a given output power and have almost no switching losses. They fall into the category of *soft switching* converters that employ resonant transitions, but are very similar to *hard switching* topologies.

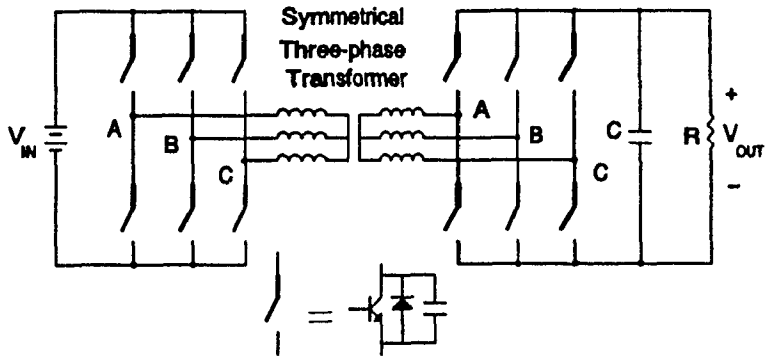


Figure 2-7: Three-phase dual bridge *soft switching* converter.

2.3.5 *Soft switching* single-phase full-bridge PWM dc-dc converter topology

In this section a *soft switching* single-phase full-bridge PWM dc-dc converter topology that experiences zero voltage switching is considered in detail. A phase-shifted PWM technique is presented. The problems associated with this topology are identified. The various topologies proposed in this research area are discussed.

2.3.5.a Phase-shifted PWM technique for single-phase full-bridge converter

When the conventional PWM technique is employed with the single-phase full-bridge topology shown in Fig. 2-8, the diagonal switches are turned on simultaneously (S_1 - S_4, or S_2 - S_3) to apply the input voltage V_{IN} across the primary circuit of the high frequency transformer. Fig. 2-9 shows the switch gating signals as well as the respective voltage waveform V_L across the transformer primary winding. To achieve a freewheeling mode, all the switches are turned off forcing the primary current to decrease towards zero. The load current freewheels through the rectifier diodes and the transformer magnetizing current circulates through the secondary winding and the rectifier diodes as well.

In the phase-shifted PWM technique, the gating signals are such that, instead of turning on the diagonally opposite switches in the bridge simultaneously, like in the conventional PWM technique, a phase-shift is introduced between the gating signals of the switches in the left leg and those in the right one. This phase-shift determines the duty cycle of the converter. The switch gating signals and the respective voltage V_L across the primary circuit are shown in Fig. 2-10. Specifically, with this method, top and bottom switches of the same bridge leg are alternately gated for the fixed interval of nearly half a period (delays to avoid short-circuit path are necessary). Output power control or voltage regulation is obtained by phase shifting the fixed duty cycle gating signals of the two bridge

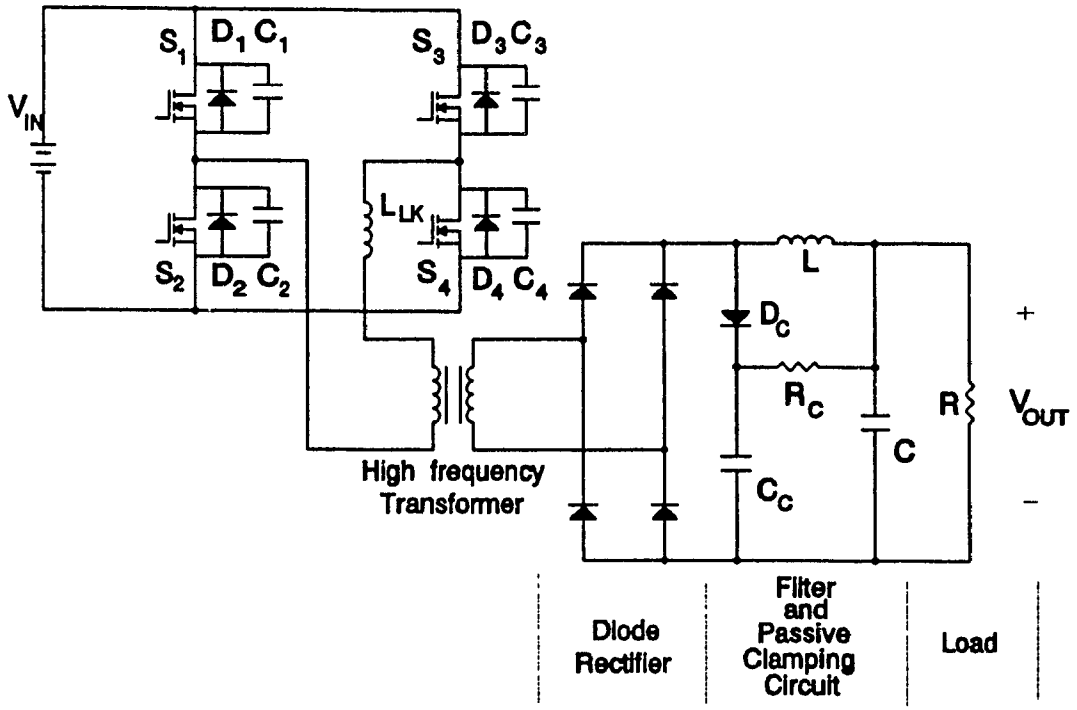


Figure 2-8: Zero voltage switching converter topology with a passive clamping circuit across the secondary side employing phase-shifted PWM technique.

legs with respect to each other. Consequently, when the two pairs of gating signals are in phase, the output voltage is zero and when they are completely out-of-phase, the output voltage is maximum. During the freewheeling mode, either the top two (S_1, S_3) or the bottom two (S_2, S_4) switches are on (Fig. 2-10). The load and the magnetizing currents reflected to the primary can therefore continue to flow in the primary winding, through one switch and one antiparallel diode, thus providing a zero volts interval across the primary circuit. The secondary also freewheels using the energy stored in the output filter inductor.

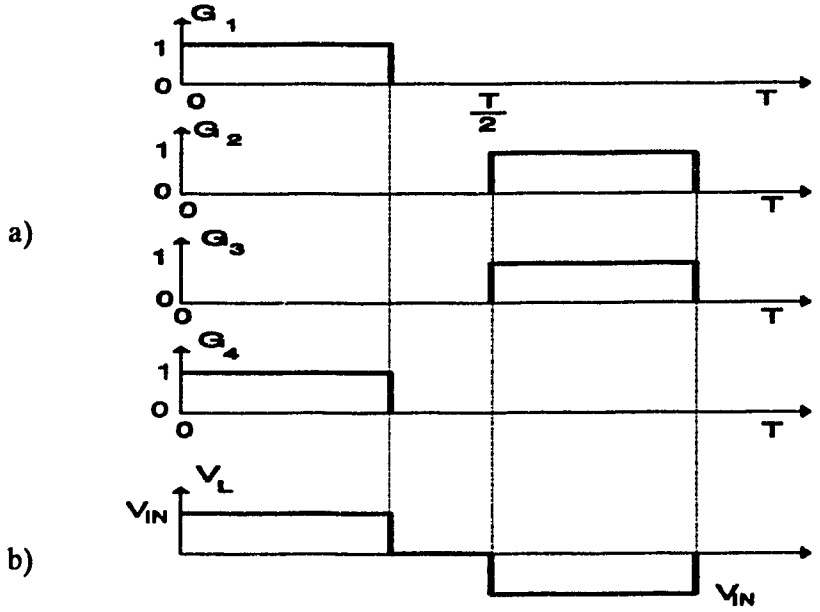


Figure 2-9: Conventional PWM technique for single-phase full-bridge converter.
a) Switch gating signals.
b) Voltage waveform across the primary circuit.

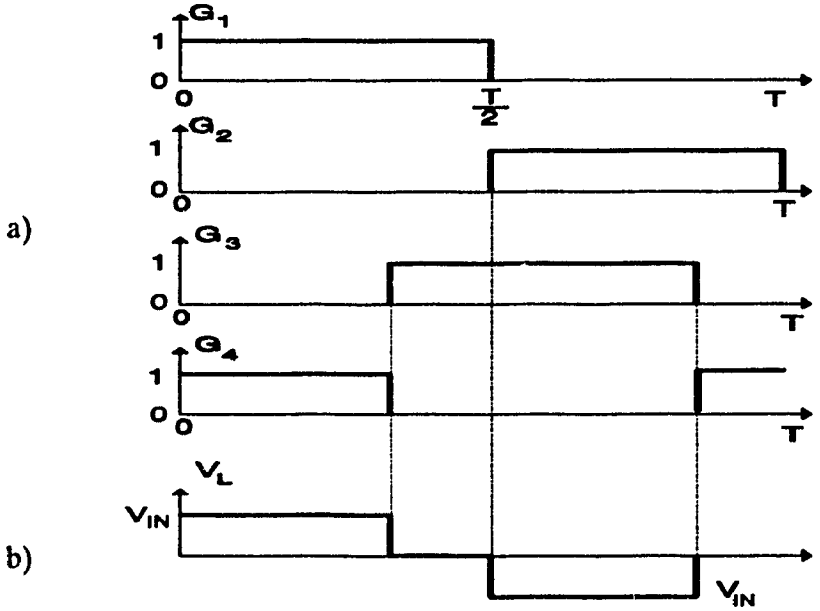


Figure 2-10: Phase-shifted PWM technique for single-phase full-bridge converter.
a) Switch gating signals.
b) Voltage waveform across the primary circuit.

2.3.5.b Phase-shifted PWM technique and zero voltage switching (ZVS)

Employing the phase-shifted PWM technique, and utilizing circuit parasitic elements (L_{LK} and C_1, C_2, C_3, C_4, Fig. 2-8), zero voltage switching conditions for all the devices (S_1 - S_4) can be obtained as follows [32],[33],[34]:

The zero-voltage turn-on is achieved by using the energy stored in the leakage inductor L_{LK} (Fig. 2-8) of the transformer to discharge the switch capacitors (C_1 - C_4) before turning the transistors on. Specifically, S_4 and S_1 are conducting and switch S_4 is turned off. The current through the primary of the transformer charges first the respective capacitor C_4 and discharges the capacitor C_2, turning on the antiparallel diode D_2. After diode D_2 conduction, S_2 can be turned on with zero voltage across the switch. However, in order to achieve zero-voltage turn-on, the energy stored in the leakage inductor L_{LK} needs to be larger than the energy trapped in the switch capacitor. For the other leg, the ZVS is obtained as follows. Switch S_1 is turned off and the current through the primary discharges the capacitor C_3. Consequently, diode D_3 is turned on. After D_3 starts conducting, S_3 can be turned on under zero voltage conditions. In this case, when S_1 is turned off, the current through the primary of the transformer is the output current reflected to the primary. Furthermore, ZVS for switches S_1, S_3 is achieved easily since the energy of the large filter inductor in the secondary side is used to obtain ZVS.

2.3.5.c Advantages of the single-phase full-bridge phase-shifted *soft switching* PWM topology

The advantages of the single-phase full-bridge converter (Fig. 2-8) operating with the phase-shifted PWM technique (Fig. 2-10) can be summarized as follows:

- zero-voltage-switching (ZVS) which enables high frequency operation due to

reduced switching losses;

- simplicity of the control circuit due to the PWM technique compared with the resonant converter control circuit which is very complicated;
- snubberless topology since parasitic elements are utilized to achieve *soft switching* conditions;
- easy optimization of the magnetics and filter designs due to the constant frequency operation;
- the Miller effect for MOSFET devices is minimized due to the ZVS resulting in reduced EMI;
- lower RMS currents than the resonant converter;

2.3.5.d Drawbacks of the single-phase full-bridge phase-shifted *soft switching* PWM topology

On the other hand, for the topology under consideration, the following disadvantages can be identified:

- zero voltage switching conditions are difficult to obtain at very low load (typically lower than 50%);
- the topology is not symmetrical; that is the ZVS conditions for one leg are obtained easier than the other one;
- increased conduction losses due to the higher circulating primary currents;
- the delay time between turn-off of one switch and turn-on of the other in the same leg is not precisely controllable due to the inherent delays associated with the drive circuits;
- higher RMS currents than the conventional *hard switching* PWM topology;

- energy loss during switching turn-off of the rectifier diodes since they are switched at finite but not zero voltage;

In order to overcome the aforementioned drawbacks, improved single-phase full-bridge topologies employing phase-shifted PWM technique have been recently proposed. A brief presentation of these topologies is provided in the following section.

2.3.5.e Improved single-phase full-bridge PWM *soft switching* topologies

The topology discussed above (Fig. 2-8) however, does not provide any means of absorbing the parasitic capacitors of the rectifier diodes [32],[33]. The interaction of the diode rectifier parasitic capacitors with the leakage inductor of the high frequency transformer causes severe voltage overshoot and ringing across the diodes. This problem cannot be solved easily since the leakage inductor of the power transformer is necessary for the operation of the circuit (ZVS).

A passive snubber *R-C* network that clamps the maximum peak voltage of the ringing and returns part of the energy to the output load is proposed in [34]. This arrangement has been shown in Fig. 2-8. The same network is employed in [35] but it is also shown in this paper that this solution can be impractical for high-frequency high-voltage applications. Moreover, this circuit clamps the peak voltage in the secondary circuit, but does nothing to damp or prevent the ringing. The excessive ringing causes EMI and control problems.

More recently, an alternative topology with an active clamping circuit across the secondary winding and the rectifier diodes is investigated [38]. In this case, when the secondary voltage is high, the active clamp circuit, consisting of a clamp capacitor, a snubber diode and an auxiliary switch, connects a large capacitor (voltage source) in parallel with

the diode rectifiers. Therefore, there is no voltage overshoot in the secondary circuit. In steady-state, the average power flow through the clamping capacitor is zero. Energy from the leakage inductor of the transformer is transferred to the clamp capacitor through the snubber diode. The extra energy is discharged to the load through the snubber auxiliary switch. However, the main drawback of this topology is that the duty cycle is restricted to close to unity values. The reason being that under lower values of duty cycle, the overvoltage across the clamping capacitor is increased drastically, therefore the stresses across the semiconductor devices are also increased.

An improved single-phase full-bridge *soft switching* topology, using phase-shifted PWM technique and being able to achieve ZVS under lower load conditions, has been recently proposed [37]. An external commutating inductor and two clamp diodes, added to the phase-shifted single-phase full-bridge PWM converter, substantially reduce the switching losses of the semiconductor devices and the rectifier diodes under lower load conditions as well. However, this topology requires the use of a low leakage power transformer. The design process is complicated and ZVS conditions cannot be obtained under wide range of load.

To overcome all the problems associated with the single-phase full-bridge converter using phase-shifted PWM technique, a novel topology employing an active dc bus snubber subcircuit and conventional PWM technique is proposed and thoroughly analyzed in Chapter 4.

2.4 *Hard switching* dc-ac inverters

Many applications in power electronics require sinusoidal outputs at frequencies ranging from 0-Hz to 400-Hz. A wide variety of approaches have been reported in the

literature for realizing this conversion process. The square-wave six-step inverter which is also called variable voltage inverter (VVI) remains the simplest inverter. It was widely used in the past but has almost completely been replaced by pulse width modulation (PWM) VSI at all but the highest power levels. First, a controlled bridge rectifier or a diode rectifier/chopper as its input is required in order to adjust the dc link voltage. This dc voltage is then subsequently inverted into what is typically a six step ac voltage. The frequency of the output is controlled by the inverter stage while the amplitude is controlled by the rectifier stage or by the chopper. However, it has a number of undesirable features. The most serious problem associated with this topology is that the filter components are bulky and therefore its transient response is very slow.

The six-switch PWM voltage source inverter (VSI) topology overcomes the above mentioned problems. The respective schematic of the six-switch PWM VSI is shown in Fig. 2-11. It is widely used for a dc to 3-phase ac energy conversion due to its simple power structure. The control strategy is reasonably simple and provides a fully regenerative interface between the dc source and the ac load. The use of PWM VSI results in a single power stage for controlling fundamental output voltage and frequency control

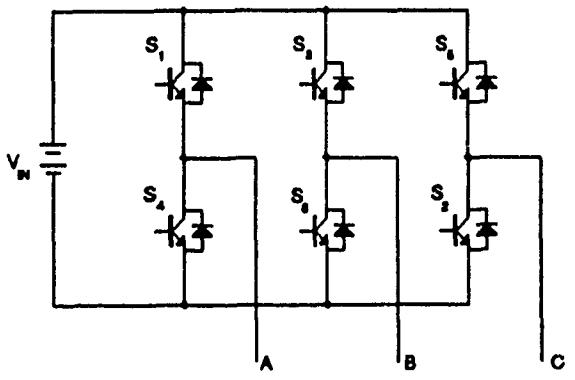


Figure 2-11: *Hard switching* six-switch voltage source inverter.

simultaneously. The use of an uncontrolled diode rectifier front end further reduces the cost especially for low and medium power applications and whenever regeneration capability of the overall system is not extensively required. Different modulation techniques can be employed to achieve certain system performance. The harmonic cancellation or minimization, the sine PWM, the modified sine PWM, the third harmonic injection PWM, the space vector modulation, are a few of the numerous modulation strategies that can be used with the six-switch PWM VSI topology [39],[40],[41]. Semiconductor devices such as MOSFET's and BJT's have almost completely replaced the thyristor at low and medium power levels, and have raised inverter switching frequencies from several hundreds Hz to the multi-kHz level. With the recent advent of IGBT's, switching frequencies in the tens of kHz are now achievable. This is particularly important in sinusoidal output systems, since the size and cost of the reactive elements of the output filter varies inversely with the switching frequency.

However, these converters have the same problems as in the case of dc-dc converters. These problems have been discussed in detail in Section 2.2.2.

2.5 *Soft switching* dc-ac inverters

Inverter topologies which use non-dissipative snubbers to obtain either zero voltage or zero current switching for the active devices are referred to as *soft switching* inverters. Some of the better known topologies are presented in the following sections.

2.5.1 Resonant ac link inverters

The first "family" of *soft switching* inverters are the resonant ac link converters [42]. The concept is to use a high frequency link as an intermediate stage in the power converter,

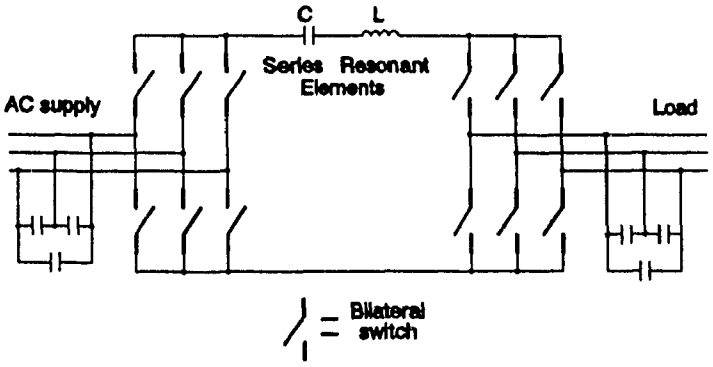


Figure 2-12: Series resonant ac link inverter topology.

as opposed to a dc link. A converter schematic of the series resonant ac link inverter is shown in Fig. 2-12. Both the input converter and the output converter consist of active bilateral devices. The devices are allowed to change state every time the high frequency ac bus voltage goes through a zero crossing, which results in low switching losses.

The output waveform is synthesized with discrete half pulses of the link voltage. Therefore, the output of this converter is a discrete pulse modulated waveform. The spectral characteristics of the output waveforms (subharmonics are typically present) are a serious drawback of the ac link inverter topologies. The use of bilateral switches is also necessary and is considered a disadvantage.

2.5.2 Resonant dc link inverters

A different and newer approach, the six-switch resonant dc link voltage source inverter topology (RDCLI), for realizing zero voltage switching (ZVS) has been recently proposed [43]. The converter schematic is shown in Fig. 2-13. In this case, the dc bus is made to oscillate at a high frequency, so that the bus voltage goes through periodic zero crossings, thus setting up good commutating conditions for all devices connected across the

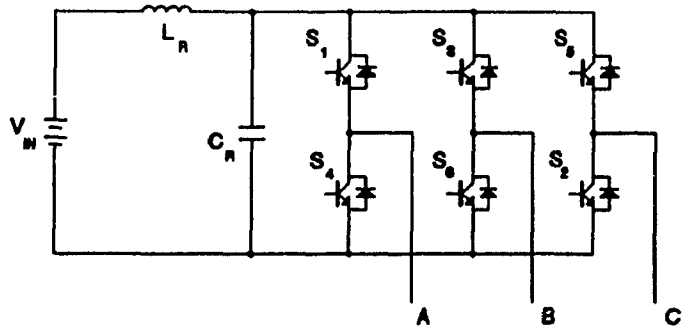


Figure 2-13: The six-switch resonant dc link inverter topology.

dc bus.

The features of the resonant dc link inverter (RDCLI) can be summarized as follows:

- minimum number of power devices;
- elimination of switching losses and snubbers;
- high switching frequency achievable;
- low acoustic noise;
- excellent transient response;
- multi-quadrant operation;
- maximization of power density;
- simple power structure;
- suitable for high power levels with GTO devices;
- system reliability is improved because the devices experience nearly zero switching losses.

However, the topology introduces substantial voltage stresses (>2.5 V_{IN}) across the semiconductor devices. This makes it unattractive for medium and high-power applications.

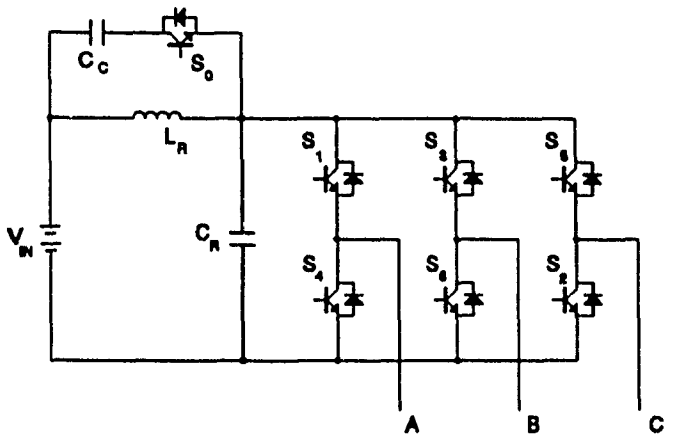


Figure 2-14: Actively clamped resonant dc link inverter topology.

An alternate topology for realizing zero voltage switching in high power converters is the actively clamped resonant dc link inverter (ACRLI) [44],[45],[46],[47]. Fig. 2-14 shows the respective converter topology. This topology has a mode of operation similar to resonant dc link inverter. However, the introduction of the seventh clamp switch S_O restricts the voltage stresses to near 1.5 V_{IN} levels. The control issues associated with this topology are very critical. For instance, it is important that the clamp circuit should be lossless and should not need a continuous power feed from an auxiliary supply. By controlling the turn-off of the clamp switch, it is possible to maintain zero average power flow into the clamp capacitor at the output of the inverter and to regulate the clamping voltage (KV_{IN}) at a preset desired value.

An important and performance wise, restrictive issue associated with the resonant link inverters is their control strategy. Specifically, for the "family" of resonant dc link inverters, since their output waveforms are characterized by discrete pulses, the sigma-delta modulator ($\Sigma\Delta$M) for voltage control or the current regulated delta modulator for current control have to be employed [48],[49],[50]. However, in this case the presence of harmonics

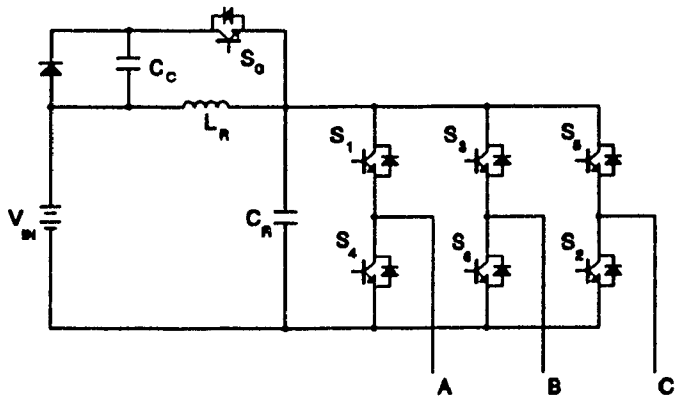


Figure 2-15: Synchronized resonant dc link inverter topology.

below the link frequency and the difficulty of eliminating them, as well as the complexity of the modulation strategies are the most serious drawbacks of these topologies.

An attempt has been made to eliminate the above mentioned problems associated with the discrete modulation strategies and the resonant dc link inverter topologies. Specifically, a synchronized resonant dc link (SRDCL) inverter to realize single-phase and three-phase *soft switching* PWM converters has been proposed [51],[52], Fig. 2-15. An additional mode (idle mode) has been introduced for the link, which allows variable pulse width selection. The control strategy is a hybrid PWM and DPM. This scheme provides improved performance for single-phase applications over the RDCLI [51]. However, it is difficult to eliminate the subharmonics for a three phase application unless the equivalent switching frequency is reduced considerably [52].

More recently a PWM technique for resonant dc link inverters has been proposed [53]. The technique itself does result in reduced levels of subharmonics. However, the PWM switching capability is obtained at the expense of significantly higher losses and device stresses. The regime over which true PWM capability can be applied is rather restricted,

being limited by the energy constraints associated with maintaining the link oscillations, and by the need to conserve charge in the clamp capacitor.

2.5.3 Dc-side commutated inverters

Dc-side commutated inverters employing thyristors are very attractive due to their simplicity and efficient use of the commutation subcircuit [54],[55],[56]. Fig. 2-16 depicts a generalized power circuit configuration without showing any specific dc-bus commutating subcircuit. The most attractive characteristic is that only one commutation subcircuit, placed between the input source and the bridge, is necessary, which considerably simplifies polyphase inverters.

On the other hand, dc-side commutation has several disadvantages such as lower programming freedom since time is needed to operate the commutating subcircuit. The operating frequency of the commutation circuit is usually considerably higher than that of the inverter switches. For these reasons, dc-side commutation can be a good option only for low- and medium-power low-frequency multiphase applications.

Recently, dc-side commutation has also been investigated as an alternative solution to realize *soft switching* three-phase voltage source inverters [57],[58],[59]. However, these dc bus commutating subcircuits are very complex, with the commutating circuit becoming a separate and complete converter by itself. Moreover, the compactness of the inverter power circuit is achieved at the expense of an additional and complicated dc-side commutating circuit, which does not significantly reduce the overall size, weight and cost of the system.

To overcome the problems with the recently proposed inverter topologies, an inverter topology that experiences *soft switching* environment (ZVS) and employs a specific

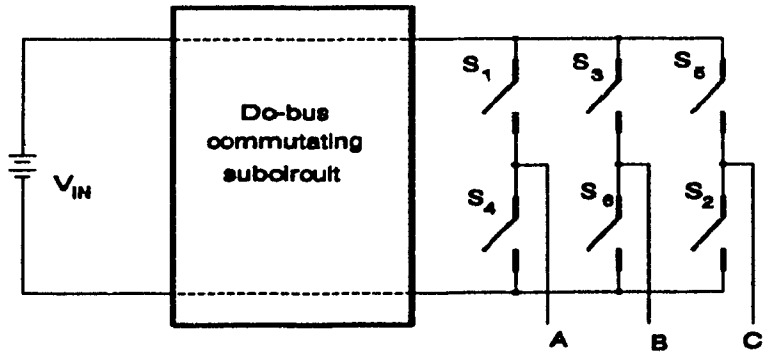


Figure 2-16: Three-phase bridge inverter with dc-side commutation.

PWM technique is proposed in Chapter 5.

2.6 Conclusions

The various converter topologies, namely the *hard switching* and the *soft switching* ones, for dc-dc and dc-ac energy conversion employing force-commutated devices have been discussed in some detail in the previous sections. The most serious problems associated with these converters as well as their advantages have also been critically evaluated.

It can be concluded that the ideal converter topology would combine the best features of resonant class and PWM class of topologies. These include low switching losses, constant frequency operation, reasonably rated reactive components and a wide control of load.

This is the purpose of this thesis and a single-phase full-bridge high-power low-frequency *soft switching* PWM converter topology is proposed and studied in the following chapter.

CHAPTER 3

AN IMPROVED LOW-FREQUENCY HIGH-POWER SINGLE-PHASE FULL-BRIDGE PWM CONVERTER TOPOLOGY

3.1 Introduction

When PWM topologies are to be used for energy conversion, it is more efficient to combine snubber components and to use for instance one reactive element (inductor to control *di/dt,* capacitor to control *dv/dt*) for both switches of the same converter leg. Such an improved snubber network suitable for BJT's or GTO's based PWM converter has been proposed in [14].

A single-phase full-bridge PWM converter topology employing the improved snubber network is shown in Fig. 3-1. However, the losses associated with the original form of the snubber subcircuit proposed in [14] (Fig. 3-1) can be substantial at high power levels. Therefore, it is an important issue to employ an energy recovery subcircuit to improve the overall system efficiency. Such a simple and active energy recovery subcircuit is investigated in this chapter [63]. Specifically, the improvement under discussion consists of replacing the discharge resistor (Fig. 3-1) with an auxiliary switch (Fig. 3-2). Detailed converter description and analysis are provided in the following sections.

3.2 Converter power circuit description

The circuit realization of a single-phase full-bridge converter with the low loss snubber network [14] is shown in Fig. 3-1. The converter power circuit includes the dc

supply voltage V_{IN} , the four converter switches (S_1 , S_2 , S_3 , S_4), the antiparallel switch diodes, the dc bus snubber inductor L_S , the storage-clamp capacitor C_C , the two snubber capacitors C_1 , C_2 , the four snubber diodes (D_1 , D_2 , D_3 , D_4), the discharge resistor R_S for the capacitor C_C , the output transformer, the full-bridge rectifier stage, the output filter and the load shown as a resistor.

The circuit realization of the single-phase full-bridge PWM topology when employing the proposed active energy recovery subcircuit is shown in Fig. 3.2 respectively.

3.3 Advantages of the proposed PWM converter topology

The type of power converter proposed in this chapter (Fig. 3-2) has the following positive features:

i) The switching behaviour of the four converter switches (i.e. GTO's, BJT's, IGBT's, etc.) is dictated by the charging rate of the two snubber capacitors C_1 , C_2 . It is therefore smooth and controllable.

ii) The recovery stress of the four switch antiparallel diodes is also controlled by the charging rate of these snubber capacitors C_1 , C_2 . Therefore, parasitic switch diodes can be used as free wheeling diodes.

iii) The recovery stress of the rectifier diodes is also controlled by the charging rate of the same capacitors (C_1 , C_2). Therefore, semiconductor stresses and losses due to the output rectifier stage are also minimized.

iv) The overall converter efficiency is increased since, at least, theoretically, all the energy associated with the snubber elements is recovered.

Consequently, the addition of this simple active energy recovery snubber network improves the performance of the converter topology under consideration and makes it even

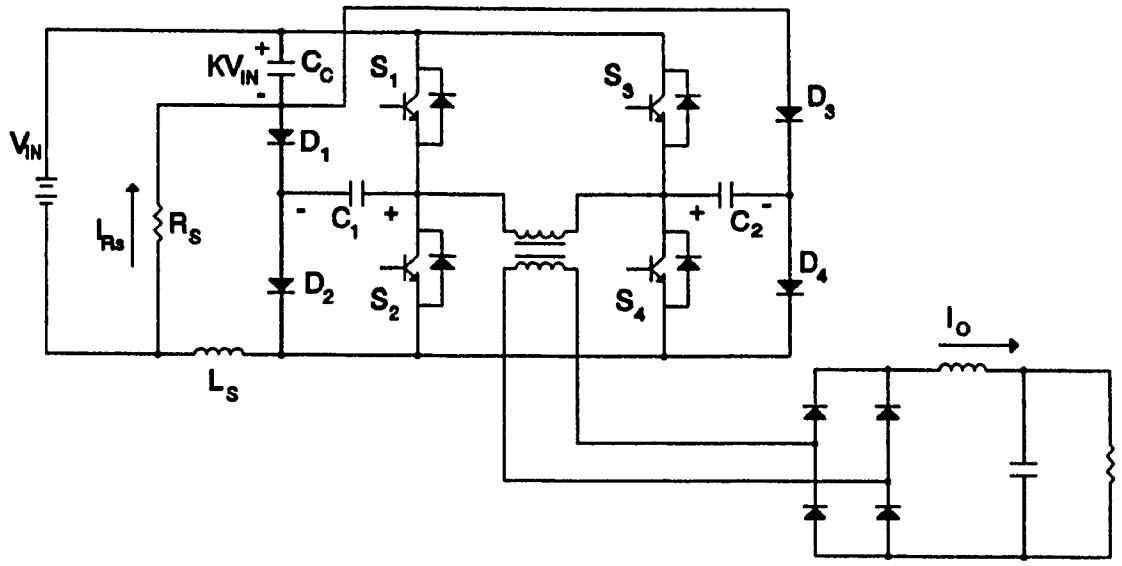


Figure 3-1: The single-phase full-bridge PWM dc-dc converter topology with the low loss snubber network [14].

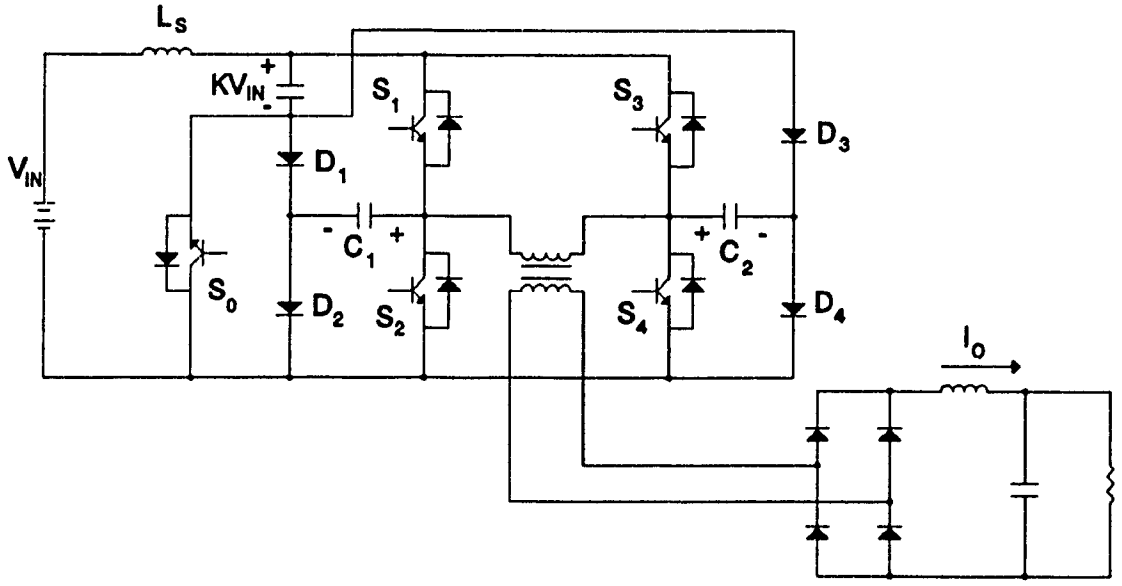


Figure 3-2: The single-phase full-bridge PWM dc-dc converter topology with the lossless snubber network.

more attractive for high power industrial applications.

3.4 Principles of operation

The principles of operation for both power circuit configurations; the original (Fig. 3-1) and the modified topology with the active energy recovery network (Fig. 3-2) are presented in this section. Identification of the topological modes (TM's) during a switching cycle is also presented, along with the voltage-current expressions.

3.4.1 PWM converter employing low loss snubber network

Because of the dc bus snubber inductor L_S , the current through the converter switches is not permitted to increase while the switch voltage is decreasing towards zero during turn-on. Therefore, since zero current turn-on conditions are obtained, the turn-on semiconductor losses are minimized. During switch S_1 , S_4 turn-on, capacitor C_1 is charged through diode D_2 to the voltage of the storage-clamp capacitor C_C , since the diode D_1 clamps the voltage. During turn-off, C_1 is discharged via diode D_1 . The snubber capacitor C_2 operates in a similar manner as C_1 during the other half of the switching period. Due to the fact that capacitors (C_1 , C_2) are connected across each switch during turn-off, the turn-off switching losses are minimized since zero voltage turn-off is achieved. The energy of the inductor L_S is transferred to the storage-voltage clamp capacitor C_C after the turn-off of the converter switches. Energy from the snubber capacitors is also transferred to capacitor C_C through a low loss path (snubber resistor R_S) and some energy is lost in the discharge resistor R_S . However, the lost energy is significantly less than in the case of using conventional snubber networks for each switch separately (Fig. 1-1).

3.4.2 PWM converter employing lossless snubber network

The circuit shown in Fig. 3-2 employs the same snubber subcircuit previously discussed in combination with a simple active energy recovery network. Specifically, the discharge resistor R_S (Fig. 3-1) is replaced by an auxiliary switch S_O (Fig. 3-2). Employing this snubber, the overall converter efficiency is increased, since, at least theoretically no energy associated with snubber elements is lost. Instead the energy is transferred to the storage-voltage clamp capacitor C_C .

There are two ways of discharging the capacitor C_C ; first, by sending the energy back to the dc bus whenever the main converter switches are conducting (the energy is transferred to the load) or secondly, whenever the load current freewheels at the output rectifier circuit (the energy is transferred back to the source). For instance, the auxiliary switch S_O could be turned on after a fixed time interval, following the turn-on time of the converter switches S_1, S_4 or S_2, S_3. That is because, it is desirable to turn-on the converter switches through the dc bus snubber inductor L_S (turn-on switching losses and respective EMI are minimized since *di/dt* is controlled). The switch S_O could be also turned-on a fixed time before the converter switches turn on. Consequently, by controlling the on time of the auxiliary switch S_O , it is possible to maintain a preset and desired value for the overvoltage across the capacitor C_C if the average power flow into the capacitor is kept zero.

The analysis presented below includes the identification of the topological modes (TM's) during a switching cycle and the perspective voltage-current expressions.

3.5 Modes of operation - Steady state analysis

In the following section, the description of the different topological modes (TM's) and the exact analytical expressions describing the converter currents and voltages

(Figs. 3-1,3-2) during a switching cycle and under rated steady-state conditions are obtained.

The analysis is based on the following assumptions:

- The switches and the diodes are ideal.
- The capacitors and the inductors are lossless.
- The value of the storage-voltage clamp capacitor C_C is very large compared with the snubber capacitors C_1, C_2, hence C_C can be replaced by a voltage source.
- The magnetizing current of the transformer is neglected.
- The load current I_O is assumed ripple-free.
- The supply voltage V_{IN} is also assumed ripple-free.
- Stray parasitics are neglected.

3.5.1 Single-phase full-bridge PWM converter topology with low loss snubber network

In this subsection the complete analysis concerning the single-phase full bridge dc-dc power converter topology with the low loss snubber network (Fig. 3-1) is presented.

Initial conditions

At $t=0$, it is assumed that the storage-voltage clamp capacitor C_C has the initial voltage (Fig. 3-4(e)):

$$V_{CC}|_{t=0} = KV_{IN} \tag{3.1}$$

where

$$K > 1 \tag{3.2}$$

The two snubber capacitors have the same value

$$C_1 = C_2 = C_S \tag{3.3}$$

and the following voltages (Fig. 3-4(b),(c));

$$V_{C1}|_{t=0} = V_{C2}|_{t=0} = \frac{KV_{IN}}{2} \tag{3.4}$$

with the polarity shown in Fig. 3-1.

All the snubber diodes D_1 - D_4 are reversed biased (Fig. 3-4(f),(g));

$$V_{D1}|_{t=0} = V_{D2}|_{t=0} = V_{D3}|_{t=0} = V_{D4}|_{t=0} = -\frac{(K-1)V_{IN}}{2} \tag{3.5}$$

The voltage across the discharge resistor R_S is as follows;

$$V_{Rs}|_{t=0} = (K-1)V_{IN} \tag{3.6}$$

hence, the direction of the current through the discharge resistor R_S is as shown in Fig. 3-1;

$$i_{Rs}|_{t=0} = \frac{(K-1)V_{IN}}{R_S} \tag{3.7}$$

The current through the dc bus snubber inductor L_S (Fig. 3-4(a)) is

$$i_{Ls}|_{t=0} = 0 \tag{3.8}$$

Turn-on process.

Mode 1, Interval $0 < t < t_1$.

The switches S_1 and S_2 are turned on at $t=0$. The load current I_O continues to freewheel in the output rectifier circuit, and the snubber inductor L_S current starts to increase (Fig. 3-4(a)). The dc bus voltage decreases towards zero. The snubber capacitors C_1 , C_2 continue to have the same voltage (3.4) (Fig. 3-4(b),(c)). The snubber diodes (D_1 - D_4) are still reversed biased by the following voltage (Fig. 3-4(f),(g));

$$V_{D1}|_{t=0^+} = V_{D2}|_{t=0^+} = V_{D3}|_{t=0^+} = V_{D4}|_{t=0^+} = -\frac{KV_{IN}}{2} \tag{3.9}$$

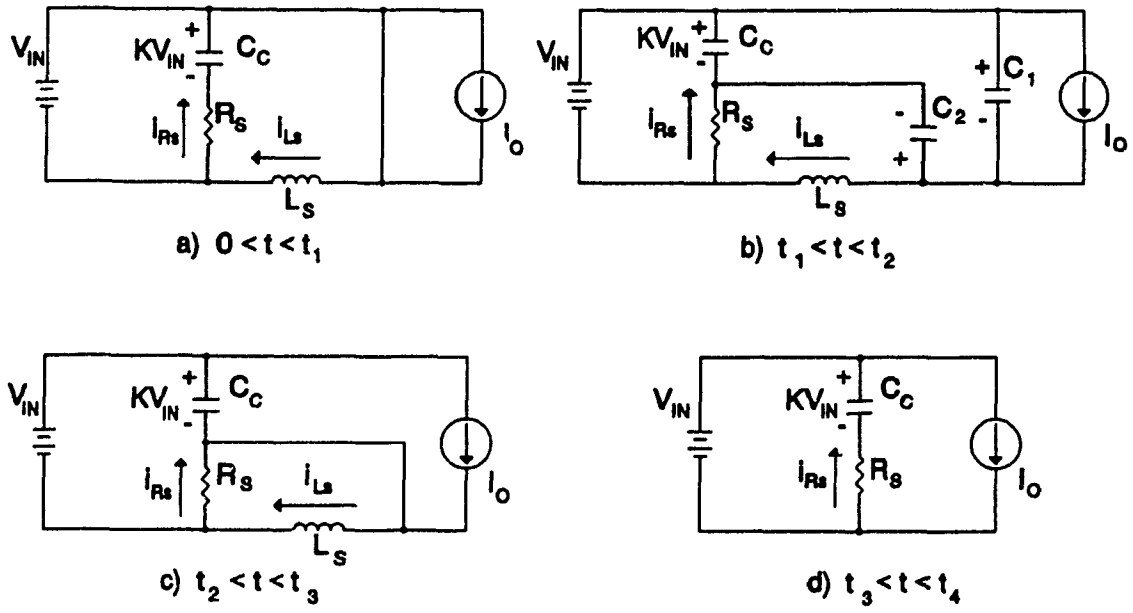


Figure 3-3: Converter topological modes (TM's) during switching cycle turn-on. Low loss snubber network.

a) Mode 1: $0 < t < t_1$.

b) Mode 2: $t_1 < t < t_2$.

c) Mode 3: $t_2 < t < t_3$.

d) Mode 4: $t_3 < t < t_4$.

The voltage of the storage-clamp capacitor C_C remains constant (3.1) (Fig. 3-5(e)). The equivalent converter circuit for this mode is shown in Fig. 3-3(a). The load current through the filter inductor is shown as a current source I_O. It is an inductive load circuit and the current through the snubber inductor L_S (Fig. 3-5(a)) is given by the following equation

$$i_{Ls}(t) = \frac{V_{IN}}{L_S} t + i_{Ls}|_{t=0} \tag{3.10}$$

This mode changes when the inductor L_S current and the current drawn from the storage capacitor C_C are equal to the load current I_O ;

$$i_{Ls}|_{t=t_1} + \frac{(K-1)V_{IN}}{R_S} = I_O \tag{3.11}$$

therefore, the duration of this mode (Fig. 3-4(a)) is

$$t_1 = \frac{I_O R_S - (K-1)V_{IN}}{R_S V_{IN}} L_S \tag{3.12}$$

Finally, switching turn-on losses are minimized since the dc bus snubber inductor L_S provides zero loss commutations for all converter switches (*di/dt* is controlled).

Mode 2, Interval $t_1 < t < t_2$.

The load current stops freewheeling through the rectifier diodes and the filter inductor. The dc bus voltage starts to increase and beyond the voltage of C_1 , C_2 ($KV_{IN}/2$), the diodes D_2 , D_3 start conducting (Fig. 3-4(g)).

$$V_{D1}|_{t=t_1^+} = V_{D4}|_{t=t_1^+} = -\frac{KV_{IN}}{2} \tag{3.13}$$

$$V_{D2}|_{t=t_1^+} = V_{D3}|_{t=t_1^+} = 0 \tag{3.14}$$

The snubber inductor L_S oscillates with the snubber capacitors C_1 , C_2 . Specifically, capacitor C_1 is charged through the diode D_2 to the voltage of the storage capacitor C_C (KV_{IN}) since the diode D_1 clamps the voltage of C_1 (Fig. 3-4(b)). Concurrently, capacitor C_2 is discharged towards zero through the snubber diode D_3 (Fig. 3-4(c)). The energy associated with C_2 is transferred to the storage capacitor C_C through the low loss path of the discharge resistor R_S . The voltage across the storage capacitor C_C is constant (KV_{IN}).

Fig. 3.3(b) demonstrates the equivalent circuit. The equation for the current through the snubber inductor L_S is as follows

$$i_{Ls}(t) = I_O + (1 - \frac{K}{2}) \sqrt{\frac{2C_S}{L_S}} V_{IN} \sin[\omega_r (t-t_1)] \tag{3.15}$$

where

$$\omega_r = \sqrt{\frac{1}{2L_SC_S}} \tag{3.16}$$

The converter mode changes (Fig. 3-4(b),(c)), when

$$V_{C1}|_{t=t_2} = KV_{IN} \tag{3.17}$$

$$V_{C2}|_{t=t_2} = 0 \tag{3.18}$$

At $t=t_2$, the inductor current has the value

$$I_{Ls}|_{t=t_2} = I_O + (1 - \frac{K}{2}) \sqrt{\frac{2C_S}{L_S}} V_{IN} \sin[\omega_r(t_2-t_1)] \tag{3.19}$$

The maximum value of the snubber inductor L_S current (Fig. 3-4(a)) is

$$I_{max} = I_O + (1 - \frac{K}{2}) \sqrt{\frac{2C_S}{L_S}} V_{IN} \tag{3.20}$$

Mode 3, Interval $t_2 < t < t_3$.

The extra energy of the dc bus snubber inductor L_S is transferred to the storage capacitor C_C during this mode, through the snubber diodes. Moreover, all the diodes D_1-D_4

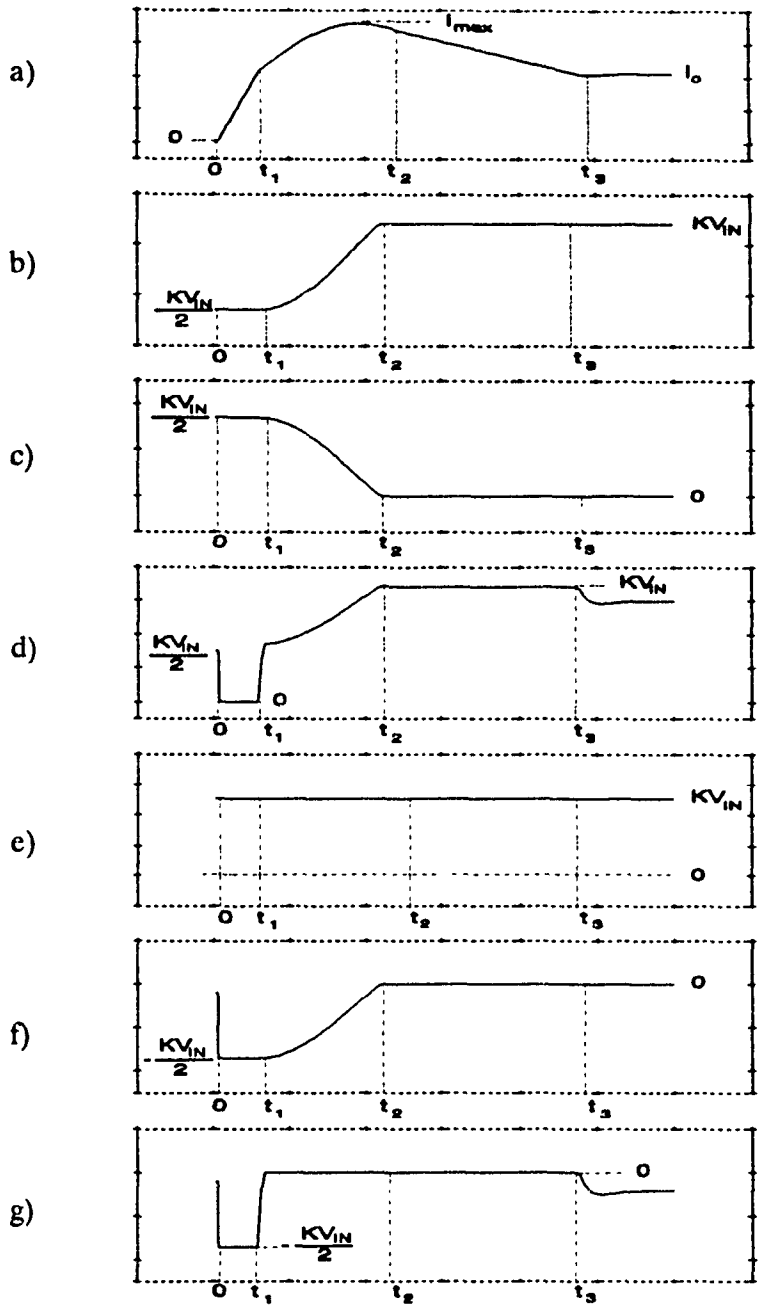


Figure 3-4: Converter waveforms at turn-on of S_1 , S_4 - Low loss snubber network.
a) Inductor L_S current.
b) Voltage of the snubber capacitor C_1 .
c) Voltage of the snubber capacitor C_2 .
d) Switch S_2 , S_3 voltage.
e) Voltage of the storage-clamp capacitor C_C .
f) Voltage across the snubber diodes D_1 , D_4 .
g) Voltage across the snubber diodes D_2 , D_3 .

are conducting (Fig. 3-4(f),(g)). The voltages across the snubber capacitors C_1, C_2 are as before (3.17),(3.18) (Fig. 3-4(b),(c)). The respective equivalent circuit is displayed in Fig. 3-3(c). Since the voltage across the storage capacitor C_C is constant (KV_{IN}), the decrease rate of the inductor current is dictated by L_S and $(K-1)V_{IN}$ as well (Fig. 3-4(a)).

$$i_{L_S}(t) = I_{L_S}|_{t=t_2} - \frac{(K-1)}{L_S} V_{IN} (t-t_3) \tag{3.21}$$

The mode changes when

$$I_{L_S}|_{t=t_3} = I_O \tag{3.22}$$

The voltage across the converter switches approaches the overvoltage KV_{IN} of the C_C. Therefore the overvoltage factor K is an important design aspect for the converter under discussion.

Mode 4, Interval $t_3 < t < t_4$.

At $t=t_3$, the turn-on process has been completed. Due to the voltage difference across the resistor R_S, the current flowing through C_C is as before (3.7);

$$i_{R_S}(t) = \frac{(K-1)}{R_S} V_{IN} \tag{3.23}$$

The current flowing through the snubber inductor L_S is constant;

$$i_{L_S}(t) = I_O - \frac{(K-1)}{R_S} V_{IN} \tag{3.24}$$

All the snubber diodes are reversed biased. Fig. 3-3(d) displays the equivalent circuit. The moment that this mode changes is dictated by the duty cycle of the converter.

$$t_4 = \frac{d}{2f_{SW}} \tag{3.25}$$

where the duty cycle is defined as follows;

$$d = \frac{t_{ON|S1,S4} + t_{ON|S2,S3}}{2} f_{SW} \tag{3.26}$$

f_{SW} is the converter switching frequency.

Turn-off process.

Mode 5, Interval $t_4 < t < t_5$.

At $t=t_4$, the switches S_1 and S_4 are turned off and the switch current begins to decrease at a rate limited only by the commutation characteristics of the switches. The rise rate of the switch voltage is dictated by the value of the snubber capacitors C_1 , C_2 and the level of the load current I_O as well. However, because of the snubber inductor L_s , the dc bus current cannot change instantaneously. Instead, the energy from the dc bus inductor L_S is transferred to the storage-voltage clamp capacitor C_C . During switch S_1 turn-off, capacitors C_C and C_1 with equal voltage and different polarity are connected through the diode D_1 across S_1 thus minimizing turn-off losses and stresses. Respectively, during switch S_4 turn-off, the snubber capacitor C_2 is connected across S_4 through the diode D_4 . Therefore, zero voltage switching turn-off conditions are provided for both converter switches (S_1 , S_4). During this mode capacitor C_1 is discharged and capacitor C_2 is charged. Moreover, the two snubber capacitors C_1 , C_2 are placed in series with the storage-clamp capacitor C_C and the load current I_O is flowing through. Capacitor energy from C_1 is transferred to the load and some is stored in the snubber capacitor C_2 . At the end of this mode, capacitors C_1 , C_2 share the voltage across the storage capacitor C_C (Fig. 3-6(f),(g)). The equivalent converter circuit is shown in Fig. 3-5(a). The current through the inductor L_S has the following equation

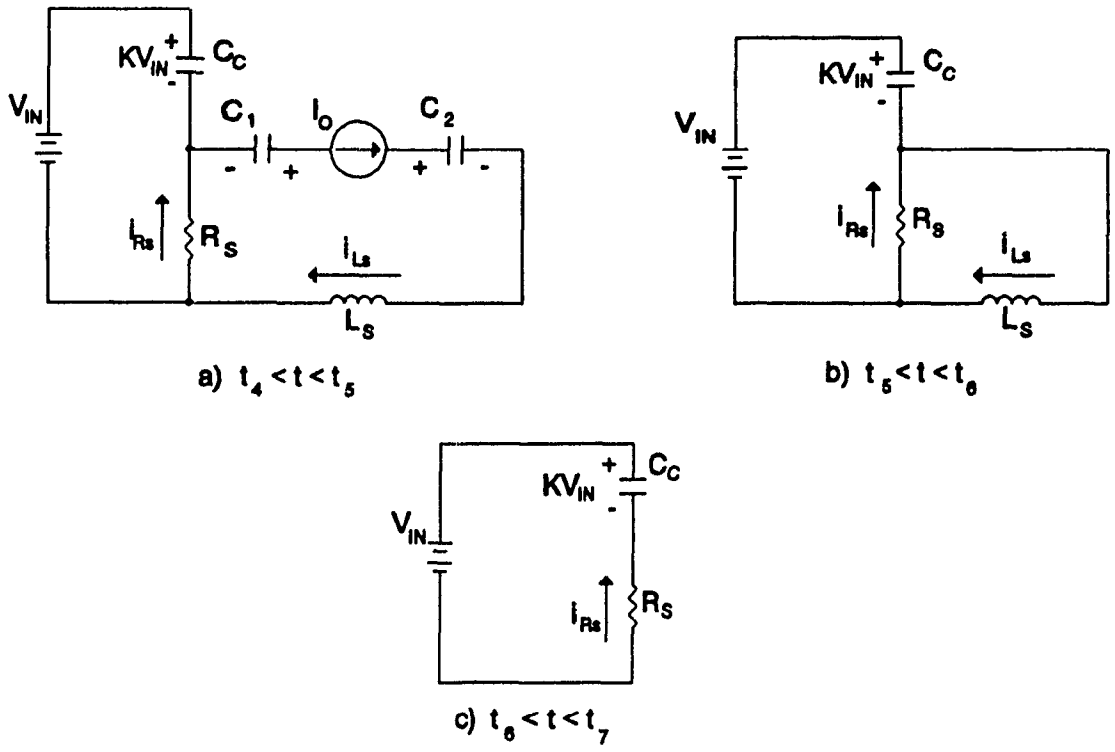


Figure 3-5: Converter topological modes (TM's) during switching cycle turn-off. Low loss snubber network.

a) Mode 5: $t_4 < t < t_5$.

b) Mode 6: $t_5 < t < t_6$.

c) Mode 7: $t_6 < t < t_7$.

$$i_{Ls}(t) = I_O - \frac{K-1}{L_S} V_{IN} (t-t_4) \tag{3.27}$$

The initial and final conditions for the snubber capacitors voltages (Fig. 3-6(b),(c)) are as follows:

$$V_{C1}|_{t=t_4} = KV_{IN} \tag{3.28}$$

$$V_{C2}|_{t=t_4} = 0 \tag{3.29}$$

The converter changes mode when the following condition is held

$$V_{C1}|_{t=t_5} = V_{C2}|_{t=t_5} = \frac{KV_{IN}}{2} \tag{3.30}$$

From these conditions and assuming that the load current is constant during this mode, the duration t_5-t_4 is approximately

$$t_5 - t_4 = \frac{KV_{IN}C_S}{2I_O} \tag{3.31}$$

The snubber capacitors can be designed so that specific *dv/dt* across the converter switches can be obtained to ensure zero turn-off switching losses. At the end of this mode ($t=t_5$), the load current starts freewheeling in the output circuit, through the rectifier diodes and the filter inductor.

Mode 6, Interval $t_5 < t < t_6$.

During this mode, the remaining inductor L_S energy is transferred in the storage capacitor C_C. All the snubber diodes (D_1 - D_4) are conducting (Fig. 3-6(f),(g)). The slope of the inductor L_S current is dictated by the voltage difference between the storage capacitor C_C voltage (KV_{IN}) and the value of the snubber inductor L_S (Fig. 3-6(a)). The respective equivalent circuit is displayed in Fig. 3-5(b). The equation for the snubber inductor current is

$$i_{Ls}(t) = I_O + \frac{(1-K)V_{IN}}{L_S}(t-t_5) \tag{3.32}$$

The duration of this mode is

$$t_6 - t_5 = \frac{I_O\, L_S}{(K-1)V_{IN}} \tag{3.33}$$

Mode 7, Interval $t_6 < t < t_7$.

All the snubber diodes are reversed biased and all the converter switches are off. The load current continues to freewheel at the output rectifier circuit. The voltage across the storage capacitor C_C is constant (Fig. 3-6(e)). Fig. 3-5(c) denotes the equivalent circuit. The current through the discharge resistor R_S is as before;

$$i_{Rs}(t) = \frac{(K-1)V_{IN}}{R_S} \tag{3.34}$$

$$i_{Ls}(t) = 0 \tag{3.35}$$

3.5.2 Single-phase full-bridge PWM converter topology with lossless snubber network

The topological modes (TM's) concerning the single-phase full-bridge power converter topology with the lossless snubber network (Fig. 3-2) are to be discussed.

The storage-clamper capacitor C_C has again an overvoltage (KV_{IN}) (3.1),(3.2) which practically might not be equal to the overvoltage obtained in the previous case. The snubber elements (L_S , C_1 , C_2) have the same values as before. The sequence of the topological modes is the same as in the case of the low loss snubber network previously presented. However due to the absence of the discharge resistor R_S all the energy associated with the snubber elements is stored in the storage-clamp capacitor C_C. The maximum current during the resonant mode is as before (3.20). Only when the auxiliary

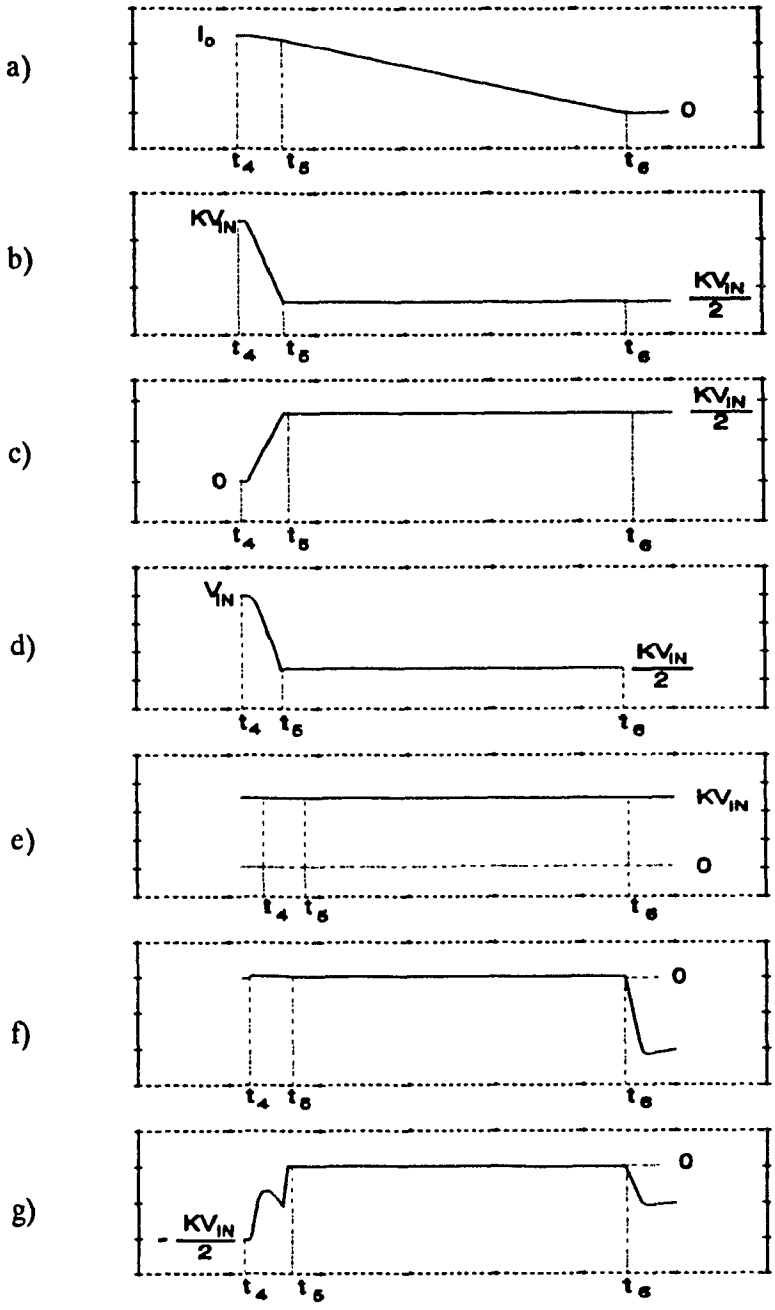


Figure 3-6: Converter waveforms at turn-off of S_1, S_4 - Low loss snubber network.
a) Inductor L_S current.
b) Voltage of the snubber capacitor C_1.
c) Voltage of the snubber capacitor C_2.
d) Switch S_2, S_4 voltage.
e) Voltage of the storage-clamp capacitor C_C.
f) Voltage across the snubber diodes D_1, D_4.
g) Voltage across the snubber diodes D_2, D_3.

switch S_O is turned on to discharge C_C, the voltage difference $(K\text{-}1)V_{IN}$ is applied across the dc bus snubber inductor L_S and current in a negative direction is flowing through the dc bus inductor L_S. The equation of the current through the dc bus inductor L_S when the auxiliary switch S_O conducts is as follows:

$$i_{L_S}(t) = -\frac{(K-1)V_{IN}}{L_S}(t-t_0) + I_{L_S}|_{t=t_0} \tag{3.36}$$

where

t_0 is the moment that S_O is turned on.

3.6 Discussion - Design guidelines

The equations presented in the preceding sections are used next to design a complete single-phase full-bridge PWM dc-dc converter employing the low loss or the lossless snubber networks under discussion. The output power P_{OUT}, the output voltage V_{OUT} and the switching frequency f_{SW} are the desired specifications of the converter. Both the topologies discussed in this chapter are off-line dc-dc converters, hence variations in the input ac line-to-line voltage in the front-end rectifier stage have to be taken into account for a worst case design. The voltage of the storage-clamp capacitor C_C is another important design aspect. The overvoltage factor K (3.2) has to be slightly higher than unity, because the voltage of C_C is the maximum voltage applied across all converter switching components.

Assuming that the input unregulated dc power supply voltage variation is

$$V_{INMIN} < V_{IN} < V_{INMAX} \tag{3.37}$$

The dc output voltage (assuming a 1:1 output transformer turns ratio) for the case of the maximum duty cycle is

$$V_{OUT} = d_{MAX} V_{INMIN} \tag{3.38}$$

Respectively, for the case of the minimum duty cycle

$$V_{OUT} = d_{MIN} V_{INMAX} \tag{3.39}$$

The output load current under rated conditions is as follows:

$$I_O = \frac{P_{OUT}}{V_{OUT}} \tag{3.40}$$

The overvoltage factor K can be estimated as follows. For the minimum duty cycle, the dead time that all converter switches are off (free-wheeling mode) is given by the following equation;

$$t_{dead} = \frac{1 - d_{MIN}}{2 f_{SW}} \tag{3.41}$$

3.6.1 Design procedure for the single-phase full-bridge PWM converter with low loss snubber network

Theoretically, the dead time (3.41) can be equal to the duration of the mode 6 as described before assuming that the duration of the mode 5 is very small. Therefore, approximately,

$$K = 1 + \frac{2 I_O L_S f_{SW}}{(1-d_{MIN})V_{INMAX}} \tag{3.42}$$

The energy that leaves the storage-clamp capacitor C_C through the discharge resistor R_S is approximately

$$W_{OUT} = \frac{(K-1)V_{INMAX}}{R_S C_C f_{SW}} \tag{3.43}$$

Similarly, the energy that enters C_C under rated conditions is approximately

$$W_{IN} = \frac{2\, I_O^2\, L_S}{C_C\,(K-1)\, V_{INMAX}} \tag{3.44}$$

Under steady-state conditions

$$W_{OUT} = W_{IN} \tag{3.45}$$

The dc bus snubber inductor L_S has to be designed according to turn-on time of the switches, to ensure zero turn-on switching losses. The discharge resistor R_S can be calculated from the following function

$$R_S = \frac{(K-1)^2 V_{INMAX}^2}{2\, f_{SW}\, I_O^2\, L_S} \tag{3.46}$$

The energy dissipated in the discharge resistor R_S can be also estimated. The current through R_S is

$$I_{Rs} = \frac{(K-1) V_{INMAX}}{R_S} \tag{3.47}$$

and the losses can be easily computed from the following equation;

$$P_{Rs} = \frac{(K-1)^2\, V_{INMAX}^2}{R_S} \tag{3.48}$$

3.6.2 Design procedure for the single-phase full-bridge PWM converter with lossless snubber network

The same approach can be used to design the active energy recovery subcircuit. The width of the gating signal of the auxiliary switch can be estimated so that under rated load a specific overvoltage across the storage capacitor C_C can be obtained.

The energy that enters C_C is the energy stored in the snubber inductor L_S mainly and the energy stored in the snubber capacitors C_1, C_2.

$$W_{IN} = \frac{1}{2} L_S I_O^2 + 2\frac{1}{2} C_S \frac{[(K-1) V_{INMAX}]^2}{2} \tag{3.49}$$

When the auxiliary switch turns-on the energy that leaves C_C taking into account the equation for the inductor L_S current (3.36), for specific on-time ($t_{ON,So}$) is approximately

$$W_{OUT} = \frac{1}{2} \frac{(K-1)^2 V_{INMAX}^2 t_{ON,So}^2}{L_S} \tag{3.50}$$

Therefore under steady-state rated conditions the width of the gating signal applied to the switch S_O can be computed from the following formula

$$t_{ON,So} = \sqrt{\frac{L_S^2 I_O^2}{(K-1)^2 V_{INMAX}^2} + \frac{L_S C_S}{2}} \tag{3.51}$$

Theoretically, the sum of this time ($t_{ON,So}$), the time needed to reset the inductor current (mode 6) and the time needed to reset the current from the negative value to zero have to be equal to the dead time as before (3.41). Therefore

$$\frac{1-d_{MIN}}{2 f_{SW}} = \frac{2 I_O L_S}{(K-1) V_{INMAX}} + \sqrt{\frac{L_S^2 I_O^2}{(K-1)^2 V_{INMAX}^2} + \frac{L_S C_S}{2}} \tag{3.52}$$

Hence K can be estimated by iteration to satisfy the above equation (3.52). Then, the on-time of the auxiliary switch S_O can be computed using eqn. (3.51).

3.7 Design example

In this section a design example for both power converter configurations is provided. Experimental verification follows in Section 3.10.

The converters shown in Figs. 3-1,3-2 are to be designed for the following specifications.

Output power $P_{OUT} = 5.0$ kW

Output voltage $V_{OUT} = 240$ V

Switching frequency $f_{SW} = 10$ kHz

Assuming that the input unregulated dc voltage variation is

$$280 \text{ V} < V_{IN} < 300 \text{ V}$$

The duty cycle for the maximum input voltage is

$$d_{MIN} = 0.8$$

3.7.1 PWM converter topology with the low loss snubber network

The dc bus snubber inductor L_S is to be designed according to the *di/dt* rate during turn-on, to ensure zero switching losses. Taking into account

$$\frac{di}{dt} = 20 \ A/\mu s$$

and because $V_{INMAX} = 300$ V and using eqn. (3.10)

$$L_S = \frac{300 \ V}{20 \ A/\mu s} = 15 \ \mu H$$

The two snubber capacitors are to be designed according to the *dv/dt* rate during turn-off to ensure minimum switching losses. Similarly, taking into account

$$\frac{dv}{dt} = 200 \ V/\mu s$$

under rated conditions the output current (3.40) is

$$I_O = \frac{5000\ W}{240\ V} = 21.8\ A$$

therefore

$$C_S = \frac{21.8\ A}{200\ V/\mu s} = 0.1\ \mu F$$

Since for the maximun input voltage the duty cycle is $d=0.8$ under rated conditions and using eqn. (3.42) the overvoltage factor K for this particular example is

$$K = 1.133$$

Therefore

$$V_{CC,MAX} = 340\ \text{V}$$

and finally the discharge resistor R_S can be calculated from eqn. (3.46);

$$R_S = 11.5\ \Omega$$

The losses can be also estimated;

$$P_L = 138\ \text{W}$$

Hence, the losses associated with the snubber elements, currently dissipated in the discharge resistor R_S, are 2.76% of the output rated power for this particular example.

The maximum current during the resonant mode (2) is according to eqn. (3.20)

$$I_{max} = 33.5\ \text{A}$$

3.7.2 PWM converter topology with the lossless snubber network

Following the analysis previously presented concerning the converter topology that employs the lossless snubber network, and for the same specifications as before, the width of the gating signal of the auxiliary switch can be calculated as follows; By iteration,

$$K = 1.33$$

and the maximum overvoltage of the clamp-storage capacitor C_C is

$$V_{CC,MAX} = 400 \text{ V}$$

Finally,

$$t_{ON,So} = 4.4 \ \mu\text{s}$$

3.8 Component ratings

In this section, the ratings of all the converter components are provided. The worst operating point for the two converters is chosen. According to the analysis previously presented, the rated power and the maximum input voltage are considered as worst operating point.

3.8.1 Component ratings of the single-phase full-bridge PWM converter topology with low loss snubber network.

The voltage and current ratings of the various system components are ass follows:

$V_{INMAX} = 300$ V, $V_{CC,MAX} = 340$ V, $I_O = 21.8$ A, $P_{OUT} = 5$ kW, $V_{OUT} = 240$ V.

Snubber inductor L_S:	RMS current:	$I_{Ls,RMS} = 21.3$ A
	Peak current:	$I_{Ls,MAX} = 33.5$ A
	Peak voltage:	$V_{Ls,MAX} = 300$ V
	Total kVA:	$kVA_{Ls} = 10{,}050$ VA
Clamp capacitor C_C:	Peak current:	$I_{CC,MAX} = 21.8$ A
	Peak voltage:	$V_{CC,MAX} = 340$ V
	Total kVA:	$kVA_{CC} = 7{,}412$ VA
Snubber capacitors C_1,C_2:	Peak current:	$I_{Cs,MAX} = 21.8$ A
	Peak voltage:	$V_{Cs,MAX} = 340$ V

	Total kVA:	kVA_{Cs} = 7,412 VA
Snubber resistor R_S:	Power dissipation:	138 W
Snubber diodes D_1-D_4 :	RMS current:	$I_{Ds,RMS}$ = 3.8 A
	Average current:	$I_{Ds,AVG}$ = 1.7 A
	Peak current:	$I_{Ds,MAX}$ = 21.8 A
	Reverse peak volt.:	$V_{Ds,MAX}$ = 340 V
Converter switches:	RMS current:	$I_{SW,RMS}$ = 13.5 A
	Average current:	$I_{SW,AVG}$ = 8.5 A
	Peak voltage:	$V_{SW,MAX}$ = 340 V
Transformer:	RMS current:	$I_{PRI,RMS}$ = 18.7 A
	Peak current:	$I_{PRI,MAX}$ = 21.8 A
	RMS voltage:	$V_{PRI,MAX}$ = 266 V
	Peak voltage:	$V_{PRI,MAX}$ = 340 V
	Total kVA:	kVA = 4,975 VA
Rectifier diodes:	RMS current:	$I_{D,RMS}$ = 13.5 A
	Average current:	$I_{D,AVG}$ = 10 A
	Peak current:	$I_{D,MAX}$ = 21.8 A
	Reverse peak volt.:	$V_{D,MAX}$ = 340 V

3.8.2 Component ratings of the single-phase full-bridge PWM converter topology with lossless snubber network.

The voltage and current ratings of the various system components are ass follows:

V_{INMAX} = 300 V, $V_{CC,MAX}$ = 400 V, I_O = 21.8 A, P_{OUT} = 5 kW, V_{OUT} = 240 V.

Snubber inductor L_S:	RMS current:	$I_{Ls,RMS}$ = 21.4 A

	Peak current:	$I_{Ls,MAX} = 33.5$
	Peak voltage:	$V_{Ls,MAX} = 300$ V
	Total kVA:	$kVA_{Ls} = 10{,}050$ VA
Clamp capacitor C_C:	Peak current:	$I_{CC,MAX} = 24.6$ A
	Peak voltage:	$V_{CC,MAX} = 400$ V
	Total kVA:	$kVA_{CC} = 9{,}840$ VA
Snubber capacitors C_1,C_2:	Peak current:	$I_{Cs,MAX} = 21.8$ A
	Peak voltage:	$V_{Cs,MAX} = 400$ V
	Total kVA:	$kVA_{Cs} = 8{,}720$ V
Snubber diodes D_1-D_4 :	RMS current:	$I_{Ds,RMS} = 3.8$ A
	Average current:	$I_{Ds,AVG} = 1.7$ A
	Peak current:	$I_{Ds,MAX} = 21.8$ A
	Reverse peak volt.:	$V_{Ds,MAX} = 400$ V
Auxiliary switch S_O	RMS current:	$I_{AUX,RMS} = 6$ A
	Average current:	$I_{AUX,AVG} = 1$ A
	Peak voltage:	$I_{AUX,MAX} = 400$ V
Converter switches:	RMS current:	$I_{SW,RMS} = 13.6$ A
	Average current:	$I_{SW,AVG} = 8.5$ A
	Peak voltage:	$V_{SW,MAX} = 400$ V
Transformer:	RMS current:	$I_{PRI,RMS} = 19$ A
	Peak current:	$I_{PRI,MAX} = 22$ A
	RMS voltage:	$V_{PRI,RMS} = 268$ V
	Peak voltage:	$V_{PRI,MAX} = 400$ V
	Total kVA:	kVA = 5,092 VA

Rectifier diodes:	RMS current:	$I_{D,RMS}$ = 14 A
	Average current:	$I_{D,AVG}$ = 10.5 A
	Peak current:	$I_{D,MAX}$ = 21.8 A
	Reverse peak volt.:	$V_{D,MAX}$ = 400 V

3.9 Simulated results

The performance of the two dc-dc converter topologies shown in Figs. 3-1 and 3-2 was simulated using a standard electronic circuit simulation package [67]. Both power circuit configurations were simulated under steady-state operating conditions. Typical steady-state simulated results for the converter employing the low loss snubber network (Fig. 3-1) are given in Fig. 3-7. Specifically, Fig. 3-7(a) shows the dc bus current and Figs. 3-7(b) and 3-7(c) display the voltage across the snubber capacitors C_1, C_2 respectively. Fig. 3-7(d) shows the converter switch voltage. It is clearly illustrated that the slope of the switch voltage during turn-off is controllable by the value of the snubber capacitors and the load current. Therefore, turn-off switching losses are minimized. The current through the switch is depicted in Fig. 3-7(e). It is also clearly illustrated that the slope of the current during turn-on is controlled by the value of the snubber inductor L_S. Therefore, turn-on switching losses are also minimized. The voltage across the rectifier diodes is shown in Fig. 3-7(f).

Similarly, Fig. 3-8 presents typical steady-state waveforms for the converter with the lossless snubber network (Fig. 3-2). In this case, the capacitor C_C is discharged to the dc bus during the time that the load current freeewheels at the output circuit. In particular, Fig. 3-8(a) presents the dc bus current. Whenever the auxiliary switch is on, this current becomes negative (if it is zero) or decreases towards zero (if greater than zero). Fig. 3-8(b) and 3-8(c) display the voltage across the snubber capacitors C_1 and C_2 respectively. It is

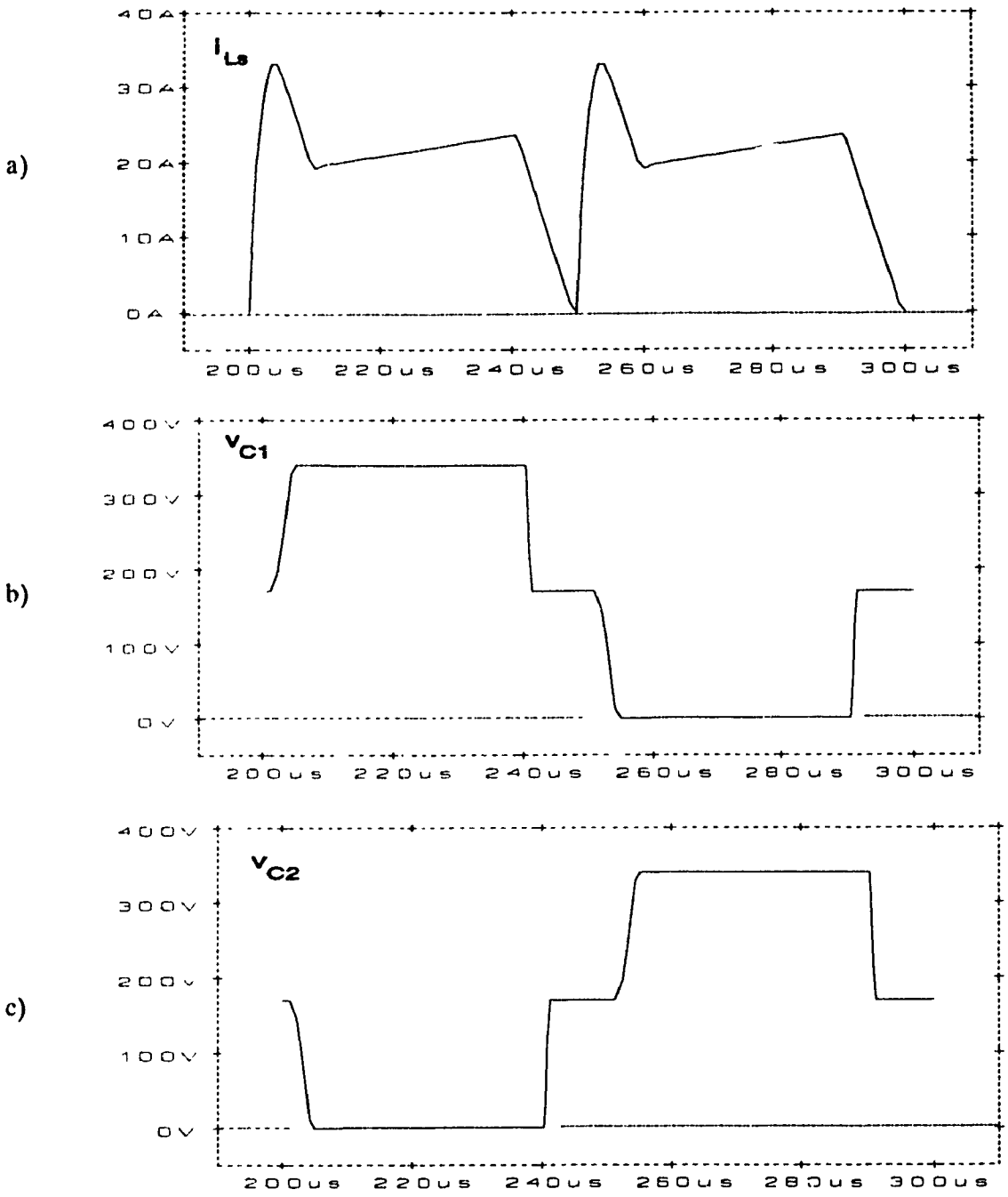


Figure 3-7: Steady-state waveforms - Low loss snubber network.
P_{OUT} = 5 kW, V_{IN} = 300 V, K = 1.133, L_S = 15 µH,
C_S = 0.1 µF, d = 0.8, f_{SW} = 10 kHz.
a) Inductor L_S current.
b) Capacitor C_1 voltage.
c) Capacitor C_2 voltage.

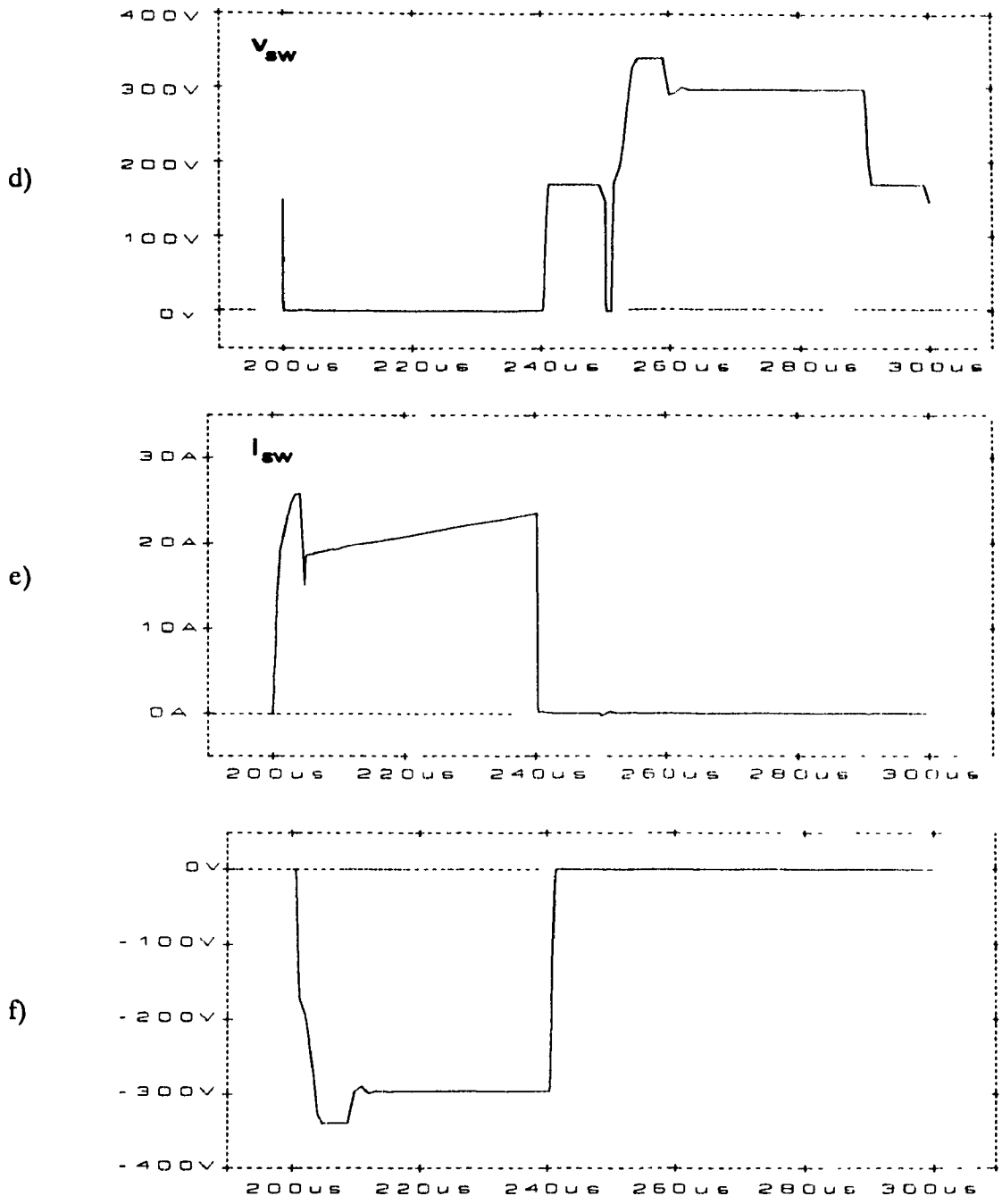


Figure 3-7: Steady-state waveforms - Low loss snubber network.
P_{OUT} = 5 kW, V_{IN} = 300 V, K = 1.133, L_S = 15 µH,
C_S = 0.1 µF, d = 0.8, f_{SW} = 10 kHz.
d) Switch voltage.
e) Switch current.
f) Rectifier diode voltage.

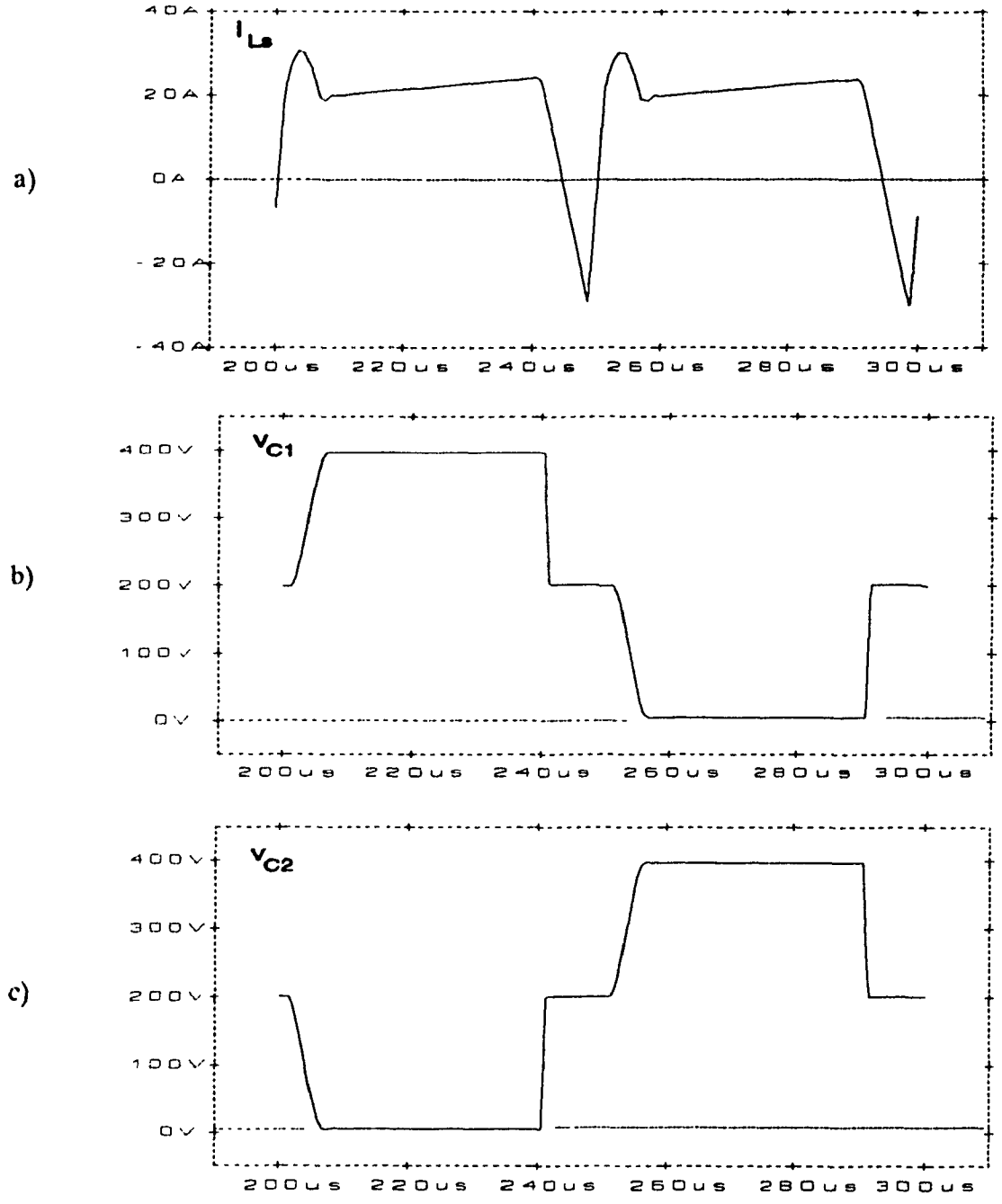


Figure 3-8: Steady-state waveforms - Lossless snubber network.
P_{OUT} = 5 kW, V_{IN} = 300 V, K = 1.33, L_S = 15 µH,
C_S = 0.1 µF, d = 0.8, f_{SW} = 10 kHz, $t_{ON,So}$ = 4.4 µs.
a) Inductor L_S current.
b) Capacitor C_1 voltage.
c) Capacitor C_2 voltage.

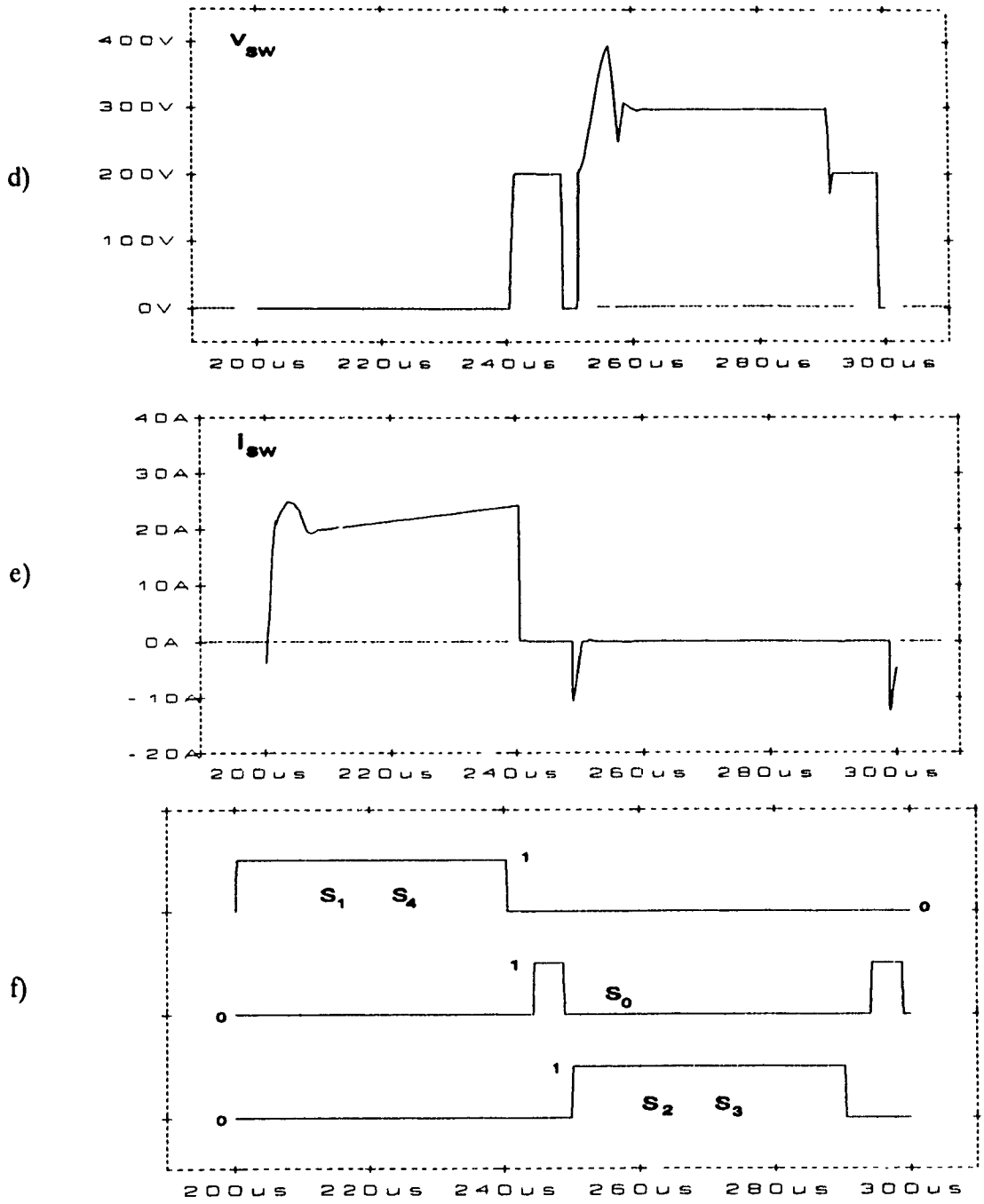


Figure 3-8: Steady-state waveforms - Lossless snubber network.
P_{OUT} = 5 kW, V_{IN} = 300 V, K = 1.33, L_S = 15 µH,
C_S = 0.1 µF, d = 0.8, f_{SW} = 10 kHz, $t_{ON,So}$ = 4.4 µs.
d) Converter switch voltage.
e) Converter switch current.
f) Converter switch gating signals.

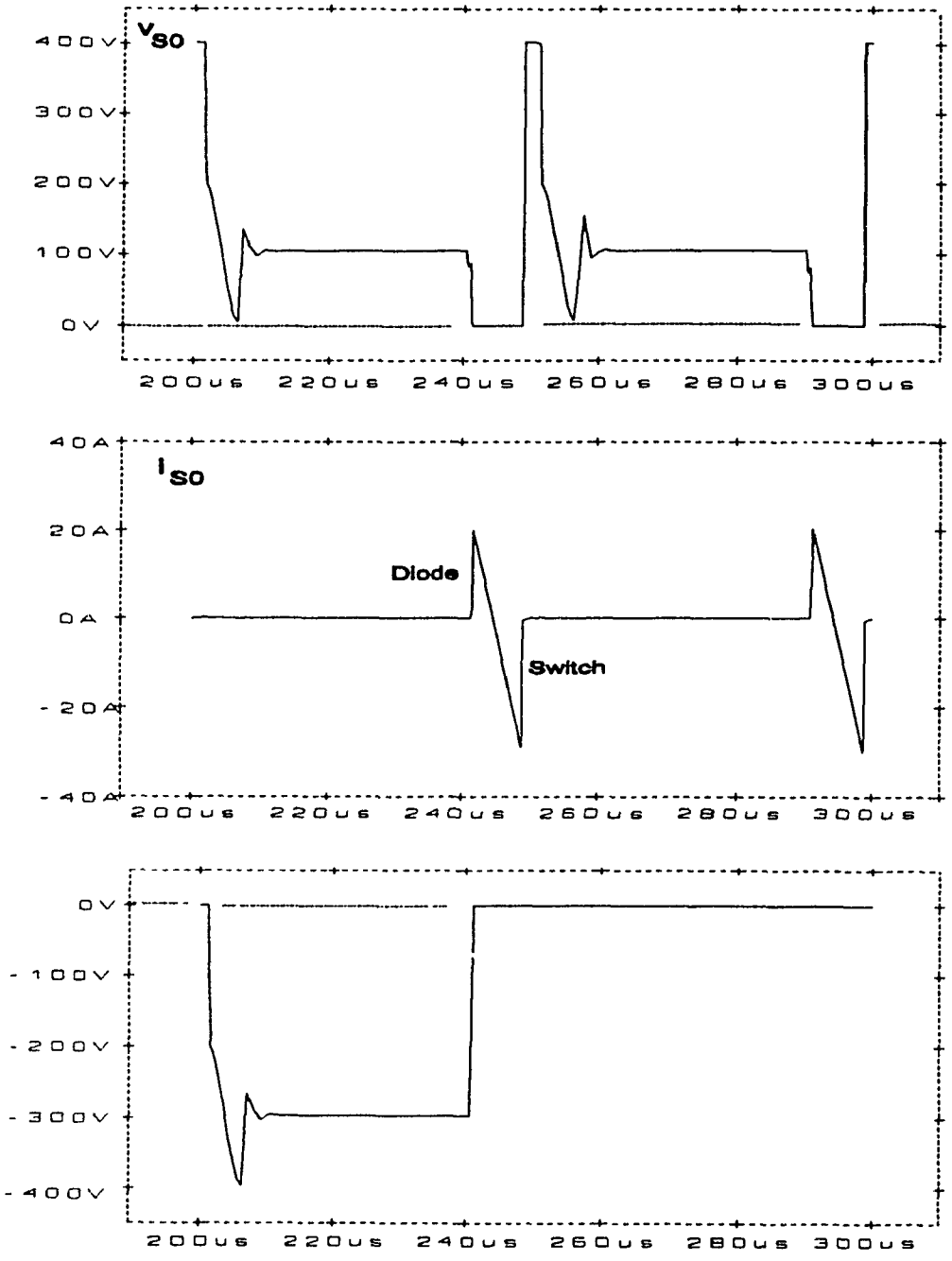


Figure 3-8: Steady-state waveforms - Lossless snubber network.
P_{OUT} = 5 kW, V_{IN} = 300 V, K = 1.33, L_S = 15 µH,
C_S = 0.1 µF, d = 0.8, f_{SW} = 10 kHz, $t_{ON,So}$ = 4.4 µs.
g) Auxiliary switch voltage.
h) Auxiliary switch current.
i) Rectifier diode voltage.

proved that the energy recovery subcircuit does not affect the waveforms across the two snubber capacitors C_1 and C_2 . That means that the modified snubber network with the auxiliary switch provides similar reduction in switching losses and stresses. The converter switch voltage and current are shown in Figs. 3-8(d) and (e) respectively. The negative part of the current as well as the zero volts interval of the switch voltage are due to the auxiliary switch S_O turn-off and the energy stored in the dc bus snubber inductor L_S when the auxiliary switch is conducting. Fig. 3-8(f) demonstrates the gating signals of all converter switches. The auxiliary switch S_O voltage and current are plotted in Figs. 3-8(g) and (h). The voltage across the rectifier diodes is depicted in Fig. 3-8(i).

3.10 Experimental results

To establish the feasibility of the two full-bridge high-power PWM converter topologies with the snubber networks under consideration and to verify the theoretical results, laboratory prototypes of 5-kW operating at 10-kHz switching frequency were built and tested. Experimental results are shown in Figs. 3-9 through 3-12. The experimental results and the simulated waveforms are in close agreement. In particular, Fig. 3-9(a) shows the dc bus current. The converter switch voltage is displayed in Fig. 3-9(b). It indicates that the voltage across the switch devices is controlled through the value of the snubber capacitors. Therefore, switching losses of semiconductor devices are minimized. The turn-on and the turn-off switching waveforms shown in Fig. 3-10(a) and (b) respectively, prove that switching losses are minimized through the effective use of the modified turn-on/turn-off snubber network being analyzed in this chapter. The experimental converter waveforms, taken from the circuit when the proposed lossless snubber is used, are shown in Figs. 3-11 and 3-12. Fig. 3-11(a) presents the dc bus current, and the converter

switch voltage is shown in Fig. 3-11(b). Fig. 3-12 shows the turn-on and the turn-off switching waveforms. The same waveforms are obtained as far as switching elements are concerned. However, due to the further minimization of the switching losses, the overall circuit efficiency is improved, since, at least, theoretically all the energy associated with the snubber elements is recovered.

3.11 Conclusions

A complete analysis and design procedure of two single-phase full-bridge high-power PWM dc-dc converter topologies using low loss and lossless snubber networks has been proposed in this chapter. Switching behaviour of the switch devices during turn-off is dictated by the charging rate of the snubber capacitors. Zero current turn-on and zero voltage turn-off switching conditions are obtained through the use of a simplified snubber network. The overall circuit efficiency is improved with the use of the simple active energy recovery subcircuit since, at least theoretically, all the energy associated with the snubber elements is completely recovered. However, this improvement in the converter efficiency is achieved at the expense of an additional auxiliary switch and higher VA ratings for snubber elements. Theoretical results have been verified for both power configurations on 5-kW laboratory prototypes operating at 10-kHz switching frequency.

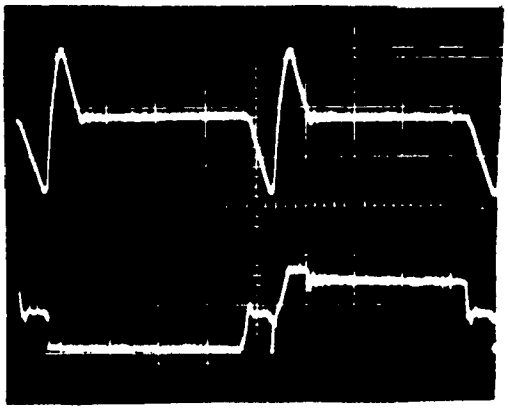


Figure 3-9: Experimental converter waveforms - Low loss snubber network.

L_S=15 µH C_S=0.1 µF C_C=10 µF K=1.13 P_{OUT}=5 kW f_{SW}=10 kHz.

a) Inductor L_S current (15 A/div,10 µs/div)

b) Switch voltage (200 V/div, 10 µs/div).

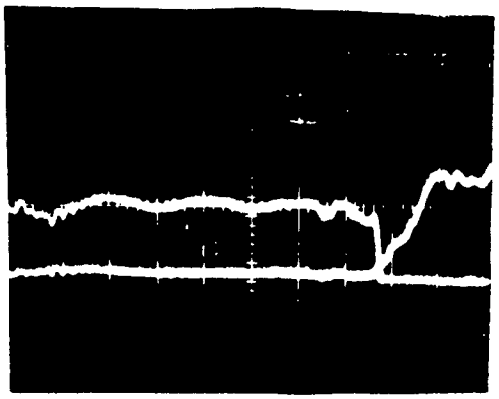


Figure 3-10: Switch voltage and current during switching interval.

Low loss snubber network.

L_S=15 µH C_S=0.1 µF C_C=10 µF K=1.13 P_{OUT}=5 kW f_{SW}=10 kHz.

a) Turn-on (200 V/div, 15 A/div, 100 ns/div).

b)

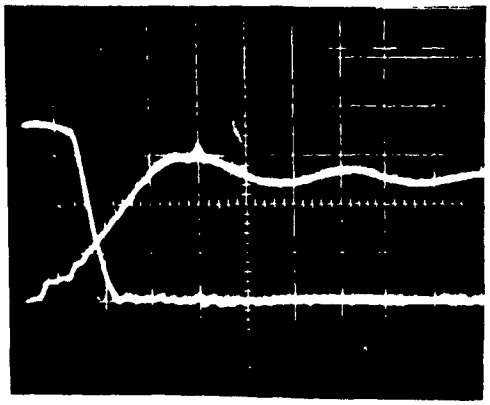


Figure 3-10: Switch voltage and current during switching interval.

Low loss snubber network.

L_S=15 μH C_S=0.1 μF C_C=10 μF K=1.13 P_{OUT}=5 kW f_{SW}=10 kHz.

b) Turn-off (50 V/div, 10 A/div, 100 ns/div).

a)

b)

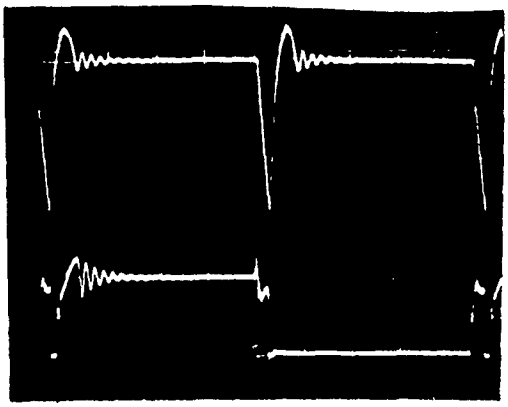


Figure 3-11: Experimental converter waveforms - Lossless snubber network.

L_S=15 μH C_S=0.1 μF $t_{ON,So}$=4.5 μs K=1.33 P_{OUT}=5 kW f_{SW}=10 kHz.

a) Inductor L_S current (20 A/div, 10 μs/div).

b) Switch voltage (200 V/div, 10 μs/div).

a)

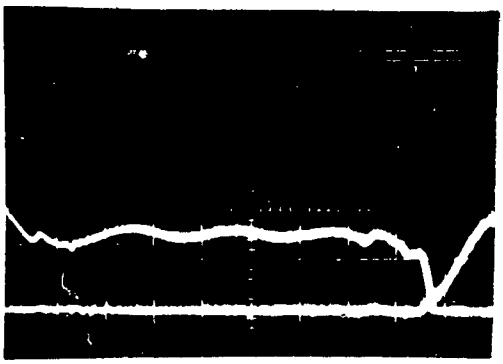


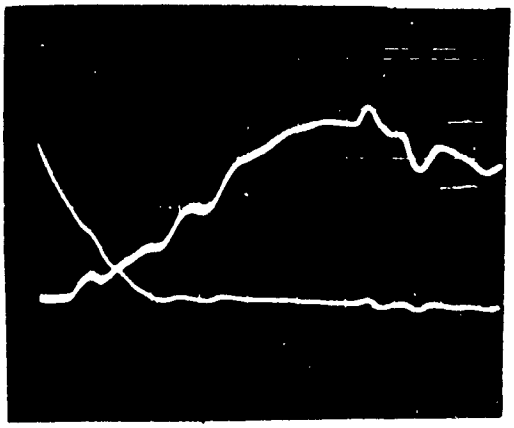
Figure 3-12: Switch voltage and current during switching interval.

Lossless snubber network.

L_S=15 μH C_S=0.1 μF $t_{ON,So}$=4.5 μs K=1.33 P_{OUT}=5 kW f_{SW}=10 kHz.

a) Turn-on (50 V/div, 10 A/div, 100 ns/div).

b)



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b) Turn-off (50 V/div, 10 A/div, 100 ns/div).

CHAPTER 4

A ZERO VOLTAGE SWITCHING MEDIUM-POWER HIGH-FREQUENCY SINGLE-PHASE FULL-BRIDGE PWM CONVERTER TOPOLOGY

4.1 Introduction

To overcome some problems associated with the single-phase full-bridge converter using phase-shifted PWM technique, a converter topology employing an active dc bus snubber subcircuit and conventional PWM technique is proposed in this chapter (Fig. 4-1).

4.2 A zero voltage switching PWM converter topology

The topology proposed here uses an active dc bus subcircuit to reduce converter switching losses and resulting stresses (Fig. 4-1) [64]. This active energy recovery subcircuit makes use of switch parasitic (or discrete) capacitors, but in a different way compared with the single-phase full-bridge converters employing the phase-shifted PWM technique. The full-bridge operates in the typical PWM fashion thus minimizing conduction losses and facilitating the use of the current mode control of operation.

The circuit realization of the proposed *soft switching* topology is shown in Fig. 4-1. The converter power circuit includes the dc supply voltage V_{IN}, the four main switches (S_1, S_2, S_3, S_4), the dc bus snubber inductor L_S, the storage-clamp capacitor C_C, the auxiliary low power switch S_O, the switch antiparallel diodes, the combined parasitic and/or small discrete switch snubber capacitors (C_1, C_2, C_3, C_4), the high frequency transformer, the output diode rectifier, the filter (L,C) and the load shown as a resistor R.

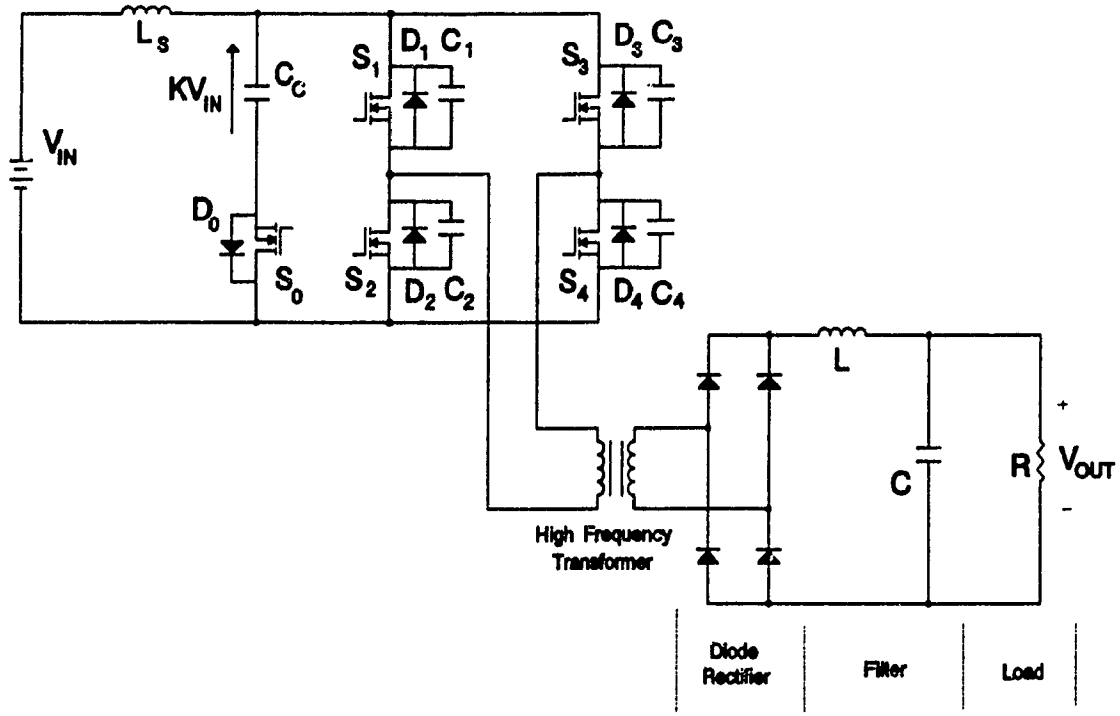


Figure 4-1: The proposed single-phase full-bridge medium-power high-frequency zero-voltage-switching (ZVS) PWM converter topology.

Because of the use of a small dc link inductor L_S , dc bus *shoot-throughs* and subsequent bridge destruction can be avoided. The discharge of the snubber capacitors (C_1-C_4) is not as directly linked to the load current level as with the phase-shifted PWM technique, therefore lossless operation can be maintained over a wider load range. The only disadvantage with the proposed method is that it requires one additional auxiliary, but low power, switch. The next section describes the operation of the topology under consideration.

4.3 Principles of operation

The principles of operation of the proposed topology (Fig. 4-1) are as follows.

The energy stored in the snubber inductor L_S is distributed between the switch capacitors C_1 , C_2 , C_3 , C_4 and the storage capacitor C_C during main switch S_1 - S_4 or S_2 - S_3 turn-off. Immediately before the main switches turn-on, the auxiliary switch S_O is turned on to discharge C_C by sending energy back to the source through L_S . The negative current flowing through the snubber inductor forces the antiparallel diodes of the main switches to conduct after the auxiliary switch S_O is turned off and prior to the turning on of the main switches. The parasitic (or small discrete) capacitors C_1 , C_2 , C_3 , C_4 are discharged and the associated energy is returned back to the source. This energy is completely recovered through S_O , in a nondissipative way. The main switches are turned on with zero voltage. Zero voltage turn-off switching conditions are also obtained due to the parasitic (or discrete) switch capacitors. The auxiliary switch S_O is turned on with zero voltage since the antiparallel diode always conduct first, when energy is transferred from the dc bus snubber inductor L_S to the storage capacitor C_C . Since turn-on and turn-off switching losses are minimized, the overall converter efficiency is increased at least theoretically. The analysis presented below includes the identification of the topological modes (TM's) during a switching cycle and the respective voltage-current expressions.

4.4 Modes of operation - Steady-state analysis

In this section, the description of the different topological modes (TM's) and the exact analytical expressions describing the converter currents and voltages during a switching cycle and under rated steady-state conditions are obtained.

The analysis is based on the following assumptions:

- The switch model includes a parasitic or discrete capacitor in parallel with the transistor. This capacitor is taken as voltage invariable.

- The auxiliary switch parasitic capacitor is neglected.
- The capacitors and the inductors are lossless.
- The value of the storage-clamp capacitor C_C is large compared with the parasitic or discrete switch capacitor, resulting in an essential constant voltage source.
- The high frequency transformer has very low leakage inductors. Moreover, for the analysis presented below, the transformer leakage inductors are neglected.
- The transformer magnetizing current is also neglected.
- The load current I_O is assumed ripple-free.
- The supply voltage V_{IN} is also assumed ripple free.

Initial conditions

It is assumed that the storage-clamp capacitor C_C has the following voltage:

$$V_{CC} = K V_{IN} \tag{4.1}$$

where

$$K \rangle 1 \tag{4.2}$$

The current flowing through the snubber inductor L_S at $t=0$ is

$$i_{Ls} \mid_{t=0} = 0 \tag{4.3}$$

and

$$C_1 = C_2 = C_3 = C_4 = C_S \tag{4.4}$$

A. Turn-on process

Mode 1, Interval $0 < t < t_1$.

The switches S_1 and S_4 are turned on at $t=0$. The antiparallel diodes of the switches

S_1 , S_2 , S_3 , S_4 are conducting due to the negative current ($t<0$) that is flowing through the snubber inductor L_S after the auxiliary switch S_O is turned off (Fig. 4-4(a)). The switch parasitic (or discrete) capacitors C_1 , C_2 , C_3 , C_4 have been already discharged (prior to the antiparallel diode conduction) and their stored energy has been returned to the dc bus. During this mode, the auxiliary switch S_O voltage is equal to KV_{IN} , the voltage across the capacitor C_C is constant (KV_{IN}) and the load current continues to freewheel in the output rectifier circuit due to the presence of the dc bus snubber inductor L_S . The equivalent circuit for this mode is shown in Fig. 4-2(b). It is an inductive load circuit and the current through the snubber inductor L_S (Fig. 4-4(a)) is given by the following equation

$$i_{Ls}(t) = \frac{V_{IN}}{L_S} t + i_{Ls}|_{t=0} \tag{4.5}$$

Since

$$i_{Ls}|_{t=t_1} = I_O \tag{4.6}$$

the duration of this mode, using the initial condition for the inductor L_S current (4.3), is

$$t_1 = \frac{I_O L_S}{V_{IN}} \tag{4.7}$$

Mode 2, Interval $t_1 < t < t_2$.

The snubber inductor L_S oscillates with the parasitic or discrete switch capacitors. Since two switches are on and the other two are blocking the input voltage, two capacitors only (C_2 , C_3 in this case) make up the equivalent resonant capacitor. The voltage across the storage-clamp capacitor C_C is constant (KV_{IN}). The equivalent circuit is shown in Fig. 4-2(c). The equation for the current through the snubber inductor L_S is as follows:

$$i_{Ls}(t) = I_O + \sqrt{\frac{2 C_S}{L_S}} V_{IN} \sin[\omega_r (t - t_1)] \tag{4.8}$$

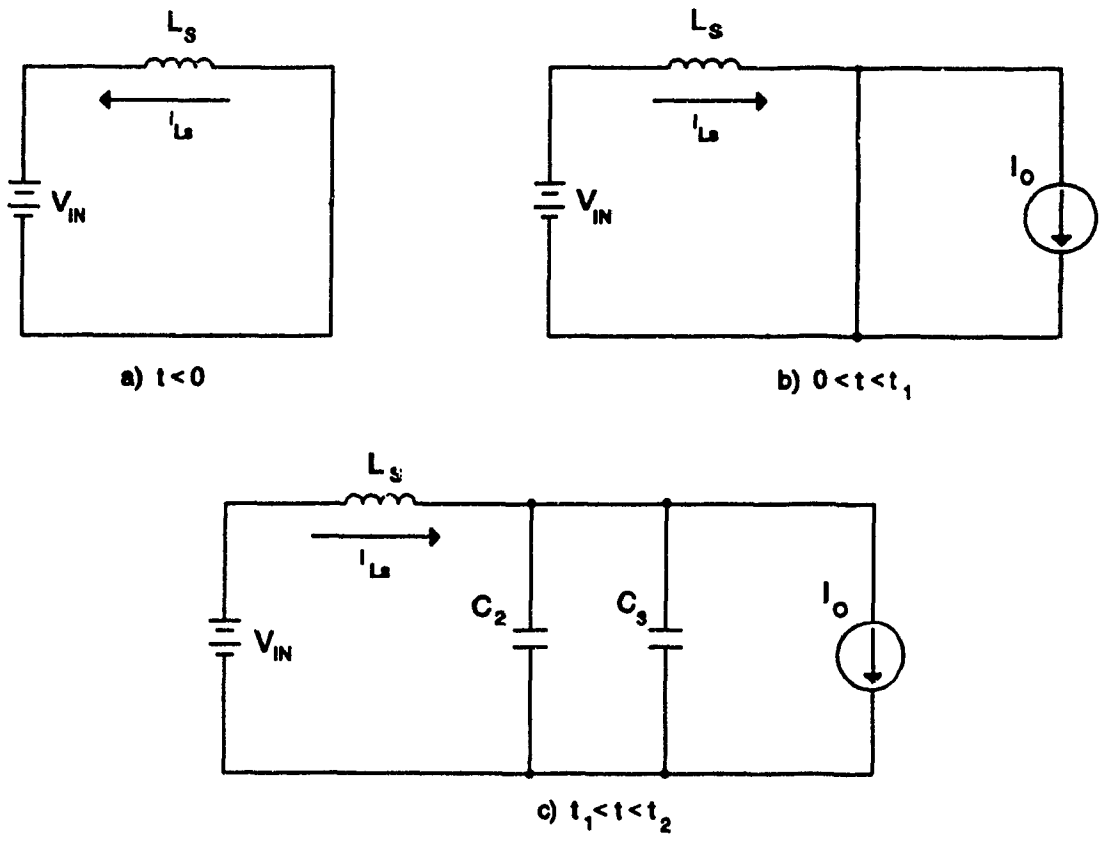


Figure 4-2: Converter topological modes (TM's) during switching cycle turn-on.

a) Equivalent converter circuit at $t < 0$.

b) Mode 1: $0 < t < t_1$.

c) Mode 2: $t_1 < t < t_2$.

where

$$\omega_r = \sqrt{\frac{1}{2\ L_S\ C_S}} \tag{4.9}$$

The maximum value of the snubber inductor L_S current (Fig. 4-4(a)) is

$$I_{max} = I_O + \sqrt{\frac{2\ C_S}{L_S}}\ V_{IN} \tag{4.10}$$

Mode 3, Interval $t_2 < t < t_3$.

At $t=t_2$, the turn-on process has been completed and the voltage across the auxiliary switch S_O is $(K\text{-}1)V_{IN}$ (Fig. 4-4(c)). The current flowing through the snubber inductor L_S is constant and equal to the load current I_O . The voltage across the storage-clamp capacitor C_C is also constant (KV_{IN}). Finally, since the voltage across the switches S_2 and S_3 is equal to the supply voltage V_{IN} , the capacitors C_2 and C_3 store some energy given by the following equation

$$W_{C2} = W_{C3} = \frac{1}{2} C_S V_{IN}^2 \tag{4.11}$$

The moment that this mode changes is dictated by the duty cycle, so that

$$t_3 = \frac{d}{2 f_{SW}} \tag{4.12}$$

where

f_{SW} is the converter switching frequency;

d is the converter duty cycle defined as the total on-time of the two pairs of the switches over the switching period.

B. Turn-off process

Mode 4, Interval $t_3 < t < t_4$.

At $t=t_3$, the switches S_1 and S_4 are turned off and the switch current begins to decrease at a rate limited only by the commutation characteristics of the switches. The rise rate of the switch voltage is dictated by the value of the parasitic (or discrete) capacitors and the level of the load current. However, because of the snubber inductor L_S , the dc bus current cannot change instantaneously. Instead, the inductor energy is distributed between

the switch capacitors and the storage-clamp capacitor C_C since current is also flowing through the antiparallel diode of the auxiliary switch S_O . The capacitor voltage KV_{IN} is applied across the main switches. The equivalent circuit is shown in Fig. 4-3(a).

Initially;

$$V_{C2}|_{t=t_3} = V_{C3}|_{t=t_3} = V_{IN} \tag{4.13}$$

$$V_{C1}|_{t=t_3} = V_{C4}|_{t=t_3} = 0 \tag{4.14}$$

and finally

$$V_{C1}|_{t=t_4} = V_{C2}|_{t=t_4} = V_{C3}|_{t=t_4} = V_{C4}|_{t=t_4} = \frac{KV_{IN}}{2} \tag{4.15}$$

The stored energy in the switch parasitic (or discrete) capacitors is given by the following equation

$$W_{C1} = W_{C2} = W_{C3} = W_{C4} = \frac{1}{2} C_s \left(\frac{KV_{IN}}{2}\right)^2 \tag{4.16}$$

The duration of this mode is dictated by the switch parasitic (or discrete) capacitor C_S and the level of the load current I_O .

Mode 5, Interval $t_4 < t < t_5$.

During this mode, the remaining inductor energy is transferred in the storage capacitor C_C . Due to the large value of the storage-clamp capacitor C_C , which operates as a voltage source, the slope of the inductor L_S current is dictated by the voltage difference between the storage capacitor C_C voltage KV_{IN} and the supply voltage V_{IN} , and the value of the snubber inductor L_S (Fig. 4-4(a)). The respective equivalent converter circuit is shown

in Fig. 4-3(b).

$$i_{Ls}(t) = -\frac{(K-1)\,V_{IN}}{L_S}(t - t_4) + I_O \tag{4.17}$$

Since

$$i_{Ls}|_{t=t_5} = 0 \tag{4.18}$$

the duration of this mode is approximately

$$t_5 - t_4 \approx \frac{L_S\,I_O}{(K-1)V_{IN}} \tag{4.19}$$

The voltage across the storage capacitor C_C increases due to the extra energy transferred from the snubber inductor L_S and it can be easily calculated as follows

$$\Delta V_{CC} \approx \frac{I_O^2\,L_S}{2\,C_C\,(K-1)\,V_{IN}} \tag{4.20}$$

However, the value of the storage capacitor C_C is large enough, so that the following approximation can be considered as valid:

$$V_{CC}\,|_{t=t_5} \approx K V_{IN} \tag{4.21}$$

Mode 6, Interval $t_5 < t < t_6$.

At $t=t_5$, the antiparallel diode of the auxiliary switch S_O stops conducting since the current flowing through the snubber inductor L_S has reached zero. By this time, the auxiliary switch S_O is turned on, thus allowing the storage-clamp capacitor C_C current ($I_{CC} = I_{Ls}$) to reverse polarity (Fig. 4-4(a)). Since the antiparallel diode of the auxiliary switch S_O is conducting prior to the turn-on of the switch, respective turn-on losses are minimal (Fig. 4-4(c)). Therefore during auxiliary switch S_O turn-on the voltage across it is

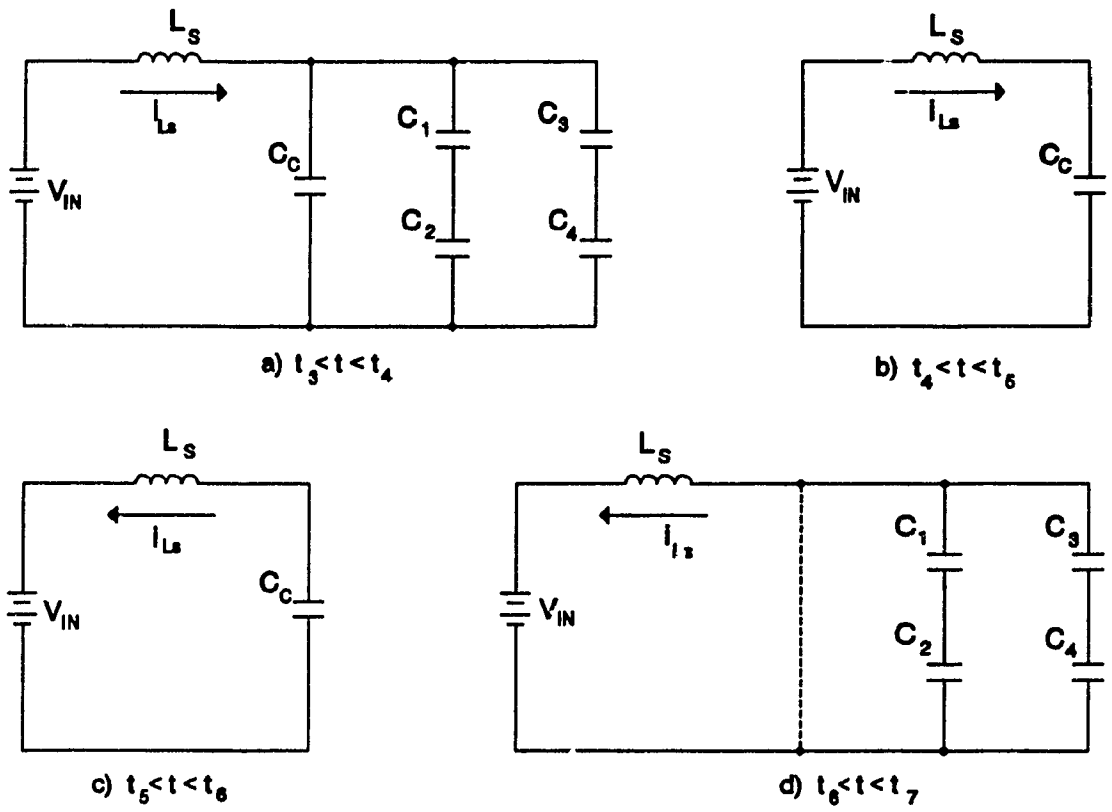


Figure 4-3: Converter topological modes (TM's) during switching cycle turn-off.

a) Mode 4: $t_3 < t < t_4$.

b) Mode 5: $t_4 < t < t_5$.

c) Mode 6: $t_5 < t < t_6$.

d) Mode 7: $t_6 < t < t_7$.

not zero for lower current levels but it is low, $(K\text{-}1)V_{IN}$. Since the auxiliary switch commutates the voltage difference $(K\text{-}1)V_{IN}$, which is low, the switching losses will be small. The voltage across the storage capacitor C_C begins to decrease since the current flowing through it is negative and the extra stored energy is returned to the dc bus. The

equivalent circuit is shown in Fig. 4-4(c). First, using the approximation of the previous mode (4.21), the current through the snubber inductor L_S is

$$i_{Ls}(t) = - \frac{(K-1)V_{IN}}{L_S} (t-t_5) \tag{4.22}$$

The duration of this mode can be estimated so that under steady state conditions the energy that enters C_C during main switch turn-off is equal to the energy that leaves C_C during this mode. Therefore, the assumed overvoltage across the storage capacitor C_C (KV_{IN}) is maintained under rated conditions since the average energy flow through C_C is kept zero. The value of the current flowing through the auxiliary switch S_O at $t=t_6$ is

$$i_{Ls}|_{t=t_6} = - \frac{(K-1)V_{IN}}{L_S} (t_6-t_5) \tag{4.23}$$

Since the voltage across the storage capacitor C_C decreases for the steady state conditions, the following equation can be applied;

$$\Delta V_{CC} = \frac{(K-1)V_{IN}}{2\,C_C L_S} (t_6-t_5)^2 \tag{4.24}$$

therefore the duration of this mode and at the same time the width of the gating signal applied to the auxiliary switch S_O can be easily calculated as follows

$$t_6-t_5 = \frac{I_O\, L_S}{(K-1)V_{IN}} \tag{4.25}$$

From eqn's (4.21), (4.23) and (4.25), the value of the current flowing through the auxiliary switch S_O at the moment that it is turned off can be calculated (Fig. 4-4(a)) and is approximately

$$i_{Ls}|_{t=t_6} \approx I_O \tag{4.26}$$

This is important from the design point of view since the auxiliary switch S_O has to be rated for the same voltage (KV_{IN}) and current (I_O) like the main converter switches.

Mode 7, Interval $t_6 < t < t_7$.

At $t=t_6$, the auxiliary switch S_O is turned off. Because of the value of the negative current flowing through the snubber inductor L_S, during this mode, first the switch parasitic (or discrete) capacitors C_1, C_2, C_3, C_4 are discharged and then all the antiparallel diodes of the main switches S_1, S_2, S_3, S_4 start conducting, providing a zero volts interval across the dc bus. The energy stored in the switch parasitic (or small discrete) capacitors is returned to the dc bus. The auxiliary switch S_O now blocks the voltage across the storage-clamp capacitor C_C (Fig. 4-4(c)) and the current flowing through the snubber inductor L_S decreases towards zero (Fig. 4-4(a)). The equivalent circuit for this interval is shown in Fig. 4-3(d). The dashed line indicates the conduction of the antiparallel diodes prior to main switches turn-on and after the discharge of the switch parasitic (or small discrete) capacitors. The snubber inductor L_S current is as follows

$$i_{Ls}(t) = - I_O + \frac{V_{IN}}{L_S} (t-t_6) \tag{4.27}$$

The current at $t=t_7$ is

$$i_{Ls}|_{t=t_7} = 0 \tag{4.28}$$

so that the duration of this mode using eqn's (4.26), (4.27) and (4.28) is

$$t_7-t_6 = \frac{I_O L_S}{V_{IN}} \tag{4.29}$$

Finally, at time $t=t_7$ the other pair of the switches (S_2, S_3) is turned on with zero

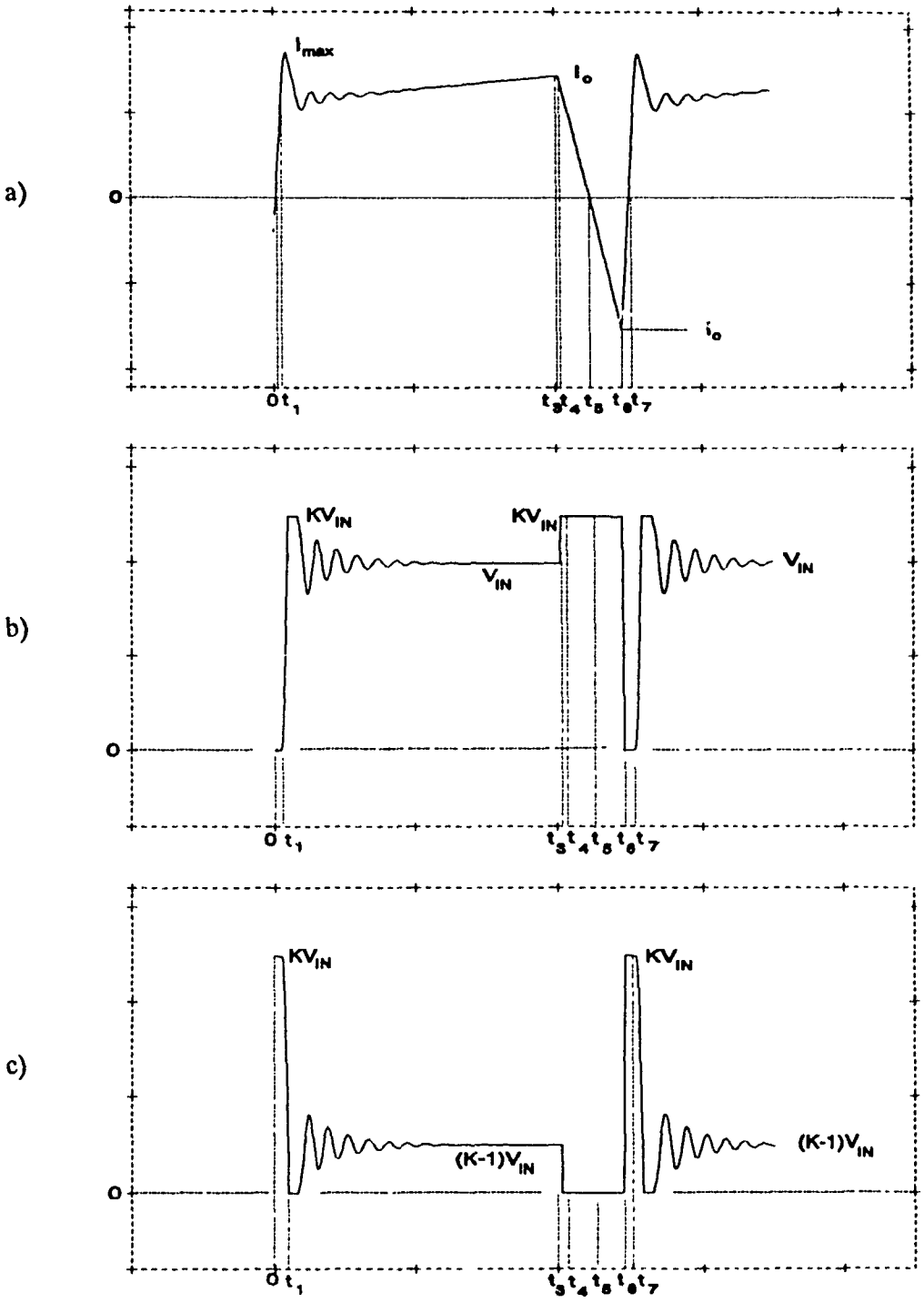


Figure 4-4: Steady-state voltage and current waveforms.
a) Dc bus current.
b) Dc bus voltage.
c) Auxiliary switch S_O voltage.

voltage and the same procedure is repeated, since the topology is symmetrical due to the conventional PWM technique employed.

4.5 Discussion - Design guidelines

The converter voltage-current expressions during a switching cycle presented in the preceding section are used next to design the converter energy recovery subsircuit (dc bus active snubber) (Fig. 4-1). The output power P_{OUT} , the output voltage V_{OUT} and the switching frequency f_{SW} are the desired specifications of the converter. Since the proposed topology has an unregulated dc bus as an input power supply, variations in the system frequency and especially in the input ac line-to-line voltage in the front-end rectifier stage have to be taken into account for a worst case components size design.

Equations (4.17) and (4.22) show that the slope of the current flowing through the snubber inductor L_S during turn-off depends upon the voltage difference between the storage capacitor C_C voltage (KV_{IN}) and the supply voltage V_{IN} . However, the capacitor C_C voltage (KV_{IN}) is reflected across the main switches (S_1 , S_2 , S_3 , S_4) and the auxiliary switch S_O as well. Therefore, the factor K has to be chosen slightly higher than unity thus avoiding semiconductor stresses due to overvoltages.

Auxiliary switch frequency is twice the inverter switching frequency. Therefore, limitations to the inverter switching frequencies attainable using the proposed topology are introduced by the dc bus active snubber subcircuit.

The output voltage V_{OUT} (assuming an 1:1 output transformer turns ratio and neglecting converter losses) for the case of the minimum duty cycle is as follows;

$$V_{OUT} = d_{MIN} V_{INMAX} \tag{4.30}$$

where

V_{INMAX} is the maximum supply voltage

d_{MIN} is the minimum duty cycle.

The output current is given by the following equation

$$I_O = \frac{P_{OUT}}{V_{OUT}} \tag{4.31}$$

The worst case for the snubber inductor L_S current (dc bus current) taking into account the converter efficiency is

$$I_{OW} = \frac{I_O}{\eta} \tag{4.32}$$

where

η is the efficiency of the converter.

The worst case storage-clamp capacitor C_C voltage as a function of the snubber inductor L_S value is investigated next as follows.

From the converter analysis presented in the preceding section, an overvoltage KV_{IN} ($K>1$) is assumed first and the analysis is based on steady state conditions. From equations (4.19), (4.25), (4.29) and assuming that the switch parasitic (or discrete) capacitor is very small, so that the duration of mode 4 can be neglected, the value of the snubber inductor L_S , choosing the factor K, can be computed using the following formula;

$$L_S = \frac{1 - d_{MIN}}{2 f_{SW} I_{OW} \left[\frac{2}{(K-1)V_{INMAX}} + \frac{1}{V_{INMAX}}\right]} \tag{4.33}$$

where

K is the chosen factor that dictates the overvoltage across the storage capacitor C_C for the case of minimum duty cycle (d_{MIN}) and maximum supply voltage (V_{INMAX}).

4.6 Design example

In this section a design example is provided. Experimental verification follows in Section 4.9. The dc bus active snubber subcircuit of the converter topology shown in Fig. 4-1 is to be designed with the following specifications:

Output power $P_{OUT} = 2.0$ kW

Output voltage $V_{OUT} = 160$ V

Switching frequency $f_{SW} = 20$ kHz

Assuming that the input voltage varies within the following limits

$$170 \text{ V} < V_{IN} < 200 \text{ V}$$

the minimum duty cycle from eqn. (4.30) is

$$d_{MIN} = 0.8$$

Taking as a typical converter efficiency

$$\eta = 0.92$$

the worst case for the snubber inductor L_S current from eqn. (4.32) is

$$I_{OW} = \frac{P_{OUT}}{V_{OUT}\,\eta} \approx 13.5 \ A$$

The last step is the calculation of the snubber inductor L_S for a desired voltage across the storage capacitor C_C. Choosing a typical overvoltage factor K under rated conditions as

$$K = 1.2$$

the snubber inductor L_S using eqn. (4.33) is approximately

$$L_S = 6.7 \ \mu\text{H}$$

Typical snubber (switch parasitic) capacitor value for this power level is

$$C_S = 2.4 \ \text{nF}$$

The maximum value of the current that is flowing through the snubber inductor L_S during

the mode 2 can be calculated from eqn. (4.10) and it is

$$I_{max} = 17.8 \text{ A}$$

Following the analysis presented in the preceding section, the width of the gating signal applied to auxiliary switch S_O, using eqn. (4.25) is

$$t_6 - t_5 = 2.26 \ \mu\text{s}$$

The dead time between auxiliary switch S_O turn-off and inverter switches turn-on is using eqn. (4.29)

$$t_7 - t_6 = 450 \text{ ns}$$

Therefore the auxiliary switch S_O is turned on 2.71 μs before the main switches for a duration of 2.26 μs.

4.7 Component ratings

In this section, the component ratings of the converter are given. The worst operating point for the converter is chosen. According to the analysis previously presented, the rated power and maximum input voltage are considered as worst operating conditions.

The voltage and current ratings of the various system components are as follows:

$V_{IN,MAX} = 200$ V, $V_{CC,MAX} = 250$ V, $I_O = 12.8$ A, $P_{OUT} = 2000$ W, $V_{OUT} = 160$ V

Snubber inductor L_S :	RMS current:	$I_{Ls,RMS} = 12.3$ A
	Peak current:	$I_{Ls,MAX} = 17.2$ A
	Peak voltage:	$V_{Ls,MAX} = V_{IN,MAX} = 200$ V
	Total KVA:	$KVA_{Ls} = V_{IN,MAX} I_{Ls,MAX} = 3{,}430$ VA
Clamp capacitor C_C :	Peak current:	$I_{CC,MAX} = 17.2$ A
	Peak voltage:	$V_{CC,MAX} = 250$ V
	Total KVA:	$KVA_{CC} = I_{CC,MAX} V_{CC,MAX} = 4{,}300$ VA

Auxiliary switch S_O :	RMS current:	$I_{AUX,RMS}$ = 4 A
	Peak Current:	$I_{AUX,MAX}$ = 17.2 A
	Average current:	$I_{AUX,AVG}$ = 0 A
	Peak voltage:	$V_{AUX,MAX}$ = 250 V
Converter switches:	RMS current:	$I_{SW,RMS}$ = 8 A
	Average current:	$I_{SW,AVG}$ = 5 A
	Peak voltage:	$V_{SW,MAX}$ = 250 V
Transformer:	RMS current:	$I_{PRI,RMS}$ = 11.5 A
	Peak current:	$I_{PRI,MAX}$ = 13.2 A
	RMS voltage:	$V_{PRI,RMS}$ = 180 V
	Peak voltage:	$V_{PRI,MAX}$ = 250 V
	Total kVA:	kVA = 2070 kVA
Rectifier diodes:	RMS current:	$I_{D,RMS}$ = 9 A
	Average current:	$I_{D,AVG}$ = 6.5 A
	Peak current:	$I_{D,MAX}$ = 13.2 A
	Reverse peak volt.:	$V_{D,MAX}$ = 250 V

4.8 Simulation results

The performance of the proposed *soft switching* topology shown in Fig. 4-1 was simulated using a standard electronic circuit simulation package [67]. The simulated waveforms obtained from the analysis performed with the simulator are depicted in Fig. 4-5. In particular, Figs. 4-5(a) and 4-5(b) show the dc bus current and voltage respectively. As discussed before, the dc bus current becomes negative when the auxiliary switch S_O is turned on and the energy stored in the snubber inductor L_S is used to introduce a zero volt interval

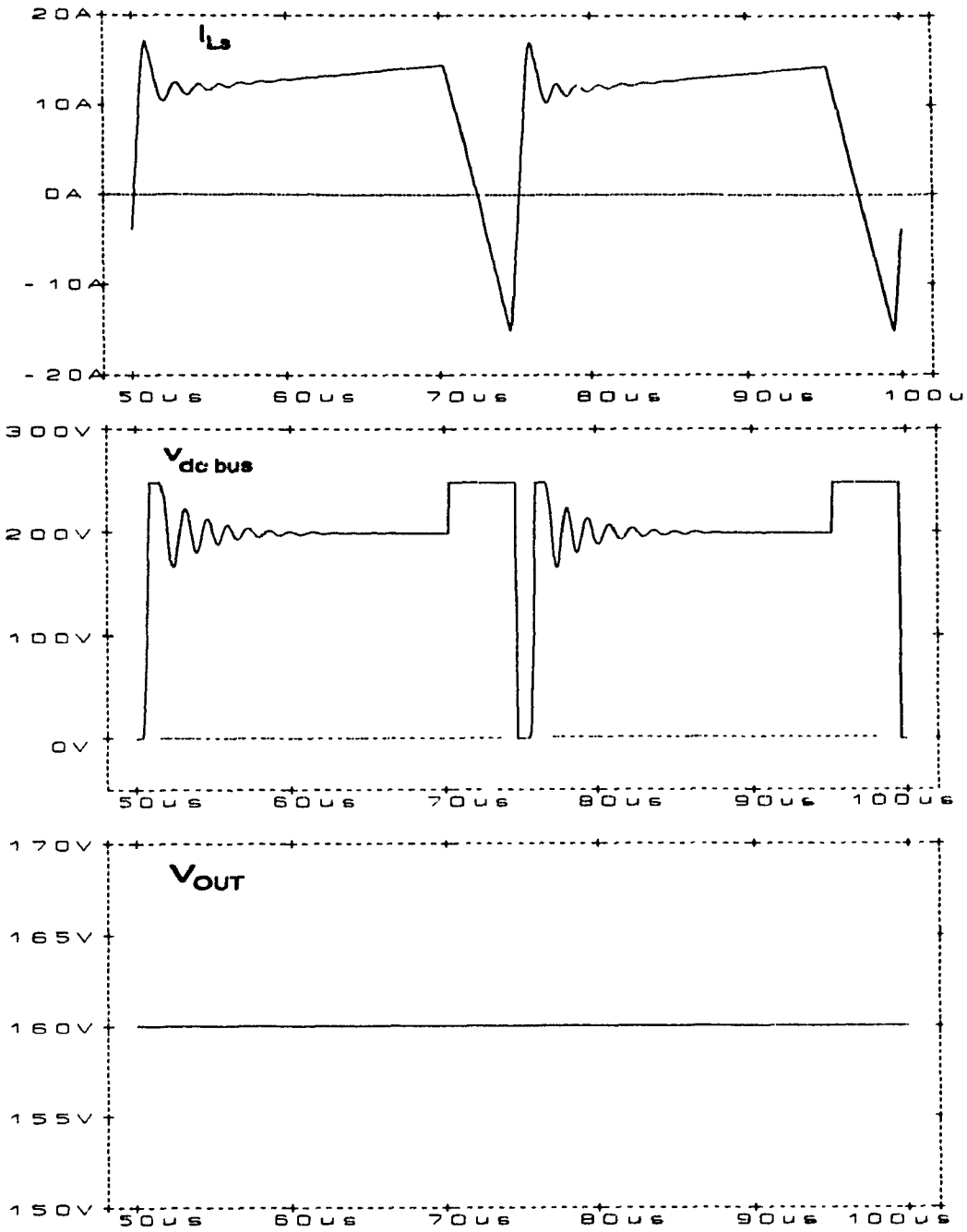
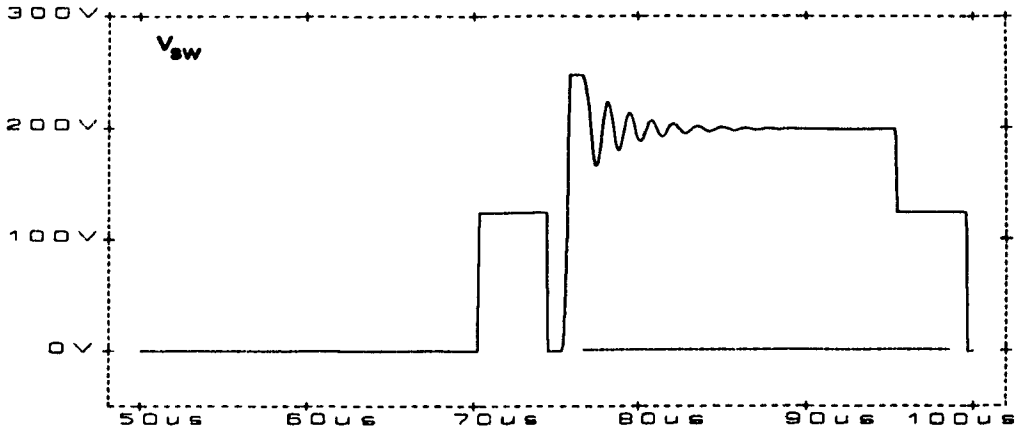
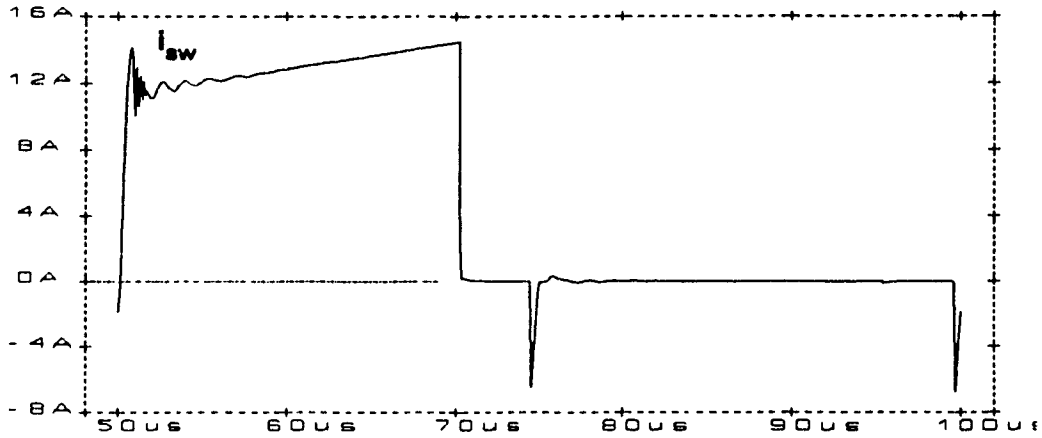


Figure 4-5: Converter steady-state simulated waveforms.
V_{INMAX} = 200 V, $V_{CC,MAX}$ = 250 V, I_O = 12.8 A, P_{OUT} = 2 kW.
L_S = 7 μH, d = 0.8, f_{SW} = 20 kHz.
a) Dc bus current.
b) Dc bus voltage.
c) Load voltage.

d)



e)



f)

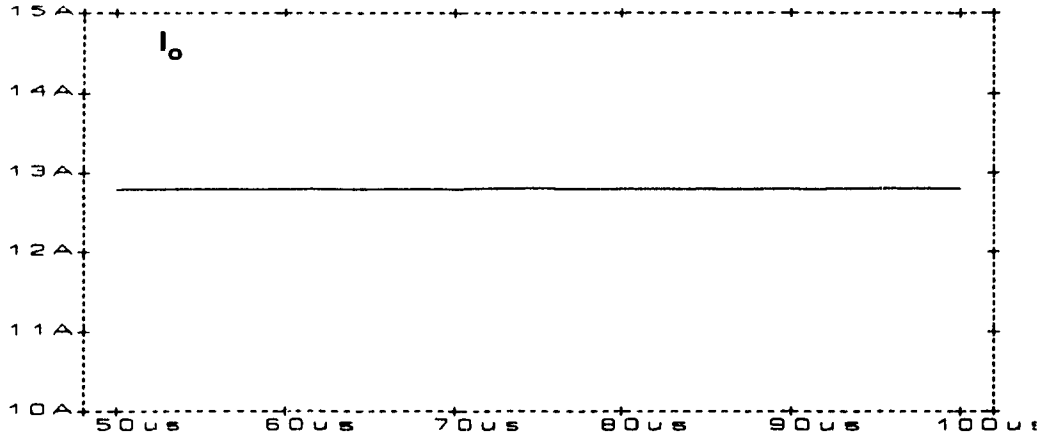


Figure 4-5: Converter steady-state simulated waveforms.
V_{INMAX} = 200 V, $V_{CC,MAX}$ = 250 V, I_O = 12.8 A, P_{OUT} = 2 kW.
L_S = 7 μH, d = 0.8, f_{SW} = 20 kHz.
d) Switch voltage.
e) Switch current.
f) Load current.

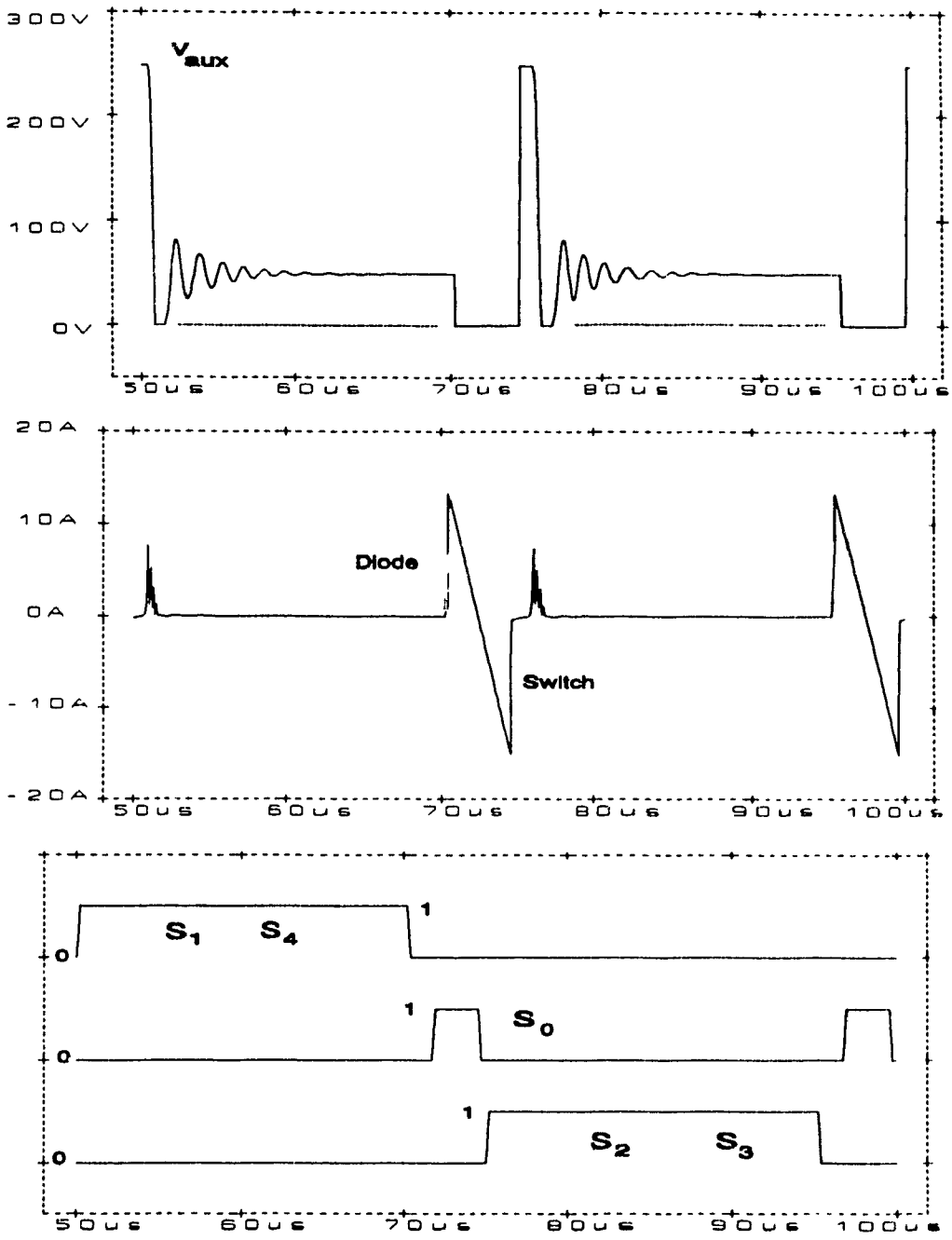


Figure 4-5: Converter steady-state simulated waveforms.
V_{INMAX} = 200 V, $V_{CC,MAX}$ = 250 V, I_O = 12.8 A, P_{OUT} = 2 kW.
L_S = 7 µH, d = 0.8, f_{SW} = 20 kHz.
g) Auxiliary switch voltage.
h) Storage-clamp capacitor current.
i) Switch gating signals.

across the dc bus, whenever the auxiliary switch is turned off. The load voltage is depicted in Fig. 4-5(c). The respective switch voltage and current are demonstrated in Figs. 4-5(d) and (e). It is clearly shown that before the main transistors turn-on moment, the current is flowing through the antiparallel diodes thus providing *soft switching* conditions (ZVS). The load current is shown in Fig. 4-5(f). The voltage and current waveforms of the auxiliary switch S_o are depicted in Figs. 4-5(g) and (h) respectively. Finally, the gating signals of all converter switches are plotted in Fig. 4-5(i).

4.9 Experimental results

To establish the feasibility of the proposed full-bridge medium-power high-frequency zero voltage switching PWM converter topology and to verify the theoretical results, a 2-kW laboratory unit operating at 20-kHz switching frequency was built and tested. Experimental results are shown in Fig. 4-6. In particular, Fig. 4-6(a) shows the dc bus voltage, which as predicted in Section 4.4 (Fig. 4-4(b)), decreases towards zero before the main switches of the converter turn-on. Fig. 4-6(b) shows the respective dc bus current. As predicted (Fig. 4-4(a)) this current becomes negative due to the auxiliary switch S_o turn-on, thus discharging the storage capacitor C_c. It also forces the antiparallel diodes of the main switches to conduct prior to the switch turn-on, as predicted in Section 4.4. Fig. 4-6(c) shows the voltage across the auxiliary switch S_o and finally Fig. 4-6(d) shows the converter switch voltage.

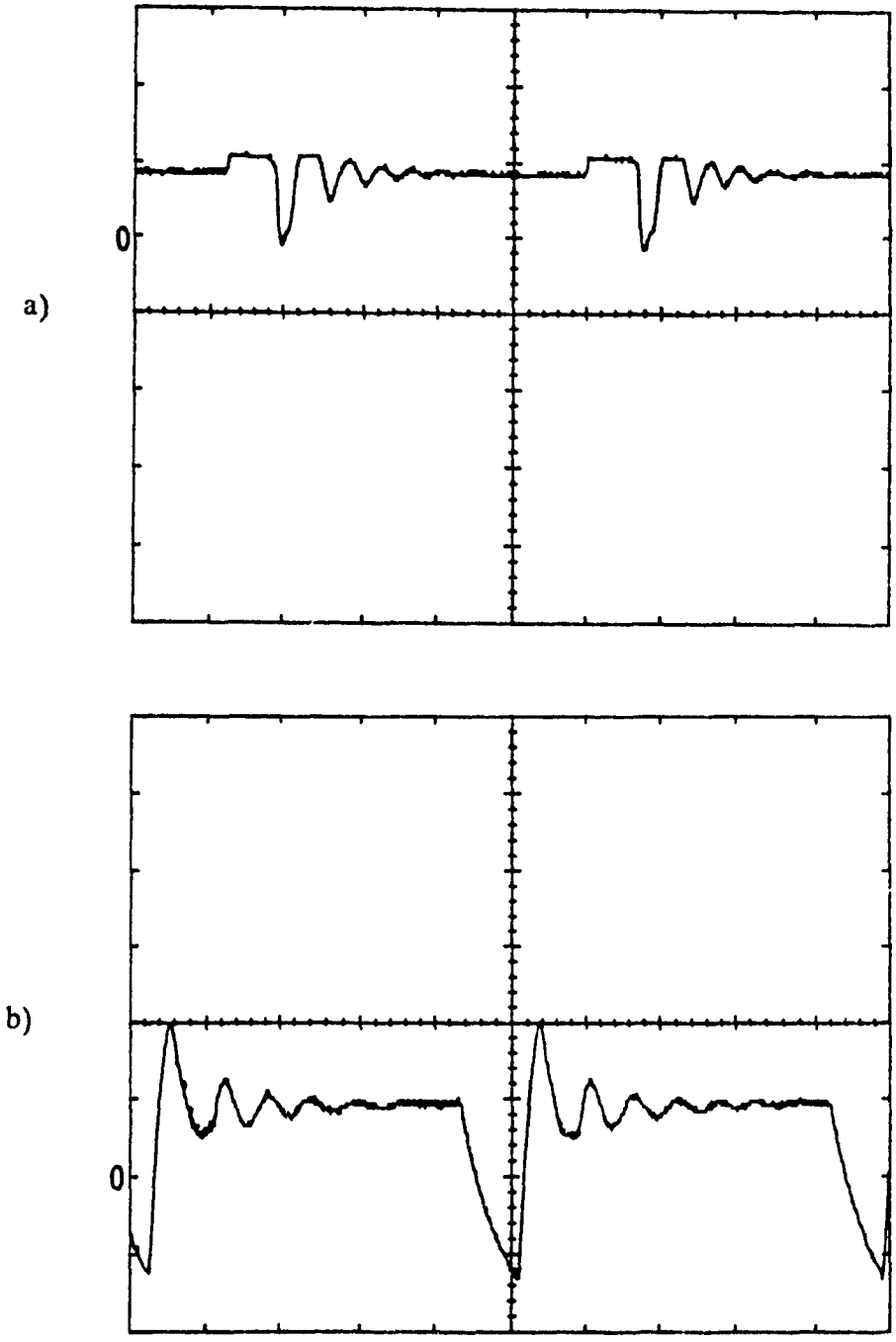


Figure 4-6: Experimental converter waveforms.

L_S = 7 μH, C_C = 10 μF, f_{SW} = 20 kHz, d = 0.8, P_{OUT} = 2 kW.

a) Dc bus voltage (200 V/div, 5 μs/div).

b) Dc bus current (10 A/div, 5 μs/div).

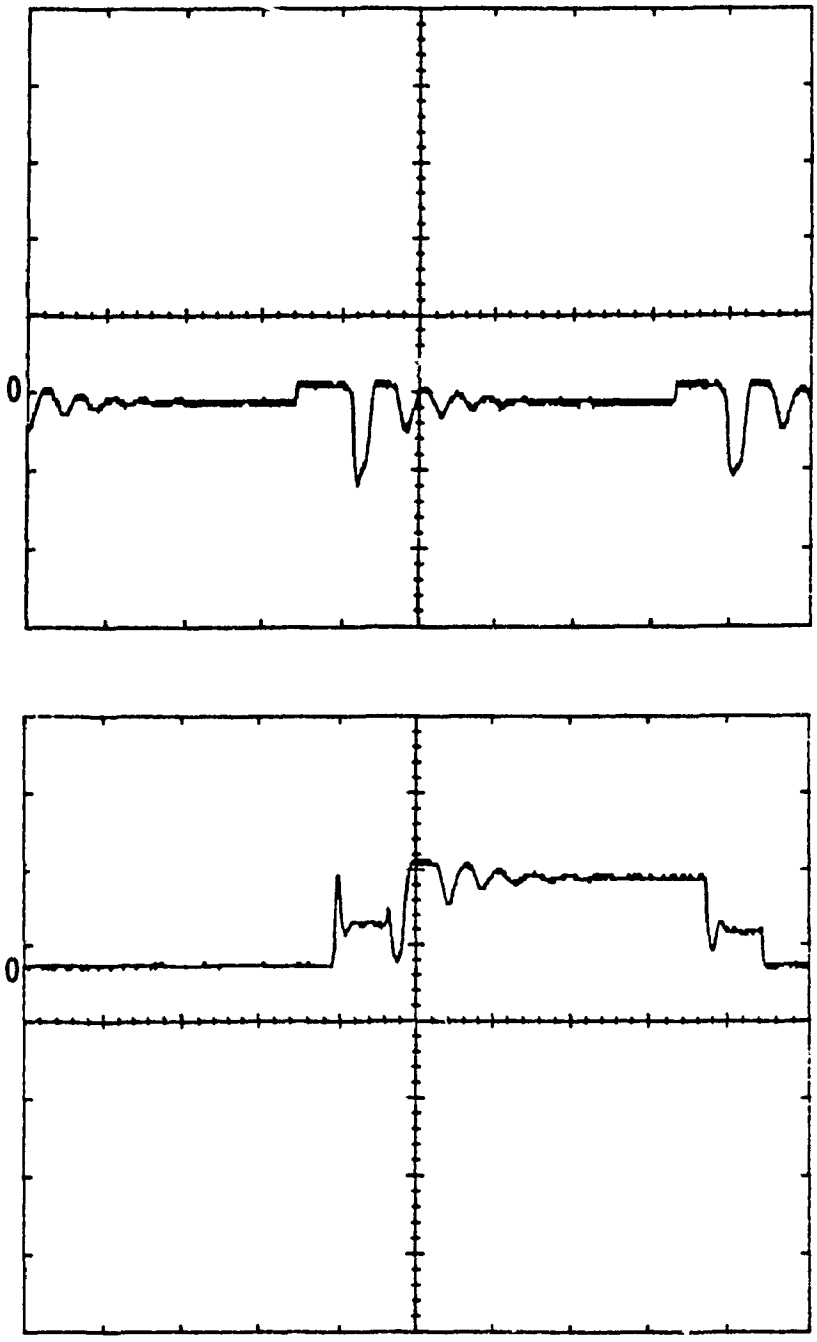


Figure 4-6: Experimental converter waveforms.

L_s = 7 µH, C_c = 10 µF, f_{sw} = 20 kHz, d = 0.8, P_{OUT} = 2 kW.

c) Auxiliary switch S_o voltage (200 V/div, 5 µs/div).

d) Converter switch voltage (200 V/div, 5 µs/div).

4.10 Conclusions

A thorough analysis and design procedure of a full-bridge medium-power high-frequency zero voltage switching (ZVS) pulse width modulated (PWM) converter topology has been provided in this chapter. Zero voltage turn-on/off switching conditions are obtained through the use of an energy recovery subcircuit (dc bus active snubber) that ensures the prior discharge of the parasitic (or small discrete) capacitors of the main switches before they are turned on. The topology under consideration makes use of switch parasitic capacitors (mainly present in power MOSFET's). Moreover, by providing zero voltage switching conditions, it reduces the electric noise generated by the converter. *Soft switching* environment for converter switches as well as the auxiliary switch are obtained for a wide range of load current. The converter has been thoroughly analyzed and steady-state waveforms obtained through a circuit simulator (PSPICE) have been presented. Theoretical results have been verified experimentally on a 2-kW, 20-kHz laboratory prototype.

CHAPTER 5

A NOVEL THREE-PHASE SOFT SWITCHING PWM VSI TOPOLOGY

5.1 Introduction

The continuing search for an optimum three-phase *soft switching* (namely zero voltage switching, ZVS), voltage source inverter (VSI) topology over the last decade has led to the development of various novel inverter circuits. These topologies have been critically discussed in Chapter 2.

In this chapter, a novel three-phase ZVS PWM VSI topology employing a simple dc bus active snubber subcircuit is proposed [65], [66]. The main advantage of this topology is that the dc bus snubber subcircuit is activated only when required, that is, when dictated by the respective pulse width modulator (PWM). Detailed analysis and the principles of operation of the proposed power inverter scheme are provided in the following section.

5.2 Inverter power circuit description

The schematic of the three-phase inverter topology with the proposed dc bus commutating subcircuit is shown in Fig. 5-1. The converter power circuit includes the dc supply voltage V_{IN} , the six main inverter switches (S_1 - S_6), the switch antiparallel diodes (D_1 - D_6), the switch parasitic (or small discrete) capacitors (C_1 - C_6), the dc bus commutating subcircuit consisting of the dc bus snubber inductor L_S , the storage-voltage clamp capacitor C_C , the auxiliary *notch* switch S_O , the auxiliary switch antiparallel diode D_O and the three phase load.

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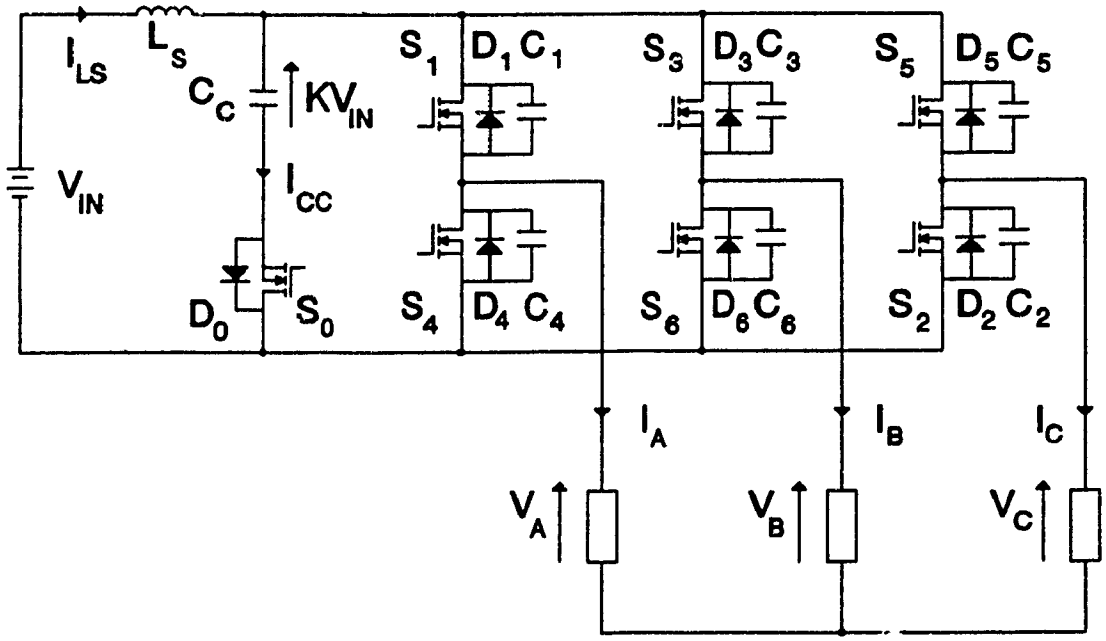


Figure 5-1. The novel *notch* commutated three-phase PWM ZVS VSI topology.

5.3 Principles of operation

The switching environment resulting from the inverter topology (Fig. 5-1) is investigated in this section. Firstly, due to the purely capacitive snubber employed, any switching turn-off point is considered as a *soft switching* point since the discharged switch capacitor always provides zero voltage turn-off conditions. On the other hand, any switching turn-on point is considered as a *soft switching* one, whenever the switch antiparallel diode (due to the direction of the load current) conducts prior to the main transistor turn-on. Finally, a *hard switching* point could occur any time that switch capacitor is charged to the dc bus voltage and is required to discharge through the switch during turn-on. Moreover, when the load current (due to its polarity) is to flow through the switch, capacitor energy needs to be dissipated inside the transistor thus increasing switching turn-on losses and

current is going to flow through D_3 even if S_3 is turned on. To avoid this situation, the auxiliary switch S_O is turned on ($t=t_4$, Fig. 5-2(d)) immediately before the instant that a *hard switching* point is to occur ($t=t_6$, Fig. 5-2(c), S_1 , S_5 are turned on). Since the voltage level of the voltage-clamp capacitor C_C is higher than the input voltage, a negative voltage, namely the difference between the input supply voltage V_{IN} and the overvoltage of C_C is applied across the dc bus inductor L_S thus allowing the dc bus current to reverse polarity (Fig. 5-2(b)). The negative current flowing through the snubber inductor L_S (Fig. 5-2(b)) first discharges the switch parasitic capacitors C_1 - C_6, after the auxiliary switch S_O is turned off ($t=t_5$, Fig. 5-2(d)). Then it forces the antiparallel diodes (D_1 - D_6) to conduct thus providing a zero volt *notch* across the dc bus (Fig. 5-2(a)). All the energy associated with the switch parasitic (or small discrete) capacitors is completely recovered through the use of an active dc bus network and is returned back to the source. Consequently, the dc bus commutating circuit sets good conditions for all inverter switches to turn-on with minimum switching losses. Furthermore, because these turn-on instants are associated with the vertical edge of the carrier waveform, switches of the same leg are also turned-off under zero voltage conditions before the respective turn-on moment $t=t_6$. Therefore, some of the turn-off points occur under zero voltage and this is achieved due to the presence of the parasitic (or small discrete) capacitors. Turn-off switching points also occur under zero voltage conditions due to the zero volts *notch* introduced by the operation of the dc bus commutating subcircuit as explained above.

5.4 Modulation strategy

The *soft switching* topology (Fig. 5-1) discussed in this chapter, however, requires a particular PWM technique to yield optimum overall performance. This technique is shown

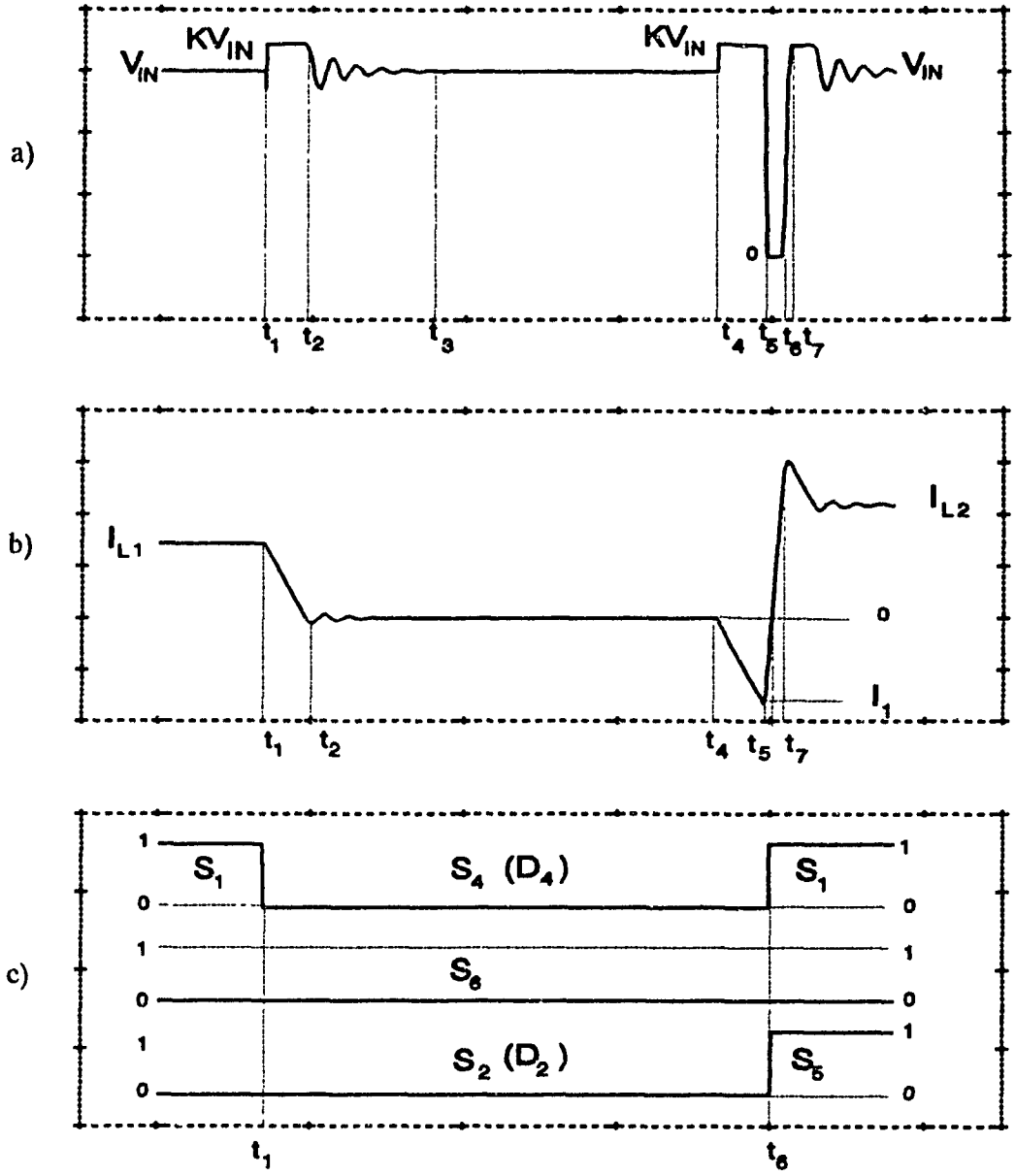


Figure 5-2: A microscopic view of the dc bus commutating subcircuit operation.

a) Inverter dc bus voltage.

b) Dc bus current I_{Ls} .

c) Inverter switch gating signals.

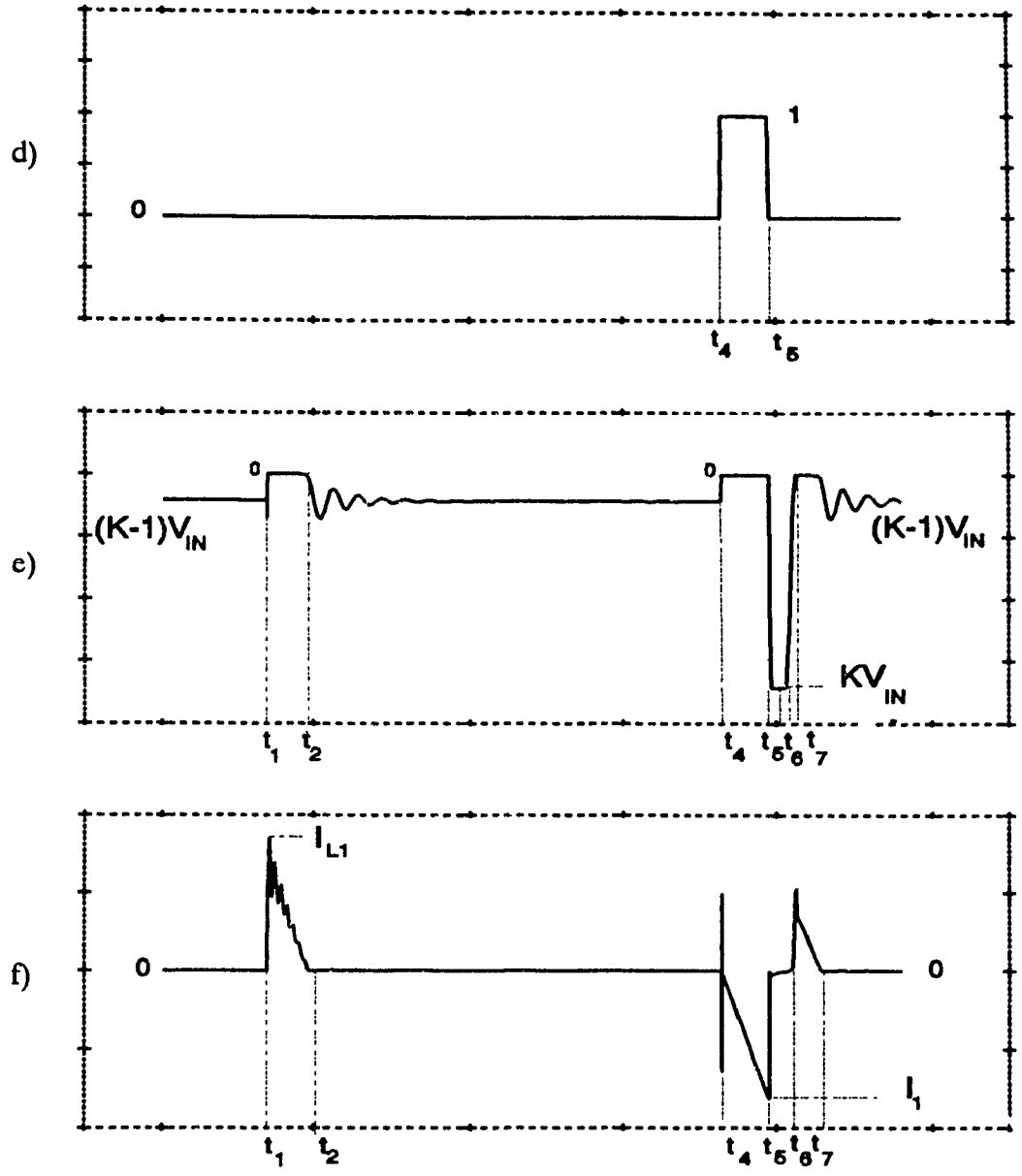


Figure 5-2: A microscopic view of the dc bus commutating subcircuit operation.

d) Auxiliary switch gating signal.

e) Auxiliary switch voltage.

f) Capacitor C_c current, I_{cc} .

in Fig. 5-4. Moreover, the respective description and modulation index control on a line-to-neutral basis is plotted in Fig. 5-4. The use of sawtooth carrier instead of triangular one is dictated by the following reasons:

- The number of possible commutations occurring simultaneously is increased;
- Almost half of the switching points are provided *a priori;*
- A free-wheeling mode associated with the vertical edge of the carrier waveform is introduced.

The proposed combination of the novel *notch* commutated PWM inverter and this refined PWM technique is optimum for the following reasons:

- The overall system provides all the advantages of a *soft switching* and PWM topology;
- The dc bus goes periodically, at the carrier frequency, through narrow zero volt intervals, but only when needed and as dictated by the PWM technique;
- *Soft switching* environment is achieved at a lowest possible switching frequency;
- The introduction of the dc bus commutating subcircuit has only a minimal affect on the inverter output waveforms.

This section also identifies the modulation technique that is well suited to the novel *notch* commutated three phase voltage source inverter topology (Fig. 5-1). For this purpose two PWM techniques, one well-known and the other being the proposed one, are discussed next.

5.4.1 The third-harmonic injection PWM technique

This technique has been derived from the original sine PWM technique through the addition of the 17% third-harmonic component to the original sine reference waveform.

The analytical expression for the reference waveform is as follows;

$$y = 1.15 \sin(\omega t) + 0.19 \sin(3\omega t) \tag{5.1}$$

Fig. 5-3 shows the implementation of the harmonic injection sinusoidal PWM (HIPWM - 1st and 3rd). In particular, it shows the triangular carrier with the respective reference waveform (line-to-neutral) and their corresponding points of intersections (i.e. switching points) for one phase only. For the other two phases, the same reference is used displaced by 120° and -120°.

5.4.2 The refined PWM technique

A visual description of a complete cycle of a line to neutral PWM generator based on the refined PWM technique is shown in Fig. 5-4. Moreover, for the first 60°, a segment of a sine waveform that has its maximum value at the 30° point is used as a reference waveform. Then and for the next 60°, the amplitude of the reference waveform is increased so that no intersections between the reference and the carrier occur. Afterwards, for the next 60° a segment of a sine waveform that has its maximum value at the 90° point is used as a reference. That completes the first half cycle and the same procedure is also repeated for the second half cycle. The amplitude of the sine segments, that are used to produce the overall reference waveform, control the magnitude of the fundamental component of the line-to-line voltage waveform (modulation index). It is also noted that the carrier waveform has a positive slope for the first half period, and a negative slope for the other half. The same kind of reference displaced by 120° and -120° is used for the other two phases.

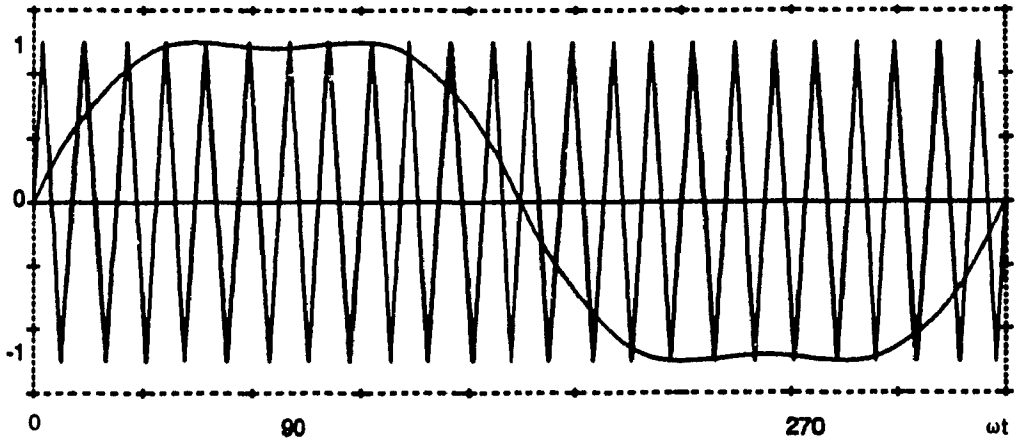


Figure 5-3: HIPWM (1st - 3rd) - Description and modulation index control.

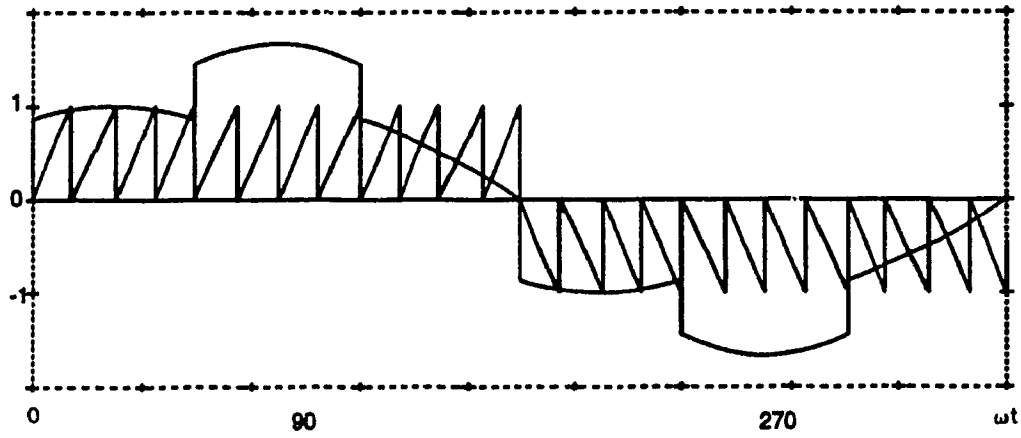
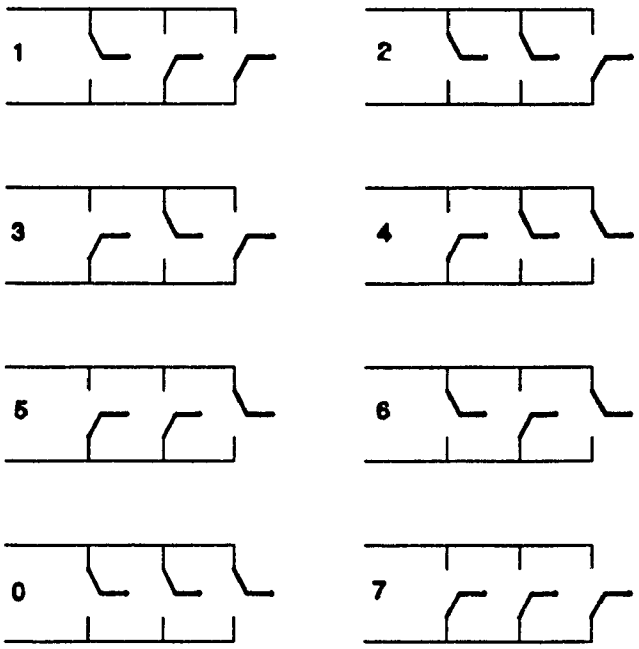


Figure 5-4: Refined PWM technique - Description and modulation index control.

INVERTER STATE	GATED DEVICE			NORMALIZED VOLTAGES		
	LEG A	LEG B	LEG C	V_{AB}	V_{BC}	V_{CA}
0	1	3	5	0	0	0
1	1	6	2	1	0	-1
2	1	3	2	0	1	-1
3	4	3	2	-1	1	0
4	4	3	5	-1	0	1
5	4	6	5	0	-1	1
6	1	6	5	1	-1	0
7	4	6	2	0	0	0

Table 5-1: Switching states of the three-phase inverter and normalized output voltages.

The eight possible inverter switching states are summarized in Table 5-1 along with the respective line-to-line voltages in a normalized form. Furthermore, the inverter switching states for a generalized bridge are shown in Fig. 5-5(a) and the respective vectors associated with these states are depicted in Fig. 5-5(b).



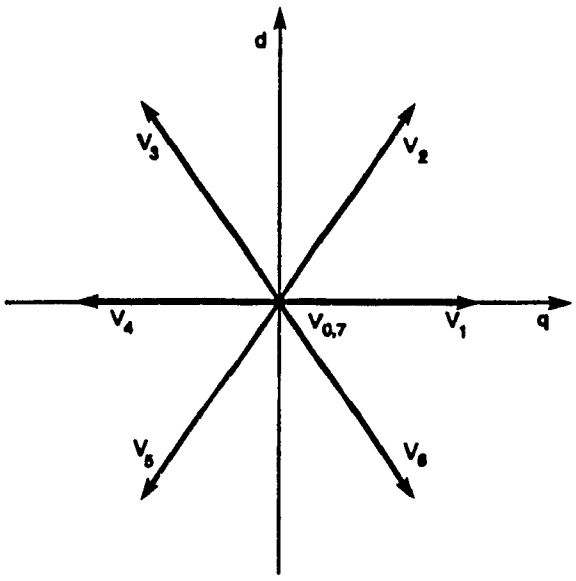


Figure 5-5: a) Inverter switching states.

b) Associated inverter output voltage vectors.

To illustrate further that the refined PWM technique is more compatible with the novel *notch* commutated inverter topology (Fig. 5-1), equivalent of 45° expanded segments of gating signals generated by the HIPWM (1st and 3rd) and the refined PWM technique are plotted in Figs. 5-6 and 5-7 respectively. The same conditions such as carrier frequency and modulation index are used with both modulators. Specifically, the carrier frequency is 24 pu and the modulation index is 1.

It is further assumed, and without loss of generality that currents I_A and I_C are positive and current I_B is negative. Therefore, referring to Figs. 5-1 and 5-6, any rising edge of waveforms G_1 and G_5 ($I_A>0$, $I_C>0$) results in a potentially *hard switching* point according to the considerations of the switching environment given in Section 5.3. Similarly any falling edge of waveform G_6 ($I_B<0$) results in an also potentially *hard switching* point. Referring now to Figs. 5-1 and 5.7, any rising edge of waveforms G_1 and G_5 results in a potentially *hard switching* point as well. However, due to the fact that each switch conducts completely for 60°, it happens that switch S_6 conducts for the whole interval under consideration thus there is no switching point associated with this leg of the inverter bridge. For clarity purposes, all the possible *hard switching* points are identified in Figs. 5-6 and 5-7 by a thick line.

Generally, the refined PWM scheme offers 1/3 fewer switching points compared with the HIPWM (1st and 3rd). Furthermore, comparing the gating signals demonstrated in Figs. 5-6 and 5-7, it is clearly illustrated that the refined PWM technique also provides 1/3 fewer potentially *hard switching* points (6/9). However, due to the ramp carrier, it happens that the possible *hard switching* points occur concurrently. Therefore, and when the refined PWM technique is used the switching frequency of the proposed dc bus commutating subcircuit is reduced by 66%. This remarkable reduction in switching frequency is the main

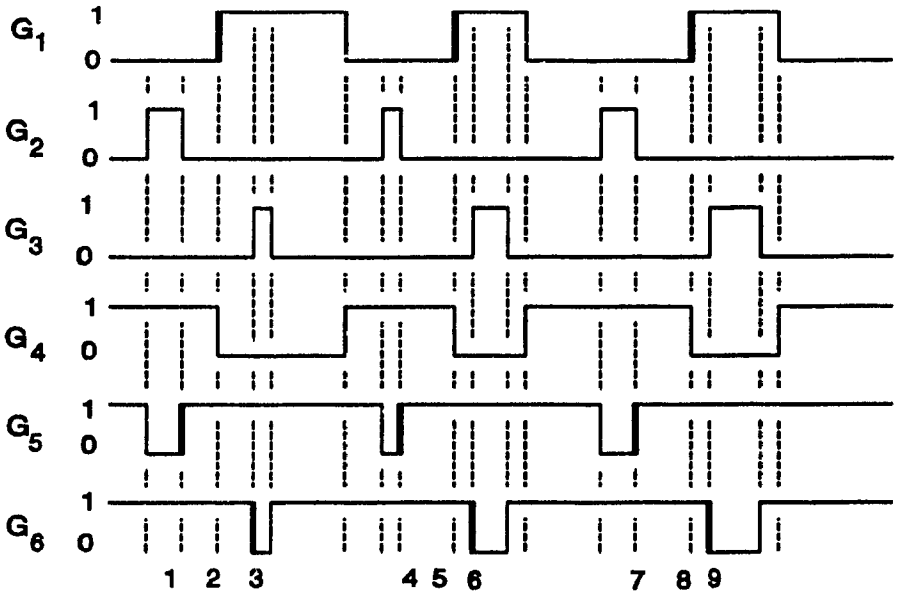


Figure 5-6: An expanded 45° segment of gating signals generated with the HIPWM (1st - 3rd) technique. The thick line indicates a potential *hard switching* point.

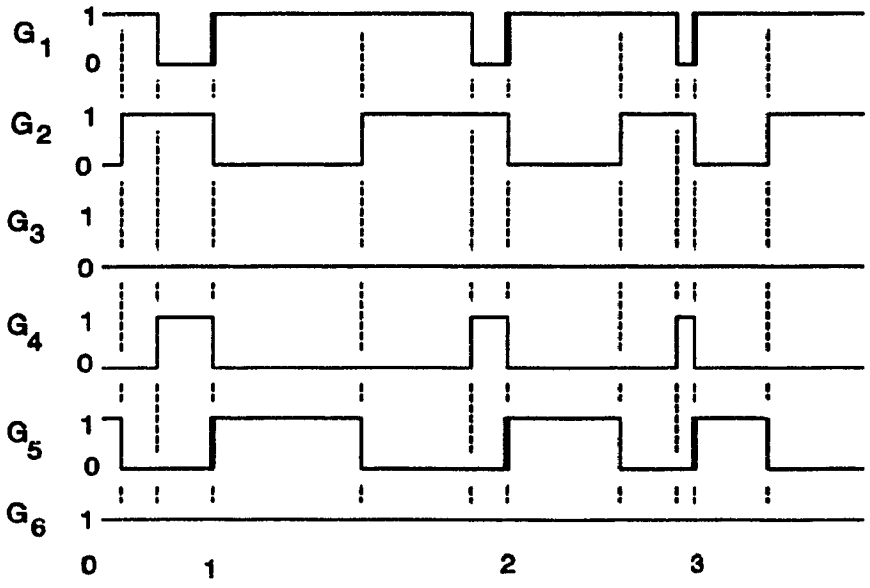


Figure 5-7: An expanded 45° segment of gating signals generated with the refined PWM technique. The thick line indicates a potential *hard switching* point.

reason for claiming that the combination of the refined PWM technique and the proposed dc bus commutating subcircuit yields an optimum switching performance.

It is further noted that these possible *hard switching* points (Fig. 5-7) are associated with the vertical edge of the carrier waveform thus providing an easy way of synchronizing the dc bus commutating subcircuit with the pulse width modulator. Moreover, the vertical edge always provides intersection independently of the modulation index. It is also clearly shown (Fig. 5-6) that the *hard switching* points in the case of the HIPWM (1st and 3rd) do not follow a fixed pattern and it is practically impossible to synchronize this scheme with this dc bus commutation approach (ZVS) since the modulation index changes the instants that the dc bus subcircuit needs to be activated.

It is also noted that the free-wheeling mode associated with the vertical edge of the refined PWM technique does not always occur in the case of the HIPWM scheme, since a triangular waveform is used as carrier. Specifically, only the points 1,4,7 (Fig. 5-6) occur after a free-wheeling mode (either switches S_2, S_4, S_6 or the respective antiparallel diodes D_2, D_4, D_6 are conducting). Therefore, and for the rest of the points, reversing the dc bus current employing the dc bus commutating circuit described previously is rather difficult, and depending on the load current, might be impossible.

Finally, from the above discussion, the ZVS approach and optimum system performance using the inverter topology shown in Fig. 5-1 can be achieved if and only if this inverter topology is combined with the refined PWM modulation strategy.

Other advantages of the proposed combination are as follows:

- The implementation of the PWM technique is simple since it can be done using only typical digital or analog electronic components. Even if a μP is used, the algorithm required is very simple and fast since almost half of the switching points

are known *a priori*;

- The refined PWM technique has similar ac and dc gains as the HIPWM (1st and 3rd);
- Higher switching frequencies can be achieved, limited only by the necessary time to operate the dc bus commutating subcircuit;
- Reduction in switching losses is further enhanced by reduction in inverter switching frequency (1/3 fewer switching points compared with the HIPWM).

It must be said that the turn-on process associated with the auxiliary switch S_O is not completely lossless. However, the losses in the commutating circuit itself are low due to the low voltage being commutated $(K\text{-}1)V_{IN}$ during turn-on. Nevertheless, a parasitic or a small discrete capacitor in parallel with the auxiliary switch can provide zero voltage switching turn-off.

The analysis and the description of the various topological modes (TM's) due to the presence of the dc bus commutating subcircuit are presented in the following section.

5.5 Steady-state analysis - Modes of operation

In this section, the description of the different topological modes (TM's) and the analysis of the inverter topology under consideration due to the introduction of the dc bus commutating subcircuit are presented in detail. The analysis is based on the following assumptions:

- The switch includes a parasitic (or small discrete) capacitor in parallel. This capacitor is taken as voltage invariable;
- The capacitors and the inductors are lossless;
- The supply voltage V_{IN} is assumed ripple free;

- The value of the storage-voltage clamp capacitor C_C is large resulting in an essential constant ripple-free clamping voltage;
- The three phase load is balanced.

It is assumed that the storage-voltage clamp capacitor C_C has the following voltage:

$$V_{CC} = K V_{IN} \tag{5.2}$$

where

$$K \rangle 1 \tag{5.3}$$

It is further assumed that

$$C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = C_S \tag{5.4}$$

The sequence of the topological modes (TM's) (Fig. 5-2) is as follows.

Mode 1, Interval $t_1 < t < t_2$.

At $t=t_1$ (Fig. 5-2), the inverter enters the freewheeling mode dictated by the sawtooth carrier waveform. All the three line-to-line voltages become zero. That implies that during this mode the current flowing through the dc bus snubber inductor L_S decreases towards zero (Fig. 5-2 (b)). All the energy from L_S is transferred to the storage-voltage clamp capacitor C_C through the diode D_O which becomes forward biased. The respective switch capacitors either the bottom or the top ones are charged up to the value KV_{IN}. The specific slope of the current depends upon the difference in voltage $(1-K)V_{IN}$ and the value of the inductor L_S.

$$i_{Ls}(t) = \frac{(1-K)V_{IN}}{L_S}(t-t_1) + i_{Ls}|_{t=t_1} \tag{5.5}$$

where

$$i_{Ls}|_{t=t_1} = I_{L1} \tag{5.6}$$

At the end of this mode

$$i_{Ls}|_{t=t_2} = 0 \tag{5.7}$$

As stated earlier, during this mode the storage-voltage clamp capacitor C_C is charged up.

Mode 2, Interval $t_2 < t < t_3$.

During this mode, the switch capacitors are discharged from the previous value KV_{IN} to the dc supply voltage V_{IN} since all the stored energy in L_S has been transferred into the capacitor C_C and the diode D_O now blocks the voltage.

Mode 3, Interval $t_3 < t < t_4$.

During this mode, the dc bus current is equal to zero, the inverter still operates in the freewheeling mode.

$$i_{Ls}|_{t=t_4} = 0 \tag{5.8}$$

Mode 4, Interval $t_4 < t < t_5$.

During this interval, the current flowing through the dc bus snubber inductor L_S reverses polarity since the auxiliary switch S_O is turned on at $t=t_4$ (Fig. 5-2(d)). Due to the overvoltage of the storage-voltage clamp capacitor C_C, the voltage applied across L_S is equal to $(1\text{-}K)V_{IN}$. Energy is transferred from the capacitor C_C back to the source through L_S .

The current c ˆ the dc bus inductor decreases towards a negative value linearly due to the constant overvoltage of C_C and the respective equation is as follows:

$$i_{Ls}(t) = \frac{(1-K)V_{IN}}{L_S}(t-t_4) + i_{Ls}|_{t=t_4} \tag{5.9}$$

At the end of this mode the value of the current flowing through the dc bus snubber inductor L_S is

$$I_1 = \frac{(1-K)V_{IN}}{L_S}(t_5-t_4) \tag{5.10}$$

The on time of the auxiliary switch S_O (t_5-t_4) can be adjusted to achieve a specific clamp voltage that is not higher than 1.1~1.3 times the input voltage V_{IN}. Consequently by controlling the on time of the auxiliary *notch* switch, it is possible to maintain a preset value for the clamping voltage (KV_{IN}) if the average power flow into the capacitor C_C is kept zero.

It is also noted that whenever the auxiliary switch is turned on, the switch parasitic or discrete capacitors C_1 - C_6 are charged up from the input voltage V_{IN} to the overvoltage KV_{IN}. Due to the presence of the dc bus inductor L_S, this extra energy is provided from the storage-voltage clamp capacitor C_C through S_O. Therefore, the commutation of the auxiliary switch is not completely lossless as in the case of the main inverter switches. However, it can be said that the losses are very low since only the voltage difference $(K-1)V_{IN}$ is being commutated.

Mode 5, Interval $t_5 < t < t_6$.

The current through the dc bus snubber inductor has already reversed polarity and now the auxiliary switch S_O is turned off ($t=t_5$, Fig. 5-2(d)). The extra energy stored in the inductor L_S discharges all the switch parasitic or small discrete capacitors (C_1 - C_6) first. Then it forces the antiparallel switch diodes D_1 - D_6 to conduct. Therefore, *soft switching* commutation (ZVS) for the incoming turn on of inverter switches is achieved. Moreover, inverter switches of the same leg are turned off under zero voltage before the respective turn on time of the other switches ($t=t_6$, Fig. 5-2(c)). The dc bus current increases from its negative value towards the zero value while linearly controlled only by the input voltage source V_{IN} and the inductor value L_S as follows:

$$i_{Ls}(t) = I_1 + \frac{V_{IN}}{L_S}(t-t_5) \tag{5.11}$$

The current at $t=t_6$ is equal to zero (Fig. 5.2(b))

$$i_{Ls}\,|_{t=t_6} = 0 \tag{5.12}$$

therefore the duration of this mode can be easily calculated from the following equation:

$$t_6 - t_5 = \frac{I_1 L_S}{V_{IN}} \tag{5.13}$$

Taking into account eqn. (5.10)

$$t_6 - t_5 = (K-1)t_{ON,So} \tag{5.14}$$

This mode introduces a zero volts *notch* across the dc bus. Since the turn-on time of the semiconductor devices is known, the necessary time that the dc bus voltage needs to be at

zero value to ensure minimized switching losses is also known.

Mode 6, Interval $t_6 < t < t_7$.

During this mode the dc bus current is increasing linearly depending as before only upon the value of the input voltage source V_{IN} and the value of the dc bus inductor L_S (Fig. 5-2(b)). The respective equation is the following:

$$i_{Ls}(t) = \frac{V_{IN}}{L_S}(t-t_6) + i_{Ls}|_{t=t_6} \tag{5.15}$$

This mode changes whenever the dc link current equals the load current.

$$i_{Ls}|_{t=t_7} = I_{L2} \tag{5.16}$$

where I_{L2} is the dc link inverter input current.

Moreover, when the load current is equal to the dc link current, the dc bus voltage starts increasing. Therefore, the duration of the zero volts interval across the dc bus that can be introduced, employing the proposed snubber is greater than the value given by eqn. (5.14). However, the duration of the zero volts interval due to the mode 6 is not constant since the load current is not constant. That means that for the design procedure the time given by eqn. (5.14) has to be large enough to ensure zero voltage switching conditions.

Mode 7, Interval $t_7 < t < t_8$.

This is the resonant mode, since the dc bus snubber inductor L_S and the equivalent dc bus capacitor made up by the switch parasitic capacitors C_1 - C_6 oscillate. Since, three semiconductor elements are to conduct the effective dc bus capacitor is equal to three times

the switch capacitor C_S . This mode is another mechanism that charges the capacitor C_C . The equation for the current flowing through the inductor L_S is as follows:

$$i_{Ls}(t) = I_{L2} + \sqrt{\frac{3C_S}{L_S}}\, V_{IN} \sin[\omega_r(t-t_7)] \tag{5.17}$$

where

$$\omega_r = \sqrt{\frac{1}{3\,L_S C_S}} \tag{5.18}$$

and I_{L2} is the inverter input current.

Mode 8, Interval $t > t_8$.

Due to the presence of the storage-voltage clamp capacitor C_C , the voltage across the dc bus is clamped to an acceptable level (KV_{IN}). This is achieved through the antiparallel auxiliary switch diode D_O which becomes forward biased any time that the dc bus voltage increases beyond the value of the overvoltage KV_{IN} (Fig. 5-2(a)). All the extra energy stored in the dc bus snubber inductor L_S during this mode is transferred to the capacitor C_C . The respective slope of the dc bus current is dependant upon the voltage difference $(K\text{-}1)V_{IN}$ and the value of L_S .

Mode 9, Interval $t > t_9$.

The current through the dc bus inductor L_S equals the load current. The power inverter operates like a typical six-switch PWM VSI until the moment that the dc bus commutating subcircuit is again activated before the vertical edge of the carrier waveform

and according to the carrier frequency.

5.6 Discussion - Design guidelines

The design aspects associated with the proposed commutating process are discussed in this section.

First of all, it is important to be noted that for inductive load all the possible *hard switching* points are associated with the vertical edge of the carrier waveform only. However, this is not true for load power factors lower than 0.5.

The necessary time that the dc bus needs to be at zero volts is known from the characteristics of the switching devices. However, it is necessary that this interval is much longer than this time (turn-on time) to ensure that zero voltage switching does occur under different conditions (modulation index, load current, etc.).

The overvoltage of the storage-voltage clamp capacitor C_C (KV_{IN}) increases with an increase of the value of the dc bus snubber inductor L_S, the value of the switch capacitors and the load current. It is very a important point that the switch capacitors C_1 - C_6 are parasitic or very small discrete ones. The reason being that in the case that these capacitors are not completely discharged for any reason, destruction of the inverter switches due to the high stresses is avoided.

It is noted that the slope of the current through L_S is controlled by the voltage $(K\text{-}1)V_{IN}$ and the value of the inductor L_S when the current reverses polarity. The slope is changed when the auxiliary switch is turned off and depends upon the input voltage source V_{IN} and the value of the inductor L_S as well.

Generally, the on time of the auxiliary switch S_O needs to be small since the operation of the dc bus commutating subcircuit introduces limitations to the achievable

switching frequency. Moreover, the on time of the auxiliary switch can be adjusted to obtain a specific value of the clamp voltage. This voltage is necessary to be as close to the input voltage V_{IN} as possible since it dictates the losses in the auxiliary switch during turn on. Consequently, by controlling the on time of the switch S_O, it is possible to maintain a preset and desired value of KV_{IN} if the average power flow into the capacitor C_C is kept zero.

5.7 Design example

In this section a design example is provided.

The inverter output power is as follows:

$$P_{OUT} = 6 \text{ kVA}$$

The input dc power supply voltage

$$V_{IN} = 300 \text{ V}$$

The inverter output frequency

$$f_O = 60 \text{ Hz}$$

Since the ac term gain of the refined PWM technique is

$$G_{AC} = 1$$

The amplitude of the fundamental component of the line-to-line voltage and for MI=1 is

$$V_{L\text{-}L} = 300 \text{ V}$$

therefore the respective RMS value is

$$V_{L\text{-}L,RMS} = 212 \text{ V}$$

The RMS value of the line current is

$$I_{L,RMS} = \frac{P_{OUT}}{\sqrt{3}V_{L\text{-}L,RMS}} = 16.3 \ A$$

The overvoltage factor is chosen

$$K = 1.14$$

hence

$$V_{CC,MAX} = 342 \text{ V}$$

The inverter switching frequency is chosen 24 pu since it has to be multiple of 6 for symmetry, hence

$$f_{SW} = 1440 \text{ Hz}$$

For this power level, the switch parasitic capacitor can be approximated by the following value:

$$C_S = 2.5 \text{ nF}$$

The dc bus snubber inductor L_S is chosen to provide

$$di/dt = 40 \text{ A/}\mu\text{s}$$

therefore

$$L_S = 7.5 \ \mu\text{H}$$

Finally, the on time of the auxiliary switch S_O needs to be for rated power (MI=1)

$$t_{ON,So} = 3 \ \mu\text{s}$$

The duration of mode 6 needs to be around 1 μs. Therefore, the gating signal of the auxiliary switch S_O is applied nearly 3.5 μs before the respective instant of the vertical edge of the carrier waveform and has the same frequency.

5.8 Simulated results

The proposed ZVS PWM VSI topology shown in Fig. 5-1 was simulated using a well-known electronic circuit simulation package [67].

Steady-state simulated waveforms for the *soft switching* inverter shown in Fig. 5-1

employing the proposed dc bus commutating subcircuit and the refined PWM scheme are shown in Fig. 5-8. The respective load power factor has been 0.8 (inductive). In particular, Fig. 5-8(a) shows the respective dc bus voltage. The dc bus voltage is reduced to zero after the auxiliary switch is turned off and some time before the vertical edge of the respective carrier waveform. During the time that the dc bus voltage is zero, inverter switches of the same leg are either turned on or turned off, with the respective delay time, under *soft switching* conditions (ZVS). As discussed before, the dc bus current becomes negative whenever the auxiliary switch is on. Fig. 5-8(b) demonstrates the current flowing through the dc bus snubber inductor L_s. Fig. 5-8(c) displays the inverter line-to-line voltage and Fig. 5-8(d) depicts the inverter output currents. Lastly, the spectrum of the inverter output waveforms, namely line-to-line voltage and line current are displayed in Fig. 5-8(e) and (f) respectively. Analysis of the waveforms confirms that inverter performance, namely the output harmonics are not affected by the proposed commutating process. Furthermore, it is clear that the proposed combination forms an effective ZVS PWM VSI topology.

5.9 Experimental results

To check the feasibility of the proposed ZVS PWM VSI topology, selected theoretical results were verified on an experimental prototype unit. The respective steady-state results obtained with the experimental set up are given in Figs. 5-9, 5-10, 5-11, 5-12. Specifically, Fig. 5-9 shows the dc bus voltage and the dc bus current. As predicted in the analysis section, the dc bus current becomes negative whenever the auxiliary switch is on. The dc bus voltage is clamped due to the storage-voltage clamp capacitor C_c. The dc bus voltage is reduced towards zero volts after the auxiliary switch is turned off. Fig. 5-10 shows the commutation process of the auxiliary switch S_o. As predicted this process is not

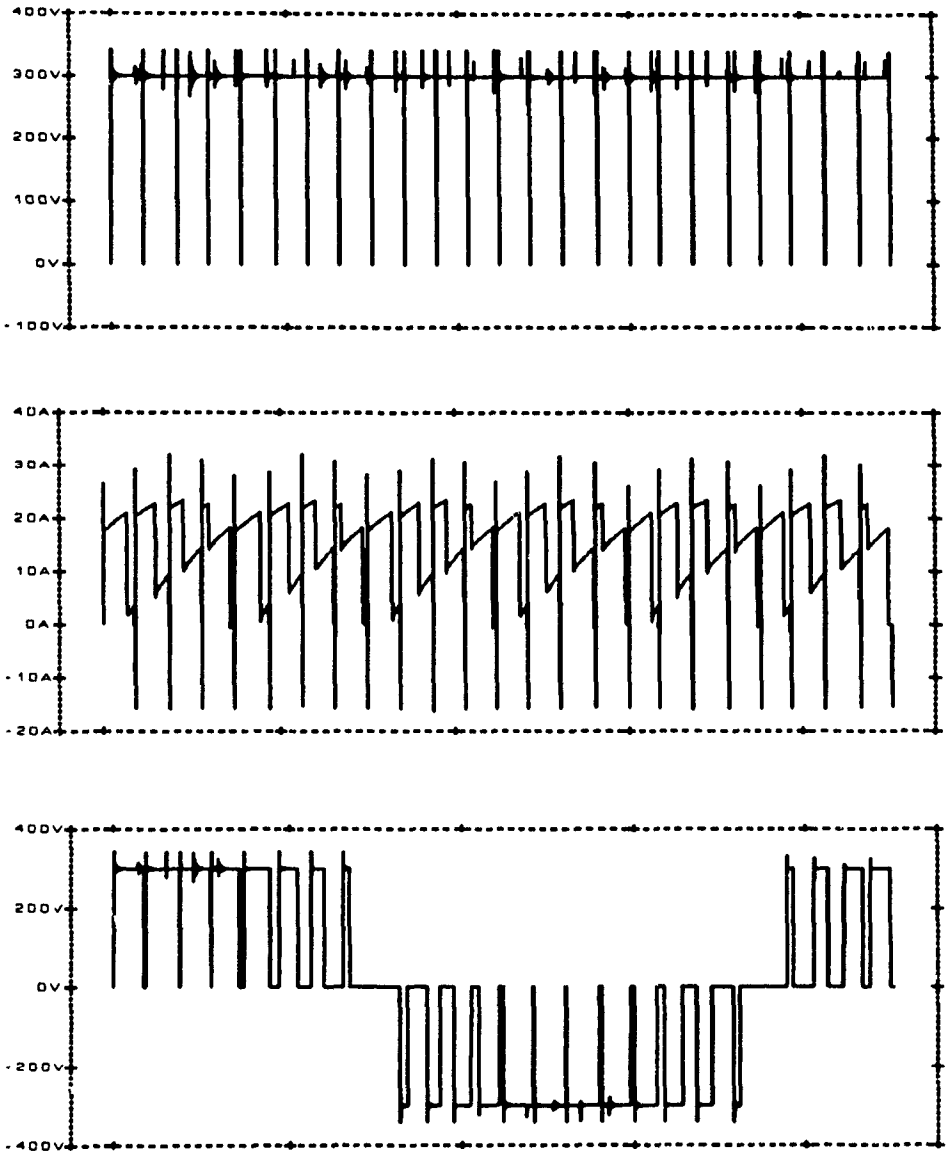


Figure 5-8: Typical steady-state simulated waveforms.

f_O = 60 Hz, f_{SW} = 1440 Hz, MI = 1, V_{IN} = 300 V, K = 1.14.

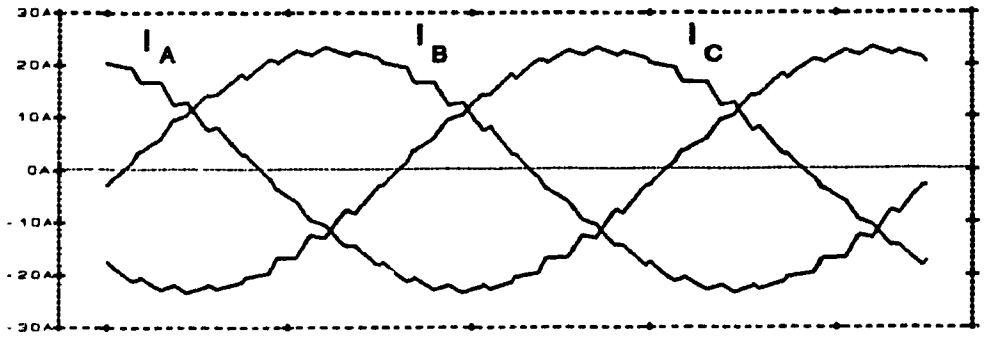
L_S = 7.5 μH, C_S = 2.5 nF, P_{OUT} = 6 kVA.

a) Dc bus voltage.

b) Dc bus current.

c) Inverter line-to-line voltage.

d)



e)

f)

Figure 5-8: Typical steady-state simulated waveforms.

f_O = 60 Hz, f_{SW} = 1440 Hz, MI = 1, V_{IN} = 300 V, K = 1.14.

L_S = 7.5 µH, C_S = 2.5 nF, P_{OUT} = 6 kVA.

d) Inverter line currents.

e) Spectrum of the line-to-line voltage.

f) Spectrum of the line current.

completely lossless and that is the most serious disadvantage of the proposed inverter topology. However, it can be said that the low voltage being commutated $(K-1)V_{IN}$ results in very low switching losses. Comparison between the simulated results depicted in Fig. 5-2 and the experimental waveforms (Figs. 5-9,5-10) reveals a close agreement. Furthermore, Fig. 5-11 shows the respective dc bus voltage and dc bus current for a complete cycle. The dc bus commutation process introduces zero volts intervals across the dc bus according to the carrier frequency and in synchronization with the vertical edge. Finally, Fig. 5-12 demonstrates the line-to-line voltage and the line current of the inverter. As predicted the operation of the dc bus commutating subcircuit introduces minimal distortion in the inverter output waveforms.

a)

b)

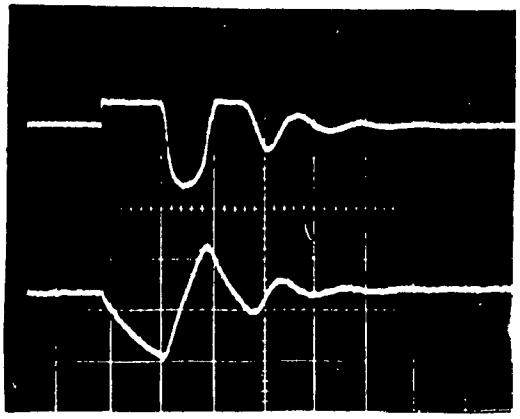


Figure 5-9: Experimental results - Dc bus commutating subcircuit operation.

L_s = 8 μH, C_c = 10 μF, MI = 1, P_{OUT} = 2 kVA.

a) Dc bus voltage (100 V/div, 5 μs/div).

b) Dc bus current (5 A/div, 5 μs/div).

a)

b)

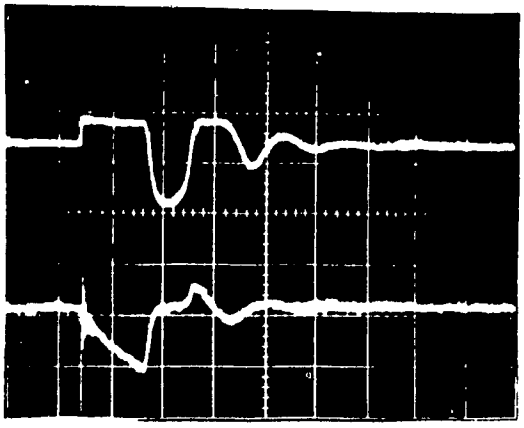


Figure 5-10: Experimental results - Dc bus commutating subcircuit operation.

L_s = 8 μH, C_c = 10 μF, MI = 1, P_{OUT} = 2 kVA.

a) Auxiliary switch voltage (100 V/div, 5 μs/div).

b) Clamp capacitor C_c current (5 A/div, 5 μs/div).

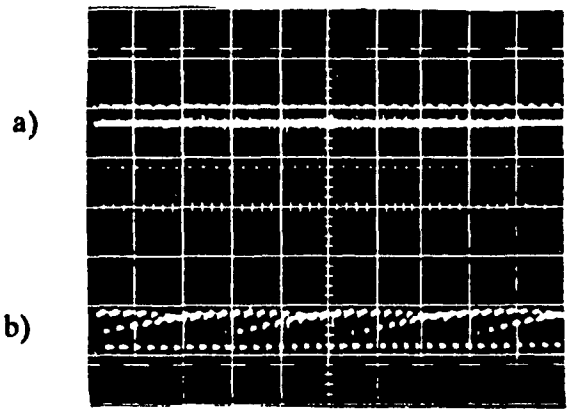


Figure 5-11: Experimental results - Inverter waveforms.

f_O = 60 Hz, f_{SW} = 3600 Hz, MI = 1, P_{OUT} = 2 kVA.

a) Dc bus voltage (100 V/div, 2 ms/div).

b) Dc bus current (10 A/div, 2 ms/div).

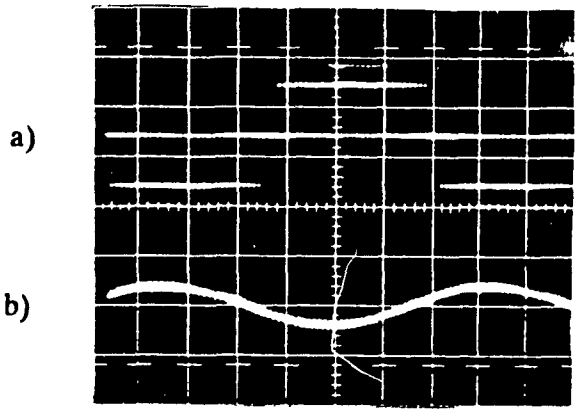


Figure 5-12: Experimental results - Inverter waveforms.

f_O = 60 Hz, f_{SW} = 3600 Hz, MI = 1, P_{OUT} = 2 kVA.

a) Line-to-line voltage (100 V/div, 2 ms/div).

b) Line current (10 A/div, 2 ms/div).

5.10 Conclusions

An optimum combination between a novel *notch* commutated inverter topology and a modulation strategy is proposed in this chapter. It is shown that this combination yields the required *soft switching* conditions at a lowest possible switching frequency. A significant additional advantage of the proposed ZVS topology is that the switching points of the dc bus commutating subcircuit are synchronized with the PWM technique. Specifically, the dc bus voltage goes through zero volts intervals according to the carrier frequency and only when is needed to prevent *hard switching* commutations. Finally, theoretical results have been verified by simulation and experimentally on a 2-kVA laboratory converter.

CHAPTER 6

SUMMARY AND CONCLUSIONS

6.1 Summary of the thesis

One of the more significant issues in static power converters, semiconductor switching losses, is extensively addressed in this thesis. Solutions, such as switch dissipative and improved snubber networks for pulse width modulated (PWM) converters are reviewed in Chapter 1.

Recent advances, in what are referred to as *soft switching* converter topologies, promise improved semiconductor utilization and substantially higher switching frequencies. These developments are presented in Chapter 2. The problems associated with these topologies are identified. It is concluded that the ideal converter topology should combine the best features of resonant and PWM of topologies. These features include low switching losses, constant frequency operation, reasonably rated reactive components and a wide range of control of load.

The proposed concepts are applied in Chapter 3, to a single-phase full-bridge high-power low-frequency PWM topology. One of the resulting topologies employs a low loss snubber network and the other one an improved lossless network. Both topologies provide zero current switching during turn-on and zero voltage switching during turn-off. Converter efficiency is improved, since, all the energy associated with snubber reactive elements is recovered.

In Chapter 4, a *soft switching*, namely zero voltage switching (ZVS), pulse width modulated (PWM) single-phase full-bridge medium-power high-frequency converter

topology is proposed and analyzed in detail. The various topological modes of the converter are identified. The proposed approach utilizes the switch parasitic capacitors to achieve zero voltage switching turn-off. The dc bus active snubber and clamping subcircuit ensures the prior conduction of the antiparallel diodes before the main switch turn-on. The effect of the drain-to-source parasitic capacitance associated with MOSFET technology and EMI problems are minimized. Design equations are provided. Simulated results are presented and verified experimentally.

In Chapter 5, a simple dc bus snubber subcircuit is investigated for *soft switching* three-phase PWM voltage source inverter. The operation of the dc bus commutating subcircuit is synchronized with an appropriate PWM technique. Inverter performance is improved since all commutations occur under *soft switching* environment. The PWM technique further reduces switching losses since 30% fewer switching points are obtained. A detailed analysis is presented and key theoretical results are verified by simulation and by experiment.

6.2 Conclusions

Some novel pulse width modulated topologies that provide a *soft switching* environment have been proposed and investigated in this thesis.

The single-phase full-bridge PWM topology employing the modified lossless snubber network (Chapter 3) is an attractive solution for high power applications when high frequency is required, since the proposed modified snubber network reduces switching losses. The energy associated with snubber reactive elements is recovered. The size of the converter is reduced since there is no dissipating resistor and the associated cooling requirements, as in the case of the low loss snubber network. However, this improvement

is obtained at the expense of one additional, but low power switch, switching at double the frequency of the main switches. Also, the VA ratings of converter components are slightly higher in the case of the lossless snubber network.

The single-phase full-bridge zero voltage switching topology proposed in Chapter 4 provides improved converter performance. The effect of the drain-to-source parasitic capacitor associated with MOSFET technology is eliminated. Specifically, the switch parasitic capacitors are discharged to the dc source, prior to the main transistor turn-on by means of one additional but low power switch. This switch has to be rated for the same voltage and current as the main inverter switches. The converter switching frequency can increase because of the ZVS feature, but the approach necessitates a low leakage inductance high frequency transformer. This transformer is difficult to manufacture, and, even with low leakage, high frequency ringing with the switch parasitic capacitors and parasitic capacitors associated with the diode rectifiers may occur. The auxiliary switch frequency is double the inverter switching frequency. This may introduce a limitation to the maximum inverter switching frequency attainable.

The three-phase inverter topology proposed in Chapter 5 provides improved converter performance due to the *soft switching* environment. The auxiliary switch frequency is equal to the inverter switching frequency. Unlike the auxiliary switch used in the single-phase converter based on the same dc bus subcircuit. The free-wheeling mode associated with the vertical edge of the carrier waveform ensures the charge of the storage-clamp capacitor. That means that no separate power source, as in the case of the actively clamped dc link inverter, is needed. The effect of the drain-to-source parasitic capacitor associated with MOSFET technology is minimized since zero voltage switching is achieved. The commutation of the auxiliary switch is not completely lossless but the higher the switching

frequency the more times that zero voltage switching is achieved even for this switch. The operation of the dc bus commutating subcircuit introduces limitations to switching frequency since a minimum time is required to activate the auxiliary switch.

6.3 Suggestions for future work

As a follow-up of the work carried out in the research project, the following areas could be further investigated:

- The power converter topologies discussed in Chapter 3 have been verified experimentally with BJT's. The same topology can be investigated using IGBT's. This approach has been studied in reference [15] without energy recovery subcircuits.
- A comprehensive comparison and evaluation between the topology proposed in Chapter 4 and the phase-shifted PWM topology reviewed in Chapter 2 can be performed.
- For the three-phase inverter topology proposed in Chapter 5, the effect setting the resonance frequency closer to the switching frequency can be studied. This is expected to minimize the problem of the commutation of the auxiliary switch, which is not completely lossless.

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