MOS

METAL OXIDE SEMICONDUCTORS

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ABSTRACT

Interest in the semiconductor memories has grown rapidly the past few years. The main reason for this interest is the increasing number of applications. It is now generally agreed that semiconductor memories will comprise a growing fraction of the computer memory.

Computer memory is the most obvious area of application for semiconductor memories. However, many other applications become apparent as low-cost semiconductor memories become available. Growing areas of application are desk and pocket calculators, minicomputers, peripheral controllers for computer sustems, manufacturing control equipment, communication systems and electronic watches.

The pace of development has been sutch that many potential users have difficulty anticipating the direction and rate of future progress. Systems designers must anticipate the characteristics of components well in advance in order to arrive at competitive new designs.

C. D. ADAMOPOULOS

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SYMBOLS AND ABREVIATIONS

MOS : Metal Oxide Semiconductors

PMOS : P-channel MOS

NMOS : N-channel MOS

CMOS : Complimentary MOS

ROM : Read Only Memory

RAM : Rantom Access Memory

FET : Field Effect transistor

IGFET : Insulated Gate Field Effect Transistor

MOSFET : Metal Oxide Semiconductor FET

IC : Integrated Circuit

LSI : Large Scale Integration

TTL : Transistor Transistor Logic

DTL : Diode Transistor Logic

CPU : Central Processing Unit

SOS : Silicon On Sapphire

Class 100 : When we have 100 particles of size less than 1μ per cubic foot.

V_G : Gate Voltage

V_D : Drain Voltage

I_D : Drain Current

V_{DS} : Drain to Source Voltage

V_{GS} : Gate to Source Voltage

V_T : Threshold Voltage

C_{OX} : Capacitance per unit area of the oxide

T_{OX} : Width of the inversion layer

C_O : Permitivity of free space

C_{OX} : Permitivity of the oxide

K_{OX} : Dielectric constant of the oxide

C_{GD} : Gate to drain capacitance

C_{GS} : Gate to source capacitance

C_{DS} : Drain to source capacitance

C_D : Depletion layer capacitance

C_G : Gate capacitance

INTRODUCTION

As late as 1960 transistors were packaged in individual containers varying in size upward from 0.2 inches. To construct a complete electronic circuit, individual transistors had to be linked together with other components, such as resistors, capacitors, diodes and other transistors. About 1960 methods were developed to combine most of the components of a circuit on a single crystal wafer of silicon to form an integrated circuit.

The highest component densities on integrated circuits are achieved by the fabrication technology called MOS, which stands for metal oxide semiconductors. The MOS technology produces transistors of the unipolar type in contrast to earlier double junction transistors which are bipolar. Unipolar transistors use majority carriers only, either electrons or holes but not both.

The objective of this technical report is to describe the MOS devices, clarify their principle of operation, produce an up to date evaluation of the existing devices and discuss their advantages and limitations.

1 GENERAL MOS

Although MOS technology is considered relatively new in the semiconductor world, the basic concepts of the IGFET (Insulated-Gate Field Effect Transistors), commonly called MOS or MOSFET type transistors, predate the bipolar transistor. Only through the comparatively recent development of stable predictable and high yield manufacturing process has MOS become reality in LSI (Large Scale Integration) form. Prior to this development, poor control and lack of complete understanding of solid state surfase conditions resulted in low yields and unstable electrical characteristics. The technology and application of IGFET have been reviewed recently by J.T. Wallmark and H. Johnson[1]

Initial attempts to realize active solid state transistors that operate on the field effect principle, were made by J.E. Lilienfield and O. Heil in the early 1930[2]. The first working model of the principle was developed at Bell Telephone Laboratories in 1948 by J. Bardeen and W.H. Brattain[3]. They observed the field effect principle during a series of experiments in which they attempted to modulate current through point contact and bipolar junction transistors. Attention was then focused on these two types of bipolar transistors and the development of the field effect transistor was halted. In 1952 W.B. Shockley[4] published the theory of the field effect transistor and a practical form of the device was built by G.C.Dacey and I.M. Ross in 1953[5].

This device used an electric field to control conduction in a germanium semiconductor structure. Early attempts to fabricate MOSFETs were unsuccessful due to lack of controlable and stable surfaces.

During the 1950's silicon began to supplant germanium as the preferred material because of its stability over a greater range of temperatures, its higher voltage breakdown,and because of promised better manufacturing control and hence better yield and lower cost. A body of knowledge about the surface properties of silicon was developed rapidly, along with fabricating techniques for highly stable structures in which the interface properties between silicon and silicon dioxide were better understood. The IGFET has also been made on various semiconductors such as Ge[6],Si[7], and GaAs[8], using various insulators such as SiO_2, Si_3N_4 and Al_2O_3.

A major breakthrough in semiconductor process occured in the early 1960[9] with the development of the silicon planar process. The planar process depends upon the fact that a layer of silicon oxide on the surface of a semiconductor slice will prevent the diffusion of certain dopant elements into the semiconductor. Thus patterns of oxide can be used to control the locations of diffused regions. The name "planar" comes from the fact that all three regions-emiter, base and collector-come to the surface of the device, which makes possible large scale integration.

Process control problems continued to plug the MOS manufacturing until 1967. At that time the yield of MOS type circuits with stable performance characteristics was increased through refinements in the basic MOS process in conjunction with tightened process control and institution of strict, class 100 clean room environments at critical process steps. Since then, yields have continued to rise as a result of manufacturing experience and development of better production equipment, tools and row materials. The silicon suppliers have not only produced high quality silicon wafers, but have also produced the larger diameter wafers (2 to 3 inches) to reduce manufacturing costs. Better wafer fabrication equipment, such as that needed to provide high accurary required in the sequence of photomasking operations, has also become available.[10]

In addition to the general upgrading of the quality and capability of the manufacturing materials and equipment, knowledge of semiconductor surface phenomena has increased greately, resulting in improvement at various critical process steps. Another factor that helped sustain the rise in yield was the development of circuit design techniques to take better advantage of the unique character of MOSFETs. These techniques generally tented to reduce circuit and array size with no loss in performance. Then in the late 1960s, computers were to control the generation of artwork and photomasks thus providing more uniform tooling and usage of proven predesigned circuits.

2. FIELD EFFECT TRNSISTORS (FET)

2.1 General

The basic building block of a MOS type integrated circuit is the field effect transistor, which is based on the lateral conductance within a silicon crystal by an electric field applied at right angles to the surf ce of the silicon. The junction or bipolar transistor, on the other hand,consists of two junctions formed within the body of a single crystal of silicon. The two junctions separate three regions called the emmiter, the base and the collector. The flow of current from the emmiter to the collector is controlled by changes in the signal applied to the base.

2.2 The FET Principle

Since p-channel MOSFET is the most widely used of the basic MOS technologies, the p-channel MOSFET will be used to illustrate the FET principle. A cross section of MOS transistor is shown in Fig 2-1. It is made up as follows: A thin slice (8 to 10 mils) of lightly doped n-type silicon material, called a wafer,serves as the substrate or body of the MOS transistor. Two closely spaced (10 to 20 μm) p-type regions, the source and the drain, are formed within the substrate by selective diffusion using the planar technique. A thin (1000 to 2000 A^0) layer of insulating silicon dioxide (SiO_2) is grown over the surface of the structure, and holes are cut into the oxide layer, allowing contact with the source and the drain. Then a

thin layer of metal called the gate is overlaid covering the area between the source and the drain regions. Simultaneously metal contacts are made to the source and the drain through the holes cut into the oxide layer, Fig. 2-1. The area between the source and the drain is called the channel and the contact to the metal above the channel area is the gate terminal. The chip area of a MOSFET is 5 square mils or less, about 5 percent of that required by a bipolar junction transistor.[11]

The gate of a MOSFET serves as the control element creating, when properly biased a conduction path or channel between the source and the drain regions as shown in Fig. 2-2. When a negative voltage is gradually applied at the gate, electrons are driven away from the interface of the oxide and silicon under the gate, and a positive charge is induced. With a sufficiently negative gate voltage, an inversion occurs that changes a very thin region of the silicon under the gate N-type (with electrons) to p-type (with holes), Fig. 2-2. The converted region is called p-channel and provides a conduction path for holes.

If a negative voltage is applied to the drain, current will flow from the source to the drain through the channel. The gate voltage controls the amount of the current. The higher the voltage (more negative) the higher the current. The minimum value of gate voltage just sufficient to cause channel formation is known as the gate threshold voltage and is given by the equation: 2-1

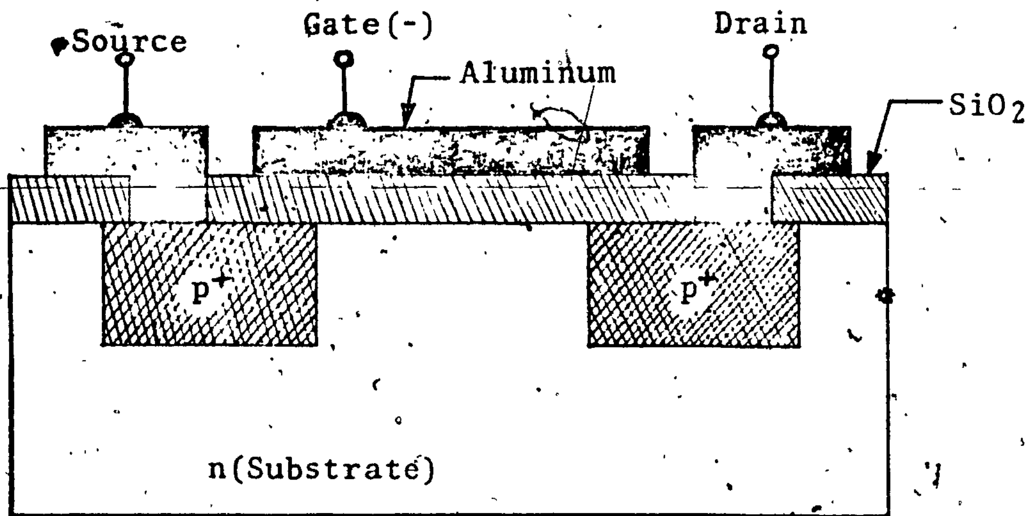


Fig. 2-1

P-Channel MOSFET before channel formation (cross section)

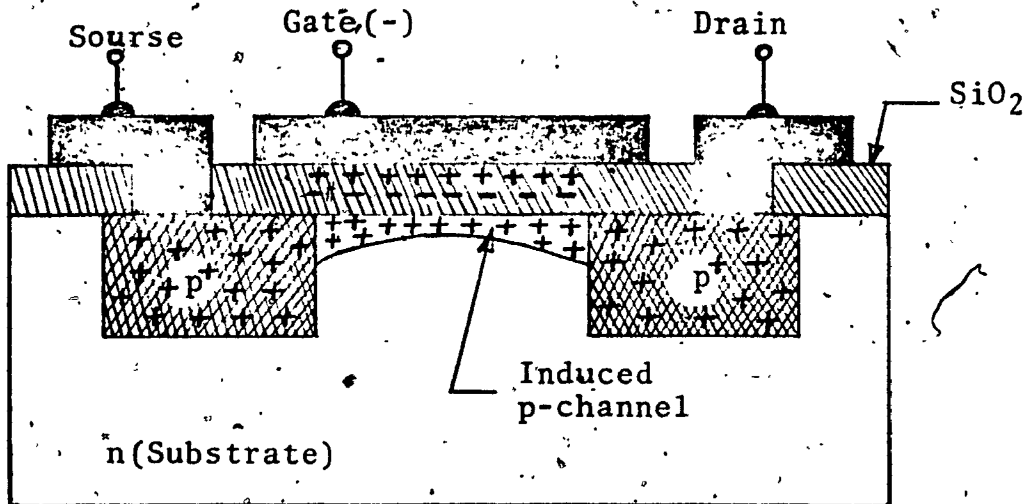


Fig. 2-2

Enhancement in a p-type MOSFET (cross section)

$V_T = 2\psi_0 + \frac{\sqrt{2\varepsilon_s e N_A 2\psi_0}}{C_i}$ where $C_i = A\,\frac{\varepsilon(ox)}{t(ox)}$. The threshold (where C_i dielectric constant, t_{ox} width of inversion layer) voltage is dependent upon the particular manufacturing, doping concentration, dielectric thickness and the crystal lattice orientation, of the silicon ingot from which the wafer is sliced. Above the conduction threshold(more negative) the gate voltage enhances the channel charge between the source and the drain thereby increasing the channel conduction. Such devices are called enhancement-type MOS devices.

If the drain voltage is increased (more negative) while the gate voltage remains constant, provided it is equal or more negative than the threshold voltage, the current from the source to drain increases. Eventually it reaches a point at which the current remains the same regardless of the increase of the drain voltage. This point is called pinch-off point.

2.3 The Depletion MOSFET

It is also possible to built a transistor in which a channel of the same polarity as the source and the drain exists without a bias on the gate. This is done by diffusing a channel between the source and the drain, with the same type of impurity as ussed for the source and the drain. Such a structure is shown in Fig. 2-3.

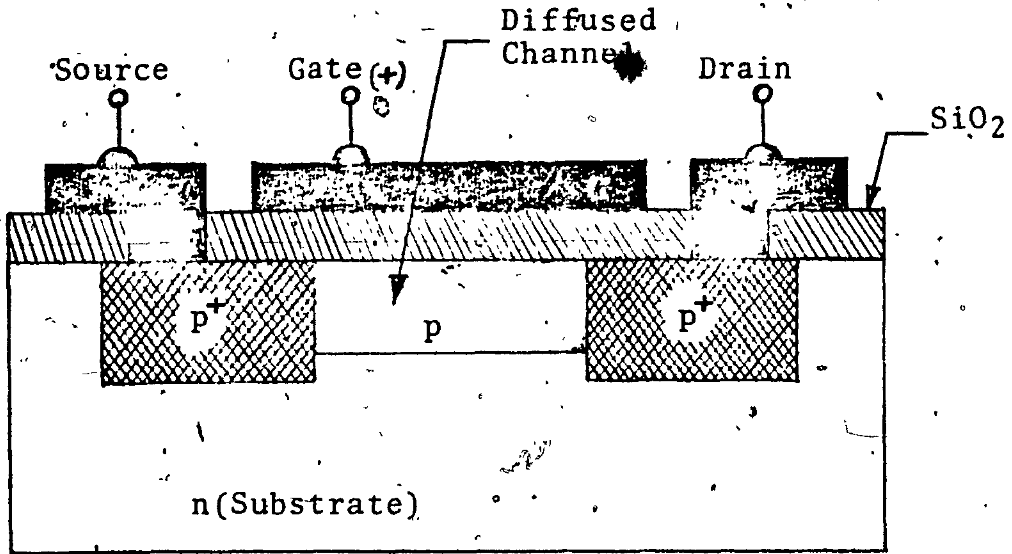


Fig. 2-3
A p-channel depletion type MOSFET.

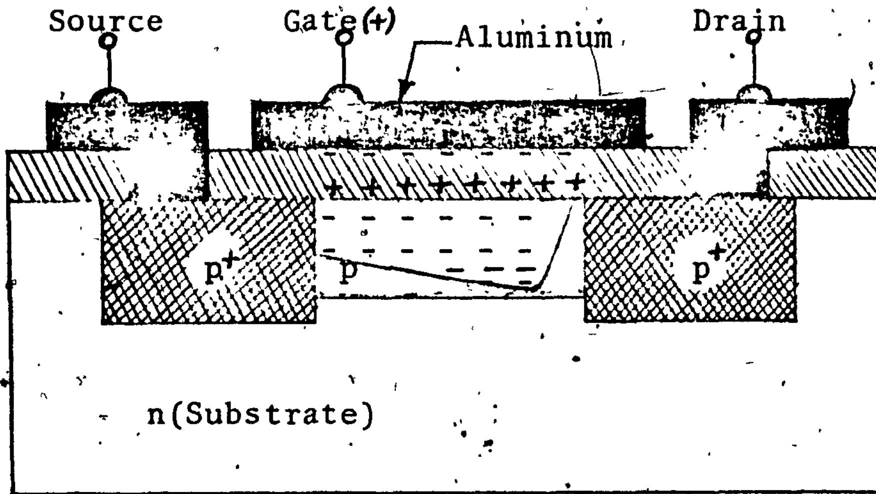


Fig. 2-4
Channel depletion with the application of positive gate voltage.

In this device an appreciable drain current I_{DSS} flows for zero gate-to-source voltage $V_{GS}=0$. This structure has been made with an p-type diffusion between the source and the drain regions. In this type of transistor, conduction decreases as positive gate voltage is applied. When the gate voltage is made positive, negative charges are induced in the channel, Fig. 2-4. Since the current in an FET is due to the majority carriers (holes for p-type material), the induced negative charges make the channel less conductive, and the drain current drops as V_{GS} is made more negative. The redistribution of charge in the channel causes an effective depletion of majority carriers, thus the name Depletion MOSFET. Note that the region near the drain Fig. 2-4 is more depleted than near the source because of the voltage drop due to drain current[11].

2.4 Comments

MOS integrated circuits are simpler than bipolar integrated circuits because bipolar circuits require at least two more masking steps plus a number of additional operations, such as oxide deposition, etching, alloying etc. as we shall see in chapter 4. It has been this basic simplicity, with the promise of very low cost, that has spurred work on MOS structures and processes. MOS transistors differ significantly from junction transistors in operating principles. MOS transistors can be used to advantage in many circuits because their properties are similar to those of vacuum tubes.

Their output response varies almost linearly with input and they have a high input impedance because of the layer of SiO_2 which results in an input resistance of 10^{10} to 10^{15} ohms. In contrast, bipolar transistors, which are current operated rather than field-effect devices, are quite non linear and have a much lower input impedance. The high impedance of MOS transistors makes it simpler to drive a large number of successive circuit stages and thereby to design more complex integrated circuits than with bipolar transistors.

3. OPERATING CHARACTERISTICS AND CIRCUIT SYMBOLS

The operating characteristics of the Enhancement MOSFET will be considered first followed by the characteristics of the Depletion MOSFET.

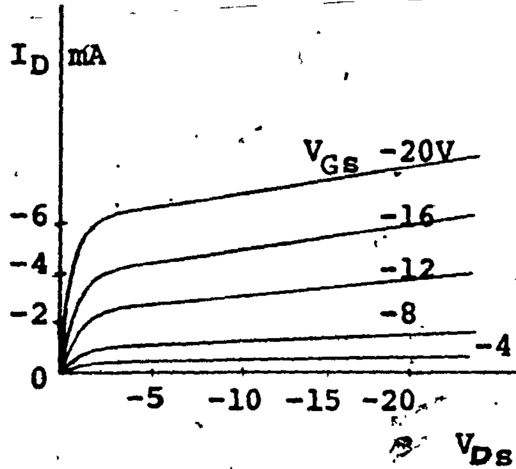
3.1 Enhancement MOSFET

The volt-ampere drain characteristic curves of a p-channel enhancent-mode MOSFET may be plotted using the gate voltage V_{GS} as the control variable, Fig. 3-1a. Its transfer curve is shown in Fig.3-1b. As it is shown from the transfer characteristic curve the current I_D (drain current) at $V_{GS} \geq 0$ is very small, of the order of few nanoamperes. As V_{GS} becomes more negative the current I_D increases slowly at first and then rapidly. The value of V_{GS} at which I_D reaches some defined value say 10μA, is called V_T or threshold voltage. The value of V_T for the standard p-channel MOSFET is typically -4 volts, and it is common to use a -12 volts power supply for the drain. However this power supply voltage is incompatible with the 5V power supply used in bipolar integrated circuits. In general a low threshold voltage allows:

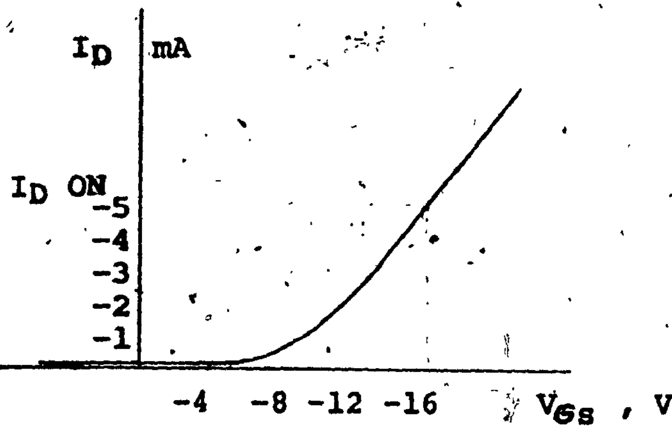
a) The use of small power supply voltage.

b) Campatible operation with bipolar devices.

c) Smaller switching time due to the smaller voltage swing required during switching.



a) The volt-ampere drain characteristics of a p-channel enhancement type MOSFET



b) The transfer curve (V_{DS}=10 V.) of a p-channel enhancement type MOSFET

FIG. 3-1

There are many methods used to lower the magnitute of threshold voltage V_T. The first method uses a silicon crystal lattice orientation in the ⟨100⟩ direction. It is found that in this orientation the V_T is one-half that of ⟨111⟩ crystal lattice orientation. The second method is to use a layer of silicon nitride Si_3N_4 and SiO_2 instead of SiO_2 alone. In this structure the dielectric constant is about twice that of SiO_2 alone and reduces V_T to about 2 volts. The third method is to use polycrystaline silicon doped with boron as the gate electrode instead of aluminum. This reduces the contact potentials between the gate electrode and the gate dielectric which in turn reduces V_T. The device produced with such a method is called silicon gate MOS. As it can be seen from equation 2-1 and graph Fig.3-2, V_T depends also on semiconductor doping density and insulator thickness. Fig. 3-2 shows a graphical presentation of the dependance of threshold voltage on the doping density and insulator thickness for a $Si-SiO_2$ system.

3.2 Depletion MOSFET

Depletion mode MOSFET. The depletion type MOSFET may also be operated in an enhancement mode. If we apply a positive gate voltage Fig.2-3, negative charges are induced into the p-type channel. Since the current in an FET is due to the majority carriers (holes for an p-type material), the induced negative charges make the channel less conductive, and the drain current drops as V_{DS} is made more positive.

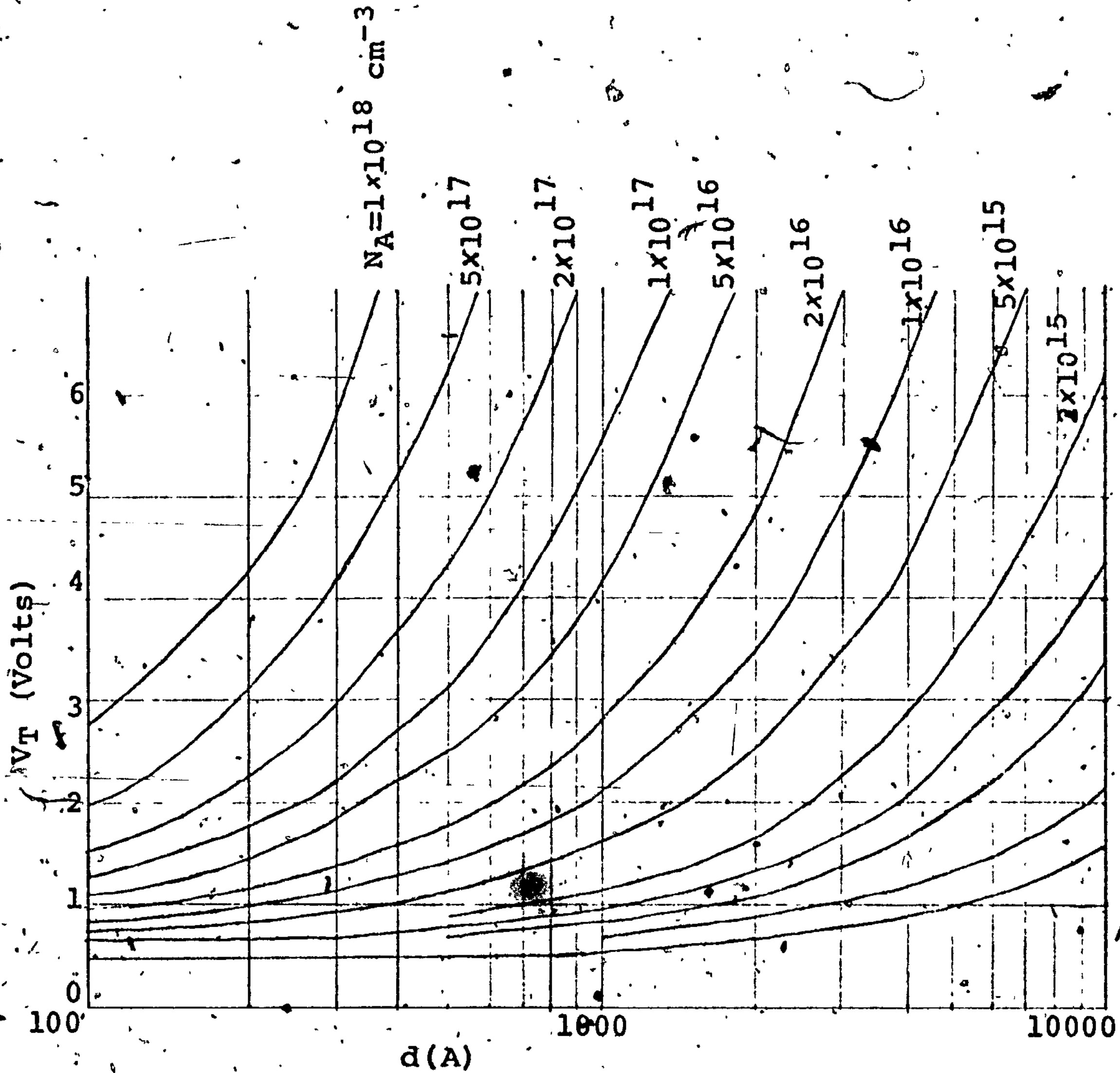


FIG. 3-2

Turn-on voltage as a function of thickness of the SiO_2 layer for various Si substrate dopings.[12]

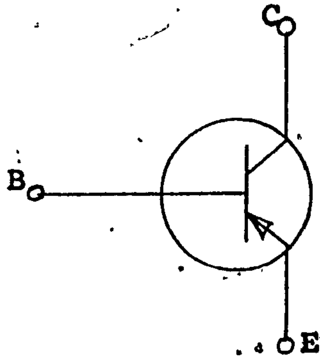
The redistribution of charge in the channel causes an effective depletion of majority carriers, which accounts for the designation depletion MOSFET.

3.3 Symbols

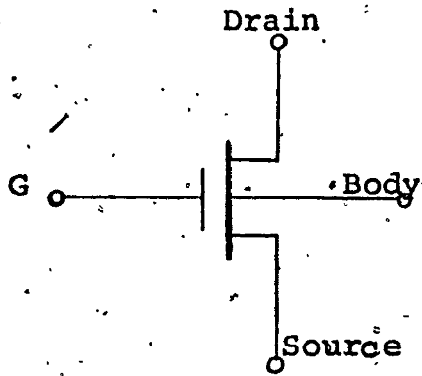
The MOS and bipolar transistor symbols are compared in Fig. 3-3. The MOS device may also be represented by two diodes and a control plate in the " OFF " state. The source is the reference terminal and by convention is positive with respect to the drain just as the emitter in the bipolar devices. The drain is the output terminal in the MOS device as it the collector in the bipolar device. The gate in the MOS device is the control terminal as is the base in the bipolar device. The gate is a metal plate isolated from the substrate by a thin oxide dielectric. The fourth terminal on the MOS device is the substrate often called the bulk or body.

In switching circuits it is desirable that the device is normally "OFF" therefore enhancement type MOS devices are mostly used. This means that a potential must be applied to the control element to cause conduction. The process has been described earlier.

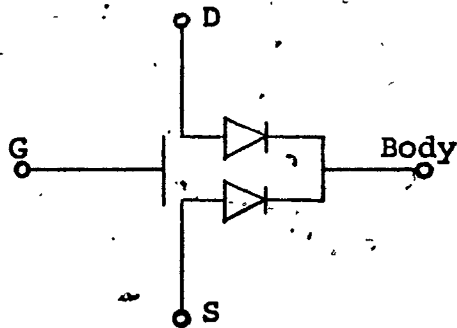
Fig. 3-4 shows the electrical symbols, the transfer characteristics, and output characteristics of the four types of MOSFETs, p-enhancement, p-depletion, n-enhancement and n-depletion, for purposes of comparison[12].



a) PNP Transistor



b) MOS Transistor



c) MOS device represented by two diodes and a control plate in the OFF state.

FIG. 3-3

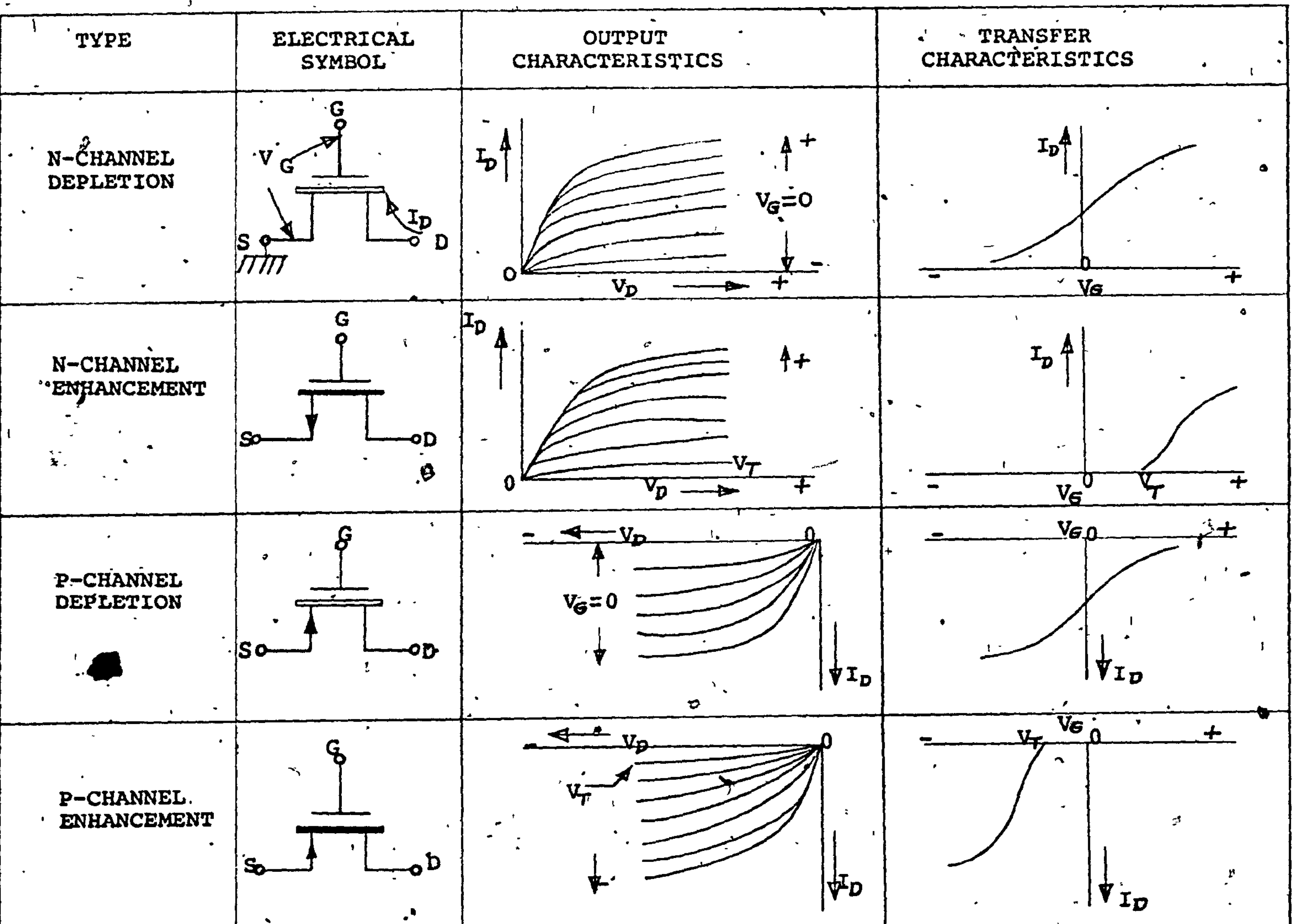


FIG. 3-4

Electrical symbols, output characteristics, and transfer characteristics of the four types of mosfets.[12]

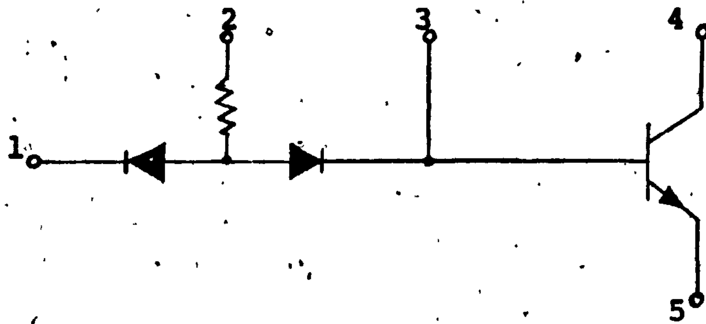
4. FABRICATION

4-1 General

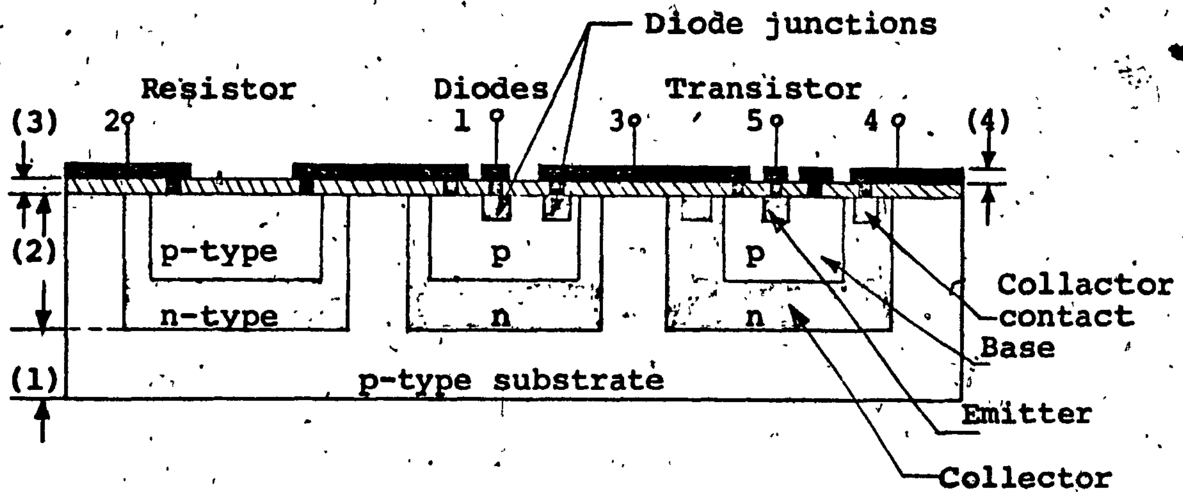
It was stated earlier that MOS integrated circuits are simpler than bipolar integrated circuits. To appreciate this , and as a comparison of the two technologies, the fabrication of bipolar I.C.s is also discussed here. The bipolar I.C. fabrication will be discussed first and then the MOS fabrication will follow.

4-2 Bipolar Fabrication

The basic structure of a bipolar integrated circuit comprised of one resistor, two diodes, and a transistor, is shown in Fig.4-1 and consists of four distinct layers of material. The bottom layer (1) (about 10 mils) is p-type silicon and serves as a substrate upon which the integrated circuit is built. The second layer (2) is thin ($\frac{1}{2}$ mil), (10μ) n-type material which is grown epitaxially as a single crystal extension of the substrate. All active and passive components are built within the n-type layer. A round silicon ingot with predetermined impurities, is sliced into wafers approximately 16 mils thick and each wafer is lapped and polished to eliminate surface imperfections. Once p-type silicon substrate is obtained, an n-type epitaxial layer, typically 10 μm thick, is grown on the substrate by Epitaxial Growth. The epitaxial process produces a thin film of single crystal silicon from the vapor phase upon an existing crystal wafer of the same material. The basic chemical



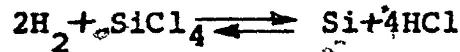
a) A circuit containing a resistor, two diodes, and a transistor.



b) Cross sectional view of the circuit above containing a resistor, two diodes and a transistor in integrated form. Bipolar I.C.

FIG. 4-1

reaction that describes the epitaxial growth of pure silicon is the hydrogen-reduction of silicon tetracloride.



$$2H_2 + SiCl_4 \rightleftharpoons Si + 4HCl$$

Since it is required to produce epitaxial films of specific impurity concentrations, it is necessary to introduce impurities into the silicon tetrachloride-hydrogen gas stream. A thin layer of SiO_2 is formed then over the entire wafer, Fig.4-2a, by exposing the epitaxial layer to an-oxygen atmosphere while being heated to about 100° C[11].

The second step in bipolar I.C fabrication is the Isolation Diffusion. But before that, it is required to selectively remove the SiO_2, to form the openings through which impurities will be diffused. This is done by photolithographic-etching process. First the wafer is uniformly coated with photoresist. Then the mask with the desired patern of openings is placed over the photoresist. By exposing the photoresist to ultraviolet light through the mask, the photoresist becomes polymerized under the transparent regions of the mask. The mask is removed and the wafer is developed by a chemical that dissolves the unexposed portions of photoresist, Fig.4-2b. It is then immersed in an etching solution of hydrofluric acid, which removes the oxide from the areas of the windows uncovered by the photoresist openings through which dopants are to be diffused. The portions of SiO_2 that are protected by the photoresist are not affected by the acid. The photoresist is then removed and it is ready for the isolation diffusion

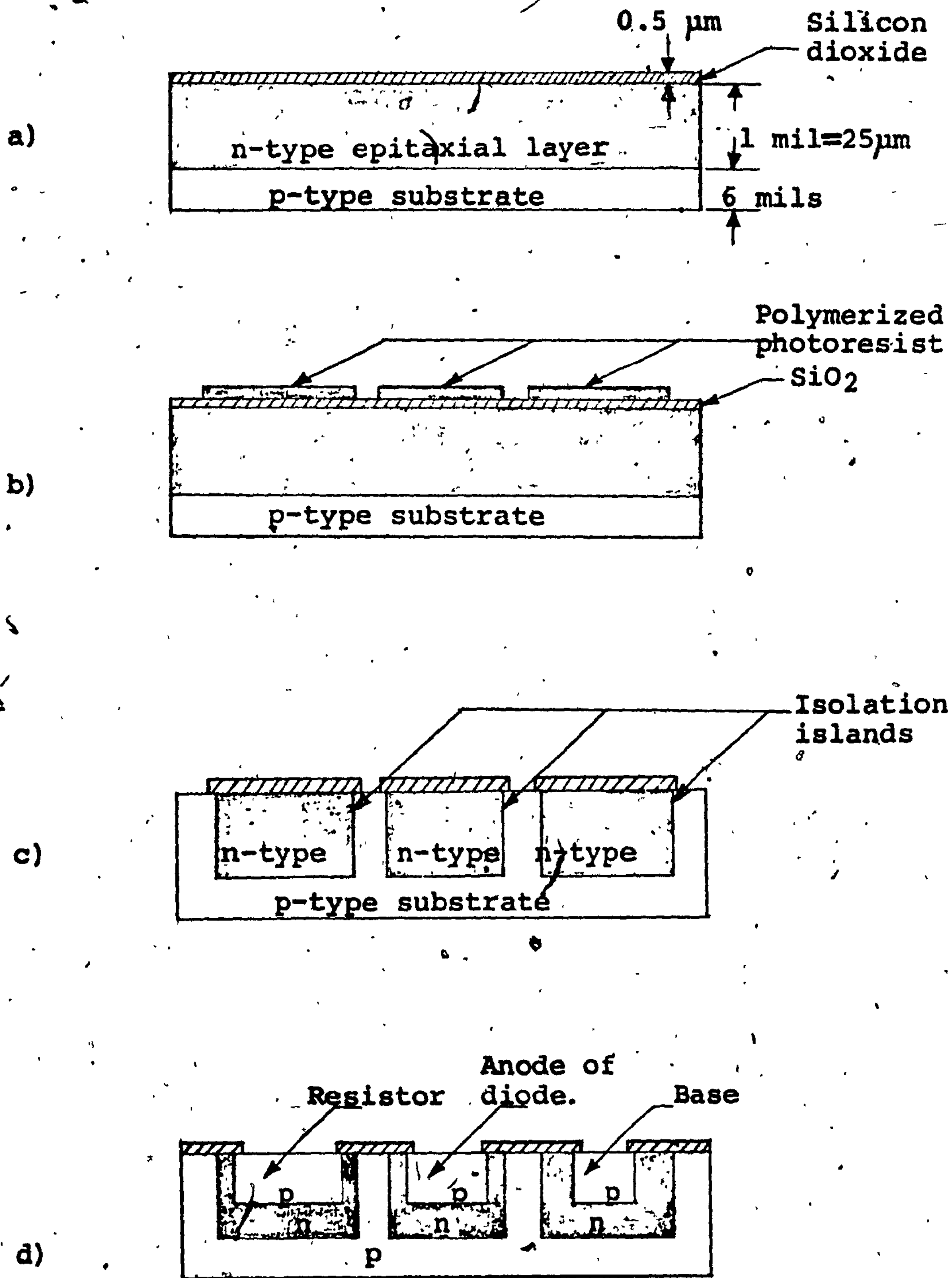


FIG. 4-2

The steps involved in fabricating a monolithic circuit.

a) Epitaxial growth; b) masking operation;

c) isolation diffusion; d) base diffusion.

Bipolar I.C.

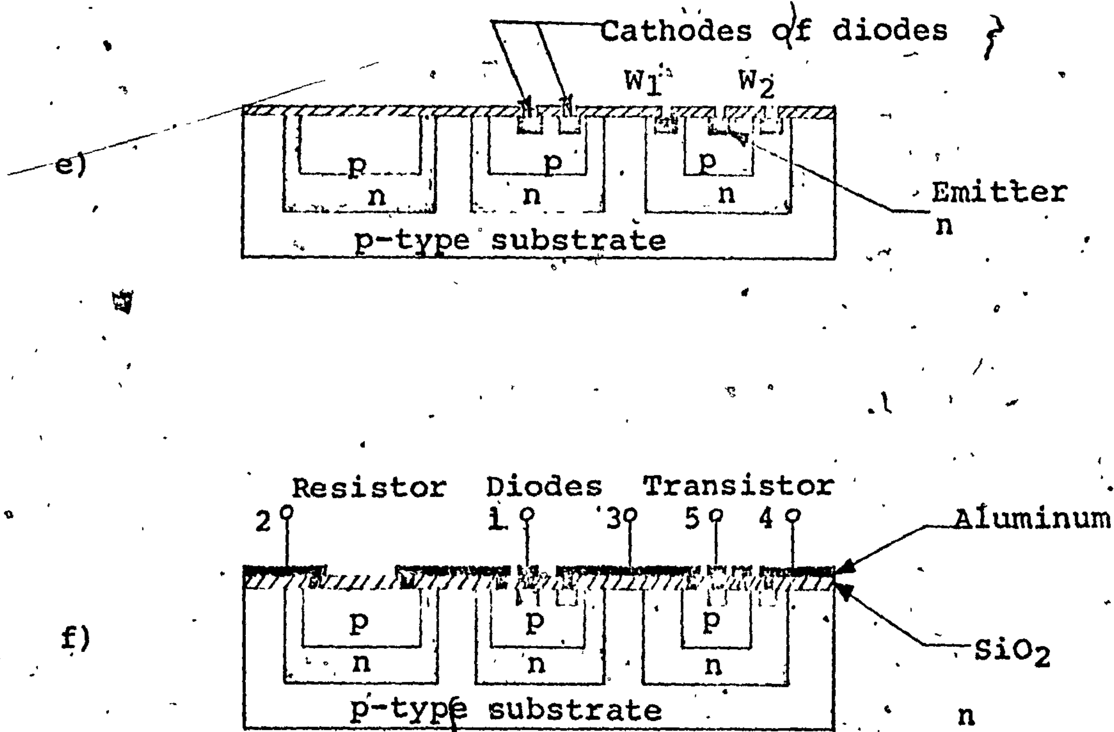


FIG.4-2

The steps involved in fabricating a monolithic circuit.

e) Emitter diffusion; f) aluminum metalization.

Bipolar I.C.

of acceptor impurities. The isolation diffusion lasts long enough to permit the p-type impurities to penetrate through the epitaxial layer and reach the p-type substrate, Fig.4-2c.

Base Diffusion. A new layer of oxide is formed. The photolithographic process is used again to create the pattern shown in Fig.4-2d. The p-type impurities are diffused through the openings of this pattern and are shown in Fig. 4-2d. In this way the transistor base regions, the resistors, anode diodes and junction capacitors are fopmed.

Emitter Diffusion. A new oxide layer is formed over the entire surface. The masking and etching operations are repeated to open windows in the p-type regions as shown in Fig. 4-2e. Through the openings n-type impurities are diffused for the formation of transistor emitters, and the cathode regions of diodes. Additional windows (w_1 and w_2) are often made into the n regions to which a lead is to be conneeted, Fig. 4-2e, for the lower resistance collector contacts.

Aluminum Metalization. To interconnect the various components of the integrated circuit a fourth set of windows is opened into a newly formed SiO_2 layer at the points where contact is to be made. After the windows are opened by photolithographic process, the interconnections are made using vacuum deposition of a thin even film of aluminum over the entire wafer. The photoresist technique is then applied again to etch away all undesired aluminum areas, leaving the desired pattern of interconnections only[11], Fig.4-2f.

The package leads are connected, after alloying the aluminium into the slicon, to the integrated circuit by stitch bonding of a 1 mil aluminum or gold wire from the terminal pad on the circuit to the package lead.

4-3 MOS Fabrication.

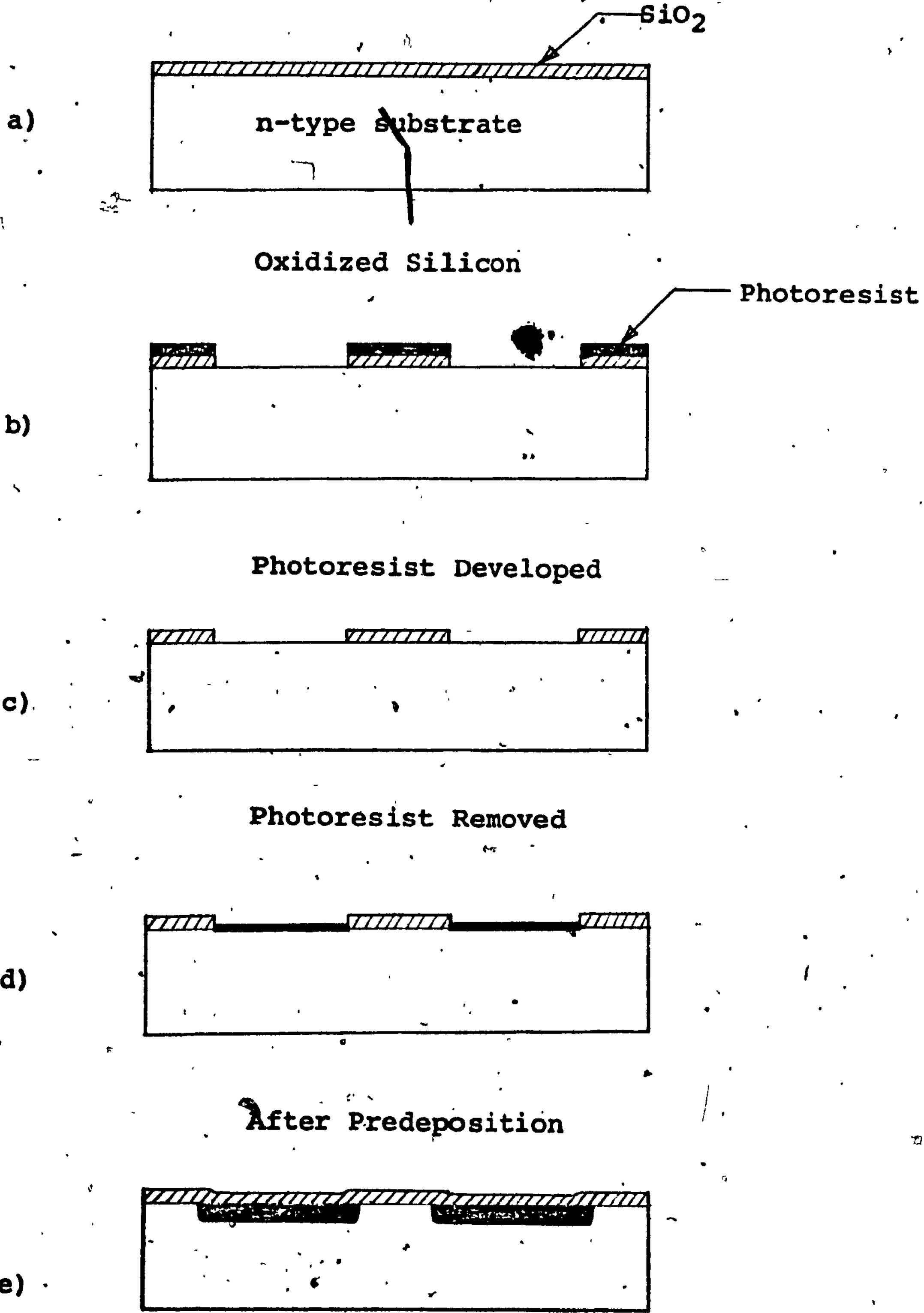
Since p-channel MOSFET is what we have been using in our discussion, the p-channel fabrication process will be described. The starting material for the p-channel processing is polished n-type lightly doped wafers in a resistivity range of 3 to 6 ohm cm, with ⟨111⟩ crystal orientation.[1] After the wafer is thoroughly cleaned, a masking (o.6μm) oxide is grown over its entire surface to serve as a mask against subsequent diffusion, Fig. 4-3a. The growing of the oxide by thermal oxidation is similar to the one already discussed in the bipolar fabrication.

After the oxidation we proceed with the first masking step which defines the source and the drain regions, Fig.4-3b. The kodak hoto Resist (KPR) KTFR, or KMER considered, is of the negative type and therefore it is soluble in certain liquid developers (i.e tricloroethylene) unless polymerized by exposure to ultraviolet light. The whole photolithographic-etching process for defining the source and the drain is identical to the one described for the bipolar device. After the photoresist is removed the wafer is ready for boron predeposition, Fig. 4-3c. The diffusion of dopants is usually accomplished by a two step process[12]. The first step called "predeposition", is used to introduce

dopant impurities to only a shallow depth in the oxide layer codeposited with the dopant on the silicon, Fig. 4-3d. The second step called "drive-in diffusion", diffuses the dopant impurities deeper into the silicon to the desired depth, in oxydizing atm. Fig. 4-3e. Predeposition is performed in a diffusion furnace typically in the temperature range of 1000° to 1000°c. Volative compounds of boron, such as diborane (B_2H6) and boron thrichloride (BCl_3) or liquid compounds, such as boron tribromide (BBr_3), are commonly used sources of boron predeposition.

The wafer is now ready for drive-in diffusion. The drive-in diffusion serves not only to diffuse the dopant impurities further into the silicon, but also to form a protective layer of oxide over the sensitive p-doped silicon, Fig. 4-3e.

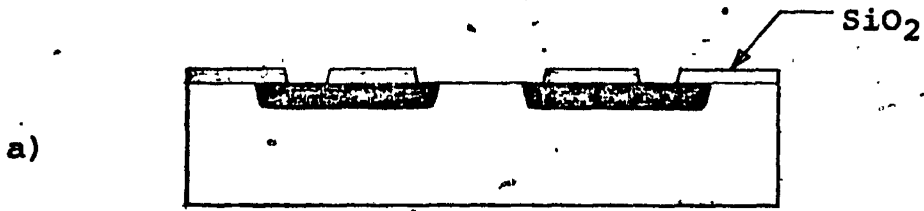
We are now ready for the second or gate masking step. The oxide layer is completely removed over the gate only and subsequently regrown to the final gate oxide thickness, 1000 A° maximum. The masking and etching operations are similar to the previous masking step, except that the alignment of the gate mask must be very precise, since the gate oxide region must extend to both source and drain. The tolerance for misalignment depends on intentional gate overlap and the amount of lateral diffusion of the source and drain.. After the completion of the etch and photoresist removal the wafer appears as in Fig.4-4a.



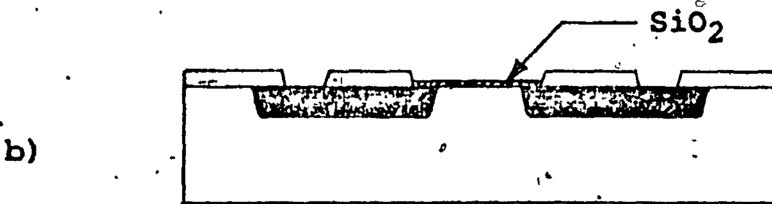
After p-region diffution-oxidation

FIG. 4-3

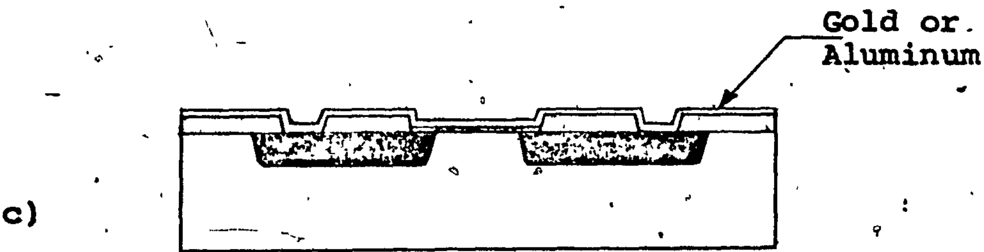
The process steps in MOS fabrication



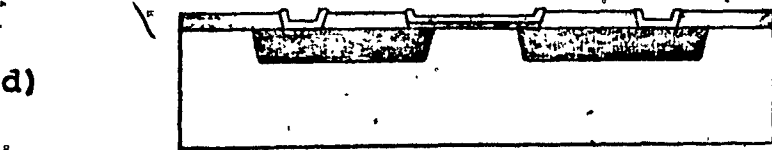
Second mask etched and potoresist removed



After gate oxidation



After metalization



Completed MOSFET

FIG. 4-4

The process steps in MOS fabrication

The gate oxidation step follows the gate masking step. Oxidation of this layer is usually done in a dry oxygen atmosphere. The gate oxidation step also simultaneously diffuses the junctions to their final depth. Since a thin layer of oxide is grown on the p-region contact areas at the same time, it must be removed. A third masking and etching operation completes this task[10], Fig. 4-4b.

We are now ready to apply metalization interconnect. Gold is the most common metalization used. By means of an electron beam evaporator ultrapure films on the order of 1μ thick are deposited, Fig. 4-4c.

A fourth masking step is used to delineate the interconnects and bonding pads. Precise edge definition and freedom from defects is necessary in this step. Otherwise shorts from metal bridging or opens from metal voids may result. After this masking step and optional oxide overcoat may be applied from protection against scratches. A fifth and final masking operation is required to create pad windows to remove this oxide from the bonding pad regions, Fig. 4-4d.

The MOSFET is now complete, after alloying the contacts into the silicon, and we can see that in its fabrication there is only one diffusion step and no epitaxial growth. In bipolar I.C.s on the other hand there are 4 diffusion steps and an epitaxial growth. The masking steps are approximately the same. It is therefore obvious that the MOS fabrication is simpler.

5. MOS RESISTOR

5.1 Resistor

An active MOS transistor can be operated as a load resistor by connecting the gate of the device to a constant supply voltage or by shorting the gate and drain together, Fig. 5-1. In either case the resistor will operate in the saturated region of the transistor characteristic curves. The variation of the resistance is small as compared with the non saturated region. The curves are nearly flat, Fig. 5-2, which means that a large change in drain voltage has little effect on the drain current. Since the oxide characteristics have been established to give the desired threshold voltage, the resistance is primarily a function of the devise geometry.[14]

The operating of a MOS resistor as the load of a simple inverter is shown in Fig. 5-1, while Fig. 5-2 shows the characteristics of the transistor combined with the resistor characteristics[13]. Q_2 acts as the inverter and Q_1 acts as the resistor. The inverter has two stable operating points:

1) When $V_G > V_T$, Q_2 is on and the output voltage is near ground since the drop across the transistor is negligible. The supply voltage, V_D, is dropped across the resistor and the resistor value is determined by the drain current through the resistor: $R=\frac{V_D}{I_D}$.

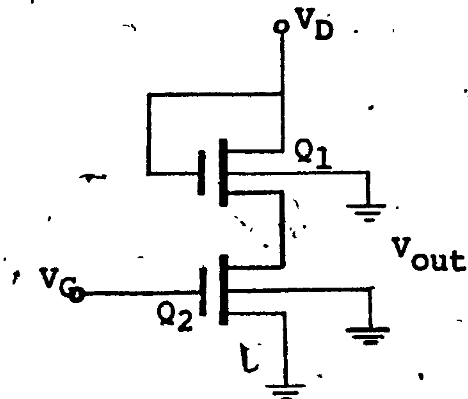


FIG. 5-1

An inverter circuit with a MOS transistor Q_1 operated as a load resistor.

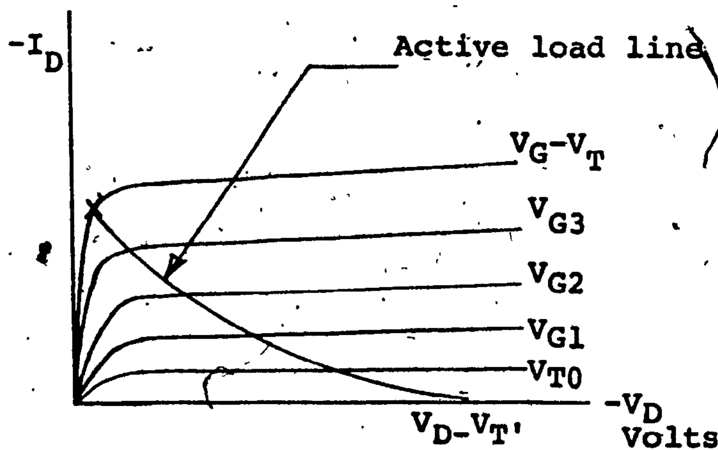


FIG. 5-2

Transistor and resistor characteristics of the circuit FIG. 5-1 combined.

2) When $V_G < V_T$. For this condition, the transistor Q_2 is turned "OFF" and the output voltage becomes $V_D - V_{T'}$ as shown in the characteristic curves FIG. 5-2, where $V_{T'}$ is modified threshold voltage of MOS resistor Q_1 due to source biasing. The current flowing through the resistor at this point will be leakage current only and the voltage drop will be $V_{T'}$.

6 MOS CAPACITANCE

6.1 General

As it was indicated in chapter 4 Fig. 4-4, the MOS transistor is made up of a silicon substrate covered with a thin layer of silicon dioxide, and on top of that the metal gate, usually alluminum. The electrical sandwich formed by the gate metal, the oxide and the substrate, forms the MOS capacitance.

The MOS capacitance is closely related to the intrinsic operation of the transistor. Accordingly, all the capacitances associated with the actual transistor are devided into two classes, intrinsic and parasitic.

6.2 Intrinsic Capacitance

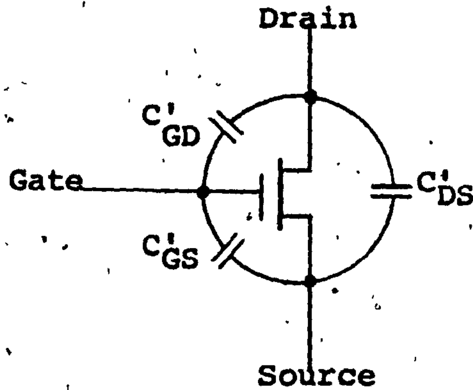
The intrinsic capacitances are associated with the charges stored on the gate electrode and in the channel itself. These capacitances are illustrated in Fig.6-1 and their values vary with voltage because the charge distribution on the gate and in the channel changes as the voltages change. Table 6-1 gives the range of values of these capacitances in the nonsaturation and saturation regions[15]. Cox is the capacitance per unit area of the gate oxide parallel plate capacitor and is expressed as:

$$Cox = \frac{\epsilon_{ox}}{t_{ox}} = \frac{K_{ox}\epsilon_o}{t_{ox}} \qquad \text{----- (6-1)}$$

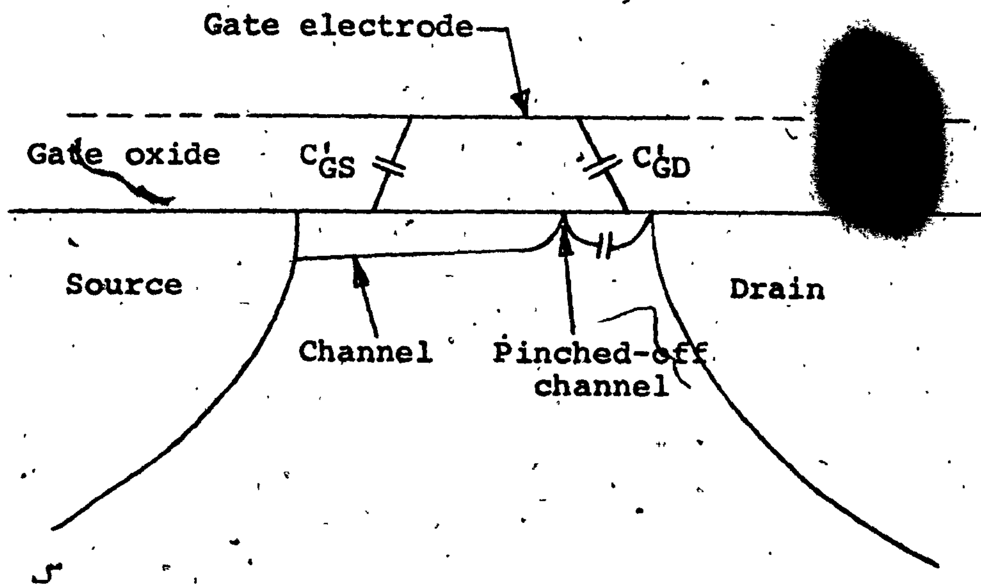
where: ϵ_{ox} = permitivity of the oxide

K_{ox} = dielectric constant of the oxide (=4 for SiO_2)

ϵ_o = permitivity of free space = 8.85×10^{-6} pF/μ



a) Schematic representation of intrinsic capacitance



b) Location of the intrinsic capacitance

FIG. 6-1

Table 6-1

Summary of Capacitance Values

Intrinsic Capacitance	Range of Values in the nonsaturation region	Value in Saturation region
C'_{GD}	0 to $\frac{1}{2} C_{ox}$	0
C'_{GS}	$\frac{1}{2} C_{ox}$ to $\frac{2}{3} C_{ox}$	$\frac{2}{3} C_{ox}$
C'_{DS}	0	0

t_{ox} = oxide thickness

In nonsaturation operation, the intrinsic gate to drain capacitance (C'_{GD}) and gate to source capacitance (C'_{GS}) will very anywhere within the ranges given in the table 6-1 depending on the bias condictions involved.

6.3 Small Signal Gate Capacitance.

The gate capacitance can be considered as a series connection of C_{ox} and a depletion layer capacitance C_d. Before discussing the gate capacitance let us define what we mean by depletion. The electrical condition of the silicon near the surface is described as being in accumulation, depletion, or inversion, according to whether the mobile charge density at the surface is greater than, less than, or opposite type to that in the bulk, respectively. So when the gate voltage is positive the silicon surface is strongly charged and the capacitance is that of a parallel plate capacitance with the oxide as the dielectric, $C_G = Cox$. (6-2)

When the gate voltage becomes more negative, a depletion layer begins to form under the gate region, starting as a very thin layer and gradually increasing in thickness, thus decreasing in capacitance. When the gate voltage approaches the threshold voltage, an inversion layer begins to form and the depletion layer no longer grows. The capacitance C [illegible] levels off at its minimum capacitance given by $\frac{1}{C_G} = \frac{1}{C_{ox}} + \frac{1}{C_d}$ (6-3).

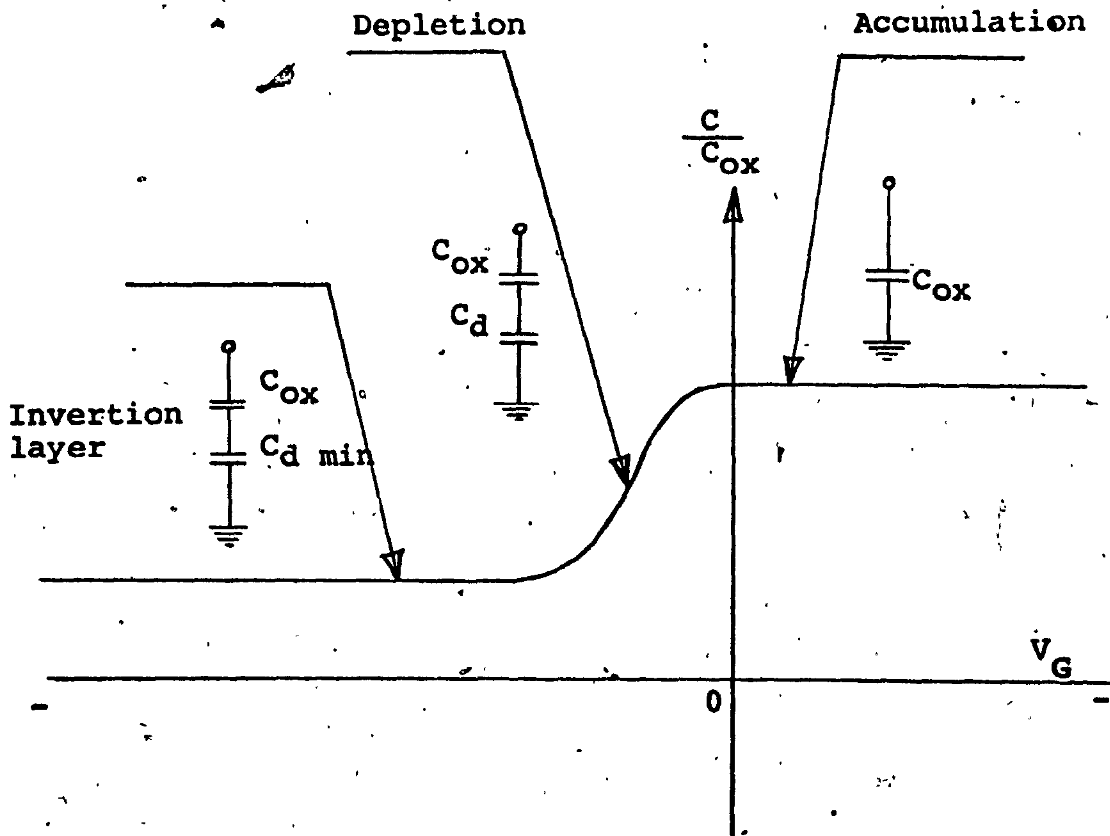


FIG. 6-2

Capcitance of MOS structure as a function of gate voltage. This is the small signal capacitance between the gate metal and the silicon substrate as a function of the gate to substrate voltage.

A curve representing the condition just described is give in Fig. 6-2 where :

C = capacitance per unit area.

C_{ox} = capacitance per unit area of the gate oxide parallel plate.

C_d capacitance of the depletion layer.

6.4 Parasitic Capacitance.

In addition to the intrinsic MOS capacitance, several other capacitances are important in determining the performance of the circuit. These are:

C_{MOS} Metal-thin oxide-silicon capacitance. Approximately 0.2 pF/mil^2. This is the capacitance that actually forms the transistor channel and is intrinsic to device operation.

C_P Junction capacitance, p-region to substrate. Approximately 0.1 pF/mil^2. Capacitance is a function of junction voltage. This is frequently one of the most significant of the parasitic capacitances.

C_M Metal over field capacitance. Similar to C_{mos} and approximately 0.02 pF/mil^2. C_M can become significan in chips with complex interconnections and large metal areas.

C_{MP} Metal-thic oxide p-region capacitance. Approximately 0.02-0.03 pF/mil^2. This is the capacitance that frequently contributes noise coupling from one signal to another in crossovers.

C_{MPT} Metal-thin oxide-p-region capacitance, approximately 0.2 pF/mil^2.

7. COMPARISON OF MOS PROCESSES

7.1 P and N - Channel MOS

The first commercial MOS integrated circuits were of the p-channel enhancement type (PMOS), and today PMOS circuits constitute about 80 percent of the total MOS market. The PMOS process was the easiest to control and therefore emerged as the first in volume manufacture. Because of this, PMOS has been the basis of the development of many MOS process variations. Initial work however was directed at producing N-channel transistors. The fabrication sequence for N-channel process is essentially identical to that for p-channel. The reason for selecting N-Channel, was the theoritical advantage of employing electron conduction vs hole conduction in silicon[10].

The problem with N-channel is the fact that most of the contaminants is MOS fabrication are mobile ions which are positively charged and are trapped in the oxide layer between gate and substrate. In an N-channel device the gate is normaly positive with respect to the substrate and, therefore, the positively charged contaminants are repulsed towards the interface between the SiO_2 and the substrate. The positive charge from these contaminants attracts free electrons in the channel which tends to make the transistor turn on prematurily. In p-channel devises, the positive contaminantions are attracted to the aluminum-SiO_2 interface by the negative gate voltage where they cannot effect the channel[11].

It was stated earlier that the theoretical advantage of n-channel over the p-channel was due to electron conduction versus hole conduction respectively. The electron mobility μ in the lightly dopped material is about 1300 cm^2 $volt^{-1}$ sec^{-1} while the hole mobility is $\approx$ 500 cm^2 $volt^{-1}$ sec^{-1}. Because of this the "ON" resistance of P-channel device is almost three times that of the N-channel. In other words, the P-channel device must have more than twice the area of the N-channel device to achieve the same resistance. Therefore N-channel MOS circuits can be smaller than P-channel devices. Since the operating speed is limited primarily by the internal RC time constants, and the capacitance is directly proportional to the junction cross sections, the N-channel MOS is faster in switching applications. However, there are more fabrication problems with the n-channel than with the p-channel, such as control of the threshold voltage, tendency of boron dopant in the p-type substrate to redistribute during thermal oxidation, difficulty in making good aluminum contact e.t.c.

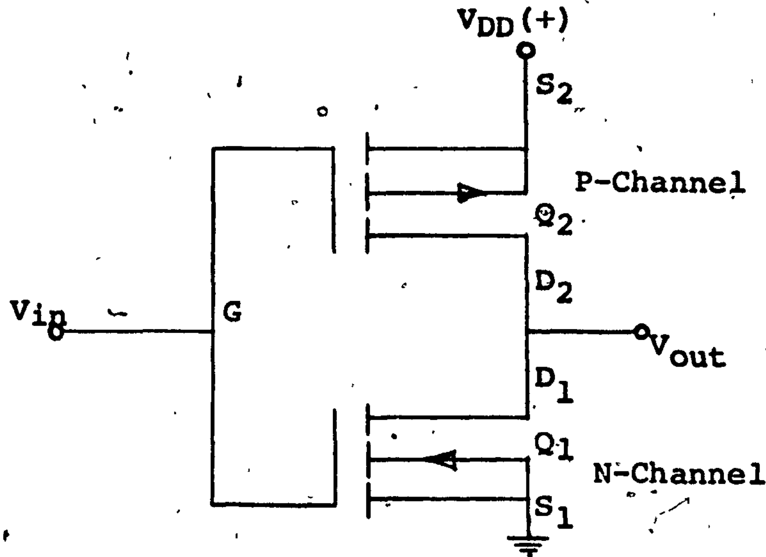
7.2 Complementary CMOS

The combination of PMOS and NMOS is used to produce the CMOS or complimentary MOS. With both channel types combined in one circuit it is possible to gain performance advantages over all other varieties of integrated circuits currently being manufactured.

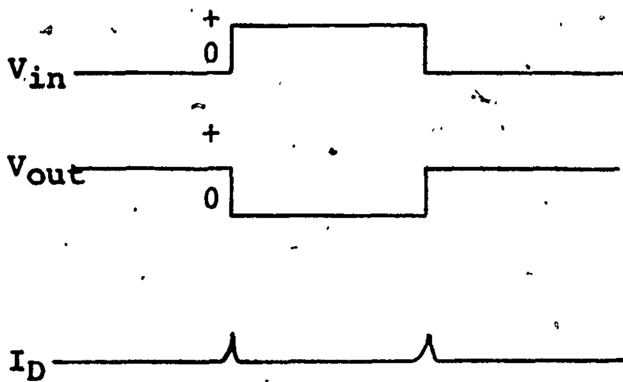
A basic CMOS circuit is the inverter, which consists of one p-channel and one N-channel transistor connected as shown in Fig. 7-1. The CMOS technology is the most sophisticated of the MOS processes. In the circuit shown, Fig. 7-1a, a low input signal means the N-channel transistor Q_1 is OFF and the P-channel transistor is ON (logic 1). The output is shorted to the positive supply, but virtually no load current is drawn if a similar high impedance MOS gate input is assumed as the load.

When the input signal goes high, ($V_{in} = +V_{DD}$), Q_1 is turned ON and Q_2 is turned OFF. THe output is pulled to ground, Fig. 7-1b, but no steady state current is drawn (logic 0). Power dissipation in the coplimentary MOS circuit (CMOS) is thus limited to the crossover conditions existing as the transition occurs from state to state. Proper device design for rapid turn-on and turn-off results in a dissipation factor as low as 2 nw per gate. The high noise immunity is also a direct result of the complimentary configuration, since two separate configurations must be crossed. This threshold is a direct function of power supply voltage and is typically 45% of the supply voltage[14].

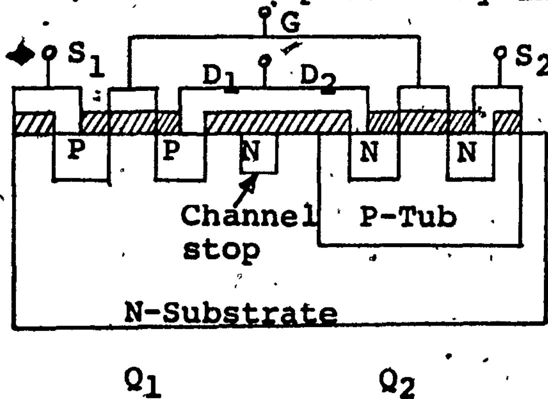
The CMOS circuit results in a more complex fabrication process. Fig. 7-1c, shows a cross section of the CMOS integrated circuit inverter. The P-channel device remains directly within the N-substrate. To form the n-channel device, however, a P-type "tub" must be created into which the device is placed.



a) Typical Coplementary Inverter



b) Input voltage, output voltage and output current waveforms, of the complementary inverter.



c) Typical cross section of cmplementary MOS inverter

FIG. 7-1

In addition channel stops must be placed between the "tub" and the P-drain to prevent channeling effects.

7.3 Some Applications.

The inverter just discussed is a highly effective digital switch with the lowest power consumption in either the "on" or the "off" state of any semiconductor device. By interconnecting a number of inverter stages one can built a variety of useful circuits with extremely low power consumption. This property makes CMOS circuits preferred for any application where the power supply is limited, like the battery powered devices.

A p and n-channel pair can also be connected in parallel with the power supply to form a transmission switch that can handle both digital and analog signals in either direction. It is possible to make such a switch with a complementary pair of bipolar transistors, but such a circuit is too costly to be commercially useful.

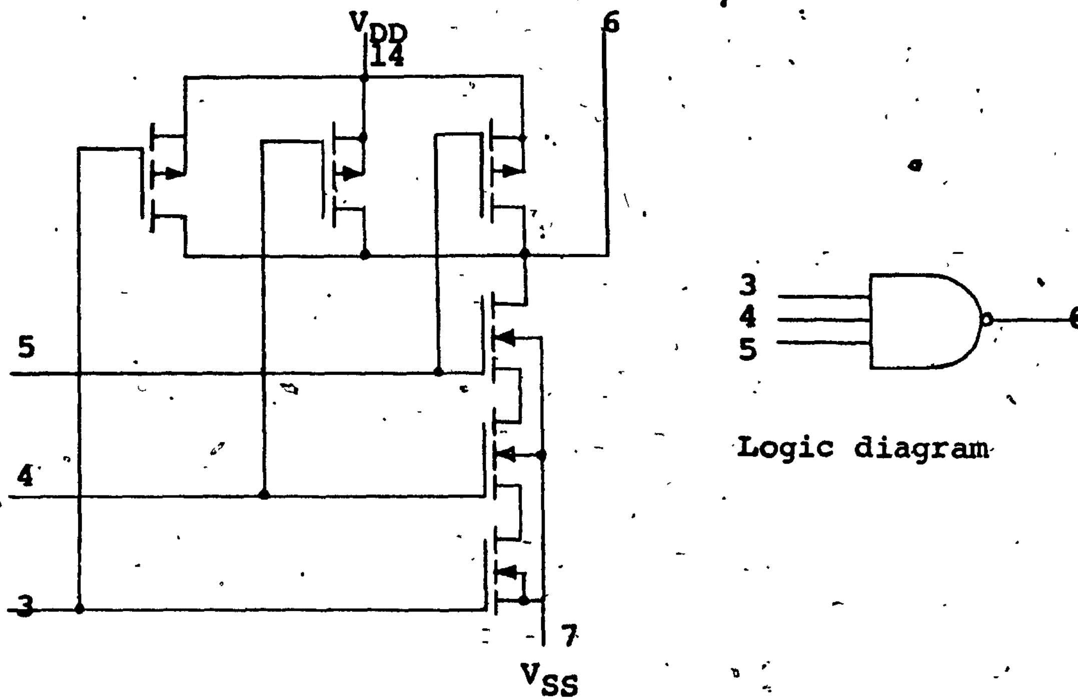
A rapidly growing market for integrated circuits, CMOS in particular, is in watches and clocks. Electronic time pieces are now being built that have an accuracy impossible to attain by mechanical means. The circuit consists of a quartz-crystal oscillator whose highly accurate fundamental frequency is devided down in many steps by counting circuitry to the speed required to drive clock hands or perhaps an electro-optic digital device such as a liquid crystal display or a light emmiting diode array. The low price of integrated

circuit counters in combination with their accuracy and reliability has created a profound change in the industry. Figures 7-2a and 7-2b show the diagrams of some applications of CMOS and Fig. 7-3 shows the diagram of a PMOS device.

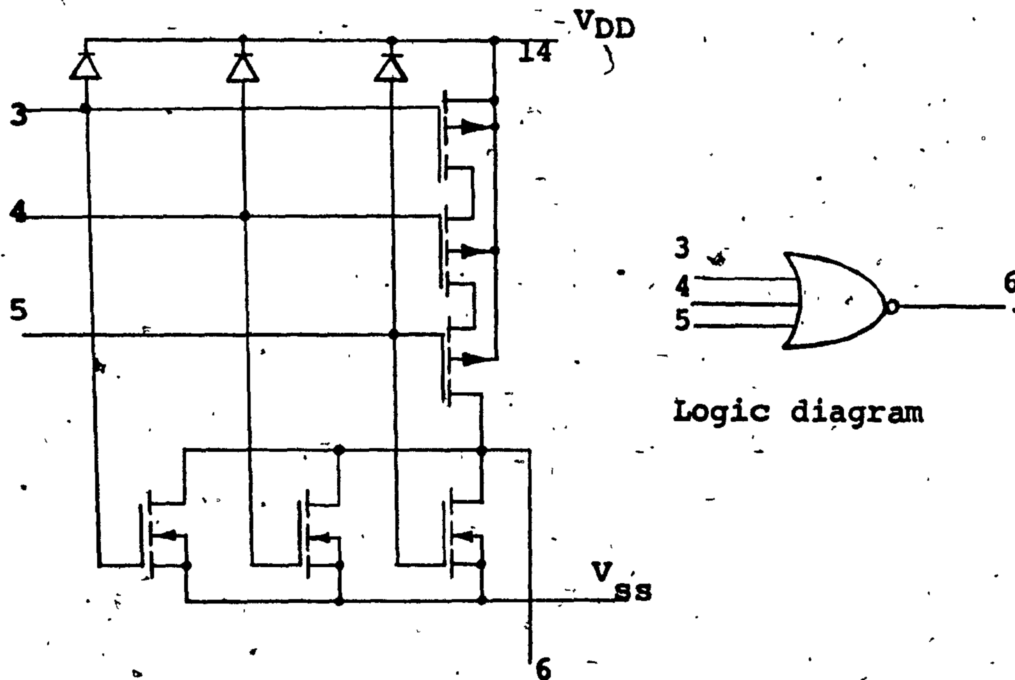
7.4 New Technologies

Although PMOS integrated circuits have lower operating speeds, 450 nsec access time, than the fastest bipolar circuits, 50 nsec, even this limitation will be minimized in the near future. The relative low MOS speeds are due primarily to the parasitic capacitance discussed earlier. Capacitance refers to the ability of an insulator or a semiconductor to hold an electric charge. The effect of parasitic capacitance is to impede the flow of charge carriers through the field effect structure, thereby slowing down its overall switching time. If these capacitances could be minimized, the inherent speed of the MOS transistor, which is defined by the mobility of the charge carriers and the dimentions of the structure, would be comparable to that of the fastest bipolar transistor[16].

An important step toward increasing the speed of MOS transistors has been the developent of a technique for depositing a very thin layer of single-crystal silicon on an insulating substrate. It is now posible to deposit silicon layers only one micron thick on flat substrates of synthetically grown sapphire[16]. As a result the capacitances of the

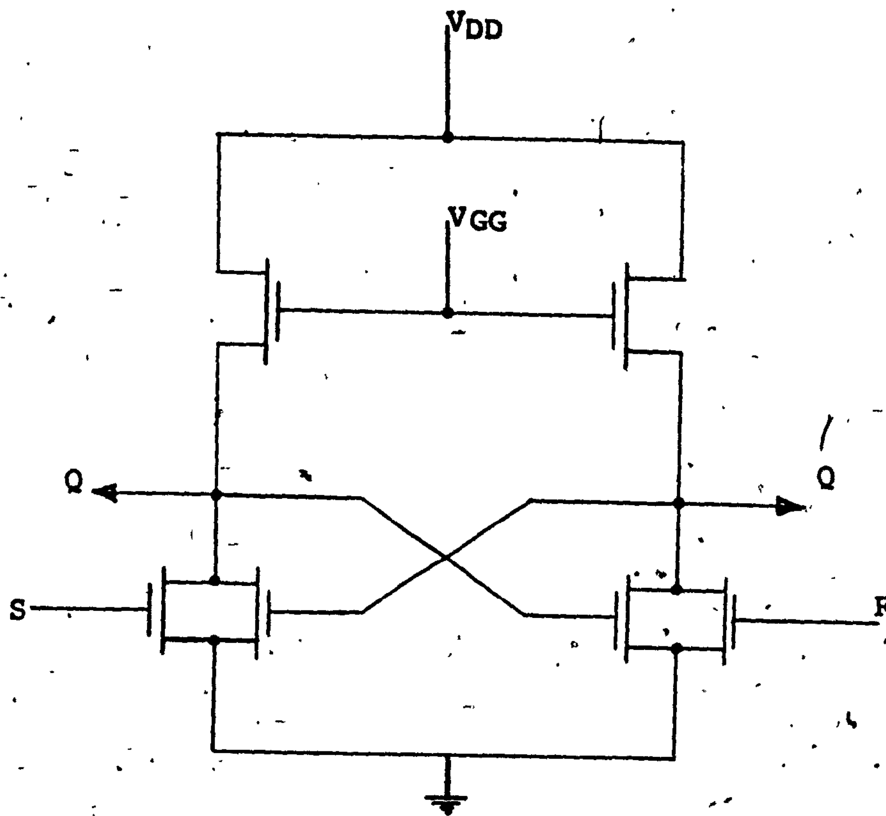


a) CMOS circuit schematic of a 3-input NAND gate

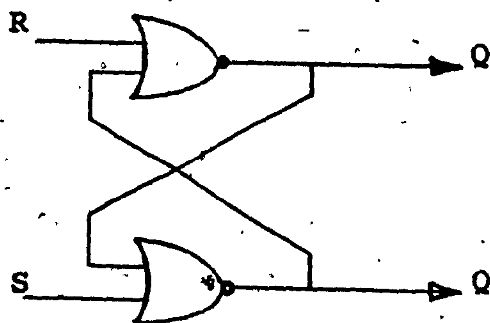


b) CMOS circuit schematic of a 3-input NOR gate

FIG.7-2



Circuit diagram



Logic diagram

FIG. 7-3

The cross-coupled latch (RS flip-flop), MOS device using NOR gates.

source and the drain are reduced by a factor of roughly 20 over MOS transistors made of bulk silicon material, in which the source and the drain are diffused only partially into a relativelly thick substrate. Individual transistors are easily isolated by chemically removing the silicon film between devices. The interconnecting wiring sits directly on the insulating sapphire and thereby does not contribute the additional unwanted capacitance that arises when the wiring is deposited on a bulk silicon substrate. When MOS circuits are made in this thin-film form, called SOS (silicon on sapphire) they combine the unique properties of MOS bulk devices with the high speed of bipolar ones. At the present time the SOS structures are more expensive than bulk devices and will be used only when the additional cost is justified. As the cost decreases SOS devices should be more widely used. As an example, an SOS eight-channel TTL compatible analog multiplexer is 10 times faster (50 ns channel-to channel) than previous MOS devices. The 50 nsec access time for an SOS 64-bit static RAM (random-access memory) puts it in a class with many bipolar RAM's though it uses 10 times less power. The 1,024-bit RAM achieves the lowest propagation-delay power product of any RAM[16]. Finally, SOS 256-bit shift registers have 10 times the speed of comparable static registers-and all their inputs are TTL compatible .

8. ADVANTAGES OF MOS DEVICES

8.1 General

There are two basic advantages for many manufactures for using MOS LSI's: economy and performance. Because of the successful application of MOS LSI's in numerous systems, the economic advantage is generally conceded, particularly where production of volumes are high. It is important to distinguish between superior system performance and transistor circuit performance. The principal limitations of MOS arrays are a result of lower speed characteristics of present MOSFETS.

The two basic advantages are further subdevided into the following categories.

8.2 Economic Factors

a) Lower Initial Cost of System

The low cost of system is primarily a result of the large decrease in the number of semiconductor circuits, which in turn causes a significant reduction in the number of interconnections, printed circuit packs, connectors, motherboards, enclosures etc. For example Intel's 8080 microprocessor is an 8 bit parallel central processing unit (CPU) fabricated in a single chip n-channel silicon gate MOS and replacing a large number of circuits previously reguiring many IC's. Other examples are ROM's (read only memories) RAM's etc. These reductions provide large savings in labour

costs because the assembly and checkout of the system are simplified. The combined effect of these savings is the principal advantage of MOS.

The small number of interconnections within the MOS LSI system is probably the most important single factor responsible for both lower initial cost and increased system reliability. This is a result of the ability of a single MOS array, such as a RAM and ROM, to replace many conventional IC's and their associated interconnections. As pointed out by Chang[17], studies inticate that the cost of permanently connecting two terminals electrically varies from $ 0.05 for highly automated high volume production to more than $ 1.00 for low volume, high reliability equipment. The cost of connecting two points on an integrated circuit using photolithographic techniques can be as litle as a few thousandths of a cent.

b) Low Cost of Complex Arrays due to Simpler Process

The low cost of arrays is a consequence of the simpler, standardized manufacturing process as compared to bipolar IC technology. Table 8-1 shows a comparison of the basic manufacturing steps of the two technologies[10].

A similar comparison by Warner[18] suggests that the bipolar process is about 30% more difficult to manufacture than the MOS process when all factors are considered. However when the MOS-process is compared with the bipolar process that is required for LSI, the differences

Table 8-1

Comparison of Metal Gate MOS and Double-Diffused Epitaxial Bipolar Fabrication Process

	P-MOS	Double Diffused
Diffusion	1	4 + Epitaxial
Process steps	38-45	130
High Temp. Process Steps	2	10
Masking Steps	4-5	8

are considerably higher. Unlike the bipolar process the MOS process requires no additional steps to provide two layers of interconnect. A number of critical process steps, particularly the high temperature diffusions plus the masking operations, are greately reduced in MOS process. Consequently the yield of MOS arrays greatly exceed those of bipolar chips of comparable functional complexity. Of even greater importance is the fact that the MOS process can be held constant regardless of the array that is being fabricated. With MOS process, circuit performance is varried by the design of the MOSFET geometry not by varying the process as is often done in bipolar technology. More realistically therefore the bipolar process is 50% more difficult than the standard metal gate MOS[10].

Another factor that gives MOS LSI cost performance advantage is the relatively small size of MOS arrays. Since yield varies inversely with die area, this means lower die costs and therefore lower selling price. The small size of arrays is due to the use of active MOS load transistor in place of large diffused resistors. The simpler process provides three benefits. First since there are fewer steps, there is less tolerance built up and therefore less area required for accumulation of tolerances. Second it requires no isolation junction as do bipolar transistors. Isolation junctions consume a lot of area due to the wide lateral diffusion step. Provision of two layes of interconnect is the third benefit. The second layer of intercon-

nect is formed during the normal processing. The interconnect lines act as resistors and since they use low currents, they are tolerable for many circuits, unlike pipolar IC's which use higher currents.

d) Automation possible due to the design process.

The design of the MOSFET, unlike the bipolar transistor, is accomblished by straight forward mathematical techniques. It is therefore easily automated.by a computer program[17]. Frequently used common functions can be designed, checked and stored on magnetic tape for use in designing new MOS arrays. The automated design process is particularly well suited for MOS LSI memories, such as RAM's, ROM's and variable bit length shift memories.

8.3 PERFORMANCE FACTORS

a) Improved System Performance

One of the most significant advantages of MOS LSI is the fact that the system designer has freedom of choice. He can design a high performance system with no significant increase in system cost. Because of the small size of the typical MOSFET in an array, active devices can be used as needed with litle increase in chip area. Also its extremely high input impedance permits high fanout within the chip. These two features permit much more logic within a given die size. MOS LSI's reduce the cost per logic function so much

that it is no longer a design criterion. This increased logic capability can be used to provide greater computing or processing power[19].

High system noise immunity is another advantage provided by MOS technology. The relatively high threshold voltage of the standard p-channel process coupled with large logic level swings, in dynamic logic circuits, results in typical noise margins of at least 1 volt over the normal commercial equipment temparature range of 25° - 50°c.

b) Improved Reliability

The mere reductions in parts and interconnect are obvious contributors to better system reliability. Even though the total number of interconnections in the system is not greatly reduced, extensive tests and usage have established the reliability of these mass fabricated connections. The quality of interconnections within an MOS chip is relatively easy to control and detect compared to the difficulty of controlling and detecting the external to MOS chip connections.

An increase in system reliability, through reduction of system interconnect and quality of parts, inherently tends to improve system maintainability.

c) Predictable Design

Another feature of MOS that leads to performance advantages as well as economic advantages is the relative ease with which MOS circuits can be designed to meet spe-

cific performance requirements. This means that there is a high propability that an array will meet specifications in the first design effort. The key to successful MOS LSI designs is a stable process thoroughly characterized so that a designer need only to vary the topology of the MOSFET to achieve a given set of performance characteristics[10]. Once the process is characterized and the design limits are set, the average designer has little trouble determining proper MOSFET dimentions. He has no concern for diffusion times, temperatures, doping concentrations etc., parasitic diode effects are minimal with MOS technology. MOS design automation further guarantees consistent performance.

8.4 PROBLEMS AND LIMITATIONS

a) High Development Costs

The development costs of MOS LSI chips can be very high and it depends on the required performance type of logic and circuit complexity. The use of computer programs[20] to automate much of the routine tasks helps reduce the direct costs associated with the design of an array. The cost to develope and maintain the design automation programs however plus the costs of equipment to performe the actual tasks are very high. In addition if a design change is required in a chip after the tooling is complete, the entire tooling may have to be changed or redone.

b) High Testing Costs

The cost of developing a test program or pattern for the MOS array must also be considered. The magnitude of the testing problem can be appreciated when one consideres the number of possible inputs on an array plus the number of internal storage elements. With n inputs (which can be either a 1 or 0) and m internal states (also binary) as many as 2^{n+m} test words may be required to thoroughly check out the array.

c) Limited Production Quantities

Because of the small volume of production required, the high costs of design and development must be amortized over fewer units than before. The fact that a single MOS array replaces numerous discrete parts and conventional IC's limits its volume of usage to several orders of magnitude.

d) High Packaging Costs

The MOS LSI must be packaged to protect it from contaminants, and yet the package must be convenient to handle. Multilead, hermitic packages suitable for MOS LSI are very costly relative to the 14 and 16 lead dual in-line packages used for most bipolar ICs. For minimum costs, packages with the least number of pins should be used, but this would most

likely result in more MOS LSI chips per system. It is almost certain that the high cost of ceramic and metal hermetic packages will eventually force the development of suitable plastic packages. As matter of fact this has already been started.

8.4.1 Performance Limitations

a) Slow Speed

The principal performance limitation of MOS LSI is the comparatively slow switching speed of the MOSFET. The slow speed of the MOSFET is due to its limited ability to charge and discharge capacitive loads. These loads consist of the self or intrinsic capacitance of the device, which is a function of the device dimensions and process parameters, plus the stray capacitances. The limited ability to charge and discharge capacitance is a consequence of the low transconductance (g_m) of typical MOSFET used in LSI. Since the g_m of a MOSFET is highly dependent upon the state of the art of MOS technology, we can expect improvements in the future. For instance variations of the basic process such as ion implantation and silicon gate reduce the self capacitance. Complementary MOS improves the situation further but the process becomes more complicated and therefore more costly.

b) Incompatibility With Bipolar Circuits.

The standard threshold voltage channel MOS process operates from power supply levels (12v) that are quite different from those required by bipolar ICs (5v). Of even greater importance are the incompatibilities of the input and output logic voltage levels of MOS circuits and bipolar IC's. Existing systems that contain only bipolar IC's require buffers or level transistors if they have to interface with standard threshold voltage MOS arrays. When interfacing with widely used TTL or DTL inputs, the MOS output device must be capable of sinking 1.6 MA per input. Since the current handling capability of the MOSFET is a direct function of the device size, output stages are not only slow but consume considerable chip area. This increases the die size and therefore the cost of the product[10].

8:4.2 Business-Management Problems

a) Costumer Supplier Interface

The MOS LSI has created many problems common to both the semiconductor supplier and the systems manufacturer. The loss of the distinct line that once separated the market of the system manufacturer from that of the semiconductor supplier is a most important one. The primary cause of this problem is the increasing number of system functions now performed by a single MOS LSI chip. Naturally the system manufac-

turers are concerned as they see their suppliers contributing more to the value of their product. The successful solution to this problem requires involvement by top management of both costumer and supplier[21].

CONCLUSION

MOS technology, be it of p-type, n-type or complimentary type, has had and will continue to have a tremendous effect on semiconductor technology in general. MOS devices have already captured a large section of the semiconductor market; and will continue to do so in the near future.

It was stated earlier that the main advantages of MOS devices have been their high density, low power consumption and simpler fabrication process. It was the high density advantage that led to the development of Large Scale Integration. Today LSI devices such as ROM's and RAM's constitute a major portion of dollars spend on semiconductors. The total sales of MOS devices in 1973 have been 250 million dollars while those of bipolar devices for the same year have been 400 million dollars. A generation of microcomputers such as Intel's 8080 CPU replacing many IC's are coming into the market, and the trend continues towards miniturization. MOS devices with their small chip size are ideal for this trend.

The simpler fabrication of MOS devices in comparison to the bipolar process, as shown in table 8-1, has the benefit of being cheaper and therefore more competitive.

The main disadvantages of MOS devices have been their slower speed and incompatibility with bipolar circuits. However SOS (silicon on sapphire) technology coupled with CMOS devices have improved the speed of MOS devices by a factor of 10. For example a 64 bit static RAM using SOS technology has 50 nsec access time which puts it in the same class with many bipolar RAM's though it uses 10 times less power.

The other disadvantage of MOS devices, the incompatitility with bipolar circuits, is being taken care of by the new devices that come into the market. They are TTL compatible.

The competition between the MOS and bipolar devices will continue and in many cases the technologies of both are combined to achieve better results. Such a case happened at Bell Telephone Laboratories.

Bell Telephone Laboratories have developed the so called Right Scale Integration (RSI) using "beam leads" technology: 64 bipolar chips, each 0.046 by 0.063 inches, are mounted on a ceramic wafer and connected into large memory array. The 64 chips fit within an area of 0.6 by 0.75 inches and contains 40,960 devices. This equals 90,000 devices per square inch.

R E F E R E N C E S

1. J. T. Wallmark and H. Johnson, "Field Effect Transistor, Physics Techology and Application", Prentice Hall, 1966.

2. J. E. Lilienfield, U.S.Pat. NO 1,745, 175 (1930), and O. Heil, British Pat. NO 439,452 (1935).

3. J. Bardeen and W.H. Bratain, "The Transistor: A Semiconductor Triode", Phys. Rev., 74, 230 (July, 1948)

4. W. Shockley, "A Unipolar Field-Effect Transistor", Proc. I.R.E., 40, 1365-1376(Nov, 1952).

5. "MOS", Scientific American, Vol.229, # 2, Aug. 1973, pp. 48-59.

6. L.L. Chang, H.N. Yu, "The Germanium IGFET", Proc., IEEE, 53, 316 (1965).

7. M.H. White and J.R. Cricchi, "Complementary MOS Transistors" Solid State Electronics, 9, 991 (1966).

8. H. Beche, R. Hall, J. White, "Callium Arsonide MOS Transistors", Solid State Electronics, 9, 783 (1966).

9. G.E. Moore, "Semiconductor Integrated Circuits", Chap. 5 of "Principle of Microelectronic Engineering", E. Keonijian, McGrow-Hill, New York, 1962.

10. Engineering Staff of American Micro-Systems, "MOS Integrated Circuits", Van Nostrant Reinhold Co. 1972.

11. J. Millman and C. Halkias, "Integrated Electronics", N.Y., McGrow Hill, 1972.

12. S.M.SZE, "Physics of semiconductor Devices"; J.Wiley and Sons, 1969.

13. A.S.Grove, Physics and Technology of Semiconductor Devices.

14. "McMOS Integrated Circuits Data Book" Motorola 1974.

15. C.T. Sah, Characteristics of the "Metal Oxide Semiconductor Transistor", IEEE Trans. Electron Devices, ED-11, 324-345 (July 1964).

16. "Silicon on Sapphire Substrates Overcome MOS Limitations" A. Rapp and E.C. Ross, Electronics Vol. 54, No 20 Sept. 25, 1972.

17. M. Chang, "Developments in Digital Integrated Circuits", presented at WESCON New Solid State Devices Session, San Francisco, (Aug. 1966).

18. R.M. Warner, "Comparing MOS and Bipolar Integrated Circuits" IEEE Spectrum 4; 50-58 (June 1967).

19. W.A. Notz, "Benefiting the System Deginer" and "Organizing for Processing Power", Electronics, 40, 130-133 and 139-141 (February 20, 1967).

20. J.Foltz and F. Musa, "Computer Helps Design of Comp-

limentary MOS Logic", Electronics Vol. 54, No 13 (June 19, 1972).

21. G.E. Penistem, "Impact of LSI Technology on the Electronics Market", paper presented at WESCON, San Francisco, August 1969.