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Improved Power Supply Topologies for Fixed and Variable Frequency Operation

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A Thesis

in

The Deparment

of

Electrical Engineering

Presented in Partial Fulfillment of the Requirements
for the Degree of Doctor of Philosophy at
Concordia University
Montréal, Québec, Canada

June 1985

ABSTRACT

Improved Power Supply Topologies for Fixed and Variable Frequency Operation

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Concordia University, 1985.

The theory of switching power converters is in a state of flux mainly for two reasons. First, because no comprehensive framework for the analysis of power converters has been established and second, because power semiconductor technology has been evolving continuously. These reasons have motivated this contribution to the development of a unified theory for power converters. In particular, with the introduction of a transfer function for switch mode converters some basic principles can be stated, new relationships developed and the behaviour and characteristics of power converters studied. For example, common mathematical expressions are introduced to analyze controlled rectifiers, voltage source inverters, and current source inverters. Altogether, these converters are by far the most important and frequently used in contemporary power applications. Further, time domain operations are proposed as an alternative to the more complex, slower, and less accurate frequency based operations. Finally, this unified approach is enhanced by a computer aided design (CAD) method for switch mode converters.

Moreover, while utilizing the technological advances in the field, this study contributes to them by introducing two power supply

topologies for fixed and variable frequency applications. The power supply topology first presented, intended primarily for fixed-frequency fixed-voltage applications (e.g. UPS systems), incorporates the regulation of the dc link to significantly increase the utilization of the system components. The performances of the two modes of operation of the system (PCU and CCU) are discussed and evaluated against the performance of a standard VSI-SPWM power supply system. An optimized fixed PWM pattern is also introduced to further boost the dc link utilization and reduce the operational switching frequency. The second power supply topology proposed, intended primarily for variable-voltage variable-frequency applications (e.g. ac motor drives), utilizes a PWM controlled rectifier and a PWM current source inverter. The system has a number of intrinsic advantages which include: bilateral power flow (regeneration), high reliability (current source), sinusoidal input-output currents and voltages, reduced reactive components, improved input power factor and simpler current feedback sensors.

Finally, to facilitate the application of the CAD and the design of the proposed topologies, practical design examples are included, and selected predicted results are verified experimentally.

With love to my wife Soledad

ACKNOWLEDGEMENTS

I would like to express my gratitude to:

my supervisor, Dr. Phoivos D. Ziogas, for his friendship, guidance, and support throughout my graduate studies and in the development of this work. It has been a great honor to be a member of his research team;

my co-supervisor, Dr. Victor R. Stefanovic, for his support and for the valuable discussions, also, for his encouragment in initiating my interest in graduate studies;

my friends and research colleagues, Michael Boost and Donato Vincenti, for the interesting discussions we shared.

my friend, Dr. Carlos Martinez P., for the uncounted services made available to me in my homeland during my leave.

and finally, to Ms. Madeleine Klein for her reliable typing services and refreshing sense of humour.

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LIST OF ACRONYMS

CR : Controlled Rectifier.

CSI : Current Source Inverter.

VSI : Voltage Source Inverter.

PWM : Pulse Width Modulation.

CAD : Computer Aided Design.

UPS : Uninterruptible Power Supply.

PCU : Partial Chopper Utilization.

CCU : Continuos Chopper Utilization.

DF : Distortion Factor.

THD : Total Harmonic Distortion.

CSR : Current Source Reactor.

LIST OF SYMBOLS

1. General

$x(t)$	:	Instantaneous values.
X	:	Average (for dc) or rms (for ac) values.
$\bar{x}(t)$	:	Matrix of dimension 1X3 representing a 3Ø phase system (each component of the matrix is a function representing each phase).
$\bar{x}_l(t)$	:	Matrix representing line quantities.
x_a, x_b, x_c	:	Components of $\bar{x}_l(t)$.
$\bar{x}_p(t)$	:	Matrix representing phase quantities.
x_{pa}, x_{pb}, x_{pc}	:	Components of $x_p(t)$.
$\bar{x}_1(t)$	:	Matrix of fundamental components (sinusoids at fundamental frequency, usually 60 or 50 Hz).

2. Voltages

v_d, V_d	:	Converter input dc voltage and respective average value (also called secondary dc link in Chapter 4).
v_o	:	Output load voltage.
v_i	:	Input voltage with reference to Fig.(2.10).
e_a, e_b, e_c	:	Utility phase voltages
v_c	:	Capacitor voltage.
E, Er	:	Primary dc link voltage and respective rated value.

3. Currents

i_d	:	Converter dc input current.
i_o	:	Output load current.
i_{cf}	:	Capacitor current.
i_{lf}	:	Utility line currents.
i_s	:	Switch current.
i_T	:	Controlled semiconductor current (Fig. 3.1b)).
i_D	:	Diode current.

4. Transfer Functions

$\bar{H}(t)$	:	Bidirectional common transfer function for VSI, CSI, and CR.
$\bar{S}$, $\bar{C}$, $\bar{R}$	:	Bidirectional transfer functions for VSI, CSI and CR respectively.
$\bar{S}v, \bar{C}v, \bar{R}v$	:	Voltage transfer functions for VSI, CSI and CR respectively.
$\bar{S}i, \bar{C}i, \bar{R}i$	:	Current transfer functions for VSI, CSI, and CR respectively.
G_c	:	Boost Chopper Gain.

5. Electrical Components

Ro, Lo	:	Load resistor and load inductor.
Lfo, Cfo	:	Output inductor and output capacitor filter components.

L_{fi}, C_{fi} : Input inductor and input capacitor filter components.

C_f : Capacitor filter (first order) for CSI in Chapter 5.

L_{csR} : Inductance value of the current source reactor.

6. Frequency and Time Variables

f_o, : Fundamental frequencies (usually f_o=60 or 50 Hz).

f_c, f_{cn} : Carrier and normalized carrier frequency.

: Break filter frequency.

: Switching frequency (conmutations per second).

: Time shift between voltage and current (i.e. $\tau=\phi/\omega$)

7. Impedances and Phase Displacement

$Z(j\omega)$: Load impedance at fundamental frequency (usually equal to one per-unit).

ϕ : Phase displacement between voltage and current.

X_{cd}, X_{c1} : Impedance of the filter capacitor Cf (Chapter 5) at the dominant and fundamental frequency respectively.

8. Miscellaneous

M : Modulation factor (Fig.(2.16)).

a_n	:	Magnitude of the nth harmonic component of a PWM waveform.
Ac	:	Magnitude of the carrier signal (Fig.(2.16)).
Ar	:	Magnitude of the reference signal (Fig.(2.16)).
Por	:	Rated output power.
Ns	:	Number of switches.
Suf	:	Switch utilization factor (2.33).
Svuf	:	Switch components utilization factor (3.3).
pf	:	Power factor.
Pfe	:	Equivalent power fator seen by a VSI (4.8).
FUm	:	Utilization factor produced by the PWM technique.
FUv	:	Utilization factor produced by variations in the dc link.
FUo	:	Overall utilization factor.
r	:	Order of the first significant harmonic (i.e. with a magnitude over 3% of the fundamental).
d	:	Order of the dominant harmonic or equivalent dominant harmonic.

CHAPTER 1

INTRODUCTION

1.1 General Introduction

Progress in power semiconductors such as silicon rectifiers and thyristors has been a step-by-step evolutionary process, with gradual but steady improvements in operating characteristics, ratings and packaging concepts. Progress has been quite dramatic when viewed in relation to the modest early beginnings of these devices some twenty seven years ago.

Specifically, power semiconductor technology, has seen the recent emergence of several types of improved power semiconductors such as the Mosfet, Asymmetrical Thyristors, Gate Turn-off Thyristors and Bipolar Transistors. Some authors [1]...[8] have anticipated considerable improvements in the power converter area made possible by these new breakthroughs in semiconductor technology. These new power converters, implemented with gated turn-off semiconductors, are replacing the traditional power conversion topologies. Undoubtedly, the constant increase in the quality of performance and the drop in cost of these new semiconductor components makes affordable new goals for industrial processes, ensuring a growing field of applications for static converters.

This thesis takes advantage of these technological advances, and contributes to these new trends by focussing its objective on the improvement of power supply topologies for constant and variable

frequency applications. Moreover, in order to establish a common theme and facilitate the analysis of these new topologies, a common analytical framework is first established. Within this framework converters are classified and analysed according to their respective transfer characteristics instead of topologies. As a result new powerful analytical tools are established, eliminating old conceptual difficulties.

1.2 Functional Approach to Power Converter Analysis

The contemporary study, analysis and synthesis of power converters is classified, and therefore developed, according to converter circuit topologies, such as controlled rectifiers, choppers, current source inverters, voltage source inverters, dual converters, cycloconverters and frequency changers [9]...[14]. Moreover, the study of these different converter circuits has generated new subdivisions according to auxiliary circuitry employed by the main converter, such as commutation circuits and snubber networks. This somewhat disjointed analysis approach, although successful in describing the converter behaviour, does not establish important relationships among power converter circuits, which tends to prevent the generalized application of research advances.

Pioneering work in the general theory of switching power converters [15] has demonstrated that classifying power converters according to function (instead of circuit topology) permits better understanding of converter behaviour and relationships. Moreover, it

allows the development of analytical concepts applicable to families of converters rather than to individual converters.

Previous work on circuit configurations following a functional approach has been based on switching functions [15] [16] [17]. Basically, a switching function defines the on-off instants of switch conduction. However, current source converters and voltage source converters require completely different switching functions. Consequently, the analysis of voltage and current source converters has been treated separately.

This thesis presents a functional approach based on transfer functions rather than on switching functions [18] [19]. Following this approach current and voltage source converters can be analysed simultaneously (i.e. the transfer function does not depend on the nature of the analysis variables (current or voltage)). Therefore, the transfer function concept constitutes a more abstract but convenient method to relate the input-output variables of power converters.

This approach allows the reclassification of power converters into converter functional families (Table(2.1)), and the identification of significant commonalities among the converters. For example, a unique bidirectional transfer function is established for voltage source inverters (VSI's), current source inverters (CSI's) and controlled rectifiers (CR's). From a classical viewpoint this is a surprising result, although not unexpected in the context of the functional transfer function based analysis approach, because the three above mentioned converters perform the same ac/dc power conversion

function (considering bilateral power flow).

Also, it is noted that VSI, CSI and CR converters do not share switching functions (used extensively in the contemporary analysis of converters [15] [16] [17] [20]) in spite of sharing functional transfer function. This fact reveals the importance of the functional transfer function defined in this thesis (2.1).

Relevant practical relationships deduced for ac/dc converters sharing a common bidirectional transfer function can be summarized as follows:

i) the same generalized circuit topology can be used by VSI, CSI, and CR to perform their conversion functions,

ii) identical pulse width modulation control techniques can be utilized by VSI's, CSI's and CR's, and

iii) voltage source converters (VSI's) are the dual converters of current source converters (CR's, CSI's).

Converter duality implies that there is a one to one correspondance between reciprocal dependant variables for voltage source and current source converters. Specifically, Chapter 2 will demonstrate that the input current of a VSI, the input voltage of a CSI, and the output voltage of a CR have identical waveforms, and also that output voltages of a VSI, output currents of a CSI and input currents of a CR also have identical waveforms [19].

The converter duality between voltage and current source converters itself has important theoretical consequences. For example,

Chapter 5 will show that while VSI's can be connected parallel to a single dc supply, their dual CSI's can be connected in series to a single dc power supply [21].

A transfer function based functional approach also reveals a common converter filter (input-output) design approach and common PWM control techniques which are essential for the design of the overall power conversion system.

1.3 Generalized Model for the Controlled ac/dc dc/ac Conversion Functions

Among the various power conversion functions performed by static power converters, the controlled ac/dc and dc/ac are by far the most significant and numerous in terms of applications.

Contemporary analyses of power converters performing these functions have been formulated using frequency domain expressions (Fourier Series) to obtain converter generated input-output waveforms. This analysis based approach provides exact input-output spectral content data [20] normally required for filter design and PWM technique optimization. However, the approach has some intrinsic disadvantages:

i) it requires complex mathematical transformations and leads to infinite trigonometric series multiplications [15] [16] [20],

ii) it requires frequency-to-time domain transformations which are intrinsically time consuming and inaccurate, thereby leading to inaccurate predicted time domain waveforms,

iii) it cannot provide good user-computer interaction, particularly in power converter simulation programs, and

iv) it cannot handle transient phenomena and non-linear loads.

These disadvantages have motivated research which focuses on the development of a generalized analysis approach which unifies the ac/dc and dc/ac conversion functions. As shown in this thesis, this approach yields a generalized converter model suitable for the unified analysis of VSI, CSI and CR converters, which is based on the extension of the concepts of switching functions [15] [16] and converter transfer function [18]. In addition according to the functional approach previously described, this study:

i) presents a generalized converter model for the three phase VSI, CSI and CR families of converters,

ii) provides state space analysis formulation capable of describing converter performance under transient and steady state conditions,

iii) produces generalized converter design data for switch ratings, input-output filters and operating frequencies applicable to all aforementioned converter families.

To conclude, Chapter 2 will show that the proposed functional converter model:

i) requires extremely simple and easily programmable mathematical operations,

ii) facilitates computer-aided design by reducing the computer

processing time required by the contemporary approach,

iii) simplifies converter analysis and design by providing exact input-output predicted current and voltage time domain waveforms and respective spectra,

iv) can be used to study transient converter performance, thus reducing considerably breadboarding costs and testing times.

1.4 Improved Voltage Source Inverter Design Method

The analytical concepts discussed in the previous sections are then employed to facilitate the analysis and design of some well known static converters, as follows.

Today, the majority of power converter systems employing inverters use voltage source inverters. Therefore, since this thesis is concerned with the improvement of some important families of static power supplies, a critical examination of the contemporary VSI design method has been performed. Chapter 3 will show that a basic VSI design assumption, introduced by the contemporary approach, is responsible for a severe under-utilization of the VSI components. Specifically, the problem with the contemporary approach stems from the assumption that the VSI switch component ratings are identical to VSI switch ratings [11] [14].

By computing the exact VSI component ratings it will be shown that a substantial improvement in component utilization can be accomplished. Also, by using this design approach, the contemporary task of optimizing a VSI design evolves into a precise design method

[22] from an empirical (trial and error) approach.

Together with the generalized description of the analysis and synthesis method, Chapter 3 will present specific normalized design data applicable to fixed and variable output frequency VSI based systems. Moreover, to account for a wide variety of applications, wide ranges of inverter modulation and load power factors will be considered. Finally, for comparison purposes, the design data provided include three different PWM control schemes, namely, sinusoidal PWM [23], six-step PWM [22] and a optimized fixed PWM pattern proposed in Chapter 4 [24].

A comparative design example is used to illustrate the design method, as well as to produce a quantitative measure of the improvements accomplished in a specific case. The example shows a 64 % improvement in the semiconductor utilization factor.

To check the validity of the proposed design method, selected theoretical results will be verified with an experimental 2 KVA unit. Those experimental results, including pictures of actual VSI waveforms will be presented.

To conclude, the proposed design approach of Chapter 4 can be used to substantially increase the processed power per-unit of converter mass (and volume), and to significantly reduce the cost of a VSI based power supply.

1.5 Improved Power Supply for Fixed Frequency Operation

Continuing with the application of the analytical concepts

developed in Chapter 2 of this thesis, Chapter 4 focuses on the improvement of power supplies for fixed frequency operation. From this large family of applications, UPS systems are of primary importance and quite representative of this family. A study on UPS systems is justified by the increasing demand for more light, economical, and reliable UPS systems [25]. A UPS system is normally operated at a constant output frequency (usually 50 or 60 Hz) to ensure good quality power for computers, hospitals, telephone switching systems, military installations, and in general, for any critical load that cannot tolerate disturbances associated with normal utility power such as; voltage dips and surges, frequency variations and momentary or sustained losses of power. Previous work on UPS systems have incorporated sinusoidal PWM for the UPS-VSI [26]. Further progress has been made by utilizing improved PWM techniques [27] and optimal filtering [28]. A system employing a variable voltage input (VVI) six-step VSI, with the idea of a boost regulator in the dc link was presented in [29]. However, prior to the appearance of this publication, the author of this thesis had already presented this concept in his Doctoral Seminar (Concordia University, Fall 1982). Furthermore, a more sophisticated overall system which incorporates an optimized fixed PWM pattern for the VSI inverter, together with the dc link boost chopper regulator, is presented in Chapter 4 [24]. The optimization of the control pattern is based on a weighted harmonic optimizing criterion. Chapter 4 also presents an important evaluation of the traditional power conversion method for UPS, identifying some

important sources of component system under-utilization. Finally, several solutions to enhance system design are proposed and experimentally tested to verify predicted results.

For the purposes of completeness, a complementary study on UPS systems based in current source inverters has been performed on [30]. However, VSI based systems are finally recommended (instead of CSI) because in general, a UPS cannot be subjected to the restriction of load linearity and balance required for an efficient CSI system design (a study on effects of unbalanced loads on CSI is performed in Chapter 5 [21]).

As a result of the study and review of this UPS-VSI power conversion process, it is concluded that at least 65 % extra power handling capability can be added to the system without compromising cost or system performance. Furthermore, the improved results obtained for this power supply, are in addition to the improvements of VSI based systems obtained in Chapter 3. Therefore, further improvements of the UPS-VSI system components utilization can be obtained, if the design approach of Chapter 3 is followed to design the UPS topologies proposed in Chapter 4.

Finally, experimental results that demonstrate the feasibility of the proposed UPS-VSI system are obtained using a laboratory unit of 2 KVA.

1.6 Novel Power Supply for Variable Frequency Operation

Chapter 5 of this thesis deals with the improvement of power

supplies for variable frequency operation usually required in variable speed ac drives. A major research effort in that area is justified because, in spite of the many advantages ac machines have over dc machines, the cost, control complexity, and poor perfomance and reliability of their respective power converters have prevented the widespread application of ac drive systems. However, with the continously falling prices of power semiconductors, relatively fixed prices of motors, and development of complex control strategies in low priced VLSI circuits, the differences in cost and complexity between ac and dc drives have been slowly disappearing [2] [3] [31]. Consequently, by taking advantage of these developments, today's research and development efforts are focused on improving the converter and overall drive performance. These efforts have created three complementary research fronts. The first deals with control techniques that further improve the dynamic torque speed ac drive characteristics [32]...[35]. The second is engaged in induction motor design for switch mode operation and the development of new motors, such as the permanent magnet (PM) motor [36] [37]. Finally, the third research area is engaged in searching for power converter topologies that further improve the overall power conversion process such as the one developed in Chapter 5 [38]...[44].

Previous work on these types of power supplies for ac drives can be classified according to three existing power converter families. The first based on diode rectifier PWM-VSI systems for general purpose drives, a scheme not regenerative unless a second front end converter

is added to operate in the inversion mode. Otherwise, dynamic braking can be accomplished only by using a contactor resistor combination across the dc link. So far, and because of its relative simplicity, the most popular technique for the PWM control of the VSI has been the sinusoidal PWM technique [23]. However technological advances, particularly in VLSI circuits, have made possible the consideration of improved modulation schemes for higher drive performance. Other converter types based in VSI will not be considered because they are in clear disadvantage when compared to the PWM-VSI [40].

The second scheme is based on the current control of the VSI, offering substantial advantages in the elimination of stator dynamics in high performance ac drives, compared to their voltage controlled counterparts. However, this scheme is also non-regenerative and has some inherent limitations. It requires three ac current feedback sensors, and sophisticated current controllers which can be expected to produce adverse interactions between phases if the load has no-neutral connection [41].

The last scheme is based on CSI. The six-step CSI is preferred in medium to high power industrial drives, particularly in traction applications [31]. To improve the CSI performance and reduce low order current harmonics, fixed modulation patterns have been successfully introduced [44].

The simultaneous PWM control of the front end controlled rectifier and the CSI stages will be introduced and discussed in Chapter 5 [21]. Basically, this power conversion system consists of a

PWM-CR interconnected with a PWM-CSI. The generalized ac/dc power conversion function studied in Chapter 2 is used twice in this power supply, for the PWM-CR and for the PWM-CSI.

When compared with a diode rectifier PWM-VSI, a PWM CR-CSI system possesses a number of intrinsic advantages based primarily on its natural current shoot-through protection and reverse power flow capability. However, severe restrictions on the type of load to be used, have to be imposed in order to realize an efficient design of the converter. In fact, a three phase balanced load is required for a good design. This type of load, though restrictive, is encountered in a large family of applications which include ac drives.

Another system design requirement is to utilize improved PWM techniques such as the modified sinusoidal PWM [21] [46] at a chopping frequency over 1 KHz. Specifically, a chopping frequency of 1.38 KHz (well within the range of available gate turn-off devices), ensures:

i) low order harmonics free dc link operation, thus reducing considerably the size of the bulky dc link reactor employed by six-step CSI's,

ii) sinusoidal output currents, thus improving the ac motor performance, and

iii) sinusoidal input currents, thus improving the input power factor and reducing the EMI.

Furthermore, any fault in the inverter side can be cleared by rectifier gate control. Linear operation and controlled regeneration

become natural for the PWM-CR supplying the continous current demanded by the CSI. Finally, the PWM-CR can control load variations by the means of a single dc link feedback. This feature cannot be accomplished using PWM-VSI due to the presence of flywheel diodes.

The subject of the power supply concept, together with its analysis, design, operating characteristics, and experimental results are presented in Chapter 5 [21].

CHAPTER 2

POWER CONVERTER ANALYSIS

2.1 Introduction

Cost effective switch mode power supplies must be compact, lightweight, and capable of processing a large amount of power per unit volume. Yet power supplies have to be reliable and operable for long intervals without maintenance. Therefore, to specify design and evaluate cost for effective power supply topologies, exhaustive analysis taking into consideration respective performance criteria is required.

The objective of this Chapter is the development of a functional mathematical model suitable for the analysis and evaluation of improved power supply topologies presented in subsequent Chapters. The proposed model covers and unifies the ac/dc and dc/ac power conversion functions required throughout this thesis. However, the concepts developed are general, and therefore, not restricted to these functions alone. The proposed model is obtained following a functional approach (see subsection 2.1.1). Moreover, the model is based on the definition of a transfer function for switch mode converters. This concept can be regarded as the generalized extension of the optimum gain function developed in [18] (the scope of this switch mode converter transfer function is given in subsection 2.1.2). Specifically, the converter model developed in this chapter can be used to study the behaviour of

voltage and current source inverters (dc/ac), and controlled rectifiers (ac/dc) simultaneously.

In addition to the converter model, this chapter includes respective generalized input-output converter waveforms and respective generalized spectra. This information is essential in the design of converters and respective input-output converter filters. This chapter also includes generalized design data for switch ratings and filters.

The transfer function of switch mode converters introduced in this chapter, enables:

i) the study of the duality between voltage and current converters and their waveform reciprocity,

ii) the generalized comparison of PWM control schemes,

iii) the analysis of converters in groups according to function instead of the analysis of individual converters,

iv) the modular study of systems with multiple switch mode converters,

v) a more systematic design approach for switch mode converter systems.

2.1.1 Functional Analysis Approach

The functional analysis approach treats power converters according their specific power conversion function. This function can be defined regardless of the specific application and/or circuit configuration. Table (2.1) shows a functional classification of some

important power converters.

As shown next, the ac/dc power conversion group of converters includes the controlled rectifiers and both voltage and current source inverters. Rectifiers are used to convert ac power into dc power while inverters are intended to do precisely the reverse, that is, the conversion of dc power into ac power. Therefore, they appear to perform different functions. However, when these converters operate under regeneration (reverse power flow) they also perform their reverse function. For example, rectifiers under regeneration convert dc into ac, while, inverters under regeneration convert ac into dc. Therefore, rectifiers can be also viewed and analysed as inverters and inverters as rectifiers. This point of view has been incorporated in the subject analysis approach. As a result, three major (and previously considered independent) classical converter types (controlled rectifiers, current source inverters and voltage source inverters) have been classified as one converter family that performs a common ac/dc or dc/ac function (Table (2.1)). The fact that these three converter types share identical transfer functions and thereby, can have identical input output waveforms is also to be shown. Moreover, a perfect electrical duality is found for current and voltage source converters. In fact, current and voltage variables in current source converters, have a one-to-one correspondance, with voltage and current variables in voltage source converters respectively.

FUNCTION	CONVERTER TYPE
ac/dc	controlled rectifiers current source inverters voltage source inverters
dc/dc	choppers
ac/ac.	frequency changers voltage controllers

Table (2.1): Functional classification of power converters.

2.1.2 The Transfer Function of Switch Mode Converters

The transfer function is widely used in Electrical Engineering in connection with the input-output transfer characteristics of linear systems, and for the investigation of their respective static and dynamic behaviours. Typically, transfer functions are used with linear, stationary (constant parameter) systems. Also, since a transfer function provides an input-output description of a system, it does not include any information concerning the internal structure of

the system. Naturally, the classical definition of the transfer function of linear systems is not applicable to the study of the highly nonlinear switch mode converters. However, the idea of describing the input-output behaviour of a system, regardless of its internal structure, is exploited in this chapter in order to define transfer functions for switch mode converters. This description of the converter behaviour is of tremendous relevance in power electronics. In particular, input-output converter waveforms are required:

i) for the design of input-output filters,

ii) to predict load waveforms,

iii) to predict system input currents,

iv) to estimate the degree of utilization of system components (utilization factors),

v) and to study systems with multiple stages of power conversion.

Furthermore, the idea of a suitable transfer function which is independent of the converter's internal structure allows the designer to decompose the synthesis of a power converter system into three major steps:

i) the derivation of the converter transfer function from the task to be performed by the converter,

ii) the synthesis of topologies to realize the required transfer function,

iii) the determination of the gating strategy required to produce the transfer function i) with the topology derived in ii).

The converter transfer function can be used to compute a dependent variable in terms of its respective independent converter variable. For example, the input current of a voltage source inverter (dependent input) depends on the converter transfer function and the converter output line currents (independent output). Dependent switch mode converter variables [16] depend on two factors: on the method by which the converter switches are controlled (i.e. gating signals), and also on the independent power sources (e.g. input utility voltages of a rectifier) or ideal sink sources (e.g. continuous dc output load current on a rectifier).

A summary of converter independent and dependent variables is presented in Table (2.2). This Table considers the port connected to the source of power (e.g. utility, batteries) as the input converter port, and the port connected to the load as output port.

Consequently, with the description of dependent variables, the transfer function of a switch mode converter is for convenience defined here as,

$$\text{converter transfer function} = \frac{\text{converter dependent variable}}{\text{converter independent variable}} \qquad (2.1)$$

To fully specify the power conversion process in a switch mode converter (power=[voltage][current]), it is required to compute both current and voltage at the input and output ports. By applying (2.1)

to Table(2.2), it is concluded that a transfer function for voltage and a transfer function for current is defined for every converter type. The fact that a unique (valid for voltage and current) transfer function can be found for the group of converters that perform the ac/dc conversion function is yet to be shown.

CONVERTER TYPE	PORT	CURRENT VARIABLE	VOLTAGE VARIABLE
controlled rectifier	input	dependent	independent
	output	independent	dependent
current source inverter	input	independent	dependent
	output	dependent	independent
voltage source inverter	input	dependent	independent
	output	independent	dependent

Table (2.2): Electrical variable classification for the ac/dc functional family.

2.2 Pulse Width Modulation of Converters

The practical realization of a switch mode converter transfer function is accomplished using pulse width modulation PWM [23] [27] [46] [47]. PWM in power converters refers to the synthesis of a desired voltage/current waveform by pulses of variable width in such a way that the average value of the modulated waveform has the same shape as a given reference waveform. Consequently, a sinusoidal reference will produce a modulated waveform which has a sinusoidal "average" waveform (and also some inherent but undesirable harmonics).

As stated in section (2.1), for a specific power conversion task the relationship between dependent and independent variables is given by the transfer function. The waveform subjected to modulation is the independent variable (e.g. input voltage in a voltage source inverter). The modulated waveform is the dependent variable (e.g. the output voltage of a voltage source inverter). Therefore, considering the definition of transfer function (2.1), it can be seen that a full analytical description of the modulation process is provided in the transfer function. Therefore, from the transfer function standpoint, power converters can be regarded as modulators.

An explicit mathematical representation of the transfer function (or modulator action) requires an explicit representation of the modulated (dependent) waveform and the unmodulated (independent) waveform. Fig.(2.1a) and Fig.(2.1b) show a typical pulse width modulated waveform and its associated harmonic spectrum. The specific modulation technique employed to determine the waveform of Fig.(2.1a),

x(t), is called sine PWM [23]. This thesis examines various modulation techniques and provides the criteria for selecting them depending on specific applications.

Fig.(2.1) suggests two possible mathematical representations for x(t) (modulated or dependent waveform). The first based in Fig.(2.1a) as follows:

$$x(t) = X \sum_{k=1}^{12} (-1)^{k+r} u(t-t_k); \quad \begin{matrix} 1<k<6, & r=1 \\ 7<k<12, & r=0 \end{matrix} \qquad (2.2)$$

This approach of specifying x(t) is convenient for time domain analysis and therefore can be used with the converter model whenever transient analysis is required. The second mathematical expression derived from Fig.(2.1b) as the Fourier series expansion of x(t) as follows:

$$x(t) = X \sum_{n=1}^{\infty} a_n \cos(n\omega t) \qquad (2.3)$$

The Fourier series expansion of x(t) is useful in frequency domain type of analysis and has been extensively used to predict steady state converter behaviour [15] [16] [18] [20]. Whether (2.2) or (2.3) is used, it is clear that a mathematical representation of the converter transfer function can be defined on the basis of (2.1) as:

$$F(t) = \frac{x(t)}{X} \qquad (2.4)$$

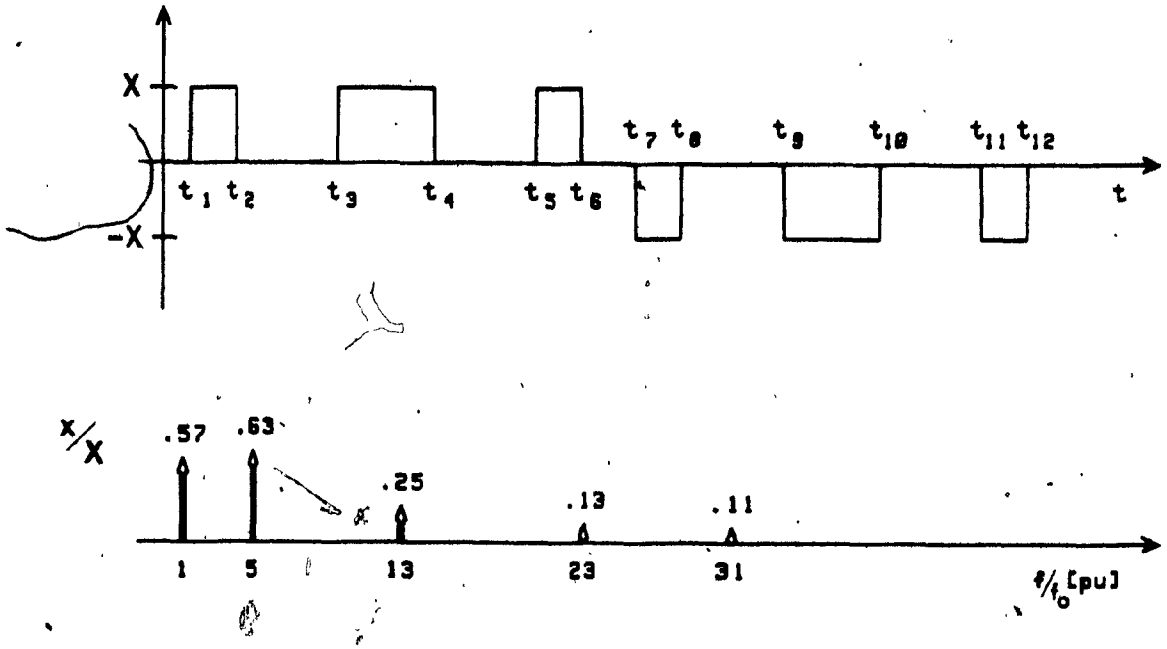


Fig.(2.1): SPWM waveform (a) and respective spectrum (b).

Sections (2.3), (2.4) and (2.5) develop specific relationships in order to define the VSI, CSI and CR common transfer function. Moreover, the subject transfer function is utilized to obtain explicit steady state common input-output waveforms encountered in the ac/dc group of converters. Moreover, Appendix 1 provides computer subprograms for the time and frequency domain solutions of two PWM techniques, namely, SPWM [23] and modified SPWM [46].

2.3 Voltage Source Inverter Transfer Function

Considering (2.1) and Table (2.2) it can be concluded that each converter type (VSI, CSI, CR) can have at least two expressions for its respective transfer function. One for voltage and the other for current variables. Moreover, different transfer function expressions result by either choosing line currents instead of phase currents to define the current transfer function or by choosing phase voltages instead of line voltages to define the voltage transfer function. However, by choosing the independent and dependent variables in a particular way (i.e. phase currents and line voltages in a VSI) it is possible to find a common transfer function for both currents and voltages, thus simplifying the analysis.

For VSI's the voltage transfer function relates input dc voltage with output ac voltage. Also, the current transfer function relates output phase current with respective input dc link current. As stated,

a common transfer function expression valid for current and voltage can be found. This transfer function will be called bidirectional in the sense that relates input to output (voltages) and output to input (currents).

2.3.1 VSI Voltage Transfer Function

From Table (2.2) the VSI voltage transfer function can be defined by the ratio between the PWM output voltage (dependent variable) and the input voltage (independent variable). Fig.(2.2) shows a 3Ø-VSI schematic diagram and respective input-output variables. The input dc source is represented by an ideal dc source.

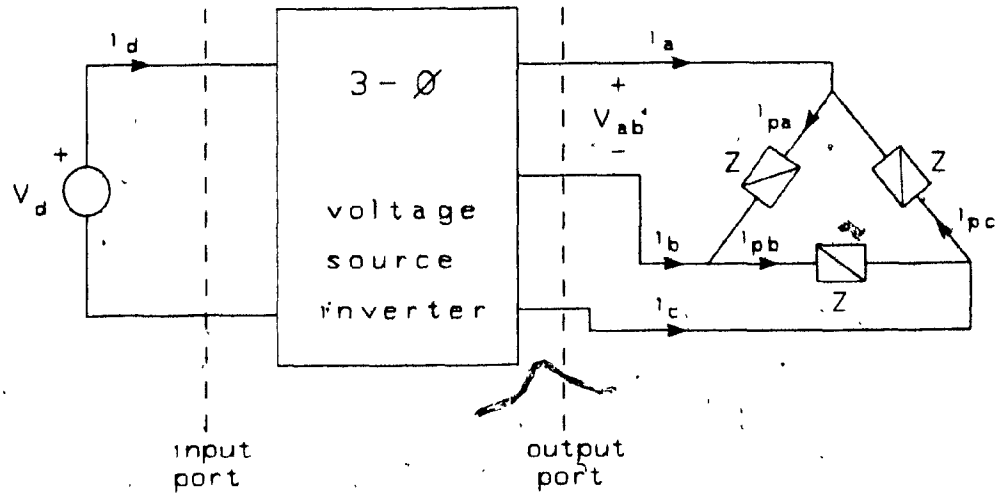


Fig.(2.2): 3Ø-VSI schematic diagram.

By choosing the output line voltages as the VSI output dependent

variables (Fig.(2.1a)) the voltage transfer function of a VSI becomes:

$$\bar{S}_v = \frac{\bar{v}_\ell}{v_d} = \frac{[v_{ab}, v_{bc}, v_{ca}]}{v_d} \qquad (2.5)$$

Specific steady state assumptions are next considered. These assumptions are required to compute typical input-output waveforms. Since, modern PWM VSI should have a dc voltage ripple with a total harmonic distortion (THD) eqn.(2.6) figure smaller than 5%:

$$THD = \frac{100}{a_1} \left(\sum_{i=2}^{\infty} (a_i)^2 \right)^{1/2} [\%] \qquad (2.6)$$

it is reasonable to assume that a small amount of dc ripple (THD 5%) will have a negligible influence on the output dependent variables. Consequently, the input inverter voltage (independent variable) is assumed to be constant for steady state analysis in this chapter. The validity of this assumption used in converter simulation has been cross checked against experimental results [21] [22] [24] [30].

$$v_d = E \qquad (2.7a)$$

and

$$[v_{ab}, v_{bc}, v_{ca}] = E \cdot \bar{S}_v \qquad (2.7b)$$

2.3.2 VSI Current Transfer Function

From Table (2.2) the VSI output currents are independent

variables and the VSI input current (i_d) is a dependent variable. Therefore, by applying (2.1) (and choosing the output phase currents as independent variables) the current transfer function becomes:

$$i_d = \bar{S}_i \cdot \bar{i}_p^T \tag{2.8a}$$

or by components:

$$i_d = [S_{ia}, S_{ib}, S_{ic}] \cdot [i_{pa}, i_{pb}, i_{pc}]^T \tag{2.8b}$$

Furthermore, assuming a converter without losses, the input instantaneous power is equal to the output instantaneous power. Therefore,

$$v_d \cdot i_d = \bar{v}_\ell \cdot \bar{i}_p^T \tag{2.9}$$

replacing (2.8a),(2.5) into (2.9),

$$v_d \cdot \bar{S}_i \cdot \bar{i}_p^T = v_d \cdot \bar{S}_v \cdot \bar{i}_p^T \tag{2.10}$$

An inspection of (2.10) reveals that $\bar{S}_i$ (2.8a) is identical to $\bar{S}_v$ (2.7a). Therefore, there is a bidirectional transfer function $\bar{S}$ that can be applied to compute both dependent variables (current and voltage) in VSI's.

$$\bar{S} = \bar{S}_i = \bar{S}_v \tag{2.11}$$

and using (2.11) and (2.5) the bidirectional transfer function $\bar{S}$ can

be defined as,

$$\bar{S} = \frac{\bar{v}_\ell}{v_d} \qquad (2.12)$$

$\bar{S}$ is bidirectional in the sense that it relates input to output ($\bar{S}_v$) and output to input ($\bar{S}_i$).

2.3.3. VSI Steady State Input Current

The input current is determined using (2.8) and the output phase currents (Fig.(2.2)). This expression (2.8) can be used for transient and steady state analysis. Consider steady state conditions for the establishment of typical generalized input current waveforms for a PWM-VSI. Steady state waveforms are relevant because they provide the basic information for PWM technique evaluation, filter design data, and converter ratings. A powerful simplifying assumption, for steady-state analysis would consider the independent VSI output current ($\bar{i}_p$) to be sinusoidal, that is, perfectly filtered. This assumption is valid because the high order harmonics present in the VSI PWM output voltages are attenuated to meet standard THD specifications (THD 5%). Such a THD figure guarantees that the ripple in the output phase current will have a negligible effect on the input dc current [24] and therefore can be neglected when computing the steady-state VSI input current. The sinusoidal phase current (fundamental of the output phase current) can be obtained with reference to Fig.(2.2) and (2.12) as follows:

$$\bar{i}_{p,1} = \frac{\bar{v}_{\ell,1}}{Z(\omega_o)} \qquad (2.13a)$$

or

$$i_{p,1} = \frac{\bar{S}_1}{E \cdot Z(\omega_o)} \qquad (2.13b)$$

and the input current (2.8a) becomes:

$$i_d = \frac{\bar{S} \cdot \bar{S}_1^T}{E \cdot Z(\omega_o)} \qquad (2.14)$$

2.4 Current Source Inverter Transfer Function

The method of the previous section can be used to determine the current and voltage transfer functions for the CSI type of converters.

2.4.1 CSI Current Transfer Function

From Table (2.2) the CSI current transfer function can be defined by the ratio between the PWM output current (dependent variable) and the input current (independent variable). Fig.(2.3) shows a 3Ø-CSI schematic diagram and respective input-output variables. The input current is represented by an ideal current source of magnitude i_d.

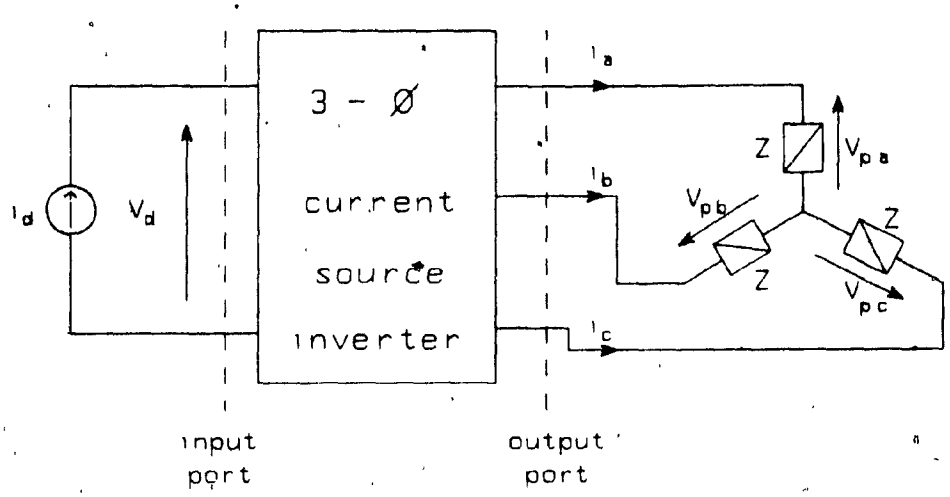


Fig.(2.3): 3Ø-CSI schematic diagram.

The output line currents of the CSI shown in Fig.(2.3) are PWM waveforms such as the one depicted by Fig.(2.1a). The CSI current transfer function can be defined by choosing the output line currents (as dependent variables) and the input current (as independent variable) as in (2.1),

$$\bar{C}_i = \frac{\bar{i}_\ell}{i_d} = \frac{[i_a, i_b, i_c]}{i_d} \qquad (2.15)$$

To obtain typical CSI line currents under steady state the dc input current is assumed constant. Basically, the same assumption is used for VSI under steady state in the previous section (i.e. constant dc

input voltage)

$$i_d = I \tag{2.16a}$$

and therefore,

$$[i_a, i_b, i_c] = I \cdot \bar{C}_i \tag{2.16b}$$

2.4.2 CSI Voltage Transfer Function

Applying the transfer function definition (2.1) and Table (2.2) (choosing phase voltages as dependent variables) the voltage transfer function $\bar{C}_v$ becomes:

$$v_d = \bar{C}_v \cdot \bar{v}_p^T \tag{2.17a}$$

$$v_d = [C_{va}, C_{vb}, C_{vc}] \cdot [v_{pa}, v_{pb}, v_{pc}] \tag{2.17b}$$

Furthermore, by equating input and output power the CSI voltage transfer function $\bar{C}_v$ can be related to the CSI current transfer function $\bar{C}_i$. Assuming a converter without losses, the input instantaneous power is equal to the output instantaneous power. Therefore,

$$i_d \cdot v_d = \bar{i}_\ell \cdot \bar{v}_p^T \tag{2.18}$$

replacing (2.17a) and (2.15) into (2.18),

$$i_d \cdot \bar{C}_v \cdot \bar{v}_p^T = i_d \cdot \bar{C}_i \cdot \bar{v}_p^T \tag{2.19}$$

by inspection of (2.19) it can be concluded that the $\bar{C}_v$ (2.17a) is

identical to the $\bar{C}_1$ (2.15). Therefore, there is a bidirectional transfer function $\bar{C}$ that can be applied to compute both types of dependent variables (i.e. current and voltage) in VSI.

$$\bar{C} = \bar{C}_v = \bar{C}_i \tag{2.20}$$

Using (2.20) and (2.15) the bidirectional transfer function $\bar{C}$ is defined as:

$$\bar{C} = \frac{\bar{i}_\ell}{i_d} \tag{2.21}$$

2.4.3 CSI Steady State Input Voltage

The input voltage can be determined using (2.17a) and the output phase voltages. Reasoning similar to the one that allows the assumption of sinusoidal waveforms for the steady-state output phase currents in a VSI (when computing the input current) can be also applied in CSI analysis. For the CSI case the output phase voltages can be assumed purely sinusoidal [21] [30] when computing the CSI steady state input voltage. Therefore, considering only the fundamental of $\bar{i}_1$ and the circuit of Fig.(2.3),

$$\bar{v}_{p,1} = \bar{i}_{\ell,1} \cdot Z(\omega_o) \tag{2.22a}$$

$$\bar{v}_{p,1} = \frac{\bar{C}_1}{I} \cdot Z(\omega_o) \tag{2.22b}$$

and the steady state input voltage (2.17a) becomes,

$$v_d = \bar{C} \cdot \bar{C}_1^T \left(\frac{Z(\omega_o)}{I}\right) \tag{2.23}$$

2.5 PWM Controlled Rectifier Transfer Function

2.5.1 CR Current Transfer Function

From Tables (2.2) and (2.1) the CR current transfer function can be defined by the ratio between the PWM input current (dependent variable) and the dc output current (independent variable)..

Fig.(2.4) shows a 3Ø-CR schematic diagram and respective input output variables. The CR output current is represented in Fig.(2.4) by an ideal current source of magnitude i_d.

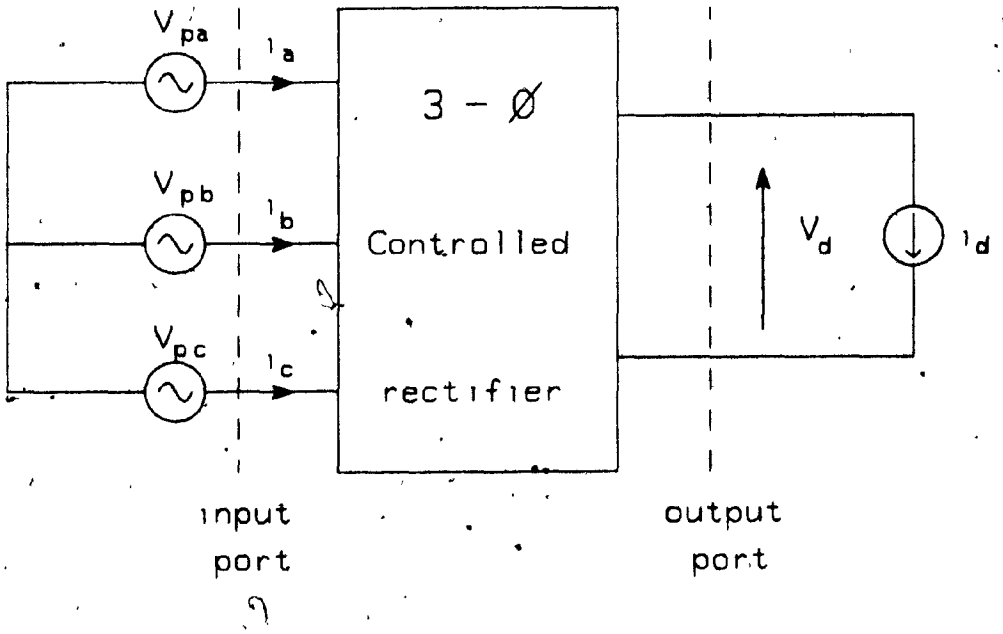


Fig.(2.4): 3Ø-CR schematic diagram.

In this case the current transfer function becomes,

$$\bar{R}_i = \frac{\bar{i}_\ell}{i_d} = \frac{[i_a, i_b, i_c]}{i_d} \qquad (2.24)$$

Also, in the analysis of VSI and CSI converters it has been assumed (for steady state) that the independent variable of the dc side of the converter is ripple free. Correspondingly, in PWM CR steady state analysis the dc output current can be assumed constant (ripple free dc). This assumption is valid because when using PWM in CR the task of filtering becomes quite simple, with the output being typically a smooth (almost ripple free) dc current. Moreover, this assumption is routinely used even in the analysis of six step CR where current filtering becomes more critical [10] [11] [14]. Therefore for steady state,

$$i_d = I \qquad (2.25a)$$

therefore,

$$[i_a, i_b, i_c] = I \cdot \bar{R}_i \qquad (2.25b)$$

2.5.2 CR Voltage Transfer Function

By applying the transfer function definition (2.1) and Table (2.2), the voltage transfer function $\bar{R}_v$ can be defined as,

$$v_d = \bar{R}_v \cdot \bar{v}_p^T \qquad (2.26a)$$

$$v_d = [R_{va}, R_{vb}, R_{vc}] \cdot [v_{pa}, v_{pb}, v_{pc}]^T \qquad (2.26b)$$

Also, assuning a converter without losses, the input instantaneous

power is equal to the output instantaneous power. Therefore,

$$i_d \cdot v_d = \bar{i}_\ell \cdot \bar{v}_p^T \tag{2.27}$$

replacing (2.26a) and (2.24) into (2.27),

$$i_d \cdot \bar{R}_v \cdot \bar{v}_p^T = i_d \cdot \bar{R}_i \cdot \bar{v}_p^T \tag{2.28}$$

An inspection of (2.28) will reveal that $\bar{R}_v$ (2.26a) is identical to $\bar{R}_i$ (2.24). Therefore, there is a bidirectional transfer function $\bar{R}$ that can be applied to compute both types of dependent variables (i.e. voltage and current) in CR's.

$$R = \bar{R}_v = \bar{R}_i \tag{2.29}$$

and using (2.29) and (2.24) the bidirectional transfer function for CR becomes:

$$\bar{R} = \frac{\bar{i}_\ell}{i_d} \tag{2.30}$$

2.5.3 CR Output Voltage

The output voltage of a CR can be determined using (2.26a) and the input phase voltages (normally the utility).

2.6 A UNIFIED FUNCTIONAL MODEL FOR VSI, CSI AND CR.

The functional commonality between VSI, CSI and CR together with the set of input output relations developed throughout sections (2.3), (2.4) and (2.5), are used in this section to show that a single model exists which can be used to describe the behaviour of this family of ac/dc converters.

2.6.1 Common Transfer Function.

The objective of this subsection is to show that the transfer functions derived earlier for each one of the VSI, CSI and CR converters ((2.12),(2.21),(2.30)) have been deliberately chosen to be identical. The advantage of such choice is that for analysis purposes all three types of converters merge into one, thus simplifying their analyses and designs.

To establish that the defined transfer functions are realizable the following (intuitively true) axiom is introduced "For any given transfer function whose resulting dependent current/voltage waveforms do not violate respective Kirchhof's laws, it is always possible to find a converter topology to implement the subject transfer function". Therefore, for each converter type under consideration (i.e. CR, CSI and VSI) there is at least one converter topology that can be used to realize a valid (i.e. respecting Kirchhof's laws) transfer function.

For a given modulation technique (e.g. sine PWM) the transfer functions defined by eqns.(2.12), (2.21) and (2.30), as the ratio of the dependent line PWM variable and the input dc independent variable,

are the normalized line PWM patterns of the given modulation, and thereby, the subject transfer functions are identical for such modulation. Therefore, for a valid line PWM pattern,

$$\bar{H} = \bar{S} = \bar{C} = \bar{R} \qquad (2.31)$$

Any valid line to line pattern (i.e. one where the instantaneous sum of the line variables is equal to zero) will define a realizable transfer function $\bar{H}$. Therefore applying the axiom, it will be always possible to find a topology for a CR, a CSI or a VSI which implements $\bar{H}$. It is worth noting that $\bar{H}$ can be used for both steady state and transient converter analysis.

From a classical viewpoint a common transfer function applicable to the analysis of VSI, CSI and CR is an unexpected result. However, this result is consistant with the functional classification of power converters (Table(2.2)). Moreover, from a practical viewpoint, and as mentioned earlier, a common transfer function enables the simultaneous analysis, design, and comparison of these converter types with the aid of a single functional model.

2.6.2 The Functional Model.

With a common transfer function $\bar{H}$ the expressions developed in sections (2.3), (2.4) and (2.5) relating dependent and independent variables constitute the basis of the common converter model. An additional step is to define a per-unit system (Table (2.3)) which allows the computation of per-unit generalized input-output waveforms.

As a result of this per-unit choice and the common transfer function (2.31), the one-to-one correspondence for all dependent and independent variables becones more apparent.

$E = 1$ pu	, VSI input voltage
$I = 1$ pu	, CSI input and CR output current
$Z(w_o)=1 \angle \emptyset$ pu	, fundamental load impedance (Fig.(2.2) and (2.3))
$V_p = a_1/\sqrt{3}$	, magnitude of mains phase voltage
	$a_1(\text{SPWM}, M=1) = \sqrt{3}/2$, Appendix 1
	$a_1(\text{MSPWM}, M=1) = 1$, Appendix 1

Table (2.3): Per-Unit System

Table (2.4) shows the common ac/dc normalized (in per-unit) functional model. This table presents general relations suitable for transient analysis (rows a and b) and simplified expressions valid for steady state conditions (rows c,d and e). To further illustrate the relevance of the simplified steady state relationships (and respective typical waveforms) a block diagram of the functional model valid for steady state is presented in Table (2.5).

The functional model of Table (2.4) has been developed by also assuming:

i) ideal semiconductors,

ii) negligible stray circuit resistance, inductance, and

	VSI	CSI	CR		
a	$\bar{v}_\ell(t)=\bar{H}(t)\circ v_d(t)$	$\bar{i}_\ell=\bar{H}(t)\circ i_d(t)$	$\bar{i}_\ell=\bar{H}(t)\circ i_d(t)$	(2.5) (2.15) (2.24)	GENERAL MODEL
b	$i_d(t)=\bar{H}(t)\circ\bar{i}_p^T(t)$	$v_d(t)=\bar{H}(t)\circ\bar{v}_p^T(t)$	$v_d(t)=\bar{H}(t)\circ\bar{v}_p^T(t)$	(2.8) (2.17 (2.26)	
c	$\bar{v}_\ell(t)=\bar{H}(t)$	$\bar{i}_\ell(t)=\bar{H}(t)$	$i_\ell(t)=\bar{H}(t)$	(2.5) (2.15) (2.24)	STEADY STATE
d	$\bar{i}_p(t)=\bar{H}_1(t-\tau)$	$\bar{v}_p(t)=\bar{H}_1(t+\tau)$	$\bar{v}_p(t)=\bar{H}_1(t)$	(2.13) (2.22)	GENERAL MODEL
e	$i_d(t)=\bar{H}\circ\bar{H}_1^T(t-\tau)$	$v_d(t)=\bar{H}(t)\circ\bar{H}_1^T(t+\tau)$	$v_d(t)=\bar{H}\circ\bar{H}_1^T(t)$	(2.14) (2.23) (2.26)	

$\tau = \frac{\phi}{\omega_o}$ ϕ: displacement angle introduced by the load impedance.

TABLE 2.4: Functional model for the ac/dc conversion function.

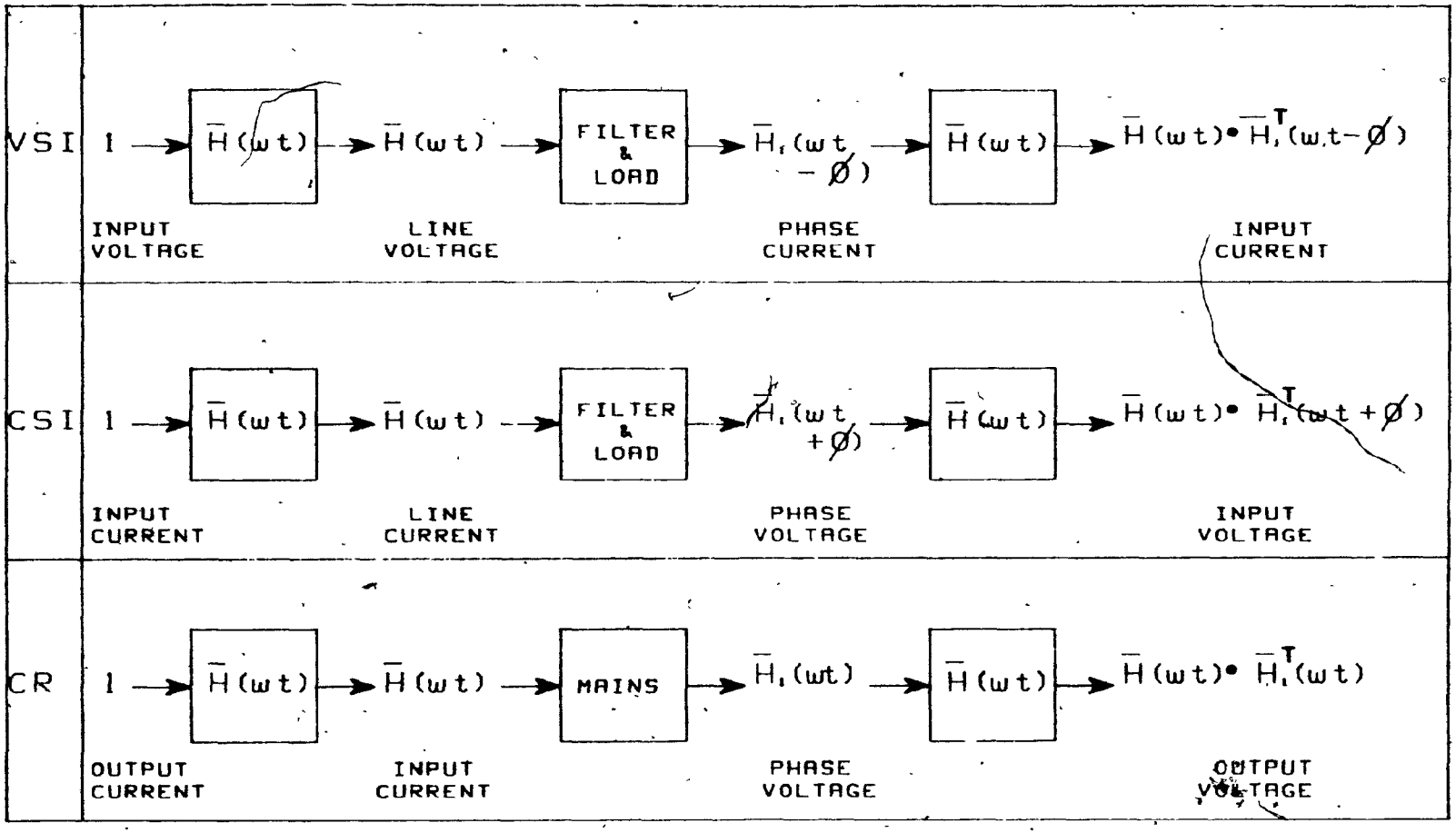


Table (2.5): Steady state block diagram of the functional model presented in Table (2.4).

capacitance,

iii) ideal operation of the converter control circuitry (perfect implementation of PWM techniques),

iv) balanced (amplitude and phase) sinusoidal ac input voltages.

Furthermore, the explicit expressions for VSI and CSI input dependent variables (i_d and v_d) are valid only under steady state ((2.14) and (2.23)). From a practical standpoint, the above set of assumptions doesn't constitute a severe restraint. In fact, in most of the situations the model describes the converter behaviour (and associated typical input-output waveforms) with a good degree of precision [21].

2.6.3 Generalized Converter Input-Output Waveforms

As stated in section (2.3.3) steady state waveforms provide the basic information to describe the converter behaviour, evaluate PWM techniques, design the input-output filter, and to specify the converter switch ratings.

The simplifying assumptions included here are:

i) constant independent dc link variables (i.e. VSI input voltage, CSI input current and CR output current),

ii) sinusoidal independent ac variables (i.e. VSI load phase currents, CSI load phase voltages and CR input phase voltages).

Fig's (2.5.1),(2.5.2),(2.5.3) and (2.6.1),(2.6.2),(2.6.3) show generalized input-output waveforms for the ac/dc power conversion function. Specifically, Fig's (2.5.1),(2.5.2) and (2.5.3) have been computed considering the sine PWM control scheme and Table(2.5) to show the ac side dependent variable H(wt) and the dc side dependent variable [H(wt)][H(wt-Ø)]. The same generalized waveforms are displayed in Fig's (2.6.1),(2.6.2) and (2.6.3) for a modified sine PWM [46].

The displacement angle Ø is defined as the phase displacement between the fundamental of the transfer function and the associated phase variable (e.g. phase load current in a VSI). A leading displacement angle (Ø<0) in the phase of a CSI (Fig's (2.5.1) and (2.6.1)) corresponds to the lead of the phase current with respect to the transfer (or normalized output line current) for an inductive load.

In VSI a leading displacement angle (Ø<0) corresponds to the lead of the phase current with respect to the transfer function (or normalized output line voltage) for a capacitive load (Fig's (2.5.1) and (2.6.1)). Lagging displacement angles for CSI and VSI are produced by capacitive and inductive loads, respectively (Fig's (2.5.3) and (2.6.3)). Inverter resistive loads Ø=0 and variable modulation controlled rectifiers (also Ø=0) produce the type of waveforms displayed in Fig's (2..5.2) and (2.6.2). Positive and negative displacement angles are also used in rectifiers as an alternative way

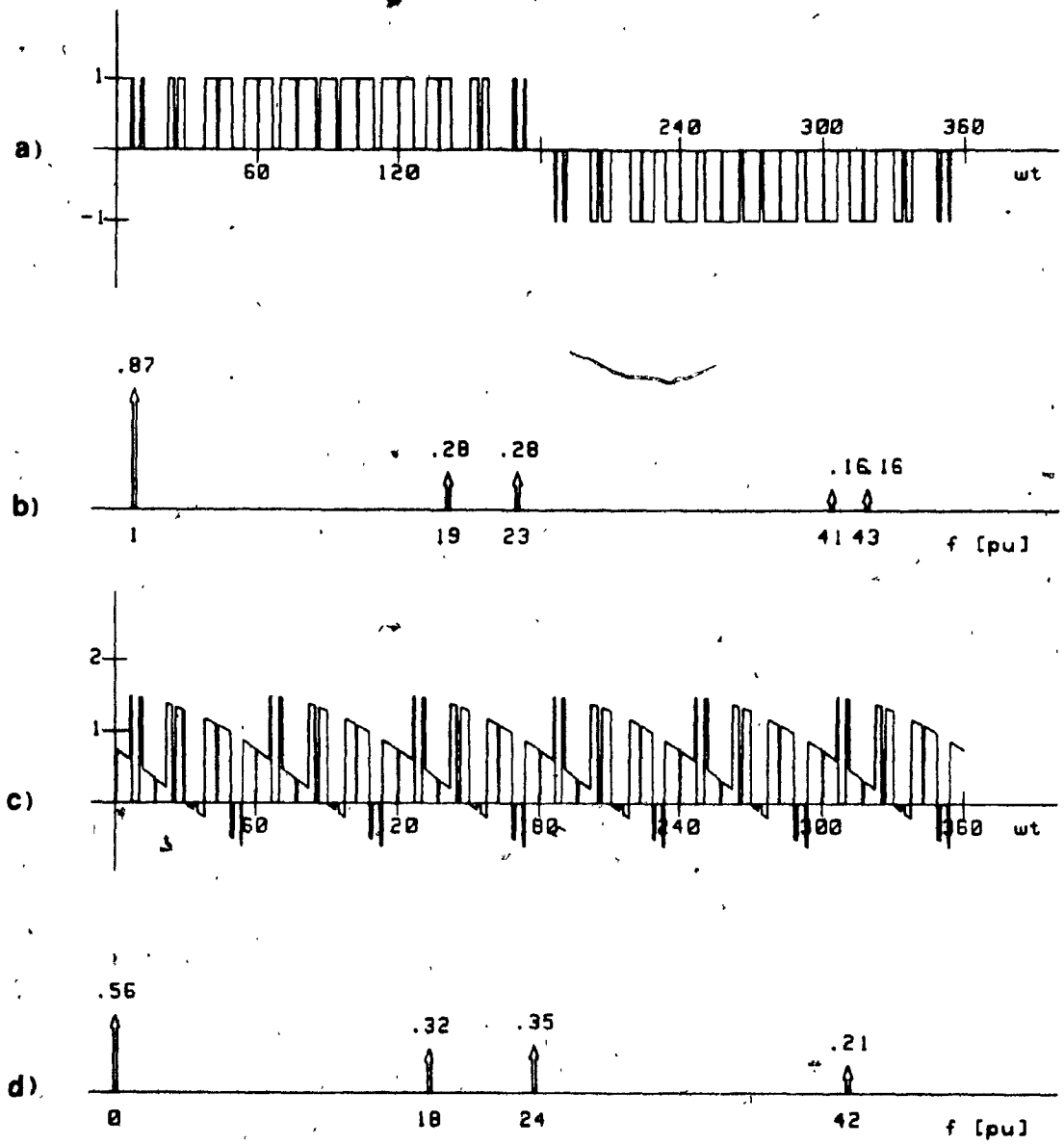


Fig.(2.5.1): Generalized waveforms for the ac/dc conversion function. SPWM control technique, M=1, $\phi<0$.
a) VSI output line voltage, CSI output line current or CR input line current.
b) Spectrum of a).
c) VSI input current, CSI input voltage or CR output voltage.
d) Spectrum of c).

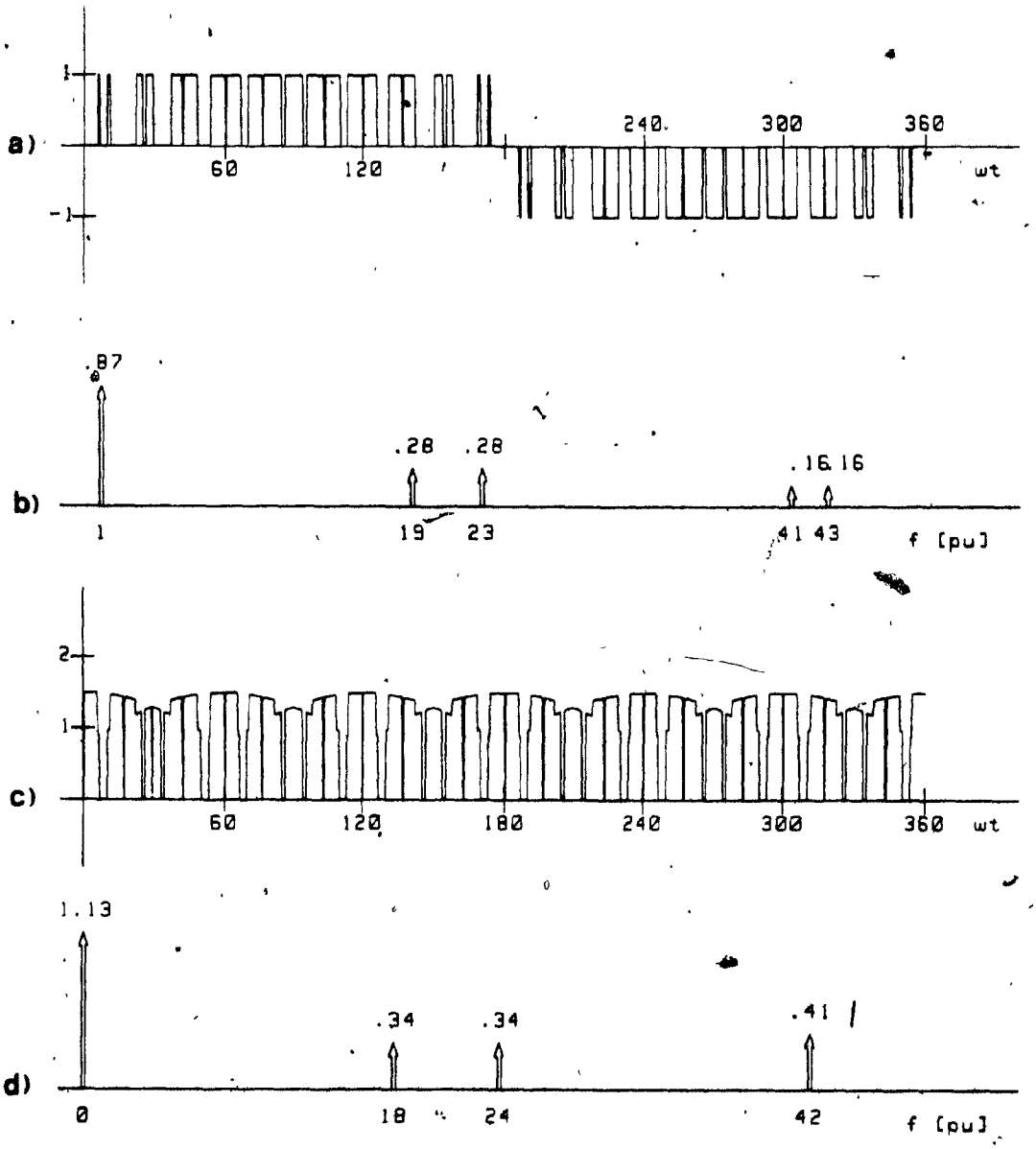


Fig.(2.5.2): Generalized waveforms for the ac/dc conversion function. SPWM control technique, M=1, ϕ=0.
a) VSI output line voltage, CSI output line current or CR input line current.
b) Spectrum of a).
c) VSI input current, CSI input voltage or CR output voltage.
d) Spectrum of c).

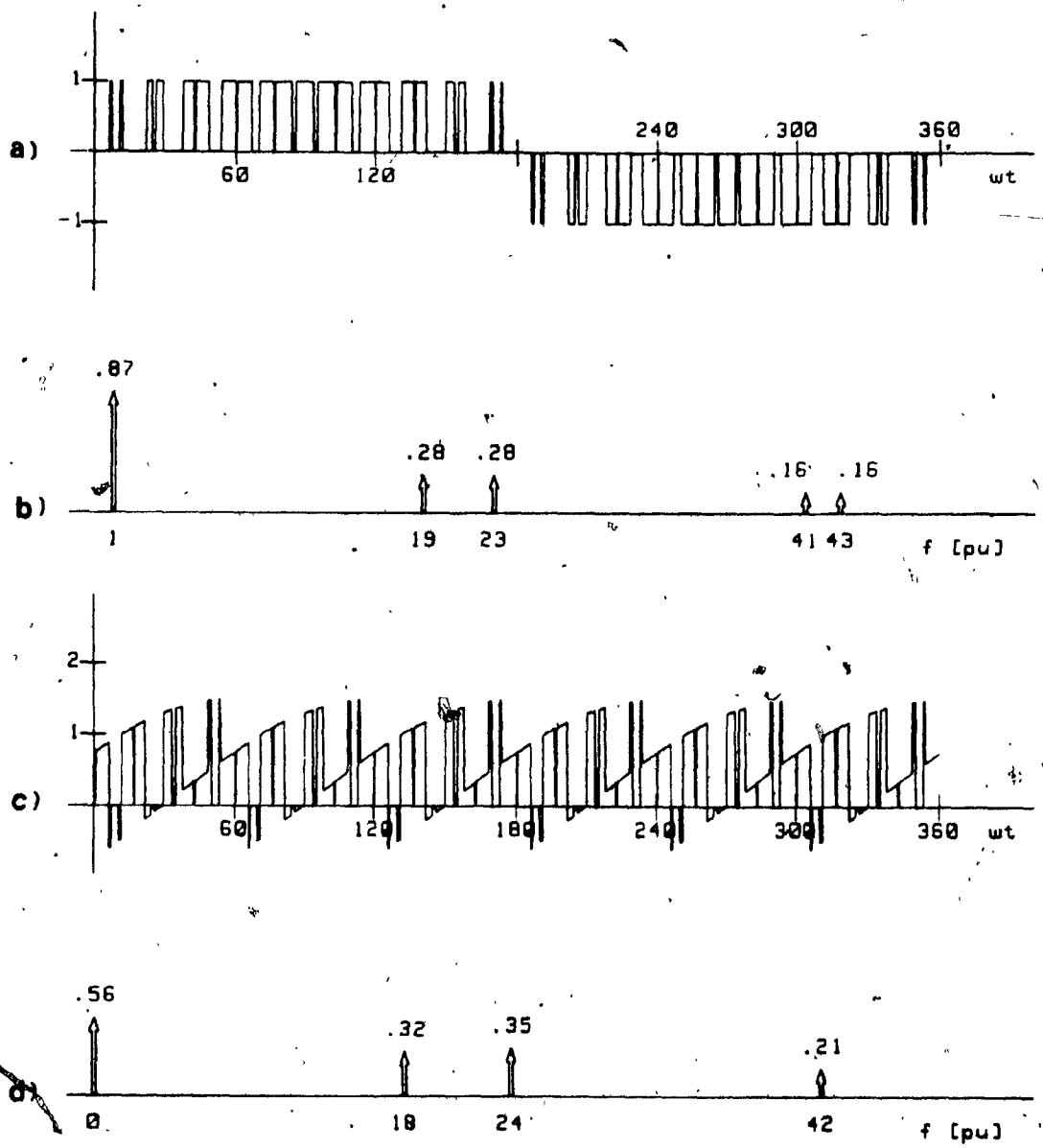


Fig.(2.5.3): Generalized waveforms for the ac/dc conversion function, SPWM control technique, M=1, $\phi \neq 0$.
a) VSI output line voltage, CSI output line current or CR input line current.
b) Spectrum of a).
c) VSI input current, CSI input voltage or CR output voltage.
d) Spectrum of c).

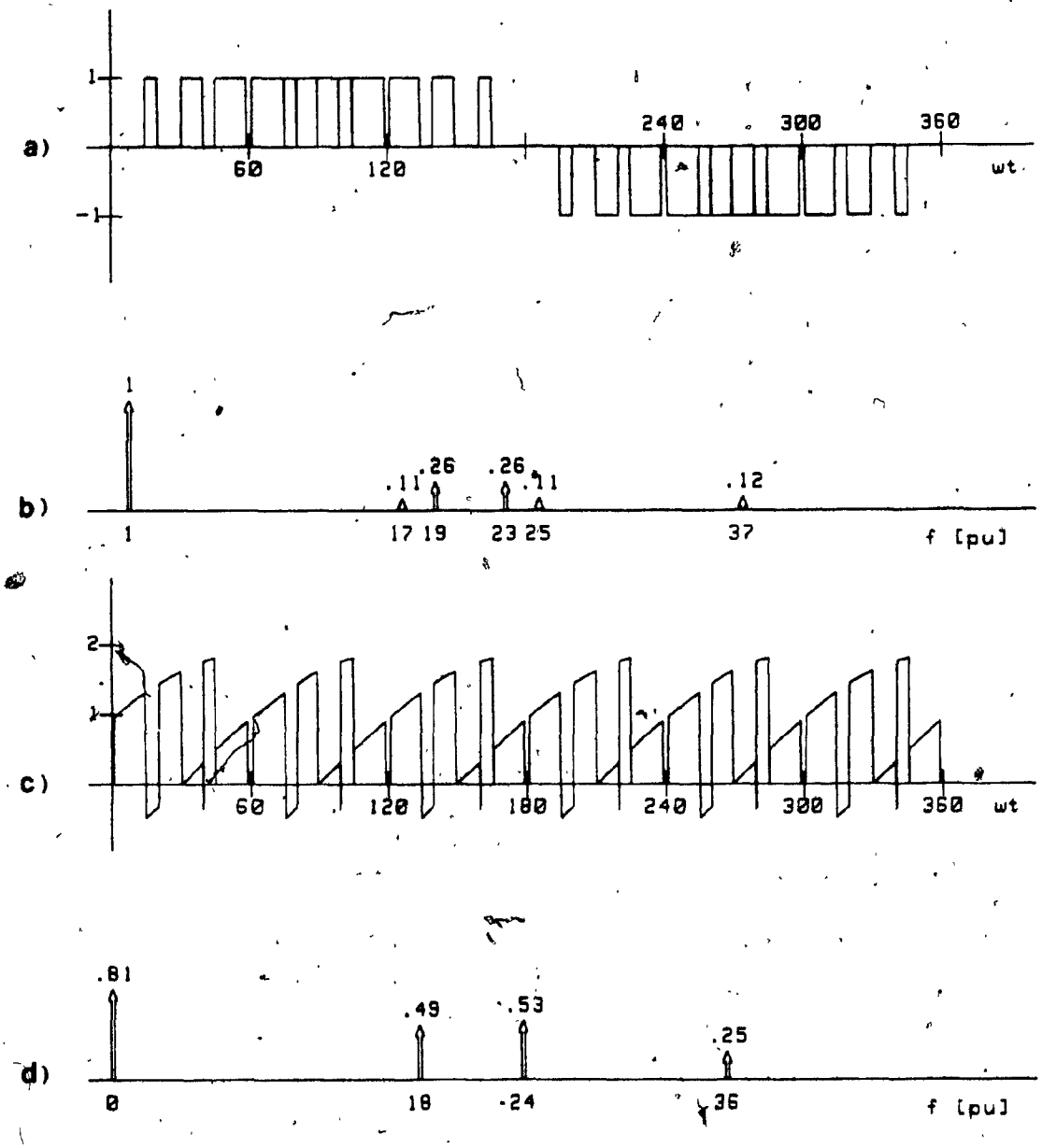


Fig.(2.6.1): Generalized waveforms for the ac/dc conversion function. MSPWM control technique, M=1, $\phi<0$.

a) VSI output line voltage, CSI output line current or CR line current.
b) Spectrum of a).
c) VSI input current, CSI input voltage or CR output voltage.
d) Spectrum of c).

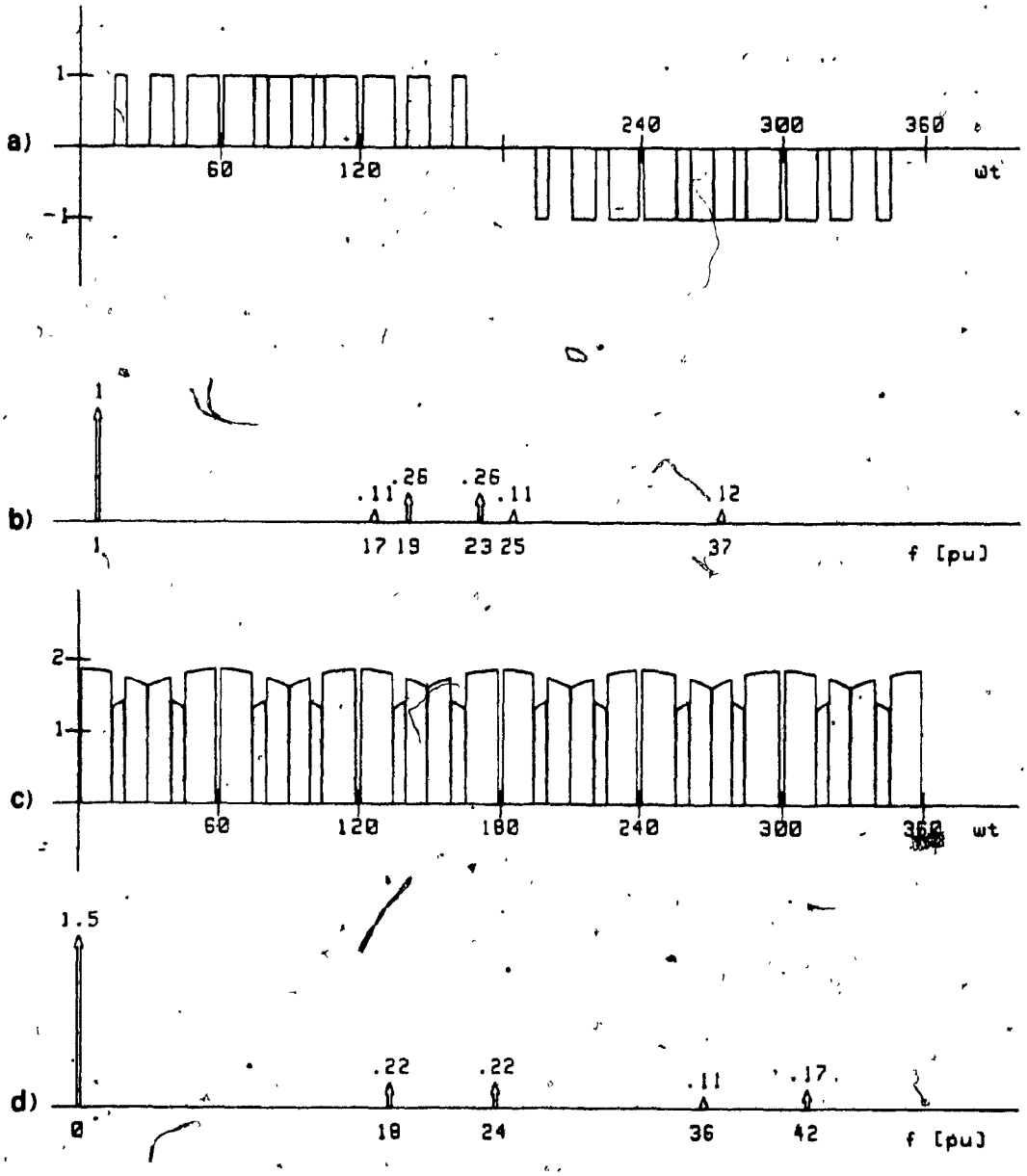


Fig.(2.6.2): Generalized waveforms for the ac/dc conversion function. MSPWM control technique, M=1, ϕ=0.

a) VSI output line voltage, CSI output line current or CR line current.
b) Spectrum of a).
c) VSI input current, CSI input voltage or CR output voltage.
d) Spectrum of c).

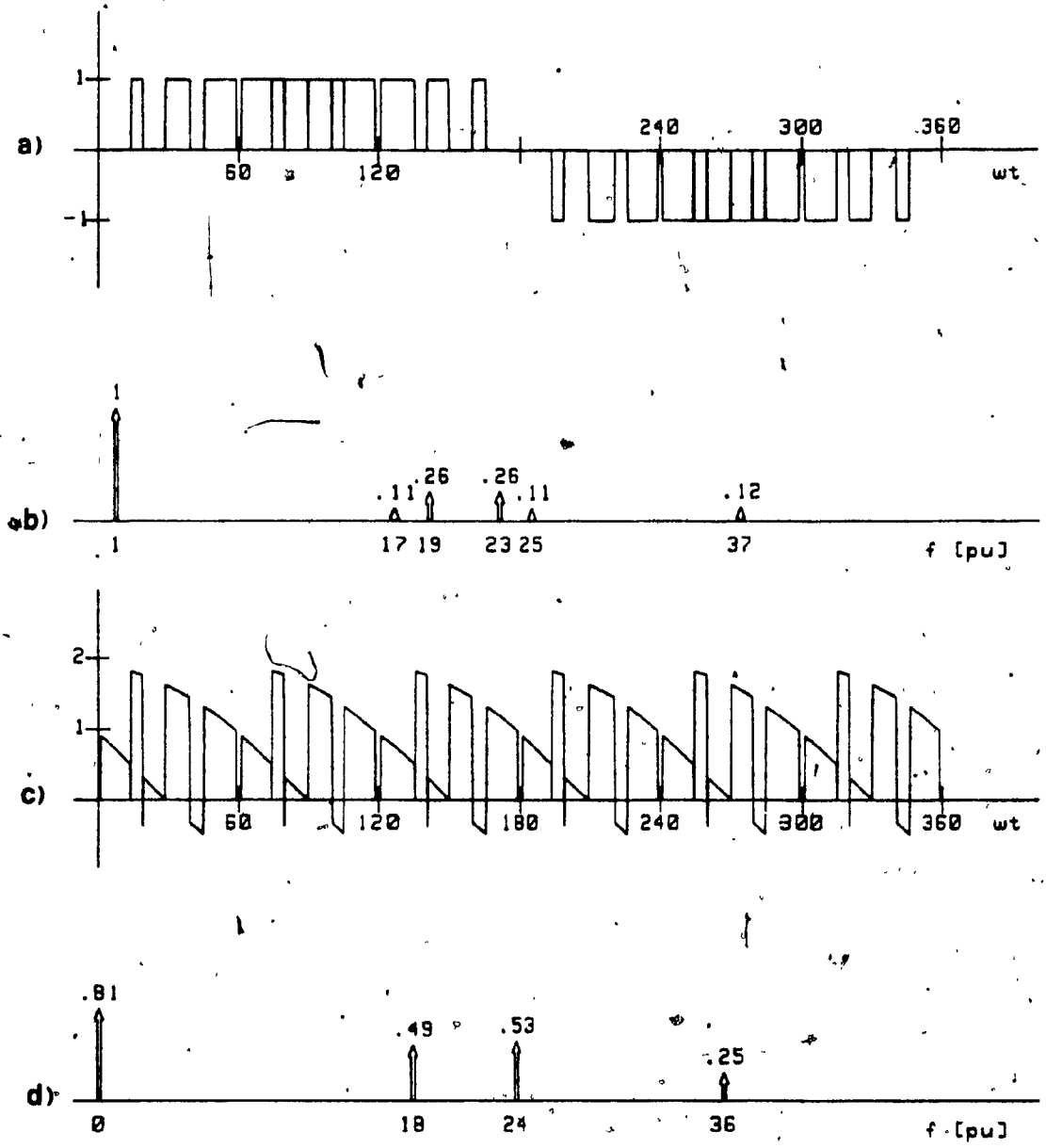


Fig.(2.6.3): Generalized waveforms for the ac/dc conversion function. MSPWM control technique, M=1, $\phi > 0$.

a) VSI output line voltage, CSI output line current or CR line current.
b) Spectrum of a).
c) VSI input current, CSI input voltage or CR output voltage.
d) Spectrum of c).

	DISPLACEMENT ANGLE ϕ		
	$\phi > 0$	$\phi = 0$	$\phi < 0$
VSI	INDUCTIVE LOAD	RESISTIVE LOAD	CAPACITIVE LOAD
CSI	CAPACITIVE LOAD	RESISTIVE LOAD	INDUCTIVE LOAD
CR	PHASE LAG	IN PHASE	PHASE LEAD

Table (2.6): Displacement angle possibilities of the ac/dc power conversion generalized waveforms (passive load under steady-state).

(to the variable modulation) of controlling the power. This mode of power control in rectifiers is denominated as "phase control". In this mode the angle between the utility and the transfer function (displacement angle) is varied to control the rectifier output power. The traditional line commutated six-step controlled rectifier uses a ($\emptyset$>0) controlled lag (firing angle or delay angle) of the transfer function with respect to the input phase voltages. Table (2.6) summarizes the different displacement angle situations (Fig's (2.5.1) to (2.6.3)) encountered in the ac/dc family of converters.

2.6.4 Input Output Converter Equivalent Circuits

The scope of the mathematical model can be extended beyond the computation of the input output waveforms with the definition of equivalent circuits for the input and output connected networks. Those equivalent circuits are constructed by replacing the power converter by ideal sources defined in Table(2.4). Furthermore, whenever it is possible in 3$\emptyset$-systems, it is important to work for analysis purposes with single phase equivalent networks. The following assumptions and consequent restrictions were considered in the development of the proposed equivalent circuits.

i) balanced 3$\emptyset$ filter-load networks,

ii) balanced PWM control techniques, and

iii) balanced initial conditions.

Therefore, the equivalent circuits next developed are valid only

per-phase equivalent networks, therefore the analysis is based on the complete three phase network. However, depending on the study to be performed, different simplifying assumptions can be established. Such a problem is addressed in Chapter 5 of this thesis in connection with the analysis of CSI under unbalance load conditions.

2.6.4.1 VSI Equivalent Circuits.

Considering Fig.(2.2) and the functional model of Table (2.3), the per-phase output equivalent circuit for a VSI is shown in Fig.(2.7)

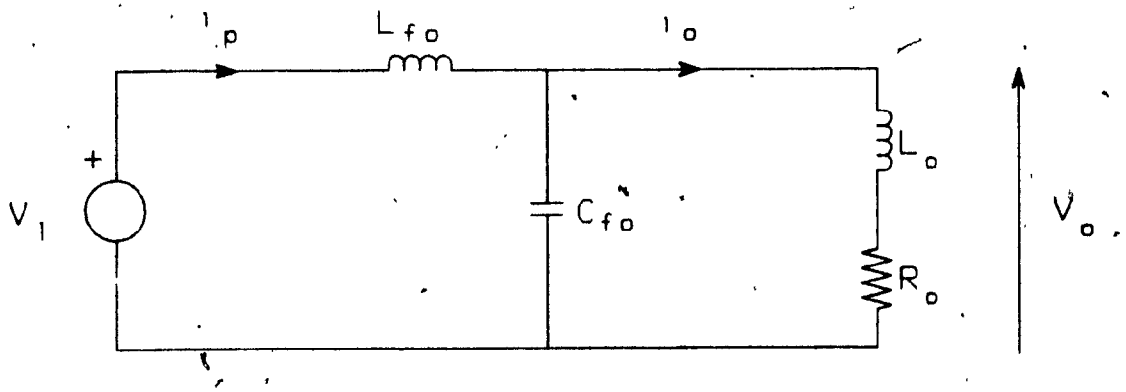


Fig.(2.7): VSI output equivalent circuit.

and the input equivalent circuit of a VSI is shown in Fig.(2.8),

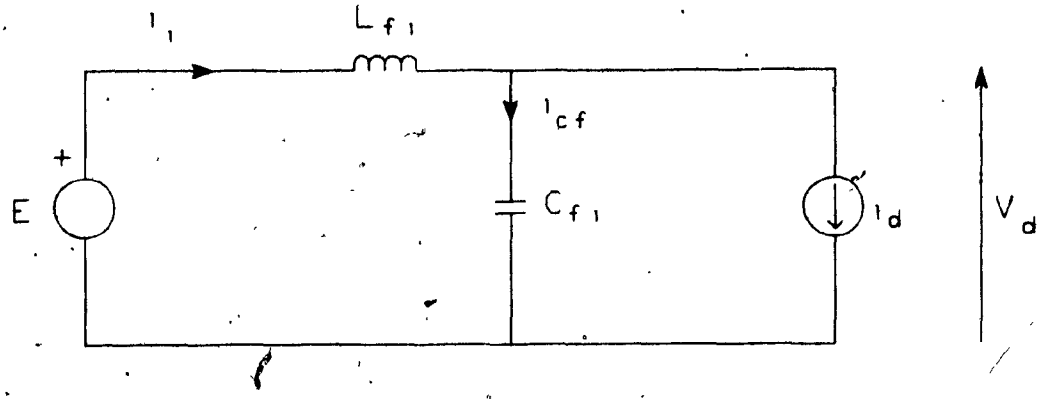


Fig.(2.8): VSI input equivalent circuit

2.6.4.2 CSI Equivalent Circuits

Considering Fig.(2.3) and the functional model of Table(2.3), the per-phase output equivalent circuit of a CSI is shown in Fig.(2.9),

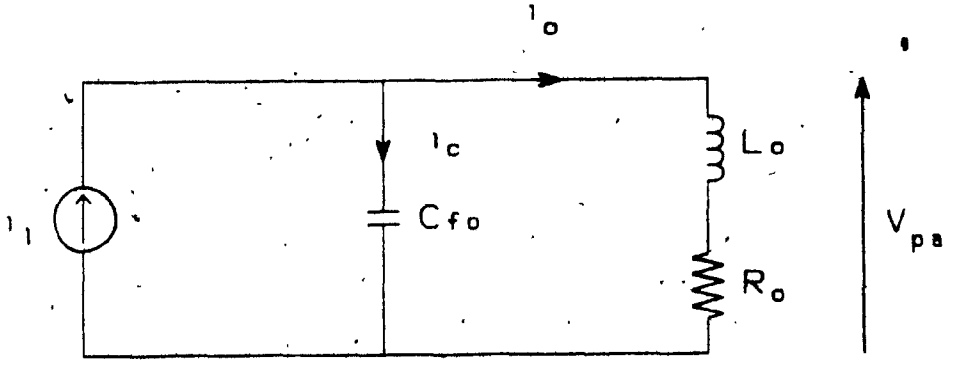


Fig.(2.9): CSI output equivalent circuit.

and the input equivalent circuit of a CSI is shown in Fig.(2.10),

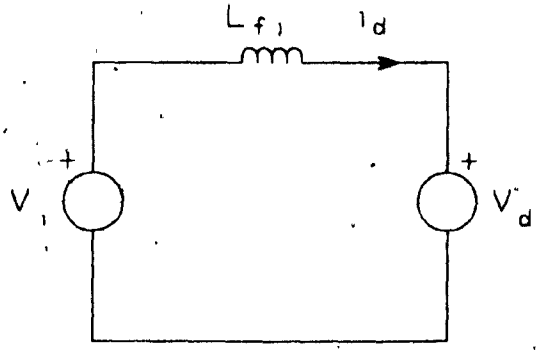


Fig.(2.10): CSI input equivalent circuit.

2.6.4.3 CR Equivalent Circuits

Considering Fig.(2.4) and the functional model of Table (2.3), the per-phase input equivalent circuit of a CR is shown in Fig.(2.11),

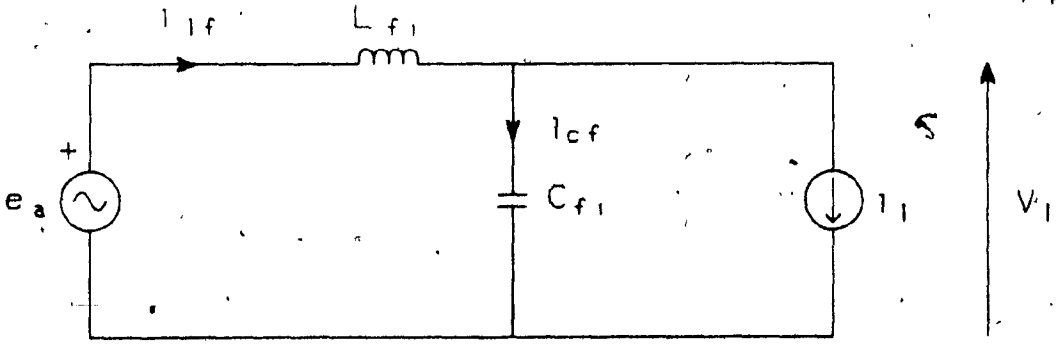


Fig.(2.11): CR input equivalent circuit

and the output equivalent circuit of a CR is shown in Fig.(2.12),

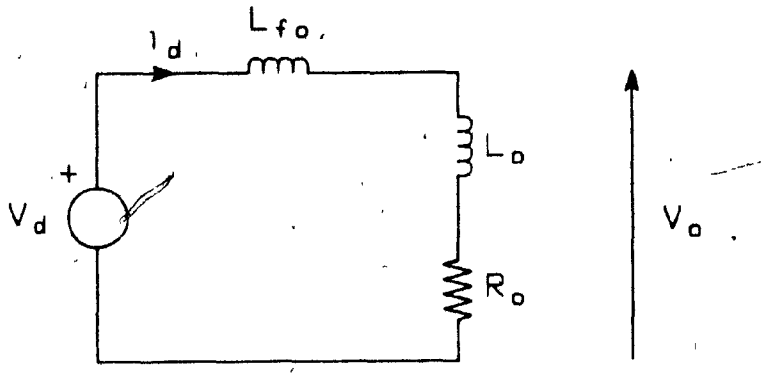


Fig.(2.12): CR output equivalent circuit

2.7 Power Converter Analysis and Design

The functional model of Table (2.4) together with the equivalent circuits can be used to perform the transient and steady state analysis and design of respective converters. The first step is to formulate the circuit dynamic equations using state space analysis and then solve the system of differential equations. Table(2.7) presents the state space formulation of the equivalent circuits obtained with the model (Table(2.4)) for VSI, CSI, and CR. This formulation is particularly important to study transient phenomena interaction between input and output networks. It can be seen in Table(2.7) that the output dynamic equations depend on input state space variables and vice versa. In the state space converter system model of Table(2.6) X_i are converter output space state variables and U_i are converter input space state variables.

2.7.1 Transient Converter Analysis.

Transient analysis in power converters is a subject of growing interest. Converter behaviour during turn on, switch stresses due to load transients, output distortion during modulation changes, etc., can be contemplated in the performance evaluation of a power supply or even included as complementary design information.

This thesis does not include transient analysis as a source of design data nor as a complementary source of information in the evaluation of power supplies performance. The subject topic is

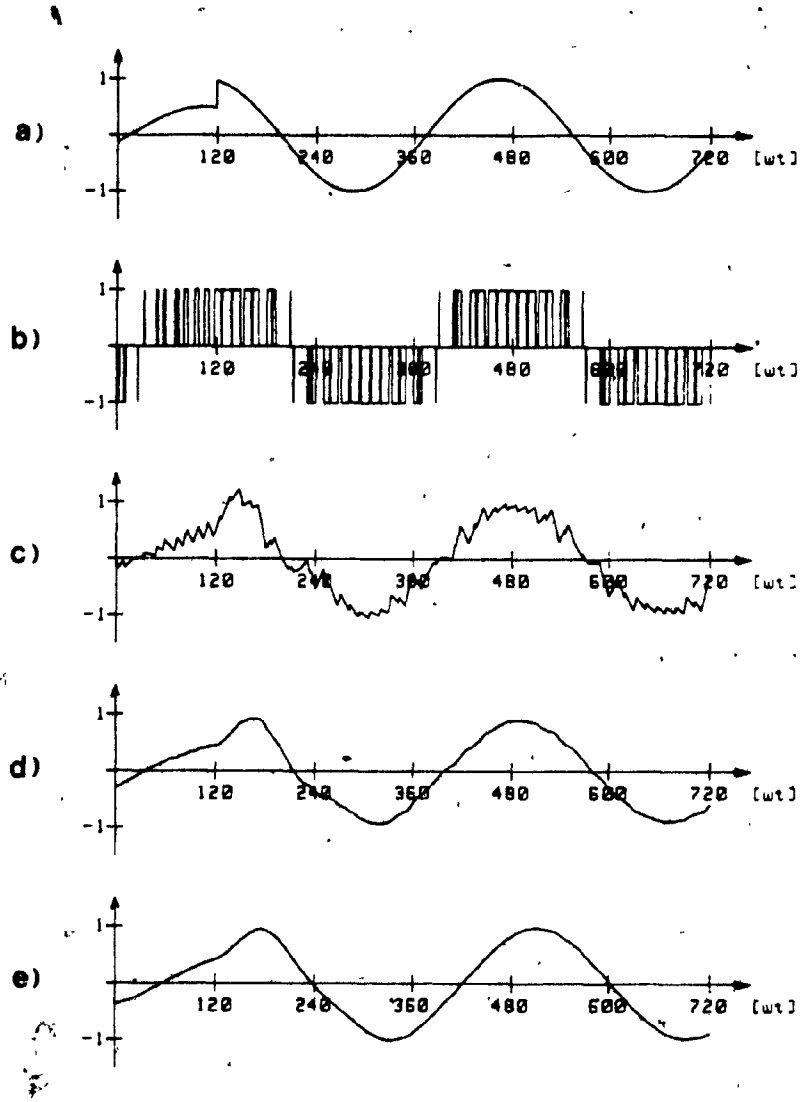


Fig.(2.13): VSI transient response. SPWM control technique. Filter impedances values with reference to Fig.(2.7), XLfo=.2 pu, XCfo=2 pu. Load=1 pu (power factor=.3 inductive).
a) Reference signal with a .5 step in the modulation factor.
b) Inverter output line voltage.
c) Inverter output line current.
d) Load voltage.
e) Load current.

recognized entirely as a field for future research. However, Table (2.7) provides some basic relations for transient analysis. The systems of differential equations (Table(2.7)) can be solved by numerical techniques such as Runge-Kutta [49] normally available in computer center libraries.

As an example of transient analysis consider a step change in the modulation factor of a SPWM-VSI (for a modulation factor definition refer to Fig.(2.16)). The resultant dynamic phenomena in the VSI system state space variables is shown in Fig.(2.13). Appendix 2 contents the computer program (based on Table (2.7) and the VSI equivalent circuit) for this transient study.

2.7.2 Steady State Analysis

The study of steady state input waveforms and particularly their spectra is a must in power converter analysis and design. Indeed, today's standard specifications in power converters include input output maximum distortion levels (THD 5% (2.5)) and maximum harmonic magnitude (usually smaller than 3%). These specifications are so relevant that PWM techniques and filter design are intented precisely to satisfy them. Both, PWM techniques and filter design can be conveniently studied under steady state conditions. Moreover, converter switch ratings such as average current, rms current, peak current and peak voltage are also determined under steady state conditions. It is true that step changes in load or in converter control variables can create transients that will not be covered by a

	VSI	CSI	CR
ac side	$\dot{x}_1 = \frac{1}{L_{FO}} (-x_2+f(u_1))$ $\dot{x}_2 = \frac{1}{C_{FO}} (x_1-x_3)$ $\dot{x}_3 = \frac{1}{L_o} (x_2 - R_o x_3)$	$\dot{x}_1 = \frac{1}{C_{FO}} (-x_2+f(u_1))$ $\dot{x}_2 = \frac{1}{L_o} (x_1-R_o x_2)$	$\dot{x}_1 = \frac{1}{C_{Fi}} (x_2-f(u_1))$ $\dot{x}_2 = \frac{1}{L_{Fi}} (e_a - x_1)$
	where: $x_1 = i_p$, $x_2 = v_c$ $x_3 = i_o$, $f(u_1)=H_a \circ u_1$	where: $x_1 = v_c$, $x_2 = i_o$ $f(u_1)=H_a \circ v_1$	where: $x_1 = v_o$, $x_2 = i_{LF}$ $f(u_1)=H_a \circ u_1$
dc side	$\dot{u}_1 = \frac{1}{C_{Fi}} (u_2-g(x_1))$ $\dot{u}_2 = \frac{1}{L_{Fi}} (-u_1+E)$	$\dot{u}_1 = \frac{1}{L_{Fi}} (v_i-g(x_1))$	$\dot{u}_1 = \frac{1}{(L_{FO}+L_2)} (-u_1 R_o+g_i x_1))$
	where: $u_1=v_d$, $u_2=i_i$ $g(x_1)=\bar{H}^T \cdot \bar{X}_1$	where: $u_1=i_d$ $g(x_1)=\bar{H}^T \cdot \bar{X}_1$	where: $u_1=i_d$ $g(x_1)=\bar{H}^T \cdot \bar{X}_1$

Table (2.7): State space formulation of converter equivalent circuits

steady state analysis. However, such transient are normally absorbed by specialized devices (transient supressors, snubbers, filters) or converter control techniques (current limit controllers), and therefore do not influence the steady state switch ratings significantly.

The steady state analysis can be performed directly in the time domain or using complex variables in the frequency domain. The contemporary approach to converter analysis is based on frequency domain expressions [15] [16] [18] [20].

2.7.2.1 Steady State Converter Analysis in the Frequency Domain.

With this approach, waveforms and transfer functions are mathematically defined by their Fourier series expansions such as (2.2). The model of Table (2.3) and the equivalent circuits for VSI, CSI and CR can be utilized. This analysis approach is popular because of the simplicity offered by complex variables. Indeed, all dynamic components are treated as impedances and the solution for every harmonic component can be obtained algebraically. This approach leads to precise computation of converter input output spectral content required for filter design and PWM technique optimization. However, this analysis approach has the following limitations:

i) leads to double summation infinite trigonometric series multiplications [15] [20 [30],

ii) requires frequency to time domain transformations which are intrinsically time consuming and inaccurate (series truncation error involved),

iii) cannot handle nonlinear loads, and finally

iv) frequency domain based signals do not provide good user-computer interaction, particularly in power converter simulation programs.

2.7.2.2. Steady State Converter Analysis in the Time Domain.

The model presented in Table (2.3) and the equivalent circuits for VSI, CSI and CR can be directly used in time domain analysis. Since precise power converter analysis is normally performed with the aid of digital computers, time domain variables and the availability of computer graphics capabilities should be considered essential for a good user-computer interaction (either in computer terminals or in PC systems).

To facilitate both, the analysis and the graphical output, waveforms can be stored in memory as numerical arrays. Experience in converter simulation and respective contrast with experimental results, [19] [21] [22] [24], indicates that waveforms with more than 1,000 points per period (typically 360·4=1440) provide accurate results (for converter chopping frequencies up to 3 KHz or 50 chops per period at 60 Hz).

To illustrate the simplicity of time domain computer based mathematical operations, consider the following operation normally required in the functional converter model of Table(2.3),

$$x_d(t) = \bar{H}(t) \cdot \bar{H}_1^T(t-\tau) \qquad (2.32a)$$

or by components,

$$x_d(t)=H_a(t)\cdot H_{a,1}(t-\tau)+H_b(t)\cdot H_{b,1}(t-\tau)+H_c(t)\cdot H_{c,1}(t-\tau) \qquad (2.32b)$$

Every addend of (2.32b) is the product of a sine waveform ($H_{i,1}(t-\tau)$) with a three level digital waveform that represents the transfer function. Fig.(2.14) displays such operands for the six-step converter control technique. Since $H_a(t)$ and $H_{a,1}(t-\tau)$ are assumed to be stored in k-dimensional arrays (computer memory), namely, Ha(k) and Hla(k) the multiplication can be performed as follows (in Hewlett-Packard Basic 3.0):

```
FOR N=1 TO k
   IF Ha(N) =1   THEN  Xd1(N)= Hla(N)
   IF Ha(N) =0   THEN  Xd1(N)= 0
   IF Ha(N) =-1  THEN  Xd1(N)= -Hla(N)
NEXT N
```

The Xd1(k) resultant waveform is shown in Fig.(2.14).

Moreover, if balanced conditions are assumed, phases b and c are identical to phase a shifted by 120° and 240° degrees respectively. Therefore, the total expression (2.32b) can be computed with the next following program lines (in Hewlett-Packard Basic 3.0),

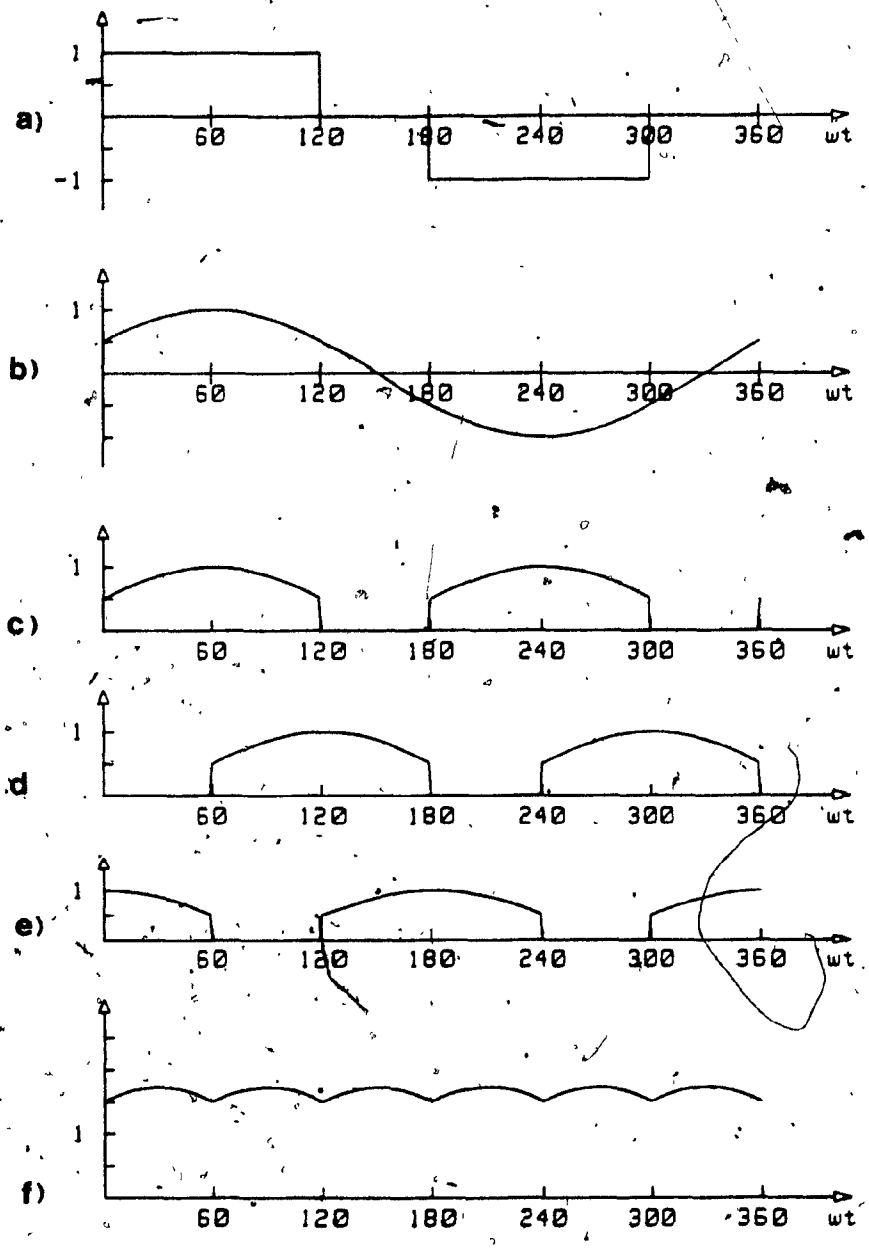


Fig.(2.14): Waveform-processing for six-step PWM (see expr. (2.32b)):
a) Ha(t) phase "a" component of transfer function H(t).
b) Ha (t-τ) phase "a" independent variable (fundamental component of Ha(t) shifted by τ sec).
c) first addend of (2.32b),
d) second addend of (2.32b),
e) third addend of (2.32b),
f) dc dependent variable (sum of (2.32b).

```
FOR N=1 TO k
   Xdb(N) = Xda((N+2*k/3) MOD k)
   Xdc(N) = Xda((N+k/3) MOD k)
    Xd(N) = Xda(N)+Xdb(N)+Xdc(N)
NEXT N
```

The resultant Xd(k) waveform is shown in Fig.(2.14).

Once the equivalent independant electrical sources required in the model of Table(2.4) (H(t) and H(t) H(t-τ)) are computed, the rest of the analysis is performed as described in section (2.71) with the aid of the converter input output equivalent circuits.

Discussion:

The current analysis approach used to obtain Xd(t) has been to express the operands of the required operations in Fourier series components [18] [20] [30], perform their multiplication (trigonometric series multiplication) and then reconstruct the time domain waveform from the resultant trigonometric series or spectrum. This method does not produce accurate results when computing generated time domain waveforms such as the one depicted in Fig.(2.14d). Furthermore, it is more complex and requires considerably more computer time (specially when performing frequency to time domain transformations).

To conclude, the analysis approach based on the time domain model

presented in this thesis has the following advantages when compared to the Fourier series based type of analysis:

i) it requires extremely simple mathematical operations, it is easier to program, and the computer processing time is several times smaller,

ii) it is by large more accurate particularly in the description of PWM time domain generated waveforms,

iii) it can be directly used to study nonlinear loads (such as another power converter), and it

iv) can be used for transient analysis.

2.7.3 Converter Switch Ratings.

The functional model Table (2.4) provides the input-output converter waveforms (Fig's.(2.5) and (2.6)). These waveforms, the nature of the converter (current or voltage), and the converter switch configuration are required to compute the steady state switch ratings. In particular, for three phase applications, the bridge arrangement of power semiconductors possesses a number of advantages over all alternative possibilities and has become a standard 3Ø configuration for rectifiers and inverters [10] [11] [14]. A bridge structure will be employed throughout this thesis for the synthesis of the improved proposed power supply topologies. Fig.(2.15) shows a generalized bridge configuration utilizing ideal switches instead of power semiconductors. The bridge switch ratings (for VSI, CSI, and CR) computed next in subsections (2.7.3.1) and (2.7.3.2) are summarized in

Table(2.8).

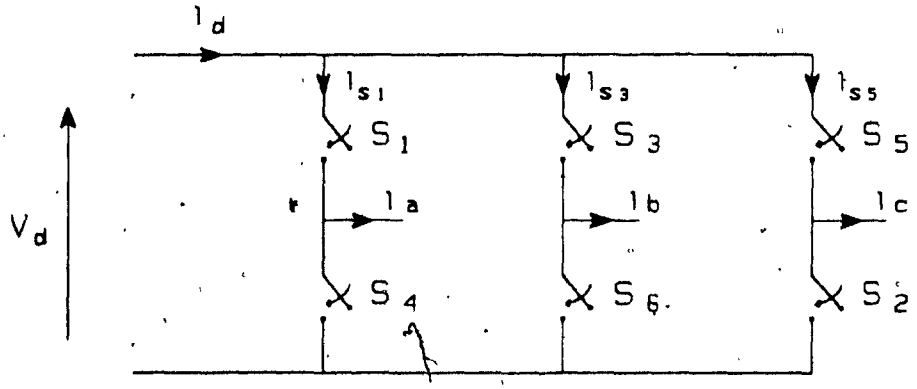


Fig.(2.15): Generalized bridge configuration.

To compare the switch ratings subsequently obtained for VSI, CSI and CR, the switch utilization factor can be defined as,

$$S_{uf} = \frac{P_{or}}{N_s\left(v_{s\ peak} \cdot i_{s\ avg}\right)} \qquad (2.33)$$

The Suf figures for the bridge structure Fig.(2.15), operating with SPWM and modified SPWM, are also summarized in Table(2.8).

2.7.3.1 VSI Switch Ratings.

To compute the current ratings of a VSI bridge converter consider the circuit of Fig.(2.2), Table(2.4) and the bridge structure Fig.(2.15). Moreover, the VSI output line currents are assumed sinusoidal under steady state, therefore,

$$\left|i_{a,1}\right| = \sqrt{3} \cdot \left|i_{p,1}\right| = \sqrt{3} \left|\frac{V_{\ell,1}}{Z}\right| = \sqrt{3}\, H_1 = \sqrt{3}\, a_1 \qquad (2.34)$$

In a VSI, switches conduct the sinusoidal output line currents with a 50% duty cycle. Therefore,

$$I_{s\ avg} = \frac{i_{al}}{\pi} = \frac{\sqrt{3}}{\pi} a_1$$

$$I_{s\ rms} = \frac{i_{al}}{2} = \frac{\sqrt{3}}{2} a_1 \qquad (2.35)$$

$$I_{s\ peak} = i_{al} = \sqrt{3}\, a_1$$

The a_1 values for SPWM and modified SPWM are computed in Appendix 1 (a_1(SPWM,M=1) = $\sqrt{3}/2$; a_1(MSPWM,M=1) = 1). Furthermore, the switch peak voltage of the VSI bridge of Fig.(2.15) can be determine by

inspection, and is equal to the input voltage (E=1pu).

2.7.3.2 CSI and CR Switch Ratings

Both, CSI and CR are current type of converters and have identical switch ratings whenever sharing the same circuit configuration. For the bridge of Fig.(2.15), and using Table(2.4), and Fig's.(2.3) and (2.4) the steady state line currents are:

$$\bar{i}_{\ell}(t) = \bar{H}(t) \tag{2.36}$$

These line currents are of the type shown in Fig.(2.1). The duty cycle of a line PWM waveform is 2/3. Therefore, a switch of a CSI or CR will have a duty cycle of 1/3 (note that two switches are connected per line). Consequently, the current ratings for a switch with a PWM waveform of amplitude I= 1pu and duty cycle of 1/3 are,

$$I_{s\ avg} = \frac{1}{3}\ pu$$

$$I_{s\ rms} = \frac{1}{\sqrt{3}}\ pu \tag{2.37}$$

$$I_{s\ peak} = 1\ pu$$

The voltage rating for these converters (peak voltage) is

identical to the peak current rating for a VSI. To probe this statement consider the CSI or CR peak line voltage (which is also the switch peak voltage) in Fig.(2.3),

$$v_{s\ peak} = \sqrt{3} \cdot |v_{p,1}| = \sqrt{3} \cdot (|i_{\ell,1}| \cdot |Z|) = \sqrt{3}\, H_1 = \sqrt{3}\, a_1 \ pu \qquad (2.38)$$

A comparison between (2.34) and (2.38) shows the ratings reciprocity between these dual converters. Again, replacing the a_1 values for SPWM and MSPWM into (2.38) the CSI-CR voltage ratings becomes defined.

A summary of the generalized per-unit ratings of the bridge ac/dc converter is presented in Table(2.8). The ratings are computed with reference to the per-unit system defined in section (2.6.2) and are valid for VSI, CSI and CR converters. Specifically, (2.34),(2.38) define the voltage ratings and (2.35),(2.37) the current ratings.

Discussion:

Inspecting Table(2.8) will lead to the conclusion that the modified SPWM offers a significantly better switch utilization Suf for current and voltage ac/dc converters than the SPWM. Furthermore, current and voltage ratings can also be used to compare current and voltage types of converters. Comparing the Suf of VSI with respective Suf of CSI and CR, the VSI has a better switch utilization. However, a switch in a VSI is implemented with a controlled semiconductor and an antiparallel diode (two semiconductors) while CR and CSI do not

	PEAK VOLTAGE		PEAK CURRENT		AVERAGE CURRENT		RMS CURRENT		P_{or} POWER		S_{uf} SWITCH	
	SPWM	MSPWM	SPWM	MSPWM	SPWM	MSPWM	SPWM	MSPWM	SPWM	MSPWM	SPWM	MSPWM
VSI	1	1	1.5	1.73	.48	.55	.75	.87	1.25	1.50	.43	.455
CSI CR	1.5	1.73	1	1	.33	.33	.58	.58	1.25	1.50	.42	.438

Table (2.8): Generalized converter switch ratings and switch utilization factors.

require the diode. This situation and its effect on component utilization will be studied in detail in Chapter 3.

2.7.4 Converter Switching Frequencies.

The converter switching frequency is directly related to the implementation of a particular modulation technique. Therefore, for the completeness of the bridge switch ratings (Table(2.10)), the switching frequencies required to implement SPWM, and the MSPWM are considered next. In general, variable modulation techniques utilize a "reference" and a "carrier signal". Fig.(2.16) shows the reference and carrier signals for SPWM. Moreover, Fig.(2.16) defines the modulation factor and the normalized carrier frequency fcn.

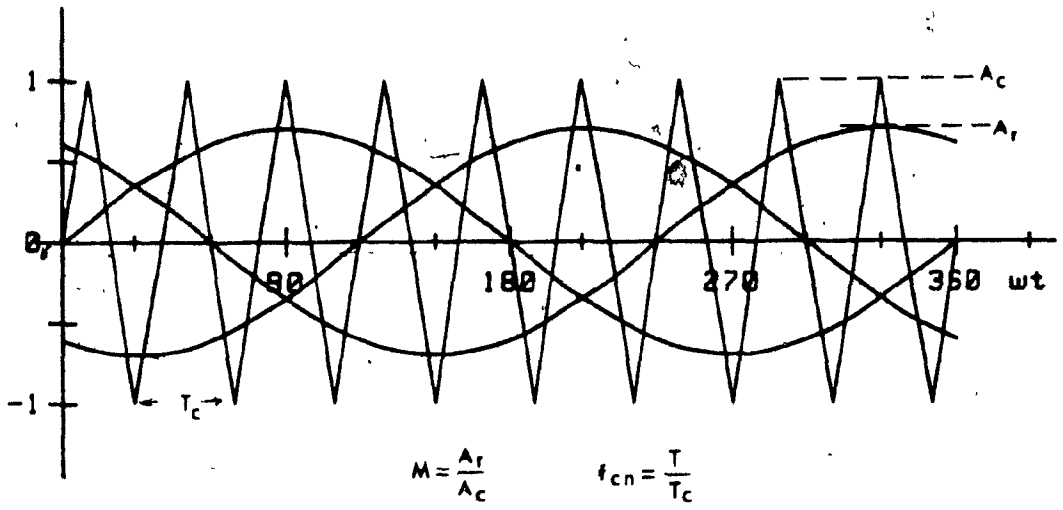


Fig.(2.16): Carrier, Reference, Modulation and fcn in PWM.

The normalized carrier frequency is important because dominant harmonic frequencies are usually specified in terms of such frequency. A dominant harmonic is defined in the context of this thesis as the "hardest" harmonic to be filtered (also see section(2.7.5)). Switching frequencies for the implementation of these techniques are given in [23] [24] [21] [46] and are summarized in Table(2.9) in terms of the fcn.

	SPWM	MSPWM
VSI	fcn	fcn
CSI-CR	fcn+2	(2/3)fcn

Table(2.9): Normalized switching frequencies.

2.7.5 Converter Filter Design Considerations.

The generalized steady state waveforms (Fig's(2.5) and (2.6)) of the ac/dc PWM converter have to be filtered to meet standard THD(2.6) specifications (usually 5%). Another usual specification, generally more restrictive, is to limit the size of the dominant harmonic to 3% of the wanted component (rated value). The method proposed in this thesis is to limit the size of the dominant harmonic (3%) and then verify if the resultant spectrum has a THD smaller than 5%.

The first step in power converter filter design is to find the

required filter break frequency which ensures that the dominant harmonic amplitude (after filtering) is bounded to 3%. Using Bode diagrams [50] it can be concluded that the filter break frequency is given by:

$$\omega_b = \omega_d \left(\frac{0.03}{a_d}\right)^{1/\alpha} \qquad (2.39)$$

The next step is to consider specific PWM techniques and related input output spectra. Using the subprograms of Appendix 1 (see also Fig's(2.5) and (2.6)) the input output dominant harmonics (frequencies and magnitude) of SPWM and MSPWM are summarized in Table(2.10) in terms of the normalized carrier frequency fcn Fig.(2.16). It is worth while to recall that converter switching frequencies are related to the fcn (Table(2.9)).

Table(2.10) and expression (2.39) enables a more precise dominant harmonic definition as follows: " the dominant harmonic, for a filter of order a is the one that requires the lowest break frequency to become smaller than 3% of the fundamental".

For example, consider the dc spectrum of MSPWM (Table(2.10)). The dominant harmonics are:

fcn-4 with first order filter

fcn-2 with second order filter

Using Table(2.10) and the specific filter required (typical converter filter configurations are given in Fig's(2.7) to (2.12)), the break frequency can be approximated with (2.39). Finally, the filter

components are chosen to produce the required wb while optimizing weight, cost, and system reliability [28].

PER UNIT FREQUENCY	SPECTRUM VALID FOR: – CR INPUT CURRENTS – CSI OUTPUT CURRENTS – VSI OUTPUT VOLTAGES	
	SPWM [%]	MSPWM [%]
1	100.0	100.0
$f_{cn} - 4$	0.0	11.4
$f_{cn} - 2$	32.2	25.6
$f_{cn} + 2$	32.2	25.6
$f_{cn} + 4$	0.0	11.4

SPECTRUM VALID FOR: – CR OUTPUT VOLTAGE – CSI INPUT VOLTAGE – VSI INPUT CURRENT		PER UNIT FREQUENCY
SPWM [%]	MSPWM [%]	
100.0	100.0	0
0.0	0.9	$f_{cn} - 9$
30.0	14.1	$f_{cn} - 3$
30.0	14.1	$f_{cn} + 3$
0.0	0.9	$f_{cn} + 9$

Table (2.10): Input-Output generalized Spectra for VSI, CSI and CR. SPWM and MSPWM control techniques (M=1, Ø=0).

2.8 Conclusions

A novel analysis approach for switch mode converters has been proposed in this chapter. The subject analysis approach is based on the definition of a transfer function for switch mode converters. With the use of this transfer function, converters can be modelled by black boxes that perform specific conversion functions (e.g. ac/dc conversion or rectification) using specific PWM techniques (e.g. sine PWM).

This treatment makes possible the simultaneous analysis of groups of converters that share conversion functions (e.g. VSI, CSI, and CR perform the same ac/dc or dc/ac conversion function). Furthermore, with this approach the analysis of systems with multiple power conversion stages becomes modular and simpler (with each module represented by its transfer function). Moreover, the approach is consistent with the technological trend towards integrated systems where the actual internal structure of the module (i.e. converter) is irrelevant to the study of the power conversion system.

The transfer function concept allows for a more systematic synthesis by allowing the decomposition of the design of power converters into three major design steps:

i) the derivation of the converter transfer function from the conversion task to be performed and available PWM techniques,

ii) the synthesis of topologies to perform the required conversion, and

iii) the determination of the gating strategy required to produce transfer function i) with the topology derived in ii).

Specifically, this chapter identifies a common bilateral transfer function for the ac/dc group of converters (VSI,CSI, and CR) merging their traditionally disjointed analysis into one. Moreover, this transfer function has been used to produce normalized steady state waveforms for VSI,CSI and CR converters. In particular, waveforms which simultaneously represent the output line voltages of a VSI, the output line currents of a CSI, and the input line currents of a CR have been established. Further, waveforms which simultaneously represent the input current of a VSI, the input voltage of a CSI, and the output voltage of a CR have also been established.

To process the proposed transfer function relationships this chapter has introduced a time domain based approach. This approach, when compared with the traditional Fourier series based approach, has the following advantages:

i) it requires extremely simple mathematical operations, it is easy to program, and the computer processing time is many times smaller,

ii) it is by large more accurate, particularly in describing PWM time domain generated waveforms, and

iii) it can be directly used for transient analysis.

Finally, generalized design data is provided for VSI, CSI, and CR 3Ø-bridge converters. The data include normalized switch ratings, semiconductor switchings frequencies, and normalized input/output frequency spectra for the sine PWM and modified sine PWM techniques.

CHAPTER 3

COMPUTER AIDED DESIGN FOR SWITCH MODE CONVERTERS

3.1 Introduction

According to the primary objective of this thesis, which is the performance improvement of static power supplies, this chapter proposes a VSI design approach that significantly improves the VSI component utilization. This topic is relevant because VSI based systems account for most of today's inverter power conversion systems. In particular, ac drives and UPS systems are two major families of applications for VSI's.

Specifically, this chapter identifies an important source of VSI component under-utilization introduced by the contemporary VSI design approach [11] [14]. The proposed design method is based on the utilization of generalized per-unit rating curves. The application of the subject method completely removes the under-utilization introduced by the contemporary approach, thereby, resulting in an improved PWM-VSI design [22].

The contemporary approach assumes that the switch component ratings Fig.(3.1b) are identical to the switch ratings Table (2.5). This design assumption is inaccurate and the resultant ratings exceed the real requirements. Although resulting component utilization is low, the assumption has been used extensively and the task of optimizing a design has been more an art than a science. However, by computing the

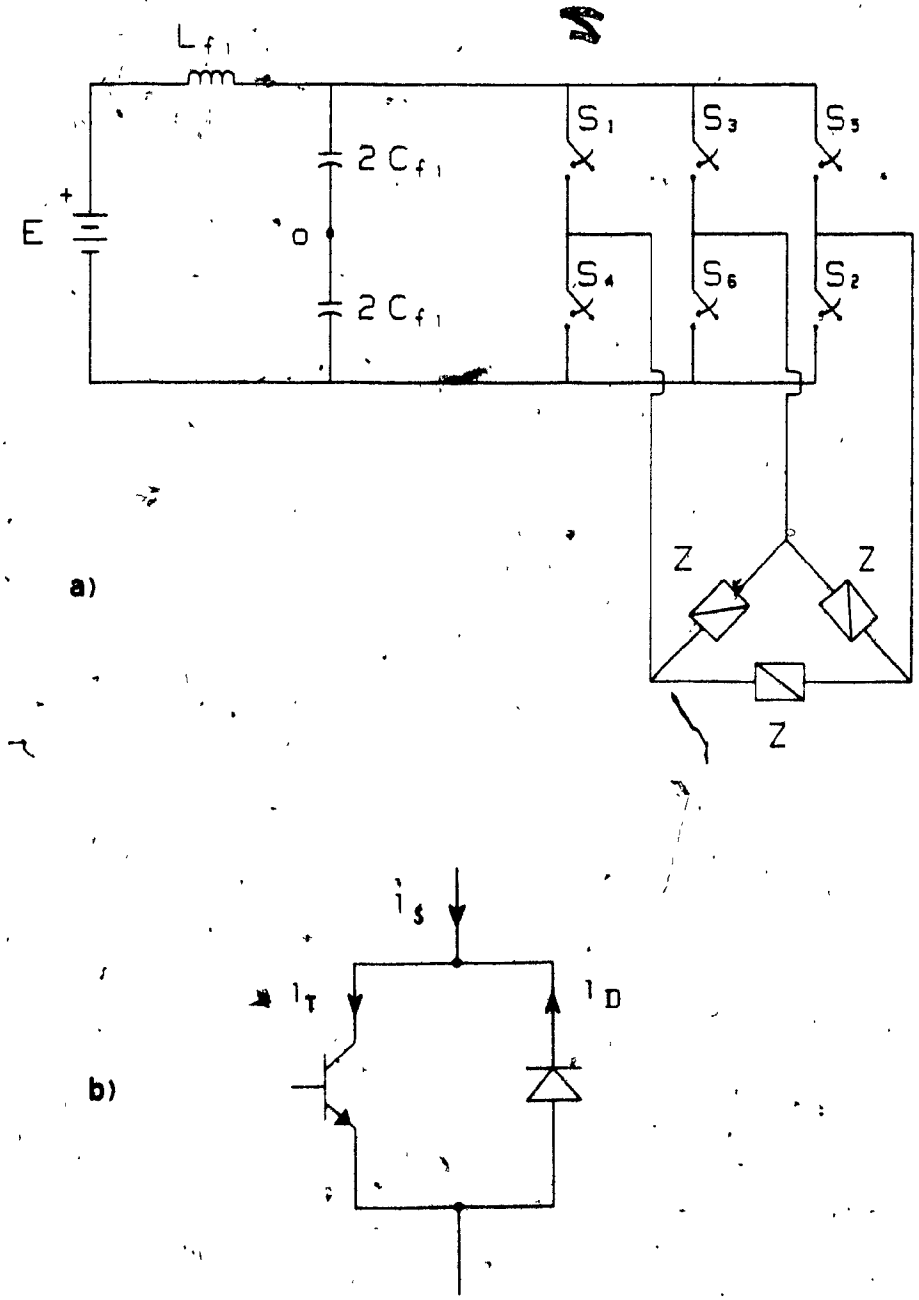


Fig.(3.1): a) simplified voltage source inverter circuit diagram.
b) actual configuration of S1,S2,..S6 switches.

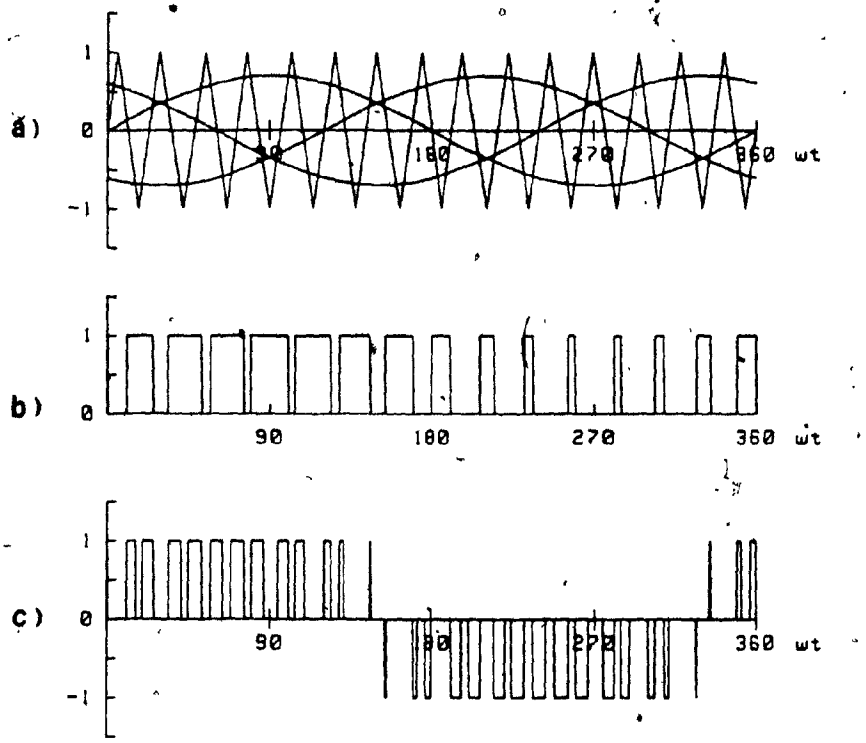


Fig.(3.2): The sinusoidal PWM control scheme.

a) method of obtaining inverter switching points.
b) Switching function of phase a.
c) Transfer function (phase a component, Ha(t)).

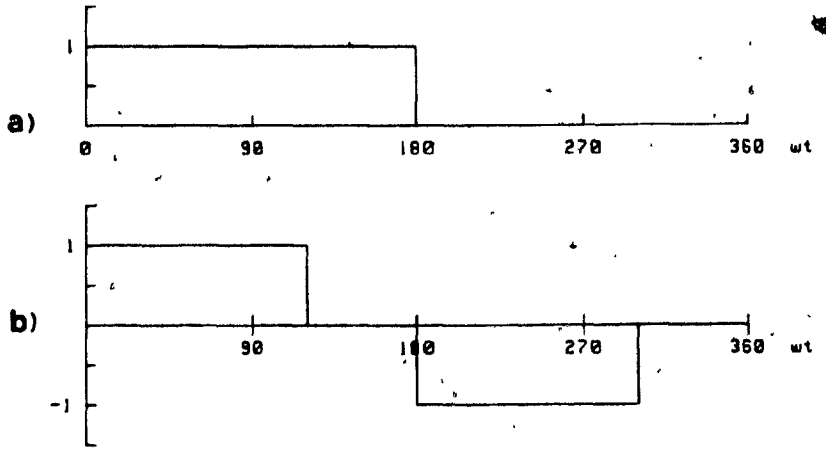


Fig.(3.3): The six-step PWM scheme.

a) Switching function of phase a.
b) Transfer function (phase a component, Ha(t)).

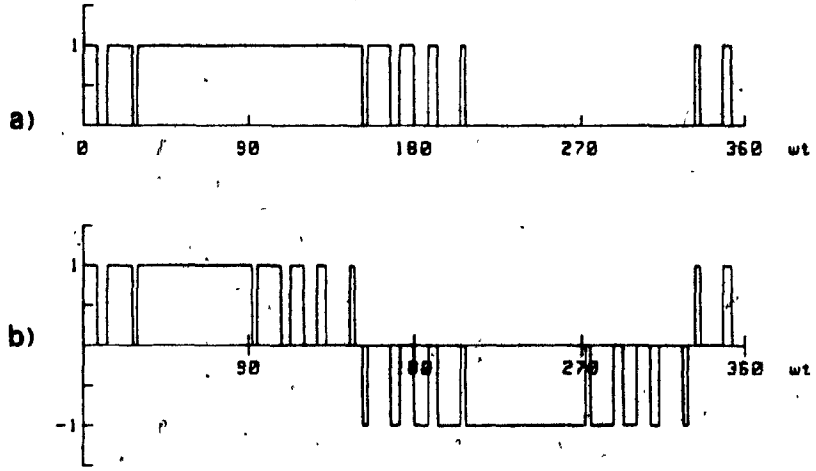


Fig.(3.4): A fixed PWM pattern control scheme (Fig.(4.7)).

a) Switching function of Swl (Fig.(3.1a)).
b) Transfer function (phase a component, Ha(t)).

exact semiconductor ratings the utilization of VSI components can be heavily improved. Thus, not only the required semiconductors will be smaller (for a particular power level) but also auxiliary components, such as semiconductor heatsinks, will be directly influenced. Therefore, the density of power processed by a power supply unit can be boosted without compromising the system complexity or cost.

The exact computation of the VSI semiconductor currents requires the exact prediction of semiconductor current waveforms. Fig.(3.1a) shows a generalized bridge converter usually chosen to perform the ac/dc conversion function [10] [22]. This converter configuration and the VSI steady state output currents computed as indicated in chapter 2 can be used to compute the current waveforms flowing through the bridge switches. Furthermore, Fig.(3.1b) shows a typical VSI switch configuration which consists of a unidirectional switch (controlled semiconductor) and an antiparallel "flywheel diode". Therefore, considering Fig.(3.1b),

$$i_s = i_T - i_D \tag{3.1}$$

This relation shows that the current flowing through the switch is not identical to current i_T or current i_D (with the exception of trivial cases). Therefore, semiconductor ratings are not identical to switch ratings.

To estimate the severity of the under-utilization introduced by the contemporary approach consider the VSI switch utilization factor (2.33) re-defined (i.e. considering the two switch components) as,

$$S_{VUF} = \frac{P_{or}}{N_S(v_{T\ peak} \cdot i_{T\ avg} + v_{D\ peak} \cdot i_{D\ avg})} \qquad (3.2)$$

And replacing the semiconductor ratings by switch ratings (as done by the contemporary VSI design method) [11] [14] results in:

$$S_{VUF} = \frac{P_{or}}{2N_s(v_{s\ peak} \cdot i_{s\ avg})} \qquad (3.3)$$

A comparison between S_{UF} (2.33) and the resultant S_{VUF} (3.3) shows that the semiconductor ratings of a VSI could have been derated up to a 100% by adopting the assumption of the contemporary approach. The severity of this figure shows the necessity for a more precise VSI design method. A precise design approach is required to determine how the switch current is distributed among the switch components. Both, the modulation factor (for a specific PWM, Fig.(2.16)) and the load power factor have influence over how the current is distributed among the switch semiconductors. Therefore, the improvement to be accomplished depends on the VSI required ranges of operation (modulation and power factor ranges). Naturally, wider ranges of operation (modulation and power factor) require higher VSI current semiconductor ratings.

To facilitate the design task, for specific ranges of operation in a particular application, generalized per-unit ratings data curves for the VSI semiconductors have been developed. The subject curves

define the subject ratings as a function of modulation and power factors. Design data has been obtained for three PWM control schemes, namely, the sinusoidal PWM Fig.(3.2), the six step Fig.(3.3), and a fixed PWM pattern Fig.(3.4) as proposed and utilized in Chapter 4 of this thesis [24].

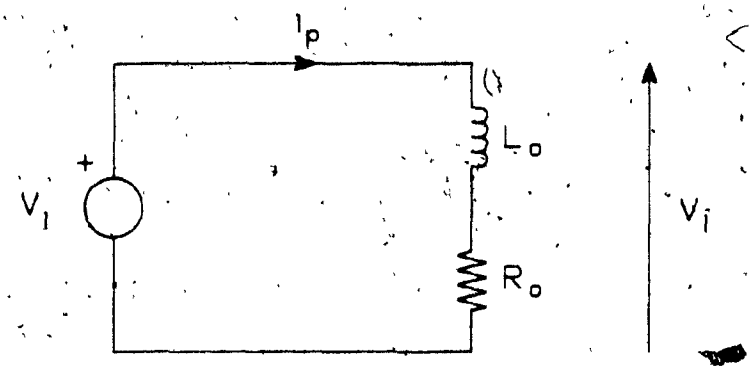
3.2 Voltage Source Inverter Load Considerations

To ensure a wide coverage, the design data have been obtained while considering the load characteristics of two important families of applications; namely, ac drives and UPS systems. In ac drive applications (speed control) the VSI normally requires a full range of modulation factors. Indeed, the output voltage (thereby the modulation) is varied proportionally to the output frequency (machine speed) to maintain a constant magnetic flux in the machine [11] [31]. Furthermore, the VSI load power factor depends on the actual mechanical load of the machine [31] [45]. The inductive power factor range considered in this chapter ($.2 < \cos(\phi) < 1$) satisfies expected ac induction machine drive requirements. Also, as required in drive applications, the data is obtained under rated output current conditions.

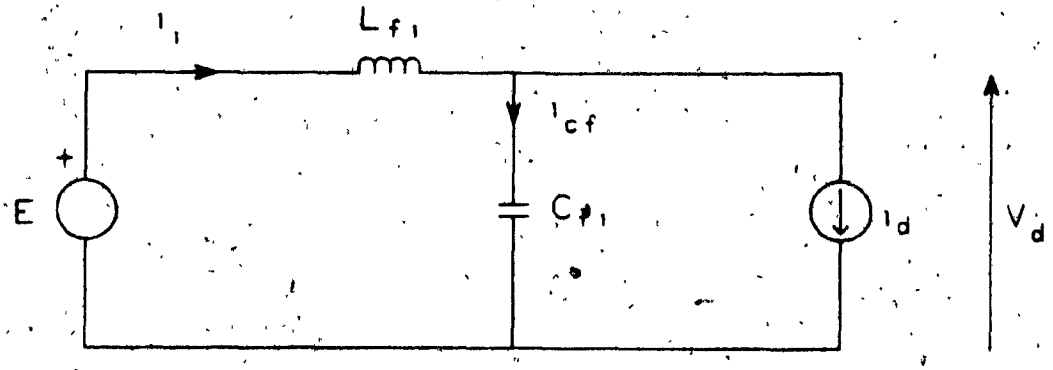
In UPS systems, the required range in VSI modulation factor is smaller compared to the range required in ac drives. Pulse width modulation in UPS is used mainly for two reasons: for the reduction of input-output filters, and to regulate the output voltage. The usual

modulation range requirement in UPS systems is ($.723 < M < 1$, [24]). This operational range is already included in the wider range required for ac drive applications. Furthermore, although the inductive power factor chosen in this chapter could be restrictive in certain UPS applications, the method of obtaining the design data is valid for any modulation and/or power factors.

With the available load model the next step in obtaining the required component ratings is to consider an adequate converter model. The analysis method of Chapter 2 and Table (2.4) are used to compute the input-output steady-state waveforms required. Moreover, Fig.(3.5) shows the input-output equivalent circuits utilized in this chapter for the prediction of the input output converter currents. The basic analysis assumptions of this chapter are ideal components, perfectly balanced conditions, and steady state operation. These assumptions cannot be considered highly restrictive and, even for the exceptional cases where they are not applicable, the given design method constitutes a good first step iteration.



a)



b)

Fig.(3.5): Per phase VSI equivalent circuits.

a) Output or load circuit.
b) Input circuit.

3.3 Voltage Source Inverter Input-Output Current Analysis

The VSI steady state line output currents are computed by applying the line output VSI voltage to the load impedance (Fig.(3.5)). Specifically, the output line currents are given by:

$$\bar{i}_{\ell} = \frac{\bar{v}_{\ell}}{Z} \tag{3.4}$$

Typical line currents are shown in Fig's(3.6), (3.7) and (3.8) for the PWM schemes under analysis. Next, the switch currents are obtained from the time domain product of the line currents times respective switching functions (3.5) (Fig's.(3.2), (3.3) and (3.4)). In the context of this thesis a switching function (SF) is the normalized control signal applied to a controlled semiconductor [15] [16] [17]. Thereby, considering the effect of the flywheel diode in a VSI, a "one" in the switching function corresponds to an on state (closed VSI switch) and a "zero" in the switching function corresponds to an off state (open VSI switch).

$$i_{S1} = i_a \cdot SF \tag{3.5}$$

Once the VSI switch current waveforms Fig's.(3.6d), (3.7c), and (3.8c) have been obtained the switch component currents can be determined (3.1). We assume (as in chapter 2) that the analysis is carried out by a digital computer. Therefore, the numerical values of a switch current are assumed to be stored in a k-dimensional array

isl(k). Consequently, the switch current components (iT, iD) can be computed by subjecting each isl(k) array element to conditional statements,

```
FOR n=1 TO k
    IF isl(n)>0 THEN iT1(n)=isl(n)
    IF isl(n)<0 THEN iD1(n)=-isl(n)
NEXT n
```

Fig's.(3.6e,f), (3.7d,e), and (3.8d,e) show typical switch current component (iT1, iD1) waveforms. To complete the VSI current analysis, the input current id is computed considering Fig.(3.1a) as follows,

$$i_d = i_{S1} + i_{S3} + i_{S5} \tag{3.6}$$

Equation (3.6) can be compared to (2.32b), since both are used to compute the VSI converter input current. Furthermore, since in this chapter the exact line current waveforms are computed (therefore not perfectly sinusoidal) the input current computed with (3.5) will be slightly different to the one predicted by the functional model of Table (2.4) under steady state conditions. Fig's.(3.6g), (3.7f), and (3.8f) show VSI simulated input current waveforms for SPWM, six step and fixed PWM pattern respectively. Moreover, Fig's(3.6h), (3.7g), and (3.8g) show the input current spectrum obtained for the three control schemes under study.

Finally, the VSI semiconductor ratings are directly determined by applying the average, rms and peak value definitions to the respective

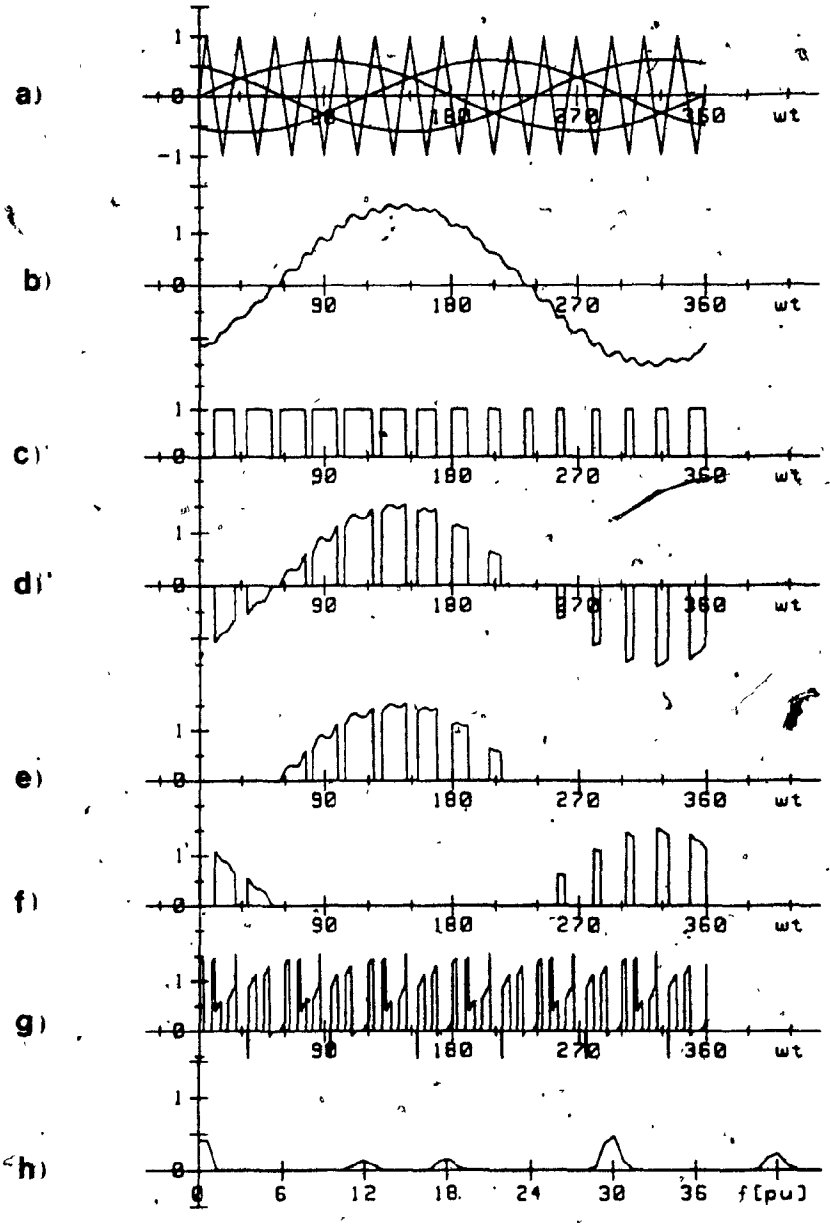


Fig.(3.6): Inverter generated current waveforms with the SPWM control scheme. (M=.6, pf=.6 inductive).

a) Method of obtaining switching points.
b) Line output current (ia(wt) waveform).
c) Switching function of switch Sw1 (Fig.(3.1a)).
d) Switch (S 1) current waveform (is1(wt)).
e) Controlled semiconductor current waveform (iT(wt)).
f) Diode current waveform (iD(wt)).
g) Inverter input current waveform (id(wt)).
h) Inverter input current spectrum.

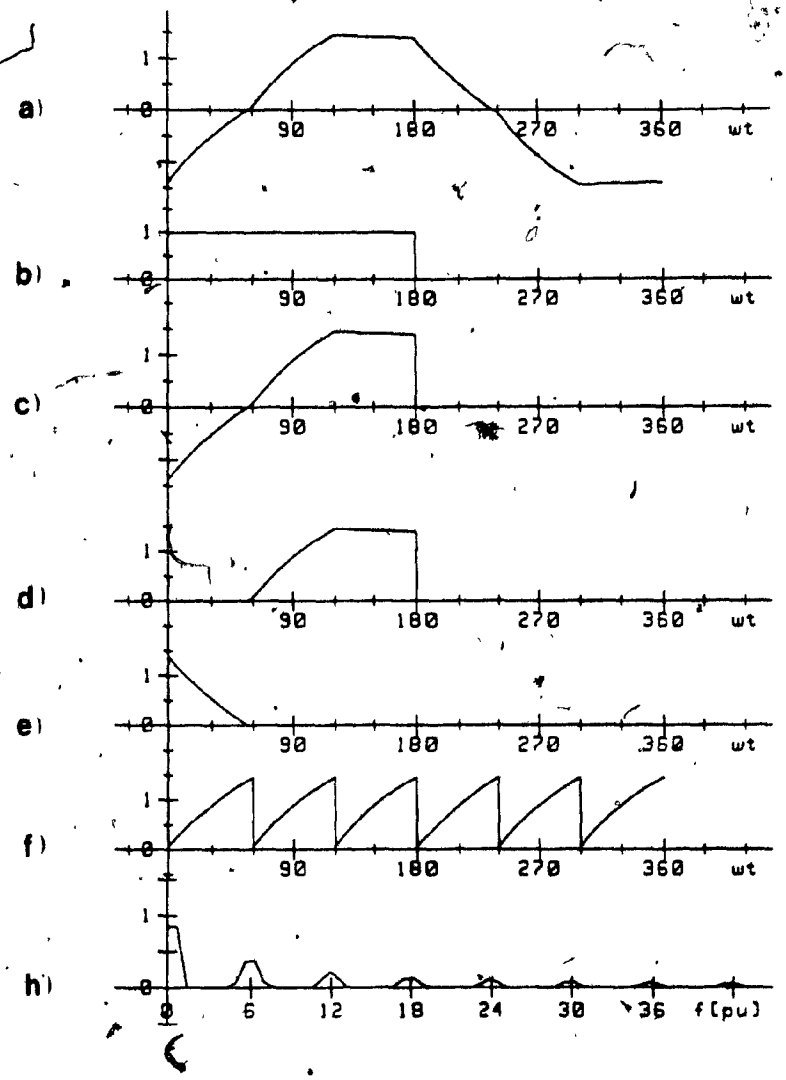


Fig.(3.7): Inverter generated waveforms with the six-step PWM scheme.

a) Line output current waveform (ia(wt)).
b) Switching function of switch Sw1 (Fig.(3.1a)).
c) Switch (S 1) current waveform (is1(wt)).
d) Controlled semiconductor current waveform (iT(wt)).
e) Diode current waveform (iD(wt)).
f) Inverter input current waveform (id(wt)).
g) Inverter input current spectrum.

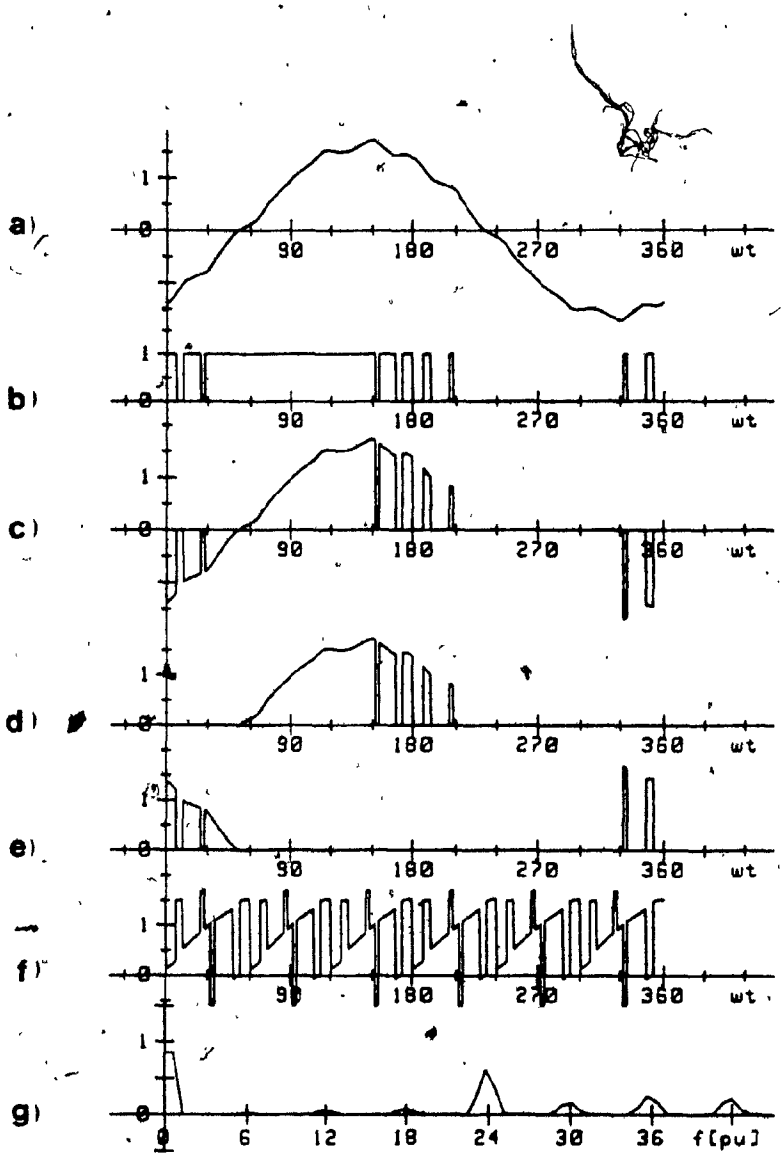


Fig.(3.8): Inverter generated waveforms with the fixed PWM pattern (Fig.(4.7)).

a) Line output current waveform (ia(wt)).
b) Switching function of switch Sw1 (Fig.(3.1a)).
c) Switch (S 1) current waveform (is1(wt)).
d) Controlled semiconductor current waveform (iT(wt)).
e) Diode current waveform (iD(wt)).
f) Inverter input current waveform (id(wt)).
g) Inverter input current spectrum.

VSI current waveforms. Specifically, for the controlled semiconductor,

$$i_{T\ avg} = \frac{1}{2k} \sum_{n=1}^{k} \left(i_T(n) + i_T(n-1)\right) \tag{3.7a}$$

$$i_{T\ rms} = \left(\frac{1}{2k} \sum_{n=1}^{k} \left(i_T^2(n)+i_T^2(n-1)\right)\right)^{1/2} \tag{3.7b}$$

$$i_{T\ peak} = \max\left(i_T(k)\right) \tag{3.7c}$$

and analog expressions for the diode.

3.4 Generalized Design Curves

Two factors influence the VSI current waveforms and thereby the component ratings computed with (3.7); namely, the modulation factor Fig.(2.16) and the load power factor. To consider both factors simultaneously a normalized per-unit family of curves has been computed in every case (average, rms, and peak). Fig's(3.9), (3.10), and (3.11) show these curves for the three PWM schemes under study.

The per-unit base has been chosen in such a way as to be consistent with the ratings of Table (2.8). Thereby, the dc input voltage for SPWM is 1 pu. However, to obtain the same per unit fundamental line currents (assuming a common load), the input voltages for the six step PWM and the fixed PWM have to be adjusted consistently. The input voltage for the six step is equal to .79 pu

and for the fixed PWM pattern, .845 pu [46].

Using (2.34) the fundamental rms value of the output line current is:

$$i_{a,1\ rms} = \frac{\sqrt{3}}{\sqrt{2}} a_1 = \frac{\sqrt{3}}{\sqrt{3}} \frac{\sqrt{2}}{2} = 1.061 \text{ pu} \qquad (3.8)$$

Discussion:

Fig's(3.9a) and (3.9b) show that the ratings of the controlled switches (average and rms) increase with a higher load power factor and/or a higher PWM modulation factor. The opposite is true with respective diode ratings Fig's(3.9d) and (3.9e). The explanation is that conduction intervals of unidirectional controlled switches decrease with M and power factors. On the other hand, reactive currents flowing through flywheel diodes increase whenever M or the power factor decreases.

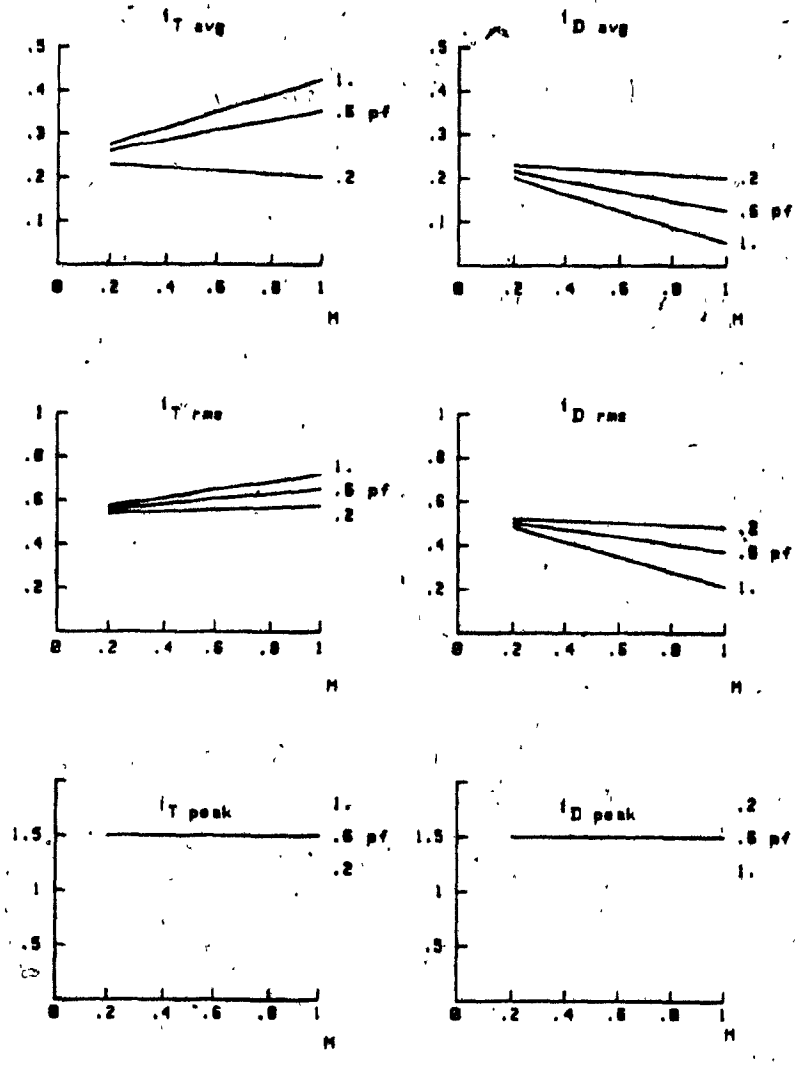


Fig.(3.9): Normalized component ratings with the SPWM control scheme.

a) Controlled switch average current ratings, iTavg.
b) Controlled switch rms current ratings, iTrms.
c) Controlled switch peak current ratings, iTpeak.
d) Diode average current ratings, iTavg.
e) Diode rms current ratings, iDrms.
f) Diode peak current ratings, iDpeak.

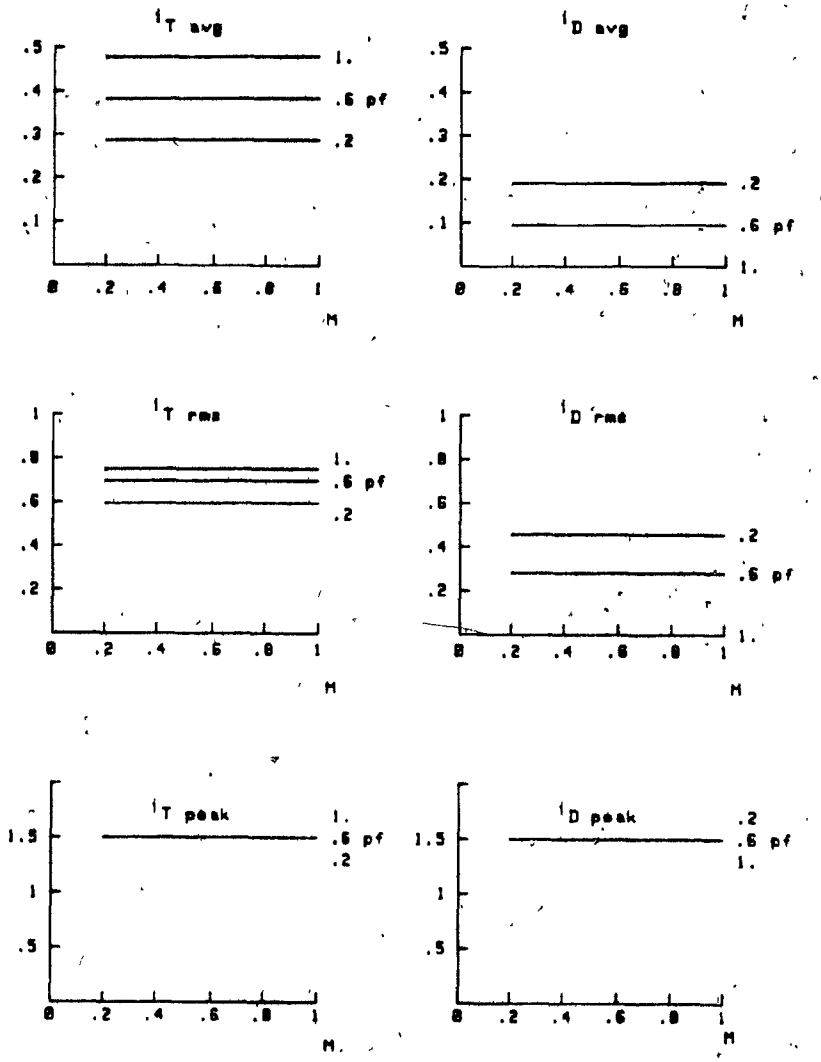


Fig.(3.10): Normalized component ratings with the six-step PWM scheme.

a) Controlled switch average current ratings, iTavg.
b) Controlled switch rms current ratings, iTrms.
c) Controlled switch peak current ratings, iTpeak.
d) Diode average current ratings, iTavg.
e) Diode rms current ratings, iDrms.
f) Diode peak current ratings, iDpeak.

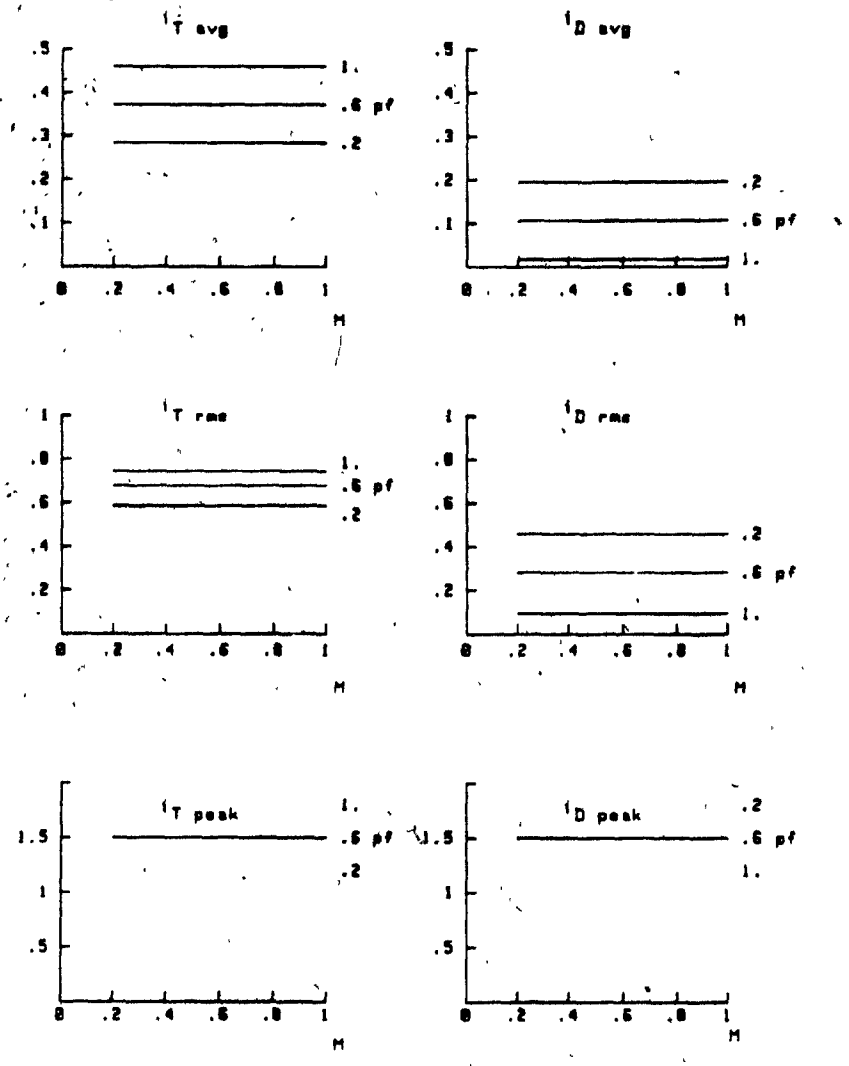


Fig.(3.11): Normalized component ratings with the fixed PWM scheme Fig.(4.7).

a) Controlled switch average current ratings, iTavg.
b) Controlled switch rms current ratings, iTrms.
c) Controlled switch peak current ratings, iTpeak.
d) Diode average current ratings, iTavg.
e) Diode rms current ratings, iDrms.
f) Diode peak current ratings, iDpeak.

3.5 A SPWM Voltage Source Design Example

In order to illustrate the significance and facilitate understanding of the generalized design curves Fig's.(3.9), (3.10), and (3.11) the following design example is presented.

Example:

Obtain the ratings of a three phase SPWM VSI Fig.(3.1) with the following specifications:

i) 30 KVA rated output power,

ii) 100 Vrms rated output phase voltage,

iii) $0.6 < pf < 1.0$ power factor range (inductive), (3.9)

iv) $0.7 < M < 1.0$ modulation factor range.

Solution:

$$\text{rated line current} = \frac{30{,}000}{3.100} = 100\ [A] \tag{3.10}$$

using (3.7) and (3.9),

$$1\ \text{pu current} = \frac{100}{1.061} = 94\ [A]\ \text{rms} \tag{3.11}$$

Solution 1: contemporary design approach method for SPWM,

using Table(2.5) and (3.10),

$$i_{T\,avg} = i_{D\,avg} = .48 \cdot 94 = 45.1\ [A]$$

iT rms= iD rms= .75 · 94= 70.5 [A]

iT peak= iD peak= 1.5 · 94= 141 [A]

Vpeak = (2/.707) · 100 = 283 [V] , [24].

Solution 2: improved design method for SPWM

iT avg= .425 · 94= 40 [A] ; Fig.(3.9a), pf =1., M =1.

iT rms= .72 · 94= 68 [A] ; Fig.(3.9b) , pf =1., M =1.

iT peak= 1.5 · 94= 141 [A] ; Fig.(3.9c).

Vpeak = (2/.707) · 100 = 283 [V] , [24].

iD avg = .16 · 94= 15 [A] ; Fig.(3.9d) , pf =.6, M =.7

iD rms= .42 · 94= 40 [A] ; Fig.(3.9e) , pf =.6, M =.7

iD peak= 1.5 · 94= 141 [A] ; Fig.(3.9f) .

Vpeak = (2/.707) · 100 = 283 [V] ; [24].

Discussion:

To have a quantitative idea of the ratings improvement in the semiconductor ratings accomplished with the proposed design method, consider the Svuf (3.2) ratio of the solutions 1 and 2,

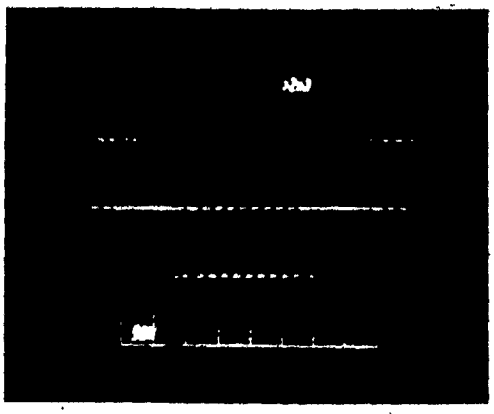
$$\text{improvement ratio} = \frac{S_{VUF2}}{S_{VUF1}} = \frac{(.48+.48)}{(.425+.16)} = 1.64 \qquad (3.12)$$

Therefore, a 64 % improvement in the semiconductor utilization factor, as defined in (3.2), has been obtained with the improved design approach in this particular example.

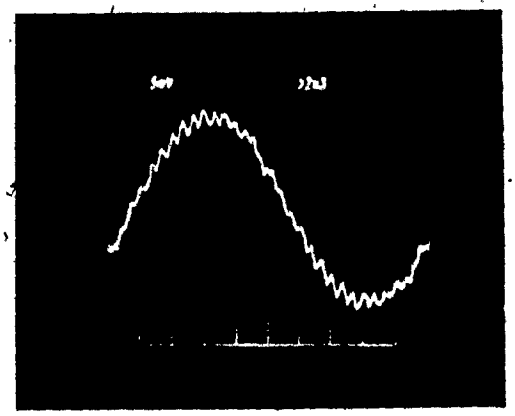
3.6 Experimental Results

To check the validity of the proposed design method, selected theoretical results were verified with an experimental 2 KVA unit. Primarily due to the fact that SPWM has been utilized in a large number of applications, the subject scheme was selected to compare analytical and experimental results.

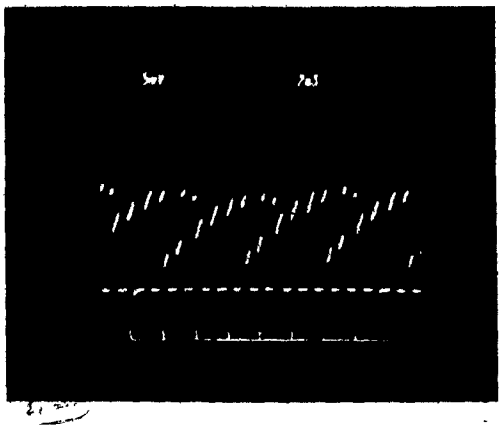
Fig's.(3.12a) and (3.12b) show experimental inverter output line to line voltage Vab(wt) and line current ia(wt) waveforms, Fig.(3.12c) shows the inverter switch current isw(wt), finally, Fig's.(3.12d) and (3.12e) show the inverter input current id(wt) and respective input spectrum. A comparison of this experimental data with the analytical results shown in Fig's.(3.2c), (3.6b), (3.6d), (3.6g), and (3.6h) reveals a close agreement between current and voltage waveforms. A quantitive measure of the precision, predicted waveforms against experimental results, is obtained by comparing predicted and experimental semiconductor ratings. Fig.(3.13) shows predicted and experimental results for the SPWM control scheme. To facilitate comparison, both experimental and predicted results have been plotted on the same set of axes. A difference between predicted and experimental below 3 % was obtained in the comparison. This figure should be considered quite acceptable.



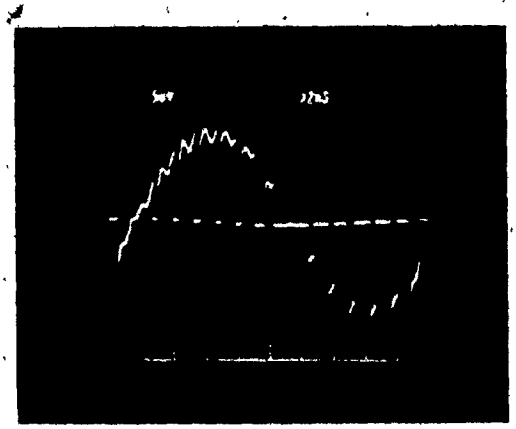
50 [V]/div.
fo= 60 Hz.
a) Inverter output line-line voltage, Vab.



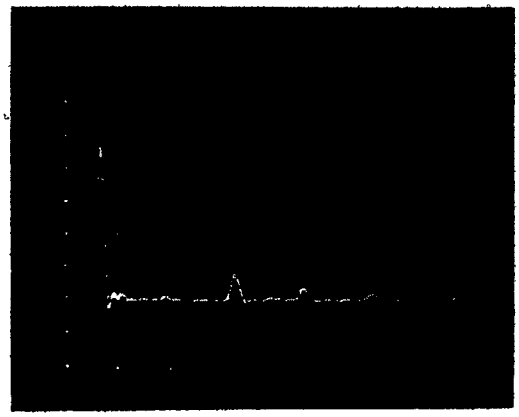
4 [A]/div.
fo= 60 Hz.
b) Inverter output line current, ia.



4 [A]/div.
fo= 60 Hz.
c) Inverter input current, id.



4 [A]/div.
fo= 60 Hz.
d) Inverter switch current, is(wt).



e) Frequency spectrum of the inverter input current, id.

Fig.(3.12): Experimental inverter voltage and current waveforms with the SPWM control scheme (M=1 and load pf=.8).

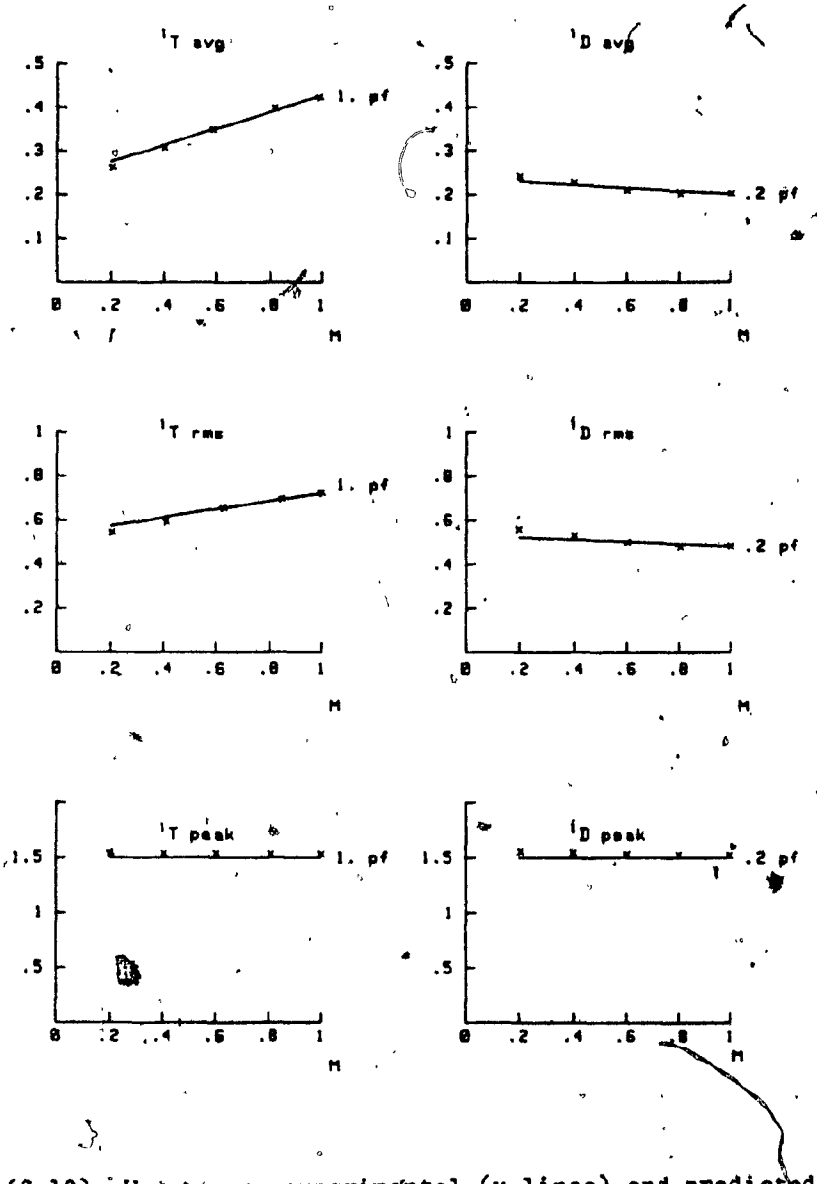


Fig.(3.13): Worst case experimental (x lines) and predicted (solid lines) inverter component current ratings with the SPWM control scheme.

a) Controlled switch average current ratings, iTavg.
b) Controlled switch rms current ratings, iTrms.
c) Controlled switch peak current ratings, iTpeak.
d) Diode average current ratings, iTavg.
e) Diode rms current ratings, iDrms.
f) Diode peak current ratings, iDpeak.

3.7 Conclusions

A generalized design approach that maximizes the utilization of semiconductor components in voltage source inverters has been proposed in this chapter. This approach has also been used to identify a source of switch component under-utilization introduced by the typical "cut and try" design approach of voltage source inverters.

The improvement of switch utilization accomplished over the typical design method depends on the required range of operation of the inverter (a 64 % improvement has been obtained in a specific example in this chapter). Therefore, is not possible to give a specific figure for the switch utilization improvement that can be accomplished. However, at least a 45 % improvement is obtained if the VSI requires the full modulation and power factor ranges considered in this chapter. Furthermore, its application is simple and direct, as observed from the given generalized design curves. Also, because of its intrinsical simplicity, the approach can be extended to any power converter configuration and implemented in personal computers. The resulting design curves were expressed in per-unit form for maximum applicability. Finally, selected predicted results have been verified experimentally on a two KVA laboratory prototype unit.

CHAPTER 4

IMPROVED POWER SUPPLY FOR FIXED FREQUENCY OPERATION

4.1 Introduction

This chapter presents a circuit topology and respective control strategies intended to improve the power conversion process in fixed-frequency power supplies. From the large family of applications of fixed-voltage fixed-frequency power supply systems, UPS have been selected to illustrate this study in a practical application. In particular, this chapter presents an evaluation of the design practices of static uninterruptible power supplies (UPS) systems and proposes a new circuit topology, based on the regulation of the dc link, to significantly improve the UPS power conversion process.

Solid state UPS systems are widely employed today to maintain an uninterruptible flow of high quality power to a critical load, independent of the status of the ac line voltage. The continuity of the energy supply is usually ensured with the use of batteries capable of storing enough energy to overcome prolonged ac line voltage interruptions. In UPS applications the battery's voltage E is typically allowed to vary from 20% below to 10% above its rated value. However, while the dc link voltage E varies, the amplitude of the ac load voltage must be kept constant. This performance requirement is usually met by varying the degree of modulation in the inverter output phase voltage Vao. Since the fundamental component Vaol of Vao is proportional to the modulation index M, it follows that the lowest M

value will correspond to the highest dc link voltage Em value and vice-versa. Therefore, the dc link is normally operating with close to Em voltage conditions (max. dc link voltage), and the UPS inverter is forced to operate with close to minimum modulation index value Mmin for most of its ON time (see Fig.(4.4)). Consequently, the dc link is under-utilized by a factor:

$$DU = 100 \left(1 - \frac{M_{min}}{M_{max}}\right) \% \qquad (4.1)$$

Eq.(4.1) also implies that the current ratings of the UPS inverter increase by the same factor for the same output power.

To appreciate the implications on UPS performance of a modulation scheme, consider the simplified circuit diagram of a typical 3-Ø UPS system shown in Fig.(4.1). Furthermore, Fig.(4.3) shows a voltage and harmonic control scheme frequently employed with the UPS inverter, while Fig.(4.4) illustrates the relation between the modulation index M and the dc link voltage E for the same system.

The specific rms values for the fundamental components of the voltages Vao, Vbo, Vco (as defined in Fig.(4.2)) resulting from the sine modulation scheme shown in Fig.(4.3) [24] are:

$$V_{a01} = V_{b01} = V_{c01} = M\left(\frac{E}{2}\right)\sqrt{2} = M(.354\ E); \quad 0<M<1 \qquad (4.2)$$

However, the respective maximum rms values that are possible with any modulation technique are (square wave or six-step control scheme, see Fig.(3.3))

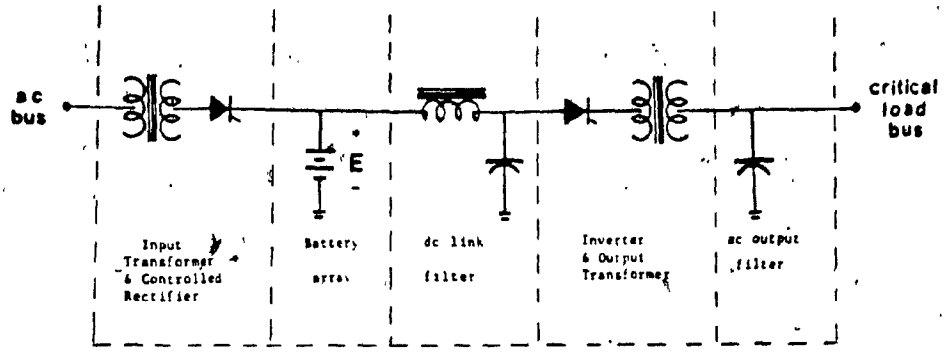


FIG.(4.1): Simplified line diagram of UPS system

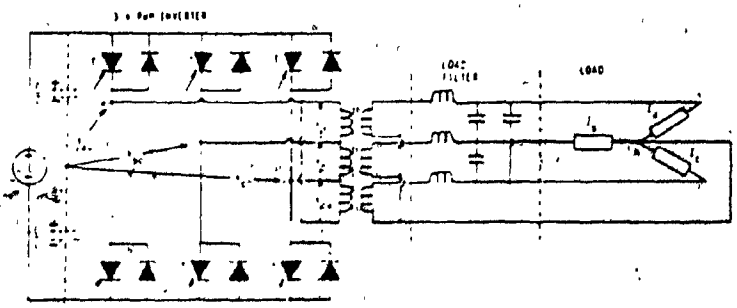


FIG.(4.2): Simplified circuit for the UPS inverter, transformer and filter components

$$V_{a01} = V_{b01} = V_{c01} = \frac{4E}{\pi 2\sqrt{2}} = \frac{\sqrt{2}\,E}{\pi} = 0.45\ E \qquad (4.3)$$

Eqs.(4.2) and (4.3) show that because of the sine modulation technique alone, the maximum utilization factor (M=1) for the link voltage is only

$$FU_m = \frac{M(0.354)E}{(0.45)E} = 0.79; \quad (M=1) \qquad (4.4)$$

Moreover, Fig.(4.4) shows that with maximum dc link voltage (i.e. E=Em, max mains operation), the modulation index M value is

$$M = 0.727 \qquad (4.5)$$

Expressions (4.5) and (4.2) imply that, because of the expected voltage variation alone, the utilization for the link voltage is only

$$FU_v = \frac{M(0.354\ E)}{(0.354\ E)} = 0.727 \qquad (4.6)$$

Finally, from (4.6) and (4.4), the overall utilization factor with normal mains operation is found to be

$$FU_o = (FU_m)(FU_v) = (0.79)(0.727) = 0.57 \qquad (4.7)$$

The equivalent load power factor Pfe "seen" by the UPS inverter is also related to the FU factor and is defined as

$$P_{Fe} = \frac{\text{Real inverter output power}}{\text{Apparent inverter output power}} \qquad (4.8)$$

By considering the phase voltage waveforms shown in Fig.(4.3) and the

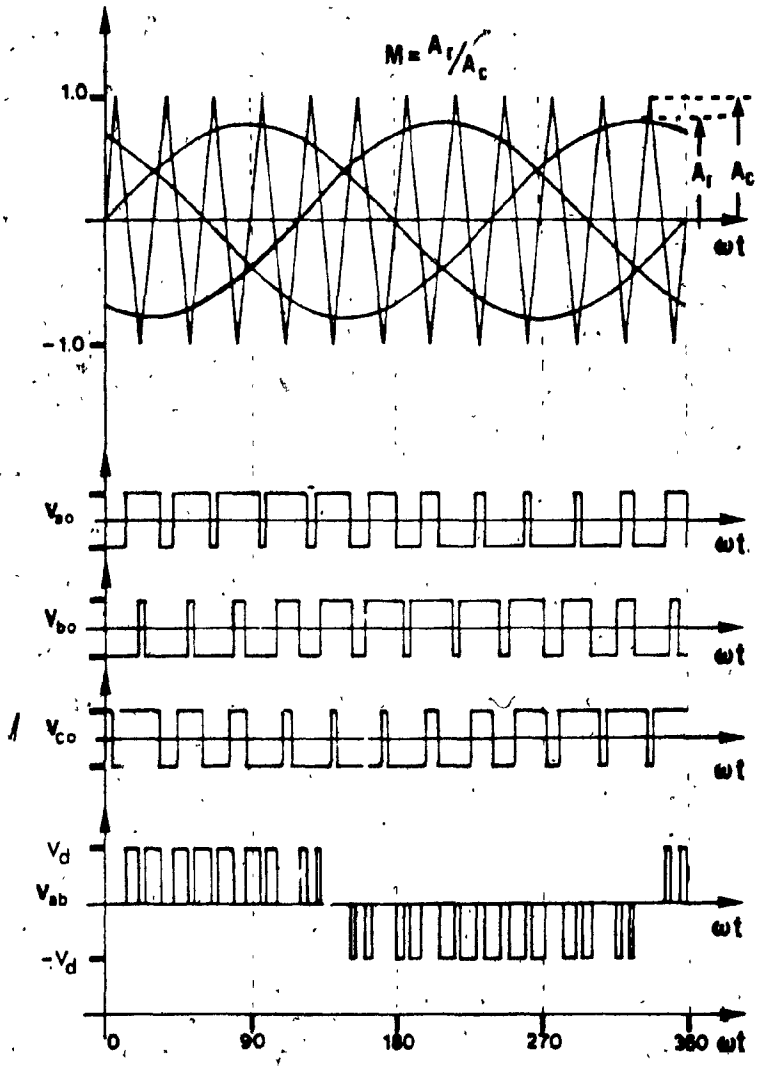


Fig.(4.3): The sine PWM control scheme usually employed in VSI for UPS (voltages Vao, Vbo, Vco, and Vab defined in Fig.(4.2)).

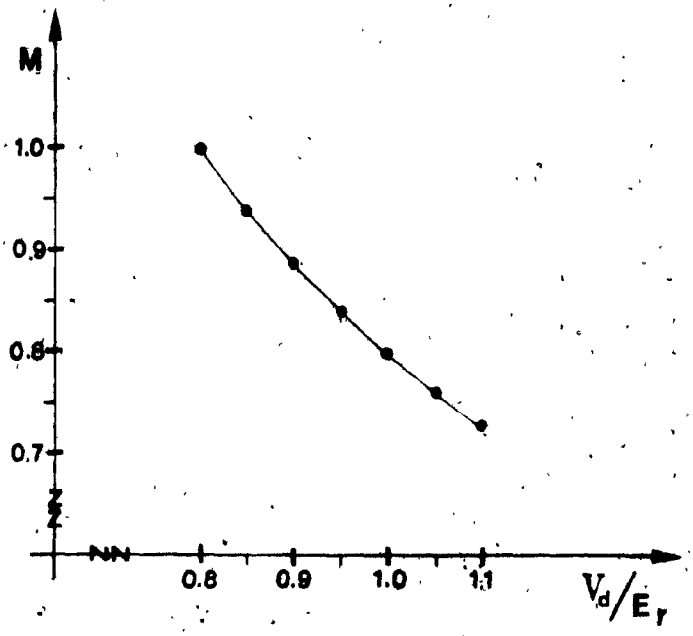


Fig.(4.4): Required VSI modulation factor as a factor of the normalized dc link voltage.

values for the effective voltage components obtained in (4.2), the equation (4.8) can be re-written as

$$P_{Fe} = \frac{(\frac{ME}{2\sqrt{2}})(I_a)(\cos\phi)}{(\frac{E}{2})(I_a)} = \frac{M}{\sqrt{2}}\cos\phi \qquad (4.9)$$

where ia(t) has been assumed sinusoidal (e.g. ia(wt)=Ia cos(wt)).

By considering the values for the effective voltage components obtained in (4.3), the maximum possible Pfe value is:

$$P_{Fe,\ max} = \frac{(\frac{\sqrt{2}E}{\pi})(I_a)(\cos\phi)}{(\frac{E}{2})(I_a)} = 0.9\cos\phi \qquad (4.10)$$

Eq.(4.9) shows that even with M=1, Pfe=0.707cos(0). From this and eq.(4.10), it is clear that the sine modulation alone reduces the effective load Pfe value from

$$P_{fe} = 0.9\cos(\phi)$$

to (4.11)

$$P_{fe} = 0.707\cos(\phi)$$

Furthermore, by employing the M value from (4.5) in (4.9), the variation of the dc link voltage alone reduces the effective load Pfe from

$$P_{fe} = 0.707\cos(\phi)$$

to

$$P_{fe} = (0.727)(0.707)\cos(\phi) = 0.51\cos(\phi) \qquad (4.12)$$

Pfe reduction means that (for the same component ratings) the UPS inverter can supply less power to the load. Therefore, the more the Pfe is reduced, the more the inverter is under-utilized. Finally, from (4.11) and (4.12), the combined effect of modulation and dc link voltage variation on the equivalent Pfe is to reduce its value from

$$P_{fe} = 0.9 \cos(\phi)$$

to (4.13)

$$P_{fe} = 0.51 \cos(\phi)$$

To conclude, (4.7) and (4.13) underline the need for upgrading power conversion practices on UPS systems. Two approaches for achieving this objective are discussed in the next section.

4.2 The dc Link Voltage Boost Approach

The outline of the UPS performance problems previously discussed suggests that one solution is to introduce a voltage boosting stage between the battery and the inverter. Such an approach is illustrated in Fig.(4.5), with the operation of the booster chopper described, and is analyzed briefly in Appendix 3. There are two basic methods available to control the dc link voltage E, the partial chopper utilization or PCU method, and the continuous chopper utilization or CCU method. A detailed description of these methods follows.

4.2.1 The PCU voltage control method

The main feature of the PCU method is that the secondary dc link voltage Vd is allowed to vary only between

$$E_m > V_d > E_r \tag{4.14}$$

To prevent the inverter input voltage Vd from decreasing below Er, a suitable voltage sensing circuit activates the boost chopper during fault intervals of ac mains. However, since such intervals account for only a small percentage of the overall ON UPS time, the boost chopper ON time is even smaller percentage-wise. Accordingly, the negative effect of cascading an extra power stage on the overall system efficiency is negligible. Moreover, with the PCU technique, the boost chopper gain Gc defined as

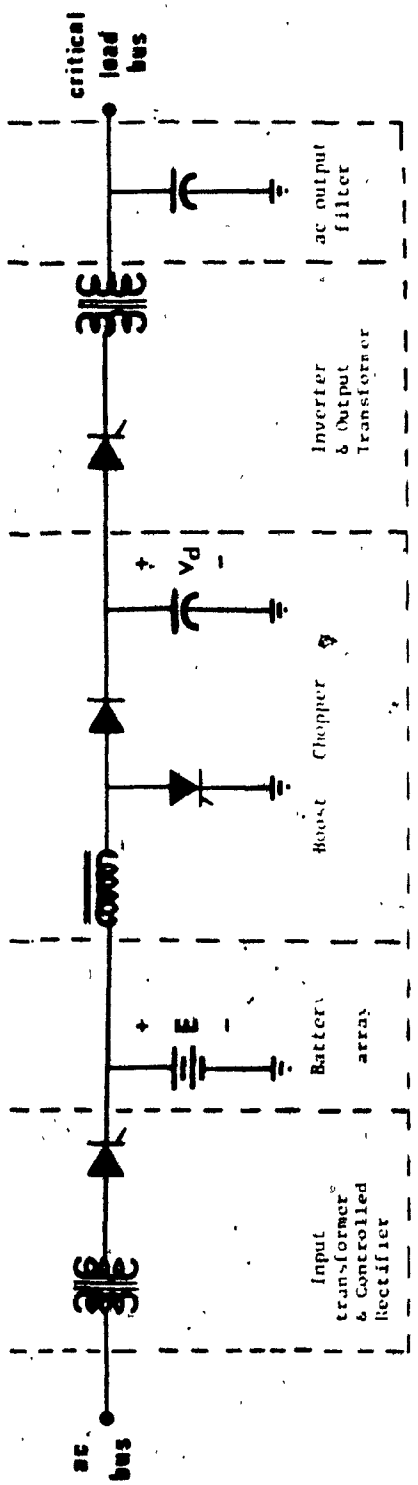


FIG.(4.5): Simplified line diagram of a UPS system with a dc link voltage boost stage

$$G_c = \frac{V_d}{E} \qquad (4.15)$$

varies between

$$1 \leq G_c \leq 1.25 \qquad (4.16)$$

as primary dc link voltage E varies between

$$E_r \geq V_d \geq 0.8\, E_r \qquad (4.17)$$

Such a low range of gain implies low average and rms current ratings for the chopper switch Swc and simple chopper (close loop) control requirements for the regulation of the dc link voltage. With the inverter input voltage Vd varying as shown in (4.14), the UPS load voltage is maintained constant by varying (within UPS inverter) the modulation index M value between

$$M_{rated} \leq M \leq 1 \qquad (4.18)$$

respectively. Expressions (4.14) and (4.18) imply that, with maximum dc link voltage, the modulation index value is theoretically equal to 0.91. Therefore, with the PCU voltage control method, the FUv factor exp.(4.6) is equal to 0.91, the FUm factor exp.(4.4) remains equal to 0.79 and the overall dc link utilization factor FUo improves from

$FU_o = 0.57$ expr. (4.7)

to (4.19)

$FU_o = (0.91)(0.79) = 0.72$

Moreover, with M=0.91, the system power factor Pfe as seen by the UPS inverter (4.9), is found to be

$$P_{Fe} = \frac{M}{\sqrt{2}} \cos(\phi) = 0.64 \cos(\phi) \qquad (4.20)$$

Again, as expected, the PCU method improves the Pfe value from

$P_{fe} = 0.51 \cos(\phi)$ expr. (4.12)

to (4.21)

$P_{fe} = 0.64 \cos(\phi)$ expr. (4.20)

For comparison, the results for FUo and Pfe, obtained with and without the use of the PCU voltage control method, are shown in Table(4.3). From these results alone, it is clear that the application of the PCU method enhances significantly the performance of the overall UPS system.

Finally, the PWM scheme employed with the UPS must be capable of maintaining a load voltage with very low total harmonic distortion (4.22) (typically less than 5 %), while the modulation index M varies within specific limits (4.18)). Thus, PWM schemes with continuosly variable switching patterns are required [27]. Fixed switching pattern

schemes become possible with the dc link voltage control method next discussed.

$$THD = \frac{1}{\text{fundamental}} \left(\sum_{n=2}^{\infty} (n^{th} \text{ harmonic component})^2 \right)^{1/2} \qquad (4.22)$$

4.2.2 The CCU voltage control method

With the CCU, the inverter input voltage Vd (see Fig.4.5) becomes independent of the primary link voltage E. This is achieved by using the boost chopper as a step-up dc/dc transformer with a voltage gain continuosly adjusted to maintain a constant ac load voltage. Such an arrangement increases significantly the range of options in choosing:

i) the operating (rated) value of the secondary dc link voltage Vd, or

ii) the PWM scheme to be used with the UPS inverter.

It also considerably simplifies the hardware implementation of the PWM inverter controller.

Regarding the choice of the secondary dc link Vd, it is generally true that the higher the input voltage the lower the conduction losses. Also, the commutation circuits of thyristor inverters become smaller in size and their ohmic losses decrease. However, since the maximum Vd value is always lower than the maximum specified forward blocking voltage of the boost chopper and inverter switches, there is a limit in the value Vd to be chosen. Another crucial limiting factor is the current ratings of the booster switch, which increase as the gain of the chopper increases. This relation is described by eqns.(A3.5) and

(A3.6) in Appendix 3.

When choosing the PWM scheme, the range is now extended to include (in addition to schemes with continuously variable switching patterns, (see Fig.4.3)) schemes with fixed switching patterns (such as the ones shown in Fig.(4.6) and (4.7)). These latter schemes are shown to offer, in general, better dc bus utilization at reduced switching frequencies. Also, since the objective of this chapter is to present a more efficient UPS system, it becomes necessary to identify the most efficient fixed pattern PWM scheme. The criteria for doing so are as follows:

i) minimization of the distortion factor (DF) of the output voltage

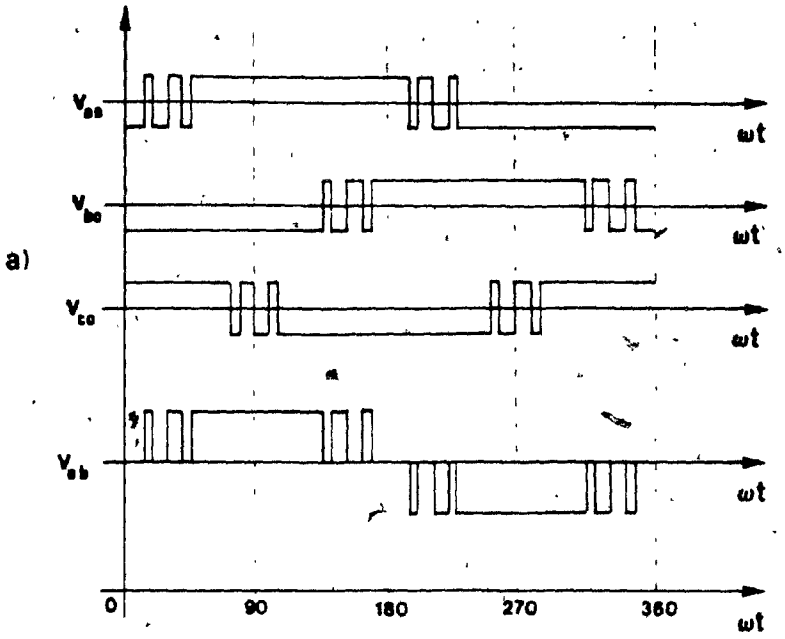
$$DF[\%] = \frac{1}{\text{fundamental}} \left(\sum_{n=2}^{\infty} \frac{(n^{th} \text{ harmonic component})^2}{n^2} \right)^{1/2} \qquad (4.23)$$

where n represents the harmonic attenuation factor of a second order (typical in UPS) load filter.

ii) to minimize the switching frequency (fs) required to obtain a prescribed DF value, and

iii) to maximize the amplitude of the effective value of the fundamental component Vaol of the output voltage vao.

Relevant results for DF, fs and Vaol obtained with the sine PWM scheme and a proposed fixed PWM scheme, (see Fig.(4.6) and (4.7)) are



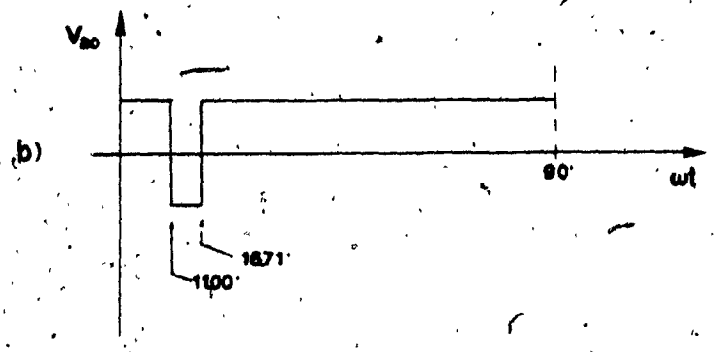
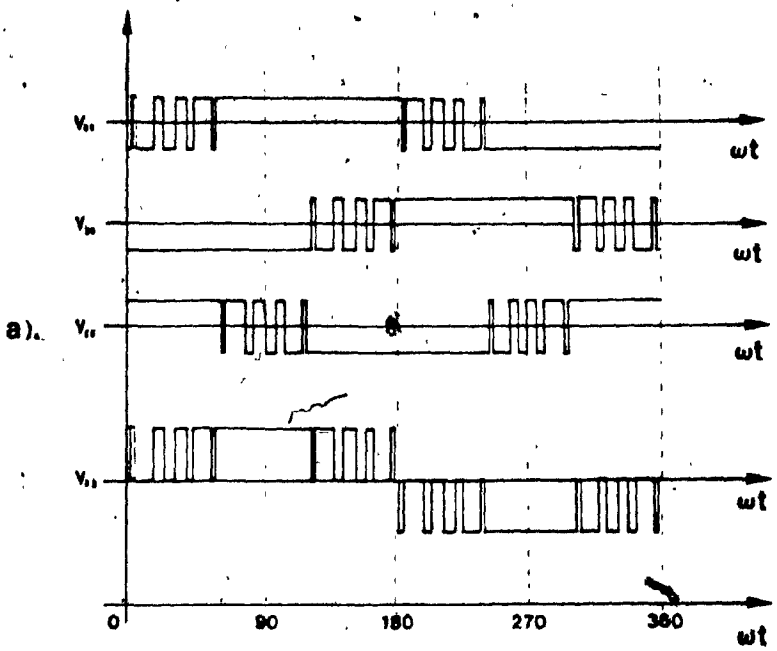


FIG.(4.6): Proposed Inverter PWM scheme for the UPS system shown in Fig. 5, with a switching frequency f_s = 600 [comm./sec] per switch.

(a) Phase and line inverter voltages
(b) Exact switching angles. (waveform posseses quarter-wave symmetry)



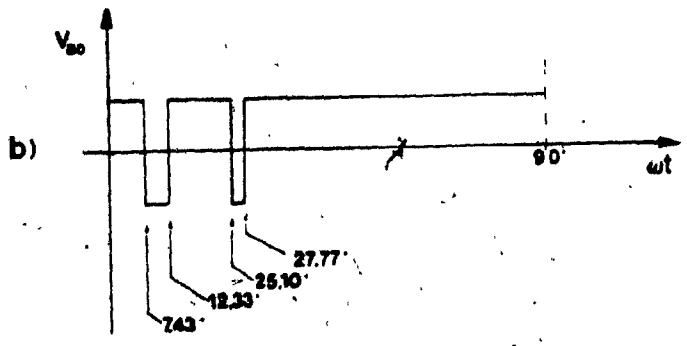


FIG.(4.7): Propbsed Inverter PWM scheme for the UPS system shown in Fig. 5, with a switching frequency f_s = 1080 [comm/sec] per switch.

(a) Phase and line inverter voltages
(b) Exact switching angles (waveform possesses quarter wave symmetry)

presented in Table 1. The application of the criteria defined above shows that the PWM scheme, which consistently yields the lowest DF and highest effective Vaol values, while requiring the least number of commutations, per cycle is the proposed scheme. It is again noted that with the CCU voltage control method the chopper gain Gc is varied continuously to render the load voltage independent of changes in dc link voltages or in loading conditions. Consequently, the variation of the main link voltage E has no effect on the use of the secondary link voltage vd and the related utilization of the UPS inverter. Therefore, the resulting utilization factor is

$$FU_v = 1 \qquad (4.24)$$

Inverter and link voltage utilization, however, are still slightly affected by the proposed PWM scheme and this is shown in the following paragraphs.

The rms values of the fundamental components of the voltages Vao, Vbo, Vco with the proposed modulation scheme (see Table (4.1)) are

$$V_{a01} = V_{b01} = V_{c01} = 0.857 \left(\frac{V_d}{2}\right) = 0.43\ V_d \text{ (with DF=0.168)} \qquad (4.25)$$

$$V_{a01} = V_{b01} = V_{c01} = 0.837 \left(\frac{V_d}{2}\right) = 0.42\ V_d \text{ (with DF=0.075)} \qquad (4.26)$$

and from (4.3) and (4.25), the subject utilization factor is found to be

$$FU_m = \frac{0.43}{0.45} = 0.95 \qquad (4.27)$$

Moreover, from (4.23) and (4.27), the overall utilization factor is

$$FU_o = (FU_M)(FU_V) = 0.95 \qquad (4.28)$$

When this FUo is compared to the respective value obtained with (4.7) it can be seen that, with the CCU approach, the FUo factor is improved by

$$\Delta\ FU_o = 100\ \frac{(0.95 - 0.57)}{0.57} = 67\ [\%] \qquad (4.29)$$

Similarly, from (4.8) and (4.24), the value of the effective load Pfe "seen" by the UPS inverter is found to be

$$P_{fe} = \frac{(0.43\ E)\ I_a\ \cos\phi}{(0.5\ E)\ I_a} = 0.86\ \cos(\phi) \qquad (4.30)$$

When this Pfe value is compared to the respective value obtained with (4.12), Pfe improves by

$$\Delta\ P_{fe} = 100\ \frac{(0.86 - 0.51)}{0.51} = 67\ [\%] \qquad (4.31)$$

It is worth noting that (4.29) and (4.31) also mean that, by introducing the CCU control method, the KVA rating of the UPS system could be increased by at least 65 [%] without exceeding the voltage and current ratings of its components.

MODULATION SCHEMES	SWITCHING FREQ. f_s	PER UNIT max V_{01}	DISTORTION FACTOR
S P W M (N = 1) SCHEME	1080	0.707	0.701
	1800	0.707	0.221
PATEL HOFT SCHEME	600	0.840	0.240
	1320	0.825	0.077
PROPOSED SCHEME	600	0.857	0.168
	1080	0.837	0.075

Table (4.1): Comparison of PWM schemes.

4.3 UPS Inverter Input-Output Spectra

UPS systems specifications require that voltage and current harmonics generated by the inverter be attenuated to an acceptable level. This is achieved through the use of suitable input and output filters with size, weight, and price directly related to the amplitude and order of inverter harmonics. Therefore, a comprehensive evaluation of any new approach requires that generated harmonics be identified and compared against respective harmonics generated when other approaches are used.

Based on the functional converter model developed in Chapter 2, (also see Fig's.(3.2) and (3.6) and, Fig's.(3.4) and (3.8)), the inverter input current spectrum and the inverter output voltage spectrum have been computed. The results obtained using the proposed pattern in Fig.(4.7) (CCU approach), and the sine PWM in Fig.(4.3) (PCU and CCU approach) are shown in Table(4.2). For comparison purposes, these results have been computed with the following common conditions:

i) the load power factor is 0.8 lagging (worst case),
ii) second order filter values as depicted in Fig.(4.8),
iii) switching frequency of 1080 [comm/cycle] per switch,
iv) sine PWM with modulation index one, and
v) dc link input inverter voltage Vd is ripple free, (harmonics generated by the booster are negligible, see Appendix 3).

Comparison of values for respective quantities shown in Table(4.2) yields the following conclusions:

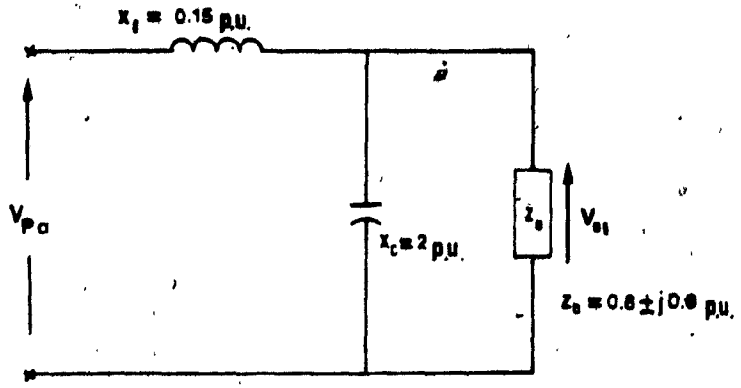


FIG.(4.8): Load Filter Configuration

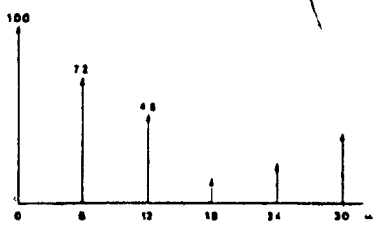
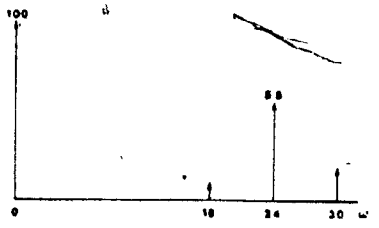
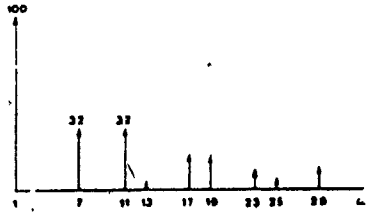
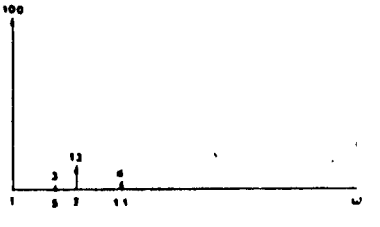
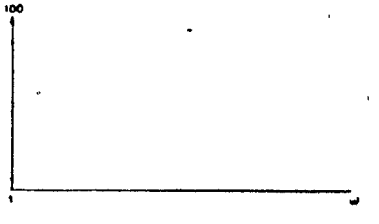
	SPWM SCHEME (M=1) fs = 1080 [comm/cycle]	PROPOSED SCHEME fs = 1080 [comm/cycle]
INVERTER INPUT CURRENT SPECTRUM	 DF = 1.49	 DF = 0.09
INVERTER PHASE OUTPUT VOLTAGE SPECTRUM	 DF = 0.701	 DF = 0.075
OUTPUT LOAD VOLTAGE	 THD = 14.44	 THD = 1.17

Table (4.2): Predicted input-output spectra.

i) the input current distortion factor (defined in (4.12)) is drastically reduced with the proposed approach, so an input filter designed to meet standard THD (4.22) levels will be considerably smaller,

ii) similarly, the smaller distortion factor obtained with the proposed pattern results in a smaller THD at the load voltage,

iii) this second point also implies that, in order to meet standard THD load voltage specifications, the proposed approach requires a smaller output filter.

4.4 Experimental Results

To verify some key predicted results for the CCU approach, an experimental 2 KVA unit has been implemented. The results displayed in Fig. (4.9) were obtained under the same conditions assumed in the analysis performed in the previous section. Specifically, Fig. (4.9a) shows the inverter input current and its spectrum. Fig. (4.9b) shows the inverter phase output voltage (which can be compared with Fig. (4.7) and its spectrum, and Fig. (4.9c) displays the load phase voltage and its spectrum. A direct comparison between the predicted input and output harmonic spectra for the proposed scheme (see Table (4.2)) and Fig. (4.9) shows that they agree.

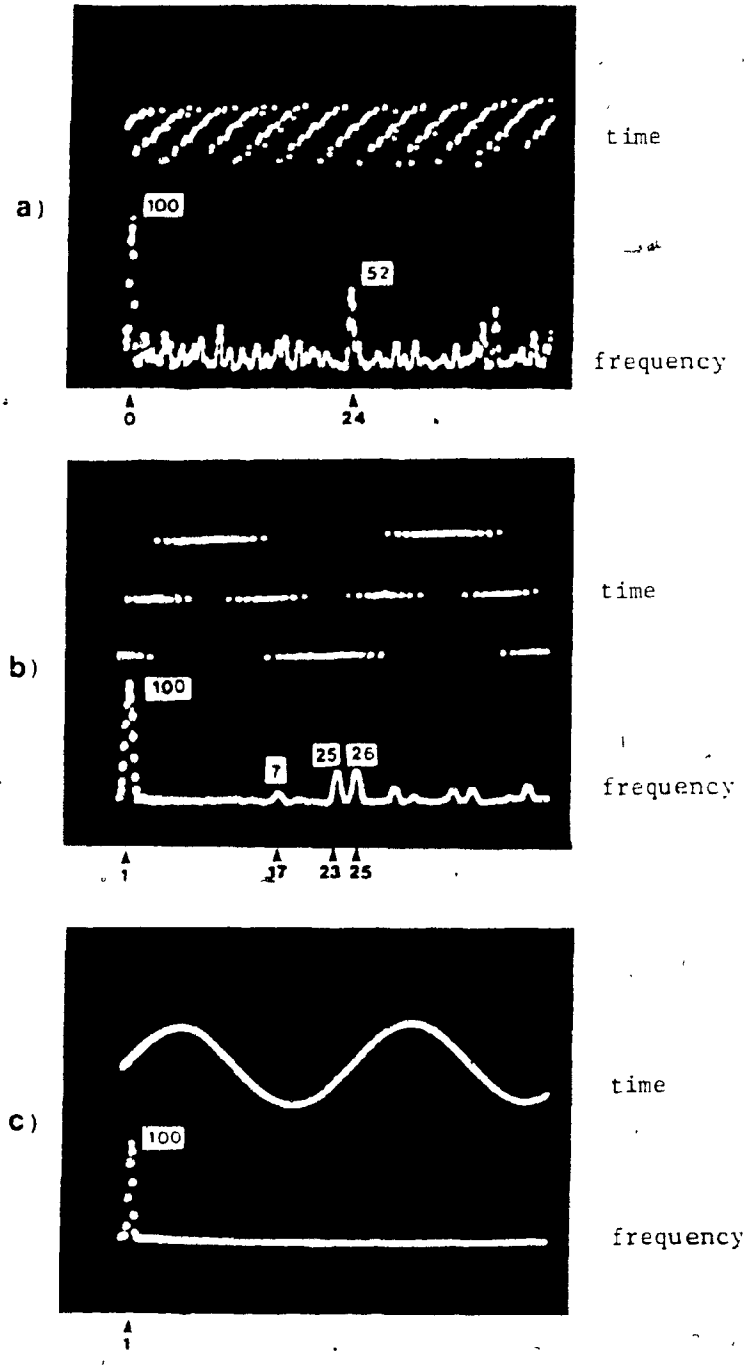


FIG.(4.9): Experimental input-output characteristics.

a) Inverter input current and its spectrum (8[A] zero to peak) and its spectrum.

b) Inverter output voltage (135[V] zero to peak) and its spectrum.

c) Output phase load voltage (110 $\sqrt{2}$ zero to peak)

4.5 Discussion

To facilitate comparison between current and proposed methods of power conversion for UPS, relevant performance data is summarized in Table(4.3). This data clearly demonstrates that the proposed methods yield a significant improvement in the system component utilization. Particularly, the CCU approach ensures an improvement of at least 65 [%] in the use of inverter components and a considerable reduction in the size of the required input-output second order filter components. Along with their advantages, the proposed power conversion methods also have certain disadvantages.

i) The extra boost chopper (see Fig.4.5) contributes to the price and complexity of the UPS system.

ii) The boost chopper also contributes to the conditions and switching losses of the UPS system.

iii) The regulation of the secondary dc bus voltage Vd requires a control loop.

In spite of these disadvantages, however, one should consider that:

i) the chopper contribution to price and complexity is cancelled by the resulting increase in the output power rating (e.g. (4.29) and (4.31)) of the UPS system. Also, the inverter control hardware is drastically simplified with the use of fixed pattern for the CCU method.

	TYPICAL APPROACH	PROPOSED PCU APPROACH	PROPOSED CCU APPROACH
INPUT INVERTER CURRENT DISTORTION	1.49	1.49	0.09
OUTPUT INVERTER VOLTAGE DISTORTION.	0.701	0.701	0.075
OVERALL VOLTAGE UTILIZATION FU_o	0.57	0.72	0.95
EFFECTIVE POWER FACTOR Pf_e	0.51	0.54	0.86

Table (4.3): Relevant UPS performance data.

ii) In relative terms, losses increase less than the increase in the output KVA. Therefore, the overall system efficiency improves.

iii) The extra control loop is required only by the PCU method. For the CCU method, the number of control loops remain the same because the voltage loop that was originally required to adjust the modulation factor M has been removed.

4.6 Conclusions

This chapter has examined the process of power conversion in fixed-frequency power supplies. In particular, for UPS systems it has been shown that some popular power conversion methods lead to severe under-utilization of the dc bus and deterioration of the effective load power factor. To ameliorate this situation, a power conversion approach which uses a secondary regulated dc bus has been proposed. In addition, two different methods for using this bus have been fully described. With one of these methods, an improved switching scheme for the UPS inverter has been identified. Finally, it has been clearly shown (see Table(4.3)) that the proposed approach significantly improves dc bus utilization and effective load power factor for UPS.

CHAPTER 5

NOVEL POWER SUPPLY FOR VARIABLE FREQUENCY OPERATION

5.1 Introduction

This chapter presents a novel variable frequency power supply intended primarily for ac drive applications. This is an area of increasing expansion due to the industrial trend towards automation and high reliability systems. Today's typical power supplies for variable speed ac drives consist of: a front-end thyristor rectifier or uncontrolled diode rectifier, a dc link, and a PWM voltage source variable frequency-inverter. With this arrangement most load performance specifications can be met at a reasonable power supply cost. However, this power conversion approach has several intrinsic disadvantages, which include:

i) poor system reliability, since voltage source inverters are very susceptible to "shoot-through's" and load short circuits,

ii) lack of capability for sustained power regeneration unless an additional controlled rectifier is employed,

iii) utilization of complex techniques to control current instead of voltage, which in turn allows direct motor torque control for better drive performance [41], and

iv) large fifth and seventh current harmonics in ac main lines.

The alternative to the aforementioned approach is to utilize a

current source power supply. This alternative would improve system reliability and capability for sustained power regeneration, but the current source approach would introduce its own intrinsic disadvantages. These include:

i) presence of a large dc filter choke to obtain current source characteristics,

ii) slow current response because of the presence of the large dc choke and the slow response of the front end phase controlled rectifier,

iii) excessive over voltage stresses (i.e. voltage spikes) because of abrupt current changes in inductive load (i.e. motor),

iv) poor system input power factor, especially at low current levels, because of the front end rectifier.

From the preceding discussion it is apparent that unless voltage and current source power conversion methods are significantly changed and improved, some basic performance disadvantages will always be present. The changes proposed in this chapter focus on current-source power supplies and eliminate all aforementioned disadvantages. They moreover, add the novel feature of having practically sinusoidal voltage and currents waveforms at both the input and the output terminals of the power supply. The configuration of a variable frequency static power supply that incorporates these changes is next discussed in detail.

5.2 Power Supply Configuration

A configuration of the variable frequency static power supply system that incorporates a significantly different and improved current source power conversion is shown in Fig.(5.1). The nature and functions performed by each major system component are described next as follows.

The first major system component is a PWM 3-Ø rectifier. The system's current source is comprised of the rectifier and the dc link reactor. The main function of this component is to regulate the level of the dc link current in response to changes in load and ac input voltage conditions. The traditional phase controlled rectifier has been replaced here by a PWM rectifier that employs the advanced PWM technique shown in Fig.(5.2) [46]. The implementation of the PWM technique requires gate turn-off switching devices such as bipolar or FET transistors, GTO's, etc., to be used as unilateral rectifier switches. The resulting rectifier structure has a number of advantages [21]. These include, drastically improved levels of input-output current-voltage harmonic distortion. This feature allows a proportional reduction in the size of the input ac filter and improvement in the rectifier input power factor. Moreover, the low harmonic distortion of the rectifier together with a low level of generated input CSI voltage harmonics allows a significant reduction in the size of the dc link reactor.

The second major system component is the current source reactor

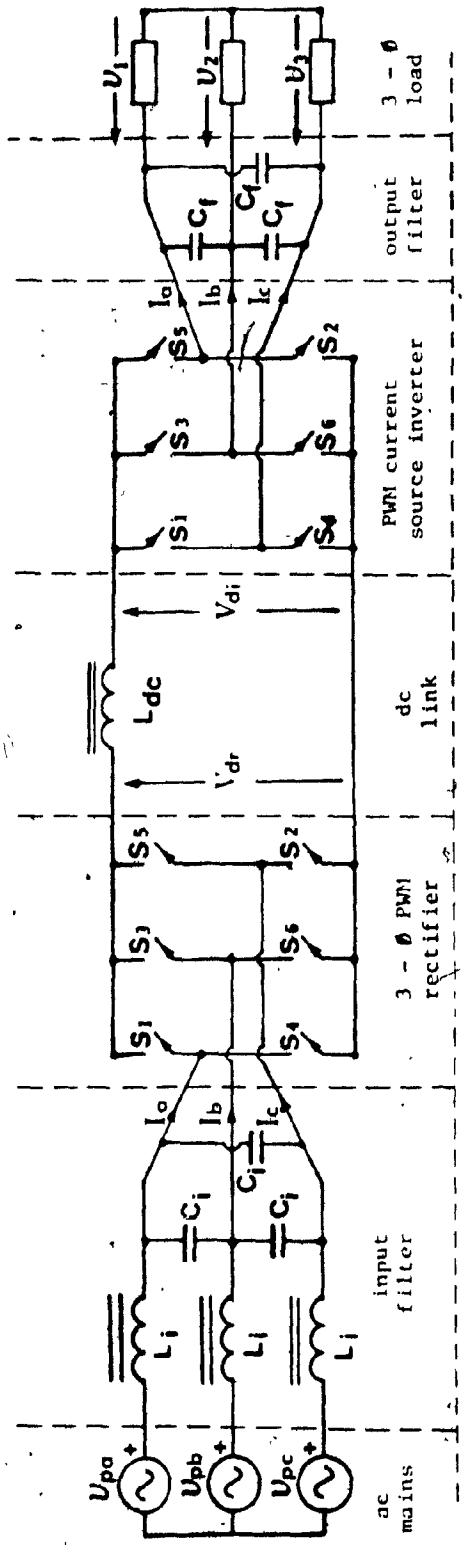


Fig.(5.1): A simplified circuit diagram for the proposed power supply system

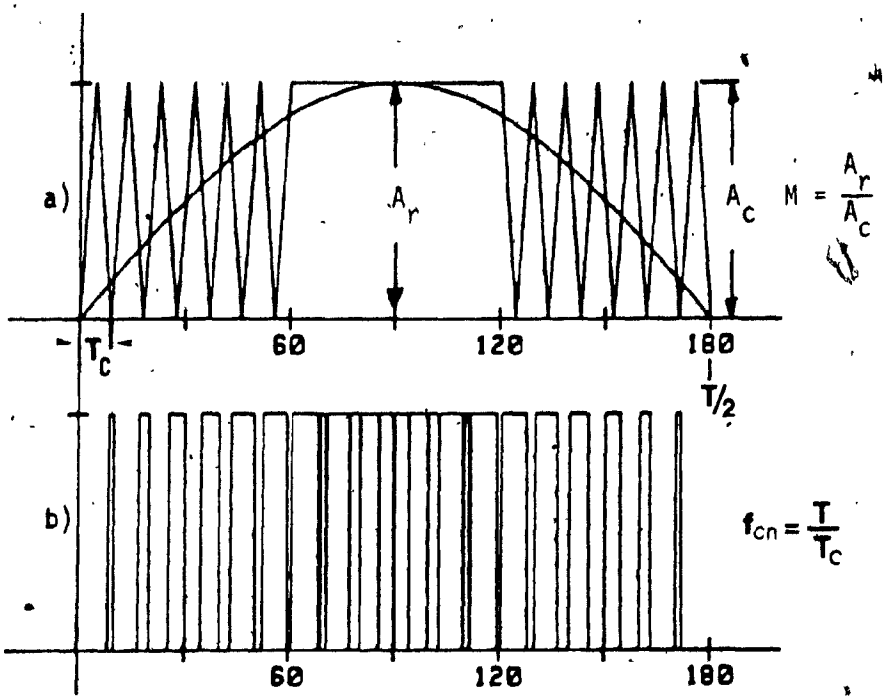


Fig.(5.2): a) Definition of the PWM technique employed with the proposed power supply system,
b) resulting switching pattern employed with PWM inverter and rectifier (first 180).

(CSR). Its main function is to maintain current continuity in the dc link, therefore acting as an input current source to the PWM inverter. The factors that determine the inductance value of CSR include; specified dc link current ripple factor and the switching frequencies of the PWM inverter and PWM rectifier.

The main system component is the current source inverter (CSI) which transforms the input dc link current into the three phase balanced ac output currents required by the load. To improve the performance characteristics of the CSI, the traditional six-step PWM scheme (see Fig.(3.3)) has been replaced with the advanced PWM method shown in Fig.(5.2). The resulting CSI structure yields input voltage and output current waveforms with drastically reduced content of low order harmonics (Figs.(5.3d),(5.3a),(5.4a),(5.4d)), respectively. These features, in turn, result in proportional size reductions for the inverter input and output filters (i.e. CSR and Cf respectively, Fig.(5.1)). Moreover, since the inverter line currents contain only high frequency harmonic components and since shunt filter capacitors (Cf) have been added (between CSI and load) the voltage stresses on the inverter components have been minimized.

Finally, the most novel feature with the proposed power supply is the shunt filter capacitors Cf. Although these components occupy the position of the familiar (with six-step CSI thyristor inverters) commutation capacitors, their function here is completely different. They act as by-pass paths for the high frequency line current components. Consequently, the load voltage and current waveforms are

practically sinusoidal. This feature in turn eliminates motor core heating associated with high frequency current harmonics, motor winding stresses associated with high frequency voltage harmonics, and torque pulsations associated with low frequency current harmonics.

5.3 PWM Rectifier-Inverter Transfer Function

Chapter 2 of this thesis has shown that CSI's and rectifiers have the same switch mode converter transfer function (if the same PWM control technique is used by both of them). A transfer function suitable for the CSI and rectifier of this power supply must have a number of special features, including:

i) the capability of eliminating any number of unwanted low order harmonics,

ii) performing the above with minimum switching,

iii) provide maximum possible rectifier output voltage and CSI output line currents, and

iv) provide smooth and continuous control of the rectifier output voltage and CSI output current while maintaining feature i).

A sample from a class of transfer functions that yield a good combination of the aforementioned features is shown in Fig.(5.2). The respective frequency spectra are shown in Tables (5.1) and (5.2). Features (ii) and (iii) can also be provided by other classes of PWM control schemes; in particular, fixed PWM patterns (see Fig.(3.4)) [24] [47]. However, these fixed PWM patterns produce transfer functions

that have two main disadvantages for this application. Firstly, as the number of the harmonics to be eliminated increases, the practical realization and implementation becomes very difficult. Secondly, the task of implementing feature (iv) (with fixed patterns) is quite difficult and complex [31]. Returning to the first class of transfer functions, Fig.(5.2), it is noted that the number of harmonics that can be eliminated increases as the normalized carrier frequency increases. This in turn implies smaller input-output filters. However, CSI and rectifier switching losses also increase with fcn. Therefore, realistic fcn values must be chosen as a compromise between size of filter components and converter losses.

Specifically, with fcn defined as;

$$f_{cn} = \frac{T}{T_c} \qquad \text{Fig. (5.2)}, \tag{5.1}$$

where:

$$\frac{T}{T_c} = 6(k+0.5), \quad k = 1,2,3.....$$

the following relations hold true:

$$\text{Number of pulses per cycle, } N_p = \left(\frac{4}{3}\right) f_{cn} - 4 \tag{5.2}$$

order of dominant harmonics

$$d_1 = f_{cn} - 2 \tag{5.3a}$$

$$d_2 = f_{cn} + 2 \tag{5.3b}$$

order of the equivalent dominant harmonic

$$d = \frac{d_1+d_2}{2} = f_{cn} \qquad (5.3c)$$

order of the lowest significant harmonic,

$$r = f_{cn} - 4 \qquad (5.4)$$

normalized chopping frequency per switch,

$$f_{sn} = \left(\frac{2}{3}\right) f_{cn} - 3 \qquad (5.5)$$

Therefore the per switch normalized chopping frequency required to eliminate up to the rth harmonic from the CSI output or rectifier input line currents is given by:

$$f_{sn} = \left(\frac{2}{3}\right)(r+4) - 3 \qquad (5.6)$$

where: $r = 6k - 1$, $k=1,2,3,.....$

Also, since for a given operating frequency fo the value of the output filter capacitors Cf is approximately inversely proportional to fcn, eqns. (5.3) will be useful in establishing a direct relation between fo, fcn and Cf values.

5.4 Rectifier-Inverter Analysis and Design

The rectifier and the inverter perform the ac-dc power conversion function, and therefore, the transfer function and the functional model developed in chapter 2 (Table (2.4)) are readily applicable. Moreover, the generalized waveforms of Fig.(2.6) are also applicable. The data obtained from the application of the model are essential in the design of the rectifier input ac filter, current source reactor, and CSI output Cf filter components.

5.4.1 CSI Computer Simulation

With the aim of testing the functional model developed in chapter 2 and to provide an accurate simulation of experimental results, the rectifier and CSI converter operation were simulated in a HP9836-DATA6000 system. The simulation was performed with the following assumptions:

i) rectifier input and CSI output ac voltages are balanced (the effects of unbalanced ac sources and loads are examined separately in this section)

ii) the dc link current employed in the computation of rectifier input and inverter output currents is ripple free,

iii) the rectifier and inverter switches are ideal (i.e. with Zero ON and Infinite OFF impedances and, Zero switching times.)

This set of assumptions is identical to the steady state assumptions of the steady state functional model of chapter 2

(Table(2.4)). The only exception is that the phase load voltages (CSI output side) are not assumed to be perfectly sinusoidal, however, this difference is not relevant because, as expected, the very small ripple content (in the phase voltages) has a negligible influence in the input CSI voltage. This can be concluded by comparing the simulated spectral content of the CSI input voltage (Fig.(5.4d)) against the spectra predicted by the functional model considering sinusoidal phase voltages (Fig.(2.6d)).

Generalized results regarding the frequency spectra of the current and voltage waveforms generated by the rectifier-CSI units are shown in Table(5.1) and Table(5.2). To be consistent, the per-unit basis adopted in previous chapters is preserved, therefore, the CSI input and rectifier output dc current is one pu. (The per-unit system is specified in Table (2.3)). Moreover, analysis spectra results obtained with the specific transfer function shown in Fig.(5.2) are presented in Fig's.(5.4a,b,c,d) for the waveforms displayed in Fig's.(5.3a,b,c,d).

Next, the effects of introducing some load and/or ac input voltage unbalance on respective circuit components are investigated as follows; since rectifier and CSI transfer functions are not affected by unbalanced loads and input voltage conditions, the quantities that become affected are the rectifier output, and the inverter reflected input voltage waveforms. In particular, voltage harmonics of the 2w, 4w, 8w,.... order begin to appear in respective voltage spectra. The first (i.e.2w) of these harmonics is of major concern because its low

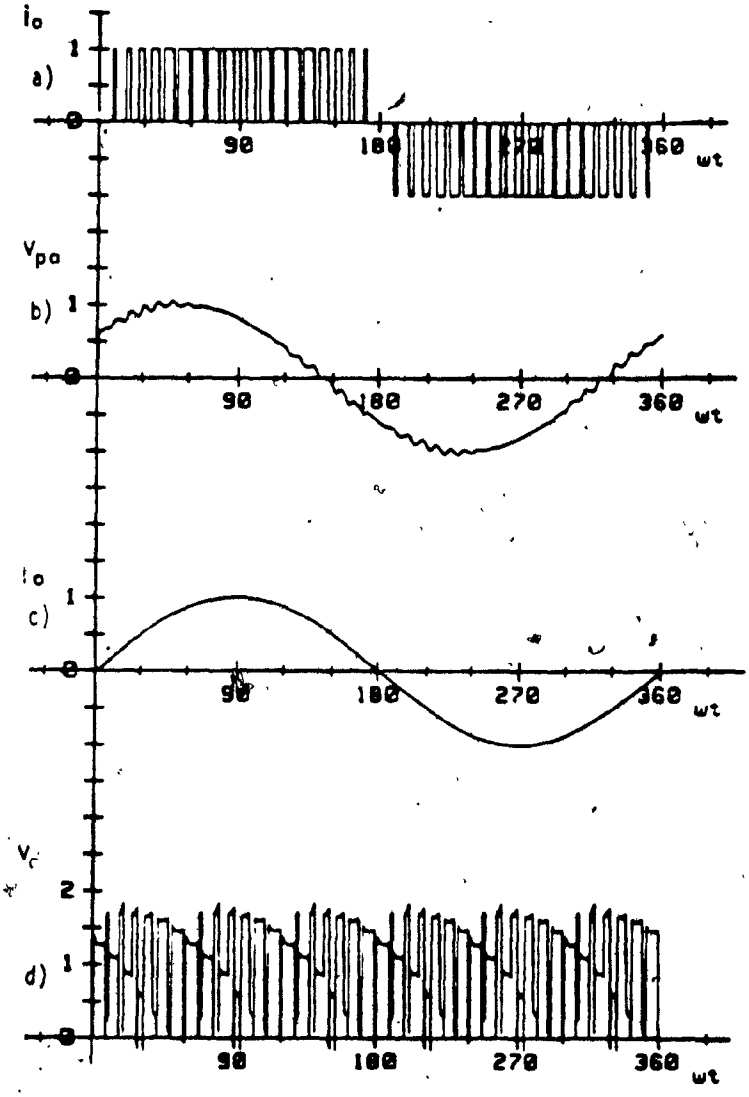


Fig.(5.3): CSI voltage and current waveforms (with load power factor 0.8 lagging):

a) line current, ia
b) output phase voltage, Vpa
c) load currents, io
d) input voltage, vd.

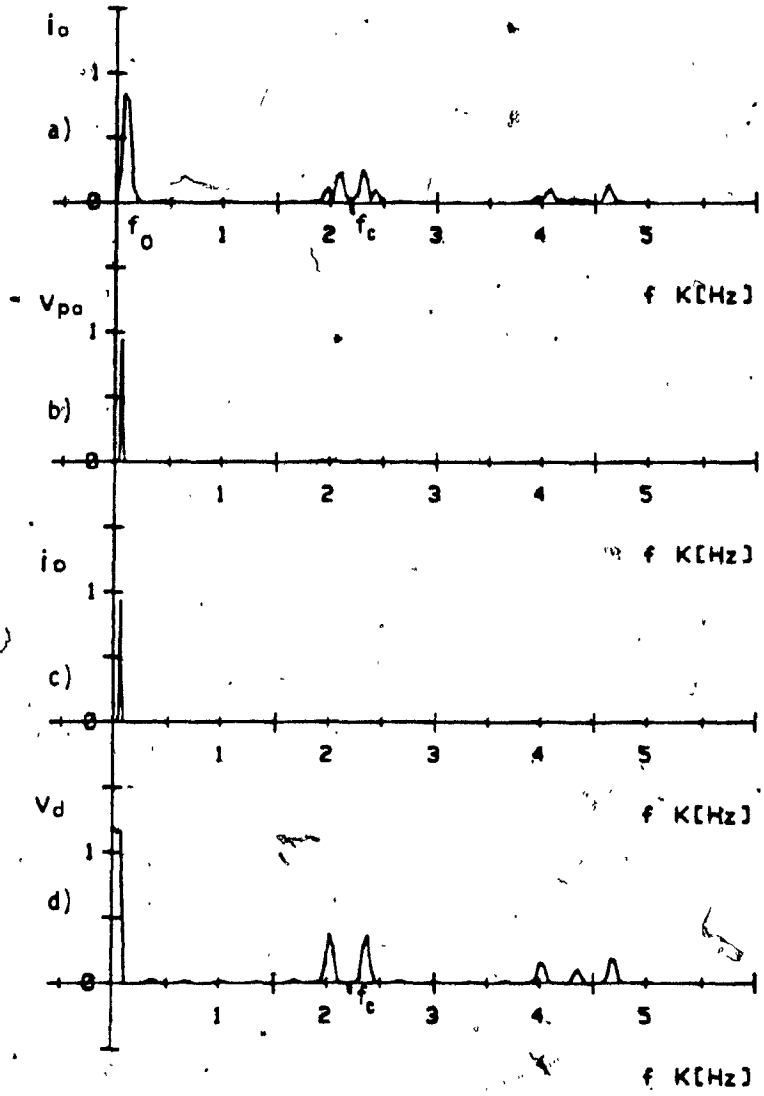


Fig.(5.4): Frequency spectra of CSI waveforms depicted in Fig.(5.3):

a) CSI line currents, ia
b) CSI output phase voltages, Vpa
c) CSI load currents, io
d) CSI input voltage, Vd.

frequency and relatively large amplitude can considerably increase the dc link ripple current. This in turn influences the size of the dc link reactor required to maintain the ripple current within acceptable limits. Furthermore, since the 2w harmonics result from interaction of only the fundamental switching function component, al cos(wt) (see eqn.(2.3)) with the respective rectifier input (or CSI output) phase voltage components (Vl cos(wt)), it follows that:

$$VH(2\omega) = a_1 \sin(\omega t)\, V_1 \sin(\omega t) + a_1 \sin(\omega t-120)\, V_1(1\pm\Delta)\sin(\omega t-120\pm\theta) + a_1 \sin(\omega t+120)\, V_1(1\pm\Delta)\sin(\omega t+120\pm\theta) \quad (5.7)$$

under worse case conditions:

$$\left|VH(2\omega)\right| = \frac{(a_1 V_1)}{2}\left[\left(1-\cos(\theta)+\sqrt{3}\sin(\theta)\right)^2+\Delta^2\left(\sqrt{3}\cos(\theta)-\sin(\theta)\right)^2\right]^{1/2} \quad (5.8)$$

where: Δ denotes magnitude unbalance, and

ϕ phase unbalance of respective phase quantities.

A family of normalized H(2w) design curves obtained from eqn.(5.8) are shown in in Fig.(5.5).

5.4.2 Semiconductor Switch Ratings

Per-unit switch ratings for the bridge configuration of the rectifier and the CSI are given in Table (2.5). These ratings are computed with reference to the per-unit system defined in section (2.6.2). In particular eqn.(2.37) and eqn.(2.38) can be used to compute the current and voltage ratings.

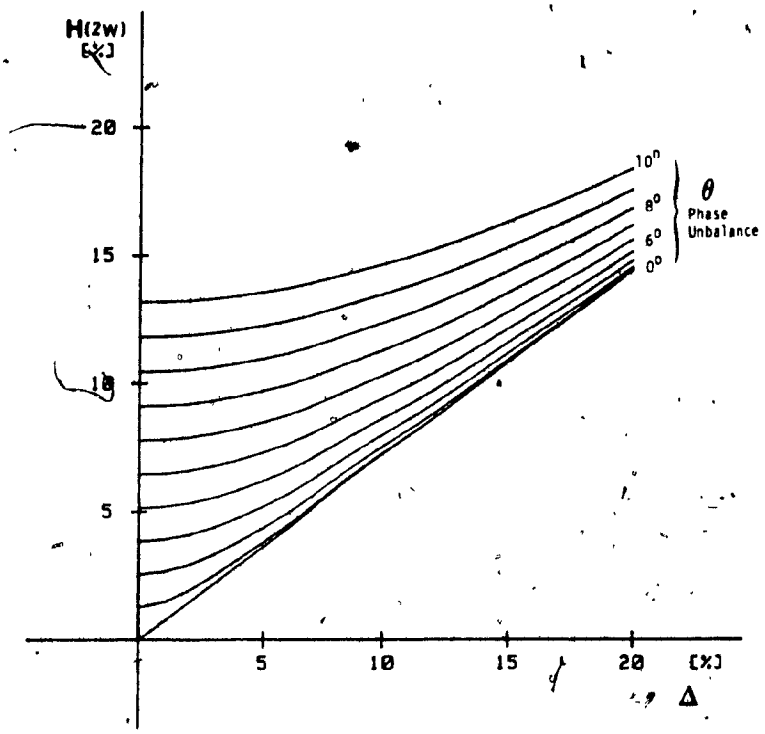


Fig.(5.5): Amplitude of second harmonic H(2w) of dc link voltage versus magnitude and phase unbalance of phase voltages.

Example: Consider a 3-ϕ power supply connected to 115V (phase) ac mains and supplying a 5KVA, 115V (phase) balanced ac load. The voltage and current ratings for the rectifier and CSI switching elements are as follows;

From section 2.6.2 the one per-unit voltage becomes, (with al=1 for modified SPWM),

$$1_{pu\ volutage} = \frac{(V_p)}{a_1} = \frac{(115\sqrt{2})}{1} = 162.63\ [V] \qquad (5.9a)$$

and the switch peak voltage (2.38) becomes;

$$V_{S\ peak} = (\sqrt{3})(162.63) = 282\ [V] \qquad (5.9b)$$

The rms per-phase output line current is given by,

$$i_{1\ rms} = (\frac{5000}{3})(\frac{1}{115}) = 14.54\ [A] \qquad (5.10)$$

The dc link current was chosen 1 pu. Therefore, the ac line current magnitude for the modified sine-PWM is also 1 pu.

$$1_{pu\ current} = (\sqrt{2})(14.54) = 20.56\ [A] \qquad (5.11)$$

Now using Table (2.5) or eqn.(2.37),

$$I_{S\ avg} = (\frac{1}{3})(20.56) = 6.85\ [A] \qquad (5.12a)$$

$$I_{S\ rms} = (\frac{1}{\sqrt{3}})(20.56) = 11.87\ [A] \qquad (5.12b)$$

$$I_{S\ peak} = (1)(20.56) = 20.56\ [A] \qquad (5.12c)$$

5.5 Analysis and Design of Passive System Components

The two major passive system components are the current source reactor (CSR) and CSI output filter capacitors Cf. These components are basically filters with the tasks of limiting the ripple of dc link and CSI load currents, respectively. Consequently, their analyses and design are drastically affected by the specific transfer functions employed with the rectifier and CSI units.

5.5.1 Load Filter Capacitors

Since the pulse width modulated CSI line currents contains only high frequency components, filter capacitors Cf are relatively small.

Proper Cf values should satisfy the following criteria;

i) they should be large enough to shunt-off all unwanted CSI line current harmonics, and

ii) they should be small enough to appear as high impedance to the fundamental component of the CSI line current.

To satisfy the first criterion, the impedance of Cf, Xcd, "seen" by the dominant line current harmonic must be much lower than 1 pu ohms (i.e. rated load impedance) specifically:

$$X_{cd} = \frac{1}{2\pi d\, f_{om} C_F} \ll 1 \text{ pu} \qquad (5.13)$$

where: d represents the order of the dominant harmonic of the CSI line current, and

fom the maximum expected CSI output frequency.

To satisfy the second criterion, the impedance of Cf, Xcl, "seen" by the fundamental component of the line current must be larger than 1 pu ohms. Specifically;

$$X_{cl} = \frac{1}{2\pi f_{om} C_F} > 1 \text{ pu} \qquad (5.14)$$

Furthermore, Pig.(5.4) and Table (5.1) show that with modulation index M=1 the CSI line current contains two dominant harmonics, Id1 and Id2, of amplitudes Id1 = Id2 = 0.26 pu (see also Fig.(2.6)). For analysis purposes Id1 and Id2 can be replaced by a single dominant harmonic Id (eqn.(5.3c)) such that;

$$d = \frac{(d_1+d_2)}{2} = f_{cn}$$

then;

$$I_d = (I_{d1} + I_{d2}) = (0.26)\sqrt{2} = 0.38 \text{ pu} \qquad (5.15)$$

Now, if the respective phase voltage harmonic magnitude Vd is to be kept below 5 % (i.e. 0.05 pu), then;

$$V_d = I_d X_{cd} < 0.05$$

or

SPECTRUM VALID FOR: – CR OUTPUT VOLTAGE – CSI INPUT VOLTAGE		PER UNIT FREQUENCY
SPWM [%]	MSPWM [%]	
100.0	100.0	0
0.0	0.9	$f_{cn} - 9$
30.0	14.1	$f_{cn} - 3$
30.0	14.1	$f_{cn} + 3$
0.0	0.9	$f_{cn} + 9$

Table (5.2): Frequency spectra of dc link (controlled rectifier output and CSI input) voltages MSPWM control technique (M=1, Ø=0).

PER UNIT FREQUENCY	SPECTRUM VALID FOR: ± CR INPUT CURRENTS — CSI OUTPUT CURRENTS	
	SPWM [%]	MSPWM [%]
1	100.0	100.0
$f_{cn} - 4$	0.0	11.4
$f_{cn} - 2$	32.2	25.6
$f_{cn} + 2$	32.2	25.6
$f_{cn} + 4$	0.0	11.4

Table (5.1): Frequency spectra of PWM controlled rectifier input and CSI inverter output line currents MSPWM control technique (M=1; Ø=0).

$$X_{cd} = \frac{1}{2\pi d\ f_{om} C_F} \geq \frac{0.05}{0.38} = 0.13 \text{ pu} \qquad (5.16)$$

From similar arguments it can be shown that criterion (ii) is satisfied if;

$$X_{cl} = \frac{1}{2\pi d\ f_{om} C_F} \geq 5 \text{ pu} \qquad (5.17)$$

The ratio of relations (5.16) and (5.17) yields:

$$\frac{X_{cl}}{X_{cd}} = d \geq 39 \qquad (5.18)$$

and by employing (5.3c) and (5.5);

$$f_{cn} = d \geq 39 \qquad (5.19a)$$

and,

$$f_{sn} = \geq \left(\frac{2}{3}\right)(39) - \geq 23 \qquad (5.19b)$$

where: fcn, the normalized carrier frequency as defined in (5.1).

fsn, the per switch normalized chopping frequency as defined in (5.5).

Also, since the maximum absolute values of carrier and semiconductor chopping frequency fc and fs are given by fc = fcn·fo and fs = fsn·fo, it follows that,

$$f_c > 39\ f_{om}\ [\text{Hz}] \tag{5.20}$$

and

$$f_s > f_{om}\ \frac{[\text{chops}]}{[\text{switch-second}]} \tag{5.21}$$

Finally, from (5.15) and (5.19a) the delta connected Cf value Fig.(5.1) is given by:

$$C_F = \frac{1}{(3)(X_{cd})(f_{cn})}\ \text{pu}\ [\text{F}] \tag{5.22a}$$

where: 2 fom is taken as 1 pu angular frequency, and by using (5.16) and (5.19a) with (5.22a)

$$C_F > \frac{1}{(3)(0.13)(39)} > 0.066\ \text{pu}\ [\text{F}] \tag{5.22b}$$

Example: Continuing with the example presented earlier in this chapter, it is also assumed that the peak CSI output frequency fo is 90 [Hz] and that the tolerable peak dominant harmonic ripple load voltage is 0.05 pu.

From (5.21)

$$f_S = 23\ f_{om} = (23)(90) = 2070\ [\text{chops/switch-second}] \tag{5.23}$$

Now, at fo = 90 [Hz] the load 1 pu impedance is;

$$Z = \frac{162.63[\text{V}]}{20.51[\text{A}]} = 7.935\ [\text{ohm}] \tag{5.24}$$

then,

$$1_{pu\ capacitance} = \frac{1}{2\pi f_{om}^2} = 222.8\ [F] \qquad (5.25)$$

And from (5.22b) and (5.25) the value of the delta connected line capacitors are

$$C_F = (0.066)(222.8) = 15\ [\mu F] \qquad (5.26)$$

5.5.2 Current Source Reactor (CSR).

The CSR is connected between the rectifier and the CSI. Its task is to ensure current continuity in the dc link reducing the ripple, caused by the dominant harmonics Vdr and Vdi of the rectifier output and CSI input voltages. By assuming the same normalized carrier frequencies fcn (5>1) for both rectifier and CSI, the order of Vdr and Vdi harmonics become the same. Moreover, Table (5.2) and Fig.(5.4d) show that there are two Vdr (and Vdi) harmonics whose respective orders are:

$$d_{d1} = f_{cn} - 3 \qquad (5.27a)$$

$$d_{d2} = f_{cn} + 3 \qquad (5.27b)$$

and whose peak amplitudes, at maximum dc link voltage (i.e. M=1), are

the same and given by (Table(5.2));

$$V_{dr} = V_{di} = 0.22 \text{ pu } [V] \tag{5.28}$$

Also, since the fcn 3 values in (5.27) are much larger than one, the two Vdr (and Vdi) can be replaced by a single equivalent dominant harmonic of peak amplitude;

$$V_{de} = 2 V_{dr} = 0.44 \text{ pu } [V] \tag{5.29}$$

and of order

$$d_d = \frac{d_{d1} + d_{d2}}{2} = f_{cn} \tag{5.30}$$

Now, the dc link ripple current ΔI is maximum when the rectifier output and CSI input dominant voltages harmonics are out of phase by 180. Therefore;

$$\Delta I_{i,max} = \frac{2 V_{de}}{2\pi f_{om} f_{cn} L_{CSR}} = \frac{0.88}{f_{cn} L_{CSR}} \text{ pu } [A] \tag{5.31}$$

where Lcsr is the inductance value of CSR reactor.

Finally, solving for Lcsr;

$$L_{CSR} = \frac{0.88}{f_{cn} \Delta I_{max}} \text{ pu } [H] \tag{5.32}$$

Example: Continuing with the example discussed previously in this chapter, it is furthermore assumed that, ΔI max = 0.1 pu (i.e.

10 % of rated dc link current).

From (5.24);

$$l_{\text{pu inductance}} = \frac{Z}{2\pi f_{om}} = \frac{7.935}{2\pi\ 90} = 14\ [\text{mH}] \qquad (5.33)$$

From (5.33) and (5.19a)

$$L_{CSR} = \frac{0.88}{(39)(0.1)} = 0.23\ \text{pu}\ [\text{H}] \qquad (5.34)$$

therefore, using (5.33) the actual value of CSR inductance is;

$$L_{CSR} = (0.23)(14) = 3.2\ [\text{mH}] \qquad (5.35)$$

5.6 Multiple CSI Operation from Single Current Source

When a comparison is made between current and voltage source ac power supplies, it is frequently mentioned that the former do not allow the simultaneous operation of more than one CSI load units from a common dc link. From the theoretical point of view, this statement is false since voltage and current sources are dual. Duality in this case implies that if voltage sources allow the parallel connection of more than one inverter, current sources should, and do, allow the series connection of more than one inverter. The problem with the classical six-step CSI has been that the power can be controlled only through the respective front end rectifier, which makes individual inverter control impossible. With the proposed scheme, the series operation becomes feasible by controlling CSI output power individually, through modulation factor control, consequently, eliminating the disadvantage.

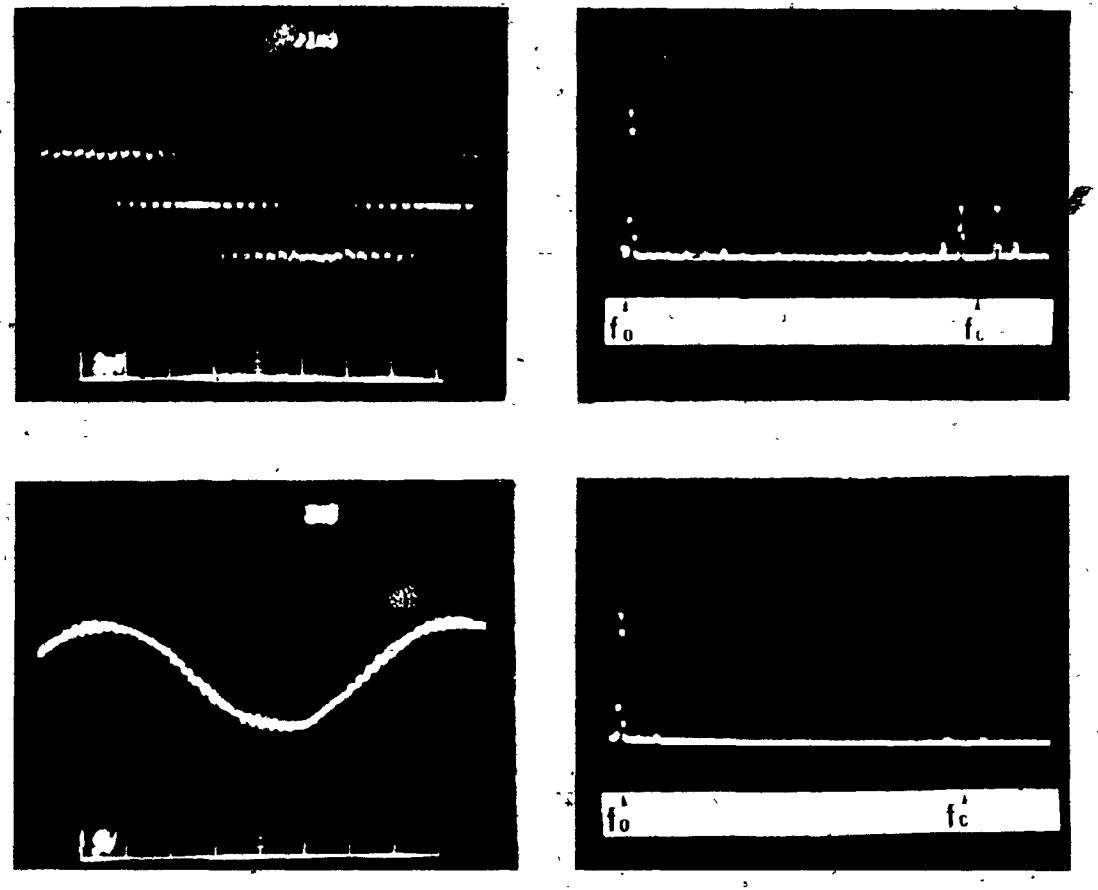
Furthermore, the duality principle is also applicable to the voltage and current ratings of the respective front end rectifiers. If switching components of rectifiers supplying k number of voltage source inverters are rated at 1 pu voltage and at k pu current, then respective components of rectifiers supplying k CSI's should be rated at k pu voltage and at 1 pu current. It is worth mentioning that the inverter ratings for both, the parallel and the series connection, remain unchanged. However it is true, regarding the rectifier ratings, that state of the art technology and practical experience favor the use of low-voltage high-current gate turn-off devices, therefore the number of CSI-load units that can be connected in series is limited [21].

5.7 Experimental Results

To demonstrate the feasibility of the proposed current source power conversion scheme, an experimental 2KVA unit was implemented. Results obtained with this breadboard unit are depicted in Fig.(5.6).

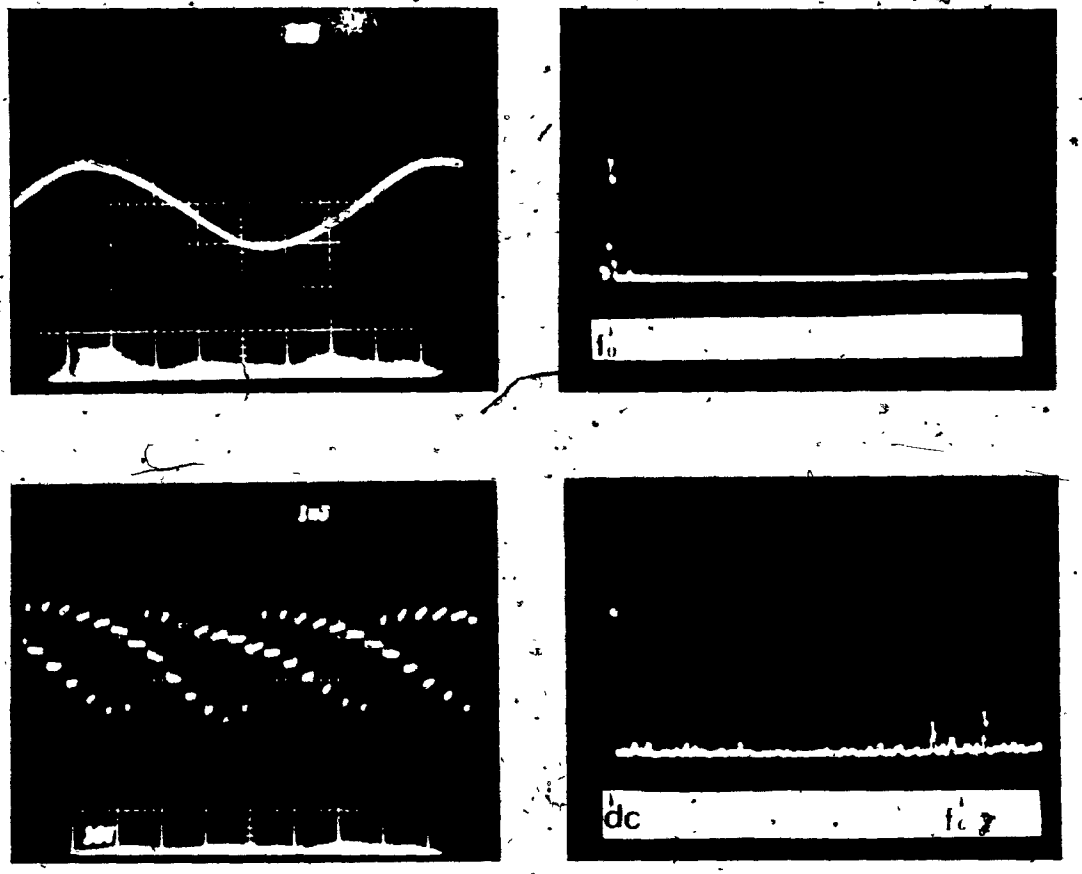
Figs.(5.6a) and (5.6c) illustrate the CSI line and load current and their respective spectra (corresponding computer simulated results are depicted in Figs.(5.3a),(5.4a) and (5.3c),(5.4c) respectively; also see Table(5.1)).

The load voltage and CSI input voltage with respective spectra are depicted in Figs.(5.6b) and (5.6d). (Figs.(5.3b),(5.4b) and (5.3d),(5.4d) show respective computer simulated results; also see Table(5.2)). The close agreement between simulated and experimental results [21] proves the validity of the analysis and the feasibility of the proposed power supply.)



a) Inverter line current ia waveform (5 [A/div]) and ia frequency spectrum (fc=2,340 [Hz] i.e. fcn=39).

b) Phase load voltage Vpa waveform (100 [V/div]) and Vpa frequency spectrum (fc=2,340 [Hz] i.e. fcn=39).



c) Output load current io waveform (5 [A/div]) and io frequency spectrum (fc=2,340 [Hz] i.e. fcn=39).

d) Inverter input voltage Vd waveform (100 [V/div] and Vd frequency spectrum (fc=2,340 [Hz] i.e. fcn=39).

Fig.(5.6): Experimental CSI waveforms and respective spectra (modulation factor M = 1, fo=60 [Hz], power factor 0.8 lagging).

5.8 CONCLUSIONS

An improved power conversion scheme for variable frequency inductive type of loads has been presented in this chapter. To increase system reliability and allow bilateral power flow this scheme employs current instead of voltage source inverters. Moreover, by utilizing advanced PWM techniques for both the front end rectifier and the current source inverter, the subject scheme therefore:

a) generates sinusoidal input and output currents and voltages at practical converter switching frequencies,

b) minimizes the size of passive system components such as input-output filters and current source reactors,

c) allows for faster system response to transients because of the smaller CSR,

d) allows the series operation of more than one CSI-load units connected in a common dc link.

Finally, the feasibility of the proposed scheme has been tested and verified on a 2 KVA laboratory unit.

CHAPTER 6

SUMMARY AND CONCLUSIONS

6.1 Summary and Conclusions

A novel analysis approach for switch mode converters has been presented in Chapter 2 of this thesis. The analysis is based on the definition of a transfer function for switch mode converters. An important advantage of this approach is that it makes possible the simultaneous analyses of groups of converters that share conversion functions (e.g. VSI, CSI and CR). Furthermore, with this approach the analysis of systems with multiple power conversion stages becomes modular and simpler. This concept enables to decompose the synthesis of power converter systems into steps, namely: the derivation of the transfer function, the synthesis of converter topologies, and the required gating strategy. In the context of this thesis, this approach provides a unified analysis method suitable for the study and evaluation of the power supply topologies proposed for fixed and variable frequency of operation.

Specifically, Chapter 2 identifies a common bilateral transfer function for the ac/dc group of converters (i.e. VSI, CSI and CR), which is, by large, the power conversion type most often required in today's practical applications. With the use of this transfer function and a set of simplifying assumptions for steady state, normalized waveforms for VSI, CSI, and CR have been identified. In particular,

waveforms which simultaneously represent the output line voltages of a VSI, the output line currents of a CSI, and the input line currents of a CR have been established. Further, waveforms which simultaneously represent the input current of a VSI, the input voltage of a CSI, and the output voltage of a CR have been also established.

To process the proposed transfer function relationships, Chapter 2 introduces a time domain approach as an alternative to the more complex Fourier series based approach. Respective comparison between the two approaches results in the following advantages for the proposed time domain approach:

i) it requires extremely simple mathematical operations, it is easier to program, and the computer processing time is much smaller,

ii) it is largely more accurate, particularly in describing PWM time domain waveforms,

iii) it can be used directly for transient analysis.

Finally, Chapter 2 provides generalized design data for VSI, CSI and CR 3Φ-bridge converters. The data include normalized switch ratings, semiconductor switching frequencies, and generalized input/output frequency spectra for the SPWM and MSPWM techniques.

A novel computer aided design (CAD) approach for switch mode converters has been presented in Chapter 3. The subject CAD can be regarded as a natural complement to the unified analysis method of Chapter 2. In particular, it is shown that the generalized switch

ratings of Chapter 2 constitute necessary but not sufficient design data for converters that utilize switches implemented with multiple semiconductors. The basic concept of the approach is to compute the exact normalized ratings of the semiconductors required by specific converter topologies. In particular, the CAD of voltage source inverters has been fully developed in Chapter 3, showing that a severe under-utilization of the converter components (introduced by the contemporary design approach) has been overcome with CAD. Specifically, per-unit VSI component ratings curves are provided for three PWM techniques, namely, sine PWM, six-step PWM and, a distortion factor optimized PWM pattern proposed in Chapter 4.

Finally, with the use of CAD in VSI's, it is concluded that at least a 45% improvement in component utilization can be accomplished for reasonably wide operational ranges (i.e. modulation and power factor ranges). Therefore, for reduced VSI operational ranges, the improvement that can be accomplished should be even greater. In practical applications these design curves can be used advantageously in the design of medium to large power VSI and in the design of integrated ("power chips") VSI units. Selected CAD predicted results have been experimentally verified.

Chapter 4 presents a critical evaluation of traditional power conversion practices in uninterruptible power supply (UPS) systems, showing that some popular power conversion methods lead to severe under-utilization of the dc bus and deterioration of the effective load

power factor. To ameliorate this situation a power supply topology using a regulated dc bus is presented. Two different operational strategies (PCU and CCU) have been fully described. Moreover, to further enhance the utilization of the dc bus, an optimized PWM technique has been proposed.

It is concluded that at least a 65% improvement in the use of inverter components and a considerable reduction in the size of the required input/output filters has been accomplished with the CCU strategy. Also shown is that the proposed topologies do not compromise the system complexity and/or cost. Predicted results have been experimentally verified on a two KVA laboratory unit. It is important to mention that the improvements obtained in Chapter 4 have been produced without the use of the VSI-CAD proposed in Chapter 3. Therefore, the VSI component utilization of UPS systems designed with the topologies of Chapter 4 can be boosted even further with the VSI-CAD of Chapter 3.

Chapter 5 presents a novel power conversion topology for variable frequency inductive type of loads. Current source inverters have been selected, rather than voltage source inverters, to increase system reliability and to allow bilateral power flow. Moreover, by utilizing advanced PWM techniques for both, the front end rectifier and the current source inverter, the subject scheme:

i) generates sinusoidal input-output currents and voltages at practical converter switching frequencies,

ii) minimizes the size of passive components such as input/output filters and current source reactors,

iii) allows for faster system response to transients because of the smaller current source reactor, and

iv) allows the series operation of more than one CSI-load units connected to a common dc link.

The analysis and design of this power supply has been greatly simplified with the aid of the concepts developed in Chapter 2. Specifically, the generalized steady state waveforms proposed in Chapter 2 are directly applicable to the two power conversion stages utilized by this power supply (i.e. controlled rectification and current source inversion). Finally, the analysis, design and feasibility of the proposed scheme have been tested and verified on a 2 KVA laboratory unit.

6.2 Suggestions for Further Work

The functional transfer function analysis approach for switch mode converters presented in this thesis is a general concept. However, Chapter 2 has introduced explicit relationships that cover only the ac/dc or dc/ac power conversion functions. Further work could be done to include the dc/dc and ac/ac power conversion functions. In particular, the ac/ac conversion function, which is of expanding interest, can be regarded as an ac/dc/dc/ac composite conversion

function (imaginary dc link). Therefore, the equivalent transfer function should be a composition of the unified bilateral transfer function H(t) defined in Chapter 2. In general, and regardless of particular applications, a functional approach can be followed to define a sequence of research steps:

i) the search for an improved transfer function (or composition of transfer functions) to perform a required power conversion,

ii) the study and selection of circuit topologies (current and/or voltage source converter topologies) to realize such transfer function (or composition of transfer functions).

iii) the determination of gating strategies to control the topologies specified in ii) in order to perform the transfer function specified in i).

iv) the development of generalized CAD (computer aided design) data for the topologies determined in iii),

v) the study, selection, and design of filter configurations required by the switch mode conversion system.

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APPENDIX 1

THE COMPUTER PROGRAMS FOR COMPUTING THE TRANSFER FUNCTIONS AND FREQUENCY SPECTRA FOR SINE PWM AND MODIFIED SINE PWM CONTROL SCHEMES

```
10        This Subprogram Computes the Intersection Points and
20        the Spectrum  for the  Sinusoidal PWM for Differents
30        Modulation Factors (MF).
40
50
60      PRINTER IS 1
70      REAL Degree(50),Vha(51)
80      Mf=1                              Default Value
90      Nf=21                             Default Value
100     INPUT "MODULATION FACTOR",Mf
110     INPUT "NORMALIZED CARRIER FREQUENCY",Nf
120     Spwm(Mf,Nf,Degree(*),Vha(*))
130     END
140     SUB Spwm(Mf,Nf,Degree(*),Vha(*))
150         RAD
160         DIM A$[45]
170         ALLOCATE REAL T(43)
180         Es=1                      Normalized Input dc
190         Tol=.0005
200         Np=2*Nf+1
210         Sf=2*Nf
220         Nn=Np-1
230         FOR N=1 TO Nn
240             Xold=T(N)+PI/180
250               using Newton Algorithm
260             FOR K=1 TO 200
270                 F=Mf*(SIN(Xold))-((-1)^N)*(Sf*Xold/PI-2*N)
280                 G=Mf*(COS(Xold))-((-1)^N)*(Sf/PI)
290                 Xnew=Xold-F/G
300                 Delta=ABS((Xnew-Xold)/Xnew)
310                 IF Delta Tol THEN GOTO 340
320                 Xold=Xnew
330             NEXT K
340             T(N+1)=Xnew
```

```
350             Degree(N+1)=T(N+1)*180/PI
360         NEXT N
370         PRINT "PHASE INTERSECTION ANGLES OF SPWM (see Fig.(4.3))"
380         PRINT "Modulation Factor = 1,  Normalized Carrier = 21",""
390         FOR I=1 TO Np
400             PRINT USING """SPWM DEGREE (",2D,")=",5D.3D";I,Degree(I)
410         NEXT I
420         I=0
430         PRINT "LINE TO LINE SPECTRUM (see Fig.(2.5.2))"
440         PRINT "Modulation Factor = 1, Normalized Carrier = 21";""
450         FOR L=1 TO 49 STEP 2 HARMONIC SPECTRUM FOR SPWM
460             IF L MOD 3=0 THEN L=L+2
470             B=0
480             FOR M=1 TO Nn
490                 Am=(-1)^M
500                 P=L*T(M+1)
510                 Q=L*T(M)
520                 B=B-(Am/L)*(COS(P)-COS(Q))
530             NEXT M
540             Vha(L)=Es*B/PI/Mf/2*SQR(3)
550             Per=Vha(L)*100/Vha(1)*Mf
560             A$="""SPWM HARMONIC (",DD,") = ",3D.4D,7D.3D,"
570             PRINT USING A$;L,Vha(L)*Mf,ABS(Per)
580         NEXT L
590         DEALLOCATE T(*)
600     SUBEND
```

PHASE INTERSECTION ANGLES OF SPWM (see Fig.(4.3))

Modulation Factor = 1, Normalized Carrier = 21

SPWM DEGREE (1)=	0.000
SPWM DEGREE (2)=	7.977
SPWM DEGREE (3)=	18.503
SPWM DEGREE (4)=	23.973
SPWM DEGREE (5)=	36.856
SPWM DEGREE (6)=	40.097
SPWM DEGREE (7)=	54.936
SPWM DEGREE (8)=	56.429
SPWM DEGREE (9)=	72.662
SPWM DEGREE (10)=	73.043
SPWM DEGREE (11)=	90.000
SPWM DEGREE (12)=	90.000
SPWM DEGREE (13)=	106.957
SPWM DEGREE (14)=	107.338
SPWM DEGREE (15)=	123.571
SPWM DEGREE (16)=	125.064
SPWM DEGREE (17)=	139.903
SPWM DEGREE (18)=	143.144
SPWM DEGREE (19)=	156.027
SPWM DEGREE (20)=	161.497
SPWM DEGREE (21)=	172.023
SPWM DEGREE (22)=	180.000
SPWM DEGREE (23)=	187.977
SPWM DEGREE (24)=	198.503
SPWM DEGREE (25)=	203.973
SPWM DEGREE (26)=	216.856
SPWM DEGREE (27)=	220.097
SPWM DEGREE (28)=	234.937
SPWM DEGREE (29)=	236.429
SPWM DEGREE (30)=	252.662

SPWM DEGREE (31)= 253.043
SPWM DEGREE (32)= 270.000
SPWM DEGREE (33)= 270.000
SPWM DEGREE (34)= 286.957
SPWM DEGREE (35)= 287.338
SPWM DEGREE (36)= 303.571
SPWM DEGREE (37)= 305.064
SPWM DEGREE (38)= 319.903
SPWM DEGREE (39)= 323.144
SPWM DEGREE (40)= 336.027
SPWM DEGREE (41)= 341.497
SPWM DEGREE (42)= 352.023
SPWM DEGREE (43)= 360.000

LINE TO LINE SPECTRUM (see Fig.(2.5.2))
Modulation Factor = 1, Normalized Carrier = 21

SPWM HARMONIC (1) =	.8660	100.000
SPWM HARMONIC (5) =	-0.0000	0.000
SPWM HARMONIC (7) =	0.0000	0.000
SPWM HARMONIC (11) =	-0.0000	0.000
SPWM HARMONIC (13) =	-0.0000	0.000
SPWM HARMONIC (17) =	-.0154	1.782
SPWM HARMONIC (19) =	-.2753	31.793
SPWM HARMONIC (23) =	-.2753	31.793
SPWM HARMONIC (25) =	-.0154	1.782
SPWM HARMONIC (29) =	-0.0000	0.000
SPWM HARMONIC (31) =	-0.0000	0.000
SPWM HARMONIC (35) =	-.0019	.218
SPWM HARMONIC (37) =	-.0287	3.319
SPWM HARMONIC (41) =	-.1569	18.119
SPWM HARMONIC (43) =	.1569	18.119
SPWM HARMONIC (47) =	.0287	3.319
SPWM HARMONIC (49) =	.0019	.218

```
10          This Program Computes the Intersection Points
20          and the Spectrum for the Modified Sine PWM.
30
40
50      REAL I1(101),T(48)
60      INPUT "Select Modulation Factor",Mf
70      INPUT "Select Carrier Frequency",Cf
80      N=(Cf-3)/6
90      Japanese(N,Mf,T(*),Sav)
100     Spectra(N,T(*),I1(*))
110     END
120     SUB Japanese(N,Mf,T(*),Sav)
130          FOR I=1 TO 2*N
140               IF (-1)↑ 0 THEN J=J+1
150       SECANT METHOD FOR THE SOLUTION
160       F(X)=SIN(X)-Y(X)
170       INITIAL APPROXIMATIONS
180               P0=0
190               P1=60
200               N0=100  MAX. NUMBER OF ITERATIONS
210               Tol=.0001
220               K=2
230               DEG
240               Function(N,Mf,I,J,P0,Q)
250               Q0=Q
260               Function(N,Mf,I,J,P1,Q)
270               Q1=Q
280               P=P1-Q1*(P1-P0)/(Q1-Q0)
290               IF K N0 AND ABS(P-P1) Tol THEN
300                    S=S+1
310                    T(S)=P
320                    GOTO Fin
330               ELSE
340                    K=K+1
```

```
350                     P0=P1
360                     Q0=Q1
370                     P1=P
380                     Function(N,Mf,I,J,P,Q)
390                     Q1=Q
400                     GOTO 280
410                 END IF
420 Fin:
430             NEXT I
440             ALLOCATE Six(24),Degree(50)
450             FOR I=1 TO 2*N
460                 Six(I)=-T(2*N+1-I)+120
470             NEXT I
480             K=0
490             FOR I=2*N+1 TO 4*N
500                 IF (-1)^ 0 THEN K=K+1
510                 B=K/2-K DIV 2
520                 IF B .001 THEN
530                     Jj=Jj+1
540                     T(I)=Six(Jj)
550                 ELSE
560                     Gg=Gg+1
570                     T(I)=T(Gg)+60
580                 END IF
590             NEXT I
600             PRINT "LINE INTERSECTION ANGLES OF MSPWM (see Fig.(5.2))"
610             PRINT "Modulation Factor = 1, Normalized Carrier = 21","

620             FOR I=1 TO 4*N
630                 Degree(I)=T(I)*180/PI
640                 PRINT USING """MSPWM DEGREE (",2D,")"",5D.3D";I,T(I)
650             NEXT I
660             DEALLOCATE Six(*)
670         SUBEND
```

```
680     SUB Function(N,Mf,I,J,X,Y)
690         DEG
700         Y=Mf*SIN(X)-(((-1) I)*((2*N+1)/60)*X+((-1) (I+1))*2*J)
710     SUBEND
720     SUB Spectra(N,T(*),I1(*))
730         DEG
740         DIM A$[45]
750         PAUSE
760         PRINT "LINE TO LINE SPECTRUM (see Fig.(2.6.2))"
770         PRINT "Modulation Factor = 1, Normalized Carrier = 21","
780         A$="""MSPWM HARMONIC (",DD,") =",3D.4D,7D.3D,"
790         FOR I=1 TO 33 STEP 2
800             Bt=0
810             IF (I) MOD 3=0 THEN I=I+2
820             FOR J=2 TO 4*N STEP 2
830                 Pt=I*T(J)
840                 Qt=I*T(J-1)
850                 Dmt=(1/I)*(COS(Pt)-COS(Qt))
860                 Bt=Bt-Dmt
870             NEXT J
880             I1(I)=4.*Bt/PI
890             Per=I1(I)*100/I1(1)
900             PRINT USING A$;I,I1(I),ABS(Per)
910         NEXT I
920     SUBEND
```

LINE INTERSECTION ANGLES OF MSPWM (see Fig.(5.2))
Modulation Factor = 1, Normalized Carrier = 21

MSPWM DEGREE (1)	14.934
MSPWM DEGREE (2)	20.087
MSPWM DEGREE (3)	30.000
MSPWM DEGREE (4)	39.769
MSPWM DEGREE (5)	45.333
MSPWM DEGREE (6)	58.757
MSPWM DEGREE (7)	61.243
MSPWM DEGREE (8)	74.667
MSPWM DEGREE (9)	74.934
MSPWM DEGREE (10)	80.087
MSPWM DEGREE (11)	80.231
MSPWM DEGREE (12)	90.000

LINE TO LINE SPECTRUM (see Fig.(2.6.2))
Modulation Factor = 1, Normalized Carrier = 21

MSPWM HARMONIC (1) =	.9968	100.000
MSPWM HARMONIC (5) =	.0034	.337
MSPWM HARMONIC (7) =	-.0036	.358
MSPWM HARMONIC (11) =	.0048	.483
MSPWM HARMONIC (13) =	-.0083	.835
MSPWM HARMONIC (17) =	-.1120	11.240
MSPWM HARMONIC (19) =	-.2590	25.981
MSPWM HARMONIC (23) =	.2596	26.040
MSPWM HARMONIC (25) =	.1108	11.113
MSPWM HARMONIC (29) =	.0120	1.208
MSPWM HARMONIC (31) =	-.0138	1.389
MSPWM HARMONIC (35) =	-.0521	5.226

APPENDIX 2

THE COMPUTER PROGRAM FOR TRANSIENT ANALYSIS OF A VSI UNDER STEP MODULATION CHANGES

```
10 Uuu1=TIMEDATE
20 DATA .5,15,1
30 READ Mf,Nf,Np
40 INTEGER Hsp(720),Hs(720),Hf(720)
50 REAL Degree(100),X(2,1440)
60 Spwm(Mf,Nf,Degree(*))
70 T_f(Np,Degree(*),Hf(*))
80 DISP "ENTER THE NEW MODULATION FACTOR AND THE # OF TRIANGLES"
90 INPUT Mfp,Nfp
100 Mfp=1.
110 Nfp=15
120 Spwm(Mfp,Nfp,Degree(*))
130 T_f(Np,Degree(*),Hs(*))
140 DISP "ENTER THE PERTURBATION ANGLE"
150 INPUT "Pa",Pa
160 DISP ""
170 Pa=120
180 Pa=Pa*2
190 Mix(Pa,Np,Hf(*),Hs(*),Hsp(*))
200 Uuu2=TIMEDATE
210 PRINT USING """PWM SCHEME COMPUTATION TIME"",3D.2D";Uuu2-Uuu1
220       PER UNIT DATA OF ORDER 3 LOAD-FILTER.
230 MAT Hf= Hf*(.5)
240 MAT Hs= Hs*(.5)
250 MAT Hsp= Hsp*(.5)
260  GOTO Graph
270 DATA 60,.20,.3,2,1
280 READ F_o,L_f,L_1,C,R
290 K1=2*PI*F_o/L_f
300 K2=C*2*F_o*PI
310 K3=2*PI*F_o/L_1
320 T=1/(F_o*720/Np)
330 Runge:
340 Runge(T,Np,K1,K2,K3,R,X(*),Hf(*),Hsp(*),Hs(*))
350 Uuu3=TIMEDATE
360 PRINT USING """RUNGE-KUTTA PROCESSING TIME"",3D.2D";Uuu3-Uuu2
370 PRINT USING """PROCESSING TIME WAS:"",3D.2D";Uuu3-Uuu1
380 ALPHA OFF
390 Again:
400 GINIT
410 GRAPHICS ON
420 ON KEY 0 LABEL "PLOTTER" GOTO Plo
430 ON KEY 2 LABEL "SCREEN" GOTO Scr
440 ON KEY 4 LABEL "EXIT" GOTO Exi
450 ON KEY 7 LABEL "DATA6000" GOTO Dta6
460 Spin:GOTO Spin
470 Plo:PLOTTER IS 705,"HPGL"
480 OUTPUT 705;"VS5"
490 GOTO Graph
500 Scr:PLOTTER IS 3,"INTERNAL"
```

```
510 Graph:
520 OFF KEY
530 GRAPHICS ON
540 DEG
550 LDIR 90
560 CSIZE 2.6
570 LORG 6
580 Ssinplot(Mf,Pa,Mfp,0,20,1.5,-1.5)
590 Splot(25,45,1.5,-1.5,Hsp(*),Hs(*))
600 Srplot(50,70,1.5,-1.5,0,X(*))
610 Srplot(75,95,1.5,-1.5,1,X(*))
620 Srplot(100,120,1.5,-1.5,2,X(*))
630 PEN Up
640 BEEP
650 BEEP
660 GOTO Again
670 Dta6:Data6(X(*),Hsp(*),Hs(*))
680 GOTO Again
690 Exi:OUTPUT 2;"P"&"LOAD KEY"&"X"&"C";
700 END
710 Spwm:
720  xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
730 SUB Spwm(Mf,Nf,Degree(*))
740
750    THIS SUBPROGRAM COMPUTES THE INTERSECTION POINTS AND
760    THE SPECTRUM FOR THE SINUSOIDAL PWM FOR DIFFERENTS
770    MODULATION FACTORS (MF).
780
790 ALLOCATE REAL T(100)
800 RAD
810 Es=SQR(2)
820 Tol=.0005
830 Np=2*Nf+1
840 Sf=2*Nf
850 Nn=Np-1
860 FOR N=1 TO Nn
870   Xold=T(N)+PI/180
880   FOR K=1 TO 200          SPWM USING NEWTON ALGORITHM
890      F=Mf*(SIN(Xold))-((-1)^N)*(Sf*Xold/PI-2*N)
900      G=Mf*(COS(Xold))-((-1)^N)*(Sf/PI)
910      Xnew=Xold-F/G
920      Delta=ABS((Xnew-Xold)/Xnew)
930      IF Delta Tol THEN GOTO 960
940      Xold=Xnew
950   NEXT K
960   T(N+1)=Xnew
970   Degree(N+1)=T(N+1)*180/PI
980 NEXT N
990 GOTO Jump
1000 FOR I=1 TO Np
```

```
1010  PRINT USING """SPWM DEGREE (",2D,")=",5D.3D";I,Degree(I)
1020 NEXT I
1030 GOTO Jump
1040 FOR L=1 TO 51 STEP 2          HARMONIC SPECTRUM FOR SPWM
1050  IF L MOD 3=0 THEN L=L+2
1060  B=0
1070  FOR M=1 TO Nn
1080     Am=(-1)^M
1090     P=L*T(M+1)
1100     Q=L*T(M)
1110     B=B-(Am/L)*(COS(P)-COS(Q))
1120  NEXT M
1130  Ss(L)=.5*B/PI
1140 NEXT L
1150 Jump:
1160 DEALLOCATE T(*)
1170 SUBEND
1180 T_f:
1190 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
1200 SUB T_f(Np,Degree(*),INTEGER Hs(*))
1210 L=0
1220 Qq=+1
1230 ALLOCATE INTEGER Hs1(720),Hs2(720)
1240 FOR I=0 TO 720
1250  IF (I/2) Degree(L) THEN
1260     Hs1(I)=(-1)*Qq
1270  ELSE
1280     L=L+1
1290     Qq=-Qq
1300     Hs1(I)=(-1)*Qq
1310  END IF
1320 NEXT I
1330 FOR I=0 TO 720
1340  Hs2(I)=Hs1((I+240) MOD 720)
1350 NEXT I
1360 FOR I=0 TO 720
1370  Hs(I)=Hs1(I)-Hs2(I)
1380 NEXT I
1390 SUBEND
1400 Mix:SUB Mix(Pa,Np,INTEGER Hf(*),INTEGER Hs(*),INTEGER Hsp(*))
1410 FOR I=0 TO Pa
1420  Hsp(I)=Hf(I)
1430 NEXT I
1440 FOR I=Pa+1 TO 720
1450  Hsp(I)=Hs(I)
1460 NEXT I
1470 SUBEND
1480 Runge:SUB Runge(T,Np,K1,K2,K3,R,X(*),INTEGER Hf(*),INTEGER Hsp(*),INTEGER H
s(*))
1490        COMPUTING THE INITIAL CONDITIONS
1500 FOR I=1 TO 720*Np
```

```
1510  IF (I MOD Np)=0 THEN J=J+1
1520  U=Hf(J MOD 720)
1530
1540  C11=T*(-K1*X2+K1*U)
1550  C12=T*(K2*X1-K2*X3)
1560  C13=T*(K3*X2-K3*R*X3)
1570
1580  C21=T*(-K1*(X2+C12/2)+K1*U)
1590  C22=T*(K2*(X1+C11/2)-K2*(X3+C13/2))
1600  C23=T*(K3*(X2+C12/2)-K3*R*(X3+C13/2))
1610
1620  C31=T*(-K1*(X2+C22/2)+K1*U)
1630  C32=T*(K2*(X1+C21/2)-K2*(X3+C23/2))
1640  C33=T*(K3*(X2+C22/2)-K3*R*(X3+C23/2))
1650
1660  Uu=Hf((J+1) MOD 720)
1670
1680  C41=T*(-K1*(X2+C32)+K1*Uu)
1690  C42=T*(K2*(X1+C31)-K2*(X3+C33))
1700  C43=T*(K3*(X2+C32)-K3*R*(X3+C33))
1710
1720  X1=X1+(1/6)*(C11+2*C21+2*C31+C41)
1730  X2=X2+(1/6)*(C12+2*C22+2*C32+C42)
1740  X3=X3+(1/6)*(C13+2*C32+2*C33+C43)
1750 NEXT I
1760 PRINT "THE INITIAL CONDITIONS HAVE BEEN COMPUTED"
1770       COMPUTING THE POSITIVE TIME
1780 J=0
1790 FOR I=1 TO 1440*Np
1800  IF (I MOD Np)=0 THEN J=J+1
1810  IF J 720 THEN
1820     U=Hsp(J MOD 720)
1830  ELSE
1840     U=Hs(J MOD 720)
1850  END IF
1860
1870  C11=T*(-K1*X2+K1*U)
1880  C12=T*(K2*X1-K2*X3)
1890  C13=T*(K3*X2-K3*R*X3)
1900
1910  C21=T*(-K1*(X2+C12/2)+K1*U)
1920  C22=T*(K2*(X1+C11/2)-K2*(X3+C13/2))
1930  C23=T*(K3*(X2+C12/2)-K3*R*(X3+C13/2))
1940
1950  C31=T*(-K1*(X2+C22/2)+K1*U)
1960  C32=T*(K2*(X1+C21/2)-K2*(X3+C23/2))
1970  C33=T*(K3*(X2+C22/2)-K2*(X3+C23/2))
1980
1990  IF J 720 THEN
2000     Uu=Hsp((J+1) MOD 720)
```

```
2010  ELSE
2020     Uu=Hs((J+1) MOD 720)
2030  END IF
2040
2050  C41=T*(-K1*(X2+C32)+K1*Uu)
2060  C42=T*(K2*(X1+C31)-K2*(X3+C33))
2070  C43=T*(K3*(X2+C32)-K3*K*(X3+C33))
2080
2090  X1=X1+(1/6)*(C11+2*C21+2*C31+C41)
2100  X2=X2+(1/6)*(C12+2*C22+2*C32+C42)
2110  X3=X3+(1/6)*(C13+2*C32+2*C33+C43)
2120
2130  X(0,J)=X1
2140  X(1,J)=X2
2150  X(2,J)=X3
2160 NEXT I
2170 SUBEND
```

APPENDIX 3

BOOST CHOPPER, PRINCIPLES OF OPERATION

APPENDIX 3; Boost Chopper Principles of Operation

The boost chopper shown in Fig.(A3.1) is analyzed with the following assumptions:

i) input current Ic is continuous and ripple-free,

ii) output voltage Vd is also ripple free.

Both assumptions are compatible with rated output power and properly selected dc filter capacitors. With these assumptions, the equivalent circuit for the boost chopper and its associated current waveforms are as shown in Fig.(A3.1b). Also, in an ideal chopper,

$$P_{in} = P_{out} = E \cdot I_c = I_d \cdot V_d \qquad (A3.1)$$

and with reference to Fig.(A3.1b),

$$I_d = \left(\frac{t_2}{T}\right) I_c \qquad (A3.2)$$

Substitution of Id in (A3.1) using (A3.2) gives

$$\frac{V_d}{E} = \frac{T}{t_2} = G_c \qquad (A3.3)$$

where

$1 < G_c < \infty$ is the chopper gain.

Finally, from Fig.(A3.1c) and (A3.3), the current ratings for the switch S are found to be:

$$I_{s,ave} = I_d \left(\frac{t_1}{T_o}\right) = I_d\left(1 - \frac{1}{G_c}\right) \qquad \text{(A3.4)}$$

$$I_{s,rms} \left[I_d \left(\frac{t_1}{T_o}\right)^{\frac{1}{2}} = I_d \left(1 - \frac{1}{G_c}\right)^{\frac{1}{2}}\right. \qquad \text{(A3.5)}$$

$$I_{s,peak} = I_{d,peak} \qquad \text{(A3.6)}$$

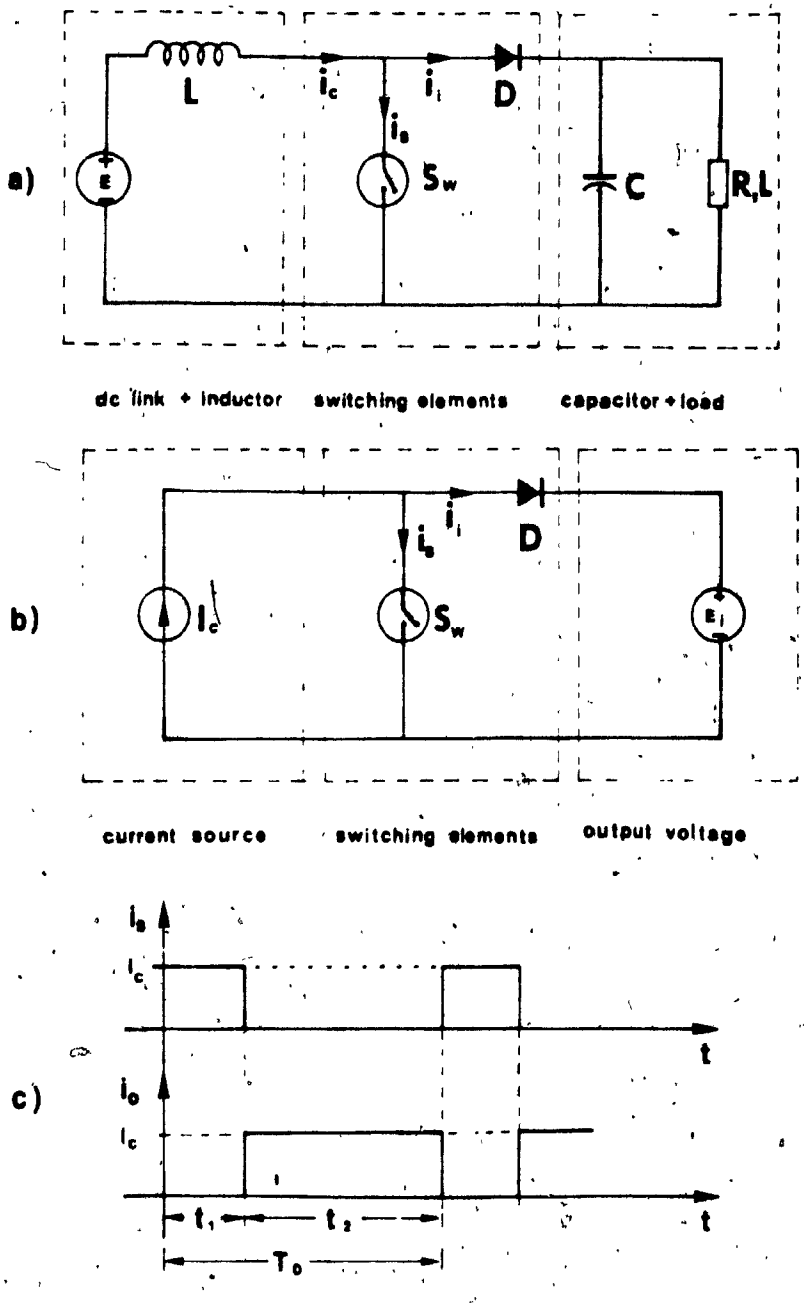

FIG.(A3.1): Ideal Boost Chopper
(a) Simplified diagram
(b) Equivalent circuit
(c) Current waveforms