NOTICE

AVIS

The quality of this microform is heavily dependent upon the quality of the original thesis submitted for microfilming. Every effort has been made to ensure the highest quality of reproduction possible.

If pages are missing, contact the university which granted the degree.

Some pages may have indistinct print especially if the original pages were typed with a poor typewriter ribbon or if the university sent us an inferior photocopy.

Reproduction in full or in part of this microform is governed by the Canadian Copyright Act, R.S.C. 1970, c. C-30, and subsequent amendments.

La qualité de cette microforme dépend grandement de la qualité de la thèse soumise au microfilmage. Nous avons tout fait pour assurer une qualité supérieure de reproduction.

S'il manque des pages, veuillez communiquer avec l'université qui a conféré le grade.

La qualité d'impression de certaines pages peut laisser à désirer, surtout si les pages originales ont été dactylographiées à l'aide d'un ruban usé ou si l'université nous a fait parvenir une photocopie de qualité inférieure.

La reproduction, même partielle, de cette microforme est soumise à la Loi canadienne sur le droit d'auteur, SRC 1970, c. C-30, et ses amendements subséquents.

Canada

ANALYSIS, DESIGN AND CONTROL OF ZERO VOLTAGE SWITCHED HIGH FREQUENCY PWM FORWARD CONVERTERS

Lautaro D. Salazar

A Thesis

in

The Department

of

Electrical and Computer Engineering

Presented in Partial Fulfillment of the Requirements

for the Degree of Doctor of Philosophy at

Concordia University

Montreal, Quebec, Canada

March 1995

Your file   Votre référence

Our file   Notre référence

ISBN   0-612-05074-2

Canada

ABSTRACT

ANALYSIS DESIGN AND CONTROL OF ZERO VOLTAGE SWITCHED HIGH FREQUENCY PWM FORWARD CONVERTERS

Lautaro D. Salazar
Concordia University, 1995

This thesis presents the analysis, design procedure and experimental results of a number of new high-frequency single-ended DC/DC forward converters topologies, to be used in switch-mode rectifier or off-line switch-mode power supplies. These proposed topologies are to supply load in the range of 1 kW to 10 kW with switching frequency, in the range of 20 kHz to 50 kHz. The main features include, high frequency pulse width modulated control (PWM) with zero voltage switching (ZVS), simplicity of the power circuit with minimum component count, fast transient response, and improved reliability. The applications cover a wide variety of AC/DC OR DC/DC switch-mode power supply for sensitive loads such as, telephone systems, communication equipment's, computer systems, space vehicles, factory automation, and other electronics systems needing reliable electric power in a form of DC voltage.

In order to reduce the switching losses, the voltage stresses, and the EMI problems in HF PWM converters, several new single-ended forward topologies with inherent active snubber circuit, providing zero-voltage-switching (ZVS) performance for the main power switch, are proposed. To allow transformer flux

balancing and extended duty cycle operation, the resulting modes of operation for each topology are thoroughly investigated. Systematic and comprehensive design approaches are outlined in detail. Each design approach is subsequently employed to design and to implement the respective power circuits.

The last part of this thesis reports the investigation of new output voltage regulation methods, needed to compensate for the input voltage and the load variations in HF PWM switching converters. Finally, in order to establish the feasibility of the proposed new converters topologies and control methods, simulations and experimental results are presented.

ACKNOWLEDGMENTS

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ACRONYMS

BJT	Junction Bipolar Transistor
CMC	Current Mode Control
FBR	Full Bridge Rectifier
HFT	High Frequency Tranformer
HBR	Half Bridge Rectifier
IGBT	Isolate Gate Bipolar transistor
MOSFET	Field Effect Metal Oxide Silicon Transistor
NR	Non Resonant Mode
PWM	Pulse Width Modulation
PI	Proportional Integral
QRAC	Quasi Resonant Auxiliary Circuit
RTW	Reference Triangular Waveform
SEFC	Single Ended Forward Converter
SPS	Switching Power supply
SMR	Switch Mode Rectifier
TM	Topological Mode
VMC	Voltage Mode Control
ZVS	Zero Voltage Switching
ZCS	Zero Current Switching

LIST OF SYMBOLS

1.   Circuit Parameters

C_o, C_f, C_{fo}	Output filter capacitance
C_{in}	Input filter Capacitance
C_s, C_1, C_2	Snubber capacitance
L_{in}	Input filter inductance
L_f, L_{fo}	Output filter inductance
L_s	Snubber inductance
L_1	Leakage transformer inductance, primary side
L_2	Leakage transformer inductance, secondary side
L_b	Inductance of the DC input bus
L_r	Inductance of a resonant circuit
L_m	Magnetizing transformer inductance
Z, Z_m, Z_1, Z_2, Z_r	Characteristic impedance of a resonant circuit
n, n_t	Turn ratio of the transformer
r_c	Series resistance of the output filter capacitor
R_L, R_l, R_{Lo}, R_o	Output load resistance

2.   Voltages

V_s, V_i, V_g	DC input voltages
V_c	Initial DC value of the snubber capacitor

V_m	Carrier wave amplitude
v_o	Load voltage
V_o	DC value of v_o
V_r	Maximum voltage value in a resonant circuit
v_t	Input voltage of the switching modulator
V_t	DC value of v_t
Δv_t	Small-signal AC variation of v_t

3.   Currents

i_{Lf}	Output filter inductor current
I_{Lf}	DC value of i_{Lf}
Δi_{Lf}	Small-signal variation of i_L
i_o	Load Current
I_o	DC value of i_o
i_t	Input current of the switching modulator
I_t	DC value of i_t
Δi_t	Small-signal AC variation of i_t

4.   Frequencies and Time Constants

f_r	Output filter resonant frequency
f_b	Output filter cut-off frequency
f_m	Modulation waveform frequency

f_s	Switching frequency
f_c	Cross-over frecuency of the loop transfer function
t_{on}	On-time of the main power switch
T_d	Delay time in the describing function for the PWM modulator and converter
T	Switching period
τ	Time variable
ω_m	Modulation wave frequency in rad/sec
ω_s	Switching frequency in rad/sec

5.   Miscellaneous

d	Duty cycle of the switchmode system
D	DC value for d
$H_1(s)$	Output filter transfer function
$H_2(s)$	All-pass filter transfer function
H_o	Control/output DC gain of a PWM power converter
$H_a(s), H_b(s)$	Control transfer function
$H_c(s)$	Control/output transfer function
$H_d(s)$	Differential amplifier transfer function
$H_i(s)$	Current loop transfer function
$H_v(s)$	Voltage loop transfer function

H_t	Transfer function of the current transformer
G	Gain of the feedback loop
Rm	Describing function of the PWM modulator
D1,D2	Diodes of the lossless snubber circuit
k1, k2	Resonance/switching frequency ratio
K1, K2, Kr, Ke	Inductances Ratio
$\delta(t)$	Switching function
Q	Quality factor of the resonance circuit with resistance
rv, Irv	Ripple factor of the output voltage
ri, Iri	Ripple factor of the output filter current
s(t)	AC control pulse
Tn	Loop transfer function of the feedback control system
ξ	Damping ratio of the feedback/output filter

CHAPTER 1: INTRODUCTION

The objective of this thesis is to develop reliable, efficient and fast-response DC/DC converters with pulse width modulation (PWM) control at ultrasonic switching frequency (i.e. 20-40 kHz). To achieve this objective, several low-losses single-ended forward topologies and control method are proposed and investigated. They are intended to be used as the main modules in low-voltage (i.e. 24-48 V) one-quadrant switching power supply (SPS) or switch-mode rectifier (SMR) systems for medium power applications (i.e. 1-10 kW).

1.1   Background

Switching power supply systems, with output power capability higher than 1 kW, are required to supply digital communication equipment, robotics, satellites, digital control systems and computers. The new generation of power supplies for these applications must meet stringent design specifications such as higher power density, better efficiency, good reliability, stiff output voltage regulation, fast-response, and lower cost. Due to the power switching operation, with sensitive electronic primary control circuits, modern SPS must meet power quality, environment and safety standards as well. There are several electrical institutes and government agencies around the world such as the Institute of Electrical and Electronics Engineers (IEEE), the Canadian Standards Association (CSA), the Underwriters' Laboratories (UL), the Federal Communications Commission

(FCC), the Verband Deutscher Elektrotechniquer (VDE). They continuously propose new regulations and standards for SPS or SMR concerning the harmonic pollution to the AC power system, the input power factor, the surge withstand capability, electric isolation level for safety, conducted-mode radio-frequency interference (RFI) and Electro-Magnetic Interference (EMI) emission limits.

Fig 1.1 shows an application for a cellular telephone station. In this system,
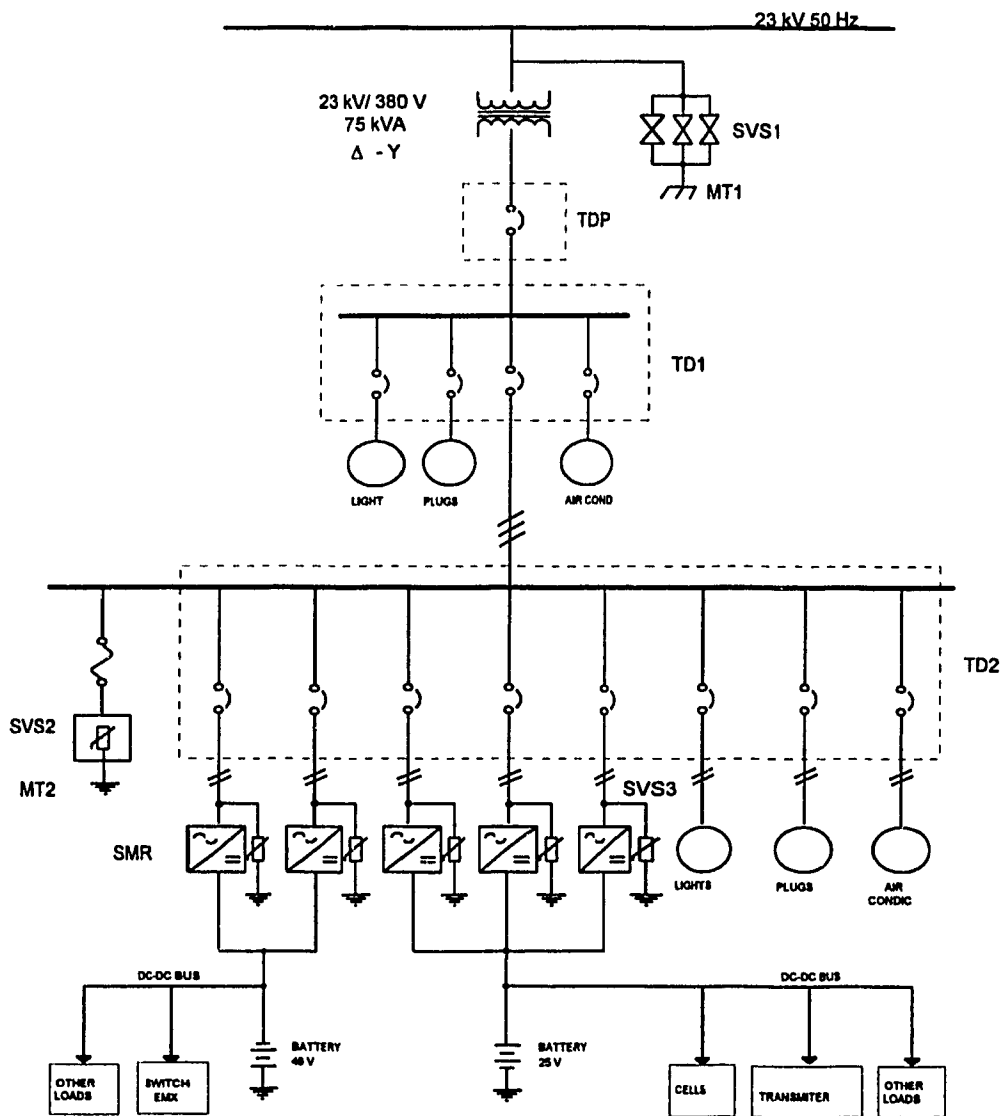
Figure 1.1 Typical Power Supply System for a Cellular Telephone Station [5]

the digital telecommunication equipments arc supplied from several 2500-W, low-voltage SPS's and two battery banks (24 V and 48 V DC bus). **Table 1-I** summarizes the design specifications for such a SPS's system.

Table 1-I

Design Specifications for a 2500 W, 50 V SPS [6]

1	Input	176 VAC to 265 VAC
2	Input frequency range	47 Hz to 63 Hz
3	Input surge	Up to 3000 V, 50 μsec pulse, st. ANSI/IEEE 62.41
4	Isolation	3000 VAC between input and output side
5	Power factor	>0.9 for three phase supplies, >0.95 for single phase, between 50% and full load
6	Input current harmonic distortion	<3% three phase, <5% single phase
7	Output voltage range	Adjustable, 40 to 65 V
8	Parallel operation	Any identical supplies will share load when connected in parallel
9	Dynamic response	Output will not vary by more than 5% and shall recover in less than 2 msec for a load step change of 10% to 90% or 90% to 10%
10	Voice frequency output noise	Less than 22 Dbrnc
11	Output noise	Peak to peak < 250 mV (oscilloscope > 100 MHz)
12	Ripple	Output ripple noise <100 mV RMS
13	Efficiency	>85%
14	Line regulation	Better than 1%
15	Current limit	110% of rated load
16	Inrush current	Will not exceed 1.2% of the steady state input rated current
17	Environment	0° C to 50° C
18	EMI	Compliant with FCC class A applications
19	Maximum Output Power	2500 W, 50 A

1.2 Overview of Switch-Mode Power Supply Structures

The overall performance for the SPS described in section 1.1 strongly depends on its own internal structure. In high power application, some intrinsic reliability is required to select the basic topologies for the internal conversion stage (AC/DC and DC/DC), including the control strategy to regulate the output voltage [1]. This section presents a brief review and discussion of the main structure used today to design SPS's or SMR's.
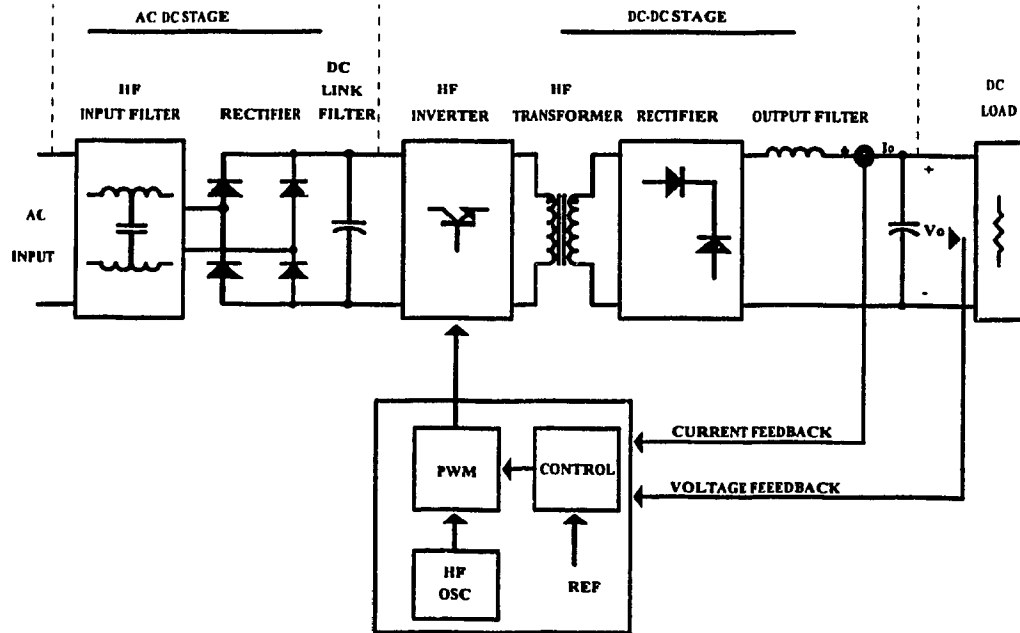
Figure 1.2 The SPS Structure with an Input Rectifier [7].

1.2.1 The SPS Structure with an Input Rectifier

A typical PWM SPS has two conversion stages; an input AC/DC stage in cascade with an output DC/DC stage. The input stage consist of a diode rectifier feeding a large electrolytic capacitor filter to build a DC bus. The output stage is a

high frequency (HF) DC/DC switching regulator with current and voltage feedback loops. This structure is shown in the Fig. 1.2 and it is usually called *direct off-line SPS or SMR* [2-4]. The capacitor filter increases the DC conversion ratio and reduces the HF harmonics generated by the output switching regulator and the input rectifier. The RF input filter, which conducts RF and EMI (common and differential mode), is required to meet the line regulation limit in noise due to the switching phenomenon of the SPS's power devices [4,5].

The main role of the HF DC/DC switching regulator is to maintain the DC output voltage constant, despite circuit parameters, load and line input voltage variations. For low voltage applications, this stage is designed by using a step-down forward converter topology equipped with a HF isolation transformer [3]. Isolation is very important to meet safety regulation and to minimize the grounding current loop. The HF transformer is usually designed with several taps to obtain different output voltage levels required by the loads and the control circuits [6,7].

It should be noted that this structure does not have an isolation transformer between the utility and the power switches. When this type of power supply is used in a system such as in shown in Fig. 1.1 the robustness of the power conversion stage becomes a very important issue. Since voltage perturbations are normally present in the utility, they can affect the normal operation or damage the power supply unit.

The reliability and the efficiency of this type of power supply can be improved when single ended forward converters are used to design the internal DC/DC conversion stage. This is so because a single ended topology has low component count as compared with other topologies, and the transformer impedance is always in series with the power switches. Since higher speed switches, such as MOSFET, IGBT, etc., are available, with higher current and voltage capability, new single ended topologies can be designed for higher power and switching frequency, reducing further the size and the cost of the SPS.

On the other hands, investigation of better control methods for higher power and frequency is further motivated by the problems of higher input voltage and load variations, the sensor required for higher level of DC current, the phase lagging and the noise problems affecting the HF PWM feedback control loop [1,6-8]. Improvements of the conventional control methods are required, or new control approach need to be develop.

1.2.2 The Modular SPS Structure

Another type of SPS uses a modular structure to provide better input-output performance [2,8-10]. Such a structure is shown in Fig. 1.3. To improve the input characteristics, the input stage is a high frequency switchmode rectifier as the line conditioner. The rectifier usually uses step-up boost topology to provide some form of preregulated DC bus at a manageable voltage level (e.g. 300 V, 600 V, and

800 V). This input stage enhances the input power factor to near unity, achieving

almost sinusoidal input current waveform.

The DC/DC output stage, on the other hand, includes one or several HF
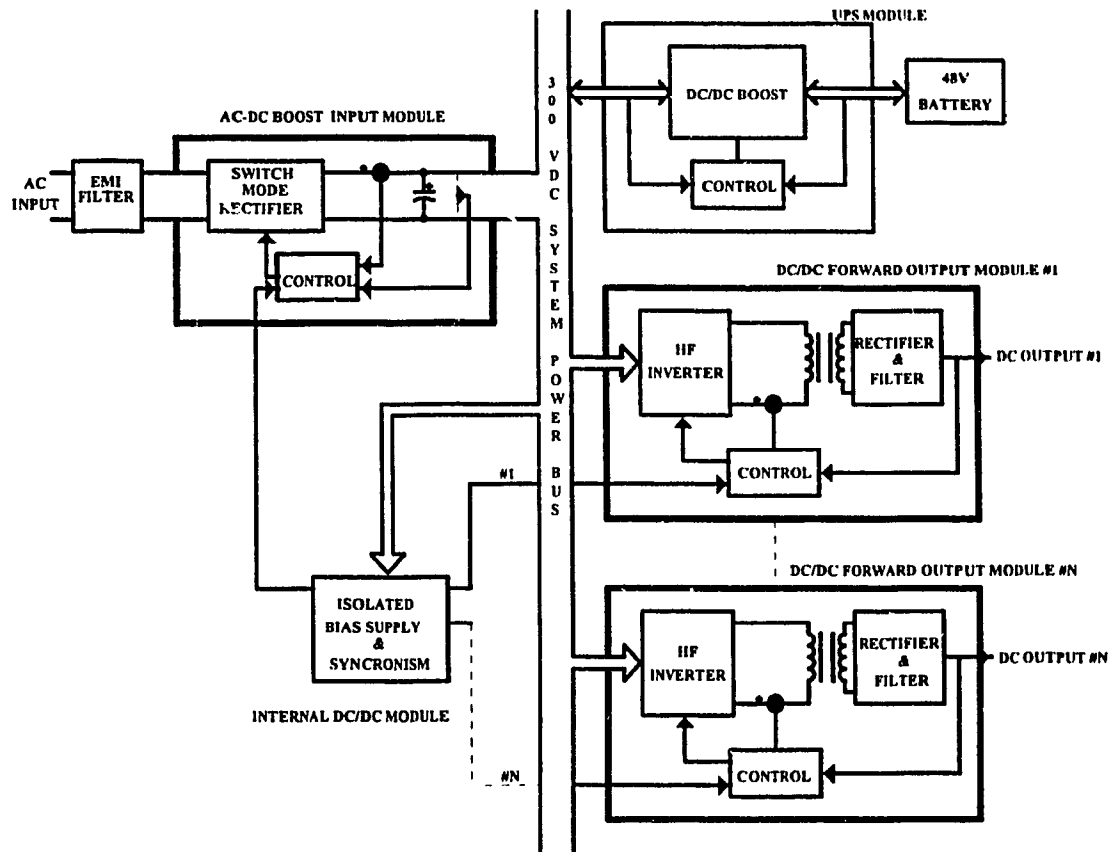
Figure 1.3 The Modular PWM SPS Structure [2].

forward switching regulators connected in parallel to the DC bus, depending on the

number of different loads and the output power required. Paralleling provides

power supply redundancy to critical load, and the defective modules can be

replaced on line.

The modular SPS structure is meaningful because it provides built-in

expansion capability, reduces the design costs, improves line noise immunity, and

can be easily adapted to different levels of power and loads. However, there are several problems that still need to be solved in this structure, notably the EMI, the overall size, the switching losses, the cost and the robustness of the basic modules

1.2.3 The SPS Structure with Distributed DC/DC Converters

Distributed SPS structures with single ended quasi-resonant topologies have been proposed [11,12] to minimize the main drawbacks of the SPS structure shown in Fig. 1.2. In this approach, the output DC/DC switching regulators are distributed and located close to the loads to minimize size and parasitic inductances. This *on-site DC/DC converter* is optimized for maximum power density, low switching losses and fast voltage regulation. However, this approach is being used only for low-power high-density SPS (<1 kW) to supply satellite and portable computer systems. New converter topologies for the distributed modules with higher power capability need to be developed to take more advantages of this structure in other applications (e.g. Fig 1.1).

1.3 DC/DC Single Ended Converter Topologies for High Power

Clearly, the overall performance of the above SPS's structure strongly depends on the characteristics of the basic converter topology employed to design the internal conversion stages. Therefore, most of the research and development efforts are dedicated to improve the performance, decrease the cost and increase the power density of the basic topologies. The trends to do this is by using high

switching frequency and fewer power components.

Single-ended forward topologies are very attractive to achieve these requirements because the simplicity of the power circuit. The basic circuit configuration uses only one power switch [3] so that only one polarity of the DC input source is applied to the primary of the HF isolation transformer. Different power conversion methods have been proposed to control the flow of power giving origin to the following single ended DC/DC topologies:

1)   Square-wave converter with PWM control [3,12,21];

2)   Sinusoidal-wave resonant converter [16,18,37];

3)   Quasi-resonant/multi-resonant converter [17];

4)   Discrete converter [34] .

The single ended resonant, quasi-resonant/multi-resonant and discrete converters have received considerable attention for designing HF SPS for low-power applications [13-15,34,37]. Some of the advantages in using such converters are the EMI emission reduction, low switching loss, fast transient response and high power density. However, most of those topologies have the following practical limitations for medium or higher power applications:

1)   The power switches conduct a much higher sinusoidal current pulse. Consequently, a larger conduction losses exist as compared to its PWM counterpart;

2) They require a frequency variation to achieve the output voltage regulation, which may cause filter design problems, as well as having an ill-defined voltage feedback control loop.

3) The circuit components need kVA ratings that are far larger than the converter rating, with the switching devices subject to high peak current/voltage stresses.

Due to the above limitations, DC/DC converter with resonant switch topologies do not yet offer good reliability and enough robustness for high power applications. They are usually used to design high density low power SPS (<1 kW).

A HF PWM forward converter presents better reliability for applications higher than 1 kW. In fact, the peak voltage-current stresses for the power circuit are lower than a resonant converter due to the squared current/voltage waveforms generated by the PWM control. Also, this feature provides a better output-input voltage DC conversion ratio, improving the utilization of the power switch. However, the present single-ended PWM forward topologies have low efficiency at high switching frequency and the isolation transformer requires special design or flux resetting circuits to avoid saturation. The PWM square voltage and current waveforms cause a hard turn-on and turn-off, increasing the switching losses and the EMI problems.

The main causes of switching losses are:

1)   *Power dissipation due to the non zero switching of the transistor*: At turn-off/turn-on, each transistor operates for a given time in the active region, having both high voltage and high current at the same time. The shorter the switching time of the transistor, the less the average dissipation will be.

2)   *The external reactances around the power transistor*: The parallel capacitances cause the stored $CV^2/2$ energy to be dissipated on the switch at each turn-on, and the stored $LI^2/2$ energy in the series inductances at each turn-off. These power dissipations are independent of the transistor switching times.

The most severe voltage stress in the forward topologies occurs during the turn-off, due to the intrinsic inductances of the HF isolation transformer (leakage-magnetizing inductances) and the parasitic inductance of the DC bus. All of these are inductive loads requiring a large Safe Operation Area on the V-I characteristics of the switches. Diodes with poor reverse recovery characteristics significant add to this phenomenon which also produces EMI. To be able to withstand such large stresses, power semiconductors devices would have to be de-rated.

Low frequency PWM converters incorporate dissipative diode-resistor-inductor (turn-on) and Diode-resistor-capacitor (turn-off) snubber circuits to alleviate the above problems [22]. Those circuits dissipate on a resistor most of the

energy that could be dissipated on the switch during the switching transition. This decreases the operating temperature in the power transistor, requiring smaller heatsinks and improving the reliability. However, the sum of the total stored energy ($CV^2/2+LI^2/2$) in the snubber circuits and parasitic components increases approximately with the square of the converter power rating, and the amount of the dissipated energy. Moreover, the power dissipated on the snubber resistors is proportional to the switching frequency. Obviously, the overall efficiency of such a converter system will decrease substantially when both power and switching frequency are increased. Therefore, a dissipative snubber circuit is an unusable solution for HF PWM converter technology in high power applications.

The first trend to reduce switching losses in HF PWM converters is to select new available faster switches such as MOSFET or IGBT. However, due to the faster on/off switching transitions, the parasitic L of the wiring in series and the C around the switch becomes more important, producing large di/dt and dv/dt, which in turn increases the current/voltage stresses, the losses and the EMI problems.

1.4   Objectives and Scope of the Thesis

This thesis focuses on the analysis, design, and experimental testing of a number of HF PWM single ended forward DC/DC converters for output power in the range of 1kW to 10 kW and for output voltage in the range of 24 to 50 Volts. They are intended to be used as the DC/DC modules for the SPS structures

described in the section 1.2. The research objective is to develop single-ended topologies with one or more switches and by using a HF transformer without the resetting winding.

This thesis investigates solutions to the switching losses and transformer flux balancing problems by combining resonant and PWM technology. The research trend is to keep the main power control features of the PWM and use resonant circuits to shape the voltage/current waveforms only during the switching transition, in such a way that voltage and current do not occur at the same time. Such a nondissipative circuit provides a soft switching reducing EMI and switch power dissipation allowing higher converter efficiency.

Zero voltage switching methods are investigated to remove the energy on the parasitic and snubber capacitors in parallel with the main switch. Analytical closed form solutions are obtained, and numerical method are applied to get the steady state voltage/current solutions in the different modes of operation. The design procedure for the proposed topologies are illustrated through examples.

Control of the output voltage is essential in most power supply systems, either to compensate for input voltage, circuit parameters and load variations, or to suit different load demands. This thesis proposes an unified design procedure to design a PWM voltage mode control for the proposed forward converters. Moreover, a new PWM control technique is investigated and is called here "PWM

current assisted voltage mode control." Finally, to verify the validity of the theory, simulated and experimental result are presented.

1.5 Previous Work

High-efficiency single-switch HF PWM forward converter for power higher than 2 kW, using two winding HF transformer, has not been reported before. For output power lower than 1 kW, the conventional design is to use a forward converter and a three winding transformer with a feedback diode and D-R-C snubbers [3]. The drawback of this converter for HF high power applications are the size and the complexity of the transformer, the limitation in the maximum duty cycle (to avoid saturation of the HF transformer), the low efficiency due to the dissipative snubber required, and the voltage stresses in the power semiconductor devices (rectifier diodes and the main switch).

Sokal [14] proposed an auxiliary resonant circuit as alternative to reset the core and reduce the switching losses. However, the analysis did not include the effect of the load in the DC magnetizing current of the HF transformer, and the experimental verification was for a low power unit (< 1 kW). No information was given with respect to the efficiency, and how the value of the magnetizing inductance can affects the maximum switch voltage.

Vinciarelli [15,16] proposed a method for transformer core resetting and zero current switching for single-ended forward converters. An active snubber

using an extra switch was connected in parallel with the transformer resetting the core during the turn off. However, the ZVS feature was not identified and this method can not eliminate the energy in any series parasitic inductance.

Single-ended quasi-resonant topologies have been also analyzed by F. C. Lee [2] and L. Casey [18]. These topologies present low switching losses but the peak current and voltage in the switch are high and they require frequency variation to regulate the output voltage. Therefore, they are more suitable for low power applications.

Control methods for DC/DC are widely discuss in the litterature, including current mode and voltage mode PWM control [6-8,43-47]. However, these control methods have been applied in very compact low power DC/DC converters and there is not information about the performance in higher power applications.

1.6   Thesis Outline

This thesis has been organized in the following manner:

Chapter Two focuses on the analysis and design of 1kW, 20 kHz, single-ended single-switch forward topologies with auxiliary quasi-resonant circuits to reduce switching losses and to reset the core of the HF transformer. These are forward topologies using a two-winding transformer with low component count, improving the reliability and the utilization of the power circuit.

Chapter Three extends the research work toward series and parallel

connected single-switch topologies, to reduce voltage stresses and to increase output power. A novel two switch single-ended topology is thoroughly analyzed. The main feature of this topology is the simplicity and the reduced switching losses. This configuration uses one resonant capacitor to provide zero voltage switching transition for both parallel switches.

Chapter Four presents single-ended forward topologies coupled in a three phase core. They are proposed for output power applications higher than 5 kW. Three different topologies are investigated regarding the flux balancing problem. A design procedure is proposed for each of them and the advantages and disadvantages are summarized. To verify the feasibility of each topology, a general multiphase flux transformer model is proposed and used. Simulation results are presented by using the PSPICE software package.

Chapter Five focuses on control methods. A design procedure for a PWM voltage mode control is outlined and applied in a two-switch single-ended forward converter with the extended duty cycle capability. A new PWM current assisted voltage mode control method is proposed. It is shown that this control method has features of both voltage and current mode control. Simulated and experimental results verify the predictions of the theory.

Finally, *Chapter Six* summarizes the conclusions. Directions for further areas of research are identified.

CHAPTER 2

SINGLE-SWITCH FORWARD CONVERTERS

2.1   Introduction

Single-switch single-ended forward converter topologies have some important advantages over other types of topologies. These advantages include good reliability, power circuit and control logic simplicity [1].

On the other hand, the following disadvantages are found :

1)   Switch voltage stresses increase;

2)   Transformer flux balancing is not inherent and therefore requires special voltage clamping components;

3)   Turn-off switching losses are particularly unfavorable for the power switch due to the switch turn-off under maximum current and voltage conditions, and the inability to recover the energy stored in transformer leakage and circuit stray inductances. This energy must be dissipated either within or around the switch.

In this chapter, two single-switch single-ended forward topologies with non dissipate turn-off snubber circuit are described and thoroughly analyzed. The snubber circuit are designed to provide zero voltage switching during turn-off and flux reset for the HF transformer.
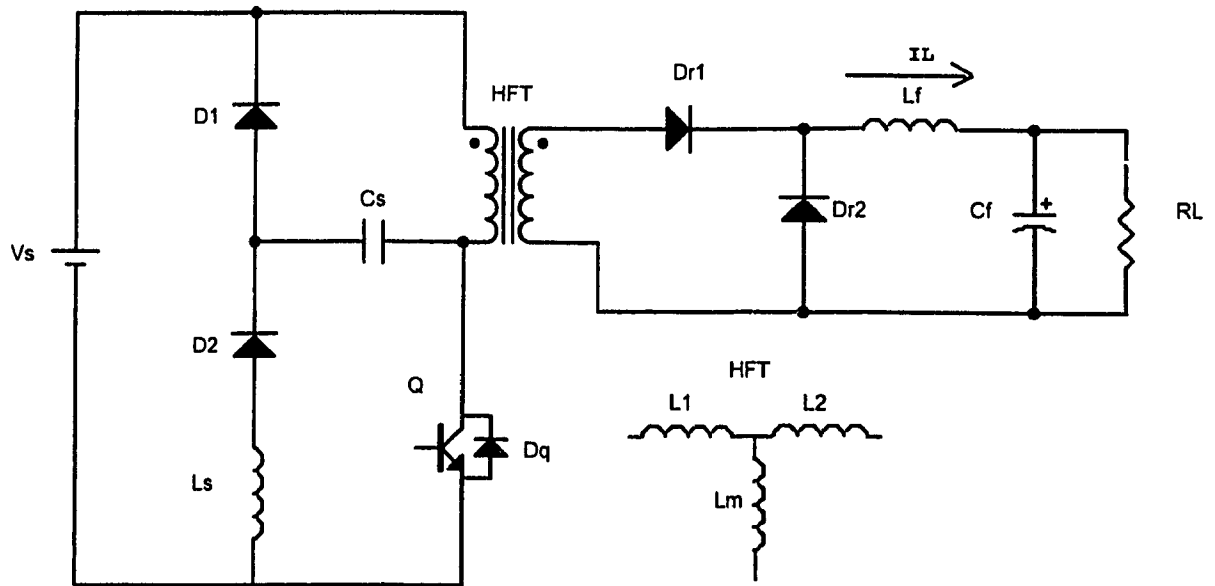
Figure 2.1 The Single Ended Forward Converter with a LC Snubber Circuit

2.2 Topology I: Nondissipative LC Snubber Circuit

The subject topology is shown in Fig. 2.1. Similar schemes using the same lossless LC snubber circuit have been described before for both a flyback converter and a forward converter [14,23]. However, the application was for a low power converter (< 1 kW). Also, it is unclear from these references how the LC circuit ensures transformer flux balance under various circuit parameters and operating conditions. This thesis contributes to the previous works with a detailed analysis of this circuit in order to know the effects of the load current, the leakage inductances, and the magnetizing inductance on the switch maximum voltage stress and transformer flux balancing condition. Identification of the topological modes (TM's) during a switching cycle are also presented, along with the

respective voltage/current expressions derived under steady state operating conditions. Finally, a design procedure is proposed and verified on a 1-kW 20-kHz experimental unit.

2.2.1 Principles of Operation

The simplified power converter circuit diagram depicted in Fig. 2.1 shows the DC supply voltage V_s, the HF transformer equivalent circuit with the magnetizing inductance L_m and the leakage inductances L_1 and L_2, the forward and freewheeling HF rectifier diodes D_{r1} and D_{r2}, the load current (through the rectifier filter inductor) as current source I_L, the main switch and its integral anti parallel diode D_q, the flux balancing and energy recovery resonant capacitor C_s, the energy recovery resonant inductor L_s, and the two energy-recovery diodes D_1 and D_2. The TM's for a quasi-resonant mode of operation, identified in sequence during turn-on and turn-off, are presented in Figs 2.2 and 2.3, respectively. Operation of the circuit is illustrated with the aid of the waveforms depicted in Fig. 2.4. Initially, it is assumed that the capacitor C_s has a negative voltage $V_{Cs}(0) = -V_c$ (Fig. 2.1) and the output current I_L flows through diode D_{r2}.

A. Turn-On

1) Mode T1a, interval $0<t<ta$: When the transistor Q is on, inductances L_1 and L_2 begin to store magnetic energy because the transformer is connected to V_s with

the secondary in short circuit via D_{r_1}, D_{r_2}, and Q. The rate of rise of the transistor current is limited by L_1 and L_2.

2) Mode T1b, interval $0<t<tb$: In addition, when transistor Q is on, C_s is connected in parallel with L_s through Q and D_2. The V_c polarity (VCs(0)) becomes reversed because of the resonant action of L_s and C_s.

3) Mode T2a, interval $ta<t<ton$: At $t = t_a$ (Fig. 2.4), the current $i_{L2} = I_L$. After that the output circuit (i.e., current source I_L) becomes connected to the HF transformer. Hence energy is now delivered to the load from the supply.

4) Mode T2b, interval $tb<t<tc$: If V_c is less than $-V_s$ at t=0, the final voltage of the capacitor C_s at $t = tb$ becomes positive and is clamped to V_s by both diodes D_1 and D_Q.. After that, the magnetic energy still in L_s is returned back to the source V_s via D_1 and D_2.

B. Turn-Off

1) Mode T3, interval $ton<t<t1$: At $t = t_{on}$, the transistor Q is turned off, and the collector current begins to fall at a rate limited only by the commutation speed of the transistor. However, because of the inductive impedance of L_m, L_1, and L_2, the external current i_{L2} (Fig. 2.1) cannot change instantaneously. Instead, it flows through C_s and D_1. At this point, the C_s voltage polarity is positive ($V_c \leq V_s$). Next, the capacitor voltage begins to vary slowly (towards changing polarity), limiting the rate of rise of the collector emitter voltage; thus the transistor
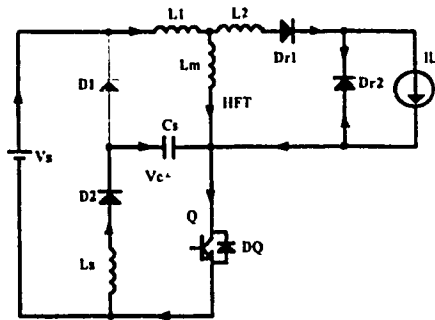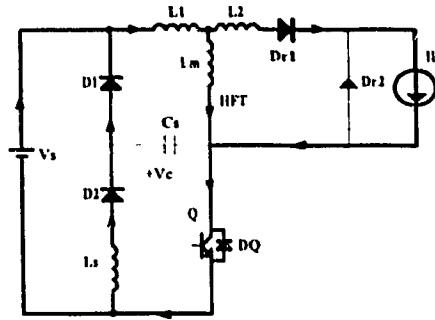
Mode T1a and T1b   Mode T2a and T2b

Turn-on
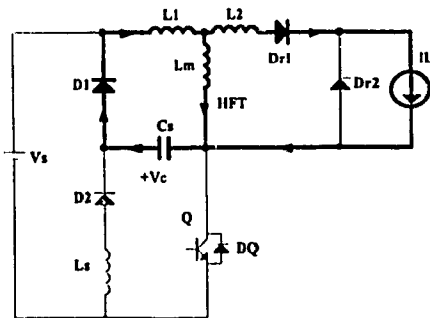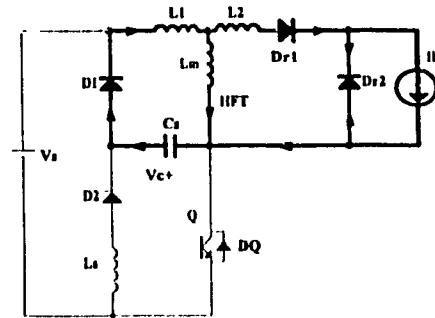
Mode T3   Mode T4
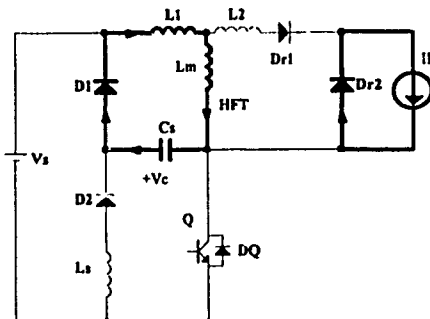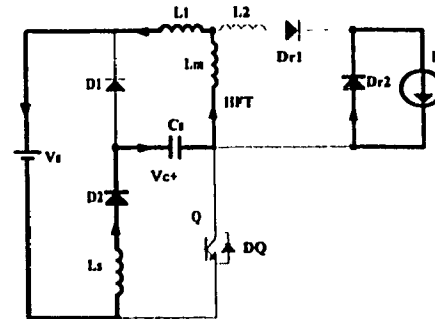
Mode T5   Mode T6

Turn-off

Figure 2.2   Equivalent circuits during a switching period

2-5
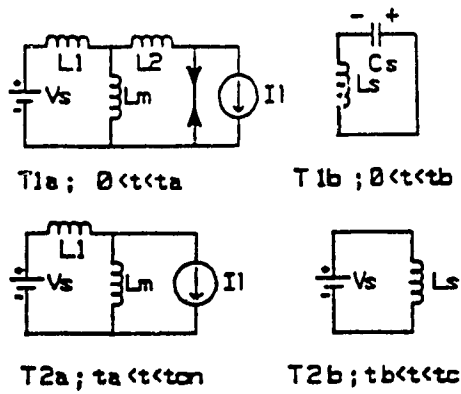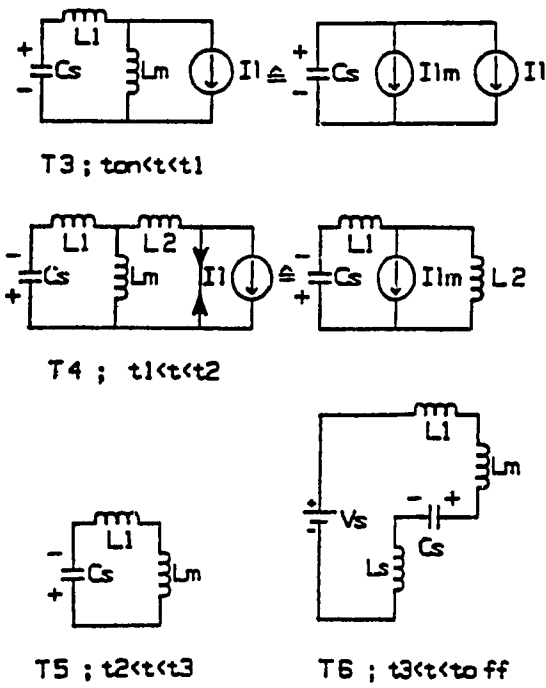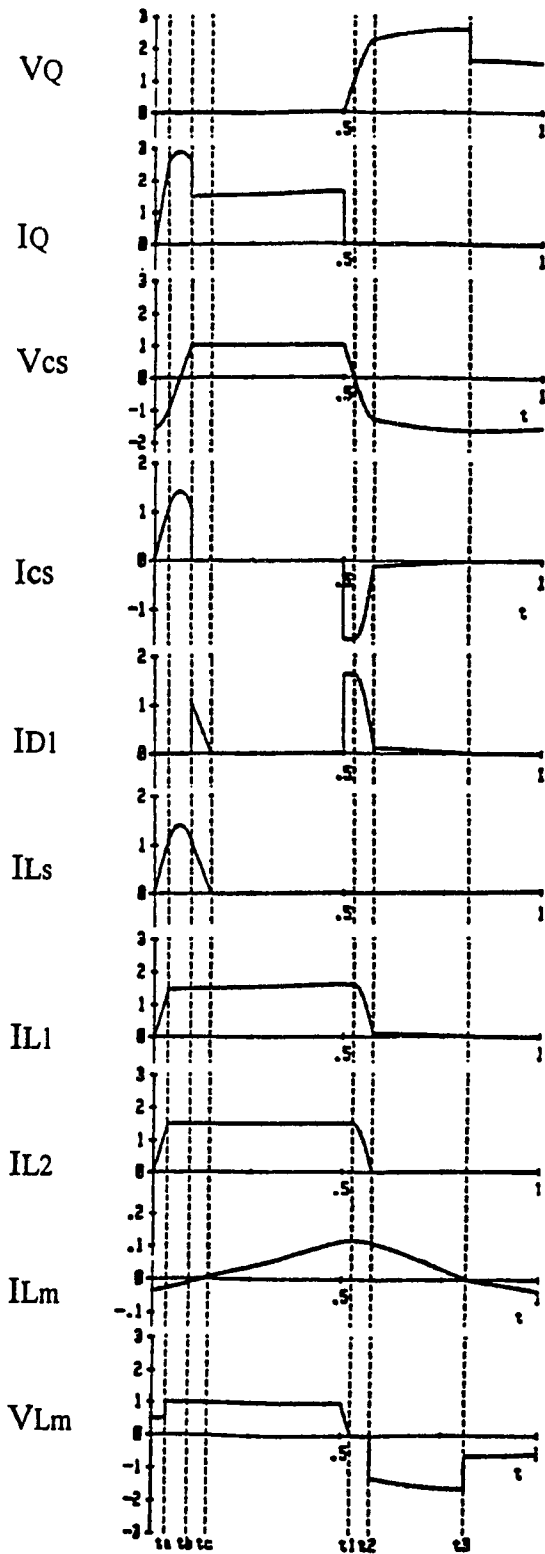
Figure 2.3 Topological Modes.

Figure 2.4 Analytical Voltage/Current Waveforms (ton=0.5)

2-6

turn-off losses are substantially reduced. Note that in this mode, energy stored in the capacitor flows to the load

2) *Mode T4, interval t1<t<t2*: At t > t_1, diode D_{r2} takes the load current and the secondary of the transformer becomes short circuited via conducting diodes D_{r1} and D_{r2}. Also, the capacitor absorbs the magnetic energy stored in the leakage inductance's L_1, L_2, and partially from the magnetizing inductance L_m. Thus the polarity of V_c change to negative.

3) *Mode T5, interval t2<t<t3*: At t = t_2, i_{L2} becomes zero. After that, the load I_L is effectively disconnected. The rest of the magnetic energy stored in L_m gets transferred to C_s, and the voltage V_c assumes its maximum negative value at t = t_3. Also at this time, the transformer flux reset condition is satisfied because the magnetizing current is equal to zero.

4) *Mode T6, interval t3<t<toff*: If the period T of the control signal is larger than t_3 and $|V_c|>V_s$, one oscillation begins via D_2 between L_1, L_m, C_s, and L_s, so that some of the electric energy stored in the capacitor is sent back to the source. Note that the magnetizing current become negative (Fig. 2.4).

2.2.2 Power Circuit Converter Analysis

In this section, the exact analytical expressions describing the converter currents and voltages during a switching cycle are obtained. The analysis is based on the following assumptions.

1) The switches and diodes are ideal;

2) Capacitor and inductors are lossless;

3) The transformer is considered linear and lossless;

4) The sources are ideal;

5) The transformer leakage-stray inductances are included in L_1 and L_2.

A. *State Equations and General Solution*

To obtain the state equations for all modes shown in Figs. 2.2 and 2.3, only three circuits need to be considered. They are:

1) An inductor connected to a voltage source;

2) An L-C parallel circuit connected or disconnected to a current source;

3) An L-C series circuit connected to a voltage source.

Moreover, the currents and voltage expressions applicable to each mode (Fig. 2.3) can be obtained by solving only the state equations of the basic circuits 1) and 2) above. By inspection, the independent state equations can be written as

$$\frac{d}{dt} i_L(t) = \frac{V_s}{L_e} \tag{2.2.1}$$

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_{Cs}(t) \end{bmatrix} = \begin{bmatrix} 0 & \dfrac{1}{L_e} \\ \dfrac{1}{C_s} & 0 \end{bmatrix} \cdot \begin{bmatrix} i_L(t) \\ v_{Cs}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ -\dfrac{1}{C_s} \end{bmatrix} \cdot I_L \quad , \quad \begin{bmatrix} i_L(0) \\ v_{Cs}(0) \end{bmatrix} \tag{2.2.2}$$

where L_e is the equivalent circuit inductance` shown to the source or to the capacitor C_s. The general solutions to (2.2.1) and (2.2.2) have the form:

$$i_L(t) = \frac{V_s}{L_e}t + i_L(0) \qquad (2.2.3)$$

$$X(t) = e^{At}X(0) + A^{-1}\left[e^{At} - I\right]Bu \qquad (2.2.4)$$

where

$$X(0) = \begin{bmatrix} i_L(0) \\ v_{Cs}(0) \end{bmatrix} \qquad A = \begin{bmatrix} 0 & \dfrac{1}{L_e} \\ \dfrac{1}{C_s} & 0 \end{bmatrix}$$

$$I = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \qquad Bu = \begin{bmatrix} 0 \\ -\dfrac{I_1}{C_s} \end{bmatrix} \qquad (2.2.5)$$

$$e^{At} = \begin{bmatrix} \cos\dfrac{t}{\sqrt{L_e C_s}} & \sqrt{\dfrac{C_s}{L_e}}\sin\dfrac{t}{\sqrt{L_e C_s}} \\ -\sqrt{\dfrac{L_e}{C_s}}\sin\dfrac{t}{\sqrt{L_e C_s}} & \cos\dfrac{t}{\sqrt{L_e C_s}} \end{bmatrix} \qquad (2.2.6)$$

The general solution to circuit 3) is obtained from (2.2.4)-(2.2.6) by applying the duality principle. The solutions are completed by using a dependent state equation in all modes with all-inductor cut sets.

B. Current and Voltage Equations

In the following subsections the piece wise voltage and current solutions (Fig. 2.4) regarding a quasi-resonant mode of operation are presented .

1) **Turn-On:**

a) *Interval 0 <t <t_a, Mode 1a*: The equivalent circuit is shown in Fig. 2.2 . From (2.2.3) an by using current division, the magnetizing current of the transformer is shown to be

$$i_{Lm}(t) = \frac{L_2}{P_1} V_s t + i_{Lm}(0) \qquad (2.2.7)$$

where

$$P_1 = L_1 L_m + L_1 L_2 + L_2 L_m \qquad (2.2.8)$$

The dependent state equation is

$$L_m \frac{d}{dt} i_{Lm}(t) = L_2 \frac{d}{dt} i_{L2}(t) \qquad (2.2.9)$$

Therefore,

$$i_{L2}(t) = \frac{L_m}{P_1} V_s t + i_{L2}(0) \qquad (2.2.10)$$

$$i_{L1}(t) = \frac{L_0}{P_1} V_s t + i_{L1}(0) \qquad (2.2.11)$$

where

$$L_0 = L_m + L_2 \qquad (2.2.12)$$

$$v_{Lm}(t) = \frac{L_m L_2}{P_1} V_s \qquad (2.2.13)$$

b) Interval $t_a < t < t_{on}$, *Mode 2a*: During this mode, the load current I_L is supplied from the transformer. The equivalent circuit is shown in Fig. 2.2. The respective analytical expressions become

$$i_{L1}(t) = \frac{V_s}{L_i} \tau_a + i_{L1}(t_a) \qquad (2.2.14)$$

$$i_{L2}(t) = I_1 \qquad (2.2.15)$$

$$i_{Lm}(t) = i_{Li}(t) - I_1 \qquad (2.2.16)$$

where

$$L_i = L_1 + L_m \qquad (2.2.17)$$

$$\tau_a = t - t_a \tag{2.2.18}$$

$$t_a = \frac{P_1}{L_m}\frac{I_1}{V_s}, \quad \text{if } i_{L2}(0) = 0 \tag{2.2.19}$$

c) Interval $0 < t < t_b$, Mode 1b: The capacitor voltage V_c undergoes a polarity reversal oscillation. The equivalent circuit is shown in Fig. 2.2. By using (2.2.4) with u = 0, the respective solution becomes

$$\begin{bmatrix} i_{Ls}(t) \\ v_{Cs}(t) \end{bmatrix} = \begin{bmatrix} \cos\dfrac{t}{\sqrt{L_sC_s}} & -\sqrt{\dfrac{C_s}{L_s}}\sin\dfrac{t}{\sqrt{L_sC_s}} \\ \sqrt{\dfrac{L_s}{C_s}}\sin\dfrac{t}{\sqrt{L_sC_s}} & \cos\dfrac{t}{\sqrt{L_sC_s}} \end{bmatrix} \cdot \begin{bmatrix} i_{Ls}(0) \\ i_{Cs}(0) \end{bmatrix} \tag{2.2.20}$$

Also

$$i_{D2}(t) = i_{Ls}(t) = i_{Cs}(t) \tag{2.2.21}$$

$$i_{D1}(t) = 0 \tag{2.2.22}$$

$$i_Q(t) = i_{Lm}(t) + i_{L2}(t) + i_{Ls}(t) \tag{2.2.23}$$

$$v_{Di}(t) = V_s - v_{Cs}(t) \tag{2.2.24}$$

d) Interval $t_b < t < t_c$, Mode 2b: This mode occurs only if the capacitor voltage is clamped to V_s at t = t_b. The equivalent circuit is shown in Fig. 2.2 . The respective analytical expressions become

$$i_{Ls}(t) = -\frac{V_s}{L_s}\tau_b + i_{Ls}(t_b) \tag{2.2.25}$$

$$v_{Cs}(t) = V_s \tag{2.2.26}$$

where $\quad \tau_b = t - t_b \tag{2.2.27}$

and with $i_{Ls}(0) = 0$

$$t_b = \begin{cases} \pi\sqrt{L_sC_s}, & \text{if } v_{Cs}(t_b)\langle V_s \\ L_sC_s\cos^{-1}\dfrac{V_s}{v_{Cs}(0)}, & \text{if } v_{Cs}(t_b) = V_s \end{cases} \qquad (2.2.28)$$

Also,

$$i_{Cs}(t) = 0 \qquad (2.2.29)$$

$$i_{D1}(t) = i_{D2}(t) = i_{Ls}(t) \qquad (2.2.30)$$

$$i_Q(t) = i_{Lm}(t) + i_{L2}(t) \qquad (2.2.31)$$

$$t_c = \frac{L_s}{V_s}i_{Ls}(t_b) + t_b \qquad (2.2.32)$$

and with $i_{Ls}(0) = 0$

$$i_{Ls}(t_b) = -v_{Cs}(0)\sqrt{\frac{C_s}{L_s}}\sin\frac{t_b}{\sqrt{L_sC_s}} \qquad (2.2.33)$$

2) **Turn-Off:**

a) Interval $t_{on} < t < t_1$, *Mode 3*: At $t = t_{on}$, the transistor Q is turned off and the resulting effective circuit topology is shown in **Fig. 2.3**. The energy stored in the capacitor flows to the load through diode D_1. The respective analytical expressions become

$$\begin{bmatrix} i_{Lm}(t) \\ v_{Cs}(t) \end{bmatrix} = \begin{bmatrix} \cos\dfrac{\tau_1}{\sqrt{L_iC_s}} & -\sqrt{\dfrac{C_s}{L_i}}\sin\dfrac{\tau_1}{\sqrt{L_iC_s}} \\ \sqrt{\dfrac{L_i}{C_s}}\sin\dfrac{\tau_1}{\sqrt{L_iC_s}} & \cos\dfrac{\tau_1}{\sqrt{L_iC_s}} \end{bmatrix} \cdot \begin{bmatrix} i_{Lm}(t_{on}) \\ v_{Cs}(t_{on}) \end{bmatrix} + \begin{bmatrix} \cos\dfrac{\tau_1}{\sqrt{L_iC_s}} & -1 \\ \sqrt{\dfrac{L_i}{C_s}}\sin\dfrac{\tau_1}{\sqrt{L_iC_s}} & 0 \end{bmatrix} I_1$$

$$(2.2.34)$$

where
$$\tau_1 = t - t_{on} \qquad (2.2.35)$$

and

$$i_{Lm}(t_{on}) = \frac{V_s}{L_1} t_{on} - I_1 \frac{L_1}{L_1} \qquad (2.2.36)$$

Also

$$v_{Lm}(t) = \frac{L_m}{L_1} v_{Cs}(t_{on}) \cos \frac{\tau_1}{\sqrt{L_1 C_s}} - (i_{Lm}(t_{on}) + I_1) \frac{L_m}{\sqrt{L_1 C_s}} \sin \frac{\tau_1}{\sqrt{L_1 C_s}} \qquad (2.2.37)$$

$$i_{L2}(t) = I_1 \qquad (2.2.38)$$

$$i_{L1}(t) = i_{Lm}(t) + I_1 \qquad (2.2.39)$$

$$v_Q(t) = V_s - v_{Cs}(t) \qquad (2.2.40)$$

$$v_{D2}(t) = V_s \qquad (2.2.41)$$

$$i_{Cs}(t) = -i_{L1}(t) = -i_{D1}(t) \qquad (2.2.42)$$

$$i_{D2}(t) = i_{Ls}(t) = 0 \qquad (2.2.43)$$

$$t_1 = \sqrt{L_1 C_s} \tan^{-1} \left[\frac{v_{Cs}(t_{on})}{i_{Lm}(t_{on}) + I_1} \sqrt{\frac{C_s}{L_1}} \right] \qquad (2.2.44)$$

Relationships (2.2.39)-(2.2.42) remain applicable through modes 4 and 5. For large values of L_m, the capacitor current is practically constant during this mode (Fig. 2.4), so that the equivalent circuit can be simplified as shown in Fig. 2.3 . In this case, the relevant voltages and currents expressions are found to be

$$i_{lm}(t) \approx i_{Lm}(t_{on}) \qquad (2.2.45)$$

$$v_{Cs}(t) \approx -\frac{i_{Lm}(t_{on}) + I_1}{C_s}(t - t_{on}) + v_{Cs}(t_{on}) \qquad (2.2.46)$$

and

$$t_1 \approx \frac{C_s v_{Cs}(t_{on})}{i_{Lm}(t_{on}) + I_1} + t_{on} \qquad (2.2.47)$$

b) *Interval $t_1 < t < t_2$; Mode 4*: In this mode the capacitor absorbs the energy stored in the leakage inductance's L_1, L_2, and some energy stored in L_m. The equivalent circuit is shown in Fig. 2.3. The expressions describing the respective voltages and currents become

$$\begin{bmatrix} i_{L1}(t) \\ v_{Cs}(t) \end{bmatrix} = \begin{bmatrix} \cos\dfrac{\tau_2}{\sqrt{L_t C_s}} & \sqrt{\dfrac{C_s}{L_t}}\sin\dfrac{\tau_2}{\sqrt{L_t C_s}} \\ -\sqrt{\dfrac{L_t}{C_s}}\sin\dfrac{\tau_2}{\sqrt{L_t C_s}} & \cos\dfrac{\tau_2}{\sqrt{L_t C_s}} \end{bmatrix} \cdot \begin{bmatrix} i_{L1}(t_1) \\ 0 \end{bmatrix} \qquad (2.2.48)$$

where

$$L_t = \frac{P_1}{L_0} \qquad (2.2.49)$$

$$\tau_2 = t - t_1 \qquad (2.2.50)$$

$$i_{L1}(t_1) = \sqrt{v_{Cs}^2(t_{on})\frac{C_s}{L_t} + (i_{Lm}(t_{on}) + I_1)^2} \qquad (2.2.51)$$

The independent state equation is

$$\frac{d}{d\tau_2}i_{Lm}(\tau_2) = \frac{L_2}{L_0}\frac{d}{d\tau_2}i_{L1}(\tau_2) \qquad (2.2.52)$$

Therefore,

$$i_{Lm}(t) = \frac{L_2}{L_0}(i_{Lm}(t_1) + I_1)\left(\cos\frac{t_2}{\sqrt{L_t C_s}} - 1\right) + i_{Lm}(t_1) \qquad (2.2.53)$$

$$v_{Lm}(t) = \frac{L_m L_2}{L_0}\frac{(i_{Lm}(t_1) + I_1)}{\sqrt{L_t C_s}}\sin\frac{\tau_2}{\sqrt{L_t C_s}} \qquad (2.2.54)$$

$$i_{L2}(t) = i_{L1}(t) - i_{Lm}(t) \qquad (2.2.55)$$

2-14

$$t_2 = \sqrt{L_t C_s} \cos^{-1}\left[1 - \frac{L_0 I_1}{L_m i_{L1}(t_1)}\right] + t_1 \qquad (2.2.56)$$

During this interval, the magnetizing current $i_{Lm}(t)$ remains practically constant (Fig. 2.4). therefore, the equivalent circuit can also be simplified as shown in Fig. 2.3. The relevant expressions become

$$i_{L1}(t) \approx (i_{Lm}(t_{on}) + I_1) \cos\frac{\tau_2}{\sqrt{(L_1 + L_2)C_s}} \qquad (2.2.57)$$

$$v_{Cs}(t) \approx -(i_{Lm}(t_{on}) + I_1)\sqrt{\frac{L_1 L_2}{C_s}} \cdot \sin\frac{\tau_2}{\sqrt{(L_1 + L_2)C_s}} \qquad (2.2.58)$$

The time t_2 at the end of the interval is determined by:

$$t_2 \approx \sqrt{(L_1 + L_2)C_s} \cos^{-1}\left[\frac{i_{Lm}(t_{on})}{(i_{Lm}(t_{on}) + I_1)}\right] + t_1 \qquad (2.2.59)$$

c) *Interval $t_2 < t < t_3$, Mode 5*: During this mode, the capacitor voltage $v_{Cs}(t)$ assumes its maximum negative value at $t = t_3$, at which time the magnetic transformer energy is zero. The equivalent circuit is shown in Fig. 2.3. The respective voltage and current expressions become

$$\begin{bmatrix} i_{Lm}(t) \\ v_{Cs}(t) \end{bmatrix} = \begin{bmatrix} \cos\dfrac{t_3}{\sqrt{L_i C_s}} & -\sqrt{\dfrac{C_s}{L_i}}\sin\dfrac{t_3}{\sqrt{L_i C_s}} \\ \sqrt{\dfrac{L_i}{C_s}}\sin\dfrac{t_3}{\sqrt{L_i C_s}} & \cos\dfrac{t_3}{\sqrt{L_i C_s}} \end{bmatrix} \cdot \begin{bmatrix} i_{Lm}(t_2) \\ v_{Cs}(t_2) \end{bmatrix} \qquad (2.2.60)$$

where

$$\tau_3 = t - t_2 \qquad (2.2.61)$$

$$i_{Lm}(t_2) = i_{L1}(t_1) - \frac{L_0}{L_m} I_1$$

(2.2.62)

$$v_{Cs}(t_2) = -\sqrt{(i_{Li}^2(t_1) - i_{Lm}^2(t_2))\frac{L_i}{C_s}}$$

(2.2.63)

and

$$v_{Lm}(t) = \frac{L_m}{L_i}\cos\frac{\tau_3}{\sqrt{L_iC_s}} - i_{Lm}(t_2)\frac{L_m}{\sqrt{L_iC_s}}\sin\frac{\tau_3}{\sqrt{L_iC_s}}$$

(2.2.64)

$$i_{L2}(t) = 0$$

(2.2.65)

$$i_{L1}(t) = i_{Lm}(t)$$

(2.2.66)

$$t_3 = \sqrt{L_iC_s}\tan^{-1}\left[-\frac{i_{Lm}(t_2)}{v_{Cs}(t_2)}\sqrt{\frac{L_i}{C_s}}\right] + t_2$$

(2.2.67)

d) Interval $t_3 < t < T$, Mode 6: The equivalent circuit is shown in Fig. 2.3 . The following voltage and current expressions have been obtained from (2.2.34) by applying the duality principle.

$$\begin{bmatrix} i_{Lm}(t) \\ v_{Cs}(t) \end{bmatrix} = \begin{bmatrix} \cos\dfrac{\tau_4}{\sqrt{L_aC_s}} & \sqrt{\dfrac{C_s}{L_a}}\sin\dfrac{\tau_4}{\sqrt{L_aC_s}} \\ -\sqrt{\dfrac{L_a}{C_s}}\sin\dfrac{\tau_4}{\sqrt{L_aC_s}} & \cos\dfrac{\tau_4}{\sqrt{L_aC_s}} \end{bmatrix} \cdot \begin{bmatrix} i_{Lm}(t_3) \\ v_{Cs}(t_3) \end{bmatrix} + \begin{bmatrix} \sqrt{\dfrac{C}{L}}\sin\dfrac{\tau_4}{\sqrt{L_aC_s}} & 0 \\ \cos\dfrac{\tau_4}{\sqrt{L_aC_s}} & -1 \end{bmatrix} V_s$$

(2.2.68)

where

$$\tau_4 = t - t_3$$

(2.2.69)

$$L_a = L_i + L_s$$

(2.2.70)

$$i_{Lm}(t_3) = 0$$

(2.2.71)

$$v_{Cs}(t_1) = \sqrt{i_{Lm}^2(t_2)\frac{L_1}{C_s} + v_{Cs}^2(t_2)\frac{L_0}{C_s}} \qquad (2.2.72)$$

and

$$v_{Lm}(t) = \frac{L_m}{L_a}(V_s + v_{Cs}(t_3))\cos\frac{\tau_4}{\sqrt{L_aC_s}} \qquad (2.2.73)$$

$$v_{L1}(t) = \frac{L1}{L_a}(V_s + v_{Cs}(t_3))\cos\frac{\tau_4}{\sqrt{L_aC_s}} \qquad (2.2.74)$$

$$v_Q(t) = V_s - v_{L1}(t) - v_{Lm}(t) \qquad (2.2.75)$$

$$v_{Di}(t) = v_{L1}(t) + v_{Lm}(t) - v_{Cs}(t) \qquad (2.2.76)$$

$$i_{L1}(t) = i_{Lm}(t) = i_{Ca}(t) = i_{L2}(t) = -i_{D2}(t) \qquad (2.2.77)$$

$$i_{D1}(t) = 0 \qquad (2.2.78)$$

Finally, regarding the simplified equivalent circuit for modes 3 and 4, an approximate expression can be found for $v_{Cs}(t_3)$.

$$v_{Cs}(t_3) \approx -\sqrt{(I_1^2 + 2I_1 i_{Lm}(t_{on}))\frac{L_1+L_2}{C_s} + i_{Lm}^2(t_{on})\frac{L_1 L_m}{C_s}} \qquad (2.2.79)$$

where

$$t_3 \approx \sqrt{L_i C_s}\tan^{-1}\left[\frac{i_{Lm}(t_{on})}{\sqrt{I_1^2 + 2I_1 i_{Lm}(t_{on})}}\sqrt{\frac{L_1+L_m}{L_1+L_2}}\right] + t_2 \qquad (2.2.80)$$

C. *Discussion*

1) Equation (2.2.79) shows that the maximum negative capacitor voltage $V_{Cs}(t_3)$ can be decreased by reducing L_1, L_2, $i_{Lm}(t_{on})$ (using a transformer with a large magnetizing inductance) and increasing C_s. Furthermore, $V_{Cs}(t_3)$ is dependent on the load current and is independent of $V_{Cs}(t_{on})$.

2) The available turn-off time to reset the transformer t_3-t_{on} (see 2.2.80) is reduced when the load current increases. This is so because the capacitor voltage changes faster during t_2-t_{on}.

3) The maximum transistor current during turn-on can be reduced by increasing L_s. However, the available turn-on time, t_{on}-t_b, decreases.

4) If t_3=T and $|V_{Cs}(t_3)| > V_s$, the recovered energy during a switching period can be calculated as follows.

a) The energy returned to the source is

$$E_{RV} = \frac{1}{2} C_s [|V_{Cs}(t_3)| - V_s]^2$$

b) The energy delivered to the load is

$$E_{RL} = \frac{1}{2} C_s (V_s)^2$$

Fig. 2.4 illustrates also that, with these conditions, the magnetizing current at t=T is negative, e.g., if E_{Lm} denotes the magnetizing stored energy, then

$$i_{Lm}(t_{on})\big|_{t_3 = T} > i_{Lm}(t_{on})\big|_{t_3 < T}$$

Hence

$$E_{Lm}(t_3 = T) > E_{Lm}(t_3 < T)$$

Furthermore, if E_{L1} denotes the energy stored in leakage inductance then

$$E_{RL} > E_{L1} \quad \text{if} \quad \sqrt{\frac{C_s}{L_1 + L_2}} > \frac{I_1}{V_s}$$

Therefore, regarding the last two expressions one can conclude that

$$V_{Cs}(t_3 = T)\big|_{I_1=0} \;\rangle\; V_{Cs}(t_3 = T)\big|_{I_1\rangle 0} \;\rangle\; V_{Cs}(t_3 \langle T)\big|_{I_1\rangle 0}$$

Which means that the maximum voltage across the capacitor occurs under light load and decreases as the load increases. In fact, because the magnetizing current becomes negative with $t_3 < T$ the total energy stored in the transformer decreases.

5) If the resonant frequency, $1/\sqrt{L_e C_s}$, is large as compared with the switching frequency (no-resonant mode), the elements of the transition matrix (2.2.6) can be calculated as follows:

$$\sin\frac{1}{\sqrt{L_e C_s}}\tau \approx \frac{1}{\sqrt{L_e C_s}}\tau$$

$$\cos\frac{1}{\sqrt{L_e C_s}}\tau \approx 1$$

2.2.3   Design Procedure and Example

A design procedure is presented in this section. The exact expressions obtained in Section 2.2.3 are used. The design procedure is as follows.

1) The voltage and current equations are normalized and expressed in terms of design parameters. These parameters are the circuit components, the load current, and the duty cycle.

2) The steady-state solutions for resetting the transformer at $t_3 = T$ are found. By using these solutions, normalized operating-limit curves are obtained for different design parameter values.

3) Finally, the operating-limit curves together with a complementary set of normalized design equations are used to design the circuit.

A.   Per-Unit Values and Design Parameters

To express the equations presented in Section 2.2.3 in per unit (p.u.) form, the following quantities are chosen as respective base values.

$$V_b \quad = V_s \qquad \text{V}$$

$$I_b \quad = I_1 \qquad \text{A}$$

$$Z_b \quad = V_b/I_b \qquad \Omega$$

$$W_b \quad = 2\pi f_b \qquad \text{rad/s}$$

$$L_b \quad = V_b/I_b W_b \quad \text{H}$$

$$C_b \quad = I_b/V_b W_b \quad \text{F}$$

Hereafter, the capital letters denote p.u. values and the following design parameters will be used.

Leakage Inductance Factor :

$$K_1 = L_1/L_m \tag{2.2.81}$$

$$K_2 = L_2/L_m \tag{2.2.82}$$

Magnetizing Current at t = t_{on} :

$$I_{Lm}(\delta) \qquad \text{(from (2.2.36) in p.u.)}$$

Load Transformer Current Ratio :

$$K_i = \frac{I_1}{I_{Lm}(\delta)} \tag{2.2.83}$$

Base Voltage :

$$V_r = I_{Lm}(\delta)\sqrt{\frac{L_m}{C_s}}$$ (2.2.84)

Duty Cycle :

$$\delta = \frac{t_{on}}{T} \quad (with\ t_3 = T \ and\ \delta = \delta_{max})$$ (2.2.85)

B. Operating-Limit Design Curves

With $t_3 = T$ ($\delta = \delta_{max}$) and under steady operating conditions, the circuit

(Fig. 2.1) may be characterized by using the following set of normalized functions

$$V_{Cs}(1) = f\ (V_{Cs}(\delta),\ V_r,\ K_i,\ K_1,\ K_2)$$ (2.2.86)

$$\delta = f\ (V_{Cs}(\delta),\ V_{Cs}(1),\ K_i,\ K_1,\ K_2)$$ (2.2.87)

$$V_r = f\ (\delta,\ K_i,\ K_1,\ K_2)$$ (2.2.88)

Also from (2.2.86),

$$V_r = f\ (V_{Cs}(\delta),\ V_{Cs}(1),\ K_i,\ K_1,\ K_2)$$ (2.2.89)

In addition, by using (2.2.36), the function (2.2.88) yields

$$V_r = \frac{2\pi\delta}{\sqrt{L_m C_s}}\ \frac{1}{K_1(K_i+1)+1}$$ (2.2.90)

The function (2.2.86) and (2.2.87) are derived by using (2.2.51), (2.2.62), (2.2.63),

(2.2.72), and (2.2.44), (2.2.51), (2.2.56), (2.2.62), (2.2.67), respectively. To

illustrate the effect of the leakage inductances, the magnetizing and the load

currents, different solutions are obtained for $K_1 = K_2 = 0$ and $K_1 = K_2 > 0$ (0.0008).

1) $K_1 = K_2 = 0$: The design functions (2.2.87) and (2.2.89) can be shown to be:

2-21

a) *If* $V_{Cs}(\delta) = V_{Cs}(1) < 1,$

$$V_r = -\frac{K_i}{K_i + 0.5}V_{Cs}(1), \quad K_i > 1 \tag{2.2.91}$$

$$\delta = \frac{V_r}{V_r + \dfrac{\pi}{2} + \tan^{-1}\left[\dfrac{V_{Cs}(\delta)}{(K_i + 1)V_r}\right]} \tag{2.2.92}$$

b) *If* $V_{Cs}(\delta) = 1, -V_{Cs}(1) > 1,$

$$V_r = -\frac{0.5K_i}{K_i + 0.5}V_{Cs}(1) + \sqrt{\left[\frac{K_i}{K_i + 0.5}V_{Cs}(1)\right]^2 + \left[\frac{(V_{Cs}(1))^2 - 1}{K_i + 0.5}\right]^2} \tag{2.2.93}$$

$$\delta = \frac{V_r}{V_r + \dfrac{\pi}{2} + \tan^{-1}\left[\dfrac{1}{(K_i + 1)V_r}\right]} \tag{2.2.94}$$

The respective operating-limit curves are shown in Fig. 2.5(a) and (b). To reduce the capacitor voltage under rated load, the ideal K_i value has to be ≥ 20, i.e., maximum magnetizing current $i_{Lm}(t_{on}) \leq 0.05 I_L$. Fig. 2.5(b) depicts the time restriction required to obtain the flux balancing condition at $t_3 = T$. The equal-volts-seconds area to L_m is achieved earlier as K_i increases. At 50 percent of duty cycle and with $K_i \geq 20$, the maximum negative capacitor voltage is 1.55 p.u. (2.55 across the switch). With the same duty cycle but with $K_i = 0$ (open circuit) this voltage becomes 2.25 p.u. (3.25 p.u. across the switch)

2) $K_1 = K_2 > 0$: Similarly, design functions have been obtained for this case. The respective operating-limit curves are shown in Fig. 2.6 (a) and (b). As illustrated

in Fig. 2.6 (b), increasing the load current increases the rate of voltage change across the snubber capacitor C_s. So, the available turn-off time needed to achieve the transformer flux balancing condition under rating load, is larger than with $K_1=K_2=0$. For this case, at 50% of duty cycle and with $Ki \geq 20$, the maximum capacitor voltage decreases to 1.25 p.u. (2.25 p.u. across the switch).

C.   Design Equations

The maximum voltage $\hat{V}$, maximum currents $\hat{I}$, and the element values can be calculated by using the normalized design equations outlined hereafter in **Table 2.2-I**.

<div align="center">

Table 2.2-I
Design Equations

</div>

$I_{Lm}(\delta) = \dfrac{I_1}{K_1}$	$I_o = nI_1$
$\hat{I}_{Cs} \approx I_1 + I_{Lm}(\delta)$	$\hat{I}_{Lm} \approx I_{Lm}(\delta)$
$\hat{I}_{Ls} = \sqrt{\dfrac{C_s}{L_s}}(-V_{Cs}(1))$	$\hat{I}_{D1} = \hat{I}_{Cs}$
$\hat{I}_Q \approx I_1 + \hat{I}_{Ls}$	$\hat{I}_{D2} = \hat{I}_{Ls}$
$\hat{V}_{Cs} = -V_{cs}(1)$	$\hat{V}_{Lm} \approx -V_{cs}(1)$
$\hat{V}_{D2} = \hat{V}_{D1} = \hat{V}_Q$	$\hat{V}_Q = -V_{Cs}(1) + 1$
$L_m = \dfrac{2\pi\delta}{I_{Lm}(\delta)(K_1(1+K_i)+1)}$	$C_s = \left[\dfrac{I_{Lm}(\delta)}{V_r}\right]L_m$
$L_s = \dfrac{(2\pi\delta_{min})^2}{C_x}$	$\delta = \delta_{max}$
$\delta_{min} \approx \dfrac{t_b}{T}$	$t_b = \pi\sqrt{L_r C_s}$
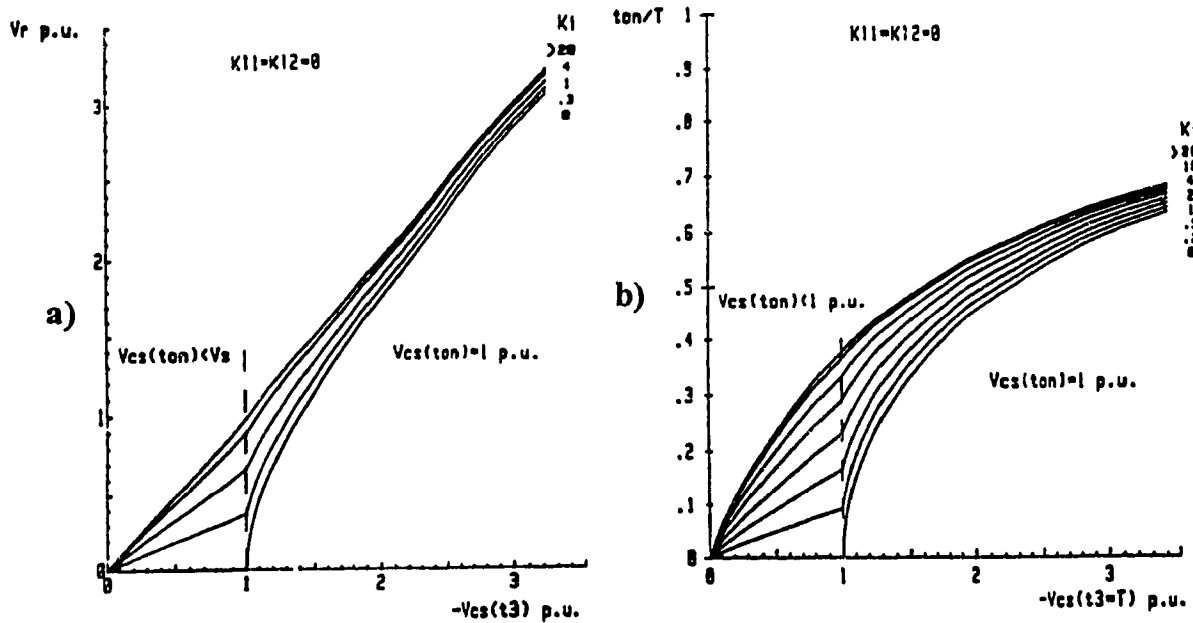
Figure 2.5 Limit Operating Curves; Current Factor Ki as a parameter; K11=K12=0. a) Voltage Vr versus maximum capacitor voltage $V_{cs}(t3)$. b) $(ton/T)_{max}=\delta_{max}$ versus maximum capacitor voltage $V_{cs}(t3)$.
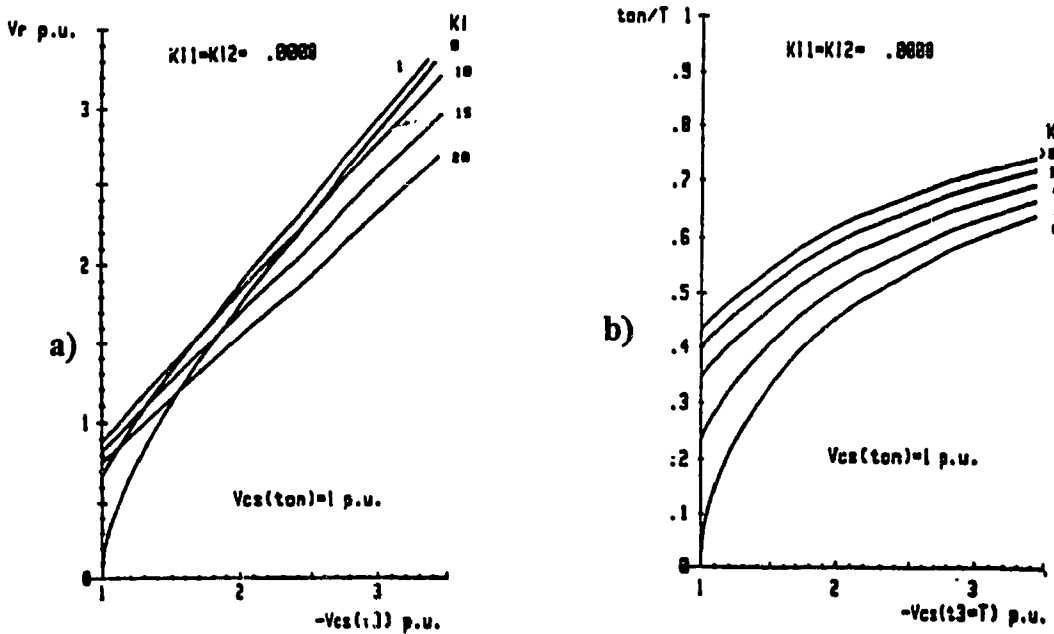
Figure 2.6 Limit Operating Curves; Current Factor Ki as a parameter; K11=K12=0.0008 a) Voltage Vr versus maximum capacitor voltage $V_{cs}(t3)$. b) $(ton/T)_{max}=\delta_{max}$ versus maximum capacitor voltage $V_{cs}(t3)$.

D.   *Design example*

In this section a design example is provided. Experimental verification follows in Section 2.2.4. The Single-Switch Forward converter shown in Fig. 2.1 is designed regarding the following specifications:

Output power: P_0 = 1.0 kW

Source voltage: V_s = 150 V

Switching frequency: f_s = 20 kHz

Duty cycle: δ_{max} = 0.5, $\delta_{min} = 0.1$

Transformer ratio: n   = 1.33

Leakage factor: K_1 = $K_2 = 0.0008$

The respective base values are

V_b = 150 V

I_b = 15 A

w_b = $2\pi f$ rad/s

C_b = 0.796 μF

L_b = 0.0795 mH

The maximum switch voltage is determined with light load. Therefore, from Fig. 2.6 (b), with $\delta_{max} = 0.5$ and $K_i = 0$, it is found that

$$-V_{Cs}(t_3) = -V_{Cs}(1) = 2.25$$

From Fig. 2.6 (a), with $K_i = 0$ and $-V_{Cs}(t_3) = 2.25$, it is seen that

$$V_r = 2.01$$

The maximum current values are calculated at maximum duty cycle with maximum load. The maximum magnetizing current ($I_{Lm}(\delta_{max})$) is assumed to be 15 % of the maximum load current. The design is summarized in **Table 2.2-II.**

2.2.4 Experimental Results

To establish the feasibility of the proposed converter topology and to verify the selected theoretical results, a 1-kW prototype unit operating at 20 kHz switching frequency was built and tested. The transformer uses an EE ferrite core with a small air gap, the magnetizing inductance is 1800 µH, and the leakage inductance is 2 µH (primary). The power switch is a Powerex KS524505, 50A/600V, single darlington BJT module.

The **Table 2.2-II** compares the theoretical and the experimental values. It is shown that the experimental values are in some extension lower than the theoretical values. These is an expected result due to the assumption of ideal circuit components in the analysis and the practical component values selected to implement the experimental setup.

Key experimental waveforms for a quasi-resonant and a non resonant mode of operation are shown in Figs. 2.7 (I), 2.7 (II), 2.8 and 2.9, respectively The resulting experimental waveforms are in close agreement with the analytical waveforms shown in Fig. 2.4. In particular, Figs. 2.7 (I) and 2.7 (II) illustrate a set

Table 2.2-II

Summary of the Design Example
Vs=150 V, Po=1 kW, Vo=50 V, fs=20 kHz

Variable	Design			Experiment	
	p.u. Value	Actual Value			
n	-	1.33		1.33	
L_m	20.944	1665.000	μH	1800	μH
C_s	0.093	0.074	μF	0.100	μF
L_s	0.430	34.190	μH	20.000	μH
$\hat{I}_1$	1.000	15.000	A	15.900	A
$\hat{I}_o$	1.300	25.000	A	25.000	A
$\hat{I}_{Lm}$	0.150	2.250	A	2.000	A
$\hat{I}_{Cs}$	1.150	17.250	A	15.500	A
$\hat{I}_{D1}$	1.150	17.250	A	15.500	A
$\hat{I}_{Ls}$	1.046	15.696	A	12.500	A
$\hat{I}_{D2}$	1.046	15.696	A	12.500	A
$\hat{I}_Q$	2.046	30.690	A	26.100	A
$\hat{V}_Q$	2.250	487.500	V	440.000	V
$\hat{V}_{Cs}$	2.250	337.500	V	290.000	V
$\hat{V}_{Lm}$	3.250	337.500	V	-	
$\hat{V}_{D1}$	3.250	487.500	V	440.000	V
$\hat{V}_{D2}$	3.250	487.500	V	440.000	V

Maximum voltage are with light load, e.g. 4 A. Maximum current are at rated load, e.g. 20 A

of experimental converter voltage and current waveforms for light load (4 A) and rated load (20 A). As predicted, the maximum voltage in the switch was higher at light load than at rated load (e.g. 440 V and 400 V respectively). It is also verified that the switch voltage stresses and the DC magnetizing current decreases as the

load increases. In addition, as was predicted in the discussion of 2.2.3 C., when the load increases the maximum switch voltage is achieved early, e.g. at a time $t_3 <$ T (flux reset condition, see Fig. 2.4).

Figs. 2.7. (I) and (II) (c) and (d) illustrate the snubber capacitor voltage and current. It is shown how the resonant LC circuit takes the energy from the transformer inductances during the turn-off increasing the capacitor voltage. Them how this voltage is inverted during the turn-on until it gets clamped to the input voltage (150 V).

Figs. 2.7 (I) and (II) (e) show the resonance current through the Ls inductance during the turn-on and Figs. 2.7 (I) and (II) (e) (f) show the input converter current with the energy recovery "notch" during the turn-on. (energy flowing to the input source).

Figs. 2.8 (a) and (b) depict the collector-emitter voltage and current during turn-off and turn-on and these prove that the switching losses are minimized (ZVS). For load power variation from 0.2 to 1 p.u., the experimental measured efficiency was higher than 93%. It is observed a high frequency oscillation during the turn-off transition, mainly due to the resonance between the parasitic inductance and the parasitic capacitance of the diodes D1, D2 of the LC circuit.. These oscillations can be minimized with a better layout of the power circuit, by

using schottkys diodes in the output rectifier and ultrafast soft-recovery diodes in the LC circuit.

Finally, Fig. 2.9 illustrates experimental results using a large capacitor C_s (non resonant mode of operation) and a resonant inductor L_s equal to the magnetizing inductance L_m. In particular, Fig. 2.9 (a) reveals that the collector-emitter voltage is now reduced to two times V_s. However, in this mode of operation the turn-off losses increase and the HF transformer shown saturation when the duty cycle is changed.
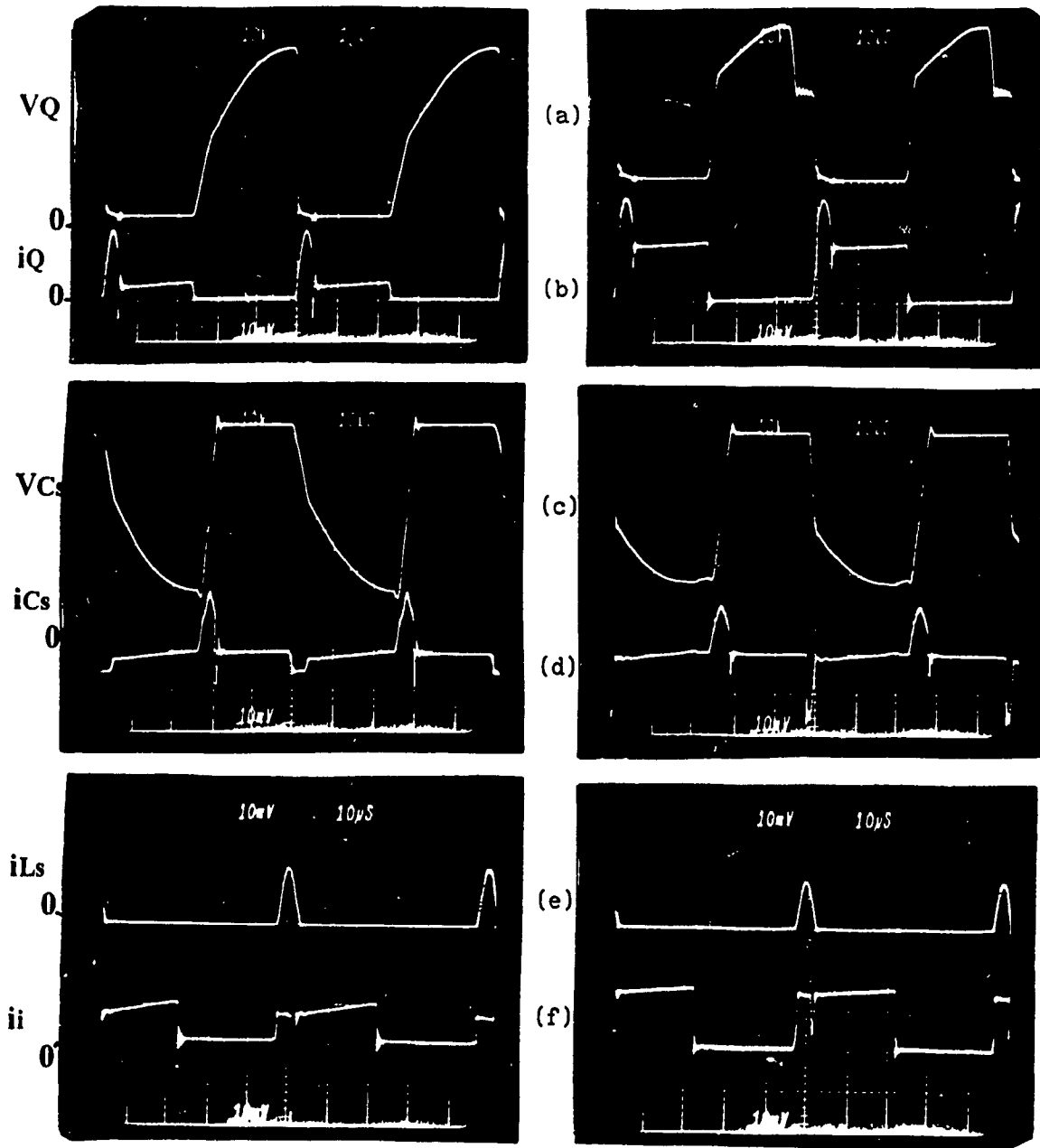
(I) Io=4 Amp   (II) Io=20 Amp

Figure 2.7   Experimental Converter Voltage and Current Waveforms
Ls=20μH, Lm=1800μH, Cs=0.1μF, Vs=150 V, Vo=50 (20 A).V, D=50%
Voltage scale 100V/Div., current scale 10 Amp./Div. Time scale 10μs/Div.
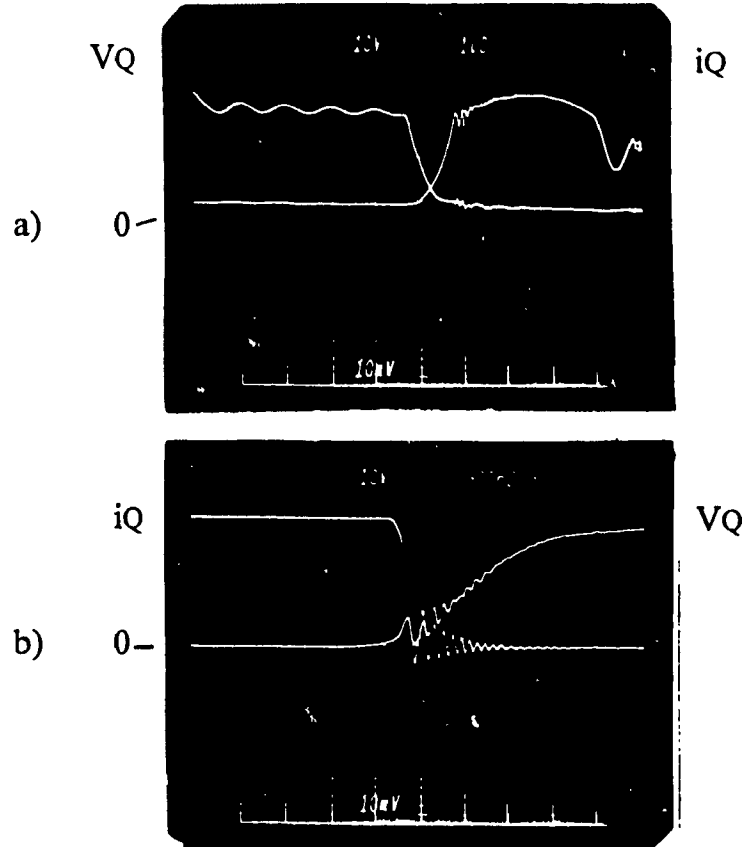
Figure 2.8 Transistor Losses During a Switching Period
a) Turn-on: time scale 1 μs/Div., current scale 10 Amp./Div b) Turn-off: time scale 500 ns/Div., current scale 20 Amp./Div. Voltage scale 100 V/Div.
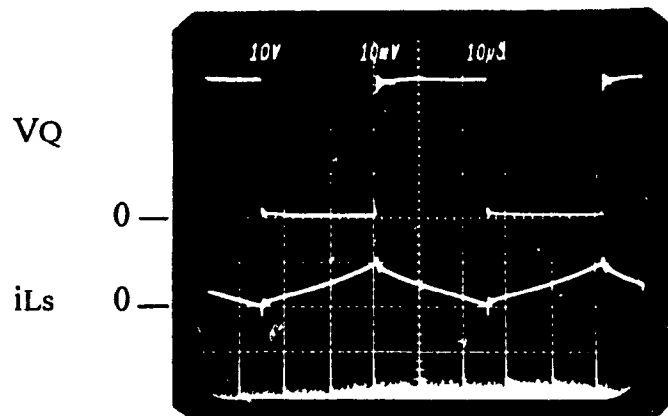
Figure 2.9 Experimental Waveforms in a Non-resonant Mode
Voltage scale: 100v/Div., Current scale 2 Amp./Div., Time scale: 10μs/Div.

2-31

2.3 Topology II: Complementary-Switch and Active Snubber Circuit

The forward single-switch converters with a demagnetizing winding are widely used in low power applications ($P_o < 1$ W). For medium and high power applications, the design of this HF transformer is more difficult and expensive when it must be designed for higher voltage, frequency and extended duty cycle operation. A typical solution for medium power applications is the two-switch forward converter shown in Fig. 2.10. However, it has the following disadvantages:

1) It requires two main switches and two transformer flux reset diodes.

2) It requires one isolated gate driver

3) The associated HF transformer operates with a DC flux component.

4) It cannot operate with more than a 50% duty cycle.

5) Because of the parasitic inductance of the DC bus, special shunt capacitors are always required to prevent reverse biased-second breakdown.

The proposed single ended forward converter topology shown in Fig. 2.11 needs only one main switch and one auxiliary switch, and it has none of the aforementioned disadvantages. Moreover, because there is only one high-power switch in series with the source (i.e., IGBT), this topology yields less conduction losses and therefore better efficiency. One intrinsic disadvantage, however, is that the voltage rating of these two switches, depending on the maximum operating duty cycle, input voltage, and load current variation. On the other hand, step
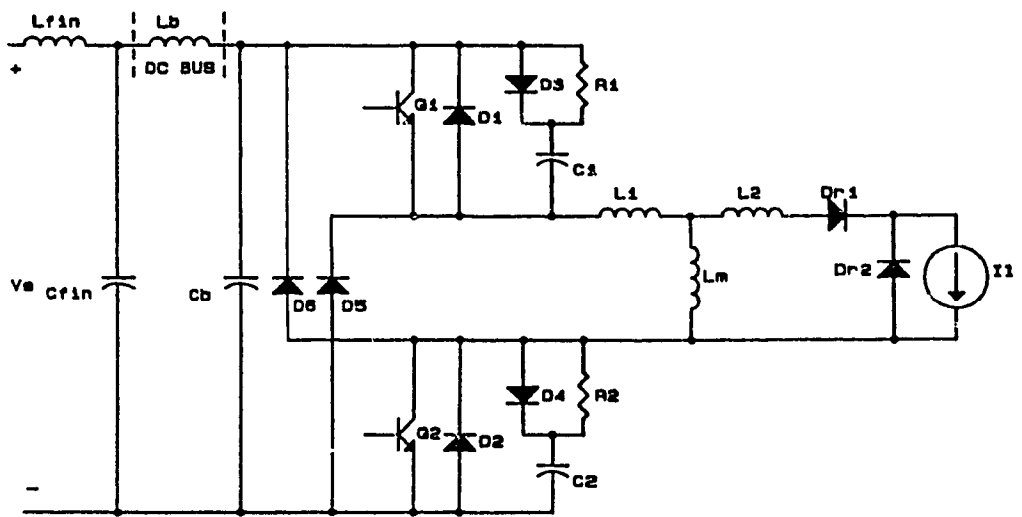
Figure 2.10 Typical Two-Switch Single-Ended Forward converter
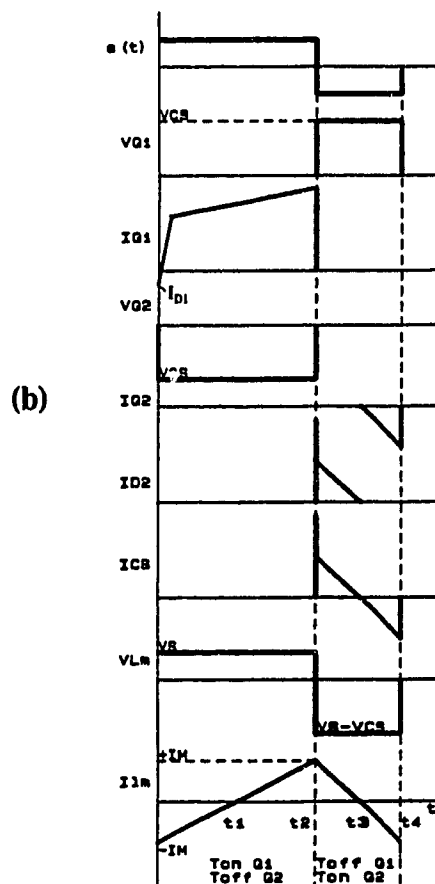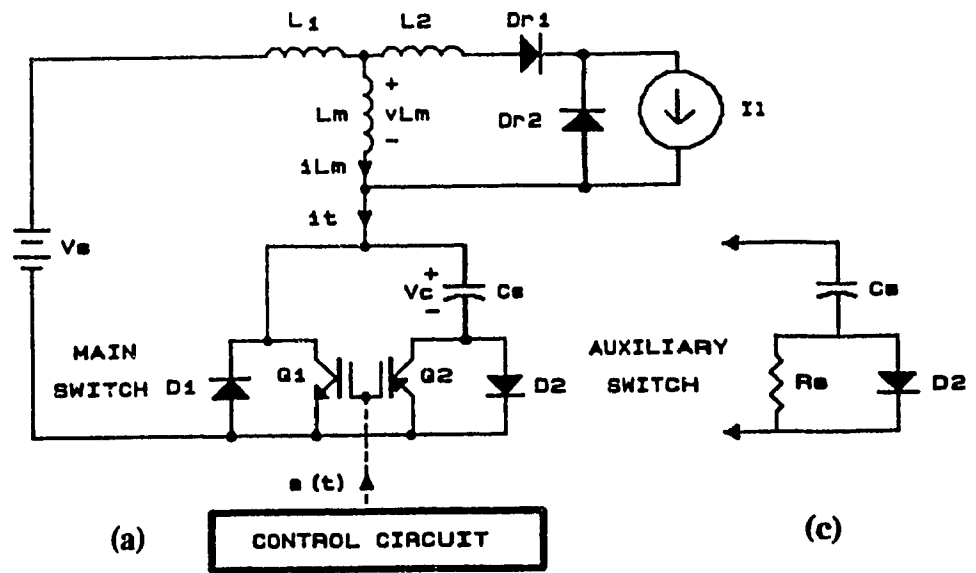
Figure 2.11 The Proposed Forward Converter with a Complementary Switch. a) Simplified Power Circuit. b) Ideal Waveforms. c) Alternative with a DRC Snubber Circuit

change in the duty cycle may produce low-frequency oscillations in the magnetizing current, which can saturate the HF transformer core The oscillation problem is solved if a current mode type of control is used with the current sensor in series with the main switch.

The principle of transformer flux balancing through the use of a magnetizing-energy-trap capacitor and an auxiliary switch was proposed in references [1] and [15]. The circuit realization presented in [15] has the disadvantage of not providing a means for recovering the energy stored in the parasitic circuit inductances. Several schemes, which could solve this problem, are discussed in [1], but no analysis and design procedures have been reported. One important feature no identified before is that, due to the negative magnetizing current, this topology provides ZVS during the turn on and turn off switching intervals. This is an important advantage as compared with the previous topology with the LC snubber circuit which can not provides ZVS during the turn-on.

The performance of the proposed topology depends mainly on the capacitor C_s value. With a large C_s value, the *capacitor voltage* during turn off (V_c) becomes practically ripple free, thus emulating a DC voltage source. This topology, therefore, works in a *non resonant* mode of operation. In this mode, the switches have lower voltage stresses, but the time response is slow. With a small

C_s value, the initial turn-off capacitor voltage V_C becomes *equal to the input* voltage V_s, and the topology now works in a *quasi resonant* mode of operation. The circuit has a faster transient response, but the voltage stresses across the switches increase to more than twice the bus voltage.

In both modes of operation discussed above, the capacitor C_s stores all the reactive energy of the parasitic, leakage, and magnetizing inductances and protects the switches from switching over voltages. In addition, the capacitor blocks the DC component of the leakage and magnetizing inductance currents, which means that the energy stored during the turn-on is sent back from the capacitor to the source through the same inductances during the turn off, thus keeping them magnetically balanced. Moreover, energy associated with stray circuit inductances is also returned to the DC source.

In both modes of operation, a very low-power auxiliary switch can be used to conduct the reverse current. This is because for a practical forward converter, the RMS value of this current is very small (almost magnetizing current) compared with the rated load current. However, the maximum voltage of the auxiliary switch is equal to the main switch. Also, the peak current of the diode D2 is almost equal to the load current, but only during a very short interval at the beginning of turn-off (see Fig. 2.11 b)).

The transformer flux balancing condition with zero DC component can also be achieved if the auxiliary switch is replaced by a suitable resistor R_s (Fig. 2.11 (c)). This is a DRC snubber circuit but is proposed here for the first time to operate in a *quasi-resonant* mode to reset the transformer core and to minimize the losses during turn-on due to parasitic capacitance of the switch. The capacitor C_s is designed to resonates with the magnetizing inductance of the transformer. Similar to the conventional DRC snubber, the circuit provides ZVS during the turn-off, although the turn-on losses associated with R_s and the main switch increase since the capacitor Cs need to be discharged each time the main switch is turned on.

This section presents the analysis of the DC/DC converter shown in Fig. 2.11. The active snubber circuit is analyzed operating in a non-resonant and quasi-resonant mode. The DRC snubber circuit is analyzed operating in a quasi-resonant mode. Design procedures are proposed and illustrated by examples. Finally, to verify the theory, experimental results from a 1 kW, 20 kHz prototype unit are presented.

2.3.1 Description and Principles of Operation

The simplified circuit diagram is shown in Fig. 2.11 (a). It includes the supply voltage V_s, the HF transformer magnetizing inductance L_m, the parasitic and leakage inductances L_1 and L_2, the forward and free-wheeling HF rectifier diodes D_{r1} and D_{r2}, the load current (through the rectifier filter inductor) as current

source I_1, the main high-power switch Q_1 and its integral diode D_1, the auxiliary low-power switch Q_2 and its integral diode D_2, the flux balancing and energy recovery capacitor C_s, and the switch control logic circuit.

The waveforms shown in Fig. 2.11 (b) illustrate the steady-state *non resonant mode* of operation, assuming ideal switches and neglecting the effects of L_1 and L_2. The switches Q_1 and Q_2 are operated according to the control signal s(t). At time zero, the converter ON interval begins by turning switch Q_1 on and Q_2 off. During this period, V_s is applied across L_m, causing the magnetic flux of the transformer's core to change with the time, as dictated by Faraday's law. The concurrent change in the magnetizing current is given by

$$\Delta I_{m_{on}} = V_s \frac{t_2}{L_m} \tag{2.3.1}$$

At time t_2 (Fig. 2.11 (b)), the main switch Q_1 is turned off, and the auxiliary switch Q_2 is turned on, initiating the OFF converter interval. The load current is transferred to diode D_{r2}. The total current $i_t(t)$ is equal to the magnetizing current i_{Lm}, and it is positive ($i_{Lm}(t_2) = + I_M$). Thus, $i_t(t)$ flows through D_2 and C_s. The voltage across the switch is clamped to the capacitor voltage V_c. The voltage across the magnetizing inductance L_m is now the difference between V_s and V_c. It has a negative value so that the slope of the magnetizing current is also negative. During the interval $t_3 > t > t_2$ (Fig. 2.11 (b)), the magnetizing current charges the capacitor C_s, and the associated energy is gradually transferred from the

transformer to the capacitor. During the interval $t_4 > t > t_3$, $i_t(t) = i_{Lm}(t)$ (Fig. 2.11 (b)), and it becomes negative. Thus, $i_t(t)$ flows via Q_2 and discharges C_s. The stored energy is now transferred back from capacitor C_s to the transformer core and the input source via Q_2. Since V_c remains practically constant during the OFF period, the magnetizing current changes linearly. The total change in the current is given by

$$\Delta I_{m_{off}} = (V_c - V_s)\frac{(t_4 - t_2)}{L_m} \qquad (2.3.2)$$

By equating the magnitude of the current change during the ON period (2.3.1) to the corresponding current change during the OFF period (2.3.2), it follows that

$$V_c = V_s \frac{1}{1 - \delta} \qquad (2.3.3)$$

where δ is the duty cycle which is given by

$$\delta = \frac{t_2}{t_4} \qquad (2.3.4)$$

Therefore, in order to maintain practically zero DC magnetizing current when the duty cycle changes, the capacitor voltage V_c (t3) will be adjusted automatically to reset the transformer at $t = t_4$.

2.3.2 Power Circuit Analysis

This section presents the analysis for both topologies shown in Fig. 2.11 (a). It is assumed ideal switches, a lossless transformer operating in linear flux mode,

but with parasitic-leakage inductances L_1 and L_2. The analysis is concerned with the identification of the topological modes (TM) during a switching cycle, the solution of the state equations in each TM, the operating modes and the transformer flux balancing conditions.

A.   State Equations

The analytical expressions describing the converter currents and voltages for each mode of operation are obtained by solving the following independent state equations:

Turn on

$$\frac{d}{dt} v_{Cs}(t) = \frac{-1}{RC_s} v_{Cs} \quad \text{(only DRC snubber circuit)} \tag{2.3.5}$$

$$\frac{d}{d\tau} i_L(\tau) = \frac{V}{L_e} \tag{2.3.6}$$

Turn off

$$\frac{d}{d\tau} \begin{bmatrix} i_L(\tau) \\ v_{Cs}(\tau) \end{bmatrix} = \begin{bmatrix} \dfrac{-R}{L_e} & \dfrac{-1}{L_e} \\ \dfrac{1}{C_s} & 0 \end{bmatrix} \cdot \begin{bmatrix} i_L(\tau) \\ v_{Cs}(\tau) \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L_e} \\ 0 \end{bmatrix} V_s, \quad \begin{bmatrix} i_L(0) \\ v_{Cs}(0) \end{bmatrix} \tag{2.3.7}$$

where L_e is the equivalent circuit inductance seen by the source and the capacitor C_s and R must be zero for the case of the active snubber circuit operating in both a *non-resonant* mode and a *quasi-resonant* mode. Equation (2.3.5) represents the

discharge of the capacitor C_s during turn on when a DRC snubber circuit is used is used.

B. Voltages and Currents solutions

The Fig. 2.12 shows the respective TM's identified in sequence during a switching cycle. The Fig. 2.13 illustrates the sequences of topological mode that occur in each mode of operation for the two topologies. For the non-resonant mode the TM sequence is always the same. However, for the quasi-resonant mode (active or DRC snubber circuit) the TM sequence could be different depend on the initial voltage of the capacitor Vc at the beginning of the turn-off cycle.

The voltage/current solutions for (2.3.6) and (2.3.7) are found for the DRC snubber circuit (more general case) operating in a quasi-resonant mode. These solutions are presented below.

Turn on

Mode 1 : $0 < t < t_1$, D_{r1} on, D_{r2} on, Q_1 on, Q_2 off, D_2 off

The resulting voltage and current equations are:

$$i_{L1}(t) = i_{L1}(0) + \frac{t}{L_{e1}} V_s \qquad (2.3.8)$$

$$v_{Cs}(t) = v_{Cs}(0) e^{\frac{-1}{RC_s}} \quad 0 < t < t_{on} \qquad (2.3.9)$$

$$i_{Cs}(t) = \frac{v_{Cs}(t)}{R} \quad 0 < t < t_{on} \qquad (2.3.10)$$

where

$$t_1 = \frac{P_1}{L_m} \frac{(I_1 - i_{L2}(0))}{V_s} \qquad (2.2.11)$$

$$L_s = L_2 + L_m \qquad (2.3.12)$$

$$P_1 = L_1 L_m + L_1 L_2 + L_2 L_m \qquad (2.3.13)$$

$$L_{e1} = \frac{P_1}{L_s} \qquad (2.3.14)$$

Mode 2 : $t_1 < t < t_{on}$, D_{r1} *on,* D_{r2} *off,* Q_1 *on,* D_2 *off*

$$i_{L1}(t) = i_{L1}(t_1) + \frac{\tau_1}{L_p} V_s \qquad (2.3.15)$$

where

$$L_p = L_1 + L_m \qquad (2.3.16)$$

$$\tau_1 = t - t_1 \qquad (2.3.17)$$

Turn off

Mode 3 : $t_{on} < t < t_2$, D_{r1} *on.* D_{r2} *off,* Q_1 *off,* D_2 *on*

$$i_{L1}(t) = i_{L1}(t_{on}) \cos\omega_1 \tau_2 + \frac{1}{Z_1}(V_s - v_{Cs}(t_{on}))\sin\omega_1 \tau_2 \qquad (2.3.18)$$

$$v_{Cs}(t) = i_{L1}(t_{on}) Z_1 \sin\omega_1 \tau_2 - (V_s - v_{Cs}(t_{on}))\cos\omega_1 \tau_2 + V_s \qquad (2.3.19)$$

where

$$\tau_2 = t - t_{on} \qquad (2.3.20)$$

$$t_2 = \frac{1}{\omega_1}\tan^{-1}\left[\frac{V_s - v_{Cs}(t_{on})}{i_{L1}(t_{on})Z_1}\right] + t_{on} \qquad (2.3.21)$$

$$Z_1 \sqrt{\frac{L_p}{C_s}} \qquad (2.3.22)$$

2-42
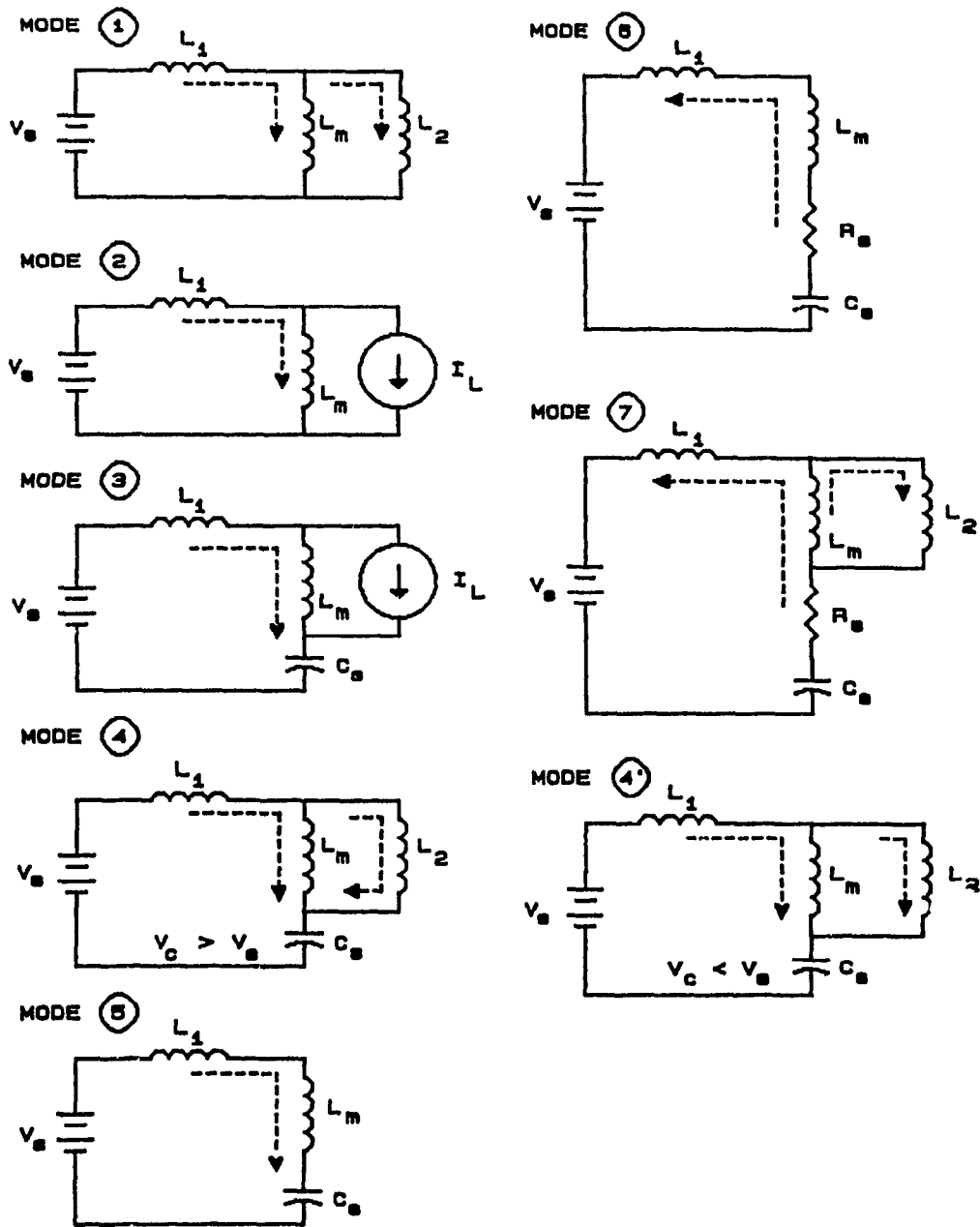
Figure 2.12 Topological Modes in a Quasi-resonant Mode with a DRC Snubber
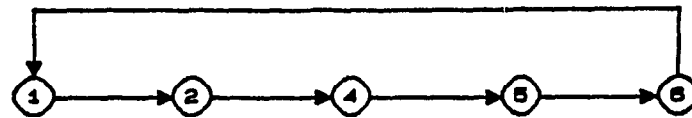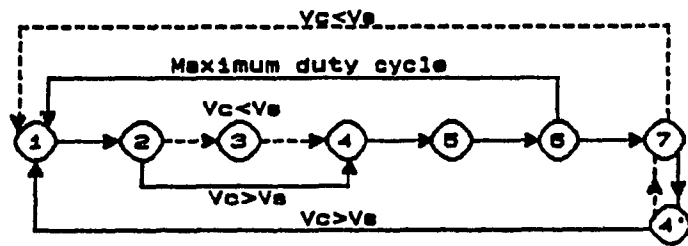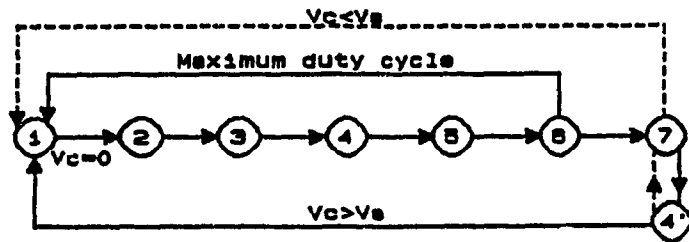
Figure 2.13 Different Modes of Operation a) Active Snubber, Non Resonant Mode. b) Active Snubber, Quasi-Resonant Mode c) DRC Snubber, Quasi-Resonant Mode.

$$\omega_1 = \sqrt{\frac{1}{C_s L_p}} \tag{2.3.23}$$

Mode 4 : $t_2 < t < t_3$, D_{r1} *on,* D_{r2} *on,* Q_1 *off,* D_2 *on*

$$i_{L1}(t) = i_{L1}(t_2) \cos\omega_2 \tau_3 + \frac{1}{Z_2}(V_s - v_{Cs}(t_2))\sin\omega_2 \tau_3 \tag{2.3.24}$$

$$v_{Cs}(t) = i_{L1}(t_2)Z_2 \sin\omega_2 \tau_3 - (V_s - v_{Cs}(t_2))\cos\omega_2 \tau_3 + V_s \tag{2.3.25}$$

where

$$\tau_3 = t - t_2 \tag{2.3.26}$$

$$Z_2 = \sqrt{\frac{L_{el}}{C_s}} \tag{2.3.27}$$

and

$$Z_2 \approx Z_1 \sqrt{\frac{L_1 + L_2}{L_m}} \tag{2.3.28}$$

$$\omega_2 = \frac{1}{\sqrt{C_s L_{el}}} \tag{2.3.29}$$

$$t_3 = \frac{1}{\omega_2}\sin^{-1}\left[\frac{K_1}{K_2}\right] - \tan^{-1}\left[\frac{i_{L1}(t_2)Z_2}{V_s - v_{Cs}(t_2)}\right] + t_2 \tag{2.3.30}$$

$$K_1 = \left(i_{L1}(t_2) - i_{L2}(t_2)\frac{L_s}{L_m}\right)Z_2 \tag{2.3.31}$$

$$K_2 = \sqrt{(Z_2 i_{L1}(t_2))^2 + (V_s - v_{Cs}(t_2))^2} \tag{2.3.32}$$

Mode 5 : $t_3 < t < t_4$, D_{r1} *off,* D_{r2} *off,* Q_1 *off,* D_2 *on*

$$i_{L1}(t) = i_{L1}(t_3) \cos\omega_1 \tau_4 + \frac{1}{Z_1}(V_s - v_{Cs}(t_3))\sin\omega_1 \tau_4 \tag{2.3.33}$$

$$v_{Cs}(t) = i_{L1}(t_3)Z_1 \sin\omega_1\tau_4 - (V_s - v_{Cs}(t_3))\cos\omega_1\tau_4 \qquad (2.3.34)$$

where

$$\tau_4 = t - t_3 \qquad (2.3.35)$$

$$t_4 = \frac{1}{\omega_1}\tan^{-1}\left[\frac{-i_{L1}(t_3)Z_1}{V_s - v_{Cs}(t_3)}\right] + t_3 \qquad (2.3.36)$$

Mode 6: $t_4 < t < t_5$, D_{r1} *off,* D_{r2} *off,* Q_1 *off,* D_2 *on*

$$i_{L1}(t) = \frac{1}{Z_{r1}}(V_s - v_{Cs}(t_4))e^{-\xi_1\tau_5}\sin\omega_{r1}\tau_5 \qquad (2.3.37)$$

$$\upsilon_{Cs}(t) = V_s - (V_s - v_{Cs}(t_4)) \cdot e^{-\xi_1\tau_5}\left(\cos\omega_{r1}\tau_5 - 3\frac{\xi_1}{\omega_{r1}}\sin\omega_{r1}\tau_5\right) \qquad (2.3.38)$$

where

$$\tau_5 = t - t_4 \qquad (2.3.39)$$

$$\xi_1 = \frac{R}{2L_p} \qquad (2.3\ 40)$$

$$\omega_{01} = \frac{1}{\sqrt{C_s L_p}} \qquad (2.3.41)$$

$$\omega_{r1} = \sqrt{\omega_{01}^2 - \xi_1^2} \qquad (2.3.42)$$

$$Z_{r1} = \omega_{r1}L_p \qquad (2.3.43)$$

$$t_5 \frac{1}{\omega_1}\tan^{-1}\left[\frac{\omega_{r1}}{3\xi_1}\right] + t_4 \qquad (2.3.44)$$

Mode 7 : $t_5 < t < t_6$, D_{r1} *on,* D_{r2} *on,* Q_1 *off,* D_2 *off*

$$i_{L1}(t) = e^{-\xi_2\tau_6}(A_1\sin\omega_{r2}\tau_6 + i_{L1}(t_5)\cos\omega_{r2}\tau_6) \qquad (2.3.45)$$

$$v_{Cs}(t) = V_s - Z_{r2}e^{-\xi_2\tau_6}\left\{A_1\left(\cos\omega_{r2}\tau_6 + \frac{\xi_2}{\omega_{r2}}\sin\omega_{r2}\tau_6\right) + i_{L1}(t_5)\left(\frac{\xi_2}{\omega_{r2}}\cos\omega_{r2}\tau_6 - \sin\omega_{r2}\tau_6\right)\right\}$$

$$(2.3.46)$$

where

$$A_1 = \frac{V_s - v_{Cs}(t_5)}{Z_{r2}} - i_{L1}(t_5)\frac{\xi_2}{\omega_{r2}} \qquad (2.3.47)$$

$$\tau_6 = t - t_5 \qquad (2.3.48)$$

$$\xi_2 = \frac{R}{2L_{el}} \qquad (2.3.49)$$

$$\omega_{02} = \frac{1}{\sqrt{C_sL_{el}}} \qquad (2.3.50)$$

$$\omega_{r2} = \sqrt{\omega_{02}^2 - \xi_2^2} \qquad (2.3.51)$$

$$Z_{r2} = \omega_{r2}L_{el} \qquad (2.3.52)$$

Mode 8. $t_6 < t < t_7$, D_{r1} *on,* D_{r2} *on,* Q_1 *off,* D_2 *on*

$$i_{L1}(t) = i_{L1}(t_0)\cos\omega_2\tau_7 + \frac{1}{Z_2}(V_s - v_{Cs}(t_6))\sin\omega_2\tau_7 \qquad (2.3.53)$$

$$v_{Cs}(t) = i_{L1}(t_6)Z_2\sin\omega_2\tau_7 - (V_s - v_{Cs}(t_6))\cos\omega_2\tau_7 + V_s \qquad (2.3.54)$$

where

$$t_7 = T \text{ (switching period)}$$

$$\tau_7 = t - t_6 \qquad (2.3.55)$$

$$i_{L1}(t_6) \langle\ 0 \qquad (2.3.56)$$

$$v_{Cs}(t_6) \langle\ V_s \qquad (2.3.57)$$

Finally, the total solution is obtained by using the following expressions :

$$i_{L1}(t) = i_{Lm}(t) + i_{L2}(t) \qquad (2.3.58)$$

$$L_m \frac{di_{Lm}}{dt} = L_2 \frac{di_{L2}}{dt} \qquad (2.3.59)$$

C.   Steady State Solution

The voltage and current solutions $X(t) = [i_L \ v_C]^T$ outlined in Section 2.3.3 were normalized, and a computer program was written to calculate the steady state. The program selects the respective equations for each mode of operation according to the sequences shown in Fig. 2.13 and modifies them by using $R_s = 0$ in TM's 5 and 6 (Fig. 2.12) when the auxiliary switch is considered. The steady-state solutions for different circuit parameters, duty cycles, and load currents are determined by solving

$$X(0) - X(T) = 0 \qquad (2.3.60)$$

To solve (2.3.60) a Broyden algorithm [25] has been used. The algorithm is described in Appendix A1. Relevant steady-state waveforms at 50% duty cycle for the three cases are illustrated in Fig. 2.14.

The modes of operation depend on the initial condition of the capacitor $V_{Cs}(t_{on})$, the characteristic impedance Z_1 (Z_2), the load current, and the duty cycle.

1) Non-resonant Mode with the Active Snubber: Fig. 2.14 (a) shows the waveforms for this mode. The topology operates in a *non-resonant* mode if in steady sate, $V_{Cs}(t_{on})$ is always larger than V_s for any duty cycle and load current.
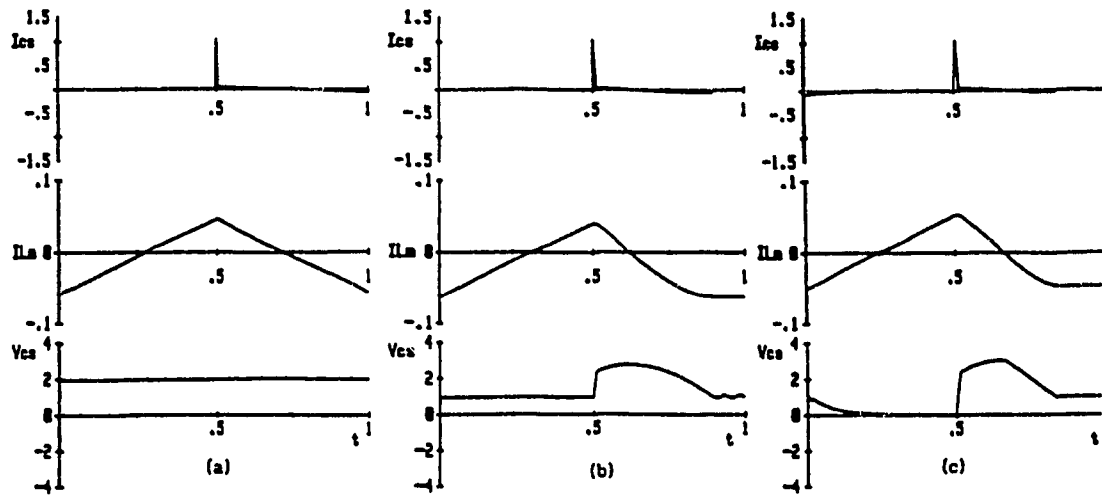
Figure 2.14 Steady-State Voltage/Current Solutions. I_{Cs}, I_{Lm} and V_{cs}. a) Non Resonant Mode by using the Active Snubber. b) Quasi-Resonant Mode by using the Active Snubber. c) Quasi-Resonant Mode by using the DRC Snubber.
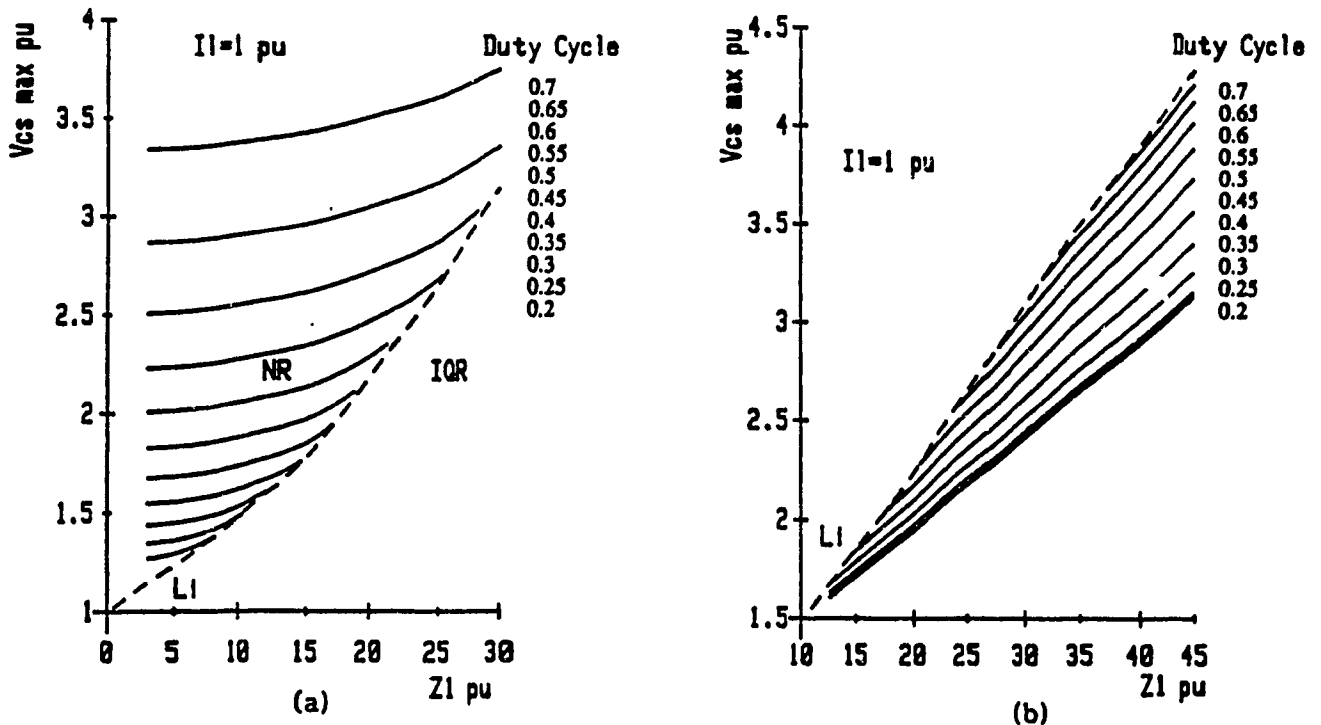
Figure 2.15 Maximum Snubber Capacitor Voltage VCs as a function of the Characteristic Impedance Z1. Duty Cycle as a Parameter. a) Non-resonant Mode with the Active Snubber. b) Quasi-resonant Mode with the DRC Snubber

D.   DC Magnetizing Current and Modes of Operation.

As is shown in Fig. 2.13, the TM's sequence is always the same. The effect of Z_1 on the maximum capacitor voltage for different duty cycle (rated load) is illustrated in Fig. 2.15 (a). Each curve gives the range of values of Z_1 for a *non-resonant* mode. The line L_j indicates the boundary between this mode and the *quasi-resonant* modes.

The value of Z_1 should be chosen with regard to the minimum duty cycle, the maximum voltage of the capacitor (switches), and the time response (Z_1 large as possible). Fig 2.16 illustrates the operating characteristics for $Z_1 = 5$ pu. Because the DC component of the leakage inductances current, during the turn off, can not circulate through the capacitor, there is always a small negative DC component in the magnetizing current, which changes with the duty cycle and the load current (Fig. 2.16 (d) and (e)). The magnitude of this DC component decreases as the duty cycle increases and increases if the load current increases. Fig. 2.16 (f) shows the maximum capacitor voltage as a function of duty cycle and load. As can be seen, this voltage is independent of the load current and it is in close agreement with (2.3.3) ($V_c = V_{cmax}$).

2) Quasi-resonant Mode with the Active Snubber : The Fig. 2.14 (b) shows the waveforms for this mode. In this case, $V_{Cs}(t_{on})$ is practically equal to V_s for any duty cycle and load current (steady state). As can be seen I in Fig. 2.13, the TM's
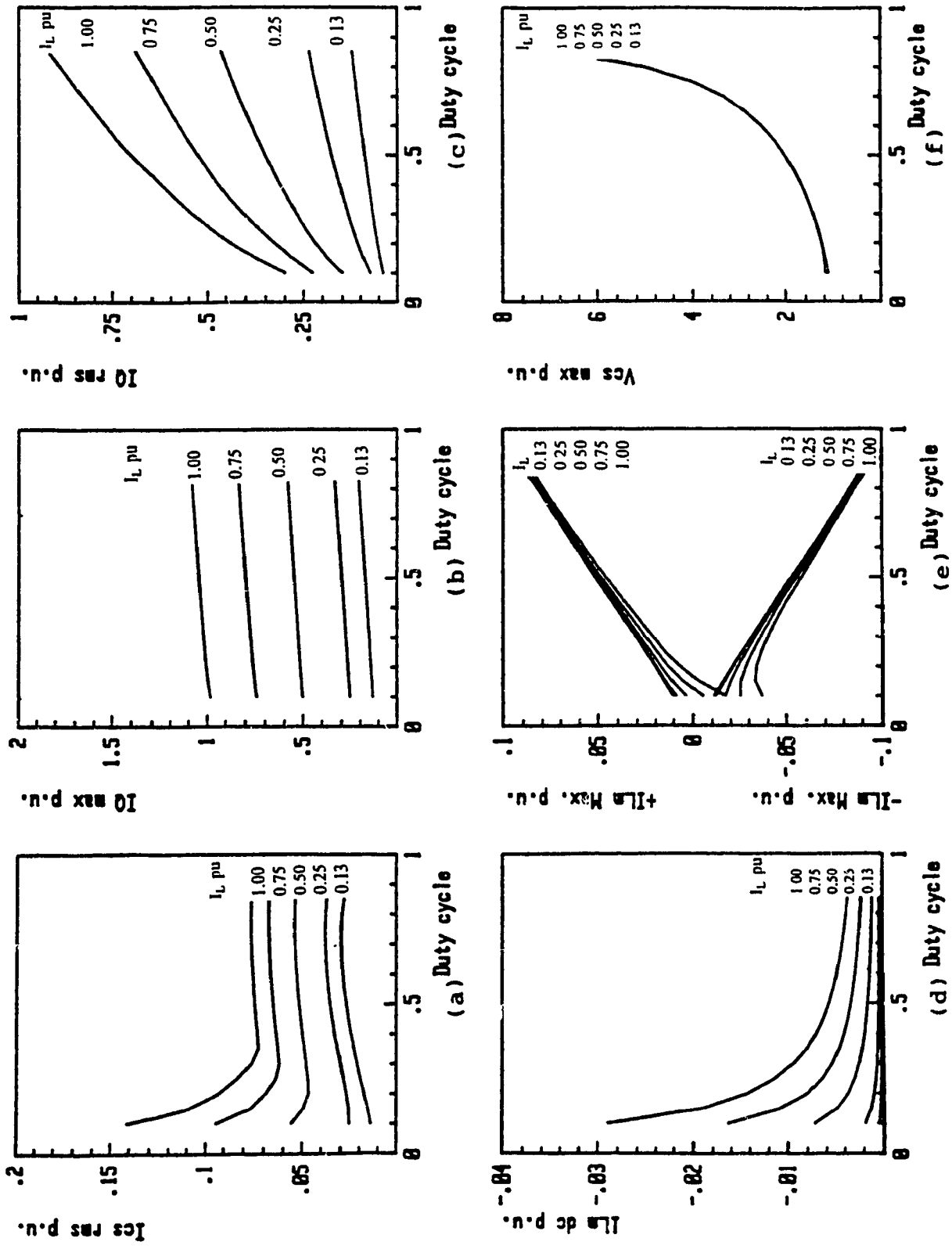
Figure 2.16 Operating Characteristics (pu) with active snubber. *Non-Resonant Mode.* a) $I_{Cs}rms$, b) $I_{Q}max$, c) $I_{Q}rms$, d) $I_{Ln}DC$, e) $I_{Ln}max$, and f) $V_{Cs}max$ as a function of the Duty Cycle. The Load Current I_L as a parameter.

Figure 2.17 Operating Characteristics (pu) with DRC snubber. *Quasi-Resonant Mode* a) I_{Cs}rms, b) $I_Q$max, c) $I_Q$rms, d) I_{Lm}DC, e) I_{Lm}max, and f) V_{Cs}max as a function of the Duty Cycle. The Load Current IL as a parameter.

sequence may be different this mode, depending on the final value of the capacitor around V_s at $t = T$. Moreover, if the TM's sequence is extended more than TM 6, negative magnetizing current is trapped in the transformer, and the TM's can oscillate between 7 and 4'.

3) Quasi-resonant Mode with the DRC snubber: The Fig. 2.14 (c) shows the waveforms for this mode. In this case, $V_{Cs}(t_{on})$ is always equal to zero, and $V_{Cs}(T)$ is selected to be equal to V_s for any duty cycle and load current. The range of values for Z_1 that ensure this operation are presented in Fig. 2.15 (b). A minimum value of Z_1 (to limit V_{Csmax}) must be chosen at maximum duty cycle and rated load; the boundary is indicated by the curves L_i.

Operating characteristics for this mode with $R_s = 10$ and $Z_1 = 30$ pu are shown in Fig. 2.17. It should be noted that for this particular value of R_s, a zero DC component in the magnetizing current is obtained at 60% duty cycle and $I_1 = 1$ pu (Figs. 2.17 (d) and (e)) and the maximum voltage in the capacitor is a function of the load (Fig. 2.17 (f)).

2.3.3 Design Procedure and Example

A.   Design Procedure

Converter design procedure, based on the analysis method presented in Section 2.3.3 , is as follows :

1) A transformer with a minimum leakage inductance and a maximum magnetizing inductance must be used.

2) From Fig. 2.6, a value is determined for the characteristic impedance Z_1.

3) The value of capacitor C_s is calculated by using (2.3.22).

4) With the values determined in steps 1) to 3), steady-state solutions for different duty cycles and load currents are determined by solving (2.3.59).

5) For each solution in 4) above, the i_{RMS}, i_{DC}, i_{max}, and $VC_{s_{max}}$ values are computed (moreover, an optimum value that eliminates the DC magnetizing current at maximum duty cycle can be found in this step).

6) Finally, from these data, operating characteristics cur·es in term of design parameter are obtained. Those curves are used to determinate the maximum voltages and currents in each element of the circuit.

B.   Design Example

In order to illustrate the design procedure, design examples example are provided in this section. The F1S topology shown in Fig. 2.11 will be designed with the active snubber to operate in the *non-resonant* mode, and with the DRC snubber to operate in the *quasi-resonant* mode.

1) Design Specifications :

Maximum output power : $P_O = 1.0$ kW

Maximum output voltage : $V_O = 50$ V

Maximum source voltage : $V_{Smax} = 150 \ V$

Minimum source voltage : $V_{Smin} = 140 \ V$

Operating frequency : $f = 20 \ kHz$

Duty cycle : $\delta_{min} = 0.3, \ \delta_{max} = 0.6$

Transformer inductances : $L_m = 1800 \ \mu H, \ L_1 = L_2 < 2.0 \ \mu H$

Open loop voltage regulation : $R_e = 5\%$

2) Transformer ratio : The transformer ratio is calculated as follows :

$$n = \frac{V_{primary}}{V_{secondary}} = \frac{V_{s \ min}\delta_{max}}{V_0(1+R_e)} = 1.6$$

3) Base Values :

$$V_b \quad = V_{Smax} \quad = 150 \ V$$

$$I_b \quad = I_{1max} \quad = 15 \ A$$

$$\omega_b \quad = 2 \ \pi f$$

Hence

$$C_b = \frac{I_b}{V_b \ \omega_b} = 0.796 \quad \mu F$$

$$L_b = \frac{V_b}{I_b\omega_b} = 0.0795 \quad mH.$$

4) Design :

a) Active snubber, non-resonant mode : From Fig. 2.15 (a), with $\delta_{min} = 0.3$, a maximum value for Z_1 is

$$Z_{1max} = 13 \text{ pu}$$

and with $Z_{1max} = 13$ pu and $\delta_{max} = 0.6$. V_{Csmax} is

$$V_{Csmax} = 2.51 \text{ pu.}$$

b) DRC snubber, quasi-resonant mode : From Fig. 2.15 (b), with $\delta_{max} = 0.6$ a

minimum value for Z_1 is

$$Z_{1min} = 30.5 \text{ pu.}$$

The design is completed by using (2.3.22) and Figs. 2.16 and 2.17. The resulting

components, voltages, and current values for both modes of operation are

summarized in **Table 2.3-I.**

Table 2.3-I

Summary of the Design Example

Active Snubber in a NR mode and DRC Snubber in a QR Mode.

	PU VALUES		ACTUAL VALUES		
	ACTIVE SN.	DRC SN	ACTIVE SN	DRC SN	Unit
L1	0.025	0.025	<2	<2	µH
L2	0.025	0.025	<2	<2	µH
Lm	22.640	22.640	1800	1800	µH
Cs	3.769	0.024	3	0.019	µF
VCsmax	2.400	3.300	360	495	V
VQ1max	2.400	3.300	360	495	V
VQ2max	2.400	3.300	360	495	V
ICsmax	1.070	1.075	16.050	16.120	A
ICsrms	0.080	0.090	1.200	1.350	A
IQ1max	1.070	1.100	16.050	16.120	A
IQ1rms	0.800	0.810	12.000	12.150	A
IQ2max	0.070	-	1.050	-	A
ID1max	0.070	0.075	1.050	1.125	A
ID2max	1.070	-	16.050	-	A
ILmmax	0.070	0.075	1.050	1.125	A

2.3.4 Experimental Results

In order to establish the feasibility of the proposed converter topology and to verify the selected theoretical results, a 1-kW prototype unit operating at 20 kHz switching frequency was built and tested. The TOSHIBA IGBT module MG25N2YS1 with two switches was used to implement the power circuit.

Relevant experimental waveforms at 55% duty cycle are shown in Figs. 2.18, 2.19, and 2.20. These results are in close agreement with the theoretical waveforms shown in Figs. 2.14. In particular, Figs. 2.18 (a), 2.19(a), and 2.20 (a) illustrate the capacitor currents and voltages. The peak capacitor current at the beginning of the turn off corresponds to the leakage-parasitic-inductance energy stored for the capacitor. After this time, the capacitor current is equal to the magnetizing inductance current. It is clearly shown that the magnetizing current is almost zero for the three cases.

With the active snubber circuit, the *non-resonant* mode of operation was achieved by using a capacitor of 3 μF. The Fig. 2.18 (a) shows that the capacitor voltage becomes practically constant and is 2.1 times the input voltage. The quasi-resonant mode was achieved by using a capacitor value equal to 0.40 μF. The Figs. 2.19 (a) verify that the capacitor voltage becomes sinusoidal during the turn-off with a peak value equal to 2.66 times the input voltage. As was predicted, at the end of the resonance this voltage is equal to the input voltage.

Fig. 2.20 (a)) shows the experimental results with the DRC snubber circuit operating in a quasi-resonant mode. In this case the peak voltage becomes 3.10 times the input voltage.

The Figs. 2.18 to 2.20 (b) illustrate the switching losses of the main switch during turn on for the three cases under study. The experimental results proof that the highest turn-on losses occur with the DRC snubber circuit, and they are negligible with the active snubber circuit operating in the *non-resonant* mode (Fig. 2.18 (b)). In order to provide ZVS during the turn-on in this case, a dead time of 1 μs was introduced between the signal of the main switch and the complementary switch. During the dead time both switches are off and the negative magnetizing current is used to discharge the parasitic capacitance of the main switch.

Similarly, Figs. 2.18 to 2.20 (c) illustrate the switching losses of the main switch during the turn off. These losses are neglected with the DRC snubber circuit due to the ZVS feature. For the case of the active snubber is seem that the losses increases. This is so because wiring need to be added to measure the current through the switch, increasing the parasitic inductance in series. It should be noted that the ZVS in this case is provided by the parasitic capacitance of the main switch. Experimental values of the converter efficiency (η%) for the three modes of operation with 1 and 0.5 pu output load are presented in **Table 2.3-II**.
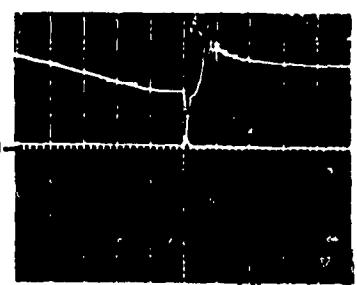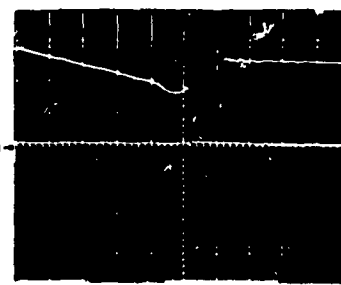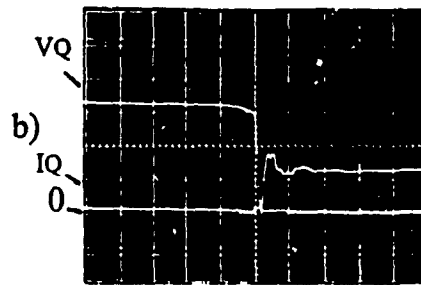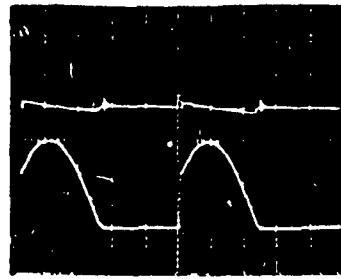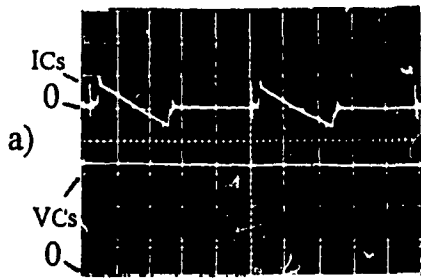
Turn-on
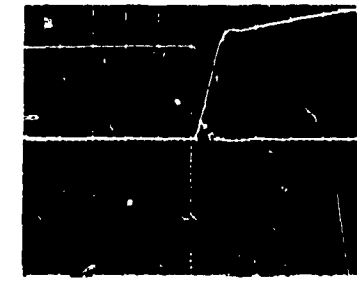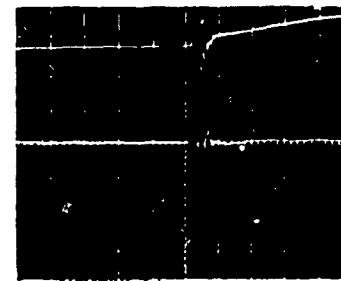
Turn-off

Figure 2.18 Experimental Results with Active Snubber, NR Mode.	**Figure 2.19** Experimental Results with Active Snubber, QR Mode.	**Figure 2.20** Experimental Results with DRC Snubber, QR Mode.
Voltage scale: 100 V/div. a) Current scale: 1A/div. Time scale: 10us/div. b) Current scale: 10A/div. Time scale: 1us/div c) Current scale: 10A/div. Time scale: 1us/div.	Voltage scale: 100 V/div. a) Current scale: 5A/div. Time scale: 10us/div. b) Current scale: 5A/div. Time scale: 1us/div c) Current scale: 5A/div. Time scale: 1us/div.	Voltage scale: 100 V/div. a) Current scale: 5A/div. Time scale: 10us/div. b) Current scale: 5A/div. Time scale: 1us/div c) Current scale: 5A/div. Time scale: 1us/div.

Table 2.3-II

Experimental Efficiency ($\eta\%$)

D=50%, Vo=50 V

LOAD	ACTIVE SNUBBER		DRC SNUBBER
	NON-RESONANT	QUASI-RESONANT	QUASI-RESONANT
0.5 PU	95.00	94.30	93.00
1.0 PU	94.00	94.60	92.36

2.4. Summary

In this Chapter, two HF single-switch single-ended forward DC/DC converter topologies with ZVS, transformer flux balancing, and extended duty cycle capability have been thoroughly analyzed. A simple HF transformer which does not require a third winding to reset the core is used. Those features lead to a better current utilization of the power switch, provide better utilization of the transformer core and improves the efficiency of the single-ended forward converters.

In Section 2.3, a complete analysis and design procedure of an improved single-ended Forward converter using a nondissipative LC-type snubber circuit has been presented. The main advantages of this topology are the reduction of switching stresses and increased efficiency through the use of a quasi-resonant energy recovery subcircuit. However, this circuit can not provide ZVS during the turn-on. This is an important requirement to improve the efficiency at higher

frequency and by using MOSFET. In addition, the energy stored on the parasitic inductance of the DC bus can not be recovered. This means that an extra RC snubber must be used in parallel with the input DC bus or with each recovery diodes to dissipate the energy and to minimize the resulting voltage spike in the DC input bus. It has been also proof that with this topology, the resulting maximum switch voltage is 2.93 times the supply voltage V_S at 50 percent duty cycle and the worst case for the voltage occurs under light load operating condition.

In Section 2.4, a topology with an active snubber has been proposed to solve the problem of the parasitic inductance of the DC bus and to obtain ZVS during turn-off. It is found that by using a combination of a main switch, a low-power switch and a small capacitor connected in series with the primary of the HF transformer, a practically zero DC transformer magnetizing current can be achieved at rated load. This topology can be operated at duty cycles larger than 50% without loss of the aforementioned characteristics. Moreover, it can be designed to operate in a non-resonant and quasi-resonant mode and in both modes the proposed converter presented an efficiency larger than 93% at a 55% duty cycle (see **Table 2.3-II**). However, the property of ZVS during turn-off and turn-on diminish at low duty cycle due to the DC magnetizing current becomes positive as shown in Figs. 2.16 (d).

The structure shown in Fig. 2.12 suggests that complementary p an n types of transistor switches could be integrated into a single block so that a common gating signal could be applied to both switches. Such a block would have three power terminals and two control terminals, thus considerably simplifying the overall converter hardware. Finally, the theoretical results have been verified experimentally on 1 kW 20 kHz laboratory prototype units.

CHAPTER 3

TWO-SWITCH FORWARD CONVERTERS

3.1 Introduction

The main drawback of the single-switch single-ended forward topologies analyzed in the Chapter 2 is the voltage stress of the main power switch. When a L-C snubber or an active snubber circuit is designed to reduce the switching losses and to provide transformer core flux balancing, the maximum switch voltage at 50% duty cycle can be 3.25 times the DC input voltage (quasi-resonant mode), or higher if the duty cycle is increased. This constraint limits the application of these topologies for higher voltage. However, to obtain higher power capability, a single ended forward converter can be designed employing two power switches, connected in series or in parallel, thus reducing stresses by 50%.

Fig. 3.1 shows the simplified power circuit of a conventional two switches single-ended DC/DC forward converter. This topology is designed by using two power switches connected in series, and each switch with a DRC snubber connected in parallel. The diodes D_3 and D_4 are incorporated to reset the flux of the HF transformer by connecting the DC input voltage source Vs in reversed polarity during the turn-off. This topology is widely used for power applications in the range of 1 to 5 kW [2]. In comparison with the half-bridge and full-bridge topologies, this converter yields more reliable performance because of the inductances of the HF transformer (HFT) limit the di/dt of any short circuit current
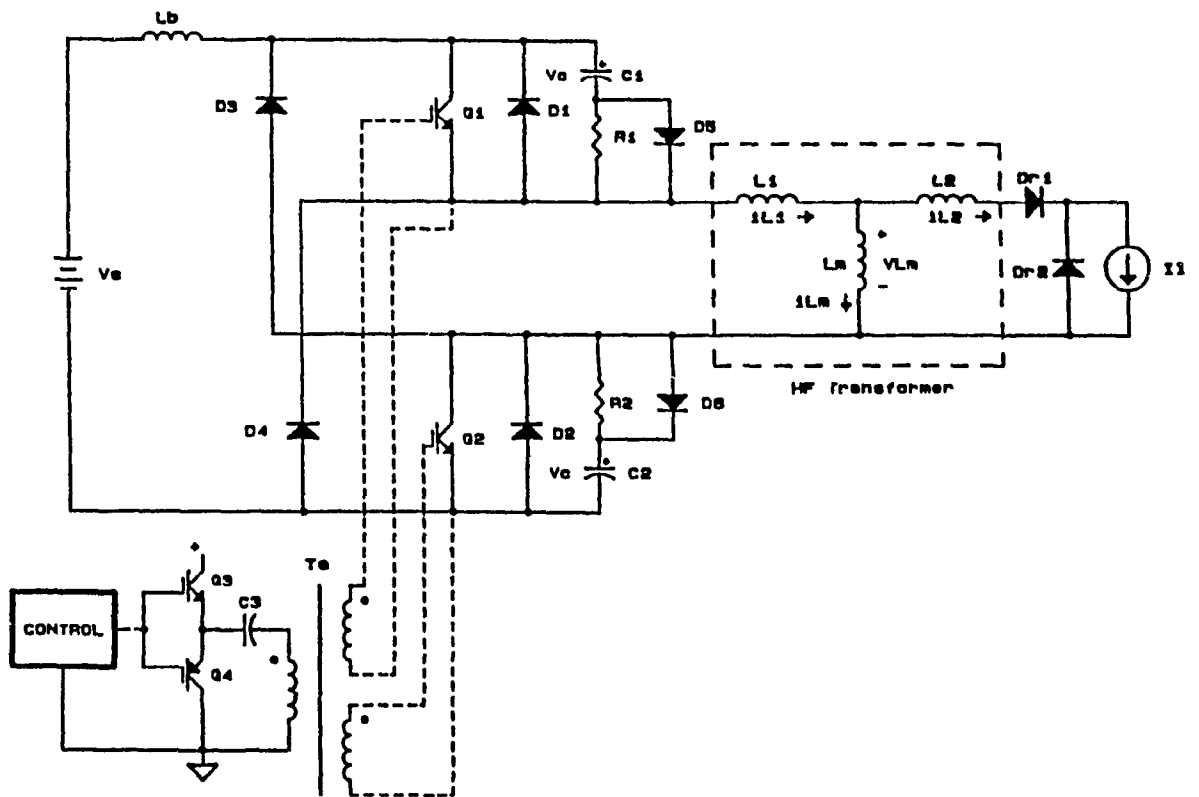
Figure 3.1 Typical two-switch forward converter topology. Simplified power circuit.

through the power switches. In addition, as compared with the high-power resonant converter, the power switches are subjected to lower voltage and current stresses [1,2,18]. However, it cannot operate with more than a 50% duty cycle and the associated HFT operates with a DC flux component. Also, it requires DRC snubber circuit and the transformer resetting diodes D3,D4. These two diodes do not allow to recycle the energy stored in the parasitic inductance of the DC bus.

The aforementioned drawbacks means, increased size of the HFT core and higher losses at high frequency due to the increased losses in the semiconductor devices required to protect the switches against overvoltage. Moreover, the two switches usually operate with a nominal duty cycle less than 50% to allow instantaneous output voltage regulation without saturating the HFT core. This implies a low utilization of the power circuit.

Lossless L-C snubbers for the topology shown in Fig. 3.1 have been proposed in [2,24,26] to reduce the turn-off switching losses and to clamp the voltage spikes across the switches. However, these solutions require extra elements, and they do not remedy disadvantages mentioned before.

In this chapter, a new single-ended forward converters (SEFC) with two power switches in series, and for output power higher than 1kW, is investigated. The reduction of the switching losses, extended duty cycle of operation, and better utilization of the HF transformer are the main features of the proposed

configurations. Moreover, a novel two-switch zero-voltage switching single-ended forward converter is proposed and thoroughly analyzed.

3.2 Topologies I: Two Switches in Series

Two variations of the SEFC topology shown in Fig. 3.1 are studied in this section; the proposed power circuits are shown in Fig. 3.2. To improve the performance, the resetting diodes, D_3 and D_4, have been eliminated, and the main switches have been replaced by the switching structures analyzed in Chapter two. Fig. 3.2 a) shows the resulting topology (F2SA) with the complementary n and p transistors and Fig. 3.2 b) shows the resulting topology (F2SB) with the quasi-resonant DRC snubber. This section presents an extended analysis of these structures. Moreover, a design procedure for each of them is proposed and illustrated with examples. Finally, the analytical predictions are substantiated by using a 4-kW, 40-kHz experimental unit.

3.2.1 Principle of Operation

The combination of the main switches (Q_1, Q_2), the inductances of the transformers (L_m, L_1, L_2), and L_b in series with each Quasi-Resonant Auxiliary Circuit (QRAC) shown in Fig. 3.2, constitutes a bi-directional low current boost converter, which provides transformer flux balancing and extended duty cycle operation. This boost converter operates first with the leakage inductances of the HF transformer (unidirectional current) and then with the magnetizing inductance
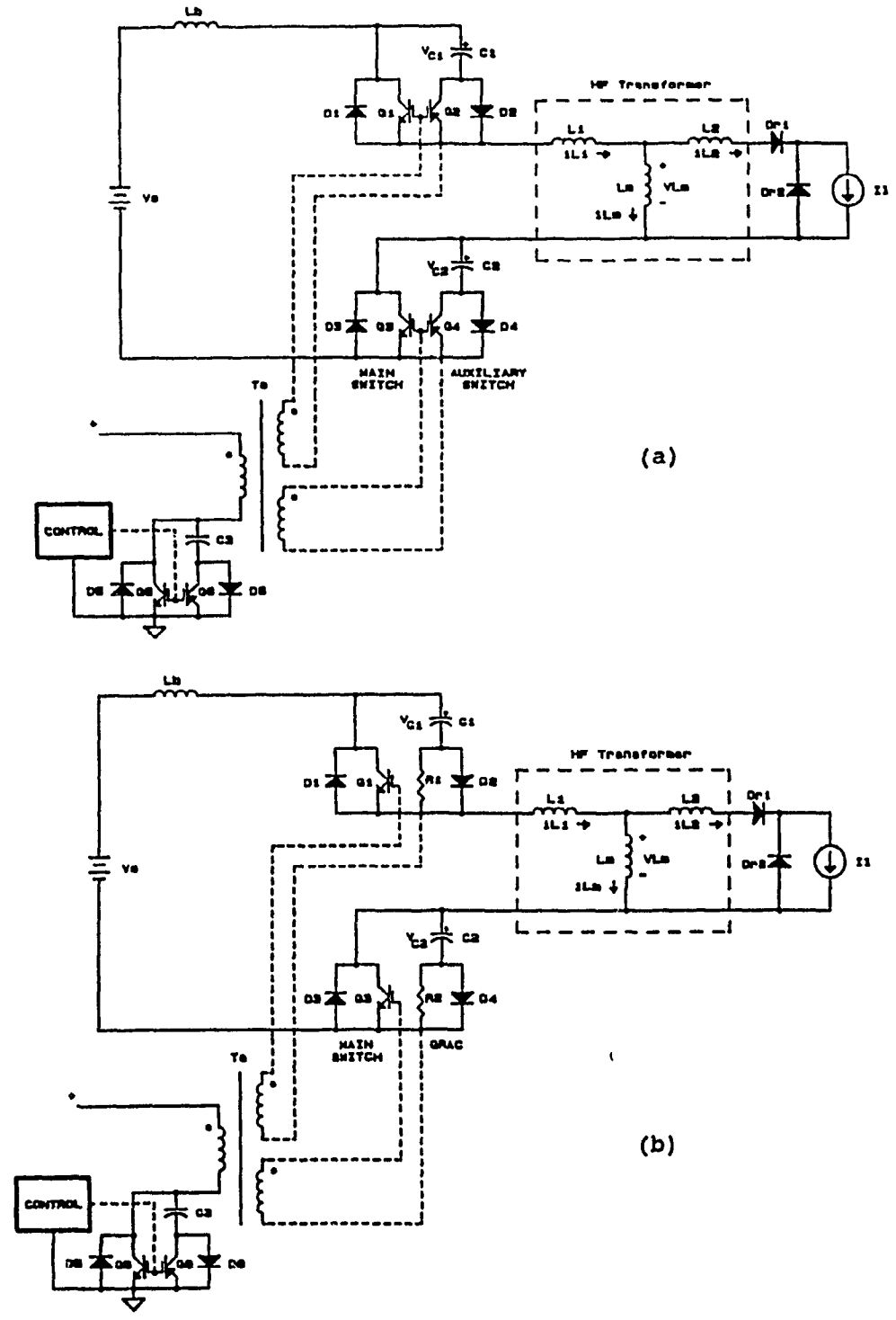
Figure 3.2 The proposed two-switch forward topologies. a) With a complementary switch. b) With a quasi-resonant DRC snubber.

(bi-directional current). Indeed, during the turn-off cycle, the capacitors C_1 and C_2 store first the energy from L_b, L_1 L_2 and then, from L_m during turn-on. After that, this energy is sent back to L_m again, and toward the input voltage source V_s. As a result, the HFT can be operated with practically no DC flux at rated load which means that a reduction in the size of the transformer core is possible. Moreover, the capacitors, C_1 and C_2, are connected in parallel with the respective main switch, providing ZVS (during the turn-on and turn-off), and reducing the switch voltage stress.

3.2.2 Power Circuit Analysis

The analysis presented here assumes ideal switches and a lossless transformer operating in a linear flux mode. A 'T' equivalent circuit is used to model the HFT. The output filter and load are represented by a current source (continuous current). This circuit is reflected to the primary side of the HFT, as shown in Fig. 3.2. The main objectives of the analysis are :

1) To identify the topological modes (TM's) or states of the circuit during one switching cycle and the resulting modes of operation

2) To find the voltage-current equations for each TM.

3) To find the steady-state solutions and the boundaries for each mode of operation.

To maximize the use of the analysis and design results derived here, all the components values and current-voltage ratings hereafter will be referenced with respect to the following base values:

$V_{base} = V_S$: input voltage

$I_{base} = I_1$: rated load current reflected to the primary side of the HFT

$f_{base} = f_s$: switching frequency

Hence,

$$Z_{base} = \frac{V_{base}}{I_{base}} = \frac{V_s}{I_1}$$

$$L_{base} = \frac{Z_{base}}{2\pi f_{base}}$$

$$C_{base} = \frac{1}{2\pi f_{base} Z_{base}}$$

Because the design specifications are usually given to the input/output terminals of the converter, and there are more than one resonant circuit, the value of Z_{base} in this section has been defined as the ratio of the input voltage to the maximum load current.

A. Topological Modes

The various topological Modes (TM) during one switching cycle (steady state), are shown in Fig. 3.3 (F2SB). The sequence corresponds to the more general case (i.e. DRC designed in a quasi-resonant mode of operation).

B. Normalized Voltage-Current Equations

To facilitate the circuit analysis and the design, normalized parameters with respect to base values are defined as follows :

D   normalized on time

Dn   normalized limit time for interval n

θ angular variable

θn   normalized limit angle for interval n

k_1 resonant frequency of modes M3 and M5

k_2 resonant frequency of mode M4

k_r resonant frequency of mode M6

Z_1 characteristic impedance of modes M3 and M5

Z_2 characteristic impedance of mode M4

Z_r characteristic impedance of M6

K_1 primary inductance factor of HFT

K_2 secondary inductance factor of HFT

Q   'Q' factor of the resonant circuit M6

With the above parameters, the angular form of the normalized state-equation solutions (V_c and I_{L1}) for each TM (F2SB) can be shown to be

Mode M1 : $0 \le \theta \le \theta_1$

$$I_{L_1}(\theta) = I_{L_1}(0) + \frac{1}{Z_2} k_2 \theta \qquad\qquad (3.2.1)$$

Mode M2 : $\theta_1 < \theta \leq \theta_2$

$$I_{L_1}(0) = I_{L_1}(\theta_1) + \frac{1}{Z_1}k_1(\theta - \theta_1) \tag{3.2.2}$$

Mode M3 : $\theta_2 < \theta \leq \theta_3$

$$\left[I_{L_1}(\theta) \right]^2 + \left[\frac{V_c(\theta) - 1}{Z_1} \right]^2 = \left[I_{L_1}(\theta_2) \right]^2 + \left[\frac{1}{Z_1} \right]^2 \tag{3.2.3}$$

Mode M4 : $\theta_3 < \theta \leq \theta_4$

$$\left[I_{L_1}(\theta) \right]^2 + \left[\frac{V_c(\theta) - 1}{Z_2} \right]^2 = \left[I_{L_1}(\theta_3) \right]^2 + \left[\frac{1 - V_c(\theta_3)}{Z_2} \right]^2 \tag{3.2.4}$$

Mode M5 : $\theta_4 < \theta \leq \theta_5$

$$\left[I_{L_1}(\theta) \right]^2 + \left[\frac{V_c(\theta) - 1}{Z_1} \right]^2 = \left[I_{L_1}(\theta_4) \right]^2 + \left[\frac{1 - V_c(\theta_4)}{Z_1} \right]^2 \tag{3.2.5}$$

Mode M6 : $\theta_5 < \theta \leq \theta_6$

$$\left[I_{L_1}(\theta) \right]^2 + \left[\frac{V_c(\theta) - 1}{Z_r} \right]^2 = \left[\frac{1 - V_c(\theta_5)}{Z_r} \right]^2 \rho(\theta) \tag{3.2.6}$$

Mode M7 : $\theta_6 < \theta \leq 2\pi$

$$I_{L_1}(\theta) = 0, \quad V_c(\theta) = 1, \quad I_{L_m}(\theta_6) \tag{3.2.7}$$

where

$$\rho(\theta) = e^{-\frac{R}{Z_r}k_r(\theta - \theta_5)} \left(1 + \frac{R^2}{4Z_r^2}\sin^2 k_r(\theta - \theta_5) + \frac{R}{2Z_r}\sin 2k_r(\theta - \theta_5) \right) \tag{3.2.8}$$

$$\theta_1 = \frac{\alpha}{k_2}; \quad \alpha = 2\pi k_2 D_1 = \left[\frac{I_1 - I_{L_2}(0)}{1} \right] Z_2 \tag{3.2.9}$$

$$\theta_2 = \theta_1 + \frac{\beta}{k_1}; \quad \beta = 2\pi k_1 (D_2 - D_1) \tag{3.2.10}$$

$$\theta_3 = \theta_2 + \frac{\gamma}{k_1}; \quad \gamma = 2\pi k_1 (D_3 - D_2); \quad \tan\gamma = \frac{1}{I_{L_1}(\theta_2) Z_1} \tag{3.2.11}$$

$$\theta_4 = \theta_3 + \frac{\delta}{k_2}; \quad \delta = 2\pi k_2 (D_4 - D_3); \quad \cos\delta = \frac{I_{L_1}(\theta_3) - \dfrac{1+K_2}{K_2} I_1}{I_{L_1}(\theta_3)} \tag{3.2.12}$$

$$\theta_5 = \theta_4 + \frac{\varepsilon}{k_1}; \quad \varepsilon = 2\pi k_1 (D_5 - D_4); \quad \tan\varepsilon = -\frac{I_{L_1}(\theta_4) Z_1}{1 - V_c(\theta_4)} \tag{3.2.13}$$

$$\theta_6 = \theta_5 + \frac{\zeta}{k_r}; \quad \zeta = 2\pi k_r (D_6 - D_5); \quad \tan\zeta = -\frac{2 Z_r}{R} \tag{3.2.14}$$

$$\theta = \omega_s t = 2\pi \frac{t}{T} = 2\pi D \tag{3.2.15}$$

$$Q = \frac{Z_1}{R} \quad \text{where} \quad R = 2R_1 = 2R_2 \tag{3.2.16}$$

$$k_1 = \frac{1}{\sqrt{CL_m(1+K_1)}} \quad \text{where} \quad C = \frac{C_1}{2} = \frac{C_2}{2} \tag{3.2.17}$$

$$k_2 = \frac{1}{\sqrt{CL_e}} \approx \frac{1}{\sqrt{CL_m(K_1+K_2)}} = \frac{k_1}{\sqrt{K_1+K_2}} \tag{3.2.18}$$

$$k_r = k_1 \sqrt{1 - \left[\frac{1}{Q}\right]^2} \tag{3.2.19}$$

$$Z_1 = k_1 L_m(1+K_1) = \sqrt{\frac{L_m(1+K_1)}{C}} \approx \sqrt{\frac{L_m}{C}} \tag{3.2.20}$$

$$Z_2 = k_2(L_e) = \sqrt{\frac{L_m(K_1+K_1 K_2 K_2)}{C(K_2+1)}} \approx Z_1 \sqrt{K_1+K_2} \tag{3.2.21}$$

$$Z_r = k_r(1 + K_1) = Z_1 \sqrt{1 - \left[\frac{1}{Q}\right]^2} \qquad (3.2.22)$$

$$K_1 = \frac{L_1}{L_m} \quad (L_1 \text{ including } L_b), \quad K_2 = \frac{L_2}{L_m} \qquad (3.2.23)$$

Equations (3.2.1) and (3.2.2) represent the linear charge of the inductance circuit during turn on. Equations (3.2.3)-(3.2.6) represent the resonant TM's during the turn-off. Finally, the dependent inductance current solutions i_{Lm} and i_{L2} in each TM are found using the following expressions :

$$i_{L_{m_{k+1}}}(\theta) = \frac{K_2}{1 + K_2} \Delta i_{L_{1_{k+1}}}(\theta) + i_{Lm}(\theta_k) \qquad (3.2.24)$$

$$i_{L2_{k+1}}(\theta) = i_{L1_{k+1}}(\theta) - i_{Lm_{k+1}}(\theta) \qquad (3.2.25)$$

where
$$\Delta i_{L1_{k+1}}(\theta) = i_{L1_{k+1}}(\theta) - i_{L1}(\theta_k) \quad k = 0,.7. \qquad (3.2.26)$$

C. Modes of Operation and Boundaries

Depending on the value of Z_1 for each topology shown in Fig. 3.3, two modes of operation are identified during turn off. The sequence of TM's for each of them is summarized in **Table 3.2-I**. Only the modes of operation that minimize the DC component of the magnetizing current are considered.

Table 3.2-I

Topological Modes (TM) and Modes of Operation (MO)

Topology	Z1 pu	TM	MO
F2SA: Complementary	5	M1, M2, M4, M5	MO1, non-resonant
switch	30	M1, M2, M4, M5, M7	MO2, quasi-resonant
FS2B: DRC snubber	40	M1, M2, M3, M4, M5, M6, M7	MO1, quasi-resonant
	<40	M1, M2, M3, M4, M5	MO2, non practical
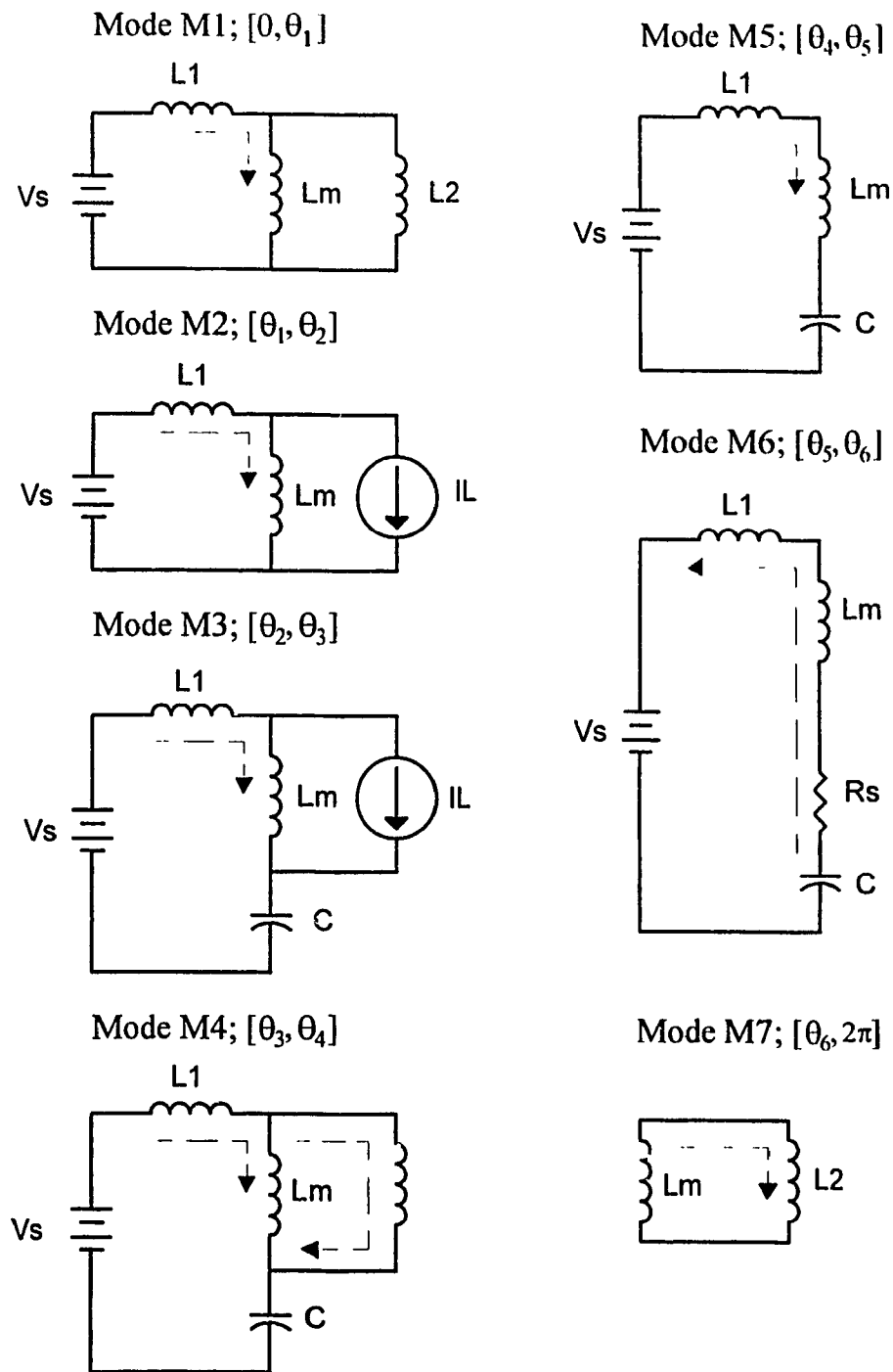
Figure 3.3 Topological Modes (TM) during a switching cycle. Quasi-resonant mode of operation with a DRC snubber circuit.

The normalized voltage-current equations presented in section B and the TM's presented in Table 3.2-I show that the circuit can be characterized by the following normalized functions :

$$V_{c_{max}} = V_c(\theta_5) \begin{cases} f(Z_1,k_1,I_1,D_2,K_1,K_2) & \text{F2SA} \\ f(Z_1,k_1,I_1,D_2,K_1,K_2,Q) & \text{F2SB} \end{cases}$$

Therefore, the respective design problem is solved by finding the steady-state solution of these functions in the different modes of operation for the different parameter values Z_1, K_1, K_2, Q and for different operating conditions: k_1, I_1, D_2. A computer program using a Broyden algorithm (Appendix A1) was written to find the solutions and the respective boundaries. Fig 3.4 shows the solutions on the state plane and Fig. 3.5 shows the resulting current-voltage waveforms for the different modes of operation. The performance is similar to the topology II studied in Chapter 2. However, to better understands the operation of the circuit, the analysis will be extended here after as follows:

F2SA topology

a) Nonresonant mode by using a low value of Z1 (MO1): The maximum values of the capacitor ($V_{c1}+V_{c2} = V_c (\theta_5)$) in term of Z1 are shown in Fig. 2.15 (a). It follows that for a low value of Z_1 ($Z_1 < 5$ pu), the capacitor voltage is almost constant during turn-off and it is only a function of switch duty cycle. Therefore, it is not affected by the load current and can be calculated by using the typical expression for a boost converter [3]. However, under transient conditions, a low
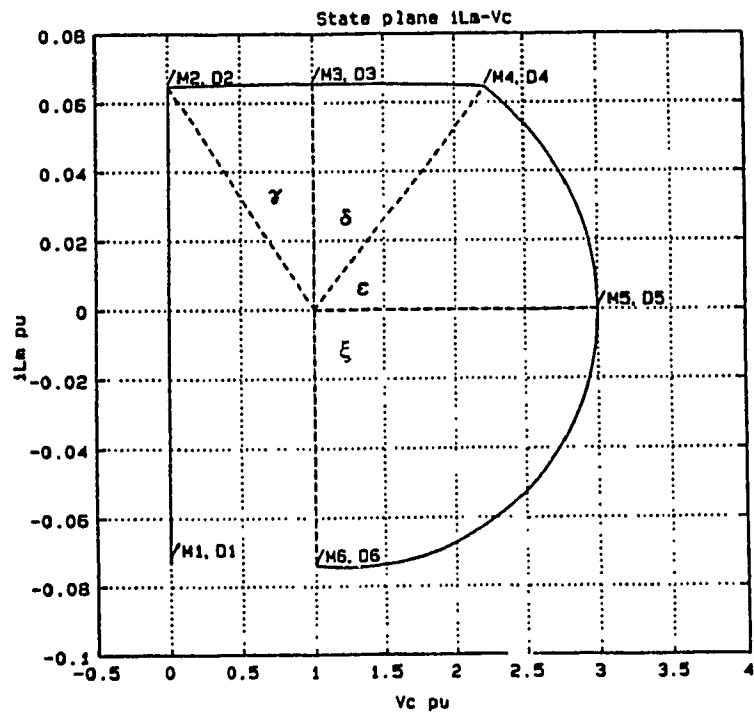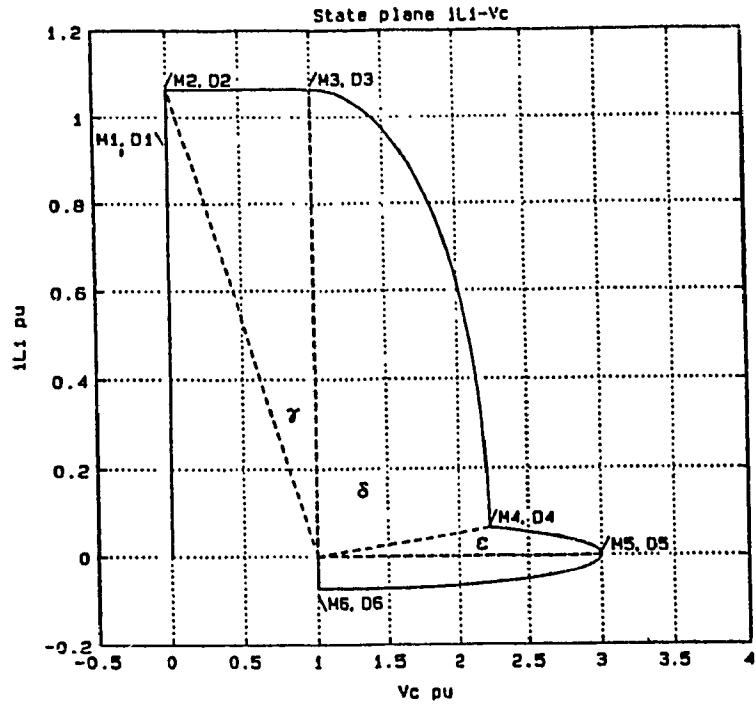
Figure 3.4 The voltage/currents solutions for iL1, iLm, and Vc on the state plane.
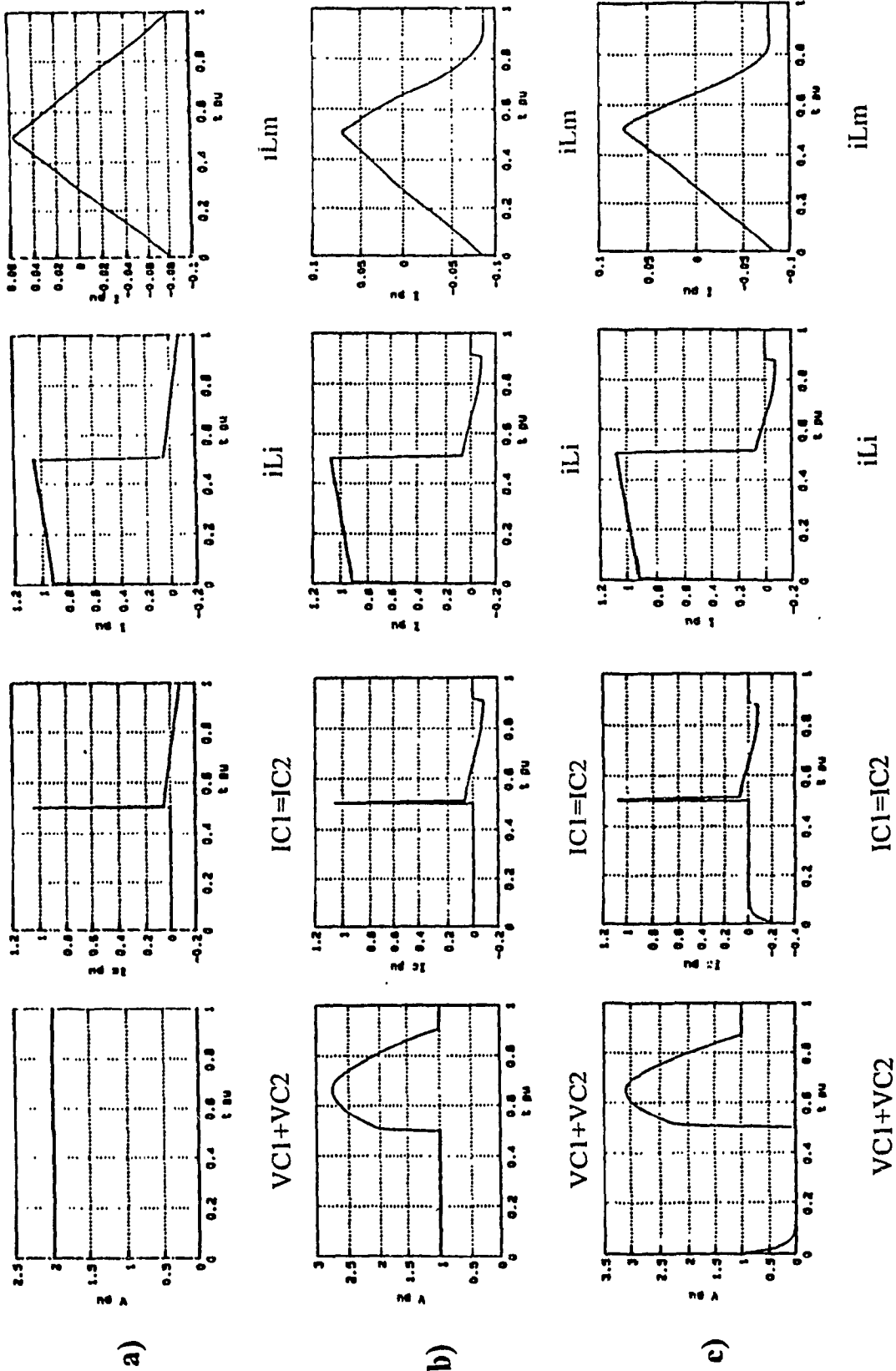
Figure 3.5 Steady state voltage/current piecewise waveforms during a switching cycle. iL=1pu, δ=0.5, K1=0.002, K2=0.001. a) Active snubber; non-resonant mode design; Z1=5 pu. b) Active snubber; quasi-resonant mode design; Z1=30. c) DRC snubber, quasi-resonant-mode design; Z1=40, Q=4.

value of Z_1 will produce low frequency resonance between L_m and C with a high-amplitude magnetizing current and capacitor voltage. On the other hand, increasing Z_1 will increase the maximum capacitor voltage, which becomes more dependent on the load, and circuit parameter values, but it also improves the transient response. A good compromise is to use Z_1 close to 5 pu.

b) Quasi-resonant mode by using a high value of Z1(MO2): The initial condition in the capacitor C_1 (C_2) at the beginning of turn-off is equal to 0.5 pu ($V_s/2$). This mode of operation is a good compromise between time response and overvoltage.

It should be noted that the two above modes of operation provide ZVS during turn-on and turn-off while the magnetizing current remains negative at the end of the turn-off. A dead time between the control signal of the main switch and the complementary switch is required.

F2SB topology

a) Quasi-Resonant mode by using a high value of Z1(MO1): The initial condition in the capacitor C_1 (C_2) at the beginning of turn-off is equal to zero. Therefore, this topology provide zero voltage switching transition during the turn-off

b) Quasi-resonant mode by using a low value of Z1 (MO2): This mode of operation produces a positive DC magnetizing current, high voltage across the switches, and high switching losses. Therefore, this operation must be avoided.

3.2.3 Design Example

The design example presented in this section provides a guideline for determining the components values and the current-voltage stresses of the power semiconductor devices. The F2S topologies shown in Fig. 3.2 (a) and (b) are designed in the operating mode MO1 with the following specifications :

Output power, $\qquad P_O$ = 4 kW

Output voltage, $\qquad V_O$ = 50 V

Input voltage, $\qquad V_S$ = 300 V

Operating frequency, $\quad f_S$ = 40 kHz

Extended duty cycle, $\quad \delta_m$ = .55

Efficiency, $\qquad \eta > 85\%$

The base values are

$$V_b = V_s = 300V$$

$$I_b = I_1 = \frac{P_o}{\eta V_s \delta} = \frac{4000}{0 \cdot 85 \cdot 300 \cdot 0.55} = 28.52A$$

$$Z_b = \frac{V_s}{I_1} = \frac{300}{28.52} = 10.52\Omega$$

Hence

$$L_b = 41.85\ \mu H$$

$$C_b = 0.38\ \mu F$$

Assuming 5% regulation (Re), the turns ratio n for the transformer is

$$n = \frac{V_{primary}}{V_{secondary}} = \frac{V_s d}{V_o(1+Re)} = \frac{300 \cdot 0.55}{50 \cdot 1.05} = 3.14$$

Other data of the HFT are

$$L_m = 43.00 \text{ pu } (1800 \text{ }\mu H)$$

$$K_1 = 0.002, \quad K_2 = 0.001$$

Hence, the maximum magnetizing current for both topologics is

$$i_{Lm}(\theta_2) \approx \frac{V_s}{L_m}\pi D_2 = \frac{1}{43} \cdot \pi \cdot 0.55 = 0.040 \text{ pu}, \quad \text{i.e., } 0.42 \text{ A.}$$

The voltage stress and component values are determined as follows :

1) **F2SA:** For MO1 from Fig. 2.15 a) with δ=0.55

$$Z_1 = 5 \text{ pu}$$

$$V_{c1} + V_{c2} = V_{cmax} = 2.2 \text{ pu}$$

Hence, $V_{c1} = V_{c2} = V_{Q1} = V_{Q2} = V_{Q3} = V_{Q4} = 1.1$ pu, i.e., 330 V. The capacitor

value C is obtained by using (3.2.20) as follows :

$$C = \frac{L_m(1+K_1)}{Z_1^2} = 1.72 \text{ pu}$$

Hence, $C_1 = C_2 = 3.44$ pu, i.e., 1.31 μF.

2) **F2SB:** Similarly, for MO1 from Fig. 2.15 (b) with $\delta = 0.55$ on Li

$$Z_1 = 40 \text{ pu}$$

$$V_{c1} + V_{c2} = V_{cmax} = 2.75 \text{ pu}$$

$$V_{c1} + V_{c2} = V_{cmax} = 2.75 \text{ pu}$$

hence, $V_{c1} = V_{c2} = V_{Q1} = V_{Q2} = V_{D1} = V_{D2} = 1.38$ pu, i.e., 414 V. By using (3.2.20), the capacitor value C is

$$C = 0.027 \text{ pu}$$

Hence $C_1 = C_2 = 2C = 0.054$ pu, i.e., 0.020 μ F. By using (3.2.16) with Q = 4, the resistor value is

$$R = Z_1 / Q = 10 \text{ pu}$$

Hence, $R_1 = R_2 = R/2 = 5$ pu, i.e., 52.6 Ω. The power dissipated in R_1 or R_2 is obtained considering the energy stored in C_1 (C_2) and the power dissipated in R_1 (R_2) due to the negative magnetizing current flowing through the DRC snubber circuit during the turn-off. Therefore, by using the following expression :

$$P_R = \frac{1}{2} C_1 \left[\frac{V_s}{2} \right]^2 \cdot f_s + \frac{(i_{Lm}(\theta_2))^2}{12} \cdot R_1$$

Hence,

$$P_R = 0.5 \cdot 0.020 \cdot 10^{-6} \cdot 150^2 \cdot 40 \cdot 10^3 + (0.42^2 / 12) \cdot 52.6 = 9.77 \text{ W}$$

3.2.4 Experimental Verification

Relevant experimental waveforms at 55% duty cycle for the F2SA topology working in a non-resonant mode (MO1), and for the F2SB topology working in a quasi-resonant mode (MO1) are shown in Figs. 3.6 to 3.8, respectively. In

particular, Figs. 3.6 and 3.7 (a) illustrate the capacitor currents and voltages. It can be seen that the theoretical and experimental waveforms are in close agreement. Figs. 3.6 (b),(c), and 3.7 (b),(c) illustrate the switching losses of the main switch during the turn-on and the turn-off for both topologies. Figs. 3.6 (b),(c) show that for the F2SA topology (active snubber) the losses are negligible during the turn-on (ZVS performance) but not during the turn-off. This means that the speed of the switch and the parasitic capacitance in parallel are not enough to provide ZVS during the turn-off. The parasitic inductance in series, added when a sensor is used to measure the switch current, must also be reduced to reduce these losses.

Figs. 3.7 (b),(c) show that by using the quasi-resonant DRC snubber circuit (F2SB) switching losses exist during the turn-on but they are negligible during the turn-off. Experimental data for the regulation and efficiency measured on the experimental prototype for F2SB in MO1 are shown in Fig. 3.8(a) and (b), respectively. The average value of the voltage regulation for high load is 5.5% (open loop), and the maximum efficiency is 90% at 0.42 pu load (duty cycle 55%). For the F2SA topology the efficiency was 91% in MO1 and 92% in MO2 for the same load.
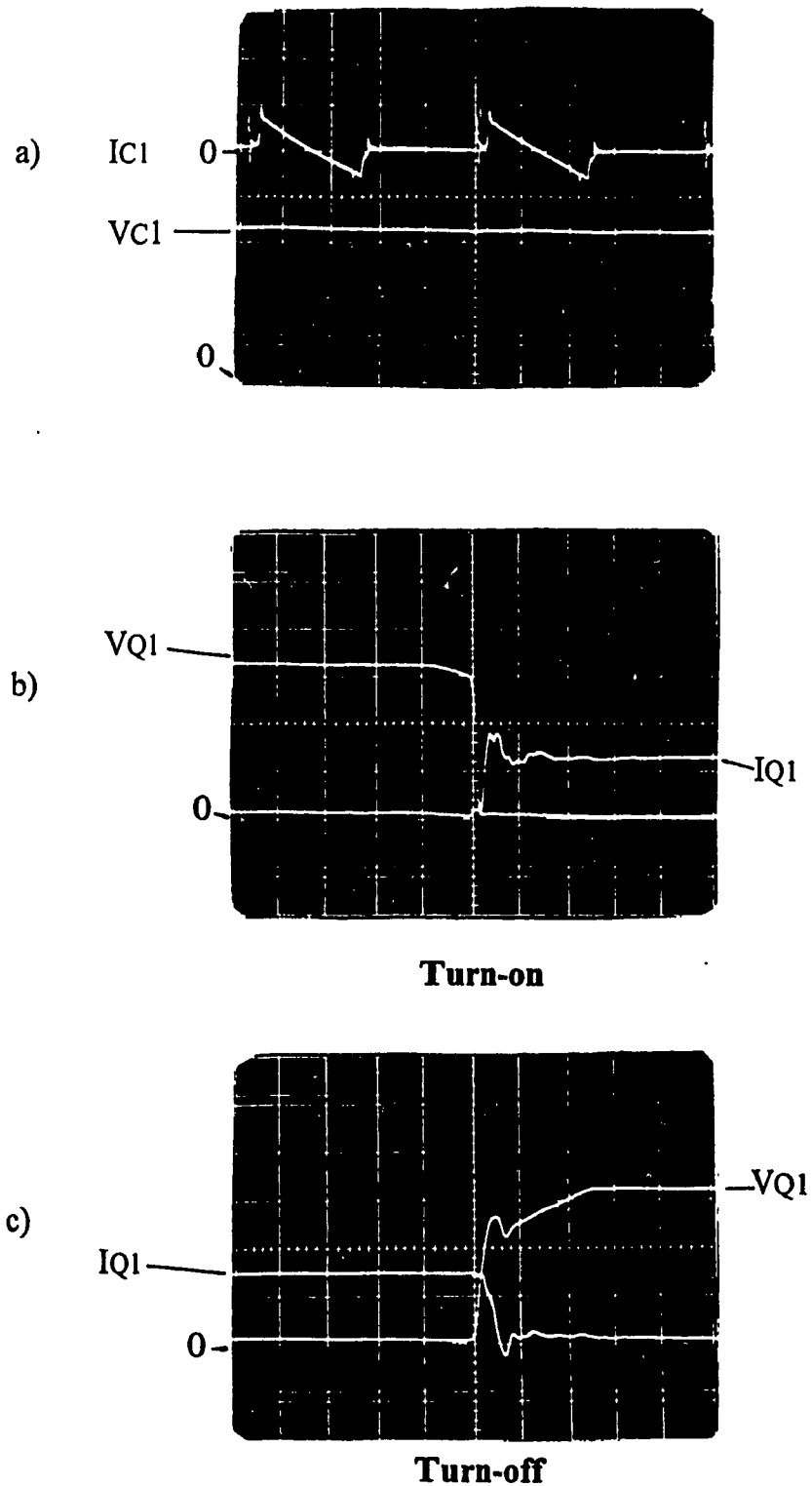
Turn-on

Turn-off

Figure 3.6. Experimental waveforms with the complementary switch topology. Non-resonant Mode design. a) Capacitor C1: Top: Ic1, 2 A/Div.; bottom: Vc1, 100 V/Div.; Time: 10 µs/Div. b) Main switch Q1, Turn-on: IQ1, 20 A/Div; VQ1, 100 V/Div.; c) Main switch Q1, Turn-off: IQ1, 20 A/Div.; VQ1, 100 V/Div.

a) IC1 0 —

Vc1 —

0 —

b) VQ1 —

0 —

IQ1

Turn-on

c) IQ1 —

0 —

VQ1
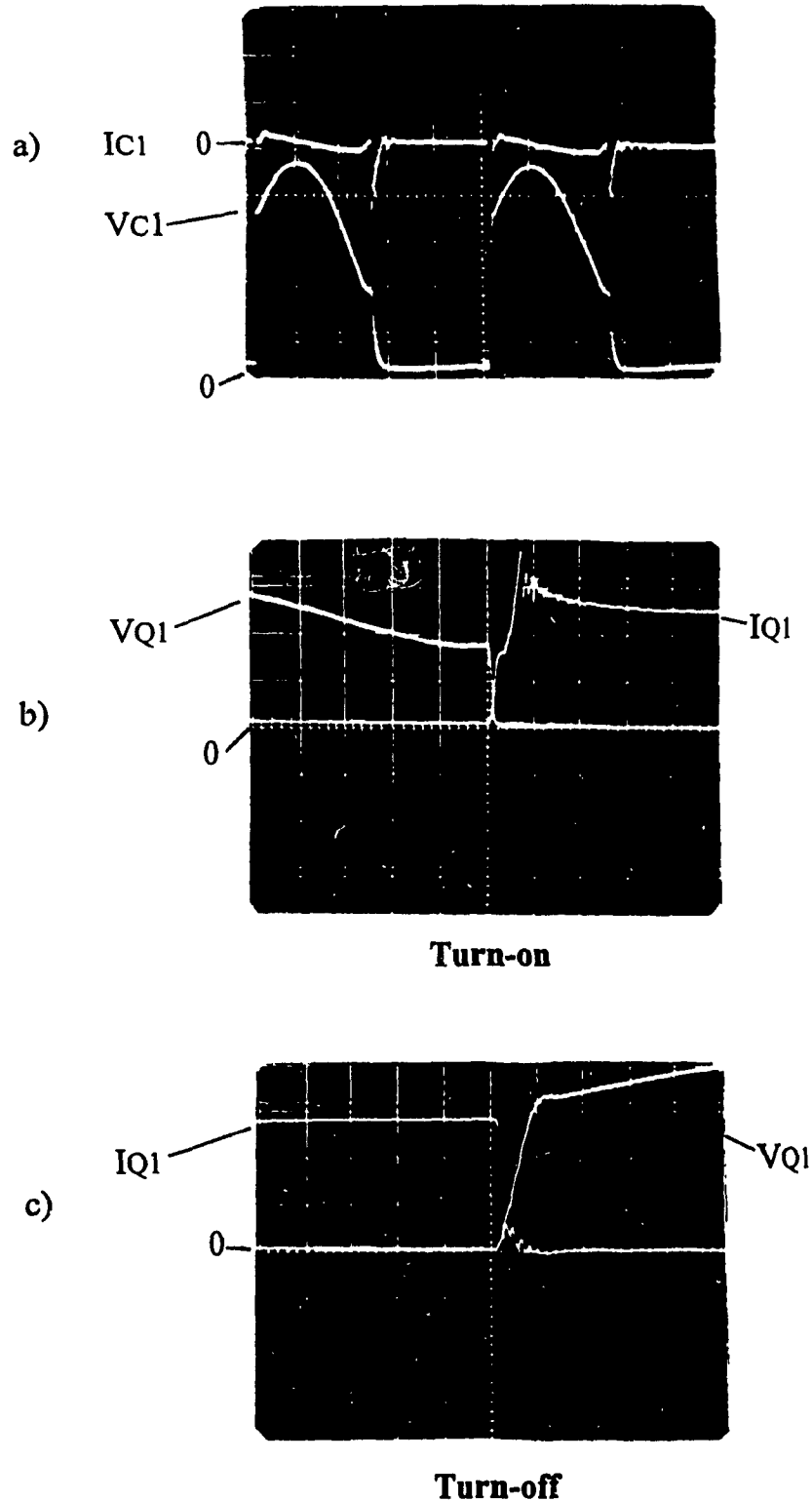
Turn-off

Figure 3.7. Experimental waveforms with the DRC snubber topology. Quasi-resonant Mode design a) Capacitor C1: Top: Ic1, 10 A/Div; bottom: Vc1, 100 V/Div; Time: 10 µs/Div. b) Main switch Q1,Turn-on: IQ1, 20 A/Div.; VQ1, 100 V/Div.; c) Main switch Q1, turn-off: IQ1, 20 A/Div; VQ1, 100 V/Div.
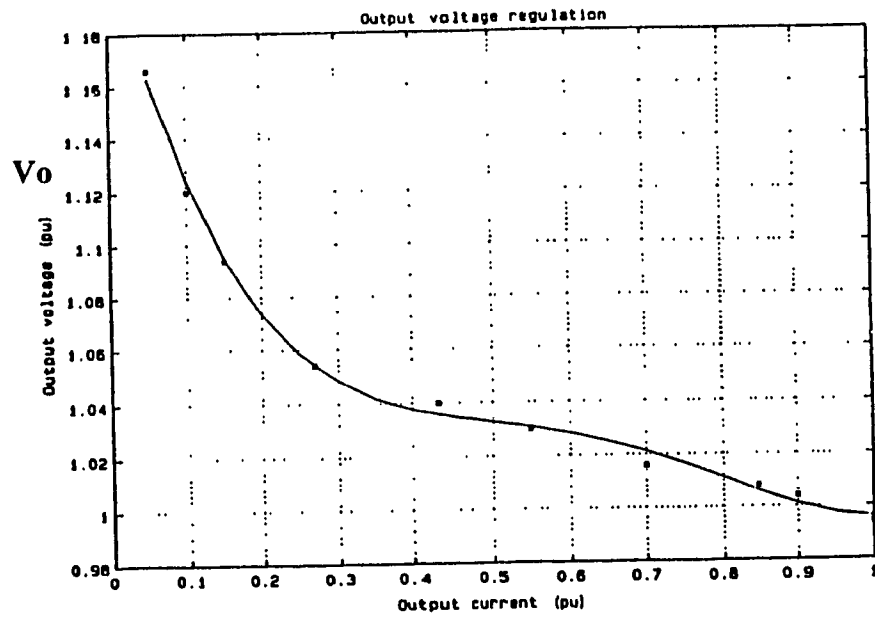
(a)
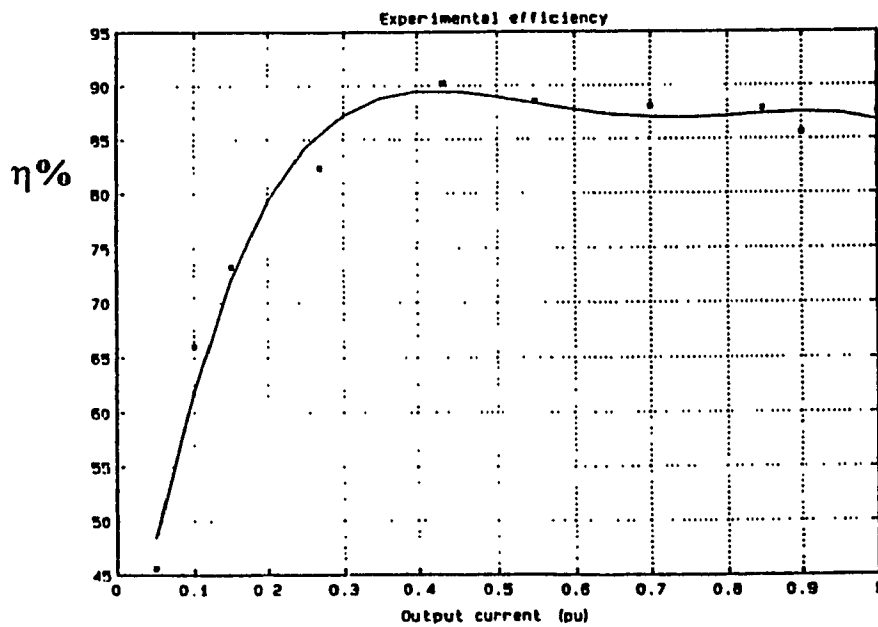
(b)

Figure 3.8 Experimental output voltage and efficiency in term of the load current. DRC quasi-resonant design. a) Output voltage regulation. b) Efficiency $\eta\%$.

3.3   Topology II: Two-Switch Hybrid-Bridge

In this section a novel HF-ZVS-PWM single-ended forward DC/DC converter for medium-power application is proposed. The circuit diagram is shown in Fig. 3.9. This topology is called here two-switch hybrid-bridge forward converter. This converter works with two switches in parallel during most of the turn-on cycle, thus controlling more power than the typical single-switch converter. Further, it has the combined advantages of a quasi-resonant boost and a PWM forward converter. The main features include near-zero switching losses, a reduced component count, fixed frequency PWM operation, and a low-average switch current. This section presents the analysis of this converter when either a half-bridge or a full-bridge rectifier is used on the secondary of the HFT. The performance of this converter operating in a discontinuous current mode is investigated and a design procedure is proposed, and illustrated by an example. Finally, to verify the theory, simulated and experimental results are presented for a 1 kW, 40 kHz prototype unit.

3.3.1   Principles of Operation

Figure 3.9 shows a simplified version of the power circuit using the 'T' modeling circuit for the HF transformer. The inductor L_m represents the magnetizing inductance, while L_1 and L_2 represent the primary and secondary leakage inductances and any other inductance in series with them. In this model, the output rectifier, the output filter, and the load are reflected to the primary side.
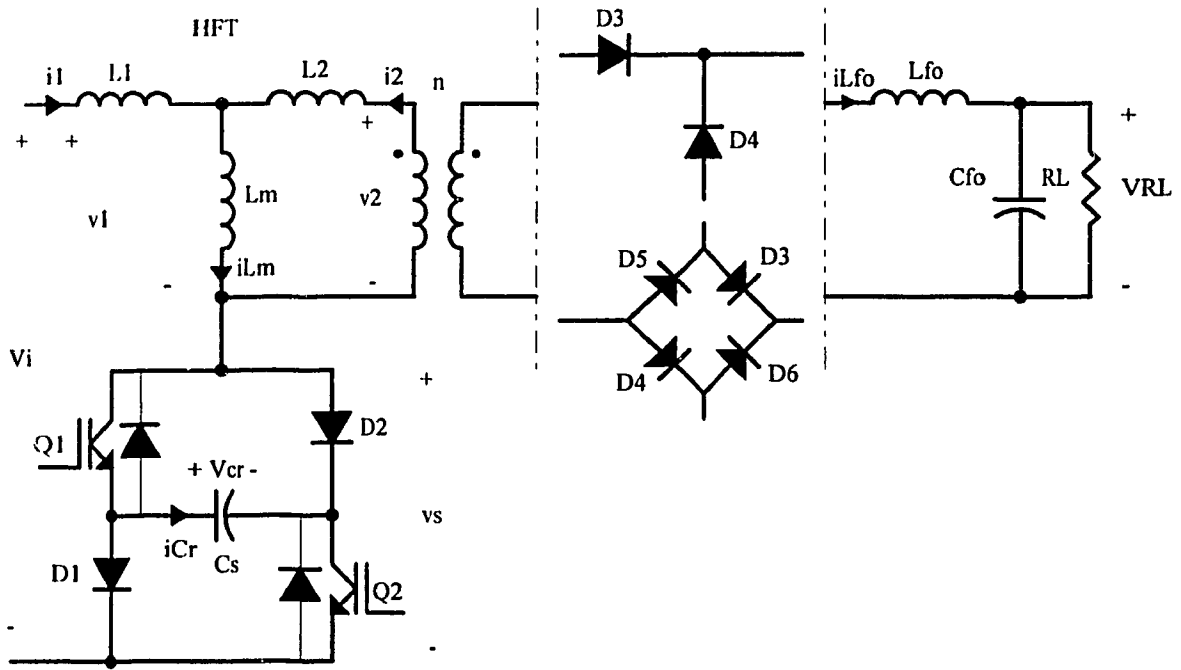
$$Lr = n^2 \cdot Lfo$$

$$iLr = \frac{iLfo}{n}$$

$$vo = n \cdot vRL$$

Figure 3.9 The proposed two-switch hybrid-bridge single-ended forward converter. A full-bridge or a half-bridge rectifier is used on the secondary of the HF transformer.

The two power switches, Q1 and Q2 (BIPOLAR or IGBT), are connected in series with the two HF diodes, D1, D2, and the primary of the HF transformer. Both switches are controlled by the same PWM gating signal. The Lr is a low value output filter inductance, and Cr is the snubber capacitor.

A.   Converter Operation Using a Half-Bridge Rectifier

The different topological modes identified in sequence for this case are shown in Fig. 3.10 (a). Typical current waveforms illustrating the time-interval for each of them are shown in Fig. 3.10 (b). The operation of the converter is described hereafter.

Mode M1 Interval t =[0,t1]: At t = 0, the initial voltage across the capacitor Cr is negative, and all the inductors have zero currents. At this time transistors Q1 and Q2 are turned ON and the voltage across the switch becomes zero. Since Cr has a negative initial voltage, both switches start conducting in series. The inductors L1, L2, and Lr produce a high frequency series resonance with the capacitor Cr. The output filter capacitor Co does not affect the frequency of this resonance because it is much larger than Cr.   As a result of this resonance, the current through the switches increases from zero sinusoidally, reducing switching losses during the turn-on. At the same time, the voltage across the capacitor Cr decreases also sinusoidally. Finally, at t=t1 the two diodes D1, D2, and the internal diodes of the switches are forward biased by the reversing polarity of the capacitor, so that they
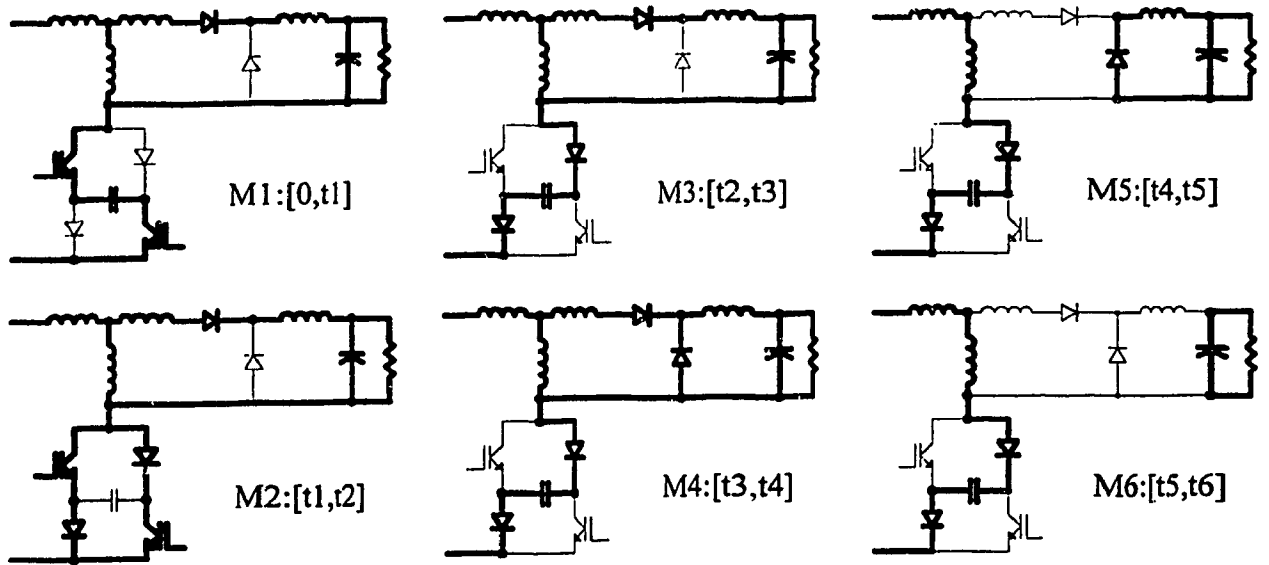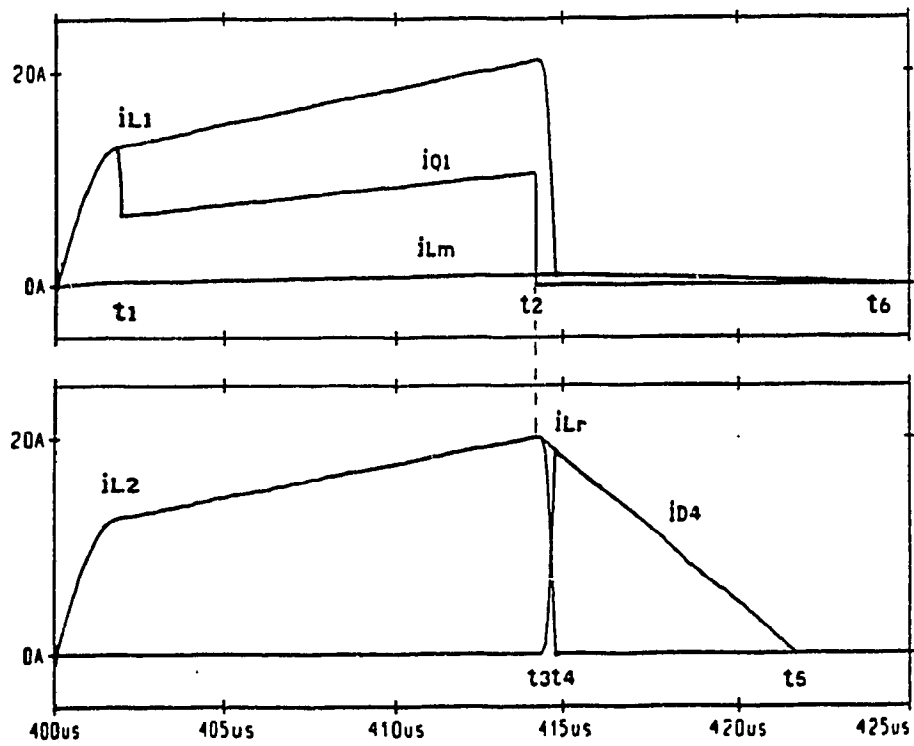
Figure 3.10 Topological Modes and analytical current waveforms during a steady state switching cycle when a half-bridge rectifier is used.

clamp the voltage across the capacitor Cr close to zero volt.

Mode M2 Interval t =[t1,t2]: After t = t1, switches Q1 and Q2 are connected in parallel through diodes D1 and D2, and the current through Cr is zero. Energy is transferred from the source to the load as in a forward converter, but with both switches carrying only half of the load current.

Mode M3 Interval t = [t2,t3]: Immediately after t =t2, switches Q1 and Q2 are turned off, and diodes D1 and D2 are connected in series with Cr thus conducting the load and the magnetizing current of the HF transformer. The voltage across the capacitor Cr changes to a negative value with a limited slope, depending on the values of Cr, L1, Lr, L2, and the load current. This process provides a ZVS transition for both switches thus minimizing the switching losses during turn-off. In addition, the energy stored in L1, Lr, and L2 is transferred to the load, Co, and Cr as in a resonant-boost converter.

Mode M4 Interval t = [t3,t4]: Immediately after t = t3, Diode D4 starts conducting and the output voltage of the transformer is clamped to zero until all the energy stored in L1 and L2 is transferred to the capacitor Cr after which Diode D3 is off.

Mode M5 Interval t =[t4, t5]: Diode D4 assumes the role of a free-wheeling diode at t = t3 in Mode 4, allowing energy stored in the output filter inductance Lr to be transferred to the output filter capacitor and the load. In order to avoid high peak

currents during Mode 1, the energy in Lr should be eliminated before t = T (discontinuous current in the output filter).

Mode M6 Interval t =[t5, t6]: After t = t4, the HFT is disconnected from the output filter and the magnetizing energy is storage on the resonant capacitor Cr. Before the end of the switching cycle, the magnetizing current is zero (t6 ≤ T). After that, diodes D1 and D2 stop conducting and the capacitor voltage, VCr (t6), is at its maximum value.

B.   Converter Operation Using a Full-Bridge Rectifier

The main difference between using a half-bridge rectifier (HBR) and a full-bridge rectifier (FBR) is that, with the latter, most of the magnetizing energy is sent to the load during the turn-off cycle. As a result, lower switch overvoltages (almost twice the input voltage) can be obtained. The TCM's identified in sequence for this case are shown in Fig. 3.11 (a). Typical current waveforms illustrating the time-interval for each of them are shown in Fig. 3.11 (b). Modes M1, M2, M3, and M4 are identical to these already described in the previous section , the differences begin in mode M5.

Mode M5 Interval t =[t4, t5]: The output rectifier is a short circuit while the energy stored in Lr is being transferred to the load. As a result, the magnetizing current free-wheeling through the secondary of the HFT until t = t5 when the current through Lr becomes equal to the magnetizing current.
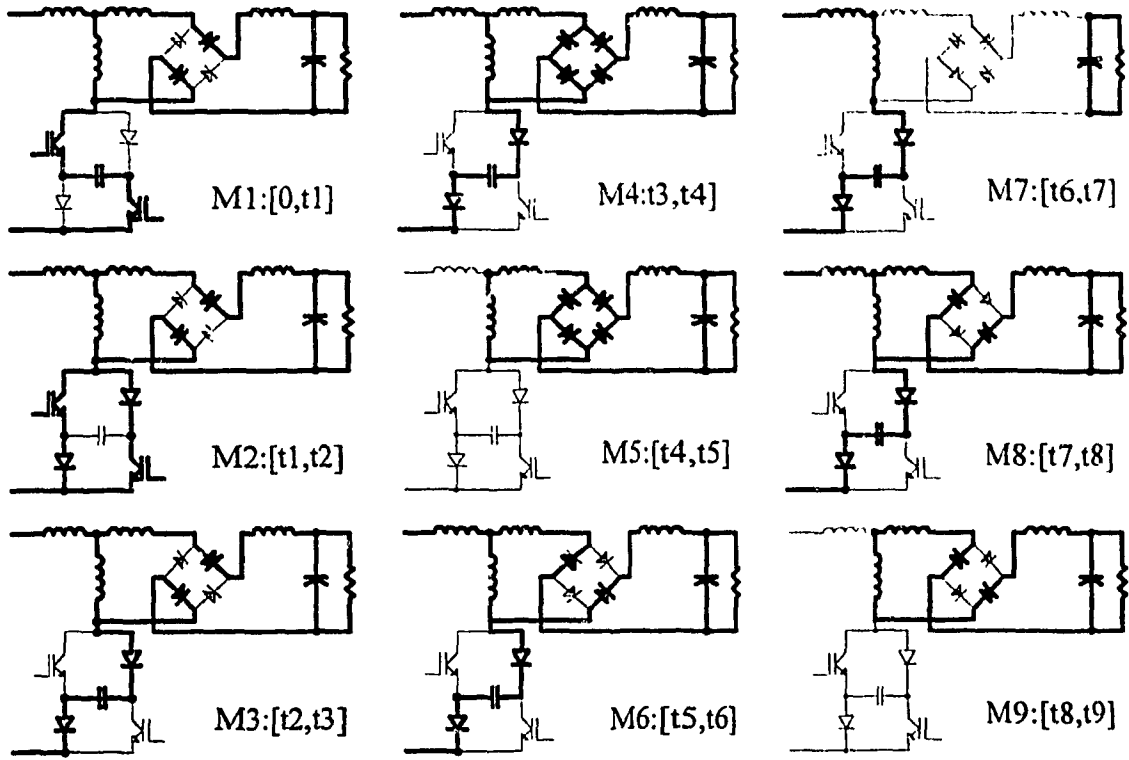
(a)
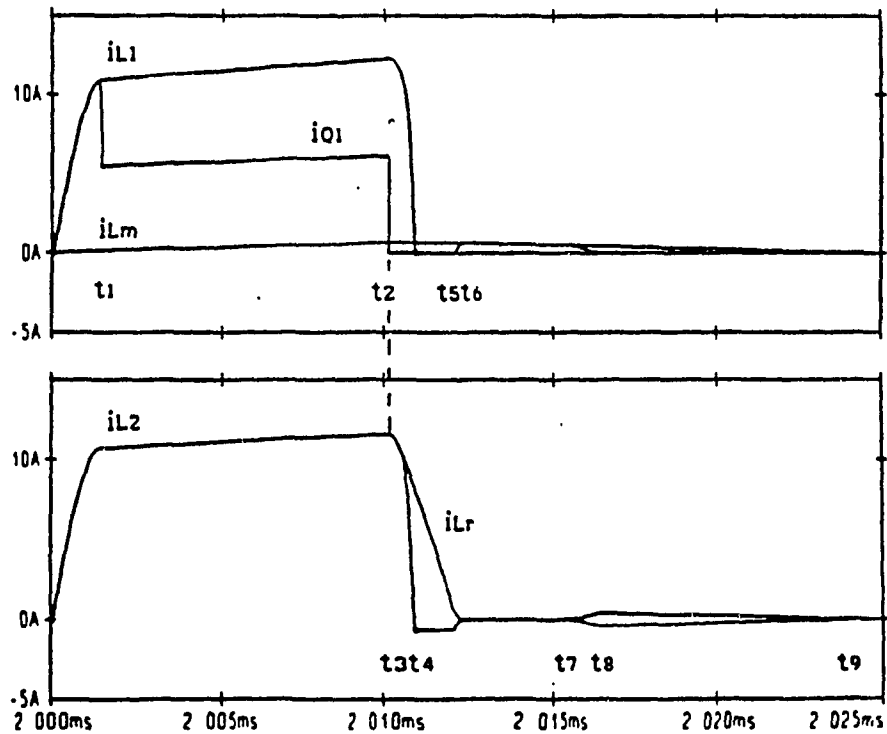
(b)

Figure 3.11 Topological Modes and analytical voltage/current waveforms during a switching cycle when a full-bridge rectifier is used.

Mode M6 Interval t =[t5, t6]: Diodes D1, D2, D5, and D6 start conducting, and diodes D3 and D4 are off. The magnetizing current circulates now through capacitor Cr and the inductances Lr and L2 until t = t6.

Mode M7 Interval t = [t6, t7]: After t = t6, iLr(t)=0 and diodes D3, D4, D5 and D6 are off. Therefore, the output filter and the load are disconnected from the secondary of the HFT, and all the magnetizing current circulates through Cr.

Mode M8 Interval t = [t7, t8]: At t = t7, the two diodes D5 and D6 of the output rectifier are forward biased. Therefore, the filter and the load are connected again to the secondary side of the HF transformer. The magnetizing current circulates toward both the load and Cr. When all the energy stored in L1 is transferred to the capacitor Cr, diodes D1 and D2 are off, and the voltage across the capacitor Cr is at its maximum value.

Mode M9 Interval t = [t8, t9]: Only diodes D5 and D6 are ON, so that the secondary of HF transformer is connected to the output circuitry and the primary is an open circuit. Therefore, the rest of the magnetizing energy is sent to the output filter capacitor and the load as a flyback converter.

3.3.2 Power Converter Analysis

The state equations and the respective voltage and current solutions for all TM's identified in Sections *A* and *B* above are obtained hereafter. It is assumed that the circuit includes a linear transformer without losses, ideal switches and diodes,

and a ripple-free constant output voltage. Also, to account for the variable structure of the circuit during a switching cycle, two switching variable, $\delta 1$ for the rectifier and $\delta 2$ for the switches, are introduced. These variables assume the values 1, 0, -1. Hence, from Fig. 3.9

$$iLr(t) = i2(t)\delta 1 \tag{3.3.1}$$

$$v1(t) = Vi-vs(t) \tag{3.3.2}$$

$$i1(t) = Crvs(t) \tag{3.3.3}$$

$$vCr(t) = vs(t)\delta 2 \tag{3.3.4}$$

$$iCr(t) = i1(t)\delta 2 \tag{3.3.5}$$

$$iLm(t) = i1(t) + i2(t) \tag{3.3.6}$$

The state equation modeling the transformer with the output rectifier, and filter included is shown to be

$$\begin{bmatrix} L1 + Lm & Lm \\ Lm & L2 + Lm + Lr\delta_1^2 \end{bmatrix} \cdot \frac{d}{dt}\begin{bmatrix} i1 \\ i2 \end{bmatrix} = \begin{bmatrix} Vi- vs(t) \\ Vo\delta_1 \end{bmatrix} \tag{3.3.7}$$

Integration of (3.3.7) with $Vs(t) = 0$ gives the solution of the non-resonant modes. This solution is shown to be

$$\begin{bmatrix} i1(t) \\ i2(t) \end{bmatrix} = \begin{bmatrix} \dfrac{L2 + Lm + Lr\delta_1^2}{\Delta 1} & -\dfrac{Lm}{\Delta 1} \\ -\dfrac{Lm}{\Delta 1} & \dfrac{L1 + Lm}{\Delta 1} \end{bmatrix} \cdot \begin{bmatrix} Vi \\ Vo\delta_1 \end{bmatrix} + \begin{bmatrix} i1(tn) \\ i2(tn) \end{bmatrix} \tag{3.3.8}$$

where $\Delta 1$ is the determinant of the inductance matrix in (3.3.7) and is given by

$$\Delta 1 = (L2 + Lm + Lr\delta_1^2)(L1 + Lm) - Lm^2 = L1L2 + L2Lm + (L1 + Lm)Lr\delta_1^2 + LmL1 \tag{3.3.9}$$

The vector $[i1(tn), i2(tn)]^T$ are the initial inductances currents. To obtain the state equations for the resonant modes, i2 is eliminated from (3.3.7), then by using (3.3.2) and (3.3.3), it is found that

$$\frac{d}{dt}\begin{bmatrix} i1(t) \\ vs(t) \end{bmatrix} = \begin{bmatrix} 0 & \dfrac{L2 + Lm + Lr\delta_1^2}{\Delta 1} \\ \dfrac{1}{Cr} & 0 \end{bmatrix} \cdot \begin{bmatrix} i1(t) \\ vs(t) \end{bmatrix} + \begin{bmatrix} \dfrac{L2 + Lm + Lr\delta_1^2}{\Delta 1} & -\dfrac{Lm}{\Delta 1} \\ 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} Vi \\ Vo\delta 1 \end{bmatrix} \quad (3.3.10)$$

Therefore, the independent solution for each resonant modes becomes

$$\begin{bmatrix} i1(t) \\ vs(t) \end{bmatrix} = \begin{bmatrix} \cos\omega 1 & -\dfrac{1}{Z}\sin\omega t \\ Z\sin\omega t & \cos\omega t \end{bmatrix} \cdot \begin{bmatrix} i1(tn) \\ vs(tn) \end{bmatrix} + \begin{bmatrix} \dfrac{1}{Z}\sin\omega t & -\dfrac{A}{Z}\sin\omega t \\ 1-\cos\omega t & A(\cos\omega t - 1) \end{bmatrix} \cdot \begin{bmatrix} Vi \\ Vo\delta 1 \end{bmatrix} \quad (3.3.11)$$

With $\delta 1 = \pm 1$:

$$A = A1 = \frac{Lm}{Ls1}, \quad \omega = \omega 1 \frac{1}{\sqrt{Le1Cr}}, \quad Z = Z1 = \sqrt{\frac{Le1}{Cr}}, \quad Le1 = \frac{\Delta 1}{Ls1} \quad (3.3.12)$$

Where $Ls1 = L2 + Lm + Lr$

With $\delta 1 = 0$:

$$A = A2 = \frac{Lm}{Ls2}, \quad \omega = \omega 2 = \frac{1}{\sqrt{Le2Cr}}, \quad Z = Z2\sqrt{\frac{Le2}{Cr}} \quad (3.3.13)$$

Where $Le2 = \dfrac{\Delta 2}{Ls2}$, $Ls2 = L2 + Lm$, and $\Delta 2 = \Delta 1_{\delta 1=0}$

In the case of a resonant mode with i2(t)=0 (the secondary of the HFT is open circuited), the solution is obtained from (3.3.11) by making L2 an infinitive value, and $\delta 1 = 0$. Therefore, (3.3.11) is reduced to

$$\begin{bmatrix} i1(t) \\ vs(t) \end{bmatrix} = \begin{bmatrix} \cos\omega3t & -\dfrac{1}{Z3}\sin\omega3t \\ Z3\sin\omega3t & \cos\omega3t \end{bmatrix} \cdot \begin{bmatrix} i1(tn) \\ vs(tn) \end{bmatrix} + \begin{bmatrix} \dfrac{1}{Z3}\sin\omega3t \\ 1-\cos\omega3t \end{bmatrix} \cdot Vi \quad (3.3.14)$$

where $\omega3 = \dfrac{1}{\sqrt{Le3Cr}}$, $Z3 = \sqrt{\dfrac{Le3}{Cr}}$ and $Le3 = L1 + Lm$ (3.3.15)

A. Design Parameters

For simplicity, the following design parameters are introduced :

$$K1 = \frac{L1}{Lm} \qquad\qquad (a) \qquad\qquad (3.3.16)$$

$$K2 = \frac{L2}{Lm} \qquad\qquad (b)$$

$$Kr = \frac{Lr}{Lm} \qquad\qquad (c)$$

$$Ke1 = \frac{Le1}{Lm} = \frac{K1K2 + K2(K1+1)Kr + K1}{K2 + Kr + 1} \qquad\qquad (a) \qquad\qquad (3.3.17)$$

$$Ke2 = \frac{Le2}{Lm} = \frac{K1K2 + K2 + K1}{K2 + 1} \qquad\qquad (b)$$

$$Ke3 = \frac{Le3}{Lm} = K1 + 1 \qquad\qquad (c)$$

$$Ks1 = \frac{Ls1}{Lm} = K2 + Kr + 1 \qquad\qquad (a) \qquad\qquad (3.3.18)$$

$$Ks2 = \frac{Ls2}{Lm} = K2 + 1 \qquad\qquad (b)$$

$$B1 = \frac{K2 + Kr}{K2 + Kr + 1} \qquad\qquad (a) \qquad\qquad (3.3.19)$$

$$B2 = \frac{K2}{K2 + 1} \qquad\qquad (b)$$

$$B3 = \frac{K1}{K2 + Kr} \qquad \text{(c)}$$

$$Zm = \sqrt{\frac{Lm}{Cr}} \qquad \text{(a)} \qquad (3.3.20)$$

$$\omega m = \frac{1}{\sqrt{LmCr}} \qquad \text{(b)}$$

Therefore, the characteristic impedance and the resonant frequency of the resonant modes can be expressed in terms of the above parameters as follows

$$Z1 = Zm\sqrt{Ke1} \qquad \text{(a)} \qquad (3.3.21)$$

$$Z2 = Zm\sqrt{Ke2} \qquad \text{(b)}$$

$$Z3 = Zm\sqrt{Ke3} \qquad \text{(c)}$$

$$\omega1 = \frac{\omega m}{\sqrt{Ke1}} \qquad \text{(a)} \qquad (3.3.22)$$

$$\omega2 = \frac{\omega m}{\sqrt{Ke2}} \qquad \text{(b)}$$

$$\omega3 = \frac{\omega m}{\sqrt{Ke3}} \qquad \text{(c)}$$

and for the non-resonant modes

$$Zr = 2\pi Kr \frac{Zm}{\omega m} \qquad \text{(a)} \qquad (3.3.23)$$

$$Zs1 = 2\pi Ls1 = 2\pi (K2 + Kr + 1)\frac{Zm}{\omega m} \qquad \text{(b)}$$

With these arrangement the parameters to design the circuit are reduced to K1, K2, Kr, Zm and ωm.

B.   Normalized Equations

The current and voltage equations including component values are normalized with respect to the following base values :

1   pu voltage = input voltage : $Vi=V_b$

1   pu current=maximum average load current: $Io=I_b$

1   pu frequency=switching frequency : $fs = \dfrac{1}{T} = f_b$

Hence : $Zb = \dfrac{V_b}{I_b} = \dfrac{Vs}{Io}$, $Lb = \dfrac{Z_b}{2\pi fs}$, $Cb = \dfrac{1}{2\pi fsZb}$

$$d = \frac{t}{T}, \qquad \omega = F = \frac{f}{fs}, \qquad Z = L \ \ pu$$

The respective normalized voltage and current equations are summarized in Appendix A2

3.3.3   Design Procedure

The design is reduced to find the optimum values for K1, K2, Kr, Zm, ω_m and a maximum duty cycle for given values of input-output voltage and output current upon the following constraints :

1) Discontinues output filter current;

2) Zero transformer magnetizing current at the end of the switching cycle;

3) Minimum peak-voltage across switches during turn-off.

A.   Using a Half- Bridge Rectifier (HBR)

To illustrate the performance of the proposed converter with a HBR the set of equations presented in Appendix A2 have been solved regarding the above constraints and different values of Zm and Kr. It is assumed that $K_1=K_2=0.00017$, $\omega_m=0.42$, $V_o=0.8V_i$. The results are summarized in **Table 3.3-I**, Fig. 3.12 and 3.13. On can conclude that in order to obtain a minimum maximum-switch voltage at 1 pu output current, Zm must be in the range $19<Z_m<24$, and Kr in the range $0.010<K_r<0.016$. With $Z_m=23.7$ and $K_r=0.015$ the maximum duty cycle (d_{2max}) at 1 pu load (I_{Lravg}) is 0.55, and the maximum-switch voltage (V_{Qmax}) is equal to 3.09 times the input voltage, but the average current through each switch (I_{Qavg}) is only 41% of the load current which is the main advantage of the proposed converter.

Table 3.3-I

Converter Design Using a Half-Bridge Rectifier, Values are in pu

Zm	37.5			23.70			18.75		
Kr	0.017			0.015			0.008		
d2	0.40	0.50	0.55	0.40	0.50	0.55	0.40	0.50	0.55
d5	0.63	0.77	0.84	0.65	0.79	0.86	0.62	0.76	0.83
d6	0.67	0.78	0.83	0.80	0.92	0.97	0.84	0.95	1.00
VQmax	3.39	3.86	4.11	2.64	2.94	3.09	2.38	2.65	2.78
IQmax.	0.73	0.83	0.88	0.97	1.08	1.13	1.51	1.67	1.75
IQavg	0.19	0.28	0.34	0.25	0.35	0.41	0.39	0.56	0.66
Vdmax.	3.39	3.86	4.11	2.64	2.94	3.09	2.38	2.65	2.78
Id1max	1.22	1.46	1.58	1.49	1.75	1.88	2.44	2.87	3.09
ILravg.	0.49	0.71	0.84	0.62	0.88	1.03	0.98	1.41	1.65
ILrrms	0.66	0.87	0.98	0.83	1.07	1.19	1.34	1.73	1.94
$V_o=0.8V_1, K_1=K_2=0.00017, \omega_m=0.42$									

F(Kr,d2,-Vcr), Vo=0.8Vi

a)

F(Kr,d2,Ir), Vo=0.8Vi
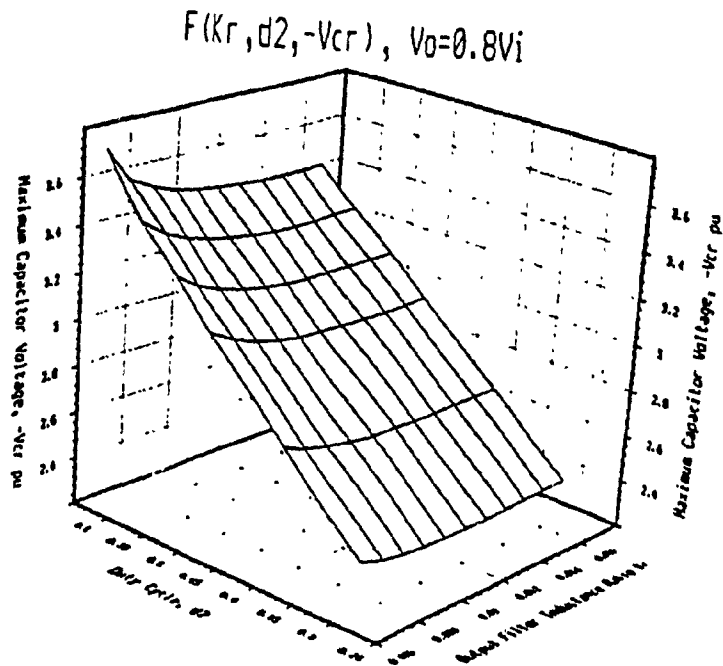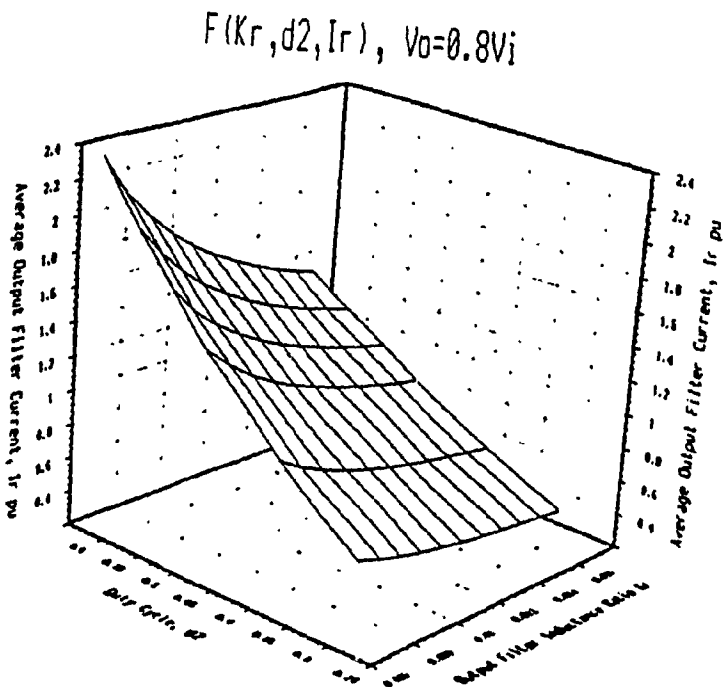
b)

Figure 3.12 Operating Characteristics of the two-switch forward converter with a half-bridge rectifier.

Control to Output Current DC Characteristic
Vo=0.8Vi, K1=L1/Lm=K2=L2/Lm=0.00017
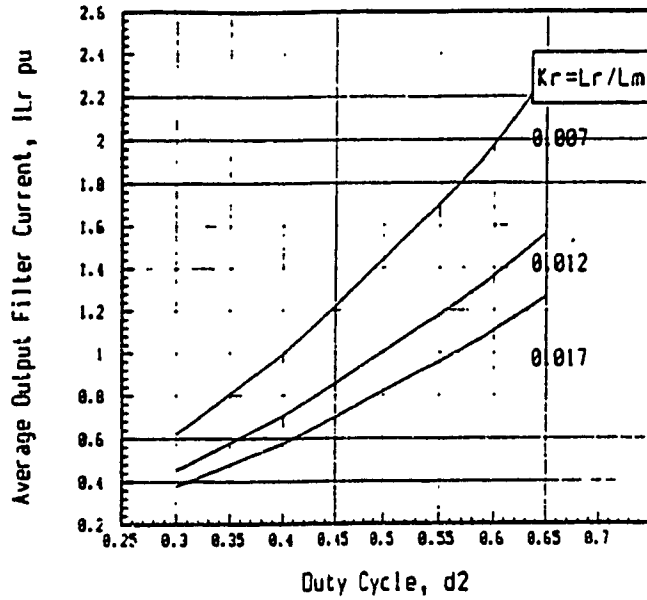
Duty Cycle, d2

a)

Ripple of the Output Filter Current (pu)

Output Filter Inductance Ratio, Kr
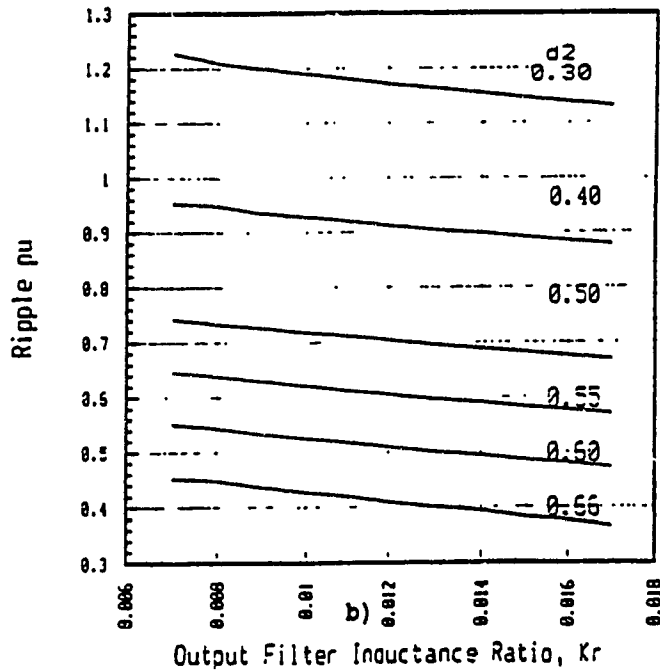
b)

Figure 3.13 Output Characteristics of the two-switch forward topolpogy with a half-bridge rectifier.

The effect of Kr and duty cycle on the maximum-switch voltage and output average current (Zm=23.7) are illustrated by the surfaces shown in Fig. 3.12. One can see that increasing Kr reduces the maximum switch-voltage (Fig. 3.12 a)), but the average output current decreases (Fig. 3.12 (b)). Moreover, the control to output current characteristic for three different values of Kr are given in Fig 3.13 (a). It shows that the non-linearity is insignificant for a Kr≥0.012. Finally, increasing Kr also decreases the ripple factor of the output current which is shown in Fig. 3.13 (b).

B.   Using a Full-Bridge Rectifier (FBR)

The proposed PWM converter with a FBR can be designed to support a maximum switch voltage equal to V0+Vi by selecting the parameters K1, K2, Kr, Zm, ωm to generate the sequence of modes M1, M2, M3, M4, M5 and M9 (Fig. 3.11) at the rating load and maximum duty cycle. The respective voltage and current equations regarding the above conditions are presented in Appendix A2. It is found that with, a small difference between Vo and Vi, the maximum voltage across the switch becomes close to two times the input voltage, and the peak current during Mode 1 is reduced. This is an important design requirement in this configuration because Kr must be small to minimize the duration (d5-d4) of Mode 5 during the turn-off time.

It should be noted that the circuit can be designed to operate in a buck mode

if Vo<Vi, a boost mode if Vo>Vi or in a 'neutral' mode if Vi=Vo. **Table 3.3-II**

summarizes the results obtained with Vo=0.9Vi, $K_1= K_2=0.00017$, $K_r=0.0045$, ω_m

= 0.42, and different Z_m.

Table 3.3-II

Converter Design Using a Full-Bridge Rectifier, Values are in pu

Z_m	8.00	10.00	12.00	14.00	16.00	18.00	20.00
ILm_{max}	0.15	0.12	0.10	0.09	0.07	0.07	0.06
IQ_{max}	3.76	3.01	2.51	2.15	1.88	1.67	1.50
Id_{max}	6.32	5.06	4.22	3.61	3.16	2.70	2.43
ILr_{avg}	2.22	1.77	1.47	1.26	1.11	0.98	0.89

d2max=0.4, output load =1pu
Vo=0.9, K1=K2=0.00017, Kr=0.0045, Wm=0.42

One can see that, to obtain 1 pu load current, Z_m must be less than 19 pu. Also,

due to Mode 5, the resulting maximum duty cycle is less than 50% (d2=0.40).

However, as compared with the previous case, the maximum voltage across the

switches is only 1.9 times the input voltage which is one important

advantage of this configuration.

3.3.4 Design Example and Simulation Results

To illustrate the results of the analysis, a design example is worked out

based on the following design specifications :

1)   Input voltage Vi=100 V

2)   Input voltage Vo=50 V

3)   Output power Po=1000 W

4) Switching frequency fs=40 kHz

In order to use the results presented in **Table 3.3-I** and **Table 3.3-II** it is assumed a buck mode of operation, and a voltage reflected to the primary side Vo=80 V with a Half-Bridge Rectifier, and Vo=90 V with a Full-Bridge Rectifier. Assuming a 90% efficiency (η) the components values and the ratings of the circuit are obtained as follows :

	Half bridge rectifier	**Full bridge rectifier**
Base Values		
Vo	80	90
$Io = \dfrac{Po}{\eta Vo}$	$\dfrac{1000}{0.9 \cdot 80} = 13.88$	$\dfrac{1000}{0.9 \cdot 90} = 12.34$
$Zb = \dfrac{Vo}{Io}$	$\dfrac{80}{13.88} = 5.76$	$\dfrac{90}{12.34} = 7.29$
Lb	22.92μH	29.00μH
Cb	0.69μF	0.55μF
Inductances, primary side		
$Lm(pu) = \dfrac{Zm}{\omega m}$	$\dfrac{23.7}{0.42} = 56.43$	$\dfrac{18.0}{0.42} = 42.85$
Lm(uH)=Lm(pu)·Lb	56.43·22.92=1293μH	42.85·29.00=1242μH
Lr=Kr·Lm	0.015·1293=19.39μH	0.0045·1242=5.58μH
Resonant Capacitor		
$Cr(pu) = \dfrac{1}{Zm\omega m}$	$\dfrac{1}{23.7 \cdot 0.42} = 0.10$	$\dfrac{1}{18.0 \cdot 0.42} = 0.13$

Cr(uF)	0.10·0.69=0.069µF	0.13·0.55=0.072µF

Switches and Diodes

IQmax.	1.13·13.88=15.68A	1.67·12.34=20.60 A
IQavg.	0.41·13.88=5.69 A	0.55·12.34=6.82 A
ID1max.=ID2max.	1.88·13.88=26.09 A	2.70·12.34=33.32 A
VQmax=VD1max.	3.09·100=309 V	90+100=190 V

Transformer ratio and
Maximum duty cycle

$n = \dfrac{Vo}{Vout}$	$\dfrac{80}{50} = 1.6$	$\dfrac{90}{50} = 1.8$
δ	0.55	0.40

Simulation results (PSPICE) for both cases are shown in Figs. 3.14 and 3.15. It shows that, when a FBR is used instead of a HBR for the same output power, the maximum currents through the switches and diodes are 31% higher, the average current through the switches and diodes are 20% higher, but the voltage stresses are 39% lower. Moreover, Fig. 3.16 illustrates that, in the case of using a full-bridge rectifier, the DC current gain (ILravg./Iiavg.) can be increased substantially by decreasing the value of the magnetizing inductance.

3.3.5 Experimental Verification

To establish the feasibility of the proposed converter topology and to verify the selected theoretical results, a 1-kW prototype unit operating at 40 kHz

switching frequency, with both a HBR and FBR, was built and tested. Key experimental results are shown in Figs. 3.17, and 3.18. The results are in close agreement with the predicted and simulated waveforms. However a ringing oscillation exist in the switch current due to the parasitic inductance of the switch-diode path which must be minimized. The experimental maximum-switch-voltage using a HBR was $3.2V_i$ and using FBR was $2.2V_i$. It verified also that the turn-on and turn-off switching losses are very low. Maximum experimental efficiency was 91% with a HBR and 90% with a FBR, at 0.8pu load.

3.4 Summary

In the first section of this Chapter, the active snubber circuit analyzed in Chapter two have been used to build a modified low losses two-switches single-ended forward topology without the feedback diodes. If the n-p complementary switch is used, the converter can be designed to operate in a non-resonant or in a quasi-resonant mode. The non-resonant design provides the lower voltage stress to the switches. However, the switching losses during turn off may not be minimized. The quasi-resonant design reduces the switching losses almost to the half, but the voltage stresses in the switches are higher. On the other hand, a quasi-resonant mode with ZVS feature is possible for the proposed topology by using the standard DRC snubber properly designed.

Furthermore, these circuits have been designed to minimize the DC magnetizing current of the HF transformer and to provide extended duty cycle
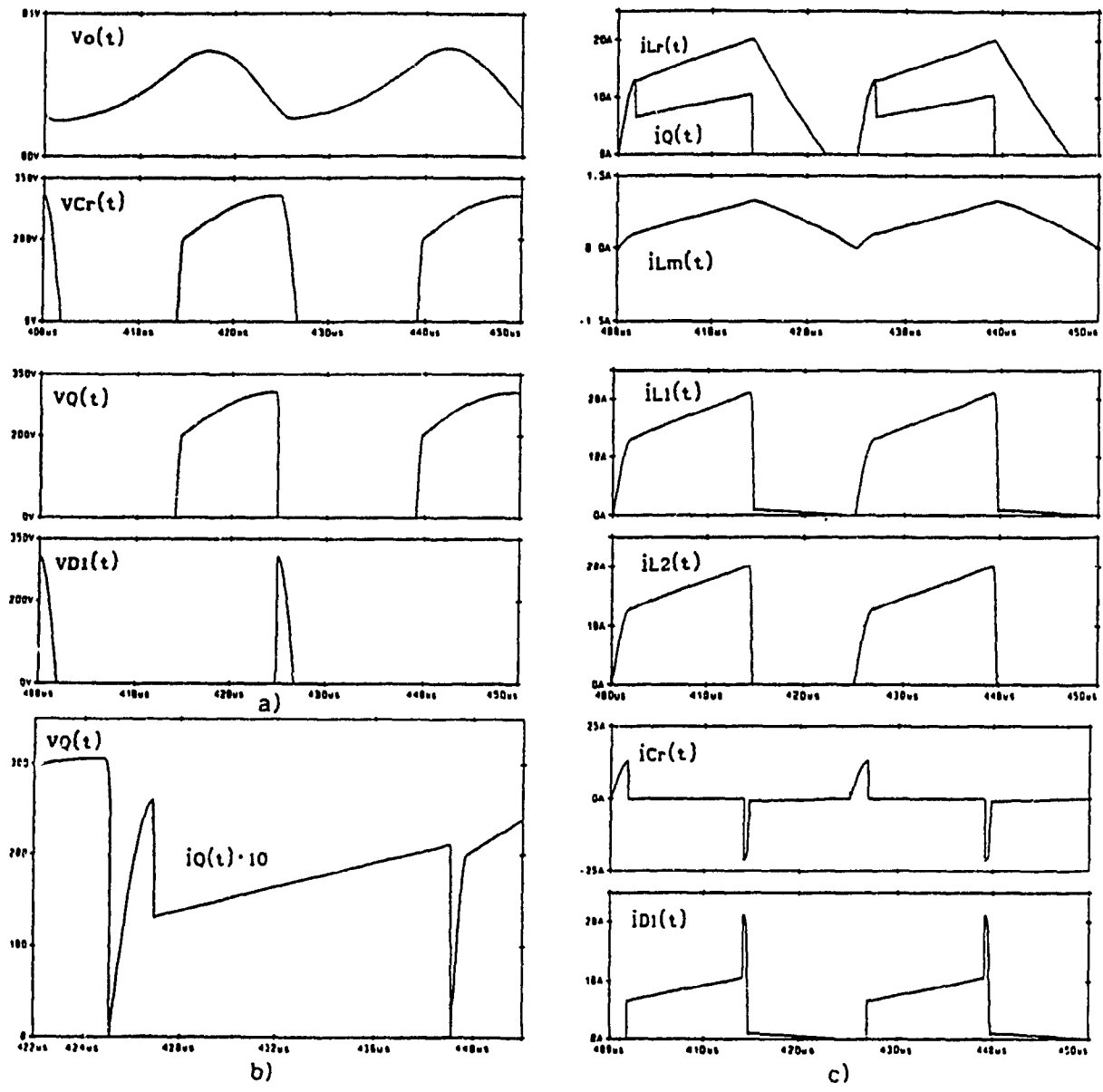
Figure 3.14 Simulation results and design verification of the two-switch forward topology with a half-bridge rectifier. a) Power circuit voltage waveforms. b) Main switch voltage/current waveforms. c) Power circuit current waveforms.

3-45
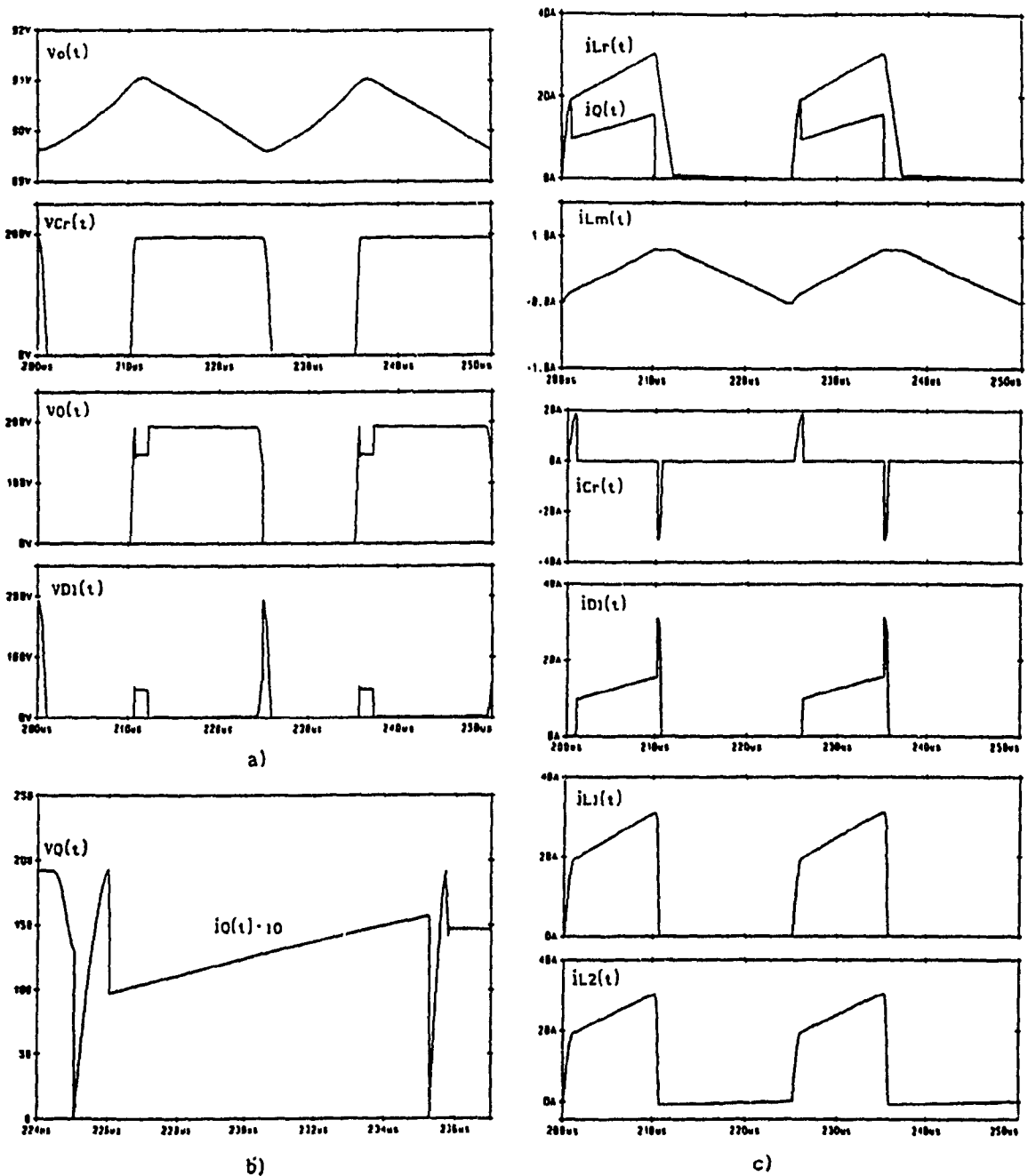
Figure 3.15 Simulation results and design verification of the two-switch forward topology with a full-bridge rectifier. a) Power circuit voltage waveforms. b) Main switch voltage/current waveforms. c) Power circuit current waveforms.

3-46
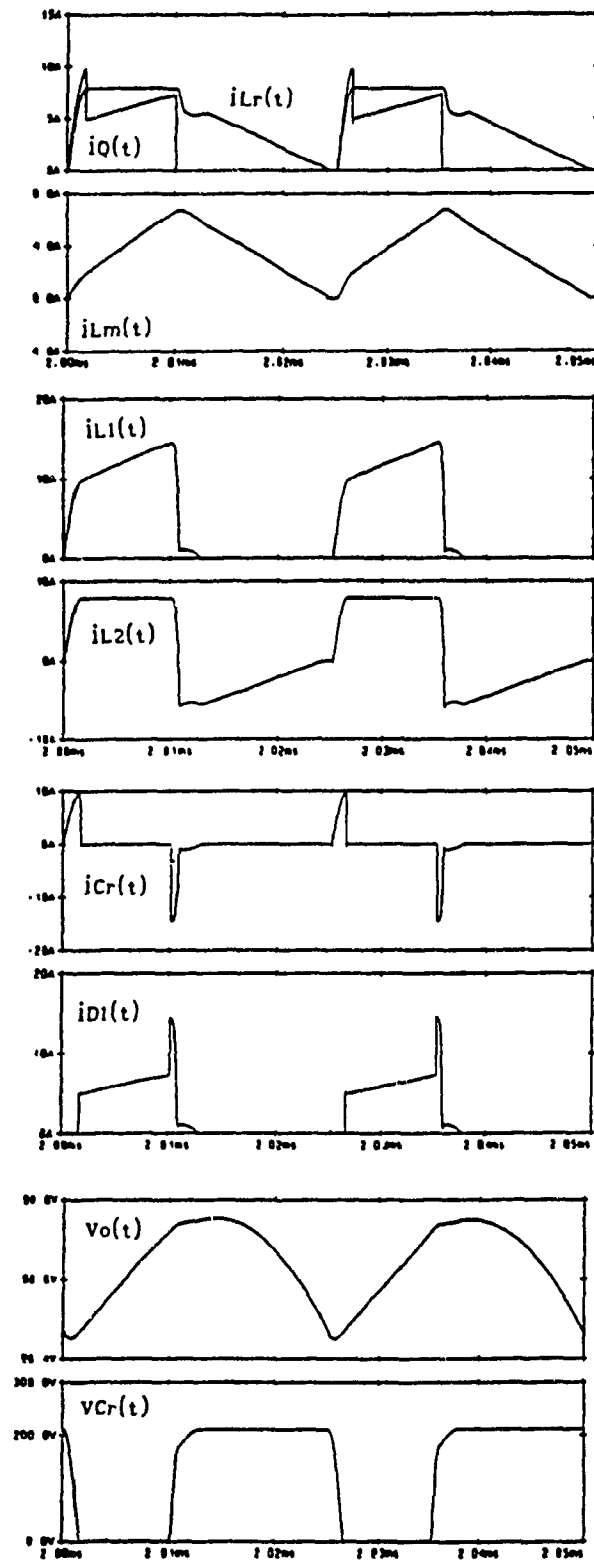
Figure 3.16 Simulated voltage/current waveforms showing the performance of the two-switch forward topology with a full-bridge rectifier and a HF transformer with reduced magnetizing inductance (Lm=180 μH).
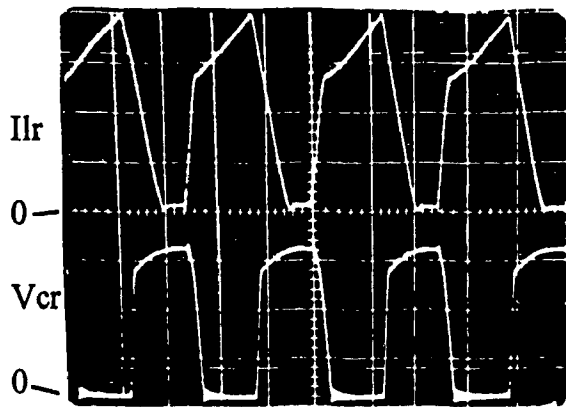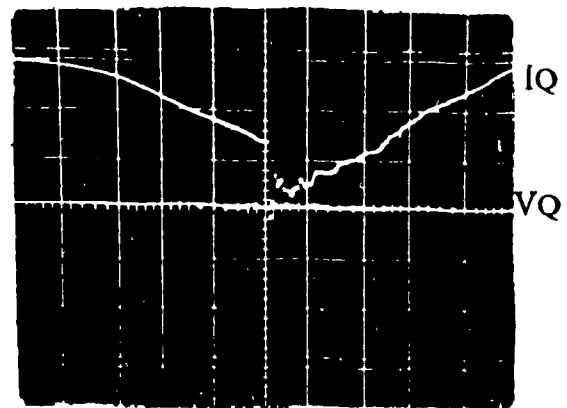
Turn-on

Current scale: 20 Amp/Div.	Current scale: 5 Amp/Div.
Voltage scale: 100 V/Div.	Voltage scale: 100 V/Div.
Time scale: 10 us/Div.	Time scale: 0.1 us/Div.
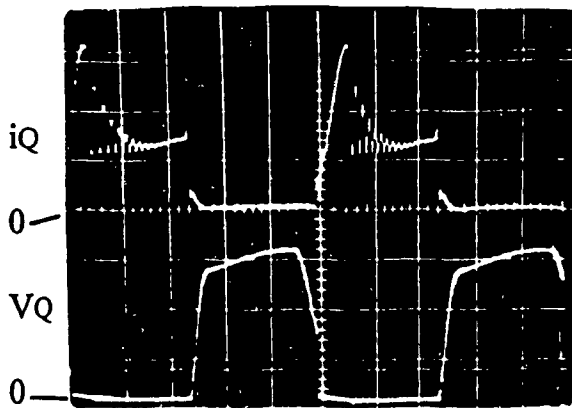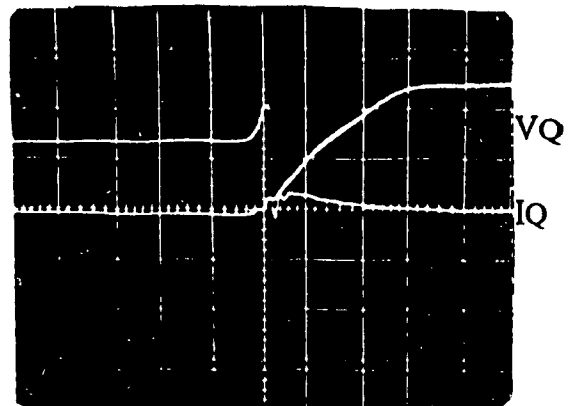
Turn-off

Current scale: 5 Amp/Div.	Current scale: 5 Amp/Div.
Voltage scale: 100 V/Div.	Voltage scale: 100 V/Div.
Time scale: 5us/Div.	Time scale: 0.1us/Div.

Figure 3.17 Experimental voltage/current waveforms of the two-switch forward topology by using a half-bridge rectifier.
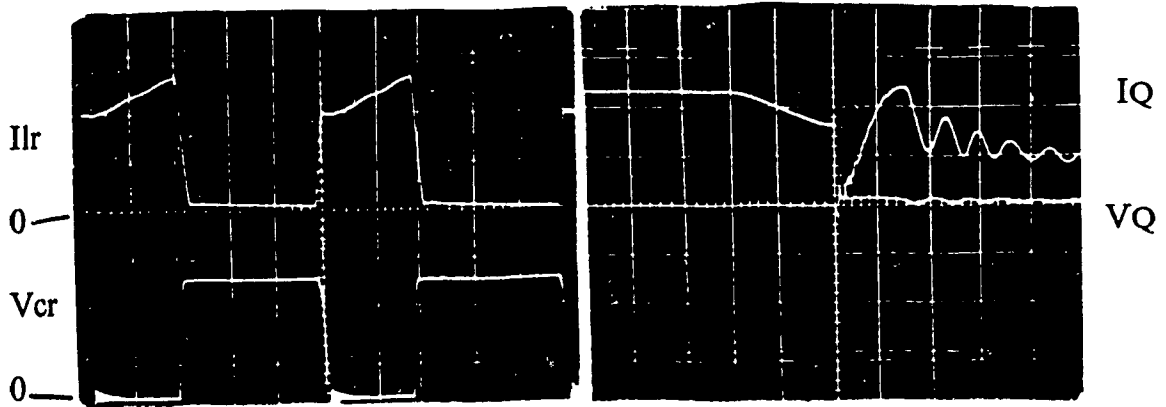
3-48

Turn-on

Current scale: 20 Amp/Div.	Current scale: 10 Amp/Div.
Voltage scale: 100 V/Div.	Voltage scale: 100 V/Div.
Time scale: 5 us/Div.	Time scale: 0.5 us/Div.
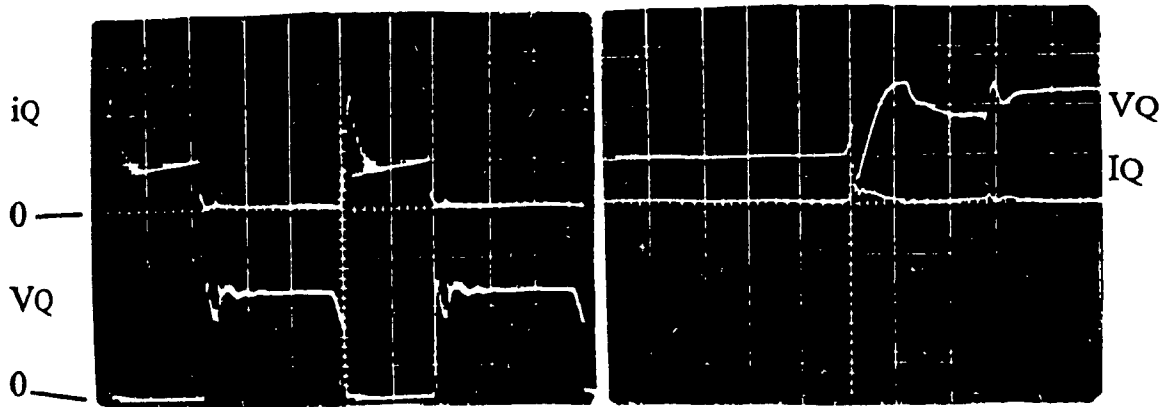
Turn-off

Current scale: 10 Amp/Div.	Current scale: 10 Amp/Div.
Voltage scale: 100 V/Div.	Voltage scale: 100 V/Div.
Time scale: 5us/Div.	Time scale: 0.5us/Div.

Figure 3.18 Experimental voltage/current waveforms of the two-switch forward topology by using a full-bridge rectifier.

operation. As a result, a reduction of the size of the transformer core becomes possible. Moreover, due to the extended duty cycle capability the utilization of the power circuit is better as compared with the widely used two switch forward converter.

In the second part of this Chapter, a novel ZVS SEFC has been proposed. The performance of this converter with a Half-Bridge Rectifier and a Full-Bridge Rectifier in the secondary of the HF transformer have been examined, and different modes of operation have been identified. This new configuration successfully solves the problem of minimizing switching losses of two switch in parallel increasing the power converter capability. The proposed topology is tailored for HF, constant output voltage and medium power applications where two switches in parallel are needed. Finally, the converter presents high efficiency, and requires only one capacitor to provide ZVS during the turn-off.

CHAPTER 4

MULTI-SWITCH FORWARD CONVERTERS

4.1 Introduction

Half-bridge and full-bridge forward topologies (Fig. 4.1) have been widely

used to design DC/DC converters for medium power applications (power higher

than 5kW). The main disadvantages of these topologies are the short circuit path

between the complementary switches and the possible saturation of the HF

isolation transformer. In high power applications the importance of the reliability

increases thus making the use of more reliable topologies mandatory. One typical

solution is to use a number of two switches single-ended forward converters

connected in parallel [2, 3] as shown in Fig. 4.2. This solution however, results in

low magnetic-core utilization of the HF transformer and output filter, an increased

number of components, and the need for a synchronized current type of control to

share the output load current.

In this Chapter, three single-ended forward converter (SEFC) topologies

using several switches and three-phase half-bridge or full-bridge rectifier are

proposed and analyzed. The proposed forward converters are derived coupling

typical single-switch forward converter on a common three-path magnetic core,

and then eliminating the redundant components. A significant reduction in the

weight, volume and amount of materials can be achieved as compared with the

solutions shown in Fig. 4.2. To compare and verify the operation of the proposed
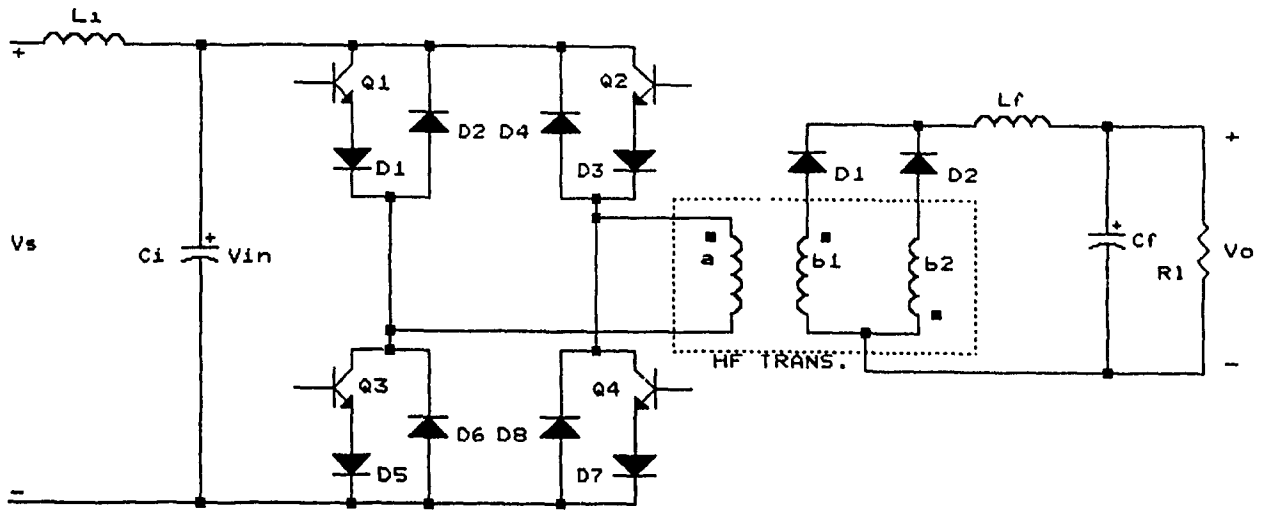
Figure 4.1   Four-Switch   Forward Converter
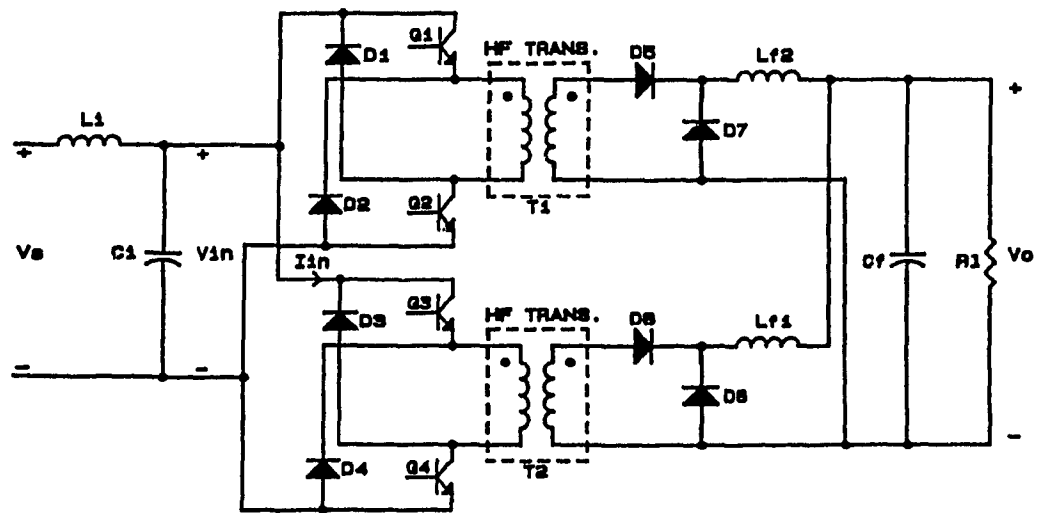
Figure 4.2   Two-switch   Forward Converter, Parallel Connection

4-2

topologies and their performance, a generalized linear mutual inductance model for the HF transformer is developed and implemented on the PSPICE software package (Appendix A3). Finally, based on the above model, key design information and simulation results are presented.

4.2   Topology I: Six-Switch SEFC with a Half-Bridge Rectifier

This topology consists of three two-switch SEFC coupled on a common three-leg magnetic core. The power circuit diagram is shown in Fig. 4.3 a).

4.2.1 Principle of Operation

A three-phase half-bridge rectifier is used at the secondary side of the HFT to obtain the DC output current. It should be noted that the free-wheeling diode is not necessary. Six ultra-fast feedback diodes, D1, D2, D3, D4, D5, and D6 are required at the primary side to reset the core during turn-off, and to provide a path for the leakage inductance energy.

4.2.2 Power Circuit Analysis

The different states of the power circuit during a switching period are illustrated in Fig. 4.3 b). The output filter and load are represented as a current source and it is assumed that the switches are ideal. The respective circuit states regarding phase a are explained below.

1) Turn-on process: During turn-on, the circuit has a single state of operation which corresponds to *State I.* Switches Q1 and Q4 are turned on, diodes D3, D6,
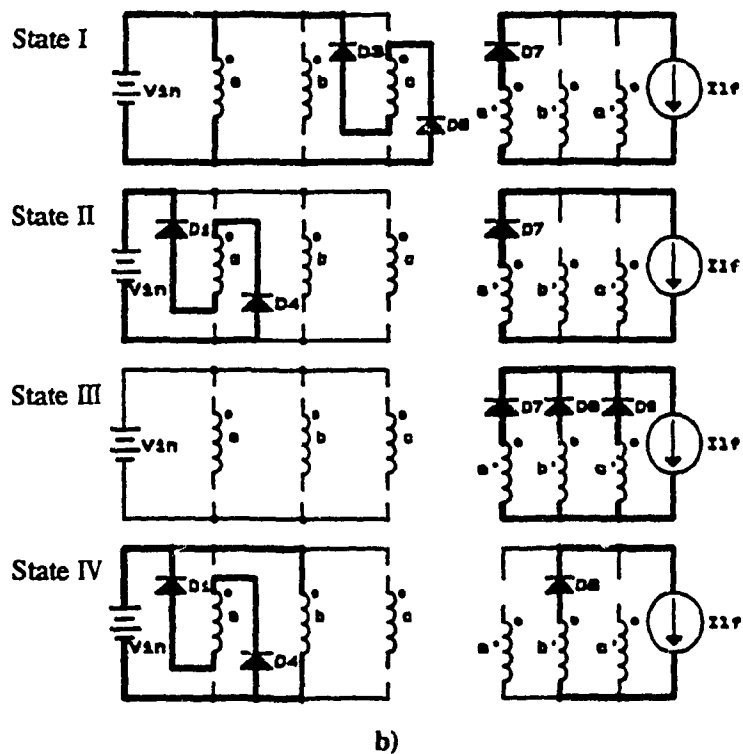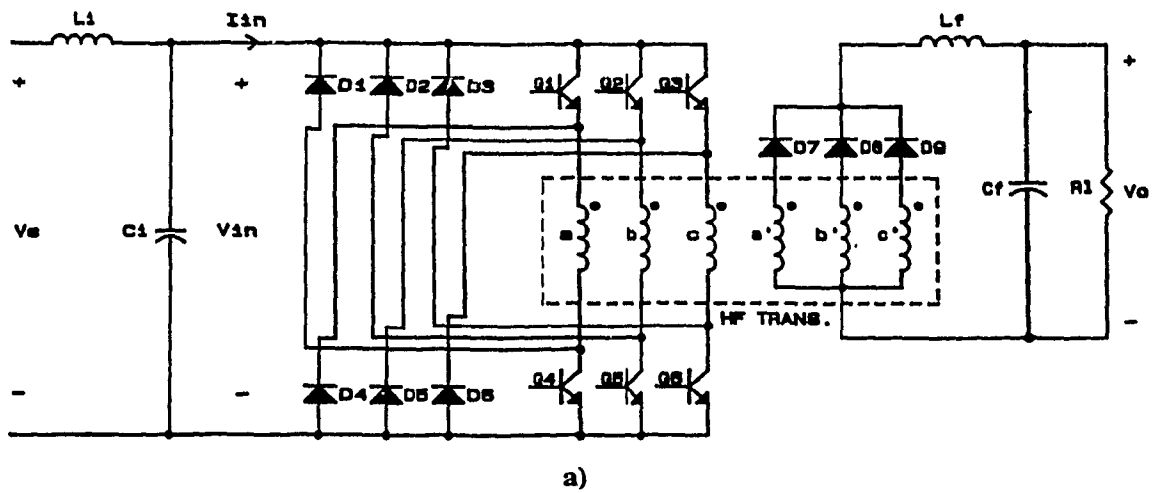
Figure 4.3 Six-switch Forward Converter with a HBR. a) Power Circuit, b) Circuit States

and D7 are on, and all other switches and diodes are off. During this state coils a and c are connected in parallel to the input voltage source, Vin. The energy is transferred to the load through phase a. Coil a stores magnetic energy from Vin, instead phase c releases energy to Vin through diodes D3 and D6, resetting the limb c of the HFT core.

2) Turn-off process: During turn-off the circuit presents the *States, II* and *III*.

State II: Diodes D1, D4, and D7 are on, all the other switches and diodes are off. Immediately after switches Q1 and Q4 are turned off, diodes D1 and D4 start conducting. Thus, coil a is reversed with respect to input source Vin. In this way, all of the energy stored in the leakage inductance's is sent back to Vin.

State III: Diodes D7, D8, and D9 are on, all the other switches and diodes are off. Once the leakage inductance energy is eliminated from the HFT, the primary side becomes disconnected from the input source. After that, the magnetic energy induces a positive voltage in coils b' and c' that forces diodes D8 and D9 to conduct. Thus, the three secondary coils, a', b', c', are now connected in parallel, trapping the magnetic energy and sharing the load current, I, during the rest of the turn-off time. The sequence of the states are similar for the phase b *(state IV)* with switches (Q2, Q5), and the phase c with switches (Q3, Q6).

4.3 Topology II: Six-Switche SEFC with a Full-Bridge Rectifier.

The previous topology has the following drawbacks :

1) Each time when two switches are turned on, two primary coils are connected in parallel and opposing one with the other, thus reducing the utilization of the primary coils;

2) The magnetizing current presents a DC component, thus reducing the utilization of the core;

3) Each secondary coil operates with a DC current proportional to the load current I, thus reducing the utilization of the secondary coils.

Those drawbacks are eliminated by using a Full-Bridge Rectifier in the secondary side of the HF transformer. The power circuit diagram is shown in Fig. 4.4 a).

4.3.1 Principle of Operation

The volt-second balance is achieved now at the secondary side of the HFT. The rectifier circuit and the output filter operate as a current source inverter which transforms the DC load current I, into an AC current source in each secondary coil. This transformation is the dual of the typical voltage source six-switch full-bridge inverter. Therefore, the utilization of the HFT of this converter becomes comparable to the typical six-switch full-bridge three-phase forward converter, with the additional advantage of better reliability since there is no short-circuit path through the switches.
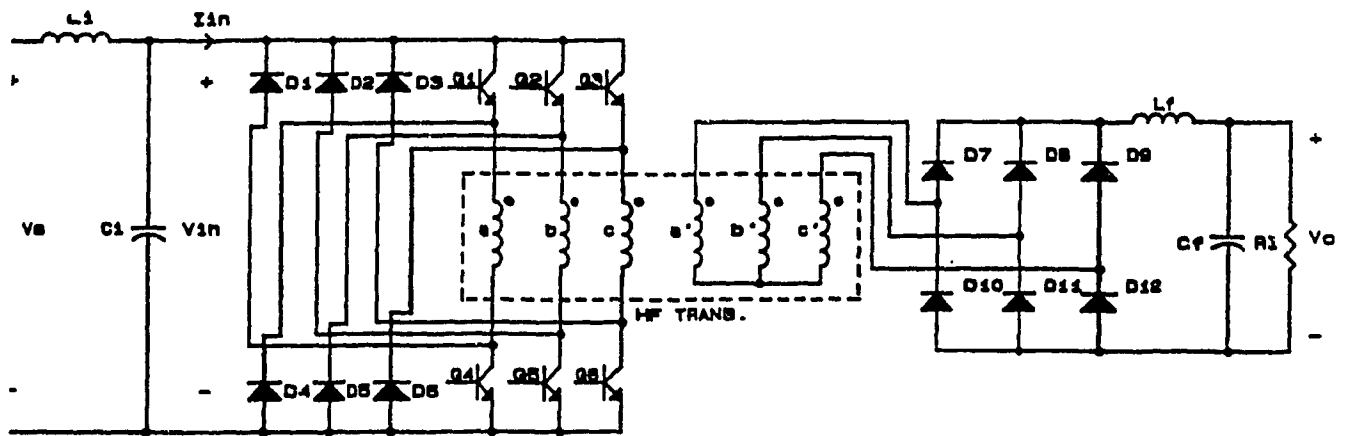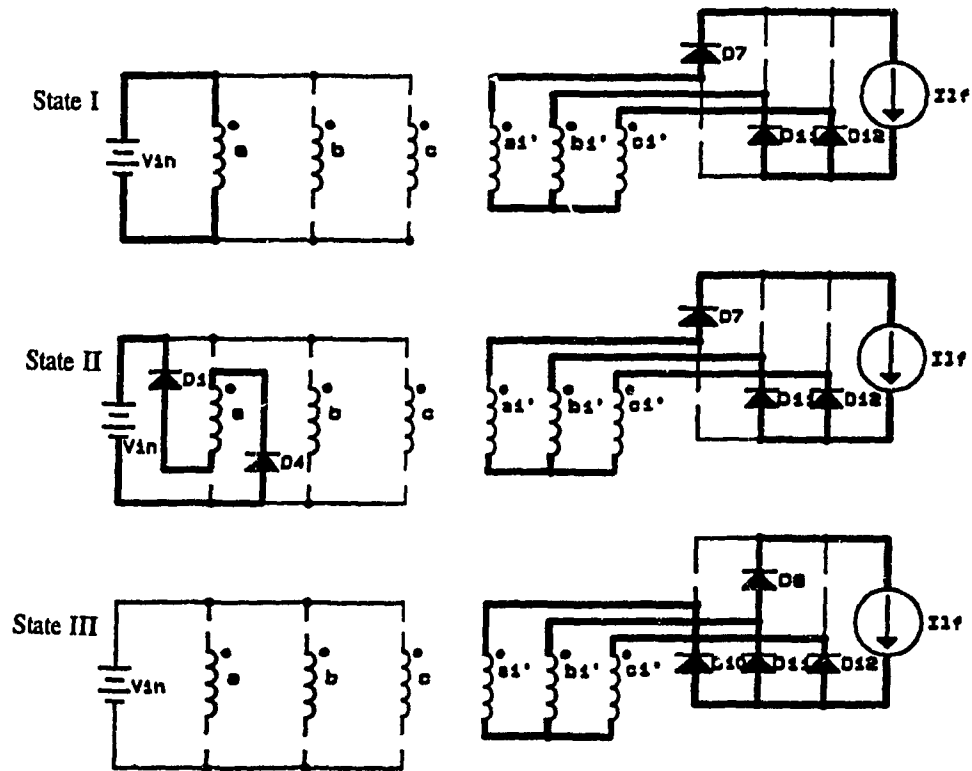
Figure 4.4 Six-switch Forward Converter with a FBR. a) Power Circuit, b) Circuit States

4.3.2 Power Circuit Analysis

The respective circuit states for phase a are depicted in Fig. 4.4 b). The sequence is the same for phase b and c.

1) Turn-on process: During turn-on, the circuit operates only in *State 1*. Switches Q1 and Q4 are on, the diodes D7, D11, and D12 are on, all the other switches and diodes are off. When switches Q1 and Q4 are on, secondary coils b' and c' become connected in parallel sharing the load current (I/2). This current flows in the negative direction through each of these coils. At the same time coil a', which is connected in series, conducts the total load current, I, but in a positive direction. Notice that in this case, the magnetizing energy corresponding to phase c does not circulate through the feedback diodes D3 and D6 as in the previous topology. The magnetizing current is divided among all the phases. The magnetizing current provided by phase a circulates on the primary side, and the magnetizing current corresponding to phase b and c circulates on the secondary side through diodes D11 and D12.

2) Turn-off process: Corresponds to the *States II and III* shown in Figs. 4.4 (b).

State II: Diodes D1, D4, D7, D11, D12 are on, all the other switches and diodes are off. Similarly, immediately after switch Q1 and Q4 are turned off, diodes D1 and D4 start conducting. Thus, the primary coil a is now reverse connected to the

input source Vin. In this way, all the energy stored in the leakage inductance's is sent back to Vin.

State III: The diodes D8, D10, D11, and D12 are on, all the other switches and diodes are off. Once the leakage inductance energy is eliminated form the transformer the magnetic energy induces a negative voltage in coil a', and positive voltage in coils b' and c'. The diodes D8, D10, D11, and D12 are conducting and the three secondary coils become connected in parallel trapping the magnetic energy during the rest of the turn-off time. The load current circulates through diodes D8 and D11.

4.4 Topology III: Three-Switch SEFC with a Full-Bridge Rectifier.

The power circuit diagram is shown in Fig. 4.5 a). This circuit reduce the number of power switches in series and it does not need the feedback diodes, although a more complex transformer is required. The proposed topology can be used for low voltage applications.

4.4.1 Principles of Operation

The circuit consists of three single-switch forward converters coupled on a common three-phase core. A zig-zag connection is implemented by using the six coils on the primary side. The zig-zag connection provides a means of magnetically resetting the respective limbs of the transformer core each time a switch is turned on. A full-bridge rectifier is implemented on the secondary side to
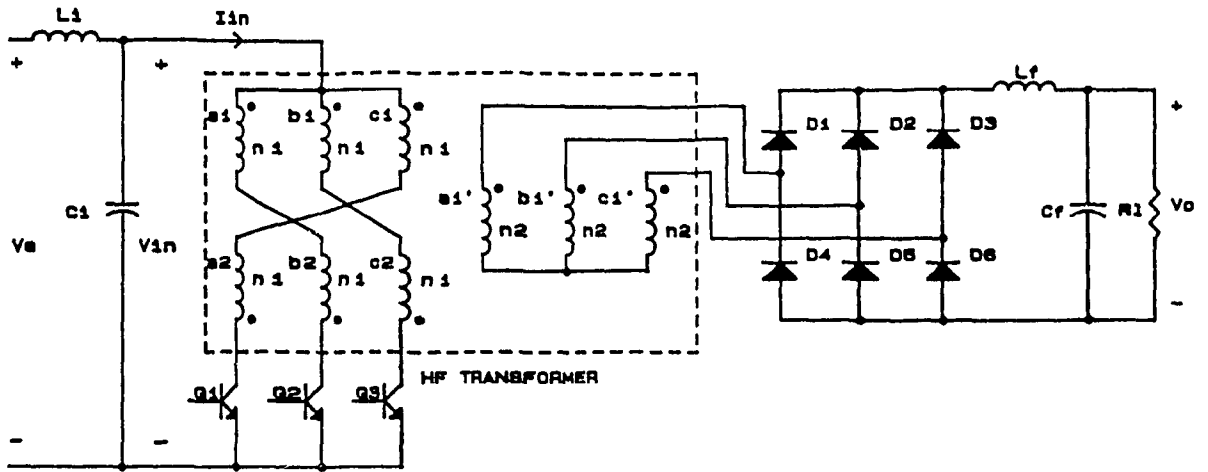
a)
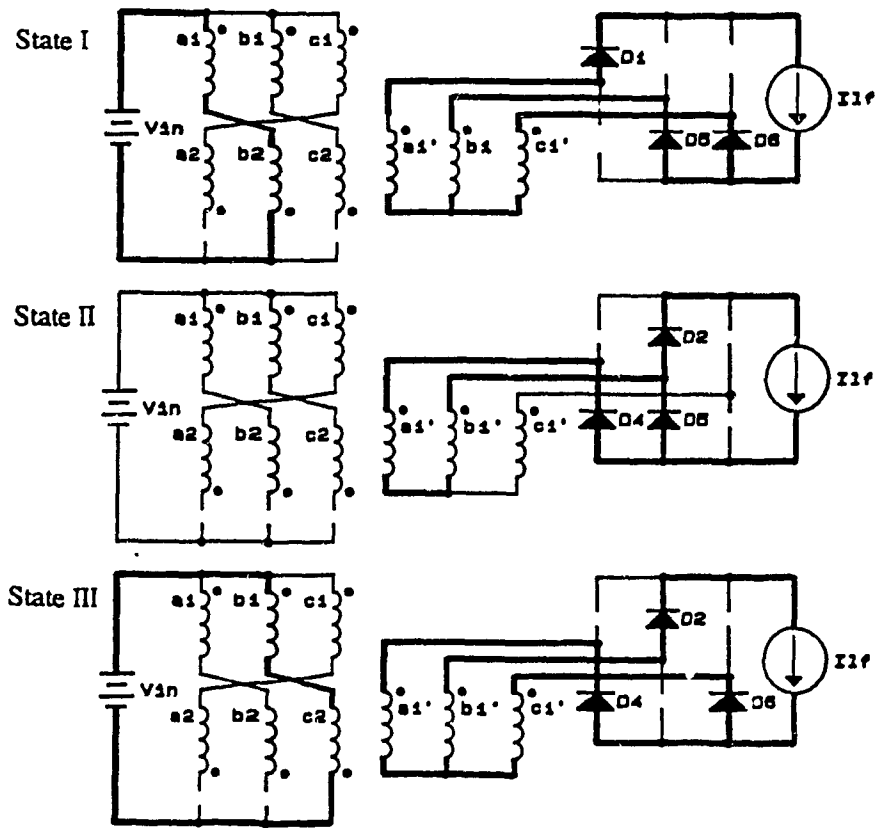
b)

Figure 4.5 Three-switch Forward Converter with a FBR. a) Power Circuit, b) Circuit States

obtain the DC output current. The rectifier also provides a path during the turn-off cycle for both, the HFT magnetizing and the output filter load current. However, snubber circuits are required (not shown) to handle the leakage inductance energy of the HFT.

4.4.2 Power Circuit Analysis

The respective states of the power circuit during a switching cycle are illustrated in Fig. 4.5 b). The description of these states with regard to the operation of switch Q2 is presented below.

1) Turn-on process: Correspond to the *State I*, when Switch Q2 is on, D1, D5, and D6 are on, all the other switches and diodes are off. At the primary side, the load and magnetizing current circulate through coils a1, b1 and switch Q2. Thus the magnetic flux increases in limbs a and b. At the secondary side, the load current flows through coils a1', b1', and diodes D1 and D5. The coils b1', and c1' to b1' through diodes D5 and D6, thus decreasing the flux in limb c.

*2) Turn-off process:* Corresponds to *States II* and *III* shown in Fig. 4.5 b). Diodes D2, D4, and D5 are on, all the other switches and diodes are off. Once the leakage energy is eliminated from the transformer, the coils a1' and b1' becomes connected in parallel trough diodes D4 and D5, trapping the magnetic energy during turn-off. The current IIf circulates through diodes D2 and D5. The states of the circuit are similar when the switches Q1 and Q3 are turned on.

4.5   Design Example and Comparison

This section presents the design equations and a numerical evaluation of the proposed topologies. Design examples are provided to illustrate the relative performance of each topology for a particular application. Finally, in order to verify the theory, simulation results are presented by using the PSPICE program. The typical four-switch full-bridge converter and the two-switch converter are included for comparison proposes. The topologies are identified as follows:

<div align="center">

TOP.A   Fig. 4.1

TOP.B   Fig. 4.2

TOP.C   Fig. 4.3.

TOP.D   Fig. 4.4.

TOP.E   Fig. 4.5.

</div>

A.   Design equations

In a practical DC/DC converter, the losses are low and the switching frequency is high as compared with the break frequency of the input and output filters. Thus, the voltage and current in each branch can be assumed to be a combination of square and triangular waveforms. With this assumption simple design equations can been derived. Those equations are presented below.

a) Effective Transformer Turns-ratio: The effective transformer turns ratio, Ne, is calculated for 90% overall converter efficiency (η), the maximum converter

duty cycle (Do) for the respective topology, the minimum dc input voltage value Vin, and the total transistor (Vce) and diode (Vdf) voltage drop. The final expression yields :

$$Ne = \frac{0.9 \cdot Do \cdot (Vin - Vce)}{Vo + Vdf} \qquad (4.1)$$

b) Peak Magnetizing Current: The peak magnetizing current is taken as 10% of the maximum output current at the maximum switch duty cycle (Ds). Referring to the primary side the final expression yields .

$$Ipm = \frac{0.1 \cdot Po}{h \cdot \hat{V}_{in} \cdot Ds \cdot p} \qquad (4.2)$$

where Po is the maximum output power and $\hat{V}_{in}$ is the maximum DC input filter voltage.

c) Primary and Secondary Self Inductances : The self inductance in the primary side (Lp) is calculated considering the maximum magnetizing current value Ipm as follows

$$Lp = \frac{(Vin - Vce) \cdot Ds}{Ipm \cdot fs} \qquad (4.3)$$

The secondary self inductance (Ls) is calculated to accommodate the turns ratio Ne give by (4.1). Hence from the Appendix A3

$$Ls = \frac{Kc^2}{Ne^2} Lp \qquad (4.4)$$

d) Branch RMS Values : The RMS values of the voltages and currents in the mains branches of the converter are evaluated by using the following expressions:

For a square waveforms :
$$IRMS = Imax \cdot (Ds)^{0.5} \qquad (4.5)$$

$$VRMS = Vmax \cdot (Ds)^{0.5} \qquad (4.6)$$

For a triangular waveforms :
$$IRMS = Imax \cdot \left[\frac{Ds}{3} \right]^{0.5} \qquad (4.7)$$

e) Transformer Volt-Amp ratings : The transformer volt-amp rating is calculated using the following general expression :

$$Total\ VA = \sum_{i=1}^{n} VRMS_i \cdot IRMS_i \qquad (4.8)$$

For comparison purposes, a core magnetizing VA ((V-A)m) is evaluated by using the following expressions:

$$(V\text{-}A)m_A = 1.154 \cdot Dsmax \cdot Ipm \cdot Vin \qquad (4.9)$$

$$(V\text{-}A)m_B = 2.308 \cdot Dsmax \cdot Ipm \cdot Vin \qquad (4.10)$$

$$(V\text{-}A)m_C = 3.464 \cdot Dsmax \cdot Ipm \cdot Vin \qquad (4.11)$$

$$(V\text{-}A)m_D = 1.154 \cdot Dsmax \cdot Ipm \cdot Vin \qquad (4.12)$$

$$(V\text{-}A)m_E = 3 \cdot (Dsmax \cdot (4 \cdot Dsmax - 1))^{0.5} \cdot Ipm \cdot Vin \qquad (4.13)$$

Therefore the total VA for the coils is evaluated as follows:

$$(V\text{-}A)w = (V\text{-}A)m + (V\text{-}A)I + (V\text{-}A)F \qquad (4.14)$$

where (V-A)I is the VA regarding a ideal converter (no ripple in the output filter), and (V-A)F is the VA due to the output filter current ripple. The resulting expressions for each topology are :

$$V-A)w_A = (V-A)m_A + \left(\frac{1}{\eta}+1\right) \cdot Po + (V-A)F_A \qquad (4.15)$$

$$V-A)w_B = (V-A)m_B + 1.414 \cdot \left(\frac{1}{\eta}+1\right) \cdot Po + (V-A)F_B \qquad (4.16)$$

$$V-A)w_C = (V-A)m_C + 1.414 \cdot \left(\frac{1}{\eta}+1\right) \cdot Po + (V-A)F_C \qquad (4.17)$$

$$V-A)w_D = (V-A)m_D + \left(\frac{1}{\eta}+1\right) \cdot Po + (V-A)F_D \qquad (4.18)$$

$$V-A)w_E = (V-A)m_E + 1.732 \cdot \left(\frac{1}{\eta}+0.707\right) \cdot Po + (V-A)F_E \qquad (4.19)$$

where the (V-A)F depends on the output filter specifications

B. Design Example

To comparatively evaluate the different converters configurations using the above equations, a design example is presented hereafter regarding the following design specifications:

Output power	Po	= 10 kW
Output Voltage	Vo	= 200 V
Input Voltage	Vin	= 800 V
Switching frequency	fs	= 40 kHz

The output filter is designed to meet a 2% maximum inductance ripple current and a 2 kHz break frequency requirements.

C. Comparison

Table 4-I summarizes the final values calculated for the different parameters obtained. The Four-Switch Full-Bridge topology requires two external fast diodes for each switch in order to allow high frequency operation, increasing the conduction and switching losses. The power circuit does not provide inherent protection for short circuits through the top and bottom switches. A fast current mode type of control is necessary to avoid both, switch short circuits and transformer saturation. The single-ended forward topology minimizes the short circuit problem because the HFT leakage inductances limit the rise time of the short circuit current through the switches.

Table 4-I

Design Example: P=10 kW, f_s=40 kHZ, V_{in}=800 V, V_o= 200 V

Topology		Transformer			Switch		Filter	Components
D_s	N_e	L_p - L_s [uH]	(V-A)m-(V-A)w	Iq_{max} - Iq_{rms}	Vq_{max}	L_f -C_f [uH] - [uF]	D: Diode S: Switch T: Transf F: Filter
A 0.46	3.28	6079 - 565	641 - 25993	17.13 - 10.78	Vin	200 - 32	10D+4S+1T+1F
B 0.46	1.64	6079 - 250	1282 - 31338	17.13 - 10.78	Vin	400 - 64*	8D+4S+2T+2F
C 0.29	3.11	7665 - 792	1213 - 31135	17.13 - 9.28	Vin	133 - 22	9D+6S+1T+1F
D 0.29	3.11	3832 - 396	780 - 16169	17.13 - 9.28	1.5Vin	133 - 22	12D+6S+1T+1F
E 0.29	3.11	3832 - 396	780 - 32339	17.13 - 9.28	3Vin	133 - 22	6D+3S+1T+1F

* Requires two inductances and two capacitors in the output filter

The parallel Two-Switch Single-Ended topology (TOP.A) presents a low HFT turns-ratio, i.e. increased value of the secondary inductance. The (V-A)m is two times higher and the (V-A)w required is 20% higher as compared with the Four-Switch full bridge scheme. Two HFT's, two output filter reactors, and two capacitors are also required. The total HFT area product (A_p) of the magnetic core and the size of the output filter is 200% larger as compared with the full bridge. Moreover, it requires a synchronized current mode control in order to share the output load current.

The three-leg core provides a 25% reduction of the Ap as compared with the parallel Two-Switch Single-Ended topology and the size of the output filter is reduced 31% as compared with the Four-Switch full-bridge topology (TOP.B). Also, the I_{RMS} current of the switch is reduced 14%.

The Six-Switch Single-Ended topology with a half-bridge rectifier (TOP.C) requires a VA rating 6% less magnetizing as compared to the parallel Two-Switch forward topology. Moreover, the secondary inductance Ls and the leakage inductance are reduced 64%. However, because two primary windings are connected in parallel each time the two-switch are on, this topology requires a higher primary inductance to get the same maximum flux. This drawback is eliminated with the Six-Switch Single-Ended full-bridge topology (TOP.D). This

new type of forward converter needs a transformer VA rating almost similar to the conventional three-phase full-bridge forward converter with six switches.

The Three-Switch Single-Ended topology (TOP.E) requires low primary and secondary inductances. Also, the (V-A)m value is only 22% higher as compared with a full bridge. However, the voltage stress of each switch is high and the utilization of the winding of the transformer is low.

D.   Simulation Results

The transformer models described in the Appendix III have been implemented on the circuit analysis program PSPICE. As a reference, the full-bridge and the parallel two-switch forward schemes shown in Figs. 4.1 and 4.2 are included in the analysis. The parameter values presented in **Table 4-I** have been used in the simulation.

The Fig. 4.6 shows the simulation results for the fourth-switch full-bridge forward converter (TOP.A). One can see an oscillation of the input current due to the offset of the DC component of the magnetizing and load circulating current in the secondary windings during turn-off. A capacitor connected in series with the primary of the HFT, or current control with the current sensor in the input terminal is necessary to eliminate this difficulty, and to avoid transformer saturation. The negative peak of this current corresponds to the leakage inductance energy which circulates through diodes D2, and D8 or D4, and D6 (Fig. 4.1).

4-18

Fig. 4.7 shows the operation of the typical two-switch forward converter (TOP.B, one unit). The magnetizing and leakage energy circulates through the feedback diodes D3, and D4 immediately after the two switches, Q2 and Q3 are turned off.

Fig. 4.8 illustrates the operation of the six-switch forward topology with a half-bridge rectifier (TOP.C). The leakage energy flows through the feedback diodes (for example D1 and D4, Fig. 4.3) immediately after the respective switches are turned-off (Q1 and Q4, phase a, Fig. 4.3). It should be noted that in this case, the transformer magnetizing energy becomes trapped in the secondary through the rectifier diodes during turn-off (Figs. 4.8 f), g) and h)). However, the magnetizing energy corresponding to phase a is returned to the input filter through diodes D1 and D4 when both switches, Q2 and Q5 are turned on (Figs. 4.8 b), c), and d). As a result, two HFT primary coils become connected in parallel during the turn-on time thus increasing the slope of the input current (Fig. 4.8 a)).

Since in both TOP.B and TOP.C, the magnetizing current is zero at the end of the turn-on, these two circuits do not present instability in the input current. Therefore, they do not need current control to avoid saturation. However, in both cases the magnetizing current has a DC component.
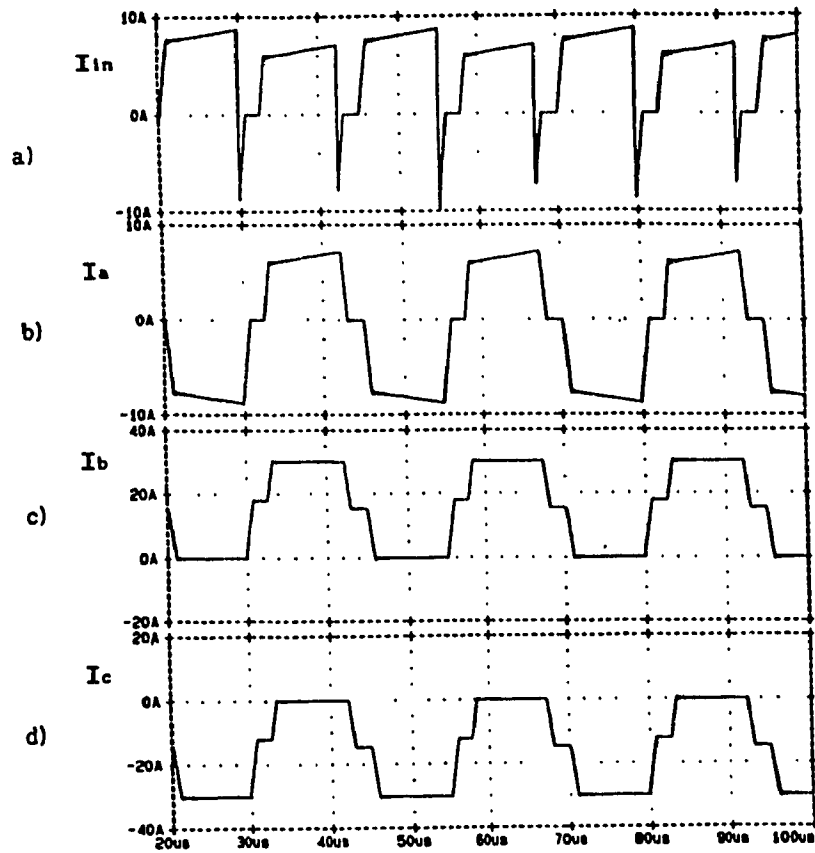
Figure 4.6   Four-switch Forward Converter, Simulation Results
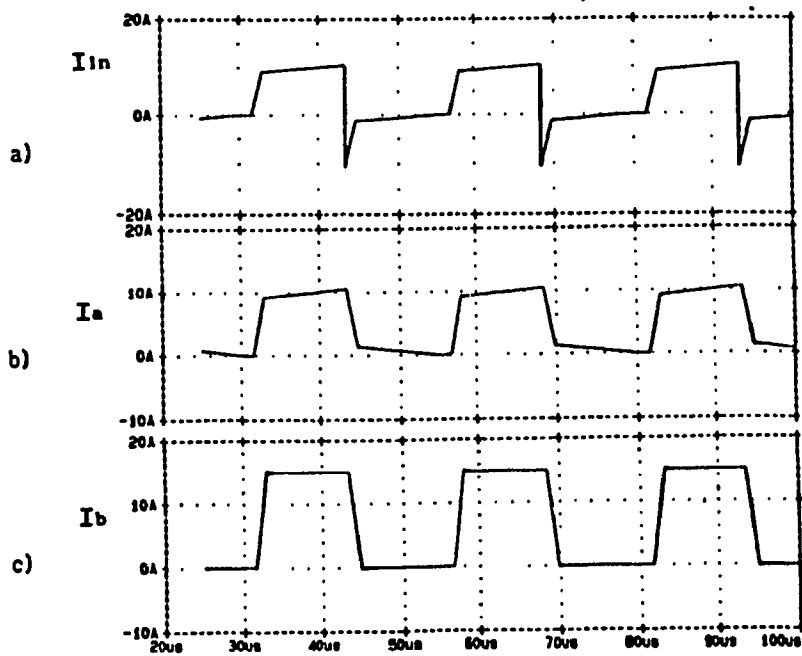
Figure 4.7   Two-switch Forward Converter, Simulation Results
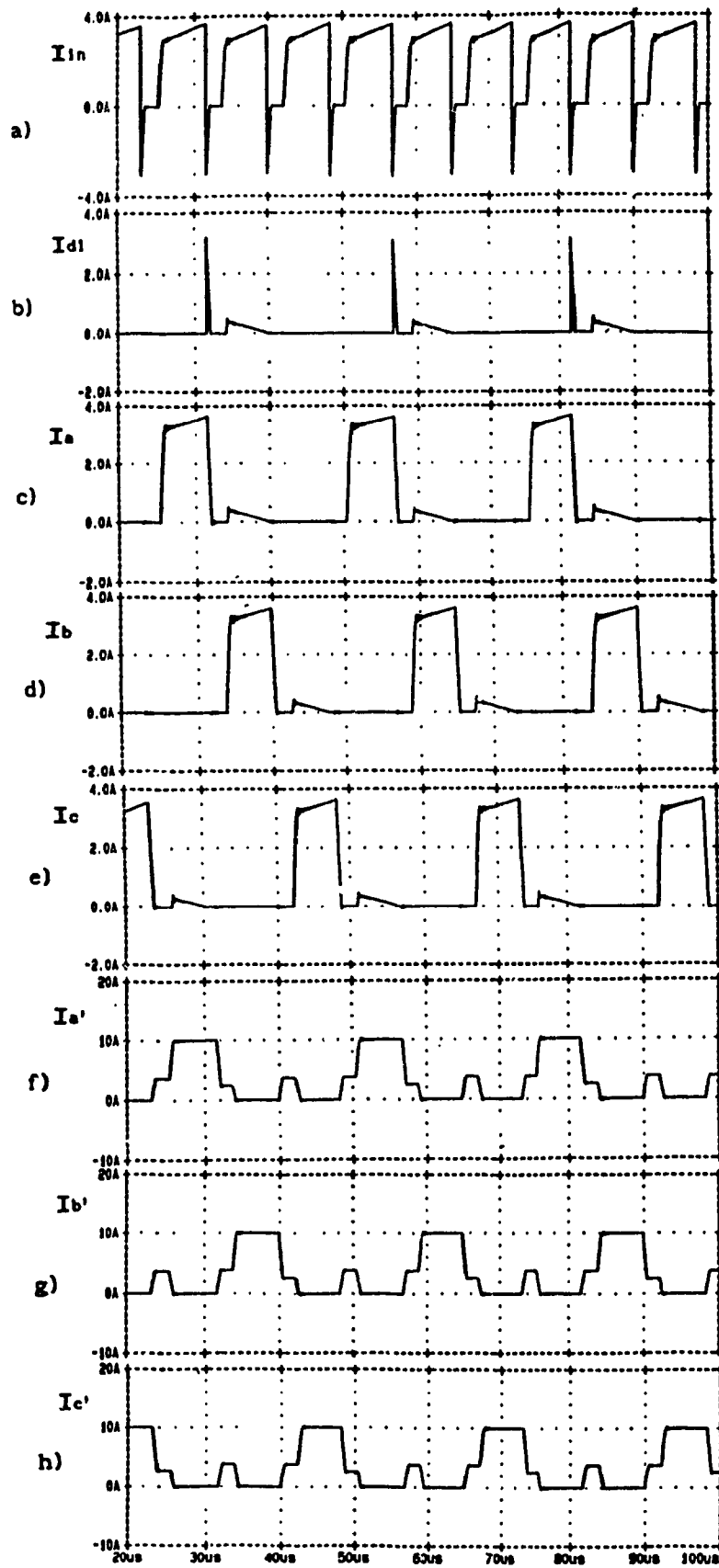
Figure 4.8 Six-switch Forward Converter with a HBR, Simulation Results

Fig. 4.9 shows the operation of the six-switch topology with a full-bridge rectifier (TOP.D) and verifies that the magnetizing current does not circulate through the feedback diodes. Also, as shown in Figs. 4.9 f), g), and h), the load current becomes an AC type of current through the three secondary windings during turn-on thereby improving the utilization of the transformer. However, when a full-bridge rectifier is used on the secondary side, the peak input current could change in each period due to the offset of the DC component of the magnetizing current of the respective phase.

Fig. 4.10 illustrates the operation of a three-switch forward converter with a full-bridge rectifier (TOP.E). Similarly in this scheme, as shown in Fig. 4.10 a), the input current does not present instability. Figs. 4.10 e), f), and g) show that the magnetizing current in each phase is zero at the end of the of turn-on cycle because the zig-zag connection resets the respective limbs of the core each time one switch is turned on.

4.6   Summary

A three-leg core has been proposed in this chapter to implement multi-switch single-ended forward DC/DC converters with increased reliability in medium power applications. A generalized linear matrix inductance model has been developed and used for simulation. The model has been implemented on the PSPICE software package.
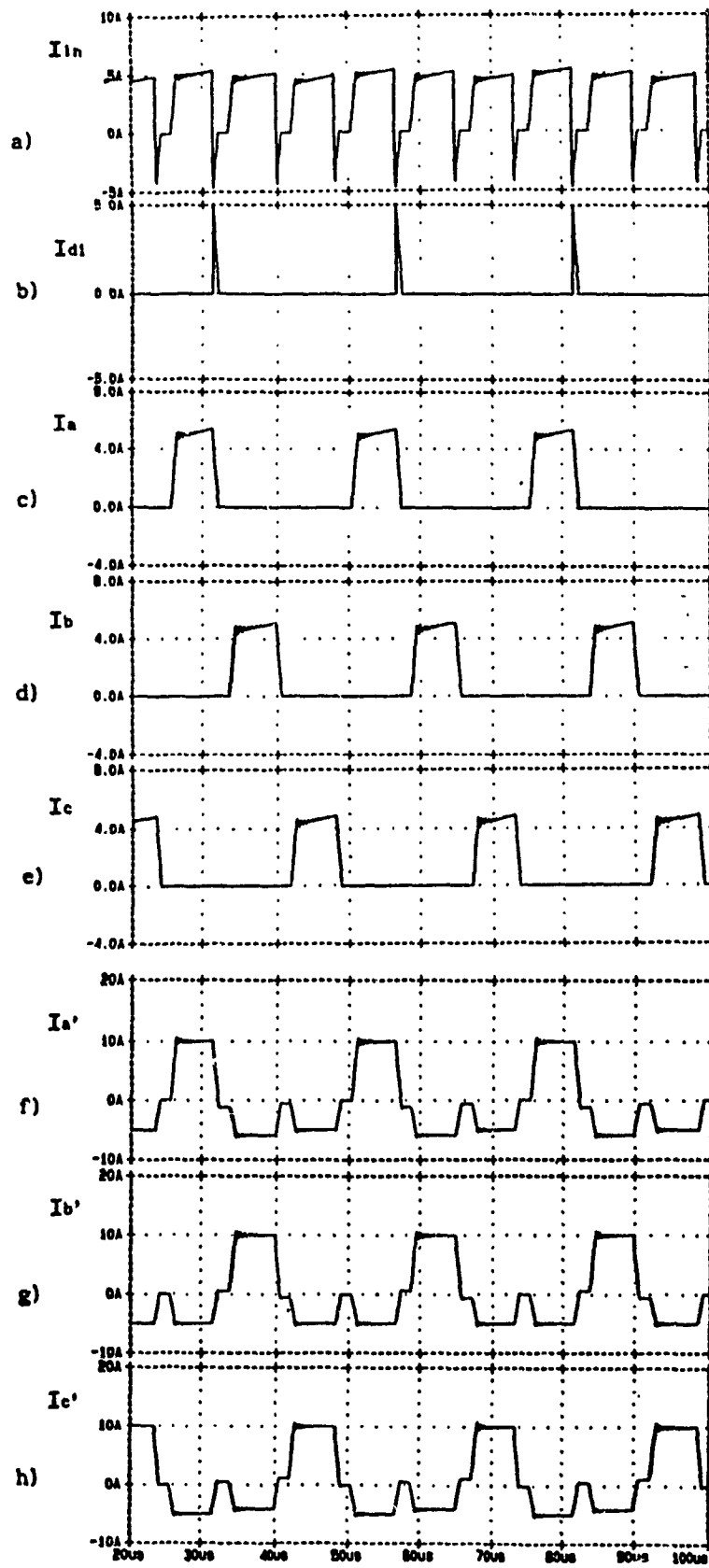
Figure 4.9   Six-switch   Forward Converter with a FBR, Simulation Results

4-23
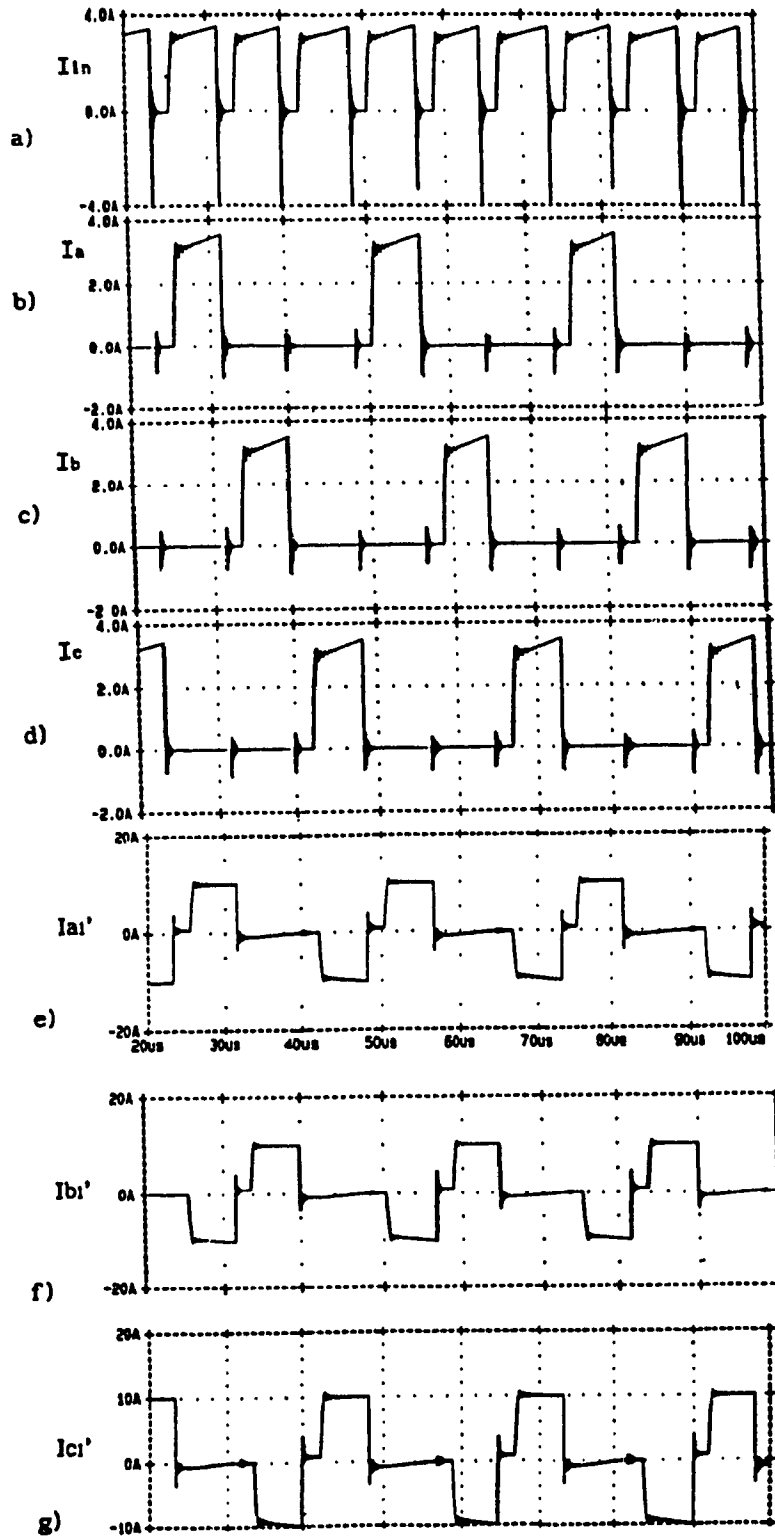
Figure 4.10 Three-switch Forward Converter with a FBR, Simulation Results

Three forward DC/DC topologies have been analyzed; two with six switches and one with three switches. Since to all of them are single-ended type of converters, the magnetic flux balancing of the HFT core must be accomplished in the final circuit configuration in order to avoid saturation. Each switch must be operated 120° phase shifted, and the maximum ideal duty cycle for each switch cannot be larger than 33%. As compared with the typical parallel two-switch forward configuration the reduction in magnetic material can be 25% for the transformer, and the output filter size is reduced three times. However, the current switch utilization is lower due to the limitation in the maximum duty cycle.

The utilization of the HFT core and windings in the proposed six-switch forward topology is improved when a full-bridge rectifier is used on the secondary side. This new converter is practically the dual of the typical three-phase full-bridge voltage inverter.

CHAPTER 5

CONTROL OF FORWARD CONVERTERS

5.1   Introduction

The output voltage of a forward converter can be regulated by using current mode control or voltage mode control.

Current mode control consists of a HF minor current feedback loop, which is inside the major voltage feedback loop via the error amplifier. This current loop applies directly to the PWM comparator an instantaneous output filter current sample. This is a fast feedback current loop transforming the output filter inductance in a current source, reducing the order of the converter and providing short circuit protection. However, the duty cycle is modified in terms of the peak value of the output filter current and not in terms of its DC value, which means that a DC error is always present in the control loop. In addition, above 50% duty cycle the performance of the circuit shows an unstable low frequency mode of operation. A ramp compensation technique is necessary to minimise the DC error and to ensure stability [6-8,19,20]. Also, to reduce the output impedance of the converter, feed-forward of the load current is required. The feedback and the feed-forward current signals directly define the duty cycle of the control pulse, so that the performance and the reliability of the converter depends mainly on the stability and quality of those two current signals.

Current mode control in constant frequency and peak value sensing, is widely used in small-size low-power switching converters [7-8]. This is because the power and the control unit can be designed on a common circuit board with very short distances between components. Therefore, it is not difficult to obtain a good-quality current signal to ensure stability. In addition, it is not necessary to scale down the DC level of the output current. Instead, in high-power HF DC/DC converters, the level of the output current is high and must be scaled down decreasing its slope. Moreover, the current sensors are far from the control circuit, and the problems of saturation, DC off-set due to temperature variation, common signal noise, and parasitic components in the HF current loops could produce random intersections in the comparator and an extra phase shift. All of those drawbacks decrease the reliability for hi-power applications.

In voltage mode control, a triangular constant frequency waveform is used to define the switching frequency and to provide PWM. The duty cycle is defined by the comparison of this waveform with the error signal after the controllers. Two controllers in cascade (current and voltage) are usually designed. The output voltage feedback signal can be obtained by using a simple differential amplifier and resistors. These features provide better noise immunity. Moreover, this control method provides a higher DC converter gain and a lower output impedance than a

current control method. However, due to the second order output filter it is difficult to achieve a good bandwidth for the converter.

In this Chapter, two PWM control systems for HF forward converters are investigated. The first one is an improved voltage mode control system proposed for the forward converter with extended duty cycle capability analysed in chapter three. The second one is a new current-assisted voltage mode control which has some features of current mode control and can be used in any forward converter.

5.2 System I: Improved PWM Voltage Mode Control

This section presents the design and evaluation of a single-loop and a dual-loop feedback voltage mode control system for the two-switch forward converter shown in the Fig. 5.1. To improve the regulation at HF, the bandwidth of this converter is increased by reducing the output filter inductance. This reduces the output impedance but increases the ripple of the output current and reduces the damping ratio. Therefore, a fast output voltage control is required. The proposed controllers are designed to improve the output voltage regulation of this converter above the resonance frequency of the output filter. The design requires an improved converter model to predict the delay at HF in the voltage loop. To do this, an all-pass constant-time delay filter in cascade with the linear transfer function of the converter is proposed.

5.2.1 Power Circuit

A 2-kW experimental breadboard circuit (Fig. 5.1) was designed to provide DC output power at 40 kHz switching frequency. The DC input voltage is 300 V and the maximum output voltage is 50 V. The converter uses pulse-width modulation (PWM) to control the output voltage. Quasi-resonant snubbers are incorporated to provided extended duty cycle capability and to minimise both the DC magnetising current of the HFT and the switching losses. The maximum duty cycle for maximum output voltage is equal to 0.6.

A.   Output Filter Design

The output filter is designed in terms of the inductance ripple current I_{ri}, and the damping ratio ξ for a constant output ripple voltage V_{ri}. The following design equations are derived

Inductance :
$$Lo = \frac{(1-D)\cdot Ro}{f_s \cdot I_{ri}}$$
(5.2.1)

Capacitor :
$$Co = \frac{I_{ri}}{8 \cdot f_s \cdot Ro \cdot V_{ri}}$$
(5.2.2)

Also, the damping ratio and the resonant frequency of the filter yields

Damping ratio :
$$\xi = \frac{\sqrt{2 \cdot (1-D) \cdot V_{ri}}}{I_{ri}}$$
(5.2.3)

Resonant frequency :
$$f_r = \frac{1}{\pi} \cdot \sqrt{\frac{2 \cdot V_{ri}}{(1-D)}} \cdot f_s \qquad \cdot$$
(5.2.4)
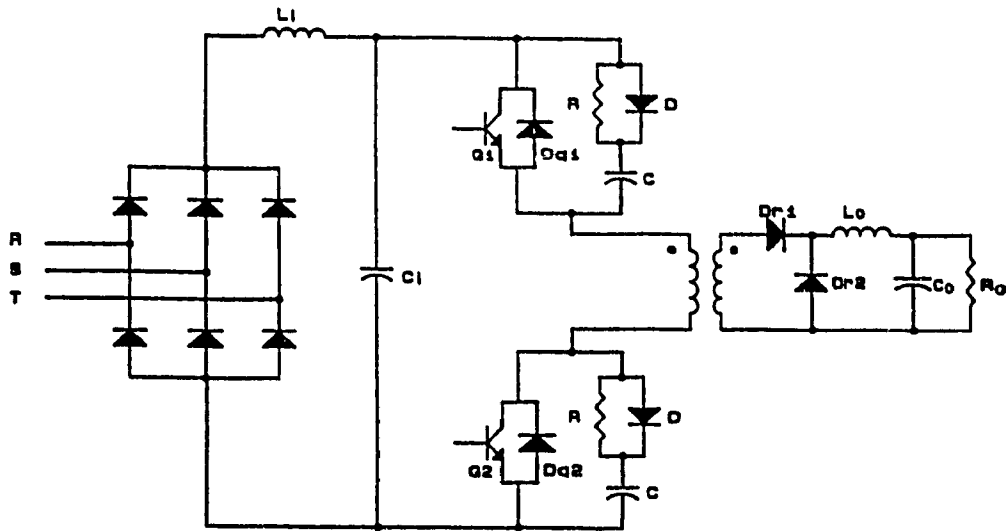
a)
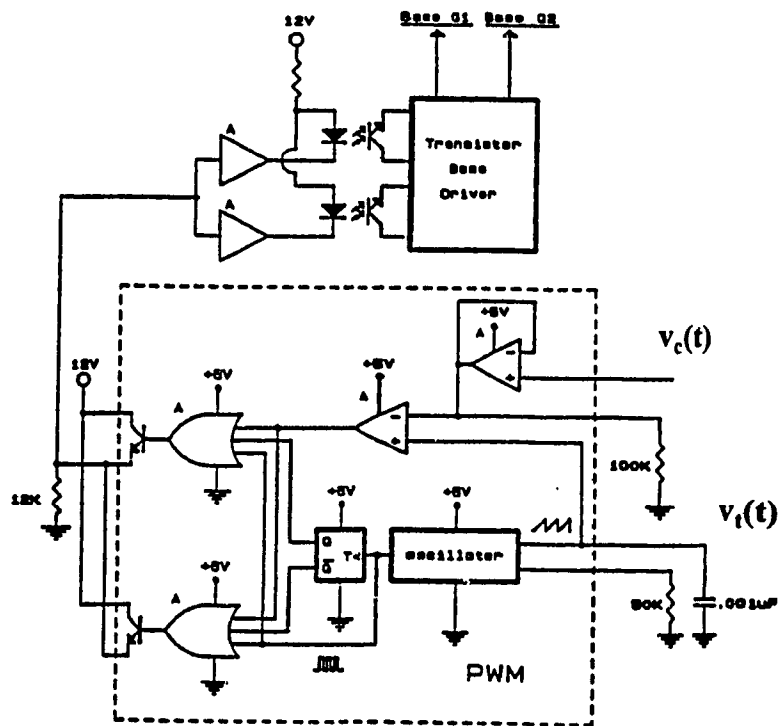
b)

Figure 5.1 The two switch forward DC/DC converter with extended duty cycle capability. a) Power circuit, Li=100 μH, Ci=1000 μF, R=50 Ω, C1=C2=C=0.033 μF, b) PWM modulator and gating signal generator.

where f_s is the switching frequency. It must be noted that the values of L_o, C_o, fr, and ξ become a function of I_{ri}, V_{ri}, and D. Moreover, from (5.2.1) and (5.2.4), shown that increasing the duty cycle decreases the value of inductance and increases the resonant frequency of the output filter. However, based on (5.2.3), higher duty cycle operation with higher ripple current, means lower damping ratio for the output filter. **Table 5.2-I** summarises the design of the filter with V_{ri} = 0.13%, duty cycle D = 0.6 and different values for I_{ri}. Fig. 5.2 illustrates the variation of the damping ratio with the ripple current for two values of duty cycle : D = 0.4 and D = 0.6.

Table 5.2-I

Output Filter Design

Vri=0.13%, D=0.6, Ro=1pu

Iri pu	ξ	Lo μH	Co μF
0.01	3.22	1250	19.2
0.02	1.61	625	38.5
0.03	1.07	417	57.7
0.04	0.81	312	76.9
0.05	0.67	250	96.2
0.06	0.54	208	115.4
0.07	0.46	179	135.0
0.08	0.40	156	153.8
0.09	0.36	139	173.1
0.1	0.32	125	192.3

B.   Open-Loop Performance

Figure 5.3 shows the experimental DC output voltage characteristic without feedback. The DC output impedance is higher at low load (I_0 < 0.3 pu) and decreases as the load current increases. From this data, one can assume an open
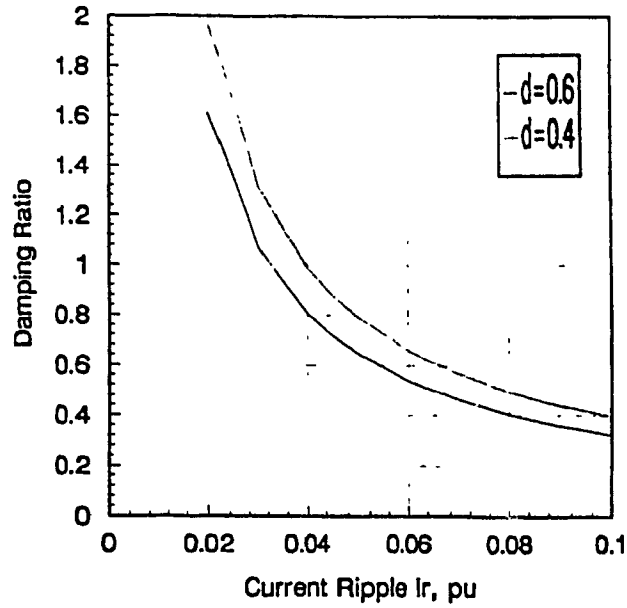
Figure 5.2 Damping ratio ξ as a function of the current ripple factor Iri in the output filter inductor.
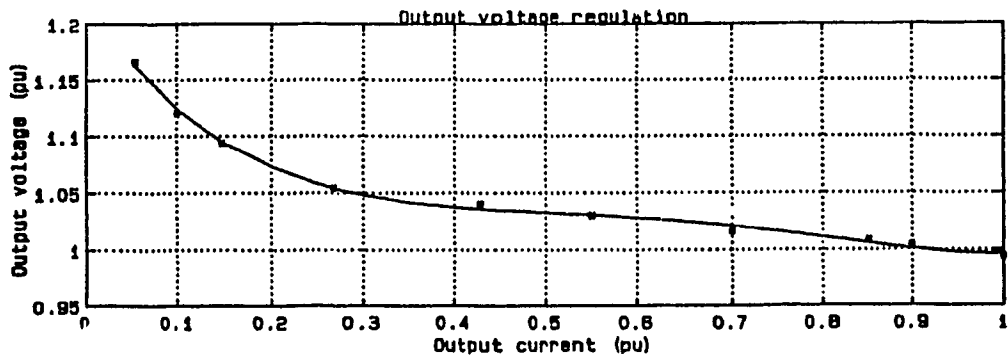
Figure 5.3 DC voltage and current characteristic that shows the open loop voltage regulation of the two-switch converter.
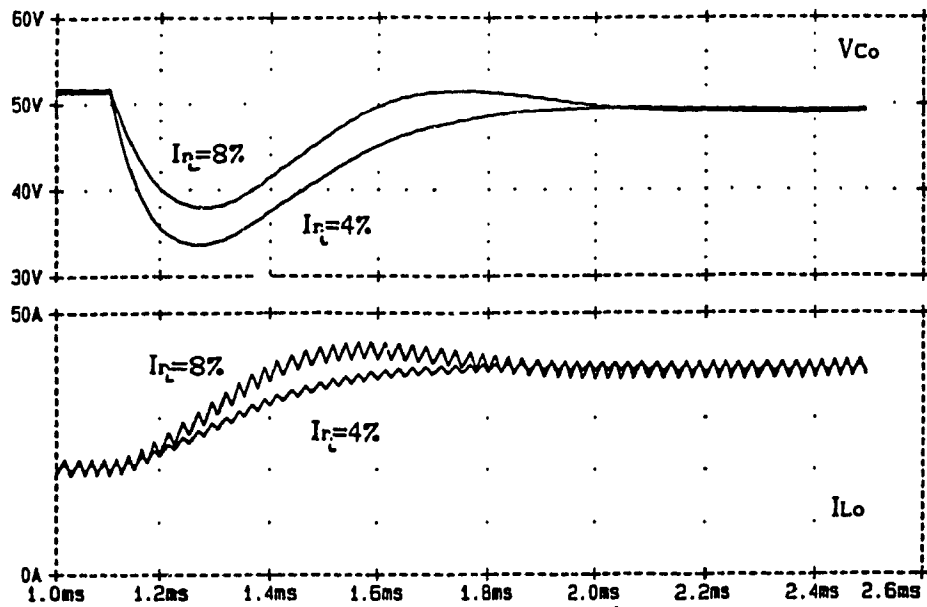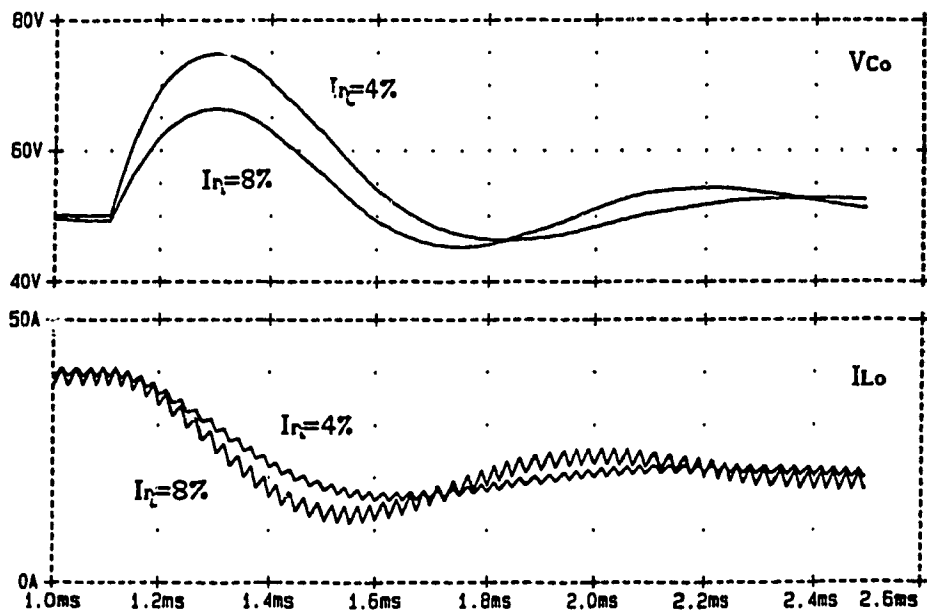
Figure 5.4   Open loop transient response for Iri=4%, Iri=8%, Vri=0.13% and fr=1kHz. a) Step change from 50% to rated load. b) Step change from rated to 50% load.

loop voltage regulation equal to 3% for the power circuit. Fig. 5.4 shows simulation waveforms for 50% step change in the resistive load. These results correspond to $I_{ri} = 4\%$, $I_{ri} = 8\%$, and $V_{ri} = 0.13\%$ for the circuit without feedback. The resonant frequency of the output filter is 1 kHz. A step change decreasing the load produces much higher variation in the output voltage. The resulting output over voltage is 50% with $I_{ri} = 4\%$, and 30% with $I_{ri} = 8\%$. A larger step change in the load will also produce discontinuous current and settling time larger than 5 ms. The aforementioned values are not acceptable for critical load. The controllers presented in this sections are designed to improve the regulation of this converter to less than 0.5%, to provide a settling time less than 0.5 ms with $I_{ri} = 8\%$, and to limit the overvoltage to less than 10% under 50% transient load variation.

5.2.2 Control-Output Transfer Function

The linear control-output transfer function for the converter is given by the following expression :

$$H_c(s) = H_0 \cdot H_1(s) \cdot H_2(s) \qquad\qquad (5.2.5)$$

where H_0 is the dc gain of the converter including the PWM circuit, $H_1(s)$ is the output filter transfer function, and $H_2(s)$ is an all-pass filter transfer function. All of them are described in the following sections.

A.   The DC Gain H_0

The circuit diagram of the PWM gating signal generator is shown in Fig. 5.1 (b). A 3524 integrated circuit (IC) is used to generate the gating signals with a

maximum nominal duty cycle equal to 0.6. The range of operation of the PWM is 1.5 V for maximum duty cycle and maximum load. Hence the DC gain yields

$$H_0 = \frac{\Delta V_0}{\Delta V_{PWM}} = \frac{50}{1.5} = 33.33. \tag{5.2.6}$$

The internal amplifier of the IC is used as a buffer for the error amplifier. The controllers are implemented externally by using other IC containing HF operational amplifiers. Limiting voltage circuits are incorporated to clamp the maximum duty cycle, and the error signal under transient condition.

B.   *The Output Filter, $H_1(s)$*

The transfer function for the output filter is given by

$$H_1(s) = \frac{a_1 s + a_0}{b_2 s^2 + b_1 s + b_0} \tag{5.2.7}$$

where $a_0 = 1$

$a_1 = R_c C_0$

$b_0 = 1$

$$b_1 = \frac{R_0 R_c + R_1 R_c + R_0 R_1}{R_0 + R_1} \cdot C_0 + \frac{1}{R_0 + R_1} \cdot L_0$$

$$b_2 = \frac{R_c + R_1}{R_1 + R_0} \cdot L_0 C_0$$

R_c and R_1 are the equivalent series resistance (ESR) of the output filter capacitor and the equivalent DC series resistance of the converter. The ESR of the output filter capacitor is assumed to be $R_c = 0.02 \ \Omega$. Moreover, from Fig. 5.3 the

equivalent DC resistance of the converter becomes $R_{lmin} = 0.08\ \Omega$ for $0.3 < I_0 < 1$ pu and $R_{lmax} = 0.5\ \Omega$ for $I_0 < 0.3$ pu. The output filter is designed to operate with $I_{ri} = 8\%$ and $V_{ri} = 0.13\%$ at maximum load ($R_{0min} = 1.25\Omega$). Therefore, from **Table 5.2-I**, the respective component values of the filter are $C_0 \approx 150\ \mu F$ and $L_0 \approx 156\ \mu H$. The resulting zero and poles of the output filter yields :

$$Zero : \qquad\qquad\qquad -333 \cdot 10^3\ rdn/s$$

$$Poles : R_{omax} = 2.5\ \Omega: \qquad (-1.643 + 6.41i) \cdot 10^3\ rdn/s$$

$$(-1.643 - 6.41i) \cdot 10^3\ rdn/s$$

$$R_{omin} = 1.25\ \Omega: \qquad (-2.94 + 6.01i) \cdot 10^3\ rdn/s$$

$$(-2.94 - 6.01i) \cdot 10^3\ rdn/s$$

C.   The All-Pass-Constant-Time-Delay Filter

Delay in the voltage loop arise due to:

1) The current commutation between the leakage inductance of the transformer and the output filter inductance during the ON-OFF and OFF-ON switching,

2) The storage time of the power transistor,

3) The parasitic delay in the driver and PWM control circuit, and

4) The sampling process of the switching converter.

The total delay is usually modelled with a zero-order hold or, more recently, with a so-called "equivalent hold". The zero-order hold is usually approximated by using

the exponential term $e^{-T/2s}$. This approach predicts excessive phase lagging at frequency close to half of the switching frequency. The "equivalent hold" is used to transform the small-signal response of the discrete model to a response that is measurable. This approach is accurate but very complicated and is only formulated for ideal converters. In this Thesis, an all-pass-constant-time-delay filter is proposed to model the sampling process of the converter and the total delay in the voltage loop. The general transfer function for this type of filter is given by

$$H_2(s) = \frac{s^2 - a_1 s + a_0}{s^2 + b_1 s + b_0} \qquad (5.2.8)$$

This transfer function can be easily loaded in any software package for control analysis because it is defined as a ratio of polynomials. To affect only the phase, the coefficients a_n and b_n are obtained as follows : $a_1 = 6\,\omega_d$, $a_0 = 2\omega_d^2$, $b_1 = a_1$, $b_0 = a_0$, where $\omega_d = 2\pi \cdot k_d \cdot f_s$. The constant k_d depends on the amount of delay to be considered. Its value is calculated to be $k_d = 0.318$. Fig. 5.5 a) compares the resulting bode diagrams for $H_c(s)$ using the proposed model, the zero-order hold model, and the average model.

5.2.3 Design of the Controllers

A third-order controller is designed to implement the single-loop system. This controller is then modified, becoming a dual-loop control system by adding current feedback. The current signal is taken from the output filter capacitor using
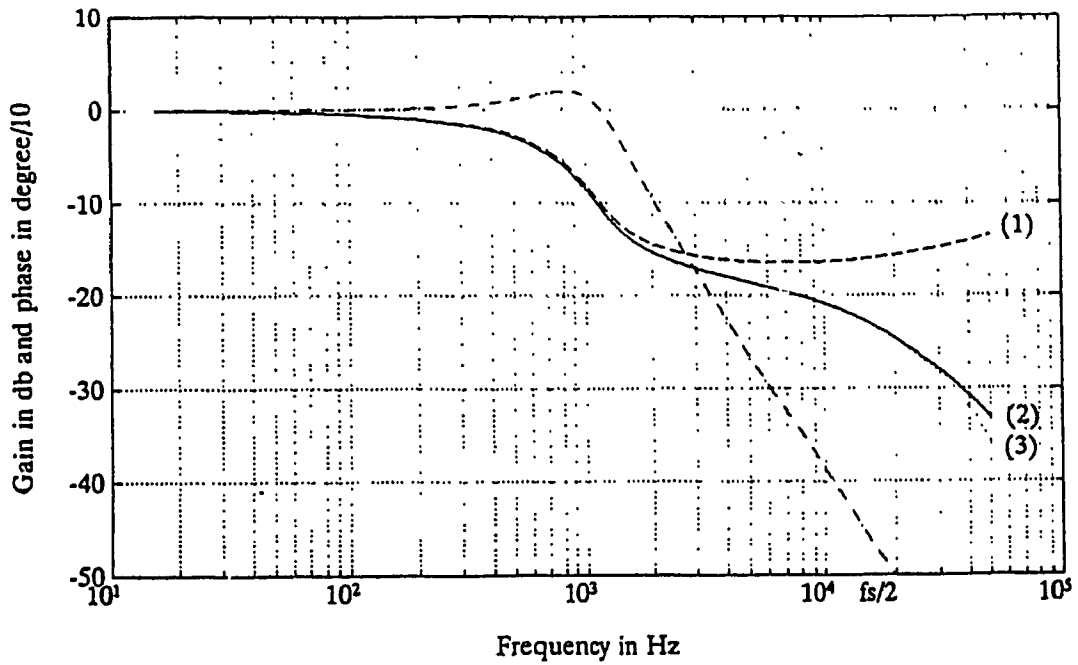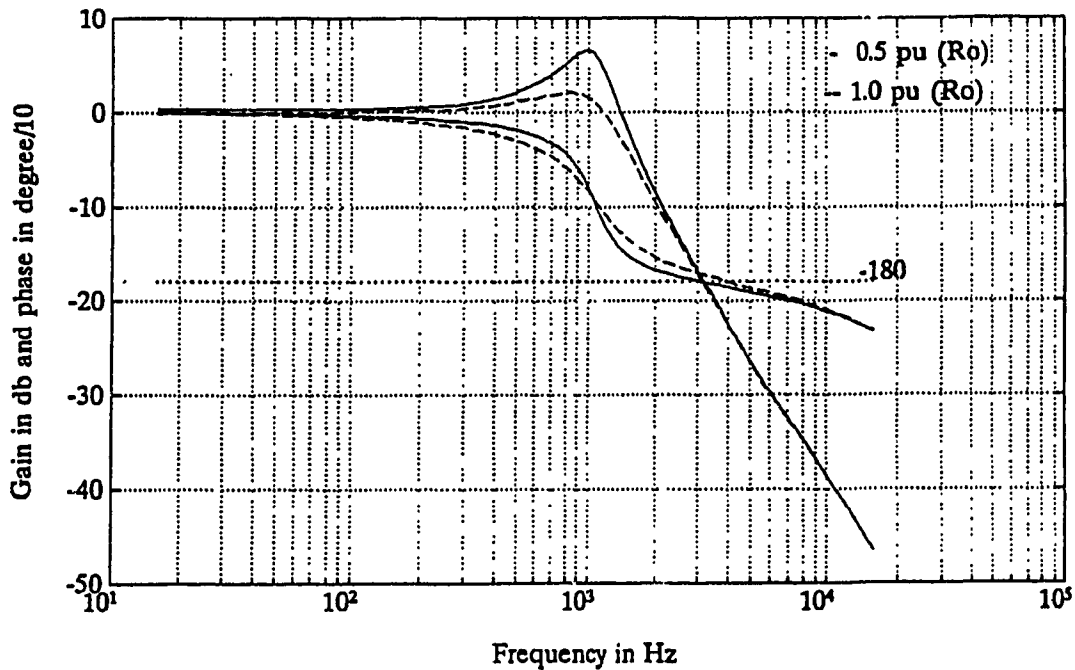
Figure 5.5 Loop Transfer Function without the control circuit. a) Using different models: (1) Average model, (2) Average model with the all-pass-constant-time-delay filter, (3) Average model with exponential term $e^{-(T/2)s}$, b) Loop transfer function with 0.5 and 1 pu load including the all-pass constant-time delay filter.

a small current transformer. The circuit diagrams for both controllers are shown in Fig. 5.6.

A. *Differential Amplifier*

A differential amplifier is used to provide the output voltage feedback signal for the controller. This type of amplifier minimises the common signal noise present in both output terminals. From Fig. 5.6, assuming $R_5 = R_6$, $R_7 = R_8$, the DC transfer function for this amplifier yields

$$H_d \approx \frac{R_7}{R_5} = \frac{R_8}{R_6} \qquad (5.2.9)$$

The resistance's values are found by using (5.2.6). Hence,

$$H_d = \frac{1}{H_0} = \frac{1}{33.3} \approx \frac{R_7}{R_5} \qquad (5.2.10)$$

Assuming input resistance $R_5 = R_6 = 100 \text{ k}\Omega$, then $R_7 = R_8 = 3.3 \text{ k}\Omega$

B. *Loop Transfer Function*

To design the controller the evaluation of the loop transfer function must be done. The loop transfer function without the controller is given by

$$T_1(s) = H_0 \cdot H_1(s) \cdot H_2(s) \cdot H_d \qquad (5.2.11)$$

The loop transfer function (5.2.11) is evaluated by using (5.2.5)-(5.2.10) and the MATLAB computer analysis program. The respective Bode diagrams for 0.5, and 1 pu load are shown in Fig. 5.5 (b). The controllers are designed to have a loop
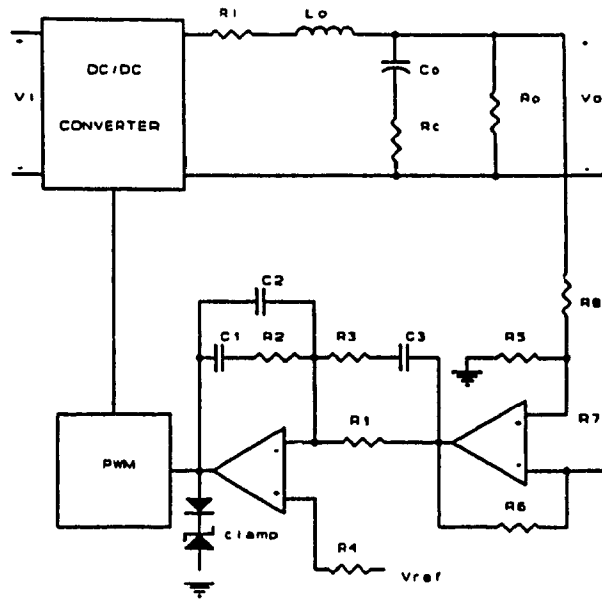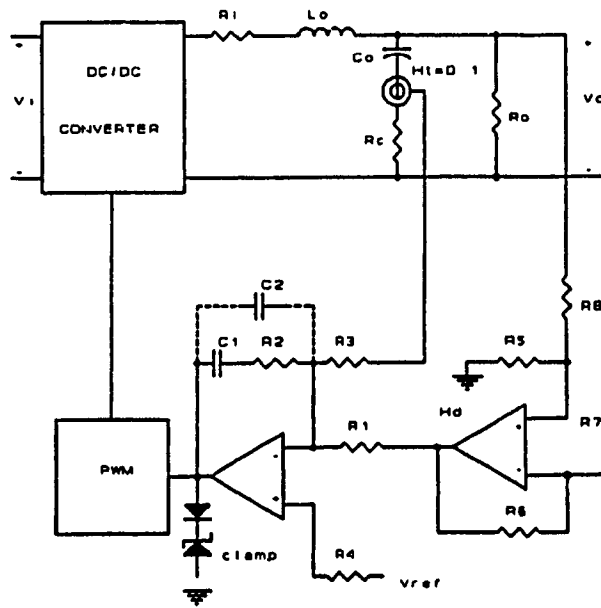
Figure 5.6 The Voltage Mode Control system. a) Controller with a single voltage loop. b) Controller with a dual current/voltage loop.

5-15

cross-over frequency f_c at 4 kHz. Hence, from Fig. 5.5 (b), the necessary gain G at

f_c = 4 kHz at 0.5 pu load is 22.5 db (G = 13.33).

C.   The Single-Loop Control System with a Third-Order Controller

The single-loop control system with the PWM circuit generator is shown in Fig. 5.6 (a). The transfer function for a third-order controller is

$$H_a(s) = \frac{a_2 s^2 + a_1 s + a_0}{b_3 s^3 + b_2 s^2 + b_1 s + b_0}$$

(5.2.12)

where

$a_0 = 1$

$a_1 = R_2 C_1 + (R_1 + R_3) C_3$

$a_2 = (R_1 + R_3) R_2 C_1 C_3$

$b_0 = 0$

$b_1 = (C_1 + C_2) R_1$

$b_2 = [(C_1 + C_2) C_3 R_3 + R_2 C_2 C_1] R_1$

$b_3 = R_3 C_3 R_2 C_2 R_1 C_1$

The factored form of (5.2.11) is

$$H_a(s) = \frac{(1 + R_2 C_1 s) \cdot (1 + (R_1 + R_3) C_3 s)}{R_1 (C_1 + C_2) s \cdot (1 + R_3 C_3 s) \cdot \left(1 + R_2 \frac{C_1 C_2}{C_1 + C_2} s\right)}$$

(5.2.13)

The third-order controller is designed by using the "K factor method" proposed in [20]. This method does not require trial-and-error effort to obtain the required

maximum boost phase at f_c Using this method the zeros and poles of (5.2.13) are located as follows: Two zeros are located at the frequency $w_z = 2\pi f_c / \sqrt{K}$. Hence,

$$w_z = \frac{1}{R_2 C_1} = \frac{1}{(R_1 + R_3)C_3} = 2\pi f_c / \sqrt{K}$$

Two poles are located at the frequency $w_p = 2\pi f_c / \sqrt{K}$. Hence,

$$w_p = \frac{1}{R_3 C_3} = \frac{1}{R_2 \dfrac{C_1 C_2}{C_1 + C_2}} = 2\pi f_c / \sqrt{K}$$

Factor K is obtained from the following expression

$$K = \{\tan[(B/4) + 45]\} \tag{5.2.14}$$

where B in (5.2.14) is the required phase boost at f_c and is given by

$$B = M - P - 90° \tag{5.2.15}$$

where P = modulator phase shift and M = phase margin. The component values for the control circuit are obtained as follows :

$$R_1 = 10 \text{ k}\Omega \qquad\qquad C_2 = \frac{1}{2\pi f_c G R_1} \tag{5.2.16}$$

$$R_2 = \frac{\sqrt{K}}{2\pi f_c C_1} \qquad (5.2.17) \qquad C_1 = C_2(K-1) \qquad (5.2.18)$$

$$R_3 = \frac{R_1}{(k-1)} \qquad (5.2.19) \qquad C_3 = \frac{1}{2\pi f_c \sqrt{K} R_3} \qquad (5.2.20)$$

where G is the gain at f_c. Fig. 5.7(a) illustrates the bode diagram of (5.2.13) for f_c = 4 kHz and G = 13.33 and different phase margin M. It follows that a large
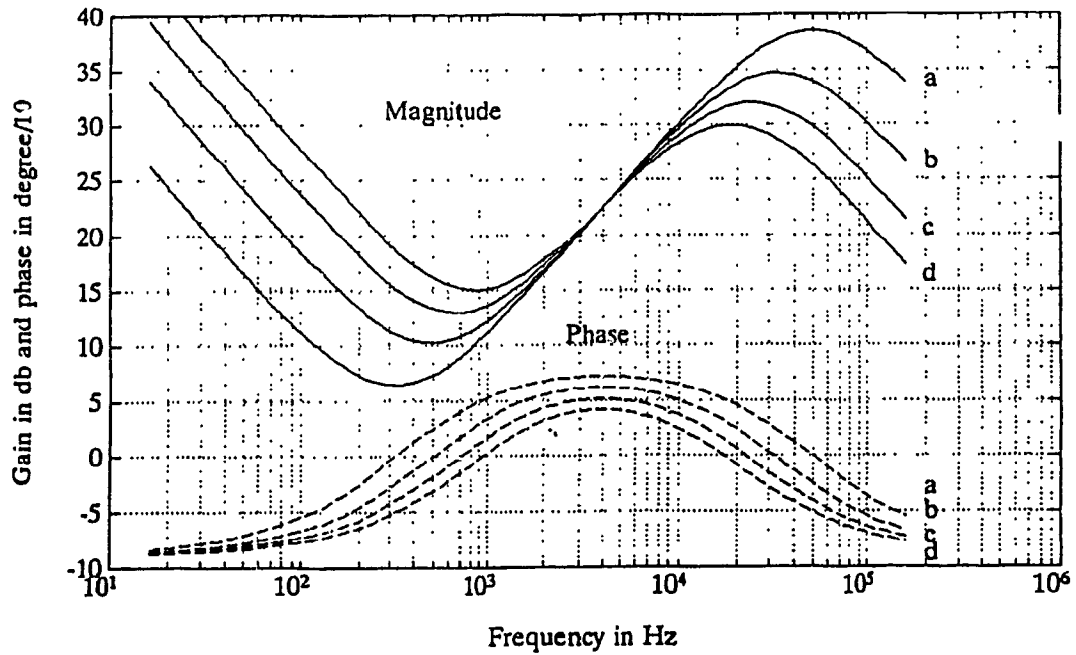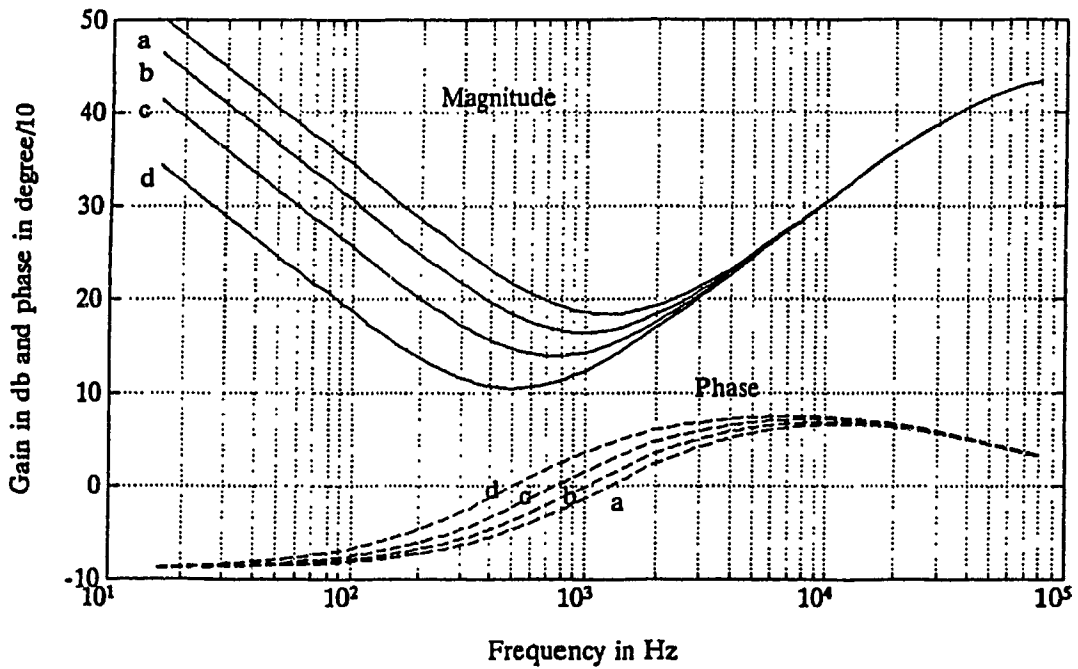
Figure 5.7 Controller transfer function design, fc=4 kHz, G=22.5 Db. a) The third order controller designed by using the K factor method. Phase margins are: a=70° b=60° c=50° d=40°. b) The equivalent voltage transfer function for the dual-loop control system without C_2. Frequency of the zeros are: a=1.25 kHz, b=1kHz, c=750 Hz, d=500Hz.

phase margin reduces the gain at low frequency and increases the resonant peak of

the filter ($f_0 = 1$ kHz). The phase margin is selected to be $60°$. From Fig. 5.5 b) the

value of P at f= 4 kHz is -182°. Therefore, from (5.2.15) the required phase boost

B = 152° and from (5.2.14) the K factor is 66.33. Finally, the synthesis of the

control circuit is done by using (5.2.16) to (5.2.20). **Table 5.2-II** presents the

component values of the control circuit

Table 5.2-II

Summary of the Control Circuit Design

Component		R_1 kΩ	R_2 kΩ	R_3 kΩ	R_4 kΩ	C_1 nF	C_2 nF	C_3 nF
fc=4kHz Ro=1.25Ω Rl=0.08Ω Rc=0.02Ω Lo=156 uH Co=150 uF Hd=1/33.33 Ht=0.1Ω								
Single loop		10.0	16.6	0.2	10.0	19.5	0.3	32.0
Dual Loop	C_2=0	10.0	33.0	32.0	7.6	4.8	-	-
	$C_2\neq0$	10.0	16.6	15.6	6.1	19.5	0.3	-

Fig. 5.8 (a) shows the Bode diagram of the transfer function. The Bode diagram of

the loop transfer function for 0.5 pu load including this controller is shown in Fig.

5.8 (b).

D.   The Dual-Loop Control System

The third-order controller in the single-loop control system has the problem

of an increased number of capacitors (3) whose values can change during the time

and the temperature variation, modifying the required minimum phase margin for

stability. Moreover, under a large transient operation condition the control loop

could be temporarily open and the capacitors of the control circuit could be
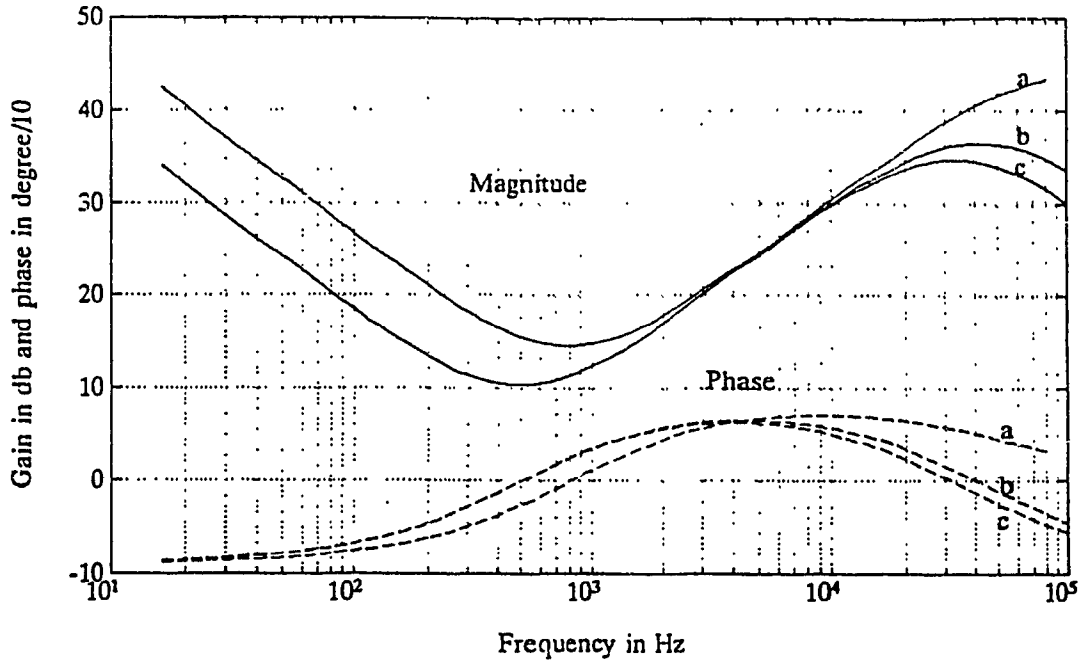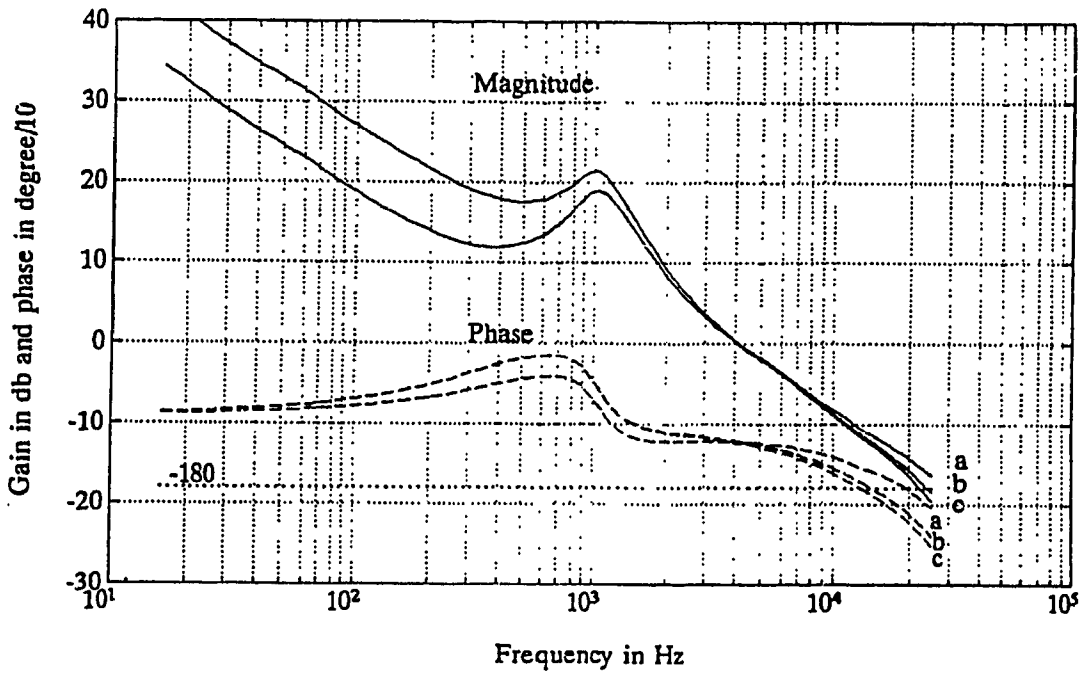
Figure 5.8   Summary of the control design, fc=4 kHz, G=22.5 db (13.33). a) Control transfer function: a=dual loop without C_2, $f_{z1,z2}$=800 Hz, b=dual loop with C_2, M=60°, c=single loop, M=60°. b) Loop transfer function including the controllers: a=dual loop without C_2, b=dual loop with C_2, c=single loop.

overcharged providing a false correction of the output voltage when the loop is again able to resume functioning. To minimise the above problems the single-loop control system is modified in a dual-loop control system including current feedback. The circuit diagram is shown in Fig. 5.6 (b). The current loop provides a direct information of the derivative of the output voltage, which means that C_3 can be removed (see Fig. 5.6 (a)). To design the controller for this system, an equivalent single-loop voltage transfer function is derived. Two cases are examined : without C_2, and with C_2 (see Fig. 5.6 (b)).

Equivalent Single-Loop Voltage Transfer Function without C_2: The voltage across the capacitor C_o is

$$V_{C_o}(s) = \frac{1}{1 + R_c C_o s} \cdot V_o(s) \tag{5.2.21}$$

Hence, the current through C_o is $I_{C_o(s)} = C_o s V_{C_o}$. Therefore, the signal provided by the current transformer is

$$V_{ki}(s) = H_t \cdot I_{C_o}(s) = H_t \cdot C_o s \cdot V_{C_o}(s) = H_t \cdot \frac{C_o s}{1 + R_c C_o s} \cdot V_o(s) \tag{5.2.22}$$

The output control signal $V_c(s)$ is a function of the current $I_{C_o}(s)$ and the output voltage $V_0(s)$. Hence it is given by

$$V_c(s) = H_i(s) \cdot H_t \cdot I_{C_o}(s) + H_v(s) \cdot H_d \cdot V_o(s) \tag{5.2.23}$$

where $H_i(s)$ is a transfer function for the current signal and $H_v(s)$ is a transfer function for the voltage signal, both defined as follows :

$$Hi(s) = \frac{(1 + R_2 C_1 s)}{R_3 C_1 s} \qquad (5.2.24)$$

$$Hv(s) = \frac{(1 + R_2 C_1 s)}{R_1 C_1 s} \qquad (5.2.25)$$

Therefore, from (5.2.21) to (5.2.25) the following equivalent single-loop voltage transfer function is obtained :

$$Hb(s) = \frac{(1 + R_2 C_1 s) \cdot \left(1 + \left(\frac{H_t R_1}{H_d R_3} + R_c \right) C_o s \right)}{R_1 C_1 s \cdot (1 + R_c C_o s)} \qquad (5.2.26)$$

Close examination of (5.2.26) shows that, with the current loop the zero in the transfer function (5.2.7) is eliminated. Then, without the pole $1/R_c C_o$, (5.2.26) is equivalent to a proportional plus integral plus derivative type of control (PID). However, one can take advantage of (5.2.26) to design this control system in the frequency domain as follows. The two zeros of (5.2.26) are considered equals and to be located close to the resonant frequency of the filter ($f_r = 1$ kHz). This will reduce the resonant peak of the loop transfer function and will provide phase boost above the resonant frequency of the output filter. With these conditions and by using (5.2.26) the following design equations are derived :

$$\frac{R_2}{R_1} \left(\frac{H_t R_1}{H_d R_3} + R_c \right) C_o = \frac{G}{2 \pi f_c} \qquad (5.2.27)$$

$$\left(\frac{H_t R_1}{H_d R_3} + R_c \right) C_o = R_2 C_1 \qquad (5.2.28)$$

$$\omega_z = 2\pi f_z = \frac{1}{R_2 C_1} \qquad (5.2.29)$$

where $R_1 = 10 \text{ k}\Omega$ $f_c = 4 \text{ kHz}$, $G = 13.33$, $H_d = 1/33.33$, $H_t = 0.1$, $C_o = 150 \text{ }\mu\text{F}$, and $R_c = 0.02 \text{ }\Omega$. Therefore, once f_z (ωz) is selected, the component values of the control circuit can be calculated by using (5.2.27) to (5.2.29). Figure 5.7 (b) shows the Bode diagrams of (5.2.26) for different values of f_z. **Table 5.2-II** and Fig. 5.8 (a) summarises the design of the control circuit for $f_z = 800 \text{ Hz}$. Fig. 5.8 (b) shows the loop transfer function including the controller. It follows that with the zeros located close to the resonant frequency of the output filter the lows-frequency gain is higher and the resonant peak of the loop transfer function is lower as compared with the previous design.

Equivalent Single-Loop Voltage Transfer Function with C_2: The capacitor C_2 can be added to eliminate high-frequency component and to minimise noise problem in the voltage loop. Following the same method of the previous section the current and voltage transfer function are

$$H_i(s) = \frac{(1 + R_2 C_1 s)}{R_3(C_1 + C_2) \cdot \left(1 + R_2 \dfrac{C_1 C_2}{C_1 + C_2} s\right)} \qquad (5.2.30)$$

$$H_v(s) = \frac{(1 + R_2 C_1 s)}{R_1(C_1 + C_2) \cdot \left(1 + R_2 \dfrac{C_1 C_2}{C_1 + C_2} s\right)} \qquad (5.2.31)$$

Therefore, by using (5.2.23), (5.2.30), and (5.2.31) the equivalent single-loop voltage transfer function yields

$$H_b(s) = \frac{(1 + R_2 C_1 s) \cdot \left(1 + \left(\dfrac{H_t R_1}{H_d R_3} + R_c\right) C_0 s\right)}{R_1 (C_1 + C_2) s \cdot (1 + R_c C_0 s) \cdot \left(1 + R_2 \dfrac{C_1 C_2}{C_1 + C_2} s\right)} \qquad (5.2.32)$$

Expression (5.2.32) has a similar form to the third-order controller (5.2.13). Thus, to design this controller the zeros can be located both at the same frequency. The frequency of these zeros can be selected to be close to the resonant frequency of the output filter or it can be calculated by using the K factor method. The first method is a better design, however to compare the performance with the control system presented in the Section 5.2.3 C the last method will be used. Hence, the component values for R_1, R_2, C_1, and C_2 are identical to these already calculated in Section 5.2.3 C The value of R_3 is obtained by using (5.2.28). The design is summarised in **Table 5.2-II**. Fig. 5.8 (a) shows the resulting bode diagram of (5.2.32) and Fig. 5.8 (b) shows the Bode diagram of the loop transfer function.

5.2.4. Simulation Results

Simulation results of the transient response with a 50% step change in the load using the single and dual-loop control system are shown in Figs. 5.9 and 5.10, respectively. The results show that the model and the design procedure predict and
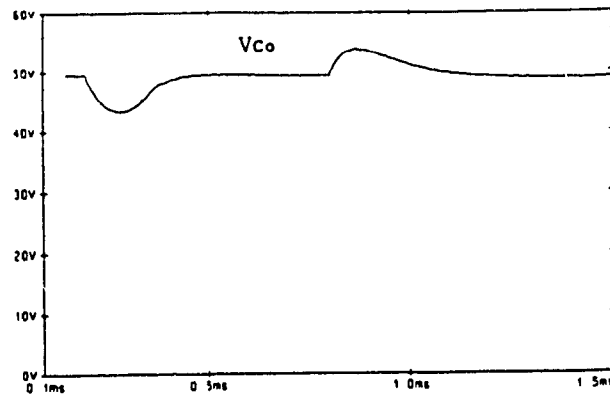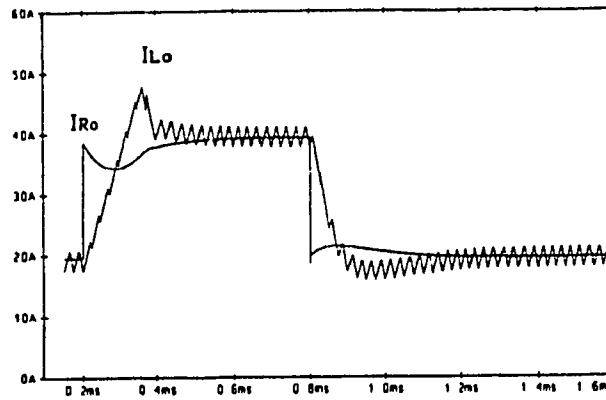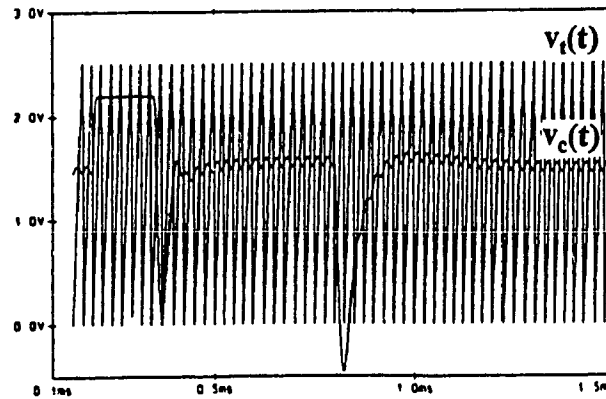
Figure 5.9 Transient response for 50% step change in the load with the single voltage loop control system. a) Output voltage. b) output filter inductance current, and load current. c) voltage error.
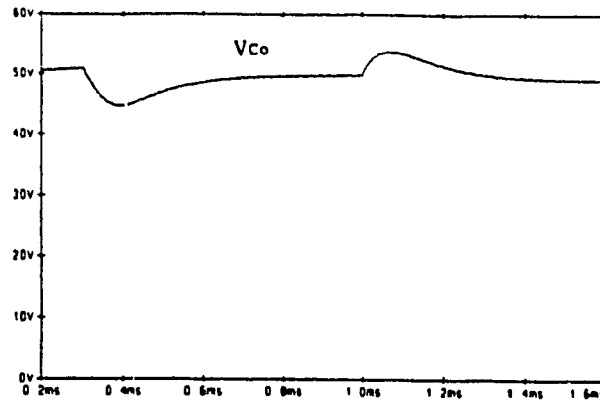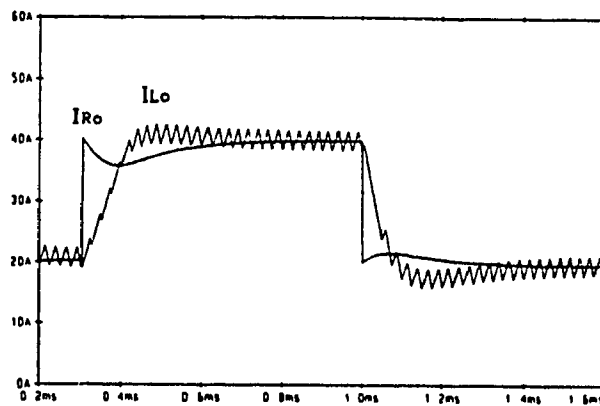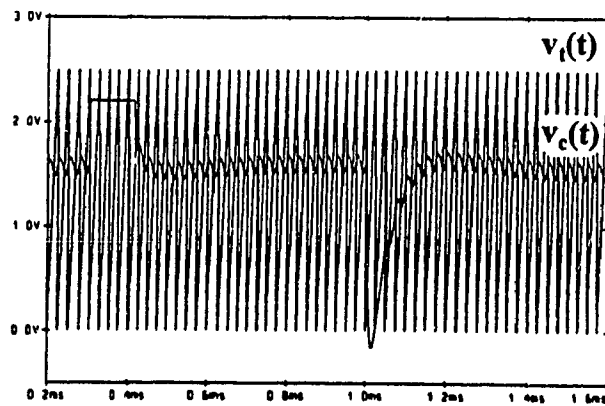
Figure 5.10 Transient response for 50% step change in the load with the single voltage loop control system. a) Output voltage. b) output filter inductance current, and load current. c) voltage error.

ensure well the stability of the system even for large variation of load. The dual

loop shows a lower overshoot in the output filter current

5.3 System II: A New Current Assisted Voltage Mode Control

This Section presents a novel approach to the regulation of the output

voltage in high-power forward converters. The proposed control scheme

implements a fast AC current loop by sensing the current through the output filter

capacitor with a small transformer as is shown in Fig. 5.11. Load current

feedforward is inherent, saving one current sensor. The control loop forces the AC

current component of the output filter to be synchronised with a symmetrical

triangular waveform defining the switching frequency. Fig. 5.12 shows a typical

waveform at 50% duty cycle. The proposed control technique has properties of

both CMC and VMC. In fact, the following features can be achieved.

1) Constant frequency operation

2) Low-output impedance

3) No dc error in the current loop

4) Fast transient responses for step change of the load

5) Synchronous operation of power stages in parallel

6) Stable current mode of operation by using a standard PI control

7) AC input voltage feedforward
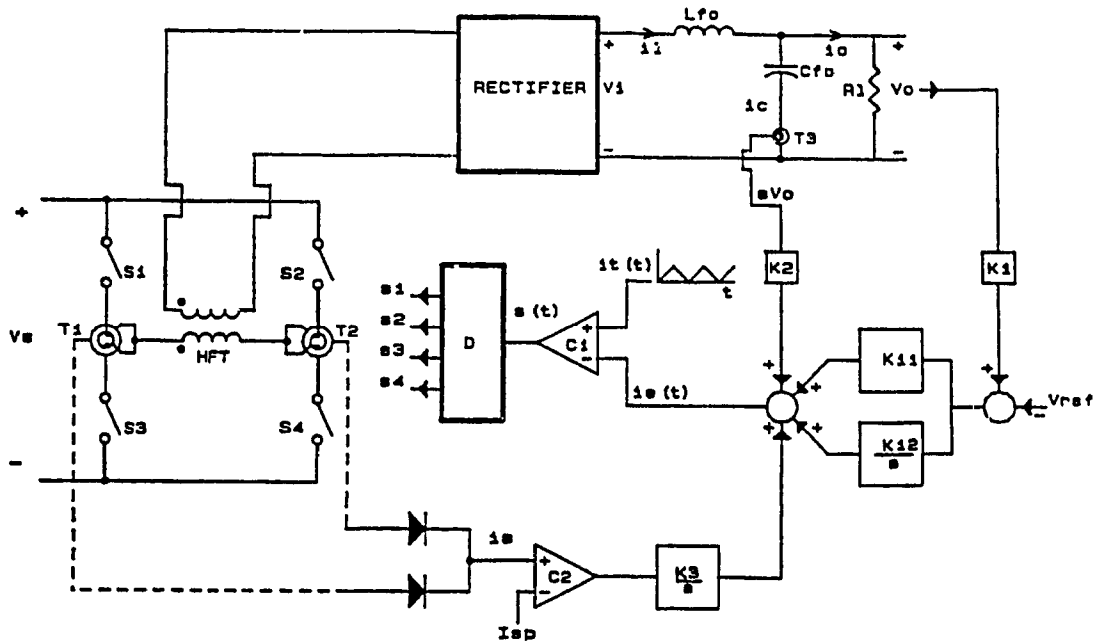
Figure 5.11   The propossed current assisted voltage control method
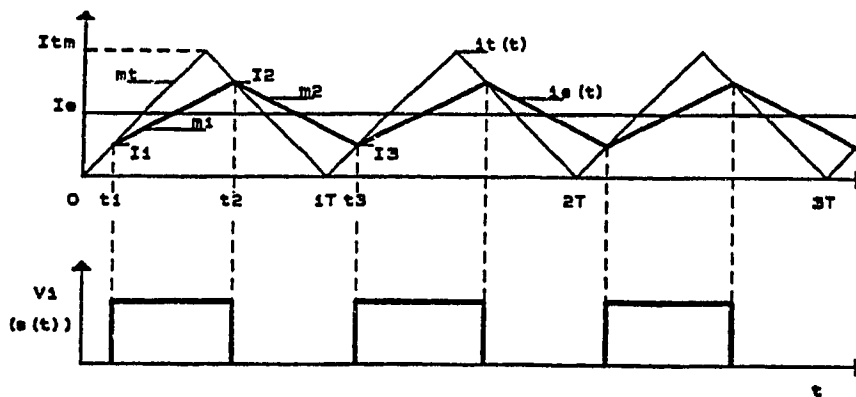
Figure 5.12 Principle of the synchronous ripple current and PWM control

This Section presents the analysis and evaluation of the proposed control technique using a buck converter. A small-signal model is derived, and the stability of the current loop by means of characteristic equation of the system is discussed. Bode diagrams for the current and voltage loop are derived to design the controllers. Finally, simulation and experimental results are presented to illustrate the main features and to verify the theory.

5.3.1 Principle of Operation

Typical forward converters require the output filter be designed to meet a maximum output voltage ripple, usually less than 1%, and with a resonant frequency much lower than the switching frequency of the converter. Because of this, and also due to the action of the voltage feedback loop, the capacitor behaves as a dc voltage source. Thus, it is practically a short circuit for the HF AC current component of the output filter inductor. The approach proposed here takes a sample proportional to this almost triangular AC current by using a small transformer and compares it with a symmetrical reference triangular waveform (RTW) as is shown in Fig. 5.12. If the slope of the RTW is much higher than this current, the ripple of the output inductor current is synchronised with the RTW. Hence, the current loop directly defines the turn-on and turn-off time of the power switches whenever the AC current sample reaches the rising of falling values of the RTW. Moreover, in the proposed control method the duty cycle is affected by

both slopes of the inductor current (double-edge PWM control), and there is no dc error in the current loop. The duty cycle can be further modified by introducing a dc signal in series with the current loop (i.e., the voltage error). Since the AC current is synchronised with the RTW. the switching frequency can be modified by changing the frequency of the RTW. However, to provide switch short-circuit protection in the proposed control method, current sensors (T1 and T2) connected in series with the power switch are required, as is shown in Fig. 5.11.

5.3.2 DC Characteristics

The circuit elements in Fig. 5.11 are assumed to be ideal. From the geometry of waveforms shown in Fig. 5.12, and by assuming a linear output inductor current variation, the following equations can be derived. The reference waveform, $i_t(t)$ is

$$i_t(t) = m_t \cdot t \qquad T/2 \geq t \geq 0 \qquad (5.3.1)$$

$$i_t(t) = - m_t \cdot (t - T) \qquad T \geq t \geq T/2 \qquad (5.3.2)$$

where T is the switching period. Also, m_t is the slope of the RTW and is given by

$$m_t = 2 \cdot f_s \cdot I_{tm} \qquad (5.3.3)$$

The sample of the AC current, $i_e(t)$ is

$$i_{eON}(t) = m_1 \cdot (t - t_1) + I_1 \quad t_2 \geq t \geq t_1 \qquad (5.3.4)$$

$$i_{eOFF}(t) = m_2 \cdot (t - t_2) + I_2 \quad t_3 \geq t \geq t_2 \qquad (5.3.5)$$

$$t_3 = t_1 + T \qquad (5.3.6)$$

where m_1 and m_2 are the positive and negative slopes of the output filter inductance current. These slopes depend on the maximum input voltage of the output filter V_i, the average value of the output voltage V_0, and the output filter inductance, L_{fo}, as follows .

$$m_1 = \frac{V_i - V_0}{L_{fo}} \qquad (5.3.7)$$

$$m_2 = -\frac{V_0}{L_{fo}} \qquad (5.3.8)$$

For synchronous ripple operation $m_1 < m_t$ and $m_2 > -m_t$. Under these operating conditions the average duty cycle D yields

$$D = \frac{t_2 - t_1}{T} \qquad (5.3.9)$$

and $$-D = \frac{t_3 - t_2}{T} \qquad (5.3.10)$$

The DC characteristics are derived by using (5.3.1)-(5.3.10). In fact, from these equations the following boundary conditions are obtained :

$$m_1 \cdot D + m_2 \cdot (1-D) = 0 \qquad (5.3.11)$$

and $$I_e = \frac{m_t \cdot (1-D)}{2 \cdot f_s} \qquad (5.3.12)$$

Also, from (5.3.7) to (5.3.12) it follows that

$$D = \frac{V_0}{V_i - V_0} \cdot \frac{2 \cdot f_s}{m_t} \cdot I_e \qquad (5.3.13)$$

The foregoing expressions show that by using the proposed AC current forward loop, the ratio of the inductor current slopes m_1 to m_2 is unique. This means that there is only one steady state for each value of the duty cycle. Moreover, (5.3.13) illustrates that if the difference V_i-V_0 increases, the duty cycle decreases. Therefore, it is not strictly necessary to compensate for AC input voltage variation.

5.3.3 The Small-Signal Converter Model

In this section a small-signal continuous linear model is developed for the pulse width modulator (PWM) including the current loop and the power circuit of the converter.

A. PWM Modulator with the Current Loop

Assuming that f_s and m_t are constant, the PWM transfer function can be obtained from (5.3.13) by using the concept of a small perturbation around of an operating point. Hence,

$$(D + \Delta D) = \frac{(V_0 + \Delta V_0)}{(V_i + \Delta V_i) - (V_0 + \Delta V_0)} \cdot \frac{2 \cdot f_s}{m_t} \cdot (I_e - \Delta I_e) \qquad (5.3.14)$$

After eliminating the small term products, the DC components products, and by using (5.3.3), the following expression is obtained :

$$\Delta D = -\Delta I_e \cdot \frac{D}{1-D} \cdot \frac{1}{I_{tm}} + \Delta V_0 \cdot \frac{1}{V_i(1-D)} - \Delta V_i \cdot \frac{D}{V_i(1-D)} \qquad (5.3.15)$$

Therefore, the respective AC PWM gains for the different variables are

$$\frac{\Delta D}{\Delta I_e} = \frac{D}{1-D} \cdot \frac{1}{I_{tm}} \qquad (5.3.16)$$

$$\frac{\Delta D}{\Delta V_0} = \frac{1}{V_i(1-D)} = \frac{D}{V_0(1-D)} \qquad (5.3.17)$$

$$\frac{\Delta D}{\Delta Vi} = \frac{D}{V_i(1-D)} = \frac{D^2}{V_0(1-D)} \qquad (5.3.18)$$

Notice that a DC component needs to be added to the current loop otherwise the PWM modulator will be saturated to the maximum duty cycle. The DC operating point is given by (5.3.13). The DC component I_e is provided by the voltage loop or by a DC reference (I_r).

B.   Converter Model

A three-port large-signal model for the converter is given by the following expressions :

$$i_g(t) = i_i(t) \cdot \delta(t) \qquad (5.3.19)$$

$$v_i(t) = v_g(t) \cdot \delta(t) \qquad (5.3.20)$$

with $v_g(t) = n_t \cdot v_s(t)$ and $i_g(t) = (i_s(t)/n_t)$, where n_t is the high-frequency transformer turns ratio (HFT) and $\delta(t)$ is a switching function. The small-signal continuous linear model for the converter is derived form (5.3.19) and (5.3.20) as follows :

$$I_g + \Delta I_g = (I_i + \Delta I_i) \cdot (D + \Delta D) \qquad (5.3.21)$$

$$V_i + \Delta V_i = (V_g + \Delta V_g) \cdot (D + \Delta D) \qquad (5.3.22)$$

Hence: $\Delta I_g \approx I_i \cdot \Delta D + D \cdot \Delta I_i \qquad (5.3.23)$

$$\Delta V_i \approx V_g \cdot \Delta D + D \cdot \Delta V_g \qquad (5.3.24)$$

C. Filter Transfer Function

Assuming a lossless capacitor and inductor, the respective function for the capacitor current and voltage in Laplace domain are

$$H_i(s) = \frac{I_c(s)}{V_i(s)} = \frac{\frac{1}{L_{fo}} \cdot s}{s^2 + \frac{1}{R_i C_{fo}} \cdot s + \frac{1}{L_{fo} C_{fo}}} \tag{5.3.25}$$

$$H_v(s) = \frac{V_o(s)}{V_i(s)} = \frac{1}{s \cdot C_{fo}} \cdot H_i(s) \tag{5.3.26}$$

The resulting linear model of the system is shown in Fig. 5.13.

5.3.4 Dynamic Performance

The dynamic performance of the converter using the proposed current control loop are discussed in this section. The respective loop gains are determined assuming that the line input voltage perturbation, $V_g(s)$, is set to zero and the output voltage perturbation due to the input voltage is minimised by the current loop (i.e., $\Delta V_o = 0$ in (5.3.15)). A signal flow graph of the system is shown in Fig 5.14. The minimum internal loops are clearly illustrated in this diagram. It will be used hereafter to determine the characteristic polynomial of the system and the voltage/current transfer functions.

A. The Current and Voltage Transfer Function

From the signal flow graph shown in Fig. 5.14 (a) three loops are identified. The respective gains are
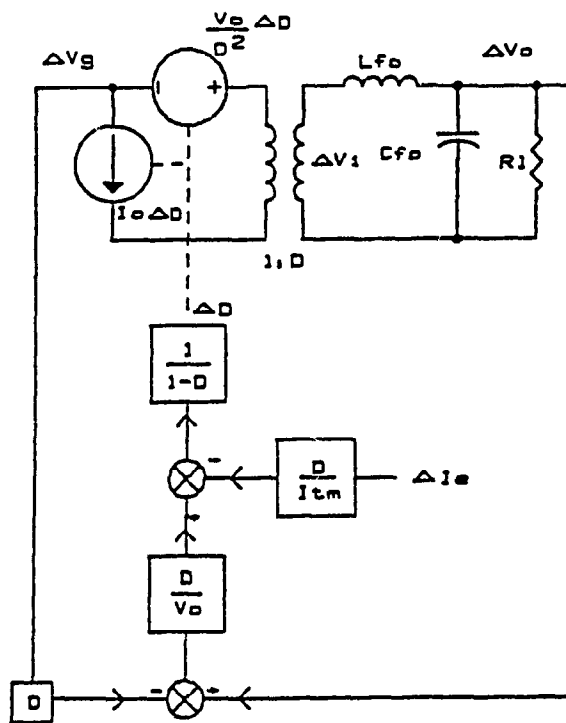
Figure 5.13 Block diagram representation of the PWM control system including the current loop. Continuous average linear model.
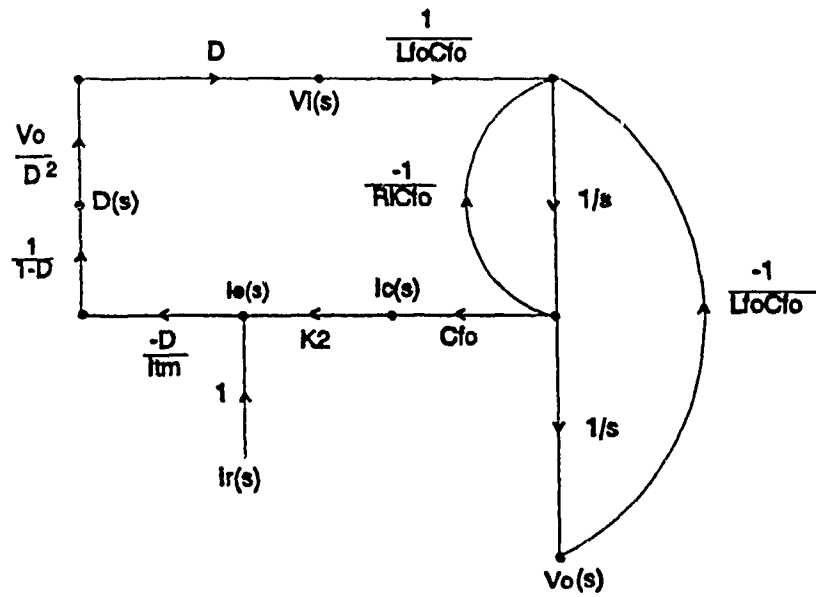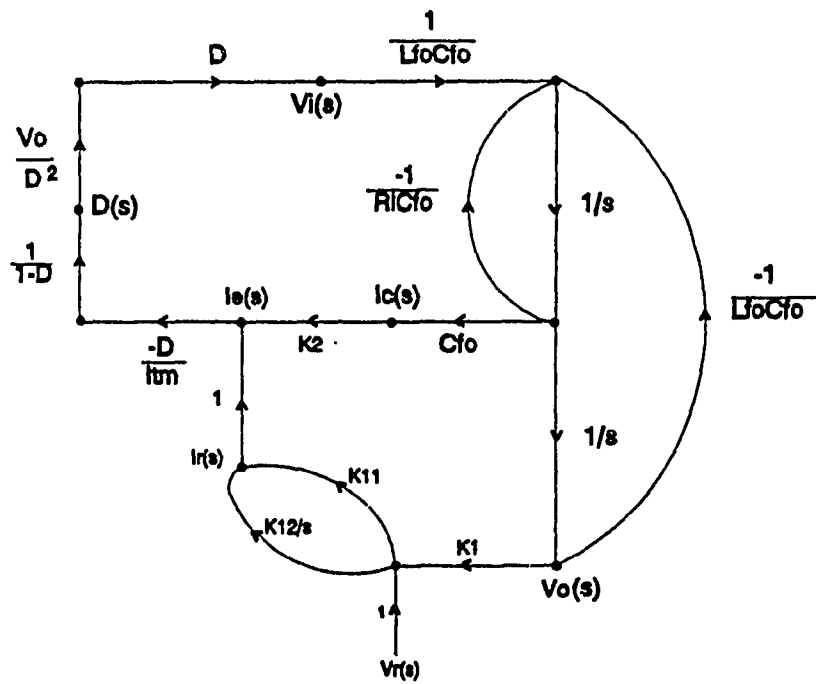
Figure 5.14 Signal flow graph of the system. a) Current loop with a DC refer. b) Current- voltage loop including a PI controller.

$$T_1 = -\frac{1}{R_1 C_{fo}} \cdot \frac{1}{s} \tag{5.3.27}$$

$$T_2 = -\frac{R_m}{L_{fo}} \cdot \frac{D}{1-D} \cdot \frac{1}{s} \tag{5.3.28}$$

$$T_3 = -\frac{1}{L_{fo} C_{fo}} \cdot \frac{1}{s^2} \tag{5.3.29}$$

where $R_m = (K_2 V_0 / D I_{tm})$. By using Mason's gain formula the characteristic polynomial of the system is obtained as follows :

$$\Delta = 1 - (T1 + T2 + T3 \ldots) + (T_1 T_2 \ldots). \tag{5.3.30}$$

The products $T_1 T_2 \ldots$ are all zero, hence the characteristic polynomial of the system including the current loop yields

$$s^2 D = s^2 + \left(\frac{1}{R_1 C_{fo}} + \frac{R_m}{L_{fo}} \cdot \frac{D}{1-D} \right) \cdot s + \frac{1}{L_{fo} C_{fo}} \tag{5.3.31}$$

Equation (5.3.31) shows that the current loop introduces the factor $R_m \cdot D/(1-D)L_{fo}$.

Thus, the position of the poles of the system are modified as follows :

$$s1 = -\frac{1}{2}\left(\frac{1}{R_1 C_{fo}} + \frac{R_m}{L_{fo}} \cdot \frac{D}{1-D} \right) \mp \frac{1}{2} \sqrt{ \left(\frac{1}{R_1 C_{fo}} + \frac{R_m}{L_{fo}} \cdot \frac{D}{1-D} \right)^2 - \frac{4}{C_{fo} L_{fo}} } \tag{5.3.32}$$

From (5.3.32) one can conclude that the current loop increases the dumping ratio of the system. Notice also that with a large value of R_m, $(R_m/L_{fo}) \cdot (D/1 - D) \gg (1/R_1 C_{fo})$. Thus, the position of the poles becomes almost independent of the load. As an example, current and voltage transfer functions have been obtained with $L_{fo} = 85 \ \mu H$, $C_{fo} = 200 \ \mu F$, $R_m = 3$, $D = 0.5$, and $R_1 = 3 \ \Omega$. The Bode

diagrams of the open loop and current and voltage transfer functions are shown in Fig. 5.15 (a), and the Bode diagrams closing the current loop are shown in Fig. 5.15 (b). A comparison of Fig. 5.15 (a) to Fig. 5.15 (b) verifies that the current loop eliminates the resonant peak of the open-loop voltage transfer function and the resulting poles are real.

B.   Voltage Loop with PI Control

The current loop reduces the output impedance and increases the damping ratio of the system but does not provide DC output voltage regulation. Because the system with the current loop has two distinct real poles, which can be located quit separated (see Fig. 5.15 (b)), a good regulation can be achieved by using a proportional-integral controller (PI) in the voltage loop. Furthermore, since one pole is located at high frequency, the PI controller can be designed with a large gain to obtain a fast transient response. The respective signal flow graph of the system with a PI controller is shown in Fig. 5.14 (b). The transfer function of the PI control is given by

$$H_c(s) = K_{11} + \frac{K_{12}}{s} \qquad (5.3.33)$$

Therefore, the gain of the voltage loop yields

$$T4 = \frac{K_1}{K_2} \cdot \frac{R_m}{L_{fo}} \cdot \frac{D}{1-D} \cdot \frac{1}{C_{fo}} \left(\frac{K_{11} \cdot s + K_{12}}{s^3} \right) \qquad (5.3.34)$$

and the characteristic polynomial of the system (closed loop) is
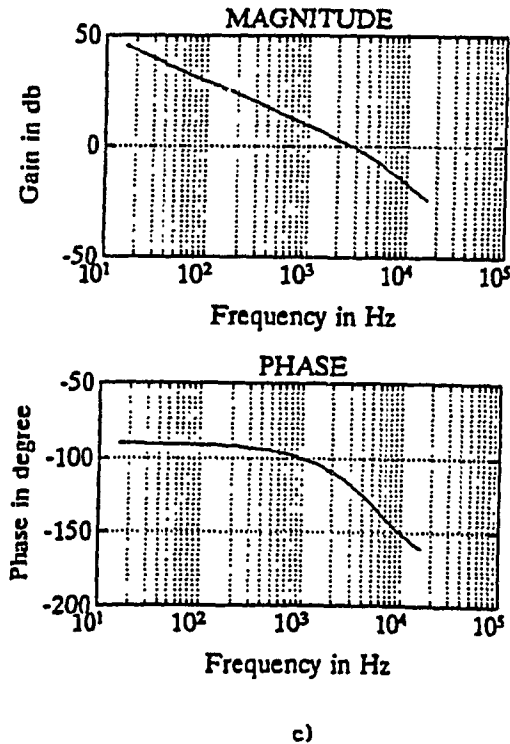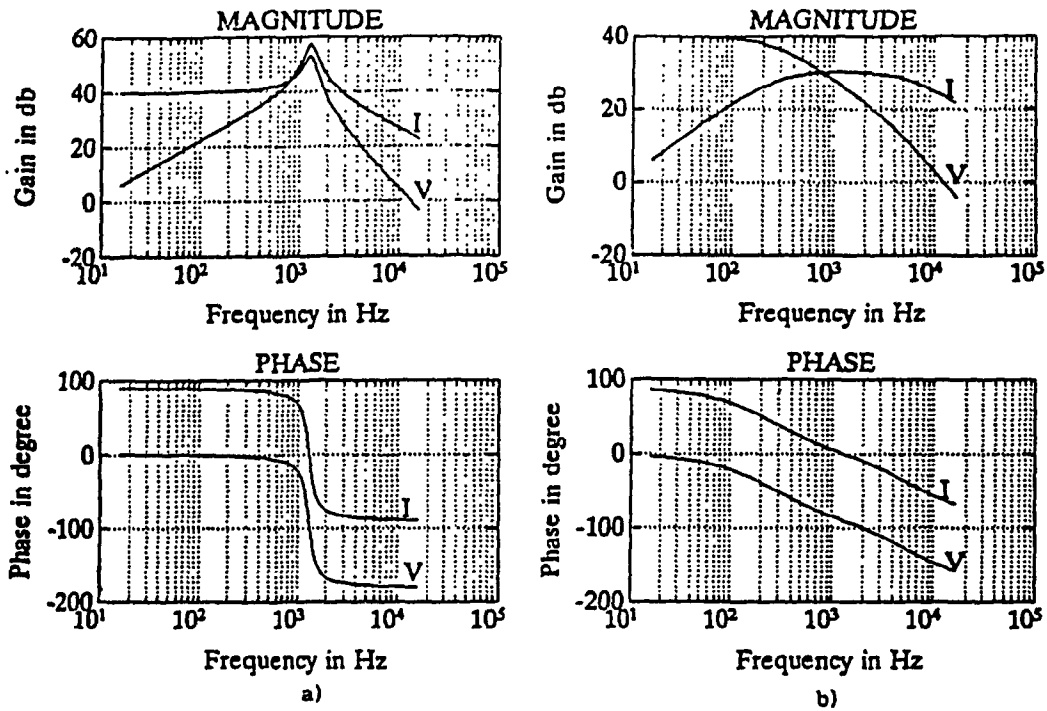
Figure 5.15 Bode Diagram of the voltage and current transfer function. a) Open loop, b) closing the current loop. c) Overall voltage transfer function with a PI controller and the propossed current loop.

$$s^3 D = s^3 + \left(\frac{1}{R_1 C_{fo}} + \frac{R_m}{L_{fo}} \cdot \frac{D}{1-D} \right) \cdot s^2 + \frac{1}{L_{fo} C_{fo}} \cdot \left(R_m K_{11} \cdot \frac{K_1}{K_2} \cdot \frac{D}{1-D} + 1 \right) \cdot s + \frac{R_m K_{12}}{L_{fo} C_{fo}}$$

$$\cdot \frac{D}{1-D} \cdot \frac{K_1}{K_2} \qquad\qquad (5.3.35)$$

One can see that the location of the poles can be further modified by the parameters of the PI control, i.e., K_{11} and K_{12}. A systematic method to calculate K_{11} and K_{12} is to use the open-loop voltage transfer function including the current loop. The following procedure is proposed.

Step 1 The output filter is designed with a high cut-off frequency but with a low-output voltage ripple, according to the load specification.

Step 2 The characteristic equations of the system including the current loop is derived (see (5.3.31)).

Step 3 The parameter R_m is calculated to have two different real poles or a damping ratio (ξ) higher than 1 (see (5.3.32)).

Step 4 The Bode diagram of the open-loop voltage transfer function including the current loop is obtained (see Fig. 5.15 (b)).

Step 5 The zero of the PI control is calculated to cancel the low frequency pole obtained in step 3.

Step 6 By using the Bode diagram obtained in step 4, the high-frequency gain of the PI control is calculated to provide a maximum crossover frequency with a phase margin higher than 60°.

C.   Using a PI Controller in the Current Loop

A PI controller in the current loop and the reconstruction of the output voltage by integrating the current signal provided by the current transformer were also examined. The PI controller in the current loop improves immunity to noise and the low-frequency gain but reduces the output current feed-forward feature.

5.3.5 Design Example

To verify the effectiveness of the proposed control technique and design procedure, a design example for the schematic circuit shown in Fig. 5.11 is presented in this section. The circuit is to be designed with a PI control in the voltage loop regarding the following specifications :

Maximum output power $P_o = 40\ kW$

Minimum input voltage $V_s = 500\ V$

Maximum output voltage $V_o = 250\ V$

Transformer turns ratio $n_t = 1$

Maximum voltage ripple $r_v = 0.0025$

Maximum current ripple $r_i = 0.23$

Steady-state duty cycle $D = 50\%$

Switching frequency $f_s = 40 kHz$

Current sensor factor $K_2 = 0.03$

Voltage sensor factor $K_1 = 0.01$

The high operating voltage and frequency suggest that isolated-gate bipolar type of transistor (IGBT) could be used as power switch.

A. Inductor Design

The output filter inductor is calculated regarding the maximum ripple and load al 50% duty cycle as follows. The load for maximum power is $R_1 = V_o^2 / P_o = 1.56W$. Hence,

$$L_{fo} = (1 - D) \cdot \frac{R_1}{f_s \cdot r_i} = 0.5 \cdot \frac{1.56}{40 \cdot 1000 \cdot 0.23} = 84.78 \; \mu H \; (i.e., 85 \; \mu H).$$

B. Capacitor Design

Similarly, the output filter capacitor yields

$$C_{fo} = \frac{r_i}{8 \cdot f_s \cdot R_1 \cdot r_v} = \frac{0.23}{8 \cdot 40 \cdot 1000 \cdot 1.56 \cdot 0.0025} = 184.3 \; \mu F \; (i.e., 200 \; \mu F)$$

with $L_{fo} = 85 \; \mu H$, $C_{fo} = 200 \; \mu F$, and $R_1 = 3$, the poles of the filter yields

Poles s1, s2 = 892.2 ± 7617.6i rad/s

Damping ratio $\xi = 0.116$

Resonant frequency $\omega_r \approx 1221$ kHz

The Bode diagrams of the open-loop current and voltage transfer functions are shown in Fig. 5.15 (a).

C.   Reference Triangular Waveform (RTW)

The maximum peak value of the triangular waveform (RTW) is calculated assuming a maximum slope in the inductor current with a drop in the output voltage equal to 0.4 V_o. Hence,

$$I_{tm} \rangle \frac{V_s - 0.4 V_o}{L_{fo} \cdot 2 \cdot f_s} K_2 = \frac{500 - 0.4 \cdot 250}{85 \cdot mH \cdot 2 \cdot 40 \cdot kHz} \cdot 0.03 = 1.76$$

Hence, a practical value must be $I_{tm} > 2$. The final value depends on the required damping ratio or poles location both defined by the gain of the current loop.

D.   Current Loop

The current loop introduces the factor R_m, which is used to modify the complex poles of the open-loop transfer function in two distinct real poles. **Table 5.3-I** summarise the real poles calculated for different R_m at 50% duty cycle.

Table 5.3-I

Poles of the Open Loop Voltage Transfer Function Including the Current Loop

Lfo=85 μh, Cfo=200 μF, RL=3 Ω

Current Loop		Damping	Real Poles
Rm	Itm	ξ	s1,s2x10^4 rdns/sec
3.00	5.00	2.41	s1=-3.53, s2=-0.17
3.75	4.00	2.98	s1=-4.45, s2=-0.13
5.00	3.00	3.94	s1=-5.95, s2=-0.10
7.50	2.00	5.86	s1=-8.92, s2=-0.07

E.   Design of the PI Controller

The PI controller in the voltage loop is designed following the procedure presented in Section 5.3.4 as follows. With the current loop and by using $I_{tm} = 5$ from **Table 5.3-I**, the real poles are

$$s1 = -1667 \text{ rad/s} \text{ or } f_{p1} = 265.30 \text{ Hz}$$
$$s2 = -35290 \text{ rad/s} \text{ or } f_{p2} = 5616.57 \text{ Hz}.$$

The Bode diagrams of the open-loop voltage transfer function closing the current loop are shown in Fig. 5.15 (b). The circuit synthesis using analogue technology is as follows. Transfer function of the PI controller is

$$H_c(s) = \frac{1 + sCR_2}{sCR_1} = \frac{R_2}{R_1} + \frac{1}{sCR_1} = K_{11} + \frac{K_{12}}{s}. \tag{5.3.36}$$

Therefore, the zero of the PI controller is

$$f_z = \frac{1}{2\pi CR_2} = \frac{K_{12}}{2\pi K_{11}} \tag{5.3.37}$$

The zero of the PI controller is located to cancel the low-frequency pole, $s1 = 265.30$ Hz. Hence, from (5.3.37) with $C = 0.1 \ \mu F$ (practical value),

$$R_2 = \frac{1}{2\pi Cf_z} = \frac{1}{2\pi \cdot 0.1\mu F \cdot 265.30} \approx 6 \ \ k\Omega$$

From (5.3.36) the high-frequency gain of the PI controller is

$$G_{hf} = \frac{R_2}{R_1} = K_{11}$$

From the Bode diagram shown in Fig. 5.15 (b) the maximum crossover frequency for a phase margin equal to 60° is $f_c \approx 3kHz$. To achieve this frequency the loop gain must be increased to 21 dB. Hence,

$$20 \log(G_{hf}) = 21 \text{ dB} \quad \text{or} \quad G_{hf} = 11.22.$$

Hence,
$$R_1 = \frac{R_2}{G_{hf}} = \frac{6k\Omega}{11.22} = 534.75\Omega$$

The resulting Bode diagrams of the open-loop voltage transfer function including the PI controller are shown in Fig. 5.15 (c).

5.3.6   Simulation and Experimental Results

A.   Simulation Results

The PSPICE software package has been used to perform transient analysis. Simulation results for a step change up and down in the load are shown in Figs. 5.16 and 5.17. The results shown in Fig. 5.16 (a) correspond to the open loop case and illustrate the oscillation in the output voltage and current due to the low damping ratio in the output filter. The action of the current loop is illustrated in Fig. 5.16 (b). It is clearly shown that when the current loop is closed the oscillation in the output current and voltage are eliminated. The performance of the PI controller is shown in Fig. 5.17. Since the PI controller has been designed to provide a high crossover frequency (above the resonant frequency of the output filter), a fast transient response is achieved. Moreover, despite a large perturbation

in the load, the system presents a good regulation. The settling time is close to 200 μs and the perturbation in the output voltage is less than 5%.

B. Experimental Results

To verify the feasibility of the proposed control method and based on the design given in Section 5.3.5 a breadboard has been implemented (Appendix A4)
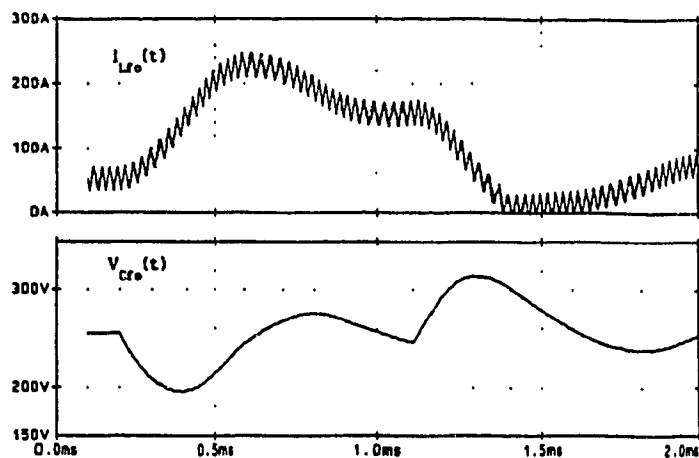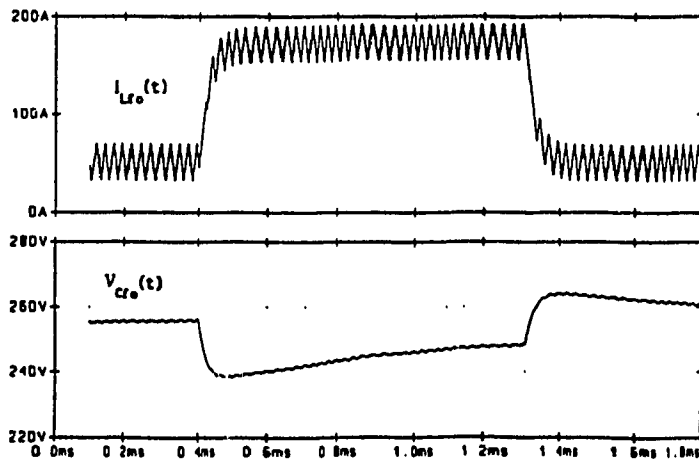
Figure 5.16 Simulated transient response. RLmax=5 Ω, Rlmin=1.5 Ω, output filter current and voltage waveforms. a) Open loop, b)closing the current loop.
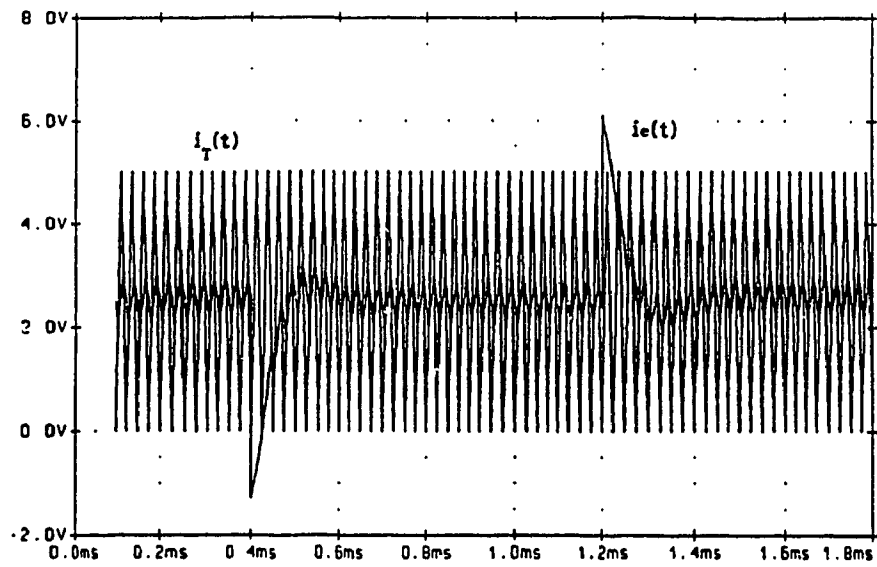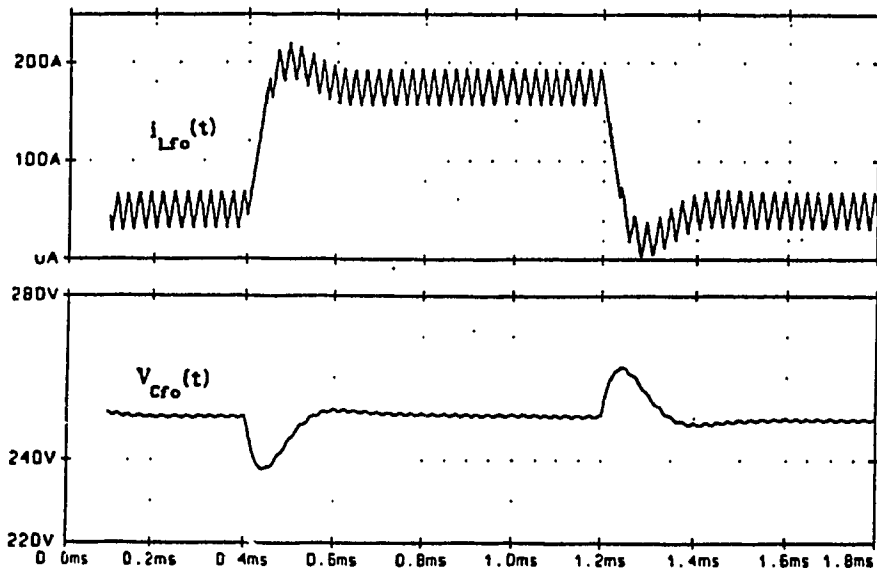
Figure 5.17 Simulated transient response with the current loop and a PI voltage controller. RLmax=5 Ω, RLmin=1.5 Ω, a) Refernce triangular waveform and error signal (ie(t)).b) Output filter current and voltage waveforms.

i.e. scale down to V_i=50 V, K_1 =0.1, K_2 =0.3). An extra switch in series with a low-value resistance load has been used to provide load transient. The results are shown in Figs. 5.18 and 5.19. These results are in close agreement with the values of the design and the simulation results shown in Figs. 5.16 and 5.17.

5.4. Summary

The control problems of the forward converter have been addressed in this Chapter. A fast voltage mode control and a new current assisted voltage control systems have been proposed and thoroughly analysed.

The first control system is proposed to improve the transient response of a high-frequency two-switch forward DC/DC converter with extended duty cycle capability. The small signal linear transfer function of this converter presents a low damping ratio and a fast voltage control loop is required to stabilise the output voltage. An all-pass constant-time delay filter has been used to model the converter at HF and a single and a dual control feedback loop have been proposed to regulate the output voltage.

It shows that the single feedback loop with a third-order controller provides excellent performance. With 8% filter inductance ripple current, 0.13% output ripple voltage, and 50% step change in the load, an overvoltage lower than 5% and a settling time less than 0.3 ms have been achieved. With the dual-loop control system the settling time is higher but the dual loop is less sensitive to control parameter variation and it minimises the capacitor overcharge in the control
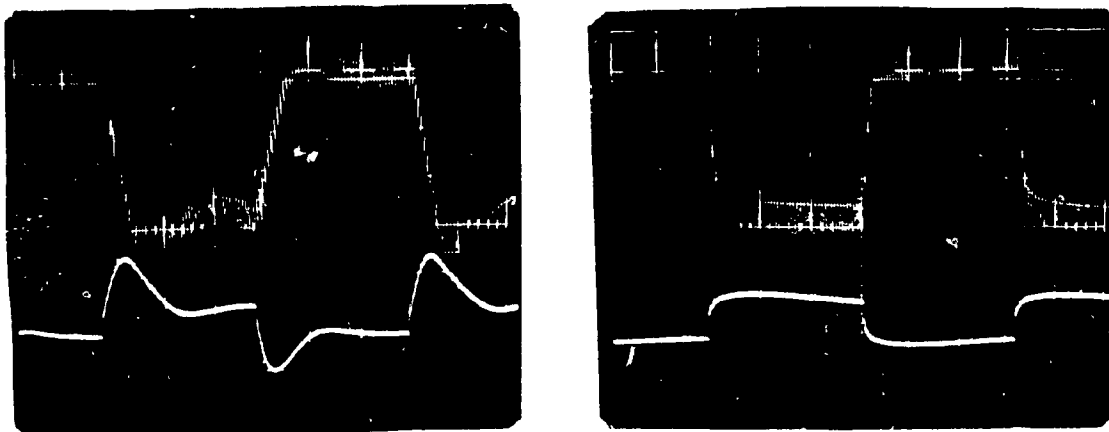
Figure 5.18 Experimental results. Output filter current and voltage waveforms. a) Open loop, b) Closing the current loop, Vi=50 V, D=50%, RLmax=5 Ω, RLmin=1.5 Ω, Lfo=90 μH, Cfo=200 μF, K1=0.1, K2=0.3, Fs=40 kHz. Top:iLfo, Vertical: 5Amp/Div; bottom:VCfo, Vertical: 1V/Div AC, horizontal:0.2 ms/Div.
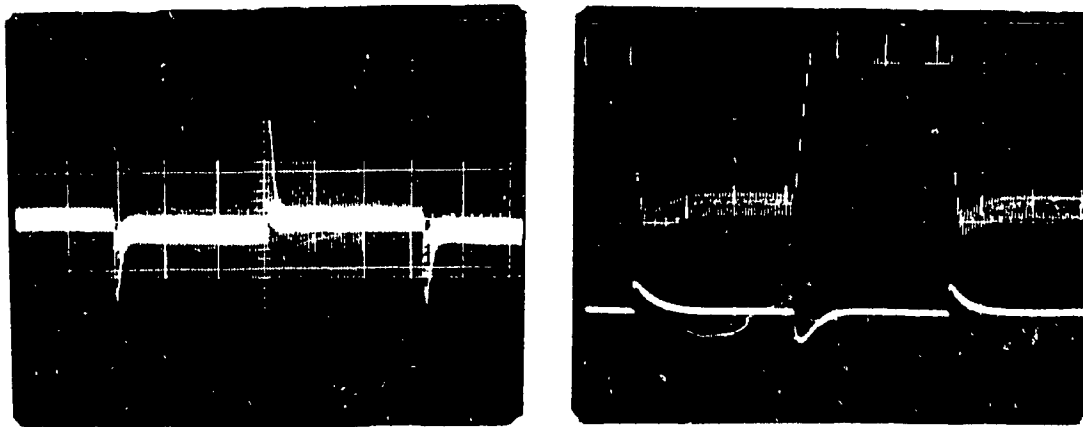
Figure 5.19 Experimental results using the inner current loop and PI controller in the voltage loop. a) Triangular waveform (RTW) and error signal, Vertical: 2 V/Div, b) Output filter current and voltage waveforms. a) Open loop, b) Closing the current loop, Vi=50 V, D=50%, RLmax=5 Ω, RLmin=1.5 Ω, Lfo=90 μH, Cfo=200 μF, K1=0.1, K2=0.3, fs=40 kHz, C=0.1 μF, R1=535 Ω. Top:iLfo, Vertical: 5Amp/Div; bottom:VCfo, Vertical: 1V/Div AC, horizontal: 0.2 ms/Div.

circuit under large transient operation condition. It has been shown that the dual-loop control system eliminates the zero of the control-output transfer function of the converter. It is designed in the same way that a single-loop control system by using an equivalent single-input/single-output voltage control transfer function like a PID or third-order controller.

The second control system is new in a way that an AC current signal is directly applied to the comparator of the PWM circuit. By sensing the current of the output filter capacitor, a synchronous ripple-current forward loop has been implemented in series with a voltage loop. The current loop modified the damping ratio of the transfer function. In fact, it was found that the voltage loop has two real poles, one at low frequency and other at high frequency. Tne low-frequency pole is a dominant pole and it can be removed with a standard PI controller. This controller can be designed to provide a crossover frequency above the resonant frequency of the output filter. The power converter presents a fast transient response and low sensitivity to load perturbation. This novel control technique is simple and offers increased reliability for high-power applications. Simulation and experimental results confirm the theory.

CHAPTER 6: CONCLUSIONS

In this thesis, several new single-ended ZVS PWM forward converters with low component count and improved performance have been studied. They are intended to be used as DC/DC modules in switch-mode power supplies in the range of 1 to 10 kW and for low voltage applications (i.e. 25-48 V). The thesis work provides a thorough understanding of the analysis procedure, design method and control of the proposed topologies. Lossless and active snubber circuits to reduce the switching losses and stress of these converters with PWM control at ultrasonic switching frequency (20 to 40 kHz) have been proposed and thoroughly analyzed.

The main contributions of the thesis can be summarized as follows:

1) New single-ended forward topologies were proposed. The research work included single-switch, two-switch, three-switch and six-switch power circuit structures.

2) Single-switch single-ended forward topologies with optimized switching losses were studied. All of them used a low cost HF transformer (ferrite core). As compared with the conventional single-switch forward converter, non resetting winding and diode were required to reset the core during the turn-off. Experimental validation was done by using darlington BJT and IGBT power switches in a 1 kW prototype unit. First, a lossless LC snubber

circuit was designed and thoroughly investigated to reduce switching losses during the turn-off, limit switch voltage stresses and avoid transformer saturation. Secondly, an active snubber circuit implemented by using a complementary auxiliary switch, in parallel with the main switch, was studied and tested. It was shown that this circuit provides ZVS during the turn-on and the turn-off, minimizes the DC magnetizing current in the HF transformer, and eliminates the energy stored in the parasitic inductance of the DC input Bus.

3) Single-ended forward topologies with two switches were investigated. They were designed to be applied in the range of 2 to 5 kW by using the darlington BJT or IGBT power switches available today. The first configuration used two complementary switches in series. The circuit was proposed as a better alternative to the conventional two-switches forward converter. It is found that the two feedback diodes were not required to reset the HF transformer and the energy stored in the parasitic inductance of the DC bus was controlled to avoid overvoltage spikes across the power switches at high switching frequency. It was also shown that in the proposed topology, a conventional DRC snubber can be designed and used to reset the HF transformer and enhance zero-voltage switching during the turn off.

The second topology analyzed used two switches in a hybrid bridge configuration with only one small capacitor to reduce switching losses in both the switches. An experimental prototype was implemented for evaluation by using IGBT. The performance of this novel converter was studied by using a half-bridge and a full-bridge rectifier with discontinuous output current. It was shown that, under this operating condition, this converter can be operated as a buck or boost converter. An interesting mode of operation was discovered in which a free-ripple current is obtained in the output filter reactor during the turn-on time (current square pulse).

4) The proposed snubber circuits for the single-switch and two-switch topologies used only one small capacitor to provide zero-voltages switching during turn-off. It was found that, due to the leakage and magnetizing inductances of the HF transformer, several resonant *topological modes* can be generated during a switching period. It was shown that, by changing the size of the snubber capacitor, the circuit parameters and the operating conditions, different sequences of these *topological modes* or *modes of operation* were obtained. The design procedure was sensitive to circuit parameters and analytical and computer solution for the steady states voltage/current waveforms during a switching period were necessary.

The identification of the operating modes and the steady state solution for the voltage/current equations during a switching period was essential to optimize performance and reduce the voltage stress. A closed form solution for the voltage/current waveforms including all the modes of operation was practically impossible and numerical algorithms were necessary. A Broyden algorithm was successfully applied to achieve the desired solutions

Non-resonant, and quasi-resonant modes of operation were evaluated. Lower switching losses but higher voltage stresses were obtained with the quasi-resonant mode. An efficiency higher than 90% was achieved (5%-7% improvement respect to the DRC snubber in a conventional forward topology).

5) A three-leg core connected with a three-phase half-bridge or a full-bridge rectifier was proposed to implement multiple-switch single-ended forward converters for output power higher than 5 kW. Three topologies were analyzed and compared; two with six switches and one with three switches. Each switch must be operated with 120° phase shift, and the maximum ideal duty cycle for each switch cannot be larger than 33%. As compared with the typical parallel two-switch forward configuration, the reduction in

magnetic material can be 25% for the transformer, and the output filter size is reduced three times.

For validation proposes, a transformer model was derived and used in the PSPICE software package. It is discovered that the utilization of the HF transformer core and windings in the proposed six-switch forward topology is improved when a full-bridge rectifier was used on the secondary side. This new converter is practically the dual of the typical three-phase full-bridge voltage inverter.

6) The control problem of a forward converter was studied. A fast voltage mode control and a new current assisted voltage control systems were proposed and thoroughly analyzed.

A single and dual control feedback loop were proposed to improve the transient response of a high-frequency two-switch forward DC/DC converter with extended duty cycle capability. An all-pass constant-time delay filter was used to model the converter at HF. The dual loop was less sensitive to control parameter variation and it minimized the capacitor overcharge of the controller under large transient operation condition. It was shown that the dual-loop controller eliminates the zero of the control-output transfer function of the converter and can be designed in the same way that a single-loop control system by using an equivalent single-

input/single-output voltage control transfer function like a PID or third-order controller.

The second control system analyzed used a fast internal current loop that directly applies an AC current signal to the comparator of the PWM . It was discovered that this fast current loop modifies the damping ratio of the second order transfer function of the converter. As a result, the voltage loop transfer function has two real poles, one at low frequency and other at high frequency. The low-frequency pole is a dominant pole and it was easily removed with a standard PI controller. The gain of this controller was designed to provide a crossover frequency above the resonant frequency of the output filter. The power converter presented a fast transient response and low sensitivity to load perturbation. This novel control technique is simple and offers increased reliability for high-power applications.

Future Work

This research can be extended as follows

1)   The proposed ideas of using a quasi-resonant mode only during the switching transition to reduce switching losses and limit voltage stress for the PWM converter can be extended to other topologies such as the boost converter

2) To investigate the operation of the proposed topologies at higher frequency by using MOSFET.

3) During the research for the proposed multi-switch single-ended forward converter analyzed in Chapter 4, three-leg core was non available to implement an experimental prototype. Further work is required to verify the concept experimentally and to know the effect the leakage inductances of the transformer. The LC snubber can also be applied to these topologies.

The application of this type of ferrite core is seen to be very attractive for designing other types of converters, such as three-phase high frequency AC/DC PWM switch mode rectifiers.

4) To further reduce the size and cost, other magnetic structures can be designed and applied. For example the integration of the output filter with the HF transformer, or a coaxial winding magnetic structure for the HF transformer can be further investigated.

5) To apply the current mode control and analyze the transformer flux balance under transient condition for the proposed multi-switch single-ended forward topologies.

REFERENCES

[1] B. Carsten, "High power smps require intrinsic reliability," in *Proc. Powercon 10,* Power Concepts. Inc., pp. 118-133, 1981.

[2] K. Nishimura, K. Kobayashi, H. Tanaka, Y. Arai, H. Shimizu, and T. Nikura, "High frequency high-power converter," in *Conf. Rec. IEEE Power Electron. Special. Conf.,* 1988, pp. 180-187.

[3] Rudolf P. Severns and Gordon E. Bloom, *Modern DC-to-DC Switchmode Power Converters Circuits,* Van Nostrand Reinhold Electrical/Computer Science and Engineering Series, 1985.

[4] K. Sum, *Switch Mode Power Conversion,* Marcel Dekker Inc., 1984.

[5] K. Sum, "Advances in power sources," in *Power Convertion and Intelligent Motion,* pp. 13-24, May 1987.

[6] P. Chetty, "Modelling and design of switching regulators," *IEEE Transactions on Aerospace and Electric Systems,* vol. AES-18, no. 3, May 1982, pp. 333-343.

[7] R. Middlebrook and S. Cuk, *Advances in Switched-Mode Power Conversion,* Teslaco, vol I-II, Pasadena California, 1983.

[8] S. Cuk and R. Middlebrook, *Advances in Switched-Mode Power Conversion,* Teslaco, vol. III, Pasadena California, 1983.

[9] T. Wilson Jr., E. Whelan, Jr., R. Rodriguez, and J. Dishman, "DC-to-DC

converter power train optimization for maximum efficiency," *IEEE Transactions on Aerospace and Electronic Systems*, vol. AES-19, no. 3, May 1983, pp. 413-421.

[10] A. Weinberg and J. Schreuders, "A high-power high-voltage dc-dc converter for space applications," *IEEE Transactions on Power Electronics*, vol. PE-1, no. 3 July 1986, pp. 148-160.

[11] R. Wu, S. Dewan, and G. Slemon, "A PWM ac to dc converter with fixed switching frequency," in *Proc. IEEE Ind. Appl. Soc.*, pp. 234-256, 1988.

[12] R. Tymerski and V. Vorperian, "Generation, classification and analysis of switched-mode dc-to-dc converters by the use of converters cells," in *Proc. Intelec Conf.*, pp. 181-195, 1986.

[13] E. Tatakis, "An analytical solution for predicting switching performances of a forward converter with insulation transformer," in *Conf. Rec. IEEE Power Elec. Special. Conf.*, pp. 666-675, 1986.

[14] M. Domb, R. Redl, and N. Sokal, "Nondissipative turn-off snubber alleviates switching power dissipation, second breakdown stress and vce overshoot: analysis, design procedure and experimental verification," in *Conf. Rec. IEEE Power Elec. Special. Conf.*, pp. 445-454, 1982.

[15] P. Vinciarelli, "Optimal resetting of the transformer's core in single ended forward converters," U.S. patent No. 4441146, April 3, 1984.

[16] P. Vinciarelli, "Forward converter switching at zero current," U.S. Patent No. 4415959, Nov. 15, 1983.

[17] T. Zeng, D. Chen, and F. C. Lee, "Variations of quasi-resonant dc-dc converter topologies," in *Conf. Rec. IEEE Power Elec. Special. Conf.*, pp. 381-392, 1986.

[18] L. Casey, M. Schlecht, "A high frequency, low volume, point-of-load power supply for distributed power systems," in *Conf. Rec. IEEE Power Elec. Special. Conf.*, pp. 439-450, 1987.

[19] H. Venable, "The K factor: a new mathematical tool for stability analysis and synthesis," in *Proc. of Powercon 10*, Power Concepts Inc., pp. 1-10, 1983.

[20] A. Pietkiewicz and D. Tollik, "Application of the unified topological modelling method to switching converters in current-programmed mode," in *Proc. Intelec*, pp. 248-253, 1987.

[21] D. Gouttenegre, B. Velaerts, and T. Michaux, "Modelling and analysis of dc-dc converters control by power equalization," in *Conf. Rec. IEEE Power Elec. Special. Conf.*, pp. 960-965, 1988.

[22] A. Ferraro, "An overview of low-loss snubber technology for transistor converters," in *Conf. Rec. IEEE Power Elec. Special. Conf.*, pp. 466-477, 1982.

[23] M. Domb, R. Redl, and N. Sokal, "Nondissipative turn-off snubber in a

forward converter: analysis, design procedure, and experimental verification," in *Proc. Powercon 10,* Power Concepts. Inc., pp. 54-68, 1985.

[24] F. Zach, K. Kaiser, J. Kolar and F. Haselsteiner, "New lossless turn-on and turn-off (snubber) networks for inverters including circuits for blocking voltage limitation," in *Conf. Rec. IEEE Power Elec. Special. Conf .,* pp. 34-41, 1984.

[25] R. Burden, J. Faires, and A. Reynolds, *Numerical Analysis Second Edition,* pp. 458, 1981.

[26] B. Belwinder, "Bed converter," in *Conf. Rec. IEEE Appl. Power Elec. Conf .,* pp. 13-19, 1986.

[27] W. McMurray, "Selection of snubbers and clamps to optimize the design of transistor switching converters," *IEEE Transactions on Industry Applications,* vol. IA-16, no. 4, July/August 1980, pp. 513-523.

[28] J. Park and T. Zaloum, "A dual mode forward/flyback converter," in *Conf. Rec. IEEE Power Elec. Special. Conf .,* pp. 3-13, 1982.

[29] C. Burgio, P. Cammelli, P. Maranesi, and V. Varoli, "The d.c. loop-gain of pwm voltage regulators," in *Conf. Rec. IEEE Power Elec. Special. Conf .,* pp. 541-549, 1986.

[30] T. Tanataka, T. Ninomiya, and K. Harada, "Design of a nondissipative turn-off snubber in a forward converter," in *Conf. Rec. IEEE Power Elec. Special.*

Conf., pp. 789-796, 1988.

[31] J. Ferrieux, E. Toutain, and H. Le-Huy, "A multifunction dc-dc converter as versatil power conditioner," *IEEE Transactions on Industry Applications*, vol. IA-22, no. 6, Nov./Dec. 1986, pp. 1037-1043.

[32] M. Jovanovic', K. Liu, R. Oruganti, and F. C. Y. Lee "State-plane analysis of quasi-resonant converters," *IEEE Transactions on Power Electronics*, vol. PE-2, no. 1, Jan 1987, pp. 36-43.

[33] J. Rockot, "Losses in high-power bipolar transistors," *IEEE Transactions on Power Electronics*, vol. PE-2, no. 1, Jan 1987, pp. 72-80.

[34] G. Verghese, M. Elbuluk, and J. Kassakian, "A general approach to sampled-data modelling for power electronic circuit," *IEEE Transactions on Power Electronics*, vol. PE-1, no. 2, April 1986, pp. 76-89.

[35] P. Ziogas, "Synthesis of optimum gain functions for static power converters," *IEEE Transactions on Industry Applications*, vol. IA-19, no. 3, May/June 1983.

[36] J. Jalade, S. Senanayake, "Reversible power cell contributes to efficient light weight inverter," in *Conf. Rec. IEEE Power Elec. Special. Conf.*, pp. 375-380, 1986.

[37] R. Steigerwald, "High-Frequency resonant transistor dc-dc converters," *IEEE Transactions on Industrial Electronics*, vol. IE-31, no. 2, May 1984 pp. 181-

191.

[38] A. Capel, D. O'Sullivan, A. Weinberg, J. Marpinard, G. Salut, M. Valentin, N. Limbourg, and J. Rym, "A bi-directional high power power cell using large signal feedback control with maximum current conduction control for space applications," in *Conf. Rec. IEEE Power Elec. Special. Conf*., pp. 684-695, 1986.

[39] B. Lau, "Small-Signal frequency response theory for ideal dc-to-dc converter systems," Ph.D. Thesis, California Institute of Technology, 1987.

[40] V. Bello, "Computer-Modelling the pulse with modulated (pwm) inverter," in *Proc. Powercon 7,* Power Concepts. Inc., March 24-27, 1980.

[41] V. Bello, "Using the SPICE II cad package to simulate and design the current mode converter," in *Proc. Powercon 7,* Power Concepts. Inc., 1984.

[42] C. Deisch, "Simple switching control method changes power converter into a current source", in *Conf. Rec. IEEE Power Elec. Special. Conf*., pp. 300-306, 1978.

[43] R. Redl and N. Sokal, "Near-optimum dynamic regulation of dc-dc converters using feed-forward of output current and input voltage with current-mode control", *IEEE Transactions on Power Electron.*, vol. PE-1, no. 3, pp. 181-192, July 1986.

[44] G. Schoneman and D. Mitchell, "Output impedance considerations for

switching regulators with current-injected control," *IEEE Transactions on Power Electron.*, vol. 4, no. 1, pp. 25-35. Jan 1989.

[45] R. Ridley, B. Cho, and F. C. Y. Lee, "Analysis and interpretation of loop gains of multiloop-controlled switching regulators", *IEEE Transactions on Power Electron.*, vol. PE-3, no. 4, pp. 489-498, Oct. 1988.

[46] R. Middlebrook, "Modeling current-programmed buck and boost regulators", *IEEE Transactions on Power Electron.* vol. 4, no. 1, pp. 35-52, Jan. 1989.

[47] G. Schoneman and D. Mitchell, "Closed-loop performance comparisons of switching regulators with current-injected control", in *Conf. Rec. IEEE Power Elec. Special. Conf.*, pp. 3-12, 1986.

[48] G. Joos, P. Ziogas, and D. Vincenti, "A model reference adaptive PWM technique", in *Conf. Rec. IEEE Power Elec. Special. Conf.*, pp. 485- 494, 1989.

[49] B. Lau, and R. Middlebrook, "Small-signal frequency response theory for piecewise-constant two-switched-network dc to dc converter systems", in *Conf. Rec. IEEE Power Elec. Special. Conf.*, pp. 186-200, 1986.

[50] D. Johnson and V. Jayakumar, *Operational Amplifier Circuits, Design and Applications*, Englewood Cliffs, NJ: Prentice-Hall, 1982, pp. 149.

[51] L. Salazar and P. Ziogas, "A single ended SMR converter topology with optimized switching characteristics," *IEEE Transactions on Power*

Electronics, vol. 4, no. 1, Jan 1989, pp. 53-63.

[52] L. Salazar and P. Ziogas, "A high frequency forward dc/dc converter topology with transformer flux balancing capability," *IEEE Transactions on Industrial Electronics*, vol. 37, no. 5, October 1990, pp. 409-418.

[53] L. Salazar and P. Ziogas, "A high frequency forward dc/dc converter topology with transformer flux balancing capability," in *Proc. IEEE Ind. Appl. Soc.*, pp. 430-340, 1988.

[54] L. Salazar and P. Ziogas, "A high frequency two-switches forward converter with optimized performance," *IEEE Transactions on Industrial Electronics*, vol. 37, no. 6, December 1990, pp. 496-505.

[55] L. Salazar and P. Ziogas, "Design-Oriented analysis of two types of three phase high-frequency forward SMR topologies," in *Proc. IEEE Applied Power Elec. Conf.*, pp. 312-320, 1990.

[56] L. Salazar, P. Ziogas, and D. Vincenti, "Simple model for spice assist power electronics circuit simulation on PC's," in *Proc. IEEE Ind. Appl. Soc.*, pp. 1063-1068, 1988.

[57] L. Salazar and G. Joós, "Pspice simulation of three-phase inverter by means of the switching function", *IEEE Transactions on Power Electronics*, vol. 9, no. 1, Jan 1994, pp. 35-42.

[58] L. Salazar and P. Ziogas, "Design and evaluation of two types of controlller

for a two-switches forward converter with extended duty cycle capability," *IEEE Transactions on Industrial Electronics*, April 1992, vol. 39, no. 2, pp. 128-140.

[59] L. Salazar, G. Joós and P. Ziogas, "A low loss soft switching converter PWM CSI," in *Conf. Rec. IEEE Power Elec. Special. Conf.*, pp. 1098-1104, 1992.

[60] L. Salazar and P. Ziogas, "A novel current assisted output voltage control technique for switch-mode-rectifier converters," *IEEE Transactions on Power Electronics*, July 1992, vol. 7, no. 3, pp. 444-452.

[61] L. Salazar, G. Joós, and P. Ziogas, "A novel zero voltage switching pwm dc/dc converter for medium power applications," in *Proc. IEEE Applied Power Elec. Conf.*, pp. 3-7, 1991.

[62] L. Salazar, P. Ziogas, and G. Joós "On the minimization of the switching losses in a boost converter," in *Proc. IEEE Applied Power Elec. Conf.*, pp. 703-708, 1992.

APPENDIX A1

The Broyden Algorithm

To approximate the solution of the nonlinear system $F(x)=0$ given an initial approximation x:

INPUT number n of equations and unknowns;

initial approximation $x = (x_1, ..., x_n)^t$;

tolerance TOL; maximum number of iterations N.

OUTPUT approximate solution $x = (x_1, ..., x_n)^t$ or a message that the number of iterations was exceeded.

Step 1 Set $A_0 = J(x)$ where $J(x)_{i,j} = \dfrac{\partial f_i(x)}{\partial x_j}$ for $1 \le i, j \le n$;

        $v = F(x)$.   (*Note:* $v = F(x^{(0)})$.)

Step 2 Set $A = A_0^{-1}$

Step 3 Set $k = 1$

        $s = -Av$;   (*Note:* $s = s_1$.)

        $x = x + s$.   (Note: $x = x(^1)$.)

Step 4 While $(k \le N)$ do Steps 5-13.

Step 5 Set $w = v$;   (*Save* v.)

           $v = F(x)$;   (*Note:* $v = F(x^{(k)})$.)

           $y = v - w$.   (*Note:* $y = y_k$.)

Step 6 Set $z = -Ay$.   (*Note:* $z = -A^{-1}_{k-1} y_k$.)

Step 7 Set $p = -s^t z$.   (*Note:* $p = s^t_k A^{-1}_{k-1} y_k$.)

Step 8 Set $C = pI + (s + z)s^t$.   (*Note:* $C = s^t_k A^{-1}_{k-1} y_k I + (s_k + A^{-1}_{k-1} y_k) s^t_k$.)

Step 9   Set $A = (1/p)CA$ (*Note*: $A = A^{-1}_k$.)

Step 10   Set $s = -A\mathbf{v}$.   (*Note*: $\mathbf{s} = -A^{-1}_k F(\mathbf{x}^{(k)})$.)

Step 11   Set $\mathbf{x} = \mathbf{x} + \mathbf{s}$.   (*Note*: $\mathbf{x} = \mathbf{x}^{(k+1)}$.)

Step 12   If $\|\mathbf{s}\| < TOL$ then   OUTPUT $(\mathbf{x})$;

                (Procedure completed successfully.)

                STOP.

Step 13   Set $k = k + 1$.

Step 14   OUTPUT ('Maximum number of iterations exceeded');

                STOP

APPENDIX A2

Normalized Voltage/Current Solutions

In this APPENDIX the normalized equations solutions to analize the Topology II presented in Chapter 3 are outlined. Section I presents the voltage/current solutions when a half-bridge rectifier is used in the secondary side of the HF isolation transformer. Similarly, Section II presents the voltage/current solutions when a full-bridge rectifier is used.

I. The Two-Switch Converter with a Half-Bridge Rectifier

Mode 1: d=[0,d1]

$$Vs(d) = (Vs(0)-1+A1Vo)\cos(2\pi F1d) + 1-A1Vo \tag{A-1}$$

$$I1(d)Z1 = -(Vs(0)-1+A1Vo)\sin(2\pi F1d) \tag{A-2}$$

$$I2(d)Zs1 = -A1I1(d)Zs1 + Vo(2\pi d) \tag{A-3}$$

$$ILm(d)Zs1 = B1I1(d)Zs1 + Vo((2\pi d) \tag{A-4}$$

$$IQ1(d)=IQ2(d)=ICr(d)=I1(d), \quad ILr(d)=I2(d), \quad VCr(d)=Vs(d)$$

Boundary mode conditions : Vs(d1)=0, hence

$$(Vs(0)-1+A1Vo)\cos(2\pi F1d1) + 1-A1Vo=0 \tag{A-5}$$

Mode 2: d=[d1,d2]

$$Vs(d)=0$$

$$I1(d)Z1 = (1-A1Vo)(2\pi F1(d-d1)) + I1(d1)Z1 \tag{A-6}$$

$$I2(d)Z1 = -A1(1-Ke3vo)(2\pi F1(d-d1)) + I2(d1)Z1 \tag{A-7}$$

$$ILm(d)Z1=B1(1+CVo)(2\pi F1(d-d1)) + ILm(d1)Z1 \tag{A-8}$$

$$IQ1(d)=IQ2(d)=I1(d)/2, ILr(d)=-I2(d), ICr(d)=0, VCr(d)=Vs(d)$$

Boundary mode condition: $d2=don$ (A-9)

Mode 3: $d=[d2, d3]$

$$Vs(d)=I1(d2)Z1\sin(2\pi F1(d-d2)) + (A1Vo-1)\cos(2\pi F1(d-d2))+1-A1Vo \tag{A-10}$$

$$I1(d)Z1=I1(d2)Z1\cos(2\pi F1(d-d2)) - (A1Vo-1)\sin(2\pi F1(d-d2)) \tag{A-11}$$

$$I2(d)Zs1=A1(I1(d2)-I1(d))Zs1 + Vo(2\pi F1(d-d2)) + I2(d2)Zs1 \tag{A-12}$$

$$ILm(d)Zs1=B1(I1(I1(d)-I1(d2))Zs1 + Vo(2\pi F1(d-d2)) + ILm(d2)Zs1 \tag{A-13}$$

$$VQ1(d)=VQ2(d)=-Vcr(d)=Vs(d), ID1(d)=ID2(d)=-Icr(d)=I1(d), ILr(d)=I2(d)$$

Boundary mode condition : $[Lm\ L2] \cdot \begin{bmatrix} \dot{Lm} & \dot{L2} \end{bmatrix}^T$ hence

$$\frac{Ke1Vo}{KrA2} = Vs(d3)-(1-A1Vo) \tag{A-14}$$

Mode 4: $d=[d3, d4]$

$$Vs(d)=I1(d3)Z2\sin(2\pi Fs(d-d3)) + (Vs(d3)-1\cos(2\pi Fs(d-d3)) + 1 \tag{A-15}$$

$$I1(d)Z2=I1(d3)Z2\cos(2\pi F2(d-d3)) - (Vs(d3)-1)\sin(2\pi F1(d-d3)) \tag{A-18}$$

$$VQ1(d)=VQ2(d)=-VCr(d)=Vs(d), ID1(d)=ID2(d)=-ICr(d)=I1(d)$$

Boundary mode condition : $I2(d4) = 0$, hence

$$A2I1(d3) - I2(d3)=A2I1(d4) \tag{A-19}$$

Mode 5: $d=[d3,d5]$

$$ILr(d)Zr=-Vo(2\pi(d-d3) + ILr(d3)Zr \tag{A-20}$$

7-13

ILr(d3)=-I2(d3)

Boundary mode condition : ILr(d5) = 0 hence

$$ILr(d3)Zr=Vo(2\pi(d5-d3)) \tag{A-21}$$

Mode 6: d=[d4, d6]

$$Vs(d)=I1(d4)Z3\sin(2\pi F3(d-d4)) + (Vs(d4)-1)\cos(2\pi F3(d-d4)) + 1 \tag{A-22}$$

$$I1(d)Z3=I1(d4)Z3\cos(2\pi F3(d-d4)) - (Vs(d4)-1)\sin(2\pi F3(d-d4)) \tag{A-23}$$

$$VQ1(d)=VQ2(d)=-VCr(d)=Vs(d), \quad ID1(d)=ID2(d)=-ICr(d)=ILm(d)=I1(d)$$

Boundary mode condition : I1(**d6**)=0 hence

$$I1(d4)Z3\cos(2\pi F3(d6-d4)) - (Vs(d4)-1)\sin(2\pi F3(d6-d4))=0 \tag{A-24}$$

II.   The Two-Switch Forward Converter with a Full-Bridge Rectifier

The following equations include the sequence of modes M1,M2,M3,M4,

M5 and M9 shown in Fig. 3.14 with the conditions that Vs(d4)=(Vo+1) and

I1(d4)=0 at a maximum duty cycle (d2) and load current

Mode 1: d=[0, d1]

From (A-1) regarding $2\pi F1d1 \approx \dfrac{\pi}{2}$ hence

$$d1 \approx \frac{1}{4F1} \tag{A-25}$$

$$I1(d1)Z1 \approx -Vs(0)=Vs(d4)=(Vo+1) \tag{A-26}$$

Mode 2: d=[d1, d2]

From (A-6)

$$[I1(d2)-I1(d1)]Z1=(1-A1Vo)(2\pi F1(d2-d1)) \tag{A-27}$$

Mode 3: d=[d2, d3]

From (A-10) and (A-11) assuming d3-d2 small

$$Vs(d3)\approx I1(d2)Z12\pi F1(d3-d2) \tag{A-28}$$

$$[I1(d3)-I1(d2)]Z1=(1-A1Vo)(2\pi F1(d3-d2)) \tag{A-29}$$

From (A-14)

$$Vs(d3) = (1 - A1Vo) + \frac{Ke1Vo}{KrA2} \tag{A-29}$$

Mode 4 and 5: d=[d3, d4], d=[d3, d5]

From (A-15) and (A-16) with I1(d4)=0

$$[I1(d3)Z2]^2 = [Vs(d4)-1]^2 - [Vs(d3)-1]^2 \tag{A-30}$$

Regarding (A-20)

$$ILr(d5) = -\frac{2\pi Vo}{Zr}(d5-d3) + ILr(d3) = ILm(d5) \tag{A-31}$$

But: ILr(d3)=I2(d3)=I1(d3)-ILm(d3) and ILm(d5)≈ILm(d3)≈ILm(d2), hence

$$[I1(d3)-2ILm(d2)]Zr=(d5-d3)2\pi Vo \tag{A-32}$$

Mode 9: D=[D5, 1]

$$ILr(1) = I2(1) = ILm(1) = -(1-d5)\frac{2\pi Vo}{Zs1} + ILr(d5) = 0 \tag{A-33}$$

But ILr(d5)=ILm(d2) hence

$$(1-d5)\frac{2\pi Vo}{Zs1} = ILm(d2) \tag{A-34}$$

APPENDIX A3

Transformer Model

The implementation of a single ended forward converter coupled on a three-phat core can be accomplished in a variety of ways. However, finding topologies that do not lead to transformer saturation is an important and difficult task, mainly due to the number of paths available to the magnetizing current through the external diodes and switches. In order to assist the analysis, and verify the operation of the proposed topologies, linear transformer models with mutual inductances are discussed in this APPENDIX.

A. Analytical Model

In a linear air-gap symmetrical core structure the n voltages (vector V) and the n currents (vector I) of the respective coils are related by a set of first order differential equations. The matrix form of this set in the Laplace domain in an interval τ is as follows :

$$V_\tau(s) = [R + s \cdot L] \cdot I_\tau(s) - L \cdot Io_\tau \qquad (A.1)$$

where Io is a vector with the n initial current conditions, R is a n x n diagonal resistance matrix whose elements are the equivalent resistances of the n coils, and L is a n x n symmetrical inductance matrix whose elements are the self inductances and the mutual inductances. Assuming that the elements in R are very

small and the elements in V_τ are constants, the respective vector solution of (A.1) in the interval τ yields

$$I_t(t) = Io_t + L^{-1} \cdot V_t(t) \cdot t \qquad t_t \langle t \le t_{t+1} \qquad (A.2)$$

Also, the flux linking each coil is given by

$$\lambda_\tau(t) = L \cdot I_\tau(t) \qquad (A.3)$$

With the assumption of no losses, (A.2) and (A.3) show that the current and flux solutions are linear combinations of ramp functions. The slope of each ramp depends on the self inductance, the mutual inductance, and the constant voltage applied to each coil. It should be noted that the current and flux solutions depend on the initial condition Io. One important design problem associated to a forward DC/DC converter is to keep the matrix Io constant to avoid saturation.

B. *Transformer Inductance and Effective Turns-ratio*

The general mutual inductance term between coils i and j and their respective turns ratios are obtained by using the following expressions

$$Lij = kij \cdot \sqrt{LiLj} \qquad (A.4)$$

$$Nij \approx \sqrt{\frac{Li}{Lj}} \qquad (A.5)$$

where kij is the magnetic coupling factor between coil i and j. For clarity, the various transformer inductances are defined below

Lp   Primary-self inductance

Lpd Primary mutual inductances between coils in different limb.

L_{pc} Primary mutual inductances between coils in the same limb.

L_{ps} Primary-secondary mutual inductances between coils in the same   limb.

L_{cw} Primary-secondary mutual inductances between coils in different limb.

L_s Secondary-self inductance

L_{sd} Secondary mutual inductances between coils in different limb.

L_{sc} Secondary mutual inductances between coils in the same limb.

The effective turns ratio of the transformer is defined as

$$N_e = N_{ps} \cdot K_c \qquad (A.6)$$

where N_{ps} can be evaluated by using (4.5) and K_c is a constant that accounts for the different ways that the coils are connected. For example, if coils b' and c' are connected in parallel on the secondary side and both are in series with coils a', K_c = 3/2.

C.   *The Single-path Core Model with Two and Three-coil*

These two models are presented here as a reference. For a single-path core with n coils, all the elements of the inductance matrix **L** are defined positive. The inductance matrixes with two and three coils are

$$
\mathbf{L} = \begin{matrix} & a & b \\ & \begin{bmatrix} L_p & L_{ps} \\ L_{ps} & L_s \end{bmatrix} & \begin{matrix} a \\ b \end{matrix} \end{matrix}
\qquad\qquad
\begin{matrix} a & b_1 & b_2 \\ \begin{bmatrix} L_p & L_{ps} & L_{ps} \\ L_{ps} & L_s & L_{sc} \\ L_{ps} & L_{sc} & L_s \end{bmatrix} & & \begin{matrix} a \\ b_1 \\ b_2 \end{matrix} \end{matrix}
$$

D. The Three-path Core Model with Six-coil

In a three-phase core with n coils the mutual inductances between the coils of different limbs are negative. For a six-coil system the inductance matrix is identified as follows

$$
\begin{array}{cccccc}
\quad\ \ \text{PRIMARY} & & & \text{SECONDARY} & & \\
a \quad\quad b \quad\quad c & & & a' \quad\quad b' \quad\quad c' & &
\end{array}
$$

$$
\left[\begin{array}{ccc|ccc}
L_p & -L_{pd} & -L_{pd} & L_{ps} & -L_{cw} & -L_{cw} \\
-L_{pd} & L_p & -L_{pd} & -L_{cw} & L_{ps} & -L_{cw} \\
-L_{pd} & -L_{pd} & L_p & -L_{cw} & -L_{cw} & L_{ps} \\
L_{ps} & -L_{cw} & -L_{cw} & L_s & -L_{sd} & -L_{sd} \\
-L_{cw} & L_{ps} & -L_{cw} & -L_{sd} & L_s & -L_{sd} \\
-L_{cw} & -L_{cw} & L_{ps} & -L_{sd} & -L_{sd} & L_s
\end{array}\right]
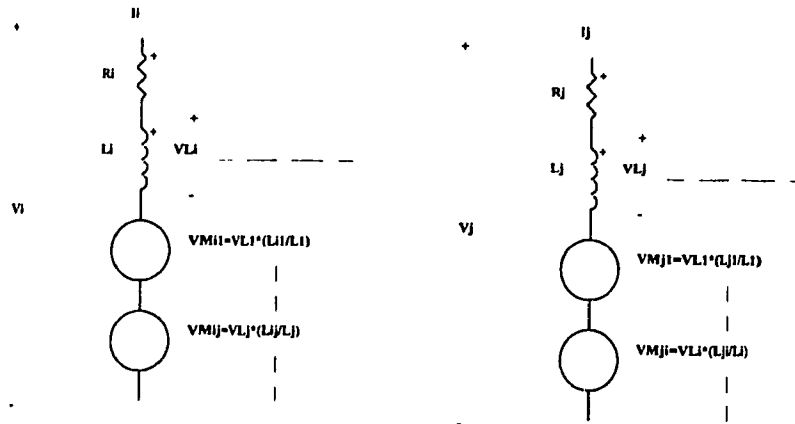\begin{array}{c}
a \\ b \\ c \\ a \\ b \\ c'
\end{array}
$$

E. The Three-path Core Model with Nine-coil

Similarly, for a three-phase nine-coil system the inductance matrix is identified as follows

$$
\begin{array}{ccccccccc}
\quad\quad\ \text{PRIMARY} & & & & & & \text{SECONDARY} & & \\
a_1 \quad a_2 \quad b_1 \quad b_2 \quad c_1 \quad c_2 & & & & & & a_1' \quad b_1' \quad c_1' & &
\end{array}
$$

$$
\left[\begin{array}{cccccc|ccc}
L_p & L_{pc} & -L_{pd} & -L_{pd} & -L_{pd} & -L_{pd} & L_{ps} & -L_{cw} & -L_{cw} \\
L_{pc} & L_p & -L_{pd} & -L_{pd} & -L_{pd} & -L_{pd} & L_{ps} & -L_{cw} & -L_{cw} \\
-L_{pd} & -L_{pd} & L_p & L_{pc} & -L_{pd} & -L_{pd} & -L_{cw} & -L_{cw} & -L_{cw} \\
-L_{pd} & -L_{pd} & L_{pc} & L_p & -L_{pd} & -L_{pd} & -L_{cw} & -L_{cw} & -L_{cw} \\
-L_{pd} & -L_{pd} & -L_{pd} & -L_{pd} & L_p & L_{pc} & -L_{cw} & -L_{cw} & L_{ps} \\
-L_{pd} & -L_{pd} & -L_{pd} & -L_{pd} & L_{pc} & L_p & -L_{cw} & -L_{cw} & L_{ps} \\
L_{ps} & L_{ps} & -L_{cw} & -L_{cw} & -L_{cw} & -L_{cw} & L_s & -L_{sd} & -L_{sd} \\
-L_{cw} & -L_{cw} & L_{ps} & L_{ps} & -L_{cw} & -L_{cw} & -L_{sd} & L_s & -L_{sd} \\
-L_{cw} & -L_{cw} & -L_{cw} & -L_{cw} & L_{ps} & L_{ps} & -L_{sd} & -L_{sd} & L_s
\end{array}\right]
\begin{array}{c}
a_1 \\ a_2 \\ b_1 \\ b_2 \\ c_1 \\ c_2 \\ a_1' \\ b_1' \\ c_1'
\end{array}
$$

F.   The Pspice Model

For analysis and simulation proposes a circuit model for the three-path

HFT in term of controlled source and regarding the respective matrix L is derived

by using (4.1). This model is presented hereafter

Experimental Control Circuit