

**A Novel Double Edge-Triggered Pulse-Clocked TSPC D Flip-Flop
for High-Performance and Low-Power VLSI Design Applications**

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Abstract

A Novel Double Edge-Triggered Pulse-Clocked TSPC D Flip-Flop for High-Performance and Low-Power VLSI Design Applications

Bill Pontikakis

Clocking is an important aspect of digital VLSI system design. The design of high-performance and low-power clocked storage elements is essential and critical to achieving maximum levels of performance and reliability in modern VLSI systems such as Systems on Chips (SoCs). In this thesis, a pulse-clocked double edge-triggered D-flip-flop (PDET) is proposed. PDET uses a new split-output true single-phase clocked (TSPC) latch and when clocked by a short pulse train acts like a double edge-triggered flip-flop. The P-type version of the new TSPC split-output latch is compared with existing TSPC split-output latches in terms of robustness, area, and power efficiency at high-speeds. It is shown that the new split-output latch is more area-power efficient, and significantly more robust, than the existing split-output CMOS latches. The novel double edge-triggered flip-flop uses only eight transistors with only one N-type transistor being clocked. Compared to other double edge-triggered flip-flops, PDET offers advantages in terms of speed, power, and area. Both total transistor count and the number of clocked transistors are significantly reduced to improve power consumption and speed in the flip-flop. The number of transistors is reduced by 56%-60% and the Area-Period-Power product is reduced by 56%-63% compared to other double edge-triggered flip-flops. Simulations are performed using HSPICE in CMOS 0.5 μm technology. This design is suitable for high-speed, low-power CMOS VLSI design applications.

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This work would not have been possible without the help of God. I completed my degree within one year even though I was diagnosed with cancer. God gave me the strength to continue and not to give up. A month after my long surgery I was already back in the university and working on my thesis. Even when I had to go through my radiation therapy treatments I did not give up. I did not listen to the doctors and rest, but instead every day after my morning treatment I was walking my way to the university. I cannot imagine how else I was able to do this, except with the help of God. He listened to every single of my prayers, He guided me, He gave me strength.

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I want to thank my supervisor Dr. Mohamed Nekili for his guidance and understanding during the period we worked together. I also like to thank Dr. M. Reza Soleymani, the M.A.Sc. director, for trusting my abilities. Finally, I want to thank the people of our research group, the interconnect and clocking group, and the people of the VLSI lab.

Dedication

I dedicate my thesis to my father, who died in November 2000 from cancer. It was his dream to see me one day graduating but unfortunately he did not have the opportunity. Throughout my life he always trusted my abilities and always wanted the best for me. He pushed me to succeed and he even sacrificed his own happiness, to see me during his last days and hours, in order for me to succeed. If it wasn't for him, I wouldn't be where I am now and I wouldn't be who I am now.

Table of Contents

List of Figures	ix
List of Tables	xii
Chapter 1 Introduction and Motivation	1
1.1 CMOS VLSI Technology	1
1.2 Clocked Logic in Synchronous Systems	2
1.3 System Clock Design	4
1.4 Clock Skew	5
1.5 Organization of the Thesis	7
Chapter 2 Review of TSPC-Based Synchronous Circuits	8
2.1 Introduction	8
2.2 Original True Single-Phase Clock Circuit Techniques	9
2.2.1 Step Response	14
2.2.2 Circuit Examples	15
2.3 A Single-Phase Clocking Scheme for VLSI Systems	18
2.3.1 Basic Components of Single-Phase Clocking	19
2.3.1.1 Storage Elements	19
2.3.1.2 Pre-charged Logic	20
2.3.2 Robust TSPCs for Low Power, High-Speed VLSI Applications	21
2.4 New TSPC Latches with Improved Speed and Power Savings	23
2.5 Conclusion	25

Chapter 3	A New Area-Power Efficient Split-Output TSPC CMOS Latch for High-Speed VLSI Applications	27
3.1	Introduction	27
3.2	Original TSPC Split-Output Latches	28
3.2.1	Original P-split-output latch, Yuan89	29
3.2.2	Modified P-split-output latch, Ghan94	31
3.3	Recent P-Split-Output Latches	33
3.3.1	Improved P-split-output latch, Yuan97	34
3.3.2	New P-split-output latch, Pontik2001	35
3.4	Operation of the New Split-Output Latch	38
3.4.1	Case I: Low-to-high transition of the input when clock is high	39
3.4.2	Case II: High-to-low transition of the input when clock is high	39
3.4.3	Case III: Low-to-high transition of the input when clock is high	40
3.4.4	CASE IV: High-to-low transition of the input when clock is low	40
3.5	Results and Comparative Study	41
3.6	Conclusion	42
Chapter 4	A Novel Double Edge-Triggered Pulsed Clocked TSPC D Flip-Flop for High-Performance and Low-Power VLSI Design Applications	43
4.1	Introduction	43
4.2	Pulse Generation Circuitry	44
4.3	TSPC Double Edge-Triggered Flip-Flops	46
4.4	Comparative Study of Double Edge-Triggered Flip-Flops	49

4.5 Conclusion	54
Chapter 5 A Four-Bit Shift Right Register Using PDET	56
5.1 Introduction	56
5.2 Implementation and Simulation of the Shift Register	57
5.3 Comparison of the Standard TSPC Style and PDET Style Shift Registers	60
5.4 Conclusion	62
Chapter 6 Conclusion and Future Work	63
References	66

List of Figures

Figure 1.1: Clock frequency vs. year for various computing systems	2
Figure 1.2: The concept of Finite-State Machine (FSM)	3
Figure 1.3: System Clocking Schemes: (a) single-phase clock; (b) two-phase clock; (c) multiple-phase clocks	5
Figure 1.4: Clock Timing Diagrams	6
Figure 2.1: C ² MOS Logic	9
Figure 2.2: NORA dynamic CMOS technique	10
Figure 2.3: True single-phase clock latches	11
Figure 2.4: Logic arrangements using true single-phase latches	12
Figure 2.5: Split-output latches	13
Figure 2.6: TSPC-1 circuit	13
Figure 2.7: TSPC-2 circuit	14
Figure 2.8: Step responses of NORA, TSPC-1, and TSPC-2	14
Figure 2.9: Output dips of NORA, TSPC-1, and TSPC-2	15
Figure 2.10: Circuits constructed by P, N-blocks, N-C ² MOS stages: (a) positive transition latch; (b) negative transition latch; and (c) divide-by-two circuit	16
Figure 2.11: Circuits constructed by split-output latch stages: (a) positive transition latch; (b) divide-by-two circuit	16
Figure 2.12: Different results with the position of the input transitions for the nine-transistor latch of Fig. 10(a)	17
Figure 2.13: a) Single-phase state machine structure and (b) the clock signal	18

Figure 2.14: Single-phase positive edge triggered flip-flop: (a) circuit diagram and (b) parameters	19
Figure 2.15: Circuits and parameters of latches: (a) N-latch and (b) P-latch	20
Figure 2.16: Pre-charged logic circuits and timing diagrams of (a) N-block and (b) P-block	21
Figure 2.17: (a) A clocked self-timed N-latch and (b) a clocked self-timed P-latch	22
Figure 2.18: Different clocked self-timed N-latches on pass transistor logic	23
Figure 2.19: Single-stage TSPC full-latch (FL) with a pre-charged node signal	24
Figure 2.20: A non pre-charged single-stage TSPC full-latch (FL)	25
Figure 2.21: A split-output non-pre-charged N-latch	25
Figure 3.1: P-type split-output latch, Yuan89	30
Figure 3.2: Output waveform for Yuan89 latch	31
Figure 3.3: P-type split-output latch, Ghan94	32
Figure 3.4: Output waveform for Ghan94 latch	33
Figure 3.5: P-type split-output latch, Yuan97	34
Figure 3.6: P-type split-output latch, Pontik2001	36
Figure 3.7: Output Waveform for Pontik2001 latch	37
Figure 3.8: N-type split-output latch, Pontik2001	39
Figure 4.1: Double edge-triggered pulsed-clock generator	45
Figure 4.2: Generated pulses on both edges of the square clock	45
Figure 4.3: Two double edge-triggered flip-flops, (a) Afghahi91a (b) Afghahi91b	46
Figure 4.4: Double edge-triggered flip-flop, Wang97	47
Figure 4.5: Proposed double edge-triggered TSPC D-flip-flop (PDET)	48

Figure 4.6: Simulation results, Afghahi91a	49
Figure 4.7: Simulation output waveform of PDET	51
Figure 4.8: Layout of the double edge-triggered pulse-clocked generator together with PDET	52
Figure 5.1: Use of registers for synchronization in core logic and its inputs and outputs	56
Figure 5.2: Two-bit shift register in split-output TSPC style	58
Figure 5.3: Four-bit shift register, using PDET Flip-Flops	59
Figure 5.4: Output waveforms of the four-bit shift register	59

List of Tables

Table 3.1: Transistor Sizes, Number Of Transistors and C-locked Transistors, and Total Capacitance	38
Table 3.2: Area, Power, and Robustness Characteristics	42
Table 4.1: Features of Double Edge-Triggered Flip-Flops	53
Table 4.2: Area, Power, Speed Characteristics	54
Table 5.1: Features of TSPC style four-bit right shift registers	61

CHAPTER 1

Introduction and Motivation

1.1 CMOS VLSI Technology

Among the different choices of digital IC technologies, CMOS technology has become and will continue to be the dominant technology for VLSI design. CMOS has become the standard technology because, silicon wafer cost is cheap, devices are easier to understand and therefore it is easier to implement CAD tools, and the circuits are easier to design [1]. CMOS offers the lowest power-delay product compared to other established technologies, and has low power consumption. Therefore, CMOS technology is the most suitable for realizing modern VLSI systems such as SoCs (Systems on Chips).

The most important property of CMOS is scaling and manufacturability. The cost per function of CMOS devices can be reduced with the continuous scaling down of the technology. A scaled-down CMOS device has reduced parasitics, reduced power dissipation per gate, an increased packing density, and increased driving current [1].

Advancement in CMOS technology will continue to be the driving force in high-performance microprocessors, in SoCs, and in DSP (Digital Signal Processors). Therefore, CMOS was the choice of technology for the design of our high-performance circuits.

before the tick of the clock, since their final values are being captured by that clock event [2]. Most synchronous digital systems consist of cascaded banks of sequential registers with combinational logic between the registers [3]. Therefore, the design of efficient sequential registers is important. In a synchronous system, each data signal is stored in a latched state within a storage element awaiting the incoming clock signal, which determines when the data signal leaves the storage element [3]. The synchronous system includes combinational logic and clock storage elements, which together constitute a finite state machine (FSM). Clock and input signal changes dictate the changes of state in the FSM as illustrated in Fig. 1.2. In digital systems, the clock designates the exact moment when the state is changing, as well as when the next state is captured [2].

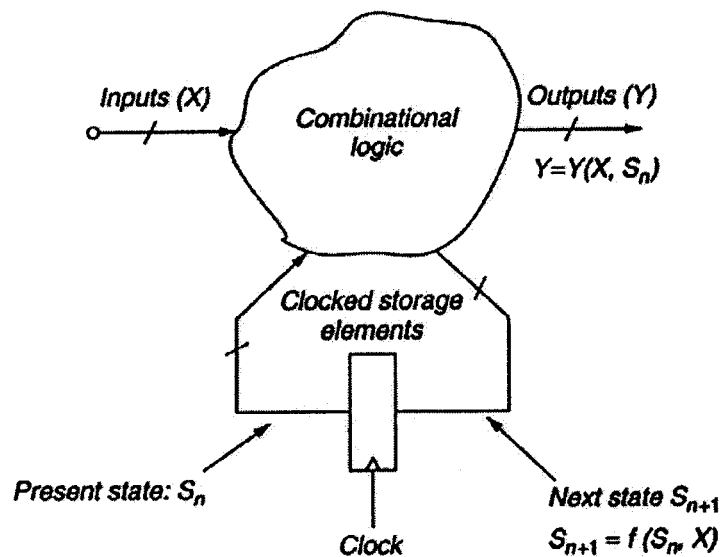


Fig. 1.2. The concept of Finite-State Machine (FSM) [2].

The delay components that constitute a general synchronous system are composed of the following three individual subsystems:

- 1) the memory storage elements,
- 2) the logic elements, and
- 3) the clocking circuitry and distribution network [3].

This work is concentrated on the design of memory storage elements, since they are critical subsystems in achieving high levels of performance and reliability in the system.

1.3 System Clock Design

The clock system is divided into two distinct categories: *clock generation* and *clock distribution* [2]. The nature of clock storage elements is intimately connected to the clock system generation and distribution, and it is the nature of clocked storage elements that dictates the requirements imposed on the clock system [2]. The different clocking schemes that are used in synchronous designs are illustrated in Fig 1.3. The clocking system can consist of a single-phase clock or multiple-phase clock. Transfer of data between different clocked storage elements is accomplished by using an active phase of the clock. Therefore, the clock phase controls the transfer of information between the clocked storage elements in the synchronous digital VLSI system. Single-phase clocking is used in high-performance systems and therefore this work is based on this clocking scheme.

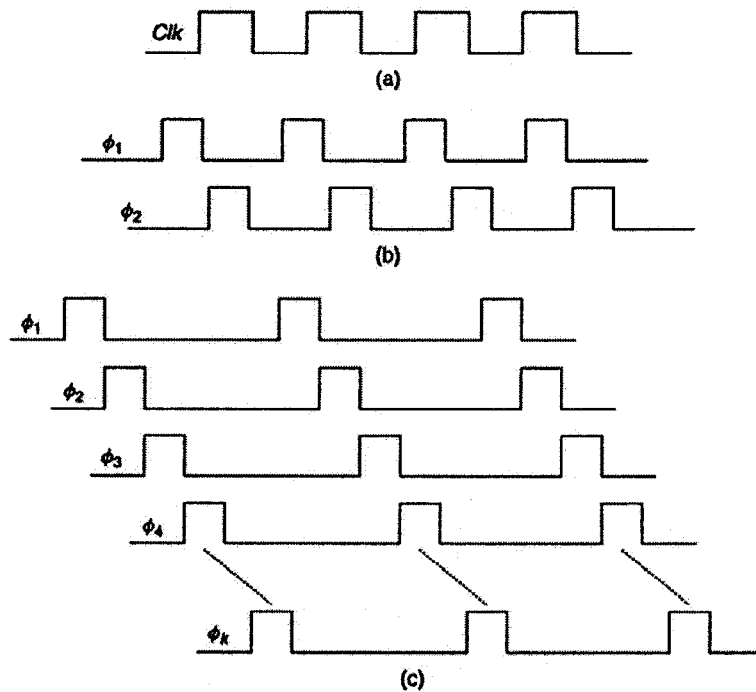


Fig. 1.3. System Clocking Schemes: (a) single-phase clock;
 (b) two-phase clock; (c) multiple-phase clocks [2].

1.4 Clock Skew

Ideally, clocking events occur at all registers simultaneously. Given this clocking strategy, the clock signal arrival times at each register are defined with respect to a universal time reference [3]. Because of various delay characteristics of the clock paths to the various points in the system, as well as different loading of the clock signal at different points, the clock signal arrives at different points at different times [2]. This difference in clock signal arrival times between two sequentially adjacent registers is defined as the *clock skew*, T_{skew} [2]. Therefore, clock skew is defined as the spatial variation of the clock signal distributed throughout the system [2].

There are positive and negative clock skews. If the arrival time of the clock signal at the final register leads that of the time arrival of the clock of the first register, then the clock skew is referred to as *positive clock skew* and, under this condition, the maximum attainable operating frequency is decreased [3]. On the other hand, if the time of arrival of the clock signal at the final register lags that of the time arrival of the clock of the first register, then the clock skew is referred to as *negative clock skew*, and this skew can be used to improve the delay of the critical path. The positive and negative clock skews are illustrated in Fig. 1.4 where C_i and C_f are the initial and final clocks, respectively.

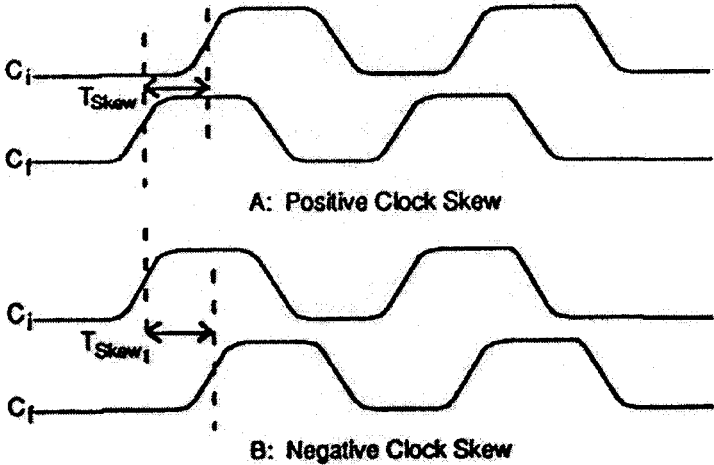


Fig. 1.4. Clock Timing Diagrams [3].

It is important to adopt a circuit technique that avoids positive clock skew in order to improve the performance of a digital system. Therefore, in our study we have adopted the TSPC (True Single Phase Clock) circuit technique, since it uses only one phase of the clock and avoids skew problems, for the design of our clocked storage elements.

1.5 Organization of the Thesis

The thesis is organized as follows. Chapter 2 discusses previous work on TSPC-based synchronous circuits. Chapter 3 introduces a new TSPC split-output latch which is more robust and achieves higher speed while dissipating lower power and consuming less area than previous TSPC split-output latches. Chapter 4 introduces a novel pulsed clocked double-edge triggered split-output TSPC flip-flop, called PDET. This novel double-edge triggered flip-flop uses a special pulse generation circuit and improves the performance while significantly reducing the area consumed by the circuit. Chapter 5 shows a 4-bit shift register that is built using four PDETs in series. Finally, Chapter 6 concludes the thesis work and suggests possible future directions of research in the area of clocked storage elements for digital system design.

CHAPTER 2

Review of TSPC-Based Synchronous Circuits

2.1 Introduction

In VLSI technology, dynamic clocking schemes such as the NORA (NO Race) scheme using true two-phase clock signals ϕ_1 , and ϕ_2 have been used to avoid race problems caused by clock skew, the imperfect synchronization between a clock signal and its inverse. This scheme requires some constraints on logic combination, such as clock edges of short duration that increases the demand on both the clock generation circuitry and the interconnections that distribute the clock signals across the chip. As a dynamic CMOS technique, NORA is sensitive to charge sharing and leakage.

The true single-phase clock dynamic CMOS circuit technique uses only one clock signal that is never inverted and fits both static and dynamic CMOS circuits. There are several benefits with this technique such as the elimination of skew due to different clock phases and the clock signal being generated off – chip, which implies significant savings in chip area and power consumption. The generation and distribution of the clock is likely not to be a factor on maximum sustainable clock frequency. A single global clock signal needs to be generated and distributed, thus simplifying the design. A few drawbacks are the need for two extra transistors in each stage, a clock delay problem that can be eliminated as long as we keep this delay less than the gate delay, thus improving the reliability. P-blocks become a speed bottleneck, pre-charged nodes consume power and clock loads might be encountered.

The aim of this chapter is to review and discuss the existing circuit solutions using the TSPC technique. This chapter is structured as follows. In section 2.2, the clocking strategy using the original true single-phase latches is discussed. A discussion on single-phase clocking scheme for VLSI systems and the introduction of new robust TSPC circuits for low power, high-speed VLSI applications follows in section 2.3. New TSPC latches and flip-flops with improved speed and power savings are mentioned in section 2.4. A conclusion of this chapter can be found in section 2.5.

2.2 Original True Single-Phase Clock Circuit Techniques

Systems using CMOS circuits of both static and dynamic nature involve a clocking strategy for the purpose of system timing. The original clocking strategy was the clocked CMOS logic (C^2 MOS) shown in Fig. 2.1, which uses a non-overlapping pseudo two-phase clock. This system is very sensitive to clock skew (one clock can experience more propagation delay than the other), which has become a dominant problem in current high-performance designs and results in difficulties in increasing circuit speed.

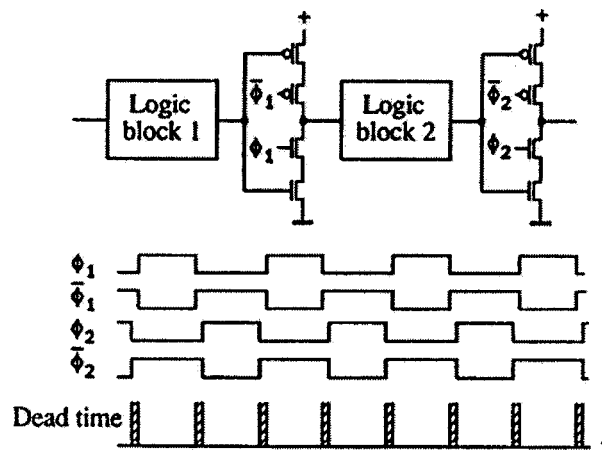


Fig. 2.1. C^2 MOS Logic [8].

The NORA dynamic CMOS technique uses a true non-overlapping two-phase-clock signal ϕ and ϕ' , and can avoid race problems caused by clock skew [8]. This technique extends the concept of the C²MOS latch to support the effective implementation of pipelined circuits by adding a precharge and an evaluation stages. In order to ensure correct operation and avoid races, the number of static inversions between C²MOS latches should be even, in the absence of dynamic nodes, and in the presence of dynamic nodes, the number of static inverters between a latch and a dynamic gate in the logic block should also be even [5]. Inputs to a dynamic ϕ block are only allowed to make a single $0 \rightarrow 1$ or $1 \rightarrow 0$ transitions during the evaluation period. NORA dynamic CMOS technique can reach higher clock rates than the C²MOS technique since there is no dead time and no skew problem [5]. The NORA dynamic CMOS technique is shown in Fig. 2.2.

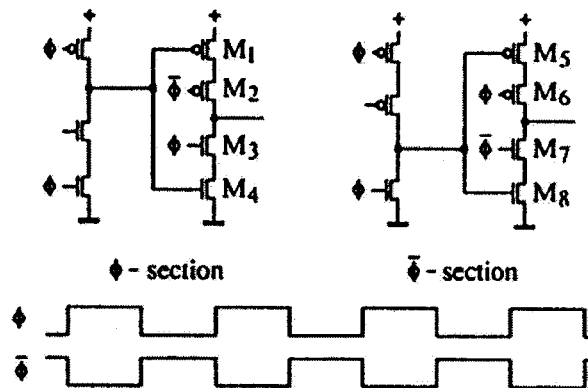


Fig. 2.2. NORA dynamic CMOS technique [8].

The NORA design can easily be simplified to use even fewer clock signals. The true single-phase clock dynamic CMOS circuit technique uses a single clock signal that is

never inverted and is sufficient to operate a dynamic CMOS circuit [7]. No clock skew exists and higher clock rates can be reached, but clock delay problems exist.

In Fig. 2.2, the ϕ -C²MOS and ϕ' -C²MOS latches can be replaced by the modified doubled N-C²MOS and doubled P-C²MOS latches, respectively [5]. If we use two doubled N-C²MOS or P-C²MOS in series, then true single-phase clock latch stages are formed, called N-latch and P-latch, respectively (Fig. 2.3).

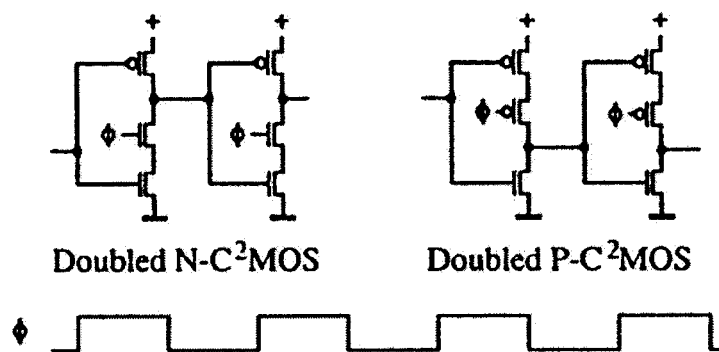


Fig. 2.3. True single-phase clock latches [8].

The N or P sections are using an N or P pre-charge block, respectively. In the N-C²MOS latch case, when ϕ is high, the latch is non-inverting, since it is in the evaluation mode and corresponds to two cascaded inverters [5]. The latch is in hold-mode when $\phi = 0$ and both inverters are disabled. Only the pull-up circuits are active while the pull-down network is deactivated. With this dual stage approach, signals cannot propagate from the input of the latch to the output, resulting in the elimination of race problems [5].

Apparently, this design is better to the C²MOS approach and can compete with the NORA design. This technique uses the same clock signal in both the N-section, consisting of an N-latch and logic blocks, and the P-section consisting of a P-latch and logic blocks. The logic blocks can be both of static and dynamic nature. The even

inversion constraint either between two latches or between a latch and a dynamic block has been removed [8]. The number of transistors per latch has been increased by two (six instead of four) but have replaced the need of distributing the ϕ' clock signal [5], [8]. The system is reliable as long as the clock delay is less than the gate delay [8]. The logic function blocks can be included in the N-C²MOS or P-C²MOS latches or placed between, as shown in Fig. 2.4.

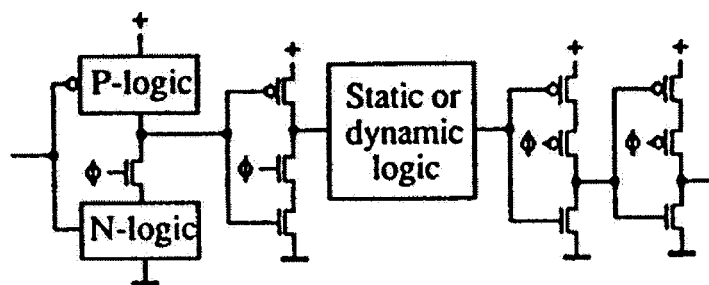


Fig. 2.4. Logic arrangements using true single-phase latches [8].

A simplified version of the true single-phase clock latch stages is shown in Fig. 2.5, called split-out latch. Only the first inverter is controlled by the clock resulting in clock load reduction by half and a reduction of the number of transistors [5]. Since some transistors are used for the transmission of both the high and low signals, a disadvantage is that not all node voltages in the latch have a full voltage swing, which results in a reduced drive for the output NMOS transistor and a loss in performance [5].

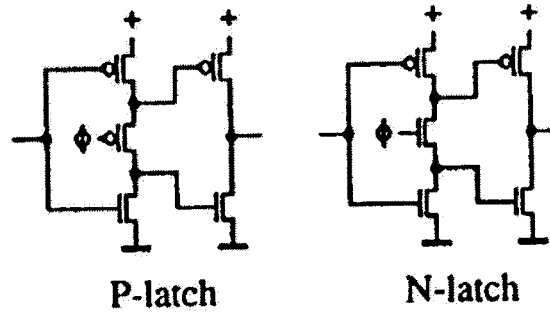


Fig. 2.5. Split-output latches [8].

Since pre-charge signals in the TSPC technique will play the same role as ϕ' in both ϕ and ϕ' sections in Fig. 2.2, the NORA circuit can be simplified to the true single-phase clock 1 (TSPC-1) of Fig. 2.6 and to the more reliable single-phase clock 2 (TSPC-2) of Fig. 2.7.

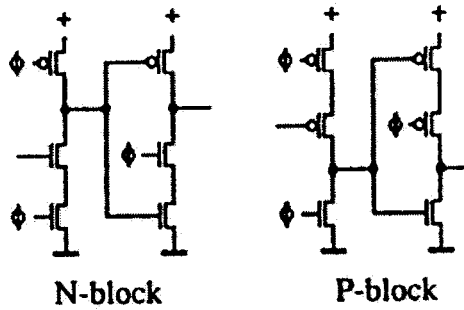


Fig. 2.6. TSPC-1 circuit [8].

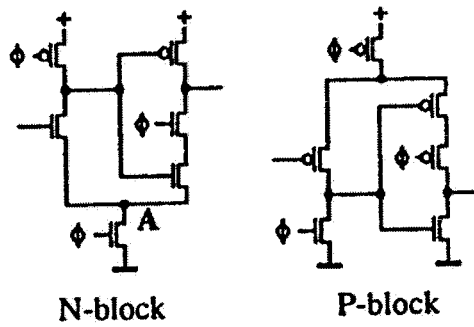


Fig. 2.7. TSPC-2 circuit [8].

2.2.1 Step Response

Because the number of transistors is reduced in the TSPC-1 and TSPC-2 models, the delay of the latch stage is reduced as well. The most critical slope in the circuit is the rise slope; therefore, by omitting the P-transistor in the latch stage gives TSPC-1 a shorter evaluation time which results in speed improvement [8]. A better performance is achieved with TSPC-2 since it does not output the pre-charge state first: i.e., it prevents the output from going low, which makes the rise time shorter as shown in Fig. 2.8 [8].

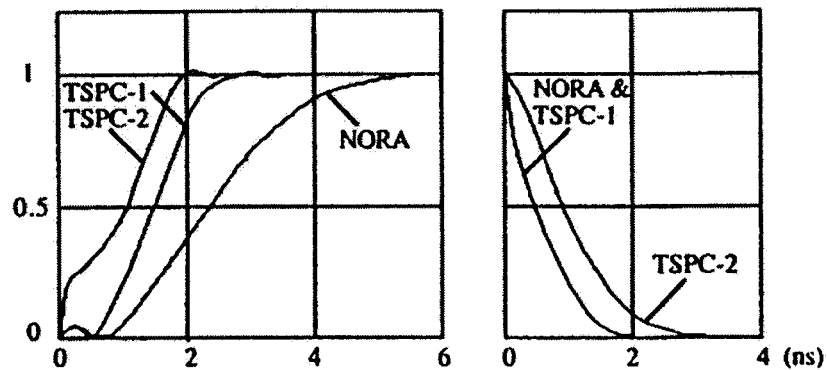


Fig. 2.8. Step responses of NORA, TSPC-1, and TSPC-2 [8].

The TSPC-2 circuit has also smaller dips in the output while the output should be kept high, as shown in Fig. 2.9 [8]. To obtain the advantages mentioned, the P-block of TSPC-2 should be widened. The TSPC-2 circuit is more reliable in latching a signal [8].

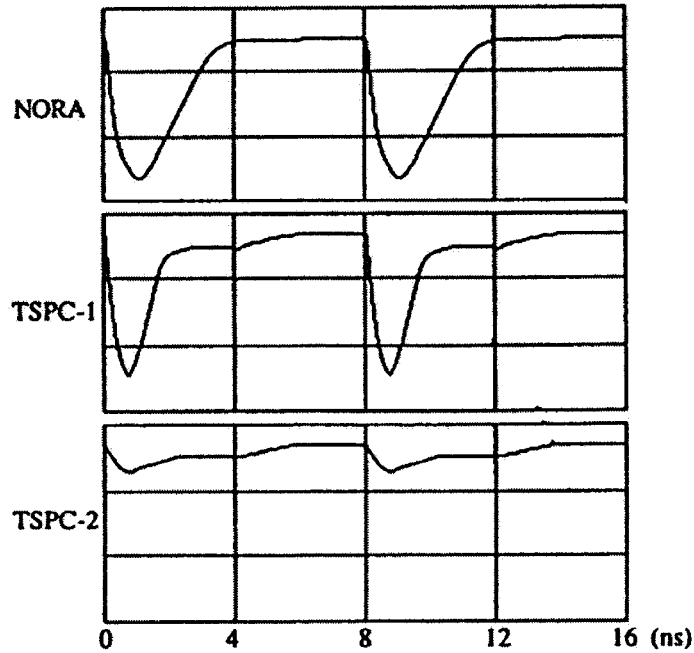


Fig. 2.9. Output dips of NORA, TSPC-1, and TSPC-2 [8].

2.2.2 Circuit Examples

The basic TSPC latches can be combined in different ways to implement all essential sequential circuits. The flexibility of TSPC is substantial since both static and dynamic circuits can be used. The N-type and P-type latches mentioned above can be cascaded to form an edge-triggered D flip-flop, as illustrated in Fig. 2.10. This flip-flop is constructed by using a P-C²MOS stage, an N pre-charge stage and an N-C²MOS stage [8]. The input data will be latched by the positive transition of the clock signal in Fig. 2.10(a), while the

negative transition of the clock signal will latch the input data in Fig. 2.10(b) [8]. A divide-by-two circuit is formed by connecting the inversion output to the input of the circuit in Fig. 2.10(a) and replacing the clock signal ϕ by an input signal. The resulting divide-by-two circuit is illustrated in Fig. 2.10(c). The five-transistor split-output latch of Fig. 2.5 is used in Fig. 2.11, which has almost the same speed as the other two circuits but only half the clock load [8]. This is of major importance for employing effective shift-register chains with fewer transistors, less load, and without output glitches.

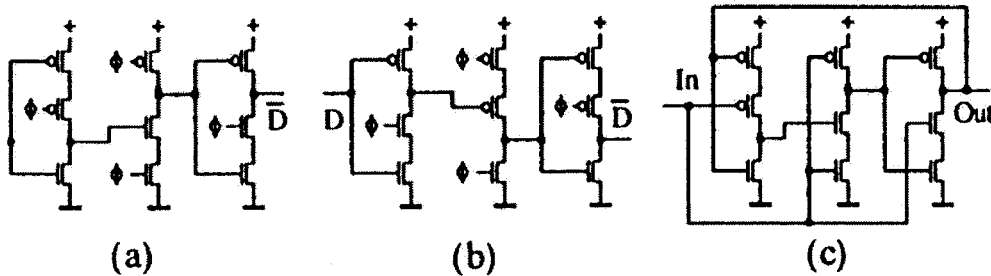


Fig. 2.10. Circuits constructed by P, N-blocks, N-C²MOS stages: (a) positive transition latch; (b) negative transition latch; and (c) divide-by-two circuit [8].

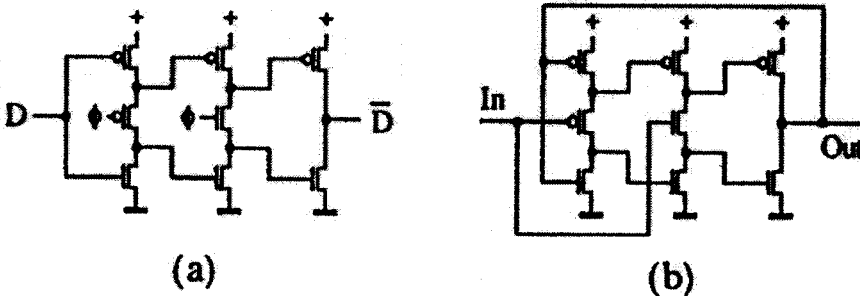


Fig. 2.11. Circuits constructed by split-output latch stages: (a) positive transition latch; (b) divide-by-two circuit [8].

The D latches of Figs. 2.10(a) and 2.11(a) use for the precharge stage a P-C²MOS stage with only three transistors. Such a configuration requires an input transition from low to high with a longer delay than the evaluation delay of the next N-block, otherwise the active transistor in the N-block may cut off too early and there will be a reduction in the output voltage swing [8]. This effect is illustrated in Fig. 2.12 where the delay in the input signal is changed from 0.8 to 0.5 ns and the output voltage swing is reduced in about the half V_{dd} . However, when these D latches are cascaded the delay of the last latch is satisfactory for the requirement of the next latch. The N-C²MOS stage behaves similarly and this behavior made hard the design of the 4-bit shift register discussed in chapter 5.

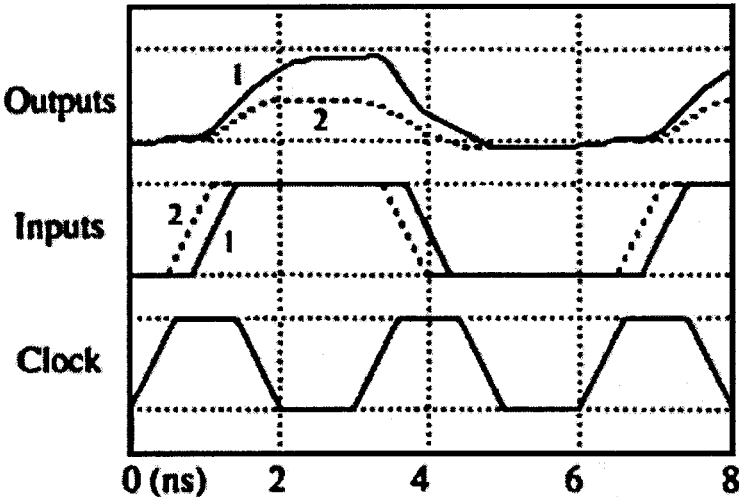


Fig. 2.12. Different results with the position of the input transitions for the nine-transistor latch of Fig. 10(a) [8].

2.3 A Single-Phase Clocking Scheme for VLSI Systems

The increase of design costs and cost of wiring are some of the consequences resulting from the increased level of integration and higher speeds of the newly developed VLSI technologies. The increased complexity of design has resulted in the increased design cost. Simplicity can make the design easier and therefore decrease the design cost. Safety reduces design cost by the decrease of the need for careful timing analysis [9]. The use of many clock phases is a partial cause for the high wiring cost of CMOS systems. The single-phase clocking is simple, safe, and transistor-count effective, making it therefore well suited for the design of CMOS circuits and systems [9]. Furthermore, it is generally enough to handle static, dynamic, pre-charged, domino logic, and array logic such as memories and PLAs, while it allows higher clock frequencies [9].

This discussion is focused on the “safety” of the timing behavior. The term “safe” is used to denote safety against races, clock skew, hazards, clock-slope problems, etc... [9]. A finite state machine structure (Fig. 2.13) that uses a positive edge-triggered D flip-flop will be used for the discussion of safe clocking. The circuit is safe if a state signal cannot pass the combinational logic block more than once during a single clock cycle [9].

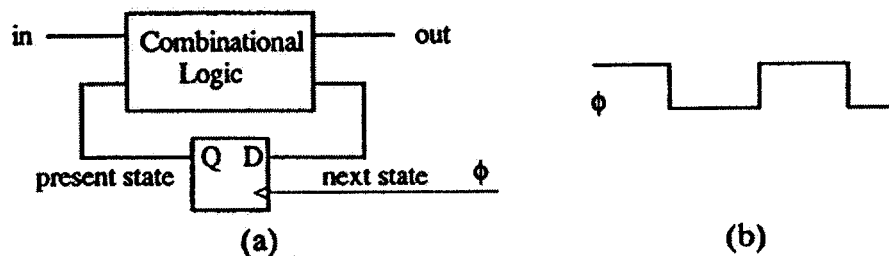


Fig. 2.13. (a) Single-phase state machine structure and (b) the clock signal [9].

2.3.1 Basic Components of Single-Phase Clocking

In this part, we will discuss the basic components of single-phase clocking, such as, the storage elements and the pre-charged logic.

2.3.1.1 Storage Elements

In this section, the timing behavior of storage elements will be considered because the movement of data in a synchronous system is controlled by clocked storage elements [9]. A dynamic positive edge-triggered D flip-flop is shown in Fig. 2.14(a). “The input data must be valid during the interval given by the setup (U) and hold (H) times of the device and the output data are available and stable D_{CQ} after the active clock edge” [9], as shown in Fig. 2.14(b). A small limitation of these circuits is that the clock rise time must be short. This dynamic single-phase clocking flip-flop can be used instead in the state machine of Fig. 2.13.

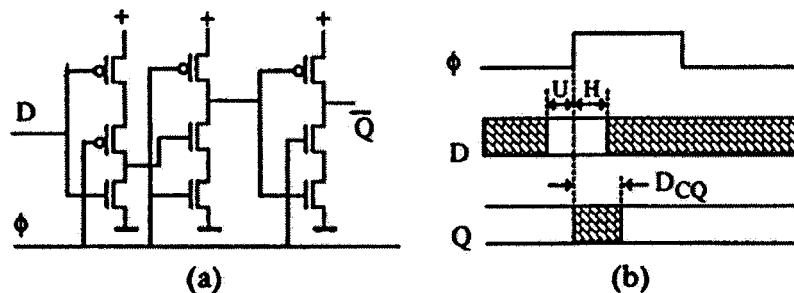


Fig. 2.14. Single-phase positive edge triggered flip-flop:

(a) circuit diagram and (b) parameters [9].

The prevention of race-through problems can be achieved by designing two latches that are transparent on the high and low part of the signal [9]. A circuit for a latch that is

transparent when the clock signal is high and latches data when the clock signal goes low is shown in Fig. 2.15(a), while Fig 2.15(b) shows a circuit for a latch that is transparent when the clock signal is low and latches the data when the clock signal goes high. Timing diagrams of these circuits are also shown in the same figure.

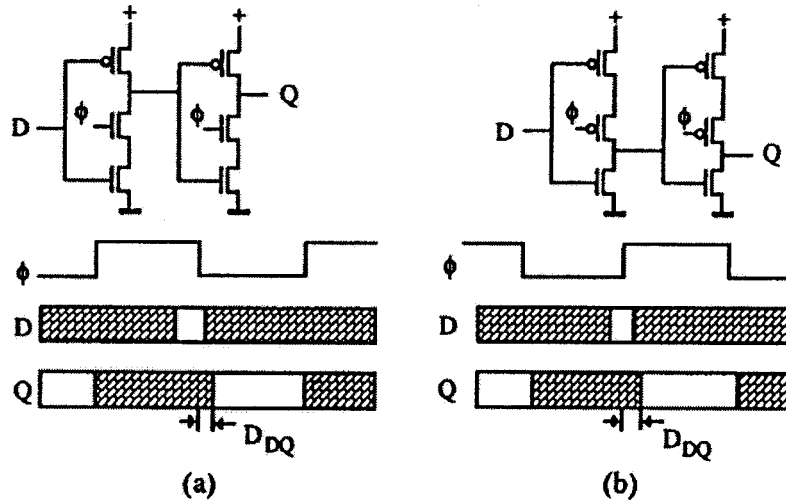


Fig. 2.15. Circuits and parameters of latches: (a) N-latch and (b) P-latch [9].

2.3.1.2 Pre-charged Logic

Several levels of n-MOS dynamic logic evaluation can be performed per clock cycle when a single-phase clock signal is used in CMOS circuits. Single-phase pre-charged dynamic logic is based on N and P blocks [9]. These blocks are shown in Fig. 2.16(a) with their respective timing diagrams in Fig. 2.16(b). An N-block is in the pre-charge phase (P) when the clock is low and in the evaluation phase (E) when the clock signal is high [9]. On the other hand, a P-block is pre-charging when the clock signal is low and evaluating when the clock signal is low. The output of an N-block that is in the evaluation phase is used to drive a P-block that is in the pre-charging phase. An N-block cannot be cascaded with another N-block because both blocks are in the same phase. The

clock frequency is determined by the pre-charging and discharging time of the P-block that is slow [12]. Thus, this is a main drawback, since the fast N-logic block is not fully utilized.

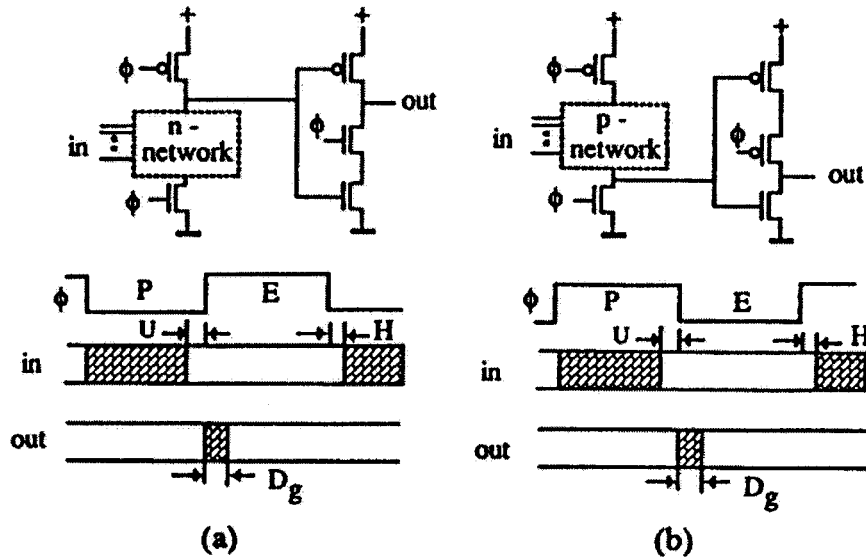


Fig. 2.16. Pre-charged logic circuits and timing diagrams of (a) N-block and (b) P-block [9].

2.3.2 Robust TSPCs for Low Power, High-Speed VLSI Applications

The need for portability and the increased cost of packaging have made low power consumption important in the VLSI system design. The originally developed true single-phase registers are very sensitive to clock signal slope. A large proportion of the power consumed in these registers is spent in pre-charging the internal nodes, which makes TSPC registers less suitable for low power applications.

A clock signal must propagate through the whole clock network to reach a transistor; therefore, the clock network must be as simple as possible. The new TSPC components

achieve low power, high speed, and robust operation by moving some of the tasks previously done by the clock signal to local data signals [10].

One implementation of the new TSPC components, a single clocked differential N-latch, is shown in Fig. 2.17(a). When the clock signal is high, the evaluation phase takes place and, depending on the differential inputs, either node out or out' is pulled down [10]. The two cross-coupled P transistors start the regenerative action and set nodes out and out' to V_{dd} and V_{ss} , respectively, or vice versa [10]. During the next evaluation phase, transition at the output nodes out and out' will occur only if the data inputs change. Latching is performed by the data inputs in a self-timed manner, making this circuit insensitive to clock signal slope [10]. Fig. 2.17(b) shows the complementary P-latch in which the evaluation phase takes places when the clock signal is low. These flip-flops need careful rationing of the P and N-type transistors for correct operation [11].

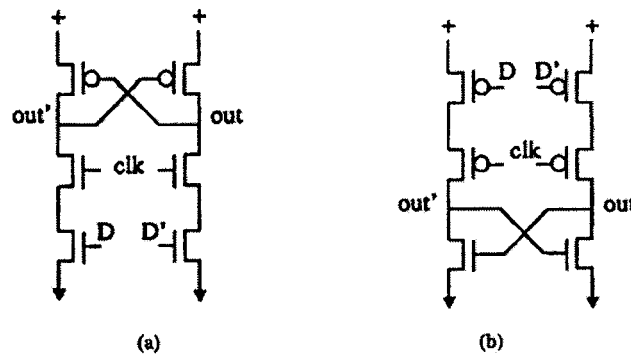


Fig. 2.17. (a) A clocked self-timed N-latch and (b) a clocked self-timed P-latch [10].

The above latches are somewhat slow because of the regenerative action of the cross-coupled load transistors [10]. Fig 2.18(a) shows an N-latch circuit that uses pass transistors to pull-up and pull-down the out and out' nodes. This latch is faster and

consumes less power. The N-latch of Fig. 2.18(b) can be used to construct a divide-by-two circuit. In Fig 2.18(c), the output nodes have been connected to two output inverters in order to increase the driving capability of the latches and to isolate them from the circuit of the next stage [10].

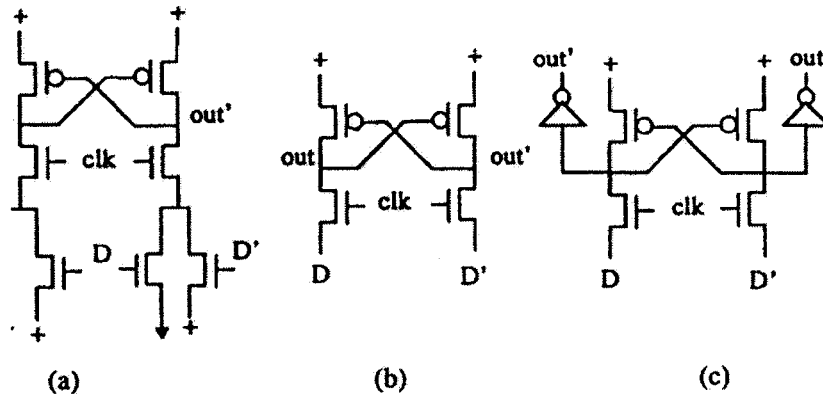


Fig. 2.18. Different clocked self-timed N-latches on pass transistor logic [10].

2.4 Recent TSPC Latches with Improved Speed and Power Savings

The recent TSPC circuits that will be introduced in this section reduce considerably the speed and power bottlenecks of the original true single-phase clocking latches and flip-flops [13]. The logic related transistors are purely N-type in both N and P-latches. This gives an advantage to CMOS circuits since the P-blocks add an additional delay to the circuit and become speed bottlenecks.

A single-stage TSPC full-latch (FL) can latch both low and high inputs by utilizing the available pre-charged node signal as shown in Fig. 2.19. The dash-line box in the figure is a TSPC full-latch which is similar to a C^2 MOS stage [13]. During the high clock phase, both P and N-blocks in the full-latch become non-conductive, and during the low clock

phase the blocks are data-dependently conductive [13]. Both one and zero data inputs are accepted. This technique has a few advantages. An inverter can be placed between stages to generate complementary inputs, regardless whether the succeeding stage is pre-charged or not [13]. The succeeding stage of an output node does not need to be pre-charged because the data is fully latched at the output node of a single stage [13]. The output node is a three-state node, which is useful in driving a bus for example [13]. The overall speed is improved in the case of generating complementary outputs. This flip-flop does not require stable inputs in both high and low clock phases [13].

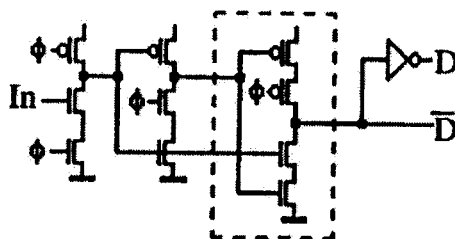


Fig. 2.19. Single-stage TSPC full-latch (FL) with a pre-charged node signal [13].

The non-pre-charged TSPC latches are more robust than the pre-charged latches due to larger noise margins [13]. We can make the N-latch “pre-charged” by adding a pre-charging P-transistor at the output node of the first static N-stage, as shown in Fig. 2.20 [13]. The size of the P-transistor marked by * in the first stage is minimized, as it is only used for preventing charge sharing which increases the robustness of the N-latch [13].

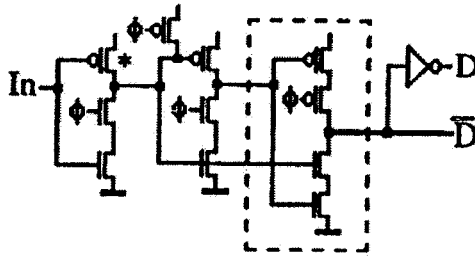


Fig. 2.20. A non pre-charged single-stage TSPC full-latch (FL) [13].

We can apply the same modification to the split-output N-latch as shown in Fig. 2.21, which has less clock load and uses only three clocked transistors in total. This flip-flop and the one of Fig. 2.20 do require stable inputs during high clock phase [13].

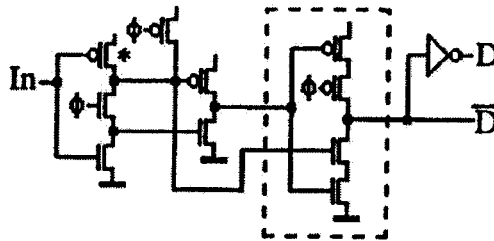


Fig. 2.21. A split-output non-pre-charged N-latch [13].

2.5 Conclusion

In this chapter, recent CMOS techniques using true single-phase clocking (TSPC) were reviewed. The advantages of TSPC are compact clock distribution, high speed, logic design flexibility, and robustness to slow clock edges that eliminates the race hazards. A single-phase clocking scheme, for high-speed and compact VLSI digital systems, that is general, safe, and simple, was discussed. It provides a structure that contains all components of a digital VLSI system including static, dynamic, and pre-charge logic.

Dynamic TSPC latches for low power and high-speed VLSI applications were also discussed. These latches are slope insensitive and the power consumption in these latches is data dependent. Finally, recent TSPC flip-flops were reviewed that reduce the speed and power bottlenecks of the original TSPC flip-flops. The logic-related transistors in these new flip-flops are purely N-type in both N and P-latches. This gives an additional speed advantage to this kind of circuits since the P-block that becomes a speed bottleneck is removed.

CHAPTER 3

A New Area-Power Efficient Split-Output TSPC CMOS Latch for High-Speed VLSI Applications

3.1 Introduction

The need for higher speeds at low power consumption has defined the research interest of digital VLSI design. This need has become very important with the latest advances in mobile devices such as the Personal Digital Assistants (PDAs) and mobile phones. A low power supply voltage is useful for such battery-powered devices, since the number of cells in the battery can be reduced. This will result in reduced weight of the devices as well extending the lifetime of the battery.

The true single-phase clock CMOS circuit technique uses only one clock signal that is never inverted and fits both static and dynamic circuits. There are several benefits with this technique, as the elimination of clock skew, the clock signal may be generated off-chip with significant savings in chip area and power consumption. A single global clock signal needs to be generated and distributed thus simplifying the design [8]. A few drawbacks are the need for two extra transistors in each stage, a clock delay problem that can be eliminated as long as we keep this delay less than the gate delay and thus improving the reliability [8]. P-blocks of a flip-flop become a speed bottleneck, since their pre-charged nodes consume power.

In this chapter, a new P-type split-output TSPC latch is introduced, and compared to existing P-type split-output TSPC latches with respect to area, power consumption, and

robustness at high speeds. Particular attention is dedicated to reducing the clock feed-through and thus, making the new latch more robust. The new latch also reduces the area used and the power consumed and therefore, appears to be more suitable for low-power and high-speed applications.

All four latches studied in this paper have arbitrary been set at a speed of 625 MHz, using a 3.3 V power supply, in a 0.5- μm CMOS process. The speed of 625 MHz is comparable to the speed of 2-3 GHz at 0.18- μm process technology. The output was loaded with a 100fF capacitor, in order to try and simulate a next stage load to the latch. For the simulation, HSPICE was used with level 3 models for the NMOS and PMOS transistors.

This chapter is structured as follows. In section 3.2, two already known P-type split-output TSPC latches are constructed, simulated, and compared. In section 3.3 a recent P-type split-output TSPC latch is constructed and simulated. This latch was extracted from its counterpart N-type, used in a flip-flop that was introduced by Yuan et al. in 1997 [13]. In the same section the new P-type split-output latch is introduced, simulated, and compared with the other latches. Section 3.4 explains the operation of the new N-type split-output TSPC latch. In section 3.5 the results of all four latches are summarized in a tabular format. Finally, conclusions and recommendations will be presented in section 3.6.

3.2 Original TSPC Split-Output Latches

Since lowering the power supply voltage on a circuit will reduce the speed of the gates in that circuit, achieving high speeds with a 3.3 V power supply was challenging.

In order to achieve high speeds, the width of the transistors was increased through careful optimization, and therefore the delay of those transistors was decreased. The switching speed of a CMOS gate is limited by the time taken to charge and discharge the load capacitance C_L . Therefore, in order to achieve high speeds the timing uncertainty of a transistor through the threshold region was minimized. This was achieved by making the rise, and fall times of the square clock and input digital signals fast enough, in this case 120 ps.

3.2.1 Original P-split-output latch, Yuan89

In 1989, Yuan et al. [8] introduced the True Single Phase Clocked (TSPC) latches. One type of the new proposed latches, the split-output latches, has only one of their transistors controlled by the clock. This implies half the clock load and therefore, a better performance [8]. The P-split-output latch is shown in Fig. 3.1. When the clocked controlled transistor is turned on, the split outputs can be used to drive the next stage like an inverter. The drawback of the Yuan89 split-output latch is that not all node voltages have a full voltage swing. In Fig. 3.1, transistor P3 has a maximum source-gate voltage of $(V_{SS} - |V_{Tp}|)$. This results in a lower current flow in the output transistor P3 than a full voltage swing would produce. Therefore the driving capability for the output circuit is reduced.

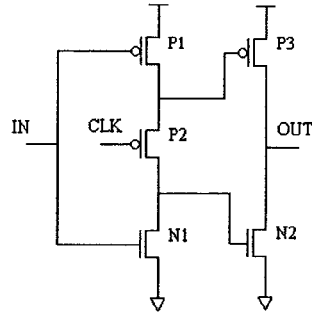


Fig. 3.1. P-type split-output latch, Yuan89.

For the simulation of Yuan89, and the subsequent split-output latches, the widths of the transistors were optimized until the speed of 625 MHz was achieved. Then, we kept that speed constant in all latches and compared them with respect to area, power consumption, and robustness. In order to decrease the delay of the latch, which improves reliability, the sizing of the transistors should be carefully designed. Making a PMOS transistor too large, both slows down the gate, and increases the capacitive load of the clock line.

The width sizes used in the transistors of Fig. 3.1 are: $W_{P1} = 15.5 \mu\text{m}$, $W_{P2} = 51 \mu\text{m}$, $W_{P3} = 78 \mu\text{m}$, $W_{N1} = 33 \mu\text{m}$, $W_{N2} = 6 \mu\text{m}$; the width length, W_L , for all transistors is $0.6 \mu\text{m}$. The total area for the latch was $\sum W_i L_i = 110.1 (\mu\text{m})^2$, and C_{ox} , the gate capacitance per unit area for the $0.5\text{-}\mu\text{m}$ process, is 3.60 mF/m^2 . Therefore, C_g , the gate capacitance, can be found by using the relationship $C_g = C_{\text{ox}} W L$ which gives us $C_g = 396.36 \text{ fF}$. Adding C_g to $C_L = 100 \text{ fF}$, the load capacitance, results in a total capacitance of $C_{\text{Tot}} = 496.36 \text{ fF}$. In order to find the power dissipated by the Yuan89 latch, we used the relationship, $P = C_{\text{Tot}} V_{\text{DD}}^2 f_c$, where $V_{\text{DD}} = 3.3 \text{ V}$ and $f_c = 625 \text{ MHz}$ in our case. The power consumed by Yuan89 split-output latch was $P = 3.378 \text{ mW}$. The simulated output is shown in Fig. 3.2.

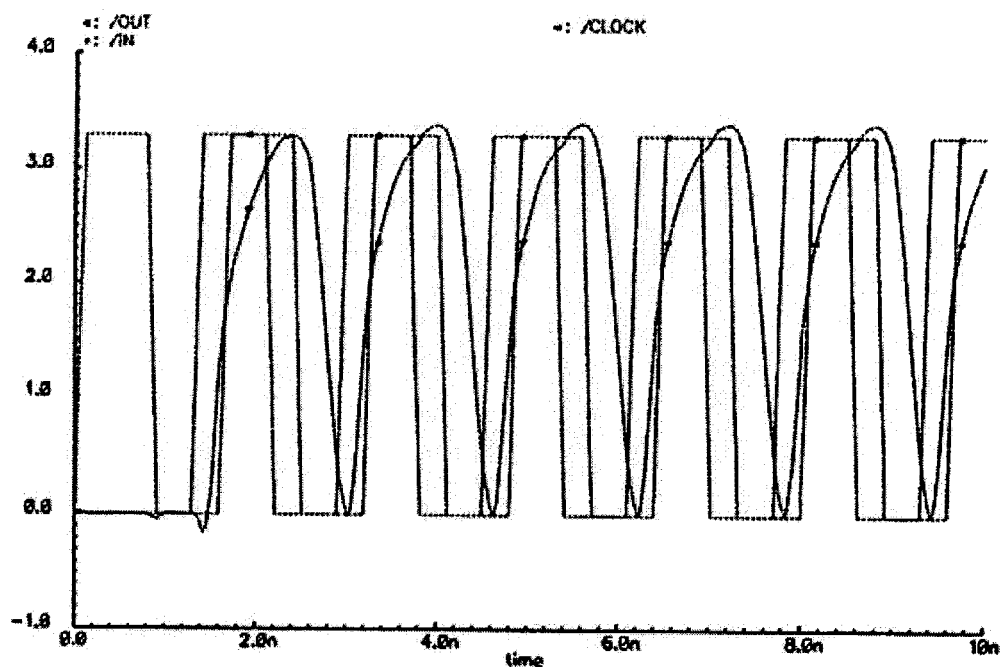


Fig. 3.2. Output waveform for Yuan89 latch.

The output signal, after the first transition, rises substantially above the supply voltage for a negative going edge of the clock. This clock feed-through, which will denote V_{Fth} , reflects the effect of the pre-charging of the intermediate nodes, being capacitively coupled to the output node. Clock feed-through might cause the normally reverse-biased junction diodes to become forward-biased [5]. The forward biasing of the diodes causes electron injection into the substrate, which can be collected by a nearby high impedance node in the high state, eventually resulting in faulty operation [5]. For the Yuan89 latch, $V_{Fth} = 89$ mV.

3.2.2 Modified P-split-output latch, Ghan94

In 1994, Ghannoum et al. proposed a modified split-output latch, which minimizes the distortion in the internal dynamic nodes [14]. The improvement of the output voltage

level was achieved by the addition of the feedback transistor N3. In Fig. 3.3, the P-split-output version of Ghan94 latch is shown.

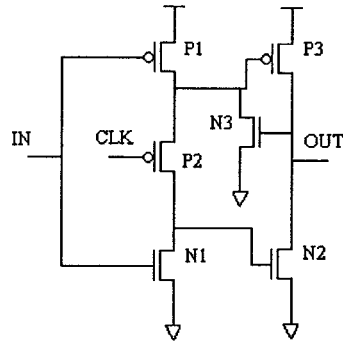


Fig. 3.3. P-type split-output latch, Ghan94.

In order to achieve a speed of 625 MHz with the Ghan94 latch, the following transistor width sizes were used in Fig. 3.3: $W_{P1} = 13 \mu\text{m}$, $W_{P2} = 24 \mu\text{m}$, $W_{P3} = 35 \mu\text{m}$, $W_{N1} = 20 \mu\text{m}$, $W_{N2} = 19 \mu\text{m}$, $W_{N3} = 2.4 \mu\text{m}$; and W_L for all transistors is $0.6 \mu\text{m}$. The total area for the latch was $\Sigma W_i L_i = 68.04 (\mu\text{m})^2$, with $C_g = 244.944 \text{ fF}$. Adding C_g to $C_L = 100 \text{ fF}$, the load capacitance, results in a total capacitance of $C_{\text{Tot}} = 344.944 \text{ fF}$. The power consumed by Ghan94 split-output latch was $P = 2.348 \text{ mW}$. The N3 transistor is a minimum size transistor. The simulated output is shown in Fig. 3.4.

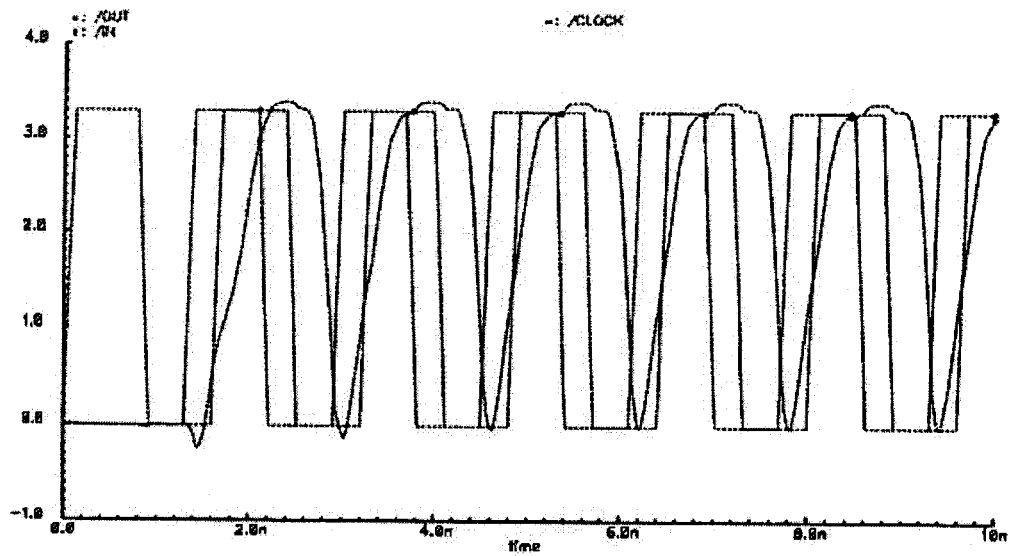


Fig. 3.4. Output waveform for Ghan94 latch.

Ghan94 latch achieved the same speed, of 625 MHz, with the Yuan89 latch, while using 42.06 μm less area and consuming 1.03 mW less power. The clock feed-through of Ghan94 latch though was a bit higher, with a value of $V_{\text{Fth}} = 93$ mV. This is 4 mV higher than the corresponding clock feed-through of Yuan89 P-type latch. Another interesting point that was found from simulations is that, this latch did not minimize the distortion in the internal dynamic nodes at high speeds, but actually was worse than Yuan89 latch at 625 MHz.

3.3 Recent P-Split-Output Latches

In this section we will discuss two newer p-split-output TSCP latches. One was developed in 1997 by J. Yuan and C. Svensson and the new one was developed by B. Pontikakis and M. Nekili in 2001.

3.3.1 Improved P-split-output latch, Yuan97

In 1997, Yuan et al. [13], proposed new single-clock latches and flip-flops with improved speed and power savings. In one of the new proposed flip-flops, an N-type split-output latch was used, Yuan97 latch, which uses an additional clocked transistor. The P-type split-output latch is shown in Fig. 3.5.

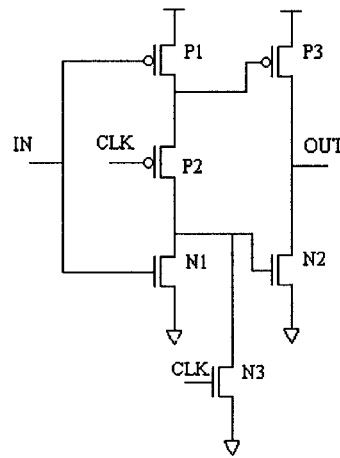


Fig. 3.5. P-type split-output latch, Yuan97.

Even though it was suggested that the size of the input PMOS transistor P1 can be minimized, as it is only used for preventing charge sharing [13], in order to achieve higher speeds through optimization, its size had to be increased.

In order to achieve the speed of 625 MHz with the Yuan97 latch, the following transistor width sizes were used in Fig. 3.5: $W_{P1} = 5 \mu\text{m}$, $W_{P2} = 35 \mu\text{m}$, $W_{P3} = 52 \mu\text{m}$, $W_{N1} = 21.5 \mu\text{m}$, $W_{N2} = 21 \mu\text{m}$, $W_{N3} = 2.4 \mu\text{m}$; and W_L for all transistors is $0.6 \mu\text{m}$. The total area for the latch was $\sum W_i L_i = 82.14 (\mu\text{m})^2$, with $C_g = 295.704 \text{ fF}$. Adding C_g to $C_L = 100 \text{ fF}$, the load capacitance, results in a total capacitance of $C_{\text{Tot}} = 395.704 \text{ fF}$. The

power consumed by Yuan97 latch was $P = 2.693$ mW. The N3 transistor is a minimum size transistor. The output of Yuan97 latch was very similar to Yuan89 latch.

Yuan97 latch achieved the same speed, of 625 MHz, with the previous latches, while using $27.96 \mu\text{m}$ less area and consuming 0.685 mW less power than the Yuan89 latch. Ghan94 latch has better results though considering area used and power dissipated. Ghan94 latch uses $14.1 \mu\text{m}$ of less area and consumes 0.345 mW less power than the Yuan97 latch. The clock feed-through of Yuan97 latch was a bit higher, with a value of $V_{\text{Fth}} = 100$ mV. This is 11 mV higher than the corresponding clock feed-through of Yuan89 P-type split-output latch and 7 mV higher than the Ghan94 latch. The full swing of the internal nodes was also worse than Ghan94 latch.

3.3.2 New P-split-output latch, Pontik2001

In order to increase the circuit robustness we tried to reduce the clock feedthrough, V_{Fth} . For the P-split-output latch, this was done with the introduction of the N-type feedback transistor, N3, in the intermediate nodes. By connecting the source of transistor N3 to the intermediate node, instead of connecting it to the ground, as with Ghan94 latch, we are able to absorb part of that clock feed-through before it reaches the output. This is done by charge sharing between the gates of the output transistors N2 and P3, which increases voltage at the gate of P3, thus reducing its driving capability, and bringing the output voltage closer to V_{DD} (i.e. lowering V_{Fth}). Voltage feed-through calls for charging and discharging of the intermediate node capacitances, thus consuming power. Therefore, by minimizing V_{Fth} , we were also able to decrease the power consumption of the circuit.

Since the feedback transistor is a minimum size transistor, we were able to optimize the circuit efficiently, and therefore save in area and power consumption. This was possible since, by keeping one of the transistors a minimum size transistor, we had only five transistors to optimize. We were also able to keep input transistor P1 close to minimum size transistor, for the technology used. Pontik2001 P-split-output latch is shown in Fig. 3.6.

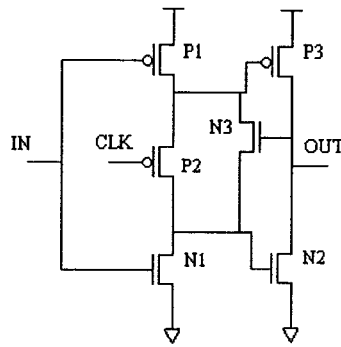


Fig. 3.6. P-type split-output latch, Pontik2001.

In order to achieve the speed of 625 MHz with the Pontik2001 latch, the following transistor width sizes were used in Fig. 3.6: $W_{P1} = 5 \mu\text{m}$, $W_{P2} = 24 \mu\text{m}$, $W_{P3} = 35 \mu\text{m}$, $W_{N1} = 20 \mu\text{m}$, $W_{N2} = 19 \mu\text{m}$, $W_{N3} = 2.4 \mu\text{m}$; and W_L for all transistors is $0.6 \mu\text{m}$. The total area for the latch was $\Sigma W_i L_i = 63.24 (\mu\text{m})^2$, with $C_g = 227.664 \text{ fF}$. Adding C_g to $C_L = 100 \text{ fF}$, the load capacitance, results in a total capacitance of $C_{\text{Tot}} = 327.664 \text{ fF}$. The power consumed by Pontik2001 latch was $P = 2.230 \text{ mW}$. The N3 transistor is a minimum size transistor. The simulated output is shown in Fig. 3.7.

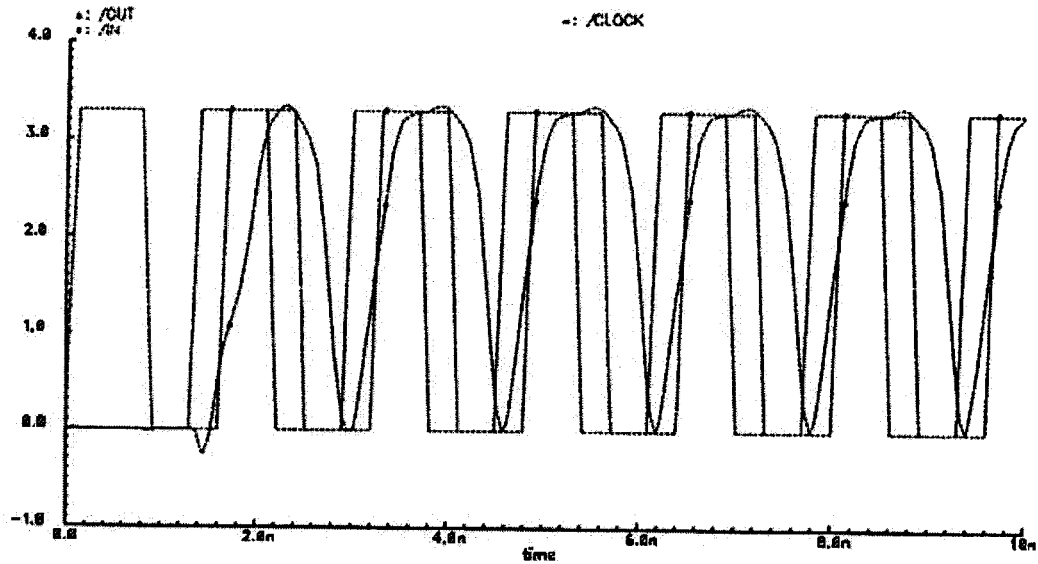


Fig. 3.7 Output Waveform for Pontik2001 latch.

Pontik2001 latch achieved the same speed, of 625 MHz, with the previous latches, while using 4.8 μm less area and consuming 0.118 mW less power, than Ghan94 latch. The clock feed-through of Pontik2001 latch was also the lowest of all the latches, with a value of $V_{\text{Fth}} = 50$ mV. This is 39 mV lower than the corresponding clock feed-through in Yuan89 latch. At this high speed of 625 MHz, the internal nodes of Pontik2001 latch also did not achieve full swing.

The widths of all transistors for the four latches are summarized in Table 3.1 along with the total capacitance at the load, the number of transistors and the number of clocked transistors for each latch.

TABLE 3.1**Transistor Sizes, Number Of Transistors and Clocked Transistors, and Total Capacitance**

Table 3.1	Yuan89	Ghan94	Yuan97	Pontik2001
P1 (μm)	15.5	13	5	5
P2 (μm)	51	24	35	24
P3 (μm)	78	35	52	35
N1 (μm)	33	20	21.5	20
N2 (μm)	6	19	21	19
N3 (μm)	N/A	2.4	2.4	2.4
N_{tr}	5	6	6	6
N_{ctr}	1	1	2	1
C_{Tot} (fF)	496.36	344.944	395.704	327.664

As seen from the Table 3.1, Pontik2001 P-type split-output latch has the smallest total capacitance.

3.4 Operation of the New Split-Output Latch

In this section, we will describe the operation of the N-type new split-output shown in Fig. 3.8. We will consider four cases, case I, a low-to-high transition of the input when clock is low; case II, a high-to-low transition of the input when clock is high; case III, a low-to-high transition of the input when clock is high; and case IV, a high-to-low transition of the input when clock is low.

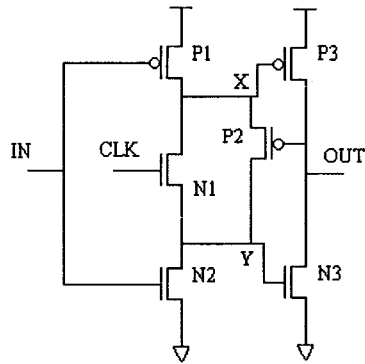


Fig. 3.8. N-type split-output latch, Pontik2001.

3.4.1 Case I: Low-to-high transition of the input when clock is low

Initially, when clock, CLK, is low, N1 is switched OFF and internal node X is high. When the input, IN, goes high, the internal node X is pulled down to low through transistors N1 and N2 and at the same time transistor P3 is turned ON. Therefore, the output, OUT, is pulled high through transistor P3. Transistors P2 and N3 are staying OFF. The activity ratio, α , is 0.5 for transistors P1, P3, N1, is 1 for transistor N2, and is between $0 \rightarrow 0.5$ for P2, N3, depending of the previous state of the output.

3.4.2 Case II: High-to-low transition of the input when clock is high

Clock, CLK, high, causes transistor N1 to be ON. If input, IN, is high, then transistor N2 is also ON. The internal node X is pulled down through N2 and N1. Therefore, transistor P3 is ON and output, OUT, is pulled up high through P2.

If the input goes low then N2 is turned OFF and P1 is turned ON. This results in intermediate node X to be pulled up through transistor P1 and intermediate node Y to be pulled up through transistors N1, and P1. Since transistor N1 is not a perfect switch when transmits a high value, we expect node Y not to have a good high value either. Y being

high turns transistor N3 ON, which results in output, OUT, being pulled down to low through N3. After output, OUT, has reached a low value, transistor P2 will be turned ON which in turn will pull up node Y to high through transistors P2 and P1 thus, providing a better high value for that node. When clock, CLK, goes low it turns transistor N2 OFF. The activity ratio, α , is 0.5 for transistors P1, P2, P3, N2, and N3, and is 1 for transistor N1.

3.4.3 Case III: Low-to-high transition of the input when clock is high

Initially, clock high will turn ON transistor N1. If input, IN, is low then transistor P1 will be ON and therefore, intermediate node X will be pulled up high through P1 and node Y will be pulled up high through P1 and N1 transistors. This will turn ON transistor N3 and the output, OUT, will be pulled down through N3, which will turn ON eventually transistor P2.

When the input, IN, goes high P1 is turned OFF, N2 is turned ON and node Y is pulled down through N2 while node X is pulled down through N1 and N2. This action turns OFF transistor N3 and turns ON transistor P3. Output, OUT, is pulled up high through P3. When OUT is high, transistor P2 is turned OFF. When clock, CLK, goes low, N1 is turned OFF. The activity ratio, α , is 0.5 for transistors P1, P2, P3, N2, and N3, and is 1 for transistor N1.

3.4.4 CASE IV: High-to-low transition of the input when clock is low

Clock, CLK, low, causes transistor N1 to be OFF. If input, IN, is low then transistor P1 is turned ON and intermediate node X is pulled up high through P1, while node Y holds

its previous value. When input, IN, goes high turns P1 OFF and turns N2 ON, which pulls down low intermediate node Y. The output still holds its previous value.

Clock, CLK, going high turns transistor N1 ON and pulls down node X to low through transistors N1 and N2, which turns ON transistor P3. This in turn pulls up the voltage at output, OUT, to high. The activity ratio, α , is 0.5 for transistors P1, P3, and N1, is 1 for transistor N2, and is between $0 \rightarrow 0.5$ for P2, N3, depending of the previous state of the output.

3.5 Results and Comparative Study

From the simulations, it was found that it was difficult to optimize Yuan89 and Yuan97 latches, in order to achieve high speeds. The difficulty is associated with making the output follow the first input transition in full swing. This can be noticed by looking at the first transition of the output in all waveforms. Therefore, it is believed that higher speeds can be achieved more easily with Pontik2001 and Ghan94 latches.

The simulation results obtained for the four different P-type split-output latches are shown in Table 3.2. All simulations were performed in a 0.5- μm CMOS process, using 3.3 V power supply, and a 100 fF capacitive load. The frequency f_c , for all simulations is 625 MHz. The $(A \cdot P)/f_c$ in the Table 1 is in $(\mu\text{m})^2$ (mW) / MHz units.

TABLE 3.2
Area, Power, and Robustness Characteristics

Table 3.2	Yuan89	Ghan94	Yuan97	Pontik2001
$A (\mu\text{m})^2$	110.1	68.04	82.14	63.24
P (mW)	3.378	2.348	2.693	2.230
$(A \cdot P) / f_c$	0.595	0.256	0.354	0.226
V_{Fth} (mV)	89	93	100	50

As seen from the Table 3.2, Pontik2001 P-type split-output latch, uses the least area, consumes the least power and has the least clock feed-through voltage among all latches.

3.6 Conclusion

In this chapter, a new split-output latch was introduced and its P-type compared with three existing P-type split-output latches. The comparison criteria were area usage, power consumption, and clock feed-through voltage, at the high frequency of 625 MHz and low voltage of 3.3 V. From the comparative analysis, it was found that our new latch significantly increases the robustness due to clock feed-through, uses the least transistor area, and consumes the least power, than the existing split-output latches. Therefore, among all latches, our new latch appears to be the most suitable split-output latch for high-speed, low-power applications.

CHAPTER 4

A Novel Double Edge-Triggered Pulse-Clocked TSPC D Flip-Flop for High-Performance and Low-Power VLSI Design Applications

4.1 Introduction

The latest advances in mobile battery-powered devices such as the Personal Digital Assistants and mobile phones have set new goals in digital VLSI design. These goals include the need for high-speed digital circuits at low power consumption. Flip-flops and latches are used as the storage elements in a clocking system. A careful design of storage elements will contribute in the increased performance and reduced power consumption of a VLSI system. True Single Phase Clocking (TSPC) has successfully contributed to the performance improvement, reliability, and power consumption in digital VLSI design. Double edge-triggered flip-flops have been demonstrated to be suitable designs for high-speed and low power VLSI applications.

A new pulse triggered double edge-triggered D-flip-flop (PDET) using the TSPC technique [8] is proposed in this chapter. The total transistor count and the clocked transistors are significantly reduced compared to previously reported double-edge triggered flip-flops. The PDET operates at high speeds while the power consumption has been kept low. The Area-Period-Power product has also been reduced significantly. That is due to the reduction of total capacitances. The pulse train generation circuitry is external to the flip-flop and therefore can be used to feed multiple double edge-triggered flip-flops and other devices.

Simulations have been performed using HSPICE and a 3.3 V power supply in a 0.5- μm CMOS process. For PDET simulations are performed on netlists extracted from layout. The output is loaded with a 100 fF capacitor, in order to try and simulate a next stage load to the flip-flop.

This chapter is constructed as follows. In section 4.2, the double edge-triggered pulsed-clock generator is discussed. In section 4.3, three already known TSPC double edge-triggered flip-flops and PDET discussed. In section 4.4, simulations of the flip-flops are performed and the results are compared with the new PDET. Finally, the conclusions and recommendations are presented in section 4.5.

4.2 Pulse Generation Circuitry

The pulse generation circuit uses a XNOR block, with only three transistors, to sample the signal on the positive and negative edge of the input square wave together with a delay of that clock. The delay is produced using an N-type TSPC split-output latch that is proposed in [15] while keeping the clock constant at V_{DD} and using an inverter at the output. A buffer composed of two inverter cells, with the same driving capability, was used as the signal driver at the output of the XNOR block. The circuit is depicted in Fig. 4.1. The circuit takes as an input a square wave clock signal with 50% duty cycle and generates an output of short pulse train. In order to have a double edge-triggered flip-flop, the short pulse train is produced on the positive and negative edge of the input clock as shown in Fig. 4.2.

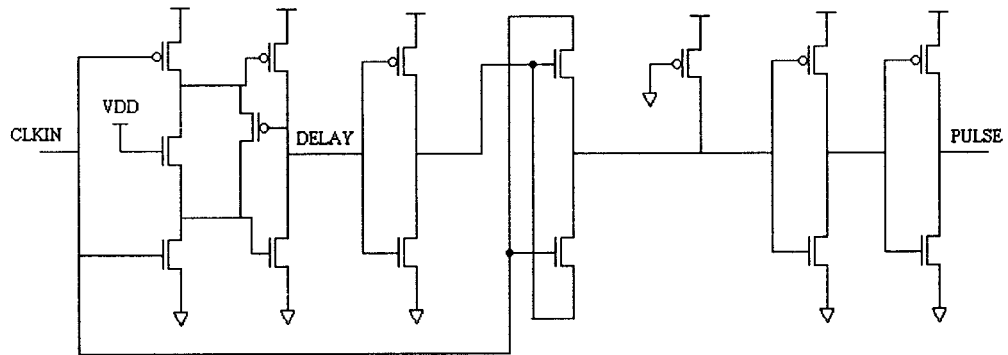


Fig. 4.1. Double edge-triggered pulsed-clock generator.

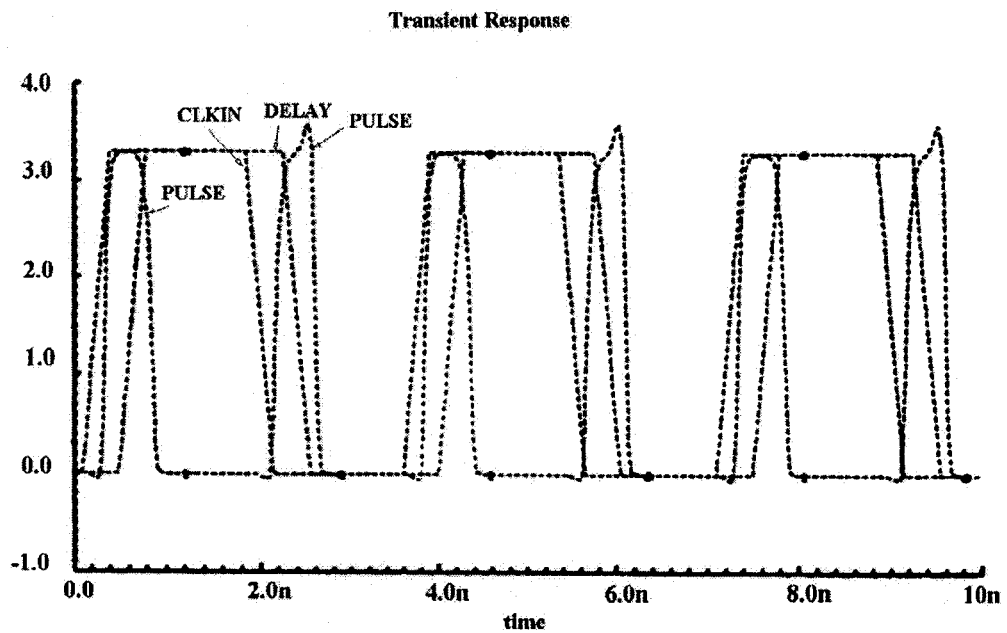


Fig. 4.2. Generated pulses on both edges of the square clock.

As seen in Fig. 4.1 only fifteen transistors are used for the circuit. The width and length of all transistors were set arbitrarily at $W = 2.4 \mu\text{m}$, $L = 0.6 \mu\text{m}$, respectively.

4.3 TSPC Double Edge-Triggered Flip-Flops

Previous double edge-triggered flip-flops were constructed using two complementary latches in parallel [16], [17]. One latch was reacting on the positive edge of the square clock pulse and the other was reacting at the negative edge. Then the outputs of the two latches were combined into a single output using a merging circuit. Within the merging circuit, when the output of one of the circuits is a high-impedance node, it lets the other circuit decide the output value and vice-versa.

Fig. 4.3 shows two double edge-triggered flip-flops that were introduced by Afghahi and Yuan [16]. We will denote them Afghahi91a and Afghahi91b respectively, as shown in the figure. Both circuits use twenty transistors in total. The main difference of the two circuits is the merging circuit. For Afghahi91b flip-flop the merging circuit is a NAND gate, which results in less clock loading [16].

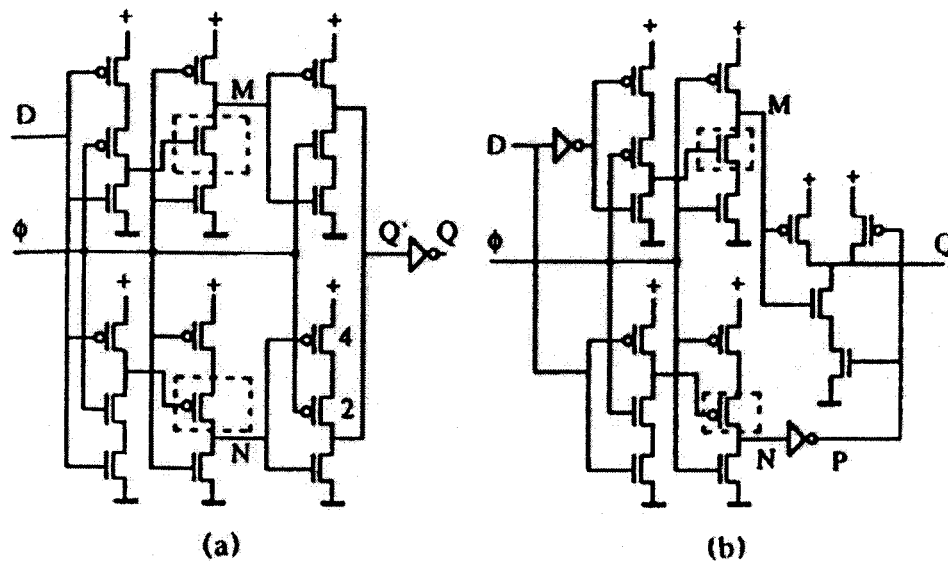


Fig. 4.3. Two double edge-triggered flip-flops,
(a) Afghahi91a, (b) Afghahi91b [16].

Another double edge-triggered flip-flop was introduced by Wang [17], which uses only eighteen transistors. The original circuit is depicted in Fig. 4.4, but we added an extra inverter at the output to obtain a true logic and not the complemented logic. We also added a 100 fF load capacitor at the output.

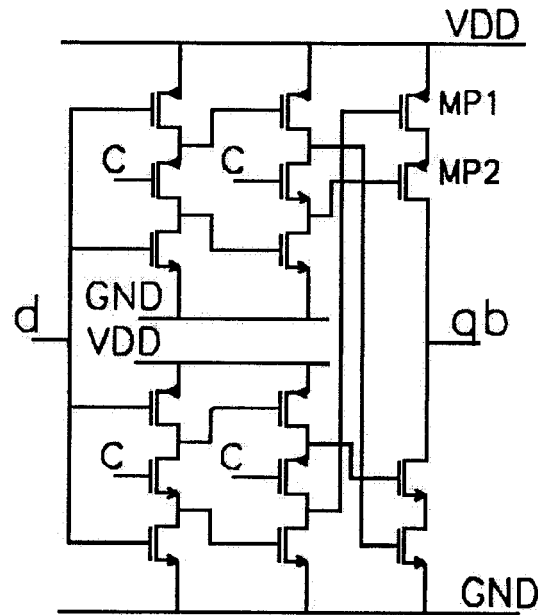


Fig. 4.4. Double edge-triggered flip-flop, Wang97 [17].

We are proposing a novel double edge-triggered pulse-clocked TSPC flip-flop (PDET) that uses only eight transistors. PDET is based on the TSPC split-output D-latch that Pontikakis and Nekili introduced in [15]. The N-type of this circuit that is used for our double edge-triggered flip-flop is depicted in Fig. 4.5. An inverter has been added to the output of the original D latch in order to obtain true logic and not complementary logic.

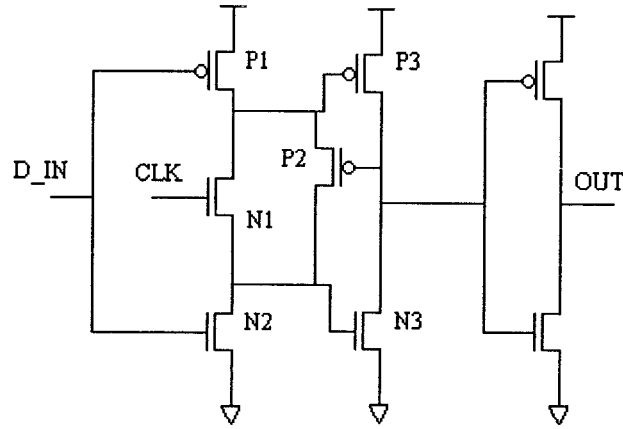


Fig. 4.5. Proposed double edge-triggered TSPC D-flip-flop (PDET).

The simple D latch circuit shown in Fig. 4.5 when applied with the short pulse train clock generated by the pulse-clocked generator of Fig. 4.1, acts like a double edge-triggered flip-flop and is called, a pulse-clocked double edge-triggered D-flip-flop (PDET).

From Fig. 4.5 we see that the circuit uses only eight transistors compared to twenty transistors used in Afghahi91a and Afghahi91b double edge-triggered flip-flops and compared to eighteen transistors used in Wang97 circuit. This is a 60% reduction compared to the number of transistors used in the Afghahi91a and Afghahi91b circuits and around 56% reduction compared to the number of transistors used in Wang97 circuit.

The pulsed-clock generator circuit is not an area overhead since it is external to the circuit. Therefore, the pulse-clock generator can be used to clock different latches, flip-flops, and other circuits in the clock distribution network.

4.4 Comparative Study of Double Edge-Triggered Flip-Flops

For our simulations, we used the same size for all transistors, $W = 2.4 \mu\text{m}$ and $L = 0.6 \mu\text{m}$ and a load capacitor, C_L , of 100 fF. The maximum frequency, f_c , achieved in Afghahi91a and Afghahi91b circuits were 277.77 MHz and 263.16 MHz, respectively.

Simulation results for Afghahi91a double edge-triggered flip-flop of Fig. 4.3(a) are depicted in Fig. 4.6. Afghahi91b simulation results were similar. The total area of the Afghahi91a flip-flop was $\Sigma W_i L_i = 28.8 (\mu\text{m})^2$, and the gate capacitance per unit area for the 0.5- μm process, is $C_{ox} = 3.60 \text{ mF/m}^2$. The total gate capacitance, C_g , can be found by the relationship $C_g = C_{ox} \Sigma W_i L_i$ which gives us $C_g = 103.68 \text{ fF}$. Adding C_g to the load capacitance $C_L = 100 \text{ fF}$, results in a total capacitance of $C_{Tot} = 203.68 \text{ fF}$. In order to find the power dissipated by the Afghahi91a flip-flop, we used the relationship, $P = C_{Tot} V_{DD}^2 f_c$, where $V_{DD} = 3.3 \text{ V}$ and $f_c = 277.77 \text{ MHz}$ in our case. The power consumed by Afghahi91a flip-flop was $P = 0.616 \text{ mW}$.

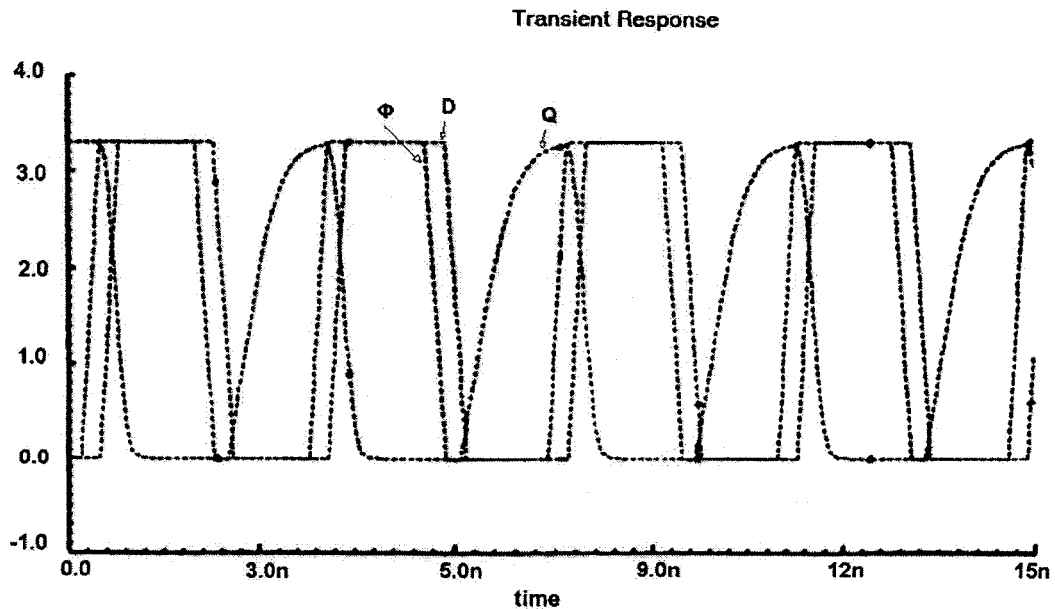


Fig. 4.6. Simulation results, Afghahi91a.

Using the same transistor sizes and same formulas as we used with Afghahi91a circuit, we were able to calculate the total area, capacitance, and power dissipation for Afghahi91b flip-flop of Fig. 4.3(b). For Afghahi91b $\Sigma W_i L_i = 28.8 (\mu\text{m})^2$, $f_c = 263.16$ MHz, $C_g = 103.68$ fF, $C_{\text{Tot}} = 203.68$ fF, and $P = 0.584$ mW. Since only the frequency f_c is different between the two flip-flops, we can conclude that the lower power consumption of Afghahi91b flip-flop is the result of that lower frequency.

After simulation for Wang97 circuit of Fig. 4.4, we obtained a maximum frequency of $f_c = 158.73$ MHz. Using the same formulas as with Afghahi91a flip-flop, the following results were obtained. $\Sigma W_i L_i = 25.92 (\mu\text{m})^2$, $C_{\text{Tot}} = 193.31$ fF, and $P = 0.334$ mW. The major contribution of this low power consumption was due to the low maximum frequency that this circuit achieved.

A simulation was performed for PDET circuit of Fig. 4.5 using the same sizes for all transistors, $W = 2.4 \mu\text{m}$ and $L = 0.6 \mu\text{m}$, except for transistor P1 for which $W = 7.2 \mu\text{m}$ and $L = 0.6 \mu\text{m}$ were used. The simulation was done using HSPICE in a $0.5\text{-}\mu\text{m}$ CMOS process. The power supply used is $V_{\text{DD}} = 3.3$ V and the results of the simulation are shown in Fig. 7. As seen in Fig. 4.7, when clocked by the short pulse train generated by the pulsed-clock generator of Fig. 4.1, the circuit does actually behave as a double edge-triggered flip-flop.

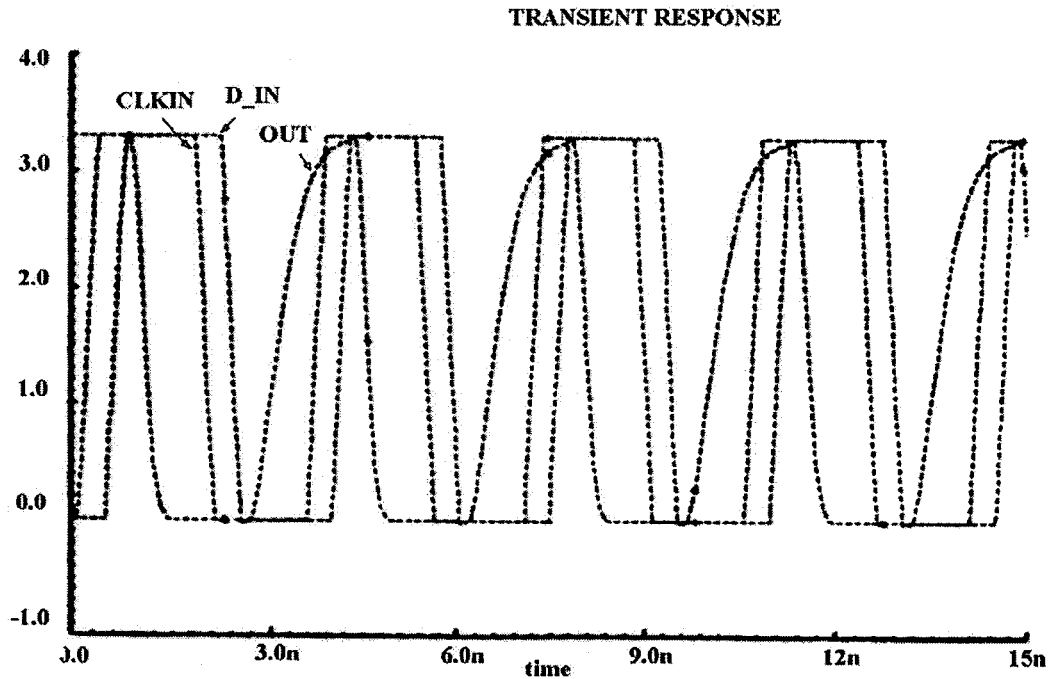


Fig. 4.7 Simulation output waveform of PDET.

After simulation on netlists extracted from layout, the maximum frequency achieved by PDET was $f_c = 285.71$ MHz. The layout of the PDET together with the pulse-generator circuitry is shown in Fig. 4.8. This layout is not optimized to maximum density. It is created to extract more accurate parasitic capacitances with simulation after layout. Using the same formulas as with Afghahi91a circuit we obtained the following values for total area used, gate capacitance, total capacitance, and power dissipated in the circuit. $\sum W_i L_i = 14.4 (\mu\text{m})^2$, $C_g = 51.84$ fF, $C_{\text{Tot}} = 151.84$ fF, and $P = 0.472$ mW.

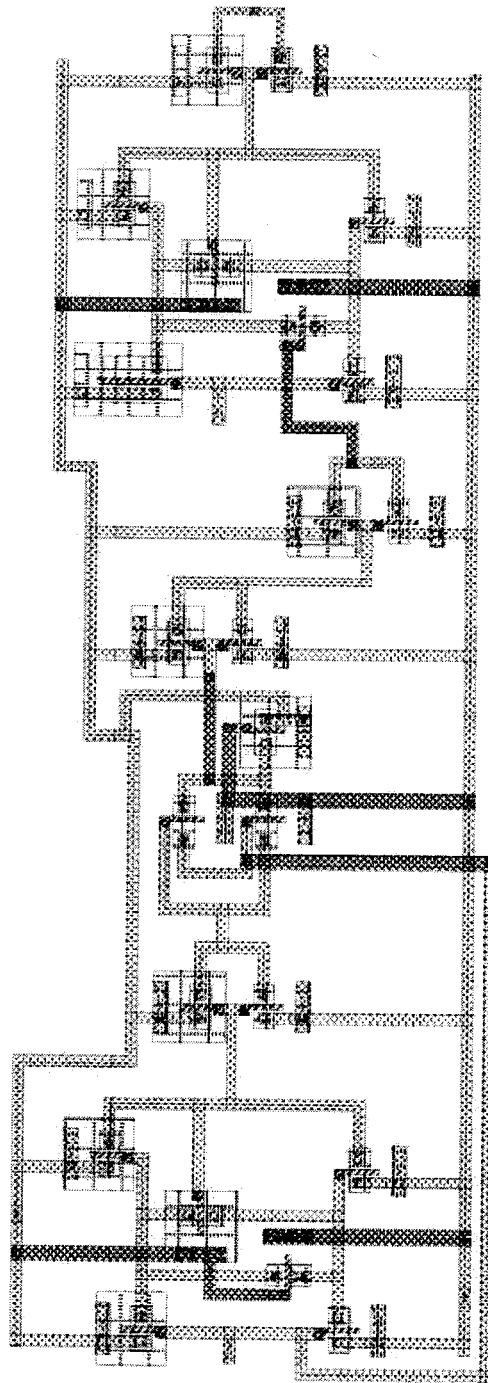


Fig. 4.8 Layout of the double edge-triggered pulse-clocked generator together with PDET.

In Table 4.1, here N_{tr} and N_{ctr} represent the number of transistors and clocked transistors, respectively, some of the characteristics of the double edge-triggered flip-flops are listed. C_{Tot} denotes the total capacitance.

TABLE 4.1
Features of Double Edge-Triggered Flip-Flops

F/F's	N_{tr}	N_{ctr}	C_{Tot} (fF)
Fig.4.3 (a)	20	8	203.68
Fig.4.3 (b)	20	6	203.68
Fig.4.4	18	4	193.31
Fig.4.5	8	1	151.84

The simulation results obtained for the four different double edge-triggered flip-flops are summarized in Table 4.2. All simulations were performed in a 0.5- μm CMOS process, using 3.3 V power supply, and a 100 fF capacitive load. On PDET only, the simulations are performed on netlists extracted from layout. The $(A * P) / f_c$ in Table 4.2 is in $(\mu\text{m})^2 (\text{W}) / \text{MHz}$ units.

As seen from the Table 4.2 the proposed PDET has the best Area-Period-Power product with an improvement of around 63% compared to Afghahi91a circuit of Fig. 4.3(a) to an improvement of around 56% compared to Wang97 circuit of Fig. 4.4.

TABLE 4.2**Area, Power, Speed Characteristics**

A, P, f_c	Afghahi91a	Afghahi91b	Wang97	PDET
$A (\mu\text{m})^2$	28.80	28.80	25.92	14.40
P (mW)	0.616	0.584	0.334	0.472
f_c (MHz)	277.77	263.16	158.73	285.71
$(A*P) / f_c$	63.86	63.91	54.54	23.79

The reason for that improvement in PDET was the reduction of transistors and the use of only one N-type clocked transistor in the circuit. The total capacitance was reduced as a result of the transistor reduction in the circuit.

4.5 Conclusion

In this chapter, a new double edge-triggered flip-flop was introduced. The proposed double edge-triggered flip-flop is clocked with short pulse train and therefore it is called pulse-clocked double edge-triggered flip-flop (PDET). The PDET has been derived from a TSPC split-output D latch and uses only eight transistors. The proposed PDET can save up to 60% in transistor count and up to 63% in the Area-Speed-Power product using 0.5-

μm CMOS technology. If optimization with respect to geometry is applied it is possible to achieve much higher speeds with the proposed PDET while keeping the power consumption low. It is then concluded that the proposed PDET appears to be the most suitable storage element in high-speed, low-power VLSI applications.

CHAPTER 5

A Four-Bit Shift Right Register Using PDET

5.1 Introduction

In this chapter, in order to show that the pulsed-clocked double-edge triggered (PDET) flip-flop, introduced by B. Pontikakis and M. Nekili in [18], is working correctly, a four-bit shift register was constructed. Synchronous design style is useful for core-based Systems on Chip (SoC) design. In a synchronous design style, data changes based on clock edges only and therefore instructions and data can be easily managed. The use of registers in random logic inside the core as well as at the inputs and outputs of every core as shown in Fig. 5.1 is very useful in managing core-to-core interaction [19]. The use of input and output registers usually creates a wrapper around a core [19].

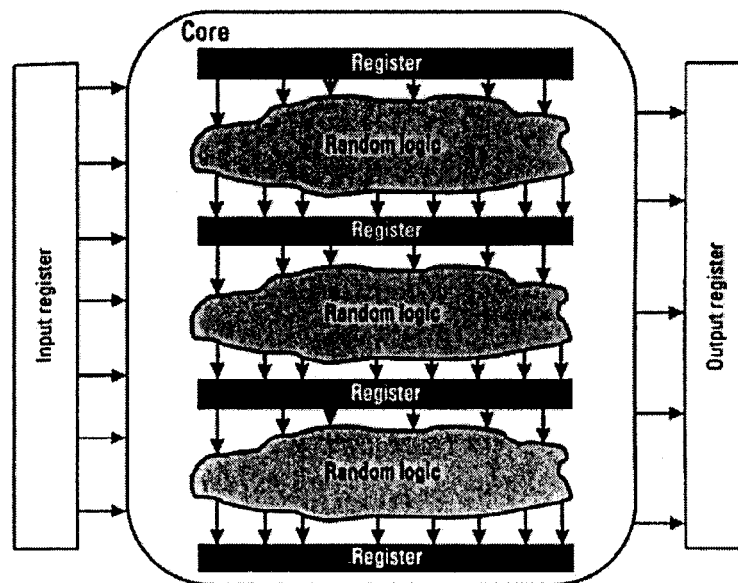


Fig. 5.1. Use of registers for synchronization in core logic and its inputs and outputs [19].

The choice of the PDET flip-flop for implementing a shift register is very promising in the design of wrappers for SoC cores. It is preferable to use flip-flops instead of latches for the design of registers used in wrappers. Latches do not capture data on a clock edge, therefore, it is hard to manage data and instruction since it requires a longer period of an active signal to capture such signals [19].

The rest of the chapter begins, in section 5.2, with the implementation and simulation of the four-bit shift register using PDET flip-flops. Section 5.3 compares the standard TSPC style of implementing shift registers, with the PDET style. Finally, the conclusions of this chapter can be found in Section 5.4.

5.2 Implementation and Simulation of the Shift Register

The shift register was constructed using a 0.5- μm TSMC CMOS process technology at $V_{DD} = 3.3\text{V}$. The rise and fall values of the original square wave clock that fed the pulse-clock generator circuitry were set at 90ps. The shift register is clocked with the PULSE signal, the output signal that the double edge-triggered pulse-clock generator of Fig. 4.1 provided. The shift register uses four stages of PDET flip-flops and two buffers, for a total of 32 transistors with only four transistors being clocked. Therefore, for each bit to be shifted there is an overhead of only one flip-flop stage with just one clocked transistor. In a TSPC design style, we normally need a PMOS and an NMOS latch to shift a bit. Therefore, if we were to use the new TSPC latch that was proposed in [5] with a square clock, we would need approximately twice as many transistors in order to construct a shift register. Such a structure was used by Antaki et. al. [20] to create a two-bit shift register in a split-output TSPC style as illustrated, in Fig. 5.2. As seen from the

figure, 26 transistors were used, including the buffers, for shifting two bits. In agreement with the TSPC design style, the chain alternates between N and P type latches [20]. The two-bit shift register of Fig. 5.2 was implemented in a 0.8 μ m CMOS process technology.

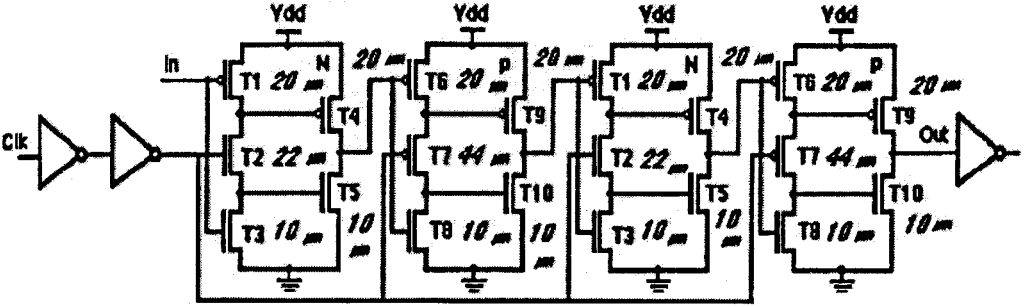


Fig. 5.2 Two-bit shift register in split-output TSPC style [20].

In addition, when using the TSPC design style, an inverter needs to be added to the output stage in order to get the true value of the output signal and not the inverted one. In our design style, we avoid the above overheads and also we avoid the overhead of using PMOS clocked transistors, which represent a bottleneck in a high-performance design due to their lower electron mobility than NMOS transistors. The only disadvantage in our design is the use of buffers after the third and fourth stages. These buffers are not large and therefore, they do not add much to the total area overhead, while at the same time guaranteeing the circuit with better output voltage levels. Using the PDET flip-flop [18], a four-bit shift register was constructed as shown in Fig. 5.3. For each stage, the criteria used are that the high and low levels should not exceed $\pm 5\%$ of V_{DD} and V_{SS} , respectively. The output of the four-bit shift register is shown in Fig. 5.4.

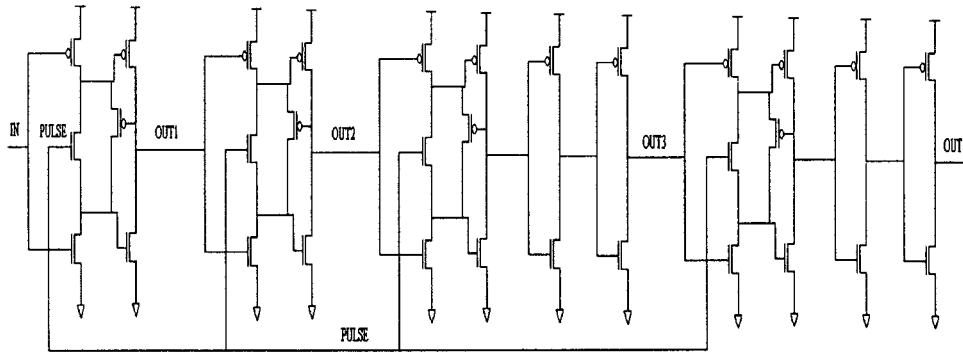


Fig. 5.3. Four-bit shift register, using PDET Flip-Flops [21].

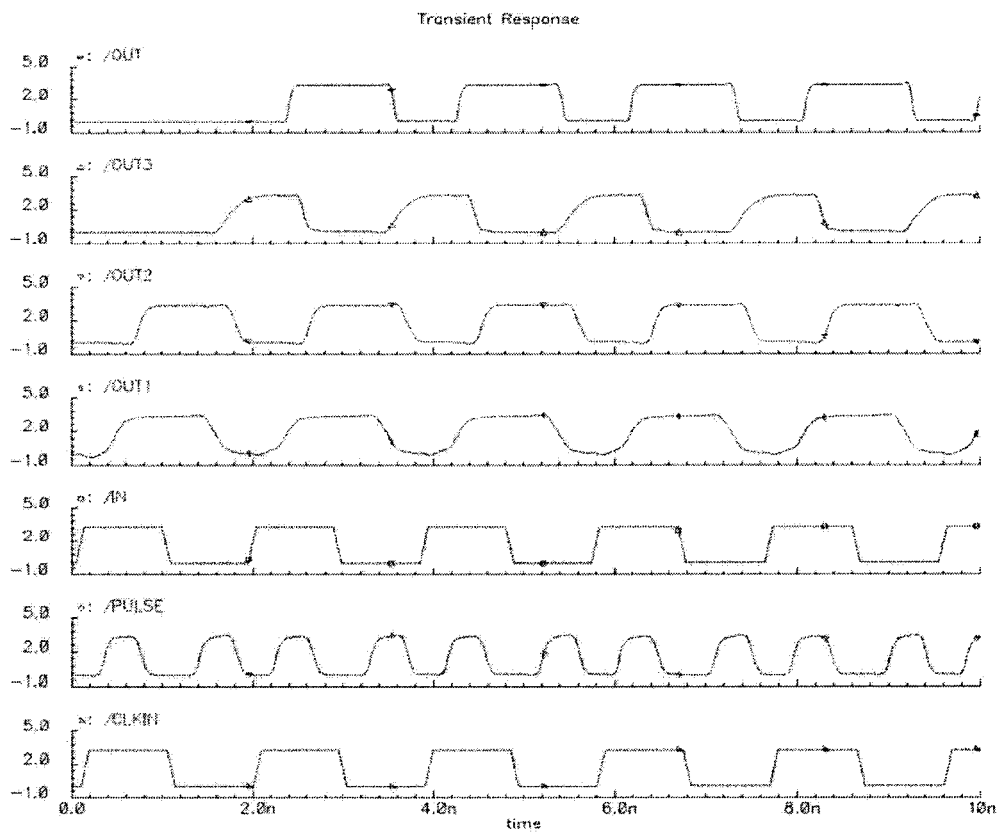


Fig. 5.4. Output waveforms of the four-bit shift register [21].

In Fig. 5.3, CLKIN, is the input of the double edge-triggered pulse-clock generator depicted in Fig. 4.1 and PULSE is the output of that circuit. For our design the circuit of Fig. 4.1 had an area overhead of $76.8 (\mu\text{m})^2$. Remember, that this circuit is not part of the shift register since it can be used to clock several circuits. The shift register of Fig. 5.3 uses PULSE as its clock signal to clock the four different PDET stages. The four-bit shift register had a total area overhead of $78.7 (\mu\text{m})^2$ and consumed 1.7mW of power while it was running at 526 MHz. This power consumption is almost four times as much as the power consumption of a single N-type PDET flip-flop as was shown in Table 4.2. Therefore, we can conclude that, generally, with every extra bit that we need to shift, we will need to add only an extra PDET flip-flop that uses only six transistors, and therefore the power consumption overhead will be only that of the extra flip-flop. However, as we increase the number of PDET we adding loading to the pulse generator circuitry and we need to compensate for the loading by readjusting the area of the pulse generator circuitry. Otherwise, we will modify the duration of the well defined pulse. In addition, the routing of such scheme will be challenging since the pulse generator circuit is external to the shift register.

5.3 Comparison of the Standard TSPC Style and PDET Style Shift Registers

The four-bit shift register using PDET flip-flops, as shown in Fig. 5.3, utilizes 32 transistors with only four N-type clocked transistors, while the two-bit shift register of Fig. 5.2 utilizes 26 transistors, with two N-type and two P-type clocked transistors. Therefore, if we were to construct a four-bit shift register using the standard TSPC style,

we would need 46 transistors in total. That translates into 70% decrease in the number of transistors used to shift four bits.

In addition, with the standard TSPC style, there are 4 P-type and 4 N-type clocked transistors for a total of 8 clocked transistors. With the PDET style, we use only 4 clocked transistors and all of them are of N-type. This translates into 50% reduction in the amount of clocked transistors and 100% reduction in the number of P-type clocked transistors. Therefore, in addition to the considerable reduction of the number of transistors and clocked transistors, the PDET style, manages to avoid the bottleneck of using the slow P-type clocked transistors. The results of the comparison are summarized in Table 5.1, where N_{tr} , N_{ctr} , and N_{P-ctr} represent the number of transistors, number of clock transistors, and number of P-type clock transistors, respectively.

TABLE 5.1

Features of TSPC style four-bit right shift registers

Shift Registers	N_{tr}	N_{ctr}	N_{P-ctr}
Standard TSPC Style	46	8	4
PDET TSPC Style	32	4	0

Another advantage of the PDET style is the fact that it is based on flip-flops compared to latches used in the standard TSPC design. As mentioned in the introduction of this

chapter, flip-flop based registers can more easily manage core-to-core interaction in SoCs while latch based designs are harder to manage.

5.4 Conclusion

In this chapter, we implemented a four-bit right shift register using the PDET flip-flop introduced in chapter 4. Simulations showed that the structure correctly shifted four bits from its input to its output. Compared with the standard TSPC style of implementing shift registers, the PDET style shift-register provides a 70% decrease in the number of transistors used, 50% decrease in the number of clocked transistors used, and 100% reduction the number of P-type clocked transistors used. It is also believed that the PDET structure can obtain much better performance in terms of speed while using less power than the standard TSPC style, since it requires fewer transistors for bit-shifting and also because the PMOS clocked transistors were eliminated. Therefore, the PDET style of shift registers seems to be the right choice of implementation of shift registers for low-power and high-speed application such as in SoCs.

CHAPTER 6

Conclusion and Future Work

In this thesis, new CMOS techniques using true single-phase clocking (TSPC) have been introduced. The advantages of TSPC are compact clock distribution, high speed, logic design flexibility, and robustness to slow clock edges that eliminates the race hazards.

A new split-output TSPC latch was introduced. Our analysis showed that our new latch significantly increases the robustness due to clock feed-through, uses the least transistor area, and consumes the least power, than the existing split-output latches.

In addition, a novel double edge-triggered flip-flop was introduced. The proposed double edge-triggered flip-flop is clocked with a short pulse train and therefore, it is called pulse-clocked double edge-triggered flip-flop (PDET). The PDET has been derived from a new TSPC split-output D latch and uses only eight transistors. The new latch significantly increases the robustness due to clock feedthrough, uses the least amount of transistor area, and consumes the least amount of power, compared to the existing split-output latches. The proposed PDET can save up to 60% in transistor count and up to 63% in the Area-Period-Power product using 0.5- μm CMOS technology. It is possible to achieve much higher speeds with the proposed PDET while keeping the power consumption low, if the geometrical sizes of the transistors were optimized.

Finally, a four-bit right shift register has been implemented using the new PDET double edge-triggered flip-flop. Compared with the standard TSPC style of implementing shift registers, the PDET style shift-register provides a 70% decrease in the number of transistors used, 50% decrease in the number of clocked transistors used, and 100%

reduction in the number of the slow P-type clocked transistors used. It is also believed that the PDET structure can offer a much better performance in terms of speed while using less power than the standard TSPC style.

Among the conclusions of this thesis is that the proposed PDET appears to be the most suitable storage element in high-speed, low-power VLSI applications since PDETs use less area and consume less power than other TSPC flip-flops. In addition, the PDET style of shift registers seems to be the appropriate choice of implementation of the shift registers for low-power and high-speed applications such as in SoCs, since such registers utilize PDET flip-flops and can shift bits using less stages than traditional TSPC registers.

As a future work, testability of TSPC circuits should be considered. A test methodology based on a BIST (Built-In Self-Test) scheme adapted to TSPC design method may be adopted. BIST, offers the possibility to test the chip internally and avoid going through the input and output ports, which is important for the performance of TSPC circuits [22]. A pseudo-random testing scheme based on CA (cellular automata) for TSPC circuits seems as a good choice of implementation, since such a scheme does not possess long feedback loops like the Linear Feedback Shift Registers (LFSRs).

In addition, the fabrication of a chip using PDET flip-flops in deep submicron technology should be considered in order to better understand, test, and prove the functionality of the new structure. Such a work will provide a valuable experience while at the same time observe the effects of process variations in TSPC circuits.

There are open questions in our work. Clock skew between different clock phases is eliminated with the TSPC technique since there is only a single clock signal, but a clock edge might reach two circuits that are communicating at different times. This may happen

because of the long wire interconnections between different PDET stages, which introduce parasitic resistance, capacitance, and inductance. Therefore, a careful timing specification must be established. The setup and hold time restrictions create a forbidden window where the input signal is not allowed to change. This forbidden window needs to be studied carefully for the correct function of high speed shift registers.

Another open question is the performance of our pulse-clock generator circuit. If not designed carefully, it could be a bottleneck in the design of pulse-clocked flip-flops. Moreover, there is room for transistor optimization for a better performance.

One problem that we addressed is the following. TSPC latches are susceptible to internal races when the clock slope is very slow, causing both NMOS and PMOS clocked transistors to be on simultaneously during the transition. By using the PDET flip-flop in the shift-registers this TSPC problem is eliminated, since PDET uses only N-type clocked transistors.

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