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ANALYSIS AND DESIGN OF AN AUXILIARY COMMUTATED FULL BRIDGE DC/DC CONVERTER FOR LOW VOLTAGE AND HIGH CURRENT APPLICATIONS

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ABSTRACT

ANALYSIS AND DESIGN OF AN AUXILIARY COMMUTATED FULL BRIDGE DC/DC CONVERTER FOR LOW VOLTAGE AND HIGH CURRENT APPLICATIONS

DHEERAJ K. JAIN

The analysis and design of an auxiliary commutated Full Bridge dc/dc converter topology including the effect of leakage inductance of the output transformer is presented in this thesis. In applications where the transformer has high turns-ratio between the primary and secondary windings, the value of leakage inductance is relatively high. This high value of leakage inductance, however, is not large enough to achieve the zero voltage switching (ZVS) of the converter over the entire range of operating load conditions, but can be effectively used in minimizing the circulating current of the auxiliary commutation circuit used for achieving ZVS. The operating principle of the circuit is demonstrated, and the steady state analysis is performed. Based on the analysis, a criterion for optimal design is given.

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Dedicated to my parents

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LIST OF ACRONYMS

AC	Alternative Current
DC	Direct Current
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
EMI	Electromagnetic Interference
ESL	Equivalent Series Inductor
ESR	Equivalent Series Resistor
IGBT	Isolated Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PWM	Pulse Width Modulation
rms. RMS	Root Mean Square value
SR	Synchronous Rectifier
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching
EDT	Externally Driven Technique
PSM	Phase Shift Modulation

LIST OF PRINCIPAL SYMBOLS

θ	phase angle expressed in fraction of a switching cycle period
C_{V1} and C_{V2}	auxiliary circuit input voltage splitter capacitors
C_o	output filter capacitor
L_1 and L_2	output filter inductors
D	duty ratio of main switches
D_{eff}	effective duty cycle
ΔD	loss in duty cycle
f_s	switching frequency
$C_{sb1}, C_{sb2}, C_{sb3}$, and C_{sb4}	snubber capacitors for each of the four switches, respectively
k	transformer turns ratio
L_{Lk}	leakage inductance of the transformer
P_o	output power of the converter
S_1, S_2, S_3, and S_4	four switches of the full bridge converter
SR_1 and SR_2	two switches of the synchronous rectifiers
R_o	the converter load
T_{fr}	power transformer
$v_{ds1}, v_{ds2}, v_{ds3}$, and v_{ds4}	instantaneous drain to source voltage of the four switches, respectively

V_o	nominal output voltage
V_d	nominal input voltage
$V_{d\,min}$ and $V_{d\,max}$	input dc voltage range
T_s	switching cycle period
t_d	switching dead time
t	time variable
I_{aux} and I_{al}	peak value of the current through the two auxiliary inductors L_{aux} and L_{al}, respectively
I_{L1pk} and I_{L1v}	peak and valley values of the current through the output inductor L_1, respectively
I_{L2pk} and I_{L2v}	peak and valley values of the current through the output inductor L_2, respectively
I_{ppk} and I_{pv}	peak and valley values of the current in primary winding of transformer T_{fr}, respectively
I_o	nominal output current
i_{ds1}, i_{ds2}, i_{ds3} and i_{ds4}	instantaneous primary current of the four switches, respectively
i_p	instantaneous primary current of the power transformer
i_{aux}	instantaneous auxiliary current through the auxiliary inductor L_{aux}

CHAPTER 1
INTRODUCTION

1.1 Introduction

Full-bridge dc/dc converters are extensively used in medium to high power level applications. For most of these applications, particularly those of the computer and telecommunication systems, the most desirable features of the converter are high efficiency, high power density, high reliability and low EMI.

Unfortunately, the standard full bridge topology operates in hard switching, and the hard switching converter is unable to achieve high efficiency and high power density, because of the following reasons. In order to achieve high power density, the switching frequency is normally increased. At increased frequency, the converter can employ smaller sized power magnetics and capacitors. However, as the switching frequency increases, the switching losses associated with the turning on and off of switches will become excessive. These losses remarkably reduce the converter's overall efficiency, and high power density can hardly be achievable due to the resultant high cooling requirements.

To solve these problems, soft switching techniques are normally used. Basically there are two types of the soft switching techniques: zero voltage switching (ZVS) and zero current switching (ZCS). Either of the techniques can greatly reduce and even completely eliminate the switching losses in a converter, and then high efficiency will be

obtained. However, it has been well understood that ZVS is more advantageous for a MOSFET switch topology than is ZCS.

High power level full bridge converters usually use IGBT switches, due to IGBT's low conduction losses and high power capability. However, IGBT is not as fast as MOSFET, and its switching frequency is hardly above 100 kHz. Unlike IGBT, MOSFET is a resistive device when it is turned-on, and the conduction losses are higher as compared to IGBT. However, MOSFET is the fastest device and is able to be operated above 1 MHz.

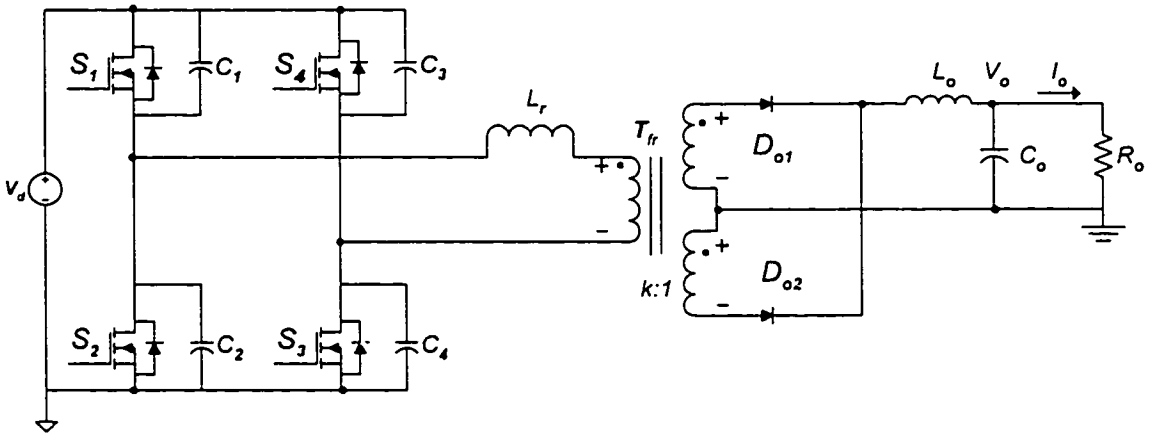
As mentioned before, the approach to achieve high power density is to operate the converter at a higher switching frequency. Thus, for power levels below 3 kW, the full-bridge converters now employ MOSFET switches. In most of these converters, ZVS is used to boost the overall efficiency and alleviate the thermal problems. However, as to be reviewed in the following section, these converters lose ZVS under some operating conditions, causing potential thermal problems and risking the reliability of the converter.

1.2 Review of Existing ZVS Full Bridge Topologies

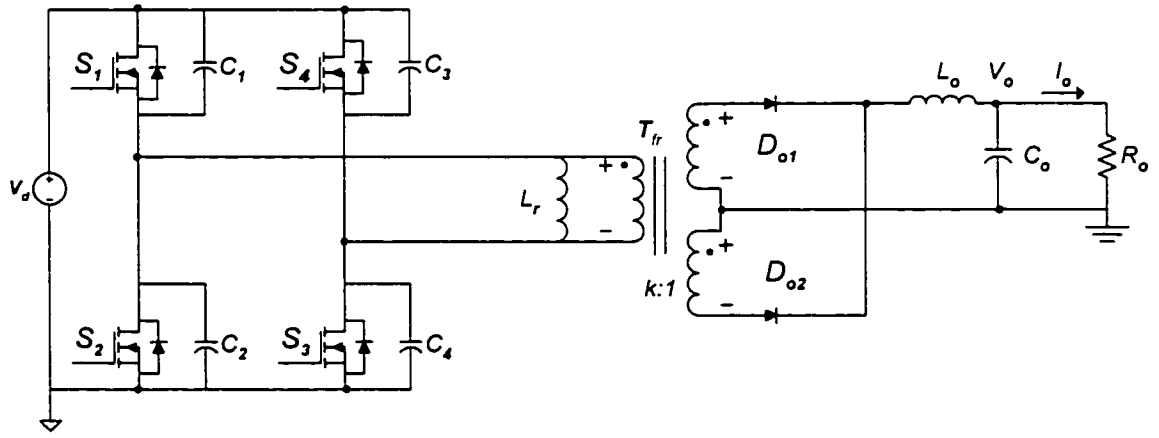
1.2.1 Conventional ZVS full bridge topologies

Fig. 1.1 shows two typical full bridge topologies those achieve ZVS. In Fig. 1.1a, ZVS is achieved by placing an inductor in series with the power transformer, while in Fig. 1.1b; it is achieved by placing an inductor in parallel with the power transformer. In both topologies, a snubber capacitor is placed across each switch. In a practical configuration, the series inductor may be the leakage inductor of the power transformer, the parallel inductor may be the magnetizing inductor of the power transformer, and the

snubber capacitor may be the inherent drain-to-source capacitor of the MOSFET switch. All these make these topologies very simple.



a : ZVS topology with series inductor



b : ZVS topology with parallel inductor

Fig. 1. 1: Conventional ZVS full bridge converter topologies.

The basic operating principles to achieve ZVS in these two topologies are as follows.

(i) ZVS turn-off is achieved by holding the drain-to-source voltage at zero or very low during the turn-off. This is accomplished by the snubber capacitor. At turn-off, the snubber capacitor significantly slows down the rising of the drain to source voltage of the pertinent switch. In this way, the overlaps between the decreasing drain current and rising drain-to-source voltage of each switch is greatly reduced, or even completely eliminated, and so are the switching losses.

(ii) ZVS turn-on is achieved by completely discharging the snubber capacitors of the switches before they are turned-on. During the dead time of the gating of the bridge switches, the residual current in the series inductor as in the former topology, or the parallel inductor as in the later topology fulfills the discharging of the snubber capacitors.

In comparison of these two topologies in Fig. 1.1, the one with the series inductor can achieve ZVS even when a short circuit (or over loading) occurs in the load, while the other one that has the parallel inductor maintains ZVS operation even when an open circuit (or no load) occurs in output terminals. Both topologies are simple. However, both of them suffer from their own shortcomings.

The drawbacks of the topology with series inductor (Fig. 1.1a) include the following.

(i) Loss of ZVS at no load or light-load. It is because the completely discharge of snubber capacitors depends on the stored energy in L_r that is proportional to the square of the peak value of the primary current. When the load is light, the

primary current is low, and consequently the stored inductor energy is too low to deplete the snubber capacitor during the dead time. Thus, ZVS turn-on will be lost.

(ii) Reduction of the effective duty ratio because of the voltage drop on the series inductor. This leads to increase the output filter inductor, because a smaller effective duty ratio relates to higher ripple component in the secondary voltage, which needs a larger output inductor to filter out.

The drawbacks of the topology with parallel inductor (Fig. 1.1b) include the following.

(i) Loss of ZVS under over load or short-circuit conditions. It is because, when short circuit occurs in the output terminal, the large load current, when it is reflected into the primary side, will override the parallel inductor current and cancel its function to achieve ZVS.

(ii) Increased conduction losses and reduced efficiency at light load. It is because the circulating current flowing along the parallel inductor, switch and the input dc line is almost independent of the load level. At light load, the conduction losses arisen from the circulating current becomes significant compared to the load current, and this remarkably increases the total conduction losses as compared to the standard full bridge converter and the ZVS topology with series inductor.

It is seen that, both topologies lose ZVS under certain operating conditions. The loss of ZVS results in the following problems: (i) increased size of heat sink due to switching losses, (ii) higher EMI due to high di/dt of the snubber discharging current when the switch is turned-on, and (iii) reduced reliability due to reverse recovery current

of the body diodes.

1.2.2 ZVS full bridge topology with auxiliary circuit

Fig. 1.2 shows a ZVS full bridge topology with passive components [1]. It employs two asymmetrical auxiliary circuits. At proper timing, the switches are turned-on and off such that the appropriate snubber capacitor of the switches is discharged immediately before the switch is turned-on. This active approach to achieve ZVS overcomes the aforementioned drawbacks existing in the topologies shown in Fig. 1.1. Specifically, it achieves ZVS even under both extreme operating conditions, namely no load and output short circuit conditions, and there is no reduction of the effective duty ratio.

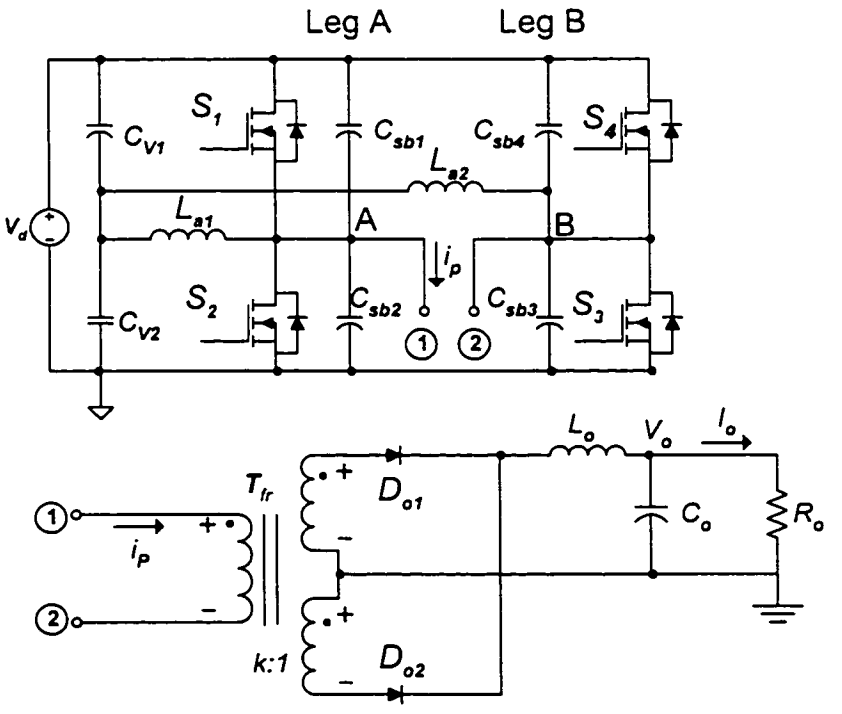


Fig. 1. 2: ZVS full bridge converter topology using auxiliary devices.

However, the topology in Fig. 1.2 is originally developed for low to medium power full-bridge converters using MOSFET's with low output current. For the same power with very high output current applications and increased switching frequency, the circuit topology should be further optimized to reduce the conduction losses caused by the auxiliary circuits. Also, at the same time efficient and synchronous rectification technique should be included in the output stage. Following section discusses a current doubler for the output rectifier circuit.

1.2.3 ZVS full bridge converter with current doubler synchronous rectifiers

Fig. 1.3 shows the operation of a ZVS full bridge topology with current doubler, synchronous rectifiers [3]. The current doubler offers an alternative rectification method for the bridge converters where bipolar voltages are utilized at the secondary side of the isolation transformer. It is well suited for low voltage and high current applications. The current doubler has following advantages [5]:

- there is no need for center-tapping
- transformer structure is simpler
- ripple currents cancel on output capacitor.
- each filter inductor carries only half of the dc output current.
- finer steps in turns ratio are possible
- transformer carries approximately half of the output current.
- operation on the primary side, including duty-cycle is unchanged.

- synchronous rectifier and output capacitor stresses are identical to the full-wave technique.

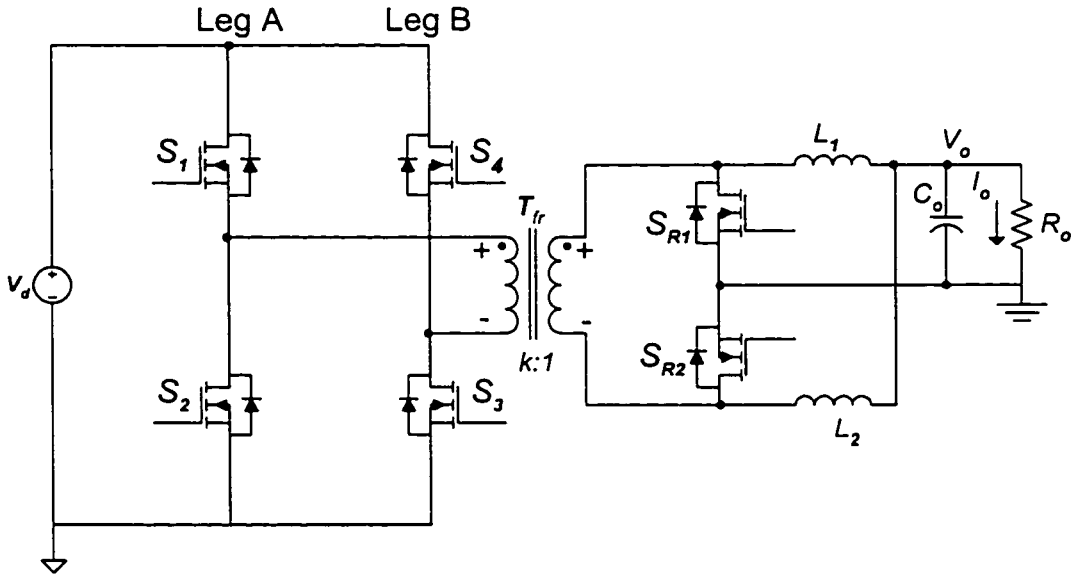


Fig. 1.3: Circuit diagram of current doubler rectifier.

Advancement in high density, low $r_{ds(on)}$ MOSFET development makes synchronous rectification a feasible and competitive rectification technique for low voltage, high current dc/dc converters. Synchronous MOSFET switches are used in the design to achieve higher efficiency [5], [16], [17]. The proper timing for the gates of the MOSFET rectifiers have an important role in determining the ultimate efficiency of the circuit. Early termination of the conduction interval will force the current into the body diode of the transistors leading to reverse recovery problems and switching losses in the devices. Conversely, any delay at the turn-off of the synchronous switches will result in a shoot through situation on the secondary side of the isolation transformer lowering the efficiency of the circuit.

Phase shift PWM technique is used as the control technique to regulate the

output voltage. Since the conventional phase-shift full-bridge converters have been extensively addressed in the literature, only the operation of the secondary side of the current doubler is discussed. The operation of the current doubler with synchronous rectification is highlighted in Fig. 1.4. In accordance with the primary side, the switching interval is divided into four intervals.

A. *Interval 1 ($t_o \le t < t_1$)*

At t_o, voltage across transformer (v_T) becomes positive at the end of last interval. During Interval 1, S_{R1} is off and S_{R2} is on. Current flows in positive direction in both filter inductors L_1 and L_2. The sum of i_{L1} and i_{L2} supplies the load current. The load current is equally shared between L_1 and L_2. The current i_{L1} flows through S_{R2} and the transformer secondary. The voltage across L_1 is equal to $v_T - v_o$. This positive voltage causes i_{L1} to increase. At the same time, L_2 freewheels through S_{R2} and i_{L2} decreases by the rate of $\frac{v_o}{L_2}$. The current through the secondary (i_T) is equal to i_{L1} and its accounts for half of the total load current.

B. *Interval 2 ($t_1 \le t < t_2$)*

In this interval, v_T becomes zero and both S_{R1} and S_{R2} are on. The voltage across L_1 becomes $-v_o$, producing a negative slope in i_{L1}, which now flows through S_{R1}. The conditions for L_2 do not change and both inductors are in freewheeling mode.

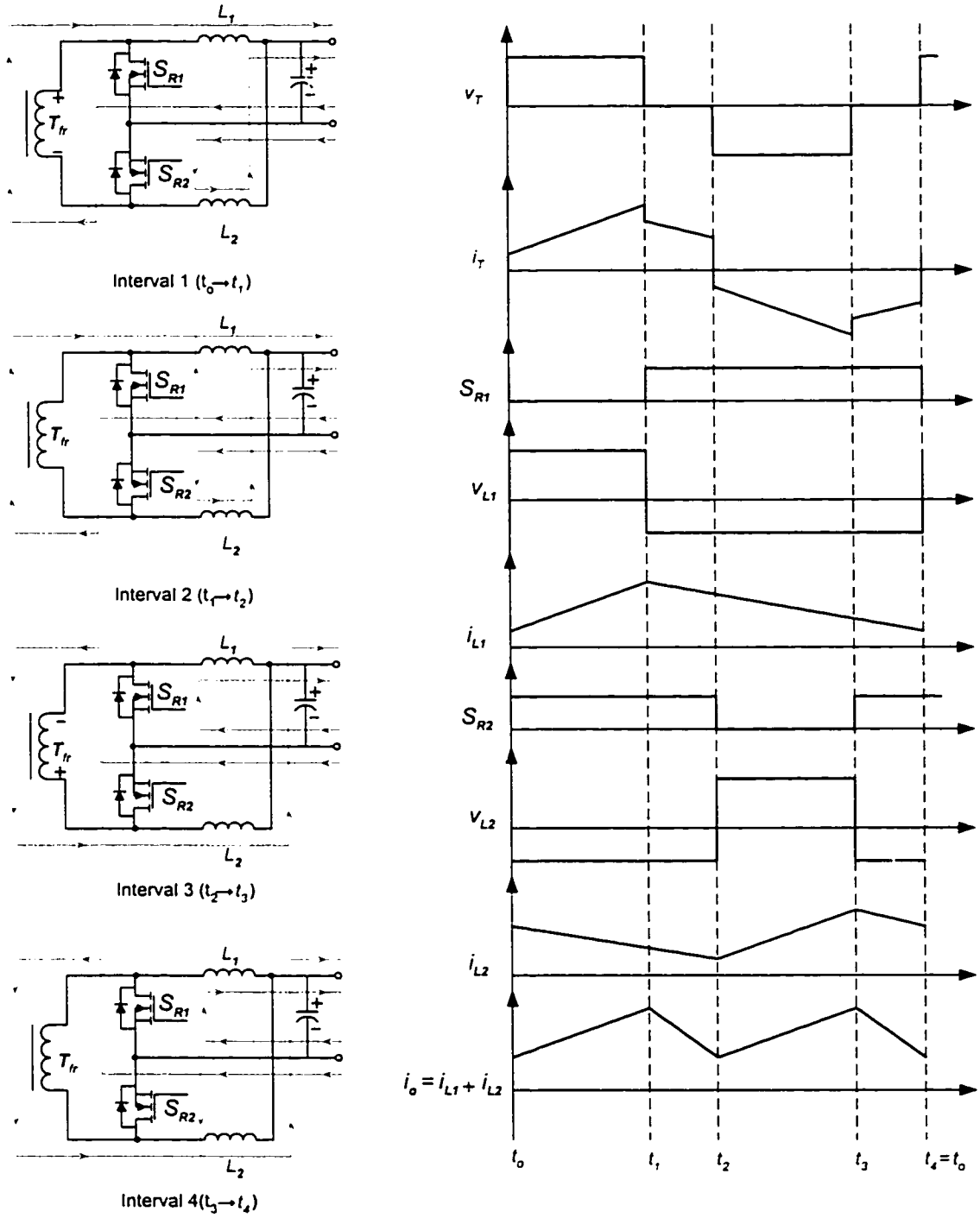


Fig. 1.4: Operation of the current doubler rectifier.

C. ***Interval 1 ($t_2 \leq t < t_3$)***

In this Interval, v_T becomes negative. S_{R1} is on and S_{R2} is off. A positive voltage $v_T - v_o$ appears across L_2 and i_{L2} starts to increase. In this state, i_T equals i_{L2} flows in the secondary again. L_1 freewheels through S_{R1} and i_{L1} decreases by the rate of $-\frac{v_o}{L_1}$.

D. ***Interval 4 ($t_3 \leq t < t_4$)***

The full operating cycle is completed by another freewheeling period. The voltage v_T becomes zero and S_{R1} and S_{R2} are on. $-v_o$ appears across L_2 causing its current to decrease and freewheel through S_{R2} while L_1 continues to freewheel as in Interval 3.

After Interval 4, the other switching cycle will start and the same operation is repeated again.

1.3 Objectives and scope of the study

The objectives of the study are as follows:

(i) presenting an optimized ZVS full bridge topology for low-voltage and high-current applications,

(ii) characterizing the proposed topology for industrial applications,

(iii) generating the design procedure.

The scope of this thesis is limited within the following frame:

(i) steady state analysis,

(ii) concept verification through ORCAD simulations and experimental results.

1.4 Thesis outline

The thesis follows the following structure.

In Chapter 2, the proposed topology is presented. Circuit description, operation and comparison and description for different gate driving techniques used for the control of synchronous rectification.

In Chapter 3, the steady state analysis is performed to understand its steady states characteristics and properties.

In Chapter 4, the performance and characteristics curves for the proposed topology has been proposed.

In Chapter 5, a design example is given for industrial application and for the proof of concept.

Conclusions of the thesis work are drawn in Chapter 6, followed by the suggestions for the future work.

CHAPTER 2

FULL BRIDGE CONVERTER WITH SYNCHRONOUS RECTIFICATION

2.1 Introduction

The improved line and load independent ZVS full bridge converter topology is presented in this chapter. This topology is simply a combination of a conventional full bridge converter and an auxiliary circuit that consists of few passive components. The effect of leakage inductance has also been taken into account. However, the advantages of the topology are remarkable: (i) it achieve ZVS independent of line and load conditions, and the power circuit is just that of the conventional full bridge converter, (ii) ZVS independent of line and load conditions results in smaller heat sinks for the switches and also the capability of operating the converter at high frequency, (iii) the design of the converter can follow well understood and well developed procedure to facilitate industrial application.

To extend the soft-switching capability of the phase shifted full bridge converter to supply low voltage, high current loads in distributed power systems, the current doubler offers an alternative rectification method, where bipolar voltages are utilized at the secondary side of the isolation transformer. Synchronous MOSFET switches are used in the design to achieve higher efficiency and zero voltage transitions from zero to full load [5], [16], [17].

In order to understand the operating principle and performance characteristics of

the proposed topology, and to provide reference in design procedure in Chapter 4, the steady state analysis is performed in the chapter 3.

In this chapter, the proposed topology is presented in Section 2.2. The working of the proposed topology is explained in Section 2.3. At the end of this chapter, some conclusions are drawn.

2.2 Circuit description

Fig. 2.1 shows the auxiliary commutated ZVS full bridge converter topology. It consists two functional sub-circuits. One sub-circuit is a PSM conventional full bridge converter, which is referred to as the power circuit hereafter. The other is an auxiliary network shown inside the dotted area in Fig. 2.1.

The power circuit employs the following devices: (i) S_1, S_2, S_3, and S_4, four MOSFET switches, (ii) T_{fr}, the power transformer with a turns ratio of k, (iii) S_{R1} and S_{R2}, two synchronous rectifying MOSFET's, (iv) L_1 & L_2 and C_o, the output filter, and (v) R_o, the load.

The auxiliary circuit is comprised by seven passive devices, i.e., (i) C_{sb1}, C_{sb2}, C_{sb3}, and C_{sb4}, four drain-to-source snubber capacitors, each connected across one switch, (ii) C_{V1} and C_{V2}, a capacitor voltage divider, (iii) L_{aux}, a auxiliary inductor.

Phase shift pulse width modulation is used as the control technique for output regulation in the proposed converter topology. When conventional PWM converters are operated at higher frequencies, the circuit parasitics are shown to have detrimental effects on the converter performance. Switching losses are specially pronounced in high frequency operations. Snubbers are normally required, thus adding significant losses in

high frequency operation. This topology enables designers to advantageously employ transformer leakage inductance along with auxiliary inductance. It has a somewhat higher rms current than the conventional full-bridge PWM converter, but with the combination with auxiliary inductor, it has much lower rms currents than other converters. The auxiliary inductor hardly interferes with the power transfer from input to the output. However, the auxiliary circuit does have significant influence on the switching transients

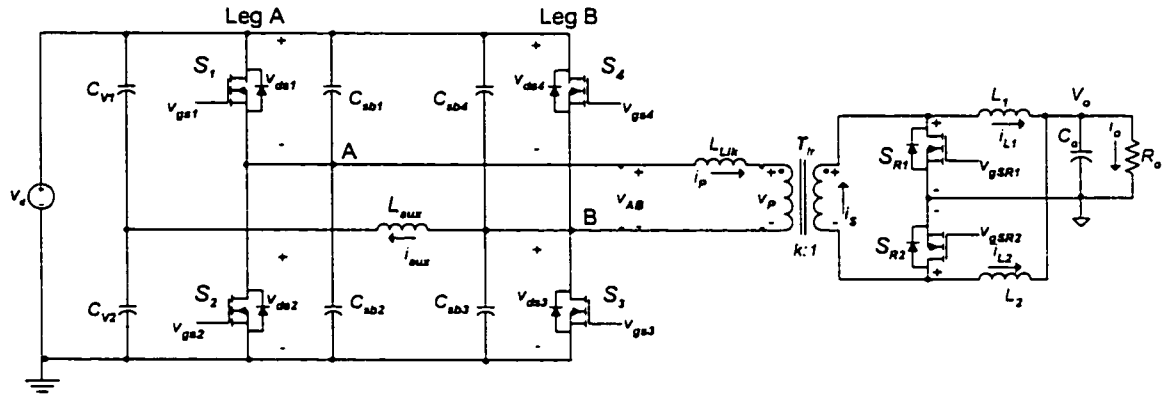


Fig. 2.1 The proposed ZVS full bridge converter topology

of the switches: it simply removes the switching losses from all the switches during both turn-on and turn-off transients. Since the higher value of leakage inductance will reduce the effective duty cycle of the power circuit, eventually resulting in lower turns ratio. This increases the reflected output current value on the primary side and the voltage stress of the secondary side rectifier devices, both leading toward lower overall efficiency of the circuit. With the addition of the auxiliary inductor, the value of leakage inductance can be reduced and as a whole the power circuit efficiency can be increased with the expense of small conduction loss.

2.3 Brief operation of the proposed converter

The gating signals are such that, instead of turning-on the diagonal opposite switches in the bridge simultaneously, a phase shift is introduced between the switches in the left leg and those in the right leg with a small delay between the switches of each leg. PSM is used as a control technique for the output voltage regulation and the externally driven technique (EDT) is used for the synchronous rectifier switches. Together, with the auxiliary circuit, the leakage inductance of the transformer, PSM control and EDT, zero voltage switching is achieved for all the switches of full-bridge converter as well as the synchronous rectifier.

The proposed converter has two modes of operation: Mode 1 and Mode 2. Mode 1 occurs at heavy loads and the converter has ten distinct operating intervals during a single switching cycle. The key waveforms and equivalent circuits are shown in Fig. 2.2 and Fig. 2.3. The other mode of operation occurs at light loads and the converter has twelve distinct operating intervals during one switching cycle. The key waveforms and equivalent circuits are shown in Fig. 2.4 and Fig. 2.5. The operation principle for Mode 1 and Mode 2 are explained in Section 2.3.1 and Section 2.3.2.

2.3.1 Mode 1

It is well understood that power transfer from the primary side to the secondary side will be there when diagonal switches are conducting. The different intervals for Mode 1 are shown in Fig. 2.2 and the equivalent circuits are shown in Fig. 2.3. Mode 1 explains the behavior of the proposed converter.

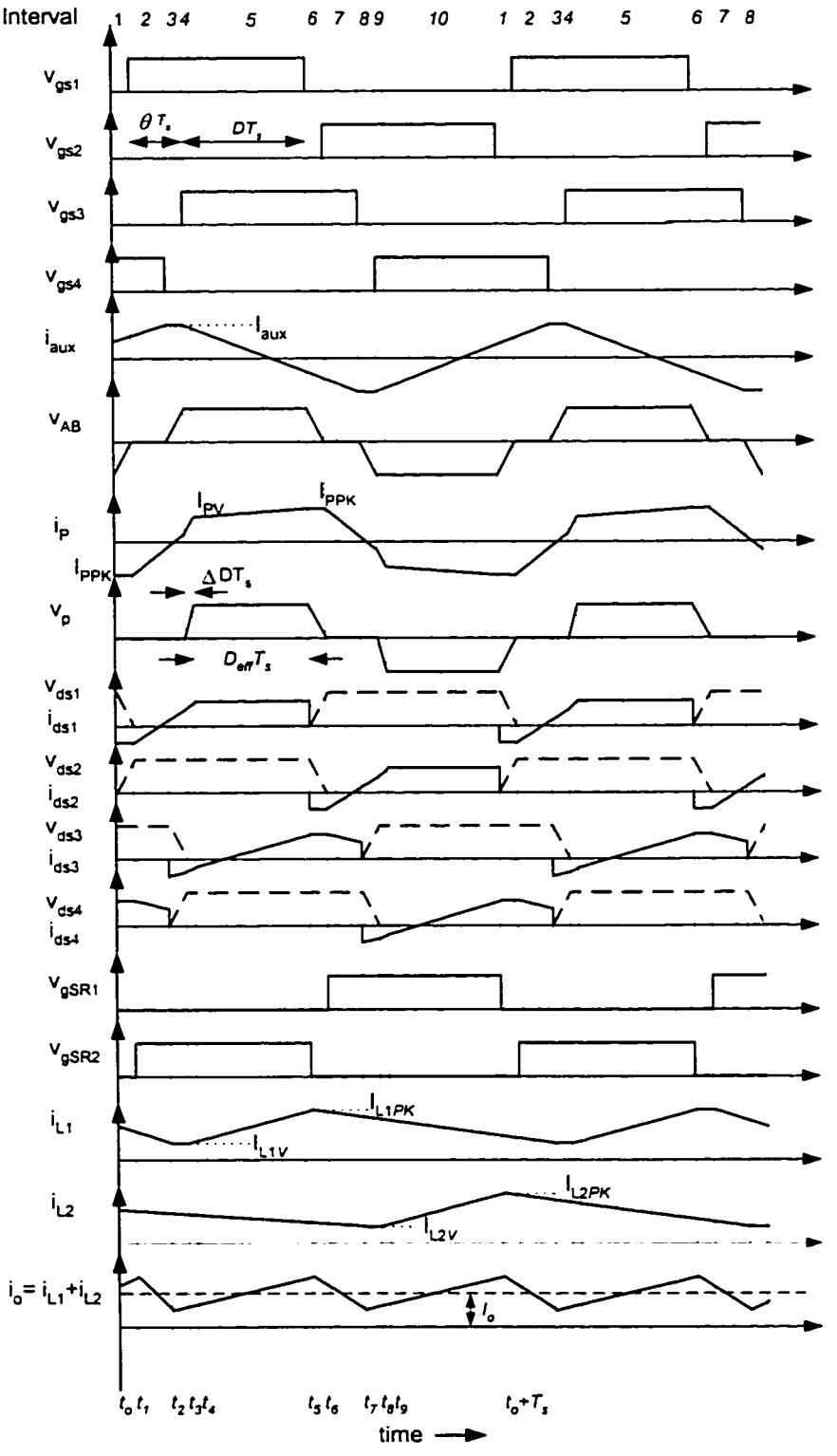


Fig. 2.2 Key waveforms for the proposed converter topology in Mode 1. The dead time and switching transient are exaggerated.

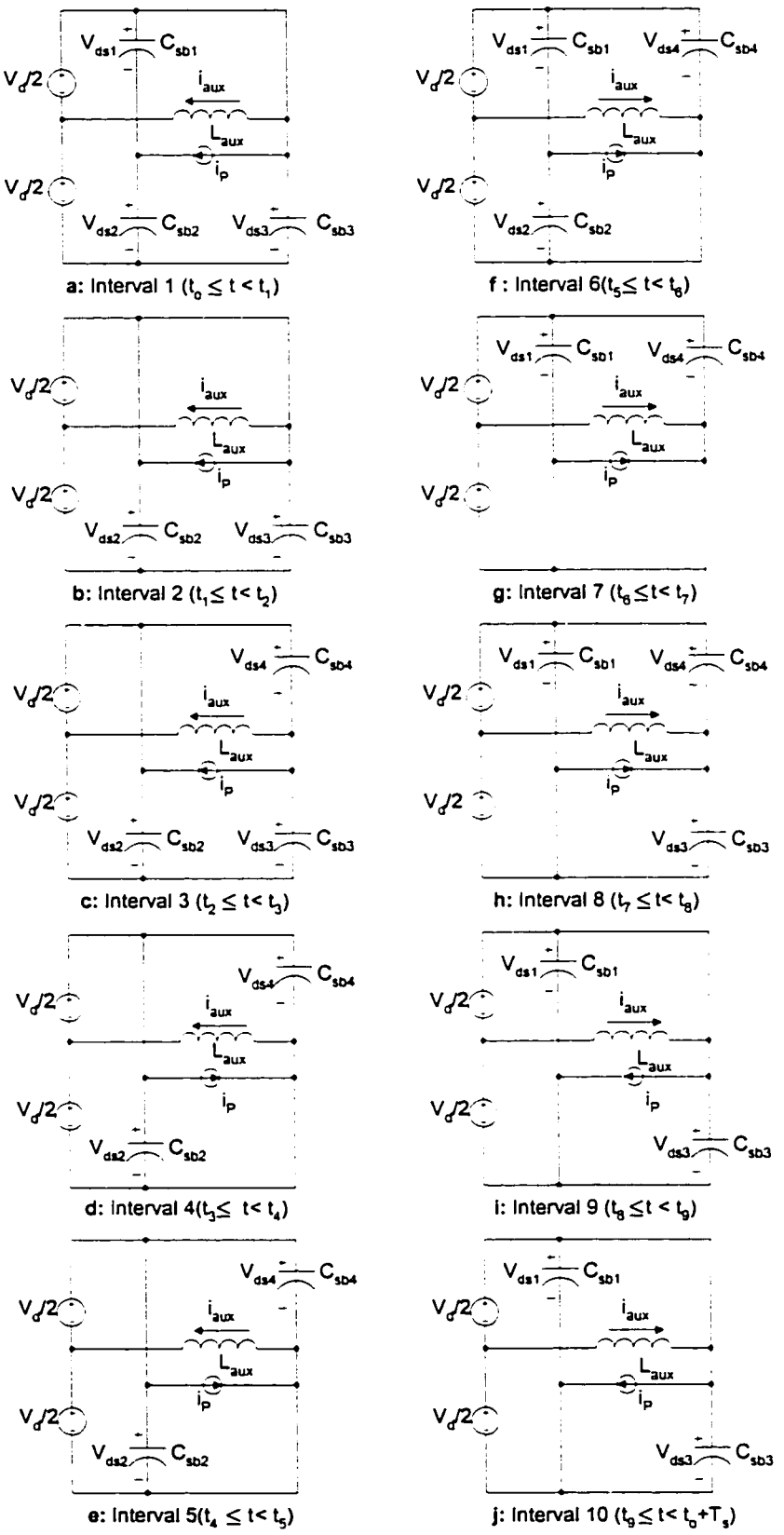


Fig. 2.3 Equivalent circuit in different intervals in Mode 1.

In the last interval of previous cycle when both S_2 and S_4 were on, the primary current of T_{fr} saw a constant voltage, $-V_d$, and S_{R1} was on and S_{R2} was off. At the end of this interval the primary current reached at its peak value I_{ppk}. At the beginning of this interval when S_2 is turned-off and no other switching action takes place. The current flowing through S_2 is the primary peak current I_{ppk} which is flowing through *leg A* starts to charge C_{sb2} and discharge C_{sb1}. During this interval T_{fr} starts to see a zero voltage which is given by dead time (t_d). During this interval none of the secondary rectifier switches S_{R1} and S_{R2} are turned-on so the current is freewheeling in both inductors. As this interval is small the primary current (i_p) remains constant. Within this interval the voltage across switch S_1, which is given by v_{ds1} falls to zero volts and the voltage across switch S_2, which is given by v_{ds2} reaches to V_d. Now S_1 has ZVS condition for turn-on. In the next interval, S_1 is turned-on in ZVS condition. As both S_1 and S_4 are on, the primary winding of T_{fr} sees zero voltage. During this interval S_{R2} is turned-on. At the beginning of Interval 3, S_4 is turned-off, the auxiliary current flowing through L_{aux} reaches to its peak, which is given by I_{aux}. In this interval primary current is still flowing in the negative direction due to the energy stored in L_{Llk}. This primary current helps auxiliary current to charge the snubber capacitor C_{sb4} and discharging snubber capacitor C_{sb3}. The duration of tnis interval is given by dead time. At the beginning of next interval, S_3 is turned-on under ZVS condition. During this interval i_{aux} starts to decrease linearly and the primary current starts to reverse the direction from

negative to positive. At the beginning of interval 5, the primary side has positive current and both diagonal switches S_1 and S_3 are on. Thus the power transfer from primary side to secondary side is there and load current is equally shared between L_1 and L_2. The rest five intervals are similar to first five intervals.

2.3.2 Mode 2

The different intervals for Mode 2 are shown in Fig. 2.4 and the equivalent circuits are shown in Fig. 2.5. Mode 2 explains the behavior of the proposed converter. This mode occurs at light loads and has twelve distinct operations. The working and operation is same as Mode 1 but due to light load it is going to have two more additional intervals per switching cycle.

In the last interval of previous cycle when both S_2 and S_4 were on, the primary current of T_{fr} saw a constant voltage, $-V_d$, and S_{R1} was on and S_{R2} was off. At the end of this interval the primary current reached at its peak value I_{ppk}. At the beginning of this interval when S_2 is turned-off and no other switching action takes place. The current flowing through S_2 is the primary peak current I_{ppk} which is flowing through *leg A* starts to charge C_{sb2} and discharge C_{sb1}. During this interval T_{fr} starts to see a zero voltage which is given by dead time (t_d). During this interval none of the secondary rectifier switches S_{R1} and S_{R2} are turned-on so the current is freewheeling in both inductors. As this interval is small the primary current (i_p) remains constant. Within this interval the voltage across switch S_1, which is given by v_{ds1} falls to zero volts and the voltage across switch S_2, which is given by v_{ds2} reaches to V_d. Now S_1 has ZVS

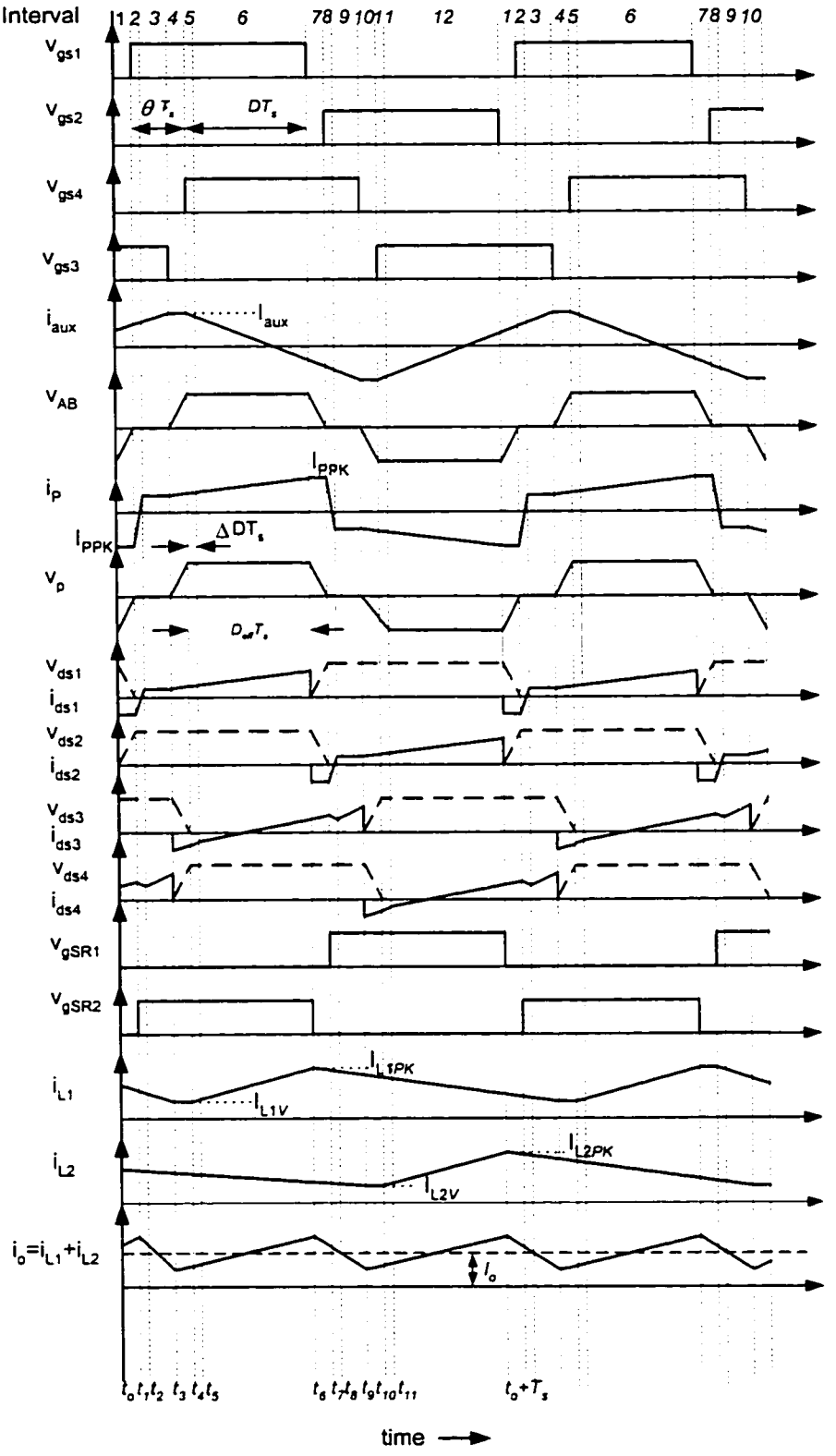


Fig. 2.4 Key waveforms for the proposed converter topology in Mode 2. The dead time and switching transient are exaggerated.

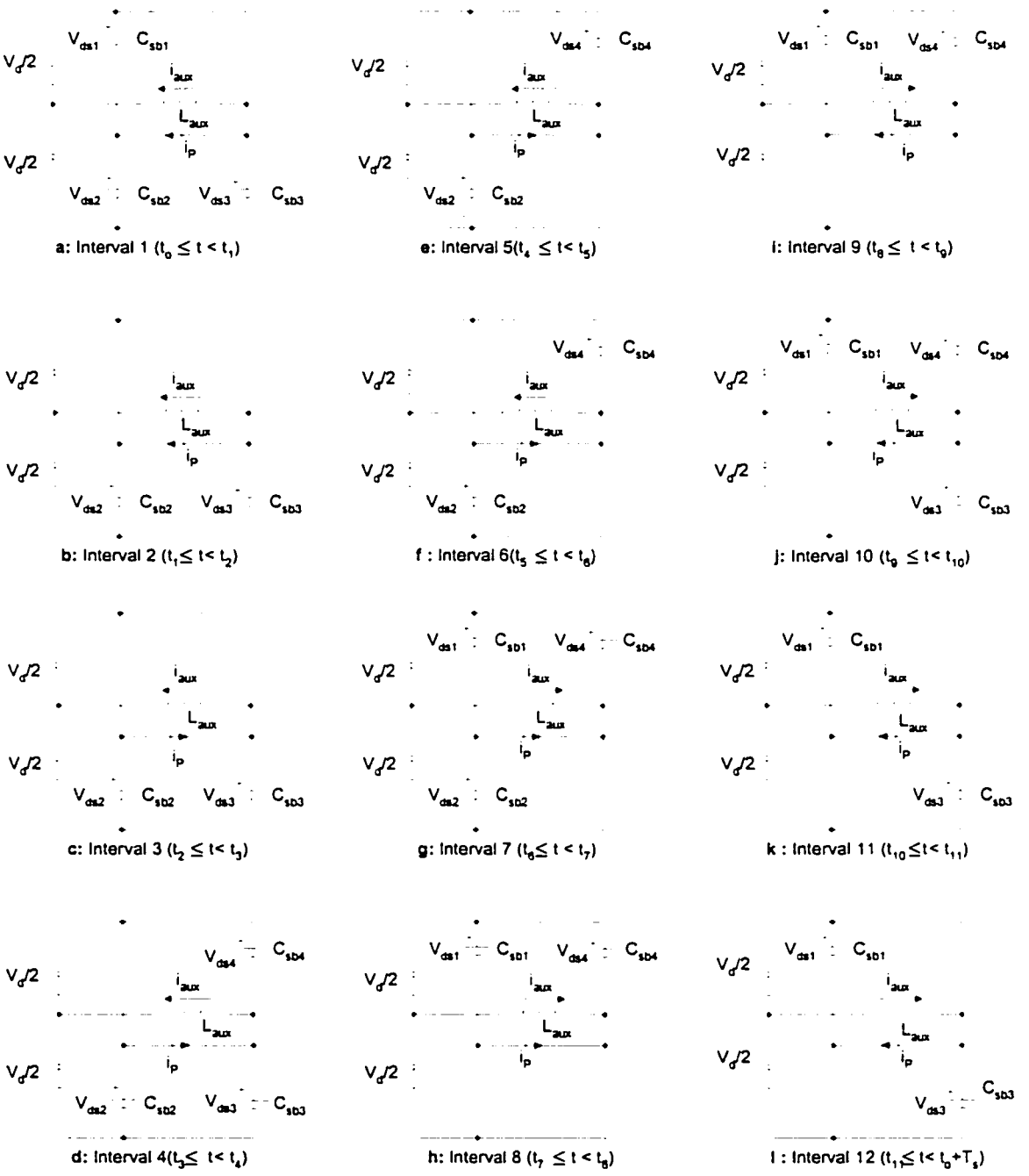


Fig. 2.5 Equivalent circuit in different intervals in Mode 2.

condition for turn-on. In the next interval, S_1 is turned-on in ZVS condition. As both S_1 and S_4 are on, the primary winding of T_{fr} sees zero voltage. During this interval S_{R2} is turned-on. In this interval primary current discharge the leakage inductance (L_{Llk}) very fast and changed the direction from negative to positive. During the beginning of next interval no switching action takes place and the primary current remains constant for the rest of interval. In the beginning of Interval 4, S_4 is turned-off, the auxiliary current flowing through L_{aux} reaches to its peak, which is given by I_{aux}. During this interval, auxiliary current is enough to charge the snubber capacitor C_{sb4} and discharging snubber capacitor C_{sb3}. The duration of this interval is very small which is given by dead time. In this interval, the primary side of the transformer starts to see the positive voltage. At the beginning of next interval, S_3 is turned-on under ZVS condition. During this interval i_{aux} starts to decrease linearly. The primary side has positive current and both diagonal switches S_1 and S_3 are on. Thus the power transfer from primary side to secondary side is there and load current is equally shared between L_1 and L_2. At the beginning of interval 6, no switching action takes place so there will be no effect on the power transfer. The rest six intervals are similar to first six intervals.

2.4 Synchronous Rectification

The conduction loss of diode rectifier contributes significantly to the overall power loss in a power supply, especially in low output-voltage application. The rectifier conduction loss is proportional to the product of its forward voltage drop, V_F and the forward conduction current, I_F. On the other hand, operating the MOSFET in third

quadrant, it can be used as a synchronous rectifier, which presents a resistive *i-v* characteristic. Under certain current level, the forward voltage drop of a synchronous rectifier can be lower than that of a diode rectifier, and consequently reduces the rectification loss [17]. Due to the fact that the synchronous rectifiers are active devices, the design and utilization of synchronous rectification need to properly address.

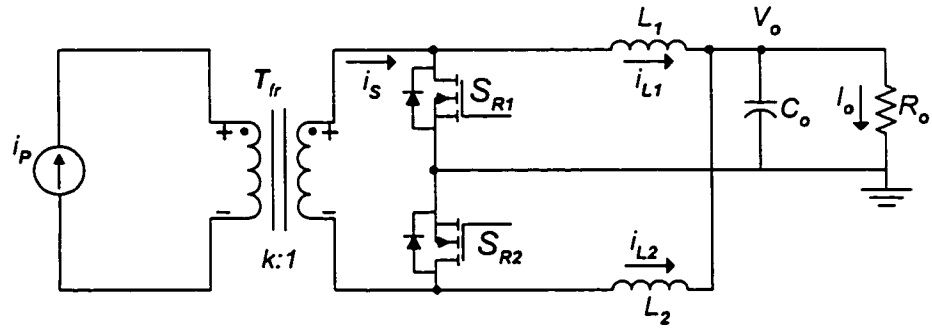


Fig. 2.6: MOSFET used as a synchronous rectifier

With the advanced technology in MOSFET design, the on-resistance is very low (in the order of a few milliohms), thus the power losses are also very low. Since the MOSFET now acts as a diode and not as a switch, the role of the source and drain become reversed. Fig. 2.6 shows the synchronous rectifier, where the current of full bridge is modeled as a square wave current source on the primary side. When the power MOSFET is used for synchronous rectification, it is configured so that the current normally flows through the channel from source to drain (in the direction of body diode). This ensures reverse blocking capability by the body diode, when the transistor is off because there is no current path through the body diode. To guarantee that the two MOSFET's do not turn- on simultaneously and create a transformer short circuit, a dead

time is usually introduced between the two gate signals. Control of the synchronous switches now becomes the main issue. The synchronous rectifiers can either be self-driven or external driven. A few examples of gate driving techniques for synchronous rectifiers have been presented in Section 2.4.1 and 2.4.2. The advantages and disadvantages of these synchronous rectification techniques have been explained briefly in Section 2.4.3

2.4.1 Self-driven technique

Fig. 2.7 shows full bridge current doubler with synchronous rectification using self-driven gate driving technique has been shown. Transformer T_{fr} has four windings $N_1 : N_2 : N_3 : N_4$ as shown in Fig. 2.7. Since no driver or control circuit is used to provide the gate-drive signals, this implementation of synchronous rectification is the simplest possible. The driving voltage now controls the conduction of MOSFET's. As the driving voltage, in the case of phase shifted bridge converter, is a quasi-voltage, the synchronous MOSFET's are on only during the positive and negative intervals of the driving voltage waveform. This results in lesser utilization of the synchronous MOSFET switches and the rectifier losses can't be reduced significantly. As every MOSFET has turn-on and turn-off delay, the load current at first flows through the body diodes of S_{R1} and S_{R2}. Due to relatively high forward voltage drops of the body diodes of S_{R1} and S_{R2}, the efficiency of synchronous rectification is reduced. The efficiency loss due to the body diode conduction depends on the duration of the dead time and the forward voltage drop of the body diodes. This loss can be minimized by connecting schottky diodes in parallel with S_{R1} and/ or S_{R2} or by minimizing the conduction times of body diodes of

S_{R1} and S_{R2}.

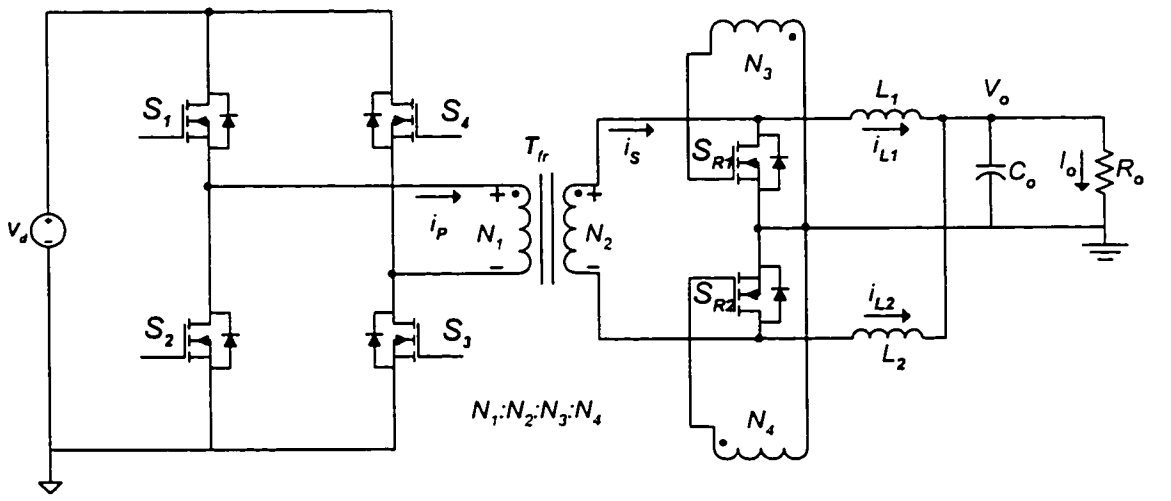


Fig. 2.7: MOSFET used as a synchronous rectifier using self-driven technique

The conduction loss of the body diodes of S_{R1} and S_{R2} is also dependent on the commutation time. To minimize the commutation times, the total inductance of the secondary side should be minimized. Moreover, it is important to make the leakage inductance of the transformer small relative to the other circuit inductance to avoid a loss of gate drive voltage for SR's.

The conduction of the body diodes of SR's not only increase the conduction loss, but also introduces the power loss due to their reverse recovery. This loss becomes more significant at high frequency at full load and high line. The only method of eliminating this loss is to parallel the schottky diodes to S_{R1} and S_{R2}.

2.4.2 External driven or control-driven technique

The problems of previous self-driven technique become more pronounced as the frequency is increased. Using external driven control circuits for the synchronous rectifier these drawbacks can be reduced. With this type of control, discrete IC's are used to drive the gate signal to achieve precise timing. The goal of whole exercise is to imitate the function of an ideal diode. When the drain-source voltage goes to zero, the MOSFET will turn-on and when the drain current goes to zero, the MOSFET will turn-off.

Fig. 2.8 shows the full bridge current doubler with synchronous rectification using external driven technique. The important issue, which justifies the use of synchronous rectifiers in place of diode rectifiers, is the timing. This is especially necessary as the operating frequencies are increased. The turn-on and turn-off of the switch has to be exactly on time, otherwise the inherent body diode will begin conducting resulting in increased conduction losses. In most cases, this could pose a problem since the external gate drive circuit will naturally have propagation delay. A brief overlapping of the gate-drive signals that turn-on both SR's simultaneously would short the secondary, causing an increased secondary current, and thus would lower efficiency or, in severe cases, would cause converter failure. To avoid simultaneous conduction of SR's in practical applications, a delay period is introduced. Since during the delay period no gate-drive signal is applied to the SR's the body diodes of the SR's are conducting. This not only increases conduction losses but also introduce reverse recovery loss. Therefore, the performance of control driven SR's is strongly dependent on the timing of the gate drive.

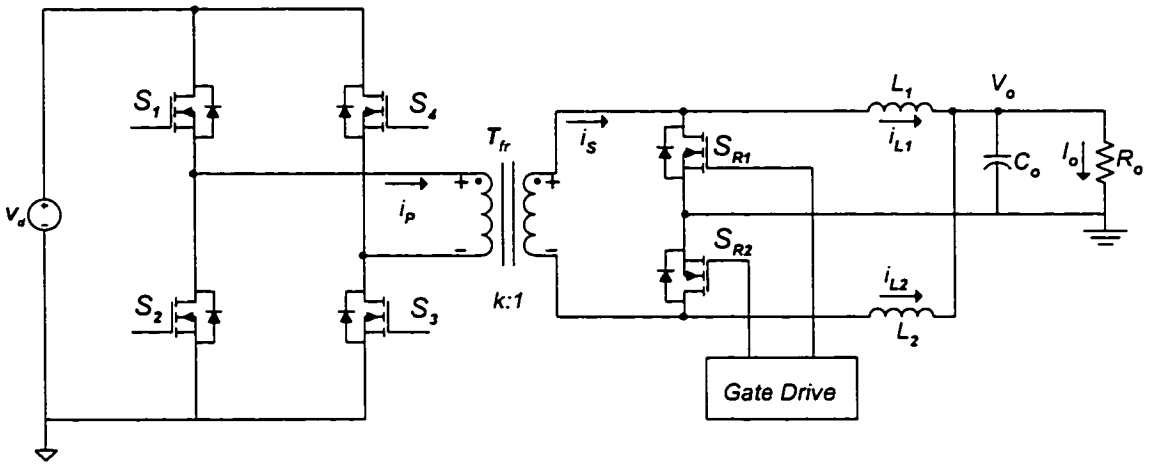


Fig. 2.8 MOSFET used as a synchronous rectifier using external-driven technique

2.4.3 Comparison of synchronous rectifier topologies

The different types of gate driving techniques for synchronous rectification have been examined. The advantages and disadvantages of the above driving techniques has been explained briefly:

Self –driven technique

Advantages:

- no external control or driver circuitry required
- simple design and requires few components

Disadvantages:

- synchronous rectifier losses increases as frequency increases
- power losses due to reverse recovery of body diodes

External driven or control driven

Advantages:

- suitable for high frequency operation
- very good accuracy
- synchronous rectifier including power MOSFET and gate/driver circuitry can be packaged together on a single chip, thus reducing losses otherwise caused by discrete components
- overcome timing delay problem

Disadvantages:

- more complex design
- packaging of synchronous rectifier on a single chip is costly

2.5 Conclusions

The operation of current doubler with synchronous rectification has been presented and it is clear by the description that the auxiliary circuit hardly interferes in the working of the proposed topology. The circuit is not complex and easy to understand. Also the different synchronous rectification techniques have been described briefly and some of conclusions based on the comparison of the different gate drive techniques used for synchronous rectification have been explained. As it is found from the comparison and description for the external and self- driven techniques for synchronous rectification that external driver is more suitable for high frequency operation.

CHAPTER 3

STEADY STATE ANALYSIS

3.1 Introduction

The analysis of improved ZVS full bridge converter with synchronous rectification shown in Fig. 3.1 has been presented in this chapter. The working principle has been described in Chapter 2. In this Chapter the detailed analysis of the proposed converter has been given.

The converter has two Modes of operation- Mode 1 occurs at full load or higher load. However Mode 2 occurs at reduced load. The difference between Mode 1 and Mode 2 is the energy stored in the leakage inductance. The optimization of leakage inductance and auxiliary inductance has been analyzed.

To better understand the operating principle and performance characteristics of the proposed topology performed in Chapter 4, and to provide reference in optimal procedure in Chapter 5, a detailed steady state analysis is performed in this chapter.

The steady state analysis is done in Section 3.2 for both Mode 1 and 2. Comparison between simulation done by ORCAD and analysis performed by Math CAD software has been given in Section 3.3.

3.2 Steady state analysis

As explained, in Chapter 2, a phase-shift control method is used in operating the converter. As conventional phase shift full bridge converters have been extensively discussed in the literature, the analysis of its operation will not be addressed in detail.

Only the operation of the auxiliary circuit with leakage inductance is analyzed below.

The analysis will be performed with the assumptions made below. In the analysis, the time varying variables such as the current and voltage of the principal components and devices are determined. Based on these variables, the performance of the converter can be illustrated, and the quantities such as rms, average or peak current and voltage of these components can be obtained. These quantities are used in designing the converter as presented in Chapter 5.

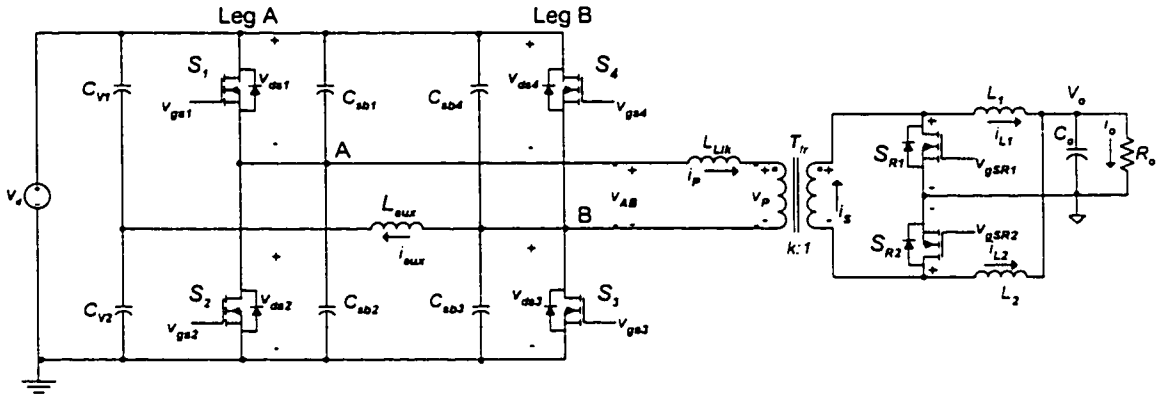


Fig. 3.1 The proposed ZVS full bridge converter topology

In the analysis presented below, a closed form solution is obtained by solving a set of differential equations in each interval and by matching the boundary conditions at the boundary of the intervals.

3.2.1 Assumptions and some constants for the analysis

To perform the steady state analysis, the following assumptions are made:

(i) The steady state conditions have been established and the converter is running in the continuous conduction mode at an input dc voltage V_d, producing the nominal output voltage V_o and delivering a power of P_o to a static load.

(ii) The gating of switches on *leg A*, namely S_1 and S_2, is leading the gating of switches on *leg B*, or S_3 and S_4, by a phase shifted angle θ which is required to regulate the output voltage,

(iii) The switching frequency is f_s,

(iv) All components and devices have ideal properties and characteristics, i.e.,

(1) T_{fr}: core works in a linear range and the transformer has a leakage inductance (L_{Llk}),

(2) L_1, L_2 and L_{aux}: all inductors are pure inductors and their losses are negligible, and their inductances are constant,

(3) C_o, C_{V1}, C_{V2}, C_{sb1}, C_{sb2}, C_{sb3}, and C_{sb4}: all capacitors are pure capacitors, their equivalent series resistance (ESR) and equivalent series inductance (ESL) are negligible,

(4) S_1, S_2, S_3, and S_4: all switches have negligible conduction losses, and the inherent capacitances are 0 F,

(5) S_{R1} and S_{R2}: the forward voltage drop is 0 V, and the recovery time is 0 s.

(6) The magnetizing inductance of the power transformer is so great that the magnetizing current is negligible.

(v) There is a very short dead time, t_d, between the on states of the two switches on each leg of the bridge,

(vi) C_{sb1} and C_{sb2} have equal capacitance value, and so do C_{sb3} and C_{sb4},

(vii) C_{V1} and C_{V2} have equal capacitance value, and they are large enough to maintain constant and ripple free voltage during the steady state operation.

(viii) Under these assumptions, the operating principle is illustrated. The proposed converter has two modes of operation: Mode 1 occurs at full load and Mode 2 occurs at reduced loads. The key waveforms for Mode 1 were shown in Fig. 2.2. Each switching cycle can be divided into ten distinct intervals. The equivalent circuit for each interval in Mode 1 has been shown in Fig 2.3. The key waveforms for Mode 2 have been shown in Fig. 2.4. Each switching cycle can be divided into twelve distinct intervals. The equivalent circuit for each interval in Mode 2 is shown in Fig 2.5.

For convenience, some constants are defined below.

In steady state, the effective duty ratio D_{eff} of each output rectifier is determined by

$$D_{eff} = \frac{D}{\left[1 + \frac{L_{Lik} \cdot f_s}{k^2 \cdot R_o}\right]} \tag{3-1}$$

where,
$$k = \frac{V_d \cdot D_{eff}}{V_o}, \tag{3-2}$$

$$D = \frac{1}{2} - \frac{t_d}{T_s} - \theta, \tag{3-3}$$

and
$$D_{\max} = \frac{1}{2} - \frac{t_d}{T_s} \tag{3-4}$$

where t_d is the switching dead time of the main switches, f_s the switching frequency, D is primary duty cycle, D_{eff} is change in duty cycle due to leakage inductance (L_{Llk}) and θ the phase shifted angle expressed in a fraction of one switching cycle.

It is not difficult to find that the current flowing through the output inductor has a waveform of saw-tooth biased by the output dc current I_o. Defining I_{L1pk} and I_{L1v} as the peak and valley values of this saw-tooth shaped current, respectively, then there are:

$$I_{L1pk} = \frac{1}{2}[I_o + \frac{V_o}{L_1}(1 - D_{eff})T_s] \tag{3-5}$$

$$I_{L1v} = \frac{1}{2}[I_o - \frac{V_o}{L_1}(1 - D_{eff})T_s] \tag{3-6}$$

For the auxiliary circuit, C_{V1} and C_{V1} act as a voltage divider, each holding half the input voltage V_d. For example, when S_3 is on for the duration of half cycle minus t_d, L_{aux} sees the positive voltage across C_{V1} that is $\frac{V_d}{2}$, and when S_4 is on, it sees the voltage across C_{V2} in opposite polarity that is $-\frac{V_d}{2}$. Then the current through, the auxiliary inductor L_{aux} alternatively rises and falls in linear mode. The magnitude of the total variation of this fluctuating current is determined as,

$$\Delta I_{aux} = \frac{V_d}{2L_{aux}}(\frac{T_s}{2} - t_d) \tag{3-7}$$

In addition, because the capacitors C_{V1} and C_{V2} the steady state auxiliary inductor current have no dc component. Thus, the current have a triangular waveform that is symmetrical about zero. Defining I_{aux} as absolute peak values of the current through L_{aux}:

$$I_{aux} = \frac{V_d}{4L_{aux}}(\frac{T_s}{2} - t_d) \tag{3-8}$$

3.2.2 Steady state analysis of each interval in Mode 1

A. *Interval 1 ($t_o \leq t < t_1$)*

In the last interval of previous cycle, both S_2 and S_4 were on while both S_1 & S_3 were off, the primary winding of T_{fr} saw a constant voltage, $-V_d$, and S_{R1} was forward biased and S_{R2} reverse biased. Thus, the output inductor current i_{L1} was reflected back into the primary side via S_{R1} and the coupling of T_{fr}. The drain current of S_2 was given by primary current and it reached its peak value at the end of the last cycle. This peak value is given by

$$I_{ppk} = \frac{I_{L1pk}}{k} \tag{3-9}$$

At the beginning of this interval, S_2 is turned-off, and no other switching action takes place during this interval. The equivalent circuit of this interval is shown in fig. (2.3), Interval 1.

As S_2 is off, I_{ppk}, which is the total current flowing into *leg A*, starts to charge C_{sb2} and discharge C_{sb1}. Thus, the drain to source voltage of S_1 (v_{ds1}) is decreasing while the drain to source voltage of S_2 (v_{ds2}) is increasing. Also S_3 remains off and S_4 is on. Then T_{fr} starts to see a zero voltage during this interval. Thus, S_{R1} and S_{R2} are both off. Both the inductors are in freewheeling stage. i_S (secondary current) equals to I_{L2pk} is

reflected back into the primary side. Thus, the primary peak current (I_{ppk}) is flowing into *leg A*.

As the interval is very small, the primary peak current (I_{ppk}) can be considered as constant. The drain to source voltage of both switches in *leg A* are governed by,

$$-C_{sb1}\frac{dv_{ds1}(t)}{dt}+C_{sb2}\frac{dv_{ds2}(t)}{dt}=I_{ppk} \tag{3-10}$$

&

$$v_{ds1}(t)+v_{ds2}(t)=V_d \tag{3-11}$$

By taking initial conditions as $v_{ds1}(t_o)=V_d$ and $v_{ds2}(t_o)=0$, and by taking the values of $C_{sb1}=C_{sb2}$, the equations (3-10) & (3-11) can be solved as:

$$v_{ds1}(t)=V_d-\frac{I_{ppk}}{2C_{sb1}}(t-t_o) \tag{3-12}$$

$$v_{ds2}(t)=\frac{I_{ppk}}{2C_{sb2}}(t-t_o) \tag{3-13}$$

Within this interval, v_{ds1} falls to zero volts and v_{ds2} reaches V_d, then the body diode of S_1 conducts to provide v_{ds1} at zero in the rest of this interval. Now S_1 has ZVS condition at turn-on.

After V_{ds1} reaches zero, the primary winding of T_{fr} will see a zero voltage as S_4 is still on. During this interval both S_{R1} and S_{R2} are off. As required by the both output inductors, the output current I_o is equally shared. This mode is a freewheeling mode as in a conventional full bridge converter.

In the meantime, the current that flows through S_4 only consist of i_{aux}, which is the current of the auxiliary inductor L_{aux}. It is found that

$$i_{aux}(t) = \frac{V_d}{2L_{aux}}(t - t_o - \theta \cdot T_s) + I_{aux} \tag{3-14}$$

The duration of this interval is the dead time t_d, i.e.,

$$t_1 - t_o = t_d \tag{3-15}$$

B. Interval 2 ($t_1 \leq t < t_2$)

At the beginning of this interval, S_1 is turned-on in ZVS condition. So, S_1 will achieve zero turn-on losses. No other switching action takes place during this interval. The equivalent circuit of this interval is shown in Fig. 2.3, Interval 2.

As both S_1 and S_4 are on, the primary winding of T_{fr} still sees zero voltage. During this interval S_{R2} is turned-on and S_{R1} is still off. The primary current is still flowing through the primary winding. Hence, S_1 consists of primary current which is governed by

$$I_P(t) = \frac{\frac{V_d}{L_{Llk}}(t_3 - t_4) + I_{pv} + I_{ppk}}{(t_3 - t_1)}(t - t_1) - I_{ppk} \tag{3-16}$$

The current passing through S_4 only has auxiliary current (i_{aux}) flowing through it, which is given by

$$i_{aux}(t) = \frac{V_d}{2L_{aux}}(t - t_1 - \theta \cdot T_s) + I_{aux} \tag{3-17}$$

The duration of this interval is determined by the phase shift angle that is required to regulate the output voltage as well as by the dead time:

$$t_2 - t_1 = \theta \cdot T_s - t_d \tag{3-18}$$

C. *Interval 3 ($t_2 \le t < t_3$)*

At the beginning of this interval, S_4 is turned-off. No other switching action takes place during this interval. The equivalent circuit of this interval is shown in Fig. 2.3, Interval 3.

When S_4 is off, i_{aux} reaches its positive peak value I_{aux} and remains constant during this interval. During this interval the primary current is still flowing and it helps in discharging and charging of snubber capacitors in *leg B*. It starts to charge C_{sb4} and discharge C_{sb3}. Owing to C_{sb4}, V_{ds4} can only rise slowly, providing the ZVS condition for S_4 to turn-off. Thus, a nearly loss less turn-off is achieved on S_4.

During this interval T_{fr} still see a zero voltage. During this interval S_{R2} is forward biased and S_{R1} is reverse biased. The load current is equally shared between L_1 and L_2. The current I_{L1} flows through SR_2 and the transformer secondary. The voltage across L_1 is equal to $V_P - V_o$. Thus, the current flowing out of *leg B* is i_{aux} plus the reflected output inductor current during the charging/discharging interval.

As this interval is small, i_{aux} is almost constant at its peak value I_{aux} and the value of primary current which is decreasing during this interval can be defined as:

$$I_P(t) = \frac{\frac{V_d}{L_{Lik}}(t_3 - t_4) + I_{pv} + I_{ppk}}{(t_3 - t_1)}(t - t_1) - I_{ppk} \qquad (3\text{-}19)$$

Similar to Interval 1, it is found that

$$V_{ds3}(t) = V_d - \int_{t_2}^{t_3} \frac{I_{aux} - \frac{\frac{V_d}{L_{Lik}}(t_3 - t_4) + I_{pv} + I_{ppk}}{(t_3 - t_1)}(t - t_1) + I_{ppk}}{2C_{sb3}} dt \qquad (3\text{-}20)$$

$$V_{ds4}(t) = \int_{t_2}^{t_3} \frac{I_{aux} - \frac{\frac{V_d}{L_{Llk}}(t_3 - t_4) + I_{pv} + I_{ppk}}{(t_3 - t_1)}(t - t_1) + I_{ppk}}{2C_{sb4}} dt \qquad (3\text{-}21)$$

Within this interval, V_{ds3} falls to zero volts and V_{ds4} reaches V_d. The equation (3-20), (3-21) shows that the secondary current relieves switch S_3 turn-on stress from i_{aux} by providing strength of i_{aux} in discharging the snubber capacitor (C_{sb3}) of S_3 but it will be increase the turn-off stress of S_4. During this Interval the primary of the transformer is till seeing zero voltage as negative current is still flowing through the primary due to the effect of leakage inductance in the primary side.

The duration of this interval is determined by the dead time:

$$t_3 - t_2 = t_d \qquad (3\text{-}22)$$

D. Interval 4 ($t_3 \le t < t_4$)

At the beginning of this interval, S_3 is turned on under ZVS condition. Thus, a nearly loss-less turn-on is achieved for S_3. No other switching action takes place during this interval.

As S_3 is on, L_{aux} sees a constant negative voltage established by C_{V2}. i_{aux} starts to decrease linearly, as given by

$$i_{aux}(t) = -\frac{V_d}{2L_{aux}}(t - t_3) + I_{aux} \qquad (3\text{-}23)$$

During this interval, primary current I_p changes from the negative polarity to the positive polarity. It is found that,

$$I_P(t) = \frac{V_d}{L_{Llk}}(t - t_4) + I_{pv} \tag{3-24}$$

The duration of this interval is determined by the loss in duty ratio due to leakage inductor required to regulate the output voltage:

$$t_4 - t_3 = \Delta D \cdot T_s \tag{3-25}$$

where, ΔD is the loss in Duty cycle due to leakage inductance and is given by:

$$\Delta D = \frac{I_o \cdot L_{Llk}}{k \cdot V_d \cdot T_s} \tag{3-26}$$

E. Interval 5($t_4 \le t < t_5$)

At the beginning of this interval no switching action takes place and the primary side starts to build up the positive voltage equals to V_d. During this interval S_{R1} is off and S_{R2} is forward biased. Current is flowing in both filter inductors. The load current is equally shared between L_1 and L_2. The value of L_{aux} is still decreasing which is governed by

$$i_{aux}(t) = -\frac{V_d}{2L_{aux}}(t - t_4) + I_{aux} \tag{3-27}$$

As the current becomes positive and diagonal switches S_1 and S_3 are on. The voltage across primary is V_d. The amount of current passing through primary is governed by

$$I_P(t) = \frac{I_{ppk} - I_{pv}}{(t_5 - t_4)}(t - t_4) + I_{pv} \tag{3-28}$$

The duration of this interval is determined by the effective duty ratio required to regulate the output voltage:

$$t_5 - t_4 = D_{eff} \cdot T_s = \frac{kV_o}{V_d} \tag{3-29}$$

F. Interval 6 through 10

The analysis of the circuit in the last five intervals of this switching cycle is similar to the first five intervals. The process will not be repeated here. After Interval 10, another switching cycle begins and operation of the circuit repeats the process from Intervals 1 through 10.

3.2.3 Steady state analysis of each interval in Mode 2

When the load is reduced, the leakage inductor has a small stored energy. As a result primary current will change the direction. The time required to discharge and charge in the other direction is based on the value of leakage inductance. So there will be an increase of one more interval. So in Mode 2 it is going to have twelve intervals per switching cycle. The analysis, key waveforms and equivalent circuit for each interval are given in the following section. The key waveforms for Mode 2 are shown in Fig. 2.4. Each switching cycle can be divided into twelve distinct intervals. The equivalent circuit for Mode 2 for each interval is shown in Fig 2.5.

A. *Interval 1 ($t_o \leq t < t_1$)*

In the last interval of previous cycle, both S_2 and S_4 were on while both S_1 & S_3

were off, the primary winding of T_{fr} saw a constant voltage, $-V_d$, and S_{R1} was forward biased and S_{R2} reverse biased. Thus, the output inductor current I_{L1} was reflected back into the primary side via S_{R1} and the coupling of T_{fr}. The drain current of S_2 was given by primary current and it reached its peak value at the end of the last cycle. This peak value is given by

$$I_{ppk} = \frac{I_{L1pk}}{k} \tag{3-30}$$

At the beginning of this interval, S_2 is turned-off, and no other switching action takes place during this interval. The equivalent circuit of this interval is shown in Fig. 2.5, Interval 1.

As S_2 is off, I_{ppk}, which is the total current flowing into *leg A*, starts to charge C_{sb2} and discharge C_{sb1}. Thus, the drain to source voltage of $S_1(V_{ds1})$ is decreasing while the drain to source voltage of $S_2(V_{ds2})$ is increasing. Also S_3 remains off and S_4 on. Then T_{fr} starts to see a zero voltage during this interval. Thus, S_{R1} and S_{R2} are both off. Both the inductors are in freewheeling stage. I_S (secondary current) equals to I_{L2pk} is reflected back into the primary side. Thus, the primary peak current (I_{ppk}) is flowing into *leg A*.

As the interval is very small, the primary peak current (I_{ppk}) can be considered as constant. The drain to source voltage of both switches in *leg A* are governed by,

$$-C_{sb1}\frac{dV_{ds1}(t)}{dt} + C_{sb2}\frac{dV_{ds2}(t)}{dt} = I_{ppk} \tag{3-31}$$

&

$$V_{ds1}(t) + V_{ds2}(t) = V_d \tag{3-32}$$

By taking initial conditions as $V_{ds1}(t_o) = V_d$ and $V_{ds2}(t_o) = 0$, and by taking the values of $C_{sb1} = C_{sb2}$, the equations (3-31) & (3-32) can be solved as:

$$V_{ds1}(t) = V_d - \frac{I_{ppk}}{2C_{sb1}}(t - t_o) \tag{3-33}$$

$$V_{ds2}(t) = \frac{I_{ppk}}{2C_{sb2}}(t - t_o) \tag{3-34}$$

Within this interval, V_{ds1} falls to zero volts and V_{ds2} reaches V_d, then the body diode of S_1 conducts to provide V_{ds1} at zero in the rest of this interval. Now S_1 has ZVS condition at turn-on.

After V_{ds1} reaches zero, the primary winding of T_{fr} will see a zero voltage as S_4 is still on. In this interval both S_{R1} and S_{R2} are off. As required by the both output inductors, the output current I_o is equally shared. This mode is a freewheeling mode as in a conventional full bridge converter.

In the meantime, the current that flows through S_4 only consist of i_{aux}, which is the current of the auxiliary inductor L_{aux}. It is found that

$$i_{aux}(t) = \frac{V_d}{2L_{aux}}(t - t_o - \theta \cdot T_s) + I_{aux} \tag{3-35}$$

The duration of this interval is the dead time t_d, i.e.,

$$t_1 - t_o = t_d \tag{3-36}$$

B. Interval 2 ($t_1 \leq t < t_2$)

At the beginning of this interval, S_1 is turned-on in ZVS condition. So, S_1 will achieve zero turn-on losses. No other switching action takes place during this interval. The equivalent circuit of this interval is shown in Fig. 2.5, Interval 2.

As both S_1 and S_4 are on, the primary winding of T_{fr} still sees zero voltage. During this interval S_{R2} is turned-on and S_{R1} off. The primary current is still flowing through the primary winding but due to reduced load the charge stored in leakage inductor (L_{Llk}) starts to decrease and change to the direction from negative to positive. Hence, S_1 consists of primary current which is governed by

$$I_P(t) = \frac{V_d}{L_{Llk}}(t - t_1) - I_{ppk} \tag{3-37}$$

The current passing through S_4 only has auxiliary current (i_{aux}) flowing through it, which is given by

$$i_{aux}(t) = \frac{V_d}{2L_{aux}}(t_1 - t) + I_{aux} \tag{3-38}$$

The duration of this interval is determined by the phase shift angle that is required to regulate the output voltage as well as by the dead time:

$$t_2 - t_1 = \frac{I_o \cdot L_{Llk}}{k \cdot V_d} \tag{3-39}$$

C. Interval 3 ($t_2 \leq t < t_3$)

At the beginning of this interval, no other switching action takes place. The equivalent circuit of this interval is shown in Fig. 2.5, Interval 3.

During this interval T_{fr} still see a zero voltage. During this interval S_{R2} is forward biased and S_{R1} is reverse biased. During this interval the primary current reached to a constant value as no switching action takes place. During this interval the primary current can be given by:

$$I_P(t) = \frac{V_d}{L_{Lik}}(t_2 - t_1) - I_{ppk} \tag{3-40}$$

The duration of this interval is determined by:

$$t_3 - t_2 = \theta \cdot T_s - t_d - t_2 + t_1 \tag{3-41}$$

D. Interval 4 ($t_3 \leq t < t_4$)

At the beginning of this interval, S_4 is turned-off and no other switching action takes place. The equivalent circuit of this interval is shown in Fig. 2.5, Interval 4.

When S_4 is off, i_{aux} reaches to its positive peak value I_{aux}. Similar to Interval 1, this current starts to charge C_{sb4} and discharge C_{sb3}. The V_{ds4} starts to rise from zero while V_{ds3} decreases from V_d.

During this interval T_{fr} starts to see a positive voltage because S_1 is already on. Therefore, the current flowing out of *leg B* is i_{aux} minus the reflected current from the load during the charging and discharging interval.

As this interval is very short, i_{aux} is almost constant at its peak value I_{aux}. The primary current starts to increase during this interval, which is given by:

$$I_P(t) = \frac{2I_{ppk} - \frac{V_d}{L_{Lik}}(t_2 - t_1)}{(t_6 - t_3)}(t - t_3) + \frac{V_d}{L_{Lik}}(t_2 - t_1) - I_{ppk} \tag{3-42}$$

Similar to Interval 1, it is found that

$$V_{ds3}(t) = V_d - \int_{t_3}^{t_4} \frac{I_{aux} - I_p(t)}{2C_{sb3}}(t - t_3)dt \tag{3-43}$$

$$V_{ds4}(t) = \int_{t_3}^{t_4} \frac{I_{aux} - I_p(t)}{2C_{sb4}}(t - t_3)dt \tag{3-44}$$

Contrary to the switches on *leg A* as seen from (3-43) and (3-44), the load current relieves S_4's turn-off current stress from i_{aux}, but it also reduces the strength of i_{aux} in discharging the snubber capacitor of S_3. In order to prepare the ZVS condition for S_3 to turn-on, I_{aux} must be greater than the reflected load current. Otherwise ZVS turn-on would be lost in C_{sb3}.

The duration of this interval is determined dead time, which is given by:

$$t_4 - t_3 = t_d \tag{3-45}$$

F. Interval 5($t_4 \le t < t_5$)

At the beginning of this interval S_3 is turned-on under ZVS condition. Thus nearly loss-less turn-on is achieved for S_3. No switching action takes place during this interval. The equivalent circuit of this interval is shown in Fig. 2.5, interval 4.

As S_3 is on, L_{aux} sees a constant negative voltage established by C_{V2}. i_{aux} starts to decrease linearly, as is governed by

$$i_{aux}(t) = -\frac{V_d}{2L_{aux}}(t - t_4) + I_{aux} \tag{3-46}$$

As the current becomes positive and diagonal switches S_1 and S_3 are on. The voltage across primary is V_d. The amount of current passing through primary is governed by

$$I_P(t) = \frac{2I_{ppk} - \frac{V_d}{L_{Llk}}(t_2 - t_1)}{(t_6 - t_3)}(t - t_3) + \frac{V_d}{L_{Llk}}(t_2 - t_1) - I_{ppk} \tag{3-47}$$

The duration of this interval is determined by the duty loss due to leakage inductance.

$$t_5 - t_4 = \Delta D \cdot T_s \tag{3-48}$$

F. Interval 6($t_5 \le t < t_6$)

At the beginning of this interval no switching action takes place and the primary side starts to build up the positive voltage equals to V_d. During this interval S_{R1} is off and S_{R2} is forward biased. Current is flowing in both filter inductors. The load current is equally shared between L_1 and L_2. The value of L_{aux} is still decreasing which is governed by

$$i_{aux}(t) = -\frac{V_d}{2L_{aux}}(t - t_5) + I_{aux} \tag{3-49}$$

As the current becomes positive and diagonal switches S_1 and S_3 are on. The voltage across primary is V_d. After this interval the primary current reached the peak value of the primary current (I_{ppk}). The amount of current passing through primary is governed by

$$I_p(t) = \frac{2I_{ppk} - \frac{V_d}{L_{Llk}}(t_2 - t_1)}{(t_6 - t_3)}(t - t_3) + \frac{V_d}{L_{Llk}}(t_2 - t_1) - I_{ppk} \quad (3\text{-}50)$$

The duration of this interval is determined by the effective duty ratio required to regulate the output voltage:

$$t_5 - t_4 = D_{eff} \cdot T_s = \frac{kV_o}{V_d} \quad (3\text{-}51)$$

G. Interval 7 through 12

The analysis of the circuit in the last six intervals of this switching cycle is similar to the first six intervals. The process will not be repeated here. After Interval 12, another switching cycle begins and operation of the circuit repeats the process from Intervals 1 through 12.

3.3 Analytical and simulated waveforms of the proposed converter

Simulation of the proposed converter topology is performed with the ORCAD software. Table 3.1 shows the principle parameters used in the simulation. It should be pointed out that the drain-to-source voltage and current of the two switches of one leg have exactly the same waveforms, although they are out of phase. Therefore, only the waveforms of S_1 and S_3 are displayed below. The waveforms obtained in ORCAD are compared by analysis done by using Math CAD software.

Figs. 3.2– 3.23 shows the voltage and current waveforms of the switches under full load and different input voltage. It is seen that ZVS on each switch is achieved at both turn-on and turn-off under all these conditions.

The waveforms shown in Fig. 3.2, Fig. 3.7, Fig. 3.12, Fig. 3.15, Fig. 3.18 and Fig.

3.21 are showing the primary current obtained from simulation and analysis. It can be seen that the peak magnitude in both the waveforms is the same. In Fig. 3.2(a), Fig. 3.7(a), Fig. 3.12(a), Fig. 3.15(a), Fig. 3.18(a) and Fig. 3.21(a) it is seen that the primary current has curve when it starts to decrease in Interval 2. This is because the snubber capacitor and leakage inductance has second order behavior. The ringing occurs in interval 3 is because of the resonance which is caused by the leakage inductance and snubber capacitor.

In Fig. 3.3(a), Fig. 3.8(a), Fig. 3.13(a), Fig. 3.16(a), Fig. 3.19(a) and Fig. 3.22(a) shows the waveforms across v_{AB}. It is seen that the voltage v_{AB} has dc level shifted. This is because in practice, the MOSFET can't be discharged fully due to a fixed voltage drop of the internal diode of the MOSFET. In analysis switches are ideal and they will discharge fully in the dead time.

In Fig. 3.4, Fig. 3.9, Fig. 3.14, Fig. 3.17, Fig. 3.20 and Fig. 3.23 are the primary voltage has same magnitude of voltage. The waveform shown in Fig. 3.4(a), Fig. 3.9(a), Fig. 3.14(a), Fig. 3.17(a), Fig. 3.20(a) and Fig. 3.23(a) has a ringing. This is because of the resonance of auxiliary inductor, leakage inductance and snubber capacitor. As the load reduces the effect of ringing also reduces.

The results shown in Fig. 3.5(a), Fig. 3.5(b), Fig. 3.10(a) and Fig. 3.10(b) shows the drain to source current and voltage for the switches in *leg A*. It is found that there is ringing shown in Fig. 3.5(a) and Fig. 3.10(a), which is due the resonance because of leakage inductance of the transformer and snubber capacitor.

Fig. 3.6(a), Fig. 3.6(b), Fig. 3.11(a) and Fig. 3.11(b) shows the drain to source current and voltage in *leg B*. It is found that the discharging current in Fig. 3.6(a), Fig.

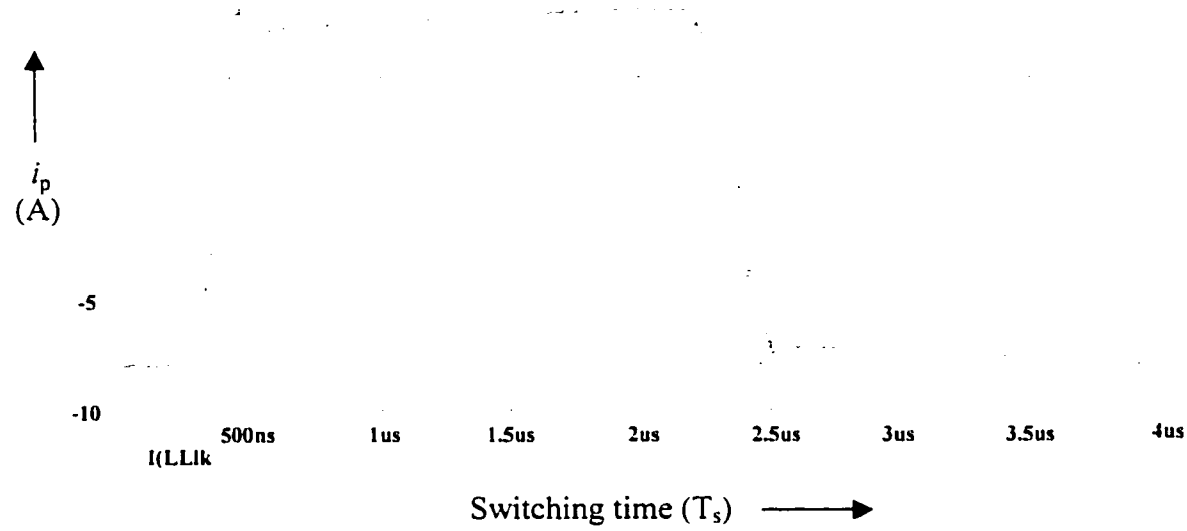


Fig. 3.2(a)

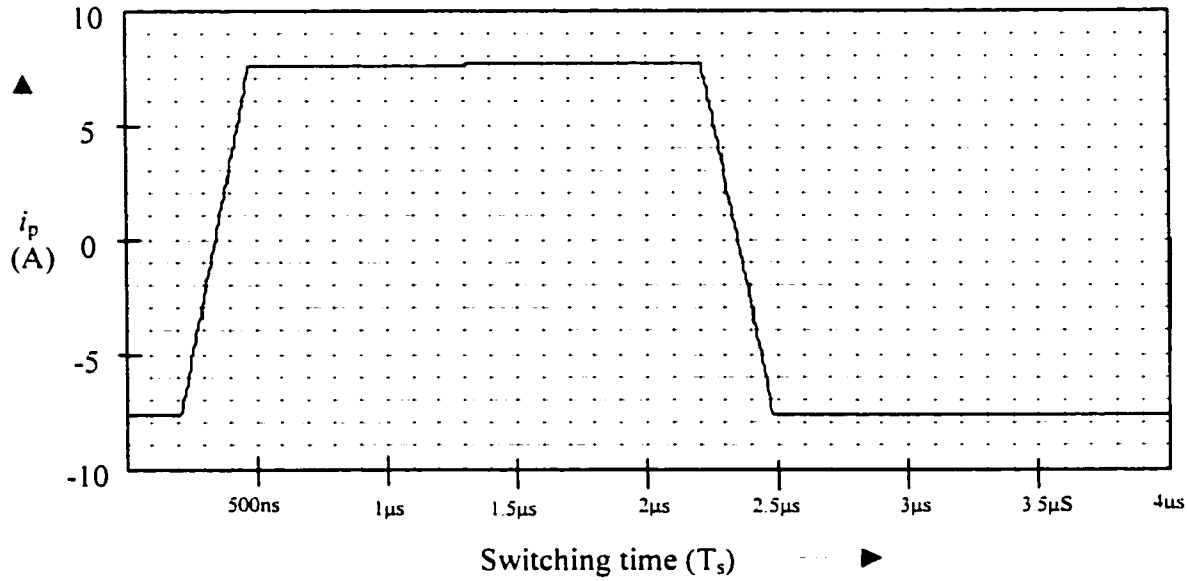


Fig. 3.2(b)

Fig. 3.2(a) Shows the simulation result for the primary current (i_p) at full load at V_d = 48V, V_o=1.6V and I_o=150A with $C_{sb1}, C_{sb2}, C_{sb3}, C_{sb4}$ =10nF, L_{aux} =2μH and L_{LLk} =0.5μH. Fig. 3.2(b) Shows the result for the same values done by analysis.

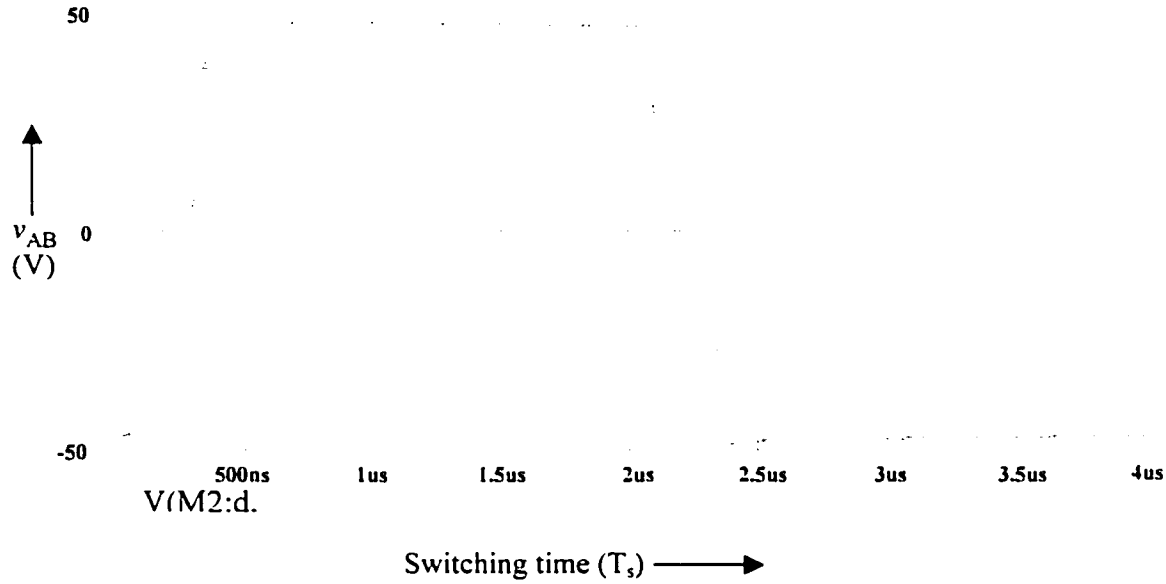


Fig. 3.3(a)

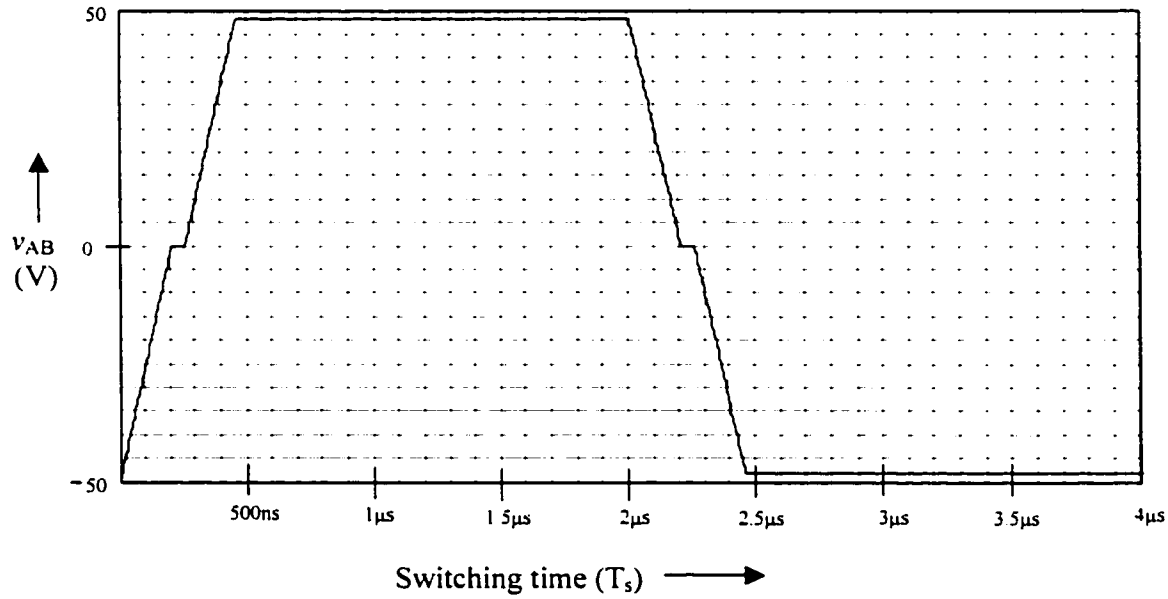


Fig. 3.3(b)

Fig. 3.3(a) Shows the simulation result for the full bridge voltage (v_{AB}) at full load at V_d = 48V, V_o=1.6V and I_o=150A with $C_{sb1}, C_{sb2}, C_{sb3}, C_{sb4}$ = 10nF, L_{aux} =2μH and L_{LLk} =0.5μH. Fig. 3.3(b) Shows the result for the same values done by analysis.

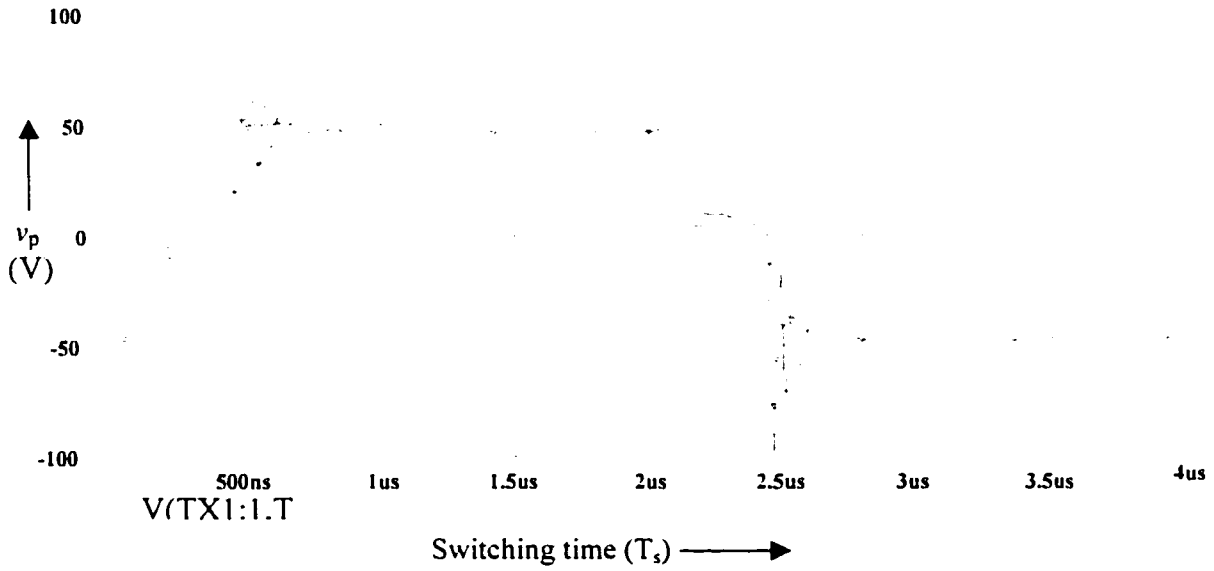


Fig. 3.4(a)

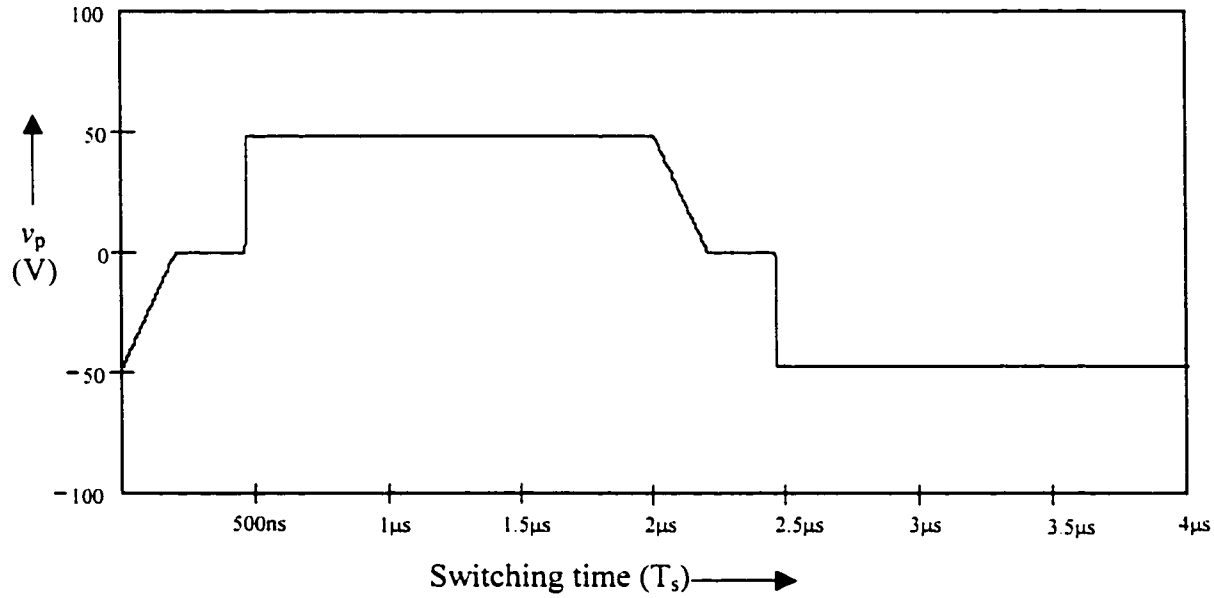


Fig. 3.4(b)

Fig. 3.4(a) Shows the simulation result for the primary voltage (v_p) at full load at V_d=48V, V_o = 1.6V and I_o=150A with C_{sb1}, C_{sb2}, C_{sb3}, C_{sb4}=10nF, L_{aux}=2μH and L_{Lik}=0.5μH. Fig. 3.4(b) Shows the result for the same values done by analysis.

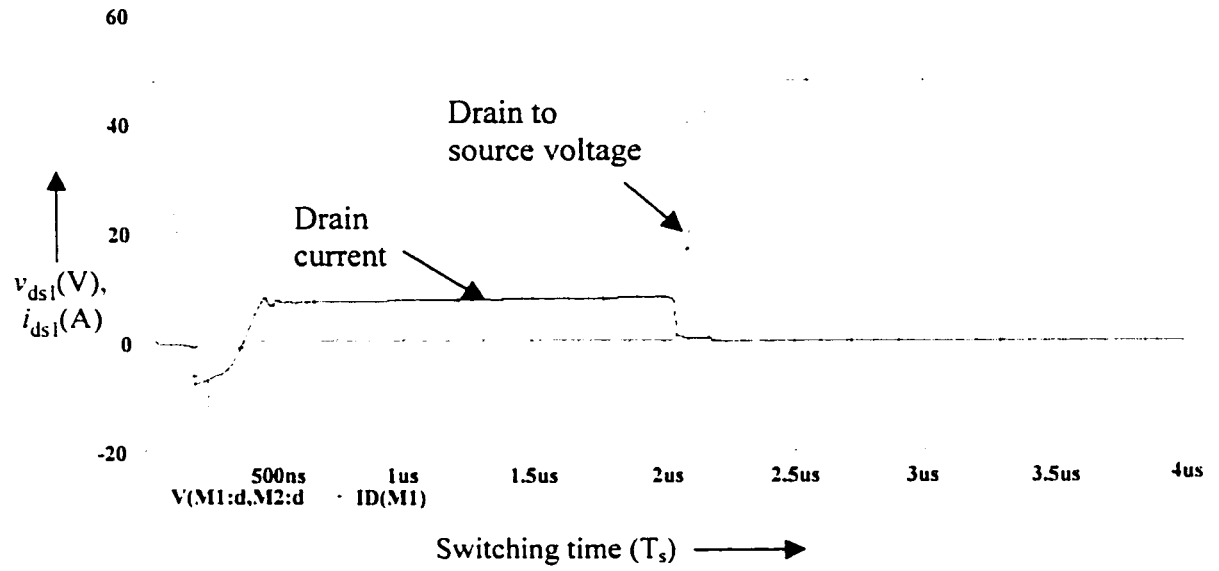


Fig. 3.5(a)

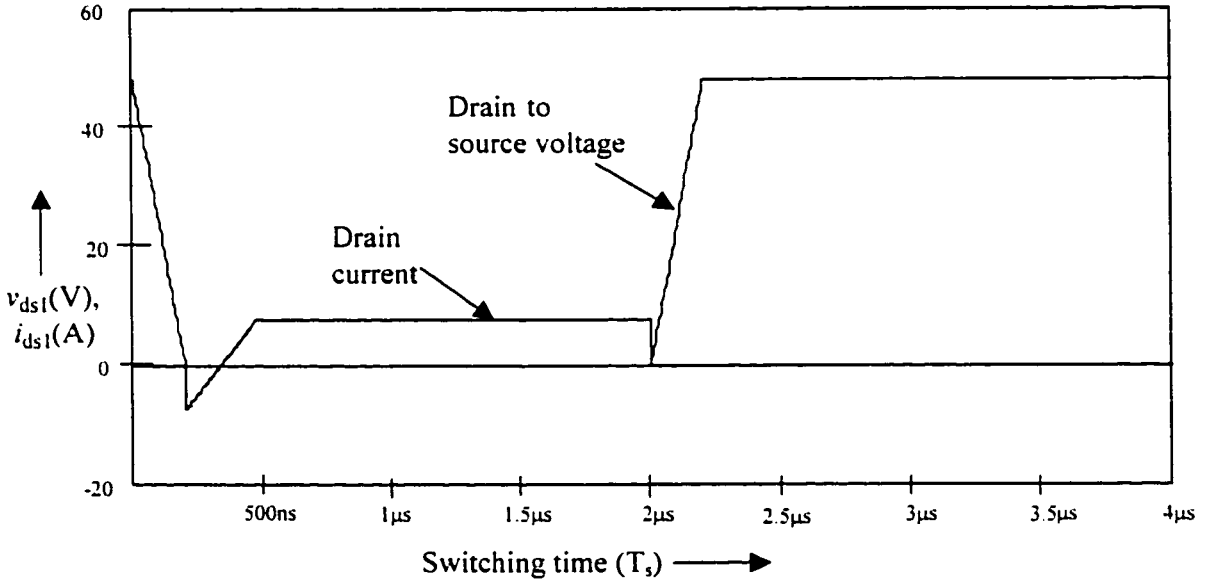


Fig. 3.5(b)

Fig. 3.5(a) Shows the simulation result for the turn-on and turn-off for switch (S_1) at full load at V_d=48V, V_o = 1.6V and I_o=150A with C_{sb1}, C_{sb2}, C_{sb3}, C_{sb4}=10nF, L_{aux}=2µH and L_{Lk}=0.5µH. Fig. 3.5(b) Shows the result for the same values done by analysis.

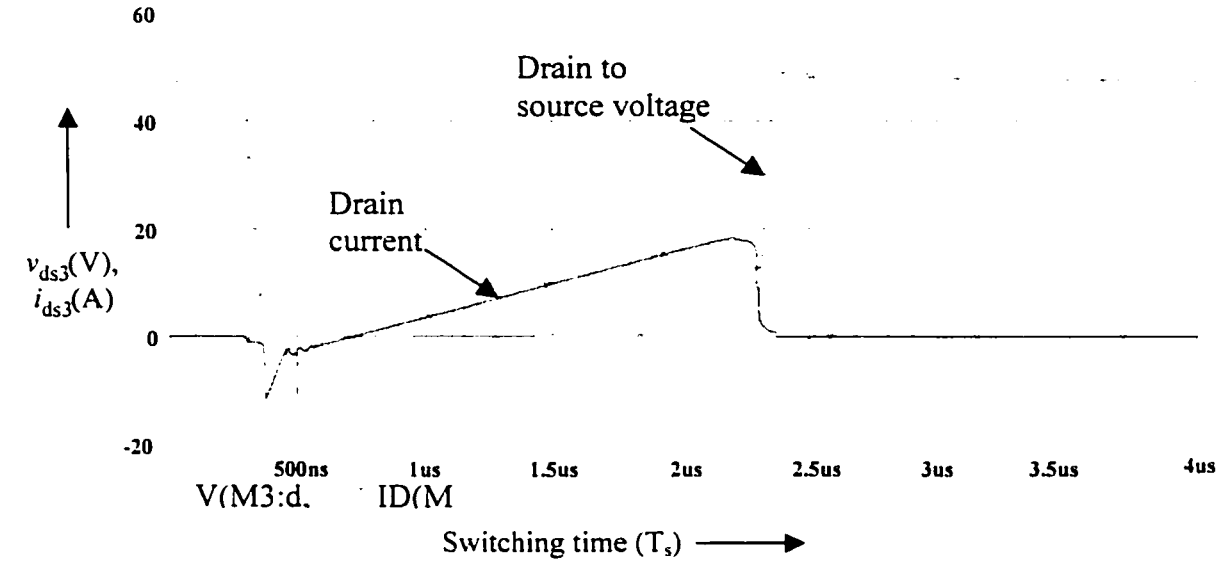


Fig. 3.6(a)

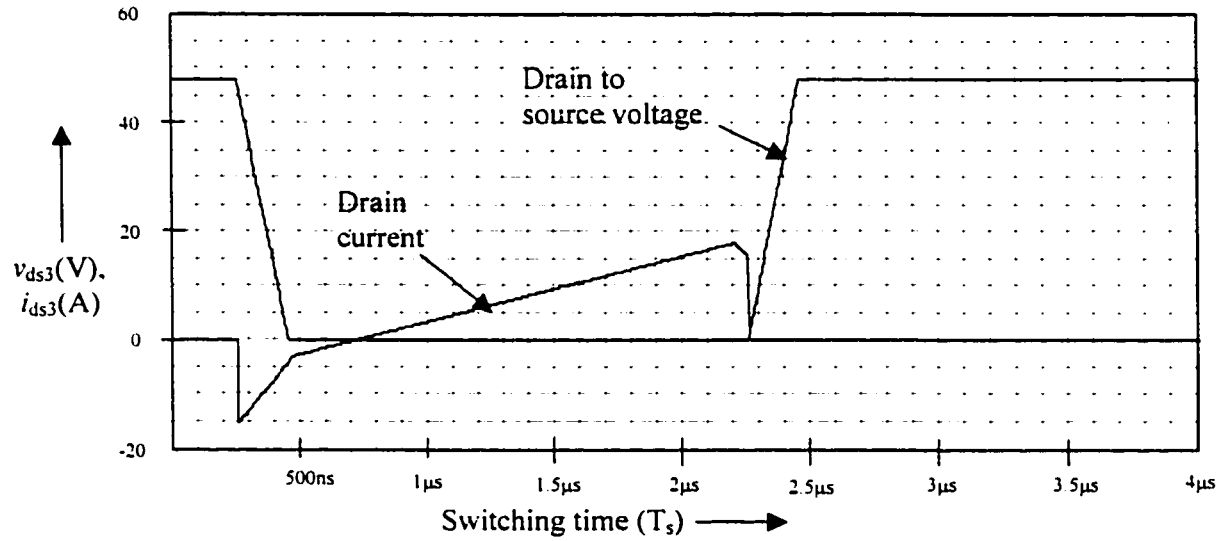


Fig. 3.6(b)

Fig. 3.6(a) Shows the simulation result for the turn-on and turn-off for switch (S_3) at full load at V_d=48V, V_o = 1.6V and I_o=150A with C_{sb1},C_{sb2},C_{sb3},C_{sb4}=10nF, L_{aux}=2μH and L_{Lk}=0.5μH. Fig. 3.6(b) Shows the result for the same values done by analysis.

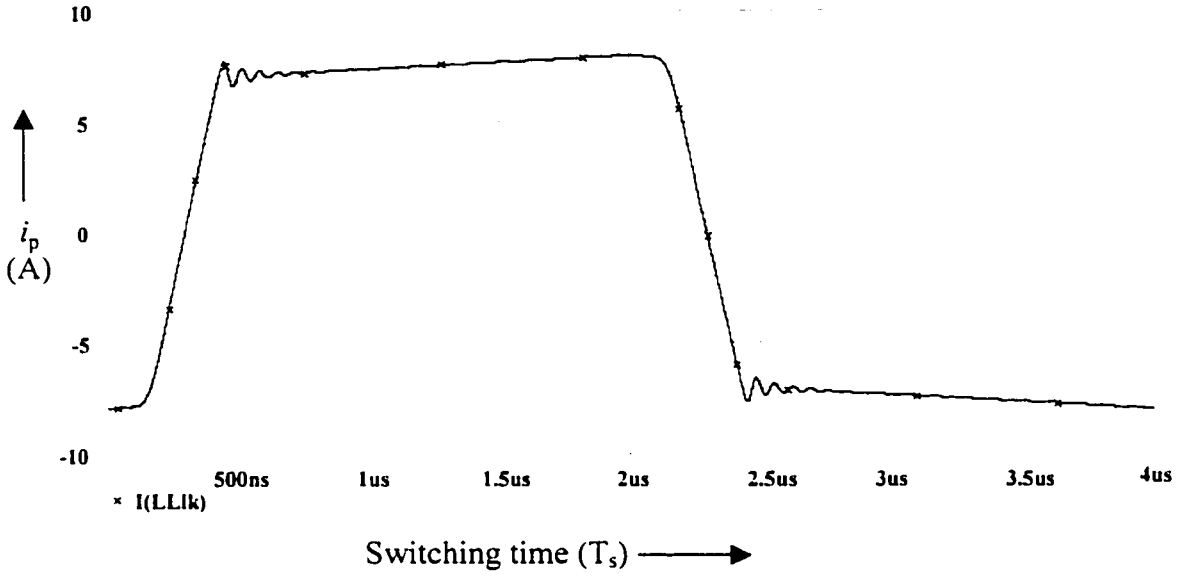


Fig. 3.7(a)

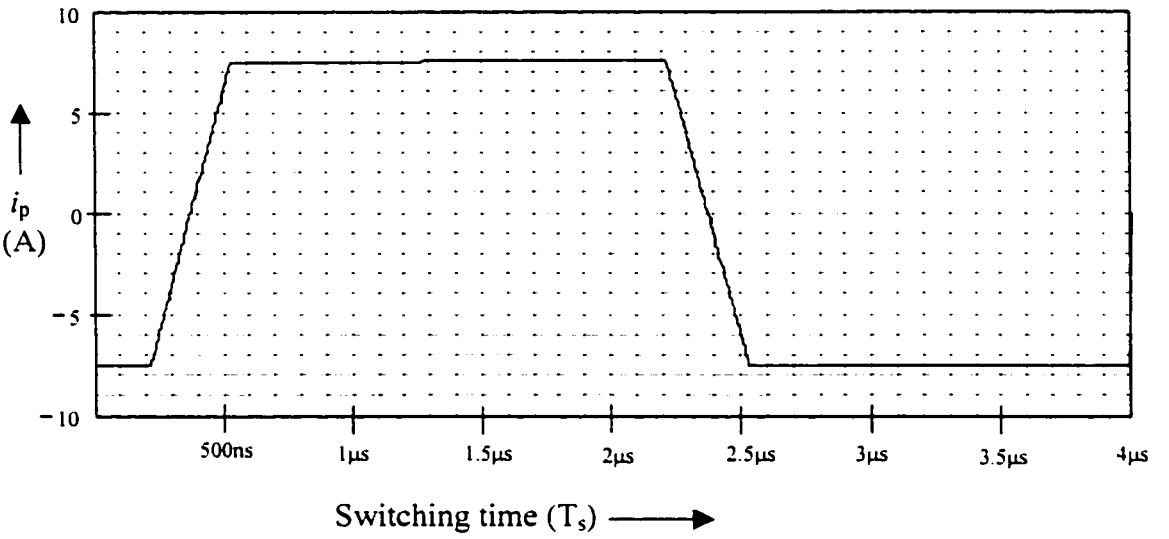


Fig. 3.7(b)

Fig. 3.7(a) Shows the simulation result for the primary current (i_p) at full load at V_d=48V, V_o = 1.6V and I_o=150A with C_{sb1},C_{sb2},C_{sb3},C_{sb4}=10nF, L_{aux}=18μH and L_{Llk}=1μH. Fig. 3.7(b) Shows the result for the same values done by analysis.

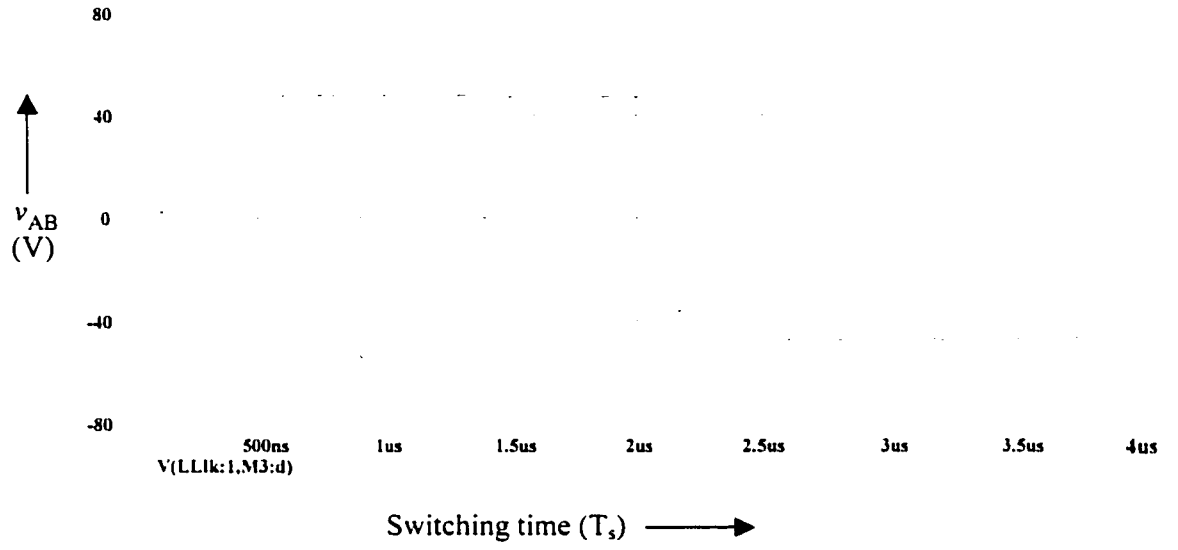


Fig. 3.8(a)

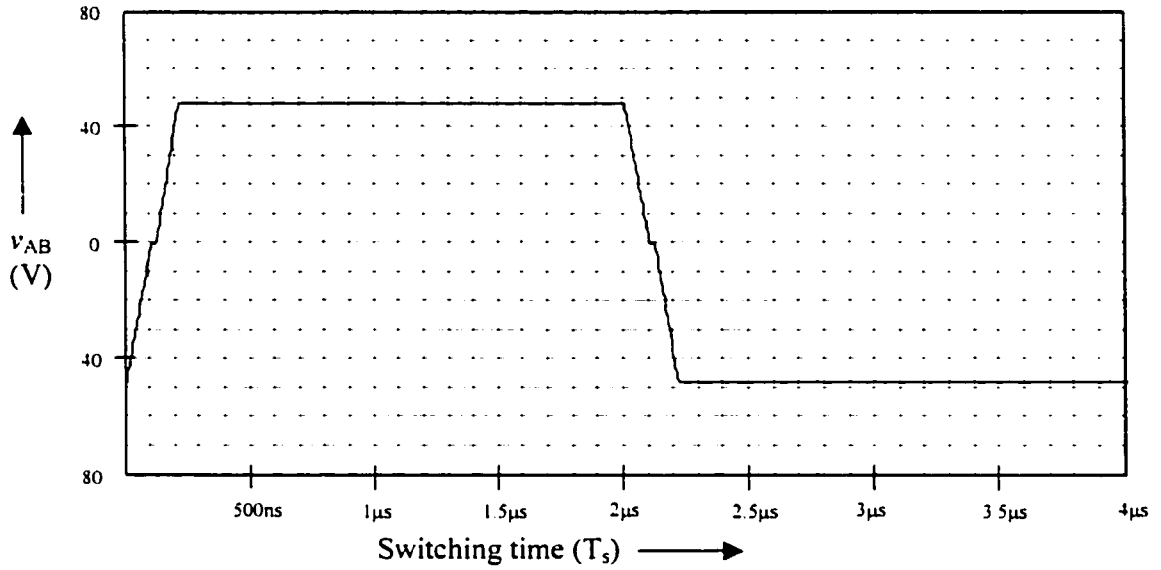


Fig. 3.8(b)

Fig. 3.8(a) Shows the simulation result for the full bridge voltage (v_{AB}) at full load at V_d=48V, V_o = 1.6V and I_o=150A with $C_{sb1}, C_{sb2}, C_{sb3}, C_{sb4}$=10nF, L_{aux}=18μH and L_{Lik}=1μH. Fig. 3.8(b) Shows the result for the same values done by analysis.

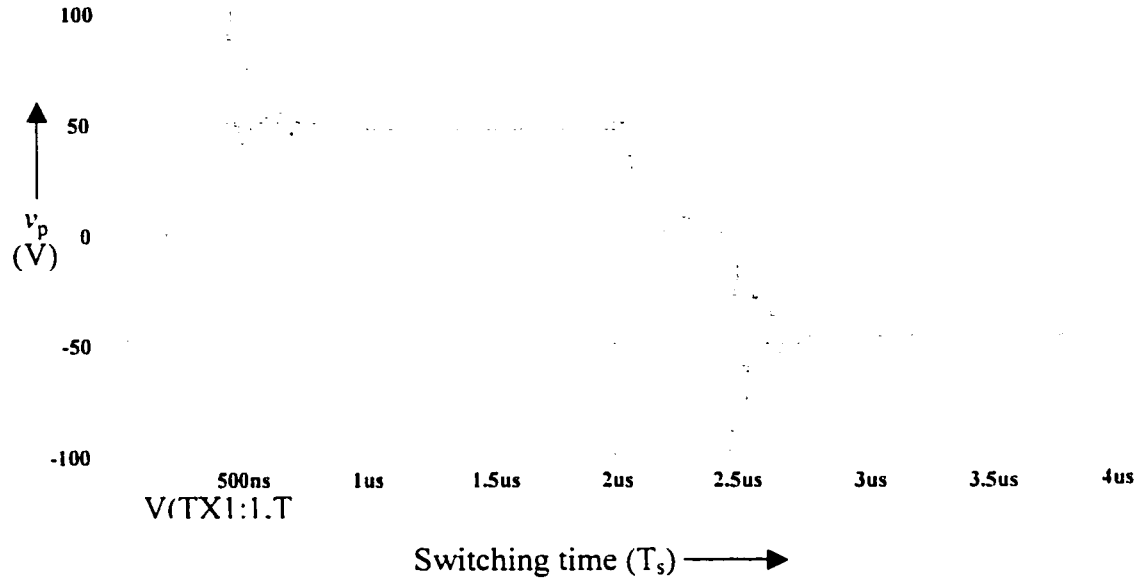


Fig. 3.9(a)

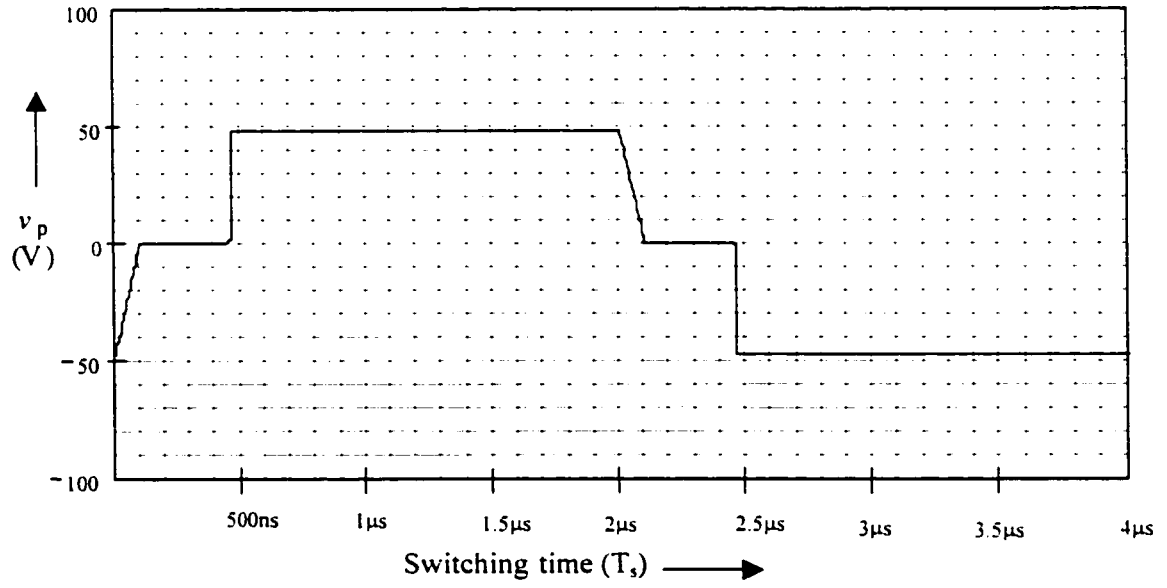


Fig. 3.9(b)

Fig. 3.9(a) Shows the simulation result for the primary voltage (v_p) at full load at V_d=48V, V_o = 1.6V and I_o=150A with $C_{sb1}, C_{sb2}, C_{sb3}, C_{sb4}$=10nF, L_{aux}=18μH and L_{Lik}=1μH. Fig. 3.9(b) Shows the result for the same values done by analysis.

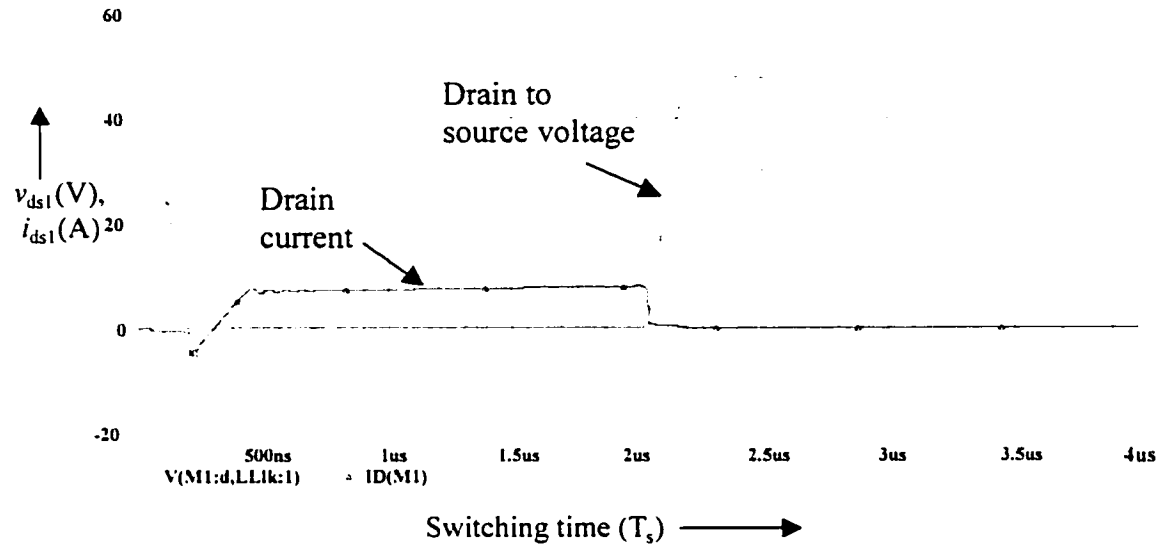


Fig. 3.10(a)

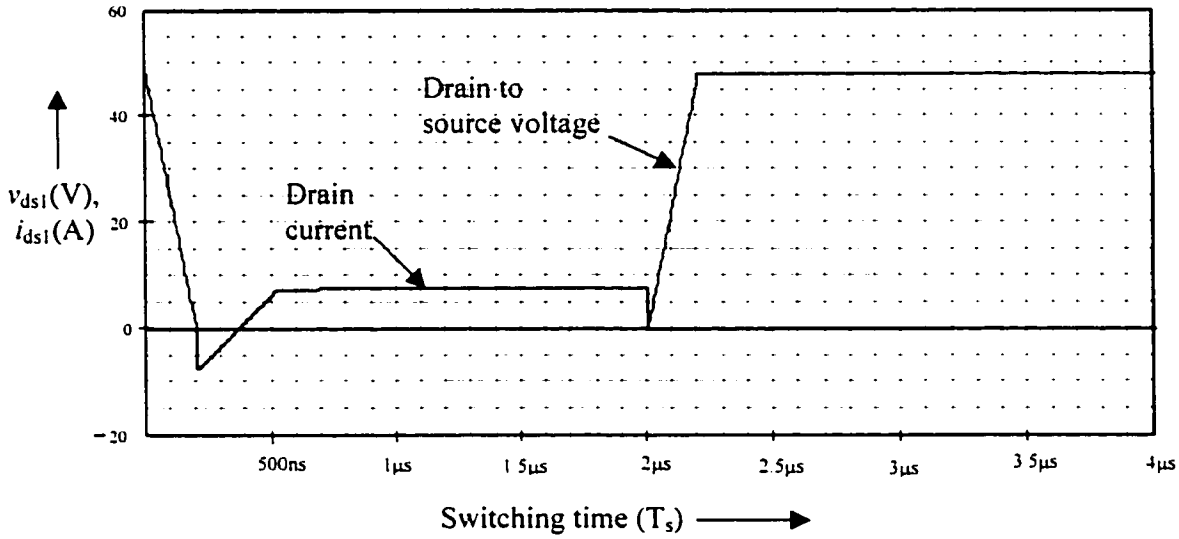


Fig. 3.10(b)

Fig. 3.10(a) Shows the simulation result for the turn-on and turn-off for switch (S_1) at full load at V_d=48V, V_o = 1.6V and I_o=150A with C_{sb1}, C_{sb2}, C_{sb3}, C_{sb4}=10nF, L_{aux}=18µH and L_{Lk}=1µH. Fig. 3.10(b) Shows the result for the same values done by analysis.

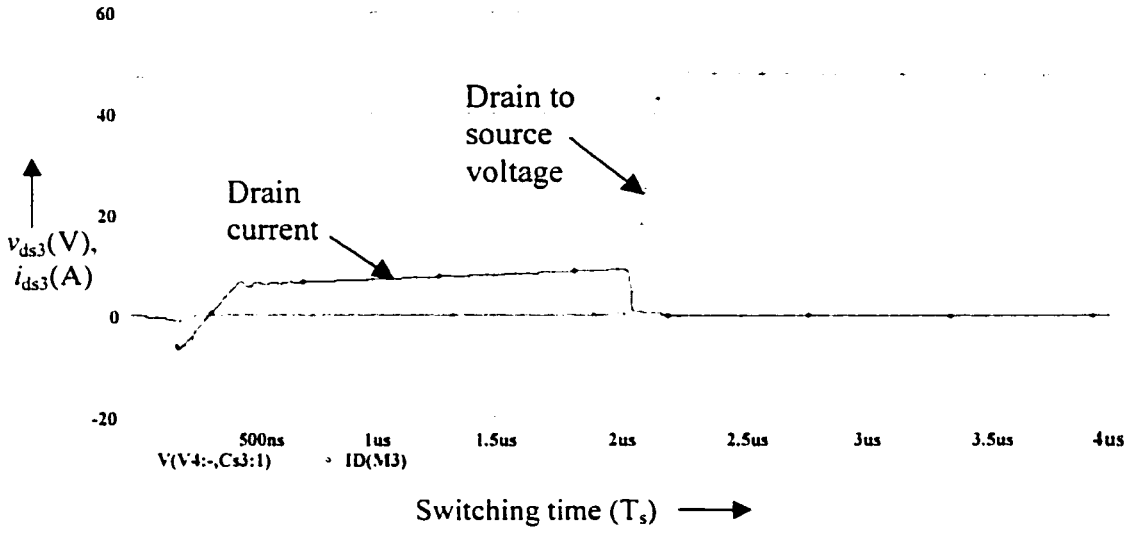


Fig. 3.11(a)

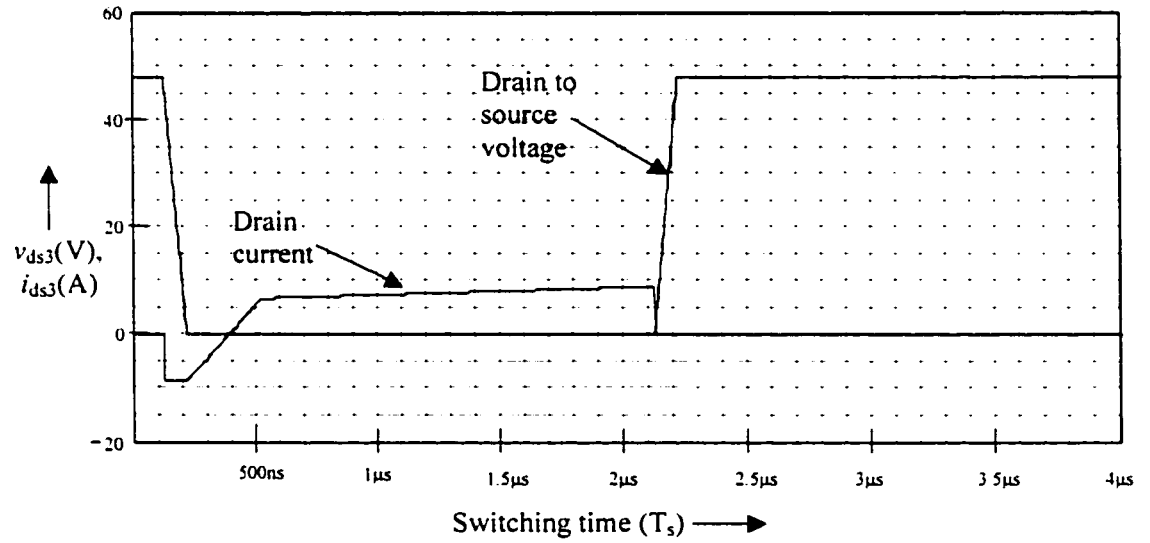


Fig. 3.11(b)

Fig. 3.11(a) Shows the simulation result for the turn-on and turn-off for switch (S_3) at full load at V_d=48V, V_o = 1.6V and I_o=150A with $C_{sb1}, C_{sb2}, C_{sb3}, C_{sb4}$=10nF, L_{aux}=18µH and L_{Lik}=1µH. Fig. 3.11(b) Shows the result for the same values done by analysis.

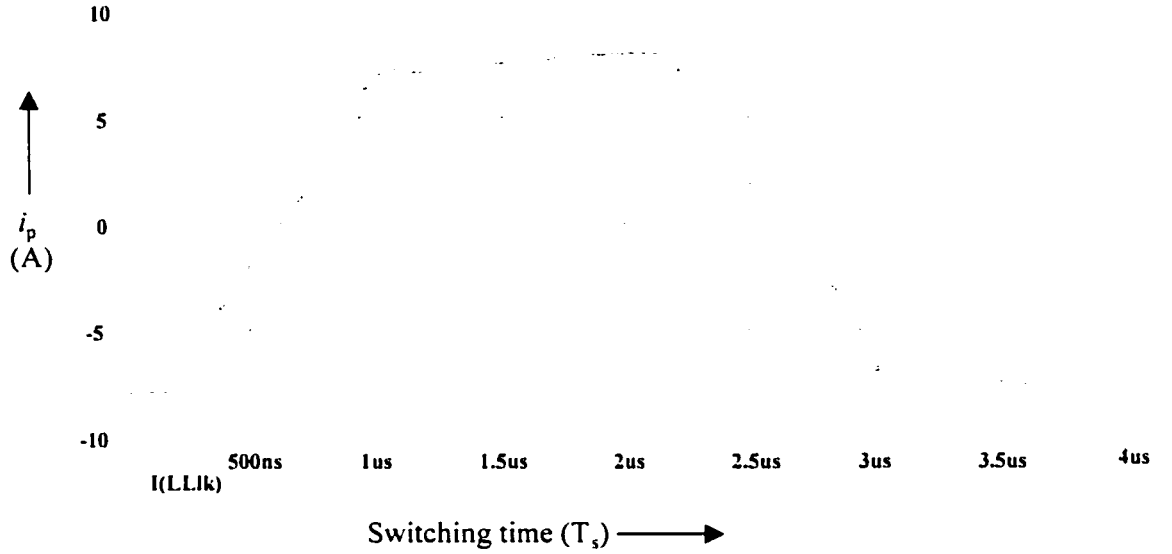


Fig. 3.12(a)

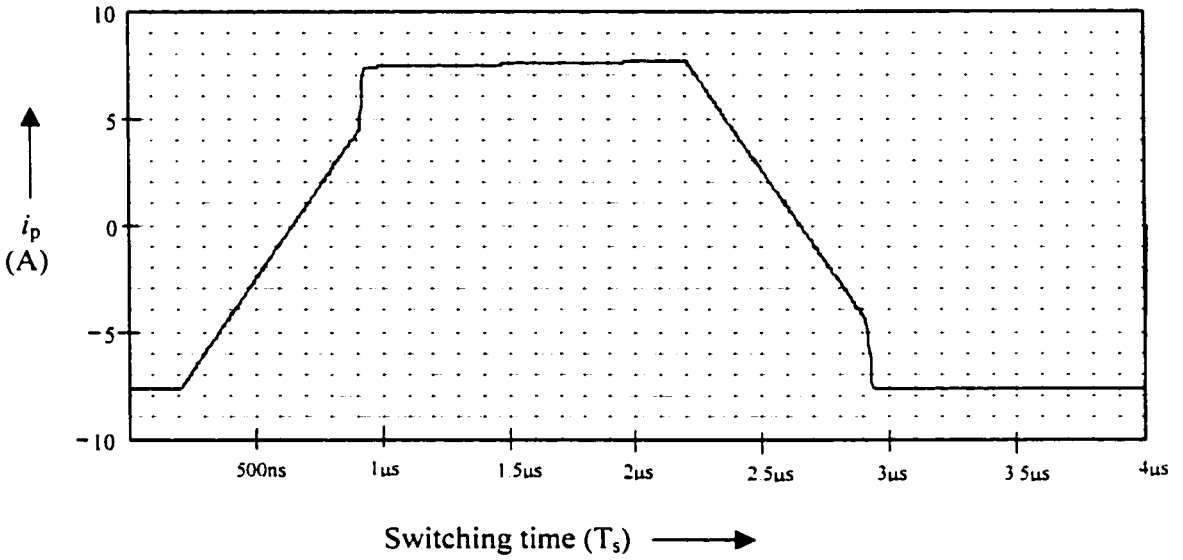


Fig. 3.12(b)

Fig. 3.12(a) Shows the simulation result for the primary current (i_p) at full load at V_d=72V, V_o = 1.6V and I_o=150A with C_{sb1},C_{sb2},C_{sb3},C_{sb4}=5nF, L_{aux}=2µH and L_{Lk}=0.5µH. Fig. 3.12(b) Shows the result for the same values done by analysis.

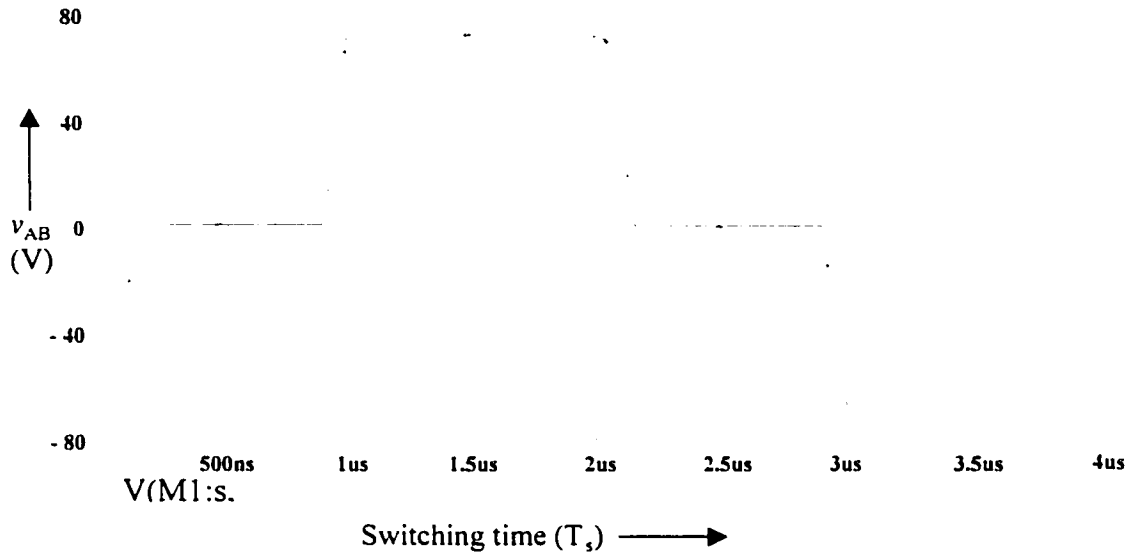


Fig. 3.13(a)

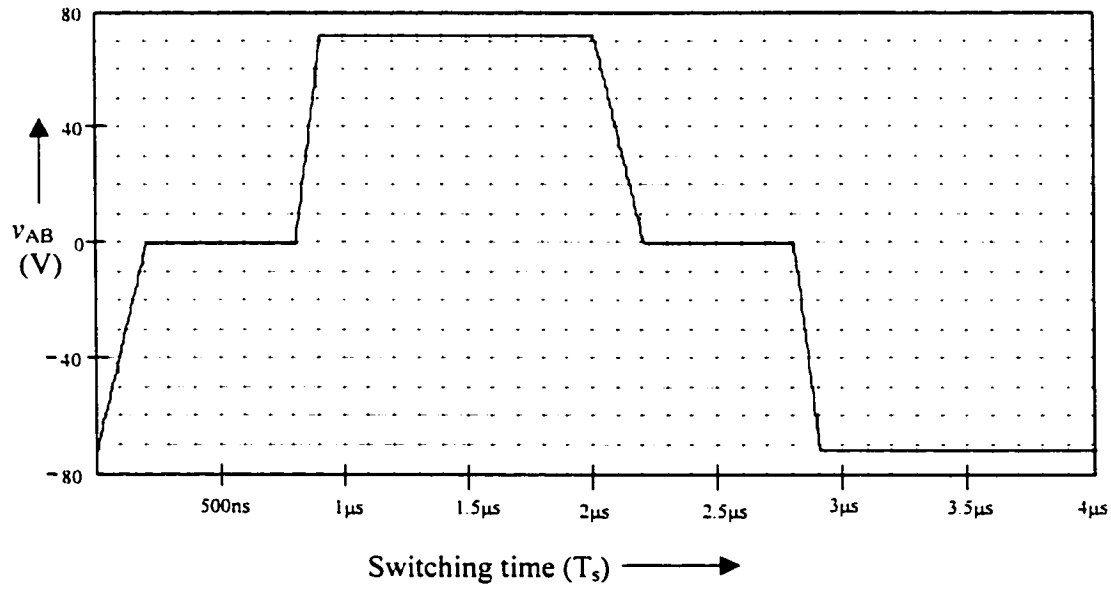


Fig. 3.13(b)

Fig. 3.13(a) Shows the simulation result for the full bridge voltage (v_{AB}) at full load at V_d=72V, V_o = 1.6V and I_o=150A with C_{sb1}, C_{sb2}, C_{sb3}, C_{sb4}=5nF, L_{aux}=2μH and L_{Lk}=0.5μH. Fig. 3.13(b) Shows the result for the same values done by analysis.

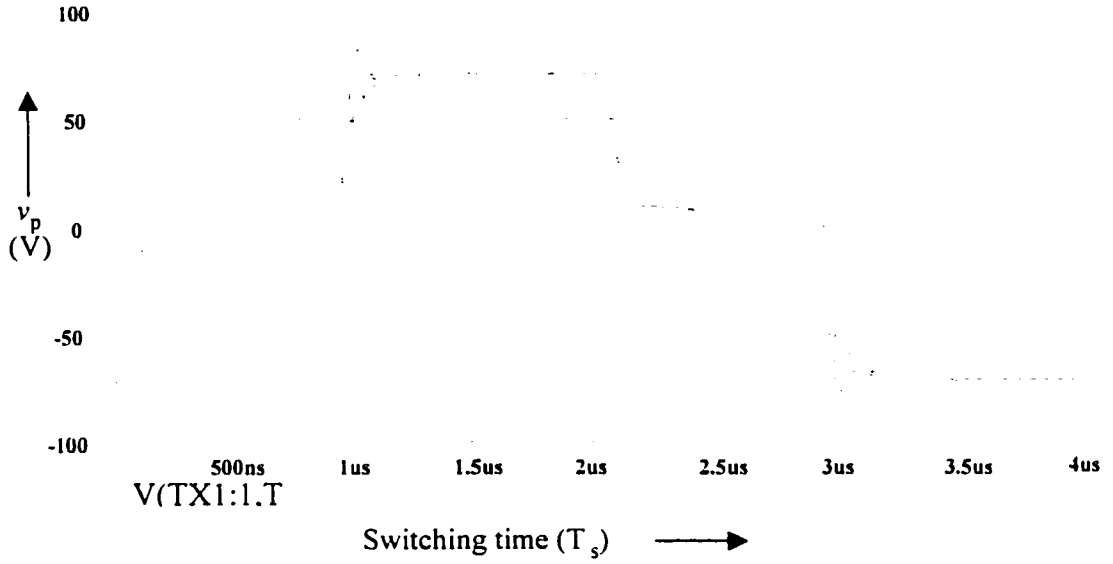


Fig. 3.14(a)

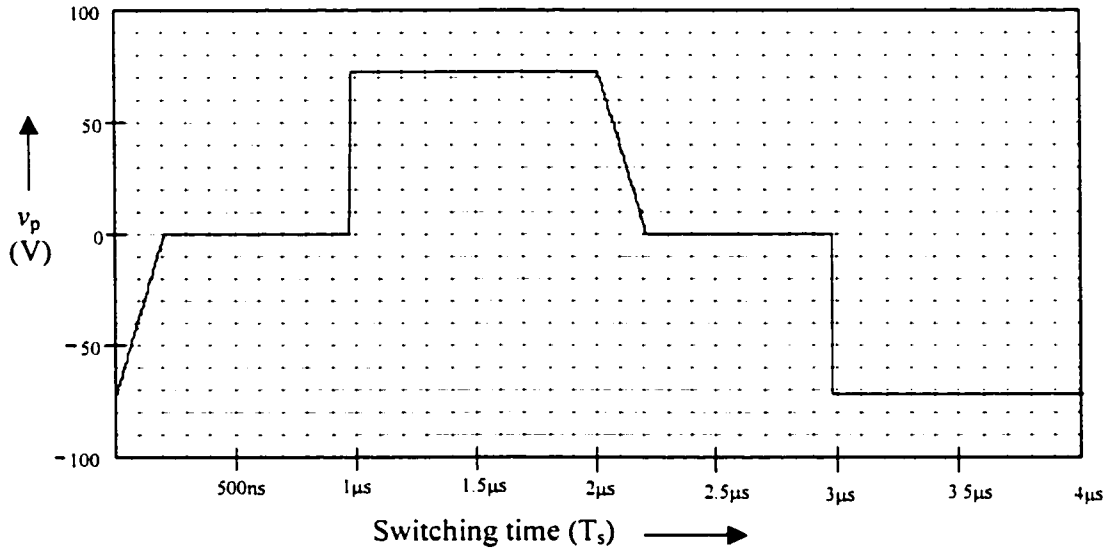


Fig. 3.14(b)

Fig. 3.14(a) Shows the simulation result for the full bridge voltage (v_p) at full load at V_d=72V, V_o = 1.6V and I_o=150A with C_{sb1}, C_{sb2}, C_{sb3}, C_{sb4}=5nF, L_{aux}=2μH and L_{Lk}=0.5μH. Fig. 3.14(b) Shows the result for the same values done by analysis.

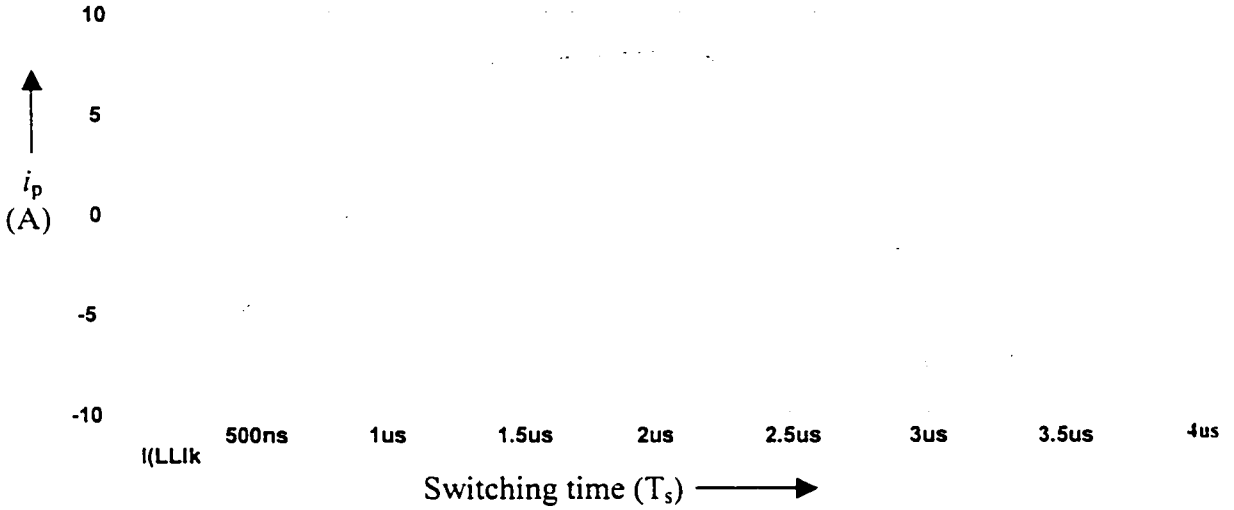


Fig. 3.15(a)

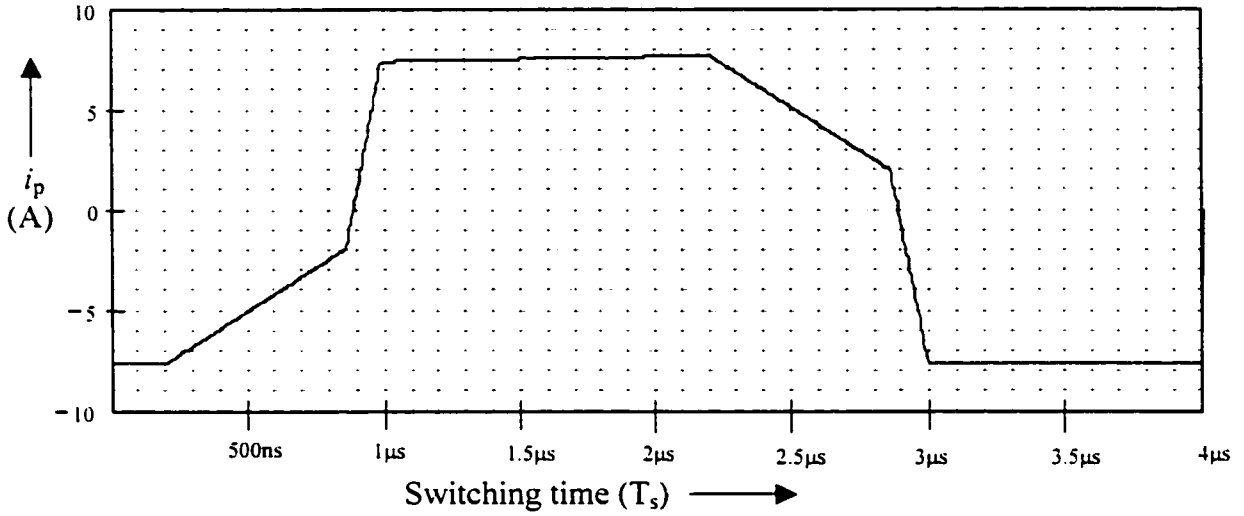


Fig. 3.15(b)

Fig. 3.15(a) Shows the simulation result for the primary current (i_P) at full load at V_d=72V, V_o = 1.6V and I_o=150A with C_{sb1},C_{sb2},C_{sb3},C_{sb4}=5nF, L_{aux}=4μH and L_{Lk}=1μH. Fig. 3.15(b) Shows the result for the same values done by analysis.

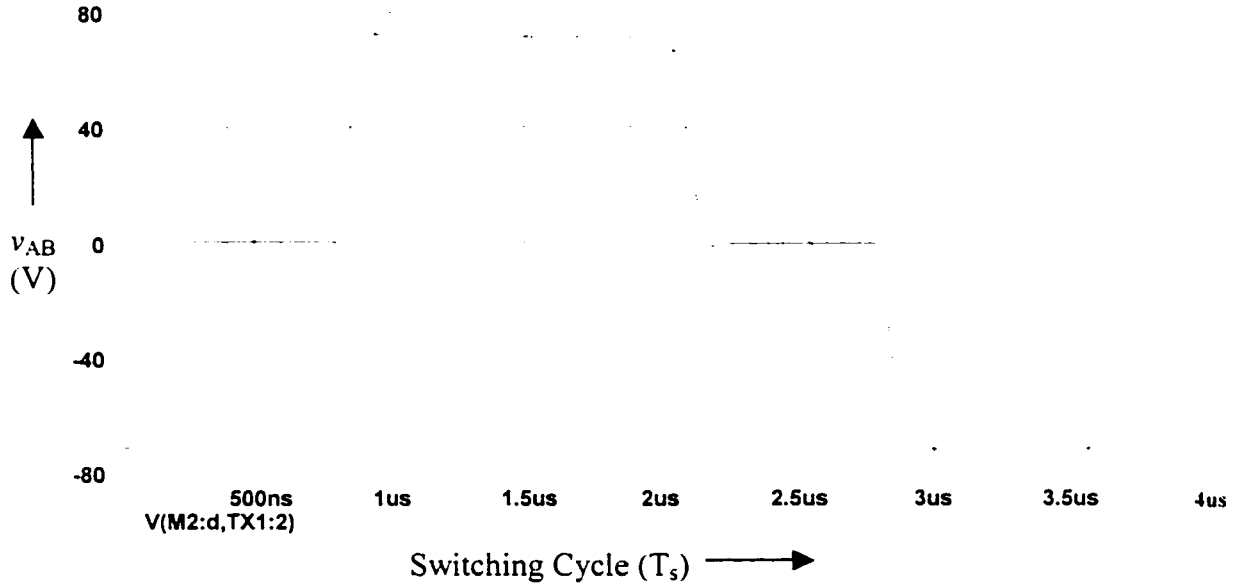


Fig. 3.16(a)

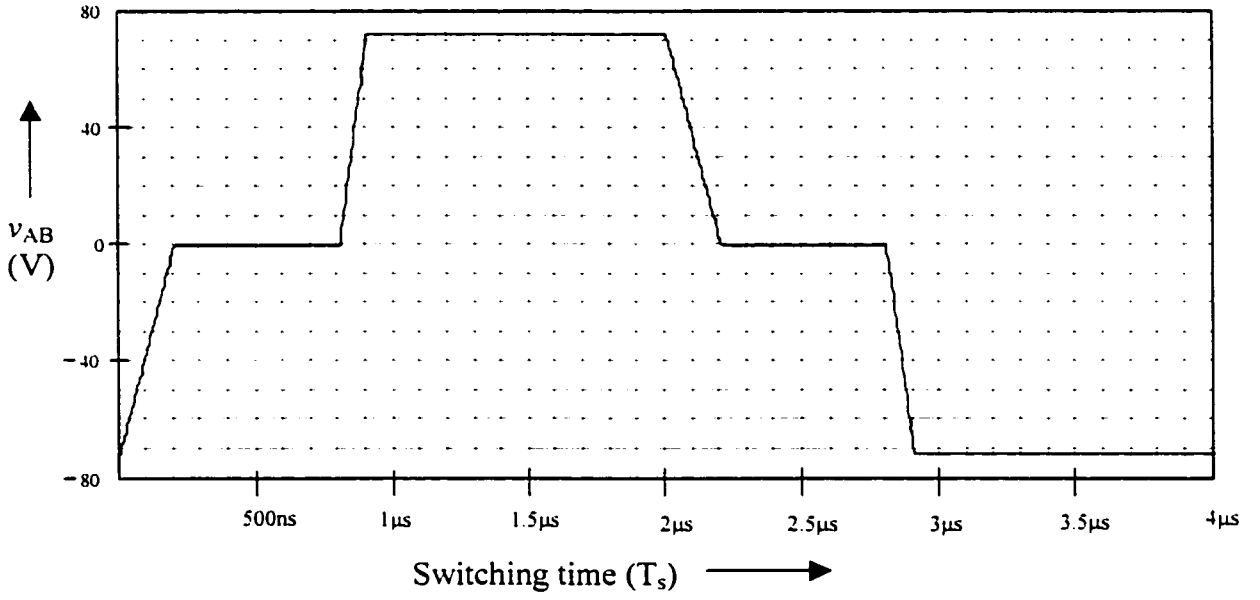


Fig. 3.16(b)

Fig. 3.16(a) Shows the simulation result for the full bridge voltage (v_{AB}) at full load at V_d=72V, V_o = 1.6V and I_o=150A with C_{sb1},C_{sb2},C_{sb3},C_{sb4}=5nF, L_{aux}=4μH and L_{Llk}=1μH. Fig. 3.16(b) Shows the result for the same values done by analysis.

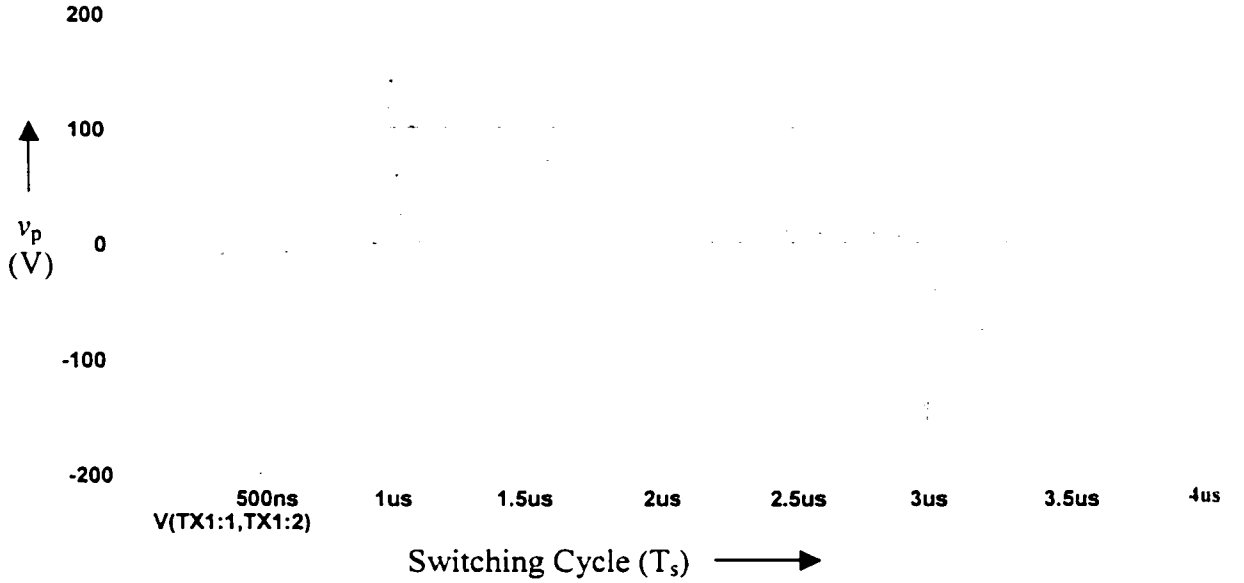


Fig. 3.17(a)

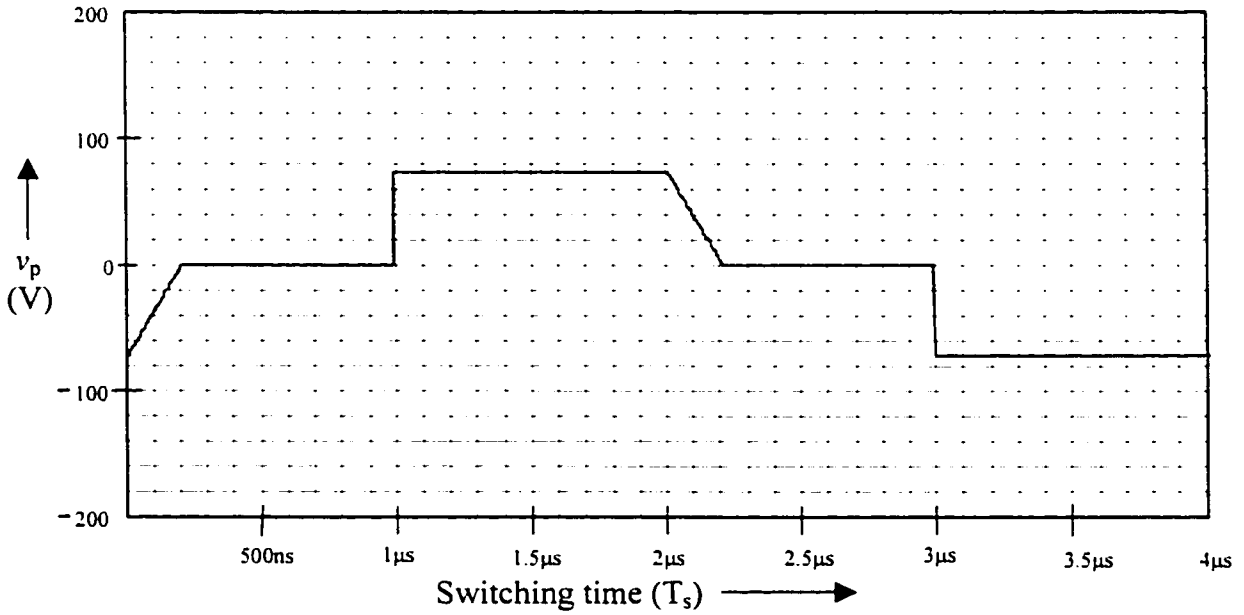


Fig. 3.17(b)

Fig. 3.17(a) Shows the simulation result for the full bridge voltage (v_p) at full load at V_d=72V, V_o = 1.6V and I_o=150A with C_{sb1}, C_{sb2}, C_{sb3}, C_{sb4}=5nF, L_{aux}=4μH and L_{Lik}=1μH. Fig. 3.17(b) Shows the result for the same values done by analysis.

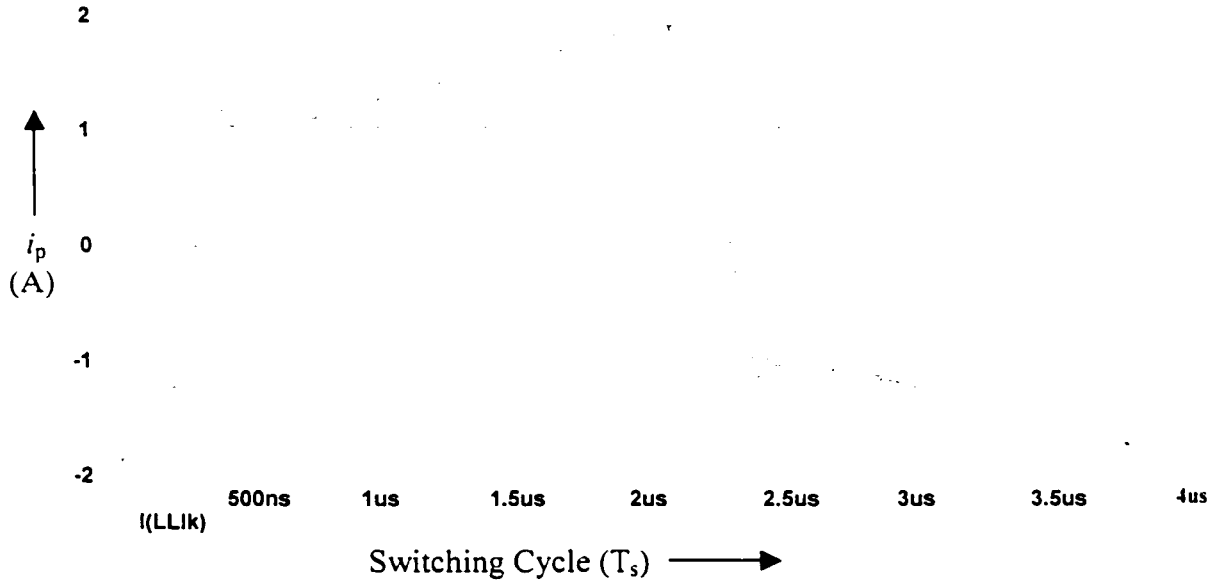


Fig. 3.18(a)

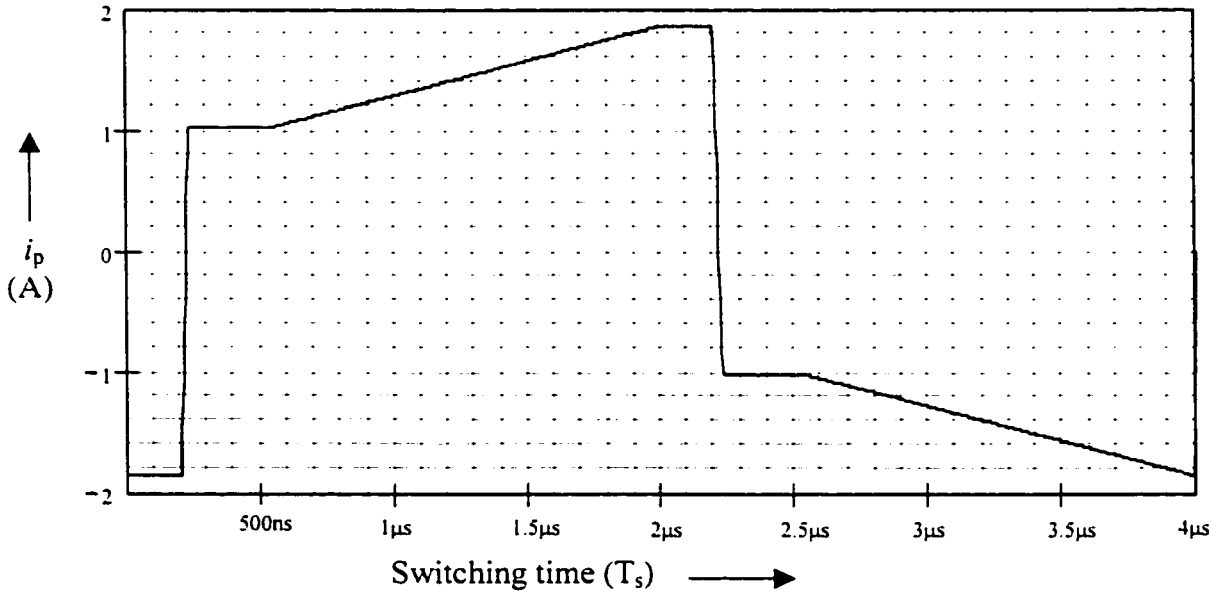


Fig. 3.18(b)

Fig. 3.18(a) Shows the simulation result for the primary current (i_p) at 20% load at V_d =48V, V_o = 1.6V and I_o=30A with C_{sb1},C_{sb2},C_{sb3},C_{sb4}=1nF, L_{aux}=8μH and L_{Llk}=0.5μH. Fig. 3.18(b) Shows the result for the same values done by analysis.

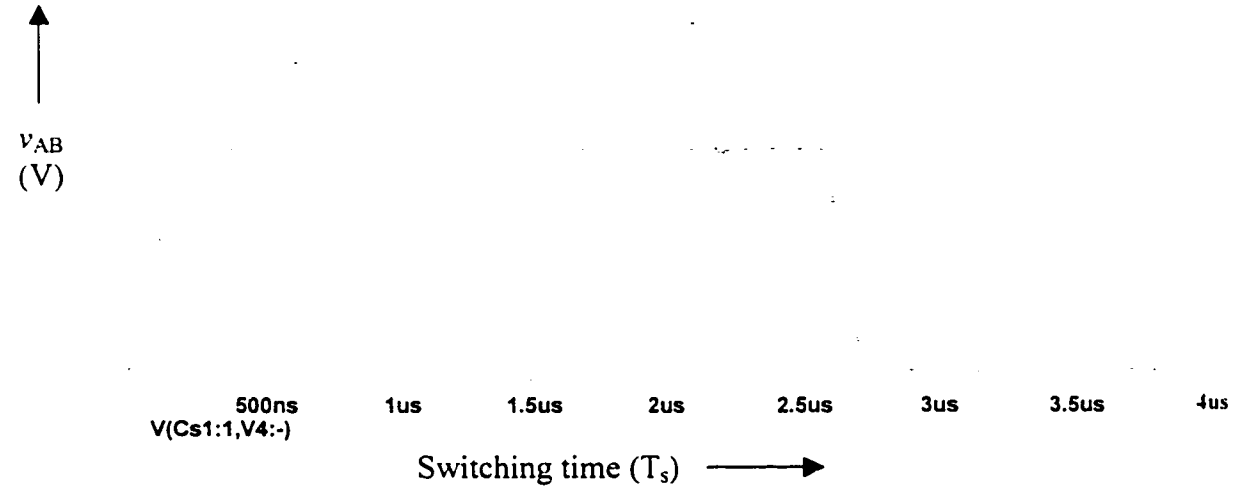


Fig. 3.19(a)

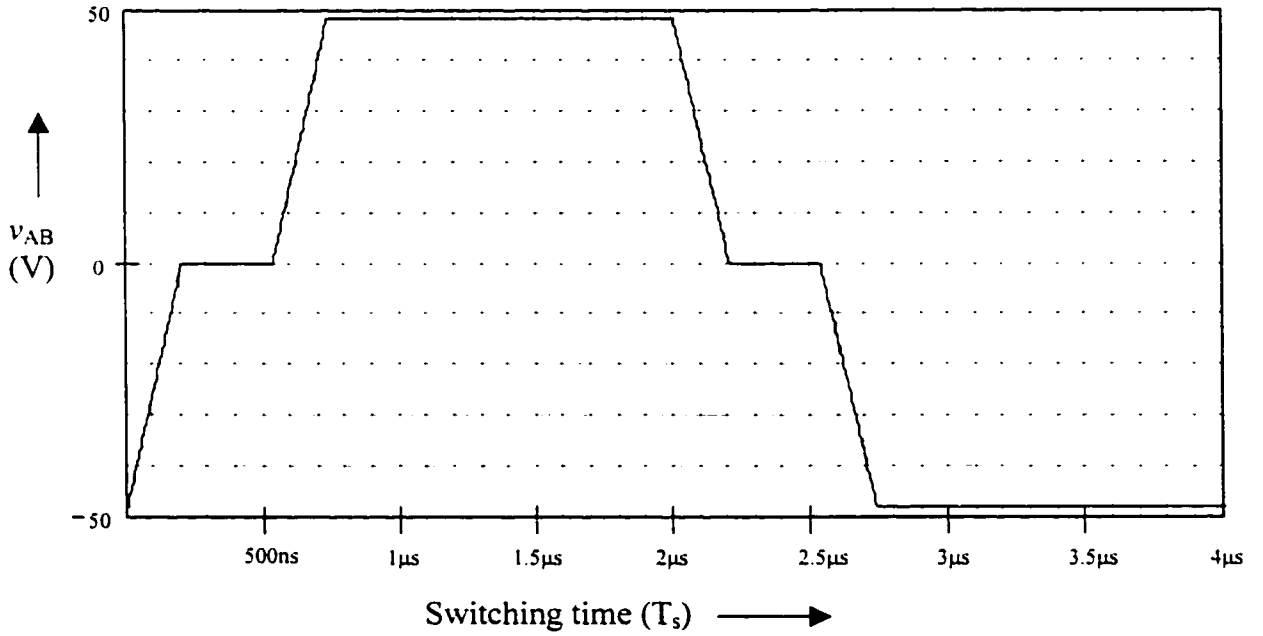


Fig. 3.19(b)

Fig. 3.19(a) Shows the simulation result for the full bridge voltage (v_{AB}) at 20% load at V_d=48V, V_o = 1.6V and I_o=30A with C_{sb1},C_{sb2},C_{sb3},C_{sb4}=1nF, L_{aux}=8μH and L_{Lik}=0.5μH. Fig. 3.19(b) Shows the result for the same values done by analysis.

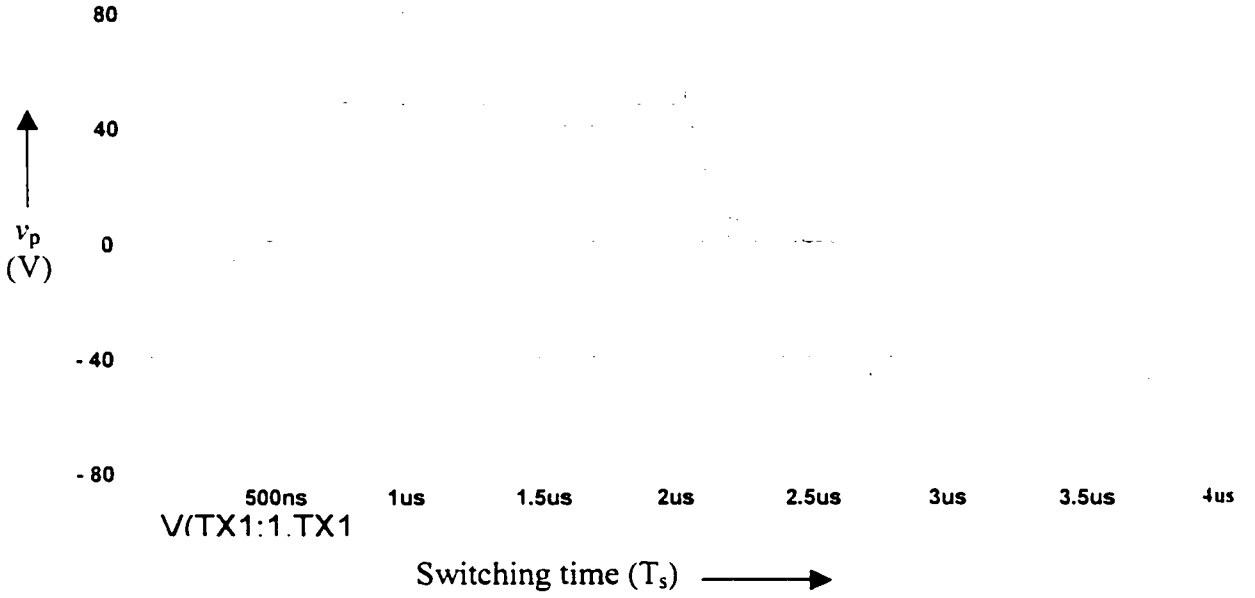


Fig. 3.20(a)

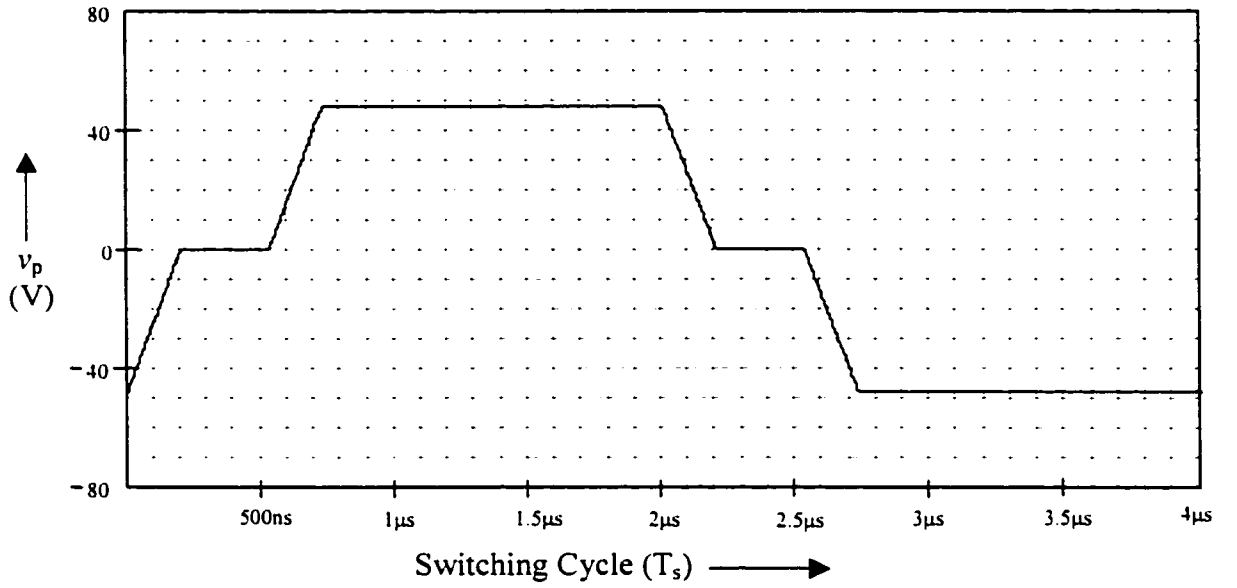


Fig. 3.20(b)

Fig. 3.20(a) Shows the simulation result for the primary voltage (v_p) at 20% load at V_d=48V, V_o = 1.6V and I_o=30A with C_{sb1},C_{sb2},C_{sb3},C_{sb4}=1nF, L_{aux}=8μH and L_{Lk}=0.5μH. Fig. 3.20(b) Shows the result for the same values done by analysis.

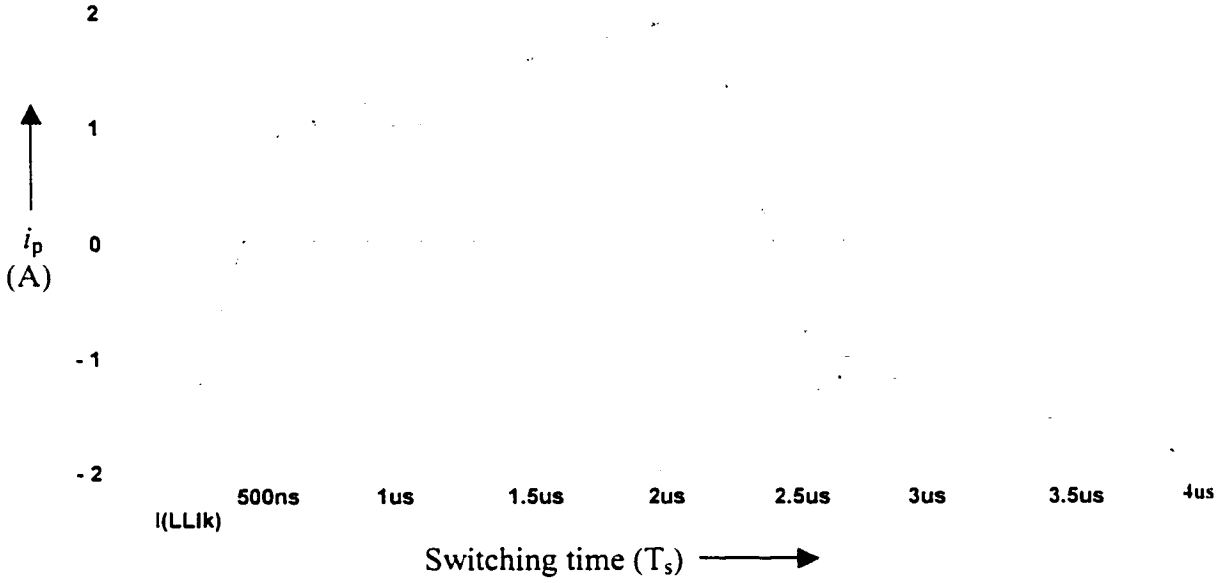


Fig. 3.21(a)

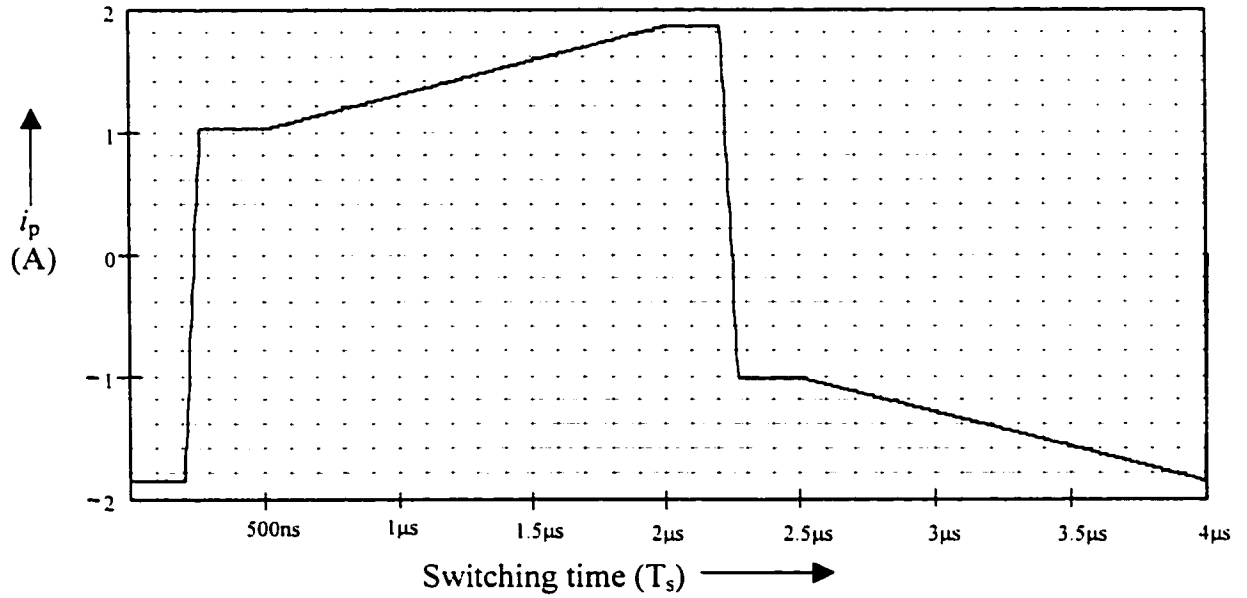


Fig. 3.21(b)

Fig. 3.21(a) Shows the simulation result for the primary current (i_p) at 20% load at V_d=48V, V_o = 1.6V and I_o=30A with C_{sb1},C_{sb2},C_{sb3},C_{sb4}=1nF, L_{aux}=8μH and L_{Llk}=1μH. Fig. 3.21(b) Shows the result for the same values done by analysis.

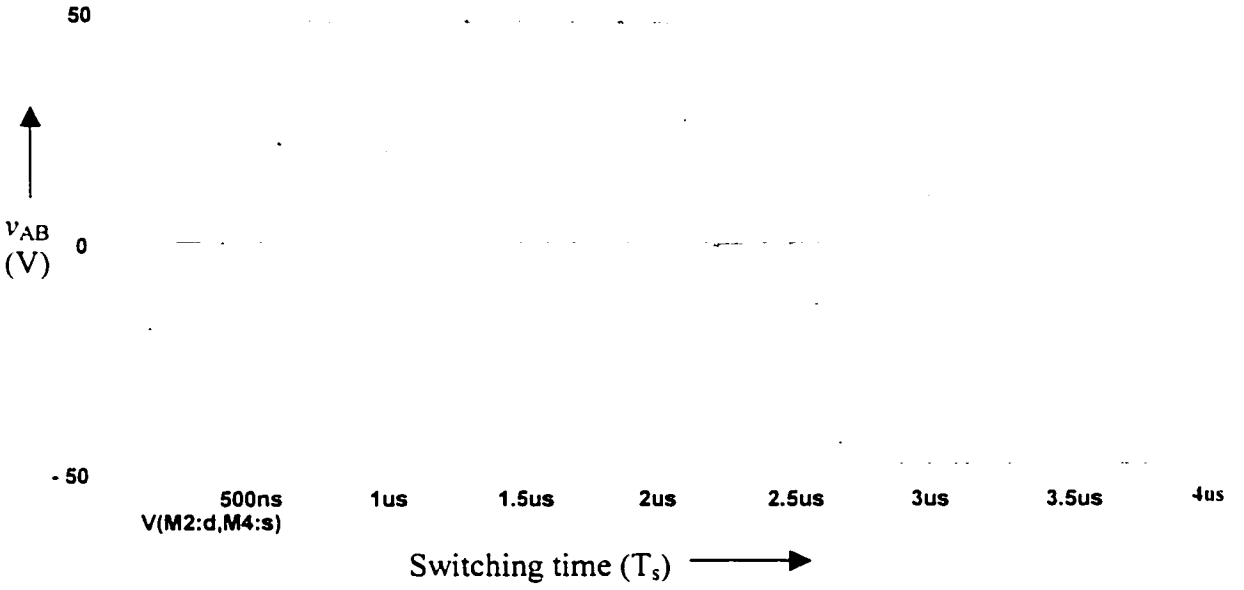


Fig. 3.22(a)

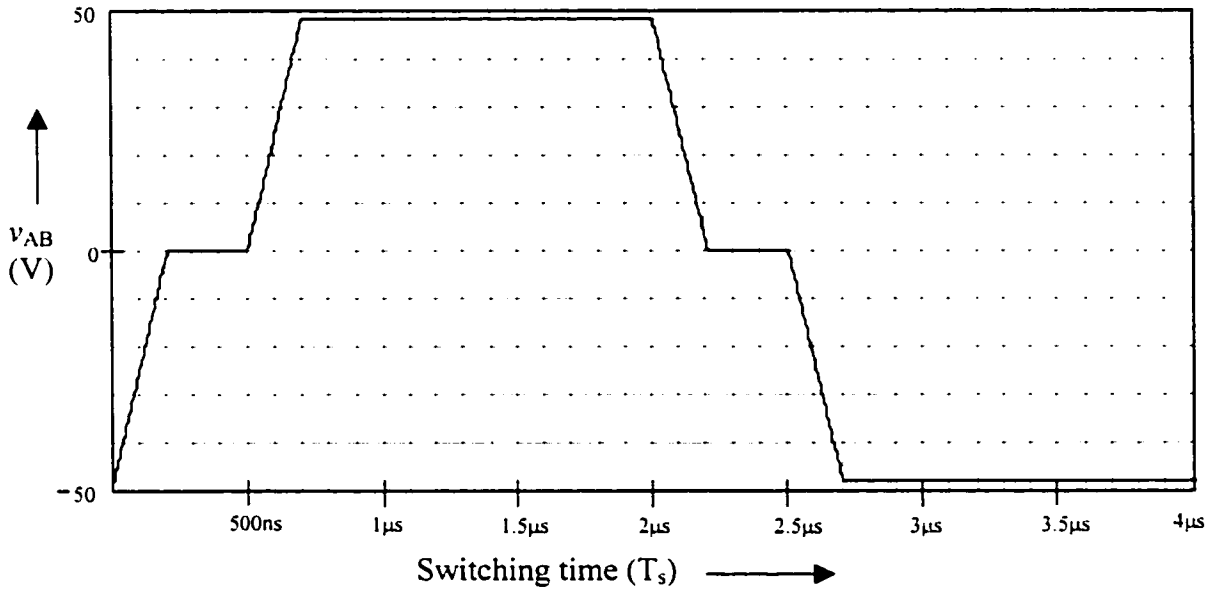


Fig. 3.22(b)

Fig. 3.22(a) Shows the simulation result for the full bridge voltage (v_{AB}) at 20% load at V_d=48V, V_o = 1.6V and I_o=30A with C_{sb1}, C_{sb2}, C_{sb3}, C_{sb4}=1nF, L_{aux}=8μH and L_{Lk}=1μH. Fig. 3.22(b) Shows the result for the same values done by analysis.

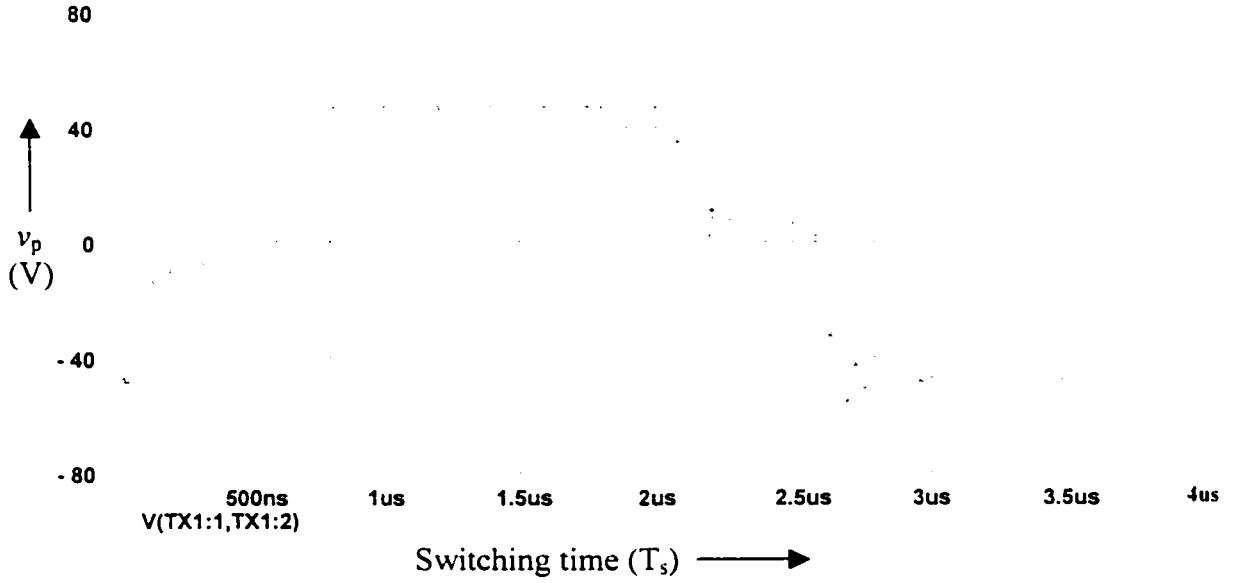


Fig. 3.23(a)

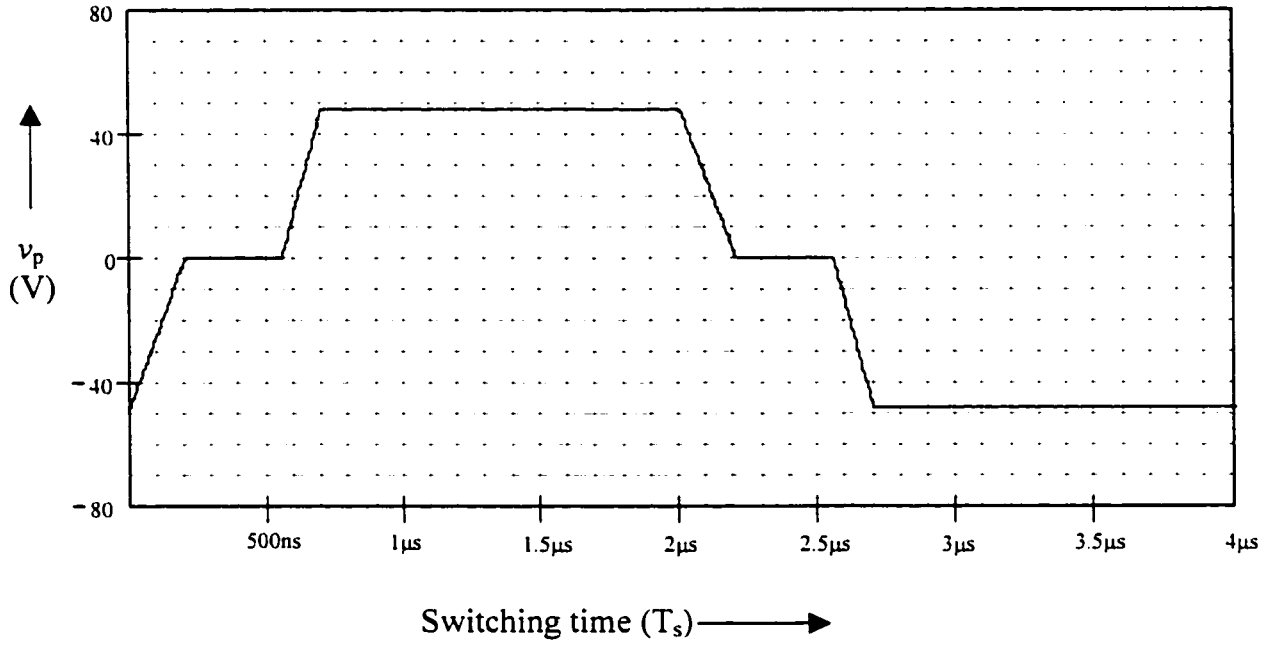


Fig. 3.23(b)

Fig. 3.23(a) Shows the simulation result for the primary voltage (v_P) at 20% load at V_d=48V, V_o = 1.6V and I_o=30A with C_{sb1},C_{sb2},C_{sb3},C_{sb4}=1nF, L_{aux}=8μH and L_{Lk}=1μH. Fig. 3.23(b) Shows the result for the same values done by analysis.

3.11(a) has less current than Fig. 3.6(b), Fig. 3.11(b). This is because in the analysis it is assumed that the auxiliary current is constant during the charging and discharging for the switches in *leg A*. But in reality the auxiliary current is not constant.

Table 3.1 Principal parameters of the simulation circuit

parameter	value	parameter	value
k	10:1	t_d	200ns
C_{V1}, C_{V2}	8μF	L_1, L_2	2μH
S_1, S_2, S_3, S_4	IRFP150	S_{R1}, S_{R2}	IRL3803

3.4 Conclusions

In this chapter the detailed analysis has been performed and the equations are derived for the different modes. The analysis is done by including the effect of transformer's leakage inductance to optimize the performance.

The theoretical and simulation results have been compared to verify the accuracy of the mathematical model defined by the equations in the previous section. Except the second order effects, such as ringing at the switching instants, the simulation results confirm the accuracy of the analysis performed in this chapter.

CHAPTER 4
CHARACTERISTICS CURVES

4.1 Introduction

In order to properly design the converter, characteristics curves showing the relationship between switch voltages, currents and various component values are needed. Using the analytical equations derived in Section 3.2 of Chapter 3 these curves can be drawn both for Mode 1 and for Mode 2. Due to the nature of equations in Section 3.2, the closed form solution of the equations can only be obtained by using an iterative method. So the Newton-Raphson method is implemented using a simple computer program built in Math CAD.

The achievement of efficient high-frequency power conversion requires reduction of switching losses. To achieve ZVS, the two legs of the bridge are operated with a phase shift. The proposed topology is a combination of a conventional full bridge converter, a small leakage inductor and one auxiliary circuit. The auxiliary circuit only consists of a few non-resistive passive components. To extend the soft-switching capability of the phase shifted full bridge converter under all load conditions, the auxiliary circuit is optimized with the inherent leakage inductance of the transformer. Also, for low voltage and high current output, a current doubler technique with synchronous rectification is used. As explained in Chapter 2, the external drive technique is employed in the rectification stage.

As it is stated in Chapters 1 through 3 that to get the ZVS in *leg B* there are two

ways to ensure the ZVS in all conditions. By using a series inductor can achieve ZVS even when there is a short circuit or overloading across the load but has some drawbacks: (i) loss of ZVS at no load or light load. When the load is light, the primary current is low, and consequently the stored energy is also low. This energy is not sufficient to discharge the snubber capacitor in the dead time. Thus, ZVS is lost at turn-on. (ii) This series inductor not only produces unacceptable high conduction losses when the load is high but also prevents slower changes of primary current polarity, which is responsible for decrease in the effective duty- cycle.

The other topology is by using auxiliary inductors to provide additional current to discharge the snubber capacitor of the switches and can achieve ZVS in any load and line condition. However, it has following drawback: (i) it provides zero voltage switching with the expense of some conduction losses due to additional auxiliary inductor. It is suitable for high voltage and low current applications but the conduction losses are pronounced in low voltage and higher current applications.

The proposed topology shown in Fig. 2.1 does not suffer from these drawbacks. The optimization of auxiliary inductor L_{aux} and transformer leakage inductor L_{Lk} has been proposed to achieve Zero Voltage Switching (ZVS) in *leg B* under all load and line conditions. For *leg A*, primary current is sufficient to achieve ZVS. The topology is simple and requires a minimum number of components.

It is clear from the analysis in Section 3.2 of Chapter 3 that the duty loss (ΔD) is depends on the value of leakage inductance (L_{Lk}). It is also known from the analysis that the design considerations for both the legs have different line and load conditions. The worst condition for each leg has been defined.

The outline of this chapter is as follows:

Section 4.2 presents the characteristics curves for effective duty cycle (D_{eff}) versus leakage inductance (L_{Llk}) at different values of D.

Section 4.3 gives the characteristics curves for *leg A* and *leg B* for the worst conditions.

The main points of this chapter are summarized and some conclusions are made in Section 4.4.

4.2 Choice of switching frequency, leakage inductance and duty cycle

As stated earlier the leakage inductor (L_{Llk}) must be kept at its minimum value in order to achieve optimum efficiency of the circuit. An inductor higher than the minimum value will lower the effective duty cycle of the power circuit, eventually resulting in lower turns ratio. This increases the reflected output current value on the primary side and the voltage stress of the secondary side rectifier devices, both leading towards lower overall efficiency of the circuit.

From equation 3-1 of Chapter 3 the effective duty cycle as a function of leakage inductance (L_{Llk}) at different values of primary duty cycle (D) is given by:

$$D_{eff} = \frac{D}{\left[1 + \frac{L_{Llk} \cdot f_s}{k^2 \cdot R_o}\right]} \tag{4-1}$$

A graph shown in Fig. 4.1 shows the effect of leakage inductance (L_{Llk}) for the proposed ZVS full bridge with synchronous rectification topology at full load.

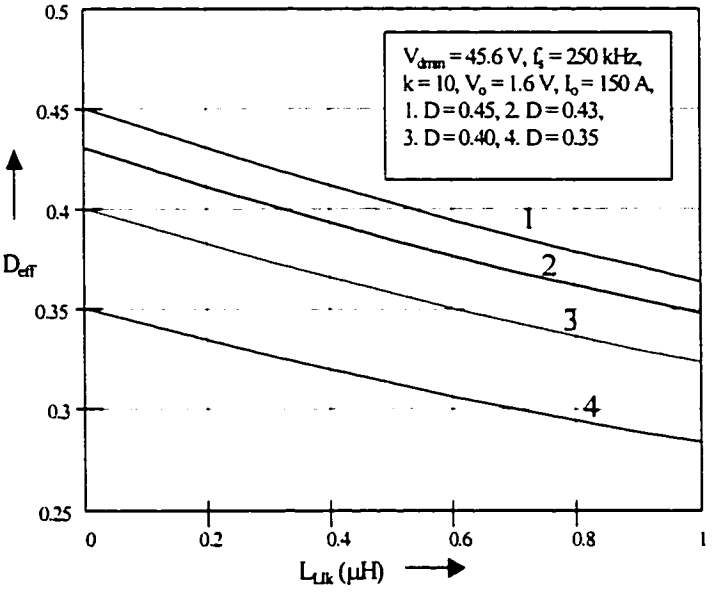


Fig. 4.1 Effective duty cycle (D_{eff}) versus leakage inductance (L_{Lk}) at full load.

The graph shown in Fig. 4.2 shows the effect of leakage inductance on effective duty cycle at reduced load and full-load. It is found that the variation in the effective duty cycle is more at full load. So, for the design point of view effective duty cycle (D_{eff})

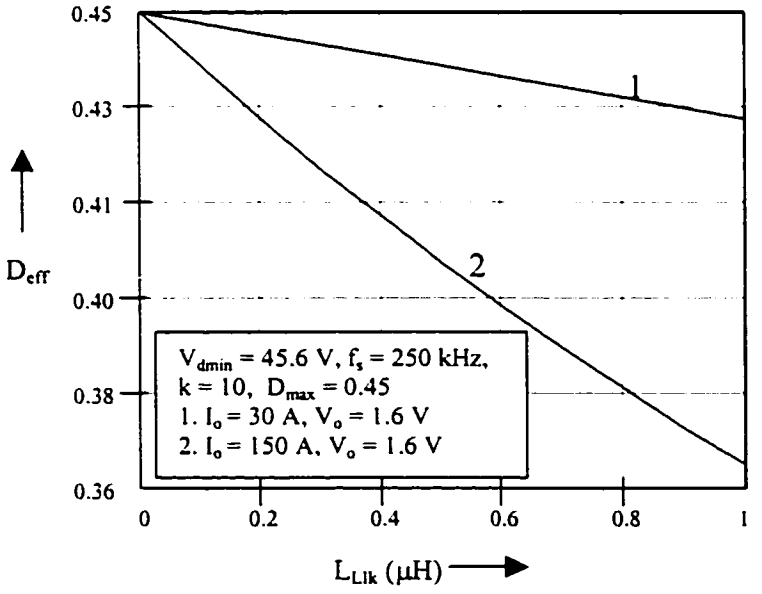


Fig. 4.2 Effective duty cycle (D_{eff}) versus leakage inductance (L_{Lk}).

is selected at full load.

4.3 Zero voltage switching range

To achieve ZVS turn-on, the snubber capacitors shall be completely discharged within the dead time t_d, under all operating conditions. The optimization of auxiliary inductor L_{aux} and transformer leakage inductor L_{Llk} has been proposed to achieve zero voltage switching (ZVS) in *leg B* under all load and line conditions. As stated earlier the leakage inductor (L_{Llk}) must be kept at its minimum value in order to achieve optimum efficiency of the circuit. For *leg A*, primary current is sufficient to achieve ZVS.

For *leg B*, the primary current assists auxiliary current in discharging and charging the snubber capacitors across S_3 and S_4. That's why the value of auxiliary inductor is higher than the value where the leakage inductance (L_{Llk}) was assumed to be zero. But the higher value of leakage inductance will reduce the effective duty cycle (D_{eff}) and lower overall efficiency of the circuit.

It is understood that the for *leg B*, auxiliary inductor is essentially required in the proposed topology to achieve ZVS turn-on of the switches, by providing the current to discharge the snubber capacitor that may be a combination of both external snubber capacitor and the MOSFET internal capacitor or the internal capacitor alone.

Particularly, to successfully discharge the snubbers for *leg B* within the switching dead time t_d, the discharging current is required to be

$$I_{B\_discharge} \geq \frac{C_{sb3,4} \cdot V_d}{t_d} \tag{4-2}$$

From (3-8), (3-19), (3-20) and (3-21), the discharging current for switches in *leg*

B has a magnitude determined by

$$I_{B\_discharge} = \frac{1}{2}\left(\frac{V_d}{4 \cdot L_{aux}}\left(\frac{T_s}{2} - t_d\right) - \frac{\frac{V_d}{L_{Llk}}(t_3 - t_4) + I_{pv} + I_{ppk}}{(t_3 - t_1)}(t - t_1) + I_{ppk} \right) \quad (4\text{-}3)$$

By substituting the value of $I_{B\_discharge}$ from equation (4-3) in equation (4-2), the value of snubber capacitor required to discharge/charge the switch for *leg B* can be calculated. Fig. 4.3 through Fig. 4.5 determines the value of snubber capacitor ($C_{sb3,4}$), which can be discharged or charged the snubber capacitor within the dead time t_d for different values of auxiliary inductor (L_{aux}) with fixed leakage inductor (L_{Llk}). This is going to meet the ZVS condition requirement. For this circuit full-load will determine the worst condition.

For *leg A*, the load current reflected back to the primary side would determine the ZVS. No-load condition is going to be the worst condition for *leg A* because during the turn-on and turn-off of switch S_1 or S_2 only primary current is flowing through these switches. For the successful discharge of the snubber capacitors for *leg A* within the switching dead time t_d, the discharging current is required to be

$$I_{A\_discharge} \geq \frac{C_{sb1,2} \cdot V_d}{t_d} \quad (4\text{-}4)$$

From (3-9), the discharging current for switches in *leg A* has a magnitude determined by

$$I_{A\_discharge} = \frac{I_{ppk}}{2} \quad (4\text{-}5)$$

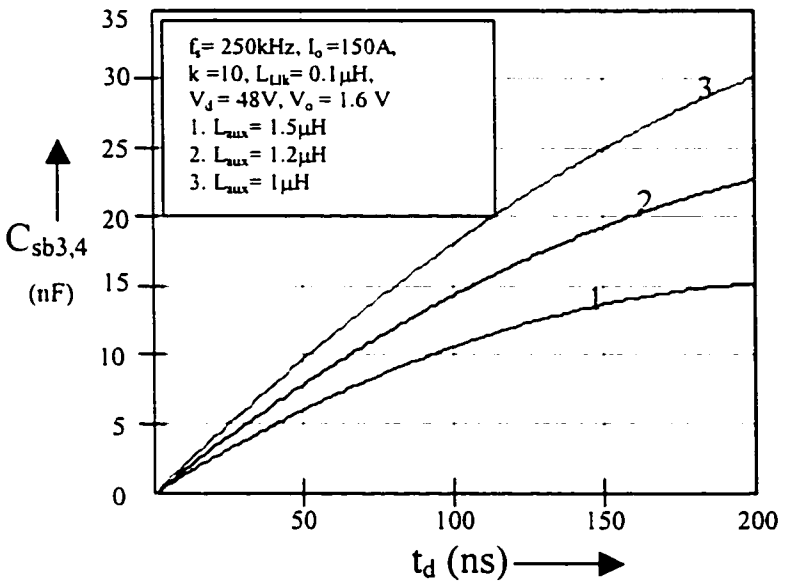


Fig. 4.3 Snubber capacitor ($C_{sb3,4}$) versus dead time (t_d) with leakage inductance (L_{Lk} =0.1μH) and k=10 for *Leg B*.

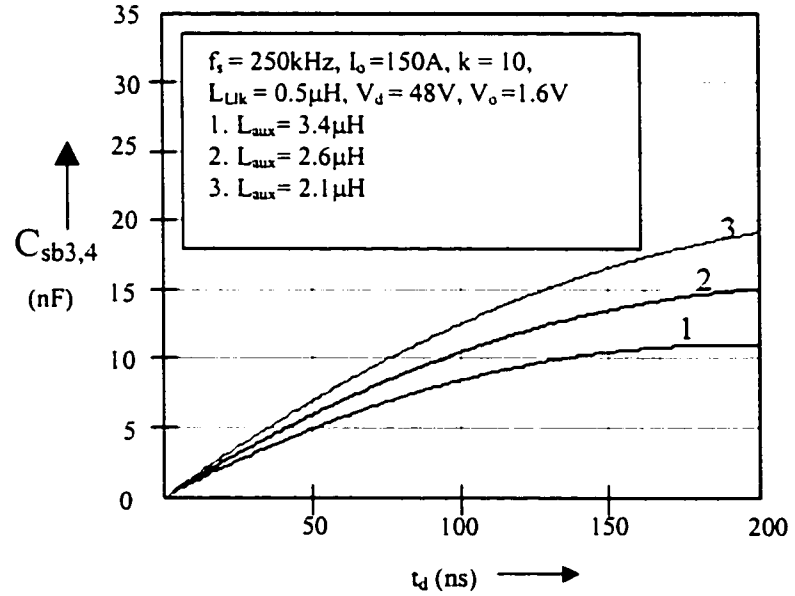


Fig. 4.4 Snubber capacitor ($C_{sb3,4}$) versus dead time (t_d) with leakage inductance (L_{Lk} =0.5μH) and k=10 for *Leg B*.

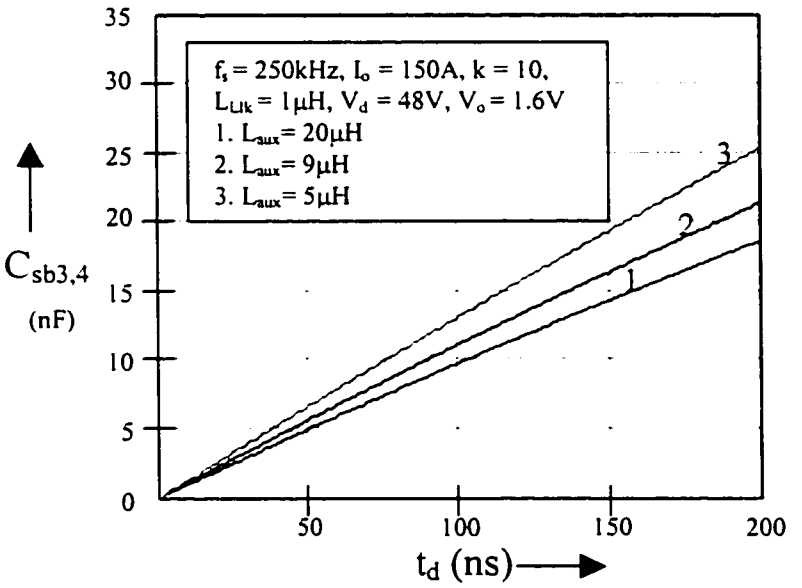


Fig. 4.5 Snubber capacitor ($C_{sb3,4}$) versus dead time (t_d) with leakage inductance (L_{Lk}=1μH) and k=10 for *Leg B*.

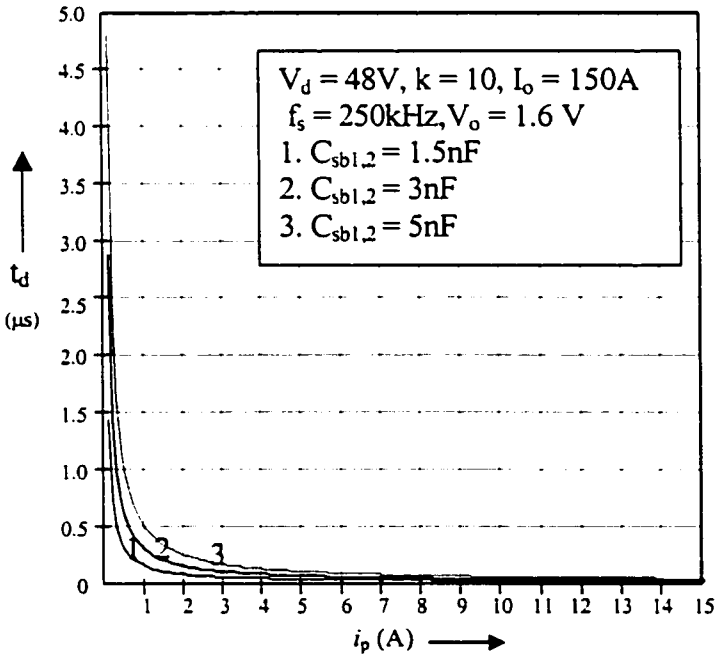


Fig. 4.6 Dead time (t_d) versus primary current (i_p) with k=10 for *Leg A*.

By substituting the value of $I_{A\_discharge}$ from equation (4-5) in equation (4-4), the value of snubber capacitor required to discharge/charge the switches for *leg B* can be calculated. The graph shown in Fig. 4.6 shows the dead time t_d required to charge and discharge the different snubber capacitor ($C_{sb1,2}$) from no-load to full-load. For typical value of t_d =200ns, it can be observed that the ZVS can be achieved up to an output load of about 20%. In applications where the output current has to go to zero, an auxiliary circuit as shown in Fig. 4.7 should be used.

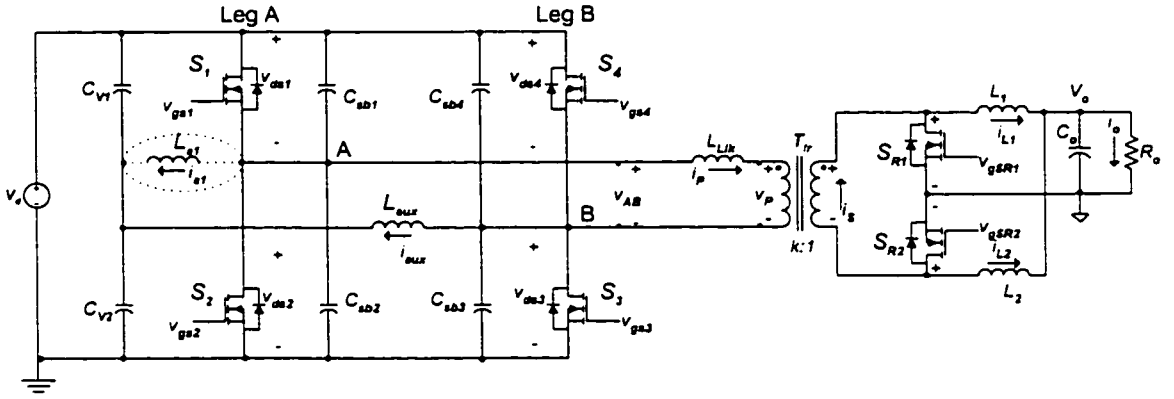


Fig. 4.7 Shows the additional auxiliary inductor (L_{al}) used in Leg A for the proposed converter to achieve ZVS from no load to full load.

Fig. 4.8 shows the effect of adding the auxiliary inductance L_{al} to achieve ZVS at no-load for the switches S_1 and S_2 of *leg A*. In the last interval of the previous cycle, both S_1 and S_3 are off while S_2 and S_4 are on. The load current is reflected back to the primary side through synchronous rectifiers. The drain current of switch S_2 in *leg A* is the sum of primary current i_p and the auxiliary current i_{al} and it reached to its peak value at the end of the last cycle. The peak value of this is current is given by

$$I_p = I_{al} + I_{ppk} \tag{4-6}$$

where, I_{al} is the peak value of the current passing through L_{al} and is given by

$$I_{al} = \frac{V_d}{4 \cdot L_{al}} \left(\frac{T_s}{2} - t_d \right) \tag{4-7}$$

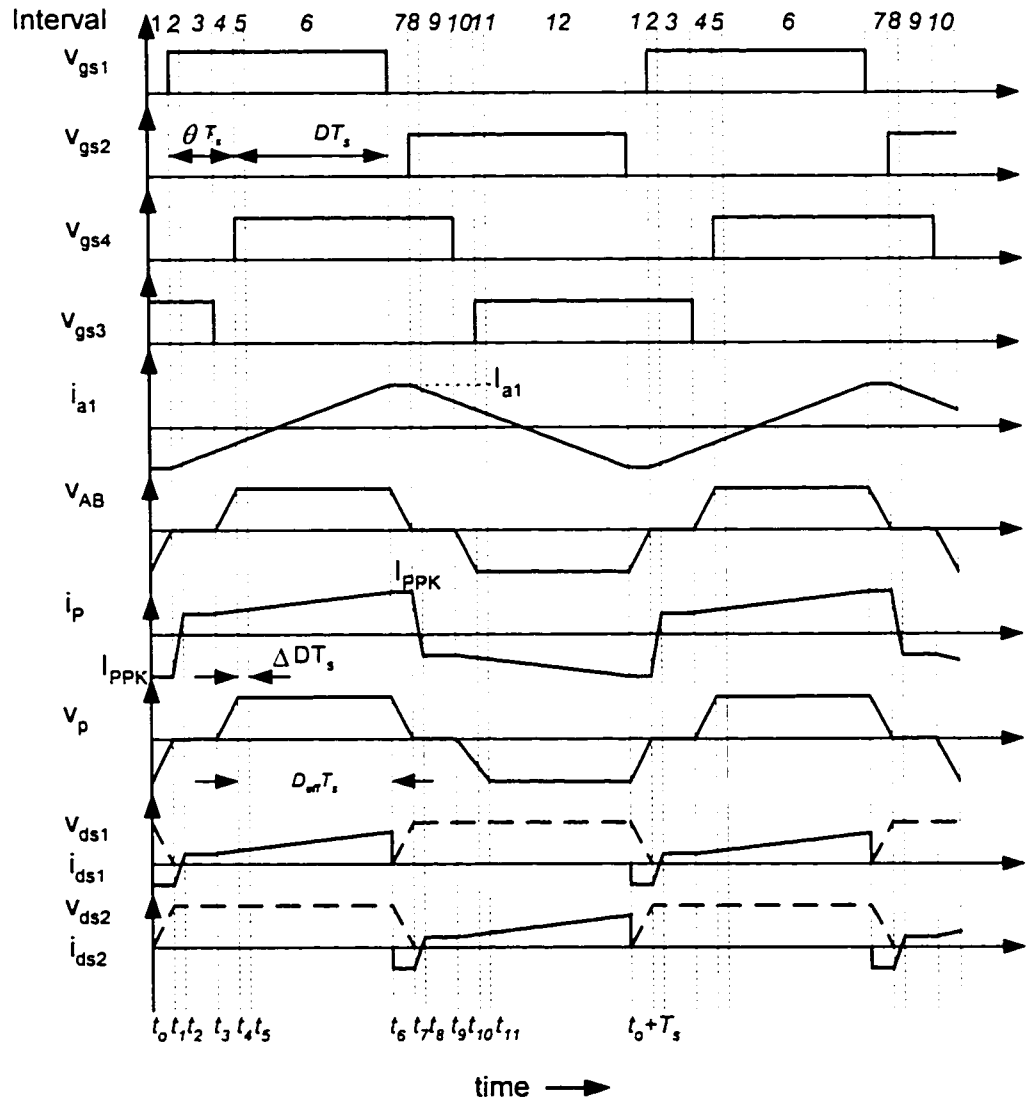


Fig. 4.8 Gating pattern and key waveforms for Leg A at no-load

To achieve ZVS at turn-on, the snubber capacitors shall be completely discharged within the dead time t_d, under all operating conditions. At the beginning of Interval 1, S_2 is turned-off and no other switching action takes place in this interval. As S_2 is off the current i_P, which is the total current flowing into *leg A*, starts to charge C_{sb2} and discharge C_{sb1}. The transformer T_{fr} continues to see a negative voltage during this interval. As this interval is very small and is given by dead time t_d, the inductor current and primary current can be assumed constant. Within this interval v_{ds1} falls to zero volts and v_{ds2} reaches V_d. It is noticed that the auxiliary current is enhanced by the load current in discharging the snubber of S_1 which is the reverse case for *leg B*, where auxiliary current was opposing the primary current. That's why the value of auxiliary inductor required in *leg A* is very high as compared to *leg B*. The peak current carried by

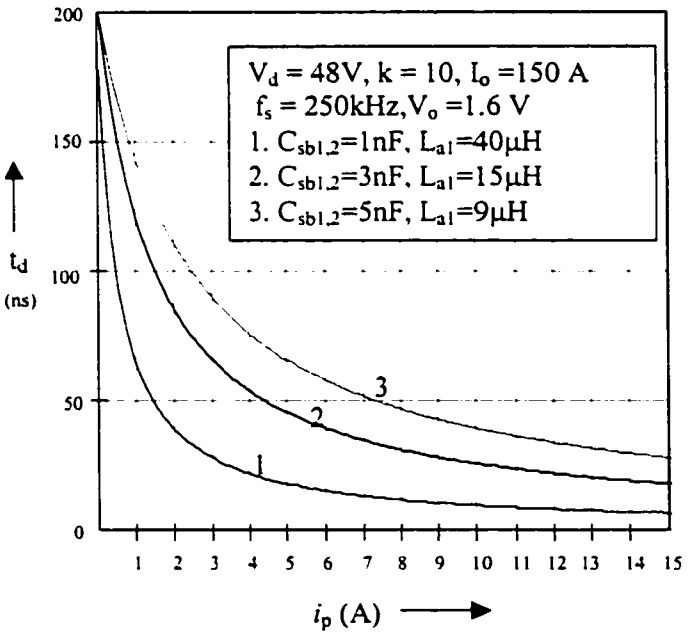


Fig. 4.9 Dead time (t_d) versus primary current (i_P) with k=10 for *Leg A*.

this auxiliary inductor is very small, which results in a physically smaller inductor used in *leg A.*

The graph plotted between primary current and dead time in Fig. 4.9 shows the different values of auxiliary inductor L_{a1} and snubber capacitor $C_{sb1,2}$ required to achieve ZVS condition, from no load to full load, within the dead time t_d. ZVS can be achieved for any load with the expense of small increase in conduction losses.

4.4 Conclusions

In this chapter characteristic curves based on the steady state analysis developed in Chapter 3 were presented. The curves have been drawn for worst conditions for each leg. The effect of leakage inductance on effective duty cycle has been discussed. The optimization of the leakage inductance with auxiliary inductor has been provided to reduce the switching and conduction losses.

To achieve ZVS at turn-on the snubber capacitors shall be completely discharged with the dead time t_d, under all operating conditions. From the curves drawn for *leg B* it is seen that as the value of leakage inductance (L_{Lik}) is increased, the peak current required to achieve ZVS by auxiliary inductor is reduced, which results in a higher value of auxiliary inductor. But this results in reduced duty ratio. So there is a trade-off between the values of leakage and auxiliary inductance to obtain the maximum efficiency. To achieve ZVS for *leg A* for the applications where the output current has to go to zero, a physically small but a very high value of auxiliary inductor has been added.

CHAPTER 5

DESIGN PROCEDURE

5.1 Introduction

This chapter presents a procedure for designing the proposed ZVS full bridge dc/dc converter topology. As seen in the previous chapters, the proposed topology is a combination of conventional full bridge converter and auxiliary circuit. To extend the soft switching capability under all load conditions, the auxiliary circuit is optimized with the inherent leakage inductance of the transformer. An example is given to illustrate the design process for the selection of converter components. The design is based on the characteristics curves derived in Chapter 4.

The outline of this chapter is as follows:

Section 5.2 presents the design procedure for the proposed topology.

Section 5.3 a design example is given.

Section 5.4 presents simulation results done by ORCAD software to validate the design process.

The main points of this chapter are summarized and some conclusions are made in Section 5.5.

5.2 Design procedure

It is important to generalize the topology so that it can be designed for different load requirements and applications. In this section, a step-by-step procedure is provided

for easy design of the power supplies for different applications.

(i) Establishment of design requirements: The first step is to know the basic requirements and specifications. It is important to know the output power, output voltage, input current, switching frequency and the output voltage ripple requirements;

(ii) Design of the transformer: The transformer should be designed for the worst conditions. The worst condition will be at minimum input voltage, maximum duty cycle and the maximum permitted leakage inductance of the transformer. The transformer can be designed using equations (3-1) and (3-2);

(iii) Selection of primary switches: It is based on the maximum voltage and current passing through the switch. As it is well described in previous chapters that both legs behaves differently and requires different current to obtain ZVS. For *leg A* the maximum current flowing through it is the primary current which occurs at full load but for *leg B* the maximum current flowing through switches S_3 and S_4 is the summation of instantaneous primary current and peak auxiliary current at full load;

(iv) Selection of synchronous rectifiers: It has been explained in the steady state analysis performed in Chapter 3 that the load current is equally shared between the two MOSFET's. For the high-current and low-voltage applications the selection of MOSFET is based on drain-to-source resistance ($r_{DS(on)}$). It is very important that $r_{DS(on)}$ should be very small;

(v) Selection of the dead time: It is based on the MOSFET turn-on time delay, turn-off delay, rise time and fall time;

(vi) Selection of input capacitor filters: It is based on the input voltage ripple requirements;

(vii) Design of output filter: The current is equally shared between the two filter inductors. Each inductor operates on the same frequency as the switching frequency;

(viii) Selection of passive components for *leg B*: It is based on the leakage inductance of the transformer. The values of auxiliary inductor, snubber capacitor and leakage inductance for a given dead time can be found by solving equation (3-19) through (3-21). This will give the proper design for *leg B* to obtain ZVS, it is also important to know the worst conditions. For *leg B* the worst condition is at the full-load;

(ix) Selection of passive components for *leg A*: The worst condition for *leg A* is at no load. From steady state analysis done in Section 3.2, it is found that only primary peak current I_{ppk} will charge or discharge the snubber capacitors C_{sb1} and C_{sb2}. Using equations (4-5) and (4-6), snubber capacitor C_{sb1} and C_{sb2} can be determined. The worst condition for *leg A* is at reduced load.

5.3 Design example

This section illustrates the design procedure using the following design example.

5.3.1 Specifications

The specifications for the design example are as follows:

(i) $P_o = 240$ W, output power at full load

(ii) $V_d = 48$ V, nominal input voltage

(iii) $V_{in(\,ripple\,)} = \pm 5$ % of V_d, peak to peak input ripple voltage

(iv) $V_o = 1.6$ V, nominal output voltage

(v) $V_{o(\,ripple\,)} = \pm 2$ % of V_o, peak to peak output ripple voltage

(vi) $f_s = 250$kHz, switching frequency

(vii) $t_d = 200$ns, switching dead time

(viii) $R_o = 0.0106\ \Omega$, output load

5.3.2 Transformer design

Conventional transformer design starts with determining the acceptable temperature rise; the corresponding minimum area product and the maximum flux swing allowed to stay within the calculated core limits of the transformer. These parameters will define the number of turns required on the primary side. The secondary number of turns calculated from the turns ratio, is based on the minimum value of the input voltage, the maximum steady state duty ratio and the dc transfer function of the converter.

The current doubler output stage needs twice the number of turns and one secondary winding [5]. The transformer has to be designed for the worst condition. It is found that the worst condition is at minimum voltage, maximum duty cycle and at maximum leakage inductance.

The turns ratio k is given by:

$$k = \frac{V_{d\,min} \cdot D_{eff\,max}}{V_o} \tag{5-1}$$

where,

$$D_{eff(max)} = \frac{D_{max}}{\left[1 + \frac{L_{Lik} \cdot f_s}{k^2 \cdot R_o}\right]} \tag{5-2}$$

By substituting the value of $D_{eff\,max}$ from equation (5-2) in equation (5-1), the transformer turns ratio (k) can be calculated. For D_{max} = 0.45, f_s = 250 kHz, L_{Lik} =1μH, R_o = 0.0106 Ω, the value of k =10:1 is selected. The advantage of using current doubler at the secondary side is that finer steps in turns ratio are possible; transformer structure is simpler as there is no need for center- tapping.

5.3.3 Selection of C_{V1} and C_{V2}, the capacitor type voltage divider

The two capacitors are employed to establish and hold almost dc voltage with little ripples for the proper operation of the auxiliary circuit. The design of these two capacitors is based on the permitted ripple voltage at the input. Assume the permitted ripple voltage on the two capacitors is about 5% of the input line voltage. The input capacitors is given by:

$$C_{V1} = C_{V2} = 2\left[\frac{I_{dc}}{V_{in(\,ripple\,)}} \cdot \frac{T_s}{2}\right] \tag{5-3}$$

where, $I_{dc} = \dfrac{P_o}{V_d}$

For the output power (P_o) = 240 W, V_d = 48 V, T_s = 4μs and $V_{in(\,ripple\,)}$ =5% of V_d, the two input capacitors (C_{V1}=C_{V2}) of 8μF has been selected.

5.3.4 Selection of L_1, L_2 & C_o, the output filter

As equivalent filter circuit for current doubler is same as the conventional full bridge with center-tap transformer but it requires two output inductors. While in

traditional full wave output stages the entire output current flows through the filter inductor, which operates at double the frequency of the isolation transformer, these inductors carry only one half of the load current and they work at half the frequency of their full wave counterparts (same as the operating frequency of the power transformer). The current waveforms are 180 degree out of phase and the ripple components partially cancel each other in the common output capacitor. For the same equivalent output ripple current that would generate by a full wave rectifier circuit, the inductance of each output inductor has to be doubled.

For the selected output capacitor (C_o) of 47μF for f_s = 250kHz, V_d = 48 V, V_o = 1.6 V, $V_{o(ripple)}$ = ± 2 % of V_o and k =10:1, the output inductors ($L_1 = L_2$) required to be 2μH each.

5.3.5 Selection of primary switches S_1, S_2, S_3 and S_4

MOSFET's are widely used where high switching speeds are important. To select the proper switches in the primary side, the current and voltage across the switches in each leg have to be calculated. It is well described in previous chapters that both legs behaves differently and requires different current to obtain ZVS.

For *leg A*, the maximum current flowing through switches S_1 or S_2 occurs at full load, which is given by $\frac{I_{ppk}}{2}$.

$$I_{S1\&S2_{MAX}} = 4 \text{ A} \tag{5-4}$$

For *leg B*, the maximum current flowing through it occurs at full load, which is given by the sum of instantaneous primary current and peak value of auxiliary inductor

(L_{aux}). In the design example given in Section 5.3, the maximum current flowing through S_3 or S_4 is at full load. The design example performed in Section 5.3 is based on Characteristics curves drawn in Chapter 4. For the transformer leakage inductance (L_{Lik}) of 0.5μH, t_d =200ns and $C_{sb3,4}$ = 15 nF, the required auxiliary inductance (L_{aux}) is 2.6 μH to obtain ZVS. So, the maximum current required for S_3 or S_4 is:

$$I_{S3\&S4_{MAX}} = 5 \text{ A} \tag{5-5}$$

The voltage across each switch is given is:

$$V_{ds1,2,3,4} = 48 \text{ V} \tag{5-6}$$

Therefore, good selection for the main switches would be IRFP150 ($r_{DS(on)}$= 0.055Ω) from International Rectifier.

5.3.6 Selection of synchronous rectifiers S_{R1} and S_{R2}

The maximum current that goes through each switch is:

$$I_{SR1\&2_{Max}} = \frac{I_o}{2} = 75 \text{ A} \tag{5-7}$$

Therefore, due to very high current in the synchronous rectifiers, these switches have to be chosen in such a way that they have the least possible drain to source resistance. ($r_{DS(on)}$). A good selection for these two switches is IRL3803 ($r_{DS(on)}$= 0.006Ω) from International Rectifier.

5.3.7 Selection of $L_{aux}, L_{Lk}, C_{sb1}, C_{sb2}, C_{sb3}$ and C_{sb4}

Fig. 4.3 through Fig. 4.5 shows the snubber capacitor ($C_{sb3,4}$) as a function of the minimum dead time (t_d), which is required to achieve the ZVS of the main inverter switches, for the various auxiliary and leakage inductance values. It is observed from these figures that for the same dead time and snubber capacitor, the value of auxiliary inductance is higher for the higher value of leakage inductance. For example, Fig. 4.4 shows that for $L_{Lk} = 0.5\mu H$, t_d =200ns and $L_{aux} = 2.6\mu H$, the required value of the snubber capacitor is 15nF.

Fig. 4.6 shows the ZVS range for the primary current from full load to reduced load for different values of snubber capacitors at different dead time for *leg A*. For typical value of t_d = 200ns, it is found that ZVS is achieved for the reduced load greater than 20%. For the applications where output current can go to zero, an additional inductor is used. The graph shown in Fig. 4.7 shows the auxiliary inductor L_{a1} and snubber capacitor $C_{sb1,2}$ required to achieve ZVS for the entire range from no-load to full-load. Now, if we examine Fig. 4.10, it is observed that for the dead time t_d=200ns with $C_{sb1,2}$=1nF, the auxiliary inductor L_{a1} required is 40μH.

5.3.8 Design summary

According to the design criteria given in this Chapter, an example circuit is designed. The principal parameters and selected devices used in simulation are listed in Table 5.1.

Parameter	value	parameter	value/device
$V_{d\,min}$ / $V_{d\,max}$	45.6 V/ 50.4 V	t_d	200ns
V_o	1.6 V	C_{V1}, C_{V2}	8μF, each
I_o	150 A	$C_{sb1,2}$ / $C_{sb3,4}$	3nF / 15nF
k	10:1	L_{aux} / L_{Lik}	2.6μH / 0.5μH
L_1, L_2	2μH	S_1, S_2, S_3, S_4	IRFP150
C_o	47μF	S_{R1}, S_{R2}	IRL3803

Table 5.1 Example circuit

5.4 Performance demonstration

Simulation of the proposed converter topology is performed with ORCAD software. As explained earlier, l*eg B* is the critical leg of the converter where natural ZVS is lost at considerably higher load current, therefore, the voltage and current waveforms for the switches of this leg are shown here. Fig. 5.1 through Fig. 5.4 shows the different simulation results at full load and 20% load for *leg A* and *leg B*. For *leg A*, by using a high value of auxiliary inductance the ZVS is achieved for any load condition. Fig. 5.5 shows the simulation done by ORCAD for *leg A*, for 1% of load. It is seen that the ZVS is achieved which is proving the concept.

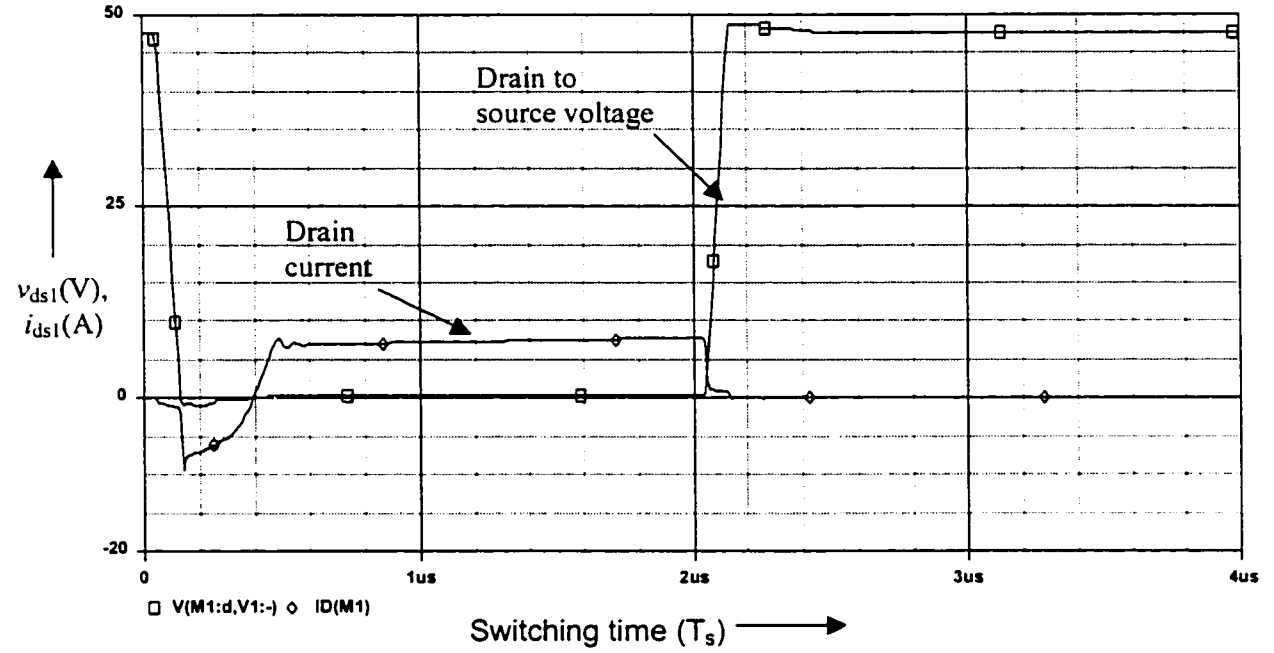


Fig. 5.1: Simulation result for Leg A at L_{Lik}=0.5μH, L_{aux}=2.6μH with $C_{sb1,2}$=3nF at full load.

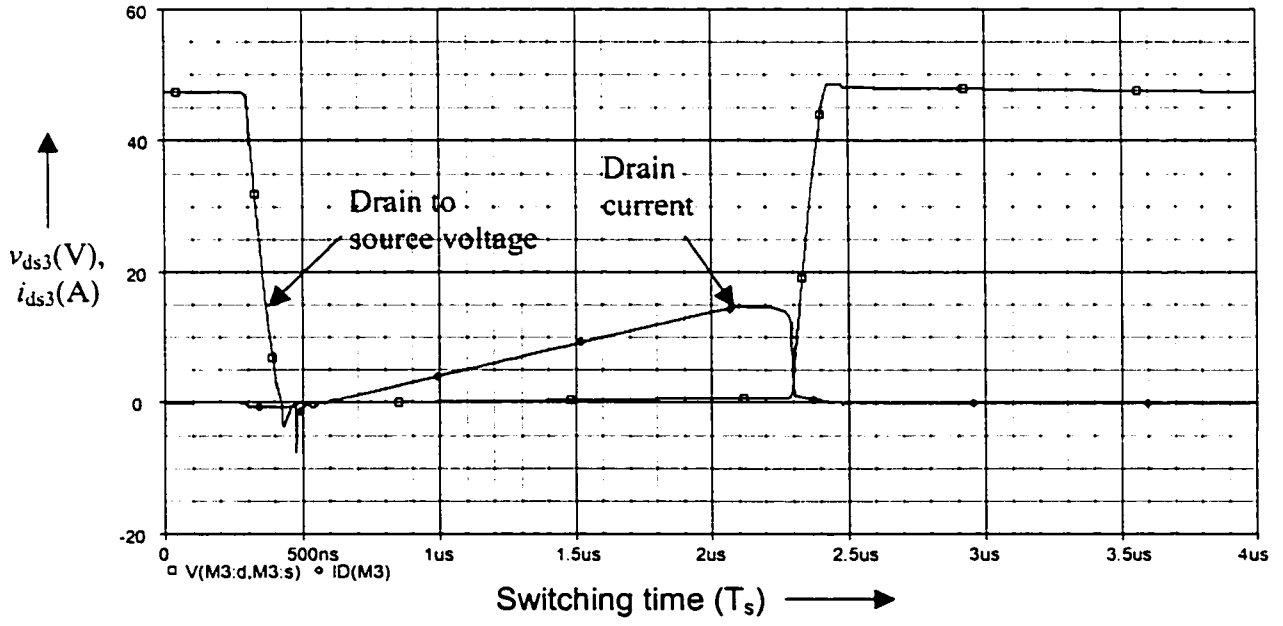


Fig. 5.2: Simulation result for Leg B at L_{Lik}=0.5μH, L_{aux}=2.6μH with $C_{sb3,4}$=15nF at full load.

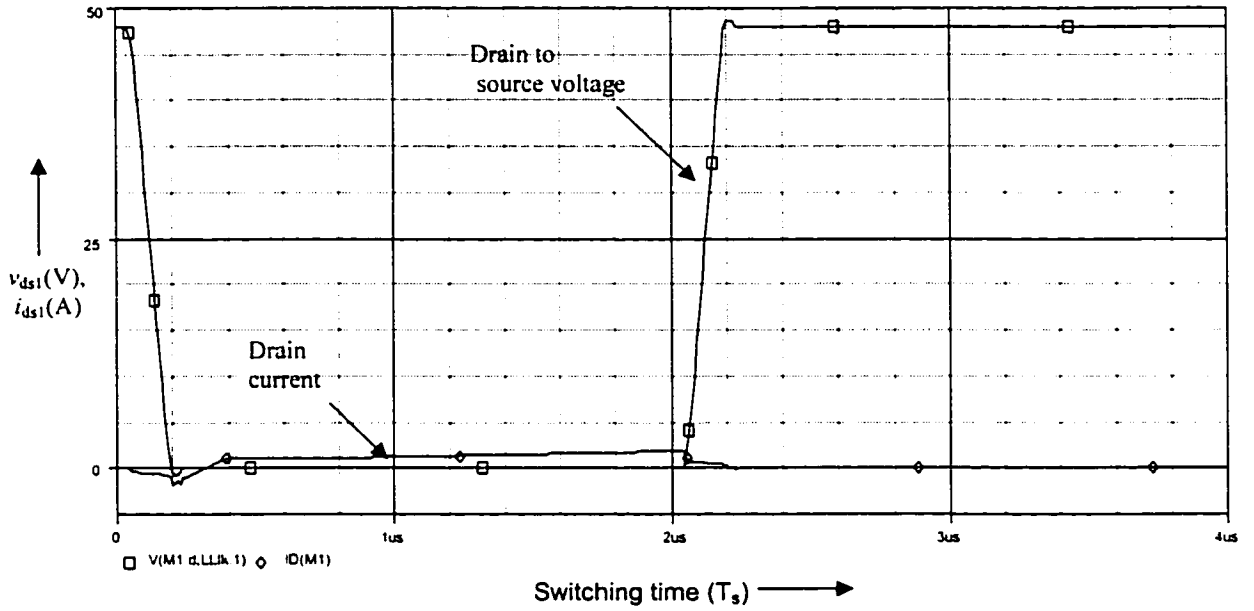


Fig. 5.3: Simulation result for Leg A at L_{Llk}=0.5μH, L_{aux}=2.6μH with $C_{sb1,2}$=3nF at 20% load.

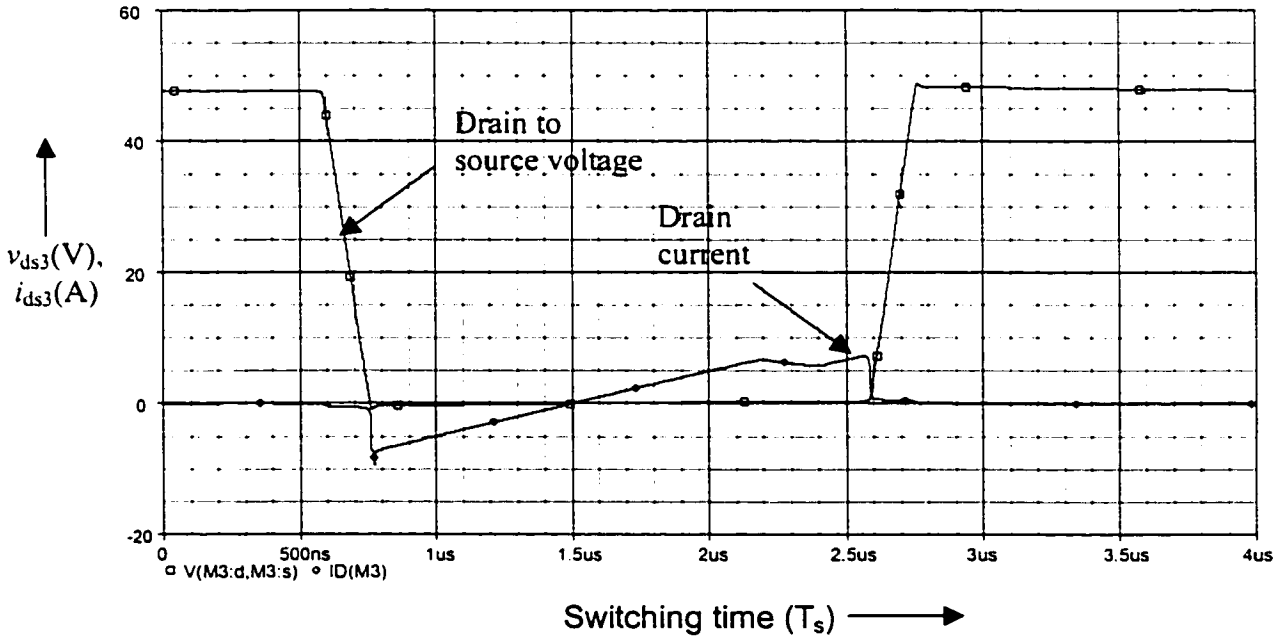


Fig. 5.4: Simulation result for Leg B at L_{Llk}=0.5μH, L_{aux}=2.6μH with $C_{sb3,4}$=15nF at 20% load.

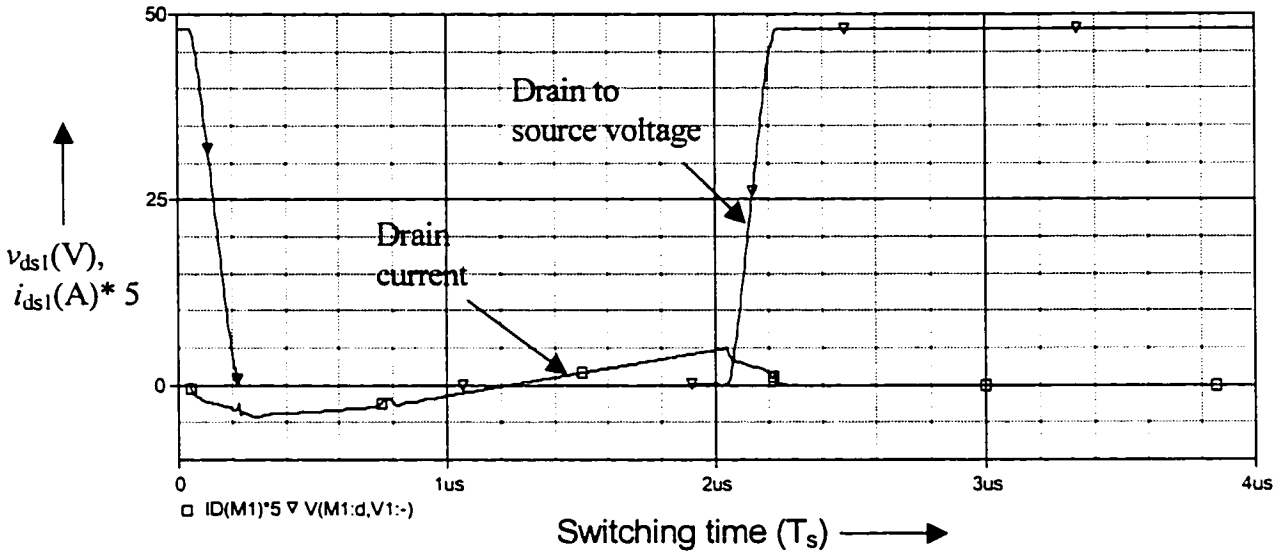


Fig. 5.5: Simulation result for Leg A at L_{Lik}=0.5μH, L_{al}=40μH with $C_{sb1,2}$=1nF at 1% load.

5.5 Conclusions

In this chapter design procedure and the selection of principal parameters has been presented. Based on these parameters a design example has been given.

CHAPTER 6
SUMMARY AND CONCLUSIONS

6.1 Summary

The analysis and design of an auxiliary commutated full bridge dc/dc converter has been presented and analyzed in this thesis. By achieving ZVS under all operating conditions, the overall conversion efficiency has been enhanced, the thermal problems on the switches are relieved, and the switching frequency can be further increased to reduce the converter's physical size. The high efficiency and high power density can be achieved.

This work can be summarized as follows:

In Chapter 1, the conventional ZVS full bridge converter topologies have been reviewed. It is found that the conventional approach can only achieve ZVS conditionally, and it would lose ZVS at light load or over load conditions.

In Chapter 2, the proposed topology used for low voltage and high current applications has been shown. The working principle has been described in detail. The different modes of operation under different line and load conditions have been explained. The optimization of leakage inductance of transformer with auxiliary inductance has been examined. The gate-drive techniques for the secondary side used for synchronous rectification have been explained. The advantages and disadvantages of those techniques have been described.

In Chapter 3, the steady state analysis using time domain has been explained in

detail, which are required to set the different parameter requirements for the design of power supply. The comparison of the theoretical analysis done by Math CAD and the simulation using ORCAD has been shown. The higher efficiency can be obtained by using this topology.

In chapter 4, the characteristics curves for the proposed topology have been presented. These curves shows the different snubber capacitors requirement because of the different values of leakage inductance. By these graphs different sets of snubber capacitors, auxiliary inductance with different value of leakage inductance can be obtained to acquire ZVS.

In chapter 5, the dc/dc full bridge converter is proposed to optimize the design. The design example is based on the analysis done in Chapter 3.

6.2 Conclusions

The following conclusions can be drawn:

(i) The proposed topology is simple and it achieves ZVS for the wide range of line and load variations. It only involves one inductor, two dc capacitors and four snubber capacitors. In some applications the snubber can be the inherent capacitance of the MOSFET, which further simplifies the design.

(ii) The optimization of leakage inductance and auxiliary inductance should be employed to reduce the conduction losses arising from the current in the auxiliary inductor. This helps to increase the overall efficiency.

(iii) By using current doubler with synchronous rectification the transformer design has become simpler and the secondary losses are reduced.

(iv) The power circuit design is very simple, which reduces the development time and facilitates its application.

(v) For *leg B*, the ZVS is achieved under any line and load condition. In applications where the output current goes to zero, *leg A* looses its ZVS. By adding an auxiliary inductor, which is proposed in Chapter 4, the proposed topology can achieve ZVS under any line and load conditions for both legs.

6.3 Contributions

The contributions of the work includes:

(i) Detailed steady state analysis of the proposed converter topology,

(ii) Proposing the optimization use of the auxiliary and leakage inductance of the transformer,

(iii) Proposing the optimal design for low voltage and high current application,

(iv) Development of the design curves and criteria for high performance computer power supplies for industrial purposes,

(v) Verification of analysis and topology from experiment and simulation results,

6.4 Suggestions for future work

As this proposed topology is used for high current applications, the switching losses are eliminated at the expense of increased conduction losses. Future investigation is recommended in which the conduction losses caused by the auxiliary circuits can be optimized with respect to the switching losses where the snubber capacitors are only discharged to a lower voltage level before the switches are turned-on. This will increase

the circuit performance and efficiency by the reduction of conduction losses. Thus it is worthwhile to investigate the overall efficiency at low voltage switching instead of ZVS.

REFERENCES

[1] Praveen Jain, Wen Kang, Harry Soin and Youhao Xi, "Load and Line Independent Zero Voltage Switching Full Bridge dc/dc Converter Topology," *Proceeding of INTELEC'98, Records*, pp.22-29.

[2] J. A. Sabate, V. Vlatkovic, R. Ridley and F. C. Lee, "Design considerations for high-voltage, high-power, full-bridge, zero-voltage-switched, PWM converter," *IEEE APEC '90 Records*, pp. 275-284.

[3] Laszlo Balogh, "Design Review: 100W, 400KHz, dc/dc Converter With Current doubler Synchronous Rectification Achieves 92% Efficiency," *Unitrode Power Supply Design Seminar*, 2.1- 2.25, 1996.

[4] Yuri Panov and Milan Jovanovic, "Design and Performance Evaluation of Low Voltage/High Current dc/dc on-Board Modules," *APEC '99 Records*, pp. 545-552.

[5] L.Balogh, "The Current doubler Rectifier: An Alternative Rectification Technique for Push–Pull and Bridge Converters," *Design Note-63, Unitrode Integrated Circuit Corporation,* DG-300, pp. 12-14.

[6] Xunwei Zhou, Bo Yang, Luca Amoroso, Fred C. Lee and Pit-Leong Wong "A Novel High-input-voltage, High Efficiency and Transient Voltage Regulator Module, Push-pull Forward Converter," *IEEE APEC'99 Records*, pp. 279-283.

[7] Joseph Drobbnik, "High Frequency Alternating Current Power Distribution," *Proceeding of INTELEC'94, Records*, pp.292-296.

[8] Ning Dai, "Effects of Powering Low-voltage, High- current Load on Components from Power Design Perspective," *IEEE APEC'2000 Records*, pp. 803-807.

[9] Bob Christiansen, "Servers, Workstations, Personal Computers: The Looming Power Bottleneck," *IEEE APEC'99 Records*, pp. 49-54.

[10] Josef Drobnik, Lilly Huang, Praveen Jain and Robert Steigerwalg, "PC Platform Power Distribution System: Past Application, Today's Challenge and Future Direction," *proceeding of INTELEC'99, Records*, 2-1.

[11] J. A. Sabate, V. Vlatkovic, R. Ridley and F. C. Lee, "High-voltage, high power, ZVS full-bridge pwm converter employing an active switch," *IEEE APEC'91 Records*, pp.158-163.

[12] Richard Redl, Brain P. Erisman and Zoltan Zansky, "Optimizing the Load Transient Response of the Buck Converter," *IEEE APEC'98*, pp. 170-176.

[13] Wojciech A. Tabisz, Fred C. Lee and Dan Y. Chen, "A MOSFET Resonant Synchronous Rectifier for High-Frequency dc/dc Converters," *IEEE PESC'90 Records*, pp. 769-779.

[14] Xunwei Zhou, Xingzhu Zhang, Jiangang Liu, Pit-Leong Wong, Jiabin Chen, Ho-Pu-Wu, Luca Amoroso, Freed C. Lee and Dan Y. Chen, "Investigation of Candidate VRM Topologies for Future Microprocessors" *IEEE APEC'98 Records*, pp. 145-150.

[15] Allen F. Rozman and Kevin J. Fellhoelter, "Circuit Considerations for Fast, Sensitive, Low-Voltage Loads in a Distributed Power System" *IEEE APEC'95 Records*, pp. 34-42.

[16] Ognjen Djekic and Miki Brkovic, "Synchronous Rectifier vs. Schottky Diodes in a Buck Topology for Low Voltage Applications" *IEEE APEC'97 Records*, pp. 1374-1380.

[17] Carl Blake, Dan Kinzer, Peter Wood, "Synchronous Rectifier versus Schottky Diodes: A comparison of the Losses of a Synchronous Rectifier Versus the Losses of a Schottky Diode Rectifier" *IEEE APEC'94 Records*, pp. 17-23.

[18] Pressman, Switched Mode Power Supplies, 2nd Ed., 1992.

[19] N. Mohan, T. M. Undeland and W.P. Robbins, "*Power Electronics*: Converters, Applications and Design," 2nd Edition, *John Wiley & Sons, Inc.* New York, 1995.

[20] George C. Chryssis, "High-Frequency Switching Power Supplies: Theory & Design," *2nd Edition, McGraw-Hill Publishing Company*, 1989.

APPENDIX 1

PERFORMANCE COMPARISON

The converter circuit analyzed in this thesis is essentially the same as reported in [1] except the following differences:

(i) Its auxiliary circuit is optimized with the leakage inductance of the transformer to minimize the circulating current while still achieving ZVS.

(ii) A current doubler is used in the output rectifying stage with the synchronous rectifier.

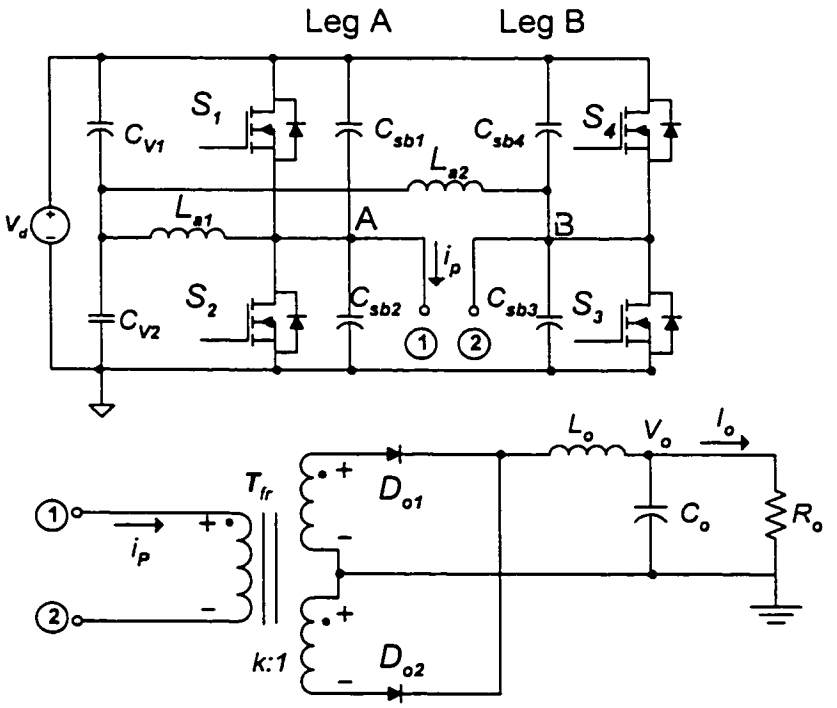


Fig. A.1 Shows the circuit reported in [1]

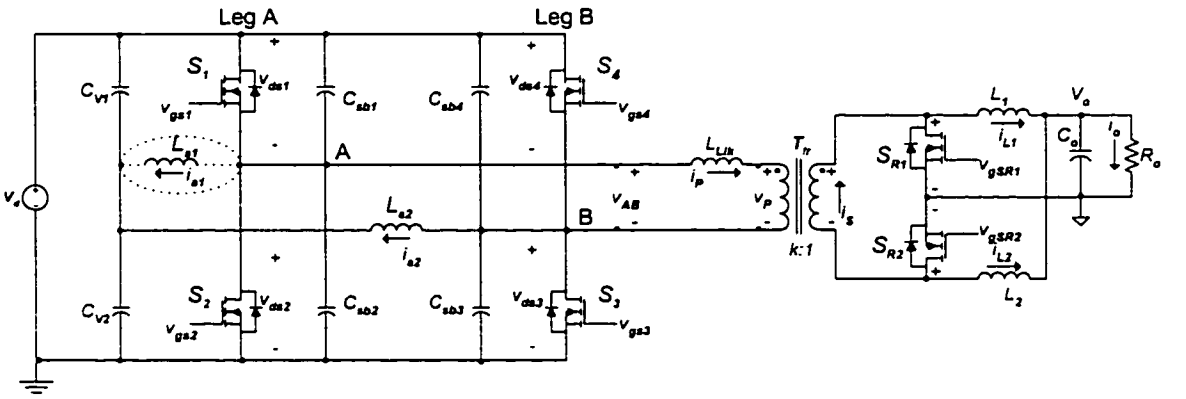


Fig. A.2 Shows the proposed circuit

Fig. A.1 and Fig. A.2 shows the proposed circuit and the circuit as reported in [1] respectively. This appendix compares the performance of these two circuits. Both the circuits are compared for (a) high-voltage, low-current and (b) low-voltage, high-current applications. Table A.1 and Table A.2 presents such a comparison for these two applications respectively.

By comparing the results shown in Table A.1 and Table A.2, it is clear that the center-tap topology and current double topology has nearly the same losses for high voltage and low current applications. But for low voltage and high current applications the optimized topology presented in this thesis has much lower losses.

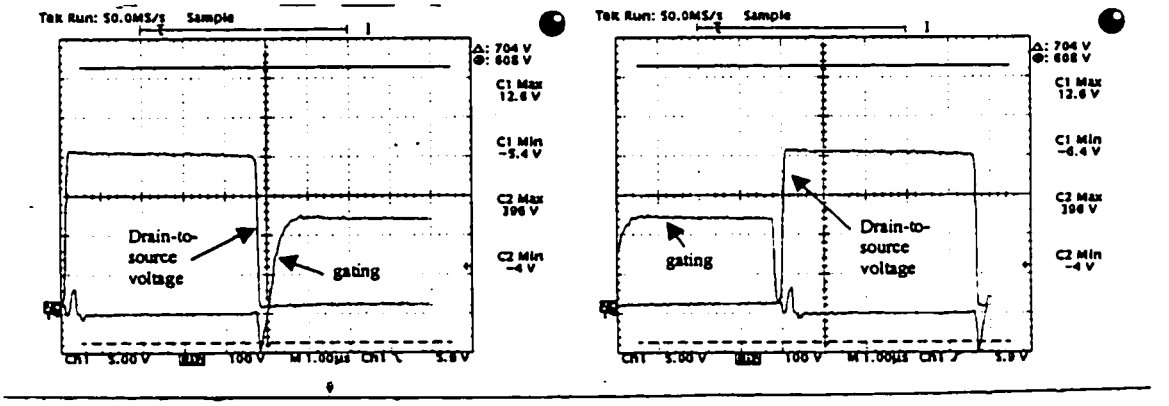
Table A.1. Comparison for high-voltage and low-current applications		
Technique	centre-tap	current-doubler
input voltage (V_d)	400 V	400 V
output voltage (V_o)	55 V	55 V
output current (I_o)	10 A	10 A
transformer turns ratio (k)	6:1	3:1
output inductor	L_o=1μH	$L_1 = L_2$=6.4μH
output capacitor (C_o)	470μF	470μF
transformer leakage inductance (L_{Lk})	0	0.5μH
auxiliary inductor (L_{a1}) for leg A	200μH	220μH
auxiliary inductor (L_{a2}) for leg B	45μH	60μH
switch rms current with $R_{ds(on)}$ = 0.27 Ω for leg A	3.54 A	3.8 A
switch rms current with $R_{ds(on)}$ = 0.27 Ω for leg B	2.8 A	2.2 A
switching losses	~ 0 W	~ 0 W
power loss	24 W	21.7 W

Table A.2. Comparison for low-voltage and high-current applications		
Technique	centre-tap	current-doubler
input voltage (V_d)	48 V	48 V
output voltage (V_o)	1.6 V	1.6 V
output current (I_o)	150 A	150 A
transformer turns ratio (k)	25:1	12:1
output inductor	L_o=0.5μH	$L_1 = L_2$=2μH
output capacitor (C_o)	47μF	47μF
transformer leakage inductance (L_{Lk})	0	0.5μH
auxiliary inductor (L_{a1}) for leg A	40μH	45μH
auxiliary inductor (L_{a2}) for leg B	1.5μH	2.6μH
switch rms current with $R_{ds(on)}$ = .055 Ω for leg A	4.636 A	4.81 A
switch rms current with $R_{ds(on)}$ = .055 Ω for leg B	10.18 A	5.86 A
switching losses	~ 0 W	~ 0 W
power loss	36 W	15 W

APPENDIX 2

EXPERIMENTAL VERIFICATIONS

A 500 W, 300-400 V dc to 55 V dc prototype converter operating at 128 kHz was built to prove the concepts of the proposed topology. Listed in Table A.3 are the principal parameters of the prototype converter.



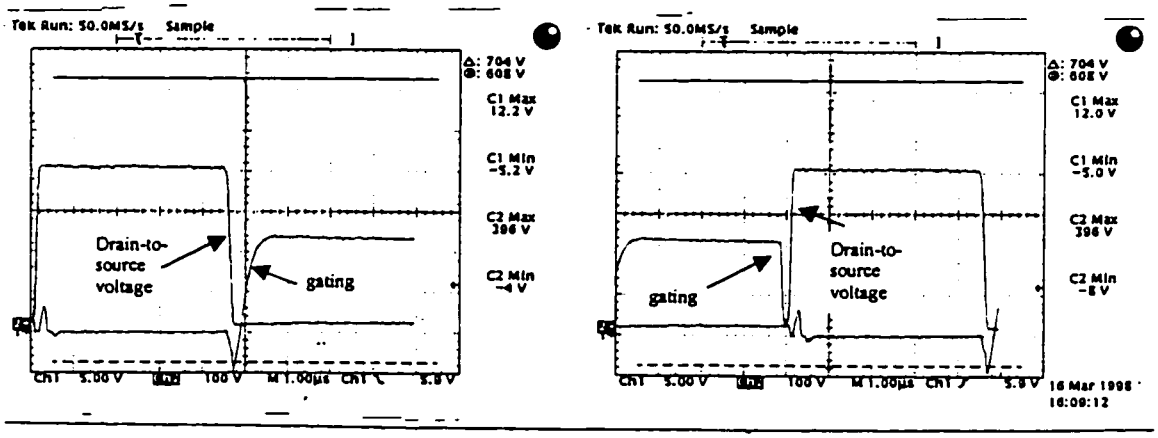
a. ZVS turn-on of switch on Leg A

b. ZVS turn-off of switch on Leg A

c. ZVS turn-on of switch on Leg B

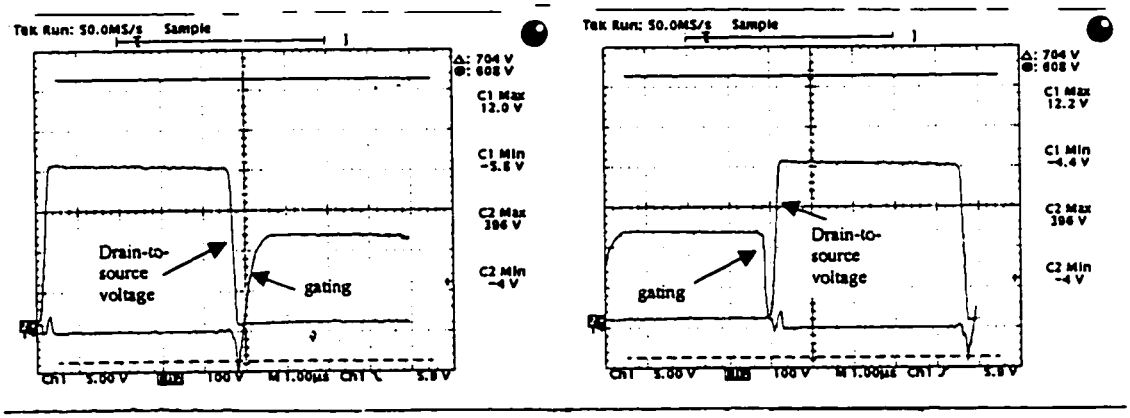
d. ZVS turn-off of switch on Leg B

Fig. A.3. The gating and drain-to source waveforms of the switches under full load condition. f_s=128 kHz, V_o=55 V, P_o=500 W, V_d=390 V.
Vertical scales: 100V/div. for the drain voltage, 5V/div. for the gating signal.
Timing:1μs/div.



a. ZVS turn-on of switch on Leg A

b. ZVS turn-off of switch on Leg A



c. ZVS turn-on of switch on Leg B

d. ZVS turn-off of switch on Leg B

Fig. A.4. The gating and drain-to source waveforms of the switches under light load condition. f_s=128 kHz, V_o=55 V, P_o=50 W, V_d=390 V.
Vertical scales: 100V/div. for the drain voltage, 5V/div. for the gating signal.
Timing:1μs/div.

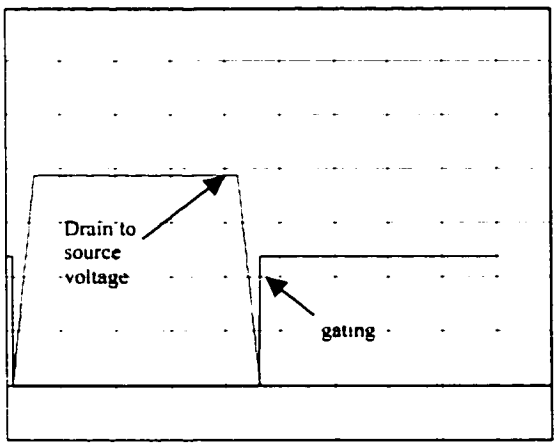
Fig. A.3 shows the gating signal and the drain-to-source voltage of the under full load condition. The waveforms of only one switch from one leg are shown. The other switch has the same waveform with a *180°* phase delay. From Fig. A.3, it can be seen that each switch has ZVS switching at both turn-on and turn-off under all those conditions. It is also seen that the gating signal comes after the drain to source voltage completely drops to zero.

Fig. A.4 shows the gating and the drain to source voltage waveforms of the switches under 10% of the rated load conditions. Similarly, it can be concluded that ZVS is achieved on each switch under all those conditions.

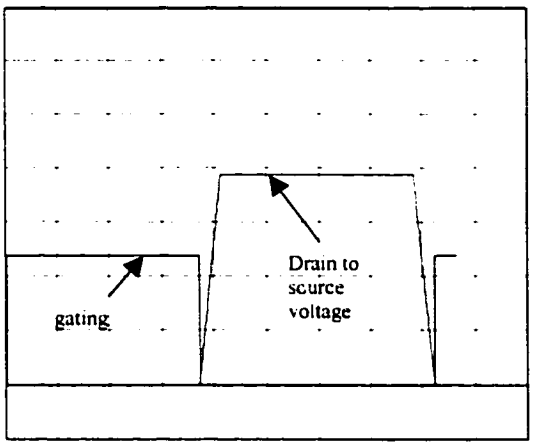
parameter	value	parameter	value
k	5.5:1	$C_{sb3,4}$	1nF
t_d	400ns	L_{a1}	200μH
C_{V1}, C_{V2}	1μF	L_{a2}	100μH
$C_{sb1,2}$	1nF	S_1, S_2, S_3, S_4	IRFP460

Table A.3. Principal parameters of the simulation circuit

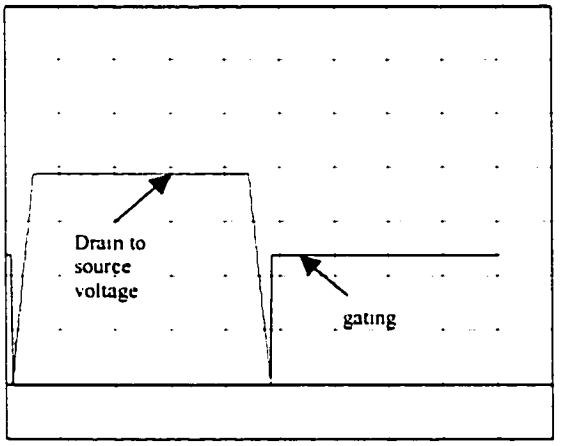
The analysis performed in Chapter 3 has been used to prove the experimental results. The analysis results shown in Figs. A.5 and A.6 are based on the analysis performed in Chapter 3 using Math CAD software. The experimental results shown in Figs. A.3 and A.4 and the analytical results obtained by analysis shown in Figs. A.5 and A.6 have the same input and output specification.



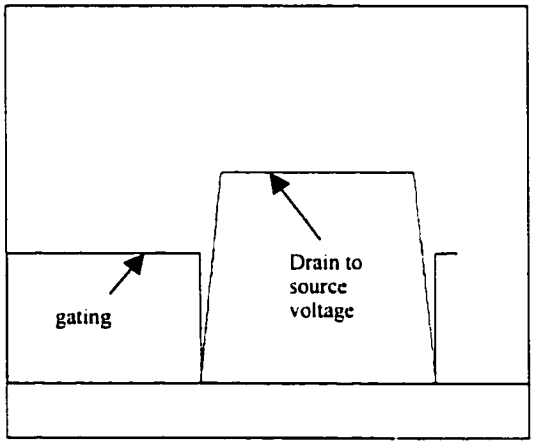
a: ZVS turn-on of switch on Leg A



b: ZVS turn-off of switch on Leg A

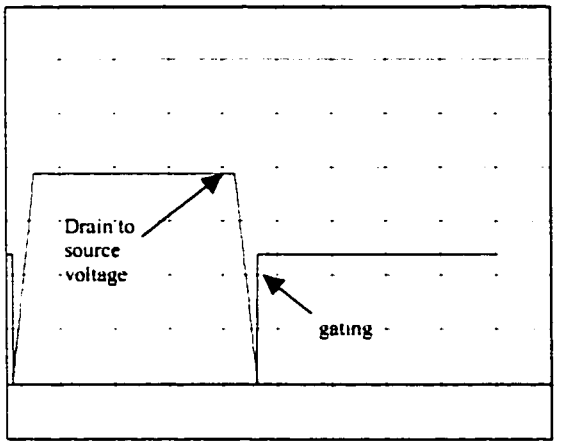


c: ZVS turn-on of switch on Leg B

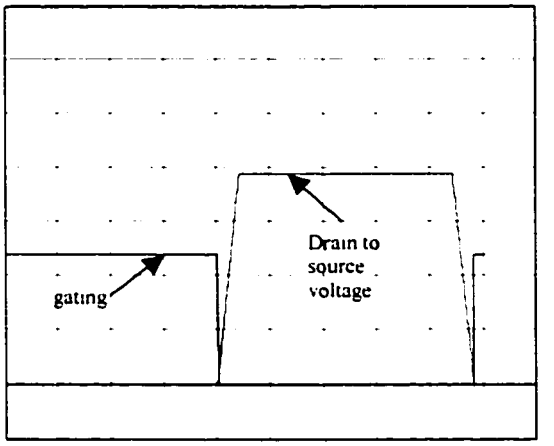


d: ZVS turn-off of switch on Leg B

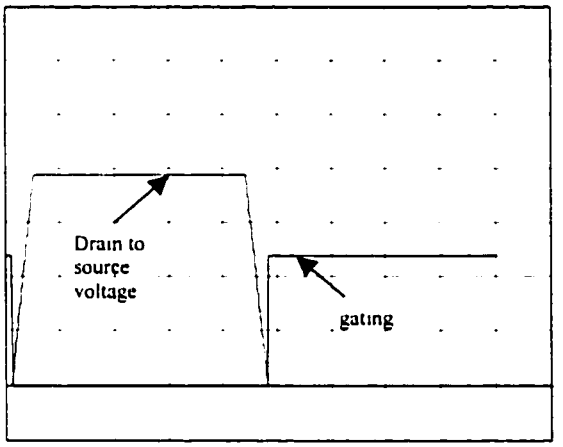
Fig. A.5. The gating and drain-to source waveforms of the switches under full load condition. f_s=128 kHz, V_o=55 V, P_o=500 W, V_d=390 V.
Vertical scales: 100V/div. for the drain voltage, 5V/div. for the gating signal.
Timing:1μs/div.



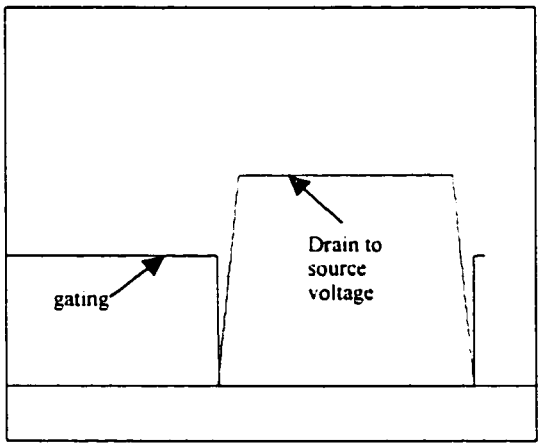
a: ZVS turn-on of switch on Leg A



b: ZVS turn-off of switch on Leg A



c: ZVS turn-on of switch on Leg B



d: ZVS turn-off of switch on Leg B

Fig. A.6. The gating and drain-to source waveforms of the switches under light load condition. f_s=128 kHz, V_o=55 V, P_o=50 W, V_d=390 V.
Vertical scales: 100V/div. for the drain voltage, 5V/div. for the gating signal.
Timing:1μs/div.