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LOW-COMPLEXITY STRUCTURES FOR DIGITAL SYMBOL TIMING RECOVERY

Robert Morawski

A Thesis

in

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ABSTRACT

Low Complexity Digital Implementation Structures for Symbol Timing Recovery

Robert Morawski

Symbol timing recovery (STR) is required in every digital synchronous communications receiver, since the output of the demodulator must be sampled periodically at symbol rate, at the precise sampling time instants in order to correctly recover the transmitted data. The major objective of this thesis is to present, analyze and prove feasibility of the new, low complexity, digital implementation structures for STR. The first presented digital structure is a feedback (FB) symbol timing recovery technique, which is based on the Costas loop principle. This technique requires only 5 constant multipliers and 7 adders, and has very low jitter feature, which is very desirable for high level modulation techniques. The structure, with its error tracking capabilities, is perfectly applicable for continuous mode communication systems, however, the required long acquisition time, makes this feedback STR not suitable for short burst mode communication systems. The feedforward (FF) STR techniques, have very short acquisition time, thus they are the perfect candidates for the short burst mode communication systems, and two such FF techniques are presented in this thesis as well. The first presented FF technique uses relatively high symbol over-sampling (16 samples per symbol) to achieve low implementation complexity (2 unsigned adders, 1 RAM block, and 1 serial magnitude comparator), and acceptable jitter, with the help of only 4 symbols long training preamble. Due to high over-sampling rate, the technique is only applicable to communication systems with relatively low bit rate. In order to expand the applicability of this new over-sampling, technique to higher bit rate systems, an optional "add-on" interpolation technique is presented, which can effectively reduce the over-sampling rate to a minimum of 3 samples per symbol. The cost for the improved performance is in the increased implementation complexity (additional 3 summers and 1 divider).

ACKNOWLEDGEMENTS

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$\star$	Convolution operator
α	roll-off factor, or excess bandwidth parameter
a_k, b_k	Transmitted k-th symbol; inphase or quadrature channel
A,B	Loop filter parameters
B	Transmitted signal's bandwidth
BER, P_b	Probability of bit error or bit error rate
B_L	Feedback loop bandwidth
C, C_{BP}	Baseband and passband channel response
$CRLB_{MOD}$	Modified CRLB on symbol timing variance
Δ	Quadrature signal delay constant
$\Delta\,\hat{\tau}_{ML}$	Difference between initial and corrected symbol timing
$\Delta\,\hat{\tau}_{ML_N}$	$\Delta\,\hat{\tau}_{ML}$ normalized to ADC sample period
D(dB)	Bit error rate degradation
E_b, E_{bavg}	Average energy per bit
E_S, E_{Savg}	Average energy per symbol
E_{g_T}	Energy of $g_T()$ transmitter pulse shaping function
E_Y	Energy of the transmitted signal
e_{ML}	Symbol timing error of initial estimate
e_{MLnew}	Symbol timing error of the corrected estimate
e_k	Discrete clock phase error of the feedback loop
e_s, e_{ss}	Steady state timing error
ϕ_I, ϕ_Q	Orthonormal carrier functions; inphase and quadrature
F(z)	Loop filter z-domain representation
f_{SA}, T_{SA}	Frequency and Period of ADC sampling
f_N, ω_N	Nyquist frequency equal to 0.5 symbol frequency

g_R, G_R	Impulse and frequency response of the receiver matched filter
g_T, G_T	Impulse and frequency response of the transmitter matched filter
g, G	Impulse and frequency response of the overall channel
H(z)	Closed loop frequency response
I	Inphase channel
$J_{pk\text{-}pk}$	Peak-to-peak jitter of symbol timing
K_o	The gain of the VCO
K_D	Timing error detector gain
$\Lambda()$	Maximum likelihood function
$\Lambda_L()$	Log-likelihood function
L	Number of samples per symbol from ADC
M	Number of symbols in the observation window
n_C, n_S	The inphase (I) and quadrature (Q) components of bandlimited AWGN
n_{BC}, n_{BS}	Baseband equivalent of I and Q components for bandlimited AWGN
n_{BP}	Passband, bandlimited, noise
N	Number of Observations
N_o	AWGN density
N_k	Equivalent loop noise
ω_{3dB}	Cut off frequency of the loop filter
$\Omega(t)$	Equivalent amplitude modulating signal
p(t), $P(\omega)$	Prefilter impulse and frequency response
P_S	Probability of symbol error
$q(e_k)$	TED characteristic
Q	Quadrature channel
$\underline{r}_I$, $\underline{r}_Q$	Received signal observation vectors; inphase and quadrature
r_I, r_Q	Received, down-converted (baseband) signal; inphase and quadrature signal
RC	Raised Cosine
S_{nc}, S_{ns}	Power spectral density of the n_c and n_s AWGN components

S_N	Power spectral density of equivalent loop noise
σ^2_{nB}	Equivalent variance of the normalized baseband noise
$\sigma^2_{\hat{t}}$	variance of symbol timing estimate
σ^2_e	variance of symbol timing error
τ	True timing offset
τ_i	Trial timing offset
$\hat{\tau}_{ML}$	Estimated optimum symbol timing
$\hat{\tau}_{MLnew}$	Corrected symbol timing
θ	Symbol clock phase error
T_{SYM}, f_{SYM}, ω_{SYM}	Symbol clock period and frequency
T_C, f_C, ω_C	Carrier period and frequency
T_o	Observation interval
T_A	Acquisition time
u_k	Discrete averaged error signal of the feedback loop
v_{nc}, v_{ns}	The I and Q noise components at the output of rcv. matched filters
$var(e_{MLnew})$	Variance of symbol timing error of the corrected estimate
var_{IMP}	Lower limit on variance due to implementation technique
v_{nPFLT}	The noise component after prefilter
$w(\tau)$	Derivative of the log-likelihood function Λ_L
x_k	Discrete error signal of the feedback loop
$y(\theta)$	Transmitted signal
y_I, y_Q	Modulating signals; inphase and quadrature
z_I, z_Q	The output of rcv. matched filter; inphase and quadrature signals
z_{MF}	Output of receiver's matched filter

CHAPTER 1.

INTRODUCTION

In digital data transmission, to perform demodulation at the receiver, there is a choice of: coherent detection (which provides optimum error performance, but requires carrier recovery CR) or noncoherent detection (which does not require CR, but results in worse error performance). Symbol timing recovery (STR), on the other hand, is required in every digital communications receiver (where the bit clock is not provided), since the output of the receiver filter must be sampled periodically at symbol rate, at the precise sampling time instants in order to correctly recover the transmitted data. The most simple digital receivers are asynchronous receivers, since they don't need the special symbol synchronization circuit. However, their application is limited only to low speed transmissions (110 bps to 19.2 kbps), since they need a lot of overhead bits to correctly receive the message data packets, and thus they have very low data throughput efficiency [1]. The synchronous systems, which provide bit clock by sending it over the separate channel (wire or wireless) are wasting channel bandwidth, which nowadays is scarce and expensive. Thus, the symbol clock recovery is truly indispensable, and the most critical function in the modern data communication systems.

Although there has been many symbol synchronizers developed in the past, the never stopping need for higher data rates pushes the previous designs to the limits, thus, the new, more accurate, faster, and more cost effective techniques have to be researched continuously. In this thesis a new structure for very accurate feedback symbol synchronizer is presented in Chapter 2, and then in Chapter 3 there are two additional, very fast, feedforward symbol synchronizers

proposed. All three synchronizers are based on digital signal processing (DSP), have low hardware complexity, and it is assumed that carrier recovery is done prior to STR [2].

The reason that two types of synchronizers (FB and FF) are investigated in this thesis is that both types might be often required in a single system. For example, most of today's internet applications need much greater (by 8 times for asymmetric digital subscriber line ADSL system) downstream throughput (960kps from the ADSL access point) than the upstream throughput (120kbps from the ADSL end user). This fact dictates higher level modulation scheme, and more precise (lower timing jitter) STR for the downstream link rather than the for the upstream link. On the other hand, the upstream short burst mode link receiver might need a STR with a much shorter timing acquisition than the downstream continuous link receiver [3, Chapter 7].

It should be noted, that the proposed feedback and feedforward symbol synchronizers (with some modification to the assumptions) can have wide range of applications (wire-line or wireless channels, point-to-point or point-to-mulitpoint systems, Local Multipoint Communication System (LMCS), Local Multipoint Distribution System (LMDS), etc.), however, for illustration purposes only the broadband wireless access (BWA) system application example is presented in this thesis. The following paragraph gives a short introduction to BWA systems.

Recently the broadband wireless access systems have received a great interest, because they are highly reliable (fixed systems) and can provide enough bandwidth (up to 155Mbps for 802.16) to deliver high speed data, video, and voice services, in places where the existing wiring is not up to the job or does not exists at all. It has been shown, that even in congested urban areas, the deployment and operating cost of BWA system is much lower when compared with optical-fiber or wire-line systems [4]. The "broadband" name implies operation in high data rates (2-155Mbps for 802.16), thus high-level modulation schemes such as 16, 64 or 256 quadrature amplitude modulation (QAM) technologies are most likely to be used. The M-ary QAM are very power efficient techniques, and are more easily implemented than M-ary phase-shift keying (PSK)

techniques. A broadband wireless access system, based on IEEE 802.16 standard (currently in development), is defined as a system that provides access, over the radio communication link, to an external network, such as the Internet, ISDN or CATV. Note: in this thesis only the line-of-sight (LOS) link is considered for simplicity, the effects of multipath or frequency selective channel would have to be rectified before applying the proposed STR techniques). As shown in Figure 1—1, an 802.16 system consists of point-to-multipoint (P-MP) fixed radios linking a base transceiver station (BTS) to one or more subscriber transceiver stations (STS) [5]. The preliminary notes on 802.16 state that the BWA system should allow for flexible asymmetry between delivered upstream (STS to BTS) and downstream (BTS to STS) bandwidth, where the expected downstream bandwidth is much greater than upstream bandwidth (assume by 8 times as in ADSL). For internet application the upstream link bandwidth requirement is usually much smaller, because the link consists mostly of requests rather than big block of data. In this thesis, a scheme in which the base station transmits a continuous mode time-division multiplexing (TDM) signal to all subscribers, and each subscriber transmits a burst mode time-division multiple-access (TDMA) signal only to the base station, is assumed.

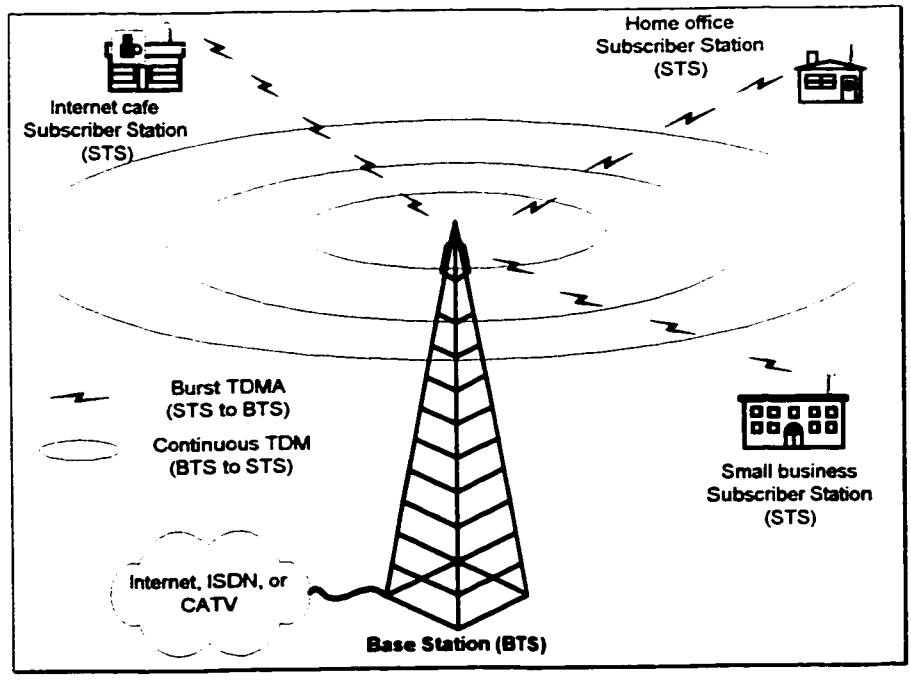

Figure 1—1. Broadband Wireless Access (IEEE 802.16) System.

1.1. Symbol Synchronization

In general, symbol synchronization, also called timing recovery, extracts symbol timing clock from the received signal, this regenerated clock is used to periodically (at symbol rate), sample the output of the demodulator, and based on these samples a decision on the received symbol is made. For a maximum noise immunity and the least bit error rate degradation, the regenerated symbol clock should sample the demodulated signal at the instant of maximum eye opening, thus the receiver must precisely know not only the symbol frequency, but also symbol clock phase (which depends on the propagation time of the signal from the transmitter to the receiver).

There are many symbol recovery techniques, which can be categorized in several ways. The synchronization techniques could be analog or digital. Further, based on the operation relative to carrier recovery, the STR can be done jointly with CR, or separately (independently or after CR is done). From the operating principle point of view the symbol timing recovery techniques can be divided into: error-tracking (or feedback, or closed loop) and feedforward (or open loop) types. The last classification, listed here is based on the utilization of the transmitted symbol sequence, that is: the synchronizer could be data-aided (DA) or decision-directed (DD), when it uses a training symbol sequence or detected symbol sequence, respectively, to help in synchronization, or the synchronizer could be non-data-aided (NDA), where no information about a particular symbol sequence is used. The above listed types of STR technique are presented in a tree form in Figure 1—2. Each type has its own advantages, the choice of a particular approach is determined by the given application requirements.

1.2. Characteristics of Symbol Synchronizers

The three most common specification characteristics used to evaluate the timing recovery algorithm are: the variance of recovered symbol clock (i.e. timing jitter or timing error), the acquisition time, and the complexity of a given symbol timing recovery (STR) technique.

1.2.1. Variance

The minimum variance of the recovered symbol clock (i.e. minimum timing jitter) is very desirable as the number of signal modulation levels increases, since the width of eye opening decreases, and the correct decision, on the received symbol, is more difficult. For example, for a 2-PAM (or 4-QAM) signal, the width of the eye opening is relatively large (see Figure 1—3), thus to satisfy the minimum bit error rate degradation due to synchronization errors, even a moderate symbol clock's variance (or jitter) is acceptable. However, for 16-PAM (or 256-QAM), the width of the eye opening is so small, that to achieve the minimum bit error rate (BER) degradation of 0.3 dB, the peak-to-peak jitter (related to variance) has to be less than 1.1 % [6]. In [7] it has been demonstrated, that the analog Costas loop, feedback, symbol synchronizer could achieve these very low jitter requirements, and this technique is modified in Chapter 2 for DSP-based version. In summary, the minimum achievable timing error, determines which modulation technique can be used with a given STR technique, and what will be the corresponding supported data rate.

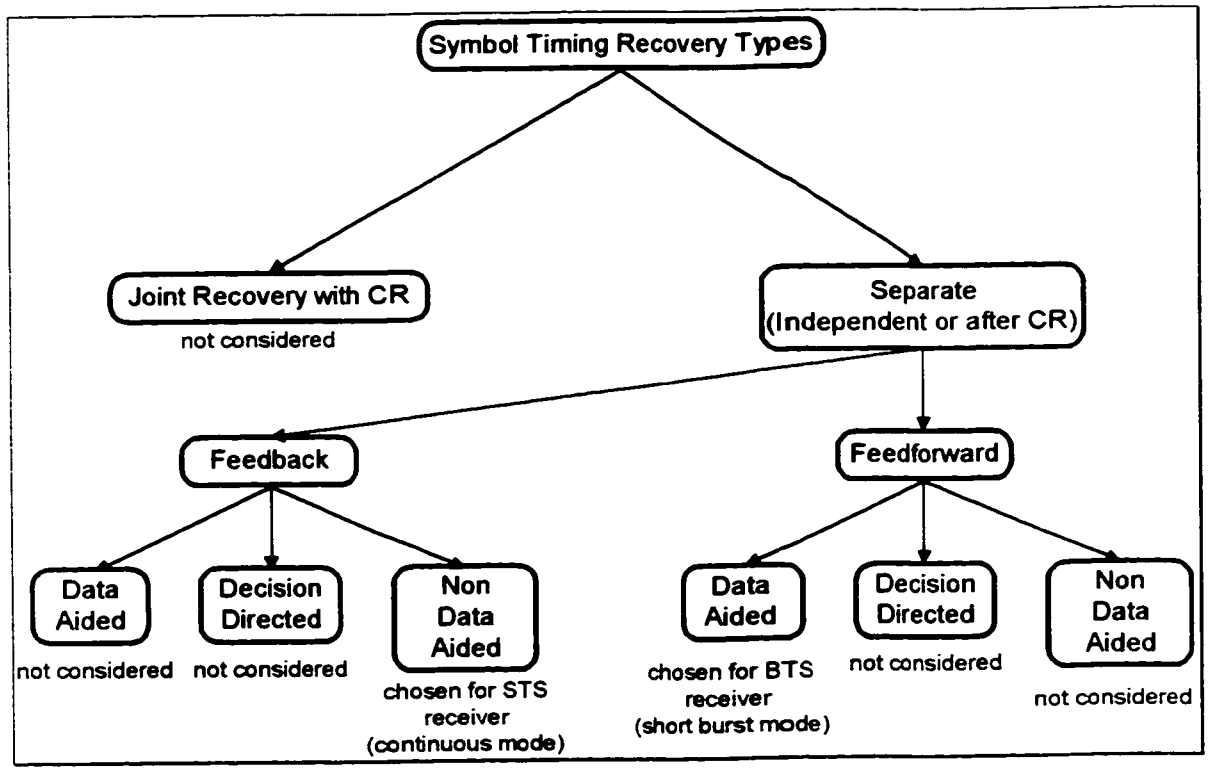

Figure 1—2. Symbol Timing Recovery Types Tree.

1.2.2. Acquisition

The acquisition time of a symbol synchronizer is the time duration from the beginning of the received signal, until the frequency and the phase of the symbol clock is successfully recovered. In continuous mode communications the acquisition time is not very critical, since the amount of time wasted for acquisition is usually insignificant when compared with the duration of the whole transmission. However, the minimum acquisition time is crucial for the short and medium burst mode communications, where the duration of a single transmission (burst) can be a low as 100 symbols.

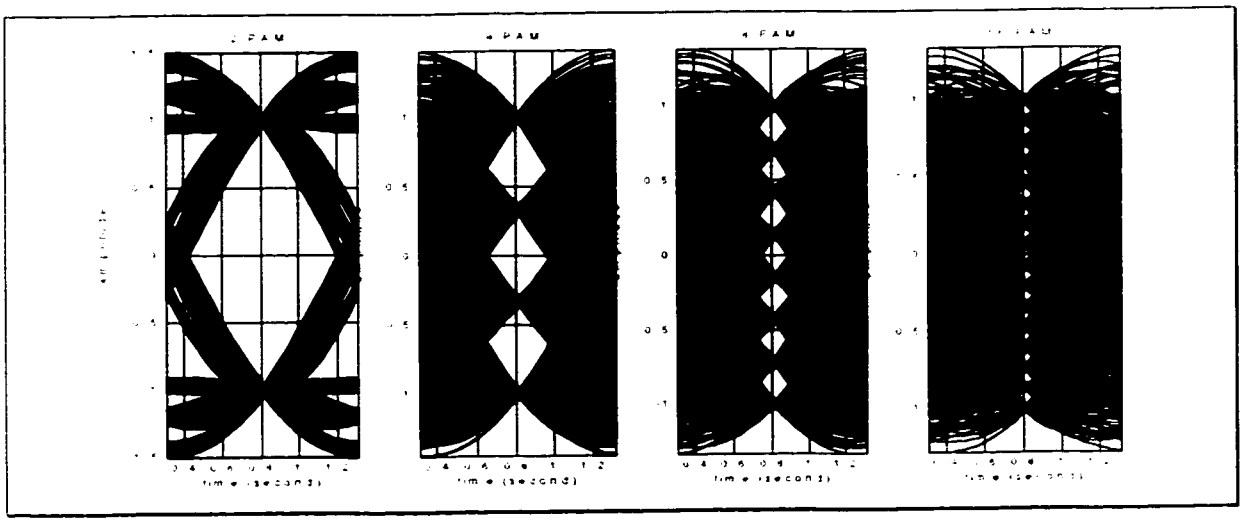

Figure 1—3. Eye Openings of PAM Signals.

A typical burst consists of preamble (containing carrier recovery, CR, [2] and symbol timing recovery ,STR, training symbol sequences and some other system specific symbols such as: Unique Word, which is used for payload data start detection, and frame synchronization, not investigated here) followed by, revenue producing, message portion (see Figure 1—4). Note: the burst segmentation in this figure is not drawn to scale, in practice the payload data section is much larger than the training section. It can be easily noticed that in order to increase message data transfer efficiency (or revenue) of the system, the length of the training section (which is directly proportional to acquisition time) should be reduced. The feedback synchronizers have

long acquisition time, and thus from data transfer efficiency point of view, are not applicable for short burst mode communication systems. As suggested in [8], for short burst mode receivers the feedforward STR techniques are a much better choice, and this idea is followed in Chapter 3.

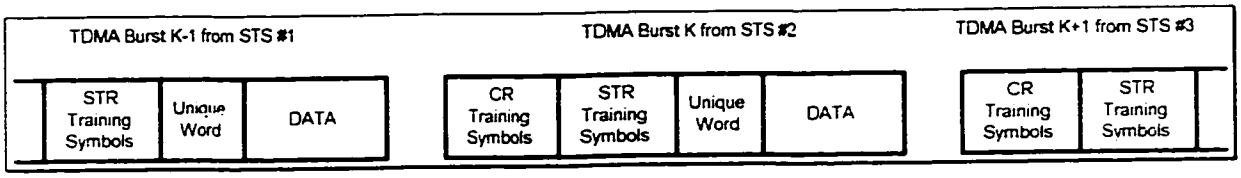

Figure 1—4. Time Division Multiple Access Bursts.

1.2.3. Complexity

The analog symbol timing recovery algorithms have been well studied and widely implemented in the past. However designing an optimum (based on ML estimation) analog symbol synchronizer is very difficult due to the required mathematical functions, which are not practically implementable using analog techniques.

In the last two decades advances in the area of digital signal processing (DSP) has allowed for many fairly complicated mathematical functions to be easily implemented on a single chip. Thus nowadays, the digital symbol timing recovery algorithms became the ultimate choice for the highest performance practically implementable designs, as pointed out in [9]. The digital algorithms not only have the computational advantage (in terms of easy implementation of delay, and other mathematical functions) over analog algorithms, but also when implemented for example on Field Programmable Gate Array (FPGA) chip, they are much easier and faster to verify in practice, do not require tuning and can also be remotely reconfigured or updated on customers premises.

The remote reconfiguration is one of the current hot research areas, called software radio. The principle idea behind the software radio is to have one universal device or circuit, which could

download a desired hardware configuration, instead of having parallel circuits and switching between them, depending on the need at the given time [10]. The reconfigurability could be very useful in the 802.16 system, which should allow for flexible asymmetry in the upstream or downstream bandwidth (satisfied by different modulation schemes 4, 16, 64 or 256-QAM).

1.3. Scope of Thesis

This chapter presented the importance of symbol synchronization and outlined symbol synchronization types and characteristics, from the broadband wireless access systems perspective.

Chapter 2 proposes a new digital implementation structure, analyzes, and presents performance simulation results, of the DSP-based Costas loop for low-jitter timing synchronization. The analysis and simulations were performed for the mean (steady state error), the variance, the acquisition time and the pull-in frequency range for 2, 4 and 8 level pulse amplitude modulation (PAM) signal. As is explained in that chapter these results also apply to 4, 16 and 64-QAM schemes. The feedback technique from Chapter 2 is applicable for the subscriber's high-level modulation, continuous mode TDM receiver in the BWA system.

Chapter 3 proposes two new digital implementation structures, analyzes, and presents simulation and practical measurement results for the data-aided, feedforward, timing estimation techniques. The analysis included the mean and the Cramer-Rao lower bound (CRLB) for the variance derivation, and the bit error rate estimation. The simulations were performed for the mean, the variance, and the bit error rate performance for 4 and 16-QAM signal. The practical measurements involved bit error rate testing for 4 and 16-QAM signals with 2 and 4 symbols long STR preamble. The feedforward techniques from Chapter 3 are applicable for the base station's burst mode TDMA receiver in BWA system.

Conclusions and suggestions for further research are given in Chapter 4.

1.4. Contributions of Thesis

The major objectives of this work are to present:

- new digital implementation of the Costas loop for timing synchronization, which needs only 4 samples per symbol analog to digital converter (ADC) sampling rate, has much faster acquisition time than the analog counter part [7], has satisfactory pull-in frequency range, and still maintains very low jitter. This error tracking, feedback, symbol timing recovery technique is for the application in high level modulation, continuous transmission mode, AWGN channel systems.
- new digital implementation of data-aided, feedforward (FF), symbol timing recovery/estimation (timing phase only, i.e. frequency is assumed to be known) technique, which is based on highly over-sampled (16 ADC samples per symbol) Maximum-Likelihood technique, but requires only 4 symbols of preamble for 0.2 dB signal to noise degradation at bit error rates down to 10^{-6}. This feedforward, estimation technique is for the application in a 4-QAM (16-QAM), short burst transmission mode, AWGN channel systems. Note: the correct timing for the whole burst is estimated only during 4 symbols at the beginning of the burst.
- new digital implementation of the optional (i.e. has to operate with previous FF technique, but with lower number of samples per symbol) inverse interpolation technique, which reduces the required ADC sampling rate down to only 3 samples per symbol, and still assures that recovered symbol timing does not degrade the system performance by more than 0.2 dB. The cost for the reduced ADC sampling rate is the increased hardware complexity. Note: this feedforward, estimation technique is also for the application in short burst transmission mode, AWGN channel systems.

CHAPTER 2.

A DSP-BASED COSTAS LOOP FOR LOW JITTER TIMING SYNCHRONIZATION

This chapter presents a new DSP based implementation of the Costas loop for low-jitter symbol synchronization. The technique is based on the prefiltering and Costas Loop symbol synchronization, which have been well studied, from analog implementation perspective, in [11] and [7]. The key feature of this particular timing recovery scheme is a very low jitter, which, as mentioned in Chapter 1, is essential for optimum performance in high capacity communication links, such as downstream (base to subscriber station) link in broadband wireless access system.

The main research contributions of this chapter are the development, and performance simulations of a low complexity, digital implementation, structure for the Costas loop symbol synchronizer. An outline of this chapter is given in the following paragraph.

This section briefly introduced what the presented symbol synchronizer is based on, what are its main features, and it pointed out what are the main research contributions of this chapter. Section 2.1 gives a background on the feedback symbol synchronizers, related to the presented technique. In Section 2.2 the assumed system configuration is outlined. Section 2.3 describes the functional operation, and frames the new modified digital Costas loop symbol synchronizer into a general structure, the equivalent, and the linearized equivalent model, in order to analyze its performance behavior in the following sections. Section 2.4 analyzes, and simulates the effect

of input noise, initial frequency offset, and loop bandwidth on the steady state (or mean) error of the proposed technique. It is important to check that on average the symbol timing error (i.e. mean error) is very close to zero, otherwise, the system might be completely unusable even in noiseless environment. Section 2.5 analyzes and simulates the variance of the timing error versus the same parameters as in Section 2.4. Even if on average the timing error (mean) is zero, a large variance could significantly degrade the bit error rate performance (as shown later), thus the system parameters minimizing the timing error variance should be always carefully selected. Section 2.6 studies the effect of loop bandwidth parameter on the maximum frequency detuning range between transmitter and receiver symbol clock oscillators. If the frequency detuning is greater than allowed, the timing recovery circuit would never synchronize to the input signal. Section 2.7 shows that the proposed digital implementation of Costas loop, with its low timing error variance (corresponding to 1-2% timing jitter), suffers less than 0.2 dB degradation with respect to ideally synchronized case. The 0.2 dB BER degradation is the maximum recommended value for good symbol synchronizers [8, Chapter 7]. The acquisition time simulation results, in Section 2.8, illustrate that the timing error convergence to the steady state value, for the proposed digital technique, is much faster (only 100 symbols of acquisition time) than for the analog counter part presented in [7]. Section 2.9 concludes Chapter 2 with the presentation of the implementation complexity in terms of adders and multipliers.

2.1. Background

The extensive treatment of symbol timing synchronization for digital receivers has been covered in [8], thus only the background directly related to the investigated technique is presented in this section. The investigated technique assumes that the receiver operates in continuous data transmission mode, i.e. not burst mode.

In communication systems, where the transmitter and receiver are in physically separate locations (as in BWA system), the local oscillator symbol clocks never have exactly the same

frequencies. Since each receiver (in STS), most likely, has a different distance from the transmitter (in BTS), the symbol clock phase (dependent on propagation time delay) will be different for each receiver. Also due to limited, long term, frequency stability of the oscillators, this symbol clock phase might be slowly varying in time. Thus, for the continuous transmission mode receiver, the implemented symbol synchronizer has to not only lock to the transmitter's symbol clock frequency, but also has to continuously track the symbol clock phase changes, in order to reliably recover the information data, throughout the whole duration of the transmission. The symbol timing synchronizers, which can satisfy these requirements belong to the feedback (error-tracking), non-data-aided (NDA), symbol timing synchronization category.

In a general error-tracking symbol timing synchronizer, the noisy demodulated input signal and the locally generated reference signal are "compared" by means of a timing error detector (TED), whose output gives an indication of the magnitude and the sign of the timing error. The filtered timing error detector output signal adjusts the timing estimate in order to reduce the timing error. At the steady state (after the acquisition period), the timing estimate is used to sample the demodulated signal once per symbol, and that sample is used for symbol decision in the next stage of the receiver [8 Chapter 2].

There has been many different feedback symbol timing synchronizers developed in the past:

- data-aided (DA), which use a special training symbol sequence transmitted with the message portion of the total symbol sequence, in order to shorten the acquisition time
- decision directed (DD), which uses the output of the receiver's symbol decision device to aid the synchronization process
- and non-data-aided (NDA), which do not require any information on the transmitted symbol sequence.

Some of the feedback symbol timing synchronizers are: Early-Late Gate [12], Data Transition Tracking Loop [13], Mueller and Müller [14] and Spectral Line Generating with phase lock loop symbol timing synchronizers [8, Chapter 2.4]. The differences between all of the error-tracking

symbol timing synchronizers are in the timing error detector implementation, and the performance characteristics. The required performance characteristics and implementation complexity usually determine which symbol synchronizer should be used for a particular system. As mentioned in Chapter 1, in the high capacity (high level modulation) receiver (as in STS of BWA system), one of the most important performance characteristics is very low variance (or jitter) of the recovered symbol timing.

The variance (or jitter) of the recovered symbol clock is caused not only by the noise in the channel, but also by the inter-symbol interference (ISI) at the zero crossing [13] [14]. In bandwidth limited communication systems, the transmitted pulse shape is designed according to the Nyquist criterion of zero ISI at the symbol sampling point [3, Chapter 6.4], but the in other regions of the symbol (including zero crossing) the ISI still exists. Thus even in the noiseless environment, the timing recovery techniques mentioned in the previous paragraph will have some nonzero jitter.

Franks and Bubrouski in [11], have proved that by applying special prefiltering (which removes ISI from the zero crossing of the received signal), and the squarer timing synchronizer with symmetric bandpass post-filtering (see Figure 2—1), a jitter-free recovered symbol timing can be achieved. The analysis of Franks and Bubrouski was extended to show that the same technique could also be applied to K-PAM (and K^2-QAM), and demonstrated, that a perfect prefiltering of the received baseband signal produces an equivalent double-sideband, suppressed carrier (DSB-SC) passband signal centered at the Nyquist frequency (half of the symbol clock frequency). Using this observation a Costas Loop (see Figure 2—2) was introduced to replace both the squarer and the bandpass post filter, thus simplifying the practical implementation. The jitter performance of this Costas Loop symbol synchronizer was measured to be 2 % (which is extremely low) of T_{SYM} for 2-PAM signal with E_S/N_o= 16 dB. The practical drawbacks of this technique, which are resolved in this thesis, are the required tuning of the analog components, and the excessively long acquisition time (reported to be 184,000 symbols [7]).

In this chapter, the prefiltering and Costas Loop symbol timing synchronization technique are is presented in a modified, low complexity, digital implementation version (which eliminates most of the tuning requirements). As will be shown by simulation results, this modified version is able to recover the symbol timing with minimal jitter and significantly reduced acquisition time, in the AWGN environment within practical range of symbol frequency offsets.

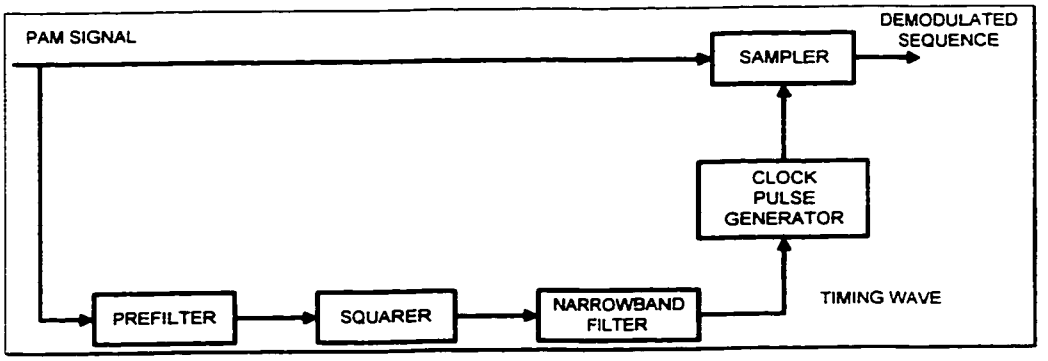

Figure 2—1. Symbol Timing Recovery Technique Proposed by Franks and Bubrouski.

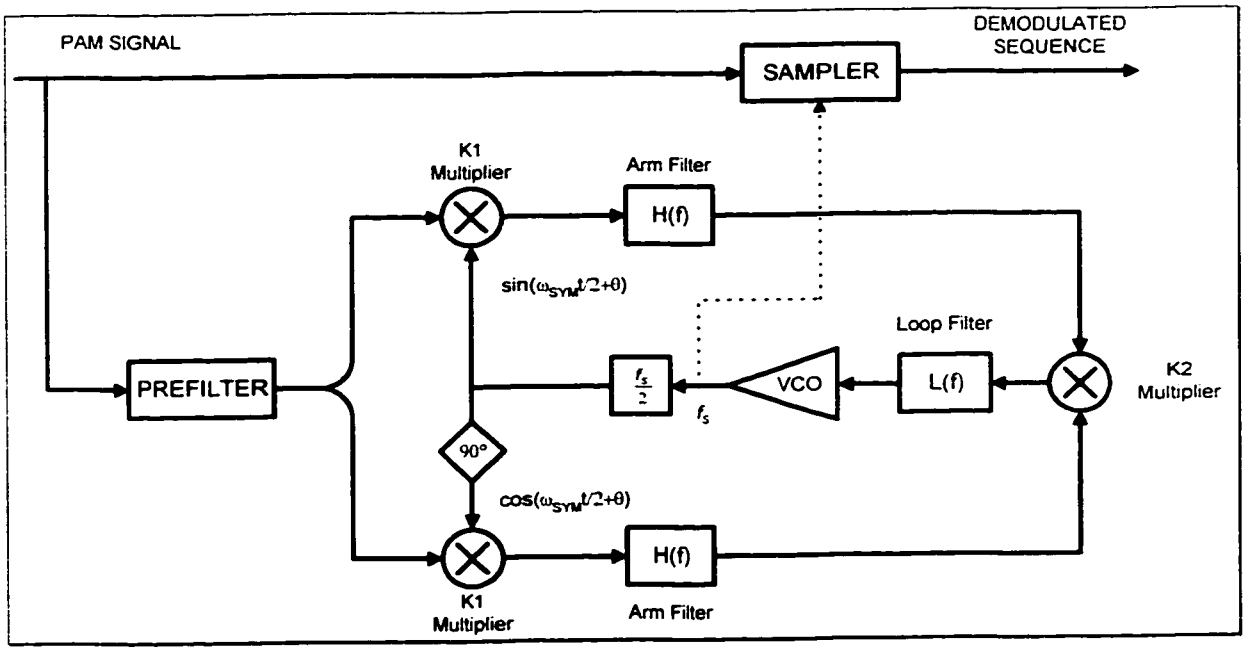

Figure 2—2. Costas Loop Symbol Synchronizer.

2.2. System Configuration

The feedback symbol timing recovery technique presented in this chapter was analyzed and simulated for 2, 4 and 8 PAM systems. However, this technique can also be easily extended to K^2-QAM systems, since the received QAM signal after quadrature down-conversion (I and Q components) is equivalent to two K-PAM signals, and one of these K-PAM signals can be used with the proposed feedback timing recovery technique. The presented technique is best suited for continuous mode and long burst mode systems, due to relatively long (100 symbols) acquisition time. However, if some form of rough initial clock phase estimate is available, this technique can also be applied to medium length burst mode communication systems as well. A good application example of this symbol synchronization technique is the receiver in the STS of BWA system, as mentioned in Chapter 1 (see Figure 1-1).

The following are the main system assumptions considered in this chapter.

The first assumption is that the received down-converted signal is already corrected for carrier phase and frequency errors, as shown in Figure 2—3 [2]. In some digital receivers, symbol timing recovery is preferred to be done prior to carrier recovery, since having only one sample per symbol reduces the computational load of the carrier recovery in the receiver [8, Chapter 5.1]. However, for this thesis project, the utilized carrier recovery algorithm, which was symbol timing independent, explicitly relied on having more than one samples per symbol (for fast acquisition) [2], thus this first assumption is justified and significantly simplified the STR design.

The second assumption is that the symbol clock phase and frequency of the received signal are not known. However, an error in symbol clock frequency, between the receiver and the transmitter, should not exceed 100 PPM for satisfactory minimum BER degradation. This requirement, on symbol frequency offset, is usually satisfied (when assumed that the transmitter's

symbol clock is derived directly from the fixed crystal oscillator i.e. not voltage controlled oscillator) [8, Chapter 6.5].

The third assumption is that the communication channels are only disturbed by AWGN, for example the wireless line of sight (LOS) communication channels of a stationary (fixed) system. The effects of other signal distortion sources, such as: multipath or frequency selective channels are not investigated here, but application of other techniques such as pre-equalization for frequency selective channels could make the presented STR technique still applicable.

The fourth assumption, based on the limitation of the technique (see Section 2.9), is that the minimum signal sampling rate at the input of the symbol synchronizer is $f_{SA}=4f_{SYM}$.

The above listed assumptions are summarized in Table 2—1, and a general block diagram of the assumed demodulator with feedback and optional feedforward symbol synchronizer is shown in Figure 2—3.

Table 2—1. General Communication System Assumptions.

	Assumption Description
1	K-PAM, K^2-QAM
2	AWGN channels
3	Unknown symbol clock frequency and phase
4	The carrier recovery is done prior to symbol timing recovery
5	Signal Sampling Rate $\geq 4\ f_{SYM}$
6	Continuous Transmission Mode

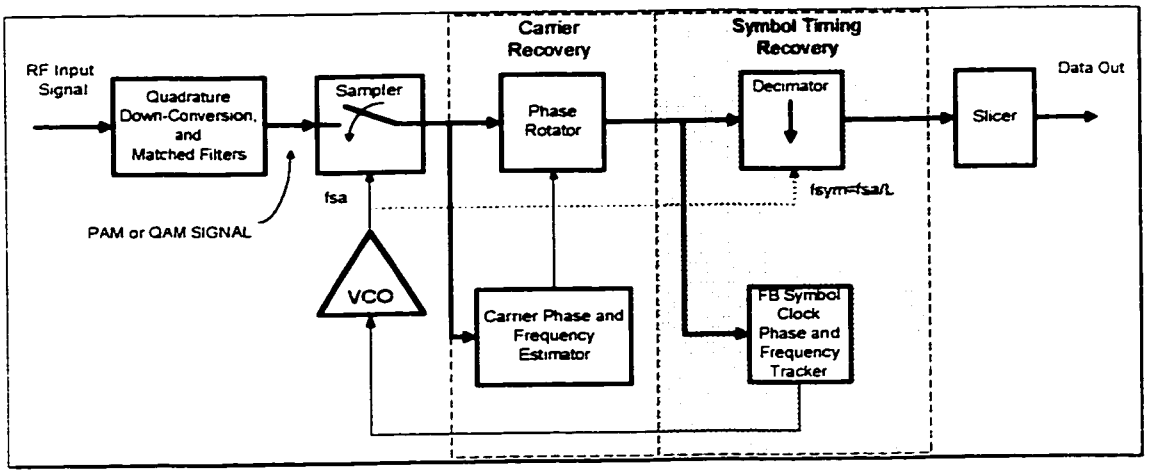

Figure 2—3. General Block Diagram of the Assumed Demodulator.

2.3. Structure of the DSP-based Costas Loop Timing Synchronizer

In this section the assumed received signal model is shown, the proposed structure of DSP-based Costas Loop for low jitter timing synchronization is presented, and the equivalent model of the synchronizer is derived.

2.3.1. Signal Model

In order to make the description of the proposed structure of DSP-based Costas Loop symbol synchronizer easier, the communication path from the transmitter to the receiver is represented by the equivalent baseband model shown in Figure 2—4, and described in the following paragraphs. The equivalent signals, at different points of the transmission path, have been derived in Appendix A.

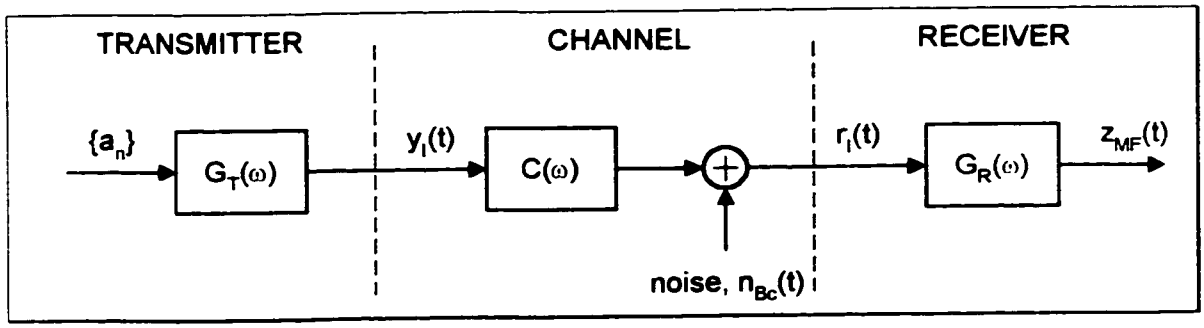

Figure 2—4. Transmission Path Equivalent Baseband Model.

Input sequence

In the above equivalent baseband model, the input sequence of the K levels data symbols $\{a_n\}$ is assumed to be produced from the continuous, random, input data bits stream.

Transmitter Filter

Data symbols, a_n, pass through the transmitter pulse shaping filter with impulse response $g_T(t)$, and the resulting transmitted signal is given by:

$$y_I(t) = \sum_{n=-\infty}^{\infty} a_n g_T(t-(n+\tau)T_{SYM}) \qquad \textbf{(2-1)}$$

where:

a_n : is a stationary sequence of channel symbols (K levels)

T_{SYM} : Symbol period

τ : Normalized symbol clock phase offset, incorporating the unknown time delay, resulting from the linear phase distortion of the channel between the transmitter and the receiver, $|\tau| \leq 0.5$.

Channel

The transmission channel is assumed to have constant magnitude frequency response, $|C(\omega)|=1$, with linear phase distortion (accounted for in a transmitted signal description, equation (2-1)), and

it is assumed that the transmitted signal is disturbed by AWGN $n_{Bc}(t)$, with zero mean and variance of $N_o/(4E_b)$ (derived in Appendix A). Thus, the received signal is:

$$r_I(t) = y_I(t) + n_{Bc}(t) \tag{2-2}$$

Receiver Filter

The received noisy PAM signal is applied to the receiver matched filter, with impulse response $g_R(t)=g_T(-t)$, thus the output of the receiver matched filter is:

$$z_{MF}(t) = \sum_{n=-\infty}^{\infty} a_n g(t-(n+\tau)T_{SYM}) + v_{nc}(t) \tag{2-3}$$

where:

- $g(t)$: is the overall system pulse shaping function, $g(t)=g_T(t)\bigstar g_R(t)$, convolution of g_T and g_R
- $v_{nc}(t)$: is zero-mean stationary noise, $v_{nc}(t) = n_{Bc}(t)\bigstar g_R(t)$

It is assumed that the pulse shaping function g(t) is a raised cosine function, with rolloff factor α. The raised cosine function, is a practical pulse shaping function choice satisfying the Nyquist criterion for distortionless baseband transmission in the absence of noise and ideal symbol timing (i.e. zero ISI at the maximum eye opening sampling point), and is defined in time domain as [3, Chapter 6]:

$$g(t) = \frac{\sin(\pi t/T_{SYM})}{\pi t/T_{SYM}} \frac{\cos(\alpha \pi t/T_{SYM})}{1-4\alpha^2 t^2/T_{SYM}^2} \tag{2-4}$$

where:

- α : is the rolloff factor chosen to be 0.5, as a compromise between the signal BW $B=(1+\alpha)/(2T_{SYM})$, and the sensitivity to timing error (when α decreases, B decreases, but the sensitivity to timing error increases)

The raised cosine function in frequency domain is defined as:

$$G(f) = \begin{cases} T_{SYM} & |f| < \frac{1-\alpha}{2T_{SYM}} \\ \frac{T_{SYM}}{2}\left\{1+\cos\left[\frac{\pi T_{SYM}}{\alpha}\left(|f| - \frac{1-\alpha}{2T_{SYM}}\right)\right]\right\} & \frac{1-\alpha}{2T_{SYM}} \le |f| < \frac{1+\alpha}{2T_{SYM}} \\ 0 & |f| \ge \frac{1+\alpha}{2T_{SYM}} \end{cases} \quad \text{(2-5)}$$

2.3.2. Structure Description

The general block diagram of the considered receiver is shown in Figure 2—3. It is assumed that the received analog signal is down-converted to the baseband, filtered by the receiver's matched filters, and this signal (or inphase and quadrature signals for K^2-QAM) is fed to the analog-to-digital converter (ADC). In practice, the Carrier Recovery (CR) module generally delays the signal's path, but here for description clarity this delay and CR module itself are ignored. The quantization effect is also being neglected. The ADC and all other symbol timing recovery circuitry is clocked by the voltage or numerically controlled oscillator (VCO or NCO), which is driven by the generated symbol timing error signal. The simplified block diagram of the synchronizer, without CR and optional feedforward estimator section (feedforward estimator might be used to improve the overall acquisition time, but is not considered here), and with the expanded feedback synchronizer, is shown in Figure 2—5. The proposed structure of DSP-based Costas Loop timing synchronizer consists of the prefilter and the modified digital Costas loop. These components are described in the following paragraphs.

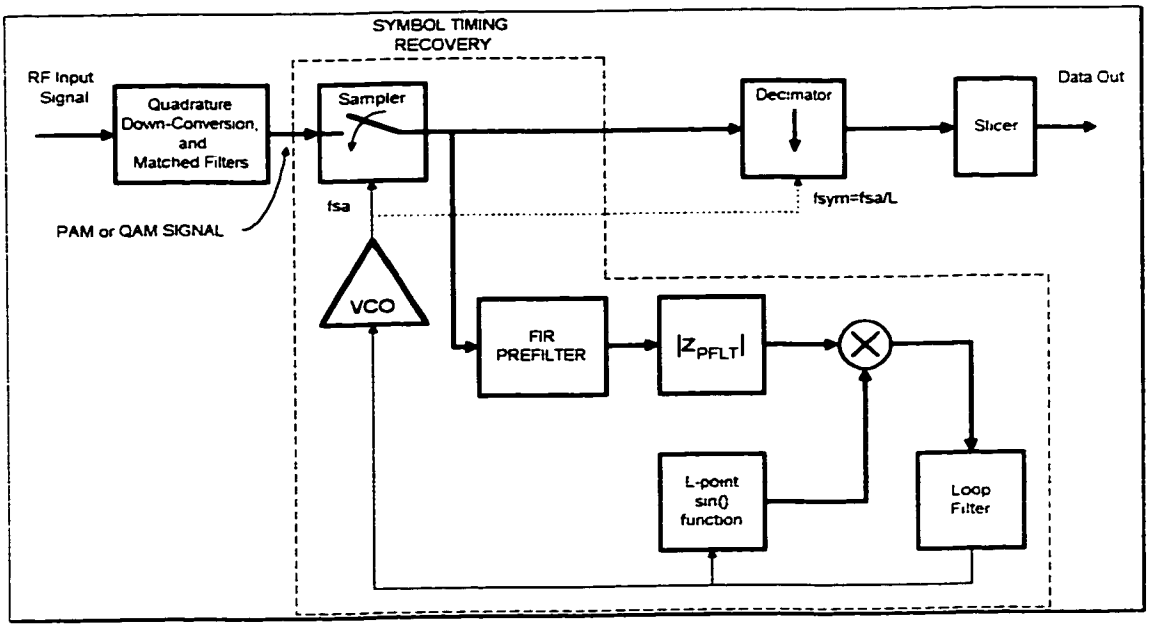

Figure 2—5. Simplified Block Diagram of Feedback Synchronizer.

Prefilter

The input signal to the feedback synchronizer is the output signal from the Quadrature Down-Conversion and matched filter block sampled at t_{sa} (see Figure 2—5). This signal is assumed to be a K-PAM signal, which, as shown in equation (2-3), can be written as :

$$z_{MF}(t_{sa}) = \sum_{n=-\infty}^{\infty} a_n g(t_{sa} - (n+\tau)T_{SYM}) + v_{nc}(t_{sa}) \qquad \textbf{(2-6)}$$

This above signal has zero ISI at the maximum eye opening (i.e. at optimum symbol sampling point), but it contains significant ISI at the zero crossings (see Figure 2—6), which would normally introduce jitter to the recovered clock. As suggested by Franks and Bubrouski [11], in order to achieve zero jitter in the recovered clock, the received baseband signal should be prefiltered, such that there is no ISI at the zero crossings and the spectrum of the prefilter's output is symmetric about the Nyquist frequency $f_N=0.5f_{SYM}$, and its bandwidth is $\leq f_N$ (see Figure 2—7). This condition can be expressed as:

$$Z_{PFLT}(\omega)=\begin{cases}0 & 0.5\omega_N>|\omega|>1.5\omega_N\\ Z_{PFLT}(2\omega_N-\omega) & 0.5\omega_N<\omega<1.5\omega_N\\ Z_{PFLT}(-2\omega_N-\omega) & -1.5\omega_N<\omega<-0.5\omega_N\end{cases} \quad \textbf{(2-7)}$$

Thus the prefilter satisfying equation (2-7) could have the following Fourier transform:

$$P(\omega)=0.5G(\omega-2\omega_N)+0.5G(\omega+2\omega_N) \quad \textbf{(2-8)}$$

The corresponding impulse response of the prefilter is:

$$p(t)=g(t)\cos(2\omega_N t) \quad \textbf{(2-9)}$$

Substituting equation (2-4) into (2-9) the required prefilter impulse response (see Figure 2—8) becomes:

$$p(t)=\frac{\sin(\pi t/T_{SYM})}{\pi t/T_{SYM}}\frac{\cos(\alpha\pi t/T_{SYM})}{1-4\alpha^2 t^2/T_{SYM}^2}\cos(2\pi t/T_{SYM}) \quad \textbf{(2-10)}$$

The output of the prefilter in time domain can be represented as the convolution of the receiver's matched filter output and the prefilter's impulse response, but as seen in Figure 2—7 the output of the prefilter has a DSB-SC shape, thus it can also be written in time domain as shown below.

$$z_{PFLT}(t)=z_{MF}(t)\bigstar p(t)=\Omega(t)\cos(\omega_N t+\theta)+v_{nPFLT}(t) \quad \textbf{(2-11)}$$

where:

$\Omega(t)$: is the equivalent amplitude modulating function

θ : is the symbol clock phase error

$v_{nPFLT}(t)$: is the noise component due to the input's AWGN

The function $\Omega(t)$ is a random variable, which depends on the random sequence $\{a_n\}$.

In [7] it was stated that the practical analog implementation of the ideal (in terms of the output spectrum symmetry) prefilter is difficult, since the actual symbol frequency might not be exactly the same as the nominal symbol frequency for which the prefilter was designed. These differences would distort the frequency spectrum symmetry requirement, and thus the output of the analog prefilter would have some undesirable ISI at the zero crossings, and zero jitter feature would not be achievable. In this thesis it is suggested that prefilter is designed as FIR filter inside the feedback loop, thus as the loop converges to the actual symbol frequency, the prefilter's output spectrum approaches the ideal symmetrical shape.

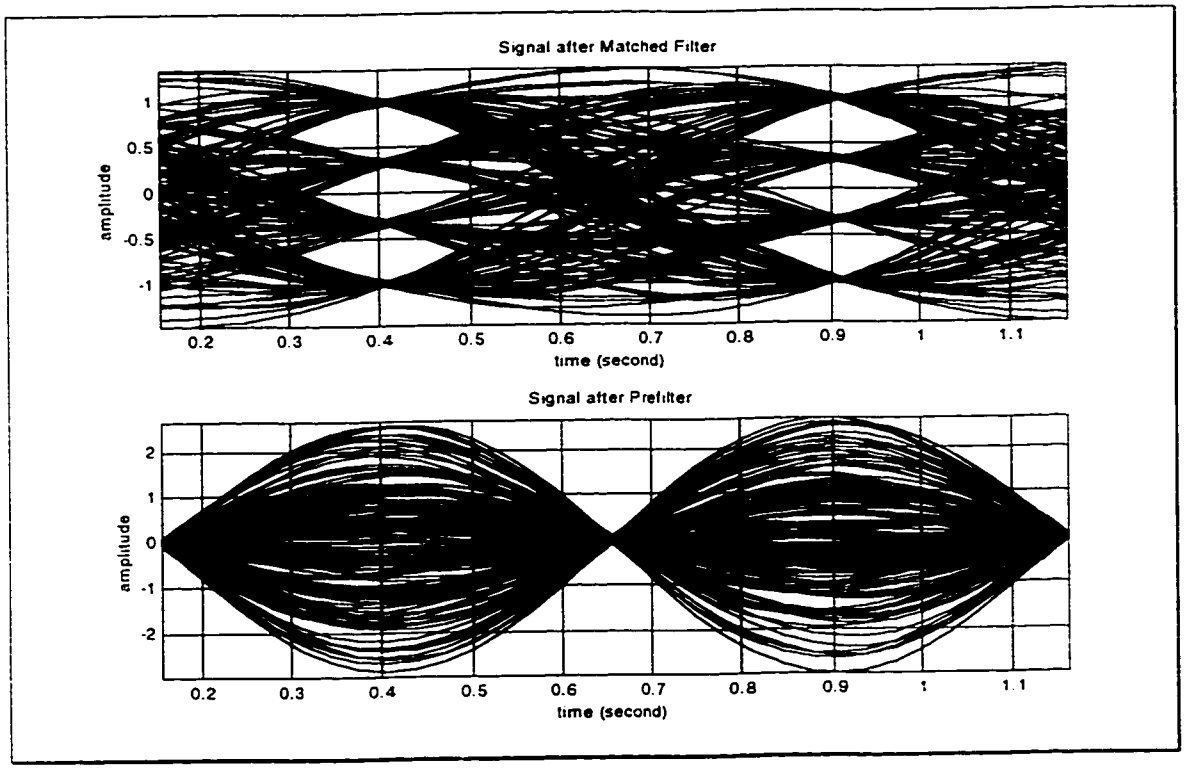

Figure 2—6. Eye Opening Before and After the Prefilter.

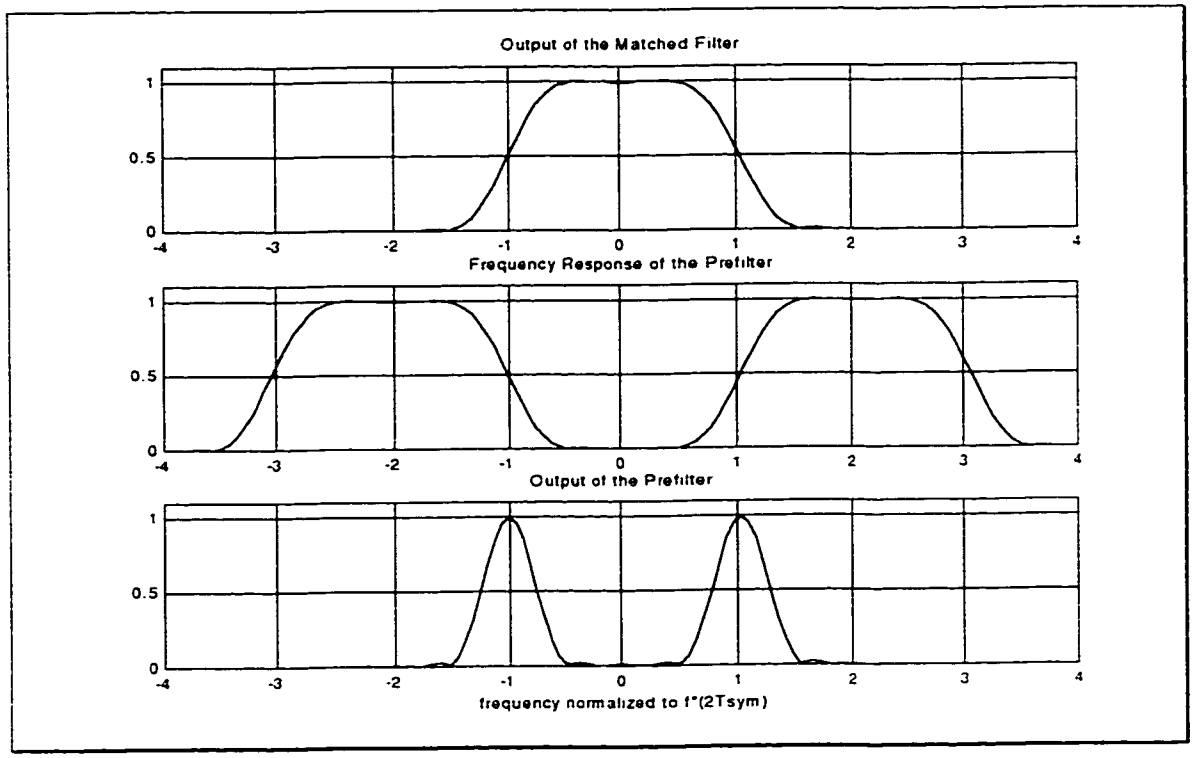

Figure 2—7. Frequency Spectrum Before and After Prefilter.

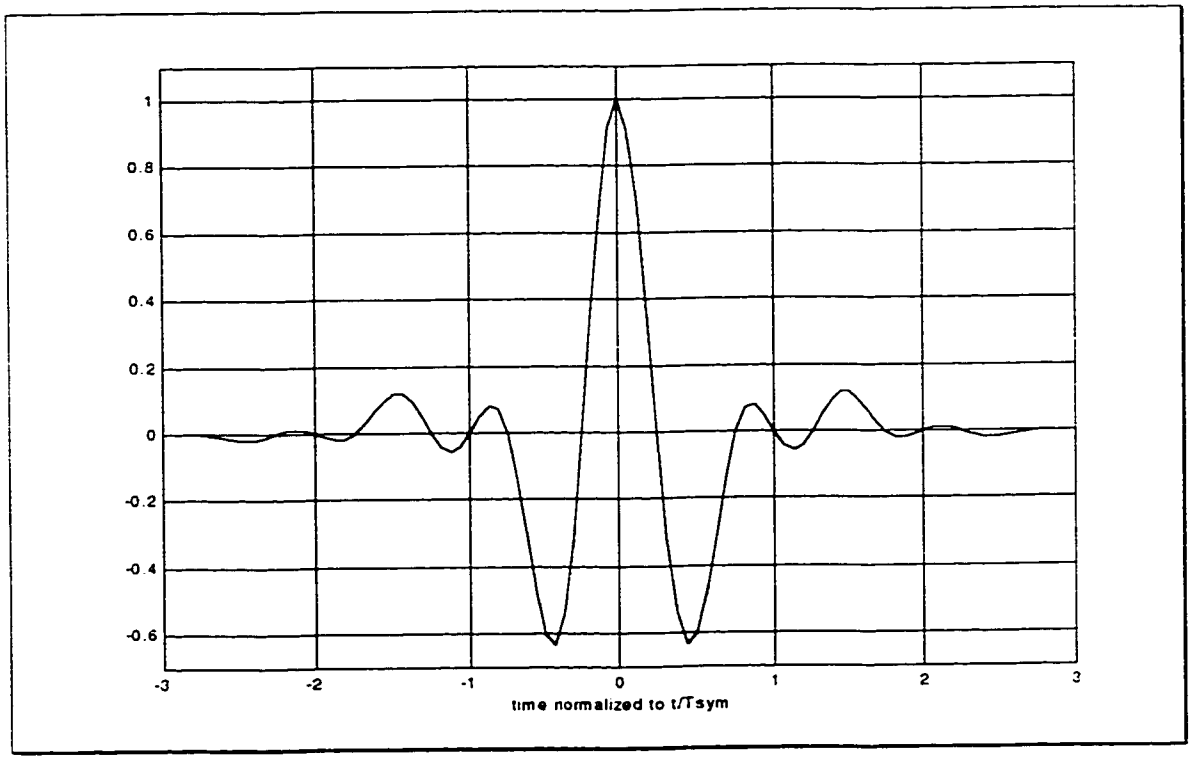

Figure 2—8. Impulse Response of the Prefilter.

Modified Digital Costas Loop

The typical analog Costas loop, as shown in Figure 2—2, produces the error signal u(t) which can be written as:

$$u(t) = \left\{ z_{PFLT}(t)\cos(\omega_N t) \right]_{LPF} \left[z_{PFLT}(t)\sin(\omega_N t) \right]_{LPF} \Big\}_{LPF} \quad \textbf{(2-12)}$$

Expanding $z_{PFLT}(t)$ term and neglecting the noise component due to AWGN, the above error signal function can be rewritten as:

$$u(t) = \left[-\frac{1}{8}\Omega^2(t)\sin(2\theta) + \frac{1}{4}\Omega^2(t)\sin(2\omega_N t) + \frac{1}{8}\Omega^2(t)\sin(4\omega_N t + 2\theta) \right]_{LPF} \quad \textbf{(2-13)}$$

and

$$u(t) = -\frac{1}{8}E\left[\Omega^2(t)\right]\sin(2\theta) \quad \textbf{(2-14)}$$

The expected value $E[\Omega^2(t)]$ could be derived, similarly as in [7], to be a constant value dependent on the number of symbol levels K of a K-PAM signal, and the loop bandwidth.

As seen in equation (2-14) the error signal controlling the instantaneous phase of the VCO is proportional to the phase difference between the received signal's symbol clock phase and the symbol clock phase of the receiver itself (for small θ).

When the error signal is zero, the VCO's output frequency is equal to its nominal value. When the error signal is positive (negative) the frequency is increased (decreased), thus progressively reducing the phase error of the receiver's symbol clock.

It can be noticed that the equation (2-12) could also be written as:

$$u(t) = \left[\frac{1}{2} z_{PFLT}^2(t) \sin(2\omega_N t)\right]_{LPF} \quad \text{(2-15)}$$

The new form of the error signal function produces the same result as equation (2-14), but reduces the practical implementation from 3 low pass filters (LPF), 3 multipliers and 90° phase shifter to only 1 LPF, 1 multiplier and a squarer. The squarer is an expensive function, from the hardware implementation point of view (both analog and digital), thus in this thesis it is proposed to replace it by an absolute value function. The absolute value function is a rough approximation of the squarer, but it is extremely efficient from the digital hardware resources point of view. Thus, the proposed modified digital Costas loop error signal function becomes:

$$u(t) = \left[\frac{1}{2} |z_{PFLT}(t)| \sin(2\omega_N t)\right]_{LPF} \quad \text{(2-16)}$$

In the following sub-sections the proposed feedback symbol synchronizer (based on prefilter equation (2-10) and the error signal equation (2-16)) is presented in a form of a general structure and the linearized equivalent model, in order to analyze its performance behavior in the next sections.

2.3.3. General Structure

The general structure of any discrete time error-tracking synchronizer, composed of timing error detector (TED), an averaging loop filter and a voltage controlled clock generator, is shown in Figure 2—9. Each of the blocks is described below.

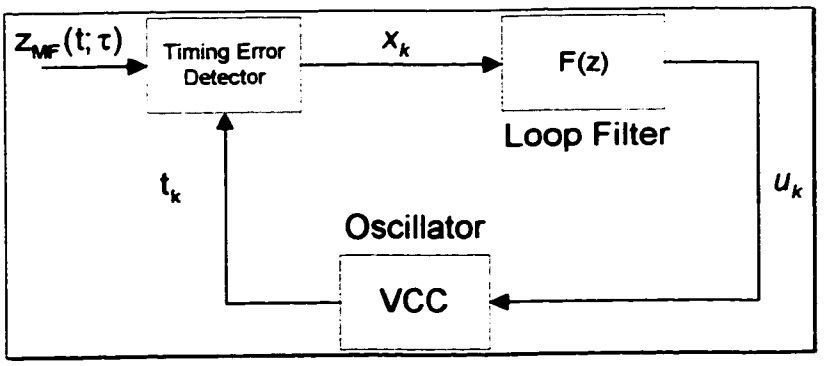

Figure 2—9. Discrete-Time Error-Tracking Synchronizer.

TED

The timing error detector performs sampling of the input signal z_{MF} at instants t_k (which are the estimates of $kT_{SA}+\tau T_{SYM}$), and based on these signal samples, it produces an error signal x_k, which corresponds to the instantaneous timing clock phase error e_k. For the modified digital Costas loop presented in Section 2.3.2, the TED output signal is expressed as:

$$x_k = \frac{1}{2}\left|z_{PFLT}(t_k)\right| \sin(2\omega_N(t_k)) \qquad \textbf{(2-17)}$$

where:

t_k : is a sampling instant equal to $kT_{SA} + \hat{\tau}_k T_{SYM}$

T_{SA} : is a sampling period equal to T_{SYM}/L (L is number of ADC samples per symbol)

z_{PFLT} : is defined in equation 2-11

Thus in terms of the ADC samples the TED expression to be implemented becomes:

$$x_k = \frac{1}{2}\left|z_{PFLT}[k]\right| \sin\left(\frac{2\pi k}{L} + 2\pi\hat{\tau}_k\right) \qquad \textbf{(2-18)}$$

For analytical derivation it is easier to use the squarer function instead of the absolute function, thus neglecting the high frequency components, and using equation (2-13), the signal x_k can be approximated by:

$$x_k \cong -\frac{1}{8}\Omega^2(t)\sin(2\theta) = C\sin(2\pi e_k) \qquad \textbf{(2-19)}$$

where:

$\theta = \pi e_k$: is the true symbol clock phase offset between receiver and transmitter

$e_k = \tau - \hat{\tau}_k$: is the timing error signal

C : is a constant corresponding to $-1/8\ E[\Omega^2(t)]$

Loop Filter

The averaging loop filter is a lowpass filter, which smoothes out the error signal and produces a control signal fed back to the VCC. One of the simplest filters, from digital implementation point of view, is a first order infinite impulse response (IIR) filter, which has the following z-domain representation:

$$F(z) = \frac{A}{1 - Bz^{-1}} \qquad \textbf{(2-20)}$$

The parameters A and B, in the above function, depend on the chosen -3 dB lowpass cutoff frequency, and can be determined as shown below:

$$B = 2 - \cos(\omega_{3dB}T_{SA}) \pm \sqrt{\cos^2(\omega_{3dB}T_{SA}) - 4\cos(\omega_{3dB}T_{SA}) + 3} \qquad \textbf{(2-21)}$$

$$A = 1 - B \qquad \textbf{(2-22)}$$

A discrete time representation of this IIR low pass filter is written as:

$$u_k = Ax_k + Bu_{k-1} \tag{2-23}$$

The cutoff frequency of the loop filter should be less than $2\omega_N$, to remove the high frequency components shown in equation (2-13), and further narrowing of the passband should be used to average the random value of $\Omega^2(t)$ shown in equation (2-19).

$$\omega_{3dB} < 2\omega_N \text{ thus assume } \omega_{3dB} = \frac{\omega_N}{2} \tag{2-24}$$

In the later sub-sections, it is also shown, that for a stable feedback system, the value of sqrt(B) should be less than or equal to 1.

VCC

The voltage controlled clock generates sampling instants, and the positive clock edge, for the digital part of the system, at time t_k according to:

$$t_{k-1} = t_k + T_{SA} + K_o T_{SYM} u_k \tag{2-25}$$

When u_k is zero, the interval between sampling instants is constant and equal to T_{SA}; thus $1/T_{SA}$ is the nominal frequency of VCC.

The sampling instant t_k can also be represented as a function of the timing error:

$$t_k = kT_{SA} + \hat{\tau}_k T_{SYM} \tag{2-26}$$

The estimated timing error $\hat{\tau}_k$ can be represented as a function of u_k:

$$\hat{\tau}_k = \hat{\tau}_{k-1} + K_o u_{k-1} \tag{2-27}$$

Thus the transfer function of the VCC in z-domain can be derived as:

$$VCC(z) = \frac{K_0 z^{-1}}{1 - z^{-1}} = \frac{K_o}{z - 1} \tag{2-28}$$

where:

K_0 : is the gain of the VCC

2.3.4. Equivalent Model

The error tracking synchronizer, shown in Figure 2—9, is often represented by the equivalent model (see Figure 2—10) [8, Chapter 2.3], based on which all error tracking synchronizers can be fairly compared with each other.

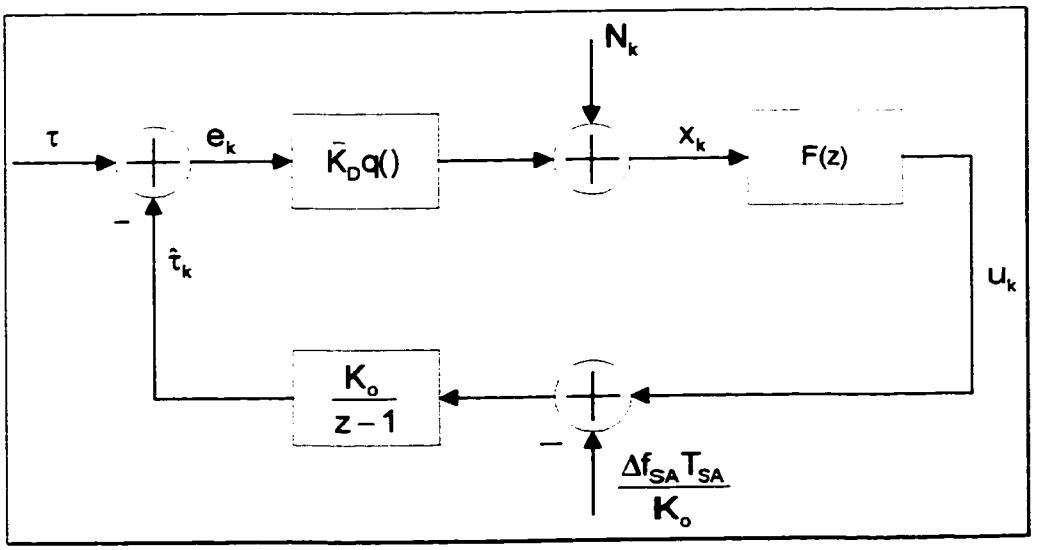

Figure 2—10. Equivalent Model of Discrete-Time Error-Tracking Synchronizer.

In the equivalent model, the timing error detector output signal, x_k, is replaced by the sum:

$$x_k = K_D q(e_k) + N_k \tag{2-29}$$

where:

$q(e_k)$: is timing error detector characteristic, periodic in error signal e with period 1

e_k : is the error between the estimated and true symbol timing offset

K_D : is the timing error detector gain determined such that q'(0)=1 [8, Chapter 2.3]

N_k : is the loop noise, which represents statistical fluctuations of TED output signal.

The statistical fluctuations of TED output signal are caused by the additive noise n(t), and the random nature of the channel symbols $\{a_n\}$, in the input signal [8, Chapter 2.3]. The equivalent $K_D q(e_k)$ term can be found by assuming the loop noise term N_k is zero, which means that the additive noise n(t) is zero and the channel symbols sequence $\{a_n\}$ is deterministic (for example alternating 1 and -1). The x_k signal, under such conditions, can be determined from equation (2-19) as:

$$K_D q(e_k) \cong C \sin(2\pi e_k) \tag{2-30}$$

where:

Constant C=0.2578 can be found from simulations shown in Figure 2—11.

Since the timing error detector gain K_D is determined such that q'(0)=1, thus:

$$K_D \cong 2\pi C \tag{2-31}$$

and,

$$q(e_k) \cong \frac{1}{2\pi} \sin(2\pi e_k) \tag{2-32}$$

The shape of the timing error detector characteristic is often used to compare the acquisition behavior of different phase lock loop (PLL) circuits, as will be explained Section 2.8.

The VCC is replaced by its z-domain frequency response, $K_o/(z-1)$, with gain K_o, and by the normalized frequency detuning factor $\Delta f_{SA} T_{SA}/K_o$.

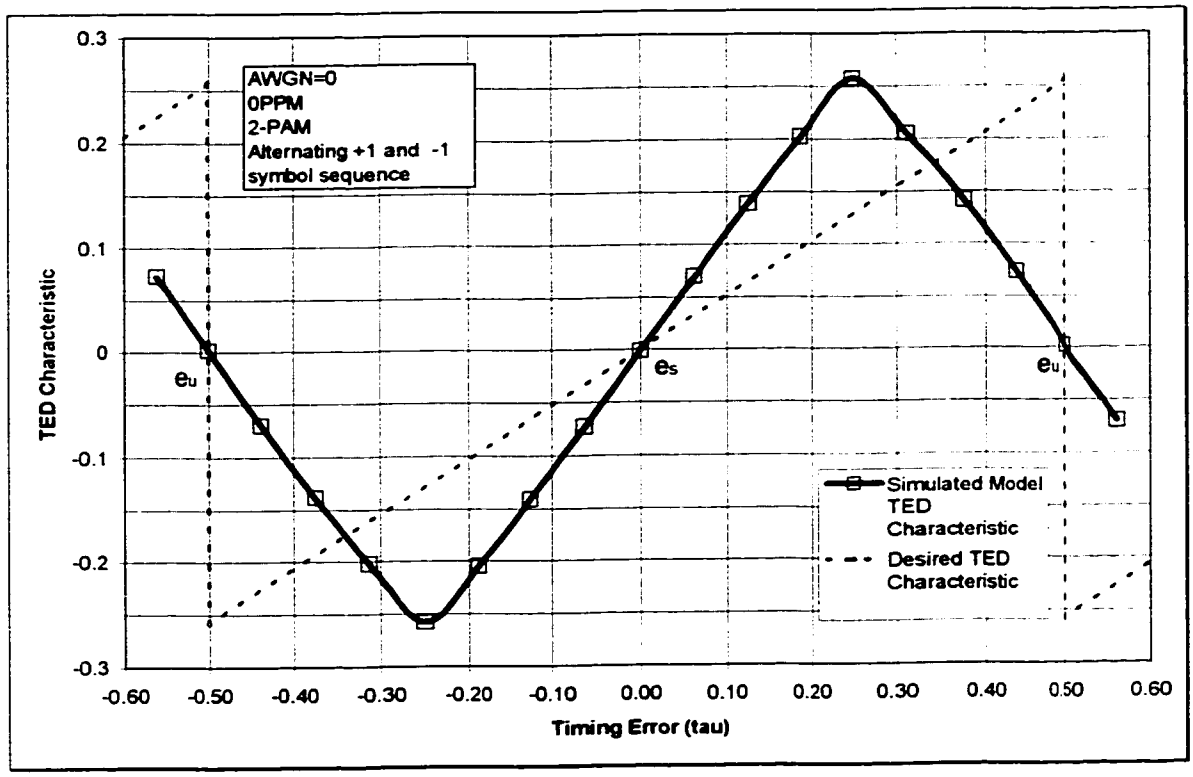

Figure 2—11. Simulated Timing Error Detector Characteristic.

2.3.5. Linearized Equivalent Model

The error timing detector characteristic is usually nonlinear, which is the case for the investigated TED, and the analysis of the synchronizer is difficult. In order to simplify the analysis, often a linearized equivalent model is used (see Figure 2—12). The linearization involves approximating timing error detector characteristic q(e), and power spectral density of the loop noise $S_N(\omega,e)$, at the stable equilibrium point e_S, [8, Chapter 2.3]:

$$q(e_k) \cong q(e_S) + (e_k - e_S)q'(e_S) \cong (e_k - e_S)q'(e_S) \qquad \textbf{(2-33)}$$

$$S_N(\omega;e_k) \cong S_N(\omega;e_S) \tag{2-34}$$

where:

$q'(e_S)$: is the TED slope at the stable equilibrium point for a small steady-state error e_S

e_S : is the small steady-state error for zero loop noise, corresponding to a positive zero crossing of $q(e)- \Delta f_{SA}T_{SA} /(K_oK_DF(1))$

$q(e_S)$: is approximately equal to $q(0)=0$, since e_S is assumed to be small

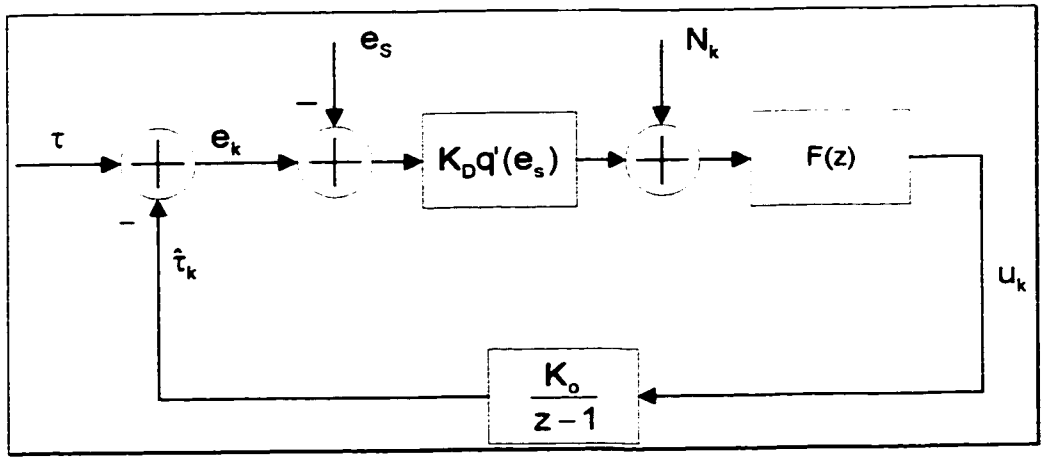

Figure 2—12. Linearized Equivalent Model.

The closed–loop frequency response H(z), in z-domain, of the timing error tracker can be derived as:

$$H(z) = \frac{K_oK_Dq'(e_S)F(z)}{z-1+K_oK_Dq'(e_S)F(z)} \tag{2-35}$$

Expanding the first order loop filter F(z), the closed loop frequency response becomes:

$$H(z) = \frac{DAz}{z^2-(B+1-DA)z+B} \tag{2-36}$$

where:

H(z) : represents 2-nd order lowpass filter, with unity gain at DC

1-H(z) : represents a highpass filter

$DA=K_0K_Dq'(e_S)A$: is called an open loop gain constant

A and B : are the loop filter parameters

It is known, that for a stable system, the poles of the transfer function H(z) have to lie inside the unit circle [15], thus:

$$\left|\frac{B+1-DA}{2} \pm \frac{1}{2}\sqrt{(B+1-DA)^2-4B}\right| \le 1 \qquad \textbf{(2-37)}$$

$$\therefore \text{for } (B+1-DA)^2 < 4B \quad \sqrt{B} \le 1 \qquad \textbf{(2-38)}$$

Using the closed–loop frequency response H(z), and the linearized equivalent model, the effect of input parameters on the error signal can be analyzed as shown in Figure 2—13.

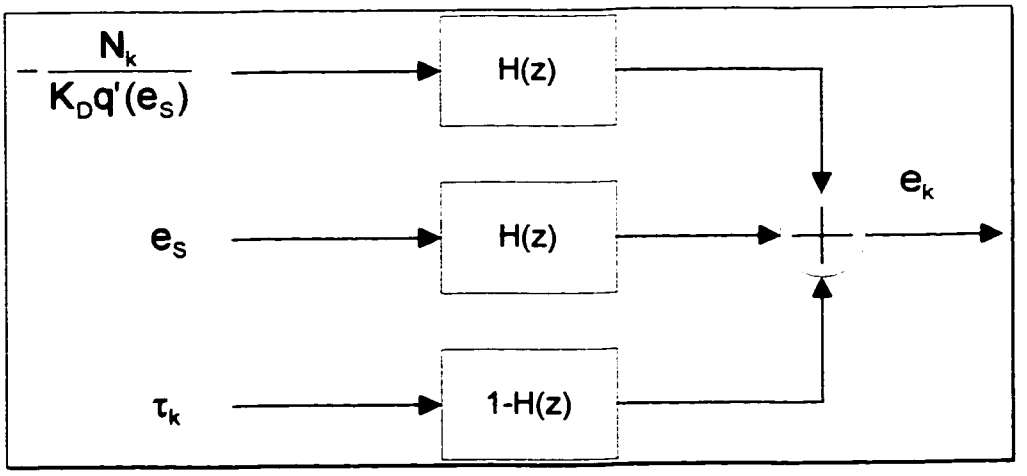

Figure 2—13. Contributions to Timing Error Variations.

The true timing position τ_k of the received signal, is usually slowly varying, and as shown in Figure 2—13, it will not have a significant effect on the timing error variations, due to the

highpass filter function. Any frequency detuning will be reflected in the timing error e_k, by an offset e_S from the ideal position. Since the changes in Δf_{SA}, during the transmission, are usually slow, and are further lowpass filtered by H(z), they also will not have major effect on the timing error variations. However, the factor significantly contributing to the linarized timing error variations is the equivalent loop noise N_k, which depends on the input AWGN and the randomness of the sequence $\{a_n\}$.

One of the important parameters, in the analysis of the error tracking synchronizers, is the one-sided loop bandwidth B_L (in hertz),which is defined for sampled process as [8, Chapter 2.3]:

$$B_L = \int_0^{\pi/T_{SA}} \left|H(e^{j\omega T_{SA}})\right|^2 \frac{d\omega}{2\pi} \tag{2-39}$$

A small loop bandwidth reduces the effect of loop noise on timing error variance, as will be shown in Section 2.5, however, it also reduces the pull-in frequency range, and increases the acquisition time as will be shown in Sections 2.6 and 2.8, respectively. The loop bandwidth can be controlled by the open loop gain DA, and in this thesis, this value was chosen on "trial and error" bases, to obtain the timing error variance corresponding to BER degradation of 0.1 dB, in presence of practical frequency detuning value of 100 PPM.

The following sections present the performance of the proposed structure for the DSP-based Costas loop timing synchronizer, based on the MATLAB simulation results obtained for different input parameters.

2.4. The Mean of Symbol Timing Error

In this section it will be shown that the mean of the symbol timing error is dependent on symbol clock frequency detuning (due to limited long term frequency stability of the oscillators) between the transmitter's and receiver's symbol clocks. The maximum symbol clock frequency detuning, resulting in negligible mean of symbol timing will be determined by simulation.

As the mean of the symbol timing error increases, the obtained symbol timing instant is further away from true maximum eye opening position, and thus can result in severe bit error rate degradation. Ideally the mean of symbol timing error should be zero, and then the symbol timing estimator (or synchronizer) would be called unbiased.

The steady state (or mean) of the timing error can be determined based on the z-transform theory stating that:

$$e_{ss} = \lim_{t\to\infty} e(t) = \lim_{z\to 1}(z-1)e(z) \qquad (2\text{-}40)$$

where:

$$e(z) = \tau(z) - \hat{\tau}(z) = \tau(z)[1 - H(z)]$$

Assuming that the true timing position changes during the transmission (due to symbol clock frequency detuning), and there is no equivalent loop noise N(t)=0, then the true timing position in time domain is represented as:

$$\tau(t) = 2\pi\Delta f_{SYM} T_{SYM} t + \tau_o \qquad (2\text{-}41)$$

where:

$\Delta f_{SYM} T_{SYM} = \Delta f_{SA} T_{SA}$: is the normalized symbol clock frequency error

τ_0 : is the initial symbol timing error

The true timing position in z-domain is:

$$\tau(z) = \frac{2\pi\Delta f_{SYM} T_{SYM}}{(z-1)^2} + \frac{\tau_o}{z-1} \qquad \textbf{(2-42)}$$

Using the transfer function H(z) for the modified digital Costas loop, and solving equation (2-40), the steady state (or mean) of the timing error is:

$$e_{ss} = e_s = \lim_{t\to\infty} e(t) \cong \frac{2\pi\Delta f_{SYM} T_{SYM}}{D} \quad \text{for small } e_s \qquad \textbf{(2-43)}$$

From equation (2-43) it can be noticed that the steady state timing error is proportional to the amount of frequency detuning and inversely proportional the open loop gain $D=K_0K_Dq'(e_S\approx 0)$. In order to reduce the steady state timing error due to frequency detuning, either the clock generator at the transmitter needs to be more stable, or at the receiver STR, the open loop gain should be increased, however, a larger open loop gain will result in a larger timing error variance (as shown in Section 2.5 equation 2-52, where loop bandwidth B_L is proportional to open loop gain, eq.2-36 and eq.2-39), thus usually a compromise will have to be made for optimum performance. The derivation of equation (2-43) did not consider the equivalent loop noise (to simplify derivation), but assuming that the noise component is zero mean (valid assumption, since as will be discussed in later sections, the equivalent loop noise depends on the data pattern sequence, and for uncoded but scrambled data transmission, data symbols are equiprobable and thus zero mean), it should not have significant effect on the steady state timing error value. The mean of timing error simulations, presented in Figure 2—14, Figure 2—15 (note: the almost flat curves indicate negligible effect of thermal noise on the mean timing error) and Figure 2—16, confirm the above dependence theory, and show that for the chosen parameters of loop bandwidth B_LT_{SA}=2.3E-4 (or 5.8E-5), which corresponds to D=-0.0913 (or D=-0.046), and for frequency detuning less than or equal to 100 PPM, the mean of timing error is below 0.5% of T_{SYM}. This mean timing error

value is very low, thus the synchronizer can be assumed unbiased, for frequency detuning less than or equal to 100 PPM. It is assumed that symbol timing at the transmitter is derived from the fixed clock oscillator, which has practical frequency accuracy of +/- 10 PPM. The unbiased symbol synchronizer property is very desirable, since it guaranties that for a large number of observations the recovered timing is close to the ideal symbol timing. As shown in Figure 2—16, the mean of timing error increases as the number of modulation levels K increase, however, for K>2 this effect is not significant.

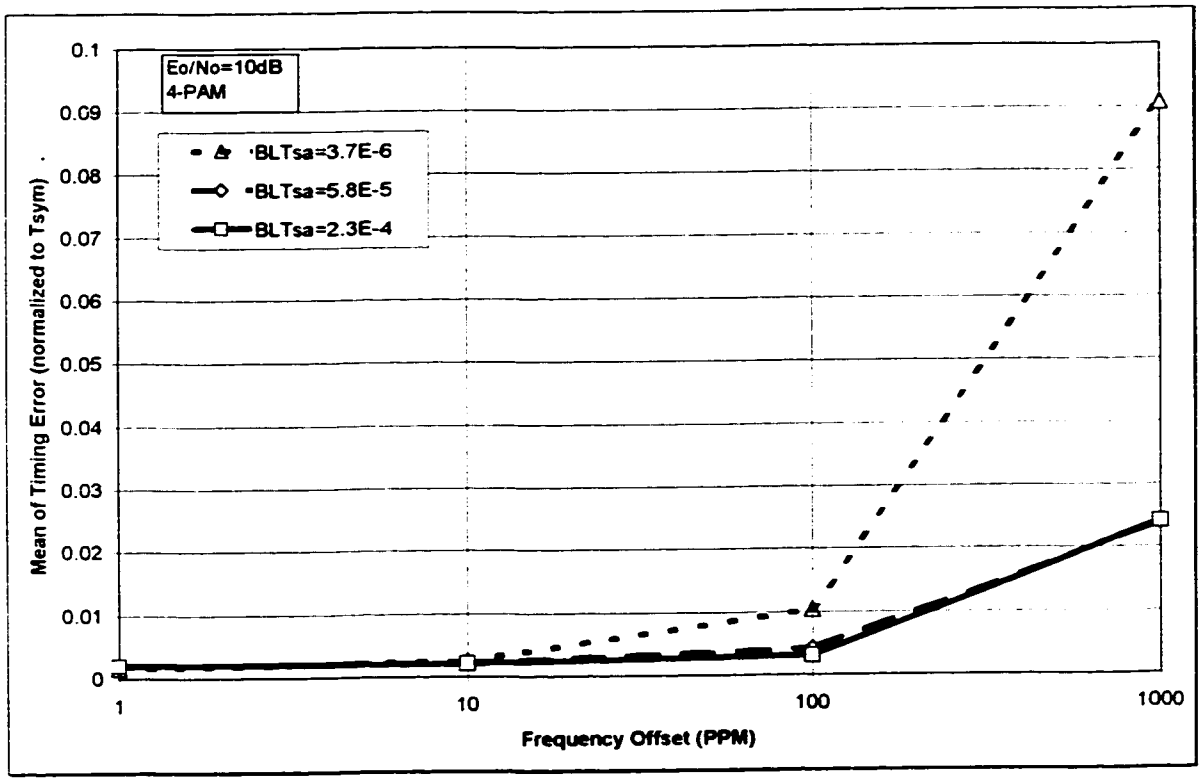

Figure 2—14. Mean of Timing Error versus Frequency Detuning.

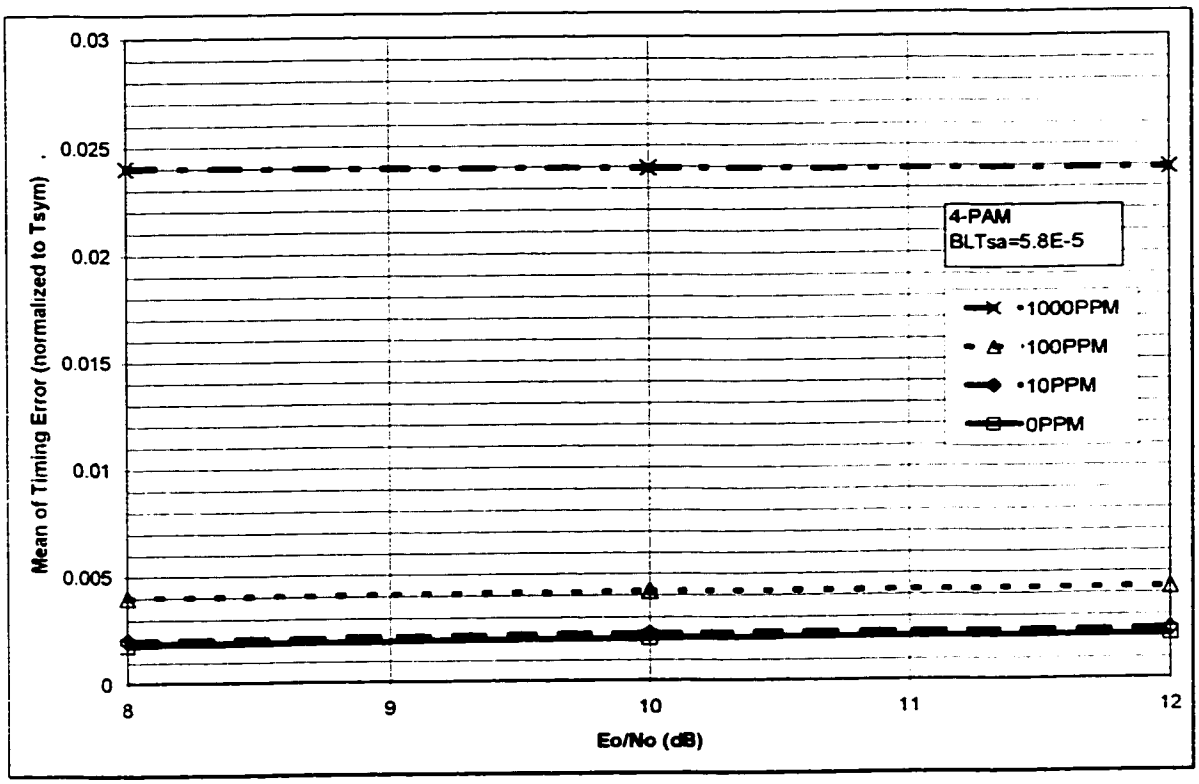

Figure 2—15. Mean of Timing Error versus AWGN Input.

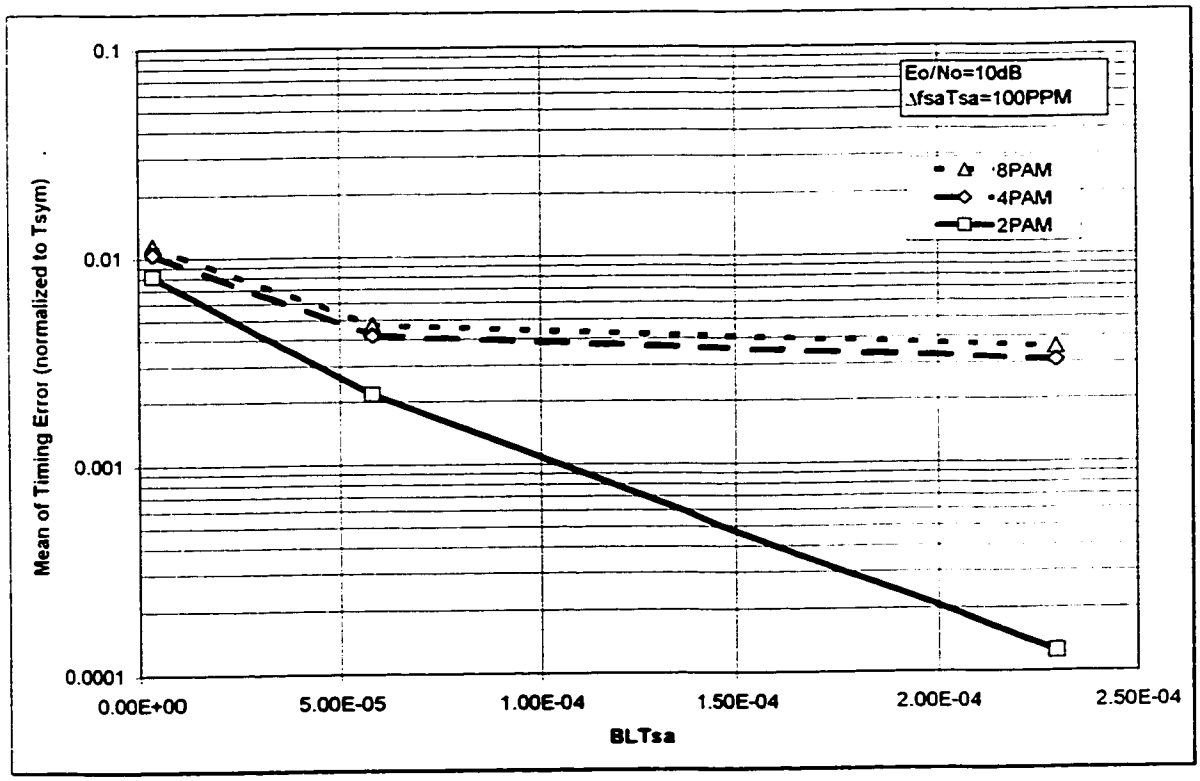

Figure 2—16. Mean of Timing Error versus Loop Bandwidth.

2.5. Variance of Symbol Timing Error

In this section, the timing error variance of the DSP-based Costas loop symbol synchronizer will be evaluated by computer simulations for different parameters of loop bandwidth, frequency detuning and AWGN. It will be shown that by selecting proper design parameters, the variance of timing error can be made acceptably small.

In the previous section it has been shown that on average the recovered symbol timing (symbol sampling position) is equal or very close to the actual optimum value (i.e. on average the timing error is zero), however, on per symbol basis this recovered symbol sampling position, most of the time, is different from the actual optimum value. That is, the timing error fluctuates around the stable equilibrium point e_S (where e_S is close to zero). Obviously, it is desirable to have these fluctuations as small as possible, in order to have minimum BER degradation. The performance measure of these variations about the actual exact optimum value is called the variance of the timing error (which is usually preferred in theoretical or simulation analysis) or jitter and phase noise of the recovered symbol clock (which are usually preferred in practical, time or frequency domain, measurements, respectively). Each, the variance, the jitter or the phase noise results can be used to roughly estimate the expected bit error rate degradation. However, in this chapter only simulation results are available, thus in Section 2.7 the bit error rate degradation is estimated based on the variance results. More on the jitter and the phase noise practical measurements will be discussed in Chapter 3.

2.5.1. Derivation of the Variance

In the following sub-section the derivation of the timing error variance, and its relation to the loop bandwidth and loop noise, is presented for the case of the linearized synchronizer model. The variance of symbol timing error is defined as:

$$\sigma_e^2 = E[e_k^2] - E[e_k]^2 \qquad (2\text{-}44)$$

From autocorrelation properties, it is known that:

$$E[e_k^2] = R_e(l \to 0)$$
$$E[e_k]^2 = R_e(l \to \infty) \tag{2-45}$$

where:

$R_e(l)$: is the autocorrelation of e_k

From Wiener–Khinchin theorem, for discrete-time stationary random process in frequency domain, the autocorrelation process can be represented as [16, Chapter 10]:

$$R_e(l) = \frac{T_{SA}}{2\pi} \int_{-\frac{\pi}{T_{SA}}}^{\frac{\pi}{T_{SA}}} S_e\left(e^{j\omega T_{SA}}\right) e^{j\omega l} d\omega \tag{2-46}$$

Based on Figure 2—13, with the assumption that true timing position τ is constant or slowly varying during the transmission, and the offset e_S is zero, the expression for timing error, in z-domain, can be obtained as:

$$e(z) = -\frac{H(z)}{K_D q'(e_S)} N(z) \tag{2-47}$$

Since H(z) is a linear system, the power spectral density at the output of H(z) can be represented in terms of the power spectral density (psd) at the input of H(z) as [16, Chapter 10]:

$$S_e\left(e^{j\omega T_{SA}}\right) = S_N\left(e^{j\omega T_{SA}}; e_S\right) \left| \frac{H\left(e^{j\omega T_{SA}}\right)}{K_D q'(e_S)} \right|^2 \tag{2-48}$$

where:

$S_N\left(e^{j\omega T_{SA}};e_S\right)$: is a psd of the equivalent loop noise, dependent on e_S

Substituting equation (2-48) into equation (2-46), the obtained autocorrelation function is:

$$R_e(l)=\frac{T_{SA}}{2\pi\left[K_D q'(e_S)\right]^2}\int_{-\frac{\pi}{T_{SA}}}^{\frac{\pi}{T_{SA}}} S_N\left(e^{j\omega T_{SA}};e_S\right)\left|H\left(e^{j\omega T_{SA}}\right)\right|^2 e^{j\omega l}d\omega \qquad (2\text{-}49)$$

As shown in Section 2.4, it can be assumed that the feedback symbol timing synchronizer is unbiased (for the practical range of symbol clock frequency detuning), thus:

$$E[e_k]^2=R_e(l\to\infty)=0 \qquad (2\text{-}50)$$

and the variance of symbol timing error is:

$$\sigma_e^2=R_e(0)=\frac{T_{SA}}{2\pi\left[K_D q'(e_S)\right]^2}\int_{-\frac{\pi}{T_{SA}}}^{\frac{\pi}{T_{SA}}} S_N\left(e^{j\omega T_{SA}};e_S\right)\left|H\left(e^{j\omega T_{SA}}\right)\right|^2 d\omega \qquad (2\text{-}51)$$

It has been shown in [8, Chapter 2.3] that for small loop bandwidth B_L the loop noise power spectral density is well approximated by its value at $\omega=0$, thus the final approximated symbol timing error variance can be obtained from:

$$\sigma_e^2=\frac{T_{SA}S_N(\omega=0;e_S)}{2\pi\left[K_D q'(e_S)\right]^2}\int_{-\frac{\pi}{T_{SA}}}^{\frac{\pi}{T_{SA}}}\left|H\left(e^{j\omega T_{SA}}\right)\right|^2 d\omega=2B_L T_{SA}\frac{S_N(\omega=0;e_S)}{2\pi\left[K_D q'(e_S)\right]^2} \qquad (2\text{-}52)$$

As shown in the above equation, the timing error variance, at steady state, is directly proportional to the loop bandwidth and the equivalent noise term.

The analytical derivation of the equivalent noise and its power spectrum density function is usually difficult, thus in this chapter only the simulation results are presented. In some practical cases the term $S_N(0)/(K_D q'(e_S))^2$ could be replaced by the variance of the uncorrelated zero mean noise at the input of the digital PLL (DPLL) [17]. However, such over-simplification, for this investigated DPLL, gives unacceptable results which are well below the simulated variance curve.

2.5.2. Variance Simulation Results

For the first set of variance simulations, the open loop gain D (which is proportional to the loop bandwidth) was chosen on a "trial and error" basis until the variance of a particular simulation model (2, 4 or 8-PAM) was within limits for 0.1 dB degradation, see Section 2.7. A default frequency detuning was assumed to have a magnitude of 100 PPM, which covers a practical range of possible deviations between the receiver's and transmitter's symbol clock oscillators (assuming fixed symbol clock oscillator at the transmitter). The simulated variance results, as a function of the input AWGN, are shown in Figure 2—17. As predicated by equation (2-52) the variance decreases as the signal to noise ratio increases. In Section 2.7 it is shown that for the considered E_0/N_0 signal to noise ratio sweep, corresponding to bit error rates down to 10^{-3}, the variance is within limits for 0.1 dB equivalent BER degradation. For convenience of comparison with practical measurements (for example from [7]), the variance results from Figure 2—17 were translated to peak-to-peak jitter results shown in Figure 2—18. The translation relationship between the variance and the jitter has been defined as:

$$J_{pk-pk}(\%\ \text{of}\ T_{SYM}) = 2\sigma_e \qquad \textbf{(2-53)}$$

From Figure 2—18 it can be noticed that, as the number of PAM levels increases the jitter value has to be smaller in order to maintain the same BER. Note, the parameters of the loop, for each M-PAM curve shown in the figure, have been selected such that the resulting jitter does not

degrade the performance by more than 0.1 dB. For 8-PAM system with a tolerance of 0.1 dB degradation, the jitter has to be less then or equal to 2%, however, for 2-PAM system a jitter of 7% is low enough to meet this tolerance requirement. The system should generally not be over-designed for lower than required BER degradation, since, as shown in Section 2.8, the reduction of $B_L T_{SA}$ compromises the acquisition time.

Another sets of simulations, Figure 2—19 and Figure 2—20, were performed to investigate the effect of different open loop gains D (or the equivalent loop bandwidth $B_L T_{SA}$) and the symbol frequency detuning on the timing error variance. From Figure 2—19 it is observed that the timing error variance increases as the loop bandwidth (or the equivalent open loop gain D) increases, this behavior agrees with equation (2-52). As shown in Figure 2—20, the timing error variance is practically independent of frequency detuning for up to 100 PPM, for larger frequency detuning the variance results were inconsistent (probably due to more significant biasing effect).

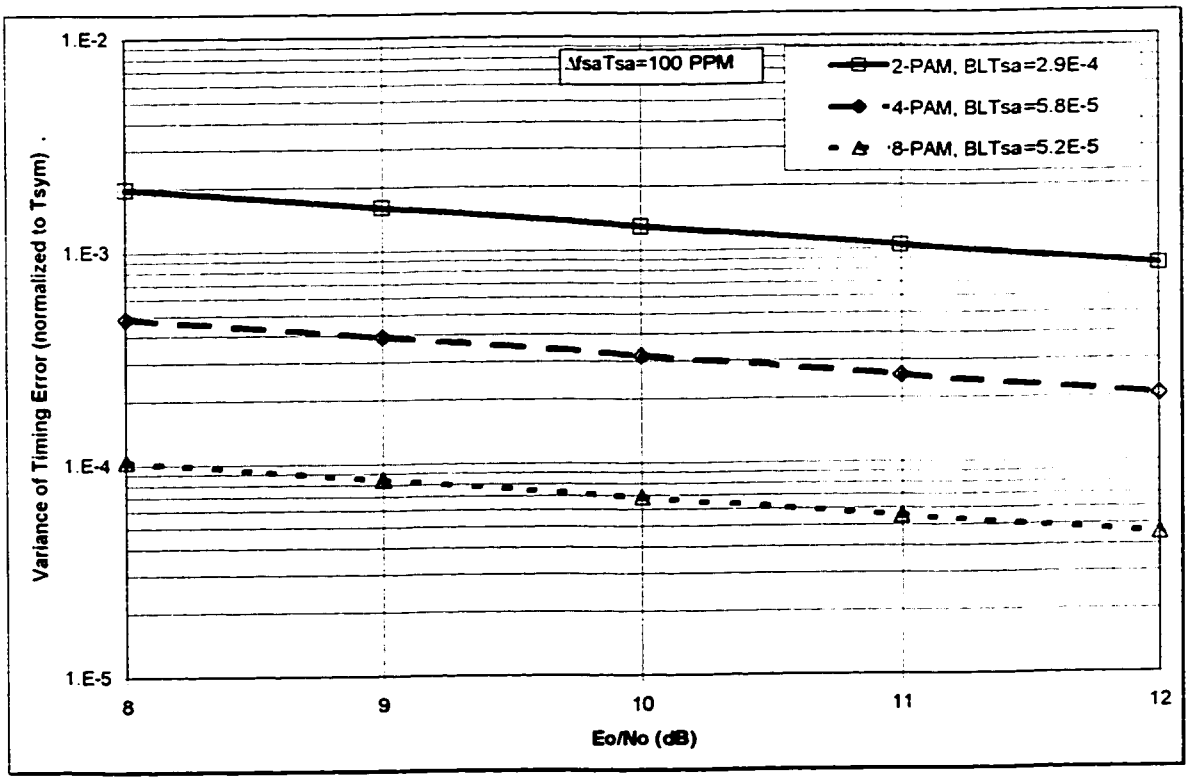

Figure 2—17. Variance of Timing Error versus AWGN Input.

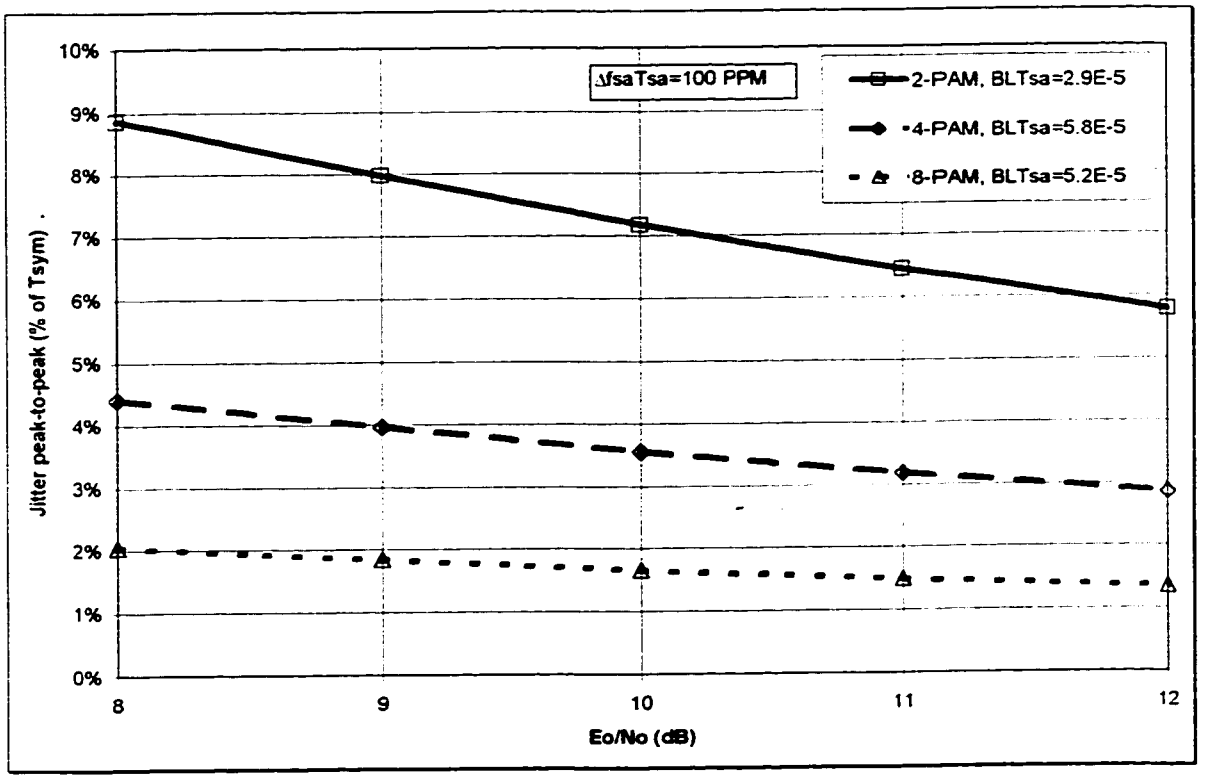

Figure 2—18. Jitter of Timing Error versus AWGN Input.

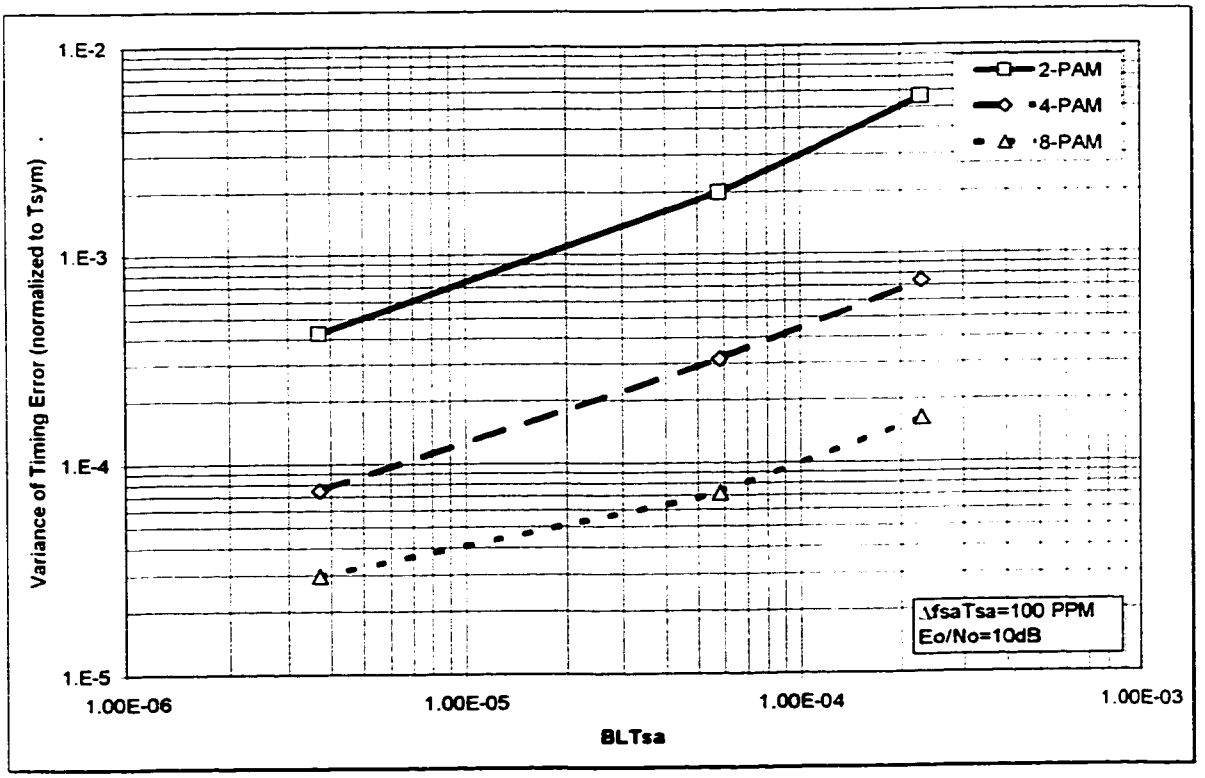

Figure 2—19. Variance of Timing Error versus Loop Bandwidth.

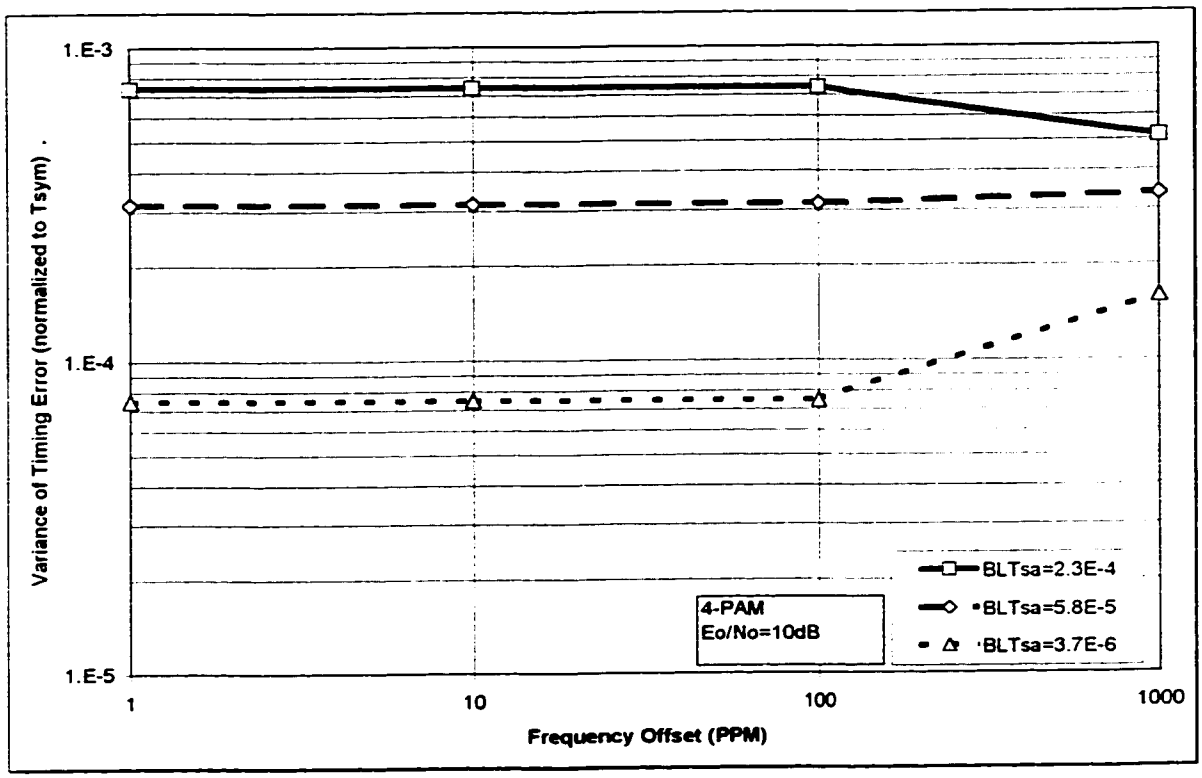

Figure 2—20. Variance of Timing Error versus Frequency Detuning.

2.6. The Pull-in Frequency Range

In this section, the pull-in frequency range, of the DSP-based Costas loop symbol synchronizer, will be determined by computer simulations.

The range of frequency detuning, over which a given synchronizer is able to lock-in, that is: adjust its local symbol clock from a nominal center frequency to the transmitter's symbol clock frequency, is called "pull-in" frequency range. When the symbol clock frequency detuning is larger than the pull-in range, the synchronizer will never achieve synchronization, and the so called cycle slipping will occur continuously.

The range of frequency detuning, over which a given synchronizer is able to maintain lock, is called "hold-in" frequency range. The hold-in range is usually larger than the pull-in range of a

given feedback synchronizer. Due to time varying frequency detuning, the hold-in frequency range is more difficult to simulate, thus only pull-in range is investigated in this thesis, and the worst case for "hold-in" range is assumed ("hold-in"="pull-in" range). Note, the transmitter oscillator's, slowly varying, long term, frequency deviation should be lower than the "hold-in" range of the receiver, in order for the receiver to stay synchronized to the incoming symbols.

The pull-in range of the feedback synchronizer is proportional to its loop bandwidth [8, Chapter 6.5]. The simulation results support that theory, since as shown in Figure 2—21, increasing loop bandwidth increased the lock-in range. Generally it is desirable to have large "pull-in" frequency range, unfortunately this desire is in conflict with the requirement for the small timing error variations, as shown in Section 2.5. However, in the case of symbol synchronization, the clock frequency is usually known quite accurately [8, Chapter 6.5] (assuming the transmitter is using fixed oscillators with +/- 10 PPM accuracy).

Although, the proposed symbol synchronizer is able to lock-in up to the frequency detuning values indicated in Figure 2—21, the steady state error is relatively high at values greater than 100 PPM, as shown in Section 2.4. Thus a maximum allowed frequency detuning should be on the order of 100 PPM or lower, which can be practically satisfied.

In comparison to the analog implementation from [7], which has the pull-in frequency range of approximately 30,000 PPM for 2 PAM signal, the digital implementation has much smaller pull-in range, but as just mentioned above such large pull-in range might not be always required in digital implementation.

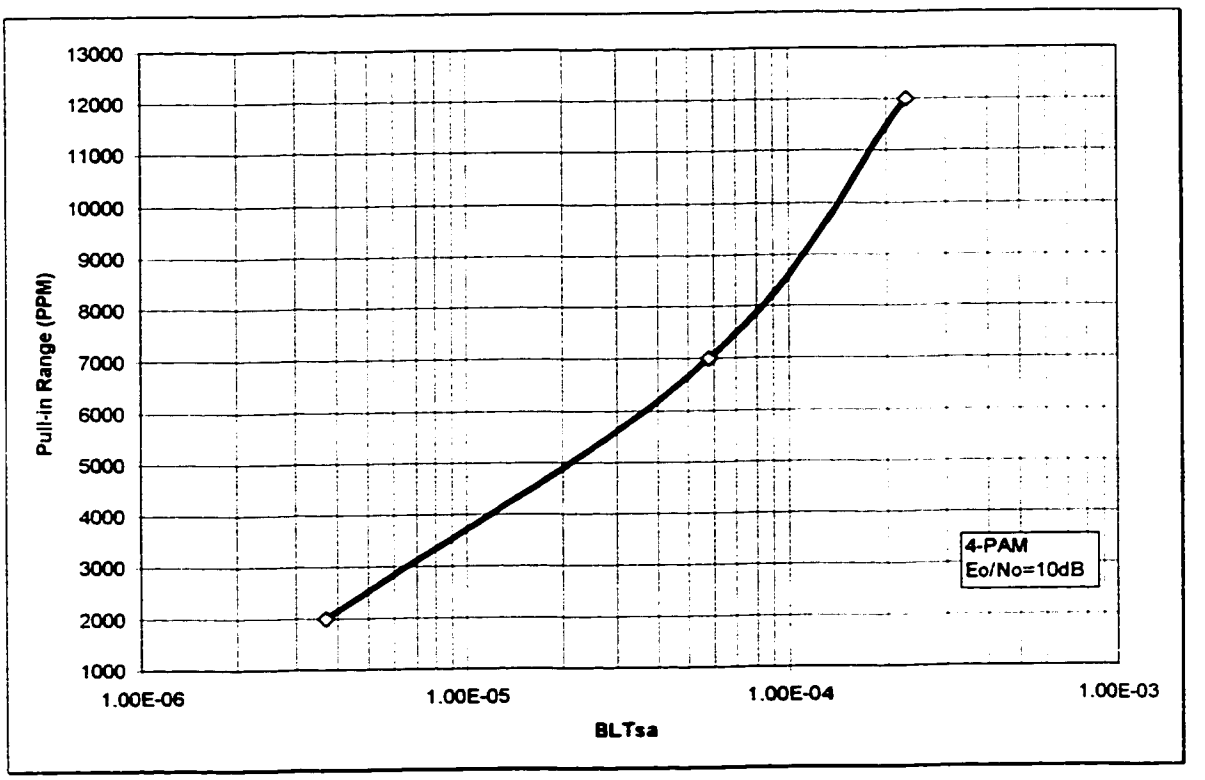

Figure 2—21. Pull-in Range versus Loop Bandwidth.

2.7. Effects of STR Quality on Channel Bit Error Rate Performance

In this section, using an expression for the bit error rate (BER) degradation (caused by symbol synchronization errors), it will be shown that the effect of the DSP-based Costas loop low jitter timing recovery on channel bit error rate performance is within the recommended range for good symbol synchronizers. The BER degradation is defined as the increase of signal to noise ratio E_b/N_o, required to maintain the same BER as the receiver without synchronization errors [8, Chapter 7.3].

The BER performance for variety of modulation schemes, with assumption of perfect synchronization, has been widely documented [3], [12]. For the case of K-PAM system, the perfect synchronization BER performance is defined as [3], [12]:

$$BER_o \cong \frac{2(1-1/K)Q\left\{\sqrt{2E_o/N_o}\right\}}{\log_2 K} \qquad \textbf{(2-54)}$$

where:

E_o : is the energy of the symbol with the lowest amplitude

$Q()$: is the Q-function

The approximate expression for BER degradation, as a function of the synchronization parameter variance, have been derived in [8, Chapter 7] for K-PAM, K^2-QAM linear modulation formats under the following assumptions:

- the signal constellation was designed using Gray-encoding,
- the signal to noise ratio is moderate, such that most of the symbol errors at the receiver are nearest neighbor symbol errors, which give rise to only one bit error per each symbol error (in practice, for operation with low bit error rates, this is often the case),
- the carrier phase and frequency synchronization is perfect (the effects of CR imperfections are accounted for by a separate expression which is added to equ. 2-54 [2]),
- and the variance of the synchronization parameter is much smaller than 1 (for approximation to be very accurate).

In a practical situation, the perfect synchronization of the carrier phase cannot be always assumed. In that case the total BER degradation equals the sum of BER degradation caused by phase, and timing errors individually [8, Chapter 7].

Here we present BER degradation (measured in dB), as a function of symbol timing error variance, for K-PAM, K^2-QAM:

$$D(dB) \cong 4.34\left\{-g''(0)T_{SYM}{}^2 + \frac{E_{Savg}}{N_o}\sum_k [g'(kT_{SYM})T_{SYM}{}^2]\right\} var(\hat{\tau} - \tau) \qquad \textbf{(2-55)}$$

where:

- g'(t), and g"(t) represent the first and the second derivative of the overall system pulse shaping function g(t) (the pulse shape at the output of the receiver matched filter)
- $E_{Savg}/N_o=(K^2-1)E_o/(3N_o)$ is the value of the signal to noise ratio (for K-PAM) yielding the required BER in the case of no synchronization errors
- and the summation term should theoretically be performed for k={-∞...-1,0,1...∞}, but in a practical case only few terms around k=0 are necessary.
- var() is the unbiased variance of symbol timing error

As shown in equation (2-55) the amount of BER degradation caused by symbol timing errors is highly dependent on the pulse shape at the output of the receiver matched filter. In this thesis it is assumed that the overall system pulse shape g(t) is a raised-cosine (RC) function, thus the effect of the raised cosine pulse shape, with different rolloff factors, on the BER degradation has been illustrated in Table 2—2 and Figure 2—22.

Table 2—2. Parameters of BER Degradation Equation versus Rolloff Factor.

Rolloff (excess BW) Factor of Raised Cosine Pulse Shape Function g(t)	$-g''(0)(T_{SYM})^2$	$\Sigma(g'(kT_{SYM})T_{SYM})^2$ where: k={...-2,-1,0,1,2,...)
0.2	3.365	2.332
0.5	3.757	1.288
0.8	4.486	0.593

As shown in Figure 2—22, as the rolloff factor (also called excess bandwidth factor) increases, there is less BER degradation introduced. However, since in practical applications it is desired to keep the rolloff factor small for bandwidth efficiency, it has been decided to compromise and choose the rolloff factor of 0.5, for this thesis simulations.

With the assumption of RC pulse shape, with the roll-off factor of 0.5, the BER degradation (for K-PAM and K^2-QAM), due to timing error variance, equation reduces to:

$$D \cong 4.34\left\{3.757 + 1.29\frac{E_{Savg}}{N_o}\right\}\text{var}(\hat{\tau} - \tau) \qquad \textbf{(2-56)}$$

The bit error rate degradation has been calculated, using the above equation and the variance results from Figure 2—17 , for different cases of signal to noise ratio. The calculation results were tabulated in Table 2—3.

Table 2—3. BER Degradation Based on Results of Figure 2—17.

BER_o	E_s/N_o	2-PAM		4-PAM		8-PAM	
	(dB)	var()	D (dB)	var()	D (dB)	var()	D (dB)
1E-4	8.40	1.8E-3	0.099	4.5E-4	0.095	9.5E-5	0.079
1E-6	10.53	1.2E-3	0.096	3.0E-4	0.100	6.0E-5	0.081
1E-8	11.97	8.5E-4	0.089	2.0E-4	0.091	4.5E-5	0.084

As shown in Table 2—3 the BER degradation is approximately 0.1 dB, which is below the maximum recommended 0.2 dB value for a good synchronizer [8, Chapter 7.1]. A larger margin has been chosen, since in the simulation model, the signal quantization effects were not considered, but in practical implementation they would contribute to the additional BER degradation. The design parameters satisfying the maximum recommended BER degradation are shown in Figure 2—17.

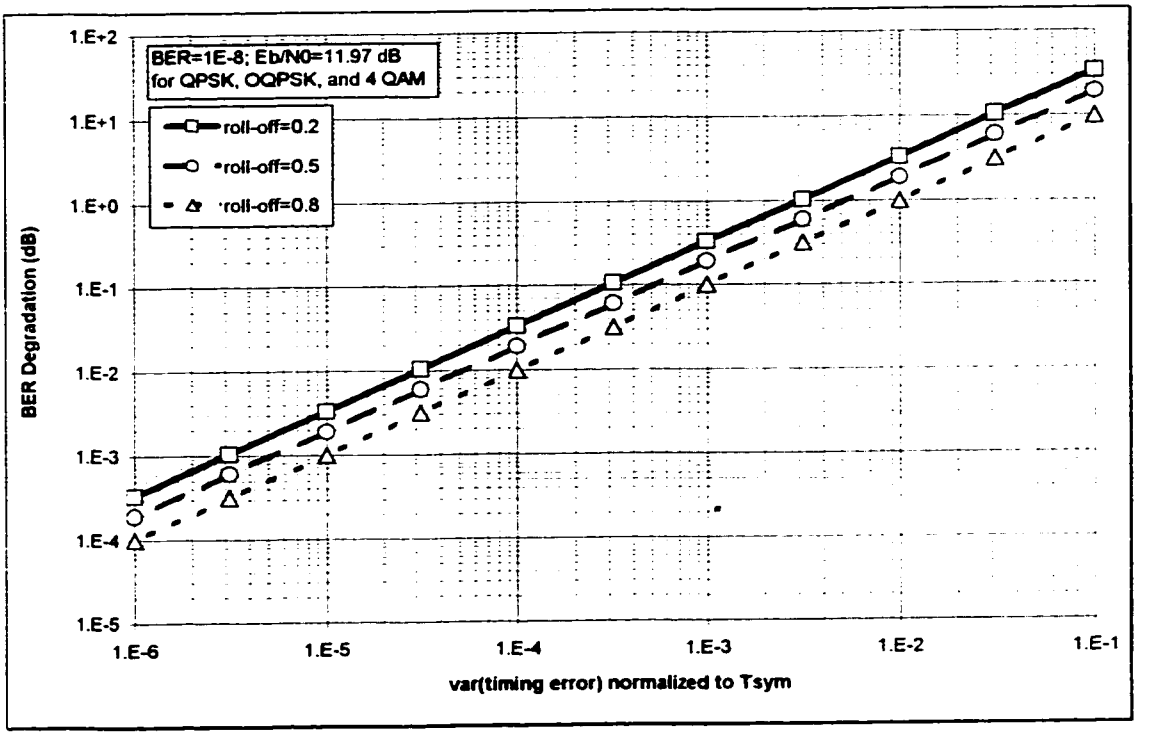

Figure 2—22. BER Degradation Curves for Different Rolloff Factors.

2.8. Acquisition Time

In this section, the acquisition time of the DSP-based Costas loop symbol synchronizer, with the initial timing offset of τ=0.375, will be investigated by means of the closed loop computer simulations. It will be shown, that the acquisition time of the DSP-based Costas loop symbol synchronizer, satisfying minimum BER degradation, is significantly lower than the acquisition time of the analog implementation presented in [7].

The timing error detector characteristic $K_D q()$ is usually used to determine the behavior of the tracking loop, when the timing error is close to the unstable equilibrium point e_U (negative slope zero crossing of $K_D q()$). Ideally this characteristic should have a sawtooth shape (as shown in Figure 2—11), such that a maximum positive or negative restoring force is applied when the timing error is near the unstable equilibrium point. However, in reality this is often not the case,

and there is always some finite slope at this point e_U. As the slope $q'(e_U)$, at point e_U, becomes smaller, the timing error value stays longer in the vicinity of this unstable equilibrium point, thus prolonging the acquisition time. This phenomenon is called hang-up [8, Chapter 2.3].

The approximate theoretical timing error detector characteristic of the DSP-based Costas loop symbol synchronizer, investigated in this thesis, is given by equation (2-30). The simulated TED characteristic obtained in the open loop environment (with assumption of no loop noise), is shown in Figure 2—11, and closely resembles the triangular TED characteristic shape. Since the slope, at the unstable equilibrium point e_U, value is relatively low, the expected hang-up effect would be significant. It should be mentioned that with some additional form of even rough feedforward symbol timing phase estimate, the chance of hung-up would be significantly reduced.

The acquisition time is also dependent on the loop bandwidth. It has been shown in [8, Chapter 6.5] that the average acquisition time, in the absence of noise, is inversely proportional to the one-sided loop bandwidth B_L, this behavior was also observed in our simulations, see Figure 2—23. The investigated DSP-based Costas loop symbol synchronizer has a relatively small bandwidth, thus the expected acquisition time is relatively long (see Figure 2—23).

As shown in Figure 2—24, the AWGN only slightly increased the timing acquisition, and such behavior is common to sinusoidal characteristic detectors [8, Chapter 6.5]. From the same simulations, it can be noticed, that the frequency detuning for up to 100 PPM did not significantly influenced the acquisition time.

It is interesting to point out, that although a symbol timing acquisition of 100 symbols, measured for 8-PAM signal and a loop bandwidth of 5.8E-5, seems long, it is significantly shorter from the timing acquisition of the analog implementation reported in [7] to be 400ms (with 460 kHz symbol rate), which translates to 184,000 symbols. This fact indicates that the proposed DSP-based Costas loop symbol synchronizer could be well suited for operation in continuous mode or long

burst mode systems. However, the acquisition time of 100 symbols, and in effect the DSP-based Costas loop symbol synchronizer, is totally unacceptable for short burst mode communication links (such as STS to BTS link in BWA system). Chapter 3 presents feedforward techniques which are well suited for short burst mode communication systems.

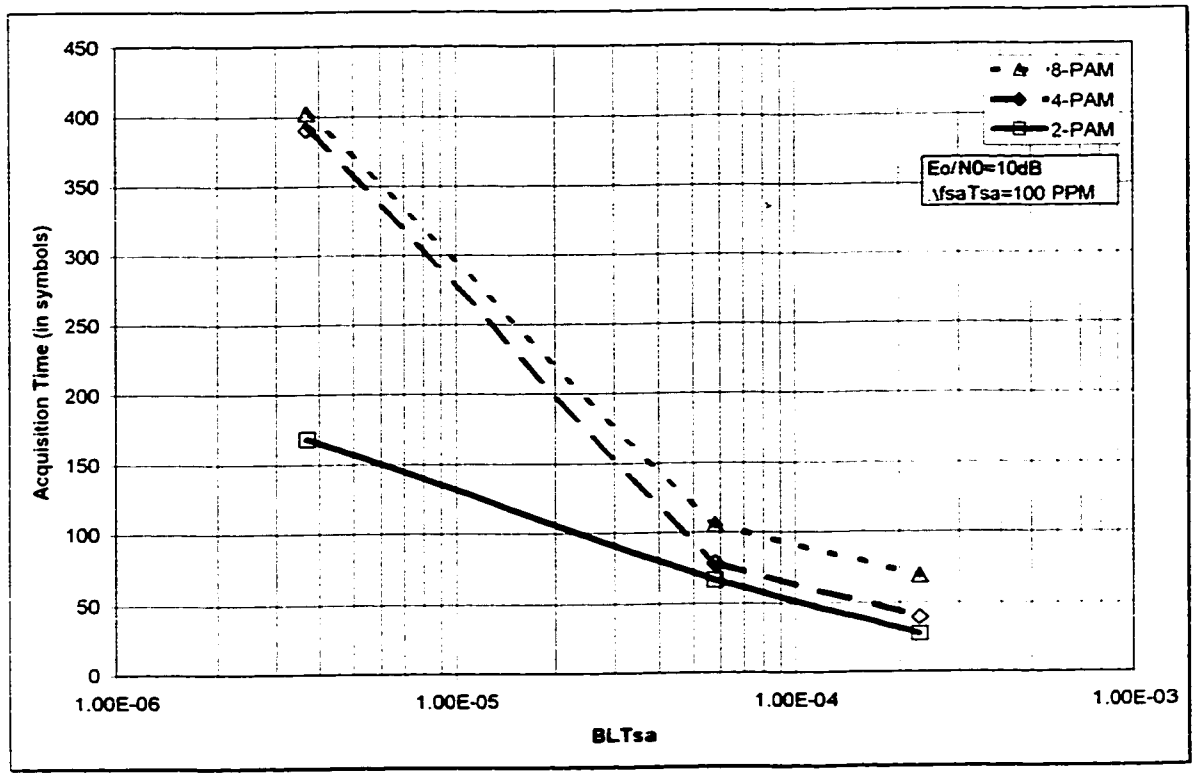

Figure 2—23. Acquisition Time versus Loop Bandwidth.

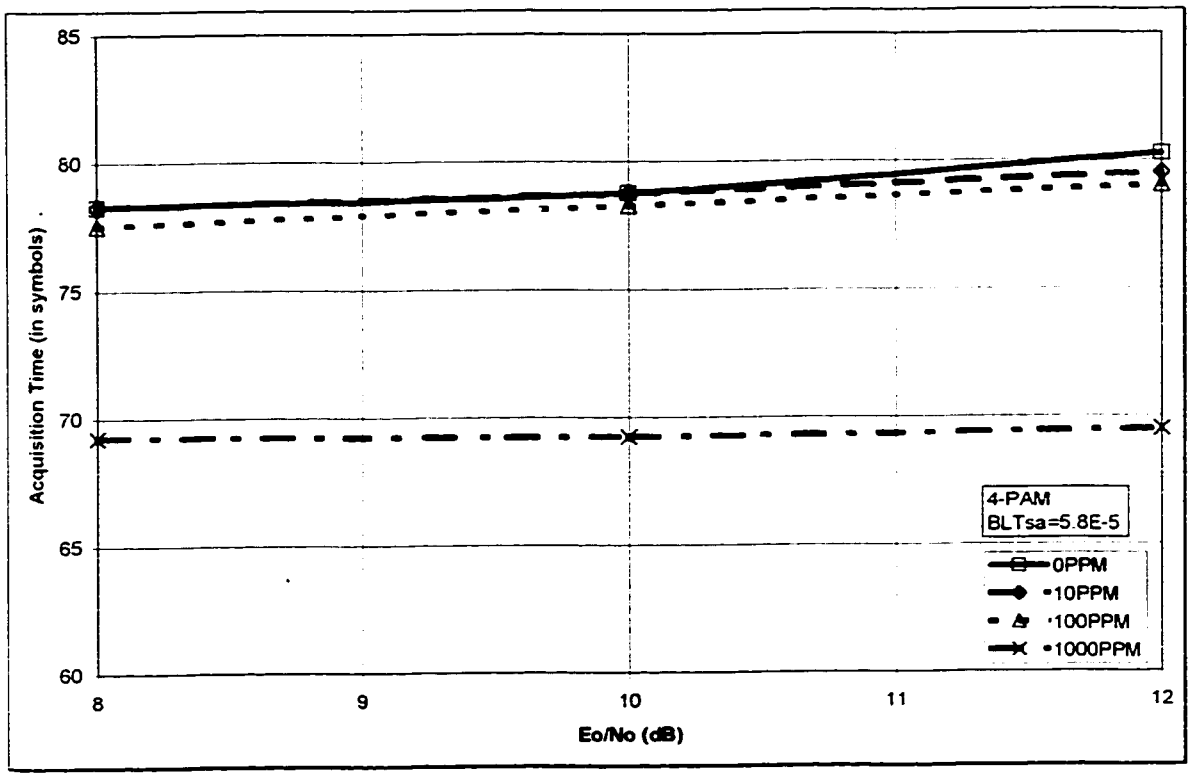

Figure 2—24. Acquisition Time versus AWGN and Frequency Detuning.

2.9. Implementation Complexity

In this section the digital implementation structure and the complexity of the proposed feedback symbol timing synchronizer will be presented in terms of multipliers and adders.

As shown in Figure 2—5 the proposed feedback timing synchronizer is made of the following digital modules: FIR prefilter, absolute value function, sine generator and IIR loop filter. It is assumed that the input signal is implemented in 2's complement form, and that L=4 samples per symbol are used. The L=4 is the minimum number of samples per symbol that can be used in proposed technique, since otherwise the result of equation (2-18) would always be zero.

2.9.1. Prefilter

From the prefilter's impulse response, equation (2-10) Figure 2—8, it can be shown that for L=4 the FIR filter with 25 coefficients can be implemented as a structure with only 3 constant multipliers and 6 adders (see Figure 2—25). Note that all simulations in this chapter were performed using this exact structure.

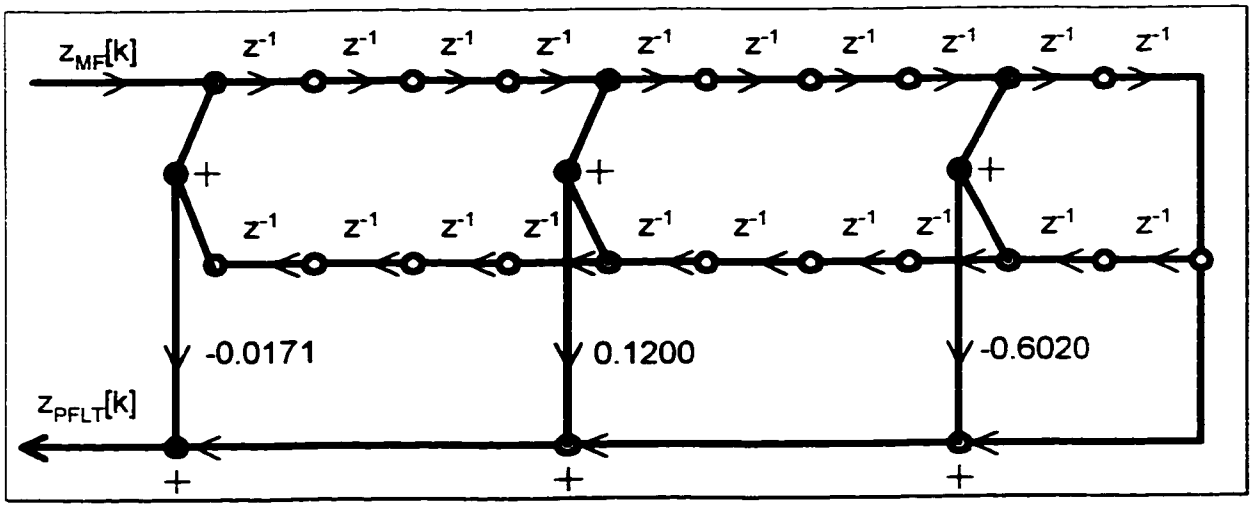

Figure 2—25. FIR Prefilter Structure.

2.9.2. Absolute Value

The absolute value of a discretized signal can be easily implemented by taking 2's complement of that number every time the sign bit indicates a negative value.

2.9.3. Sine Generator and Multiplier

From equation (2-18) it can be noticed that for L=4, the sine function will only take on values of 0 and ±1. Thus, the equation (2-18) can be implemented with only some simple logic (i.e. the true multiplier is not necessary).

2.9.4. IIR Loop Filter

Based on equation (2-23), the IIR loop filter structure can be illustrated as is shown in Figure 2—26. This implementation has only 2 constant multipliers and one adder. Note that the open loop gain can be adjusted by modifying constant A.

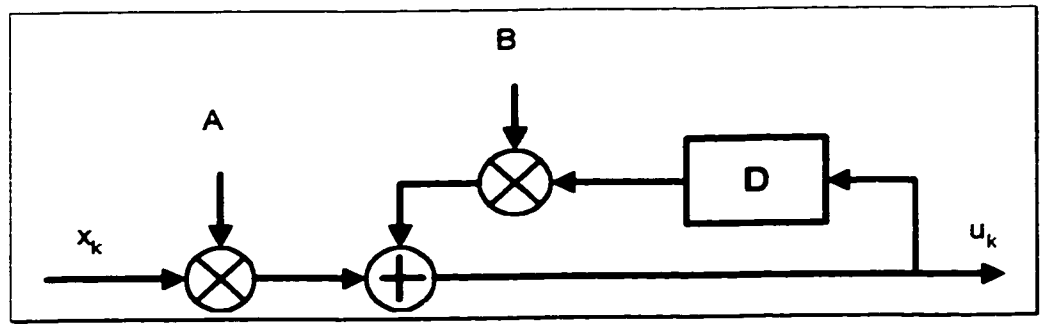

Figure 2—26. Discrete Time Representation of the 1-st Order Loop Filter.

In summary, the structure of the DSP-based Costas loop symbol synchronizer needs only 5 constant multipliers, 7 adders, some simple combinatory logic, which can all fit into a fraction of the FPGA chip, and the VCC and ADC (the only two analog components).

CHAPTER 3.

DATA-AIDED, FEEDFORWARD TIMING ESTIMATION TECHNIQUES

This chapter presents two new digital implementation, data-aided (DA), feedforward (FF) symbol timing phase estimation techniques, which have very fast acquisition time. As mentioned in Chapter 1, fast acquisition is very important for short and medium length burst mode communication links, such as upstream (subscriber to base station) link in broadband wireless access system. The first presented technique is based on the highly over-sampled maximum likelihood timing estimation technique, which results in low complexity implementation. The second technique is based on the first technique combined with the inverse interpolation algorithm, this approach results in low over-sampling version, at the cost of slightly increased complexity. Both techniques satisfy the recommended maximum bit error rate degradation for 4 and 16-QAM systems [8, Chapter 7].

The main research contributions of this chapter are the development, theoretical analysis, performance simulations, and FPGA prototype hardware bit error rate tests of a low complexity, maximum likelihood timing estimator. An outline of this chapter is given in the following paragraph.

This section briefly introduced what the presented timing estimators are based on, what are their main features, and is pointed out what are the main research contributions of this chapter.

Section 3.1 gives a background on the feedforward timing estimators (or symbol synchronizers), related to the presented techniques. In Section 3.2 the assumed system configuration is outlined. Section 3.3 describes the functional operation of the first proposed data-aided, feedforward, timing estimator, and it analytically proves that this technique is based on the optimum performance, maximum likelihood, timing estimation. Section 3.4 describes the functional operation of the second, modified, data-aided, feedforward, timing estimator. The low over-sampling techniques are usually preferred, since they can be applied for the fastest bit rate applications. Section 3.5 analytically derives and shows by simulation results that, as the estimation windows size, and/or signal to noise ratio increases, the mean error of the estimated timing approaches zero. Non zero mean timing error would result in severe bit error rate degradation. Section 3.6 derives the lower bound on variance, which specifies the best theoretically possible performance of the proposed timing estimator for given estimation window size and signal to noise ratio. In Section 3.7 the lower bound on variance, from Section 3.6, is modified to include the effects of the actual implementation techniques. The modified bound is closer to the practically achievable performance. Section 3.8 presents the simulation results for the variance of the timing error versus the size of the estimation window, the over-sampling rate and signal to noise ratio. Even if on average the timing error (mean) is zero, a large variance could significantly degrade the bit error rate performance (as shown later), thus the system parameters minimizing the timing error variance should be always carefully selected. Based on practical measurements, Section 3.9 shows that the proposed feedforward techniques, unlike general feedback techniques, do not generate self-noise or additional jitter in the recovered clock. Section 3.10 shows that the proposed feedforward timing estimation techniques, suffer less than 0.2 dB degradation with respect to ideally synchronized case. The 0.2 dB BER degradation is the maximum recommended value for good symbol synchronizers [8, Chapter 7]. Section 3.11 illustrates that the acquisition time for the proposed techniques depends only on the chosen length of the estimation window (STR preamble size). Section 3.12 concludes Chapter 3 with the detailed presentation of the implementation complexity, for the high over-sampling feedforward

timing estimator, and illustrates that this estimator can easily fit on a Field Programmable Gate Array (FPGA) chip.

3.1. Background

The extensive treatment of symbol synchronization for digital receivers have been covered in [8], thus only the background directly related to the proposed feedforward STR techniques is presented in this section.

When the receiver operates in short TDMA burst mode, it has to derive the unknown symbol clock phase (clock frequency is assumed to be known as explained in Section 3.2) of each received TDMA burst, and to establish the best sampling instant (defined as the position of the maximum "eye" openings) for optimum data recovery within a very short time. The feedforward (FF), data-aided (D-A), STR estimator algorithms, based on Maximum Likelihood (ML), potentially have the fastest acquisition time, and provide near optimum estimates [8, Chapter 6.5], [18]. Thus, these algorithms are good candidates for application in a short burst mode communication system, where fast acquisition time is essential.

The work on all-digital feedforward symbol timing recovery schemes can be found in [18], [19], [20], [21]. In [18] Gardner suggests that with the advanced digital implementation, a brute force search of the maximum likelihood (ML) function over the discretized timing offset parameter is feasible, and should provide near-optimum estimates. A general analysis of the sampled receivers, that handle arbitrary baseband pulse-shapes, and arbitrary fixed sampling rates is shown in [19]. In [20] the ML estimation (MLE) algorithm was used to design an all-digital receiver for combined modulation/coding schemes, and a fast acquisition synchronizer, which only needs 2-4 samples per symbol. However, the hardware implementation is involved. Another example of symbol timing recovery (STR), based on ML FF estimation and all-digital implementation, is shown in [21]. The approach presented in [21], uses 2 samples per symbol,

and the data interpolator for symbol timing adjustment. The simulation results show that the acquisition time of 64 symbols or more is needed.

Most of the all-digital algorithms, like the ones presented in [19], [20] and [21], concentrate on high speed communication methods, for which the sampling clock frequency cannot greatly exceed the symbol rate (due to hardware speed imposed limitations). In this type of algorithms the symbol timing adjustment must be done by data interpolation between the non-synchronized samples. A detailed discussion and analysis of the timing recovery by data interpolation is presented by Gardner in [22] and [23]. One of the drawbacks, of these data interpolation, and also the feedback algorithms, is a relatively long acquisition time, which might make these algorithms not well suited for burst mode communication systems, and especially not for short burst mode communications.

In this thesis, in order to develop a very low acquisition time symbol synchronizer, suitable for short burst mode communication systems, a low complexity technique utilizing high symbol over-sampling ratio was considered. For the applications where the sampling clock frequency cannot greatly exceed the symbol rate, a more complex symbol timing inverse interpolation technique is proposed as well, however, no extensive analysis were performed.

3.2. System Configuration

The presented FF D-A STR technique, was developed for the application in the base station (BTS) of a point-to-multipoint wireless (BWA) TDMA/TDM communication system, shown in Figure 1—1. The modulation schemes could be QPSK, OQPSK, 4-QAM or 16-QAM. The base station (BTS) transmits to various subscriber stations (STS) in a time division multiplexing (TDM) continuous mode, and receives signals from the subscriber stations (STS) in a burst mode TDMA scheme. The following are the main communication system assumptions considered in this chapter.

The first assumption is that there is always a line of sight (LOS) between the base station (BTS) and every subscriber station (STS), and all the stations are stationary, thus the AWGN channels can be assumed (see Section 2.2 for notes on multipath and frequency selective channels).

The second assumption is that the symbol clock frequency of each received TDMA burst is known to the base station, since the symbol timing clock in all subscriber stations could be derived (using classical feedback loop) from the TDM continuous signal transmitted by the base station.

Due to the difference in distances between various subscriber stations and the base station, the propagation time delay is different for each received burst. Thus, the third assumption is that the resulting phase of the symbol timing clock, for each received TDMA burst, is unknown to the base station, and has to be estimated for each received TDMA burst. Although, not investigated here, the large differences in propagation delays for each transmitter can be significantly reduced by applying "ranging" algorithm, which is usually a part of frame synchronization in a system.

In a stationary, short burst mode communication system (about one hundred symbols per burst), the clock phase for a given remote station is usually slowly varying, thus it is assumed that the clock phase error is constant during each burst, and only one estimate per burst is sufficient. This assumption allows for use of a "one-shot" estimator (using only a single observation interval) for timing recovery. Note: only the phase error due to propagation delay is assumed, the random phase jitter was not considered.

The last main assumption is that the received down-converted signal is already corrected for carrier phase and frequency errors [2].

The main system assumptions are summarized in Table 3—1, and the general block diagram of the base station demodulator, reflecting some of these assumptions, is shown in Figure 3—1.

Table 3—1. General Communication System Assumptions.

	System Assumption Description
1	QPSK, OQPSK, 4-QAM or 16-QAM
2	AWGN channels
3	Known symbol clock frequency
4	Symbol clock phase: unknown but constant during the burst
5	The carrier recovery is done prior to symbol timing recovery

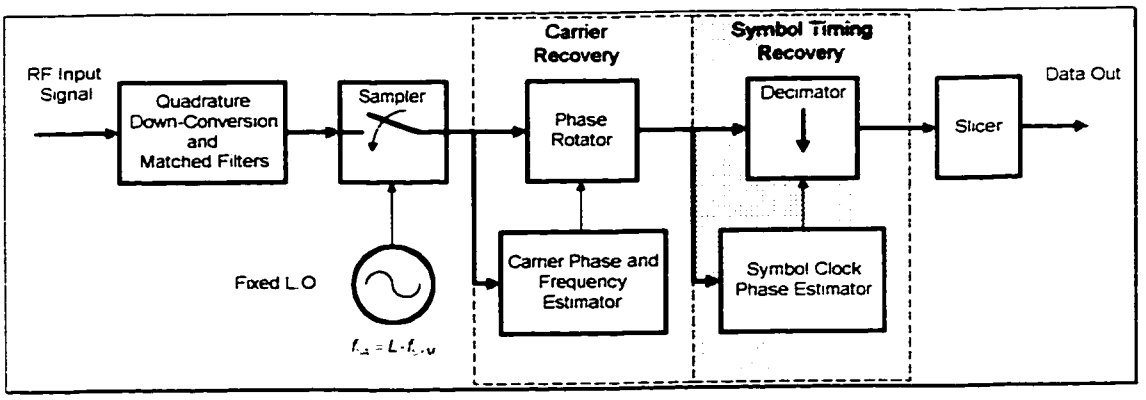

Figure 3—1. General Block Diagram of the Assumed Demodulator.

3.3. Maximum Likelihood Symbol Timing Estimation

In this section the proposed FF D-A STR technique will be presented, and it will be proved that this technique is based on the maximum-likelihood (ML) symbol timing synchronization algorithm. The ML function will be first derived for a 2-level PAM signal, and later it will be extended to QPSK, OQPSK and QAM modulation schemes.

3.3.1. Signal Model

In order to make the description, and ML derivation, of the proposed FF D-A STR algorithm easier, the communication path from the transmitter to the receiver is represented by the

equivalent baseband model shown in Figure 2—4, and described in the following paragraphs. The equivalent signals, at different points of the transmission path, have been derived in Appendix A.

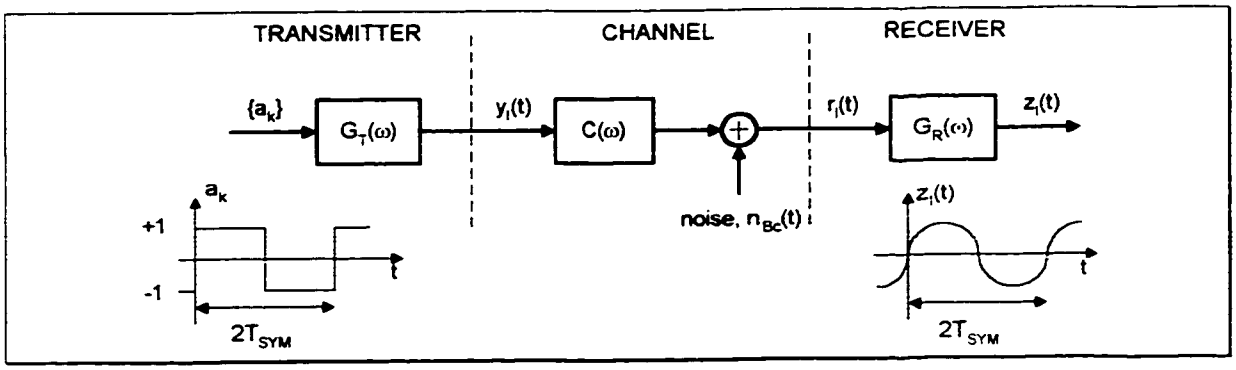

Figure 3—2. Transmission Path Equivalent Baseband Model.

Input sequence

Every transmitted packet, in the data-aided burst mode communication system, has a preamble, which is a set of known symbols added to the user's data at the transmitter, and is used to assist the receiver in acquisition. In this thesis, a classical preamble (see Figure 3—3) with three sections of: CR training sequence, STR training sequence, and unique word, was considered. Since the proposed symbol timing estimator is a one-shot estimator, it only uses a STR training sequence section out of a given packet, thus for convenience of explanation, and ML derivation, it is assumed that the input sequence $\{a_k\}$ to the transmitter is a continuous STR training sequence (i.e. the inter symbol interference, ISI, from other sections of the packet is ignored). The training sequence for STR is generally designed, such that it has as many symbol transitions as possible (for symbol timing recovery based on zero crossing). For a 2-level PAM signal, that means, that the data symbols training sequence is made of the alternating positive and negative ones, $\{a_k\}=(-1)^k$. For multiple level PAM (for example 4-PAM) the training symbol sequence would be made of alternating most outer levels. Thus in time domain, the input to the transmitter pulse shaping filter has a square wave shape with an amplitude of ± 1 (for 2-PAM) and a period of $2T_{SYM}$.

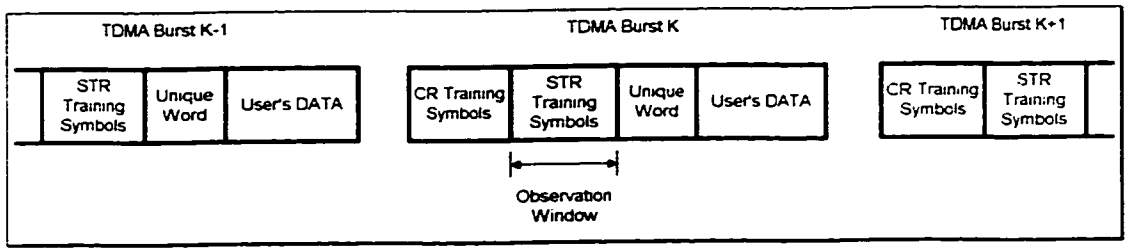

Figure 3—3. Considered Burst Modem Packet Format.

Transmitter Filter

Data symbols, a_k, pass through the transmitter pulse shaping filter with impulse response $g_T(t)$, and the resulting transmitted signal is given by:

$$y_I(t) = \sum_{k=-\infty}^{\infty} a_k g_T(t - (k+\tau)T_{SYM}) \tag{3-1}$$

where:

T_{SYM} : Symbol period

τ : Normalized symbol clock phase offset, incorporating the unknown time delay, resulting from the linear phase distortion of the channel between the transmitter and the receiver, $|\tau| \leq 0.5$.

Channel

The transmission channel is assumed to have constant magnitude frequency response, $|C(\omega)|=1$, with linear phase distortion (accounted for in a transmitted signal description, equation (2-1)), and it is assumed that the transmitted signal is disturbed by AWGN $n_{Bc}(t)$, with zero mean and variance of $N_o/(4E_b)$ (derived in Appendix A). Thus, the received signal is:

$$r_I(t) = y_I(t) + n_{Bc}(t) \tag{3-2}$$

Receiver Filter

The received noisy PAM signal is applied to the receiver matched filter, and as shown in Section 3.2.1, the output of the receiver matched filter is:

$$z_i(t) = \sum_{k=-\infty}^{\infty} a_k g(t-(k+\tau)T_{SYM}) + v_{nc}(t) \tag{3-3}$$

It is assumed that the pulse shaping function g(t) is a raised cosine function:

$$g(t) = \frac{\sin(\pi t/T_{SYM})}{\pi t/T_{SYM}} \frac{\cos(\alpha \pi t/T_{SYM})}{1-4\alpha^2 t^2/T_{SYM}^2} \tag{3-4}$$

The raised cosine function in frequency domain is defined as:

$$G(f) = \begin{cases} T_{SYM} & |f| < \dfrac{1-\alpha}{2T_{SYM}} \\ \dfrac{T_{SYM}}{2}\left\{1+\cos\left[\dfrac{\pi T_{SYM}}{\alpha}\left(|f|-\dfrac{1-\alpha}{2T_{SYM}}\right)\right]\right\} & \dfrac{1-\alpha}{2T_{SYM}} \le |f| < \dfrac{1+\alpha}{2T_{SYM}} \\ 0 & |f| \ge \dfrac{1+\alpha}{2T_{SYM}} \end{cases} \tag{3-5}$$

It can be shown, that for the raised cosine function g(t), and the alternating ±1 data symbols transmitter input sequence $\{a_k\}$, the output of the receiver matched filter can be represented by a cosine function with the noise component $v_{nc}(t)$,

$$z_i(t) = \pm\cos\left[\frac{\omega_{SYM}}{2}t - \tau\pi\right] + v_{nc}(t) \tag{3-6}$$

3.3.2. Description of the FF D-A STR Technique

From equation (3-6) it can be seen, that the expected signal at the output of the matched filter, during the symbol timing recovery training section, has the cosine wave shape with a period of $2T_{SYM}$, since the noise component $v_{nc}(t)$ is assumed to be zero mean. The best data symbol sampling position is at the maximum eye opening of $z_I(t)$, thus the position of the maximum or the minimum of $z_I(t)$ corresponds to the optimum data symbol sampling position. The proposed technique finds that maximum eye opening in the following way. First, the output signal $z_I(t)$ of the receiver matched filter is over-sampled by a relatively high ratio L, and the samples are indexed with values from 0 to L-1. Second, the magnitude value of each indexed sample is averaged over few symbols. Then, out of L resulting (averaged) samples, the sample which has the largest magnitude, and its corresponding index value, is found. This index is defined as the estimated maximum eye opening sample index. During the unique word and the user's data section of the burst, the over-sampled signal $z_I(t)$ is down-sampled at time corresponding to the estimated maximum eye opening sample index. The block diagram illustrating the above STR technique, for 2 level PAM modulation, is shown in Figure 3—5.

In QPSK, OQPSK and QAM schemes, the in-phase and quadrature channels are statistically independent, thus can be visualized as two independent PAM signals, which can be used together (i.e. averaged) in order to further reduce the effect of the additive noise. The final block diagram illustrating the FF D-A STR technique, for QPSK, OQPSK and QAM modulation, is shown in Figure 3—6.

3.3.3. Maximum Likelihood Function Derivation

In this section, it is proven that the proposed FF D-A STR technique is a Maximum Likelihood estimation technique, which means the proposed estimator is able to deliver an optimal performance.

It is well known, that the maximum likelihood estimate of a given parameter ϕ, is obtained by maximizing the likelihood function $p(\underline{r}_I|\phi)$ wrt ϕ, i.e. $\phi = \hat{\phi}_{ML}$ is the value which most likely gives rise to the observation $\underline{r}_I$. In this thesis' case, $\underline{r}_I$ denotes a set of observations $\{r_{I1}, r_{I2},\ldots,r_{IN}\}$ of the received signal, which is a baseband PAM waveform:

$$r_I(t) = y_I(t;\tau) + n_{Bc}(t) \tag{3-7}$$

where:

$$y_I(t;\tau) = \sum_{k=-\infty}^{\infty} a_k g_T(t-(k+\tau)T_{SYM})$$

ϕ : represents an unknown, but deterministic signal parameter $\phi=\tau T_{SYM}$ (fractional time delay between transmitter and receiver)

Since it is more convenient to deal directly with the signal waveforms, than vector representation, when estimating their parameter, the following continuous-time equivalent of the maximization of $p(\underline{r}_I|\tau)$ is adopted from [12].

It can be recalled that if $n_{Bc}(t)$ is AWGN with zero mean then $\underline{r}_I$ has Gaussian distribution with joint probability density function (pdf) determined as:

$$p(\underline{r}_I \mid \tau) = \left(\frac{1}{\sqrt{2\pi\sigma_{n_B}^{\ 2}}}\right)^N \exp\left[-\frac{1}{2\sigma_{n_B}^{\ 2}}\sum_{n=1}^{N}(r_{In}-y_{In}(t;\tau))^2\right] \tag{3-8}$$

It is shown in [12], that r_{In} and y_{In} can be substituted by:

$$r_{In} = \int_{T_o} r_I(t) f_n(t)dt \tag{3-9}$$

and

$$y_{ln} = \int_{T_o} y_l(t;\tau) f_n(t)dt \tag{3-10}$$

where:

$T_o \geq T_{SYM}$: is the estimation observation interval, and

$f_n(t)$: is an orthonormal function

Thus, forming the following joint pdf:

$$p(\underline{r}_l \mid \tau) = \left(\frac{1}{\sqrt{2\pi\sigma_{n_B}^2}} \right)^N \exp\left[-\frac{1}{2\sigma_{n_B}^2} \int_{T_o} (r_l(t) - y_l(t;\tau))^2 dt \right] \tag{3-11}$$

Now, following the classical ML derivation, the maximization of $p(\underline{r}_l|\tau)$ wrt signal parameter τ is equivalent to maximization of the likelihood function,

$$\begin{aligned} \Lambda(\tau) &= \exp\left[-\frac{1}{2\sigma_{n_B}^2} \int_{T_o} (r_l(t) - y_l(t;\tau))^2 dt \right] \\ &= \exp\left\{ -\frac{1}{2\sigma_{n_B}^2} \left[\int_{T_o} r_l^2(t)dt - 2\int_{T_o} r_l(t) y_l(t;\tau)dt + \int_{T_o} y_l^2(t;\tau)dt \right] \right\} \end{aligned} \tag{3-12}$$

The first term of the above equation does not involve signal parameter τ, and the third term is a constant equal to the signal energy over the observation interval T_o for any value of τ. Thus, only the second term, which involves the cross-correlation of the received signal $r_l(t)$ with the signal $y_l(t)$, depends on the choice of τ. Therefore, the likelihood function $\Lambda(\tau)$ could be expressed as:

$$\Lambda(\tau) = C \exp\left[\frac{1}{\sigma_{n_B}^2}\int_{T_o} r_I(t) y_I(t;\tau)dt\right] \quad \textbf{(3-13)}$$

where:

C : is a constant independent of τ, thus can be dropped

The ML estimate $\hat{\tau}_{ML}$ is the value of τ that maximizes $\Lambda(\tau)$. Equivalently, the value $\hat{\tau}_{ML}$ also maximizes the logarithm of $\Lambda(\tau)$ i.e. the log-likelihood function,

$$\Lambda_L(\tau) = \frac{1}{\sigma_{n_B}^2}\int_{T_o} r_I(t) y_I(t;\tau)dt = C_L\int_{T_o} r_I(t) y_I(t;\tau)dt \quad \textbf{(3-14)}$$

where:

C_L : is a constant independent of τ, thus can be dropped

Substituting for $y_I(t;\tau)$ the following is obtained:

$$\Lambda_L(\tau) = \sum_{k=-\infty}^{\infty} a_k \int_{T_o} r_I(t) g_T(t-(k+\tau)T_{SYM})dt \quad \textbf{(3-15)}$$

For implementation purposes, the infinite summation is replaced by finite summation from m=1 to m=M (where $MT_{SYM}=T_o$ is the observation time), and the finite integration over T_o is replaced with infinite integration, thus:

$$\Lambda_L(\tau) = \sum_{m=1}^{M} a_m \int_{-\infty}^{\infty} r_I(t) g_T(t-(m+\tau)T_{SYM})dt \quad \textbf{(3-16)}$$

It has been shown in section 2.3.1 that $g_R(t)=g_T(-t)$, so the integral in the above equation can be represented as the output of the receiver matched filter sampled at $t=(m+\tau)T_{SYM}$.

$$z_i((m+\tau)T_{SYM}) = \int_{-\infty}^{\infty} r_i(t) g_T(t-(m+\tau)T_{SYM})dt$$
$$= \int_{-\infty}^{\infty} r_i(t) g_R((m+\tau)T_{SYM}-t)dt \quad \textbf{(3-17)}$$

And the function $\Lambda_L(\tau)$ can be rewritten as:

$$\Lambda_L(\tau) = \sum_{m=1}^{M} a_m z_i((m+\tau)T_{SYM}) \quad \textbf{(3-18)}$$

For moderate signal to noise ratios, the product in the summation can be replaced by the magnitude of z_i

$$a_m z_i((m+\tau)T_{SYM}) \cong |z_i((m+\tau)T_{SYM})| \quad \textbf{(3-19)}$$

Thus, the log-likelihood function to be maximized is:

$$\Lambda_L(\tau) = \sum_{m=1}^{M} |z_i((m+\tau)T_{SYM})| \quad \textbf{(3-20)}$$

One of the methods to find the ML estimate $\hat{\tau}_{ML}$ value maximizing $\Lambda_L(\tau)$, in the feedforward fashion, is to sample the receiver matched filter output at several different trial timing delays τ_i, evaluate every $\Lambda_L(\tau_i)$ function, and choose, as the ML estimate $\hat{\tau}_{ML}$, that trial timing delay τ_i, which results in the maximum $\Lambda_L(\tau_i)$. The estimated $\hat{\tau}_{ML}$ is used to control the sampler for data detector during the unique word, and user's data, burst section. This technique is illustrated in Figure 3—4, and formulated as:

$$\Lambda_L(\tau_i) = \sum_{m=1}^{M} |z_1((m+\tau_i)T_{SYM})| \qquad \textbf{(3-21)}$$

$$\hat{\tau}_{ML} = \tau_i \text{ resulting in max. } \Lambda_L(\tau_i) \qquad \textbf{(3-22)}$$

where:

i : is the sampling index with range $0 \leq i \leq L-1$

The parallel implementation of the samplers at the output of the receiver's matched filter can be replaced by L times over-sampling block and demultiplexer directing each i-th sample to the appropriate $\Lambda_L(\tau_i)$ bank. This alternative implementation of the FF D-A STR for 2 level PAM signal is shown in Figure 3—5. The parallel branches operate on preamble and then the top branch operates on the rest of the burst by decimating the samples from the analog to digital converter (ADC), at the estimated best sampling time. In actual, practical implementation, the parallel branches, with magnitude blocks, are replaced by one branch with magnitude extractor and accumulator RAM block as discussed in Section 3.12.

Note: For analysis and simulations the matched filter, shown in Figure 3—4 and Figure 3—5, has been assumed to be a raised cosine filter, however, in practical implementation the analog Gaussian matched filter has been used. In other implementations the matched filter could be implemented digitally, after ADC, as the raised cosine filter.

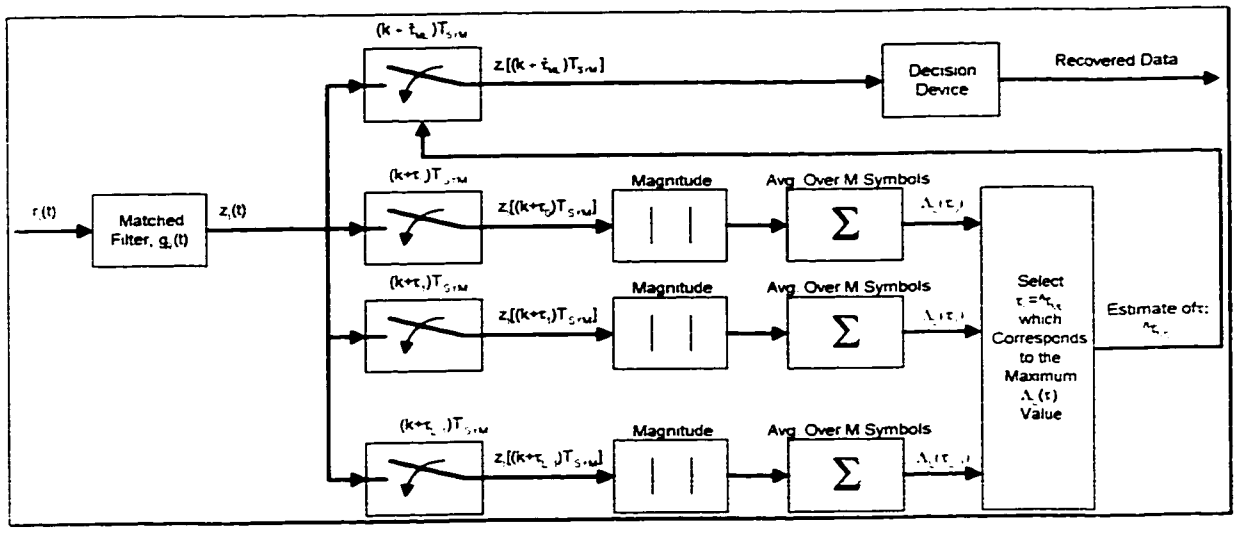

Figure 3—4. FF D-A STR for Symbol Rate Sampled 2-PAM Signal.

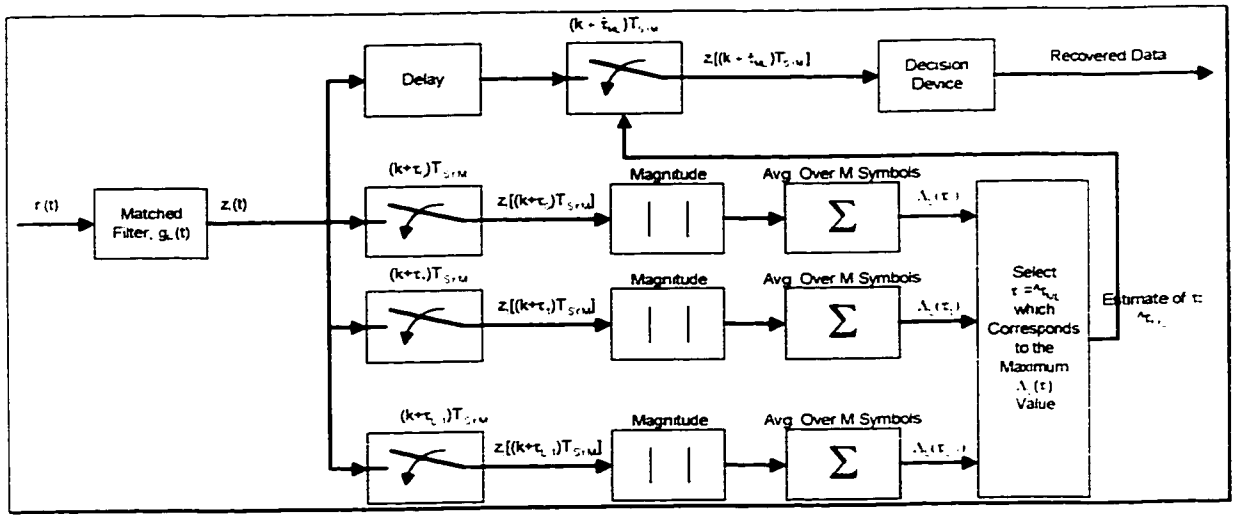

Figure 3—5. FF D-A Symbol Timing Recovery for Over-Sampled 2-PAM Signal.

The above ML derivation can be easily expanded to 2 dimensional cases, like QPSK, OQPSK and M^2-QAM, by representing the received signal r(t) and the transmitted signal y(t) as the complex functions,

$$r(t) = r_I(t) + jr_Q(t) \tag{3-23}$$

$$y(t) = y_I(t) + jy_Q(t) \tag{3-24}$$

where:

r_I, y_I : are the in-phase signals,

r_Q, y_Q : are the quadrature signals, and

$$y_I(t) = \sum_{k=-\infty}^{\infty} a_k g_T(t-(k+\tau)T_{SYM})$$

$$y_Q(t) = \sum_{k=-\infty}^{\infty} b_k g_T(t-(k+\tau+\Delta)T_{SYM})$$

Solving the likelihood function [24],

$$\Lambda(\tau) = p(\underline{r} \mid \tau) = C_1 \exp\left[-\frac{1}{2\sigma_{n_B}^2}\int_{T_o} |r(t)-y(t;\tau)|^2 dt\right] \quad \textbf{(3-25)}$$

Which similarly as equation (3-13) evaluates to:

$$\Lambda(\tau) = C_1 \exp\left[\frac{1}{\sigma_{n_B}^2}\int_{T_o} [r_I(t)y_I(t;\tau)+r_Q(t)y_Q(t;\tau)]dt\right] \quad \textbf{(3-26)}$$

The above likelihood function, for two dimensional case, reduces to the following log-likelihood function, the same way as for one dimensional case,

$$\Lambda_L(\tau) = \sum_{m=1}^{M} [|z_I((m+\tau)T_{SYM})| + |z_Q((m+\tau+\Delta)T_{SYM})|] \quad \textbf{(3-27)}$$

where:

z_I : is the output of the in-phase receiver's matched filter at $t=(m+\tau)T_{SYM}$

z_Q : is the output of the quadrature receiver's matched filter at $t=(m+\tau+\Delta)T_{SYM}$

The maximization technique of equation (3-27) is based on the same approach as for the one dimensional case and is presented in Figure 3—6. In terms of trial timing parameter τ_i, the log likelihood function to be solved is:

$$\Lambda_L(\tau_i) = \sum_{m=1}^{M} \left[\left| z_I((m+\tau_i)T_{SYM}) \right| + \left| z_Q((m+\tau_i+\Delta)T_{SYM}) \right| \right] \quad \textbf{(3-28)}$$

$$\hat{\tau}_{ML} = \tau_i \text{ resulting in max. } \Lambda_L(\tau_i) \quad \textbf{(3-29)}$$

where:

i : is the sampling index with range $0 \le i \le L-1$

Due to trial timing discretization, the estimated timing position, even in noiseless environment, has an error in range of $\pm T_{SYM}/(2L)$. When high symbol over-sampling rate is used (L is large) this discretization error is acceptably small for OQPSK or 4QAM applications. However, for higher modulations (16QAM) or for low over-sampling rate applications, the discretization error could considerably degrade the performance. Thus, for the case when high over-sampling rate is not feasible, or smaller timing error is required, it is suggested to use an additional inverse linear interpolation algorithm, presented in Section 3.4, which significantly improves the accuracy of the timing estimator at a price of increased complexity.

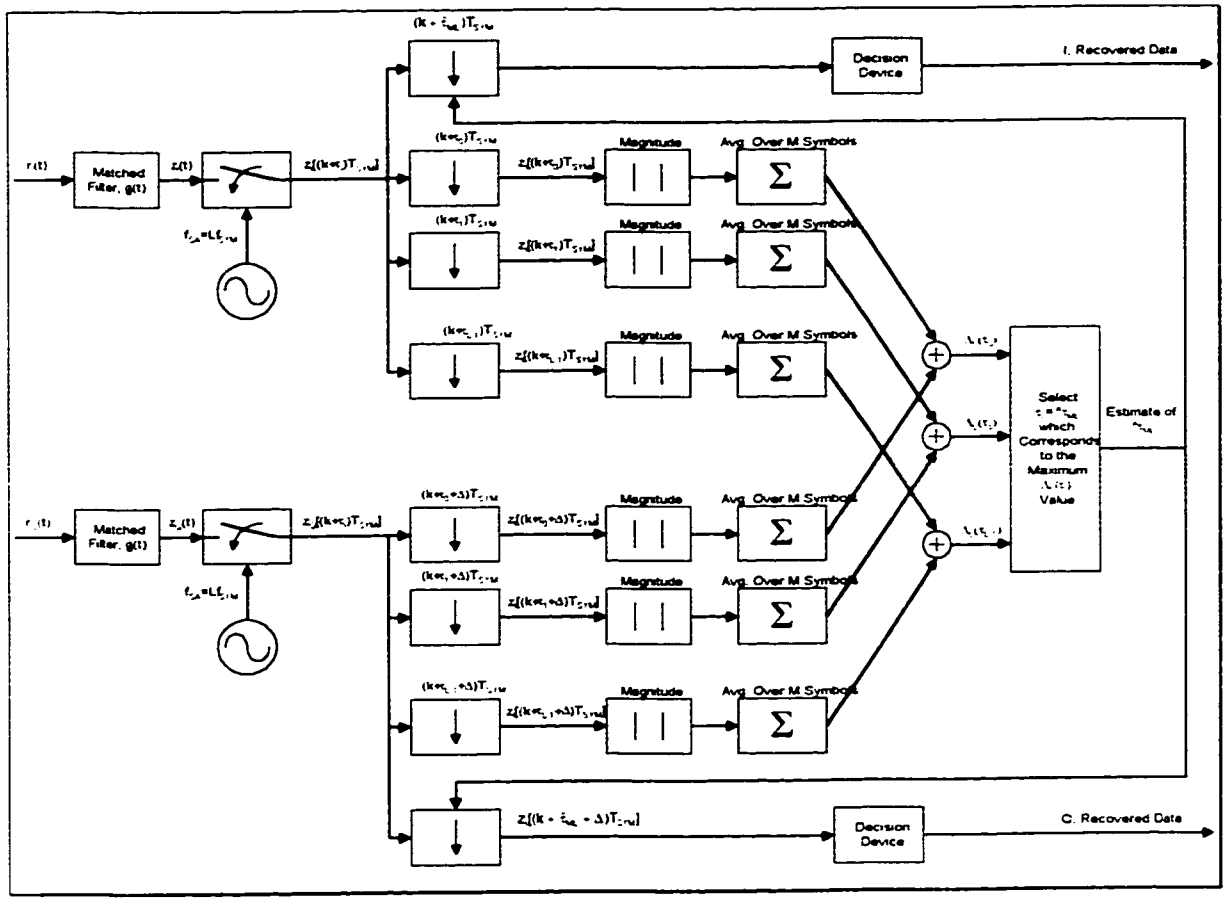

Figure 3—6. FF D-A Symbol Timing Recovery for Over-Sampled (O)QPSK Signal.

3.4. Symbol Timing Correction by Interpolation

In this section it is shown that by using an additional inverse interpolation algorithm, together with the FF D-A STR technique presented in Section 3.3, the symbol timing error, due timing discretization process, is significantly reduced ($<<T_{SYM}/(2L)$), and thus the over-sampling rate as small as 4 or 3 samples per symbol can be used without penalty to symbol timing variance.

In the following sub-sections the proposed inverse interpolation technique will be described, and the resulting maximum timing position error range will be derived, for the case of noiseless input signal. The performance evaluation in noisy environment is presented in Section 3.5, 3.7 & 3.8.

3.4.1. Description

The FF D-A STR technique, presented in Section 3.3, calculates the log-likelihood functions $\Lambda_L(\tau_i)$ for each trial timing position τ_i, where i={0,1,..,L-1}, and finds the timing position $\hat{\tau}_{ML}$ corresponding to the maximum log-likelihood function $\Lambda_L(\hat{\tau}_{ML})$. The estimated $\hat{\tau}_{ML}$ is used to decimate the over-sampled signal at the output of the matched filter, at time $t=(k+\hat{\tau}_{ML})T_{SYM}$, for symbol data detection (as shown in Figure 3—7). The equally spaced, samples of the log-likelihood function $\Lambda_L(\tau_i)$ are further used, by inverse interpolation algorithm, to find a much more accurate maximum eye opening timing position $\hat{\tau}_{MLnew}$, which is somewhere between two mid-sampling points $\hat{\tau}_{ML-0.5}$ and $\hat{\tau}_{ML+0.5}$. The difference between the new $\hat{\tau}_{MLnew}$, found by inverse interpolation, and the initial $\hat{\tau}_{ML}$ is a fraction of a duration T_{SYM}/L between two samples, denoted as $\Delta\hat{\tau}_{ML} = \hat{\tau}_{MLnew} - \hat{\tau}_{ML}$. The $\Delta\hat{\tau}_{ML}$ signal is used to phase shift the input signal sampling clock by the appropriate fraction of the sample duration T_{SYM}/L. Thus, during the user's data the input signal is sampled at the new estimated optimum sampling instant. The general block diagram of this technique is shown in Figure 3—7 (note that CR section is omitted). Although, the structure shown in Figure 3—7 may look like the feedback structure, in fact it is still a feedforward structure, since the sampling clock phase correction is done only once per burst, and is done after the initial STR estimation is completed.

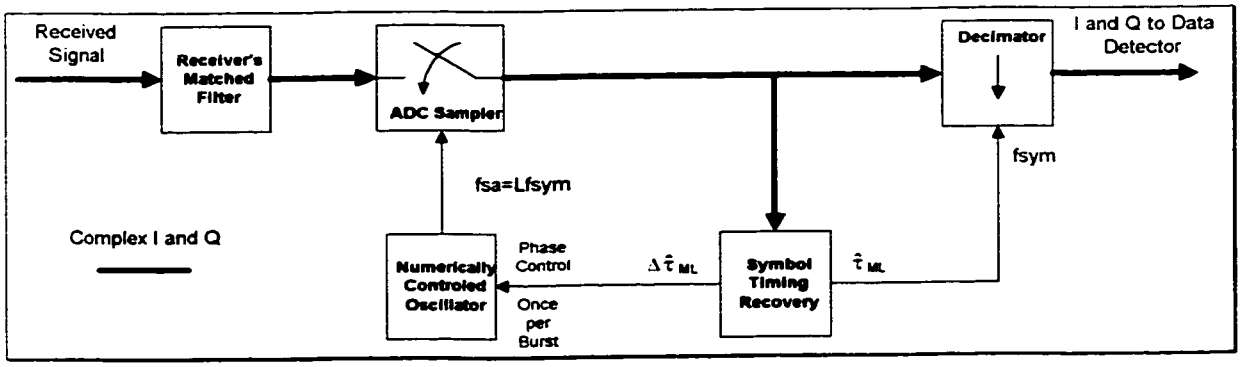

Figure 3—7. The Block Diagram of the Sampling Clock Phase Correction.

In order to find the new $\hat{\tau}_{MLnew}$, the linear inverse interpolation technique is used, which is the least complex interpolation technique, yet still sufficiently accurate for practical purposes (as will be shown later). This technique is illustrated in Figure 3—8, and described in more detail as follows. The $\Lambda_L(\tau)$ function around $\hat{\tau}_{ML}$ is piecewise convex, thus the τ corresponding to the maximum $\Lambda_L(\tau)$, can be found by equating derivative $d\Lambda_L(\tau)/d\tau$ to zero and solving for $\tau=\hat{\tau}_{MLnew}$. The three sample points $\Lambda_L(\hat{\tau}_{ML-1})$, $\Lambda_L(\hat{\tau}_{ML})$, and $\Lambda_L(\hat{\tau}_{ML+1})$, around the timing position $\hat{\tau}_{ML}$, are used to calculate piecewise derivative (slope) of the log-likelihood function at $\tau=\hat{\tau}_{ML-0.5}$ and $\tau=\hat{\tau}_{ML+0.5}$.

$$w_0 = w(\hat{\tau}_{ML-0.5}) = \left.\frac{\Delta\Lambda_L(\tau)}{\Delta\tau}\right|_{\tau=\hat{\tau}_{ML-0.5}} = \frac{\Lambda_L(\hat{\tau}_{ML}) - \Lambda_L(\hat{\tau}_{ML-1})}{\hat{\tau}_{ML} - \hat{\tau}_{ML-1}} \tag{3-30}$$

$$w_1 = w(\hat{\tau}_{ML-0.5}) = \left.\frac{\Delta\Lambda_L(\tau)}{\Delta\tau}\right|_{\tau=\hat{\tau}_{ML-0.5}} = \frac{\Lambda_L(\hat{\tau}_{ML-1}) - \Lambda_L(\hat{\tau}_{ML})}{\hat{\tau}_{ML-1} - \hat{\tau}_{ML}} \tag{3-31}$$

And, the continuous function $w(\tau)=d\Lambda_L(\tau)/d\tau$, for $\hat{\tau}_{ML-0.5}<\tau<\hat{\tau}_{ML+0.5}$ is approximated by the linear interpolation,

$$w(\tau) = \frac{d\Lambda_L(\tau)}{d\tau} \cong L_0 w_0 + L_1 w_1 \quad \text{for} \quad \hat{\tau}_{ML-0.5} \le \tau \le \hat{\tau}_{ML-0.5} \tag{3-32}$$

where:

$$L_0 = -\frac{\tau - \hat{\tau}_{ML-0.5}}{\hat{\tau}_{ML-0.5} - \hat{\tau}_{ML-0.5}} \tag{3-33}$$

$$L_1 = \frac{\tau - \hat{\tau}_{ML-0.5}}{\hat{\tau}_{ML-0.5} - \hat{\tau}_{ML-0.5}} \tag{3-34}$$

Now, substituting equations (3-33) and (3-34) into (3-32), and equating $w(\tau = \hat{\tau}_{MLnew})=0$, the new $\hat{\tau}_{MLnew}$ is found. The following is the inverse interpolation function to be solved,

$$\hat{\tau}_{MLnew} = \frac{w(\hat{\tau}_{ML-0.5})\hat{\tau}_{ML-0.5} - w(\hat{\tau}_{ML-0.5})\hat{\tau}_{ML-0.5}}{w(\hat{\tau}_{ML-0.5}) - w(\hat{\tau}_{ML-0.5})} \tag{3-35}$$

Thus, the difference between the new $\hat{\tau}_{MLnew}$ and the initial $\hat{\tau}_{ML}$ is:

$$\begin{aligned} \Delta\hat{\tau}_{ML} &= \hat{\tau}_{MLnew} - \hat{\tau}_{ML} \\ &= \frac{W_0\hat{\tau}_{ML-0.5} - W_1\hat{\tau}_{ML-0.5}}{W_0 - W_1} - \hat{\tau}_{ML} \end{aligned} \tag{3-36}$$

The difference $\Delta\hat{\tau}_{ML}$ can be normalized to a single sample interval T_{SYM}/L, such that when the normalized $\Delta\hat{\tau}_{ML} = \Delta\hat{\tau}_{MLN}$ is positive (negative) the input signal sampling clock phase is advanced (retarded) by $\Delta\hat{\tau}_{MLN}$ fraction of the sampling clock period. The following expression for the normalized fractional difference was obtained by expanding w_0 and w_1 functions, and by noticing that $\hat{\tau}_{ML-0.5} = \hat{\tau}_{ML} - (2L)^{-1}$ and $\hat{\tau}_{ML+0.5} = \hat{\tau}_{ML+0.5} + (2L)^{-1}$,

$$\Delta\hat{\tau}_{MLN} = L\Delta\hat{\tau}_{ML} = \frac{\Lambda_L(\hat{\tau}_{ML-1}) - \Lambda_L(\hat{\tau}_{ML-1})}{4\Lambda_L(\hat{\tau}_{ML}) - 2\Lambda_L(\hat{\tau}_{ML-1}) - 2\Lambda_L(\hat{\tau}_{ML\ 1})} \tag{3-37}$$

As seen from equation (3-37), the proposed inverse interpolation technique requires 3 samples per symbols, and from complexity point of view it requires 3 additions and 1 divider functions.

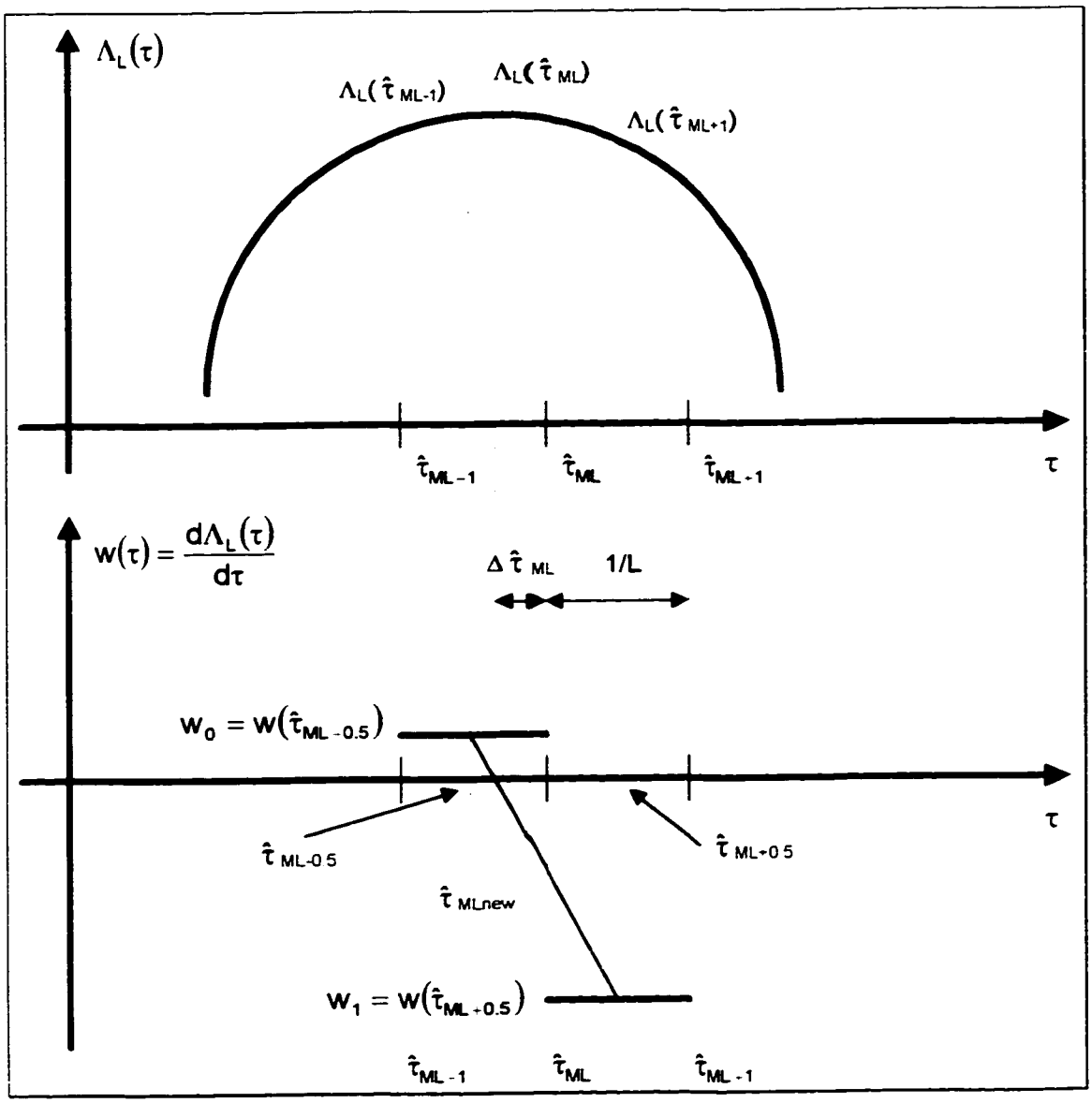

Figure 3—8. Inverse Interpolation Technique.

3.4.2. Maximum Timing Error Due Algorithm's Precision

The maximum timing error e_{MLnew} between the estimated $\hat{\tau}_{MLnew}$ and the true τ, normalized to T_{SYM}. is calculated for the case of the raised cosine pulse shaping, and noiseless signal. The general expression for the error is,

$$e_{MLnew} = \tau - \hat{\tau}_{MLnew} = \Delta\tau_{ML} - \Delta\hat{\tau}_{ML} \quad (3\text{-}38)$$

where:

$\Delta\tau_{ML} = \tau - \hat{\tau}_{ML}$ and for noiseless case its range is: $-(2L)^{-1} < \Delta\tau_{ML} < (2L)^{-1}$

Assuming raised cosine pulse shaping, noiseless signal, and utilizing equation (3-6) and (3-28), the log-likelihood function can be represented as,

$$\Lambda_L(\tau_i) = 2M\left|\cos((\tau_i - \tau)\pi)\right| \quad (3\text{-}39)$$

Substituting equation (3-37), and (3-39) into the timing error e_{MLnew}, the following expression is obtained,

$$e_{MLnew} = \frac{\left|\cos((\Delta\tau_{ML} - 1/L)\pi)\right| - \left|\cos((\Delta\tau_{ML} + 1/L)\pi)\right|}{L\left(4\left|\cos(\Delta\tau_{ML}\pi)\right| - 2\left|\cos((\Delta\tau_{ML} + 1/L)\pi)\right| - 2\left|\cos((\Delta\tau_{ML} - 1/L)\pi)\right|\right)} - \Delta\tau_{ML} \quad (3\text{-}40)$$

The above expression has been plotted as a function of $L\,\Delta\tau_{ML}$ in Figure 3—9, and as can be seen, the maximum error of the interpolating technique occurs at $L\,\Delta\tau_{ML} \cong \pm 0.29$. The maximum timing estimation error, for the case of noiseless signal, has been tabulated in Table 3—2 against different over-sampling ratios.

Table 3—2. Maximum Timing Estimation Error for Noiseless Signal.

L	3	4	8	16
max e_{ML}	±1.67E-1 T_{SYM}	±1.25E-1 T_{SYM}	±6.25E-2 T_{SYM}	±3.125E-2 T_{SYM}
max e_{MLnew}	±6.201E-3 T_{SYM}	±2.552E-3 T_{SYM}	±3.116E-4 T_{SYM}	±3.872E-5 T_{SYM}

From the results shown in Table 3—2, it is evident that the application of the presented interpolating technique, significantly reduces the timing estimation error. However, it should be noted that the above results were obtained with the assumption that the inverse interpolation algorithm is implemented with floating point precision. In discretized implementation, the error is expected to be larger, and thus a given implementation should be investigated for an optimum set of quantization parameters.

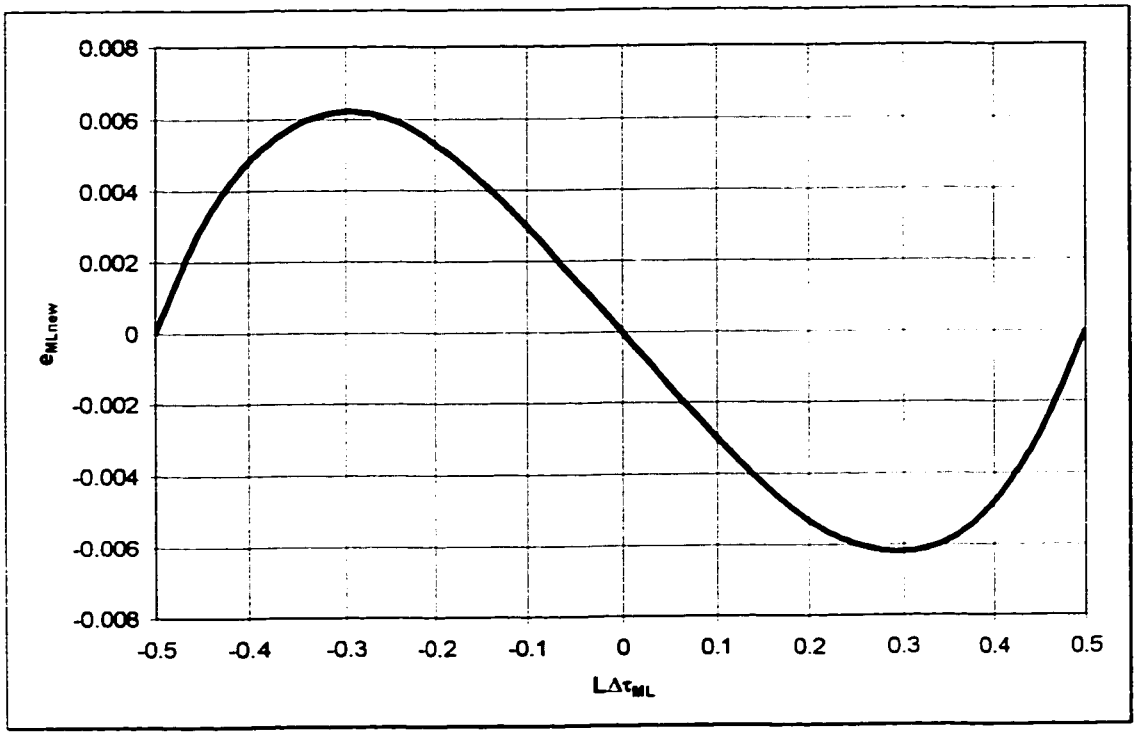

Figure 3—9. Timing Estimation Error for Noiseless Signal.

3.5. Mean of the Estimate

In this section it will be proven, by analytical derivations and by performed simulations, that the proposed symbol timing estimation is unbiased. The symbol timing offset τ is a nonrandom, but unknown parameter, and by definition the estimate of such parameter is said to be unbiased if the mean of the estimate is equal to the mean of the parameter being estimated [25].

$$E[\hat{\tau}] = \int_{-\infty}^{\infty} \hat{\tau} p(r|\tau) d\hat{\tau} = \int_{-\infty}^{\infty} \hat{\tau} \Lambda_L(\tau) d\hat{\tau} = \tau \tag{3-41}$$

Substituting equation (3-25) into equation (3-41) we obtain:

$$E[\hat{\tau}] = C_1 \int_{-\infty}^{\infty} \hat{\tau} \exp\left[-\frac{1}{2\sigma_{n_B}^2} \int_{T_o} |r(t) - y(t;\tau)|^2 dt \right] d\hat{\tau} \tag{3-42}$$

Solving equation (3-42) directly could be complicated, thus instead, an indirect prove, that equation (3-41) is satisfied, is followed. The alternative way of finding the expected value of the estimated timing phase is to: find the expected waveform shape at the output of I and Q receiver matched filters, then substitute these expected functions into the ML function $\Lambda_L(\tau)$, and finally to solve the following necessary condition for a maximum:

$$\left. \frac{\delta E[\Lambda_L(\tau)]}{\delta \tau} \right|_{\tau = E[t]} = 0 \tag{3-43}$$

As shown in Section 3.3, equation (3-6), during the STR preamble section, the output of the matched filter, for a raised cosine g(t) pulse shape, is:

$$z_I(t) = \pm \cos\left[\frac{\omega_{SYM}}{2} t - \tau\pi \right] + v_{nc}(t) \tag{3-44}$$

$$z_Q(t) = \pm \cos\left[\frac{\omega_{SYM}}{2} t - \tau\pi - \Delta\pi \right] + v_{ns}(t) \tag{3-45}$$

Since $E(v_{nc})=E(v_{ns})=0$, thus

$$E[z_I(t)] = \pm\cos\left[\frac{\omega_{SYM}}{2}t - \tau\pi\right] \tag{3-46}$$

$$E[z_Q(t)] = \pm\cos\left[\frac{\omega_{SYM}}{2}t - \tau\pi - \Delta\pi\right] \tag{3-47}$$

Substituting equations (3-46) and (3-47) into equation (3-28), the equation of the expected maximum likelihood waveform becomes:

$$\begin{aligned} E[\Lambda_L(\tau_i)] &= \sum_{k=1}^{M}\left(\left|\pm\cos[\pi(k+\tau_i-\tau)]\right| + \left|\pm\cos[\pi(k+\tau_i-\tau)]\right|\right) = \\ &= \sum_{k=1}^{M}\left(2\cos[\pi(k+\tau_i-\tau)]\right) = 2M\cos[\pi(\tau_i-\tau)] \end{aligned} \tag{3-48}$$

Since τ_i is the trial, and τ is the true timing offset with range $|\tau;\tau_i| \le 0.5$, thus

$$E[\Lambda_L(\tau_i)] = 2M\cos[\pi(\tau_i-\tau)] \quad \text{for} \quad -1 < (\tau_i-\tau) < 1 \tag{3-49}$$

Setting the derivative of the expected maximum likelihood function to zero,

$$\left.\frac{\delta E[\Lambda_L(\tau_i)]}{\delta\tau_i}\right|_{\tau_i = E[\hat{\tau}]} = -2M\pi\sin(\pi(\tau_i-\tau))\Big|_{\tau_i = E[\hat{\tau}]} = 0 \tag{3-50}$$

and solving for the expected symbol timing estimation parameter we obtain:

$$E[\hat{\tau}] = \tau \tag{3-51}$$

Thus, the expected symbol timing estimation parameter has been proved to be equal to the true timing offset.

In order to verify analytical derivations, an implementable symbol timing recovery model was created using Matlab computer program, and the sample mean of the absolute symbol timing error was simulated for different estimation window sizes and different signal to noise ratios. The obtained results (see Figure 3—10), for FF D-A STR from Section 2.3, show that the mean timing error approaches zero as the estimation window size, and signal to noise ratio increase.

When the interpolation timing correction technique was incorporated in the STR simulation model, the resulting mean symbol timing error decreased even further as shown in Figure 3—11. The analytical analysis in Section 3.4 showed that, for noiseless signal, the timing error decreases as the symbol over-sampling rate L increases. The computer simulations show, that for noisy input signal the timing error decreases as the symbol over-sampling rate L decreases. It is believed that the reason for such behavior is that when the samples are closer to each other, the absolute values of $\Delta\Lambda_L(\tau)$ are smaller, and thus the inverse interpolation technique becomes more sensitive to thermal noise. Note, the analytical verification is suggested for future research.

Both analytical derivation and simulation results generally agree with the unbiased estimator theory, thus it has been proven that the proposed estimator is unbiased.

The unbiased estimator property is very desirable in the estimators, since it guaranties that for a large number of observations the estimates are close to the true values. It also allows for a relatively simple derivation of a lower bound on the timing error variance, as will be shown in the following Section 3.6.

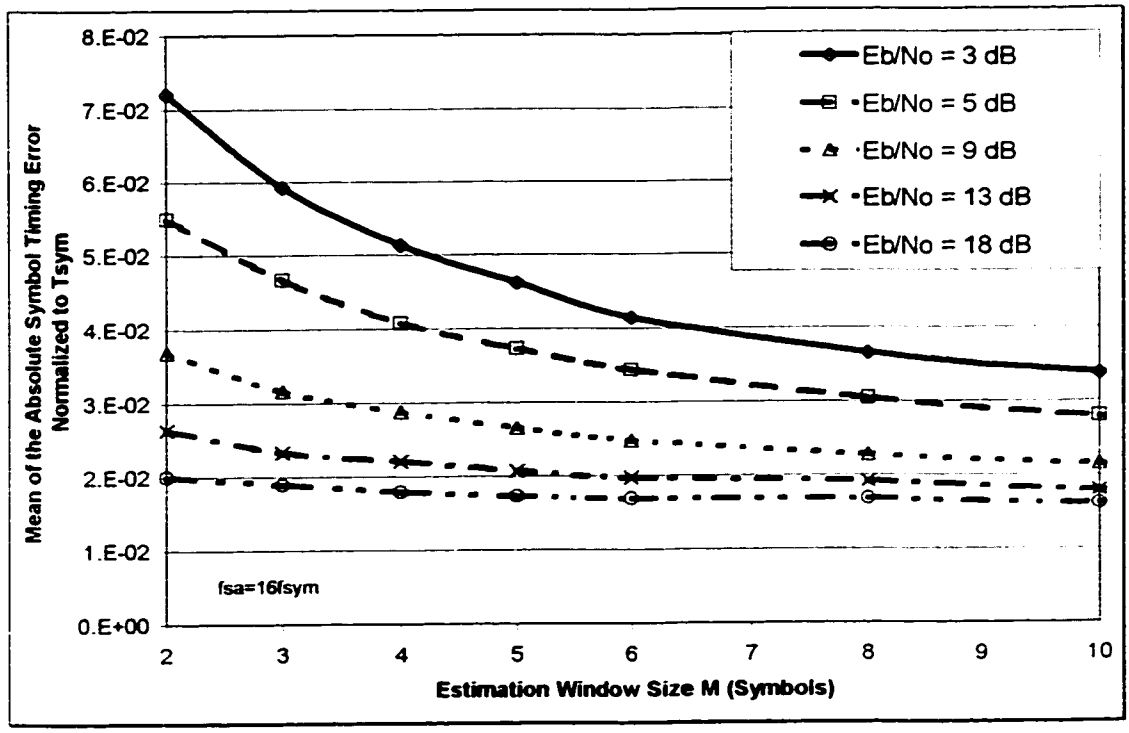

Figure 3—10. Sample Mean of the Absolute Symbol Timing Error (FF D-A STR from Section 3.3).

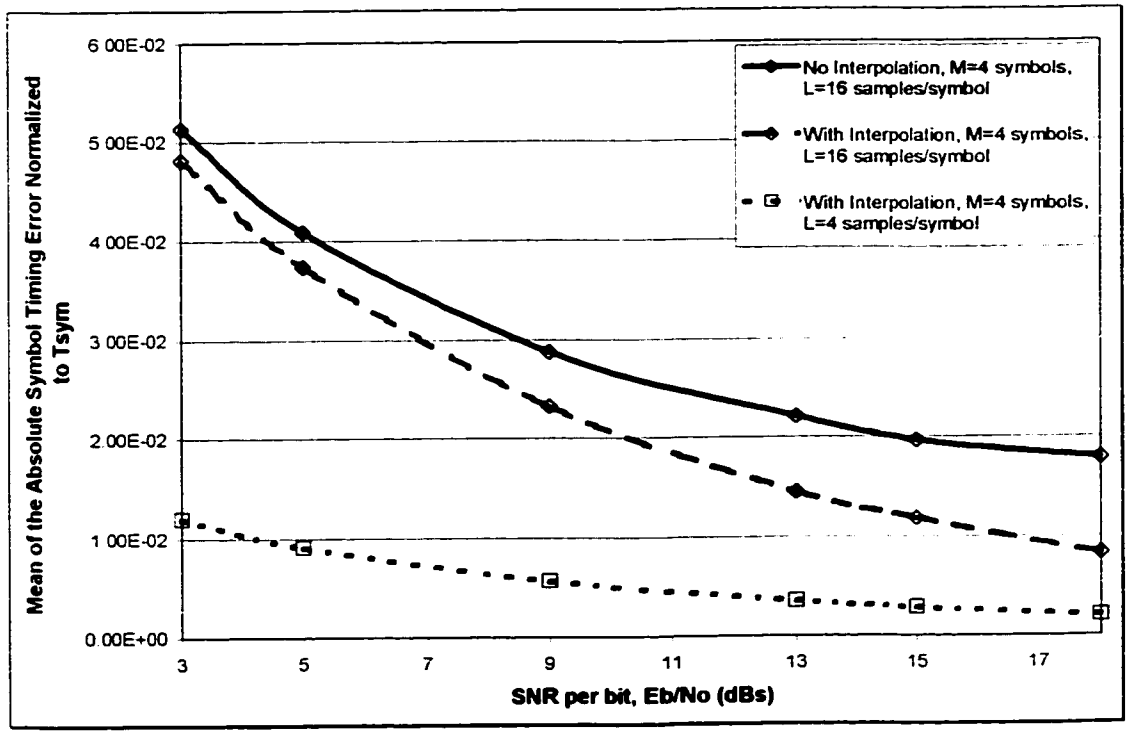

Figure 3—11. Effect of Symbol Timing Correction on Mean Symbol Timing Error.

3.6. Cramer-Rao Lower Bound on Variance

In the previous section it has been proven that on average the estimated symbol timing is equal to the true value, however, on per burst basis this "one shot" estimate most of the time is different from the exact true value. Ideally it is desirable to have these differences as small as possible. The performance measure of these variations about the true value is called the variance of the timing error. In this section a lower bound on the variance of the estimated symbol timing is derived. This bound will allow us to compare the variance of the proposed practical estimator to that of the theoretical optimum, and thus assess the implementation loss.

The lower bound on variance of any unbiased estimator can be found by applying the following theorem, which is proved by van Trees [26].

Theorem: Given that the estimate of τ (a nonrandom, but unknown parameter) is unbiased (see equation (3-41), Section 3.5), then:

$$\sigma_{\hat{\tau}}^2 = \mathrm{var}(\hat{\tau} - \tau) = E\left[(\hat{\tau} - \tau)^2\right] \geq \left\{ E\left\{ \left[\frac{\delta \ln p(\underline{r}|\tau)}{\delta \tau} \right]^2 \right\} \right\}^{-1} = -\left\{ E\left\{ \frac{\delta^2 \ln p(\underline{r}|\tau)}{\delta \tau^2} \right\} \right\}^{-1} \quad \textbf{(3-52)}$$

The above theorem for one dimensional estimator is called Cramer-Rao lower bound, and it is shown in [26] that if the lower bound is attained, then the estimate is an efficient estimate, and it must be a maximum likelihood estimate.

The log likelihood function, derived in equation (3-25), Section 3.3, is rewritten here in expanded form as:

$$\ln p(\underline{r}|\tau) = \Lambda_L(\tau) = -\frac{1}{2\sigma_{n_B}^2} \int_{T_o} \left(r_I^2 - 2r_I y_I + y_I^2 + r_Q^2 - 2r_Q y_Q + y_Q^2 \right) dt \quad \textbf{(3-53)}$$

where:

y is a function of time t, and trial symbol timing value τ_i

r is a function of time t

Taking the first partial derivative of the log likelihood function with respect to trial symbol timing parameter τ_i, we obtain:

$$\frac{\delta \Lambda_L(\tau_i)}{\delta \tau_i} = \frac{1}{{\sigma_{n_B}}^2} \int_{T_o} \left(r_I \frac{\delta y_I}{\delta \tau_i} - y_I \frac{\delta y_I}{\delta \tau_i} + r_Q \frac{\delta y_Q}{\delta \tau_i} + y_Q \frac{\delta y_Q}{\delta \tau_i} \right) dt \qquad \textbf{(3-54)}$$

Then taking the second partial derivative of the log likelihood function with respect to symbol timing parameter τ_i, we obtain:

$$\frac{\delta^2 \Lambda_L(\tau_i)}{\delta \tau_i^2} = \frac{1}{{\sigma_{n_B}}^2} \int_{T_o} \left(\begin{array}{l} r_I \dfrac{\delta^2 y_I}{\delta \tau_i^2} - \dfrac{\delta y_I}{\delta \tau_i} \dfrac{\delta y_I}{\delta \tau_i} - y_I \dfrac{\delta^2 y_I}{\delta \tau_i^2} + \\ + r_Q \dfrac{\delta^2 y_Q}{\delta \tau_i^2} - \dfrac{\delta y_Q}{\delta \tau_i} \dfrac{\delta y_Q}{\delta \tau_i} - y_Q \dfrac{\delta^2 y_Q}{\delta \tau_i^2} \end{array} \right) dt \qquad \textbf{(3-55)}$$

Rearranging the above expression we get,

$$\frac{\delta^2 \Lambda_L(\tau_i)}{\delta \tau_i^2} = \frac{1}{{\sigma_{n_B}}^2} \int_{T_o} \left[(r_I - y_I) \frac{\delta^2 y_I}{\delta \tau_i^2} - \left(\frac{\delta y_I}{\delta \tau_i} \right)^2 + (r_Q - y_Q) \frac{\delta^2 y_Q}{\delta \tau_i^2} - \left(\frac{\delta y_Q}{\delta \tau_i} \right)^2 \right] dt \qquad \textbf{(3-56)}$$

Noticing that the following expected values are zero:

$$E(r_I - y_I) = E(n_{Bc}) = 0 \quad \text{and} \quad E(r_Q - y_Q) = E(n_{Bs}) = 0 \qquad \textbf{(3-57)}$$

And evaluating the expected value of the second derivative of the log likelihood function, we obtain:

$$E\left[\frac{\delta^2\Lambda_L(\tau_i)}{\delta\tau_i^2}\right]=\frac{-1}{\sigma_{n_B}{}^2}\int_{T_o}E\left[\left(\frac{\delta y_I}{\delta\tau_i}\right)^2+\left(\frac{\delta y_Q}{\delta\tau_i}\right)^2\right]dt \qquad \textbf{(3-58)}$$

Expanding the above expression, using the equation (3-1), Section 3.3, we get:

$$E\left[\frac{\delta^2\Lambda_L(\tau_i)}{\delta\tau_i^2}\right]=\frac{-1}{\sigma_{n_B}{}^2}E\left[\int_{T_o}\left\{\begin{array}{c}\left(\sum_{k=-\infty}^{\infty}a_k\frac{\delta g_T(t-kT_{SYM}-\tau_iT_{SYM})}{\delta\tau_i}\right)^2+\\ +\left(\sum_{k=-\infty}^{\infty}b_k\frac{\delta g_T(t-kT_{SYM}-\tau_iT_{SYM}-\Delta T_{SYM})}{\delta\tau_i}\right)^2\end{array}\right\}dt\right] \qquad \textbf{(3-59)}$$

Since $E[a_ka_l]=E[b_kb_l]=0$ for all $k\neq l$, and $E[a_k^2]=E[b_k^2]=1$ then

$$E\left[\frac{\delta^2\Lambda_L(\tau_i)}{\delta\tau_i^2}\right]=\frac{-1}{\sigma_{n_B}{}^2}\int_{T_o}\left\{\begin{array}{c}\sum_{k=-\infty}^{\infty}\left(\frac{\delta g_T(t-kT_{SYM}-\tau_iT_{SYM})}{\delta\tau_i}\right)^2+\\ +\sum_{k=-\infty}^{\infty}\left(\frac{\delta g_T(t-kT_{SYM}-\tau_iT_{SYM}-\Delta T_{SYM})}{\delta\tau_i}\right)^2\end{array}\right\}dt \qquad \textbf{(3-60)}$$

For implementation purposes we replace infinite "k" summation with finite summation from m=1 to m=M (where: MT_{SYM} = observation time T_o), and we replace the finite integration with infinite integration, thus the equation (3-60) can be rewritten as:

$$E\left[\frac{\delta^2\Lambda_L(\tau_i)}{\delta\tau_i^2}\right]=\frac{-1}{\sigma_{n_B}{}^2}\sum_{m=1}^{M}\left\{\begin{array}{c}\int_{-\infty}^{\infty}\left(\frac{\delta g_T(t-mT_{SYM}-\tau_iT_{SYM})}{\delta\tau_i}\right)^2dt+\\ +\int_{-\infty}^{\infty}\left(\frac{\delta g_T(t-mT_{SYM}-\tau_iT_{SYM}-\Delta T_{SYM})}{\delta\tau_i}\right)^2dt\end{array}\right\} \qquad \textbf{(3-61)}$$

In order to transform the above equation into the frequency domain, a series of manipulations, including a change of variables is followed:

$$u=t-mT_{SYM}-\tau_i T_{SYM} \rightarrow du/d\tau_i=-T_{SYM} \qquad v=t-mT_{SYM}-\tau_i T_{SYM}-\Delta T_{SYM} \rightarrow dv/d\tau_i=-T_{SYM}$$

$$E\left[\frac{\delta^2\Lambda_L(\tau_i)}{\delta\tau_i^2}\right]=\frac{T_{SYM}^2}{\sigma_{n_B}^{\ 2}}\sum_{m=1}^{M}\left\{\int_{-\infty}^{\infty}\left(\frac{\delta g_T(u)}{\delta u}\right)^2 dt+\int_{-\infty}^{\infty}\left(\frac{\delta g_T(v)}{\delta v}\right)^2 dt\right\} \tag{3-62}$$

Now, we define new functions: $f(u)=dg_T(u)/du$ and $f(v)=dg_T(v)/dv$, and substituting back for $u=t-mT_{SYM}-\tau_i T_{SYM}$ and $v=t-mT_{SYM}-\tau_i T_{SYM}-\Delta T_{SYM}$, we get:

$$E\left[\frac{\delta^2\Lambda_L(\tau_i)}{\delta\tau_i^2}\right]=\frac{T_{SYM}^2}{\sigma_{n_B}^{\ 2}}\sum_{m=1}^{M}\left\{\begin{array}{l}\int_{-\infty}^{\infty}f^2(t-mT_{SYM}-\tau_i T_{SYM})dt+\\ +\int_{-\infty}^{\infty}f^2(t-mT_{SYM}-\tau_i T_{SYM}-\Delta T_{SYM})dt\end{array}\right\} \tag{3-63}$$

Changing the variables again:

$$s=t-mT_{SYM}-\tau_i T_{SYM} \rightarrow ds/dt=1 \quad \text{and} \quad w=t-mT_{SYM}-\tau_i T_{SYM}-\Delta T_{SYM}, \rightarrow dw/dt=1$$

We get:

$$E\left[\frac{\delta^2\Lambda_L(\tau_i)}{\delta\tau_i^2}\right]=\frac{T_{SYM}^2}{\sigma_{n_B}^{\ 2}}\sum_{m=1}^{M}\left\{\int_{-\infty}^{\infty}f^2(s)ds+\int_{-\infty}^{\infty}f^2(w)dw\right\} \tag{3-64}$$

Now, we can apply the following Parseval's relation for energy signals, to the above equation,

$$\text{Energy of } f(s) = \int_{-\infty}^{\infty} |f(s)|^2 \, ds = \frac{1}{2\pi} \int_{-\infty}^{\infty} |F(\omega)|^2 \, d\omega \tag{3-65}$$

where:

$$f(s) = \frac{dg_T(s)}{ds} \text{ and } |f(s)|^2 = \left(\frac{dg_T(s)}{ds} \right)^2 \tag{3-66}$$

since $g_T(t)$ is assumed to be a real function.

Thus
$$F(\omega) = j\omega G_T(\omega) \tag{3-67}$$

where: $G_T(\omega)$ is the Fourier Transform of $g_T(s)$

Finally, the expected second derivative of the log likelihood function in frequency domain is represented as:

$$E\left[\frac{\delta^2 \Lambda_L(\tau_i)}{\delta \tau_i^2} \right] = \frac{-2MT_{SYM}^2}{\sigma_{n_B}^{\ 2}} \frac{1}{2\pi} \int_{-\infty}^{\infty} \omega^2 |G_T(\omega)|^2 \, d\omega \tag{3-68}$$

Expanding the variance term using equation (A-15), Appendix A, we get the final expression:

$$E\left[\frac{\delta^2 \Lambda_L(\tau_i)}{\delta \tau_i^2} \right] = \frac{-8E_b MT_{SYM}^2}{N_o} \frac{1}{2\pi} \int_{-\infty}^{\infty} \omega^2 |G_T(\omega)|^2 \, d\omega \tag{3-69}$$

And thus the Cramer-Rao lower bound on symbol timing variance, normalized to symbol period, is:

$$\sigma_{\hat{\tau}}^2 = E\left[\left(\frac{\hat{\tau}-\tau}{T_{SYM}}\right)^2\right] \geq -\left\{E\left\{\frac{\delta^2 \Lambda_L(\tau_i)}{\delta \tau_i^2}\right\}\right\}^{-1} = \frac{N_o}{E_b}\frac{1}{8M}\frac{1}{\frac{T_{SYM}^2}{2\pi}\int_{-\infty}^{\infty}\omega^2 |G_T(\omega)|^2 d\omega} \quad \textbf{(3-70)}$$

Since:

$$G_R(\omega) = G_T^*(\omega)e^{-j\omega T_o} \quad \textbf{(3-71)}$$

And since functions $G_R()$ and $G_T()$ are real, thus:

$$|G_R(\omega)| = |G_T(\omega)| \quad \textbf{(3-72)}$$

The CRLB expression can be re-written as:

$$\sigma_{\hat{\tau}}^2 = \text{var}\left(\frac{\hat{\tau}-\tau}{T_{SYM}}\right) = E\left[\left(\frac{\hat{\tau}-\tau}{T_{SYM}}\right)^2\right] \geq \frac{N_o}{E_b}\frac{1}{8M}\frac{2\pi}{T_{SYM}^2\int_{-\infty}^{\infty}\omega^2 |G_R(\omega)|^2 d\omega} \quad \textbf{(3-73)}$$

where:

E_b/N_o is the signal-to-noise ratio at the input to the receiver,

M is the length of the estimation window in symbols,

$G_R(\omega)$ is the frequency response of the receiver matched filter

The derived CRLB on symbol timing variance, presented in equation (3-73) has the following properties:

- it is inversely proportional to the signal-to-noise ratio and the estimation window size,
- it is strongly dependent on the pulse shaping function $g_R(t)$ used in the system.

In analytical derivations and in simulations a raised cosine (RC) pulse shaping function was used, since it is a zero ISI Nyquist pulse shape, and it is easier to mathematically manipulate. When a RC pulse shaping function is assumed, the equation for CRLB on symbol timing variance becomes:

$$\sigma_{\hat{\tau}}^2 = \mathrm{var}\left(\frac{\hat{\tau}-\tau}{T_{SYM}}\right) = E\left[\left(\frac{\hat{\tau}-\tau}{T_{SYM}}\right)^2\right] \geq \frac{N_o}{E_b}\frac{1}{8M}\frac{1}{-8\alpha^2+\frac{\pi^2}{3}+\pi^2\alpha^2} \qquad \textbf{(3-74)}$$

A very similar function of CRLB on symbol timing variance is presented by Georghiades [19] for pulse amplitude modulation signal (PAM). Equation (3-74) reveals that as the roll-off factor α increases from 0 to 1, the variance of the estimated symbol timing decreases. However, higher roll-off factor increases the required transmission bandwidth, thus as a compromise between the bandwidth requirement and the variance of the estimate, it is suggested to choose a roll-off factor α=0.5.

The derived CRLB on symbol timing variance function for RC with roll-off factor α=0.5, equation (3-74), was plotted as a function of signal-to-noise ratio for different estimation window sizes in Figure 3—12.

As shown in Figure 3—12, the CRLB on variance of symbol timing estimate decreases as M and E_b/N_o increase. These curves will be used in the following sections for comparison with simulation results, and to determine how much implementation loss the proposed practical implementations have, and based on those results an optimum design will be selected.

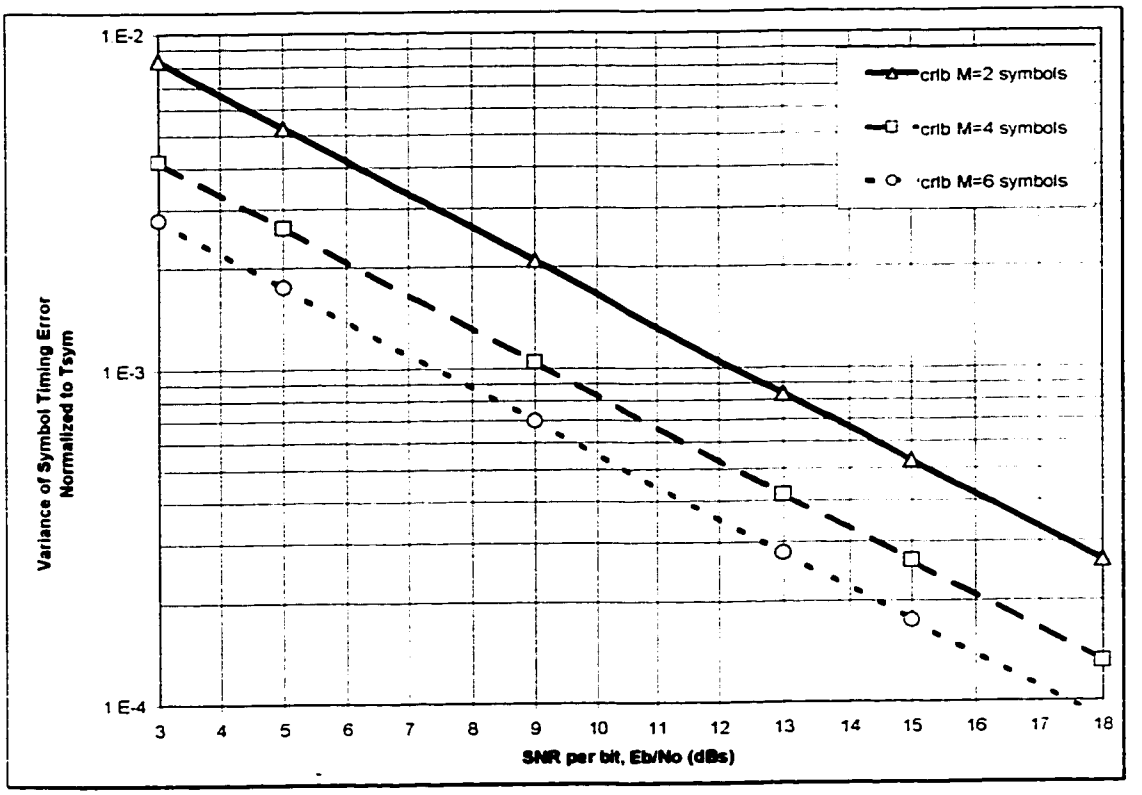

Figure 3—12. CRLB on Symbol Timing Variance for RC with α=0.5.

3.7. Modified CRLB on Variance

In Section 3.6, the CRLB on timing variance has been derived with the assumption that the trial timing parameter τ_i is a continuous signal (i.e. not discretized). However, the STR algorithms presented in this chapter explicitly use the discretized trial timing parameter for the maximum eye opening estimation, thus in this section the CRLB is modified to include the effects of the implementation technique.

The main assumption to develop a modified CRLB is that the performance degradations resulting from the signal's additive noise and the STR implementation technique are independent from each other. Thus in general the modified CRLB can be written as:

$$CRLB_{MOD} = CRLB + var_{IMP} \tag{3-75}$$

where:

var_{IMP} is the lower limit on the symbol timing variance due to implementation technique.

3.7.1. FF D-A STR (no interpolation correction)

As mentioned in Section 3.3, the timing error due to trial timing parameter discretization is in range of $\pm T_{SYM}/(2L)$. This error is assumed to be the same throughout the whole burst, however, from one burst to another its value will be random. The probability density function (pdf) of discretization error is assumed to be uniform in interval $[-(2L)^{-1}, (2L)^{-1}]T_{SYM}$, therefore the mean of the discretization error is zero, and the variance is $T^2_{SYM}/(12L^2)$. This term is the lower limit on symbol timing variance, and normalized to T_{SYM} can be written as:

$$var_{IMP\,(NO\ INTERPOLATION)} = \frac{1}{12L^2} \tag{3-76}$$

3.7.2. FF D-A STR (with interpolation correction)

The lower limit on variance of timing error, resulting from the FF D-A STR with inverse interpolation algorithm, is defined as:

$$var_{IMP\,(WITH\ INTERP)} = var(e_{MLnew}) = \int_{-\infty}^{\infty} e^2_{MLnew}(\Delta\tau_{ML}) \cdot f_{\Delta\tau_{ML}}(\Delta\tau_{ML})\, d\Delta\tau_{ML} \tag{3-77}$$

where:

$f_{\Delta\tau_{ML}}(\Delta\tau_{ML})$: is the probability density function of a uniformly distributed random variable $\Delta\tau_{ML}$

$$f_{\Delta\tau_{ML}}(\Delta\tau_{ML}) = L \text{ for } -\frac{1}{2L} < \Delta\tau_{ML} < \frac{1}{2L} \tag{3-78}$$

thus,

$$var_{IMP(WITH\ INTERP)} = var(e_{MLnew}) = L\int_{-1/(2L)}^{1/(2L)} e_{MLnew}^2(\Delta\tau_{ML})d\Delta\tau_{ML} \quad (3\text{-}79)$$

The expression for the variance of timing estimation error e_{MLnew} has been evaluated for different over-sampling ratios, and was compared with the variance of timing estimation error e_{ML} (i.e. without interpolation technique). The results have been tabulated in Table 3—3.

Table 3—3. The Variance of the Timing Estimation Error e_{MLnew} and e_{ML}.

L	3	4	8	16
$var_{IMP(NO\ INTERP)}$	9.26E-3	5.21E-3	1.30E-3	3.26E-4
$var_{IMP(WITH\ INTERP)}$	1.98E-5	3.35E-6	4.99E-8	7.71E-10

As shown in Table 3—3 the variance of timing error due interpolation algorithm is very small even for low over-sampling values.

The modified CRLB has been compared with a general CRLB for different implementation choices in Figure 3—13. It is shown in this figure that:

- The performance of the FF D-A STR with interpolation correction technique (for practical range of SNR), follows the CRLB very closely, even for low over-sampling rates.
- However, the performance of the FF D-A STR without interpolation correction technique is only acceptable at high over-sampling rates $L \geq 16$ (as will be further explained in Section 3.10).

It should be noted, that floating point implementation was assumed for the interpolation technique, and thus the performance of the practical implementation should be further investigated.

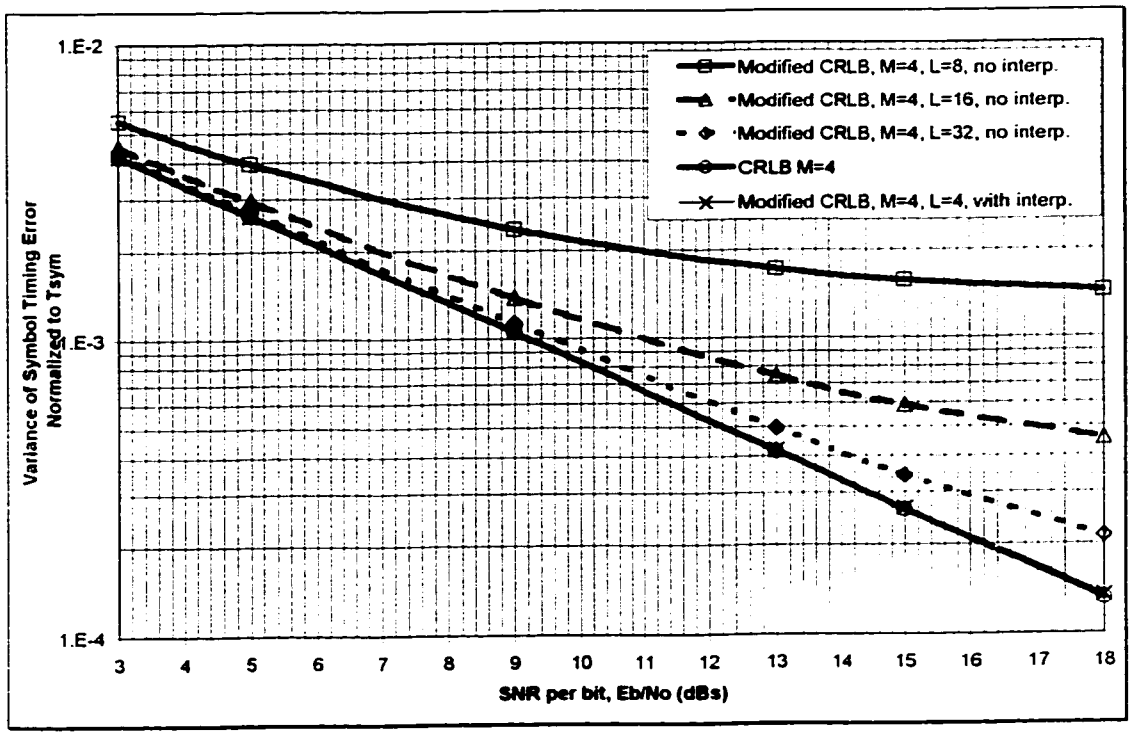

Figure 3—13. Modified CRLB on Variance of Symbol Timing Error, M=4 symbols.

3.8. Variance of the Symbol Timing Estimate

In this section it is shown (with a help of performed simulations), that the variance of the proposed symbol timing estimator, is close to the optimum value determined by the CRLB (for FF D-A STR with interpolation correction technique), and close to the optimum value determined by the Modified CRLB (for FF D-A STR without the interpolation correction technique).

The general expression for the variance of the symbol timing estimate is defined as [12]:

$$\sigma_t^2 = E\left(\left[\hat{\tau}(r)\right]^2\right) - \left(E\left[\hat{\tau}(r)\right]\right)^2 \qquad \textbf{(3-80)}$$

In general, for the practical estimators, the variance is difficult to compute using the above equation, either because the expression of the estimate is very complex, nonlinear or, as in our

case, a closed form equation for $\hat{\tau}$ does not even exists. Meyr suggests [8, Chapter 6.3], the variance of the timing estimate can be also computed, by indirect approach, based only on the objective function, $\Lambda_L(\tau)$ as shown below:

$$\sigma_{\hat{\tau}}^2 = \mathrm{var}[\hat{\tau} - \tau] = \frac{E\left((\Lambda_L'(\tau))^2\right)}{\left(E[\Lambda_L''(\tau)]\right)^2} \tag{3-81}$$

The main assumption of this alternative approach is, that under normal operating conditions, the estimate of symbol timing is close to the true symbol timing value.

Assuming that the training sequence is transmitted continuously, and that the pulse shaping is done with a RC 0.5 roll-off factor function, the objective function $\Lambda_L(\tau)$ can be expanded to (see Appendix B):

$$\Lambda_L(\tau_i) = \sum_{m=1}^{M} \left\{ \begin{array}{l} \sqrt{\left[\cos(\pi(\tau_i - \tau - m)) + v_{n_{Bc}}(T_{SYM}(m + \tau_i))\right]^2} + \\ + \sqrt{\left[\cos(\pi(\tau_i - \tau - m)) + v_{n_{Bs}}(T_{SYM}(m + \tau_i + \Delta))\right]^2} \end{array} \right\} \tag{3-82}$$

Finding the derivatives of equation (3-82) and solving equation (3-81) for variance in symbolic form is still fairly complicated, and will not even reflect the discretization effect of the trial symbol timing. Thus, these analytical derivations will not be carried out in this thesis, and instead only the variance simulation results will be used for comparison with CRLB, and for assessing the implementation loss. This option for finding the variance is often preferred in practice, because of simplicity and accurate results, which take into account the nonlinear effects, such as discretization [8, Chapter 1.4].

The sample variance of the symbol timing error, for STR without interpolation correction technique, was simulated for different estimation window sizes, and different signal to noise

ratios. The obtained results are shown in Figure 3—14. As the estimation window size, and SNR increase, the variance of the timing error decreases, these simulation results agree with the general theory, and the numerical results are very close to the modified CRLB curves.

The simulation results presented in Figure 3—15 show, that for the FF D-A STR without interpolation correction technique, the variance curve of the practical estimator approaches the CRLB curve only when the over-sampling rate is relatively high. This behavior agrees with the theoretical analysis from Section 3.7, and the numerical results are close to modified CRLB curves.

If the desired variance is very low, and resulting value of L (for the basic FF D-A STR) is too high, for a given hardware implementation, an alternative is to use the proposed FF D-A STR with interpolation correction technique. As shown in Figure 3—15 the simulated variance is much closer to CRLB, and does not flatten out until very high SNRs (>>18dBs). The reason for falling below CRLB (Interpolation Technique with L=4) was not determined, however, one possible reason is an over simplified Matlab model. Other examples of STR with interpolation can found in [19], [20], and [21].

The implementation loss, in terms of bit error degradation, is determined based on the simulated symbol timing variance results, in Section 3.10.

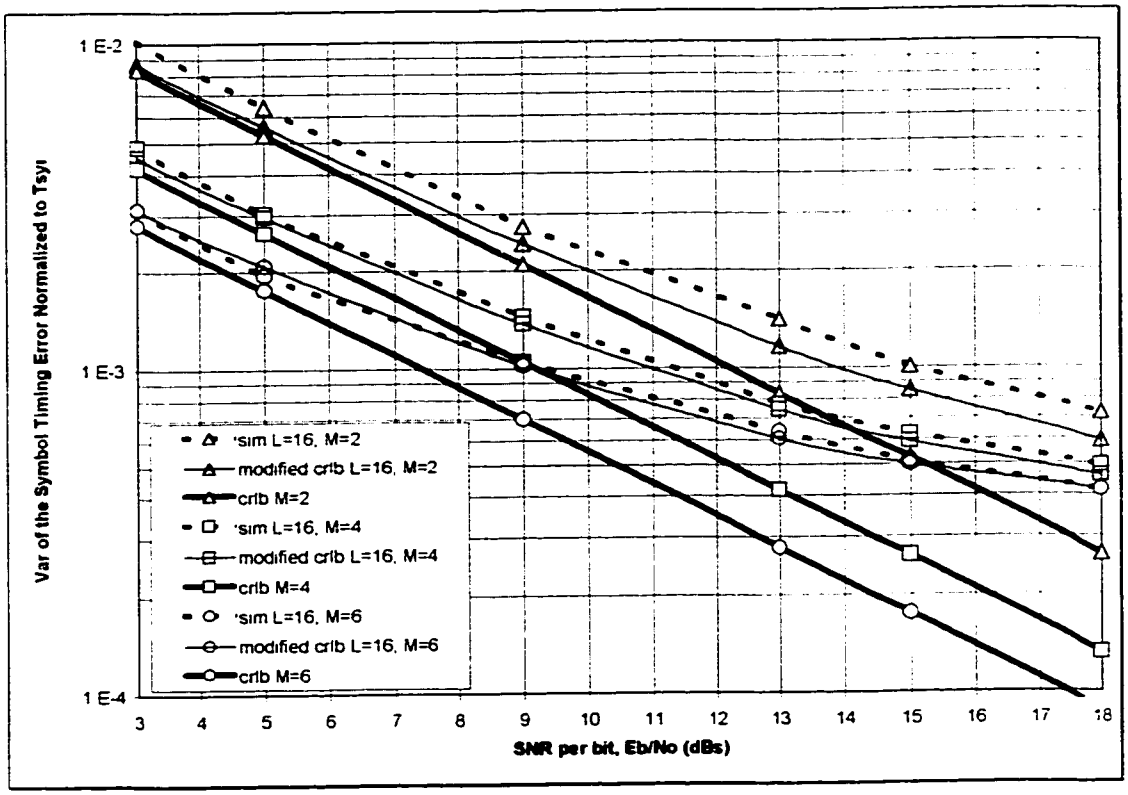

Figure 3—14. Variance of Symbol Timing Error for Different Estimation Window Sizes.

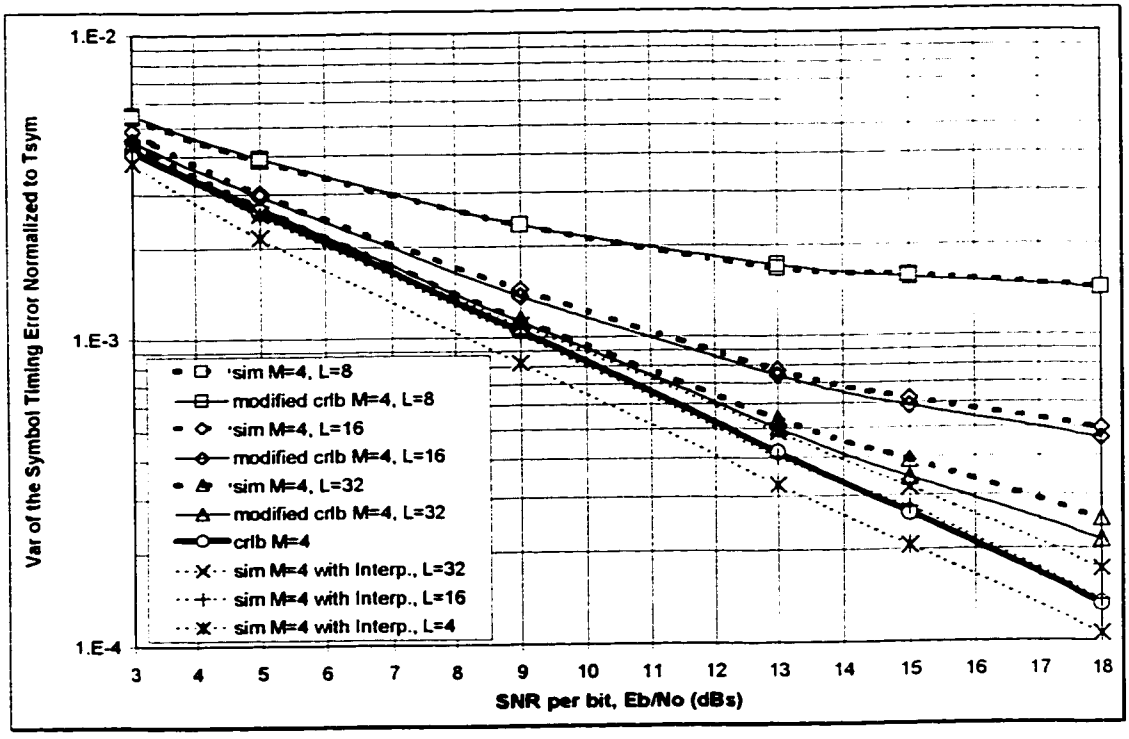

Figure 3—15. Variance of Symbol Timing Error for Different Over-Sampling Rates.

3.9. Jitter and Phase Noise

The symbol timing recovery, discussed in this chapter, is a "One shot" estimator type. Thus, as explained in the previous sections, it estimates the timing parameter in feedforward mode only during a short preamble at the beginning of the bursts, and then it uses that estimated value to detect the data during the rest of the burst duration. Since this symbol timing recovery is completely digital (i.e. after receiver's matched filters), the estimated timing value is stored in the memory, and never changes during a given burst, thus theoretically, there should be no jitter or self-noise, in the recovered symbol clock during the user's data section of the burst. In a practical situation the recovered symbol clock in a given burst, might have a small jitter, which is only due to the jitter of the system clock itself, however, if a good quality system clock is used then this introduced jitter is insignificant. In order to verify the "zero jitter" feature of the proposed symbol timing recovery, the jitter generation and the phase noise measurements were performed, with reference to the system clock. Before presenting the results of these measurements some definitions of the jitter and phase noise (based on HP application notes [27], [28], [29], [30] and [31]) are given in the following paragraphs.

ITU-T G.701 defines jitter as short-term non-cumulative variations of the rising or falling edge positions of a digital signal from their ideal positions in time. Jitter amplitude is often measured in unit intervals (UI), where 1 UI is the phase deviation of one clock period. The peak-to-peak UI deviation of the phase function with respect to time is referred to as the jitter amplitude [28]. An illustration of this definition is presented in Figure 3—16.

"Jitter generation measurement determines the amount of jitter a component or system adds to an input data signal" [27]. One of the techniques to perform jitter measurements is to use an oscilloscope with two inputs: the jitter free system clock (as a trigger reference) and the recovered symbol clock. This technique is easiest to setup in most laboratories, however, it has the following limitations:

- poor measurement sensitivity, because of the inherently high noise level, due to the large measurement bandwidth involved, and
- the technique does not provide any information about the jitter spectral characteristics or time domain waveform.

The other techniques require dedicated jitter measurement equipment, or special hardware, thus often an equivalent frequency domain measurement called "phase noise measurement" is performed in addition to simple jitter measurement.

"Phase noise is defined as a statistical distribution describing short-term frequency random fluctuations and is usually measured and presented as a spectral density plot of the modulation sidebands in the frequency domain. The amplitude of the sidebands is expressed in terms of energy within a specified bandwidth, normally a one hertz bandwidth (dBc/Hz)" [31]. Larger sidebands in frequency domain translate to more severe jitter in time domain. This phase noise definition is based on two assumptions: sideband energy due to amplitude modulation is much less than due to phase modulation, and the total phase deviations are less than one radian.

As shown in Figure 3—17 the jitter generation measurement, using oscilloscope technique, reveled no noticeable jitter (Trace 1 is the system sampling clock and Trace 2 is the recovered symbol timing strobe). The measured phase noise of the receiver symbol clock was approximately -105 dBc/Hz at 10 kHz offset from the center frequency (see Figure 3—18). The phase noise of the system clock was almost the same (-103 dBc/Hz), these values are extremely low, thus practically the implemented symbol timing synchronizer did not introduce any phase noise or jitter. The specified noise sidebands for the spectrum analyzer were <-100 dBc/Hz at 10 kHz, which can be accounted for small differences (-103 and -105.29 dBc/Hz) between the measurements.

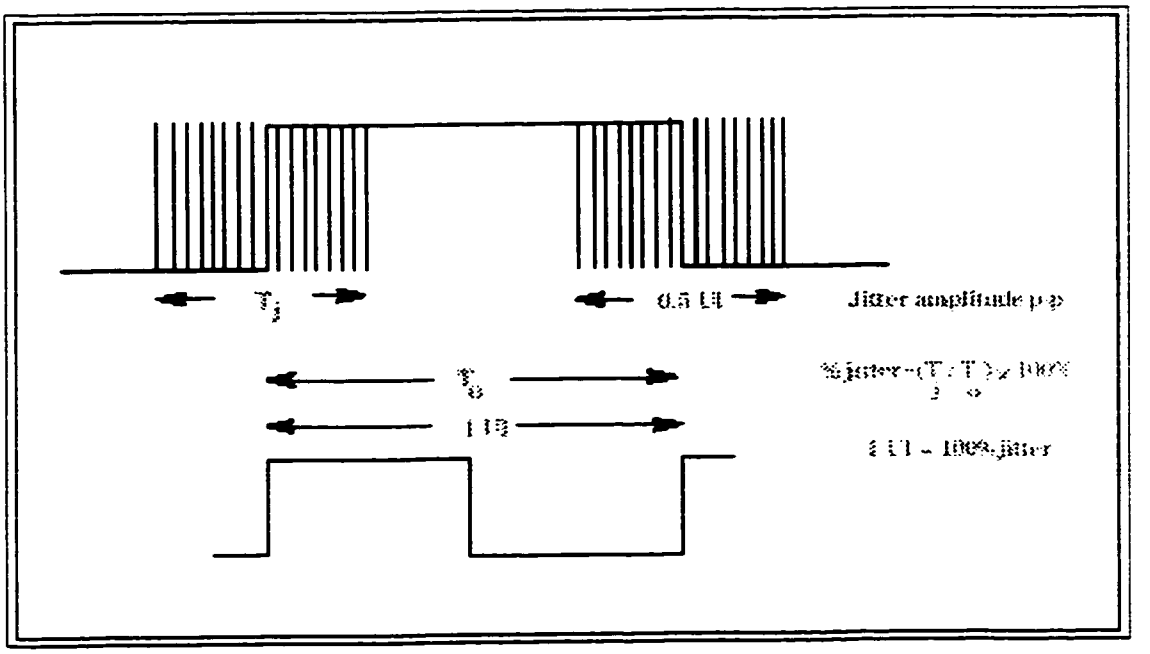

Figure 3—16 Definition of Unit Interval and Jitter [28].

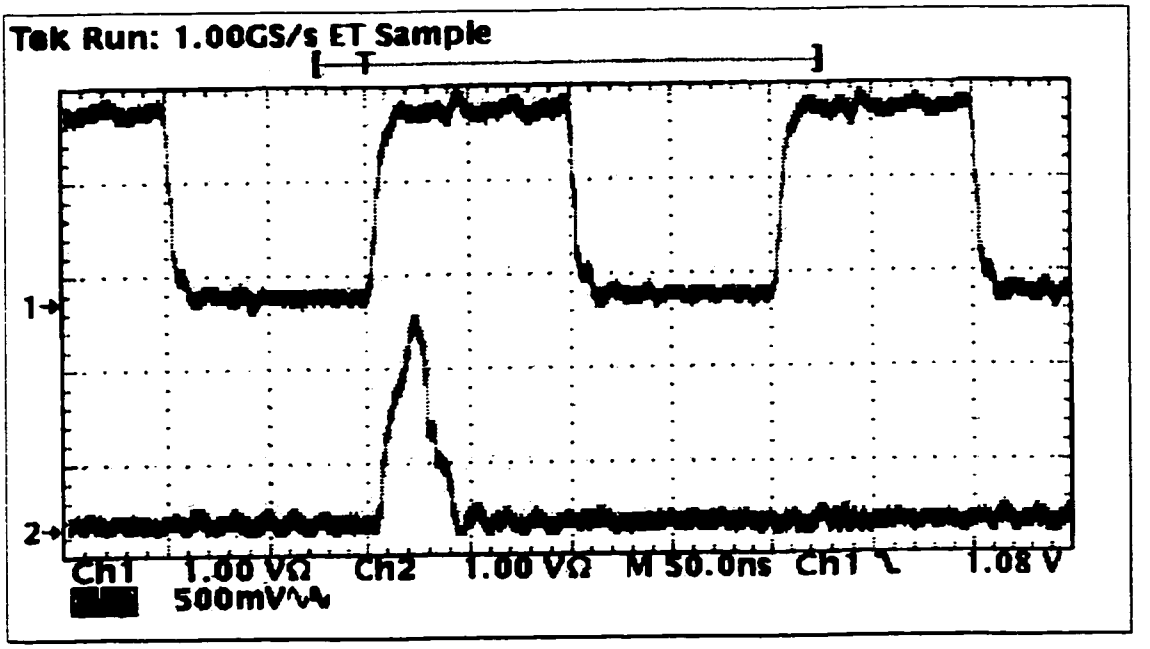

Figure 3—17. Jitter Generation Measurement of the Receiver Symbol Clock.

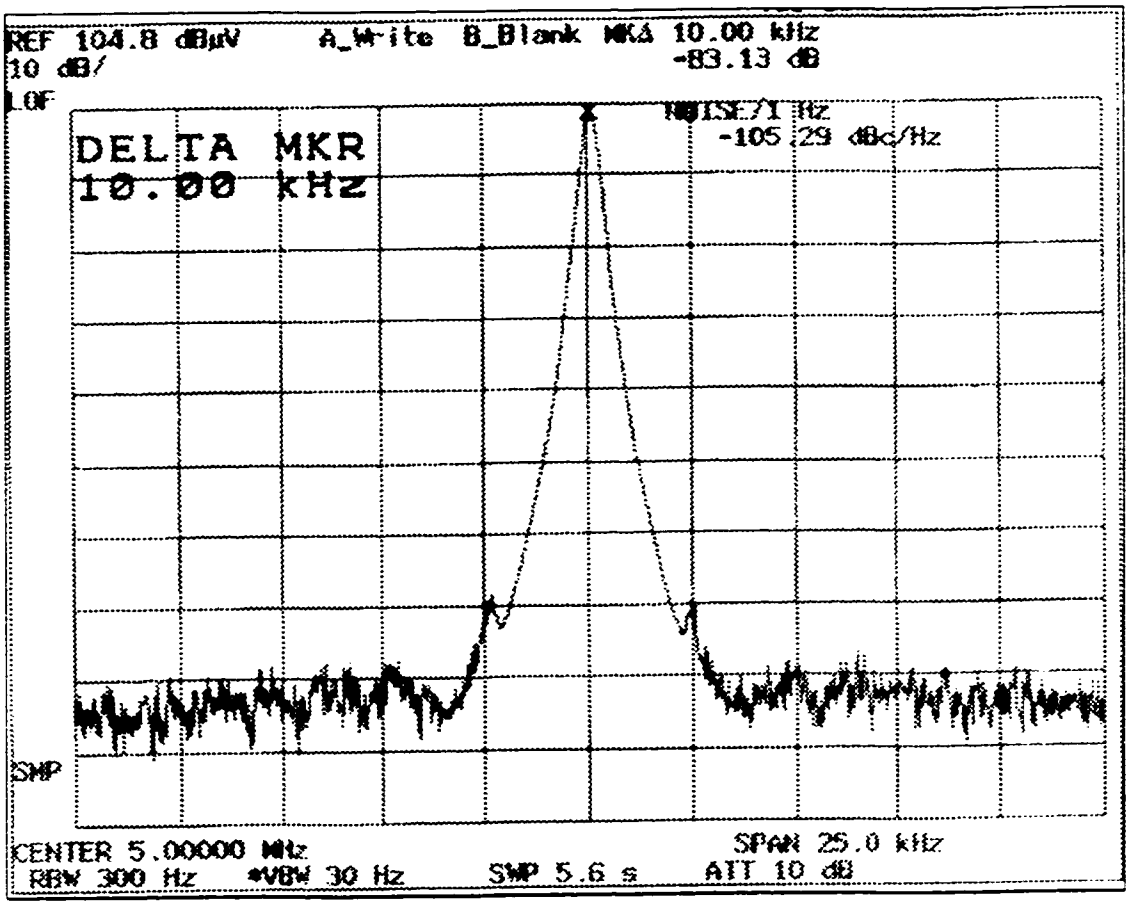

Figure 3—18. Phase Noise Measurement of the Receiver Symbol Clock.

3.10. Effects of STR Quality on Channel Bit Error Rate Performance

In this section, using an expression for the bit error rate (BER) degradation caused by timing synchronization errors, we quantify and present the implementation loss of the proposed symbol timing recovery technique. The BER degradation is defined as the increase of signal to noise ratio E_b/N_o, required to maintain the same BER as the receiver without synchronization errors [8, Chapter 7.3].

The BER performance for variety of modulation schemes, with assumption of perfect synchronization, has been widely documented [12], [3]. For QPSK, OQPSK and 4-QAM, modulation schemes, with perfect synchronization, the probability of symbol error is defined as:

$$P_S = 2Q\left(\sqrt{\frac{2E_b}{N_o}}\right) - \frac{3}{2}Q\left(\sqrt{\frac{2E_b}{N_o}}\right) = \text{erfc}\left(\sqrt{\frac{E_b}{N_o}}\right) - \frac{3}{4}\text{erfc}\left(\sqrt{\frac{E_b}{N_o}}\right) \cong \text{erfc}\left(\sqrt{\frac{E_b}{N_o}}\right) \quad \textbf{(3-83)}$$

where:

Q() and erfc() are the Q-function and complementary error function respectively, and

E_b/N_o is the signal to noise ratio at the input of the receiver.

Assuming that the symbol constellation is Gray-encoded, and that most of the symbol errors are the "nearest neighbor" errors, such that one symbol error corresponds to one bit error, then the bit error rate for QPSK, OQPSK and 4-QAM are defined as:

$$\text{BER} = P_b = \frac{1}{2}P_S \cong \frac{1}{2}\text{erfc}\left(\sqrt{\frac{E_b}{N_o}}\right) \quad \textbf{(3-84)}$$

Similarly as in Chapter 2.7, here we present BER degradation (measured in dB), as a function of symbol timing error variance, for QPSK, OQPSK and for square (i.e. 4 or 16) QAM modulations [8, Chapter 7]:

$$D(\text{dB}) \cong 4.34\left\{-g''(0)T_{SYM}{}^2 + \frac{E_S}{N_o}\sum_k [g'(kT_{SYM})T_{SYM}{}^2]\right\}\text{var}(\hat{\tau} - \tau) \quad \textbf{(3-85)}$$

where:

- E_S/N_o is the value of the signal to noise ratio yielding the required BER in the case of no synchronization errors, for QPSK, OQPSK and 4-QAM $E_S=2E_b$

With the assumption of raised cosine (RC) pulse shape, with the roll-off factor of 0.5, the BER degradation due to timing error variance equation reduces to:

$$D \cong 4.34\left\{3.757 + 1.29\frac{E_s}{N_o}\right\}\mathrm{var}(\hat{\tau} - \tau) \qquad \textbf{(3-86)}$$

The above equation, has been used to tabulate (see Table 3—4 and Table 3—5) the amount of BER degradation for different implementation cases of the symbol timing synchronizer studied in Section 3.8 , Figure 3-14 and Figure 3-15.

Table 3—4. BER Degradation for Different Over-sampling Implementation Cases, M=4 symbols (QPSK, OQPSK, 4-QAM).

BER_o	E_b/N_o	CRLB		L=32		L=16		L=8	
	(dB)	var(τ)	D(dB)	var(τ)	D(dB)	var(τ)	D(dB)	var(τ)	D(dB)
1E-4	8.40	1.2E-3	0.111	1.4E-3	0.130	1.7E-3	0.158	2.6E-3	0.241
1E-6	10.53	7.5E-4	0.106	9.0E-4	0.127	1.2E-3	0.170	2.1E-3	0.297
1E-8	11.97	5.5E-4	0.105	7.0E-4	0.133	9.5E-4	0.181	1.9E-3	0.353

Table 3—5. BER Degradation for Different Estimation Window Size Implementation Cases, L=16 (QPSK, OQPSK, 4-QAM).

BER_o	E_b/N_o	M=2 symbols		M=3 symbols		M=4 symbols		M=6 symbols	
	(dB)	var(τ)	D(dB)	var(τ)	D(dB)	var(τ)	D(dB)	var(τ)	D(dB)
1E-4	8.40	3.3E-3	0.306	2.0E-3	0.186	1.7E-3	0.158	1.2E-3	0.111
1E-6	10.53	2.2E-3	0.311	1.4E-3	0.191	1.2E-3	0.170	9.0E-4	0.127
1E-8	11.97	1.8E-3	0.334	1.1E-3	0.212	9.5E-4	0.181	7.4E-4	0.141

It is generally accepted that BER degradation should not exceed 0.2 dB for a good synchronizer [8, Chapter 7], thus based on the results of Table 3—4 and Table 3—5, the symbol over-sampling

rate of $f_{SA}=16f_{SYM}$ (L=16) and estimation window size of M=4 symbols have been chosen for the practical implementation of the FF D-A STR technique (without interpolation correction). The BER degradation curves, for the chosen parameters, have been plotted in Figure 3—19. As seen in that figure, BER degradation is 0.2 dB and 0.3 dB, for the symbol timing variance values (see Figure 3-14) corresponding to M=4 and M=2 STR training symbols, respectively.

In order to verify the theoretical derivations of the BER degradation, the simulation model of the proposed system was designed with C language, and the BER performance simulations were performed in AWGN environment. The BER simulation results shown in Figure 3—20 reveal a degradation of ≅0.2 dB and ≅0.35 dB at 1E-4 BER, for M=4 and M=2 respectively. These results approximately agree with theory, however, for lower BER, the simulated degradation is slightly larger (0.25 dB for M=4 and 0.45 dB for M=2) than theoretical values. These differences could be associated with theoretical assumptions. As the SNR increases it is expected that the simulation curves flatten out at some low BER, when the timing variance effects are more significant than the AWGN effects. Note: the simulation model did not consider the random phase jitter, i.e. the random phase offset was constant during a given burst.

Since the simulation results were promising, the proposed FF D-A STR technique (without interpolation correction) was practically implemented with OQPSK and 4-QAM systems. The measured BER performance results are shown in Figure 3—21. The absolute, measured performance of a 4-QAM system was approximately 4.5 dB worse than theoretical curve. However, the relative difference between the curve of manually adjusted symbol timing, and the over-sampled STR technique (for M=4 and M=2 STR training symbols) was close to the simulated BER degradation differences between the theoretical curve and the simulated BER curves.

Notes on Figure 3—21:

- The degradation of 4.5 dB between the theoretical and the measured BER curve could be associated with the analog sections of the systems, non-linear class C transmitter amplifier not considered in the analysis and simulations, and the imperfect transmit and receive filters.
- Although in theory, both OQPSK and 4-QAM systems have the same BER performance, in our practical setup the 4-QAM system performed slightly better than OQPSK. Since the 4QAM system seemed to have less imperfections, it was chosen for more extensive measurements (i.e. larger SNR sweep, and M=2 system)

The same FF D-A STR technique (M=4, L=16 and M=2, L=16) was also implemented for 16-QAM system. Using equation (3-86), with $E_S=4E_{bavg}$, and the variance results from Section 3.8, the theoretical BER degradation at BER_0=1E-6, was calculated to be 0.41 dB for M=4 and 0.7 dB for M=2.

From the practical measurements, (see Figure 3—22), it can be noticed, that the absolute, measured performance of a 16-QAM system was approximately 5 dB worse (at BER_0=1E-6) than theoretical curve. However, similarly as for 4-QAM system, the relative difference between the curve of manually adjusted symbol timing, and the over-sampled STR technique (for M=4 STR training symbols) was close (0.4 dB at BER_0=1E-6) to the simulated BER degradation results. For the case of M=2 STR training symbols, the measured BER degradation curve diverges more rapidly from the theoretically calculated values (1 dB at BER_0=1E-6). Thus it can be concluded that for 16-QAM modulation, the length of the STR training section should not be lower than 4 symbols.

In Section 3.4, an additional symbol timing correction by interpolation technique was proposed, and as variance simulations in previous sections show, this technique could allow for achieving systems with lower BER degradation, and lower symbol over-sampling rates. In this thesis no physical implementation of this additional technique was done, but further study is recommended.

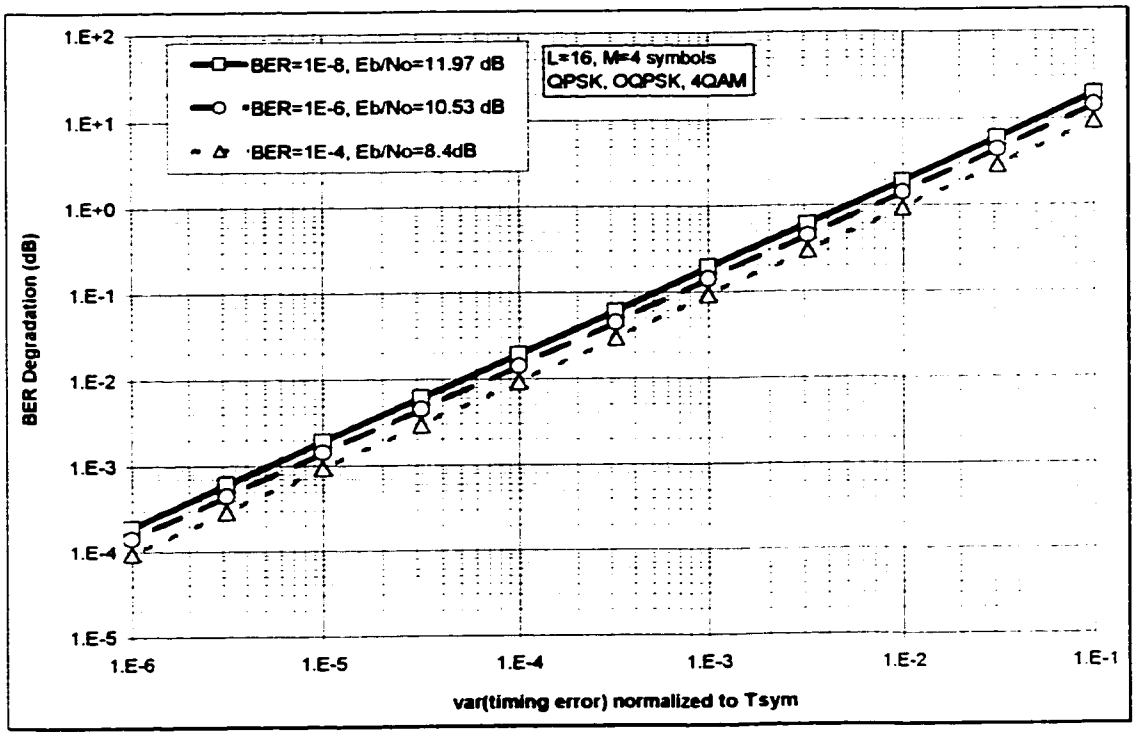

Figure 3—19. BER Degradation due to Timing Synchronization Error for L=16 and M=4

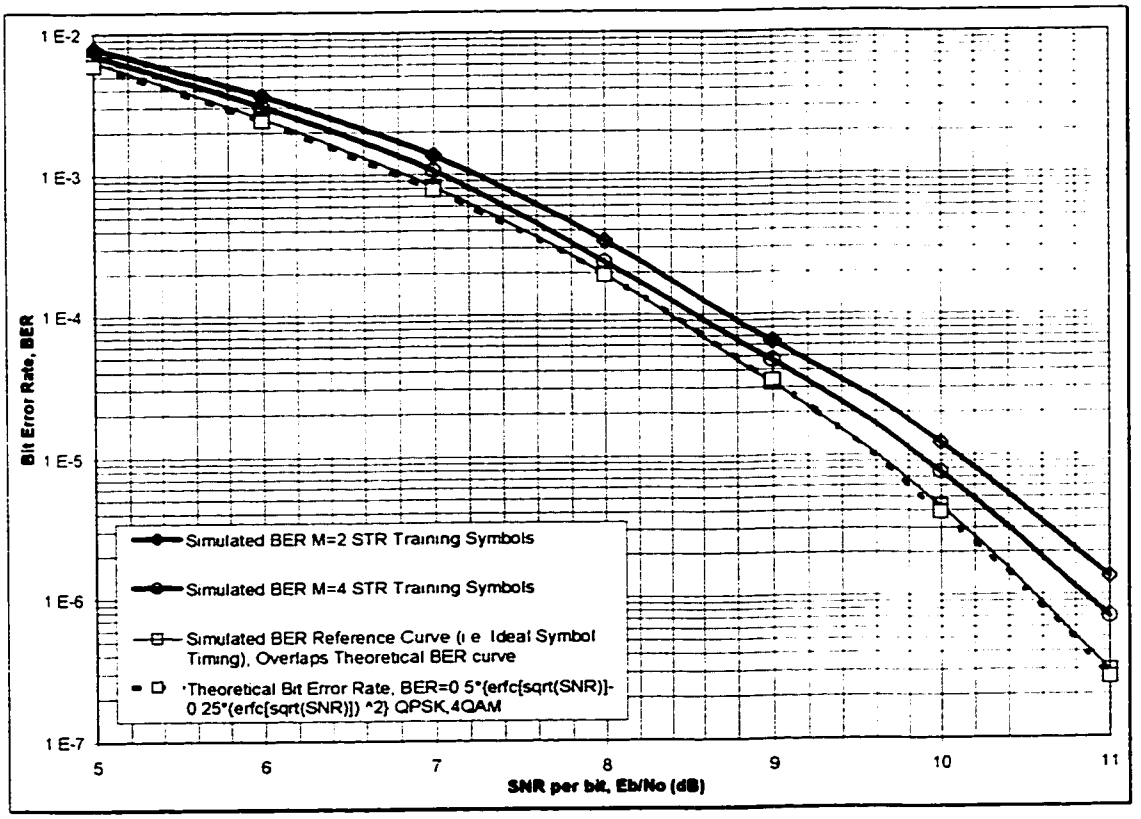

Figure 3—20. BER Simulation Results for the FF D-A STR, (no interpolation correction).

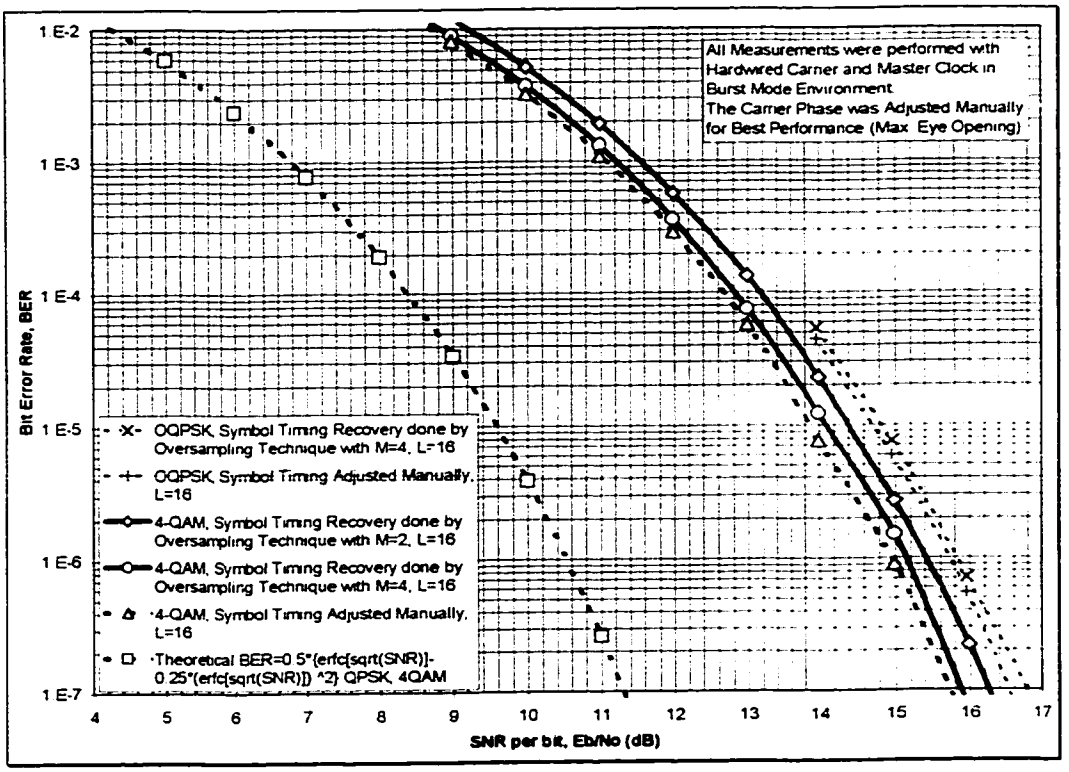

Figure 3—21. BER Measured Results for the FF D-A STR, L=16 (no interpolation correction).

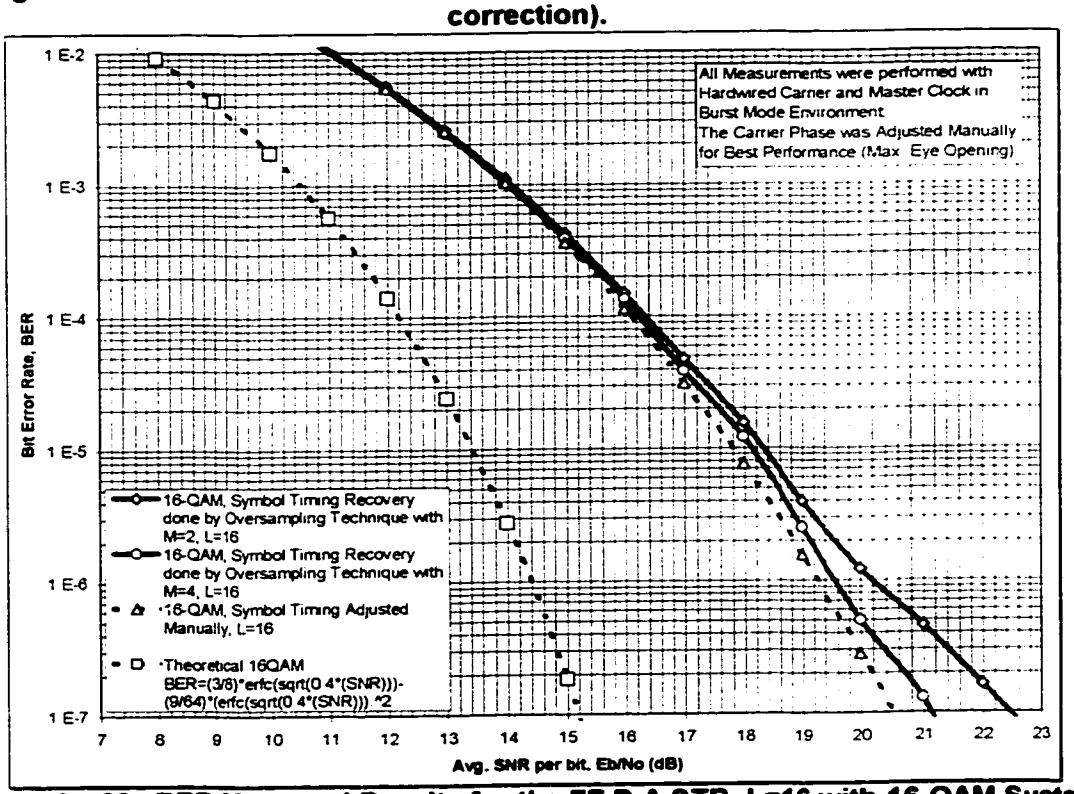

Figure 3—22. BER Measured Results for the FF D-A STR, L=16 with 16-QAM System.

3.11.Acquisition Time

The acquisition of symbol timing is defined as the time elapsed from the beginning of the burst, when the symbol timing is not known, to the time when the estimated symbol timing synchronization parameter has been established (by processing the received signal), and can be used for reliable data detection [8, Chapter 6.5]. In this thesis, it is assumed that the initial carrier recovery (CR) is feedforward, data aided, based on relatively high symbol over-sampling rate and most importantly symbol timing independent. Thus, the CR training section is preceding the STR training section in the burst's preamble, and in order to fairly compare the STR acquisition with other systems, its definition had to be slightly redefined. The modified definition is: the acquisition time of the symbol timing recovery is the time elapsed from the beginning of the STR training section in the burst, until the time when the estimated symbol timing synchronization parameter has been established (see Figure 3—23).

As indicated in Figure 3—23, the symbol timing acquisition time is lower bounded by the length (in symbols) of the STR training section. Any extra (computation) time is dependent on the implementation technique.

- The size of the STR training section (M symbols) is chosen based on the maximum allowable BER degradation and the variance of the proposed STR technique. In Section 3.10 it has been shown that for the recommended limit of 0.2 dB BER degradation the training section has to be M=4 symbols with symbol over-sampling rate of L=16. For more relaxed requirement of BER degradation of approximately 0.3 dB, it has been shown in Section 3.10, that the STR training sequence size can be reduced to M=2 symbols, for QPSK, OQPSK or 4QAM.
- Generally, the computation time is minimized when a given objective function maximization can be obtained by means of direct computation [8 Chapter 6.5]. On the other hand, direct computation is usually hardware consuming, thus a little slower, but more hardware cost efficient search algorithm was chosen for prototype implementation.

The total acquisition time, of the proposed STR technique (without signal delay blocks), is defined by:

$$T_A = M + 1 + \frac{B}{L} \cong M + 2 \,(\text{symbols}) \qquad (3\text{-}87)$$

where:

- Constant of 1 symbol is due to running a search algorithm for maximum eye opening over L number of indexes, and
- B represents the additional processing time, which is usually less than 1 symbol (few system clock cycles), and dependents on implementation style.

For the implemented prototype, with symbol over-sampling rate of L=16 and with STR training sequence length of M=4 the acquisition time was:

T_A=85 system sampling clocks = 5.3125 symbols.

And for the implemented prototype, with symbol over-sampling rate of L=16 and with STR training sequence length of M=2 the acquisition time was:

T_A=53 system sampling clocks = 3.3125 symbols.

As shown in equation (3-87), the acquisition time is constant for every burst, and depends only on the chosen length of the STR training sequence (estimation window size). The extra time (1+B/L), required for processing, could be compensated for, by adding a delay into the signal path (see Figure 3—24), thus reducing the effective acquisition time to:

$$T_A = M \;\; (\text{symbols}) \qquad (3\text{-}88)$$

The acquisition time of M symbols (where M=4 for QPSK) is very small, and thus the proposed STR technique could be applied to very short burst mode systems, and still provide high user's data throughput efficiency.

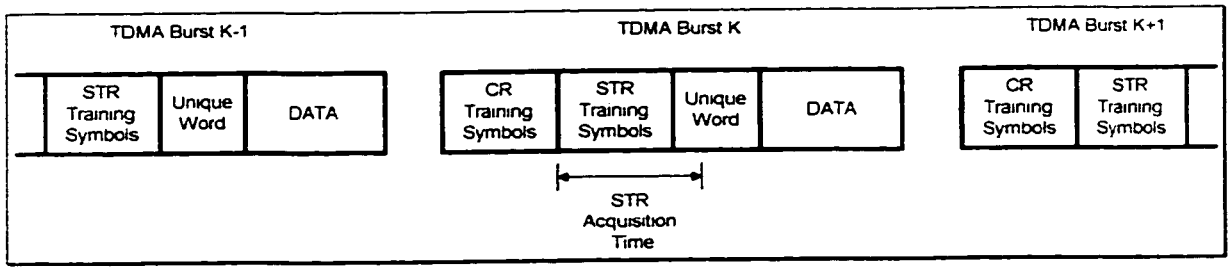

Figure 3—23. Definition of Symbol Timing Acquisition Time.

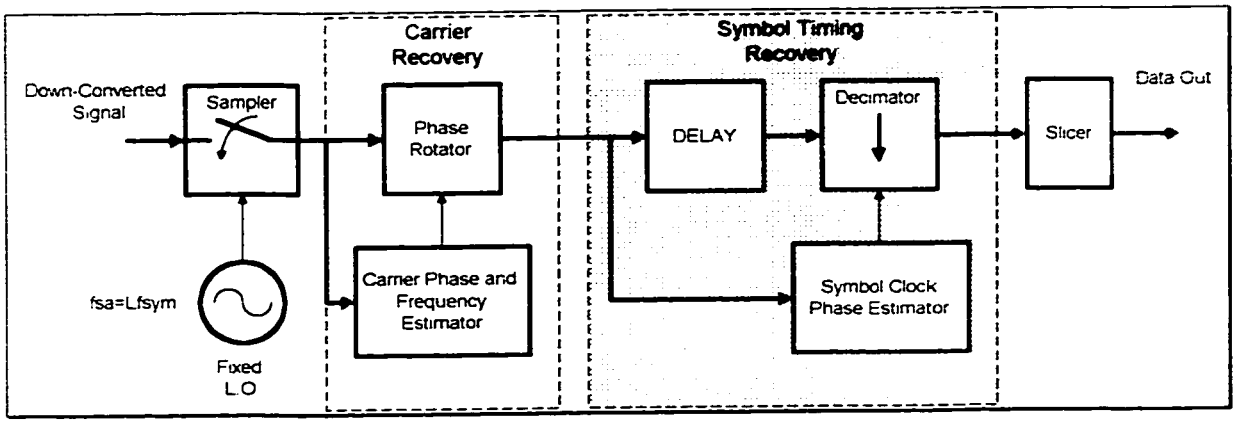

Figure 3—24. Signal Path Delay Blocks for Reducing the Effective STR Acquisition Time.

3.12. Implementation Complexity

In this section the digital implementation structure and the complexity of the proposed symbol timing recovery module will be presented. First, in general terms (i.e. technology independent), in order to make comparison and complexity assessment across all digital platforms feasible. And second, in terms of a specific Field Programmable Gate Array technology, which was chosen for prototype implementation.

In Section 3.3 the final objective function to be maximized was presented in equation (3-28), here we rewrite it for convenience:

$$\Lambda_L(\tau_i) = \sum_{m=1}^{M} \left[\left| z_I((m+\tau_i)T_{SYM}) \right| + \left| z_Q((m+\tau_i+\Delta)T_{SYM}) \right| \right] \quad (3\text{-}89)$$

where:

m is the symbol number, and i is the sampling index number {0,1,2,...,L-1}

The Figure 3—25, Figure 3—26, and Figure 3—27 present the hardware implementation block diagram of the proposed STR algorithm (the width of data paths, is shown in the figures on the block interconnection lines), and the following paragraph is a detailed description of each block. In order to make the diagrams more illustrative, fixed values for symbol over-sampling ratio L=16, and estimation window size (length of the STR training sequence) M=4, were chosen. The description, however, is more general and refers to these constants as L and M.

3.12.1. Detailed Description of Digital Implementation of STR Algorithm

a) In the receiver, after quadrature down-conversion to the baseband and filtering with the matched filter, the in-phase (I) and quadrature (Q) channels have alternating symbol pattern, during the STR training sequence sent in the preamble. Since the raised cosine pulse shaping is assumed in the considered communication system, the I and Q signals at the output of the receiver matched filter, have cosine wave shape (see Figure 3—25).

b) The In-phase and Quadrature matched filter outputs are sampled at a rate of L times the symbol rate, that is $f_{SA}=Lf_{SYM}$ (see Figure 3—25). The sampled signals are defined as $z_I((m+\tau_i)T_{SYM})$ and $z_Q((m+\tau_i)T_{SYM})$, where m is the symbol index m={1,...,M}, M is the total number of STR training symbols, and i is the sample index i={0,...,L-1}.

c) For the case of Offset-QPSK modulation, in order to simplify hardware implementation, one of the channels is delayed by half a symbol, such that the "eye" openings of I and Q channels are aligned (see Figure 3—25). The output of the delay block is $z_Q((m+0.5+\tau_i)T_{SYM})$.

d) The maximum "eye" opening occurs when the cosine wave shaped I and Q signals reach its maximum positive or maximum negative values. In order to simplify the detection of these maximum values, both channels are passed through the digital full wave rectifiers. The outputs of these blocks are defined as: $|z_I((m+\tau_i)T_{SYM})|$ and $|z_Q((m+\Delta+\tau_i)T_{SYM})|$, where Δ is 0 for QPSK, or QAM, and 0.5 for OQPSK. The resulting signals on I and Q channels have positive peaks, which correspond to the maximum "eye" opening (best symbol sampling time), see Figure 3—25.

e) As equation (3-89) suggests, the absolute values of in-phase and quadrature signals are added together, $z_{im}=(|z_I((m+\tau_i)T_{SYM})|+|z_Q((m+\Delta+\tau_i)T_{SYM})|)$ (see Figure 3—25).

f) The resulting signal samples (z_{im}) with the same index i, are averaged over M symbols, such that the outputs of the L averaging blocks are $\Lambda_L(\tau_i)=\Sigma(|z_I((m+\tau_i)T_{SYM})|+|z_Q((m+\Delta+\tau_i)T_{SYM})|)$, where: i={0,..,L-1} (see Figure 3—26). Note that since the signal samples z_{im} arrive serially, only one serial accumulator with L memory locations is sufficient.

g) The resulting outputs of the L averaging blocks $\Lambda_L(\tau_i)$ are compared to each other and the maximum value is found., $\Lambda_{LMAX}(\tau_{iMAX})=\max(\Lambda_L(\tau_i))$, where i={0,...,L-1}. The corresponding sample index i_{MAX} of that maximum value is declared as the index of the maximum "eye" opening (see Figure 3—27).

h) When the preamble is finished, then the in-phase signal samples are decimated at every $\tau_i=\tau_{iMAX}$ sample index, and the quadrature signal samples are decimated at every $\tau_i=\tau_{iMAX}+\Delta$ sample index (see Figure 3—27). Note that for the case of QPSK, or QAM modulation, both I and Q signals would be sampled at the same time, every L samples.

Based on the above description, Figure 3—25, Figure 3—26 and Figure 3—27, it can be noticed that the hardware complexity of the proposed STR technique is defined only by relatively simple components, which are listed in Table 3—6.

Table 3—6. Hardware Implementation Complexity.

Function Description	Size	Qty
2's Complement or Magnitude Extractor	q bits (where: q is the chosen quantization for I and Q signals)	2
Unsigned Adder	q+1 bits	1
Unsigned Adder (part of serial accumulator)	$q+\log_2(L)$	1
RAM Memory block (part of serial accumulator)	L(address)x[$q+\log_2(L)$](word size)	1
Serial Magnitude Comparator	For full precision [$q+\log_2(L)$]	1
Control Logic	Depends on the implementation style	1
Note: All above components must be able to operate at T_{SYM}/L system clock rate		

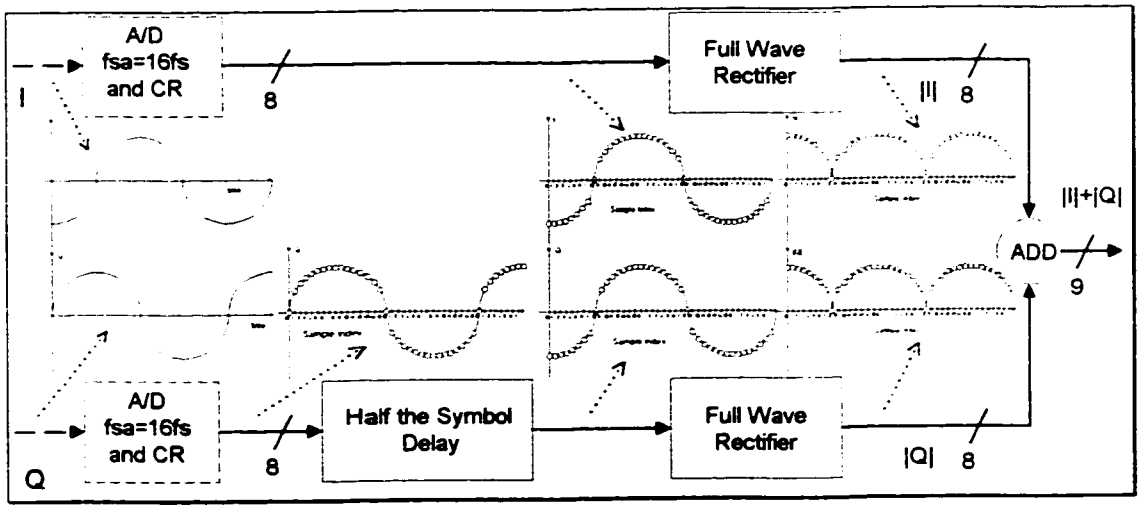

Figure 3—25. Full Wave Rectification and Channel Addition.

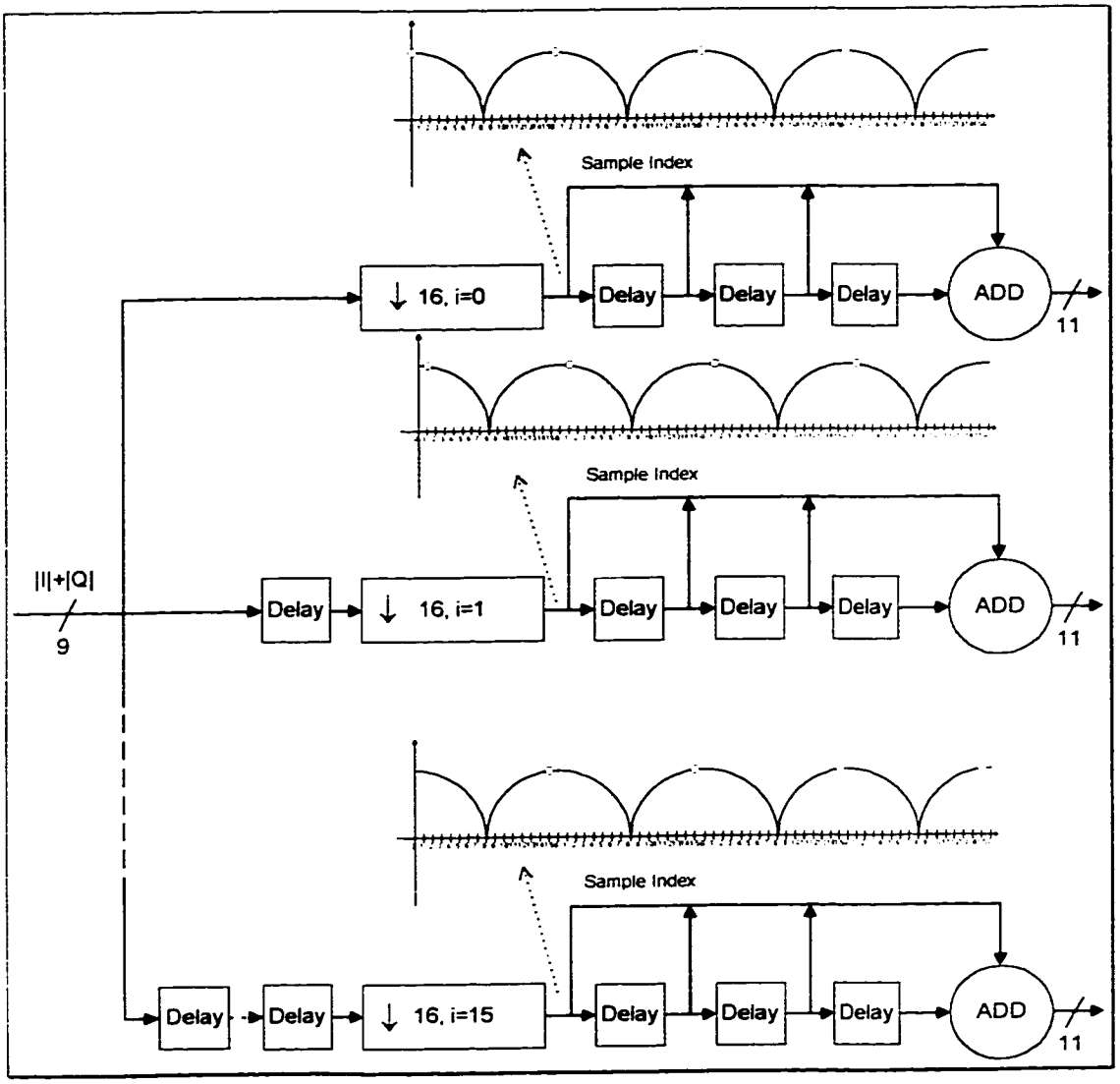

Figure 3—26. L=16 Accumulators Section

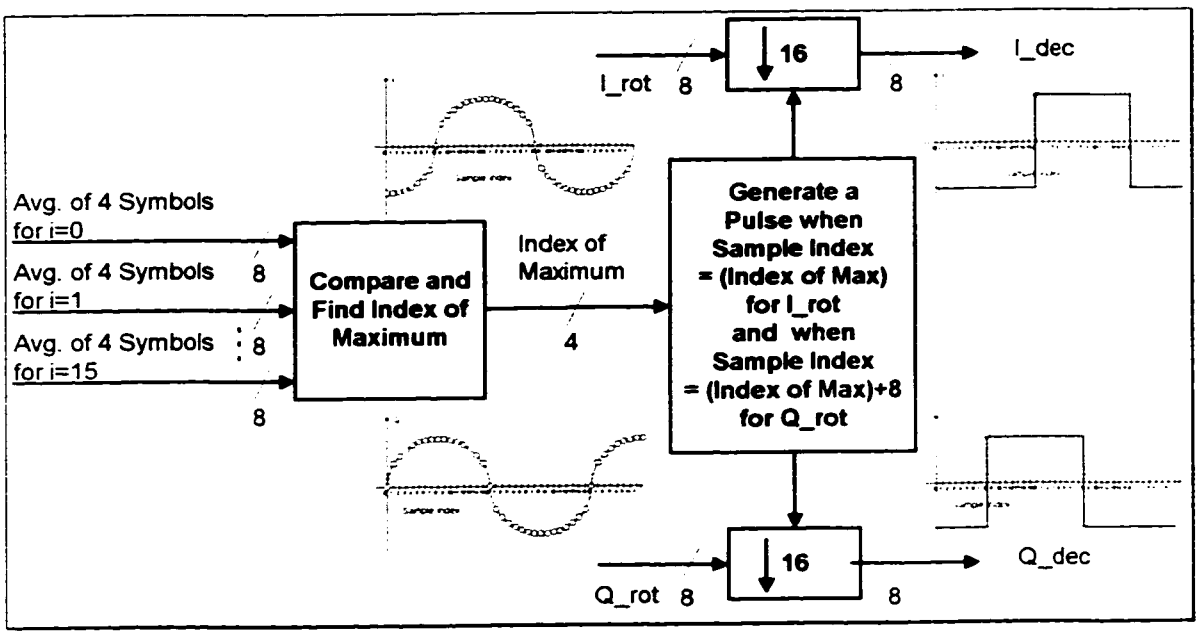

Figure 3—27. Find Index of Maximum, and Decimate I and Q

3.12.2. FPGA Implementation of the STR Algorithm.

The proposed all-digital STR technique can be implemented using three different technologies, namely:

- high speed digital signal processor (DSP), which is a single-stream instruction set processor optimized for high-speed arithmetic
- application-specific integrated circuit (ASIC), which represents hard-coded logic, and
- field programmable gate array (FPGA), which is an array of gates with programmable interconnect and logic functions that can be redefined after manufacture.

The comparison of all the above listed technologies is given in [32]. Because of the superior advantages over other technologies in terms of power consumption, size, cost, upgradability, dynamic reconfiguration, and time-to-market factors, the FPGA technology option was chosen for the prototype implementation.

The prototype of the proposed STR technique, was implemented for Offset-QPSK system on the Xilinx FPGA XC4028EX-3 chip, with the symbol rate of f_{SYM}=2.5 MHz. The optimum algorithm parameters were chosen as suggested by theoretical derivations and simulations, that is the length of STR training sequence was M=4 symbols, and the sampling frequency of I and Q channels was $f_{SA}=16 \cdot f_{SYM}$=40.0 MHz.

The circuit design was made using VHDL hardware description language with instantiation of (speed and area optimized) basic modules such as multipliers, and dual-ported RAM from Xilinx LogiCORE. The VHDL code was compiled using Synplicity tools, and automatic mapping, placement and routing of the circuit onto the FPGA chip was done using Xilinx Foundation Series tools.

The design parameters, the resulting chip area coverage in Configurable Logic Blocks (CLBs), and the maximum operating speed for this design (STR section) are summarized in Table 3—7.

Table 3—7. FPGA Design Parameters for OQPSK STR, M=4.

Parameter	**Size**
I and Q signal channel quantization, q	8 bits
Timing Offset Parameter quantization, L	16 levels
Estimation (Observation) Window Size, M	4 symbols
Implementation Results	
Number of CLBs used for STR algorithm	85 CLBs
Maximum Operating System frequency, L/T_{SYM}	57.5 MHz
Corresponding Maximum Bit Rate, $2/T_{SYM}$	7.2 Mbps
Note: If the design was to be compiled for better speed grade chips (-.9 or -1) the $2/T_{SYM}$ rate is expected to be greater	

As shown in Table 3—7 the maximum bit rate of the prototype FPGA design is relatively low ≈ 7Mbps. If much higher bit rates are desired the interpolation technique presented in Section 3.4 should be further investigated.

CHAPTER 4.

CONCLUSIONS AND SUGGESTIONS FOR FURTHER RESEARCH

4.1. Conclusions

The major objective of this thesis was to present and analyze new, low complexity, digital implementation structures for symbol timing recovery. All techniques are illustrated as an application to the part of broadband wireless access system, however, the application of these techniques can be easily expanded to other wire and wireless systems.

The first presented digital structure was a feedback symbol timing recovery technique, which was based on the Costas loop principle. This technique has been previously analyzed from analog implementation point of view in [7], its main feature was extremely low jitter of 2% (required in high level modulation systems), however, the excessively long acquisition time (184,000 symbols) made this analog technique unattractive for practical applications. The new digital implementation structure of the Costas loop symbol timing recovery technique, presented in Chapter 2 of this thesis, significantly reduced the acquisition time to only 100 symbols. This new structure maintained the very low jitter feature (2% for 8-PAM with Eo/No of 8 dB), the estimated bit error rate degradation was less than 0.1 dB, and the pull-in frequency was in satisfactory range of +/- 100 PPM. Another attractive feature of this new structure is that it only requires 5 constant multipliers and 7 adders. All the above mentioned numerical results have been obtained

by computer simulations. Note, based on practical measurements (Figure 3-22), with reference to hardwired, and manually adjusted symbol timing recovery, the implemented FF algorithm was approximately 0.2 dB worse than shown by simulations, thus the expected implementation margin for presented techniques is 0.2 dB. Although the obtained acquisition time of 100 symbols for the new digital structure is much lower than that for the analog structure, this acquisition time is too long for most of the short burst mode communication systems. Thus the feedback symbol timing recovery structure presented in Chapter 2 is limited to application in continuous and long burst mode communication systems.

The other two new digital structures were presented in Chapter 3 for the feedforward, data-aided, symbol timing recovery. The feedforward techniques have much faster acquisition time (thus can be applied to short burst mode systems), and since both techniques presented in Chapter 3 were based on the maximum likelihood estimation, they also produce near optimum estimates of symbol timing (thus can be applied to high level modulation systems). The first presented feedforward technique uses relatively high symbol over-sampling to achieve low implementation complexity and acceptable variance (or jitter). Form the theoretical analysis and simulations it has been concluded, that for the bit error rate degradation of 0.3 dB (at BER=1E-6), for 4 QAM system, the symbol over-sampling has to be equal to 16 samples per symbol, and the length of training preamble can be only 4 symbols long. The hardware complexity of this structure is very low, it only requires the following major components: 2 unsigned adders, 1 RAM block, and 1 serial magnitude comparator. This new digital structure for feedforward symbol timing recovery technique has been implemented and the simulated results have been verified by measurements. One of the drawbacks of this technique is that due to the high over-sampling rate, utilized in the design, the technique is only applicable to communication systems with relatively low bit rate (10Mbps).

In order to expand the applicability of this new over-sampling, maximum likelihood technique to higher bit rate (50Mbps using 4-QAM) systems, an optional "add-on" interpolation technique has

been developed, which can effectively reduce the over-sampling rate to a minimum of 3 samples per symbol. The simulation results show that the additional interpolation technique improves the variance of the estimated symbol timing, and the resulting bit error rate degradation is negligible even for the minimum over-sampling rate. The cost for the improved performance is in the implementation complexity, which increases by 3 additions and 1 divider functions. The above results look very promising, however, they are based only on the floating point simulations, further study should be performed.

4.2. Suggestions for Further Research

The major results of Chapter 2 clearly show that the digital implementation Costas loop for symbol timing recovery is very promising feedback technique for continuous mode, high level modulation, communication system. In order to verify the partial theoretical analysis and the obtained simulation results, the hardware implementation should be pursued and the practical bit error rate measurements should be made.

In Chapter 3, the bit error rate performance measurements of the high over-sampling symbol timing recovery technique should be repeated with a more accurate transmitter and receiver analog front end, and simulations should be done with the class C amplifier.

According to floating point simulation results the symbol timing correction by interpolation algorithm, presented in Section 3.4, promises to achieve very good bit error rate performance even in high bit rate applications, thus a quantized signal simulation and practical implementation measurements are highly recommended for further research. The analytical work with AWGN channel is also recommended.

The application of the proposed algorithms should be investigated for non-LOS transmission paths.

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Appendix A.

The Background on the Received Signals

In this section it will be shown that the received signal, equation (2-2), has a normalized baseband noise component with zero mean and variance of $N_o/(4E_b)$.

The simplified block diagram of QPSK and OQPSK systems is shown in Figure A-1.

The transmitted signal can be represented as:

$$y(t) = y_I(t) \cdot \phi_I(t) + y_Q(t) \cdot \phi_Q(t) \tag{A-1}$$

where, $\phi_I(t)$ and $\phi_Q(t)$ are orthonormal functions:

$$\begin{aligned} \phi_I(t) &= \sqrt{\frac{2}{T_C}} \cos(\omega_C t) \\ \phi_Q(t) &= \sqrt{\frac{2}{T_C}} \sin(\omega_C t) \end{aligned} \tag{A-2}$$

and,

$$\begin{aligned} y_I(t) &= \sqrt{\frac{E_b}{E_{g_T}}} \sum_{k=-\infty}^{\infty} a_k g_T(t - (k+\tau)T_{SYM}) \\ y_Q(t) &= \sqrt{\frac{E_b}{E_{g_T}}} \sum_{k=-\infty}^{\infty} b_k g_T(t - (k+\tau+\Delta)T_{SYM}) \end{aligned} \tag{A-3}$$

and,

$g_T(t)$: Transmitter pulse shaping function

E_b : Bit energy

E_{g_T} : Energy of transmitter pulse shaping function, $g_T(t)$

a_k, b_k : Normalized data symbols, ±1, for QPSK and OQPSK

$\Delta=0$: Delay constant for QPSK

$\Delta=0.5$: Delay constant for Offset QPSK

T_{SYM} : Symbol period

T_C : Carrier period

τ : Normalized symbol clock phase offset, $|\tau|\leq 0.5$

ω_C : Carrier angular frequency

The transmitted signal y(t) is energy type with the average energy defined as:

$$E_y \triangleq \frac{1}{2\pi}\int_{-\infty}^{\infty}|Y(\omega)|^2 d\omega = \frac{1}{2\pi}\int_{-\infty}^{\infty}\frac{E_b}{E_{g_T}T_C}\left[G_T^2(\omega-\omega_C)+G_T^2(\omega+\omega_C)\right]d\omega = \frac{2E_b}{T_C} = \frac{E_S}{T_C} \quad \textbf{(A-4)}$$

since:

$$E_{g_T} \triangleq \frac{1}{2\pi}\int_{-\infty}^{\infty}|G_T(\omega)|^2 d\omega \quad \textbf{(A-5)}$$

The transmission channel $C_{BP}(\omega)$ is assumed to be bandlimited, with constant magnitude frequency response, and linear phase, in the passband region, thus it does not change the shape of the signal spectrum.

The signal y(t) is assumed to be disturbed by bandpass additive Gaussian noise $n_{BP}(t)$ with constant spectral density $N_o/2$, that is $n_{BP}(t)$ is white within the signal bandwidth B. This bandpass

noise assumption is admissible, because it does not have an effect on the statistics of the down-converted signal, and it is common in the practical situations [8, Chapter 1.2]. Thus, the input signal to the receiver is:

$$r(t) = y(t) + n_{BP}(t) \tag{A-6}$$

When the noise is assumed to be bandlimited, then it can be represented in the in-phase and quadrature components as:

$$n_{BP}(t) = n_C(t)\cos(\omega_C t) - n_S(t)\sin(\omega_C t) \tag{A-7}$$

where:

the power spectral density (psd) of $n_C(t)$ and $n_S(t)$ is $N_o/2$ in the band of interest (signal bandwidth B).

Thus the input signal to receiver becomes:

$$\begin{aligned} r(t) = &\sqrt{\frac{2E_b}{T_C E_{g_T}}} \sum_{k=-\infty}^{\infty} a_k g_T(t - (k+\tau)T_{SYM})\cos(\omega_C t) + n_C(t)\cos(\omega_C t) \\ &+ \sqrt{\frac{2E_b}{T_C E_{g_T}}} \sum_{k=-\infty}^{\infty} b_k g_T(t - (k+\tau+\Delta)T_{SYM})\sin(\omega_C t) - n_S(t)\sin(\omega_C t) \end{aligned} \tag{A-8}$$

And after down-conversion by the local oscillator (ϕ_I, ϕ_Q), and lowpass filtering, in order to remove the high frequency components, we obtain:

$$\begin{aligned} r_I(t) &= \frac{1}{T_C}\sqrt{\frac{E_b}{E_{g_T}}} \sum_{k=-\infty}^{\infty} a_k g_T(t - (k+\tau)T_{SYM}) + \frac{n_C(t)}{\sqrt{2T_C}} \\ r_Q(t) &= \frac{1}{T_C}\sqrt{\frac{E_b}{E_{g_T}}} \sum_{k=-\infty}^{\infty} b_k g_T(t - (k+\tau+\Delta)T_{SYM}) - \frac{n_S(t)}{\sqrt{2T_C}} \end{aligned} \tag{A-9}$$

For convenience, the received signals are normalized by multiplying them by a constant $T_C\text{sqrt}(E_{gT}/E_b)$ thus,

$$r_I(t) = \sum_{k=-\infty}^{\infty} a_k g_T(t-(k+\tau)T_{SYM}) + \sqrt{\frac{T_C E_{g_T}}{2E_b}} n_C(t)$$
$$r_Q(t) = \sum_{k=-\infty}^{\infty} b_k g_T(t-(k+\tau+\Delta)T_{SYM}) - \sqrt{\frac{T_C E_{g_T}}{2E_b}} n_S(t) \qquad \textbf{(A-10)}$$

The $n_C(t)$ and $n_S(t)$, in equation (A-10), are statistically independent identically distributed (i.i.d.) zero-mean Gaussian random processes, with a power spectral density (psd) that equals $N_o/2$ for $|\omega|<2\pi B$, however, it is a common practice to replace $n_C(t)$ and $n_S(t)$ by truly white process (i.e. $N_o/2$ for all ω), since again it does not have an effect on the statistics of the down-converted signal [8, Chapter 1.2]. Thus for the analysis it is assumed that:

$$S_{n_c}(\omega) = S_{n_s}(\omega) = N_o/2 \quad \text{for all } \omega \qquad \textbf{(A-11)}$$

The received signal can be re-written, in the simplified form, as:

$$r_I(t) = \sum_{k=-\infty}^{\infty} a_k g_T(t-(k+\tau)T_{SYM}) + n_{Bc}(t)$$
$$r_Q(t) = \sum_{k=-\infty}^{\infty} b_k g_T(t-(k+\tau+\Delta)T_{SYM}) + n_{Bs}(t) \qquad \textbf{(A-12)}$$

where n_{Bc}, n_{Bs} are the equivalent normalized baseband noise components defined as:

$$n_{Bc}(t) = \sqrt{\frac{T_C E_{g_T}}{2E_b}} n_C(t)$$
$$n_{Bs}(t) = -\sqrt{\frac{T_C E_{g_T}}{2E_b}} n_S(t) \qquad \textbf{(A-13)}$$

For convenience, it is assumed that $T_C E_{g_T} = 1$ thus,

$$n_{Bc}(t) = \sqrt{\frac{1}{2E_b}} n_C(t)$$
$$n_{Bs}(t) = -\sqrt{\frac{1}{2E_b}} n_S(t) \qquad \text{(A-14)}$$

and the variance of the equivalent normalized baseband noise components is:

$$\text{var}(n_{Bc}) = \text{var}(n_{Bs}) = \frac{N_o}{4E_b} \qquad \text{(A-15)}$$

The expressions in (A-12) of the received, equivalent baseband signals $r_I(t)$ and $r_Q(t)$ are used in derivation of Maximum Likelihood function for symbol timing in Section 3.3.

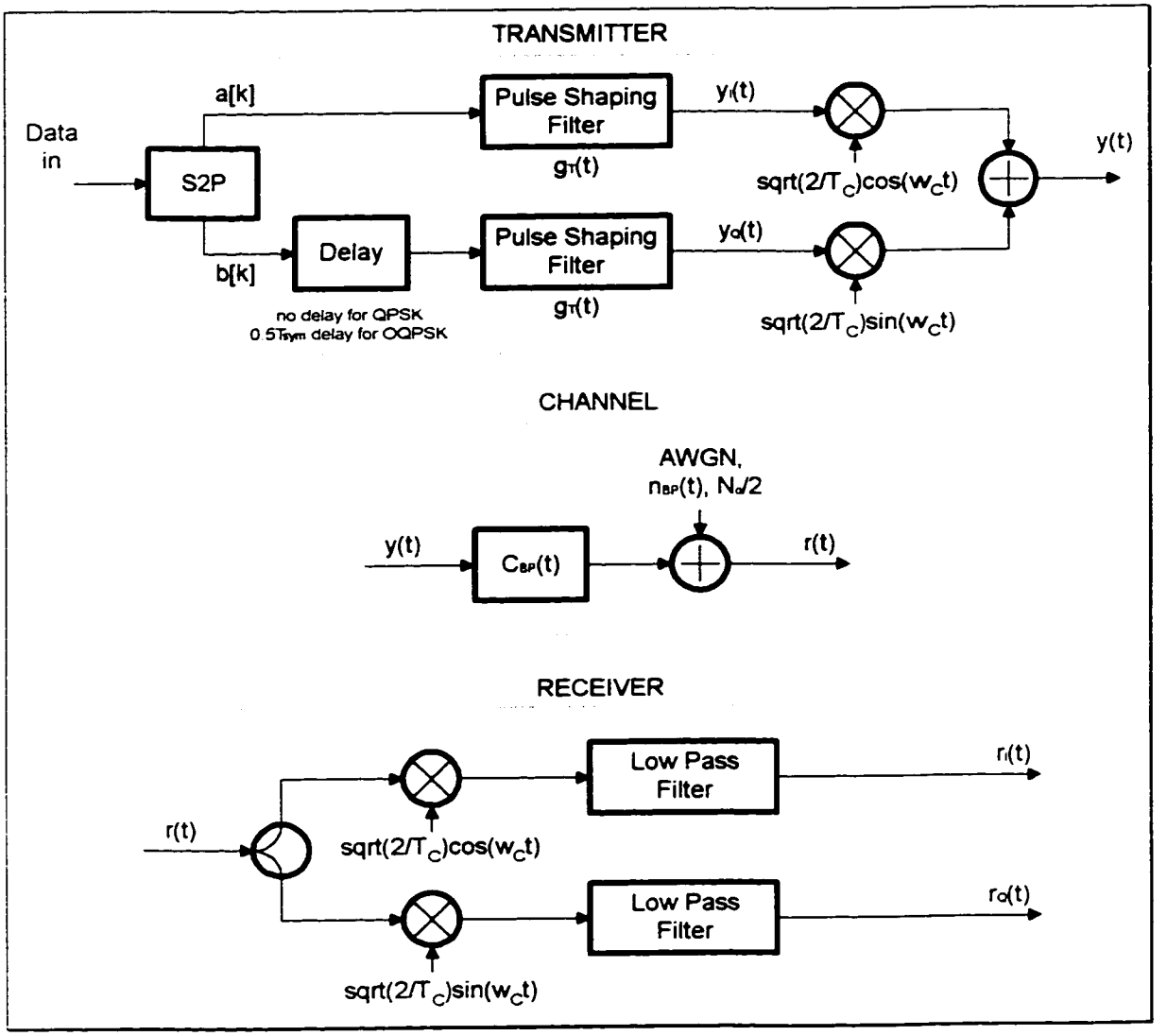

Figure A-1. General Block Diagram of QPSK and OQPSK Systems.

Appendix B.

Derivation of Equation (3-82) Section 3.8

The equation (3-82) is derived from the maximum likelihood equation (3-28) rewritten here for convenience:

$$\Lambda_L(\tau_i) = \sum_{m=1}^{M} \left[\left| z_I((m+\tau_i)T_{SYM}) \right| + \left| z_Q((m+\tau_i+\Delta)T_{SYM}) \right| \right] \quad \textbf{(B-1)}$$

Substituting the following equations, derived in Chapter 3,

$$\begin{aligned} z_I((m+\tau_i)T_{SYM}) &= \int_{-\infty}^{\infty} r_I(t) g_R((m+\tau_i)T_{SYM} - t)dt \\ z_Q((m+\tau_i+\Delta)T_{SYM}) &= \int_{-\infty}^{\infty} r_Q(t) g_R((m+\tau_i+\Delta)T_{SYM} - t)dt \end{aligned} \quad \textbf{(B-2)}$$

$$\begin{aligned} r_I(t) &= \sum_{k=-\infty}^{\infty} a_k \cdot g_T(t - kT_{SYM} - \tau T_{SYM}) + n_{B_C}(t) \\ r_Q(t) &= \sum_{k=-\infty}^{\infty} b_k \cdot g_T(t - kT_{SYM} - \tau T_{SYM} - \Delta T_{SYM}) + n_{B_S}(t) \end{aligned} \quad \textbf{(B-3)}$$

And assuming that the training sequence a_k and b_k are composed of alternating 1 and –1 levels, $a_k=b_k=(-1)^k$, the following is obtained,

$$\Lambda_L(\tau_i)=\sum_{m=1}^{M}\left[\begin{array}{l}\left|\sum_{k=-\infty}^{\infty}(-1)^k g((m-k)T_{SYM}+(\tau_i-\tau)T_{SYM})+\right.\\ \left.+\int_{-\infty}^{\infty}\frac{n_{B_c}(t)}{\sqrt{2E_b}}g_R((m+\tau_i)T_{SYM}-t)dt\right|+\\ +\left|\sum_{k=-\infty}^{\infty}(-1)^k g((m-k)T_{SYM}+(\tau_i-\tau)T_{SYM})+\right.\\ \left.+\int_{-\infty}^{\infty}\frac{n_{B_s}(t)}{\sqrt{2E_b}}g((m+\tau_i+\Delta)T_{SYM}-t)\right|\end{array}\right] \quad \textbf{(B-4)}$$

Using equation (3-3) and (3-6) to represent the above in terms of cosine function, the final equation is obtained,

$$\Lambda_L(\tau_i)=\sum_{m=1}^{M}\left[\begin{array}{l}\left|\cos(\pi(\tau_i-\tau-m))+v_{nc}((m+\tau_i)T_{SYM})\right|+\\ +\left|\cos(\pi(\tau_i-\tau-m))+v_{ns}((m+\tau_i+\Delta)T_{SYM})\right|\end{array}\right] \quad \textbf{(B-5)}$$

which can also be represented as equation (3-82),

$$\Lambda_L(\tau_i)=\sum_{m=1}^{M}\left[\begin{array}{l}\sqrt{[\cos(\pi(\tau_i-\tau-m))+v_{nc}((m+\tau_i)T_{SYM})]^2}+\\ +\sqrt{[\cos(\pi(\tau_i-\tau-m))+v_{ns}((m+\tau_i+\Delta)T_{SYM})]^2}\end{array}\right] \quad \textbf{(B-6)}$$