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RESONANT UPS TOPOLOGIES FOR THE EMERGING HYBRID FIBER COAXIAL NETWORKS

Humberto Pinheiro

A Thesis

in

The Department

of

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Presented in Partial Fulfillment of the Requirements
for the Degree of Doctor of Philosophy at
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ii

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ABSTRACT

RESONANT UPS TOPOLOGIES FOR THE EMERGING HYBRID FIBER COAXIAL NETWORKS

Humberto Pinheiro
Concordia University, 1998

Uninterruptible power supply (UPS) systems have been extensively applied to feed critical loads in many areas. Typical examples of critical loads include life-support equipment, computers and telecommunication systems. Although all UPS systems have a common purpose to provide continuous power to critical loads, the emerging hybrid fiber-coaxial networks have created the need for specific types of UPS topologies. For example, galvanic isolation for the load and the battery, small size, high input power factor, and trapezoidal output voltage waveforms are among the required features of UPS topologies for hybrid fiber-coaxial networks. None of the conventional UPS topologies meet all these requirements. Consequently, this thesis is directed towards the design and analysis of UPS topologies for this new application. Novel UPS topologies are proposed and control techniques are developed to allow operation at high switching frequencies without penalizing the converter efficiency. By the use of resonant converters in the proposed UPS topologies, a high input power factor is achieved without requiring a dedicated power factor correction stage. In addition, a self-sustained oscillation control method is proposed to ensure soft switching under all operating conditions. A detailed analytical treatment of the resonant converters in the proposed UPS topologies is presented and design procedures illustrated. Simulation and experimental results are presented to validate the analyses and to demonstrate the feasibility of the proposed schemes.

ACKNOWLEDGMENTS

I wish to express my sincere gratitude to Dr. Praveen Jain and Dr. Geza Joos for their valuable advice and support during the course of this study.

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To my wife Emilia and

daughters Mariana and Helena

TABLE OF CONTENTS

CHAPTER 2 - ZERO VOLTAGE SWITCHING RESONANT CONVERTERS

CHAPTER 3 - HIGH POWER FACTOR AC/DC RESONANT CONVERTERS

LIST OF FIGURES

LIST OF TABLES

LIST OF ACRONYMS

BJT	Bipolar Junction Transistor.
BSC	Battery Side Converter.
DPF	Displacement Power Factor.
EMI	Electromagnetic Interference.
HFC	Hybrid Fiber-Coaxial Networks.
LSC	Line Side Converter.
MOSFET	Metal Oxide Field Effect Transistor.
OSC	Output Side Converter.
PF	Power Factor.
PFC	Power Factor Correction Circuits
PWM	Pulse Width Modulation.
rms	Root-mean-square value.
SMR	Switching Mode Rectifier.
SOC	Self-Sustained Oscillating Controller.
THD	Total Harmonic Distortion.
UPS	Uninterruptible Power Supply.
UPWM	Unipolar Pulse Width Modulation.
VF	Variable Frequency Control.
VFPSM	Variable Frequency Control Plus Phase Shift Modulation.
ZCS	Zero Current Switching.
ZVS	Zero Voltage Switching.

LIST OF SYMBOLS

A	Amplitude of the first harmonic of the feedback variable x.
C_o	Capacitor of the output dc filter.
C_p	Parallel capacitor of the resonant circuit.
C_s, C_{s1}	Capacitor of the series resonant branch of the line side converter.
C_{s2}	Capacitor of the series resonant branch of the battery side converter.
C_{smo}	Nominal value of the series resonant capacitor.
f_o	Natural frequency of a LC circuit. It is defined as $f_o = \frac{1}{2\pi\sqrt{L_s C_s}}$.
G_{is_vab}, G_{is1_vab1}	Transfer function from the line side converter output voltage to the current through the series resonant branch at the line side converter.
G_{is1_vab2}	Transfer function from the battery side converter output voltage to the current through the resonant inductor at the line side converter.
G_{vcs_vab}	Transfer function from the line side converter output voltage to the voltage across the resonant inductor at the line side converter.
G_{vp_vab}	Transfer function from the inverter output voltage to the voltage across parallel capacitor of the resonant circuit.
i_b	Battery current.
$\bar{i}_b$	Battery current averaged over one switching period.
i_d	Current at the input of the line side converter.

$\hat{i}_{d2}$	Peak value of the second harmonic of the current i_d.
$\hat{i}_{dn}$	Peak value of the n-th harmonic of the current i_d.
i_g	Output current of the input diode bridge rectifier.
$\bar{i}_g$	Current i_g averaged over on switching interval.
$\hat{i}_g$	Peak value of i_g. Operation at full power.
$\hat{i}_{gm}$	Peak value of i_g with the lowest input ac voltage. Operation at full load.
$\hat{i}_{gref}$	Peak value of the template current.
i_o	Current through the inductor of the output filter.
$\hat{i}_o$	Peak value of the current through the inductor of the output filter.
I_o	Dc component of the output current i_o.
i_{s1}	Current through the series resonant inductor connected to the line side converter.
$\hat{i}_{s1}$	Peak value of the fundamental component of the current through the series resonant inductor connected to the line side converter.
I_{s1}	Phasor associated with the first harmonic component of i_{s1}.
i_{s2}	Current through the series resonant inductor connected to the battery side converter.
$\hat{i}_{s2}$	Peak value of the first harmonic component of the current through the series resonant inductor connected to the battery side converter.
I_{s2}	Phasor associated with the first harmonic component of i_{s2}.

i_{ss}	Amplitude of the sine component of the first harmonic of i_{s1}.
i_{sc}	Amplitude of the cosine component of the first harmonic of i_{s1}.
I_{ref1}	Input current template.
k_s	Current sensor gain.
k	Gain of the input current controller.
k_n	Attenuation factor for n-th the harmonic of the input current.
K_{p1}, K_{p2}	Gain constants of the sawtooth generator.
L_o	Inductance of the output dc filter.
L_s, L_{s1}	Total inductance of the series resonant branch of the line side converter.
L_{snn}	Nominal value of the series resonant inductor.
L_{s1}	Total inductance of the series resonant branch of the battery side.
L_{1eq}	Equivalent inductance of the series resonant branch of the line side.
L_{2eq}	Equivalent inductance of the series resonant branch of the battery side.
M	Voltage conversion ratio.
M_m	Maximum voltage conversion ratio of an ac-dc converter.
$M_{s\ max}$	Maximum voltage conversion ratio of the BSC.
n	Variable that indicates the order of the harmonic.
p_1, p_2	Flip-flop set and reset pulses.
p_b	Power sent to the battery.

P_b	Average power sent to the battery.
P_{in}	Peak value of the power absorbed by the converter from the input line.
p_m	Instantaneous input power.
P_{ls}	Series resonant inductor volt-amp product.
p_o	Power sent by the resonant circuit to the output stage.
P_o	Averaged power sent by the resonant circuit to the output stage.
Q_s, Q_{s1}, Q_{s2}	Quality factor of a series resonant circuit.
Q_{s_max}, Q_{s1_max}	Maximum value of Q_s when operating with unity power factor and constant output voltage.
Q_p	Quality factor of a parallel resonant circuit.
R_{eq}	Equivalent load resistance for the resonant circuit.
R_L	Load resistance.
R_p	Sawtooth reset pulse.
s	Laplace complex variable.
s_m	Switch that defines the operating mode of the UPS.
s_t	Sawtooth signal.
t	Time in seconds.
v_{ab}	Voltage across the output terminals of the inverter.
v_{ab1}	Voltage across the output terminals of line side converter.
V_{ab1}	Phasor associated with the first harmonic of the voltage v_{ab1}.
v_{ab2}	Voltage across the output terminals of the battery side converter.

V_{ab2}	Phasor associated with the first harmonic of the voltage v_{ab2}.
v_{ao}, v_{ao1}	Voltage between the center point of leg A and negative rail of the input dc bus.
v_{b_f}	Battery floating voltage.
v_{b_min}	Lowest voltage v_b that the BSC keeps constant the output voltage.
v_{bo}, v_{bo1}	Voltage between the center point of leg B and negative rail of the input dc bus.
v_{ao2}	Voltage between the center point of leg A and negative rail of the battery side dc bus.
v_{bo2}	Voltage between the center point of leg B and negative rail of the battery side dc bus.
v_{ca}	Control voltage that defines the angle γ .
v_{ca1}	Control voltage that defines the angle γ_1.
v_{ca2}	Control voltage that defines the angle γ_2.
v_{cin}	Voltage at the input of the inverter.
$\overline{v}_{cin}$	Voltage at the input of the inverter averaged over one switching interval.
v_{cp}	Voltage across the parallel resonant capacitor.
$\hat{v}_{cp}$	Peak value of the voltage across the parallel resonant capacitor.
$\hat{v}_{cp}$	Peak value of the first harmonic component of the voltage across the parallel resonant capacitor
V_{cp}	Phasor associated with the first harmonic of v_{cp}.

v_{cs}, v_{cs2}	Voltages across the series resonant capacitor.
v_{cs_rms}	Rms value of the voltage across the series resonant capacitor computed over one switching period.
v_g	Voltage across the output terminals of the input diode rectifier.
V_g	Dc voltage across the input terminal of the inverter.
$\hat{v}_g$	Peak value of v_g
$\hat{v}_{gm}$	Minimum Peak value of v_g.
v_{gs1}, v_{gs2}, v_{gs3}, v_{gs4}	Gate to source voltages for the transistors 1 to 4 of the inverter at the line side.
v_{gs1b}, v_{gs2b}, v_{gs3b}, v_{gs4b}	Gate to source voltages for the transistors 1 to 4 of the inverter at the battery side.
v_{in}	Ac input voltage
v_o	Output dc bus voltage.
v_{o_ac}	UPS output voltage.
$\overline{v}_o$	Voltage v_o averaged over one switching interval.
V_o	Voltage v_o average over one input line cycle interval.
V_p	Peak value of the constant sawtooth waveform.
v_{ps}	Peak value of the sine component of the first harmonic component of the voltage across the parallel resonant capacitor.
v_{pc}	Peak value of the cosine component of the first harmonic component of the voltage across the parallel resonant capacitor.

v_s	Voltage across the series resonant capacitor.
v_{s1}	Peak value of the sine component of the first harmonic component of the voltage across the series resonant capacitor.
v_{sc}	Peak value of the cosine component of the first harmonic component of the voltage across the series resonant capacitor.
x	Feedback variable.
xs	Internal variable of the sawtooth generator.
α	Switching frequency ratio.
β, β_1, β_2	Ratio between the series and parallel resonant capacitor.
γ	Control Angle. It is defined as the angle measured from the zero crossing point of the feedback variable to the next transition of the voltage v_{ab} .
γ_1, γ_{1a}	Control Angle. It is defined as the angle measured from the zero crossing point of the current $-i_{s1}$ to the next transition of the voltage v_{ao}, v_{ao1}.
γ_2, γ_{1b}	Control Angle. It is defined as the angle measured from the zero crossing point of the current i_{s1} to the next transition of the voltage v_{bo}, v_{bo1}.
γ_{2a}	Control Angle. Line operating mode: It is defined as the angle measured from the zero crossing point of the current i_{s1} to the next transition of the voltage v_{ao2} . Backup mode: It is defined as the

angle measured from the zero crossing point of the current $-i_{s2}$ to the next transition of the voltage v_{ab2} .

γ_{2b} Control Angle. It is defined as the angle measured from the zero crossing point of the current i_{s2} to the next transition of the voltage v_{ba2} .

γ_3 Control angle of the OSC.

ω_{60} Input ac line frequency in rad/s.

ω Frequency in rad/s.

ω_o Natural frequency of a LC circuit in rad/s.

ω_s Switching frequency in rad/s.

ψ Angular position in rad.

CHAPTER 1: INTRODUCTION

1.1 GENERAL INTRODUCTION

Uninterruptible power supply systems have been extensively applied to feed critical loads in many areas. Typical examples of critical loads in low and medium power application are life-support equipment, computers and telecommunication systems [1,2]. Although all uninterruptible power supplies have a basic feature that is to provide continuous power to a critical load, the emerging hybrid fiber-coaxial networks (Appendix 6) have created the need for a specific type of uninterruptible power supplies [6-11].

Ferroresonant based ac power supplies have been used by the cable television industry to feed the existing hybrid fiber-coaxial (HFC) networks [12,13]. However, as the cable industry upgrades their networks to provide reliable voice services, and the telephone industry moves into the digital data era, more stringent requirements, such as higher efficiency, smaller size, and electrical performances are being imposed on these power supplies. As a result, low efficiency and bulky ferroresonant power supplies will have to be replaced by more efficient and smaller uninterruptible power supplies based on high switching frequency converters.

Most of the conventional uninterruptible power supply (UPS) topologies [14-32] are not suitable to feed HFC networks. One example of this incompatibility is the line interactive type of UPS [14-23]. In a line interactive UPS the output voltage and the incoming ac line voltage are interfaced using a synchronous reactor. These two voltages

are synchronized and the displacement angle between them determines the amount of power sent to the load and to the battery. This type of UPS is not suitable for powering HFC networks, since in this application the input and output voltages have different waveforms. The input voltage is usually sinusoidal which comes from either the available utility grid or from a backup engine-alternator, while the output is usually a trapezoidal voltage, which has a frequency that may be different from the incoming ac source [6,11]. Another example is the conventional rectifier-inverter type of uninterruptible power supply [26-32]. This type of UPS provides no galvanic isolation for the battery from the output or from the input [33], and it usually requires high battery voltage [26-32]. Furthermore, a number of UPS topologies [8,12,14,33,24,25,27] require bulky and heavy low frequency isolation transformer(s) to provide isolation for the critical load [34,35].

On the other hand, power factor correction circuits (PFC) have been incorporated in electronic equipment that are intended to be connected to the utility grid to reduce the utility grid voltage distortions, which are caused by nonlinear electronic loads [3], as well as to maximize the power that can be extracted from the utility grid [36]. This trend is promoted by international agencies such as the International Electrotechnical Commission (IEC) who propose standards that impose limits on the magnitude of current harmonics injected by equipment connected to the utility grid. To meet these standards, a PFC is usually required. In the case of ac-dc converters great effort has been put to find topologies which incorporate the function of PFC and dc-dc conversion in a single circuit [37-42]. However, so far, practical integrated PFC and ac-dc-ac converters required for UPS applications, have not been proposed.

In addition, to reduce the size and weight of the filters and transformers of the UPS operation at high switching frequency is required [35]. However, in hard-switch based UPS the switching losses are proportional to the switching frequency. Therefore, the reduction of size and weight is limited by the switching losses. To overcome this limitation, the switching losses must be reduced or even eliminated. This can be accomplished by rendering the voltage across the switches and/or the current through them equal to zero during the commutations. Two types of commutations can be characterized according to the variable that is made equal to zero. In a zero voltage switching (ZVS) commutation, as the name implies, the voltage across the switch is zero during the commutation. Similarly, in a zero current switching (ZCS) commutation the current through the switch is zero during the commutation. To achieve ZVS or ZCS, capacitors, inductors, and additional switches have been used to bring the voltage or the current to zero [43-55]. As UPS are usually comprised of many converters, a soft-switching circuit is required for each one of these converters. Therefore, this increases the complexity and component-count when compared with its hard-switched counterpart. Alternatively, resonant techniques provide a means to use a single soft-switching circuit, a resonant circuit, to achieve ZVS [52,53] (or ZCS [54]) to all converters in a multi-converter arrangement. To date, however, the solutions proposed require, either a large number of switches [52], or introduce flux imbalance in the high frequency transformer [54].

This thesis focuses on the development, analysis, and design of new ac single-phase UPS topologies that overcome the drawbacks of existing UPS topologies in general and are suitable for powering the emerging hybrid fiber-coaxial networks. The proposed

UPS topologies use high frequency resonant links to provide high input power factor as well as to produce desired output waveform with a minimum number of conversion stages between the input and output. A new control technique for the proposed converters is introduced which ensures the operation of the UPS with soft-switching under all operating conditions. Together with the high frequency link and the new control technique, it will now be possible to design small, lightweight and efficient UPS for the new emerging application. In this thesis, design procedures and experimental results are given to support the analysis presented, and to demonstrate the feasibility of the proposed UPS topologies and control schemes.

1.2 CONVENTIONAL UNINTERRUPTIBLE POWER SUPPLIES

A number of different UPS topologies have been reported in the literature. Among them, the following are the candidate topologies for powering the emerging hybrid fiber-coaxial networks.

- Ferroresonant based uninterruptible power supply [12].
- Low frequency transformer based uninterruptible power supply [8].
- Conventional high frequency transformer based uninterruptible power supply [31].

1.2.1 Ferroresonant Based Uninterruptible Power Supply

Fig. 1.1 shows the basic circuit diagram of a ferroresonant based UPS. It is well known that this topology is simple and rugged, since its main elements are an inverter and a ferroresonant transformer. However, it has the following disadvantages:

(i) It has poor quality of the output voltage waveform [12,13], which can adversely affect the power delivery capability of the network, and can cause malfunctioning of the amplifiers connected to it.

(ii) It is bulky and heavy.

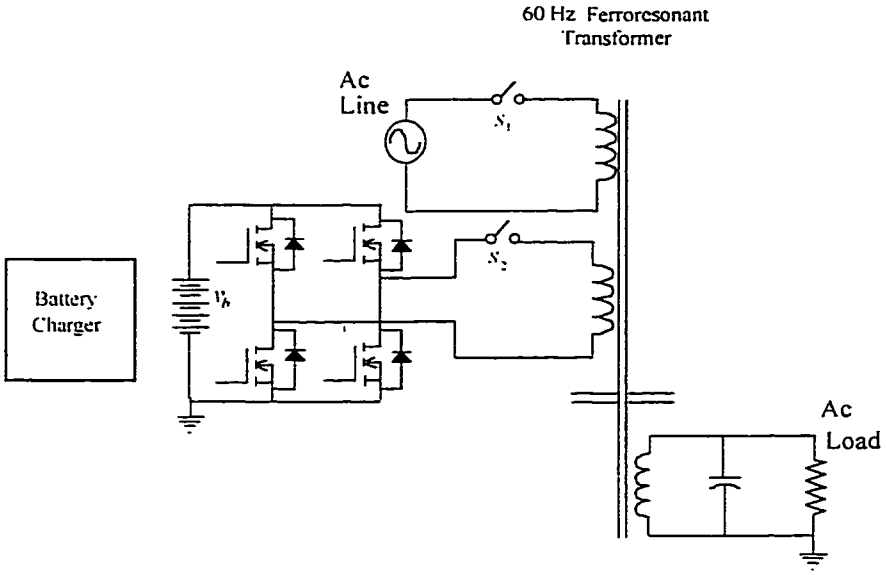


Fig. 1.1 Power circuit diagram of a ferroresonant based UPS.

1.2.2 Conventional low frequency transformer-based Uninterruptible Power Supply.

This topology has its origin in the single UPS unit with separate battery charger [1,2] and was proposed by [24] as an alternative method for powering HFC networks. The reported performance of this power supply is proved superior in comparison to that of the ferroresonant based UPS [12,25]. However, it has the following disadvantages:

(i) It requires a bulky low frequency transformer.

(ii) There is no isolation between input and the battery.

(iii) It requires high voltage storage batteries for backup power.

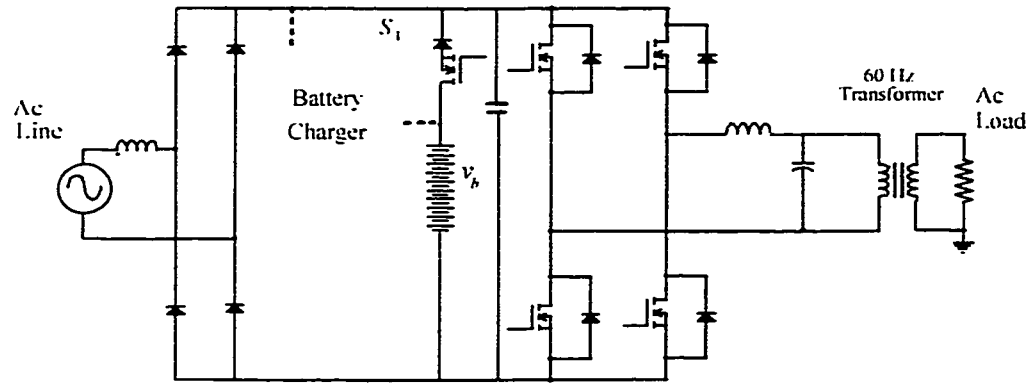


Fig. 1.2 Conventional low frequency transformer-based UPS.

1.2.3 Conventional high frequency transformer-based Uninterruptible Power Supply

The conventional rectifier-inverter UPS configuration [1] can be used to eliminate the bulky low frequency transformer of the above-mentioned topologies. This is accomplished by implementing the input stage using a switching mode rectifier [26]. Fig. 1.3 shows a UPS configuration where the rectifier is comprised of a boost pre-regulator cascaded with a dc-dc resonant converter. At the output side another boost converter is used to step-up the battery voltage to a value higher than the peak of the trapezoidal waveform. Finally, the output PWM inverter is used to generate the trapezoidal ac waveform from the output dc bus.

Admittedly, this topology allows the design and optimization of each conversion stage independently. However, this topology has the following disadvantages:

(i) It has a large number of conversion stages in cascade.

(ii) It needs a soft-switching circuit for each conversion stage in order to operate with high switching frequency, low level of noise, and high efficiency.

(iii) It does not provide galvanic isolation for the battery from the output.

A detailed comparison of above described UPS topologies is given in the Appendix 7.

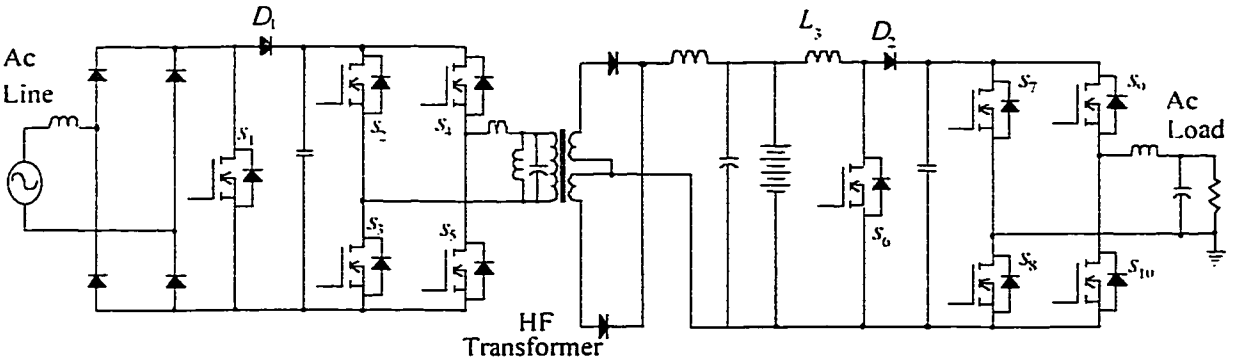


Fig. 1.3 Conventional high frequency transformer based UPS.

1.3 Derivation of Uninterruptible Power Supply Topologies for Powering Hybrid-Fiber Coaxial Networks

In this section uninterruptible power supply topologies, which are suited for powering fiber-coaxial networks, are derived. These UPS provide isolation for the input, battery, and output from each other by means of high frequency transformers. In addition, to satisfy the stringent harmonic pollution restrictions imposed by regulatory agencies [3], the derived power supplies operate with high input power factor and low input current total harmonic distortion. The generic block diagram representation a UPS is shown in Fig. 1.4. It consists of converters that interface the incoming ac line, the battery and the output. Furthermore, in Fig. 1.4 a capacitor is used to represent the element that absorb the differences between the incoming and outgoing power of the UPS.

A trivial implementation of the uninterruptible power supply of Fig. 1.4 can be obtained from the rectifier-inverter UPS configuration by introducing an isolation stage between the battery and the output. As a result, the UPS takes the form as shown in Fig. 1.5, where the storage element, which is indicated in Fig. 1.4, is in the isolated switching mode rectifier (SMR).

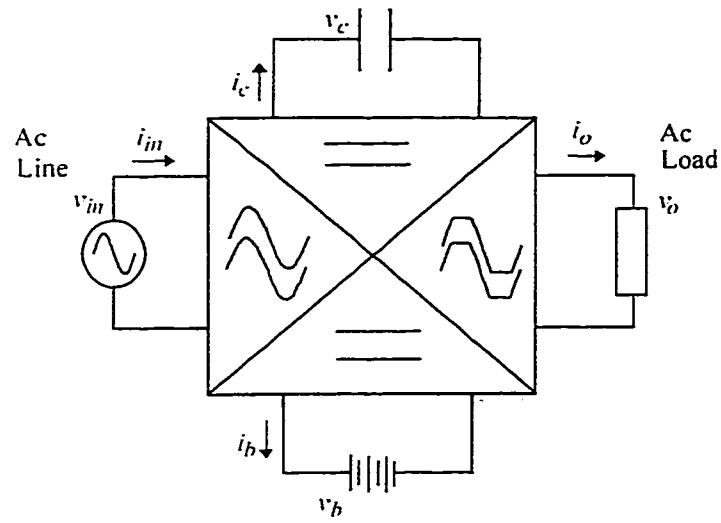


Fig. 1.4 Generic block diagram of UPS.

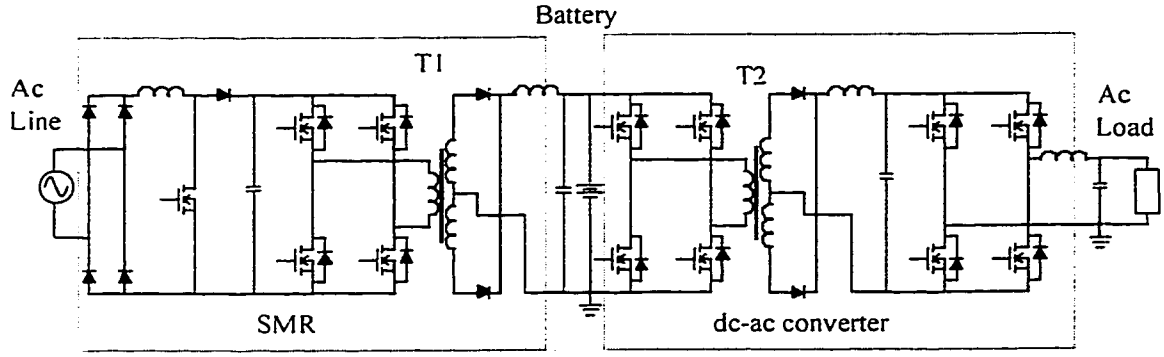


Fig. 1.5 Cascade implementation of the uninterruptible power supply with two high frequency isolation transformers.

The UPS of Fig. 1.5 has a large number of converters connected in cascade, which penalizes the overall efficiency of the UPS. It is worth mentioning that to ensure soft-switching operation, auxiliary circuits must be added to each conversion stage, and as a result, this will further increase the complexity and component-count of this topology.

An alternative UPS topology is shown in Fig. 1.6. This topology has its roots in the single UPS unit with separate battery charger [1.2]. By taking the UPS unit with separate battery as the starting point, the UPS of Fig. 1.5 can be obtained by implementing the input rectifier stage with an isolated SMR, and by introducing a

conversion stage with isolation between the battery and the dc link. This converter is kept inactive when the incoming ac line voltage is within the acceptable input voltage range. In this way, it acts as the blocking device of the single UPS unit with separate battery charger. Whenever the incoming ac line fails, this converter transfers power from the battery to the output side providing continuous operation to the critical load. The main advantage of this UPS, as compared to that of Fig. 1.5, is the reduced number of conversion stages in cascade between the input and the output. However, it still has many semiconductors and requires auxiliary circuits for each conversion stage to provide soft-switching operation. In addition, two isolation transformers are used in this topology.

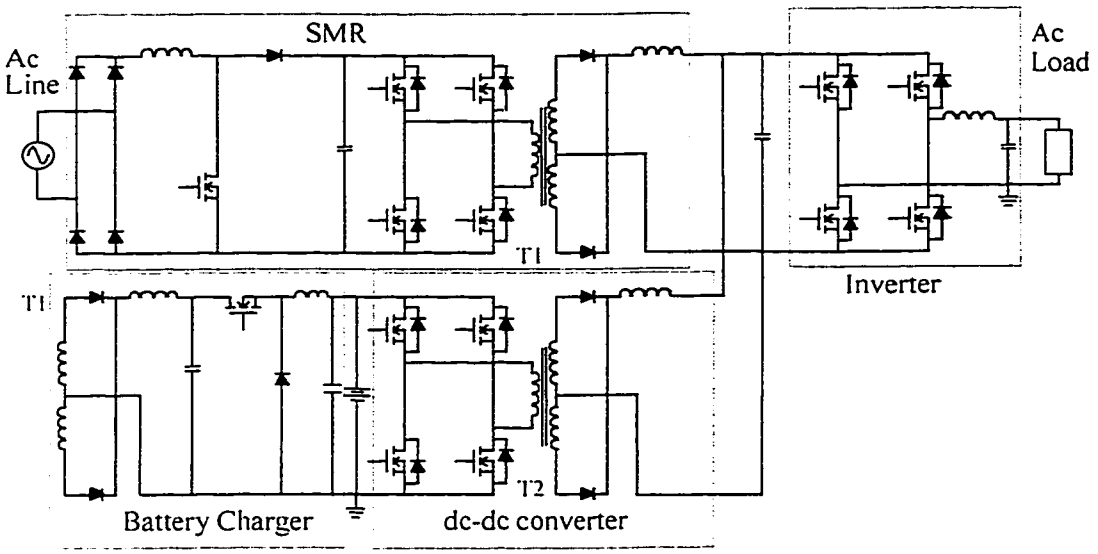


Fig. 1.6 Single UPS unit with separate battery charger implemented with two high frequency transformers.

A UPS system implemented using the concept of high frequency ac link [52] would have a single-phase ac voltage link operating at high frequency and a single high frequency transformer to connect the input, output and battery side converter. Admittedly, the switching losses are reduced by restricting the converter switching instants to the zero crossing point of the high frequency link voltage. However, these

topologies have at least one of the following disadvantages: (i) the large number of semiconductor switches; (ii) the voltage stresses in the switches are at least 1.57 times greater than the input (or output) voltage; (iii) low frequency components are introduced in the input and output due to the modulation scheme, named pulse-density modulation [52].

1.3.1 Proposed UPS topology

The minimum number of transformers required to provide galvanic isolation for input, battery and output from each other is one. Fig. 1.7 shows a UPS topology with a single high frequency transformer. This UPS topology has a point of common connection between the line side converter (LSC), battery side converter (BSC), and output side converter (OSC), that is the high frequency transformer. This creates the possibility of using a single soft-switching circuit for the three converters of the UPS. Although different soft-switching techniques have been developed in the last two decades [43-52], the majority of them are not suitable for power conversion systems with more than one type of load and source.

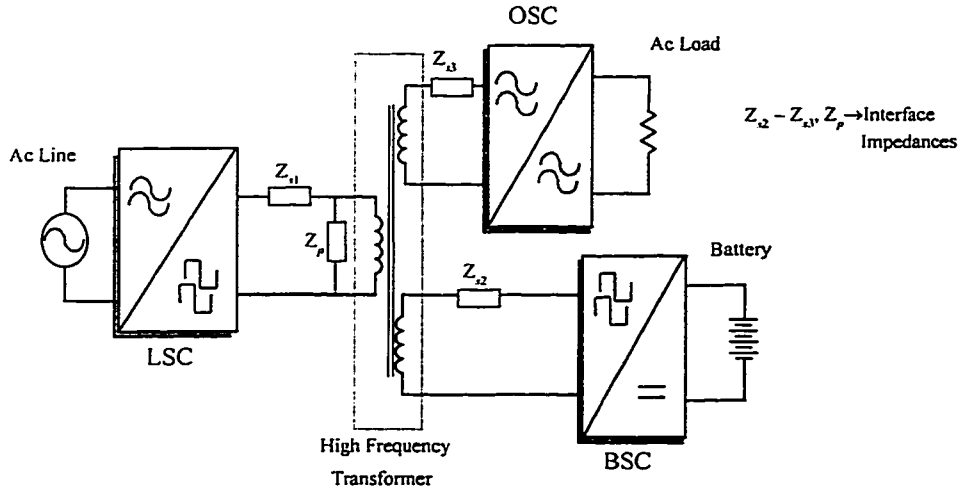


Fig. 1.7 Block diagram representation of single high frequency transformer UPS.

The impedances in the UPS of Fig.1.7 can take the form of resonant circuits to provide efficient interface among the various converters and simultaneously allow zero voltage switching commutation for the semiconductor switches. Fig.1.8 shows such implementation of the UPS of Fig. 1.7 using series-parallel resonant circuits [56.57]. In addition to the above benefits, the proposed resonant UPS can operate with high input power factor at the input ac line without using a dedicated PFC stage [56-60].

The successful implementation of the proposed UPS depends upon the minimization of the components rating and elimination of the switching losses under all input ac line voltages and output load conditions. In order to achieve this, the power circuit parameters must be carefully selected and the converters must be appropriately controlled.

This thesis is, therefore, focussed on the analysis, design and implementation of such a UPS. The following section presents the detailed objective of this thesis.

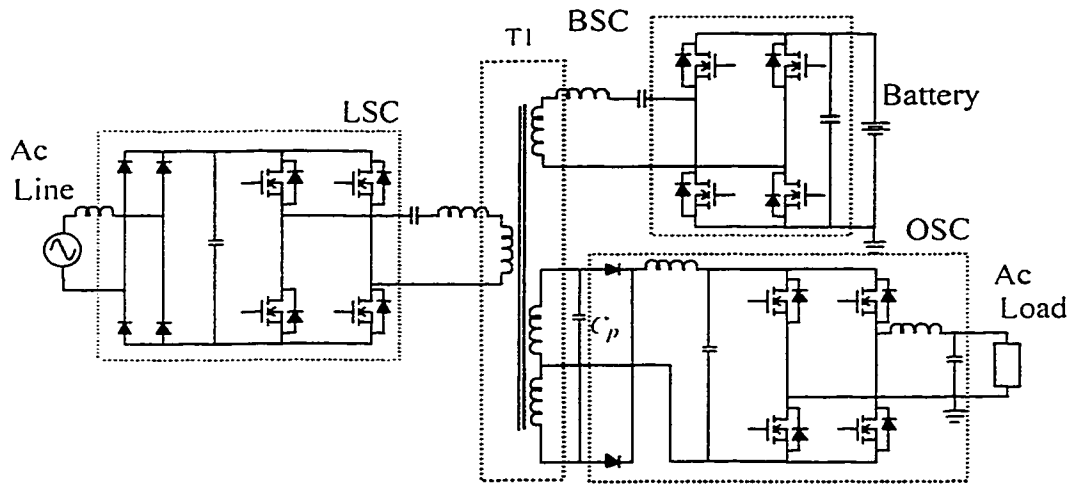


Fig. 1.8 Proposed single transformer UPS based on series-parallel resonant converters.

1.4 THESIS OBJECTIVE

The scope of this thesis is to present, analyze, design, and verify experimentally resonant converters for uninterruptible power supplies. The converters considered are of the voltage-fed resonant type operating with zero voltage switching. The main objectives of the thesis are:

(i) To propose single-phase high frequency transformer resonant based UPS topologies that allow operation at high frequency, hundreds of kHz, without commutation losses. These UPSs should produce high quality input and output waveforms.

(ii) To develop a control technique for the proposed converter which ensures operation with ZVS under all operating conditions, and to investigate its applicability for other classes of resonant converters.

(iii) To develop and verify experimentally design procedures for the proposed converters that will allow proper selection of the power circuit components, so that the stresses in the power circuit are minimized.

(iv) To recognize potential problems and propose viable solutions to optimize the performance of the proposed UPS topology mostly in terms of the efficiency and input power factor.

(v) To verify the feasibility of the proposed converters and control technique with experimental results obtained from laboratory prototypes.

1.5 THESIS OUTLINE

This thesis is divided into six chapters. A brief description of Chapters 2 to 6 is given below.

Chapter 2 proposes a new control technique for voltage-fed resonant converters. Unlike the conventional variable frequency control that imposes the switching frequency externally, the proposed scheme is based on controlling the phase shift angle between one of the resonant circuit variables and the voltage at the output of the inverter. It is demonstrated that this approach ensures operation with zero voltage switching under all operating conditions. The static characteristics and dynamic models of a series-parallel resonant converter with the proposed controller are derived. Experimental results on a 1kW prototype are included to confirm the feasibility of the proposed technique.

Chapter 3 presents the analysis and design of a single-phase single-stage unity power factor ac-dc converter employing a series-parallel resonant converter operating in self-sustained oscillating mode. The controller proposed in Chapter 2 is used to ensure zero voltage switching along all points of the input voltage and for each value of load current. In addition, a simplified control technique that improves the input power factor without resorting to active control of the input current is suggested. The performance of an ac-dc converter with the proposed control schemes is verified experimentally on a laboratory prototype. In addition, this chapter modifies the self-oscillating controller proposed in Chapter 2 for operation with variable frequency plus phase shift modulation. This technique is applied to a single-stage ac-dc series parallel resonant converter operating with unity power factor. The results obtained show that a narrow switching frequency range, and reduced current stresses, are achieved with the combination of

phase shift modulation and variable frequency control. Analysis and design guidelines are provided and key predicted results are experimentally verified on a laboratory prototype.

In Chapter 4 an uninterruptible power supply based on series-parallel resonant converters is proposed. The operation of the line side converter is similar to the ac-dc converters presented in Chapter 3. However, the battery side converter operates in two different modes depending on the condition of the incoming ac line. By using a single high frequency transformer, it is demonstrated that ZVS, under the different operating conditions of the UPS, can be achieved. This results in low commutation losses and high efficiency. A design procedure is developed and applied to the proposed UPS operating with inductive and capacitive output filter. Experimental results obtained from laboratory prototypes validate the design procedure developed and demonstrate the converter performance.

In Chapter 5, ZVS bidirectional resonant converters are proposed. With these converters a novel UPS is proposed. This UPS features ZVS for all converters at all operating conditions, high input power factor, and galvanic isolation using high frequency transformers. Experimental results obtained from prototype are presented to illustrate the converter operation.

In Chapter 6, the thesis is summarized, conclusions based on the results obtained are drawn, and suggestions for future work are presented.

CHAPTER 2: ZERO VOLTAGE SWITCHING RESONANT CONVERTERS

2.1 INTRODUCTION

The converters of the resonant based UPS topology proposed in Chapter 1 can be operated at high switching frequency if the switching losses are not significant. In voltage fed load resonant converters, the switching losses can be eliminated by ensuring that the inverter output current lags behind the inverter output voltage. In this way, the inverter output current has the right polarity to charge and discharge the snubber capacitors, ensuring that the turn-on and turn-off of the switches take place under zero voltage, therefore eliminating the switching losses. A common approach of achieving zero voltage switching (ZVS) in resonant converters is to operate them above the resonant frequency [43,56,57], since in this switching frequency range the resonant circuit operates in the lagging power factor mode which is required to provide ZVS turn-on. However, the resonant frequency of these converters depends on the power circuit parameters and can vary significantly with the load, as in the case of series-parallel resonant converters [57]. Concerning the conventional variable frequency control, in order to guarantee ZVS under all load conditions, a lower limit must be imposed on the switching frequency. This limit must be much higher than the nominal resonant frequency, resulting in derating of the converter. In addition, for the proper operation of the proposed UPS topology of Fig. 1.8, the phase angle between the voltage produced by the Line Side Converter (LSC) and the Battery Side Converter (BSC) must be adjusted to

allow the proper control of the battery charging current. Although there are a number of control techniques for resonant converters, they all have at least one of the following limitations: (i) they are based on nonlinear control law which make their practical implementation complex with analog circuitry [65,66]; (ii) the control law is derived for a particular resonant circuit configuration [67-70]; (iii) the operation above the resonance frequency is largely dependent on the power circuit parameters [69].

In order to overcome the above-mentioned limitations, this chapter introduces a new control scheme for resonant converters. The main goal of this control scheme is to ensure ZVS condition for all operating points of the converter independent of the power circuit parameters. This is accomplished by making the converter operate in self-sustained oscillation mode where the phase angle between the inverter output voltage and one of the resonant circuit variables is directly controlled.

The remainder of this chapter is organized as follows: In Section 2.2, the operation of different resonant converters with the proposed controller is demonstrated, and the static characteristics of a series-parallel resonant converter with the proposed controller are derived. In Section 2.3, dynamic models of the series resonant converter with the proposed controller are derived. In Section 2.4, experimental results validate the analysis carried out in the previous sections and demonstrate the feasibility of the proposed scheme.

2.2 CONTROL OF RESONANT CONVERTERS IN SELF-SUSTAINED OSCILLATION MODE

In this section, the operating principle of the proposed controller is described. The operation of a number of resonant converters with this controller is examined and the range of the control variable for proper operation with ZVS is identified.

2.2.1 Proposed Controller Operating Principle

A necessary condition to achieve ZVS in voltage fed load-resonant converters is to have current i_s lagging the voltage v_{ab} at the inverter output terminals, as shown in Fig. 2.1. The phase angle between the current and the voltage at the inverter output terminals can be controlled by generating the inverter output voltage from the current i_s. Fig. 2.2 (a) shows the case where the voltage v_{ab} is generated by shifting the $-i_s$ by an angle γ. According to this figure, the current i_s lags the voltage v_{ab} if $90^o < \gamma < 180^o$. It is worth noting that the switching frequency is no longer externally imposed as in the conventional variable frequency control approach since the voltage v_{ab} is generated from the current i_s. As a result, the converter is said to operate in self-sustained oscillation mode. The question that arises at this point is associated with the existence of the self-sustained oscillation. In order to help answer this question, and to clarify the operation of the converter, a control block diagram interpretation of the converter with a controller that implements the operation described above is shown in Fig. 2.2 (b). The transfer function $G_{x\ v}(s)$ is associated with the resonant circuit. The input of the block associated with $G_{x\ v}(s)$ is the inverter output voltage and the output is the current i_s. The output is named x, instead of i_s, since the self-sustained oscillations can be achieved with a feedback variable other than i_s, as will be demonstrated in the next section. The controller

is represented by a transportation delay, which shifts in time the feedback variable to provide the required phase angle between the v_{ab} and i_s. Finally, a hard-limit block is used to represent the inverter. In next sub-section, the existence of the self-sustained oscillation in different resonant converters will be investigated.

2.2.2 Characterization of the Self-Sustained Oscillations

The describing function method [71] can be conveniently used to determine the existence of self-sustained oscillations as well as to determine stability of the system of Fig. 2.2 (b). For the application of the describing function method, based on the first harmonic component, the filtering condition must be satisfied. This condition requires that the linear part of the system must attenuate the high order harmonics produced by the nonlinearity in the system. Indeed, this condition is satisfied for resonant converters operating above the resonant frequency. Resonant converters, when operating above the resonant frequency, have a low pass filter characteristic resulting in a predominant first harmonic component in the resonant circuit variables. Therefore, the representation of the resonant circuit variables by their first harmonic component is plausible since the higher order harmonics are significantly attenuated.

According to the describing function method the nonlinear element -the controller plus the inverter- is represented by its describing function. An ideal inverter with the controller as shown in Fig. 2.2 (b) are represented by the following describing function:

$$N(A,\gamma) = \frac{4\,v_g}{\pi\,A}(\cos(\gamma) - j\sin(\gamma)) \tag{2.1}$$

where A is the amplitude of the first harmonic component of the feed-back variable x, v_g is the amplitude of the inverter input voltage, and γ is the control angle.

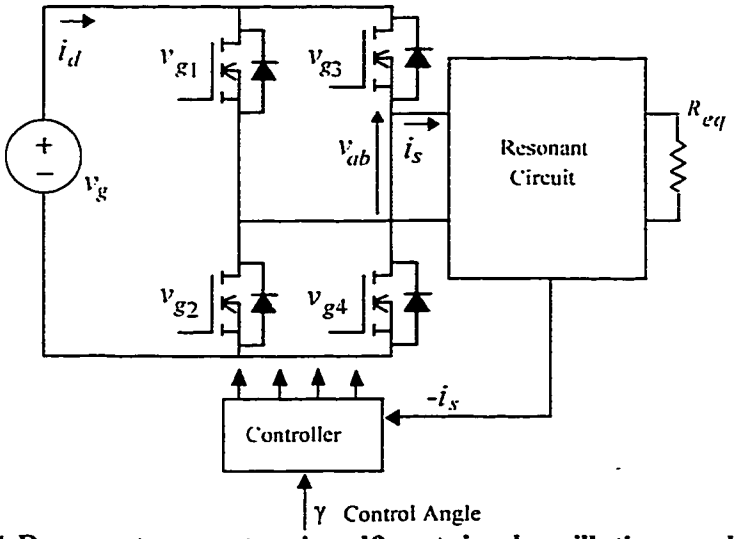


Fig. 2.1 Resonant converters in self-sustained oscillation mode.

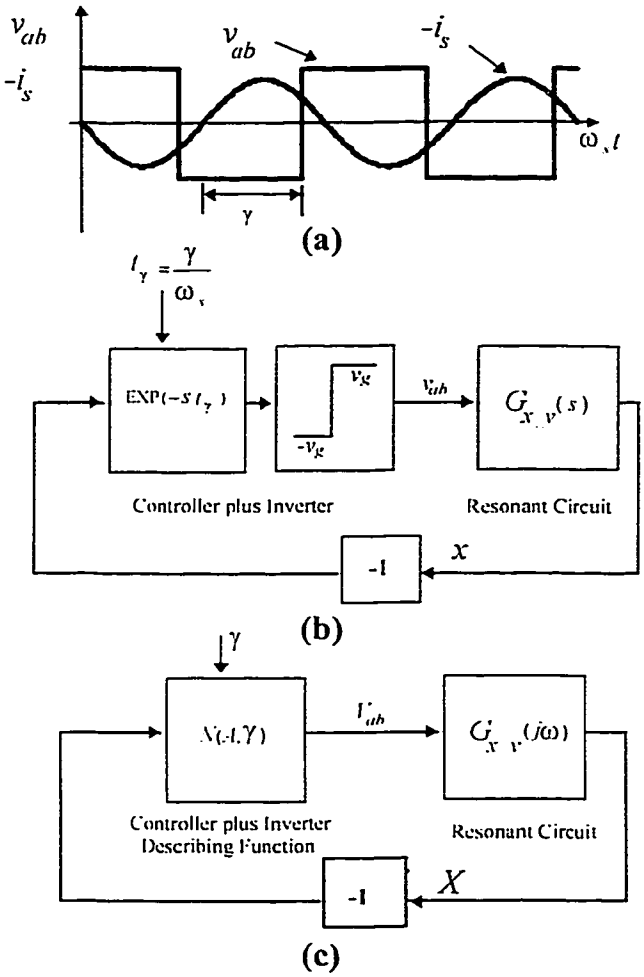


Fig. 2.2 Phase angle control of resonant converters

(a) Relevant circuit waveforms. (b) Block diagram interpretation.
(c) Describing function representation of (b).

Let us assume that there is a self-sustained oscillation of amplitude A and frequency ω in the system of Fig. 2.2 (b). Then, by replacing the nonlinearity associated with the controller and inverter by the describing function (2.1), the block diagram of Fig. 2.2(b) becomes as shown in Fig. 2.2 (c). The variables of the loop of Fig. 2.2 (c), V_{ab} and X ,are the complex quantities associated with the first harmonic component of v_{ab} and x respectively, and they must satisfy the following relations:

$$V_{ab} = N(A,\gamma)(-X) \text{ and} \tag{2.2}$$

$$X = G(j\omega)V_{ab} \ . \tag{2.3}$$

Therefore, since X is different than zero, the above equations can be written as

$$G_{x\ v}(j\omega) = -\frac{1}{N(A,\gamma)}. \tag{2.4}$$

The amplitude A and frequency ω that satisfy (2.4) are the amplitude of the first harmonic component of the feedback variable and the switching frequency of the converter ω_s respectively. Graphical solution of (2.4) can be obtained by plotting the loci of the negative inverse of the describing functions (2.1) and sinusoidal transfer function from the inverter output voltage to the feedback variable in the complex plane, as shown in Fig. 2.3.

The intersection point of the loci of Fig. 2.3 presents a possible operating point of the converter. The stability of the self-sustained oscillation can be investigated by using the extended Nyquist stability criterion [71].

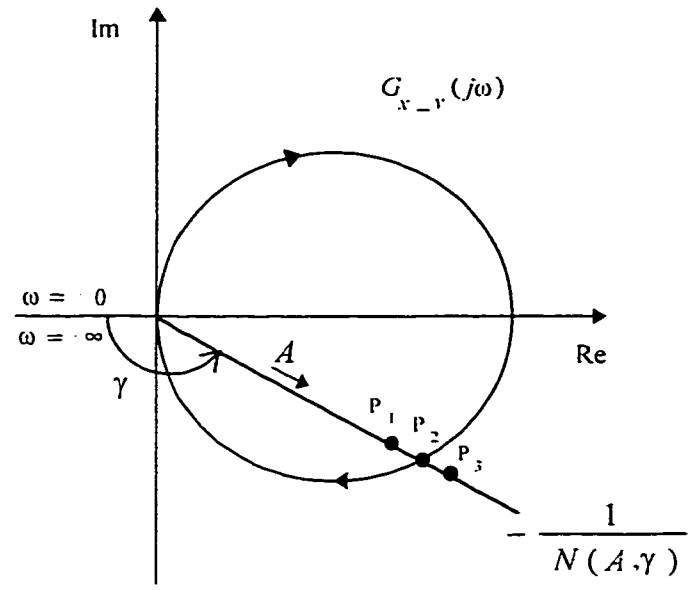


Fig. 2.3 Determination and stability of the self-sustained oscillation.
The arrow over the locus $1/N(A,\gamma)$ indicates the direction of increasing values of A.

Let us assume that the system initially operates at point P_2, with a self-sustained oscillation of amplitude A, and frequency ω_s, and due to a small disturbance, the amplitude of the feed-back variable is slightly increased, and the system operating point is moved from P_2 to P_1. Since the new point P_1 is encircled by the curve of $G_{x\_v}(j\omega)$, and taking into account that $G_{x\_v}(j\omega)$ has all poles and zeros in the right half plane, according to the extended Nyquist criterion, the converter at this operating point is unstable, and the amplitudes of the converter signals will increase. Therefore, the operating point will move along the curve $-1/N(A)$ toward the operating point defined by P_2. On the other hand, if the converter is disturbed so that the amplitude of A is increased, with the operating point moved to the point P_3, then the amplitude A will decrease since P_3 is not encircled by the curve $G_{x\_v}(j\omega)$ and thus converter at this operating point behaves as a stable system according with the extended Nyquist criterion. From the above discussion

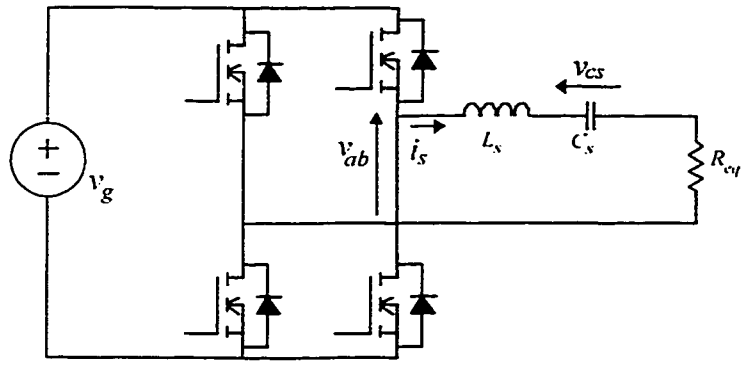
it is concluded that the self-sustained oscillation associated with the intersection point P_2 is stable.

In order to demonstrate the applicability of the above self-sustained oscillation method to ensure ZVS in resonant converters, the proposed controller is applied to the three basic resonant converter topologies, namely (i) series resonant, (ii) parallel resonant, and (iii) series-parallel resonant in the following sub-sections.

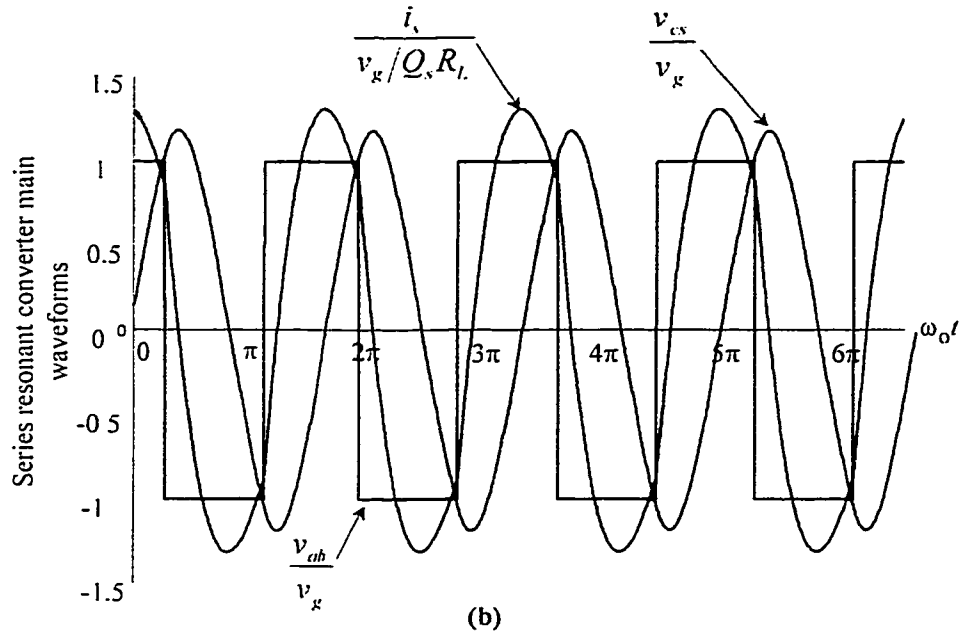
2.2.2.1 Voltage Fed Series Resonant Converter

A series resonant converter often operates from an input voltage, which is in Fig. 2.4 (a) represented by v_g. The resonant converter usually consist of a full bridge inverter and a resonant circuit, (L_s, C_s), which is placed between the inverter and the load. The full bridge inverter converts the voltage v_g into an alternate high frequency voltage v_{ab}, which in turn, feeds the resonant circuit and the load. In Fig. 2.4 the load is represented by the equivalent ac resistor R_{eq}. When the load is comprised of a diode rectifier followed by a capacitive output filter the equivalent ac resistor is given by $R_{eq} = 8/\pi^2 R_L$, where R_L is actual load resistance [57]. The main waveforms of the series resonant converter operating above the resonant frequency are shown in Fig. 2.4 (b).

The current through the resonant inductor and the voltage across the series resonant capacitor have a predominant first harmonic component and can easily be measured through current and voltage transformers. Therefore, both are considered as candidates for the feedback variable x.



(a)



(b)

Fig. 2.4 Series resonant converter.
(a) Power circuit diagram. (b) Main waveforms, Q_S=1, ω_s/ω_o=1.18

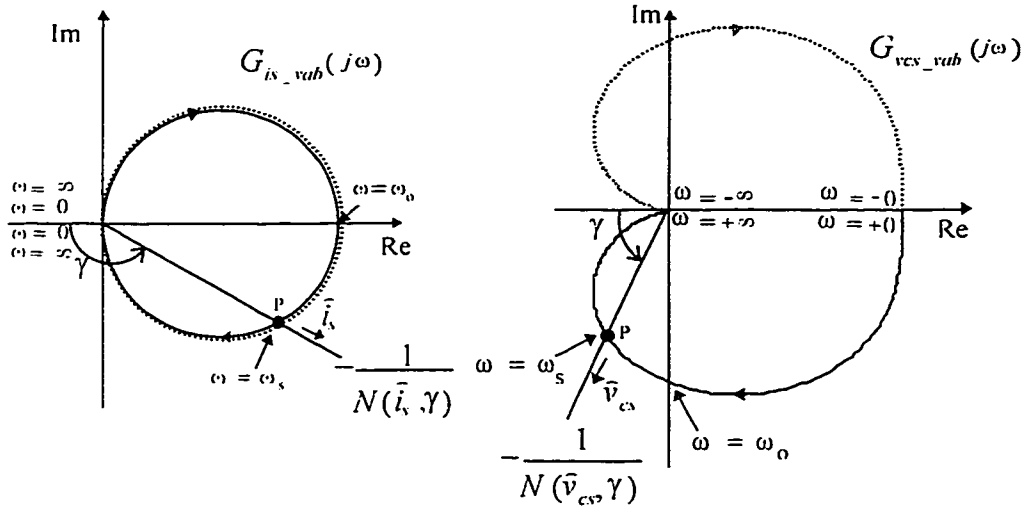
The transfer functions from the inverter output voltage to the resonant current i_s, and to the capacitor voltage v_{cs} are represented by G_{is_vab} and G_{vcs_vab} respectively, and are given by:

$$G_{is\_vab}(s) = \frac{\frac{s}{\omega_o Q_s R_L}}{\frac{s^2}{\omega_o^2} + \frac{s}{\omega_o}\frac{8}{\pi^2 Q_s} + 1} \tag{2.5}$$

$$G_{vcs\_vab}(s) = \frac{1}{\frac{s^2}{\omega_o^2} + \frac{s}{\omega_o}\frac{8}{\pi^2 Q_s} + 1} \tag{2.6}$$

where $Q_s = \frac{\omega_o L_s}{R_L}$ and $\omega_o = \frac{1}{\sqrt{L_s C_s}}$.

The plots of the transfer functions (2.5) and (2.6) in the complex plane are shown in Fig. 2.5. The arrows over the loci of the negative inverse describing functions of the nonlinearities indicate the direction of increasing amplitude of the feedback variables.



(a) **(b)**

Fig. 2.5 Determination of self-sustained oscillation in series resonant converters.

The plot of the sinusoidal transfer functions $G_{is\_vab}(j\omega)$ and $G_{vcs\_vab}(j\omega)$, and the negative inverse describing function of the nonlinearity associated with the inverter and its controller. **(a)** The case where the feedback variable is the current through the resonant inductor. **(b)** The case where the feedback variable is the voltage across the series resonant capacitor.

Fig. 2.5 (a) corresponds to the case where the current through the resonant inductor is used to generate v_{ab}, that is $x = i_s$. The amplitude of the first harmonic component of the feedback variable, A, is denoted as $\tilde{i}_s$. In this case if $90° < \gamma < 180°$, a stable limit cycle exists, as can be concluded from Fig. 2.5 (a) by applying small disturbance in $\tilde{i}_s$ at the intersection point P. Furthermore, when $90° < \gamma < 180°$ operation with ZVS can be achieved since the current i_s lags the voltage v_{ab} at the inverters output.

A similar conclusion can be drawn from the plot of Fig. 2.5 (b). This plot corresponds to the case where the voltage across the series resonant capacitor is used to generate the voltage v_{ab}. In this case, $x = v_{cs}$, and $\tilde{v}_{cs}$ is used to denote the amplitude of the first harmonic component of v_{cs}, that is $A = \tilde{v}_{cs}$. If $0 < \gamma < 90°$ a stable limit cycle exists as can be concluded by applying small disturbance in $\tilde{v}_{cs}$ at the intersection point P. For $0 < \gamma < 90°$ the voltage v_{cs} lags the voltage v_{ab} and so does the current i_s. As a result ZVS can be achieved in this control angle range.

2.2.2.2 Voltage Fed Parallel Resonant Converter

In voltage fed parallel resonant converters the load is connected in parallel with the resonant capacitor, C_p, as shown in Fig. 2.6 (a). When output stage is comprised by a diode rectifier followed by an inductive filter the ac equivalent resistor is given by $R_{eq} = \pi^2/8\, R_L$, where R_L is actual load resistance [57]. The main waveforms of the parallel resonant converter operating above the resonant are shown in Fig. 2.7(b).

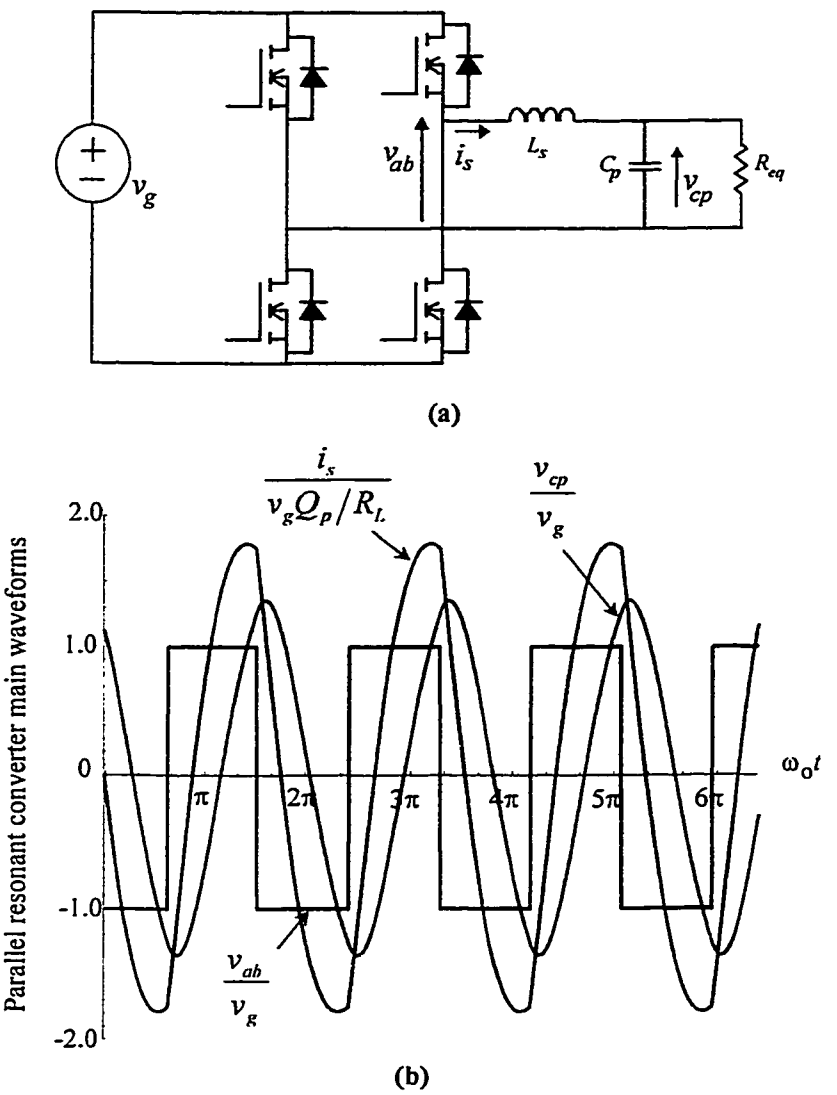


Fig. 2.6 Parallel resonant converter.
(a) Power circuit diagram. (b) Main waveforms, Q_p=1, ω_s/ω_0=1.12

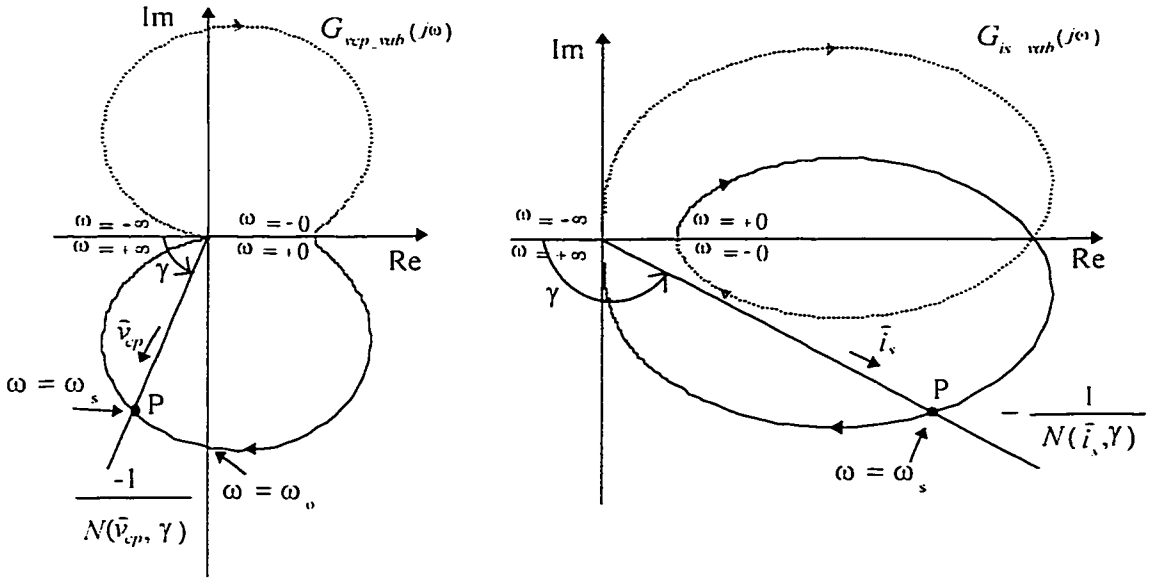
For parallel resonant converters operating above the resonant frequency, the two natural candidates for the feedback variable are the current through the resonant inductor and the voltage across the parallel resonant capacitor. The transfer functions from the inverter output voltage to the resonant current i_s, and to the parallel resonant capacitor voltage v_{cp} are represented by G_{is_vab} and G_{vcp_vac} respectively, and are given by:

$$G_{is\_vab}(s) = \frac{\frac{s}{\omega_o}\frac{Q_p\pi^2}{8}+1}{\frac{s^2}{\omega_o^2}+\frac{s}{\omega_o}\frac{8}{\pi^2 Q_p}+1}\frac{8}{\pi^2}\frac{1}{R_l} \tag{2.7}$$

$$G_{vcp\_vab}(s) = \frac{1}{\frac{s^2}{\omega_o^2}+\frac{s}{\omega_o}\frac{8}{\pi^2 Q_p}+1} \tag{2.8}$$

where $Q_p = R_L / \omega_o L_s$ and $\omega_o = \frac{1}{\sqrt{L_s C_p}}$.

The frequency responses associated with these transfer functions are shown in Fig. 2.7.



(a) **(b)**

Fig. 2.7 Determination of self-sustained oscillation in parallel resonant converters.
The plot of the sinusoidal transfer functions $G_{is\_vab}(j\omega)$ and $G_{vp\_vab}(j\omega)$, and the negative inverse describing function of the nonlinearity $N(.)$. **(a)** The case where the feedback variable is the voltage across the parallel resonant capacitor. **(b)** The case where the feedback variable is the current through the series resonant inductor.

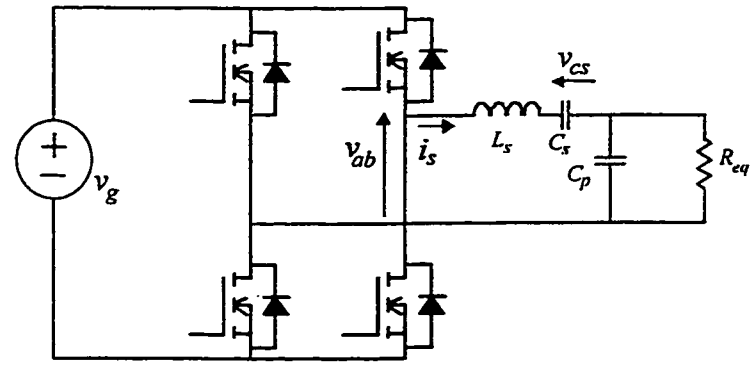
In the case where the feedback variable is the current through the resonant inductor a stable limit cycle exists and ZVS is achieved as long as the control angle is $90° < \gamma < 180°$ as is concluded from Fig. 2.7 (b). However, if the voltage across the parallel capacitor is used as the feedback variable, the range of the control angle γ that results in ZVS will depend on the quality factor Q_p. This can be concluded by comparing (2.7 and (2.8). Therefore, the current through the resonant inductor should be selected as the feedback variable.

2.2.2.3 *Voltage Fed Series-Parallel Resonant Converter*

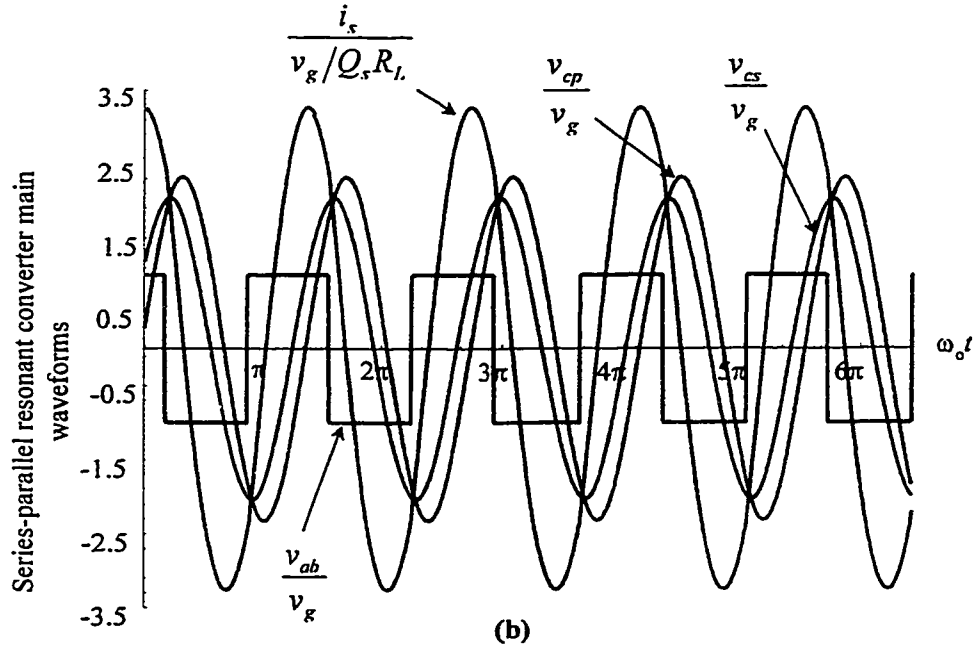
A series-parallel resonant converter combines the features of both series and parallel resonant converters. The resonant circuit, in this case, is comprised of a series branch (L_s, C_s) and a parallel resonant capacitor C_p, as shown in Fig. 2.8 (a). For operation with an inductive output filter the ac equivalent circuit is $R_{eq} = \pi^2/8\, R_L$, where R_L represents the actual load resistance.

In order to operate with self-sustained oscillation and to achieve ZVS in a well-defined range of the control angle γ, the two natural feedback variables candidate are the current through the series resonant inductor and the voltage across the series resonant capacitor. In addition, these variables have a predominant fundamental component and they can be easily measured. The transfer functions from the inverter output voltage to the resonant current i_s, and to the parallel resonant capacitor voltage v_{cs} are denoted by $G_{is\ vab}$ and $G_{vcs\ vab}$ respectively and are given by:

$$G_{is\_vab}(s)=\frac{\frac{s}{\omega_o}\frac{1}{Q_s}\left(\frac{s}{\omega_o}\frac{\pi^2}{8Q_s}+1\right)}{\frac{s^3}{\omega^3{}_o}\frac{\pi^2}{8Q_s}+\frac{s^2}{\omega^2{}_o}+\frac{s}{\omega_o}\frac{\pi^2}{4Q_s}+1}\frac{1}{R_L} \tag{2.9}$$



(a)



(b)

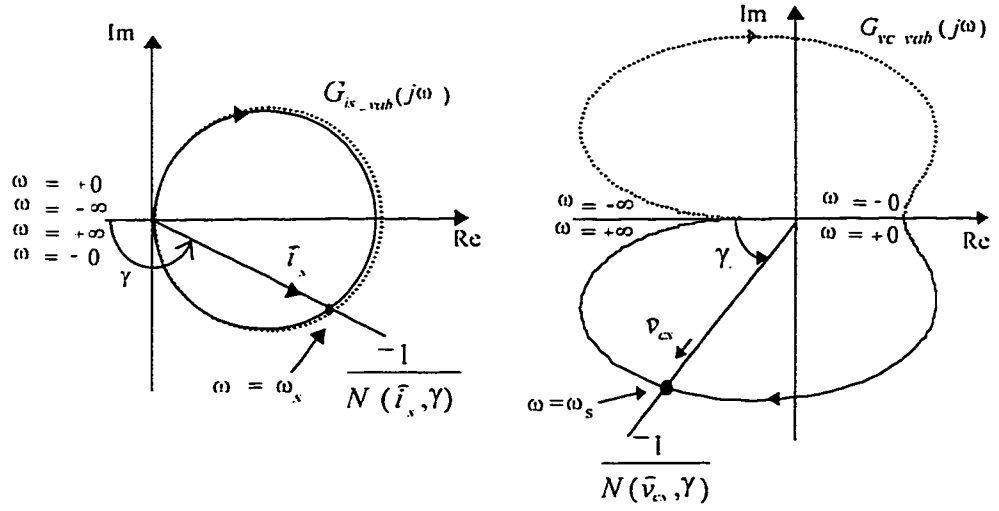
Fig. 2.8 Series-parallel resonant converter.
(a) Power circuit diagram. **(b)** Main waveforms, Q_s=1, ω_s/ω_o=1.41, C_p=C_s.

and

$$G_{vcs\_vab}(s) = \frac{\left(\frac{s}{\omega_o}\frac{\pi^2}{8Q_s}+1\right)}{\frac{s^3}{\omega^3_o}\frac{\pi^2}{8Q_s}+\frac{s^2}{\omega^2_o}+\frac{s}{\omega_o}\frac{\pi^2}{4Q_s}+1} \tag{2.10}$$

where $Q_s = \frac{\omega_o L_s}{R_L}$ and $\omega_o = \frac{1}{\sqrt{L_s C_s}}$.

The frequency response associated which these transfer functions and the negative inverse of the describing function associated with the controller and the inverter are shown in Fig. 2.9.



(a) **(b)**

Fig. 2.9 Determination of self-sustained oscillation in series-parallel resonant converters.

Plot of the sinusoidal transfer functions $G_{is\_vab}(j\omega)$ and $G_{vcs\_vab}(j\omega)$, and the negative inverse describing function of N. (a) The case where the feedback variable is the current the through series resonant inductor. (b) The case where the feedback variable is the voltage across series resonant capacitor.

In the case where the feedback variable is the current through the resonant inductor a stable limit cycle exists if the control angle is $90° < \gamma < 180°$. Furthermore, in this

particular range of the control angle, the current i_s lags the voltage v_{ab}. This provides the necessary condition to achieve commutation under zero voltage. A similar conclusion can be drawn for the case where the voltage across the series resonant capacitor is used as the feedback variable. However, in this case, the control angle must be $0<\gamma<90^{o}$.

2.2.3 Static Characteristics

The input-output characteristics of the converter, as well as, the voltage and current stresses on the components of the converter can be obtained from the static characteristics of the converter. In this section a procedure for the derivation of the static characteristics of resonant converters with the proposed controlled is given. As an example, the relationship between the control angle γ and the peak of the voltages and currents in the resonant converter are derived for a series-parallel resonant converter with inductive output filter, operating in self-sustained oscillation mode, where the feedback variable is the current through the series resonant inductor.

As demonstrated in the previous section, if the self-sustained oscillation exist, its amplitude and frequency must satisfy the following equality:

$$G(j\omega) = -\frac{1}{N(\tilde{i}_s,\gamma)}. \tag{2.11}$$

The equality (2.11) can be represented as two nonlinear equations. One of them is associated with the real part of (2.11) and the other with the imaginary part, that are:

$$[1-\alpha^2]\frac{\pi\omega_n L_s \tilde{i}_s}{V_g} = -4\left[-\frac{\alpha^2\pi^2}{Q_s 8}\cos(\gamma)+\alpha\sin(\gamma)\right] \tag{2.12}$$

$$[2-\alpha^2]\frac{\pi\omega_n L_s \tilde{i}_s}{V_g} = -\frac{32Q_s}{\pi^2}\left[\cos(\gamma)+\frac{\alpha\pi^2}{Q_s 8}\sin(\gamma)\right] \tag{2.13}$$

where $\alpha = \omega_s / \omega_o$. $\omega_o = 1/\sqrt{L_s C_s}$. The simultaneous solution of the nonlinear algebraic equations (2.12) and (2.13) results in possible operating points of the converter. This solution can be expressed in terms of the current through the resonant inductor and the switching frequency ratio α as a function of the control angle γ for different values of quality factor (Q_s) as shown in Fig. 2.10 and Fig. 2.11. It is worth noting that the above equation also has a solution which corresponds to operation below the resonance frequency. Therefore, when searching for the solution, the following constraint on the normalized frequency must be considered. which is $\alpha > 1$.

From the static characteristics shown in Fig. 2.10 and Fig. 2.11 the voltage gain of the converter can be obtained. The voltage gain of the converter will be expressed in terms of the voltage conversion ratio that is defined as the ratio of the average voltage at the output (v_o) of a full bridge diode rectifier connected across the parallel resonant capacitor and the dc input voltage (v_g). After some manipulation it is found that the voltage conversion ratio is given by:

$$M = \frac{v_o}{v_g} = \frac{\pi}{4} \frac{\omega_o L_s \tilde{i}_s}{v_g Q_s} \frac{1}{\sqrt{\left(\frac{\alpha \pi^2}{Q_s 8}\right)^2 + 1}} \quad \text{(V/V)}. \qquad (2.14)$$

The voltage conversion ratio for various normalized load parameters is shown in Fig. 2.12.

On the other hand, the inverter input current can be expressed in terms of its average value over one switching interval, that is:

$$\tilde{i}_d = \frac{1}{T_s} \int_0^{T_s} i_d \, dt = \frac{1}{T_s} \int_0^{T_s} i_s sign(v_{ab}) \, dt = \frac{1}{T_s} \int_0^{T_s} i_s sign(-i_s (t - \frac{\gamma}{\omega_s})) \, dt . \qquad (2.15)$$

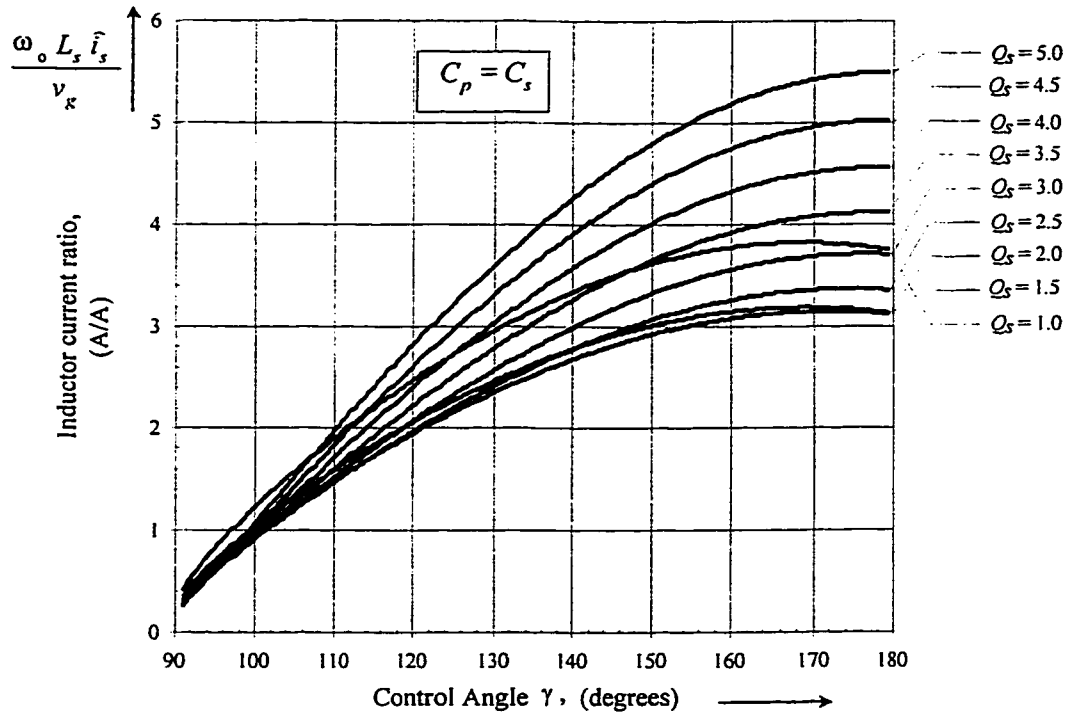


Fig. 2.10 Series resonant inductor current ratio as a function of the control angle.

Peak value of the fundamental component of the current through the series resonant inductor current as a function of the control angle for various values Q_s. Voltage fed series-parallel resonant converter.

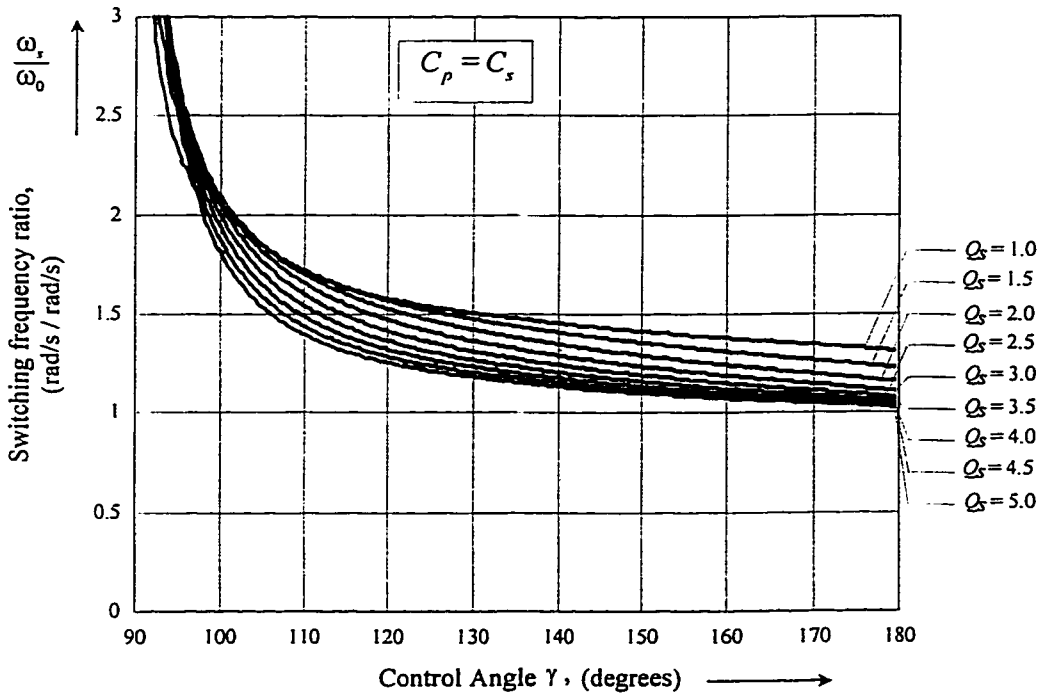


Fig. 2.11 Switching frequency ratio (α) as a function of the control angle (γ) for different values of Q_s.

Voltage fed series-parallel resonant converter with $C_p = C_s$.

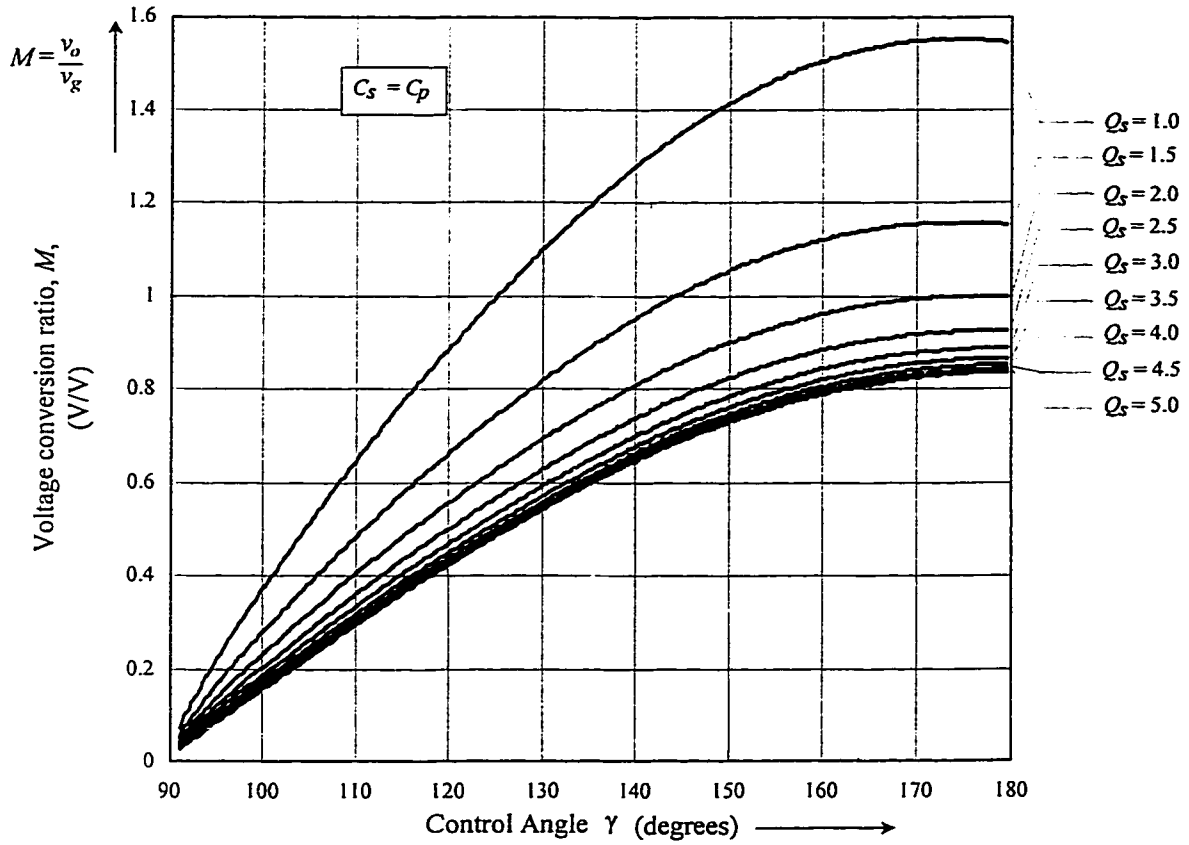


Fig. 2.12 Voltage conversion ratio as a function of the control angle.
Voltage fed series-parallel resonant converter with $C_p = C_s$.

Taking into account the fact that the inductor current can be well represented by its first harmonic component, the equation (2.15) can be expressed as

$$\bar{i}_d = -\frac{2}{\pi}\hat{i}_s \cos(\gamma) \quad \text{(A)}. \tag{2.16}$$

From the equations and curves given in this section, it now is possible to select the resonant circuit parameters to satisfy the needs of a given application. Since the selection of the resonant circuit is not unique, the following section will deal with the

impact of this selection on the stresses of the various components of the resonant converter.

2.2.4 Design Considerations

The input voltage and power are usually well defined quantities for a given application. It can therefore be concluded from (2.16) that by operating with the control angle γ close to 180^{o}, results in smaller current through the resonant inductor. Therefore, the resonant circuit parameters should be selected in such a way that at the minimum input voltage and maximum load the γ approaches 180^{o}.

On the other hand, from Fig. 2.12, it is possible to see that the voltage conversion ratio increases by increasing the control angle γ and by decreasing the quality factor, Q_s. This brings the possibility to minimize the stresses in the resonant circuit by the proper selection of Q_s when there is a transformer where the turns ratio can be adequately selected to meet the load voltage requirement. In order to guide the selection of the resonant circuit parameters, the product of volt-amps associated with the resonant inductor as well as the voltage across the series resonant capacitor, at full load and $\gamma = 180^{o}$, are shown in Fig. 2.13. It is therefore concluded from Fig. 2.13, that in order to operate with small stresses in the resonant circuit the quality factor Q_s should be $1 < Q_s < 3$.

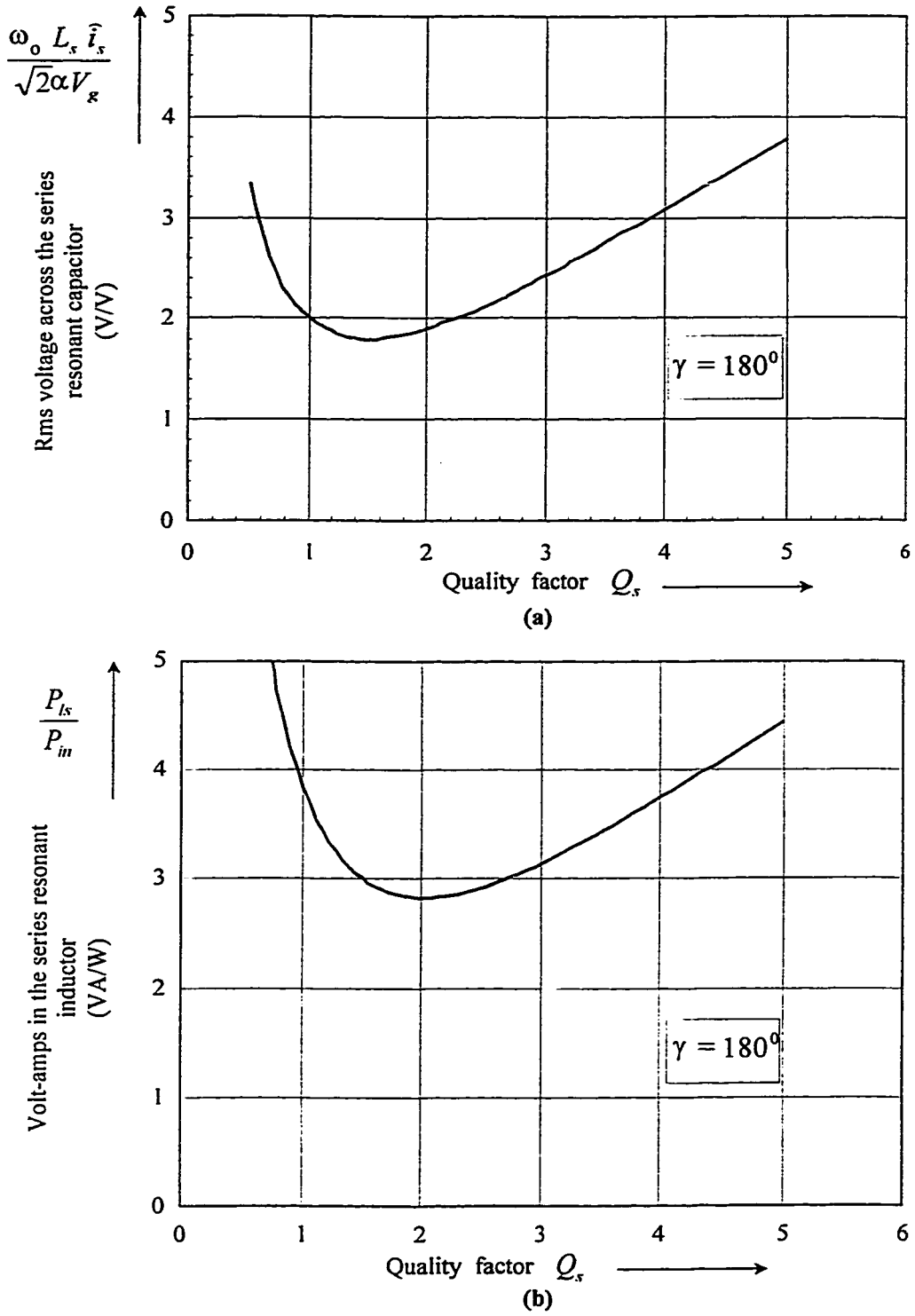


Fig. 2.13 Stresses in a series-parallel resonant converter.

(a) Ratio between the voltage across the series resonant capacitor and the input voltage as function of Q_s. (b) Ratio between the product volt-amps associated with the resonant inductor and the input power as a function Q_s. C_s=C_p.

2.2.5 Comparison between the Proposed Method and the Conventional Frequency Control

In order to clarify the advantages of the proposed controller over the conventional variable frequency control, let us consider a series-parallel resonant circuit in which its parameters such as the series resonant inductor and capacitor values can have any value within the following range

$$0.8L_{sno} < L_s < 1.2L_{sno} \tag{2.17}$$

$$0.8C_{sno} < C_s < 1.2C_{sno} \tag{2.18}$$

where L_{sno} and C_{sno} are their nominal values of L_s and C_s respectively and the parallel resonant capacitor is considered to be equal to the series resonant capacitor. In order to carry out the comparison, the nominal quality factor is selected to be equal to 2.45. Table 2.1 through 2.3 show how the quality factor, natural frequency, and resonant frequency would be if the resonant circuit parameters are in the range specified above.

TABLE 2.1 QUALITY FACTOR, Q_s

L_s/L_{sno} C_s/C_{sno}	0.8	0.9	1.0	1.1	1.2
0.8	2.45	2.31	2.19	2.09	**2.00**
0.9	2.60	2.45	2.32	2.22	2.12
1.0	2.74	2.58	2.45	2.34	2.24
1.1	2.87	2.71	2.57	2.45	2.35
1.2	**3.00**	2.83	2.68	2.56	2.45

TABLE 2.2 RATIO BETWEEN THE NATURAL FREQUENCY AND THE NOMINAL NATURAL FREQUENCY

L_s/L_{sno} C_s/C_{sno}	0.8	0.9	1.0	1.1	1.2
0.8	**1.25**	1.18	1.12	1.07	1.02
0.9	1.18	1.11	1.05	1.00	0.96
1.0	1.12	1.05	1.00	0.95	0.91
1.1	1.07	1.00	0.95	0.91	0.87
1.2	1.02	0.96	0.91	0.87	**0.83**

TABLE 2.3 RATIO BETWEEN THE RESONANT FREQUENCY AND THE NOMINAL NATURAL FREQUENCY

L_s/L_{sno} C_s/C_{sno}	0.8	0.9	1.0	1.1	1.2
0.8	**1.41**	1.34	1.28	1.24	1.20
0.9	1.31	1.25	1.20	1.15	1.11
1.0	1.23	1.17	1.12	1.08	1.05
1.1	1.16	1.11	1.06	1.02	0.99
1.2	1.11	1.05	1.01	0.97	**0.94**

TABLE 2.4 CONTROL ANGLE AT THE RESONANT FREQUENCY

L_s/L_{sno} C_s/C_{sno}	0.8	0.9	1.0	1.1	1.2
0.8	177.2	176.9	176.5	176.2	**175.9**
0.9	177.6	177.2	176.9	176.6	176.3
1.0	177.9	177.5	177.2	176.9	176.6
1.1	178.1	177.8	177.5	177.2	177.0
1.2	**178.3**	178.0	177.7	177.5	177.2

* The extreme values are printed in boldface.

In order to ensure the operation above the resonant frequency in all operating conditions, with conventional variable frequency control method, the frequency should be limited to a value higher than 1.41 ω_o, as indicated in Table 2.3. Similarly, with the proposed method, the operation above the resonant frequency is ensured, if the control angle γ is smaller than 175.9°, as shown Table 2.3. In order to understand the impact of the limits imposed on the switching frequency, in the case of the conventional variable frequency control method, and on the control angle γ, Fig. 2.14 shows the maximum voltage conversion ratio for different values of the resonant circuit parameters. It is clear, from Fig. 2.14, that with the proposed controller, a much higher output voltage can be achieved. The minimum voltage conversion ratio with the proposed controller is 4.7% lower than the nominal voltage conversion ratio. However, with the conventional variable frequency control, the minimum voltage conversion ratio would be 62.5% lower than the nominal voltage conversion ratio, which is unacceptable.

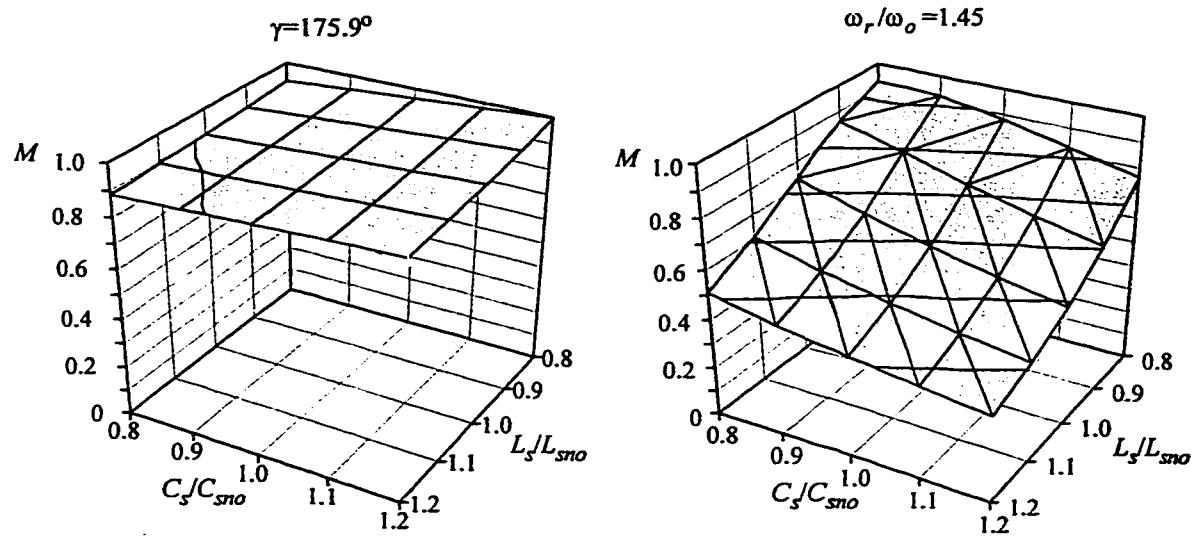


Fig. 2.14 Maximum voltage conversion ratio *M*, which ensures operation above the resonant frequency, as a function of the series resonant inductor and capacitor.
(a) Proposed controller. **(b)** Conventional variable frequency control.

2.2.6 Implementation of the Proposed Controller

The implementation of the control scheme described in the previous sections requires a control signal, here named v_{ca}, proportional to the phase angle γ. This section proposes the use of a constant amplitude sawtooth signal synchronized with the feedback variable x to accomplish this task. The block diagram of the circuit suggested for the implementation of the constant amplitude sawtooth generator and its main waveforms are shown in Fig. 2.15. The comparison the sawtooth s_t with the control voltage v_{ca} results in the pulses p_1 and p_2. These pulses are used to set and reset a flip-flop whose outputs define the gate signals of the inverter. If the amplitude of the sawtooth is kept constant then the control voltage v_{ca} defines the phase-shift between v_{ab} and x. In order to keep the amplitude of s_t constant against the variations in the switching frequency a loop is used to regulate averaged value of s_t as shown in Fig. 2.15 (a).

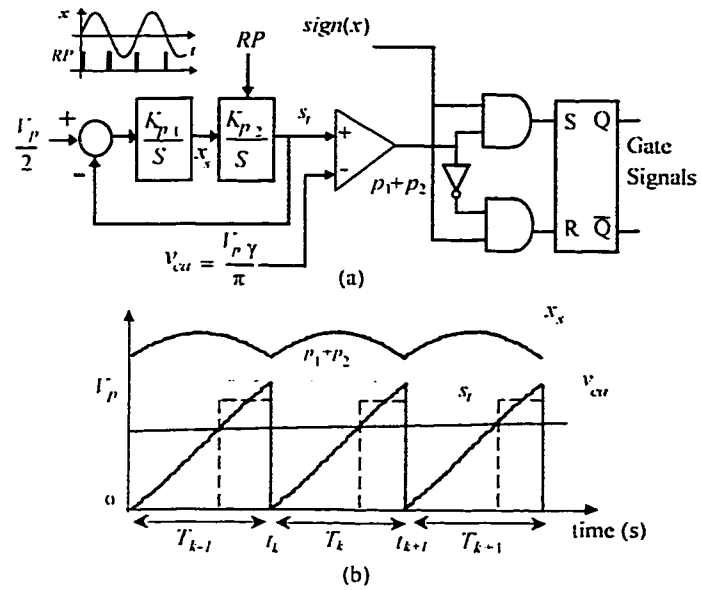


Fig. 2.15 Constant amplitude sawtooth generator.
(a) Block diagram interpretation. (b) Relevant waveforms.

In order to design the constants of the constant amplitude sawtooth generator the equations, which describe its behavior, have to be derived. These equations can be found by solving the differential equation associated with the closed loop of Fig. 2.15. The solution for $t_k < t < t_{k+1}$ with the initial conditions $x_s(t_k) = x_{sk}$ and $s_t(t_k) = 0$ is

$$x_s(t) = C_1 \sin(\omega_{st}(t - t_k)) + C_2 \cos(\omega_{st}(t - t_k)) \tag{2.19}$$

$$s_t(t) = \frac{K_{p2}}{\omega_{st}}\left[C_1(1 - \cos(\omega_{st}(t - t_k))) + C_2 \sin(\omega_{st}(t - t_k))\right] \tag{2.20}$$

where x_s is an internal variable of the sawtooth generator, s_t represents the sawtooth signal. $\omega_{st} = \sqrt{K_{p1} K_{p2}}$, $C_1 = \frac{V_p K_{p1}}{2\,\omega_{st}}$, $C_2 = x_{sk}$, and the voltage V_p represents desired peak value of the sawtooth signal.

In order to design the gains of the sawtooth generator, K_{p1} and K_{p2} , a trade-off between the speed of response, which is required to reject the variations in the switching frequency, and distortion in the sawtooth waveform, must be considered. The equation

(2.20) approaches an ideal sawtooth waveform for decreasing values of ω_{st} as shown in Fig. 2.16. However, by increasing ω_{st} faster transient responses are achieved. In order to understand the impact of ω_{st} in the transient performance of constant amplitude sawtooth generator the discrete equation which relates $x_s(t_k)$ with $x_s(t_{k+1})$ is found by solving (2.19) for $t = t_{k+1}$. The resulting discrete equation is

$$x_s(T_{k+1}) = \cos(\omega_{st} T_k) x_s(T_k) + \frac{V_p K_{p1}}{2\omega_{st}} \sin(\omega_{st} T_k) \tag{2.21}$$

According with (2.21) minimum response time are obtained when $\omega_{st} = \pi/(2T_k)$. In addition, an upper bound value for ω_{st} can be found by restricting the sawtooth signal to have positive slopes. From the steady-state solution of (2.19), it is found that to ensure positive slopes of s_1 the following inequality must be satisfied.

$$\omega_{st} < \frac{\pi}{\max(T_k)} \quad \text{(rad/s)}. \tag{2.22}$$

Appendix I derives an exact model a series-parallel resonant converter with the proposed constant amplitude sawtooth generator. Using this model, it is possible to demonstrate the stability of the system for different values of ω_{st}.

In order to give a physical interpretation for the variable x_s, this variable will be averaged value over one switching interval, and the results is:

$$\bar{x}_s = \frac{V_p}{K_{p2}} \frac{1}{T_k} = \frac{V_p}{K_{p2}\pi} \omega_s \tag{2.23}$$

where the bar symbol over x_s is used to denote averaged value over one switching period. Taking into account that V_p and K_{p2} are constant, it is therefore concluded that the averaged valued of x_s is proportional to the switching frequency.

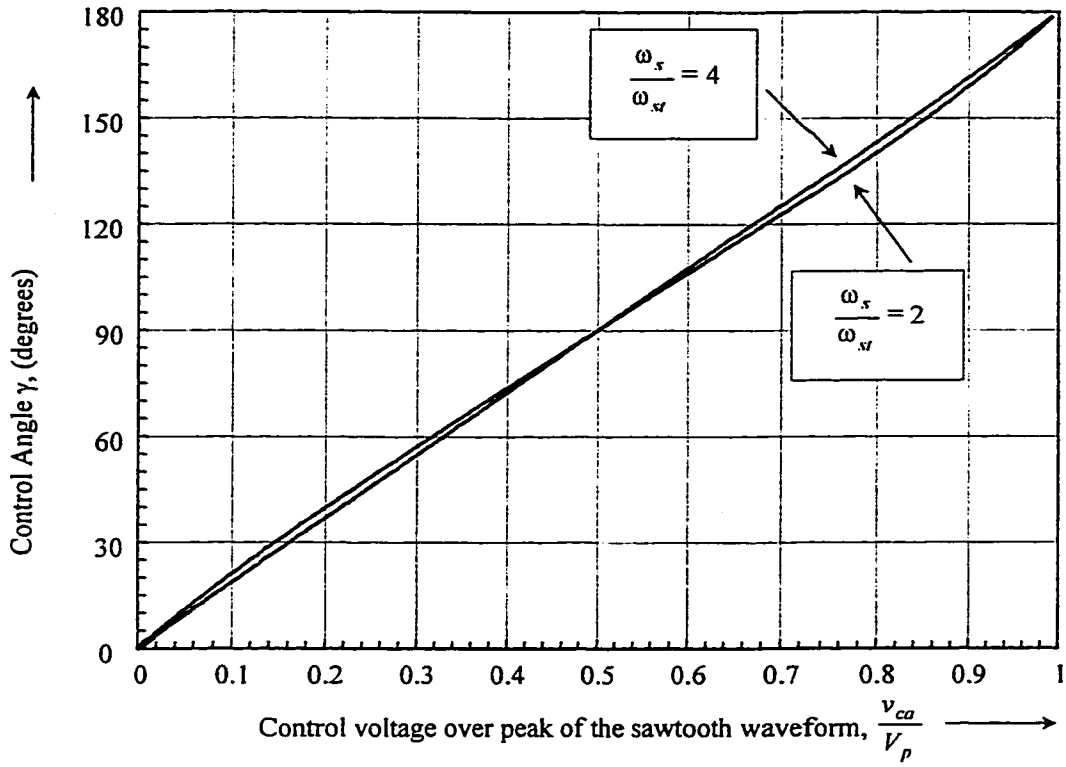


Fig. 2.16 Control angle γ as a function of the control voltage for two values of $\frac{\omega_s}{\omega_{sl}}$.

2.3 DYNAMIC MODELS

In order to design the external controllers that will regulate the output voltage or shape the input current, a dynamic model which describes the behavior of the resonant converter and its input and output filters must be derived. Both digitized models [67,72-74] and continuous models [75,76] of resonant converters have been reported in literature. Digitized models lead to accurate results at the price of requiring the explicit solution of the equations that govern the behavior of the converter in each operating mode. Continuous dynamic models, on the other hand, based on first harmonic approximation do not require the explicit solution of the equations that govern the converter in each operating mode. Continuous models are preferred to digitized ones, when the first harmonic approximation results in the desired accuracy, and when the

order of the system makes the explicit solution of converter equations complex. In this section, a continuous model, based on describing function method, will be derived as an intermediate step used to obtain a small signal model.

2.3.1 Large Signal Model and Modulation Equation

By applying the Kirchhoff's voltage and current law in the series-parallel resonant converter and considering the operation of the proposed controller, the following nonlinear large signal model can be found:

$$\begin{aligned}
\frac{di_s}{dt} &= -\frac{1}{L_s}v_{cs} - \frac{1}{L_s}v_{cp} + \frac{1}{L_s}V_g \text{sign}\,(-i_s(t-t_7)) \\
\frac{dv_{cs}}{dt} &= \frac{1}{C}i_s \\
\frac{dv_{cp}}{dt} &= \frac{1}{C}i_s - \frac{1}{C}i_o \text{sign}\,(v_{cp}) \\
\frac{di_o}{dt} &= \frac{1}{L_o}(|v_{cp}| - v_o) \\
\frac{dv_o}{dt} &= \frac{1}{C_o}(-\frac{v_o}{R_L} + i_o) \\
\frac{dx_s}{dt} &= K_{p1}K_{p2}(\frac{V_p}{2K_{p2}} - \int_{t1}^{t} x_s dt)
\end{aligned} \tag{2.24}$$

with the following constraints:

$$\begin{aligned}
v_{ca} &= \int_{t_1}^{t_2-t_1} K_{p2}x_s dt \\
i_s(t_1) &= 0
\end{aligned} \tag{2.25}$$

Taking into account that our goal is to obtain a small signal model which is valid for small perturbations around an operating point where frequency does not change significantly, the sawtooth generator will be represented by an algebraic equation which relates v_{ca} and t_7.

$$t_r = \frac{v_{cn}}{V_p}\frac{2\pi}{\omega_s}, \text{ or } \quad t_r = \frac{\gamma}{\omega_s} \quad . \tag{2.26}$$

The variables of (2.24), which are associated with the resonant circuit, have a dominant first harmonic component. Therefore, assuming that the amplitude of these first harmonics vary slowly in time the resonant circuit can be represented by:

$$\begin{aligned} i_s &= i_{ss}(t)\sin(\psi(t)) + i_{sc}(t)\cos(\psi(t)) \\ v_{cs} &= v_{sc}(t)\cos(\psi(t)) \\ v_{cp} &= v_{ps}(t)\sin(\psi(t)) + v_{pc}(t)\cos(\psi(t)) \end{aligned} \tag{2.27}$$

On the other hand, the variables associated with the input and output filter will be represented by their average value over one switching period. This representation is valid since the input and output filters parameters are designed to attenuate the high frequency components generated by the inverter and diode rectifier. As a result, their waveforms (voltage across the capacitors and current through the inductors) are dominated by their dc component.

By substituting the equation (2.27) and its time derivative into the nonlinear model (2.24) and equating the sine and cosine terms, the modulation equation (2.28) is obtained. The variables in (2.28) describe the dynamic behavior of the envelopes of the sine and cosine associated with the first harmonic components of the resonant circuit variables of (2.24) and the averaged values, over one switching period, of the input and output filters.

$$
\begin{aligned}
\frac{di_{ss}}{dt} &= -\frac{i_{ss}\, i_{sc}}{C_s\, v_{sc}} - \frac{1}{L_s}\left[r_s\, i_{ss} + v_{ps} + \frac{4}{\pi}\bar{v}_{cin}\,(\, i_{ss}\cos(\gamma) + i_{sc}\sin(\gamma)\,)\frac{1}{\sqrt{i_{ss}^{\,2} + i_{sc}^{\,2}}}\right] \\
\frac{di_{sc}}{dt} &= \frac{i_{ss}\, i_{ss}}{C_s\, v_{sc}} - \frac{1}{L_s}\left[r_s\, i_{sc} + v_{sc} + v_{pc} + \frac{4}{\pi}\bar{v}_{cin}(-i_{ss}\sin(\gamma) + i_{sc}\cos(\gamma)\,)\frac{1}{\sqrt{i_{ss}^{\,2} + i_{sc}^{\,2}}}\right] \\
\frac{dv_{sc}}{dt} &= \frac{i_{sc}}{C_s} \\
\frac{dv_{ps}}{dt} &= -\frac{i_{ss}\, v_{pc}}{C_s v_{sc}} + \frac{1}{C_p}\left[i_{ss} - \frac{4}{\pi}\bar{i}_o \frac{v_{ps}}{\sqrt{v_{ps}^2 + v_{pc}^2}}\right] \\
\frac{dv_{pc}}{dt} &= \frac{i_{ss}\, v_{ps}}{C_s\, v_{sc}} + \frac{1}{C_p}\left[i_{sc} - \frac{4}{\pi}\bar{i}_o \frac{v_{pc}}{\sqrt{v_{ps}^2 + v_{pc}^2}}\right] \\
\frac{d\bar{i}_o}{dt} &= \frac{1}{L_o}\left(\frac{2}{\pi}\sqrt{v_{ps}^2 + v_{pc}^2} - \bar{v}_o\right) \\
\frac{d\bar{v}_o}{dt} &= \frac{1}{C_o}\left(-\frac{\bar{v}_o}{R_L} + \bar{i}_o\right)
\end{aligned}
\tag{2.28}
$$

The nonlinearities sign(.) and abs(.) in (2.24) are evaluated by their describing function, and R_L is the load resistance. Simulation results demonstrated a strong correlation between the solution of (2.24) and the envelopes, which are associated with the solution of (2.28), as illustrated in Fig. 2.17.

It is worth mentioning that the modulation equation (2.28) has an equilibrium point which does satisfy (2.11). This can be demonstrated by expressing the steady state solution of (2.28), which is given by (2.30), in the form of the equations (2.12) and (2.13). As this derivation deals with the steady state solution of a loss-less series-parallel resonant converter with equal series and parallel resonant capacitors, the following equalities are valid:

$$
I_{ss} = \bar{i}_s, \quad V_{sc} = \bar{v}_{cs} = -\frac{I_{ss}}{\omega_s C_s}, \quad r_s = 0, \quad C_p = C_s. \tag{2.29}
$$

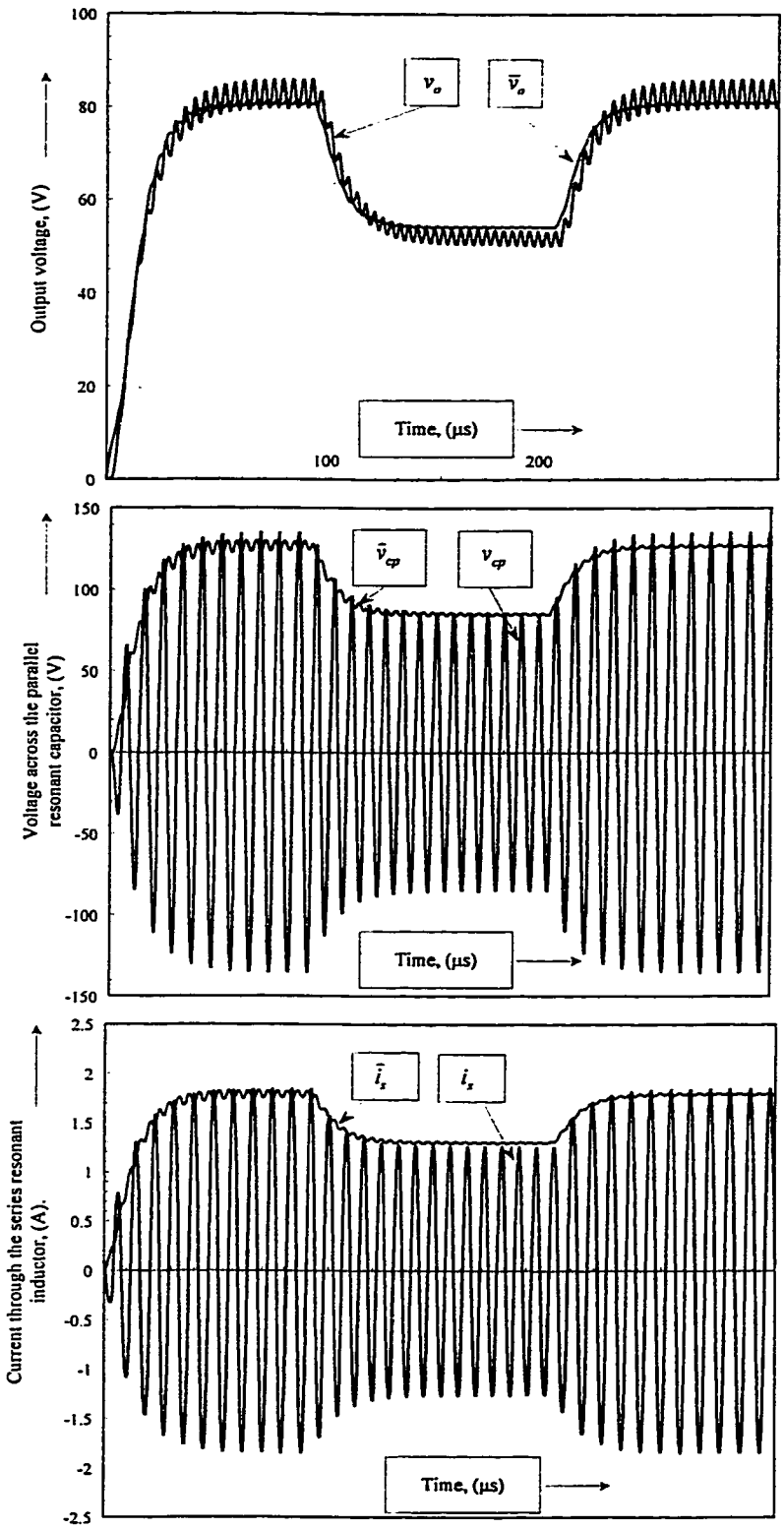


Fig. 2.17 Transient caused by step changes in the control angle.

Numerical solution of (2.24) and (2.28). Control angle step changes between 126° and 162°. L_s=220μH, C_s=C_p=16nF, L_o= 544μH, C_o=19nF, R_L=120Ω, v_g=50V. Horizontal scale: 10μs/div.

$\hat{i}_s = \sqrt{i_{ss}^2 + i_{sc}^2}$ and $\hat{v}_{cp} = \sqrt{v_{ps}^2 + v_{ps}^2}$.

The equation (2.28) can be used to derive small signal models that includes the dynamics of resonant circuit as well as the dynamics of the input and output filters. The next section addresses this issue.

2.3.2 Small Signal Model

To obtain a linear model from the modulation equation (2.28) the operating point of the converter must be found. For example, for a given control angle γ, input voltage, load, and a set of power circuit parameters, the values of i_{ss}, i_{sc}, v_{sc}, v_{ps}, v_{pc} at a equilibrium operating point can be found by setting to zero the left side of (2.28) and solve it for the unknown quantities. In order to simplify the search and avoid solutions that correspond to undesired equilibrium points, the following procedure is recommended. The first step is to find the operating frequency using the curves of Fig. 2.11, and then to compute the variables of the modulation equation using the following equations:

$$V_{ps} = -\frac{4}{\pi} V_g \cos(\gamma), \quad V_{pc} = -\omega_s C_p R_L \frac{\pi^2}{8} V_{ps},$$

$$I_{ss} = -C_p \omega_s V_{pc} + 8 V_{ps} / R_L \pi^2 \quad , \text{ and} \tag{2.30}$$

$$V_{sc} = -V_{pc} + \frac{4}{\pi} V_g \sin(\gamma) - \omega_s L_s I_{ss}$$

where the variables at the operating point are denoted by capital letters, and $\omega_s = \frac{d\psi(t)}{dt}$.

2.4 EXPERIMENTAL RESULTS

The feasibility of the proposed control scheme has been verified on an 1kW series-parallel resonant dc-dc converter operating from a 250V dc source, and producing

an isolated 100V dc output voltage. The output stage of the implemented dc-dc converter consists of a diode rectifier followed by a second order filter (L_o, C_o) with inductive input characteristics. The main parameters of the implementation are presented in Table 2.5. The values of L_s, C_s and turns ratio of the isolation transformer n_1:n_2 where obtained using Fig. 2.12 and Fig. 2.11.

TABLE 2.5 CIRCUIT IMPLEMENTATION MAIN PARAMENTERS

L_{in}	C_{in}	L_s	C_s	C_p	n_1:n_2	L_o	C_o
120μH	10.8mF	208μH	15.8nF	15.8nF	2.29	100μH	10μF

The ideal waveforms of the proposed controller are shown in Fig. 2.18. The pulses, p_1 and p_2, are generated from the comparison of the constant amplitude sawtooth signal with the control voltage v_{ca}. These pulses feed a set-reset flip-flop whose output are the signals that define the conduction states of the inverters transistors. By changing the amplitude of the control voltage, the phase angle between the feedback variable x, that in this case is the current through the resonant inductor, and the voltage across the inverter output terminal v_{ab} can be adjusted to meet the load or input current requirements.

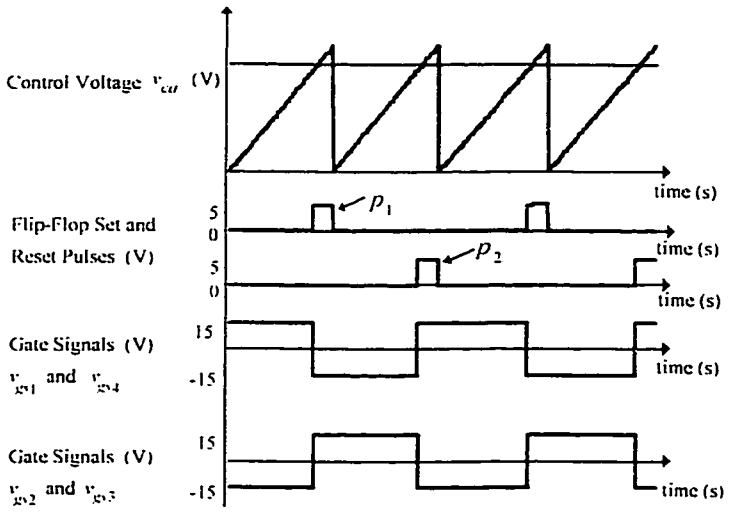


Fig. 2.18 Ideal waveforms of the proposed controller.

Fig. 2.19 shows the experimental waveforms of the proposed controller. From Fig. 2.19 (a) and (b) it is demonstrated that the amplitude of the sawtooth signal, s_r, signal remains constant at different switching frequencies. By comparing Fig. 2.18 and Fig. 2.19 it is found that the experimental waveforms have a delay between p_1 and v_{g1}. This delay results from a dead-time, which has been introduced to alow the proper reset of the snubber capacitors.

To validate the analysis carried out in the previous sections, a comparison among the describing function method, the modulation equation, large signal model, and experimental results were carried out and the results are summarized in Table 2.6.

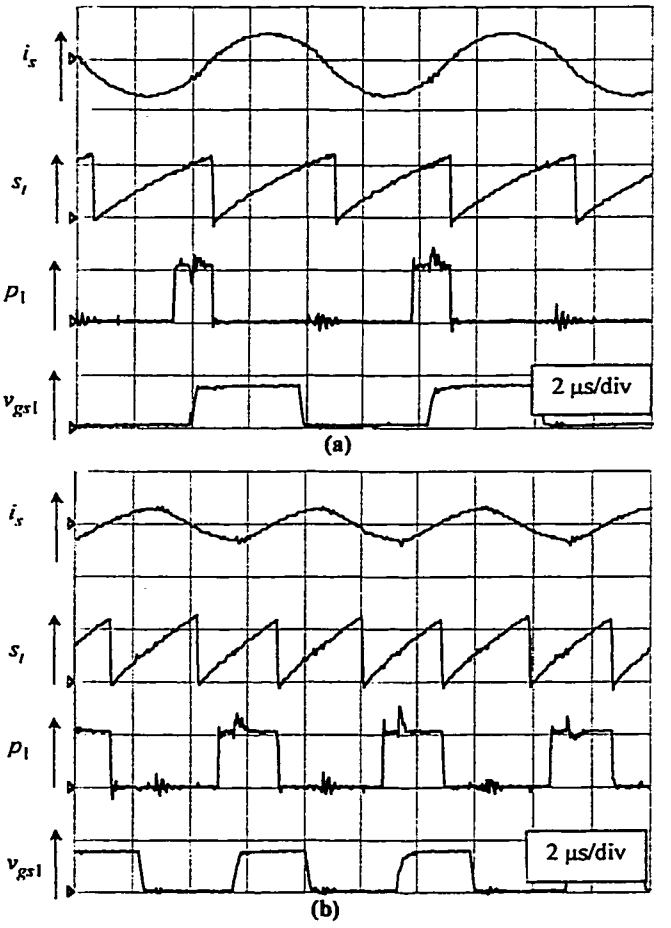


Fig. 2.19 Proposed controller experimental waveforms.
(a) Switching frequency 119 kHz, **(b)** Switching frequency 172 kHz.
ω_{st}=118080. Vertical Scales: v_{gs1}: 20 V/div., p_1 and *st*: 5V/div ; i_s:1A/div. Horizontal scale 2µs/div.

TABLE 2.6 COMPARISON OF ANALYTICAL, SIMULATED, AND EXPERIMANTAL RESULTS.

	Q_s=1.5													
	γ=100°				γ=135°				γ=170°			
	M1	*M2*	*M3*	*M4*	*M1*	*M2*	*M3*	*M4*	*M1*	*M2*	*M3*	*M4*
$\alpha = \frac{\omega_s}{\omega_o}$	2.06	2.06	2.04	1.98	1.44	1.44	1.43	1.41	1.27	1.27	1.28	1.24
$\bar{i}_s \frac{Q_s R_L}{v_g}$	1.04	1.04	1.03	1.05	1.63	2.63	2.60	2.67	3.18	3.18	3.23	3.20
$M = \frac{v_o}{v_g}$	0.28	0.28	0.26	0.27	0.89	0.89	0.84	0.87	1.15	1.15	1.17	1.13
$\bar{i}_d \frac{Q_s R_L}{v_g}$	0.11	0.11	0.10	0.12	1.19	1.19	1.15	1.21	2.00	2.00	2.09	2.01

M1 -Describing function method.
M2- Modulation equation equilibrium point.
M3- Simulation including the SOC (the control voltage v_{ca} obtained from (2.26) and the constants of the SOC $\omega_{st}= \omega_o/2$).
M4- Experimental results (L_s=208μH, C_s=15.8 nF, C_p=15.8 nF, v_g=150 V).

Table 2.6 confirms that the results of the describing function method, *M1*, and the modulation equation, *M2*, are identical. This is because both methods are based on the first harmonic component of the resonant circuit variables. The values obtained by simulation (*M3*) are in good agreement with the ones obtained analytically by means of the methods based on the first harmonic component (*M1*,*M2*). This is because for Q_s=1.5 the converter operates with continuous capacitor voltage mode (Appendix 1) where the waveforms of the resonant circuit have a predominant first harmonic component. The experimental results follow the same trend as the simulated and analytical results, where the differences are attributed to the losses associated with the power circuit, which have not been taken into account by the analytical methods.

2.4.1 Illustration of Zero Voltage Switching

In order to illustrate the operation with zero voltage switching, the voltage across the leg A of the inverter and the gate-source voltage of the bottom switches at different operating conditions are shown in Fig. 2.20 to Fig. 2.23. It is possible to see that when the gate-source voltage becomes high, the drain-source voltage is already at zero indicating that zero voltage switching takes place. It is worth mentioning that the control angle γ has to be kept close to 90° in order to satisfy the power balance between the input and output in both no-load operation and short-circuit operation, since in these conditions power is not sent to the load. On the other hand, the control angle γ has to be moved toward 180° as the load increases as shown in Fig. 2.21 and Fig. 2.22.

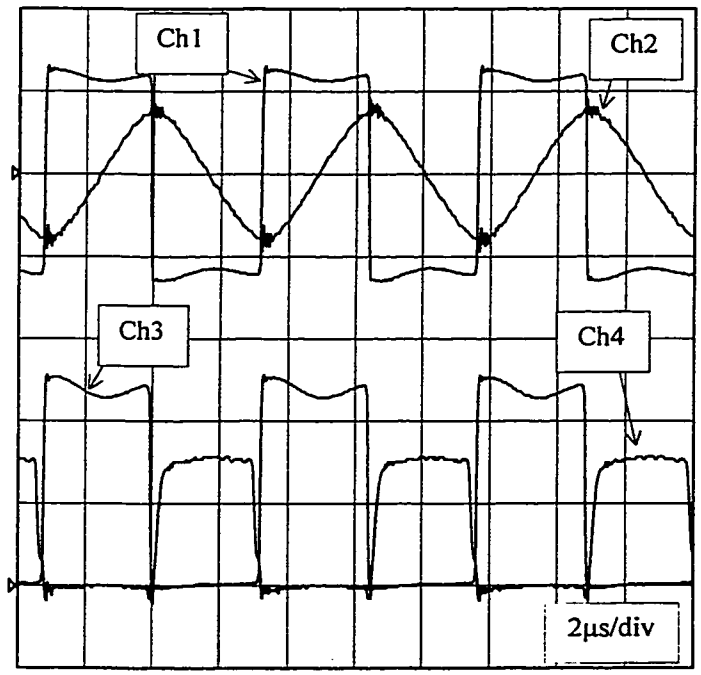


Fig. 2.20 Experimental results. Series-parallel resonant converter in self-sustained oscillation during no load operation.

Ch1: voltage v_{ab}, 200V/div ;**Ch2:** current i_s, 5A/div, **Ch3**:drain-source voltage v_{ao}, 100V/div; **Ch4:** Gate-source voltage v_{gs2},10 V/div. Horizontal scales: 2µs/div. v_g=240V, i_o=.01A, v_o=100V.

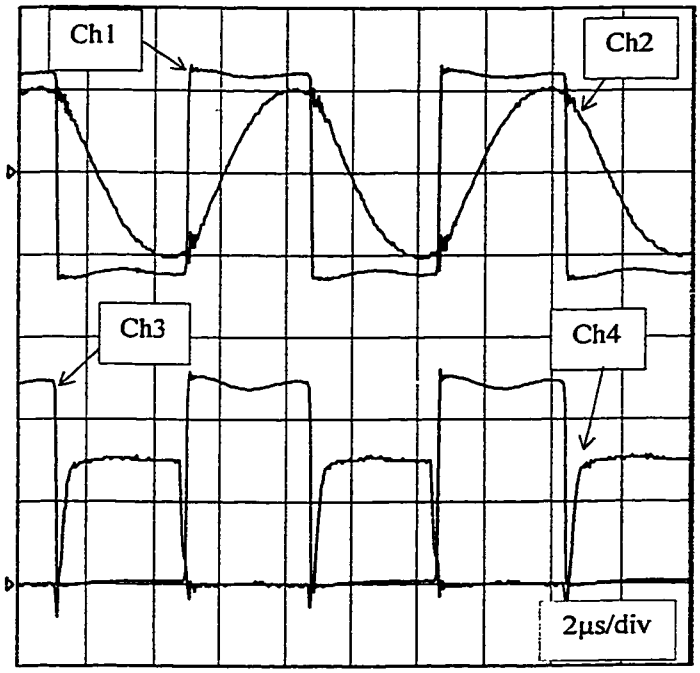


Fig. 2.21 Experimental results. Series-parallel resonant converter in self-sustained oscillation at half of full load operation.

Ch1: voltage v_{ab}, 200V/div ;**Ch2**: current i_s, 5A/div, **Ch3**:drain-source voltage v_{ao}, 100V/div; **Ch4**: Gate-source voltage v_{gs2}, 10 V/div. Horizontal scales: 2μs/div. v_g=240V, i_o=5A, v_o=100V.

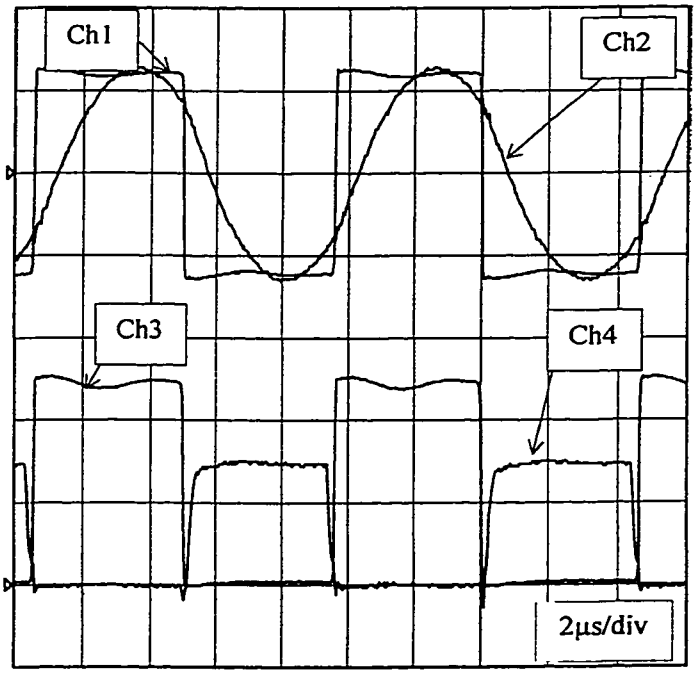


Fig. 2.22 Experimental results. Series-parallel resonant converter in self-sustained oscillation at full load operation.

Ch1: voltage v_{ab}, 200V/div ;**Ch2**: current i_s, 5A/div, **Ch3**:drain-source voltage v_{ao}, 100V/div; **Ch4**: Gate-source voltage v_{gs2}, 10 V/div. Horizontal scales: 2μs/div. v_g=240V, i_o=9.5A, v_o=100V.

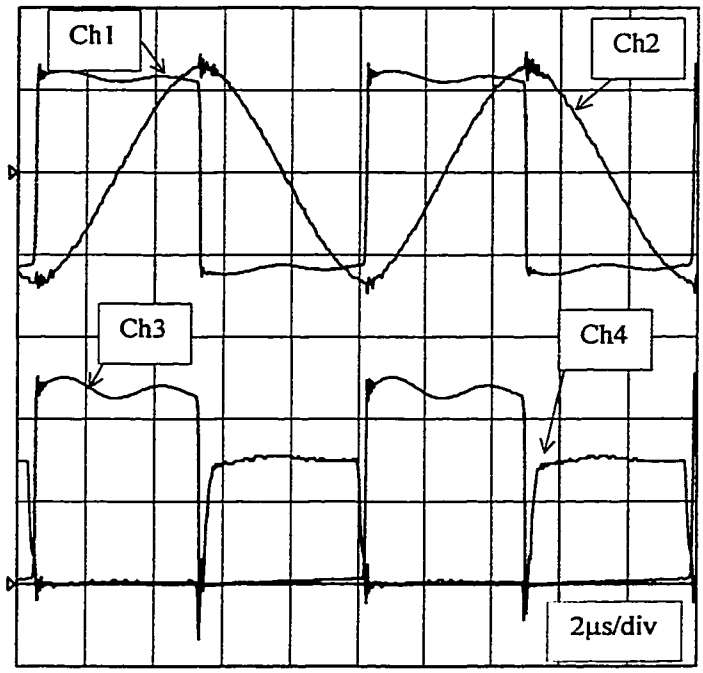


Fig. 2.23 Experimental results. Series-parallel resonant converter in self-sustained oscillation during short-circuit operation.

Ch1: voltage v_{ab}, 200V/div; **Ch2**: current i_S 5A/div, **Ch3**: Drain-source voltage v_{ao}, 100V/div; **Ch4**: Gate-source voltage v_{gs2} : 10 V/div. Horizontal scales: 2µs/div. v_g=240V, i_o=14A, v_o= 0.

2.4.2 Transient Performance

In this section, experimental and analytical results are compared aiming to validate the dynamic models developed in Section 2.3.

Fig. 2.24 and Fig. 2.25 show the transient response due to step changes in the control variable. First, Fig. 2.24 shows the output voltage, the first harmonic component of the current i_s and its amplitude obtained from the numerical solution of the modulation equation (2.28). Then, Fig. 2.25 shows the results obtained from the experimental setup in similar operating conditions. The relationship between γ and v_{ca} can be derived from (2.26), that is, $\gamma = 2\pi v_{ca}/V_p$ (rad). Through the comparison of these figures, it is concluded that there is a good correlation between the transient response from the modulation equation and the experimental results.

2.4.3 Frequency Response

A small signal model was obtained by linearization of (2.28) around an operating point. The frequency response obtained with this small signal model is plotted in Fig. 2.26. In this figure, the frequency response obtained with the experimental setup is also shown. For the experimental results two values of the constant ω_s/ω_{sl} were considered, that are (1.5 and 3.75). In spite of the change in the ratio between ω_s and ω_{sl} greater two, the frequency response is not significantly affected. Furthermore, a good agreement between the experimental and analytical results is observed for frequencies smaller than half of the switching frequency.

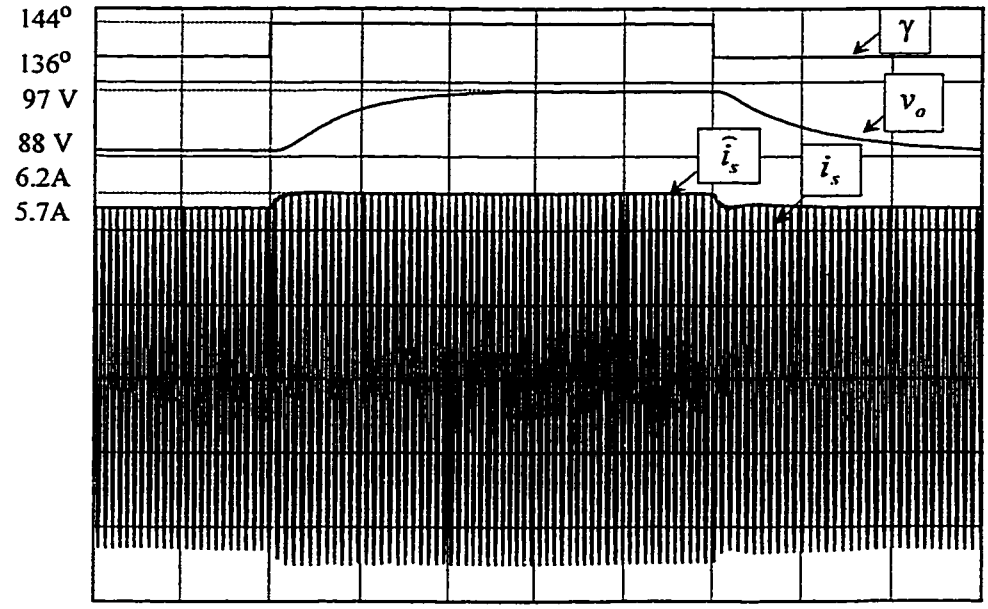


Fig. 2.24 Simulation results from the modulation equation. Transient response due to a step change in the control angle γ.

Current i_s: 2.5A/div ; Output voltage v_o: 10V/div ; Control Angle γ : 18 degrees/div. Horizontal scale:100μs/div.

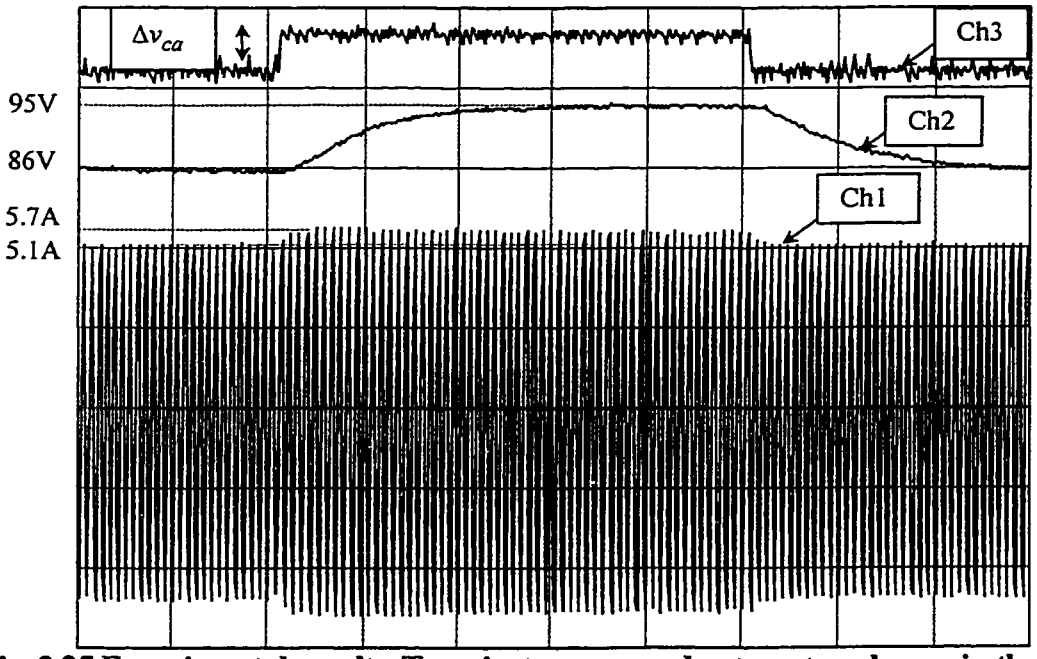


Fig. 2.25 Experimental results. Transient response due to a step change in the control voltage v_{ca}.

Ch1: current i_s: 2.5A/div ; **Ch2:** output voltage v_o: 10V/div ; **Ch3:** Control voltage v_{ca}: 0.22 V/div. Horizontal scale: 100μs/div. ω_{st}=118080. V_p = 2.7 V. Δv_{ca}=0.1V.

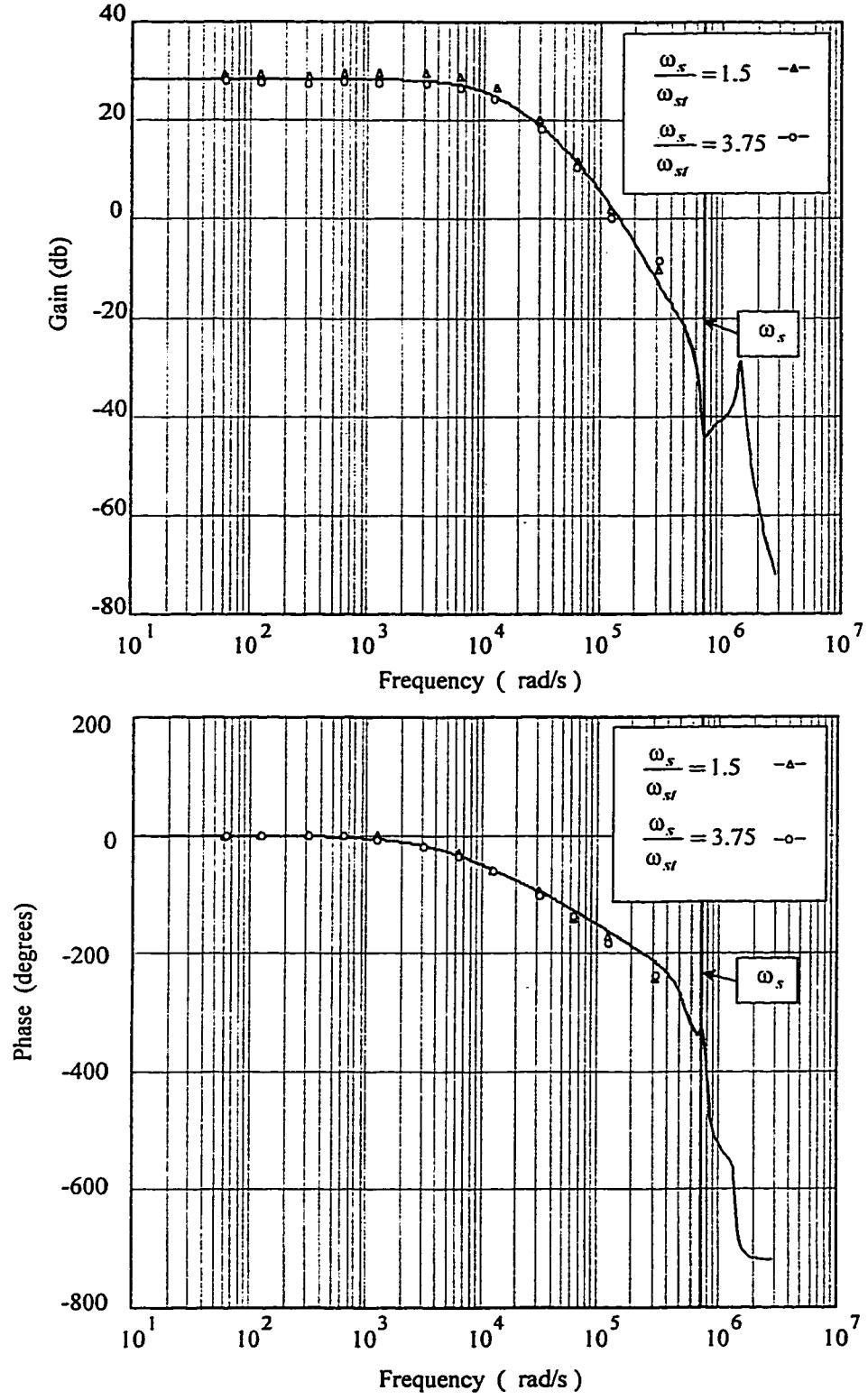


Fig. 2.26 Frequency response from the control angle γ to the output voltage v_o.
Solid line represents the small signal model. Marked points represent experimental measurements for two values of the constant ω_{sf}. v_g= 284 V; v_o= 100V; i_o=8.5A; Switching frequency f_s=112 kHz.

2.5 DISCUSSION AND CONCLUSIONS

A new control technique suitable for resonant converters has been presented in this chapter. It has been demonstrated that with the proposed controller, with a negligible derating, the converter does operate above the resonant frequency, ensuring in this way, the condition to operate with zero voltage switching, for a wide variation in the resonant circuit parameters. The static characteristics of a series-parallel resonant converter in the self-sustained oscillation mode have been derived and they can be used in the design of the power circuit components. A dynamic equation, which describes the behavior of the converter, has been derived. Experimental results confirm the operation with ZVS at different operating conditions, and validated the analysis carried-out.

CHAPTER 3: HIGH POWER FACTOR AC-DC RESONANT CONVERTERS

3.1 INTRODUCTION

In order to restrict the voltage distortion of the ac mains, standards such as IEC1000-3-2 impose limits for the harmonic currents drawn by the equipment connected to it [3,4]. Consequently, power factor correction has become a mandatory feature in such equipment. The single-phase resonant based UPS topology proposed in Chapter 1 operates either from the battery or from the incoming ac mains. Therefore, when operating from the ac mains the input harmonic current requirements must be satisfied. The operation of the line side converter (LSC) of the proposed UPS topology is similar to the operation of a resonant ac-dc converter. Therefore this chapter is dedicated to the analysis and improvement of resonant ac-dc converters.

When single-phase converters are operated with unity input power factor, they draw a sinusoidal current in phase with the input ac voltage. As a result, the converter becomes heavily and lightly loaded near the peak and zero of the ac input voltage waveform. It has been demonstrated that parallel and series-parallel resonant converters have the required characteristics needed to provide operation with both high input power factor and constant output voltage [58-60,77-79]. This is due to the fact that these converters have high voltage gain under light load and a lower gain at full load. The converter voltage gain also depends on the ratio between the switching and the resonant frequencies. It was demonstrated [58-60], that it is possible to make the converter operate

with unity input power factor by adjusting the switching frequency along the input line cycle. In addition, when operating above the resonant frequency these converters provide operation with zero voltage switching (ZVS), thereby reducing the switching losses. In spite of the presence of these features, the following issues still remain unresolved:

(i) The total harmonic distortion (THD) of the input current is high, typically 30% at full load, when operating without active control. The proper design of the resonant circuit parameters can reduce the total harmonic distortion of the input current, however, it results in the loss of zero voltage switching during full-load operation [77].

(ii) To ensure operation under ZVS, the ratio between the switching and the resonant frequencies must be kept high, typically greater than 1.2 at full load and minimum input voltage. This increases the circulating current and the losses in the circuit.

(iii) The range of the frequency variation, from full load to a fraction of full load, is large, which increases the magnetic losses.

(iv) By actively controlling the input current its THD can be reduced significantly [77]. However, the implementation of the input current controller requires a current sensor and a multiplier, which increases the complexity of the circuitry. Furthermore, if the converter has to handle overload and short-circuit conditions an additional current has to be measured either in the resonant circuit or at the output stage.

In order to overcome the above-mentioned disadvantages, this chapter proposes: (i) the application of the control technique developed in Chapter 2 to ac-dc resonant

converters as shown in Fig. 3.1, which will ensure ZVS operation under all operating conditions. (ii) the extension of the control technique proposed in Chapter 2 for operation with phase-shift modulation, which will reduce the stresses in the power circuit components, and (iii) the development of a control technique that allows the operation with high input power factor without the use of active control of the input current, which will simplify the control circuitry, and (iv) a design procedure for the selection of the resonant circuit components as well as the input and output filter components.

This chapter is organized as follows: In Section 3.2, the operation of ac-dc resonant converters with variable frequency plus phase-shift modulation is described and a comparison with the variable frequency control method is presented. Section 3.3 and 3.4 deal with the design of the power circuit components while Section 3.5 presents two methods to achieve high input power factor. Section 3.6 gives experimental results obtained from a prototype to validate the analysis. The main points of this chapter are summarized and conclusions are drawn in Section 3.7.

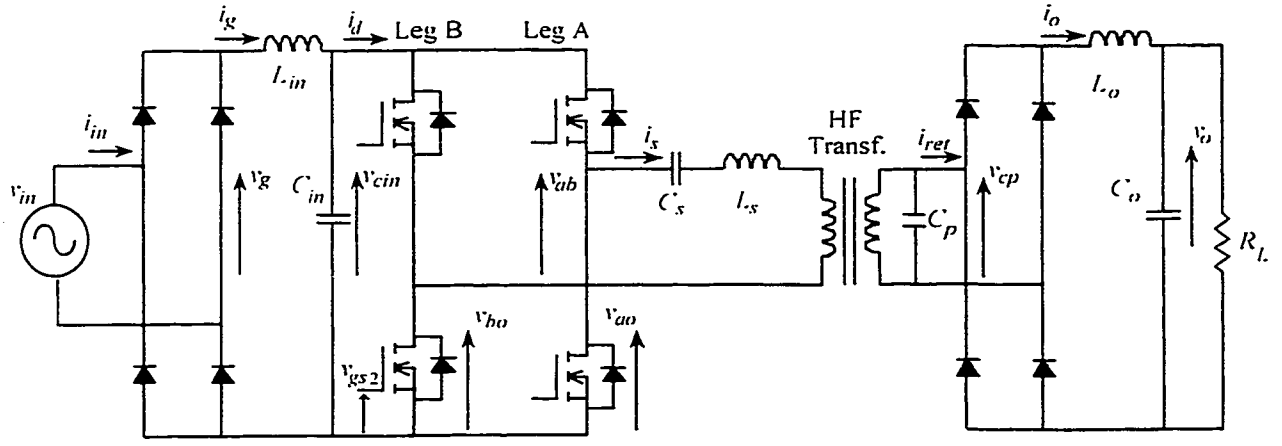


Fig. 3.1 Ac-to-dc series-parallel resonant converter power circuit diagram.

3.2 Generalization of the Self-Sustained Oscillation for Operation with Variable Frequency plus Phase-Shift Modulation

The purpose of this section is to extend the operation of the self-sustained oscillation controller (as described in Chapter 2) for operation with variable frequency plus phase-shift modulation (VFPSM). In addition, the stability of the self-sustained oscillation is examined using the describing function method.

The performance of the converters when operating with variable frequency in self-sustained oscillation mode can be improved by controlling the phase-shift between the legs of the full bridge inverter. In order to achieve zero voltage switching in phase shift modulation, the current must lag the inverter output voltage and must cross zero inside the non zero voltage pulse of v_{ab}. To ensure these conditions, the conduction states of both legs A and B, Fig. 3.1, will be defined from the zero crossing of the current through the resonant circuit. Without loosing generality, it will be assumed that the voltage produced by leg B lags the voltage produced by the leg A in the inverter of Fig. 3.1. In this way, the voltage associated with the leg A, v_{ao}, defines the positive edge of the positive voltage pulse, and the negative edge of the negative voltage pulse. Therefore, the leg A can be used to ensure that current crosses zero inside the inverter output voltage pulse. On the other hand, leg B defines the negative edge of the positive voltage pulse, as well as the positive edge of the negative voltage pulse. Therefore, leg B can be used to define the pulse width of the quasi square waveform at the output of the inverter. In Chapter 2 one control angle, γ, was used to establish a well-defined phase angle between the inverter output voltage and current. As a result, the converter operates in self-

sustained operating mode above the resonant frequency. In this Chapter it is proposed the use of two control angles. The first, γ_{1a}, defines the phase angle between the current i_s and the voltage v_{ao}. The second, γ_{1b}, defines the phase angle between i_s and the voltage v_{bo} as shown in Fig. 3.2.

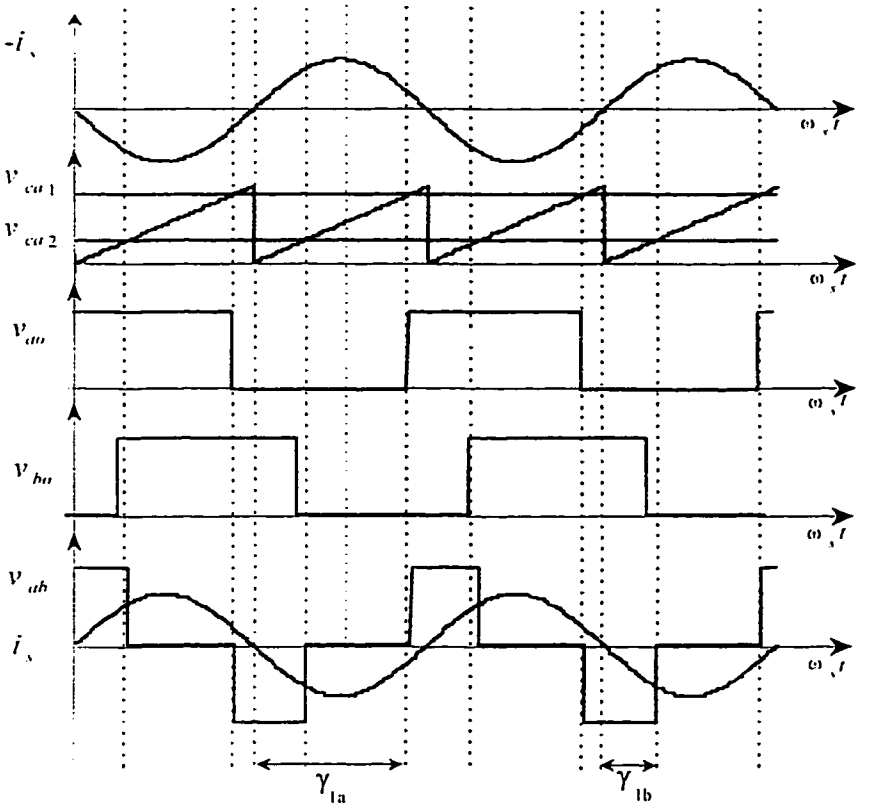


Fig. 3.2 Main waveforms for operation with phase-shift modulation.

In order to simplify the detection of the self-oscillating mode, the following assumption are made:

(i) There is an ideal voltage source at the input of the inverter.

(ii) The current through the resonant inductor has a predominant first harmonic component.

(iii) The transformer is ideal with one to one turns ratio and an equivalent resistor is used to represent the output stage.

With these assumptions, the self-sustained oscillation controller, the inverter and the resonant circuit can be represented by the block diagram shown in Fig. 3.3 (a). When the non-linearity, which is associated with the inverter and the self-sustained oscillation controller is replaced by its describing function the block diagram of Fig. 3.3 (a) takes the form shown in Fig. 3.3 (b).

The variables of the loop of Fig. 3.3 (b) V_{ab} and I_s are the complex quantities associated with the first harmonic component of v_{ab} and i_s respectively, and $\hat{i}_s$ is the magnitude of I_s. From of Fig. 3.3 (b) it is found that the following relations must be satisfied:

$$V_{ab} = N(\hat{i}_s, \gamma_{1a}, \gamma_{1b})(-I_s) \tag{3.1}$$

and

$$I_s = G(j\omega)V_{ab}. \tag{3.2}$$

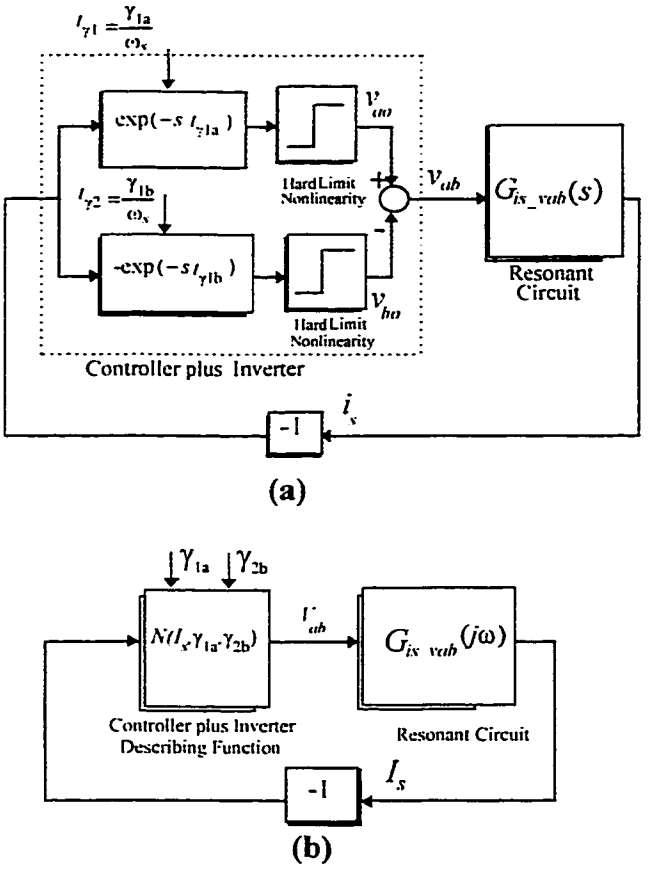


Fig. 3.3 Block diagram representations of a resonant converter operating with variable frequency plus phase-shift modulation.

(a) Block diagram. **(b)** Frequency response representation of (a).

Therefore, as I_s is different than zero, the above equations can therefore be written as:

$$G_{is\_vab}(j\omega) = -\frac{1}{N(\bar{i}_s, \gamma_{1a}, \gamma_{1b})} \tag{3.3}$$

where the describing function $N(.)$ is given by:

$$N(\bar{i}_s, \gamma_{1a}, \gamma_{1b}) = \frac{2\,v_g}{\pi\,\bar{i}_s}\left(\cos(\gamma_{1a}) + \cos(\gamma_{1b}) - j(\sin(\gamma_{1a}) + \sin(\gamma_{1b}))\right) \tag{3.4}$$

or

$$N(\bar{i}_s, \gamma_{1a}, \gamma_{1b}) = \frac{4\,v_g}{\pi\,\bar{i}_s}\cos\left(\frac{\gamma_{1a} - \gamma_{1b}}{2}\right)\left[\cos\left(\frac{\gamma_{1a} + \gamma_{1b}}{2}\right) - j\sin\left(\frac{\gamma_{1a} + \gamma_{1b}}{2}\right)\right] \tag{3.5}$$

The amplitude $\bar{i}_s$ and frequency ω which satisfy (3.3) are the amplitude of the first harmonic component of the i_s and the switching frequency of the converter ω_s respectively. In the case where γ_{1a} is equal to γ_{1b} the equation (3.5) becomes equal to the equation (2.1). The graphical solution of (3.3) is obtained by plotting the loci of the negative inverse of the describing function (3.4) and sinusoidal transfer function from the inverter output voltage to current i_s in the complex plane, as carried out in Chapter 2. The stability of the self-sustained oscillation can be examined by applying small perturbations in the amplitude of $\bar{i}_s$ at the intersection point of the above mentioned loci. If if $180° < (\gamma_{1a}+\gamma_{1b}) < 360°$ a series-parallel resonant converter operates in self-sustained oscillation with lagging power factor mode.

3.2.1 Variable Frequency

By making γ_{1a} equal to γ_{1b} the converter operates with variable frequency (VF), where a square voltage applied by the inverter in the resonant circuit. The operation above the resonance frequency can be ensured by limiting the maximum value of γ_{1a} and γ_{1b} to be smaller than 180° and greater then 90°, which is in agreement with the results presented in Chapter 2.

3.2.2 Variable Frequency plus Phase-Shift Modulation

By fixing γ_{1a}, say equal to 180°, and using γ_{1b} as the control variable, the converter operates as a combination of variable frequency and phase shift modulation (VFPSM). In

practical implementations the angle γ_{1a} is made smaller than 180°, ensuring enough current to charge and discharge the snubber capacitors during the dead time.

3.2.3 Static Characteristics for Operation with VFPSM

The static characteristics of a series parallel converter when operating in self-sustained oscillation mode will be derived using a procedure similar to that used in Chapter 2. As a first step, the equality (3.3) will be represented as two nonlinear equations. One is associated with the real part of (3.3) and the other with the imaginary part, which are:

$$[1-\alpha^2]\frac{\pi\omega_o L_s \tilde{i}_s}{\cos(\frac{\gamma_{1a}-\gamma_{1b}}{2})v_g} = -4\left[-\frac{\alpha^2\pi^2}{\beta Q_s 8}\cos(\frac{\gamma_{1a}+\gamma_{1b}}{2})+\alpha\sin(\frac{\gamma_{1a}+\gamma_{1b}}{2})\right] \tag{3.6}$$

and

$$[(1+\beta)-\alpha^2]\frac{\omega_o L_s \tilde{i}_s}{\beta\cos(\frac{\gamma_{1a}-\gamma_{1b}}{2})v_g} = -\frac{32Q_s}{\pi^3}\left[\cos(\frac{\gamma_{1a}+\gamma_{1b}}{2})+\frac{\alpha\pi^2}{\beta Q_s 8}\sin(\frac{\gamma_{1a}+\gamma_{1b}}{2})\right] \tag{3.7}$$

where β is the ratio between the series and the parallel resonant capacitors. It is worthwhile to note that the (3.6) and (3.7) become identical to the (2.12) and (2.13), respectively when γ_{1a} equals to γ_{1b} and β=1. Fig. 3.4 shows the voltage conversion ratio M obtained from the simultaneous solution of (3.6) and (3.7). In order to avoid solutions that are associated with operation below the resonant frequency, the following constraint on the switching frequency ratio α must be considered:

$$\alpha > 1. \tag{3.8}$$

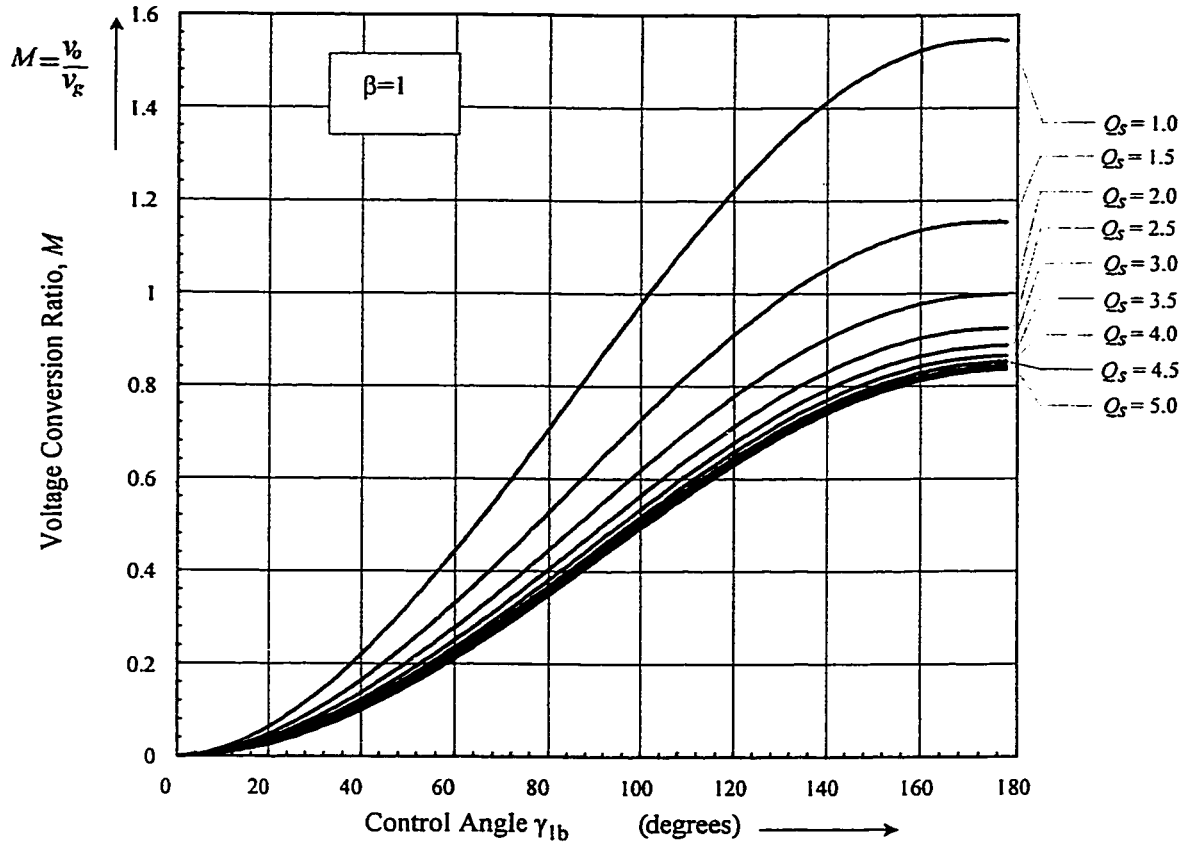


Fig. 3.4 Voltage conversion ratio as a function of the control angle for operation with variable frequency plus phase shift modulation.
(γ_{1a}=180°, β=1.)

3.2.4 Input-Output Power Balance Constraint and Quality Factor

When a loss-less resonant circuit is in sinusoidal steady-state operation, the average power sent by the inverter to the resonant circuit, p_{in}, over one switching interval, is equal to the averaged power delivered by the resonant circuit to the output stage, p_o. Therefore, the quality factor Q_s can be expressed in terms of the output voltage and input power in the following way:

$$Q_s = \frac{\omega_o L_s}{\frac{v_o^2}{p_{in}}} \tag{3.9}$$

In this section a procedure to obtain the control angles, the currents, as well as the voltages in the resonant converter when the circuit Fig. 3.1 operates with unity power factor power factor and constant output voltage is presented. This procedure will later be used as tool for the derivation of the design curves required for the selection of the power circuit components.

3.3 OPERATION WITH UNITY POWER FACTOR

When single-phase converters, as the one shown in Fig. 3.1, are operated with unity input power factor, they draw a sinusoidal current from the ac mains that is in phase with the incoming ac voltage. Therefore, the input power is

$$p_{in} = P_{in} \sin^2(\omega_{60} t) \tag{3.10}$$

where ω_{60} is the frequency of the ac mains expressed in radians per second.

Noting that the switching frequency is much higher than the ac mains frequency, usually more than 1000 times, it is reasonable to assume that the resonant circuit is in steady-state operation at each point along the input line cycle. Therefore, the static characteristics derived in the previous section can be used to investigate the operation of the ac-dc converter of Fig. 3.1.

As the power absorbed by the converter changes along the input line cycle, the quality factor Q_s also does change. The quality factor Q_s can be obtained by substituting (3.10) into (3.9), i.e.,

$$Q_s = \frac{\omega_n L_s}{v_n^2} P_{in} \sin^2(\omega_{60} t) = Q_{s\,max} \sin^2(\omega_{60} t) \tag{3.11}$$

A procedure to find the maximum voltage conversion ratio of the ac-to-dc resonant converter has to be defined since both the input voltage v_g and the quality factor

Q_s change along the input line cycle. In order to define this procedure, the first step is to identify the control angle at the resonant frequency. For operation of the resonant circuit with lag power factor the control angle $0<\gamma_{1b}<180^o$ ($\gamma_{1a}=180^o$). On the other hand, it is desirable to switch the converter above the resonance frequency, since in this range the sign of the gain of the converter does not change. However, angle γ_{1b} at the resonant frequency, depends on Q_s and β as shown in Fig. 3.5. The angle γ_{1b} at the resonant frequency is obtained from the simultaneous solution of (3.6) and (3.7). The minimum value of each curve of Fig. 3.5 represents the values at which the control angle γ_{1b} must be limited to ensure operation above the resonant frequency under all operating conditions. With the maximum value of the angle γ_{1b} defined, the maximum voltage conversion ratio as a function of the Q_s can be found by solving (3.6) and (3.7) for given value of β. The resulting curves which summarize the maximum voltage conversion ratio of the ac-to-dc converter are given Fig. 3.6. To simplify the analysis, the map from Q_s to M, will be represented as $M(Q_s,\beta)$. By using this map the inequality that must be satisfied for operation with both constant output voltage, and unity power factor the can be expressed as

$$M(Q_{s\,max}\sin^2(\omega_{60}t),\beta) \geq \frac{v_o}{|\hat{v}_g \sin(\omega_{60}t)|} \tag{3.12}$$

or

$$M(Q_{s\,max}\sin^2(\omega_{60}t),\beta)\,|\sin(\omega_{60}t)| \geq \frac{v_o}{\hat{v}_g} \tag{3.13}$$

The maximum value of the right side of (3.13) can be readily identified since the output voltage, v_o, is constant and the minimum peak value of the input voltage is usually

a well known quantity for a given application. The minimum peak value of the input voltage is here denoted by $\hat{v}_{gm}$. On the other hand, the minimum value of the product at left side of (3.13) is found for each Q_{s_max} and β since the map $M(Q_s,\beta)$ is already known. Fig. 3.7 shows this product along half period of the incoming ac line. From this figure the minimum of product at the left side of (3.13) is easily identified. In summary, the maximum voltage conversion ratio of the ac-to-dc converter can be defined as

$$M_m\big|_{Q_{s\_max},\beta} = \frac{v_o}{\hat{v}_{gm}} \min(M(Q_{s\_max}\sin^2(\omega_{60}t),\beta)\,|\sin(\omega_{60}t)|) \qquad (3.14)$$

Fig. 3.8 presents the solution of (3.14) for different values of Q_{s_max} and β. On the other hand, Fig. 3.9 shows the minimum switching frequency ratio, which is a key information to compute the resonant circuit parameters.

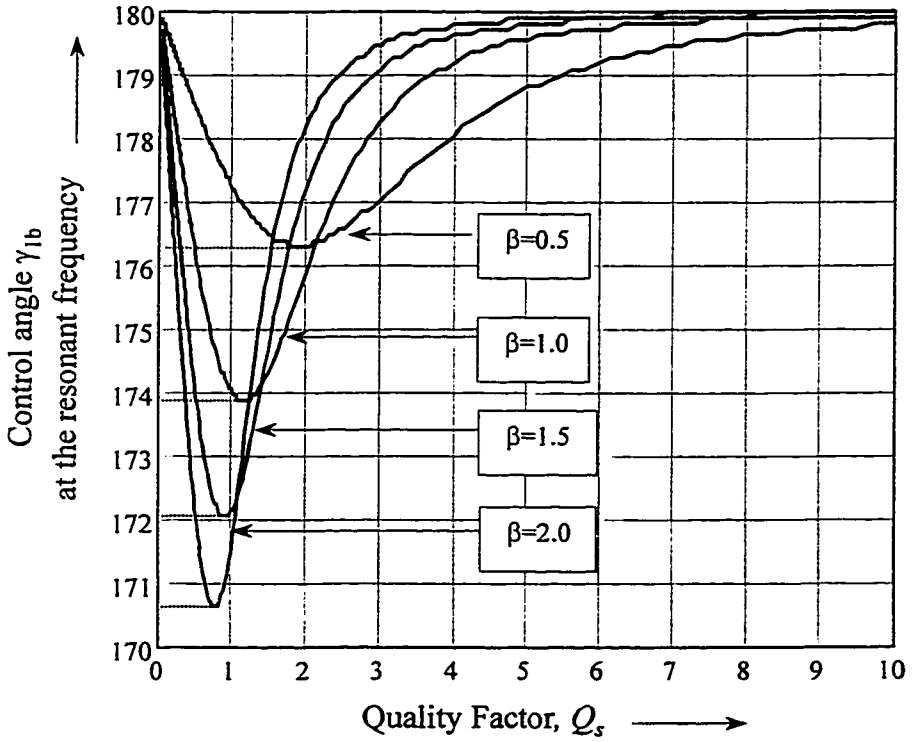


Fig. 3.5 Control angle γ_{1b} at the resonant frequency for operation with VFPSM.

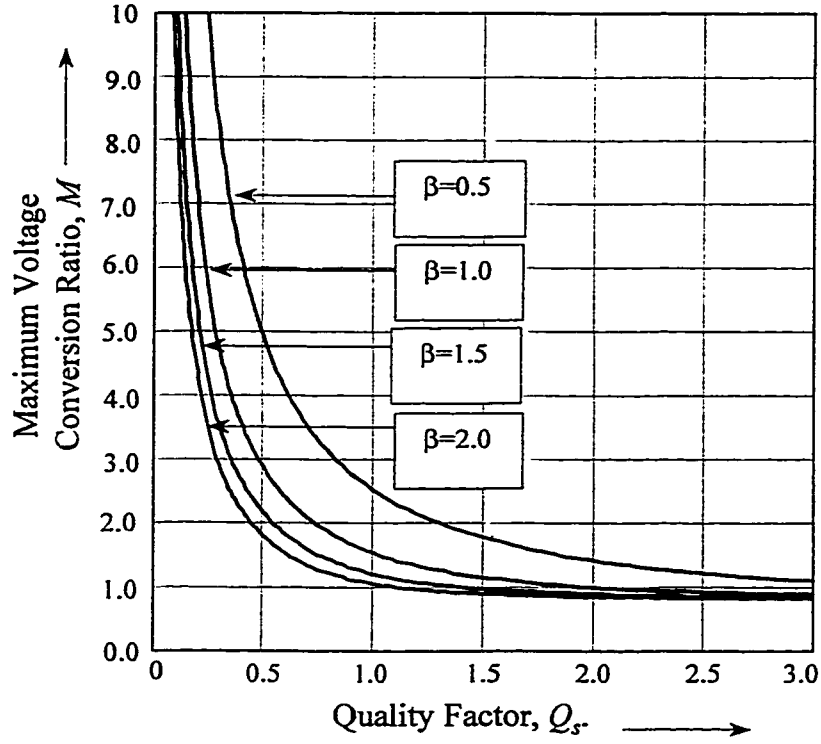


Fig. 3.6 Maximum gain of the converter for operation with VFPSM.
($\gamma_{1a}=180^{o}$, $\gamma_{1b}=176^{o}$ for $\beta=0.5$, $\gamma_{1b}=174^{o}$ for $\beta=1$, $\gamma_{1b}=172^{o}$ for $\beta=1.5$, $\gamma_{1b}=170.5^{o}$ for $\beta=2$)

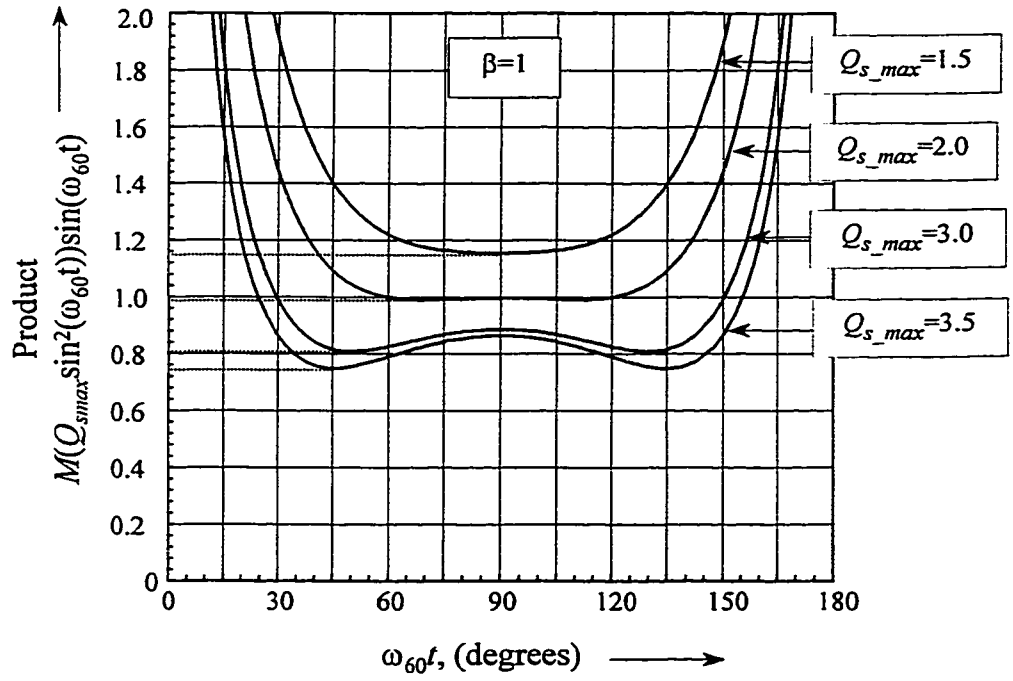


Fig. 3.7 Product $M(Q_{s\_max}\sin^2(\omega_{60}t))\sin(\omega_{60}t)$ for different values of Q_{s_max}.
($\gamma_{1a}=180^{o}$, $\gamma_{1b}=174^{o}$,$\beta=1$)

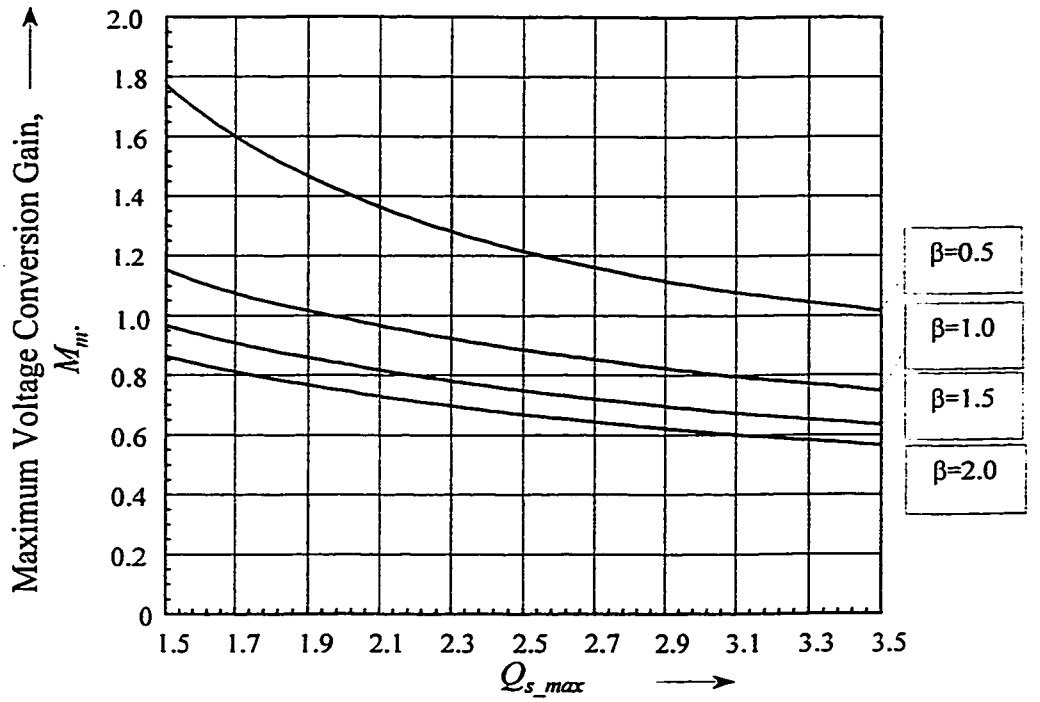


Fig. 3.8 Maximum voltage conversion ratio for operation with constant output voltage and unity input power factor.

(γ_{1a}=180°, γ_{1b}=176° for β=0.5, γ_{1b}=174° for β=1, γ_{1b}=172° for β=1.5, γ_{1b}=170.5° for β=2)

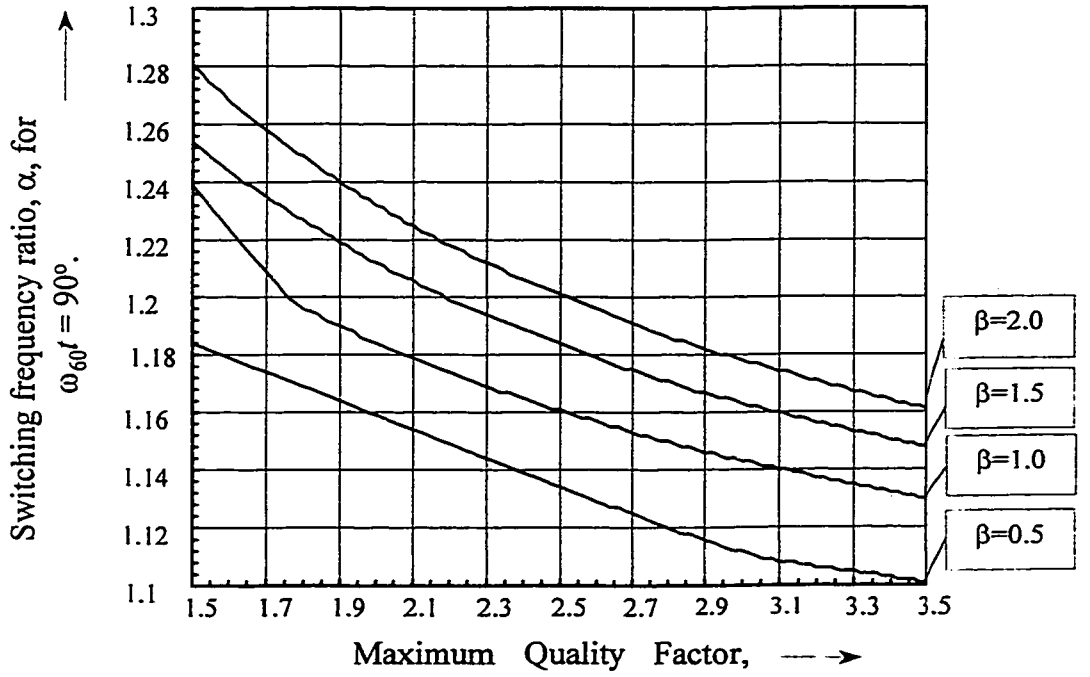


Fig. 3.9 Switching frequency ratio at $\omega_{60}t$=90°. Operation with VFPSM.

(γ_{1a}=180°, γ_{1b}=176° for β=0.5, γ_{1b}=174° for β=1, γ_{1b}=172° for β=1.5, γ_{1b}=170.5° for β=2)

3.4 COMPARISON BETWEEN VF AND VFPSM

In this Section, the two control techniques described in Section 3.2, VF and VFPSM, are compared. In comparing these approaches it is assumed that the converter operates with a input voltage ranging from 90 to 250 V and with an output load varying from full load to 10 % of the full load. In addition, typical values of Q_{smax} and β are selected for the comparison, that are Q_{smax}=2.7 and β=1. The maximum voltage conversion ratio associated with these values of Q_{smax} and β is found from Fig. 3.8 to be equal to 0.85.

The following ratios are defined and are used to carry out the comparison:

$\frac{\hat{v}_g}{\hat{v}_{gm}}$ The ratio between the peak value of the input voltage and the peak value of the lowest input voltage.

$\frac{i_{s\_rms}}{\hat{i}_{gm}}$ The ratio between the rms value of the current in the resonant inductor, computed over one switching period and the peak value of the input current when the converter is operating at full load and with the lowest input voltage.

$\frac{\omega_s}{\omega_o}$ The ratio between the switching frequency and the resonant frequency associated with the series resonant branch.

3.4.1 Control Angles for Operation with Unity Power Factor and Constant Output Voltage

Fig. 3.10 shows the control angles required for operation with unity input power factor and constant output voltage constant. At full load with minimum input voltage the control angles approach 180°. On the other hand, for increasing values of the input

voltage or for decreasing loads the control angles reduce. In the case of VF the control angle moves towards 90° and in the case of VFPSM towards 0, compensating for the high gain of the converter.

3.4.2 Current through the Resonant Inductor

The current through the resonant inductor plays an important role in the design of the converter. It is because this current has a direct impact on the inverter conduction losses, inductor rating as well as in the voltage stress across the series resonant capacitor.

Fig. 3.10 shows the "instantaneous rms" current through the series resonant inductor along the half period of the input line cycle when the converter is operating with unity power factor and a constant output voltage. VFPSM results in smaller current stresses as compared with the VF, especially when operating with voltages higher than the lowest input voltage or at a fraction of full load.

3.4.3 Switching Frequency

The main advantage of the VFPSM method over the VF method is the reduction in the switching frequency range. With VFPSM, the operating frequency range can be reduced to 50% when compared with VF, as shown in Fig. 3.12. The reduction in the switching frequency leads to a decrease in the magnetic losses on the series resonant inductor and the isolation transformer.

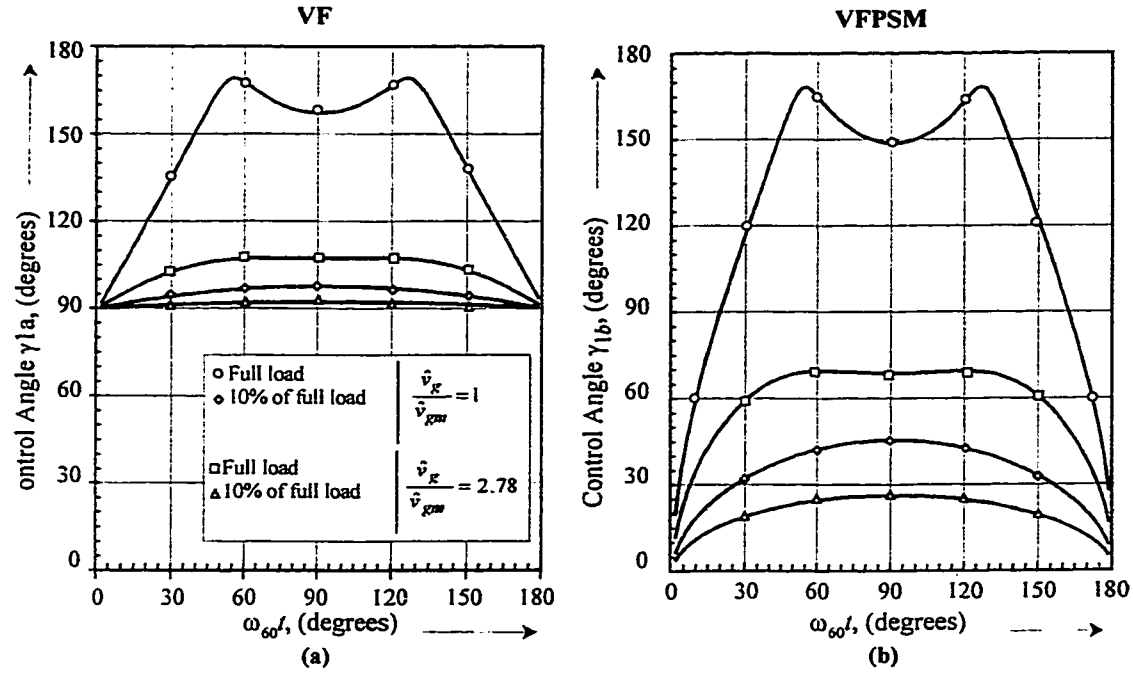


Fig. 3.10 Control angles required to keep unity input power factor and constant output voltage.

(a) Variable frequency $\gamma_{1a}=\gamma_{1b}$. (b) Variable frequency plus phase shift modulation $\gamma_{1a}=180^{o}$, $Q_{smax}=2.7.$, $\beta=1, M_m=0.85$. The lines marked with diamonds and triangles refer to operation with 10% of full load and the ones marked with circles and squares refers to operation at full load.

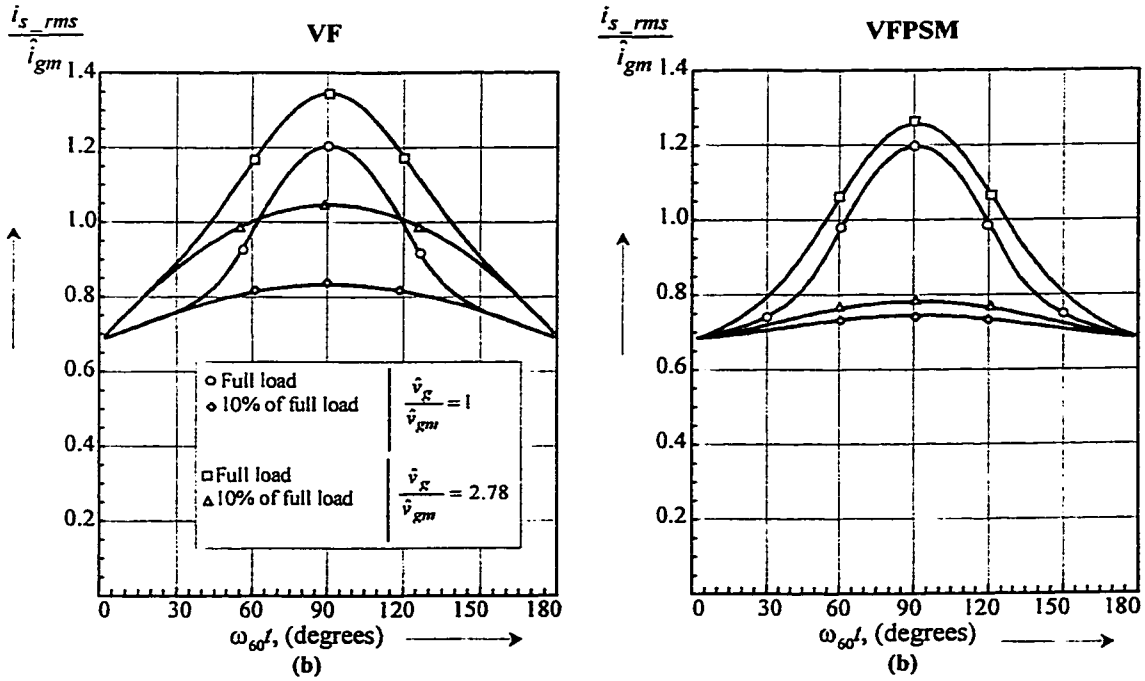


Fig. 3.11 Current through the series resonant inductor along the input line cycle.

(a) Variable frequency $\gamma_{1a}=\gamma_{1b}$. (b) Variable frequency plus phase shift modulation $\gamma_{1a}=180^{o}$. $Q_{smax}=2.7$, $\beta=1$, $M_m=0.85$. The lines marked with diamonds and triangles refer to operation with 10% of full load and the ones marked with circles and squares refers to operation at full load.

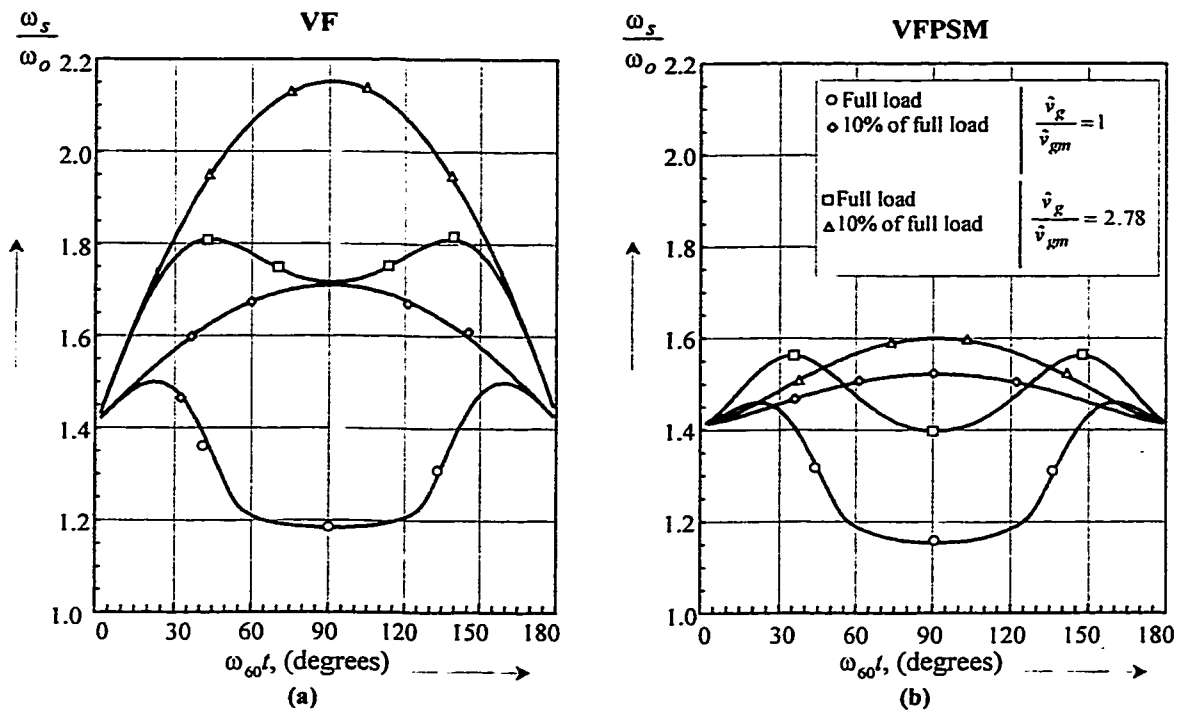


Fig. 3.12 Switching frequency ratio along half period of the input line cycle.
(a) Variable frequency $\gamma_{1a}=\gamma_{1b}$. (b) Variable frequency plus phase shift modulation $\gamma_{1a}=180^{o}$. $Q_{smax}=2.7$, $\beta=1$, $M_m=0.85$. The lines marked with diamonds and triangles refer to operation with 10% of full load and the ones marked with circles and squares refers to operation at full load.

3.5 INPUT AND OUTPUT FILTER SELECTION

This section develops a design procedure for the selection of the input and output filter parameters. These filters are designed so that the ac-dc converter of Fig. 3.1 operates with high input power factor and constant output voltage.

3.5.1 Input Filter

The input filter is used to attenuate the high frequency current harmonics injected by the inverter into the ac mains. The current at the input of the inverter i_d can be obtained from the current through the resonant inductor by considering the operation of the inverter. Once the input current waveform is defined, its harmonic components can

therefore be computed. The second and fourth harmonic components of i_d along half of ac input voltage cycle are given in Fig. 3.13 and Fig. 3.14. Clearly, with VFPSM the amplitude of the input current harmonics are smaller than with VF control.

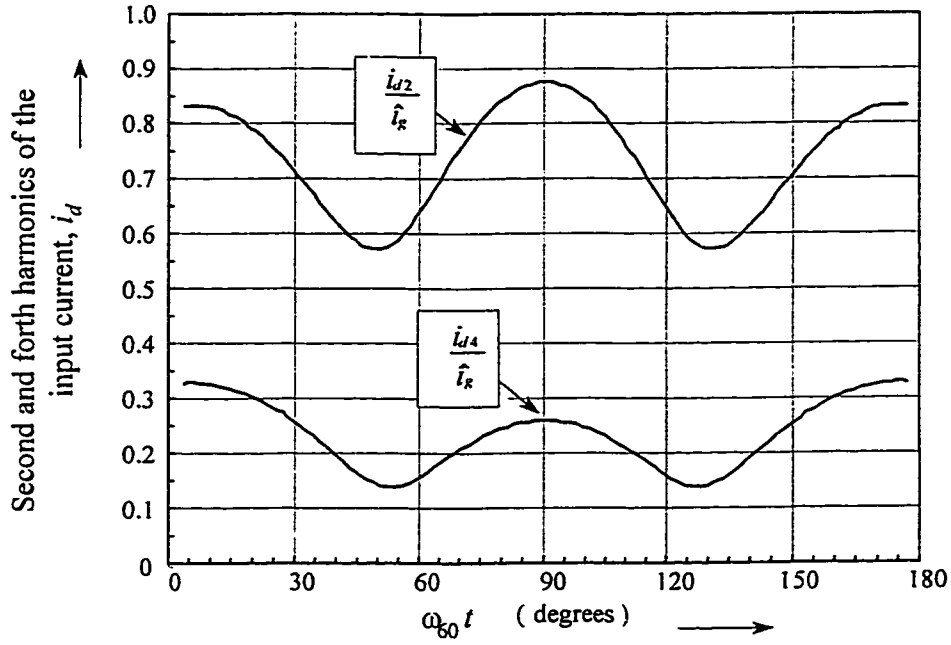


Fig. 3.13 Harmonic components of the current i_d. Operation with VF control.
γ_{1a}=180°,β=1, Q_{s_max}=2.7, M_m=0.85. Operation at full load with constant output voltage and unity input power factor.

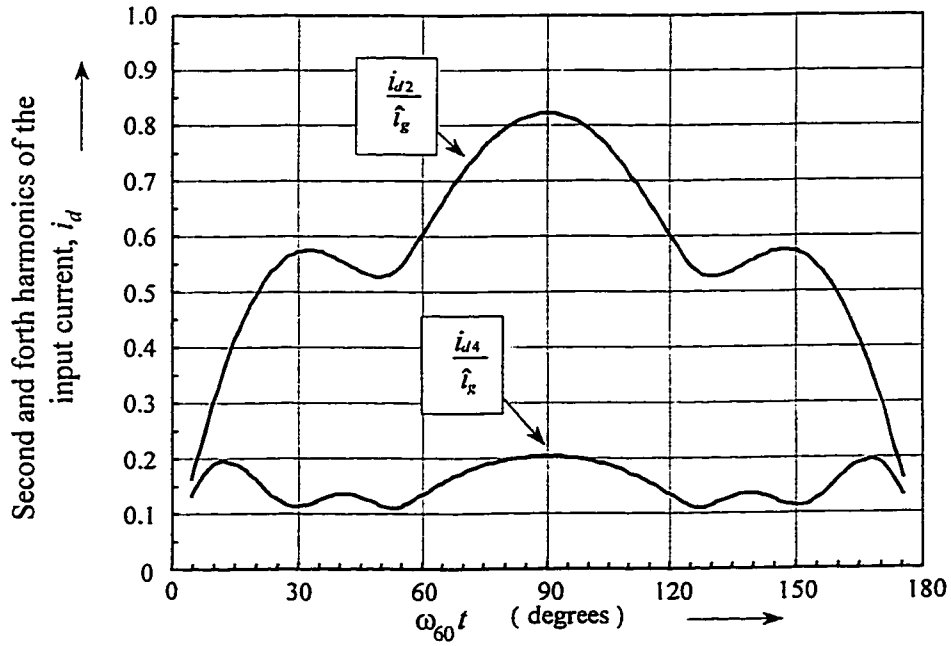


Fig. 3.14 Harmonic components of the current i_d. Operation with VFPSM.
γ_{1a}=180°,β=1, Q_{s_max}=2.7, M_m=0.85. Operation at full load with constant output voltage and unity input power factor.

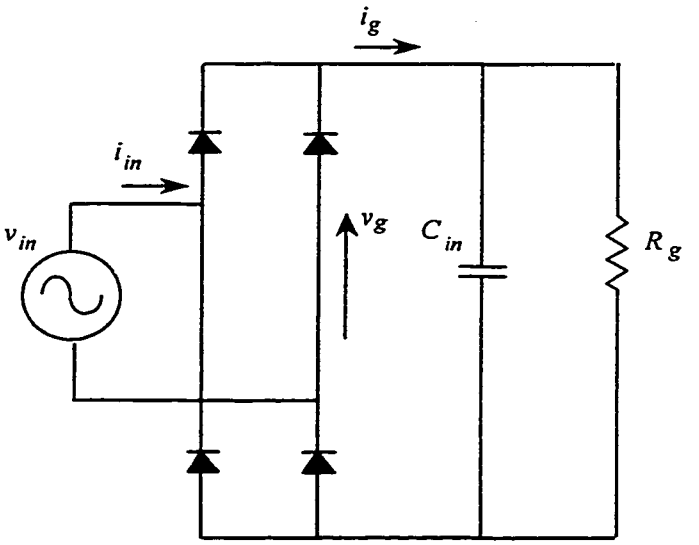
A second order LC low pass filter is usually adopted for the implementation of the input filter. Therefore, this kind of filter will be considered for the development of a procedure for the input filter design. The cut-off frequency of a second order low pass filter required to keep the amplitude of the harmonics of the input current below the maximum allowed value, can be obtained using classical ac analysis, and it is given by

$$\omega_{in} < \min\left\{\frac{n\,\omega_s\big|_{\omega_{cut}=90^\circ}}{\sqrt{\frac{1}{K_n}+1}}\right\} \quad , \; n = 2,4,\ldots \quad \text{(rad/s)} \tag{3.15}$$

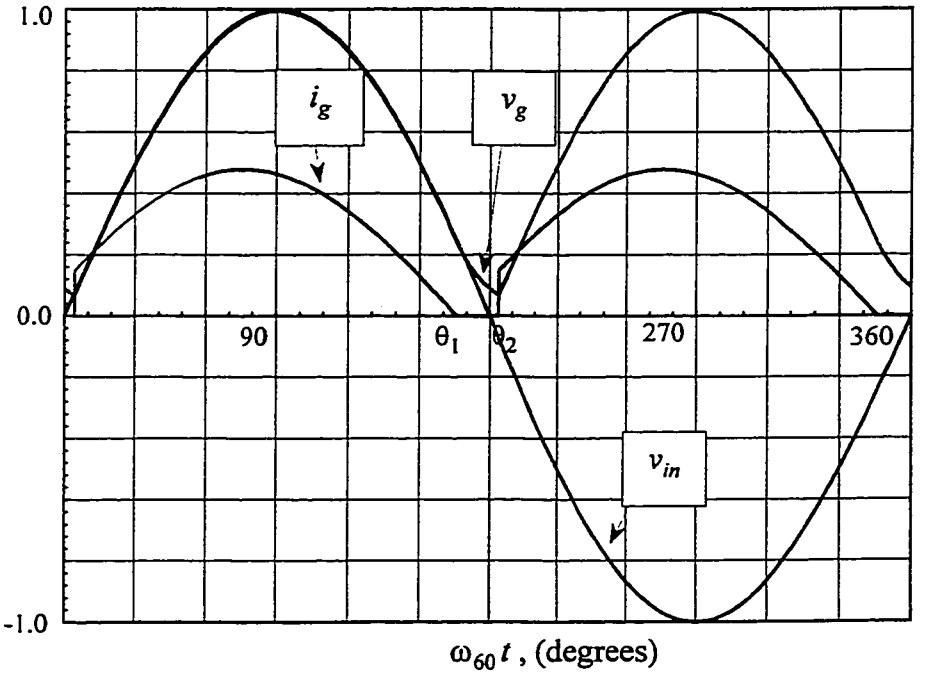
where $\omega_{in} = \frac{1}{\sqrt{L_{in}C_{in}}}$ and K_n is the attenuation factor of the *n-th* harmonic. The attenuation factor is defined as: $K_n = \frac{i_{gn}}{i_{dn}}$. For example: To attenuate the harmonic component of i_d at twice the switching frequency, i_{d2}, to 5% of the input peak current value, the attenuation factor should be $K_n = \frac{0.05}{0.9}$ and $\omega_{in} < 0.485\,\omega_s\big|_{\omega_{cut}=90^\circ}$, where ω_s is the switching frequency at full load.

When selecting the value of the input filter capacitor C_{in}, a trade-off between voltage ripple at the input of the inverter and distortion of the input current, i_{in}, near the zero crossing point of the input voltage, must be considered. When operating with low power at the output or with large values of C_{in} the current i_{in} becomes discontinuous in the vicinity of the input voltage zero crossing. As a result, the total harmonic distortion of the input current increases and the input power factor decreases. Let us consider the circuit of Fig. 3.15 (a) to quantify the impact of value of the input filter capacitor C_{in} on the THD of the input current and on the input power factor (PF). The relevant waveforms of this circuit are shown in Fig. 3.15 (b). The angles θ_1 and θ_2 define the duration of the interval when the input current is zero. These angles are obtained

considering the operation of the circuit of Fig. 3.15 (a) and they can be used to define the input current waveform, THD, and input PF.



(a)



(b)

Fig. 3.15 Input rectifier operation with capacitive input filter.
(a) Circuit diagram. **(b)** Main waveforms

Fig. 3.16 shows the THD of the input current, i_{in}, as well as the input power factor as a function of the product $C_{in}\omega_{60}R_g$. The values of ω_{60} and R_g are usually well-defined quantities. The value of R_g depends on both the input voltage and the power absorbed by the converter. By using the graph of Fig. 3.16 the value of C_{in} can be selected to result in an acceptable THD of the input current.

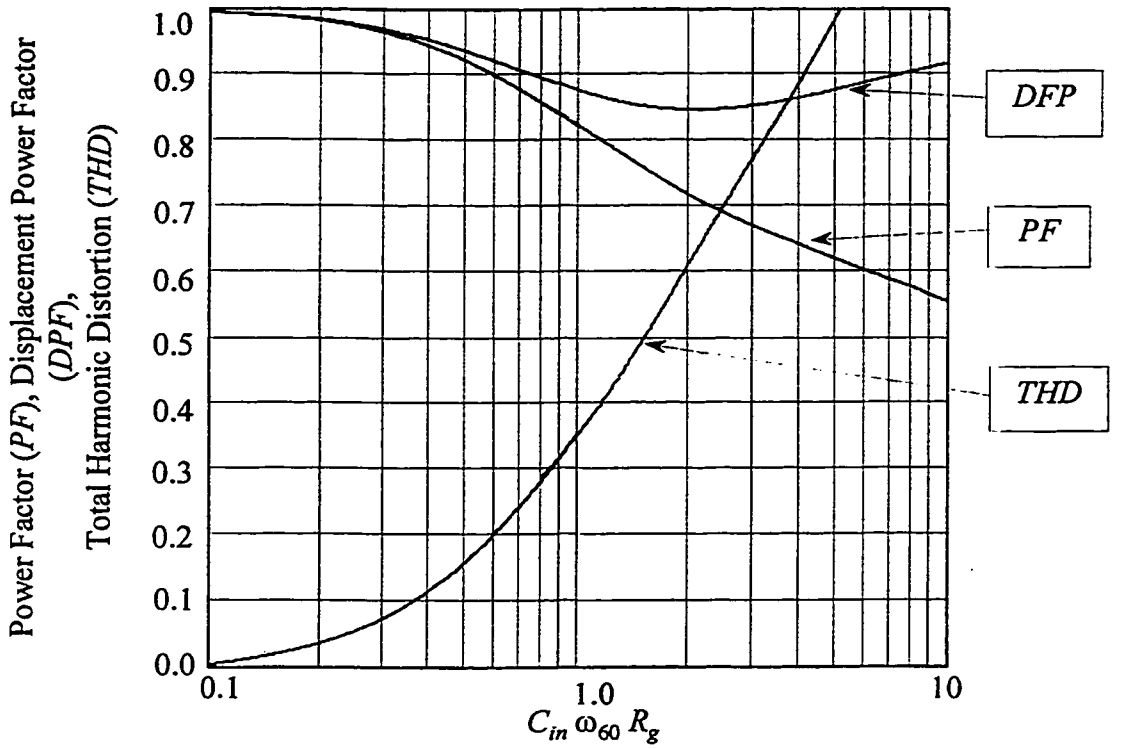


Fig. 3.16 Power factor, displacement power factor, and total harmonic distortion of the input current, i_{in}, as a function of the product $C_{in}\,\omega_{60}\,R_g$

3.5.2 Output Filter

The output filter is used for two purposes: The first is to attenuate the low frequency ripple (120Hz) in the output voltage, which comes from the pulsating nature of the power absorbed from the ac mains. The second is to attenuate the high frequency ripple current in the output dc stage. This high frequency current has a dominant

frequency component at twice the switching frequency, which is a result of the rectification of the quasi-sinusoidal voltage of the high frequency transformer. The second order LC filter at the output of the ac-dc of Fig. 3.1can be design as follows: First, the peak-to-peak voltage ripple on the output capacitor is calculated from the waveform of the current through it. It is assumed that all ac frequency components of current i_o flow through the capacitor and that the dc component of i_o flows through the load, therefore, the maximum variation of the charge of the capacitor can be found as

$$\Delta Q = \frac{1}{\omega_{60}} \int_{\frac{\pi}{4}}^{\frac{3\pi}{4}} (2I_o \sin^2(\omega_{60}t) - I_o) d\omega_{60}t \quad \text{(C)}. \tag{3.16}$$

The capacitor required to satisfy a given voltage ripple specification, based (3.16), is

$$C > \frac{1}{\omega_{60}} \frac{I_0}{v_0} \frac{1}{Ripple_v} \quad \text{(F)} \tag{3.17}$$

where $Ripple_v = \frac{\Delta v_o}{v_o}$. On the other hand, the high frequency ripple of the current i_o can be computed from the waveform of the voltage across the inductor. The inductor required to attenuate the current ripple at the output of the diode rectifier can be found as:

$$L > \frac{0.66}{\omega_s} \frac{v_o}{I_o} \frac{1}{Ripple_I} \quad \text{(H)} \tag{3.18}$$

where $Ripple_I = \frac{\Delta i_o}{I_o}$.

3.6 Dynamic Model for Operation with Variable Frequency plus Phase Shift Modulation

In applications which require low THD in the input current a controller, which is used to shape the input current into a sinusoidal waveform, is usually required. The design of the controller is often based on a model of the system. In order to obtain this

model the extended describing approach will be used in a similar way as that carried out in Chapter 2. However, the model derived here is slightly different since it considers the operation with variable frequency plus phase shift modulation.

When operating with variable frequency plus phase shift modulation the nonlinearity associated with the self-sustained oscillation controller and the inverter can be expressed as:

$$v_{ab} = -v_{cin}\,\mathrm{sgn}(i_s(t - t_{\gamma 1a}) - v_{cin}\,\mathrm{sgn}(i_s(t - t_{\gamma 1b}) \tag{3.19}$$

The nonlinearity associated with (3.19) can be evaluated using the describing function approach by making the following assumptions: (i) The current i_s is sinusoidal over one switching interval, (ii) the voltage v_{cin} is constant in one switching interval and the amplitude of the saw tooth signal is constant. In this case, the first harmonic component can be expressed as:

$$f_s(.)\sin(\psi(t)) + f_c(.)\sin(\psi(t)) \tag{3.20}$$

where the function $f_s(.)$ and $f_c(.)$ are given by:

$$f_s(.) = \frac{-2}{\pi}\frac{\bar{v}_{cin}}{\hat{i}_s}\{i_{ss}[\cos(\gamma_{1a}) + \cos(\gamma_{1b})] + i_{sc}[\sin(\gamma_{1a}) + \sin(\gamma_{1b})] \tag{3.21}$$

$$f_c(.) = \frac{-2}{\pi}\frac{\bar{v}_{cin}}{\hat{i}_s}\{-i_{ss}[\sin(\gamma_{1a}) + \sin(\gamma_{1b})] + i_{sc}[\cos(\gamma_{1a}) + \cos(\gamma_{1b})]\} \tag{3.22}$$

and the variables in equations (3.20) to (3.22) are defined as in Chapter 2.

On the other hand, the current at the input of the inverter, i_d, is given by:

$$i_d = [\mathrm{sgn}(i_s - t_{\gamma 1a}) + \mathrm{sgn}(i_s - t_{\gamma 1b})]i_s \tag{3.23}$$

Taking into account that the input dc capacitor, C_{in}, has a small voltage ripple, only the average value of (3.21) is retained. The average value of the current i_d over one switching period can be determined as:

$$\bar{i}_d = -\frac{1}{\pi}\bar{i}_s\left[\cos(\gamma_{1a}) + \cos(\gamma_{1b})\right] \tag{3.24}$$

where the bar over i_d is used to denote average value over one switching period.

The equation (2.28) can be modified to include the dynamics of the input filter and to represent the operation with VFPSM by substituting the nonlinearities associated with the inverter by the (3.21). (3.22) and (3.24), i.e.,

$$\begin{aligned}
\frac{di_{ss}}{dt} &= -\frac{i_{ss}\, i_{sc}}{C_s\, v_{sc}} - \frac{1}{L_s}\left[r_s\, i_{ss} + v_{ps} + \frac{2}{\pi}\frac{\bar{v}_{cin}}{\sqrt{i_{ss}^{\,2} + i_{sc}^{\,2}}}\left\{ i_{ss}\left[\cos(\gamma_{1a}) + \cos(\gamma_{1b})\right] + i_{sc}\left[\sin(\gamma_{1a}) + \sin(\gamma_{1b})\right]\right\}\right] \\
\frac{di_{sc}}{dt} &= \frac{i_{ss}\, i_{ss}}{C_s\, v_{sc}} - \frac{1}{L_s}\left[r_s\, i_{sc} + v_{sc} + v_{pc} + \frac{2}{\pi}\frac{\bar{v}_{cin}}{\sqrt{i_{ss}^{\,2} + i_{sc}^{\,2}}}\left\{ - i_{ss}\left[\sin(\gamma_{1a}) + \sin(\gamma_{1b})\right] + i_{sc}\left[\cos(\gamma_{1a}) + \cos(\gamma_{1b})\right]\right\}\right] \\
\frac{dv_{sc}}{dt} &= \frac{i_{sc}}{C_s} \\
\frac{dv_{ps}}{dt} &= -\frac{i_{ss}\, v_{pc}}{C_s v_{sc}} + \frac{1}{C_p}\left[i_{ss} - \frac{4}{\pi}\bar{i}_a \frac{v_{ps}}{\sqrt{v_{ps}^2 + v_{pc}^2}}\right] \\
\frac{dv_{pc}}{dt} &= \frac{i_{ss}\, v_{ps}}{C_s\, v_{sc}} + \frac{1}{C_p}\left[i_{sc} - \frac{4}{\pi}\bar{i}_a \frac{v_{pc}}{\sqrt{v_{ps}^2 + v_{pc}^2}}\right] \\
\frac{d\bar{i}_g}{dt} &= \frac{1}{L_{in}}(-r_{in}\,\bar{i}_g - \bar{v}_{cin} + \bar{v}_g) \\
\frac{d\bar{v}_{cin}}{dt} &= \frac{1}{C_{in}}\left\{ \bar{i}_g + \frac{1}{\pi}\sqrt{i_{ss}^{\,2} + i_{sc}^{\,2}}\left[\cos(\gamma_{1a}) + \cos(\gamma_{1b})\right]\right\} \\
\frac{d\bar{i}_a}{dt} &= \frac{1}{L_a}\left(\frac{2}{\pi}\sqrt{v_{ps}^2 + v_{pc}^2} - \bar{v}_a\right) \\
\frac{d\bar{v}_a}{dt} &= \frac{1}{C_a}\left(-\frac{\bar{v}_a}{R_l} + \bar{i}_a\right)
\end{aligned} \tag{3.25}$$

The frequency response of a small signal model derived from (3.25) and the experimental measurements made under the same operating conditions are shown in Fig. 3.17. Good agreement was found up to half of the switching frequency. The discrepancy near the resonant frequency is attributed to the neglected power circuit losses.

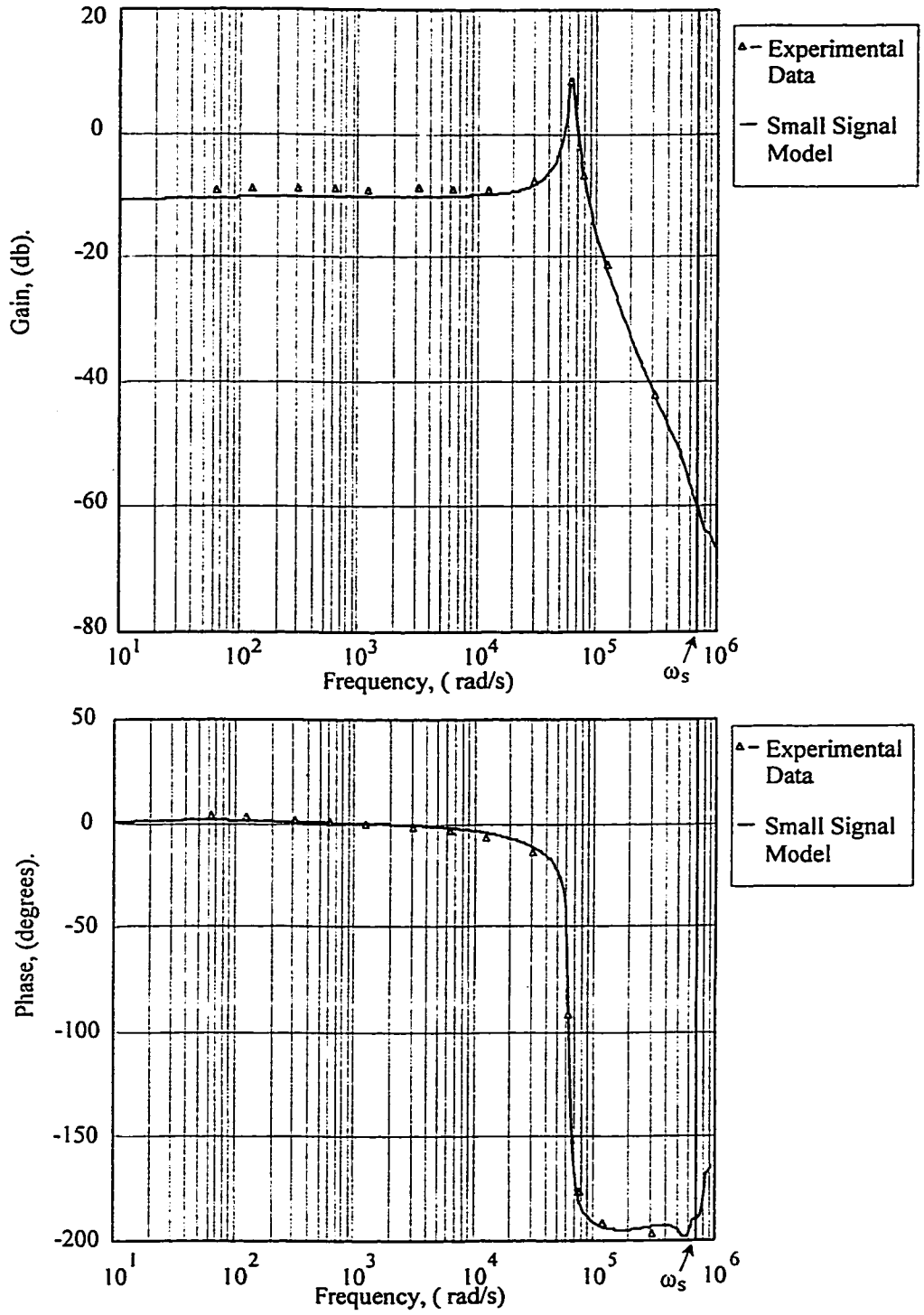


Fig. 3.17 Bode plot. Frequency response of the input current i_g to small changes in the control angle γ_{1b}.

γ_{1a}=170°, v_g=150V, v_o=136.5V, L_s=208μH, C_s=C_p=15.8nF, C_o=572μF, L_o=229μH, C_{in}=2μH, L_{in}=132μH, R_L=60.8Ω

3.7 EXPERIMENTAL RESULTS

This section presents experimental results from a 600W series-parallel resonant ac-to-dc converter prototype aiming to verify the feasibility of the proposed control technique and to demonstrate the performance of the converter. The converter operates from a 220 V ac supply and it produces an isolated 100 V dc output.

3.7.1 Design Procedure for the Resonant Circuit Parameters

In order to select the resonant circuit parameters the curves derived in Section 3.3, Fig. 3.8 and Fig. 3.9, can be used. The following procedure is suggested for the selection of the resonant circuit parameters:

(i) Select the values of Q_{smax} and β. From Fig. 3.8 find the maximum voltage conversion ratio. For example, Q_{smax}=2.94 and β=1 result in a maximum voltage conversion ratio M_m=0.82. The minimum switching frequency ratio that corresponds to this value of Q_{smax} and β can be found from Fig. 3.9, that is α =1.145.

(ii) Select the minimum switching frequency and compute the series resonant inductor and the resonant capacitors. For example, if the minimum switching frequency is 100 kHz the resonant frequency can be found as follows:

$$\omega_n = \frac{\min(\omega_s)}{\alpha} = 551 \cdot 10^3 \text{ rad/s} \ . \tag{3.26}$$

The series resonant inductor is found by solving (3.8) for L_s, that is

$$L_s = \frac{Q_s \dfrac{M_m^{\,2}\hat{v}_{gm}^2}{P_{in}}}{\omega_o} = 208.5\,\mu\text{H} \tag{3.27}$$

where, $P_{in}/2$ is made equal to 675 W to compensate for the losses in the circuit, and $\hat{v}_{gm}$ is the peak value of the lowest input voltage. The value of the series resonant capacitor and the parallel resonant capacitor reflected to the primary side of the transformer are

$$C_s = \frac{1}{\omega_o^2 L_s} = 15.8\,\text{nF} \text{ and } C_p = \frac{C_s}{\beta} = 15.8\,\text{nF}. \tag{3.28}$$

(iii) Select the turns ratio of the isolation transformer to step-down the voltage v_o to the value required at the output of the converter. The dc output voltage for operation without isolation transformer is given by

$$v_o = M_m\, v_{gm} = 229\,\text{V}. \tag{3.29}$$

Therefore, for an output voltage equal to 100V the turns ratio of the transformer is

$$\frac{n_1}{n_2} = 2.29\ . \tag{3.30}$$

3.7.2 Converter Static Performance

This sub-section aims to validate the concepts developed in the previous sections. For operation with VFPSM the angle γ_{1a} is kept constant at the value close to 180° and the γ_{1b} can be adjusted to meet the load requirements. Typical inverter output voltage and current for operation with VFPSM are shown in Fig. 3.18. It was verified experimentally that the current always crosses zero inside of the non zero voltage pulse at output of the

inverter, resulting in the required current to reset the snubbers capacitor and provide ZVS. In order to illustrate the operation with zero voltage switching, the voltage across the leg B of the inverter and the gate-source voltage of the bottom switches at three operating conditions, which are short-circuit, full-load and no-load, are shown in Fig. 3. 18. It is possible to see that when the gate-source voltage becomes high, the drain-source voltage is already zero indicating that zero voltage switching takes place.

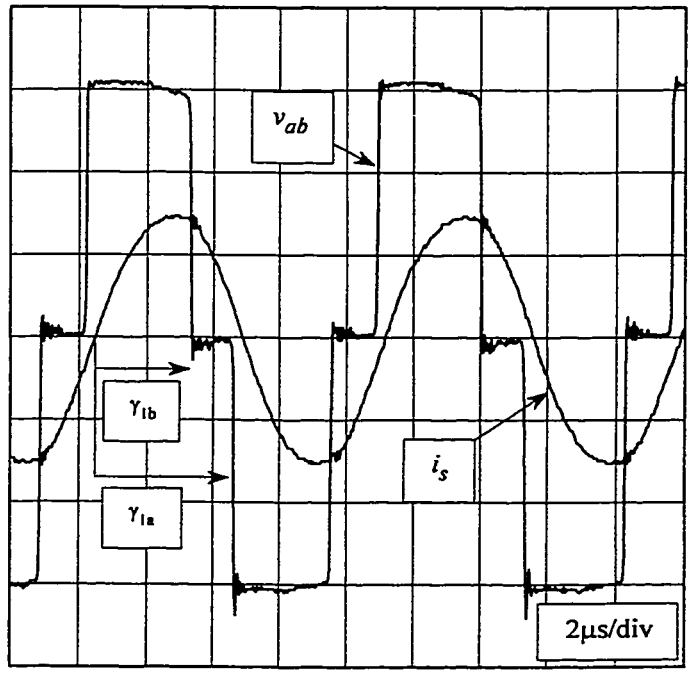
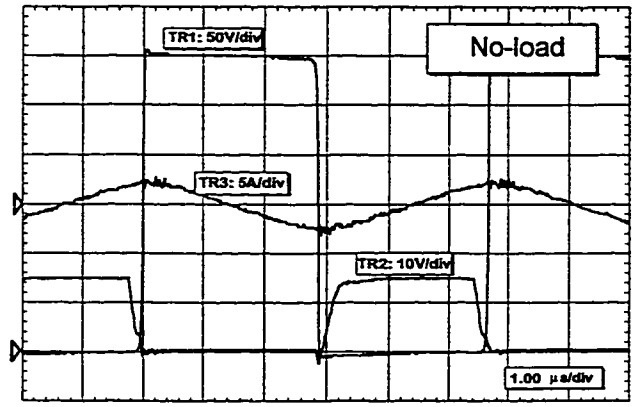
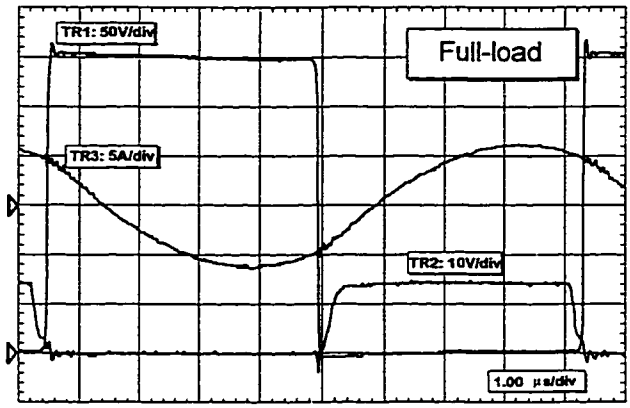


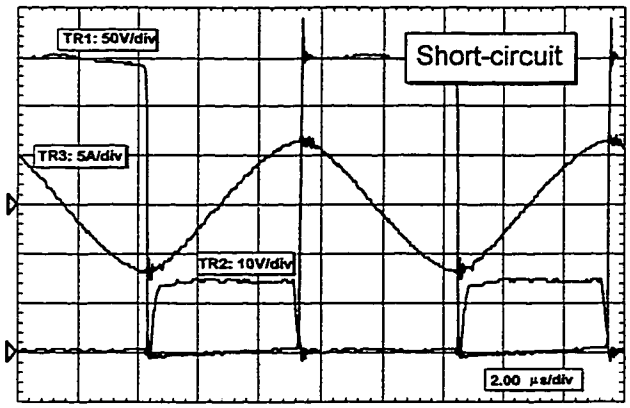
Fig. 3.18 Experimental results. Operation with VFPSM.
v_g=150V,v_o=49.8,i_o=4.49, γ_{1a}=168°, γ_{1b}=115.5°, n_1/n_2=2.29,L_s=208μH,C_s=15.5nF,C_{in}=2μF,L_{in}=138 μH.
Vertical Scales: 50V/div and 2.5A/div. Horizontal Scale: 2μs/div.



(a)



(b)



(c)

Fig. 3.19 Experimental results showing zero voltage switching during no-load, full-load, and short-circuit.

TR1 voltage across the leg B of the inverter v_{bo}, **TR2** gate to source voltage of the Leg B bottom transistor (v_{gs2}), **TR3** current through the series resonant inductor i_s,.Operation near to the peak of the input ac line.**(a)** no-load operation, **(b)** full-load operation, **(c)** short-circuit operation.

On the other hand, Table 3.1 presents results obtained experimentally and analytically using the expression derived in Sections 3.3 and 3.6. The results obtained

from describing function method and from the modulation equation are identical. As in Charter 2. it is possible to demonstrate that (3.35) has a steady state solution that satisfies and (3.3). On the other hand. experimental results for both VF and VFPSM are in good agreement with the analytically results. This is because with $\beta=1$ and $Q_s<2$, (Appendices 1 and 2). the converter operates in continuous capacitor voltage mode where the resonant circuit variables have a predominant first harmonic component.

TABLE 3.1 COMPARISON BETWEEN ANALYTICAL AND EXPERIMANTAL RESULTS

	VF			**VFPSM**		
	Q_s=1.86, γ_{1a}= 150.7°,γ_{1b}=150.7°			Q_s=1.86, γ_{1a}=178.3°,γ_{1b}=134.4°		
	M1	*M2*	*M3*	*M1*	*M2*	*M3*
$M=\frac{v_o}{v_g}$	0.93	0.93	0.91	0.90	0.90	0.91
$\alpha=\frac{\omega_s}{\omega_o}$	1.31	1.31	1.32	1.28	1.28	1.27
$\bar{i}_s\frac{Q_s R_L}{v_g}$	2.93	2.93	2.98	2.80	2.80	2.98
	Q_s=0.545 , γ_{1a}=105.9°,γ_{1b}=105.9°			Q_s=0.545, γ_{1a}=178.3°,γ_{1b}=66.4°		
	M1	*M2*	*M3*	*M1*	*M2*	*M3*
$M=\frac{v_o}{v_g}$	0.87	0.87	0.92	0.88	0.88	0.92
$\alpha=\frac{\omega_s}{\omega_o}$	1.67	1.67	1.64	1.53	1.53	1.50
$\bar{i}_s\frac{Q_s R_L}{v_g}$	2.64	2.64	2.38	2.20	2.20	2.03

M1 -Describing function method.
M2- Modulation equation equilibrium point.
M3- Experimental results (L_s=208μH. C_s=15.8 nF. C_p=15.8 nF. v_g=150 V).

Fig. 3.20 and Fig. 3.21 show the overall efficiency of the converter as a function of the input voltage and output power for both VF and VFPSM. It is possible to see that VFPSM and VF result in similar performance at full load and minimum input voltage. However, as the input voltage increases, or the output load decreases the VFPSM method results in better efficiency than VF. This is because the VFPSM results in a narrowed range of switching frequency.

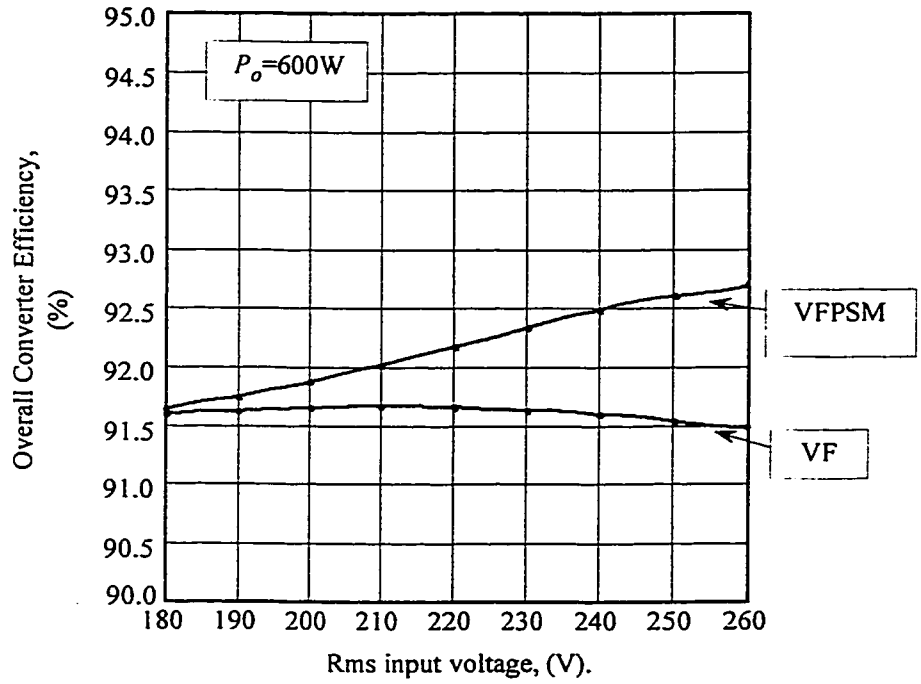


Fig. 3.20 Experimental results. Efficiency for operation with VF and VFPSM as a function of the input voltage.

Output power P_o=600 W. Converter parameters defined as in Section 3.7.1.

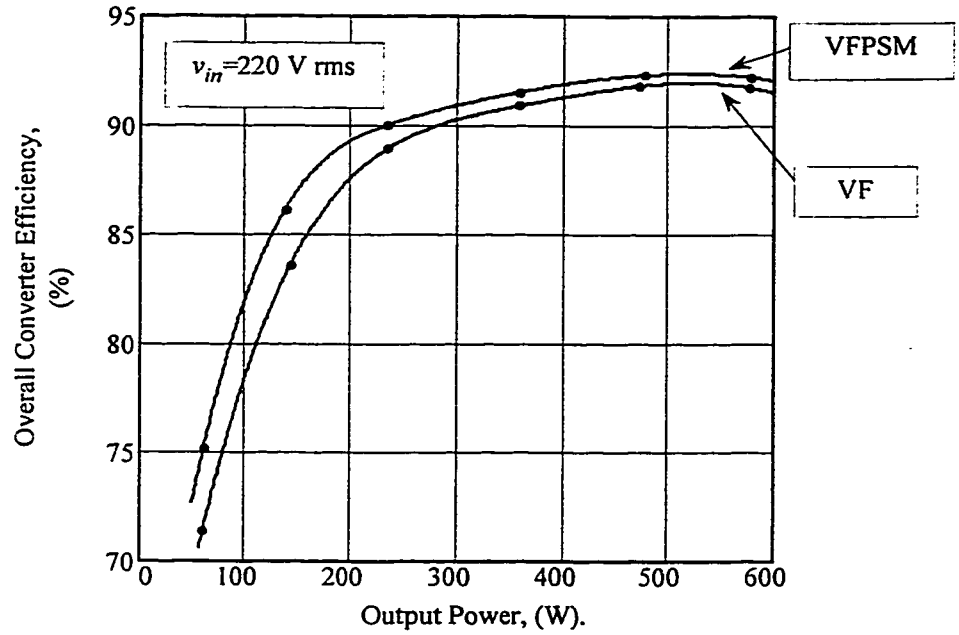


Fig. 3.21 Experimental results. Efficiency for operation with VF and VFPSM as a function of the output power.
Input voltage 220V rms. Converter parameters defined as in section 3.7.1.

In terms of input power factor, both VF and VFPSM result close unity input power factor when operating with active control of the input current. Fig. 3.22 shows a typical block diagram of an input current controller. The gain k of the compensator was selected to attenuate the gain near the resonance frequency of the input LC filter. Fig. 3.23 shows the input current and voltage waveforms when using active control of the input current. The power factor is close to one (0.999) and the THD of the input current is smaller than 5% for full load to 50% of full load.

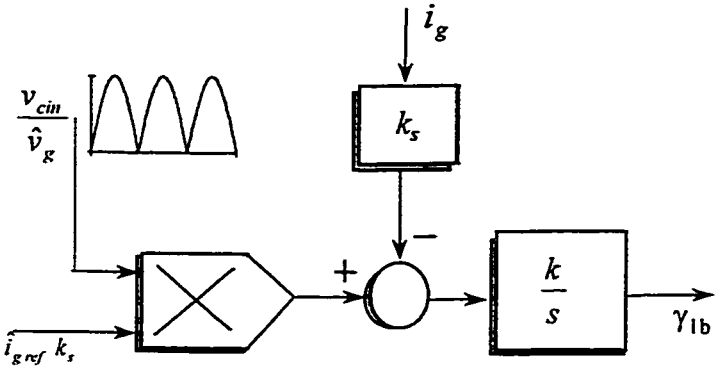


Fig. 3.22 Block diagram of the input current controller.
k_s is the current sensor gain, k is the controller gain and i_{gref} is the desired input current peak value.

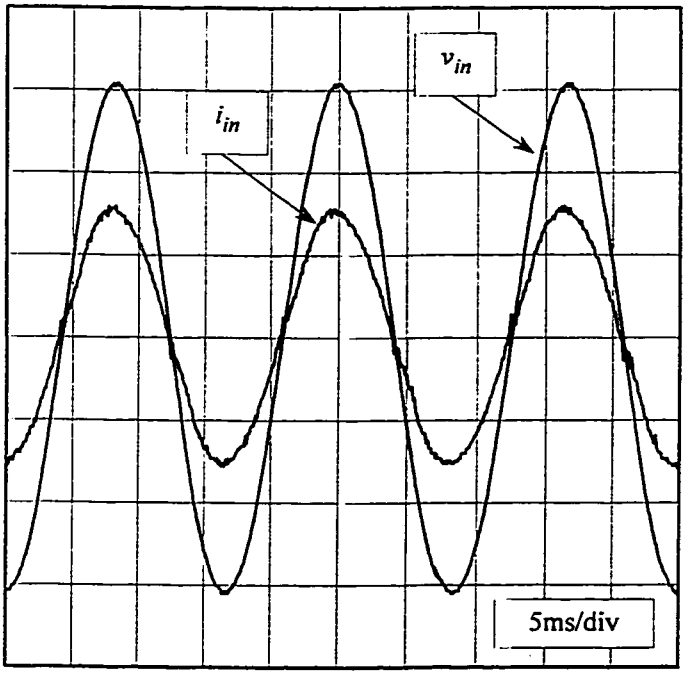


Fig. 3.23 Experimental results. Input current and voltage waveforms.
Operation with active control of the input current. P_o=550W, Input voltage 220V rms. Vertical scales: 100V/div and 2.5A/div. Horizontal scale: 5ms/div.

3.7.3 Proposed Clamped Control Action Approach

In this section, a clamped control action approach for resonant converters which decreases the amplitude of the low order harmonics of the input current, without the use

of active control of the input current. is presented. As a result. this control technique does not require multipliers nor the input current sensor. When operating without active control of the input current. the control angle is kept constant along the entire input line cycle. Therefore. the input current becomes distorted near the valleys of the input dc link voltage waveform due to the overboosting action of the resonant circuit in this region. For operation with unity power factor the control angle at full load and minimum input voltage should have the profile shown in Fig. 3.10. However. the implementation of this function is not practical since it requires the solution of (3.6) and (3.7). A good compromise between simplicity of the control circuitry and performance in terms of the THD of the input current can be achieved by approximating the profiles of Fig. 3.10. This can be done using a clamped sinusoidal waveform as indicated in Fig. 3.24 (b). In this way. the gain of the converter can be reduced in the valley of the input voltage and the THD of the input current becomes dependent on the constants k_1 and k_2 . Once the Q_s and the input voltage range are defined, these constants are selected so that the THD of the input current is minimized. According to Fig. 3.24 (b) the constant k_2 must be equal to 90° . However. the constant k_1 can not be easily found by inspection. Fig. 3.24 (c) shows how the THD of the input current changes as a function of the constant k_1 times the peak value of the lowest input voltage. v_{gm}. It is concluded that a good compromise in terms of the THD of the input current for the three input ac line voltages is found by selecting k_1 v_{gm} equal to 1.9 rad.

Fig. 3.25 shows the input current and voltage at full load for three input voltage values. It also shows the harmonic spectrum of the input current. Clearly. the amplitude of the low order harmonic components are very small with the nominal input voltage.

The upper value of the third harmonic component is 11% when operating with the lowest input voltage. Fig. 3.26 shows the input power factor as a function of the load for three input voltage values. At full load the power factor is greater than 0.99 and the THD of the input current is within the range from 6.7% to 11.8%. The amplitude of input current low frequency harmonics is well below the limits imposed by the IEC-1000-3-2 [3].

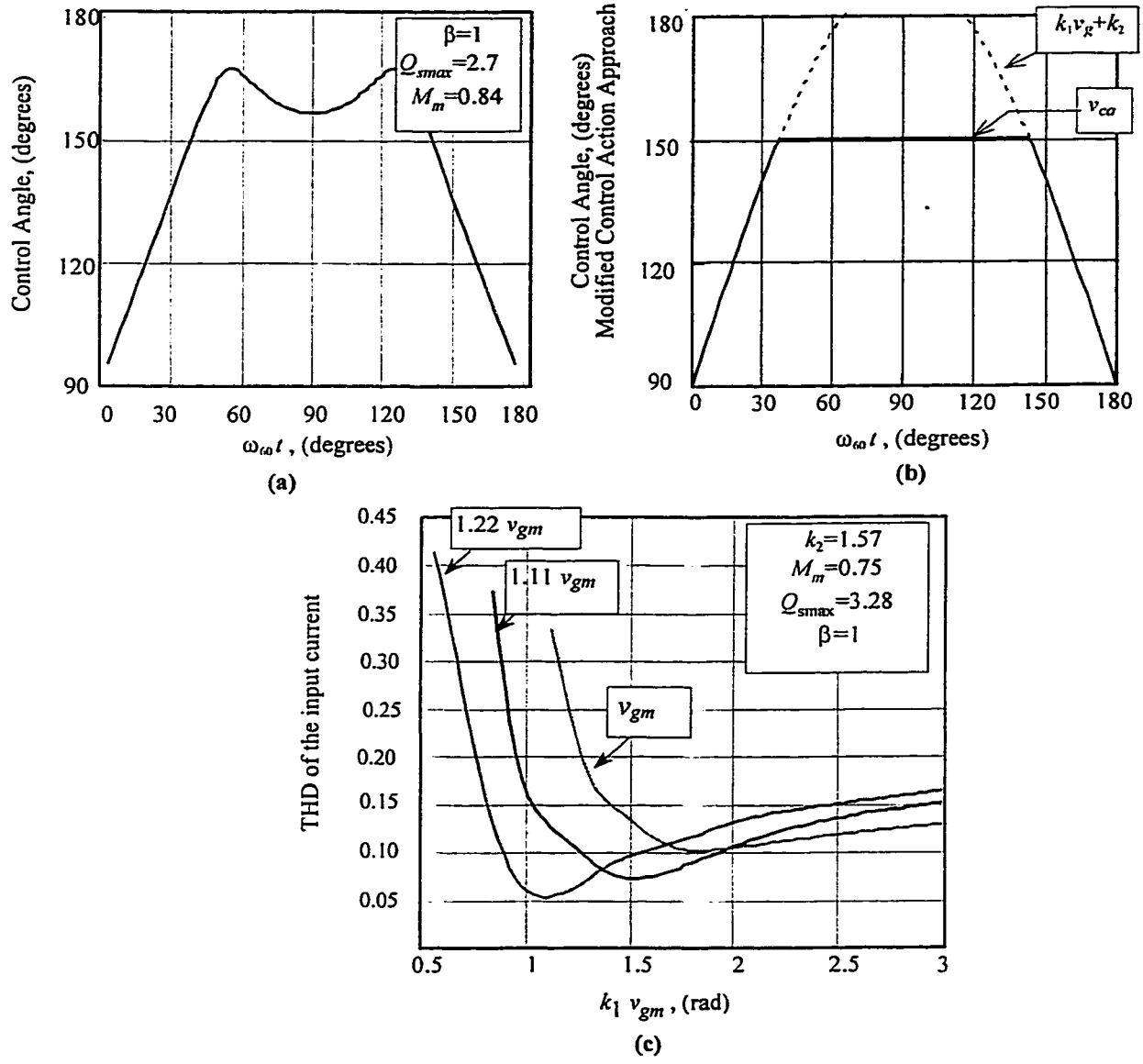


Fig. 3.24 Clamped control action approach.

(a) Control angle required to operate with unity power factor and constant output voltage along half cycle of the input source. **(b)** Control angle generated by the proposed clamped control action approach. **(c)**Total harmonic distortion of the input current as a function of the constant $k_1 v_{gm}$ for three values of the input voltage. Operation with VF at full load. Q_{smax}=3.28 and M_m=0.75.

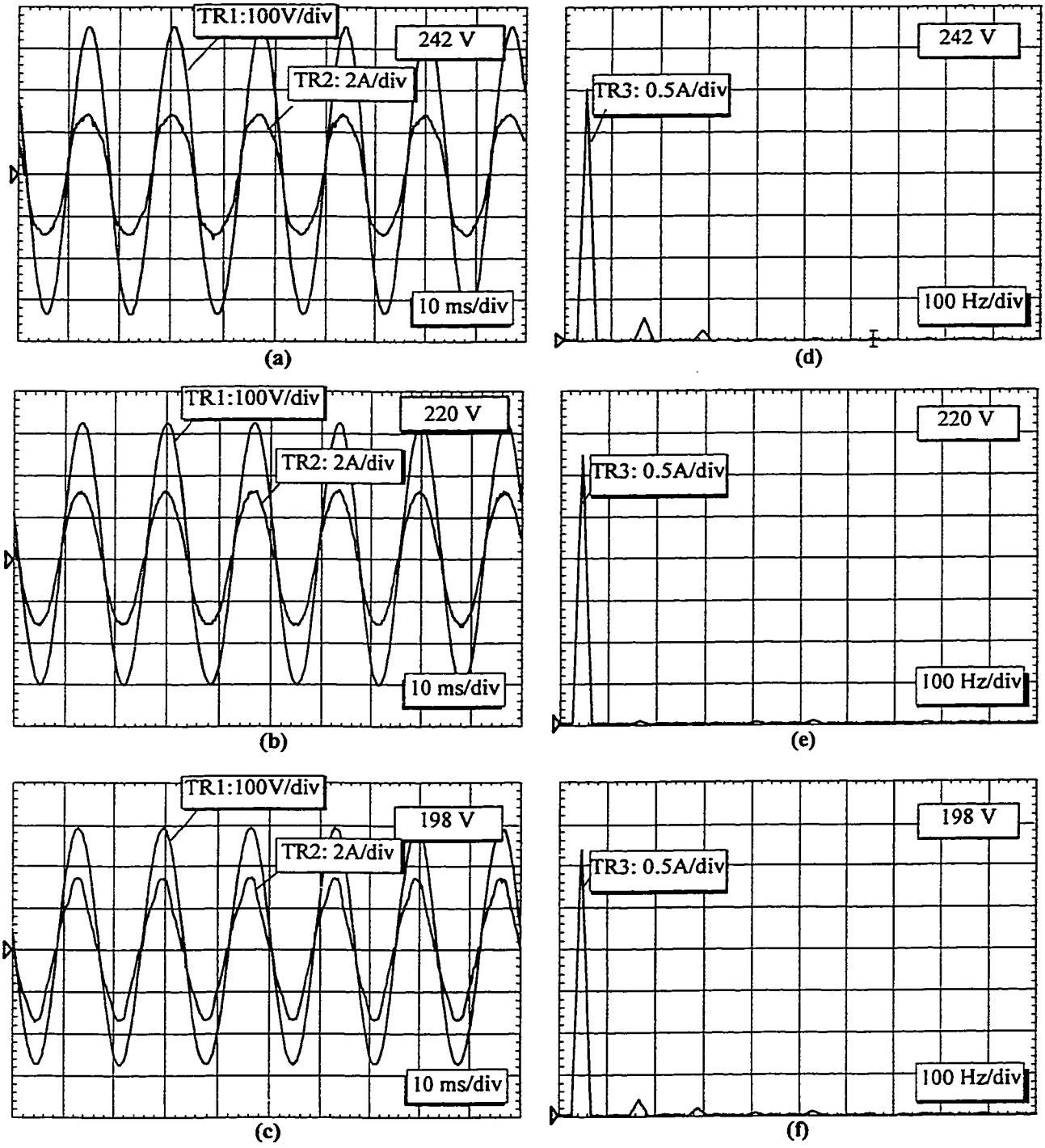


Fig. 3.25 Experimental results. Input current and voltage waveforms. Operation with the proposed clamped control action approach.

TR1: ac input voltage, 100 V/div. TR2: ac input current, 2 A/div, TR3: harmonic spectrum of the input current, 0.5A/div. Horizontal scales: 10ms/div, and 100Hz/div. **(a)** and **(d)** Operation with high input voltage. **(b)** and **(e)** operation with nominal input voltage. **(c)** and **(f)** operation with low input voltage. Output power 500 W. The gains of the modified control action controller are k_1=0.0067 rad/V and k_2 = 1.8 rad.

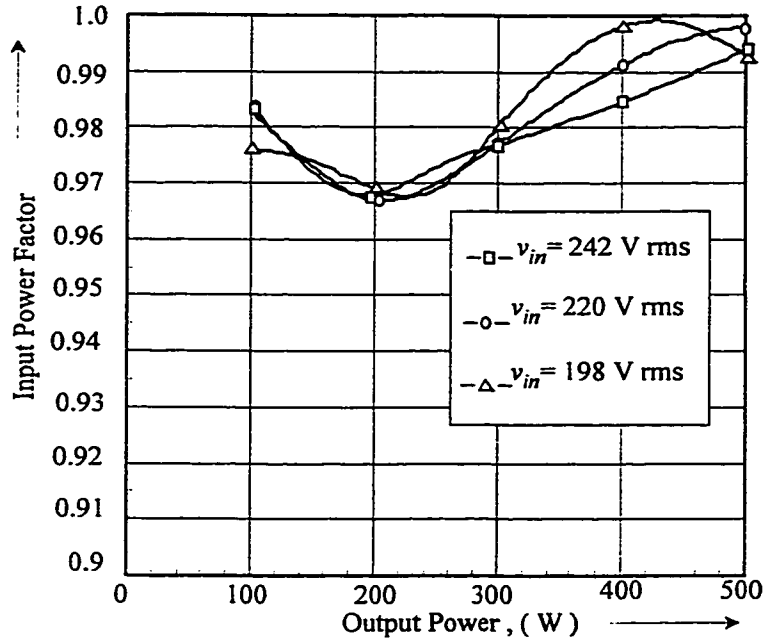


Fig. 3.26 Experimental results. Input power factor for operation with the clamped control action approach.

3.8 DISCUSSION AND CONCLUSIONS

This Chapter deals with ac-to-dc resonant converters operating with high input power factor in the self-sustained operating mode. Aiming to reduce the switching frequency range as well as components stresses in the power circuit components the concept of the variable frequency plus phase shift modulation is introduced. The range of the control angle for operation in self-sustained oscillation mode, where ZVS can be achieved, is identified and the main aspects required for operation with high input power factor and constant output voltage are addressed. For instance, the maximum voltage conversion ratio of the ac-to-dc converter as a function of the resonant circuit parameters are derived, and a procedure for the selection of the input capacitor, which allows operation with high input power factor and low THD of the input current, is presented. A

clamped control action approach which improves input power factor without the use of active control of the input current is proposed. Experimental results are given to confirm the concepts developed and to demonstrate the performance of the proposed ac-to-dc converter.

CHAPTER 4: UPS TOPOLOGY BASED ON SERIES-PARALLEL RESONANT CONVERTER

4.1 INTRODUCTION

Drawbacks of conventional UPS topologies include no galvanic isolation of the output from the incoming ac line or isolation using bulky low frequency transformer, high battery voltage, operation with hard-switching, and disturbances in the output voltage during the failure of the incoming ac line. This chapter explains the operating principle. and develops design procedures for single high frequency transformer UPS topologies based on resonant converters that overcomes the above mentioned disadvantages.

The concept of self-sustained oscillation developed in the previous chapters is applied to the proposed UPS. As a result, zero voltage switching for the converters connected at the line side and at the battery side under all operating conditions is ensured allowing in this way the operation at high switching frequency and the reduction of the size of the isolation transformer. In addition, the proposed UPS operates with high input power factor without a dedicated power factor correction stage, in a similar way as the ac-to-dc converter of Chapter 3.

In this chapter, the impact of the nature of the output dc bus filter, inductive or capacitive, on the overall performance UPS is investigated in detail. It is demonstrated

that with capacitive output dc bus filter the UPS has better performance during the backup mode than with inductive output dc bus filter. This is because, with capacitive output dc bus filter, the voltage across the high frequency transformer is clamped at the output voltage, which make it possible to select the high frequency transformer turns ratio that minimizes the current stresses in the circuit.

The outline of this chapter is as follows: The operating principle of the proposed UPS is explained in Section 4.2. A design procedure for the selection of the resonant circuit parameters when operating with inductive and capacitive output dc bus filter are developed and exemplified in Section 4.3 and Section 4.4 respectively. Experimental results that validate the concepts developed and demonstrate the performance of the proposed UPS are presented in Section 4.5. Finally, the main points of this chapter are summarized and conclusions are made in Section 4.6.

4.2 DESCRIPTION OF THE PROPOSED TOPOLOGY

The proposed UPS topology consists of three full bridge converters, one resonant circuit, one high frequency transformer, and input and output filters. The full bridge converters are named Line Side Converter (LSC), Battery Side Converter (BSC), and Output Side Converter (OSC) and they are located at the left, right, and top side of Fig. 4.1 respectively.

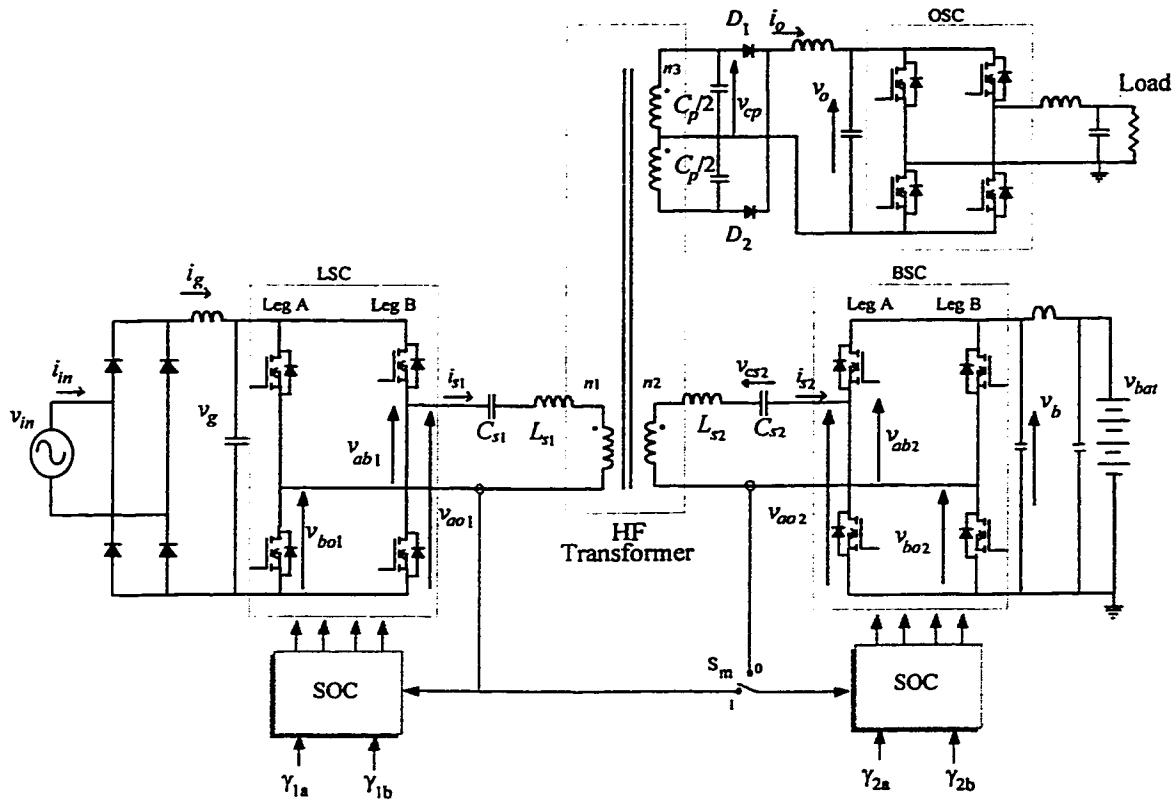


Fig. 4.1 Power circuit and simplified control block diagram of the proposed UPS.
SOC stands for self-sustained oscillating controller. s_m=1 in the line operating mode and s_m=0 during the backup mode.

The resonant circuit comprises of two series resonant branches (C_{s1}, L_{s1} and C_{s2}, L_{s2}) and a parallel resonant capacitor (C_p). The series resonant branches were introduced to allow the LSC and the BSC to be interfaced using a single high frequency isolation transformer. The parallel resonant capacitor reduces the voltage stresses in the output diode rectifier and provides the required gain to operate with constant output dc bus voltage and high input power factor. In addition, the parallel resonant capacitor provides a path for the resonant circuit current i_{s1} when operating with no load at the output. The high frequency transformer provides galvanic isolation between the input, output and battery, and a means to step-up the battery voltage to the level required to produce the output load voltage.

The proposed UPS has two modes of operation namely the line operation mode and the backup mode. These modes of operation depend on the voltage regulation of the incoming ac source. When the input voltage v_{in} is within the normal operating range the LSC transfers power from the input to the battery and to the output. A small dc input filter combined with the series-parallel resonant circuit (C_{s1}, L_{s1} and C_p) makes it possible to operate at a high input power factor and constant output dc bus voltage. The LSC operation is similar to the operation of the ac-to-dc converter described in Chapter 3. On the other hand, the BSC operates as a semi-controlled series resonant converter during the line operating mode. One leg of the BSC is kept inactive. In this way, the battery side converter becomes unidirectional in terms of the power transfer capability. Therefore, during the line operation mode the power transfer from the battery side to the resonant circuit is avoided. However, during the backup mode, the battery side converter operates as a full bridge series-parallel resonant converter sending power from the battery to the output stage. The output stage is comprised of a diode rectifier and a low pass filter followed by an inverter. The diode rectifier and the low pass filter convert the quasi-sinusoidal voltage at the output of the high frequency transformer into a stiff dc voltage bus. Finally, the output inverter converts the dc bus voltage into the desired ac output waveform.

The following sub-sections present a detailed description of the operation of the LSC and BSC during the line operation mode and backup mode.

4.2.1 Line Operating Mode

The line operation mode occurs whenever the incoming ac line is within its acceptable input voltage range. During this mode the input current i_{in} is waveshaped in a sinusoidal waveform in phase with the input voltage v_{in} using the LSC. The amplitude of the current i_{in}, for a given input voltage v_{in}, is defined from the required power to be transferred from the incoming ac source to the output load and battery. On the other hand, the BSC is used to control the battery charge current. The operation of the LSC and the BSC during this mode of operation is described in detail below.

4.2.1.1 Line Side Converter

The voltage applied by the LSC in the resonant circuit v_{ab1} can be represented by two components. The first one, is due to the voltage produced by leg A of the LSC and the second one is due to the voltage produced by leg B. These voltages (v_{a01} and v_{b01}) are generated so that the current i_{s1} always crosses zero inside the no zero voltage pulse of v_{ab1} as proposed in Chapter 3. In this way the current i_{s1} has the right polarity to charge and discharge the snubber capacitors of the LSC during the commutations of leg A and B. In order to ensure that the current crosses zero inside of the non zero voltage pulse of v_{ab1} the displacement angle between the current through the series resonant branch i_{s1} and the voltages v_{a01} and v_{b01} are controlled. This operation is illustrated in Fig. 4.2 where the control angles used to produce v_{a01} and v_{b01} are also indicated. The angle γ_{1a} is kept constant close to 180° and the angle γ_{1b} is used to vary the width of the quasi-square voltage pulse. For a given current i_{s1}, the power absorbed from the input source is increased by increasing the control angle γ_{1b}.

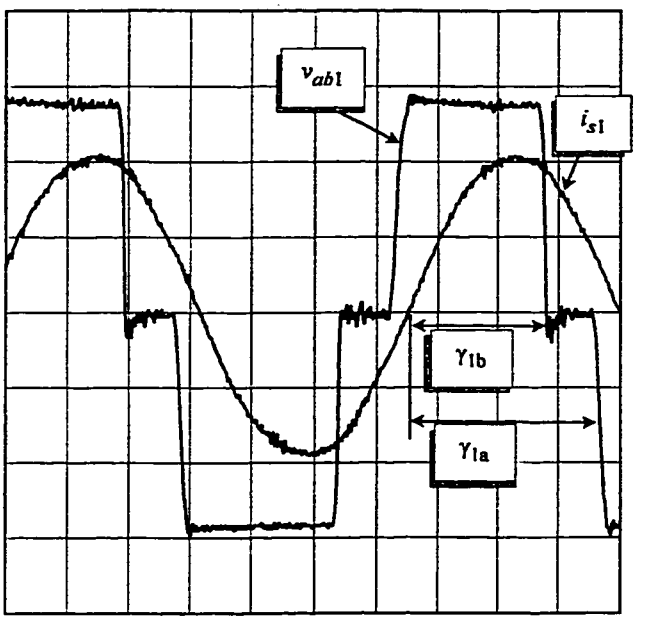


Fig. 4.2 The voltage v_{ab1}, the current i_{s1}, and the control angles.
Line Operation Mode

4.2.1.2 Battery Side Converter

The voltage impressed by the battery side converter on the resonant circuit can also be expressed in terms of two components, which in this case are v_{ao2} and v_{bo2}. The voltage v_{ao2} is produced by leg A of the battery side converter while the voltage v_{bo2} is produced by leg B. The transistors of leg B are kept off during the line operating mode. Therefore, the conduction state of the diodes of leg B defines the voltage v_{bo2}. For example, when the current i_{s2} is positive the diode at the bottom of the leg B conducts, and consequently the voltage v_{bo2} equals zero. Similarly, when current i_{s2} is negative the diode at the top of leg B conducts and as a result the voltage v_{bo2} equals v_b. Therefore, when the current i_{s2} is continuous the voltage v_{bo2} has a square waveform in phase with the current $-i_{s2}$. On the other hand, the voltage v_{ao2} is defined by the conduction state of the

transistors of leg A of the BSC. Leg A is used to control the current required for charging the battery. This operation is illustrated in Fig. 4.3.

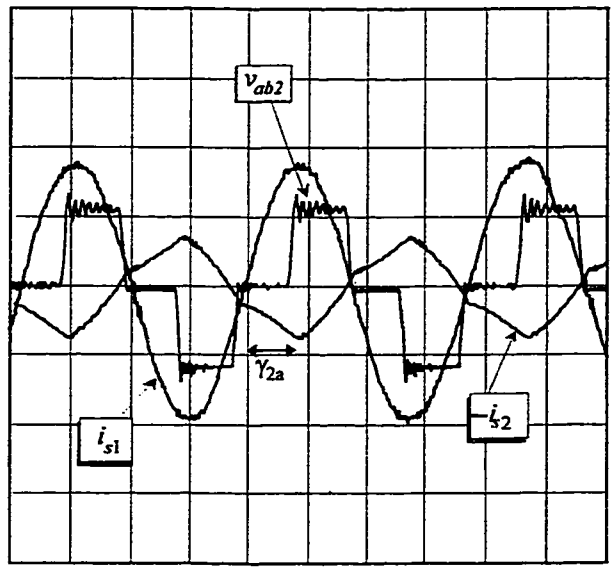


Fig. 4.3 Battery side converter voltage v_{ab2} and the current $-i_{s2}$.
Line Operation Mode.

As was mentioned earlier, the operation of the LSC is similar to the ac-to-dc converter described in Chapter 3. However, the BSC operation is quite different from the LSC since just one of the inverter's leg is active during the line operating mode. Aiming to understand the operation of the BSC during this mode, the BSC will be represented by an ac equivalent circuit, and using this circuit, the main characteristics of the BSC will be derived.

In order to simply the analysis of the battery side converter, the voltage across the parallel resonant capacitor is considered to be known and the resonant branch at the battery side (L_{s2}, C_{s2}) is assumed to be in sinusoidal steady state. Therefore, when the current i_{s2} is continuous the battery side converter can be represented as shown in Fig. 4.4.

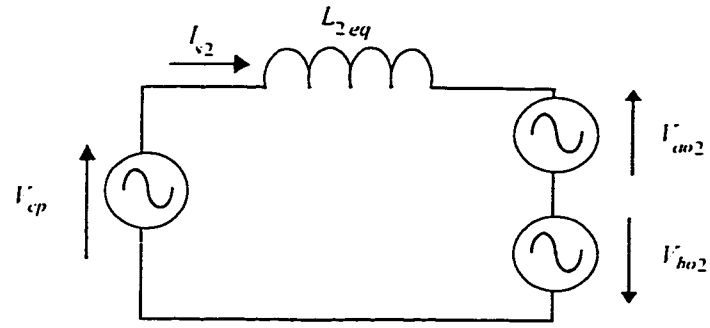


Fig. 4.4 Equivalent circuit of the BSC operating as a semi-controlled resonant converter.

Line Operation Mode

The voltages and current in capital letters in Fig. 4.4 are complex quantities associated with the first harmonic component of the variables that they represent. The equivalent inductance at the battery side is found to be:

$$L_{eq2} = \frac{\alpha^2 - 1}{\alpha^2} L_{s2} \tag{4.1}$$

where α is the switching frequency ratio, $\alpha = \omega_s / \omega_o$.

The displacement angle between the voltage V_{bn2} and the current I_2 is 180°. This is due to the operation of the uncontrolled leg of the battery side converter. By solving the circuit of Fig. 4.4 it is possible to obtain the main quantities of the BSC. Fig. 4.5 shows the power absorbed by the BSC when V_{cp} is constant. The power was derived by solving the circuit of Fig. 4.4 for different angles between the voltage V_{cp} and the voltage V_{am2}. For a given voltage V_{cp} the power sent to the battery can be made equal to the desired one by the appropriate selection of the displacement angle between v_{cp} and v_{am2}.

In order to achieve ZVS, in the active leg, the current I_2 must lead V_{am2}. The phase angle between these two variables is shown in Fig. 4.6. Zero voltage switching can be achieved in the battery side converter during the line operation mode in a well-defined

range of angle between V_{cp} and V_{ao2}. When the displacement angle between v_{cp} and v_{ao2} drops below 45°, the current i_{s2} becomes small and it usually has multiple zero crossings. Even in this case the current i_{s2} has the favorable polarity to reset the snubber capacitors at the commutation of leg A. On the other hand, leg B commutates under the zero of the current i_{s2}.

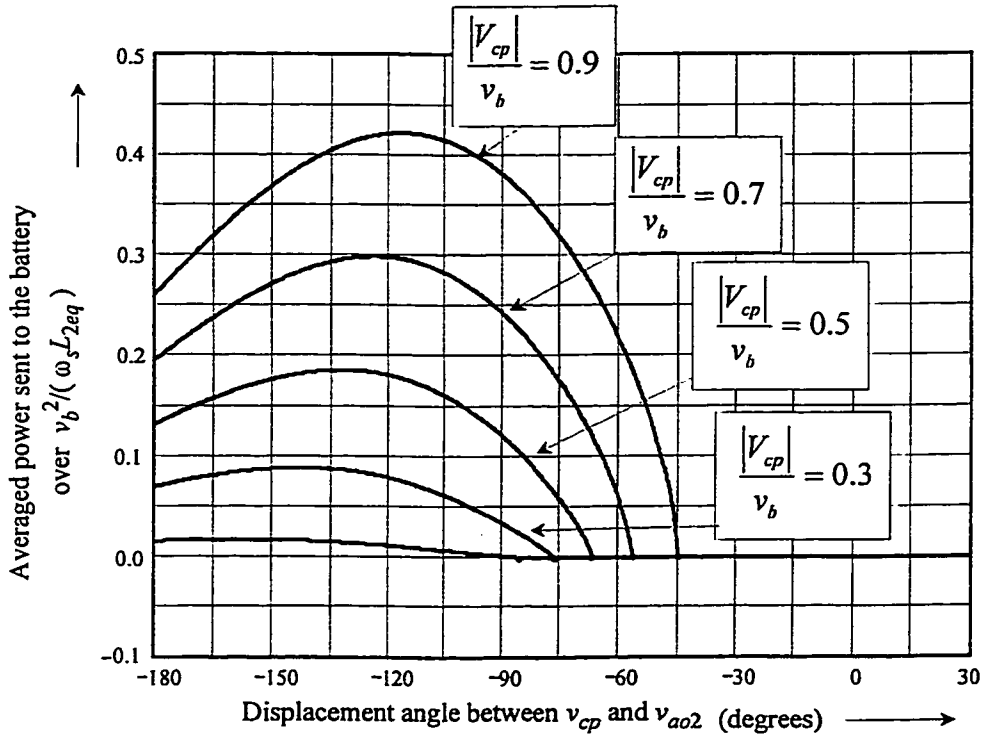


Fig. 4.5 Power sent to the battery.
Line Operation Mode

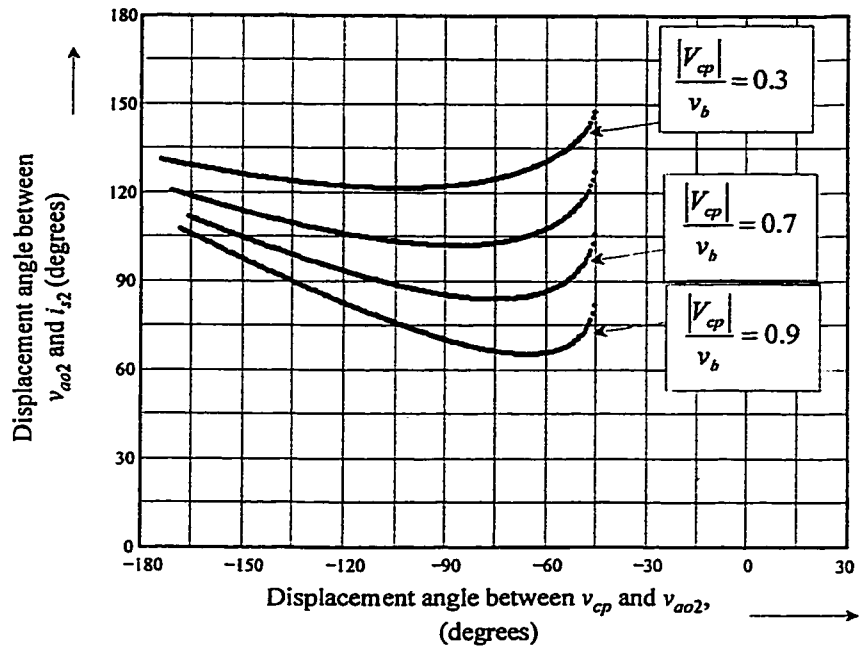


Fig. 4.6 Displacement angle between the voltage v_{ao2} and the current i_{s2}.
Line Operation Mode

On the other hand, in order to make the battery current equal to zero, for example when operating with float charging, the peak value of the voltage across the terminals of high frequency transformer must be smaller than the battery voltage. Furthermore, the ratio v_o/v_b should be kept as high as possible to reduce the amplitude of the current i_{s2} during the backup mode. Section 4.3 and Section 4.4 address the issue of selecting the transformer turns ratio and the resonant circuit parameters so that operation with zero battery current and reduced current stresses in the circuit are achieved.

4.2.2 Backup Mode

During the backup operating mode, both legs of the battery side converter are active. In this mode, the operation of the battery side converter is similar to that of the

line side converter during the line operating mode, except the input voltage v_b is constant. The angle γ_{2a} is kept constant to ensure that the current i_{s2} crosses zero inside the non zero output voltage pulse of v_{ab2}. On the other hand, the angle γ_{2b} is used to adjust the pulse width of the non-zero voltage pulse at the ac terminals of the BSC. Consequently, the battery side converter operates with a combination of variable frequency and phase shift modulation, where the angle γ_{2b} is adjusted to provide the required power transfer from the battery to the output stage.

4.3 OPERATION WITH INDUCTIVE OUTPUT FILTER

This section addresses the design of the proposed UPS when operating with an inductive output dc bus filter. At the beginning of this section, the key design issues to be considered to ensure the proper operation of the UPS during the line operating mode and during the backup mode are pointed out. Then a design procedure for the selection of the parameters of the resonant circuit as well as the turns ratio of the transformer of the UPS of Fig. 4.1 is developed and exemplified.

4.3.1 Line Operating Mode

As mentioned earlier, the operation of the LSC of the UPS topology of Fig. 4.1 is similar to the operation of the ac-to-dc converter described in Chapter 3. However, the main difference between them is the BSC in the UPS topology. In the previous section, the BSC was analyzed considering that the voltage across the parallel resonant capacitor was a known quantity. In this section, this voltage will be investigated in detail since it

plays an important role in the design of the BSC. Particularly, the peak value of the voltage across the parallel resonant capacitor (v_{cp}) is required for the selection of the transformer turns ratio. This is because the battery voltage must be larger than the peak value of v_{cp} (referred to the BSC side) to allow the operation with zero battery charge current.

The voltage across the parallel resonant capacitor can assume two kinds of waveforms depending on whether it has a zero voltage interval within the switching period or not. This characterizes two modes of operation, which are named continuous capacitor voltage mode, CCVM, and discontinuous capacitor voltage mode, DCVM.

The CCVM occurs whenever the amplitude of the current i_{s1} is greater than the output dc bus filter current, i_o, plus the current i_{s2} at the instant that voltage across the parallel resonant capacitor crosses zero. This becomes clear by applying Kirchhoff's current law to the node where the parallel resonant capacitor is connected. If the current i_{s1} is greater than i_o plus i_{s2}, at the instant that the voltage v_{cp} crosses zero, part of the current i_{s1} will flow through the parallel resonant capacitor. This ensures a continuous variation of the voltage v_{cp} when it is crossing zero. In this case, the output rectifier operates as conventional uncontrolled diode rectifier driven by a voltage source, that is, when the voltage v_{cp} is positive the diode D_1 is forward biased (D_2 is reversed biased) and it conducts the current that flows through the inductor of the output dc bus filter. When v_{cp} is negative, the diode D_2 is forward biased and the diode D_1 is reversed biased. Typical waveforms for operation in CCVM are given in Fig. 4.7.

On the other hand, the DCVM occurs whenever the amplitude of the current i_{s1} is smaller than i_o plus i_{s2} at the instant that the voltage v_{cp} crosses zero. In this case, the diodes of the output rectifier conduct simultaneously clamping the voltage v_{cp} at zero. This zero voltage interval lasts up to the instant when the current i_{s1} overcomes the sum of i_o and i_{s2}. At this instant, part of i_{s1} starts to circulate through the parallel resonant capacitor causing the voltage across it to increase (or to decrease), and consequently blocking one of the diodes of the output rectifier. Typical waveforms of the converter during this mode of operation are given in Fig. 4.8.

The describing function method can be used to accurately describe the operation of the output diode rectifier when the converter is in CCVM. However, when operating in DCVM the complexity of this method increases considerably, because the nonlinearity associated with the output rectifier depends on the voltages v_{cp}, and on the currents i_o, i_{s1}, and i_{s2}. Alternatively, the operation in DCVM can be accurately described by the discrete time generalized state-space modeling approach of static converters proposed in [73]. In order to simplify the analysis of the converter the current i_{s2} will be assumed to be zero. This assumption is supported by the fact that the purpose of investigating the operation in DCVM is to ensure that it is possible to make the battery current equal to zero, and in this operating condition, $i_b = 0$, and the current i_{s2} is very small compared with i_{s1}.

The first step towards the derivation of the discrete time model of a static converter is the identification of the cyclic operating modes of the converter. The second step is the derivation of the equations that describe the evolution of the states of the

converter from the beginning to the end of the switching cycle for all operating modes of interest. Then, in the third step, the boundaries between the different operating modes, in the circuit parameter space (say γ_{1b}, Q_{s1}, β_1) are identified. Finally, the quantity of interest, in this case the peak value of the voltage across the parallel resonant capacitor, is obtained for different values of the circuit parameters. This procedure is carried out in detail in Appendix 2. Fig. 4.9 summarizes the peak value of the voltage across the parallel resonant capacitor as a function of γ_{1b} for different values of Q_{s1}. The peak value of the voltage across the parallel resonant capacitor for other values of β_1 are found in the Appendix 2. It is seen from these figures that for a given output voltage, the peak value of the voltage v_{cp}, increases with Q_{s1} and β_1. This is because for small values Q_{s1} and β_1 the converter runs in CCVM and the voltage v_{cp} has a predominant first harmonic component. As the factors Q_{s1} and β_1 increase, the converter runs in DCVM increasing the peak of v_{cp}. The peak of v_{cp} (Fig. 4.9) is used to ensure that the battery voltage is greater the peak voltage across the parallel resonant capacitor, therefore, allowing the battery current to be equal to zero.

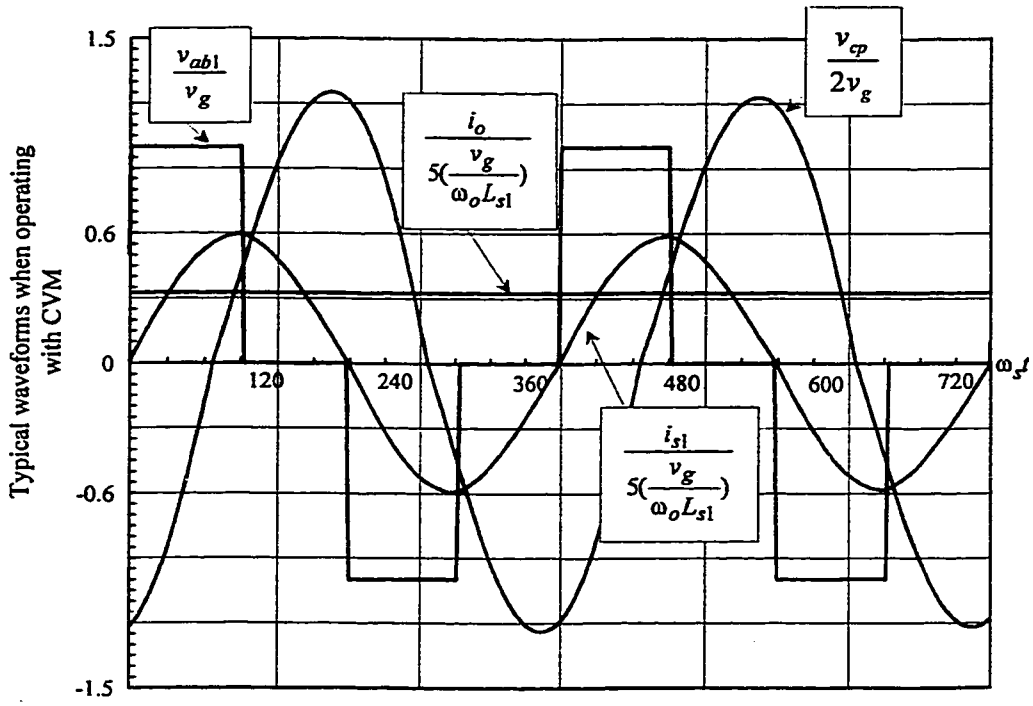


Fig. 4.7 Operation with inductive output filter and continuous capacitor voltage mode.

Simulation results. $\gamma_{1a}=180^o$, $\gamma_{1b}=91.7^o$, $i_b=0$, $Q_{s1}=0.41$,$\alpha=1.64$,$\beta_1=1.5$.

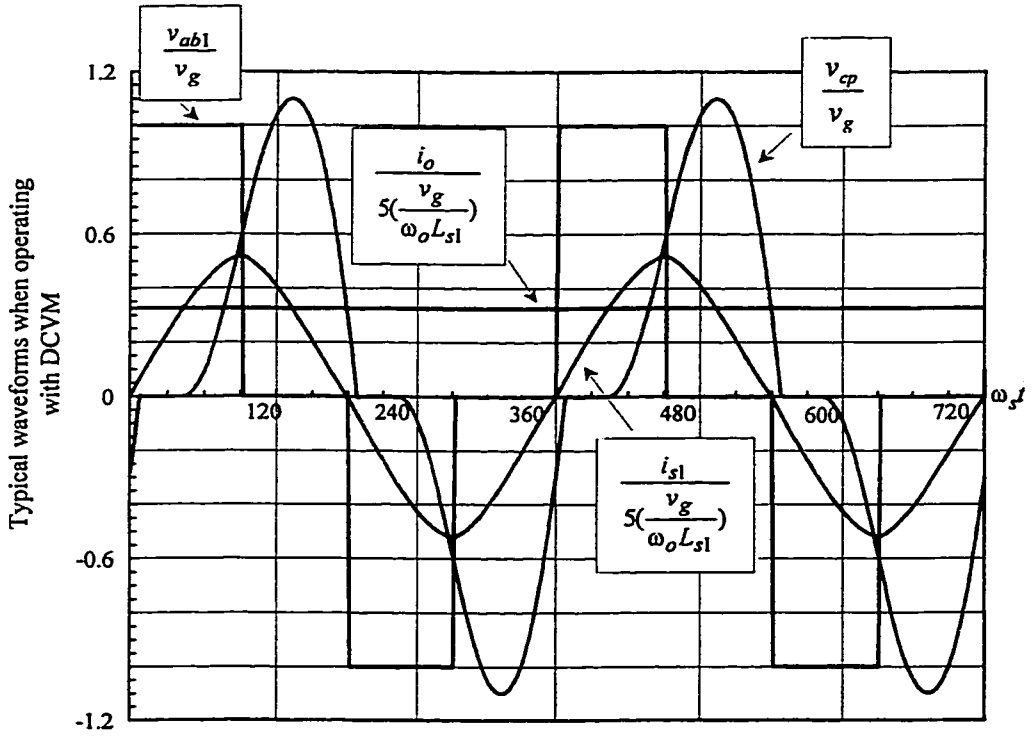


Fig. 4.8 Operation with inductive output filter and discontinuous capacitor voltage mode.

Simulation results. $\gamma_{1a}=180^o$, $\gamma_{1b}=91.7^o$, $i_b=0$, $Q_{s1}=3.26$,$\alpha=1.27$,$\beta_1=1.5$.

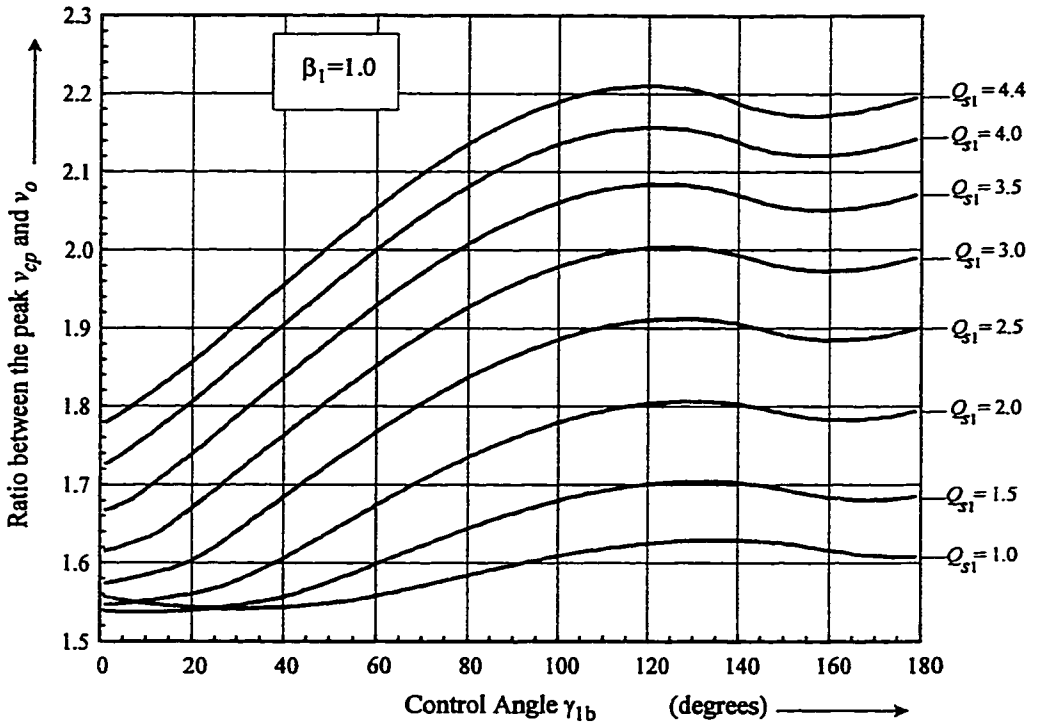


Fig. 4.9 Ratio between the peak value of v_{cp} and the average value of v_o for operation with VFPSM.
($\gamma_{1a}=180^o$, $\beta_1=1.0$)

4.3.2 Backup Mode

During the backup mode the BSC transfers power from the battery to the output stage operating as a dc-to-dc converter, where its input voltage is the battery voltage, v_b, and its output is the output dc bus voltage, v_o.

The BSC can operate with either VF, as described in Chapter 2, or with VFPSM. However, the latter is preferable since it results in smaller switching frequency range when variations in the load are considered. Another important point regarding the operation of the BSC during the backup mode is associated with the Q_{s2} factor. During the backup mode Q_{s2} is constant for a given output load and it can be expressed as:

$$Q_{s2} = \frac{\omega_o L_{s2}}{\frac{v_o^2}{p_o}} \tag{4.2}$$

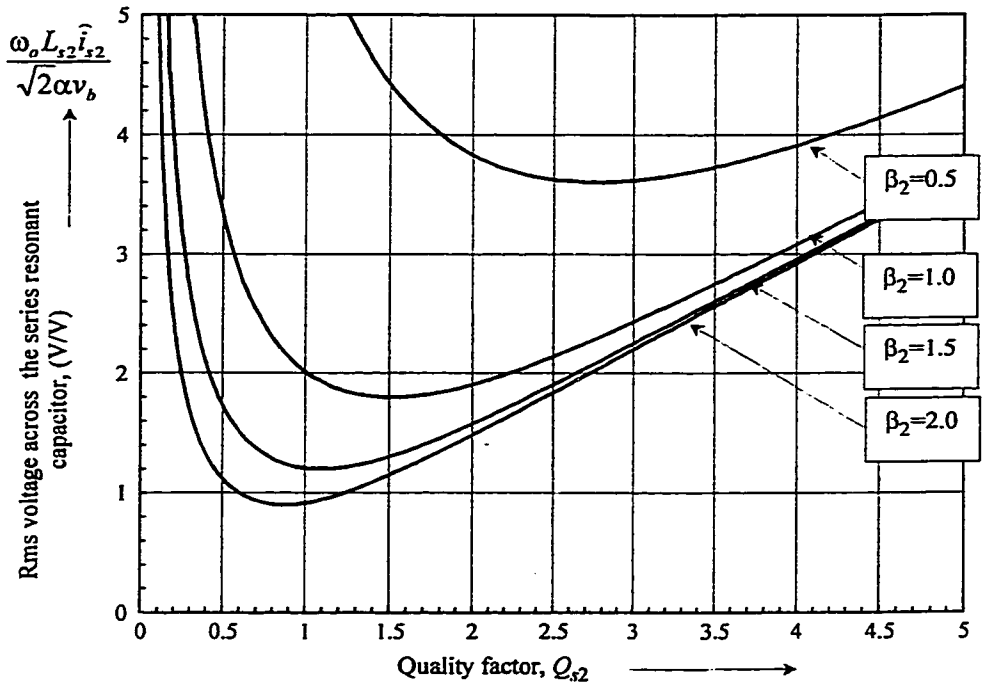
where p_o is constant for a given output load. It is seen from (4.2), that the selection of Q_{s2} factor has a direct impact on the parameters of the BSC (L_{s2} and C_{s2}) since v_o and p_o are well defined quantities and the natural frequency of the series resonant branch at the BSC is equal to the one of the series resonant branch at the LSC. In order to guide the selection of the parameters of the BSC the stresses in the resonant circuit, in terms of the volt-amperes in the series resonant inductor and the voltage across the series resonant capacitor, C_{s2}, are plotted in Fig. 4.10. It is possible to see that both P_{ls}/p_h and v_{sc}/v_h reduce by the increasing the ratio between the series and the parallel resonant capacitors, β_2. However, the switching frequency range increases with the ratio β_2. In order to exemplify this fact, the variation of the switching frequency from full load to 10% of full load are given in Table 4.1.

TABLE 4.1 VARIATION OF THE SWITCHING FREQUENCY WITH THE LOAD.

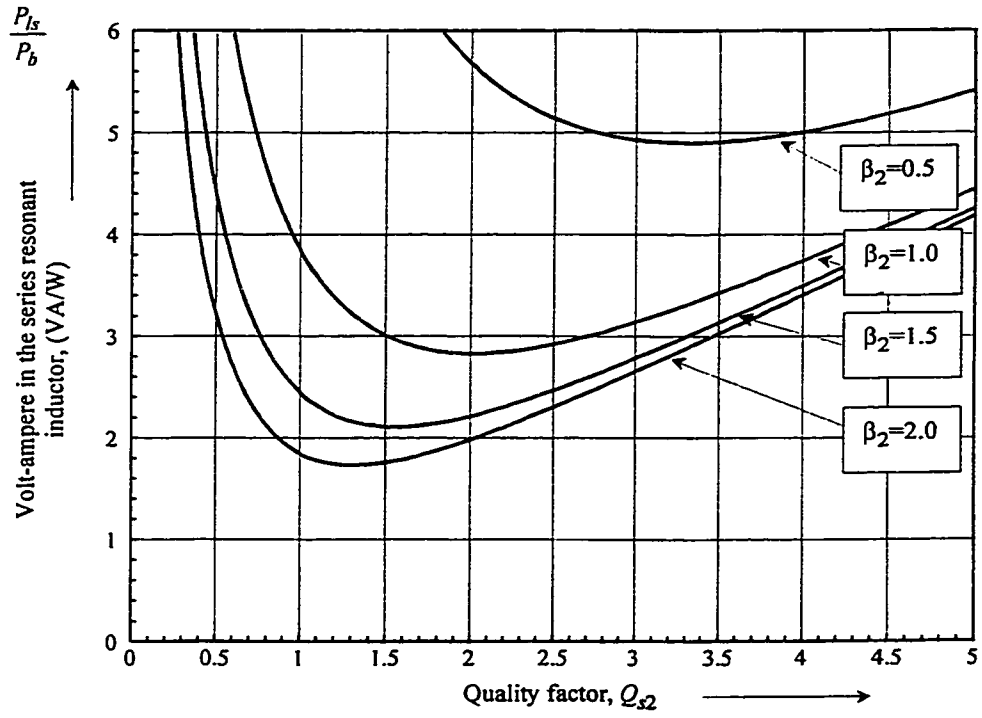
	Ratio between the series and the parallel resonant capacitor.β_2				
	0.5	1.0	1.5	2.0	3.0
$\frac{\alpha\|_{Q_{s2}=0.2} - \alpha\|_{Q_{s2}=2}}{\alpha\|_{Q_{s2}=2}} 100$	8.0 %	28.8 %	51.9%	73.3%	110.1%

At full load Q_{s2}=2.

By using the information presented in this and in the previous section, a design procedure for the selection of the parameters of the UPS will be developed and exemplified in the next sub-sections.



(a)



(b)

Fig. 4.10 Stresses in the battery side converter during the backup Mode Operation with inductive output filter.

(a) Ratio between the voltage across the series resonant capacitor, C_{s2}, and the BSC input voltage, v_b.
(b)Ratio between the volt-amperes in the series resonant inductor L_{s2} and BSC input power, p_b.
$\gamma_{2a}=\gamma_{2b}=180^o$.

4.3.3 Design Procedure

This sub-section describes a procedure for selection of the parameters of the resonant circuit of the UPS topology of Fig. 4.1, when operating with inductive output dc bus filter.

The three main aspects of the operation of the proposed UPS that should be considered when selecting the parameters of the resonant circuit and the transformer turns ratio are:

(i) During the line operating mode, the LSC should have enough gain to allow operation with unity input power factor and constant output dc bus voltage.

(ii) During the line operating mode, it should be possible to change the battery current from zero to its maximum average value.

(iii) During the backup mode, the output voltage should be kept constant and the stress in the resonant circuit should be minimized.

If the first aspect is satisfied with the lowest voltage within the acceptable incoming input voltage range, then it will also be satisfied for the other voltages of the acceptable input voltage range. This is because for input voltages higher than the lowest acceptable voltage, the gain required for operation with unity input power factor and constant output voltage is smaller.

On the other hand, regarding the second aspect, a necessary condition to make the battery current equal zero is to have the battery voltage greater than the peak value of the voltage v_{cp} (reflected to the BSC side), since the BSC operates as a series resonant boost converter during the line operating mode.

Finally, the third aspect, to minimize the stresses during the backup mode, can be met by the proper selection of the parameters of the BSC. In addition, when operating with the battery end voltage the BSC should operate with its maximum voltage gain, since in this way the current stresses in the circuit are also minimized.

Before describing the steps for the selection of the parameters of the UPS it is assumed that the transformer turns ratio is 1:1:1, and that the following quantities are known:

(i) Power absorbed from the incoming ac line: $p_{in}=P_{in}\sin^2(\omega_{60}t)$

(ii) Lowest incoming ac voltage: $v_g = \hat{v}_{gm}\sin(\omega_{60}t)$

(iii) Maximum battery charging power: P_{bav}

Once the above quantities are defined, the possible sets of parameters of the UPS can be found from the following steps:

(i) Choose a value of Q_{s1} and β_1 and find the maximum output voltage that the converter operates with unity input power factor and constant output voltage. Aiming to simplify this step, the total power of the UPS can be lumped in the main output of the UPS. In this way the design curves given in Chapter 3, Fig. 3.8 and Fig. 3.9, can be used for the selection of the parameters of the LSC (L_{s1}, C_{s1}, C'_p and the output voltage v_o).

(ii) Find the peak value of the voltage across the parallel resonant capacitor when the battery charge current is zero. It have been found both experimentally and analytically that, within the range of interest of the parameters of the resonant circuit ($1> Q_{s1\_max}> 4$ and $0.5 >\beta_1>2$), the peak value of the voltage across the

parallel resonant capacitor occurs at the peak of the incoming ac line ($\omega_{60}t$=90°). In this way, the maximum peak value of v_{cp} can be found from the curves given in Fig. 4.9, where γ_{1b} at $\omega_{60}t$=90° for different values of input voltage can be obtained from the solution of (3.6) and (3.7) using a Q_{s1} factor that is given by

$$Q_{s1} = Q_{s1\_max} \frac{P_{in}/2 - P_{bat}}{P_{in}/2}. \tag{4.3}$$

Equation (4.3) is valid for operation at full output power and no battery charge current.

(iii) Select the battery voltage. The battery floating voltage must be higher than the peak value of v_{cp}, which was found in the previous step.

(iv) Plot Q_{s2} as a function of β_2 in a graph that also indicates the pairs (Q_{s2} , β_2) that minimize the stresses in the BSC. Then, find the maximum gain of the BSC (Fig. 3.6).

(v) Repeat steps (i) to (iv) for other values of Q_{s1} and β_1.

(vi) Select a set of parameters and simulate the UPS to verify the following operating conditions:

(a) Operation at full load and full battery power

(b) Operation at minimum output load and full battery power.

The solution of the ac equivalent circuit of the converter, Appendix 3, can be used to verify these operating conditions since it results in much smaller computation effort than the simulation of the entire converter with its associated control circuit.

Aiming to illustrate in detail each step of the above-described design procedure, next section exemplifies the design of an UPS.

4.3.4 Design Example

Let us consider an UPS with the following characteristics:

- Output Power: 500 W.
- Acceptable input voltage range: 120 V rms +/- 15%.
- Maximum battery charging power: 100 W.
- Minimum switching frequency: 100 kHz.

By following the design procedure presented in the last section results.

(i) For $Q_{s1\max}$=1.5 and β_1=0.5 it is found from Fig. 3.8 that the maximum voltage conversion ratio is M_m=1.76. Therefore the output dc voltage is given by:

$$v_o = \hat{v}_{gm} M_m = 253.2 \text{ V} \tag{4.4}$$

Then, by using the given minimum switching frequency and the switching frequency ratio obtained from Fig. 3.9 the resonant frequency ω_o can be found as:

$$\omega_o = \frac{\min(\omega_s)}{\alpha} = 531.1 \text{ krad/s} \tag{4.5}$$

and the values of L_{s1}, C_{s1} and C_p as:

$$L_{s1} = \frac{Q_{s\max} \dfrac{M_m^2 v_{gm}^2}{P_{in\max}}}{\omega_o} = 150.8\,\mu\text{H} \tag{4.6}$$

$$C_{s1} = \frac{1}{\omega_o^2 L_{s1}} = 23.5\text{nF} \text{ and } C_p = \frac{C_{s1}}{\beta_1} = 47.0 \text{ nF}. \tag{4.7}$$

(ii) In order to find the peak value of, v_{cp}, the angle γ_{1b} at $\omega_{60}t$=90° for the voltages within the acceptable input voltage range has to be obtained. This can be carried out by solving (3.6) and (3.7) for γ_{1b} and α. The Q_s factor, which is required to

solve (3.6) and (3.7), is found to be $Q_{s1} = 1.25$ from (4.3), and the voltage conversion ratio varies in the range M_m to $0.74M_m$, where the factor 0.74 accounts for the possible variations of the input voltage. The angle γ_{1b} and the associated peak value of v_{cp} are plotted in Fig. 4.11.

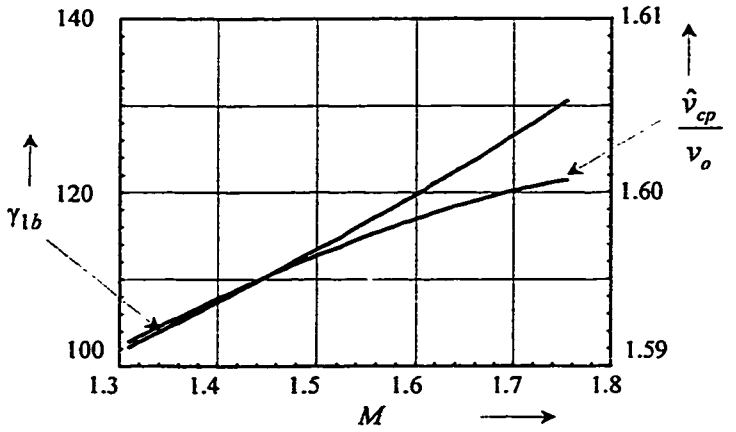


Fig. 4.11 Control angle and the peak value of v_{cp} at $\omega_{60}t$=90°.

It is possible to see from Fig. 4.11 that the maximum peak value of v_{cp} occurs at the lowest input voltage (maximum value of M) and it is about 1.6 v_o.

(iii) The battery floating voltage is selected as

$$v_{b\_f} = 1.6v_o = 405.2\,\text{V} \tag{4.8}$$

(iv) Once the parallel resonant capacitor and the output voltage are defined the factor Q_{s2} and the ratio β_2 are found to be related by:

$$Q_{s2} = \frac{P_o}{\omega_o C_p v_o^2}\frac{1}{\beta_2} = 0.312\frac{1}{\beta_2} \tag{4.9}$$

The equation (4.9) is plotted in Fig. 4.12 for $0.5 < \beta_2 < 2.0$. A region defined by the points around (+/-10%) the minimum volt-amperes in the resonant inductor L_{s2} is also indicated in Fig. 4.12. It is possible to see that for these values of Q_{s1} and β_1

the stresses in the resonant circuit are high since Q_{s2} is far from the minimum of P_{ls}.

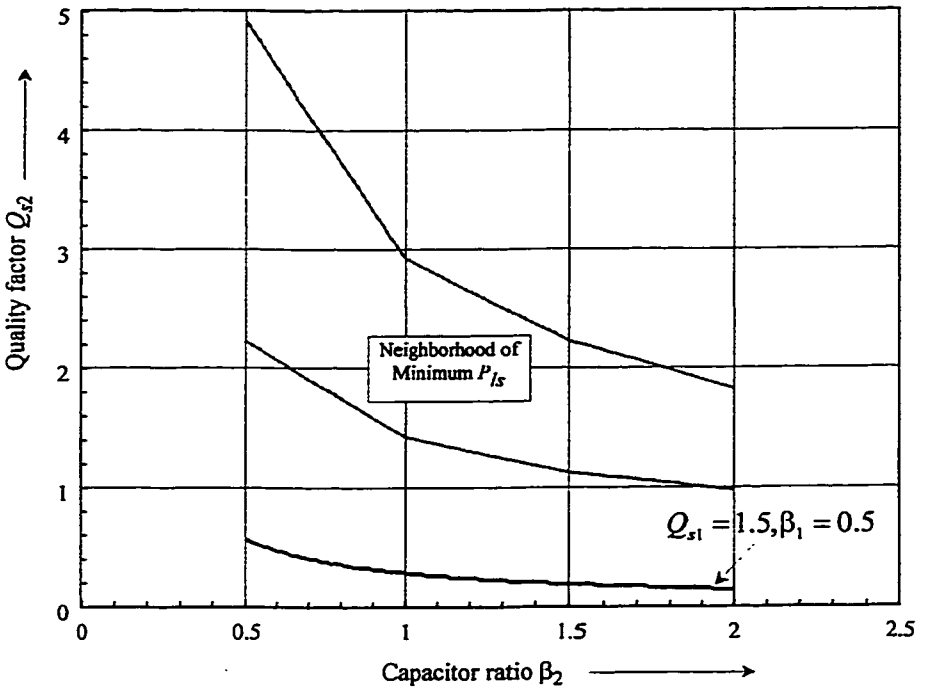


Fig. 4.12 Quality factor Q_{s2} as a function the ratio β_2

(v) By repeating steps (i) to (iv), the Q_{s2} factor as a function of β_2 can be obtained for other typical values of Q_{s1} and β_1, as shown in Fig. 4.13 to Fig. 4.16. Table 4.2 summarizes the main parameters of the UPS for the pairs (Q_{s2}, β_2) within the defined neighborhood of P_{ls} minimum.

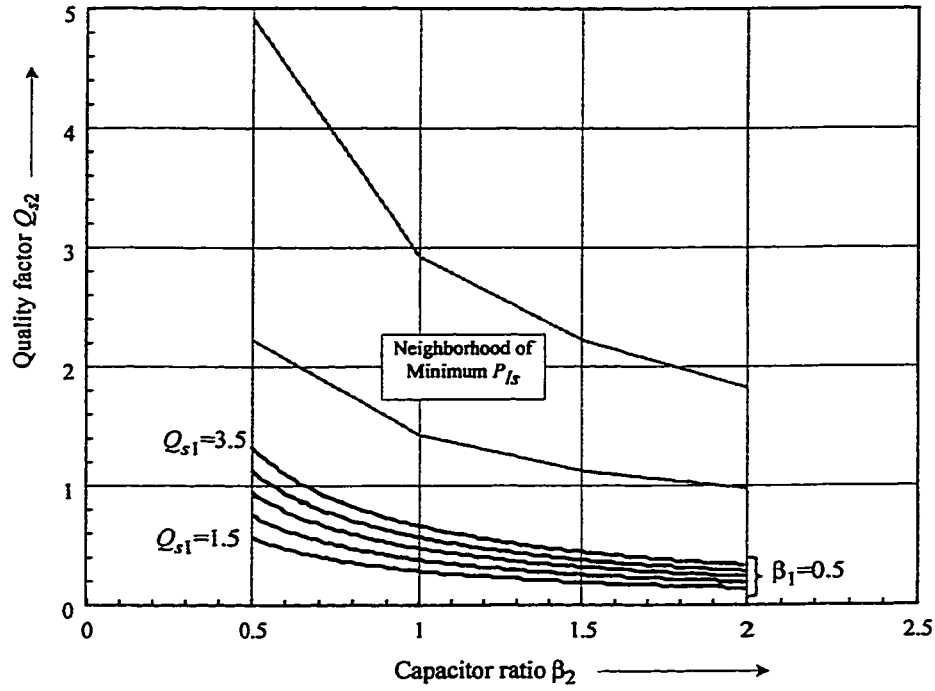


Fig. 4.13 Quality factor Q_{s2} as a function the ratio β_2 for β_1=0.5.
Q_{s1}=[1.5, 2.0, 2.5, 3.0, 3.5].

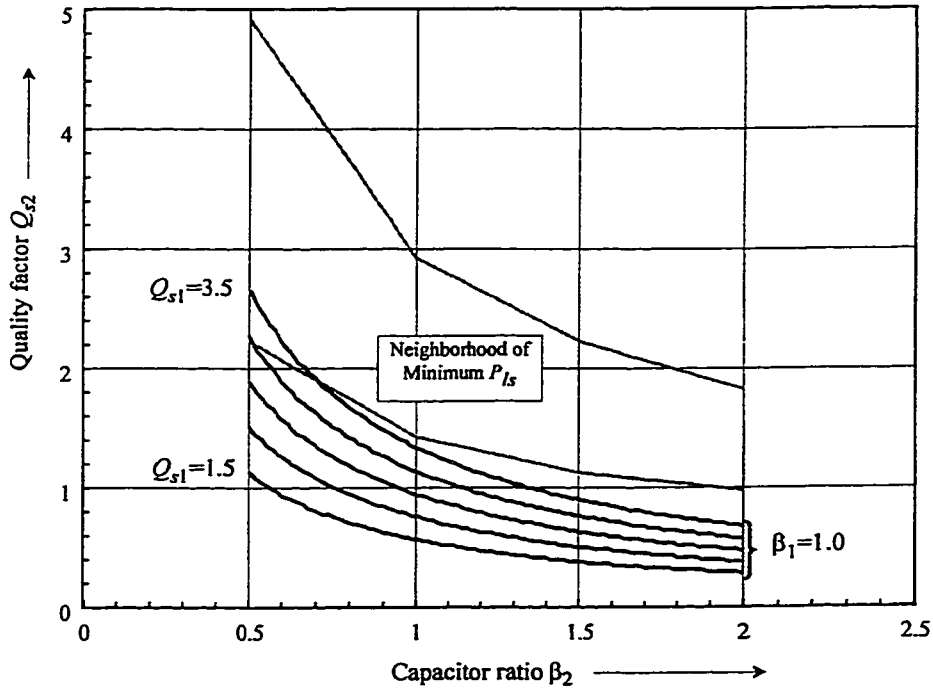


Fig. 4. 14 Quality factor Q_{s2} as a function the ratio β_2 for β_1=1.0.
Q_{s1}=[1.5, 2.0, 2.5, 3.0, 3.5].

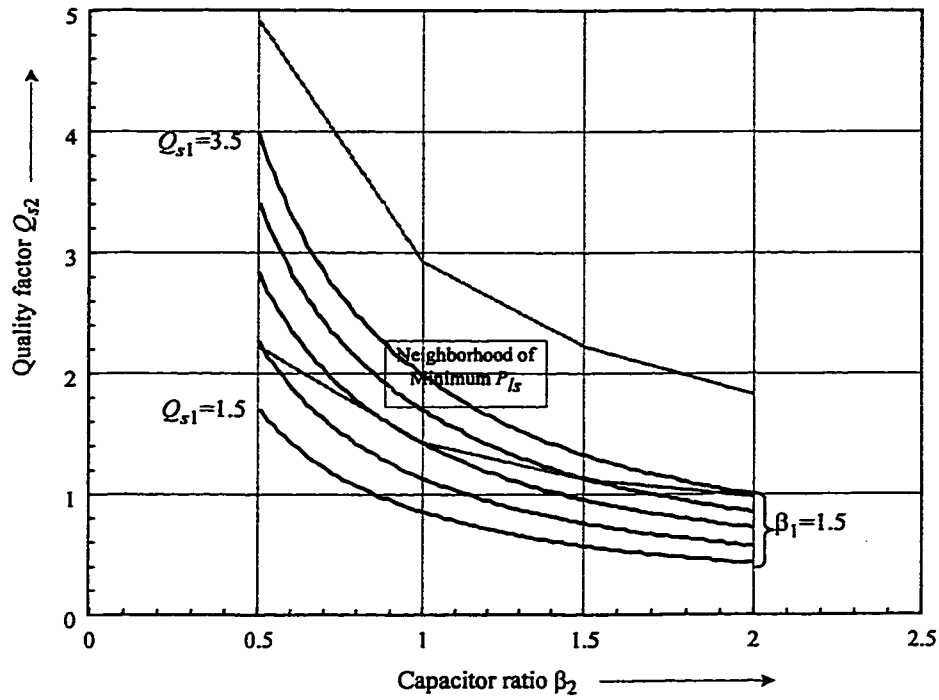


Fig.4. 15 Quality factor Q_{s2} as a function the ratio β_2 for β_1=1.5.
Q_{s1}=[1.5, 2.0, 2.5, 3.0, 3.5].

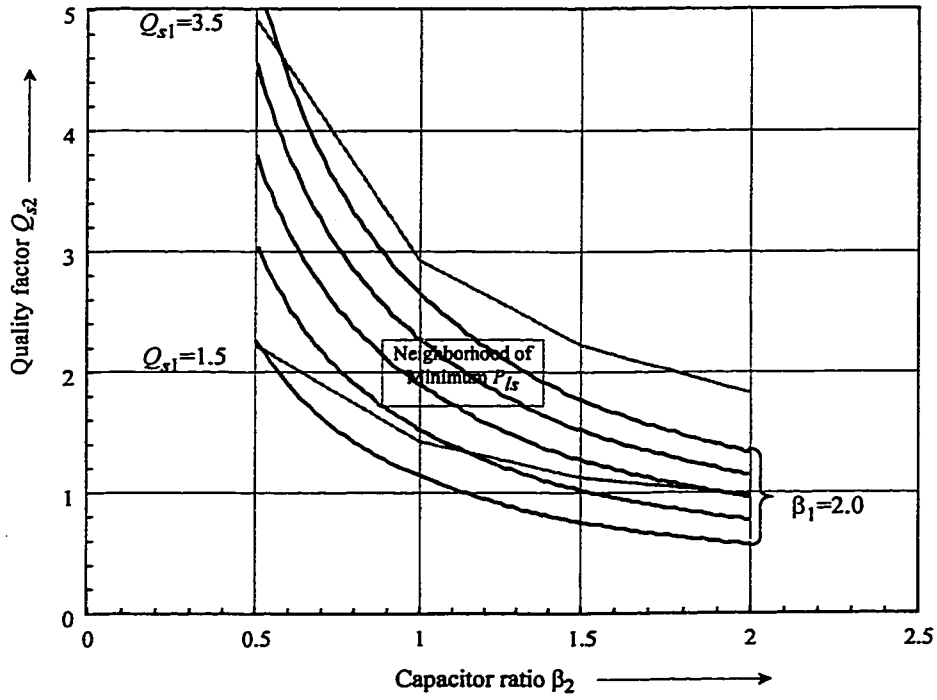


Fig. 4.16 Quality factor Q_{s2} as a function the ratio β_2 for β_1=2.0.
Q_{s1}=[1.5, 2.0, 2.5, 3.0, 3.5].

	Q_{s1}	β_1=0.5					β_1=1.0					β_1=1.5					β_1=2.0				
		1.5	2.0	2.5	3.0	3.5	1.5	2.0	2.5	3.0	3.5	1.5	2.0	2.5	3.0	3.5	1.5	2.0	2.5	3.0	3.5
β_2= 0.5	Q_{s2}	—	—	—	—	—	—	—	—	2.27	2.65	—	2.27	2.84	3.41	3.98	2.27	3.03	3.79	4.54	—
	v_o / v_{gm}	—	—	—	—	—	—	—	—	0.81	0.75	—	0.84	0.75	0.69	0.64	0.86	0.75	0.67	0.61	—
	v_{bf} / v_{gm}	—	—	—	—	—	—	—	—	1.51	1.46	—	1.54	1.46	1.40	1.35	1.55	1.47	1.40	1.34	—
	$M_{b\ max}$	—	—	—	—	—	—	—	—	1.29	1.17	—	1.29	1.13	1.03	0.97	1.29	1.09	0.99	0.91	—
β_2= 1.0	Q_{s2}	—	—	—	—	—	—	—	—	—	—	—	—	1.42	1.70	1.99	—	1.51	1.89	2.27	2.65
	v_o / v_{gm}	—	—	—	—	—	—	—	—	—	—	—	—	0.75	0.69	0.64	—	0.75	0.67	0.61	0.57
	v_{bf} / v_{gm}	—	—	—	—	—	—	—	—	—	—	—	—	1.46	1.40	1.35	—	1.47	1.40	1.34	1.30
	$M_{b\ max}$	—	—	—	—	—	—	—	—	—	—	—	—	1.19	1.07	1.00	—	1.15	1.02	0.95	0.91
β_2=1.5	Q_{s2}	—	—	—	—	—	—	—	—	—	—	—	—	—	1.14	1.33	—	—	1.26	1.51	1.77
	v_o / v_{gm}	—	—	—	—	—	—	—	—	—	—	—	—	—	0.69	0.64	—	—	0.67	0.61	0.57
	v_{bf} / v_{gm}	—	—	—	—	—	—	—	—	—	—	—	—	—	1.40	1.35	—	—	1.40	1.34	1.30
	$M_{b\ max}$	—	—	—	—	—	—	—	—	—	—	—	—	—	1.12	1.03	—	—	1.05	0.97	0.92
β_2=2.0	Q_{s2}	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0.99	—	—	—	1.14	1.33
	v_o / v_{gm}	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0.64	—	—	—	0.61	0.57
	v_{bf} / v_{gm}	—	—	—	—	—	—	—	—	—	—	—	—	—	—	1.35	—	—	—	1.34	1.30
	$M_{b\ max}$	—	—	—	—	—	—	—	—	—	—	—	—	—	—	1.06	—	—	—	0.99	0.93

TABLE 4.2 POSSIBLE PARAMETERS OF THE UPS WITH INDUCTIVE OUTPUT DC BUS FILTER.

(vi) To select a set of parameters from Table 4.2. additional criteria should be considered. One of them is the minimum voltage v_b. which the BSC can operate with constant output voltage during the backup mode. This voltage can be written as:

$$v_{b\_min} = \frac{v_o}{M_{b\_max}} \tag{4.10}$$

The equation above can also be expressed in terms of the ratios given in Table 4.2. that is:

$$\frac{v_{b\_min}}{v_{b\_f}} = \frac{v_o/\hat{v}_{gm}}{M_{b\_max}\, v_{b\_f}/\hat{v}_{gm}} \tag{4.11}$$

By using the values given in Table 4.2 it is found that $v_{b\ mim}/v_{b\ f}$ lies within the range 0.41 to 0.5. On the other hand, typical values of the ratio between the floating voltage and the end of battery discharge voltage. which are given by the manufacture of the battery. are within the range 0.66 to 0.77. Therefore. the BSC has enough gain to keep the average output dc voltage v_o constant even when operating with the lowest battery voltage. As the ratio $v_{b\ mim}/v_{b\ f}$ does not change significantly with β_1. β_2. Q_{s1} and Q_{s2}. another criterion should be considered for the selection of the set of parameters from Table 4.2 for the implementation. Both low and high values of β_2 should be avoided since they result in increased stresses in the resonant circuit (Fig. 4.10) and large switching frequency range respectively. Considering this. the set of parameters of Table 4.3 was selected for the implementation:

TABLE 4.3 SELECTED RATIOS FOR IMPLEMENTATION WITH INDUCTIVE OUTPUT DC BUS FILTER.

Q_{s1}	β_1	Q_{s2}	β_2	v_o/v_{gm}	v_{b_f}/v_{gm}
3.0	1.5	1.7	1.0	0.69	1.4

By using the ratios of Table 4.3 and considering the operation with the output dc bus at 100V and 48V battery, the power circuit parameters can be found as shown in Table 4.4.

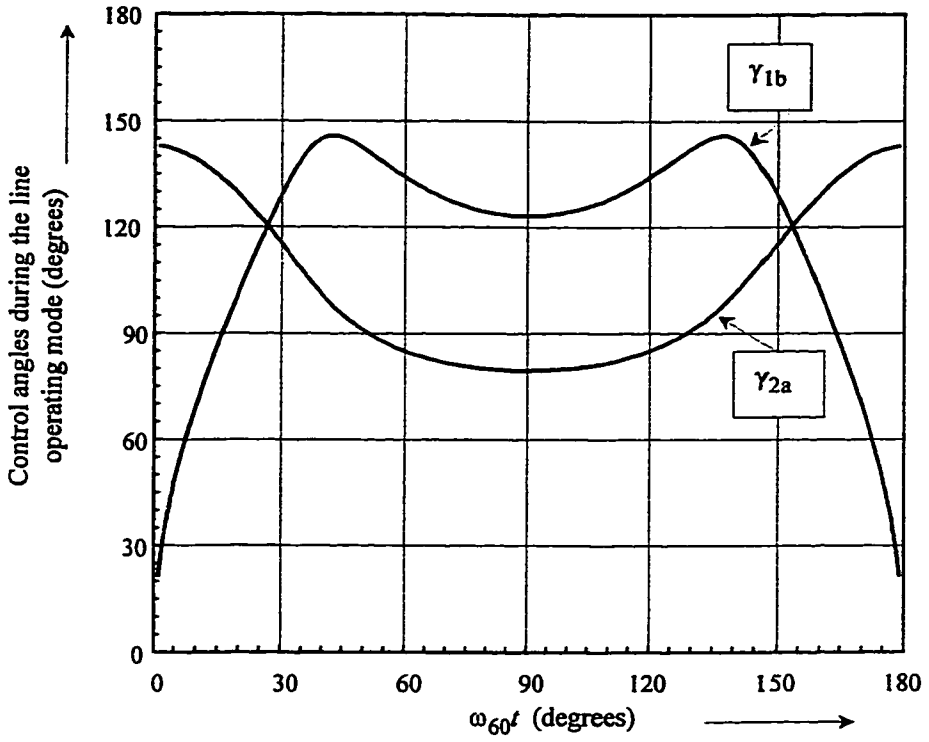
TABLE 4.4 POWER CIRCUIT PARAMETERS OF A 600W UPS WITH INDUCTIVE OUTPUT DC BUS FILTER.

L_{s1}	C_{s1}	C_p	$n_1:n_2:n_3$	L_{s2}	C_{s2}
45.3μH	75.5nF	50.3nF	100:102:26	4.7μH	0.75μF

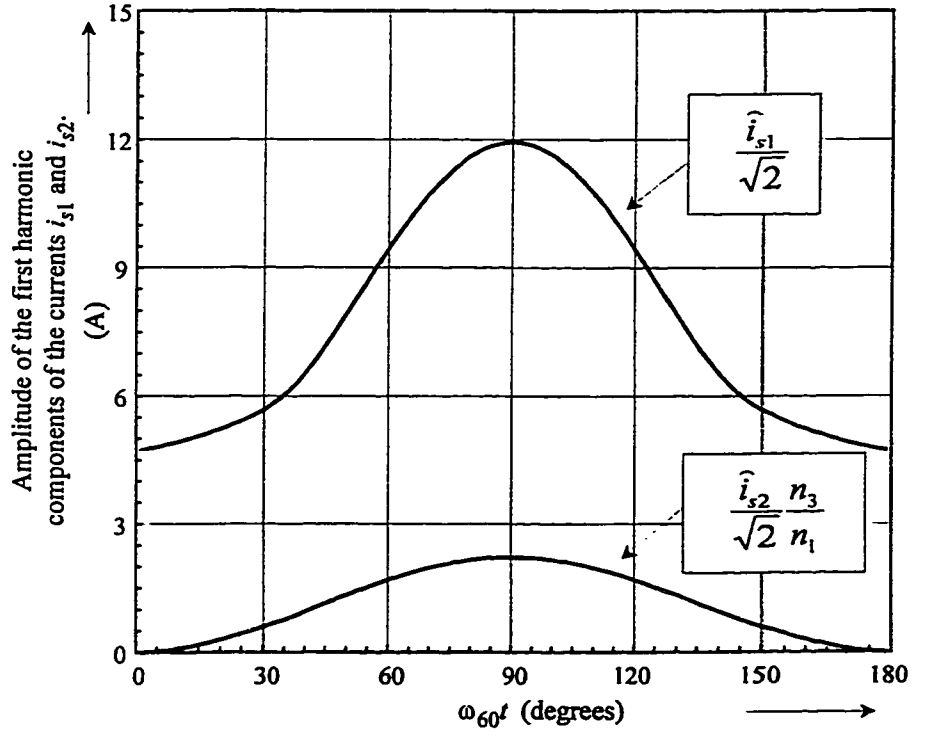
In order to verify the ability of the UPS to operate with full battery power at different output load conditions using the parameters of Table 4.4, the equivalent ac circuit described in Appendix 3 will be employed. Fig. 4.17 shows the control angles and currents when operating with full output load and maximum battery power, along half period of the incoming ac voltage. It is possible to see that the control angles γ_{1b} and γ_{2a} are within the required range for the use of the SOC proposed in Chapter 2, i.e. (0,180°). On the other hand, Fig. 4.18 shows the operation with no output load and full battery charge power. The current i_{s1} is considerably smaller than when operating at full output load, and the control angles are again between 0 and 180°. In addition, from the solution of the ac equivalent circuit for the backup mode of operation (Appendix 3) it was found that the control angle γ_{2b} is 97° for operation with $0.77v_{b\_f}$ and 172° with $0.465\ v_{b\_f}$

If the minimum value of voltage v_b is greater than $0.465v_{b\,f}$. then the current stresses in the BSC will not be minimized since the control angle γ_{2b} will never be180^{o}.

A low for $v_{b\,mim}$ was obtained due to the that the selected battery floating voltage had to be 1.6 to 2.3 times greater than the output voltage (with the transformer turns ratio 1:1:1). In order to make the floating voltage equal to v_o the peak value of v_{cp} should be limited at v_o. Series parallel resonant converters with capacitive output filter do have this feature of limiting the voltage across the parallel resonant capacitor [91-93]. The next section investigates the operation of the proposed UPS topology when operating capacitive output filter.



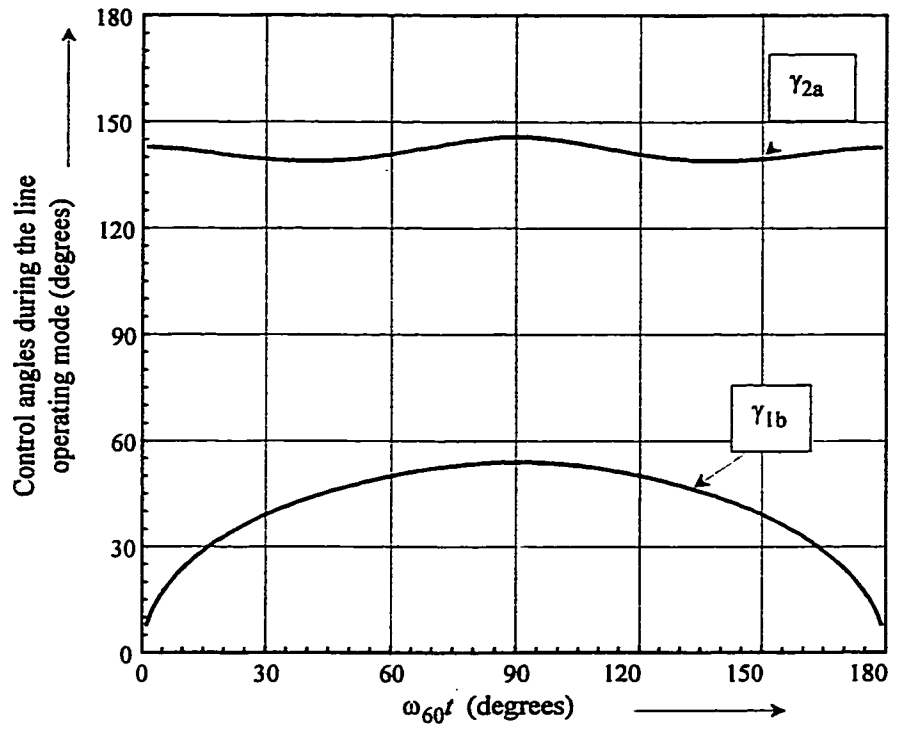
(a)



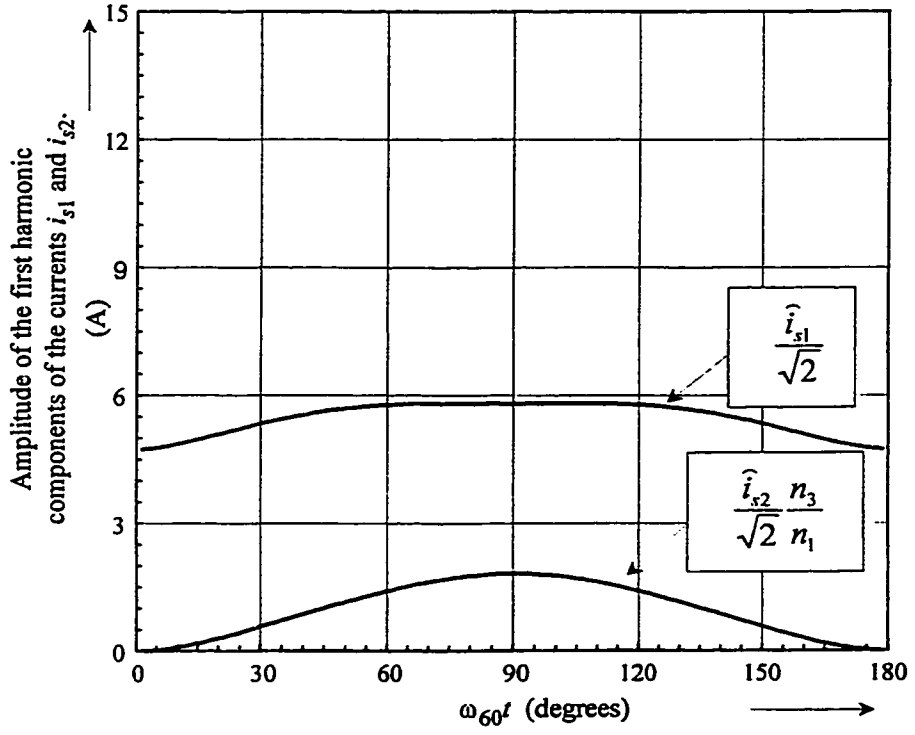
(b)

Fig. 4.17 Analytical results from the solution of the equivalent ac circuit. Full load at the output.

Parameters of the UPS as given in Table 4.5. P_o=500 W, P_b=100 W, v_{in}= 102 V rms.



(a)



(b)

Fig. 4.18 Analytical results from the solution of the equivalent ac circuit. No load at the output.

Parameters of the UPS as given in Table 4.5. P_o=5 W, P_b=100 W, v_{in}= 138 V rms.

4.4 OPERATION WITH CAPACITIVE OUTPUT FILTER

This section begins with the description of an ac-to-dc series parallel resonant converter with capacitive output filter under VFPSM, which is the starting point for the understanding of the operation LSC. The main design curves for the selection of the resonant circuit parameters are presented in a similar way to that in Chapter 3 for inductive output dc bus filter. Then, a design procedure for the selection of the parameters of the UPS is developed. Finally, a design example of a series parallel resonant UPS with capacitive output filter is presented, and verified by simulations.

4.4.1 Line Operating Mode

The main waveforms of the series parallel resonant converter operating with capacitive output filter under VFPSM are shown in Fig. 4.19. The voltage v_{ab1} has a quasi-square waveform, where the width of the non-zero voltage pulse is defined by the control angle γ_{1b}. The main difference between the operation of a series parallel resonant converter with capacitive and inductive output filter is found in the voltage across the parallel resonant capacitor, as can be concluded by comparing Fig. 4.7 and Fig. 4.8 with Fig. 4.19.

When operating with a capacitive output filter, the voltage v_{cp} is clampled at the output voltage v_o whenever one of the diodes of the output rectifier conducts. When the current i_{s1} crosses zero and changes polarity the diode of the output rectifier that was previously conducting blocks and the voltage v_{cp} starts to reverse its polarity. When the

amplitude v_{cp} reaches v_o a diode of the output rectifier is forward biased. Consequently, the current i_{s1} is transferred to the output stage and v_{cp} is again clamped at v_o.

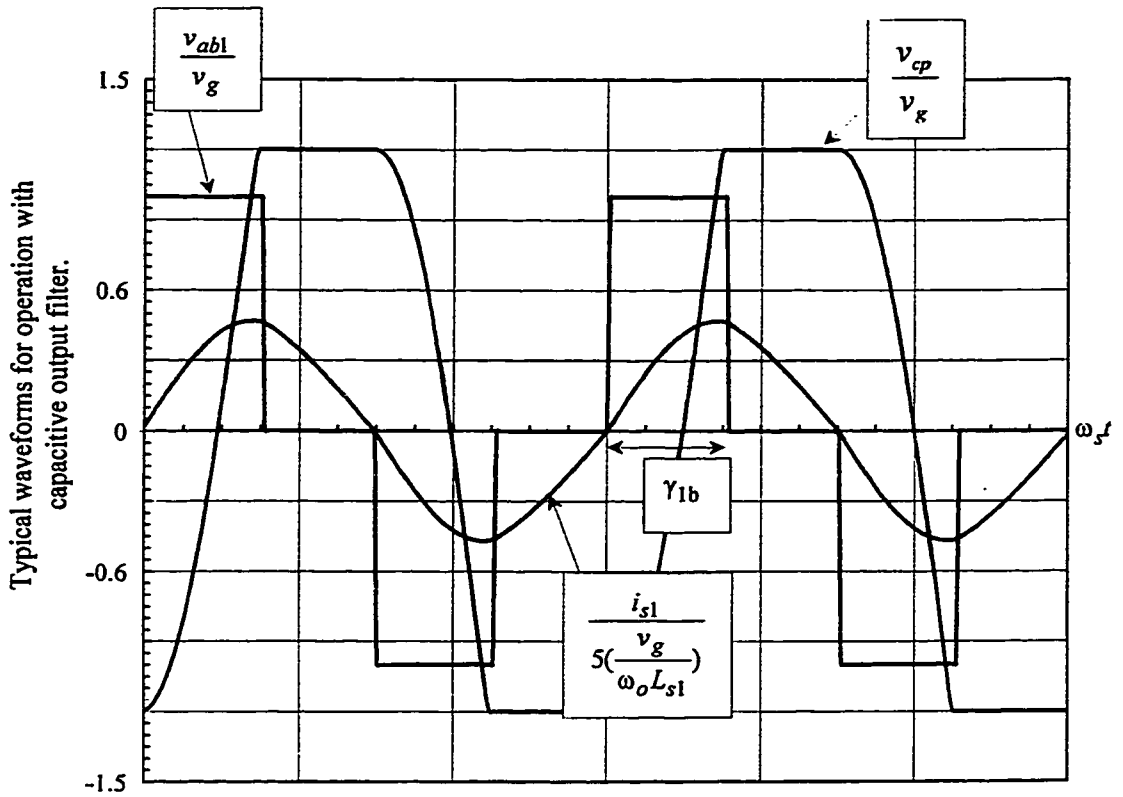


Fig. 4.19 Operation with capacitive output filter.
Simulation results. $\gamma_{1a}=180^o$, $\gamma_{1b}=91.7^o$, $i_b=0$, $Q_{s1}=0.55$,$\alpha=1.48$,$\beta_1=1.5$.

In terms of the analysis of the converter with capacitive output filter, the describing function method can not be easily applied. This is because the current drawn by the output rectifier from the resonant circuit is not in phase with the voltage v_{cp}. Therefore, the representation of the of the output stage by an equivalent load resistor is less acceptable. On the other hand, the generalized state-space modeling approach of static converters can be used to describe the operation of series parallel resonant converters with capacitive output filter. This approach is adopted in Appendix 4 for the analysis of the converter with capacitive output filter. In order to obtain the key design

curves of a ac-to-dc series parallel resonant converter operating with capacitive output filter the same approach adopted in Chapter 3 will be used. The control angle at the resonance frequency is identified for different values of Q_{s1} and β_1 from the static characteristics of the converter. Then, the maximum output voltage for the converter operating with constant output voltage and unity input power factor is determined. This maximum voltage conversion ratio, Fig. 4.20, and the switching frequency ratio at the peak of the incoming ac line, Fig. 4.21, are required to compute the parameters of the resonant circuit. A detailed description of the steps carried out to obtain these curves is given in Appendix 4.

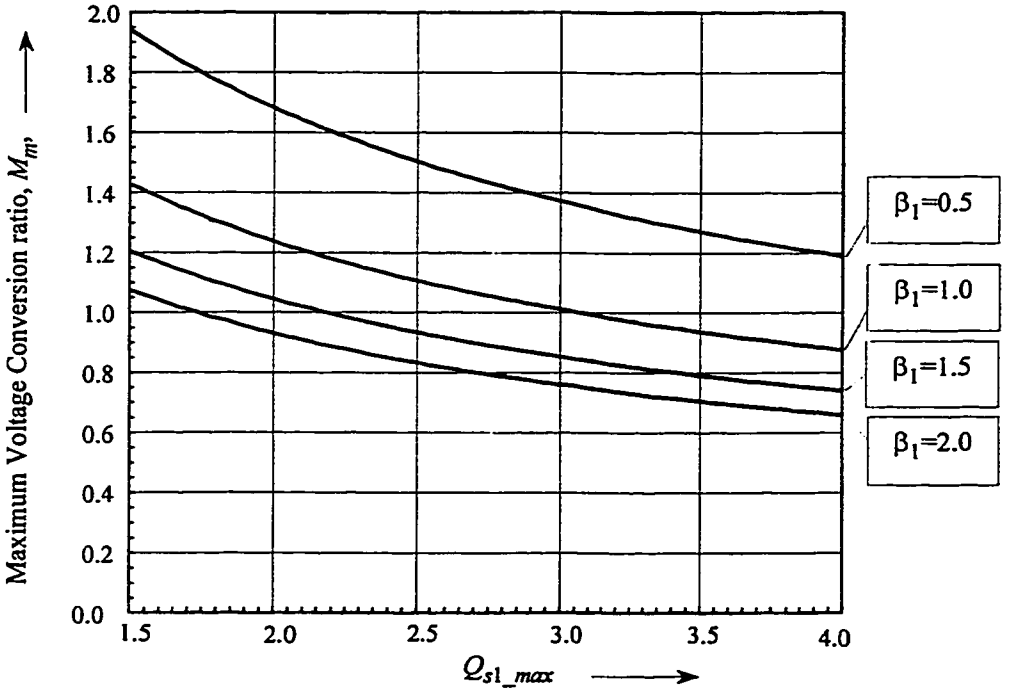


Fig. 4.20 Maximum voltage conversion ratio for operation with constant output voltage and unity input power factor with capacitive output filter.

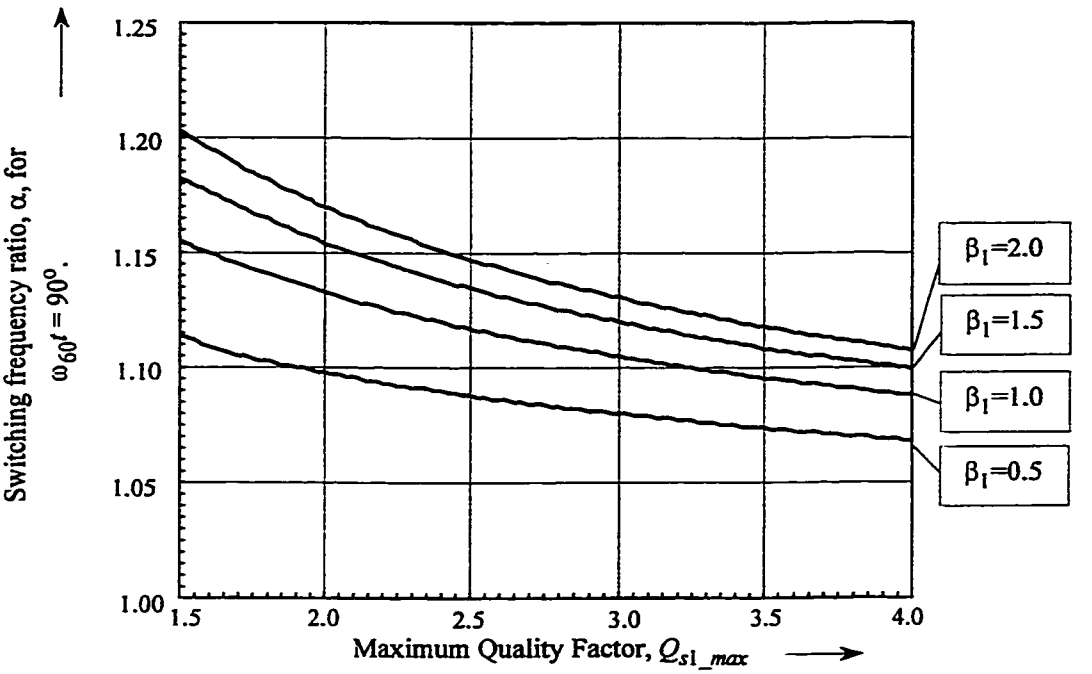


Fig. 4.21 Switching frequency ratio at $\omega_{60}t=90^{o}$. Operation with VFPSM and with capacitive output filter.

The parameters of the resonant circuit can be computed in a way similar to that in Chapter 3, i.e. from a given minimum switching frequency, input power and lowest incoming ac voltage:

$$\omega_o = \frac{\min(\omega_s)}{\alpha} \tag{4.12}$$

$$L_{s1} = \frac{Q_{s1\_max}\dfrac{M_m{}^2\hat{v}_{gm}^2}{P_{in}}}{\omega_o} \tag{4.13}$$

$$C_{s1} = \frac{1}{\omega_o^2 L_{s1}} \text{ and } C_p = \frac{C_{s1}}{\beta_1}. \tag{4.14, 4.15}$$

The equations presented above were derived for an ac-to-dc converter, however they also can be used for the design of the proposed UPS by considering that the total power of the UPS is lumped in the main output.

4.4.2 Backup Mode

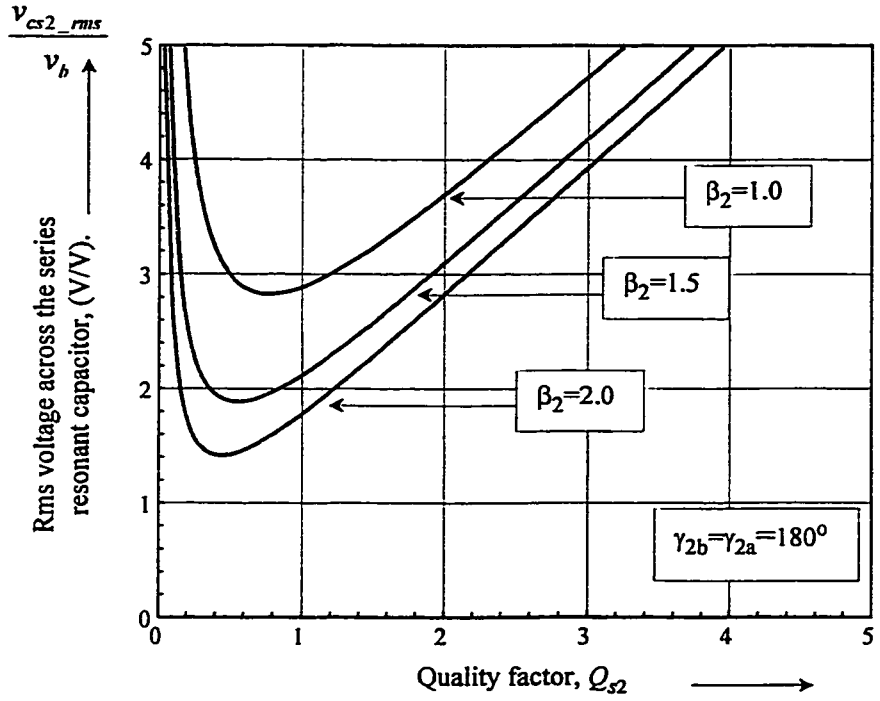
During the backup mode, the BSC operates as a series parallel dc-to-dc converter with capacitive output filter. VFPSM is again adopted since it results in smaller switching frequency range when compared with VF. It is possible to see from Fig. 4.22 that, during the backup mode, the stresses in the resonant circuit reduce by increasing β_2. β_2=0.5 is not plotted since it results in high stresses. On the other hand, it is worth mentioning that the switching frequency range increases with β_2, as can be concluded from Table 4.5.

TABLE 4.5 VARIATION OF THE SWITCHING FREQUENCY WITH THE LOAD.

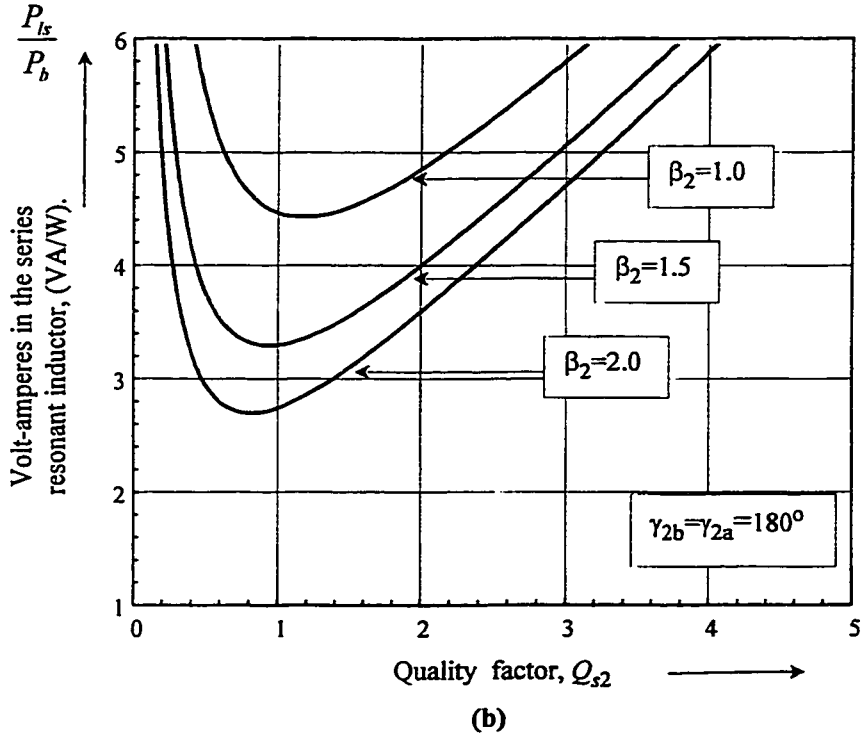
	Ratio between the series and the parallel resonant capacitors, β_2			
	0.5	1.0	1.5	2.0
$\frac{\alpha\|_{Q_{s2}=0.2} - \alpha\|_{Q_{s2}=2}}{\alpha\|_{Q_{s2}=2}} 100$	15.7%	35.18 %	52.7%	67.6%

At full load Q_{s2}=2.

By using the information gathered so far, a design procedure for the proposed UPS with capacitive output filter is developed in the next section.



(a)



(b)

Fig. 4.22 Stresses in a series-parallel resonant converter with capacitive output filter during the backup mode.

(a) Ratio between the voltage across the series resonant capacitor v_{cs2} and the battery voltage. (b) Ratio between the volt-amperes associated with the resonant inductor L_{s2} and the battery power.

4.4.3 Design Procedure and Example

The design procedure presented in Section 4.3.3 for the UPS with inductive output filter can be modified for the UPS with capacitive output dc bus filter. For the UPS with capacitive output dc bus filter, the design step (ii), which computes the peak value of the voltage across the parallel resonant capacitor, is simplified since the peak value of v_{cp} is equal to the output voltage v_o.

In order to clarify the design steps, let us consider the UPS specified in Section 4.3.4, now operating with capacitive output dc bus filter. In this case, the design steps are as follows:

(i) For Q_{s1_max}=1.5 and β_1=0.5 it is found from Fig. 4.20 that the maximum voltage conversion ratio is M_m=1.94. Therefore, the output dc voltage is given by:

$$v_o = \hat{v}_{gm} M_m = 280.35\,\text{V}\,. \tag{4.16}$$

By using the given minimum switching frequency and the switching frequency ratio obtained from Fig. 4.21 the resonant frequency ω_o can be found as:

$$\omega_o = \frac{\min(\omega_s)}{\alpha} = 565.4\ \text{krad/s}\,. \tag{4.17}$$

By using (4.13) to (4.15), the values of L_{s1}, C_{s1} and C_p can be found as:

$$L_{s1} = 173.8\,\mu\text{H} \tag{4.18}$$

$$C_{s1} = 18.0\text{nF} \text{ and } C_p = 36.0\,\text{nF}\,. \tag{4.19}$$

(ii) The peak value of v_{cp} is equal to v_o.

(iii) The battery floating voltage is selected as

$$v_{b\_f} = 1.1 v_o = 308.3\,\text{V} \tag{4.20}$$

where the factor 1.1 was included to account for the voltage rings. which result from the leakage inductance of the transformer. that may increase the peak of v_{cp} in practical setup.

(iv) Once the parallel resonant capacitor and the output voltage are defined the factor Q_{s2} and the ratio β_2 are found to be related by:

$$Q_{s2} = \frac{P_o}{\omega_o C_p v_o^2} \frac{1}{\beta_2} = 0.319 \frac{1}{\beta_2}. \qquad (4.21)$$

The equation (4.21) is plotted in Fig. 4.23 for $0.5 < \beta_2 < 2.0$. A region defined by the points around (+/-10%) the minimum volt-amperes in resonant inductor L_{s2} during the backup mode is also indicated in Fig. 4.12. It is seen that for these values of Q_{s1} and β_1 the stresses in the resonant circuit are high since Q_{s2} is far from the minimum of P_{ls}.

(v) By repeating steps (i) to (iv), the Q_{s2} factor as a function β_2 can be obtained for other typical values of Q_{s1} and β_1. as shown in Fig. 4.24 to Fig. 4.27. Table 4.6 summarizes the main parameters of the UPS for the pairs (Q_{s2}. β_2) within the defined neighborhood of P_{ls} minimum.

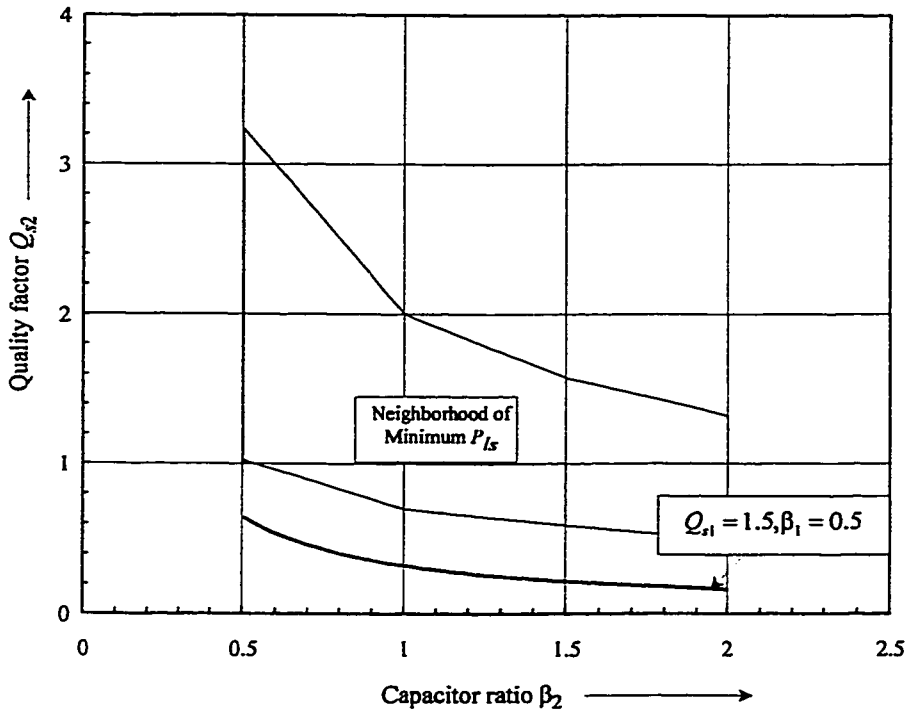


Fig. 4.23 Quality factor Q_{s2} as a function the ratio β_2

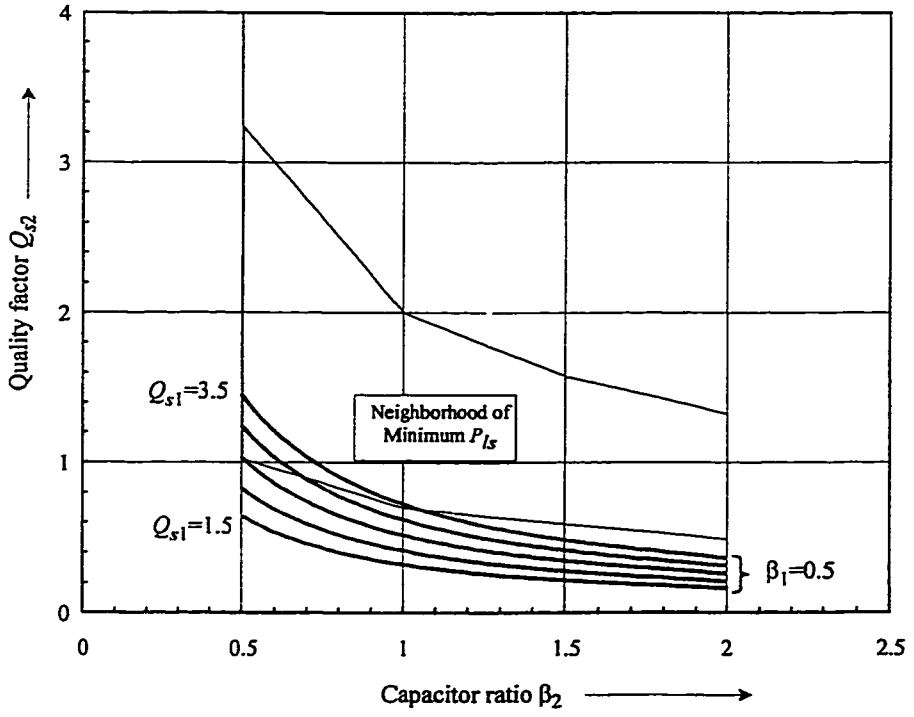


Fig. 4.24 Quality factor Q_{s2} as a function the ratio β_2 for β_1=0.5.
Q_{s1}=[1.5, 2.0, 2.5, 3.0, 3.5].

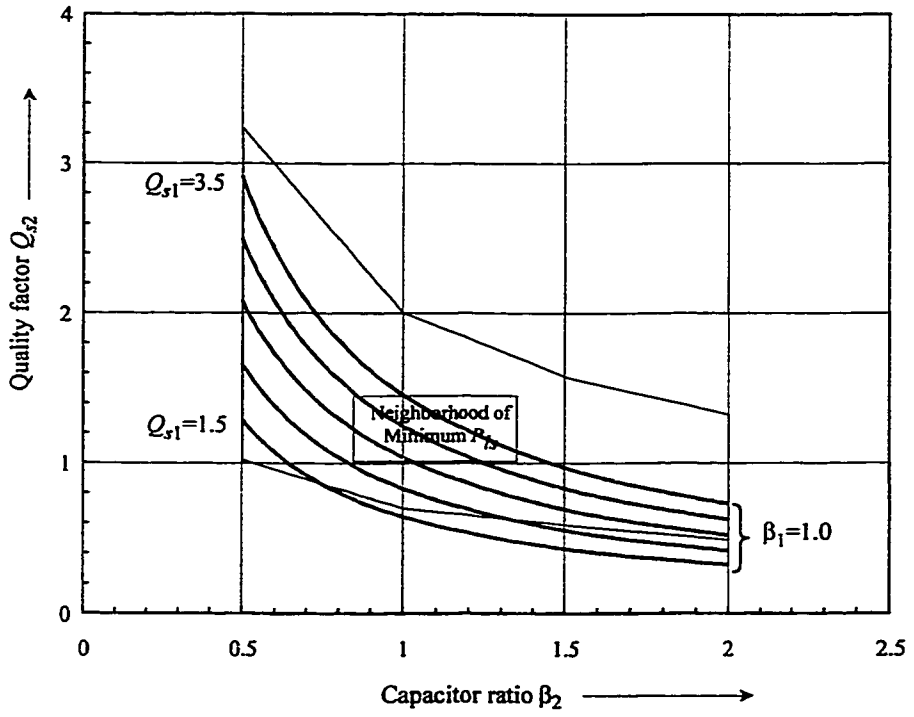


Fig. 4.25 Quality factor Q_{s2} as a function the ratio β_2 for β_1=1.0.
Q_{s1}=[1.5, 2.0, 2.5, 3.0, 3.5].

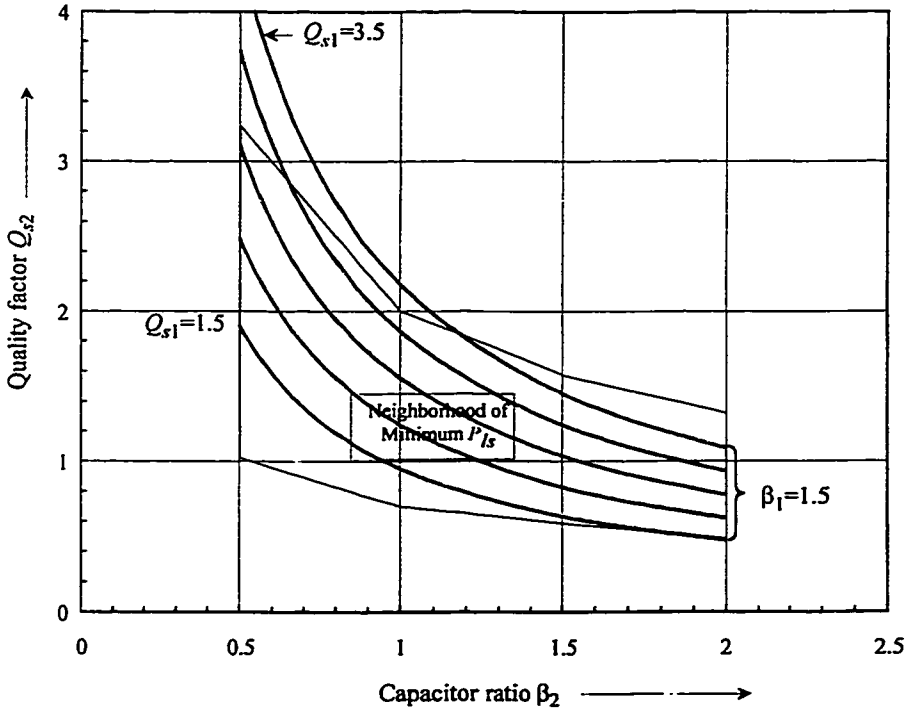


Fig. 4.26 Quality factor Q_{s2} as a function the ratio β_2 for β_1=1.5.
Q_{s1}=[1.5, 2.0, 2.5, 3.0, 3.5].

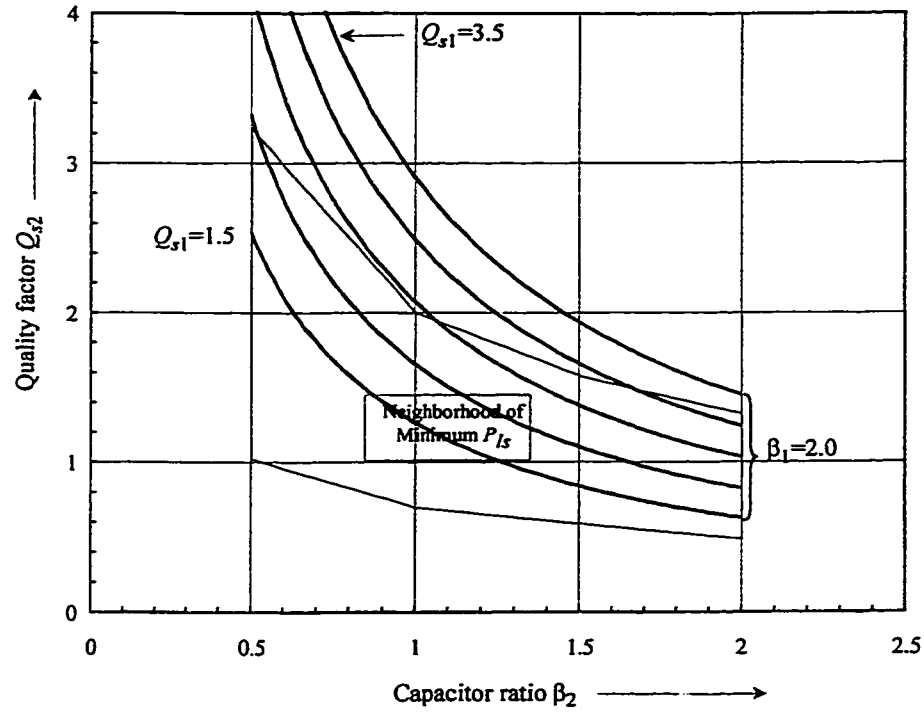


Fig. 4.27 Quality factor Q_{s2} as a function the ratio β_2 for β_1=2.0
Q_{s1}=[1.5, 2.0, 2.5, 3.0, 3.5].

(v) To select a set of parameters from the Table 4.6 an additional criterion should considered. The minimum voltage v_b, which the BSC can operate with the desired output voltage during the backup mode, is a strong candidate since it determines the current stresses during the backup mode. By using the values given in Table 4.6 it is found that v_{b_mim}/v_{b_f} increases with β_1, Q_{s1}, and decreases with β_2 . In addition, v_{b_mim}/v_{b_f} belongs to the interval 0.44 to 0.71. Therefore, the ratio v_{b_mim}/v_{b_f} is close to the typical values of the ratio between the floating voltage and the end discharge voltage, which are given by the manufacture of the battery, 0.66 to 0.77.

	Q_{s1}	β_1=0.5					β_1=1.0					β_1=1.5					β_1=2.0				
		1.5	2.0	2.5	3.0	3.5	1.5	2.0	2.5	3.0	3.5	1.5	2.0	2.5	3.0	3.5	1.5	2.0	2.5	3.0	3.5
β_2= 0.5	Q_{s2}	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	v_o / v_{gm}	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	v_{bf} / v_{gm}	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	M_{b_max}	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
β_2= 1.0	Q_{s2}	—	—	—	—	0.79	—	0.83	1.04	1.25	1.46	0.96	1.25	1.56	1.87	—	1.27	1.67	—	—	—
	v_o / v_{gm}	—	—	—	—	1.27	—	1.24	1.11	1.01	0.94	1.19	1.05	0.94	0.85	—	1.06	0.93	—	—	—
	v_{bf} / v_{gm}	—	—	—	—	1.40	—	1.36	1.22	1.11	1.03	1.31	1.15	1.03	0.94	—	1.17	1.02	—	—	—
	M_{b_max}	—	—	—	—	2.07	—	1.95	1.72	1.59	1.49	1.79	1.59	1.46	1.37	—	1.57	1.42	—	—	—
β_2=1.5	Q_{s2}	—	—	—	—	—	—	—	0.69	0.83	0.97	0.64	0.83	1.04	1.25	1.46	0.85	1.11	1.39	—	—
	v_o / v_{gm}	—	—	—	—	—	—	—	1.11	1.01	0.94	1.19	1.05	0.94	0.85	0.79	1.06	0.93	0.83	—	—
	v_{bf} / v_{gm}	—	—	—	—	—	—	—	1.22	1.11	1.03	1.31	1.15	1.03	0.94	0.87	1.17	1.02	0.92	—	—
	M_{b_max}	—	—	—	—	—	—	—	1.78	1.63	1.52	1.86	1.63	1.48	1.39	1.33	1.61	1.45	1.35	—	—
β_2=2.0	Q_{s2}	—	—	—	—	—	—	—	0.52	0.62	0.73	—	0.62	0.78	0.94	1.09	0.64	0.83	1.04	1.25	—
	v_o / v_{gm}	—	—	—	—	—	—	—	1.11	1.01	0.94	—	1.05	0.94	0.85	0.79	1.06	0.93	0.83	0.76	—
	v_{bf} / v_{gm}	—	—	—	—	—	—	—	1.22	1.11	1.03	—	1.15	1.03	0.94	0.87	1.17	1.02	0.92	0.84	—
	M_{b_max}	—	—	—	—	—	—	—	1.83	1.67	1.55	—	1.67	1.51	1.41	1.34	1.65	1.47	1.36	1.29	—

TABLE 4.6 POSSIBLE PARAMETERS OF THE UPS WITH CAPACITIVE OUTPUT DC BUS FILTER.

By taking a typical ratio between the battery floating and end of discharge voltages as 0.77 and assuming an additional voltage drop of 10% in the power circuit. the ratio between v_{b_mim}/v_{b_f} should be 0.69. The set parameters that result in v_{b_mim}/v_{b_f} close to 0.69 are highlighted in Table 4.6. Among them, the set given in Table 4.7 is selected for the implementation.

TABLE 4.7 SELECTED RATIOS FOR THE IMPLEMENTATION. CAPACITIVE OUTPUT FILTER.

Q_{s1}	β_1	Q_{s2}	β_2	v_o/v_{gm}	v_{b_f}/v_{gm}
2.5	2.0	1.39	1.5	0.83	0.92

By using the ratios of Table 4.7 in a UPS with the output dc bus at 100V and with a 48V battery. the power circuit power circuit parameters can be found as given in Table 4.8.

TABLE 4.8 POWER CIRCUIT PARAMETERS OF A 500W UPS. CAPACITIVE OUTPUT DC BUS FILTER.

L_{s1}	C_{s1}	C_p	n_1:n_2:n_3	L_{s2}	C_{s2}
55.0 µH	60.6 nF	30.3 nF	100:120:41	12.3 µH	0.27 µF

Simulations were carried out in order to verify the ability of the UPS to operate with full battery power at different output load conditions, with the parameters of Table 4.8. Fig. 4.28 shows the main waveforms of the power circuit. It is possible to see that zero voltage switching can be achieved in both the LSC and the BSC since the current i_{s1} lags v_{ab1} and i_{s2} leads v_{ab2}. Fig. 4.29 shows the control angles when operating with full output load and maximum battery power, along a half period of the incoming ac voltage. It is possible to see that the control angle γ_{1h}

becomes close to 180° as was predicted in the design. On the other hand, Fig. 4.30 shows the current drawn by the incoming ac line and sent to the battery during the line operating mode under full load. From this figure, it is concluded that the UPS is able to correct the input power factor while operating with the desired output dc bus voltage.

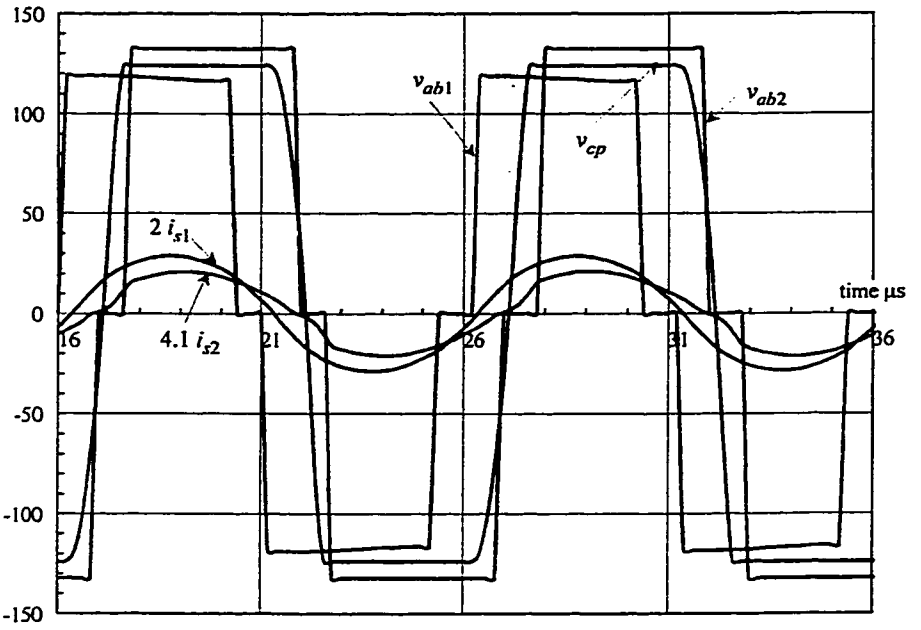


Fig. 4.28 Simulation results. Main waveform of the proposed UPS with capacitive output dc bus filter.
Parameters according with Table 4.8. Operation at full load.

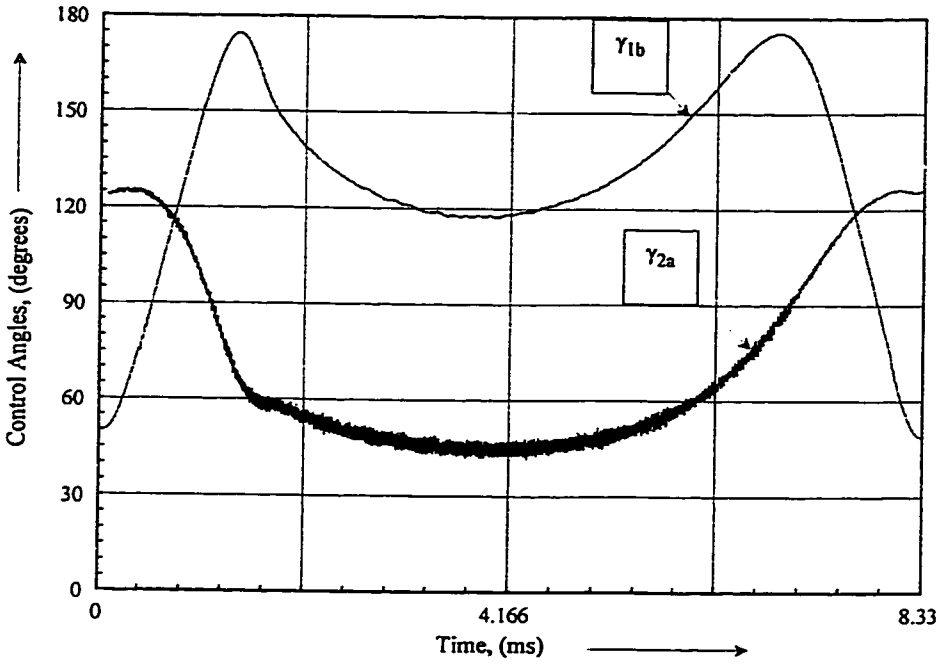


Fig. 4.29 Simulation results. Control Angles for operation with a capacitive output dc bus filter.

UPS Parameters according with Table 4.8. P_o=500W, P_b=100W, v_{in}=102V rms.

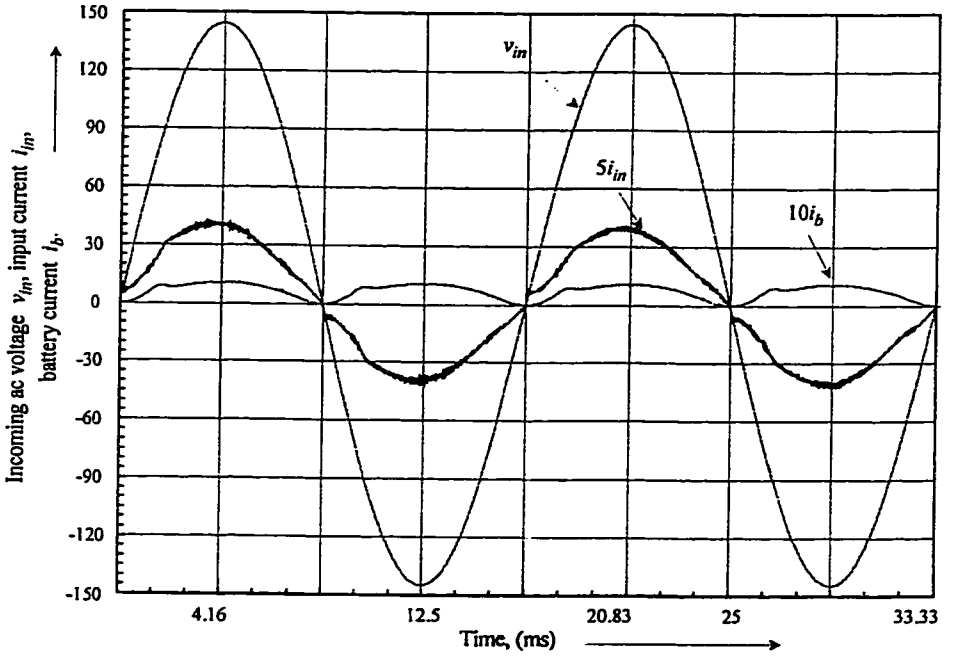


Fig. 4.30 Simulation results. Input ac current and battery current when operating with capacitive output filter.

UPS Parameters according with Table 4.8. P_o=500W, P_b=100W, v_{in}=102V rms.

Experimental results are presented in Section 4.6 and they are used to draw comparisons between the UPS with and inductive output capacitive output filter. The next section describes the output side converter, whose operation is independent on whether the UPS has a capacitive or inductive output dc bus filter.

4.5 OUTPUT SIDE CONVERTER

The output side converter produces the desired output voltage waveform from the output dc bus. This converter is comprised of a PWM inverter followed by a second order low pass filter. The output filter attenuates the harmonics generated by the inverter. There are two major modulation methods for the single phase PWM inverters, which are the bipolar switching scheme and the unipolar switching scheme (UPWM). The latter has superior performance in terms of switching losses and filter requirements when compared with the former [86]. Aiming to keep the switching losses at a reasonable value the switching frequency of the output inverter was selected to be 20 kHz. For operation at higher switching frequencies, the commutation losses reduce the output inverter efficiency significantly. Once the switching frequency is defined, the output filter and the output voltage controller can be designed. A second order filter with a cut off frequency of 3.2 kHz was selected, and a controller with state feedback and dynamic output feedback was used to control the output voltage. The performance of the implemented OSC as well as the output transient due to change in the load are given in the next section.

4.6 EXPERIMENTAL VERIFICATION

The feasibility of the proposed UPS topology operating with both inductive and capacitive output dc bus filter was verified using an experimental setup. The nominal incoming ac voltage is 120 V rms, the battery voltage is 48 V, and the output dc bus voltage is 100V. The parameters of the resonant circuit and the transformer turns ratio were obtained from the design examples of Section 4.3.4 and Section 4.4.3.

4.6.1 Operation with Inductive Output DC Bus Filter

The parameters used in the implementation are given in Table 4.9.

TABLE 4.9 IMPLEMENTED CIRCUIT PARAMETERS. INDUCTIVE OUTPUT DC BUS FILTER.

L_{s1}	C_{s1}	C_p	L_{s2}	C_{s2}	n_1: n_2: n_3
46.1μH	75nF	50nF	4.85μH	888 nF	10:10:3

Two sets of experiments were carried out. The first one considers the operation in the line operating mode and the second one in the backup mode.

4.6.1.1 Line Operating Mode

The main goal of this set of experiments is to verify the ability of the high frequency converters to sent power to the output and the batteries as predicted in the earlier sections. Table 4.10 summarized the results obtained when operating with full load during the line operating mode.

TABLE 4.10 UPS AT FULL LOAD.
INDUCTIVE OUTPUT DC BUS FILTER.

V_{in}	V_o	V_b	P_{in}	P_o	P_b
120 V	98.5V	55V	710 W	516W	102

From Table 4.10, it is concluded that with the selected parameters, the UPS has enough gain to operate with full output power while charging the battery, as predicted in the design. It was also observed that the operation with high input voltage and full battery power is achievable. The current drawn by the converter from the ac line, and the current sent to the batteries and to the output stage are shown in Fig. 4.31. The input current i_{in} follows a sine waveform in phase with the input voltage while the current i_b has a waveform that approaches a sine square.

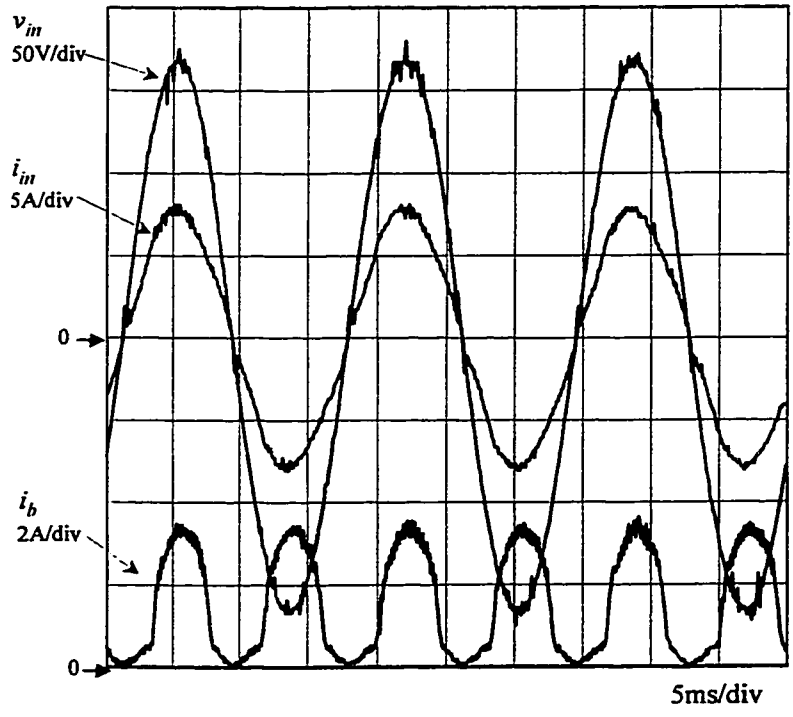


Fig. 4.31 Experimental results. Line operating mode with inductive output dc bus filter.
Operating conditions given in Table 4.10.

The equations (A3.4)-(A3.15) were solved again for the parameters shown in Table 4.9 and operating condition of Table 4.10. The peak of the current i_{s1} obtained from the analysis was 16.9A while the same current obtained from measurement in the breadboard implementation was 17.1A. The switching frequency at the peak of the line voltage obtained analytically was 101kHz while the experimental measurement shows the same frequency as 110kHz.

Fig. 4.32 shows the current and voltage at the output of the LSC and it is seen that the ZVS is achieved. On the other hand, Fig. 4.33 shows the voltage and current at the battery side converter. It is possible to identify two modes of operation. When operating with low battery charging current or near the valley of the input voltage the current i_{s2} becomes small and its magnitude may not be large enough to ensure the conduction of the anti-parallel diode before the turn-on of the transistors of leg A of the BSC. In order to avoid switching losses when i_{s2} becomes small the following steps can be taken:

(i) To increase the dead times of the BSC, or decrease the snubber capacitors.

(ii) To use an auxiliary inductive circuit to provide the required additional current to ensure zero voltage switching. This auxiliary circuit is small since the current i_{s2} is either zero or it flows in the proper direction to reset the snubber capacitors. The diagram of the implemented circuit is shown in Fig. 4.34 (a).

Fig. 4.34 (b) shows the current and voltage at the BSC when the battery charge current is zero. It is possible to see that zero voltage switching is achieved.

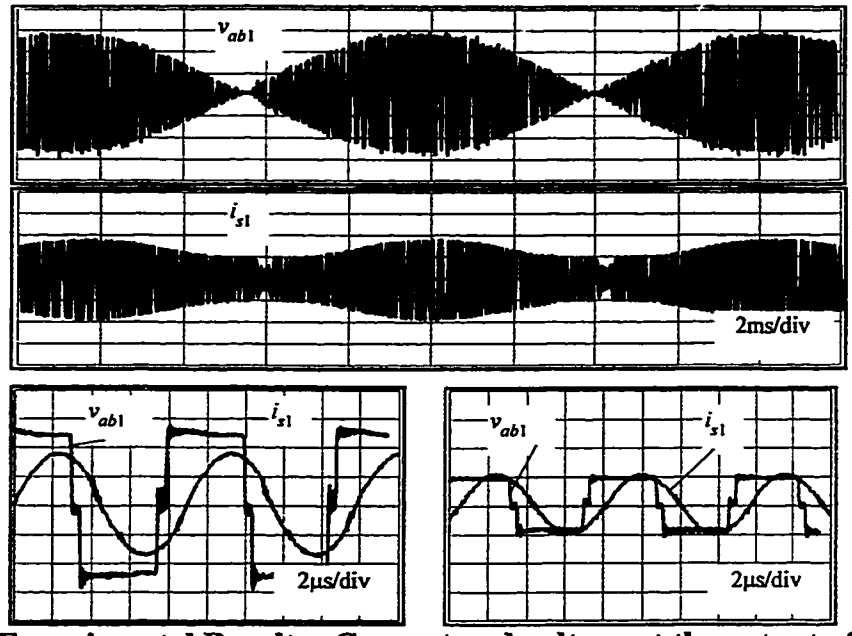


Fig. 4.32 Experimental Results. Current and voltage at the output of the LSC.
P_o=516 W and P_b=121 W. Scales: Vertical scales: 50V/div, and current 10 A/div. Horizontal scales: 2ms/div and 2μs/div.

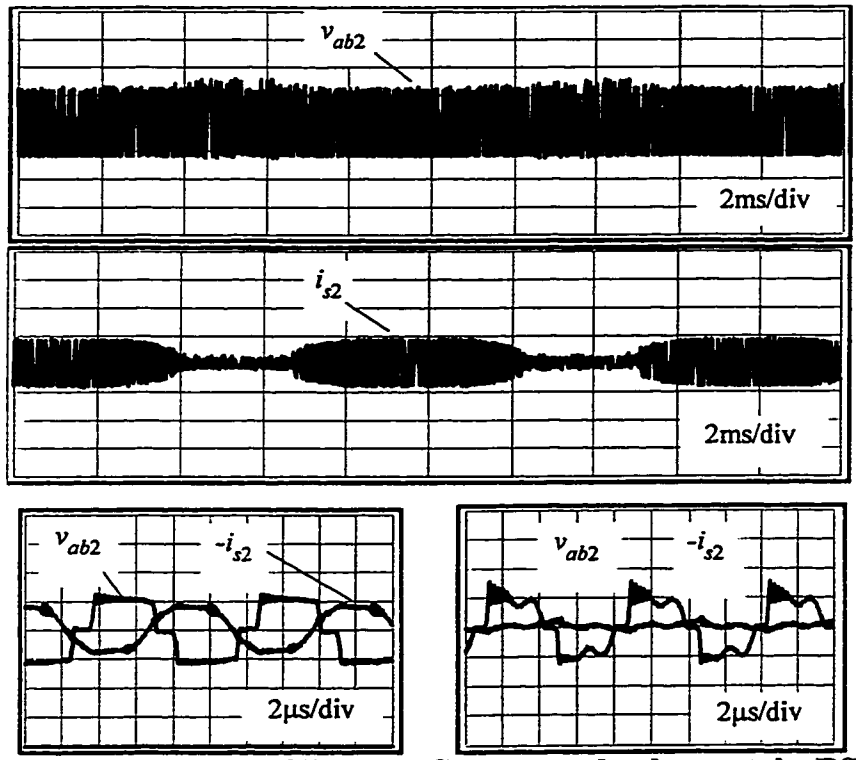


Fig. 4.33 Experimental Results. Current and voltage at the BSC.
P_o= 516 W and P_b=121 W. Vertical scales: voltage 50V/div, current 10 A/div.; Horizontal scales: 2ms/div and 2μs/div.

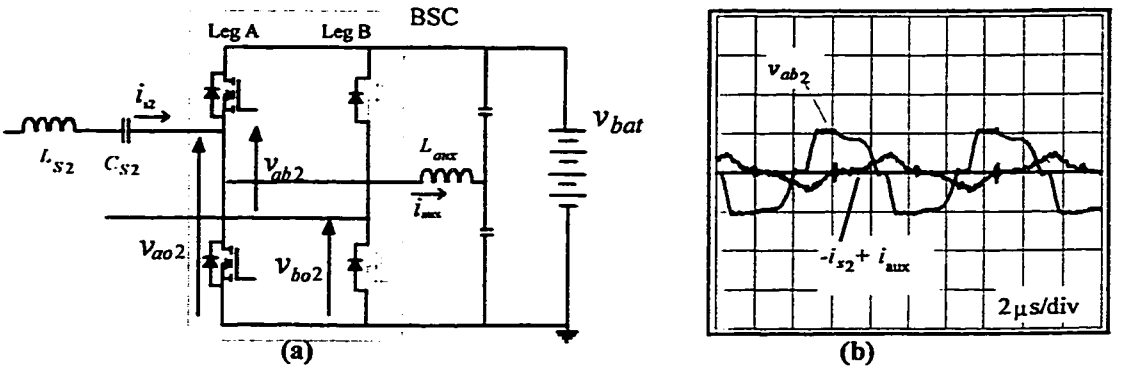


Fig. 4.34 Auxiliary circuit to ensure ZVS when i_b is zero.

(a) Circuit implementation. **(b)** Experimental Results with the circuit shown in (a). 500 W sent to the output side converter no power sent to the batteries. Scales: Voltage 50V/div; Current 5 A/div.

4.6.1.2 Backup Mode

The voltage across the terminal of the battery side converter during the backup mode operation at full load and with the typical battery end of discharge voltage is shown in Fig. 4.35. It is possible to see that the current crosses zero inside the non zero voltage pulse of v_{ab2} and that the amplitude of the current is agreement with the prediction obtained from the solution of the equivalent circuit of Appendix 3 (peak of the current i_{s2} obtained analytically was 29.4A and 27A experimentally, and γ_{1b}=106° analytically and 115° experimentally).

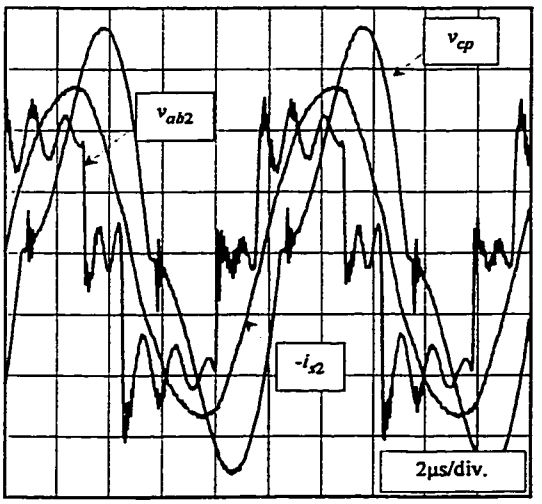


Fig. 4.35 Experimental Results. Backup mode of operation.

The current and voltage at the terminals of the BSC for operation with 500 W and 42 V battery voltage. Vertical scales: Voltage v_{ab2}: 20V/div, v_{cp}: 50V/div, and Current i_{s2}:10 A/div. Horizontal scale: 2μs/div.

4.6.2 Operation with Capacitive Output DC Bus Filter

This section is similar to the previous one, however the output dc bus filter is capacitive. The parameters used in the experimental setup were selected to match those obtained from the design carried out in Section 4.4.3. The implemented circuit parameters are given in Table 4.11. A detailed diagram of the implemented circuit is given in Appendix 5.

TABLE 4.11 IMPLEMENTED CIRCUIT PARAMETERS.
CAPACITIVE OUTPUT DC BUS FILTER.

L_{s1}	C_{s1}	C_p	L_{s2}	C_{s2}	n_1:n_2:n_3
55 μH	60 nF	41 nF	12.5 μH	300 nF	13:11:5

The next sub-sections present experimental results for both the line-operating mode and backup mode.

4.6.2.1 Line Operating Mode

Table 4.12 summarizes the results obtained during the line-operating mode with full output load and maximum battery charging power.

TABLE 4.12 LINE OPERATING MODE.
CAPACITIVE OUTPUT DC BUS FILTER.

v_{in}	v_o	v_b	P_{in}	P_o	P_b
120 V	98.7V	55.5V	690 W	481W	121

From Table 4.12, it is concluded that with the selected parameters, the converter has enough gain to delivery the nominal power to the output and to the battery, as predicted in the design. It also was observed that the operation with full output power

and zero battery power is also possible. In order to illustrate the main input and output quantities of the UPS, Fig. 4.36 shows the current drawn by the converter from the ac line and the current sent to the battery. It is possible to see that the input power factor is close to unity. The distortion in the input current can be reduced by derating the converter in the design, typically by 10%, to compensate for the losses in the circuit.

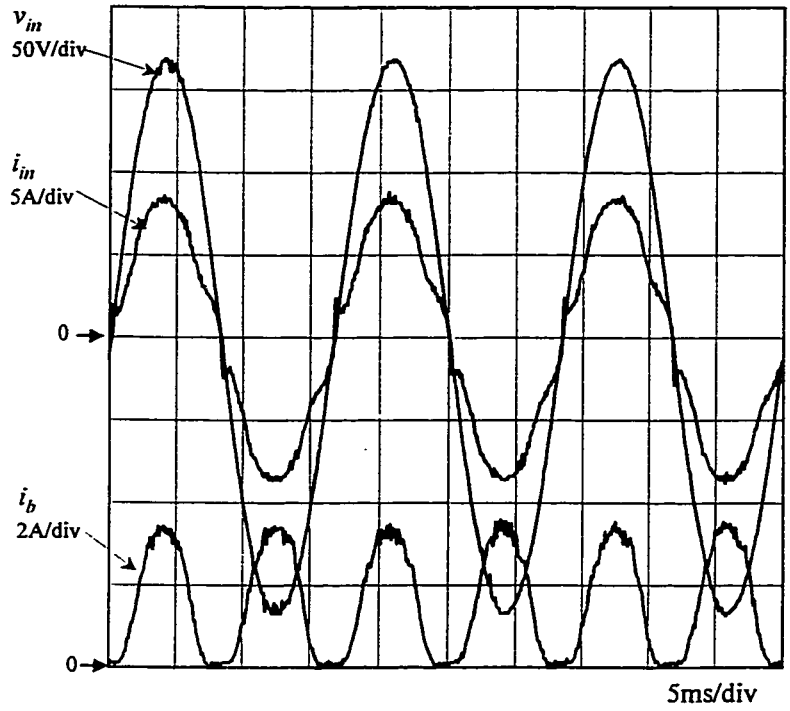


Fig. 4.36 Experimental results. Line operating mode with capacitive output dc bus filter.
Operating conditions given in Table 4.12.

Fig. 4.37 shows the current and voltage at the output of the LSC. This figure demonstrates that the current i_{s1} crosses zero inside the non-zero voltage pulse of v_{ab1} at the different points of the incoming ac line, and that ZVS can be achieved. On the other hand, Fig. 4.38 shows the voltage and current at the battery side converter, and again ZVS is achieved at the different points of operation.

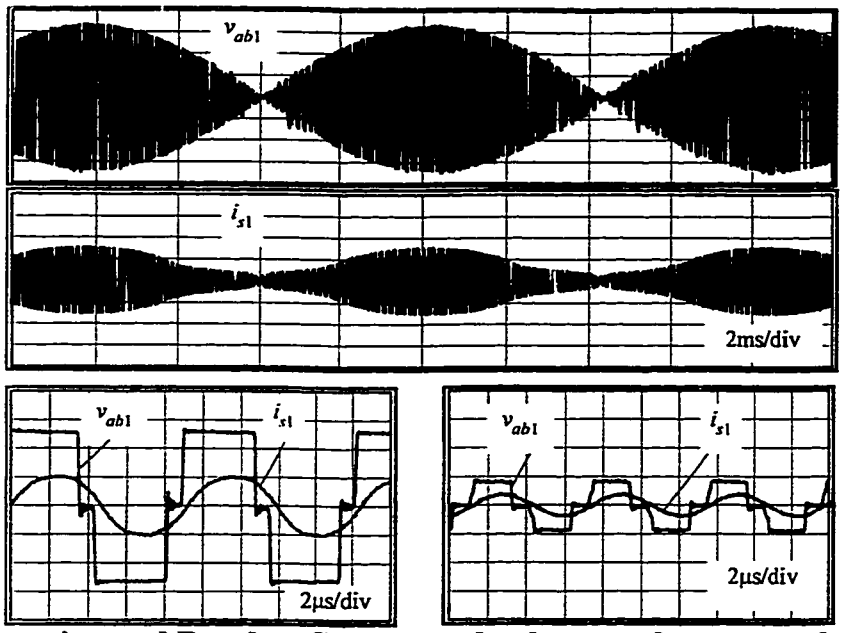


Fig. 4.37 Experimental Results. Current and voltage at the output of the LSC for operation with capacitive output dc bus filter.

P_O=481W and P_b=121 W. Vertical scales: 50V/div, and current 10 A/div. Horizontal scales: 2ms/div and 2μs/div.

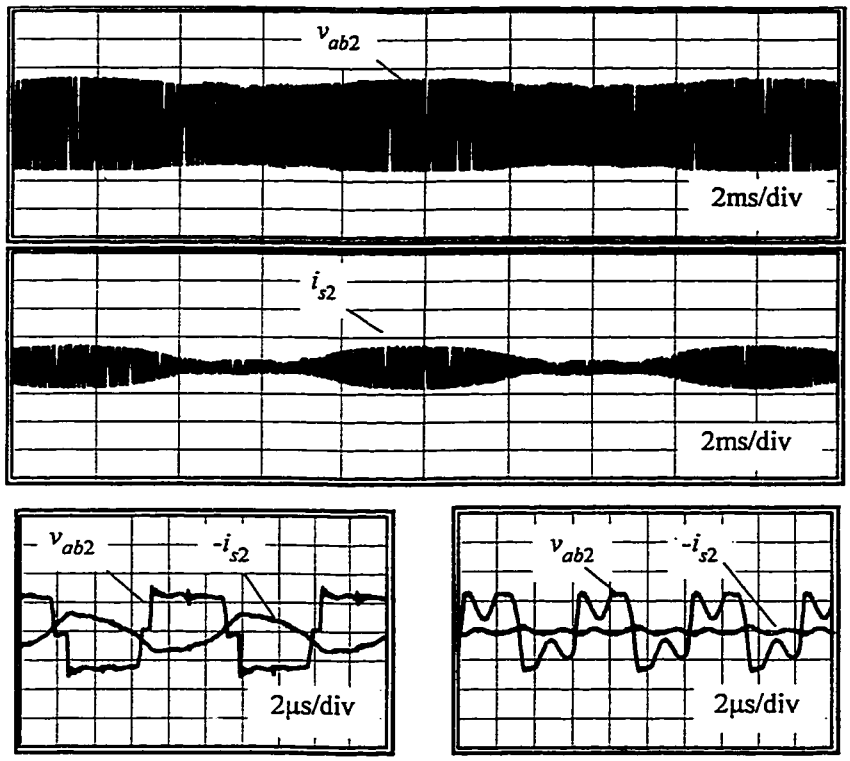


Fig. 4.38 Experimental Results. Current and voltage at the BSC for operation with capacitive output dc bus filter.

P_o= 481 W and P_b=121 W. Vertical scales: voltage 50V/div, current 10 A/div.; Horizontal scales: 2ms/div and 2μs/div.

4.6.2.2 Backup Mode

The voltage across the terminal of the battery side converter during the backup mode operation with capacitive output dc bus filter is shown in Fig. 4.39. The current $-i_{s2}$ crosses zero inside the non-zero voltage pulse of v_{ab2} and the control angle γ_{1b} is close to 180°. In addition, this figure also shows that the voltage across the parallel resonant capacitor voltage is clamped at the output dc bus voltage, v_o, which in this case is 100V.

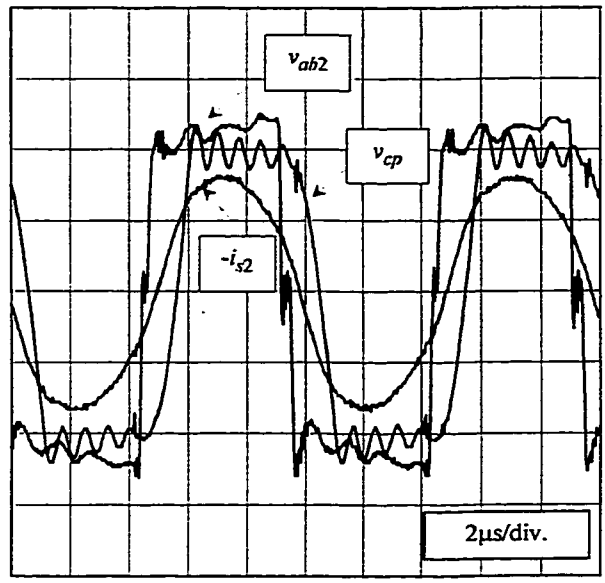


Fig. 4.39 Experimental Results. Backup mode of operation with capacitive output dc bus filter.

Operation with 470 W and 45 V battery voltage. Vertical scales: Voltage v_{ab2}:20V/div. Voltage v_{cp}: 50V/div. Current i_{s2}:10 A/div. Horizontal Scale: 2μs/div.

4.6.3 Input-output Performance

The performance of the proposed UPS in terms of input power factor and efficiency under the different modes of operation is given in this section.

Fig. 4.40 summarizes the performance of the proposed UPS with inductive output dc bus filter during the line operating mode. The input power factor is close to unity, and the total harmonic distortion is low, around 7.5 % at full load. The overall efficiency of the UPS in the line-operating mode at full load is about 87%. Similarly, Fig. 4.41 shows

the performance of the UPS with capacitive output dc bus filter. The input power factor is close to unity, however the THD of the input current at full load is about 11% and it is larger than that with an inductive output filter. The efficiency at full load with capacitive output dc bus filter is about 87%. The main differences of the performance of the UPS with capacitive and inductive output filters is found in the efficiency during the backup mode, as shown in Fig. 4.42. With inductive output dc bus filter the efficiency at full load is about 81%, however with capacitive output dc bus filter it reaches 87%. The reason for the difference in the efficiencies comes from the fact the amplitude of the current i_{s2} during the backup mode with capacitive output dc bus filter is smaller than that when operating with inductive output filter.

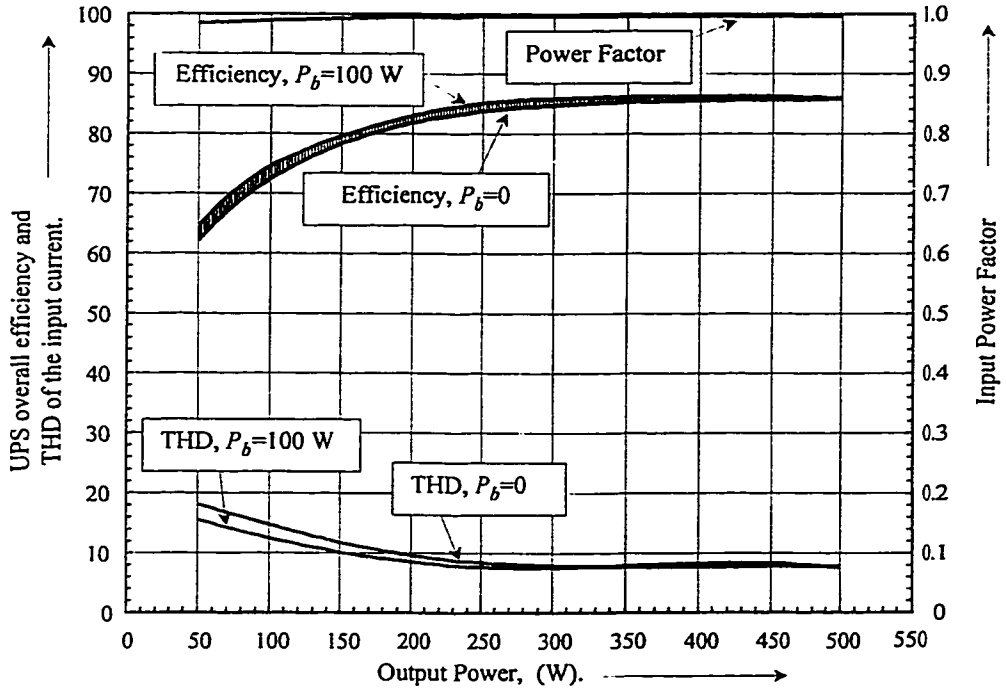


Fig. 4.40 Experimental results. Operation with inductive output dc bus filter during the line operating mode.

Input power factor and total harmonic distortion of the input current i_{in} and the UPS overall efficiency. v_{in} = 120 V, v_b=55V,v_o=100V.

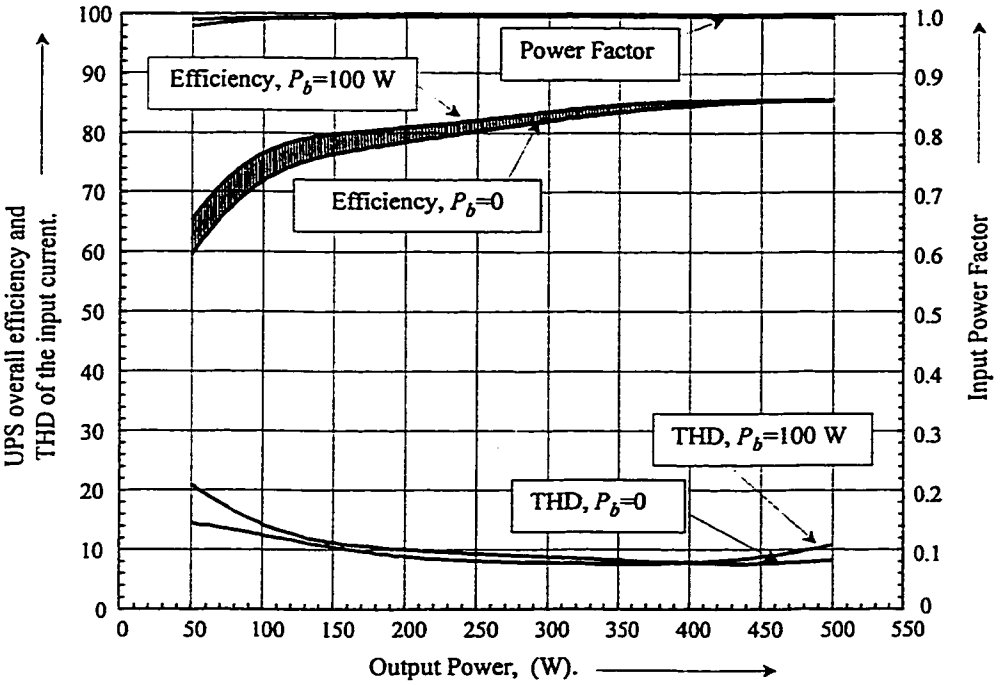


Fig. 4.41 Experimental results. Operation with capacitive output dc bus filter during the line operating mode.

Input power factor and total harmonic distortion of the input current i_{in} and the UPS overall efficiency. v_{in} = 120 V, v_b=55V,v_o=100V.

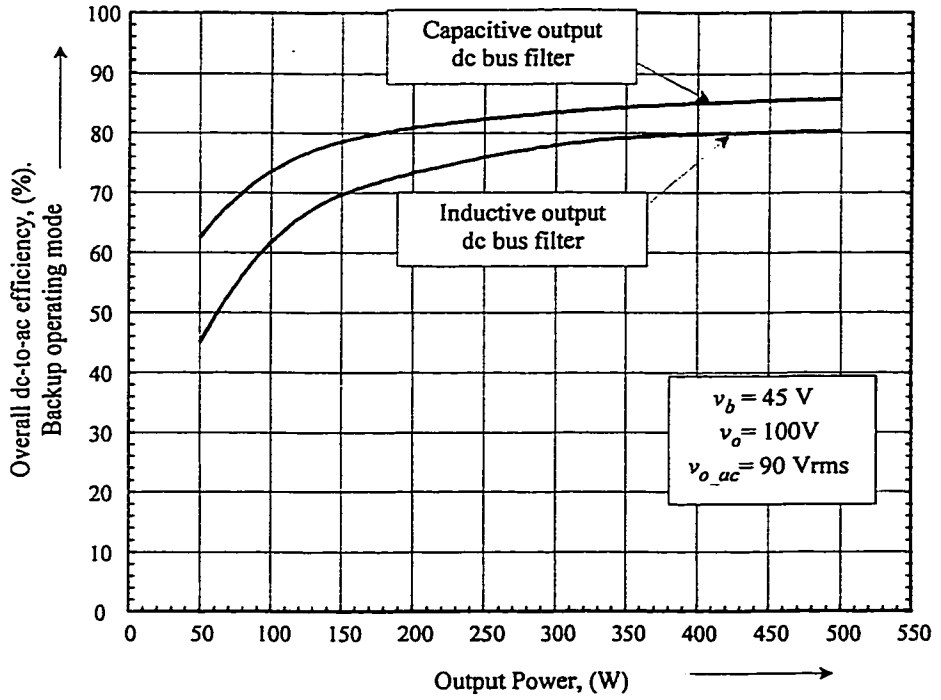


Fig. 4.42 Experimental results. Efficiency in the backup operating mode.

4.6.4 Output Side Converter

The output inverter operates at 20 kHz and produces a trapezoidal output waveform of 90V rms at 60Hz. The output transient due to change in the load is shown in Fig. 4.43. It is observed that the transient response features a very small undershoot, which is smaller than 2%.

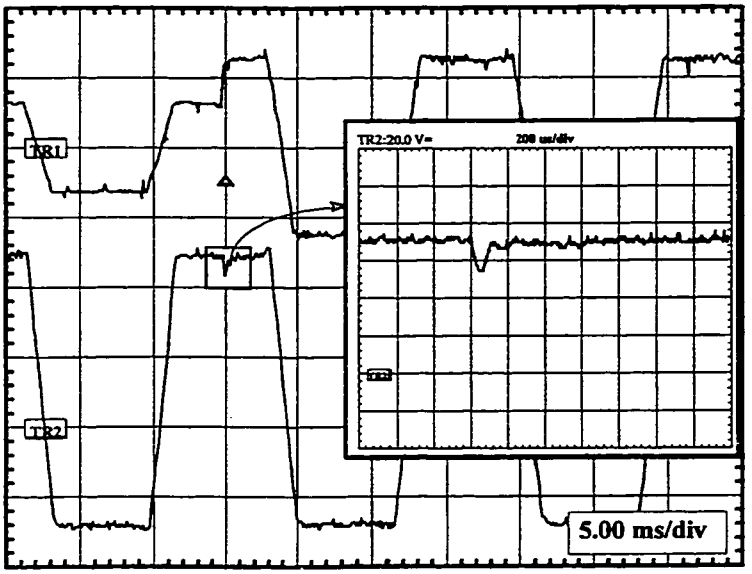


Fig. 4.43 Experimental results. Transient due to a step change in the load.
Output power changes from 200 to 400 W . Top: Output current . Bottom: output voltage . Output fitter parameters: L=500μH, C=5μF. Switching frequency 20 kHz with UPWM. Vertical Scales: 50V/div, and 4A/div.

4.7 DISCUSSION AND CONCLUSIONS

In this chapter two variations of the proposed UPS topology based on resonant converters were analyzed and verified experimentally. The main features of the proposed topologies are: (i) operation with high input power factor without the use of a dedicated power factor correction stage, (ii) flexibility in the selection of the input, battery and output voltages, (iii) zero voltage switching operation (this allows the use of high switching frequency leading to the use small isolation transformer).

A design procedure for the selection of the resonant circuit parameters of the proposed UPS was developed. This design was applied for the selection of the parameters of the UPS with inductive and capacitive output dc bus filter. It was demonstrated that operation with capacitive output dc bus filter result in better performance due to the reduced current stresses during the backup mode. Experimental results have been used to validate the design procedure developed and to demonstrate the performance of the proposed UPS topology.

CHAPTER 5: UPS TOPOLOGY BASED ON BIDIRECTIONAL CONVERTERS

5. 1 INTRODUCTION

Isolated bidirectional dc-to-dc and dc-to-ac converters are often required in UPS applications. In order to reduce the size and weight of the UPS without penalizing the efficiency a soft-switching technique must be adopted. The concept of self-sustained oscillation presented in the pervious chapters was successfully applied to ensure zero voltage switching for different resonant converters. In this chapter, this concept is extended to resonant bidirectional converters, particularly dc-to-dc and dc-to-ac converters. Then, by using these converters, a fully isolated ZVS UPS is derived, analyzed and verified experimentally.

The outline of this chapter is as follows: Section 5.2 describes a ZVS isolated bidirectional dc-to-dc converter that operates in self-sustained oscillation mode. Similarly, Section 5.3 deals with ZVS resonant dc-to-ac converter that operates in self-sustained oscillation mode. Section 5.4 presents a ZVS UPS topology that uses concepts developed in the previous sections. Finally, Section 5.5 summarizes the main points of this chapter.

5.2 ZERO VOLTAGE SWITCHING BIDIRECTIONAL DC-TO-DC CONVERTER

Among the reported bidirectional dc-to-dc converters a strong candidate for a given implementation is the dual active bridge topology [87,88]. The dual active bridge consists of two active converters interfaced by a synchronous inductance, where this inductance is usually an integral part of the transformer required to provide galvanic isolation and voltage match between the input and output of the converter. The power transfer from the input to the output and the output voltage control are accomplished by changing the phase-shift between the voltages at the output of the two converters of the dual active bridge. By proper design of the transformer leakage inductance, it is possible to operate with ZVS within a certain range of output power and input to output voltage ratio. Despite of the desired features of the dual active bridge, it has the following drawbacks:

(i) The range of ZVS operation is restricted.

(ii) The dc component that results from non-ideal characteristics of the converter components may result in saturation of the transformer.

The operation with ZVS in a larger output power range can be achieved by exploring the bi-directional power transfer capabilities of the dual active bridge. In this case, the converter is cycled sequentially between the forward and reverse power flow to maintain the desired "average" output power while operating within the ZVS range. The drawback of this approach is the low frequency components introduced in the input and output terminals. Another alternative, which does not introduce low frequency components neither increases significantly the conduction losses, is to change the

switching frequency so that ZVS is ensured at light load conditions. This alternative will be explored here, by adopting the self-sustained controller proposed in Chapter 2.

The second drawback that is associated with the dc component can be overcome by introducing a capacitor in series the transformer. Therefore, the capacitor blocks any dc component that may be generated by the converter. Fig. 5.1 shows the bi-directional dc-to-dc converter under consideration.

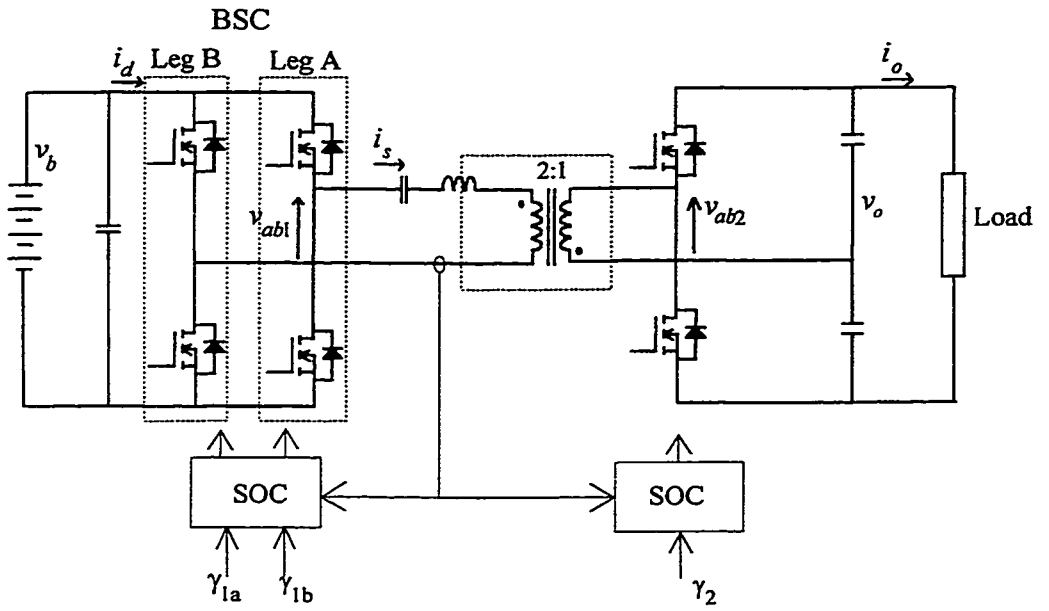


Fig. 5.1 ZVS bi-directional dc-to-dc converter operating in self-sustained oscillation mode.

The operation with zero voltage switching will be ensured by controlling the phase angle between the voltage impressed by the converters, v_{ab1} and v_{ab2}, in the series resonant circuit and the current through the series resonant circuit, i_s. The controller uses a constant amplitude sawtooth signal synchronized with the high frequency current i_s as proposed in Chapter 2. It will be demonstrated that by the proper selection of the control angles the converter operates in self-sustained oscillation mode.

5.2.1 Basic Operating Principles

In this sub-section. the range of the control angles for operation with ZVS will be identified and equations of the input current and power transfer will be derived. The following assumptions are made to simplified the analysis carried out in this sub-section:

(i) The input and output sides of the dc-to-dc converter of Fig. 5.1 are represented by voltage sources.

(ii) The resonant circuit is represented by a high frequency sinusoidal current source.

(iii) The snubber capacitors are small so that their impact on the circuit operation will be neglected.

Let us consider one leg of the converter of Fig. 5.1 and present it as shown in Fig. 5.2. In additions, let us assumed that the switch s_1 is initially conducting.

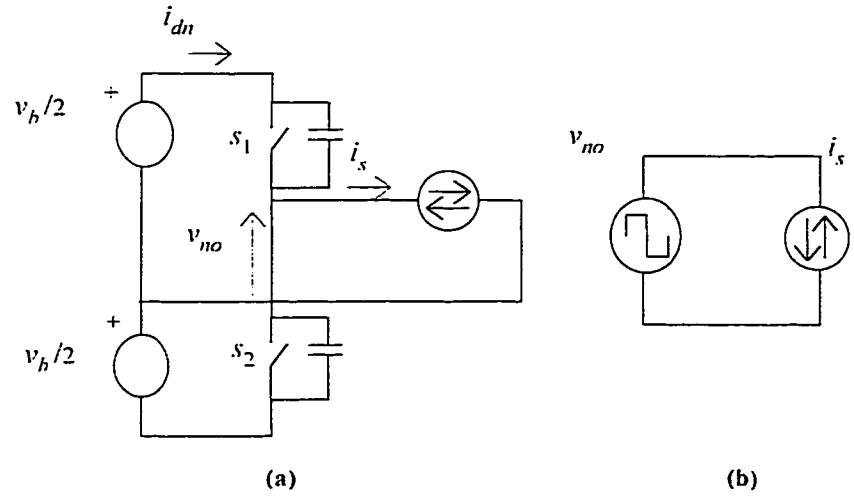


Fig. 5.2 ZVS half-bridge converter operating from a high frequency current source. The subscript n is used to identify the converter leg.

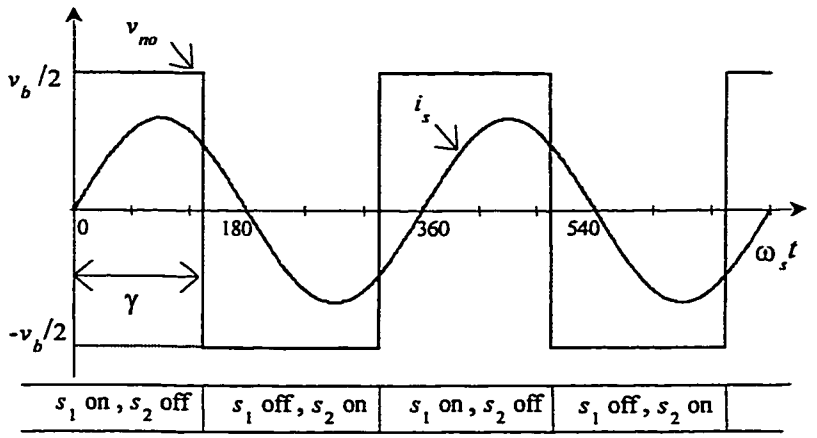


Fig. 5.3 Main waveforms of the half-bridge converter of Fig.5.2

At $\omega_s t = \gamma$, Fig. 5.3, the switch s_1 is turned off. At this instant the current i_s is greater than zero since $0<\gamma<180°$. Therefore, i_s has the right polarity to reset the snubber capacitors and provide ZVS for the turn on of the switch s_2. On the other hand, by changing the angle γ the power transfer from the dc input source (v_b) to the high frequency current source (series resonant circuit) can be adjusted, as can be seen from equation of the power transfer given below

$$p_n = -\frac{1}{\pi} v_b \hat{i}_s \cos(\gamma) \tag{5.1}$$

where p_n is the power transferred from source v_b to current source associated with i_s. It is concluded from (5.1) that if $0<\gamma<90°$ the power is transfer to v_b since p_n is negative, while if $90°<\gamma<180°$ the power is transferred from v_b to the high frequency current source. On the other hand, a variable that is usually of interest, especially when controlling any quantity at the input or output side, is the average value (over one switching period) of current i_{dn}. This current can be obtained by dividing (5.1) by v_b , which results:

$$\bar{i}_{dn} = -\frac{1}{\pi} \hat{i}_s \cos(\gamma) \tag{5.2}$$

where the bar over i_{dn} denotes the average value over one switching period.

When each leg of a full bridge inverter is switched with 50% duty cycle the equations (5.1) and (5.2) can be applied to obtain the inverter input current. In this case the full-bridge inverter is represented as two half-bridge converters. Each half-bridged converter is associated with one leg of the full-bridge inverter. For example, the current at the dc side of the full-bridge inverter of Fig. 5.1 can be found by adding the contribution of each inverter leg that is:

$$\bar{i}_d = -\frac{1}{\pi}\,\bar{i}_s \cos(\gamma_{1a}) - \frac{1}{\pi}\,\bar{i}_s \cos(\gamma_{1b}) \tag{5.3}$$

where γ_{1a} and γ_{1b} are the control angles associated with the legs A and B of the full-bridge inverter. In order to illustrate the bi-directional operation of the ZVS full-bridge inverter let us consider that $\gamma_{1a}=180^o$ and $0 < \gamma_{1b} < 180^o$, therefore from (5.3) it is found that:

$$0 < \bar{i}_d < \frac{2}{\pi}\bar{i}_s \ . \tag{5.4}$$

Similarly, if $\gamma_{1b}= 0$ and $0 < \gamma_{1a} < 180^o$ the inverter input current is:

$$-\frac{2}{\pi}\bar{i}_s < \bar{i}_d < 0 \tag{5.5}$$

Therefore, the power can flow bi-directionally since the voltage v_b is always positive.

Fig. 5.4 and Fig. 5.5 illustrate the two cases considered above. It is possible to see that the voltage v_{ab1} assumes a quasi-square pattern similar to the one produced by the conventional phase-shifted modulation method, and in addition the current i_s always crosses zero inside the non zero voltage pulse of v_{ab1}.

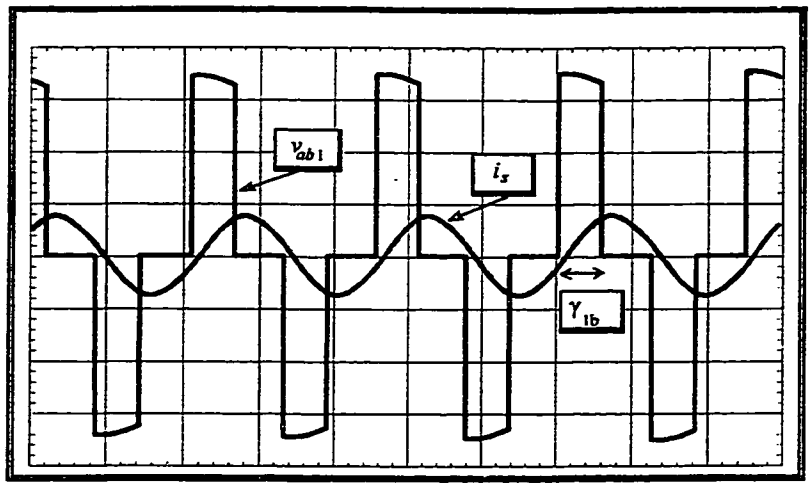


Fig. 5.4 Main waveforms of the BSC.
Operation with γ_{1b}=70° and γ_{1a}=175°

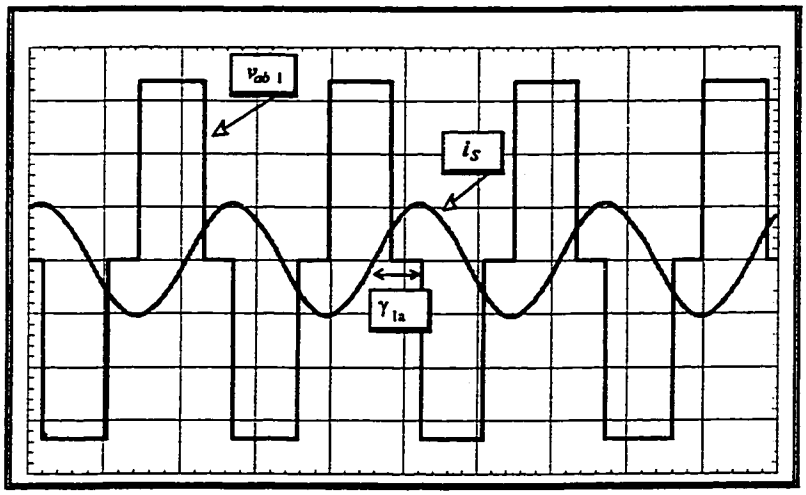


Fig. 5.5 Main waveforms of the BSC
Operation with γ_{1a}=60° and γ_{1b}=10°

The issue that arises at this point is regarding the existence of the high frequency current i_s. This issue is addressed in the next section where the stability of the self-sustained oscillation is investigated.

5.2.2 Stability of the Self-Sustained Oscillation

The high frequency ac current that circulates through the resonant circuit will be generated using the concept of self-sustained oscillation proposed in Chapter 2. In order

to investigate the existence and stability of the self-sustained oscillation, the converters of Fig. 5.1 are represented by a single nonlinearity. This representation is possible since these converters are connected in series and their output waveforms are generated from the same variable ($-i_s$). Therefore, the bidirectional dc-to-dc converter can be interpreted as a single-input/single-output system driven by a nonlinearity, as shown in Fig. 5.6 (a). As in the previous chapters, the describing function method will be used to investigate the stability of the self-sustained oscillation. According to this method, the static nonlinear characteristic of the system is represented by a gain dependent upon on the input signal ($-i_s$). By replacing the nonlinearity by its associated describing function, the characteristic equation of the system becomes:

$$1 + N_e(.)G(j\omega) = 0 \tag{5.6}$$

where $G(j\omega)$ is the transfer function associated with the resonant circuit, that is given by:

$$G(s)\big|_{s=j\omega} = \frac{sC_s}{s^2 L_s C_s + sC_s r + 1} \tag{5.7}$$

The resistor r in (5.7) represents the overall losses in the power circuit. The describing function $N_e(.)$ can be obtained by adding the describing functions associated with each leg of the converter of Fig.5.1, where these describing functions are similar to (2.1). Thereby, the $N_e(.)$ assumes the following form:

$$N_e = \frac{2}{\pi \hat{i}_s}\left(v_h(\cos(\gamma_{1a}) - j\sin(\gamma_{1a})) + v_h(\cos(\gamma_{1b}) - j\sin(\gamma_{1b})) + 2v_o(\cos(\gamma_2) - j\sin(\gamma_2))\right) \tag{5.8}$$

Let us assume that there exist a self-sustained oscillation of amplitude $\hat{i}_s$ and frequency ω_s, then this oscillation must satisfy (5.6). The solution of (5.6) represents the intersection point of the loci plotted in Fig. 5.6 (b). The stability of the self-sustained

oscillation can be investigated by applying a slight disturbance in the amplitude of $\bar{i}_x$ at the intersection point. By increasing $\bar{i}_x$ the system operating point moves outside the locus of $G(j\omega)$. Since the new operating point is not encircled by the locus of $G(j\omega)$, according to the Nyquist criterion, in this operating point, the system behaves as a stable system, and the current $\bar{i}_x$ decreases toward the intersection point. A similar argument can be used when $\bar{i}_x$ is decreased. Therefore, the converter will operate a stable self-sustained oscillation above the frequency ω_o if the lumped nonlinearity $N_e(.)$ has a describing function with an angle smaller than -90° and greater than -180°.

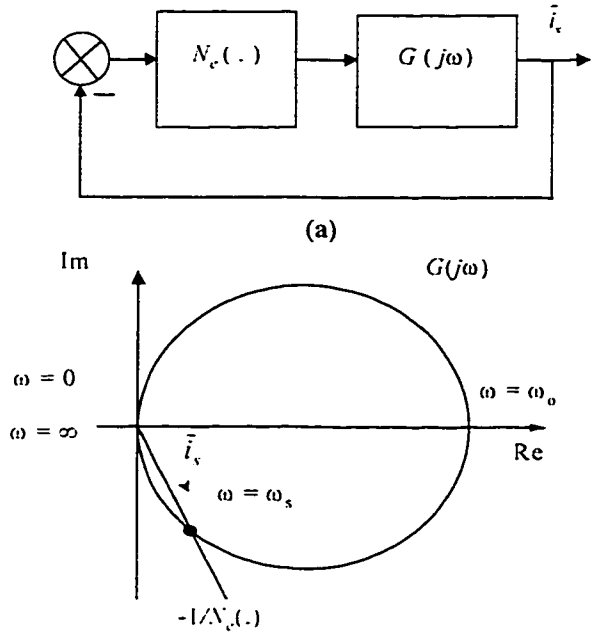


Fig. 5.6 Detection of the self-sustained oscillation.

(a)Feedback system interpretation for the converter in self-sustained oscillation. (b) Nyquist plot of the resonant circuit sinusoidal transfer function and the plot of the negative inverse of the describing function.

5.2.3 Simulation and experimental results

This section demonstrates the feasibility of the proposed bidirectional dc-to-dc converter by means of simulation and experimental results. It is worth mentioning that in

order to implement the proposed converter the amplitude of the current i_s must be regulated. The inverter at the left side of Fig.5.1 can be used for this purpose while the converter at the right can be used, for instance, can regulate the output voltage.

The simulated and implemented circuit operates from a 48V battery and it produces an isolated 100V output dc bus. Fig. 5.7 and Fig. 5.8 show simulation and experimental results when power is been transferred from the battery to the output stage. According to the analysis of the previous sections the control angle γ_2 should be greater than zero and smaller than 90°. From Fig. 5.7 and Fig. 5.8 it is possible to see that the control angle γ_2 is closed to zero. On the other hand, Fig. 5.9 and Fig. 5.10 demonstrate the operation when power is transferred from the output to the battery. The control angle in this case should be $90° < \gamma_2 < 180°$ and it is found from simulation and experimentally that the γ_2 is close to 180°. In addition, the current i_s always lags the voltage v_{ab2} and it lags v_{ab1} while crossing zero inside non zero voltage pulse, therefore, providing a way to reset the snubber capacitors and achieve ZVS. The simulation and experimental results presented are in good agreement. The differences found between simulation and experimental results are the high frequency oscillations with result from the interaction between the power circuit capacitors of the inductance associated with the wires used to interconnect the components in the experimental setup which are not included in the simulation.

The next section extends the concepts developed in this and previous sections for operation with ac output voltages.

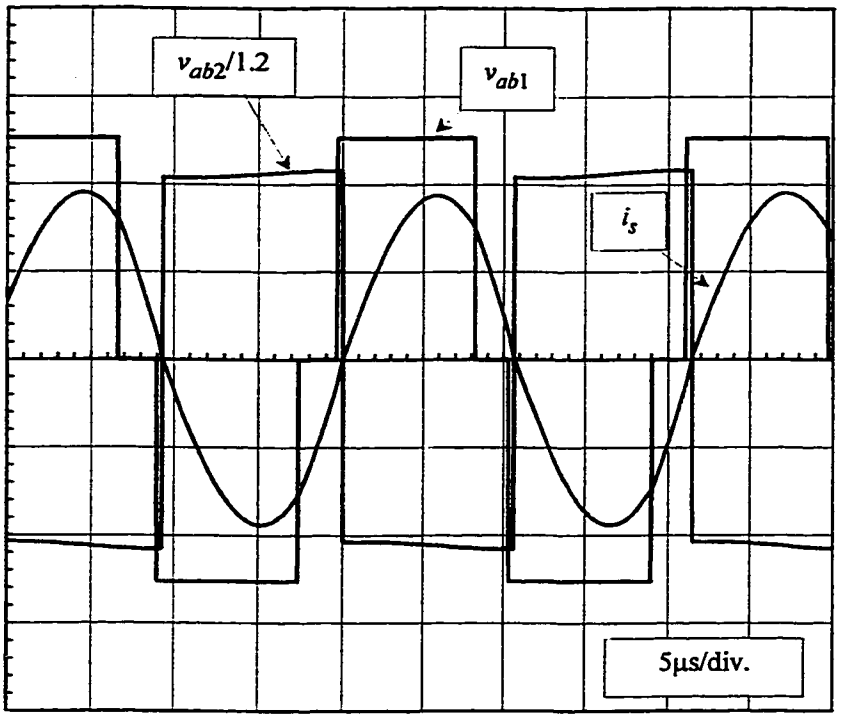


Fig. 5.7 Simulation results of the bidirectional dc-to-dc converter. P_o>0

P_o=250W, v_b=50 , v_o=100V. Vertical scales: Voltages: 20V/div., Current: 5A/div. Horizontal Scales: 5μs/div. L_s=55μH, C_s=250nF, n_1/n_2=1.2.

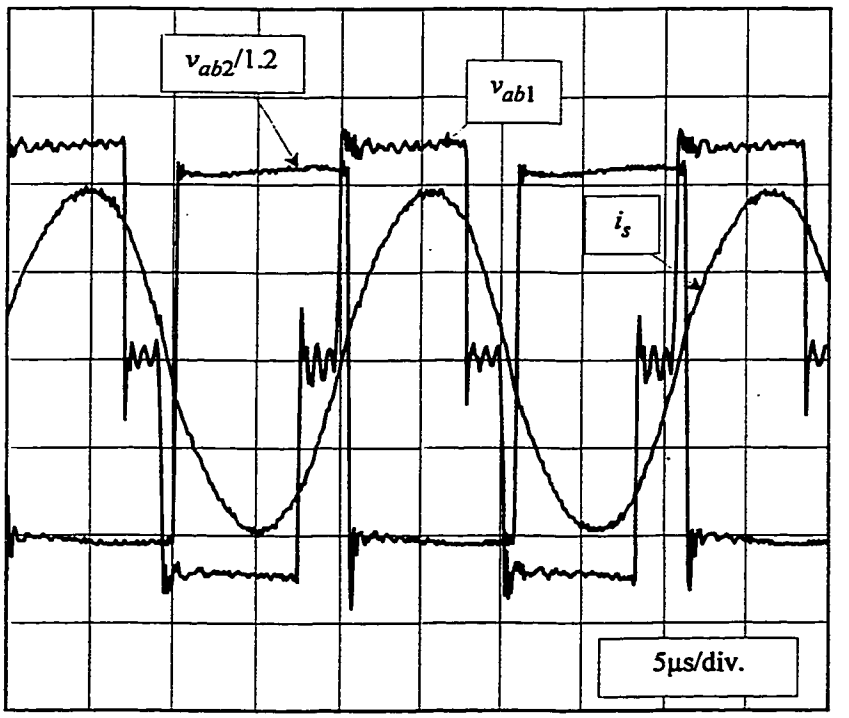


Fig. 5.8 Experimental results of the bidirectional dc-to-dc converter. P_o>0.

P_o=250W, v_b=50 , v_o=100V. Vertical scales: Voltages: 20V/div., Current: 5A/div. Horizontal Scales: 5μs/div. L_s=55μH, C_s=250nF, n_1/n_2=1.2.

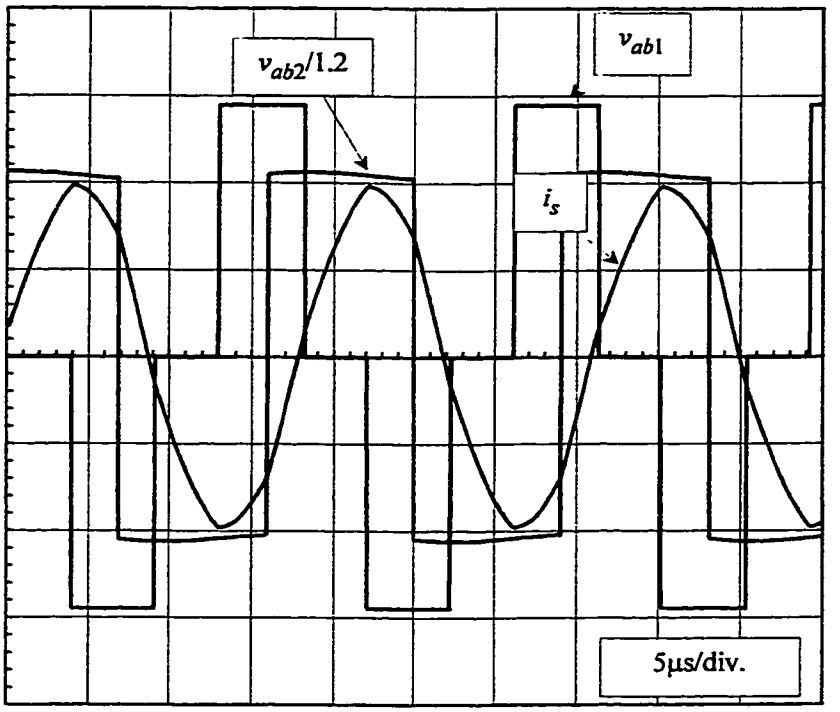


Fig. 5.9 Simulation results of the bidirectional dc-to-dc converter. P_o<0

P_o=-200W, v_b=57 , v_o=100V. Vertical scales: Voltages: 20V/div., Current: 5A/div. Horizontal Scales: 5μs/div. L_s=55μH, C_s=250nF, n_1/n_2=1.2.

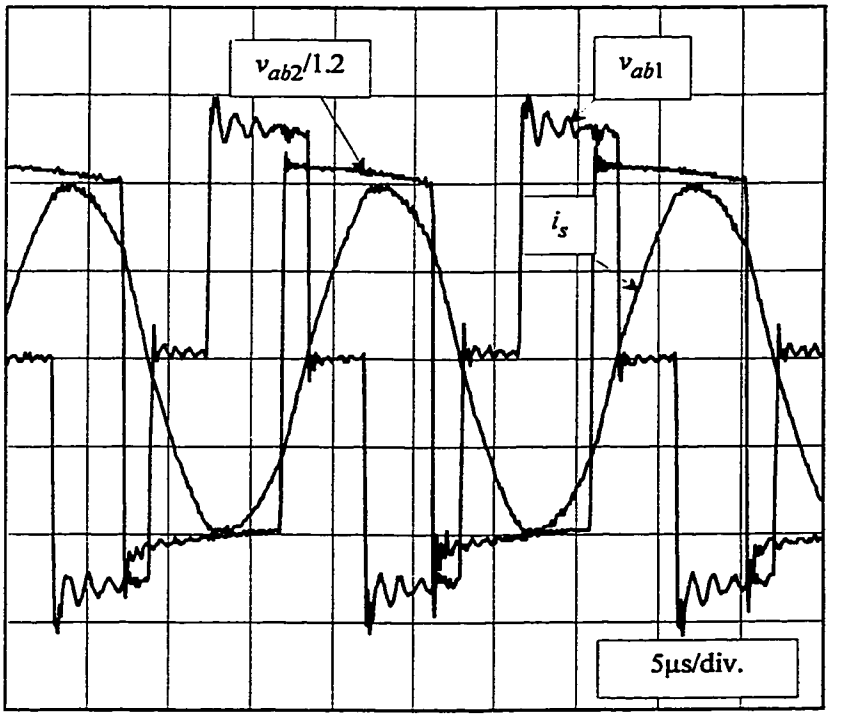


Fig. 5.10 Experimental results of the bidirectional dc-to-dc converter. P_o<0.

P_o=-200W, v_b=57 , v_o=100V. Vertical scales: Voltages: 20V/div., Current: 5A/div. Horizontal Scales: 5μs/div. L_s=55μH, C_s=250nF, n_1/n_2=1.2.

5. 3 ZERO VOLTAGE SWITCHING DC-TO-AC CONVERTER

Isolated dc-to-ac converters are often required in UPS to step-up the battery voltage the value required to synthesize the output voltage and to provide galvanic isolation between the battery and the output.

It will be demonstrated in this section that by replacing the switches of the leg at the right side of the dc-to-dc converter of Fig. 5.1 by bidirectional switches the resultant converter is capable to synthesize ac output voltages. Fig. 5.11 shows an isolated dc-to-ac converter where the BSC is implemented with a full bridge converter and OSC with a half-bridge cycloconverter.

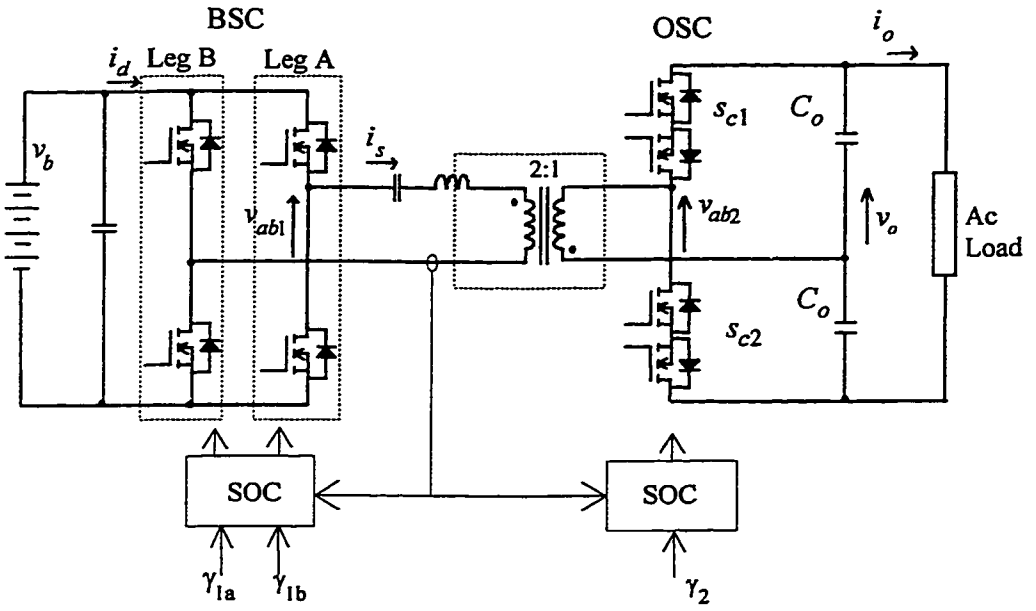


Fig. 5.11 Power circuit of the proposed series resonant based dc-to-ac converter.

The dc-ac converter of Fig. 5.11 operates as follows: Let us assume that the output voltage v_o is positive. When the switch s_{c1} is closed, the voltage across the high frequency terminals of the output side converter (OSC) v_{ab2} is positive with an amplitude equal to $v_o/2$. Similarly, when the switch s_{c2} is closed, the voltage v_{ab2} is equal to $-v_o/2$.

Therefore, if the switches s_{c1} and s_{c2} are switched in a complementary manner, a square voltage waveform is produced across the high frequency transformer. The operation with positive output voltage is illustrated in Fig. 5.12 (a). This figures indicates that two transistor of the OSC are kept on and the other two transistors are switched in a complementary manner using the gate signals v_{gc1a} and v_{gc2a}. It is also shown in Fig. 5.12 (a) the voltage v_{ab2}, the current i_{o1}, and the control angle γ_2. If the control angle γ_2 is greater then zero and smaller than 180° the current i_s lags the voltage v_{ab2}. In addition, the average value of the current sent by the OSC to the output capacitor and load over switching period can be found as:

$$\bar{i}_{o1} = \frac{2}{\pi}\bar{i}_s \cos(\gamma_2) \qquad \text{for } v_o>0. \tag{5.9}$$

Similarly, Fig. 5.12 (b) illustrates the operation with negative output voltage. The main difference from the operation with positive output voltage is found in the gate signals. When the output voltage is negative the gate signals v_{gc1b} and v_{gc2b} are complementary and as results the average value of the current i_{o1} over switching period becomes:

$$\bar{i}_{o1} = -\frac{2}{\pi}\bar{i}_s \cos(\gamma_2) \qquad \text{for } v_o<0. \tag{5.10}$$

By combining the equations (5.9) and (5.10) using the sign function results

$$\bar{i}_{o1} = sign(v_o)\frac{2}{\pi}\bar{i}_s \cos(\gamma_2). \tag{5.11}$$

(5.11) can be used to obtain the equation that describes the dynamic behavior of the output voltage. By applying Kirchhoff's current law to the node 1, Fig. 5.12, it found that the variation of the output voltage given by:

$$\frac{C_o}{2}\frac{dv_o}{dt} = sign(v_o)\frac{2}{\pi}\hat{i}_s \cos(\gamma_2) - i_{load}\,. \tag{5.12}$$

Taking into account the control angle γ_2 can be assume any value greater zero and smaller than 180°, and assuming that the amplitude of the current i_s is constant, the output voltage can be controlled if the following inequality is satisfied:

$$\hat{i}_s > \frac{\pi}{2}|i_{load}|\,. \tag{5. 13}$$

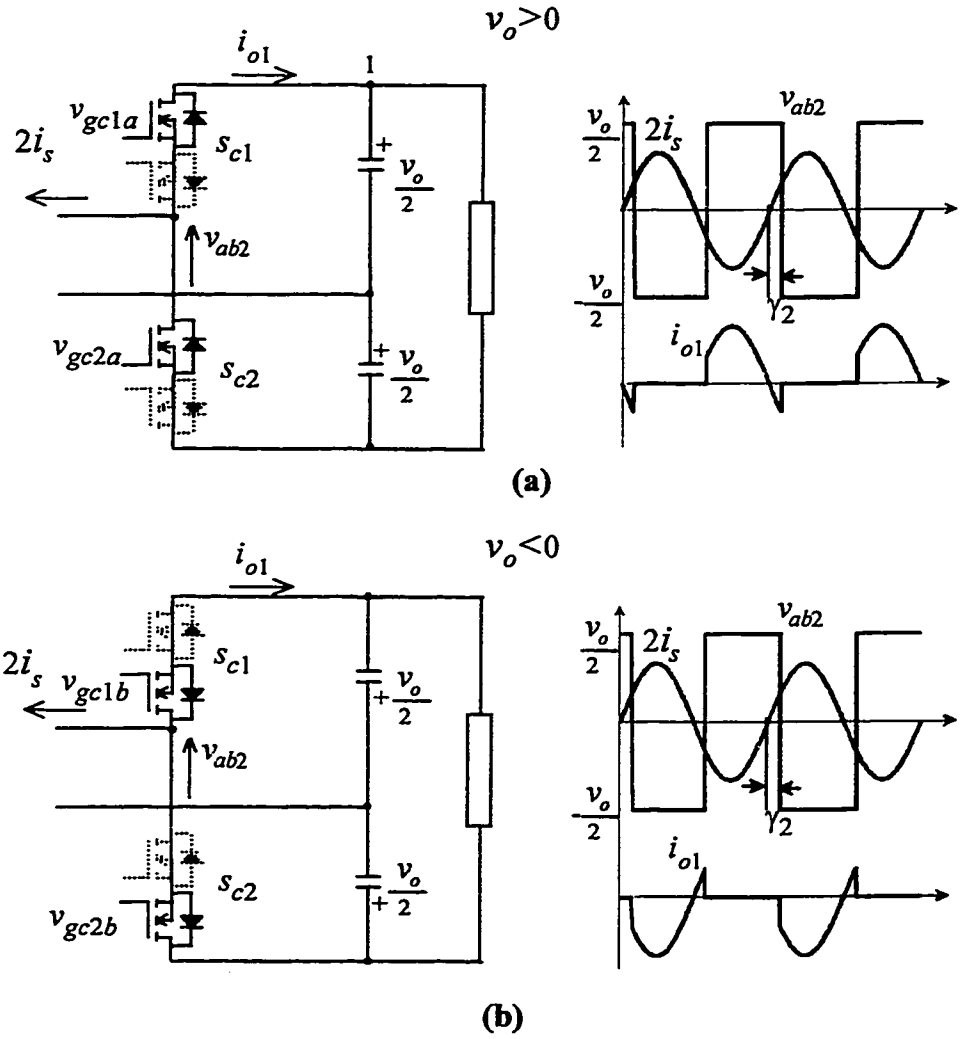


Fig. 5.12 Simplified representation of the OSC. (a) v_o>0. (b)v_o<0.

In order to validate the concepts presented above a experimental setup was implemented. The amplitude of the current i_s was kept constant by the appropriated control of the angles γ_{1a} and γ_{1b} of the BSC and the control angle γ_2 was used to control the output voltage. The experimental setup operates from a 48 V battery and produces a sinusoidal output voltage of 100V peak at 60Hz. Fig. 5.13 shows the output voltage v_o and the voltage v_{ab2}. The amplitude of v_{ab2} is half of the output voltage since it is measured from the capacitor center tap to the center of the cycloconverter leg. It is also shown in this figure the signal associated with the sign of v_o, which is required to change the sign of the gain of output voltage controller and to selected the gate signals of the cycloconverter. On the other hand, Fig. 5.14 shows a zoom of the waveforms of Fig. 5.13. It is also shown in Fig. 5.14 the current i_s. It is possible to see that the current i_s lags the voltage v_{ab2} in more the 90° which indicates that power is been transferred from the battery to the output load.

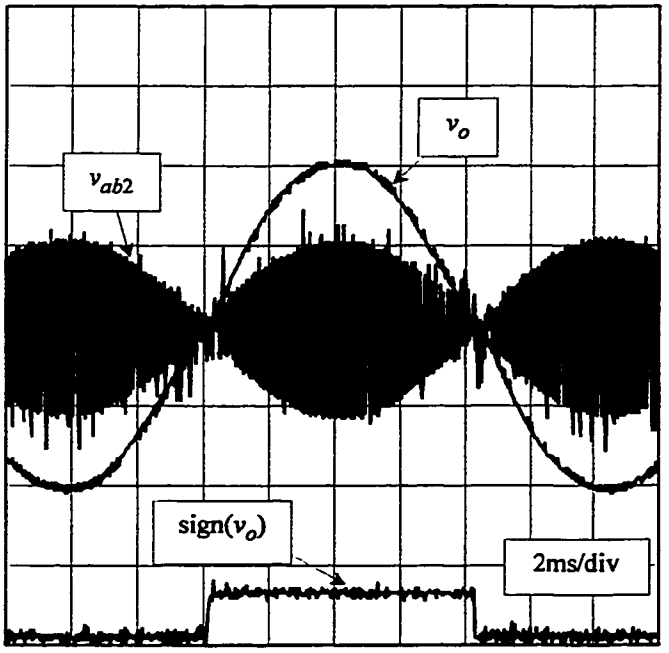


Fig. 5.13 Experimental results of the isolated dc-to-ac converter.
P_o=210W, v_b=50 V, v_o=70.7Vrms. Vertical scale: 50V/div. Horizontal scale: 2m/div. L_s=55μH, C_s=250nF, n_1/n_2=1.2.

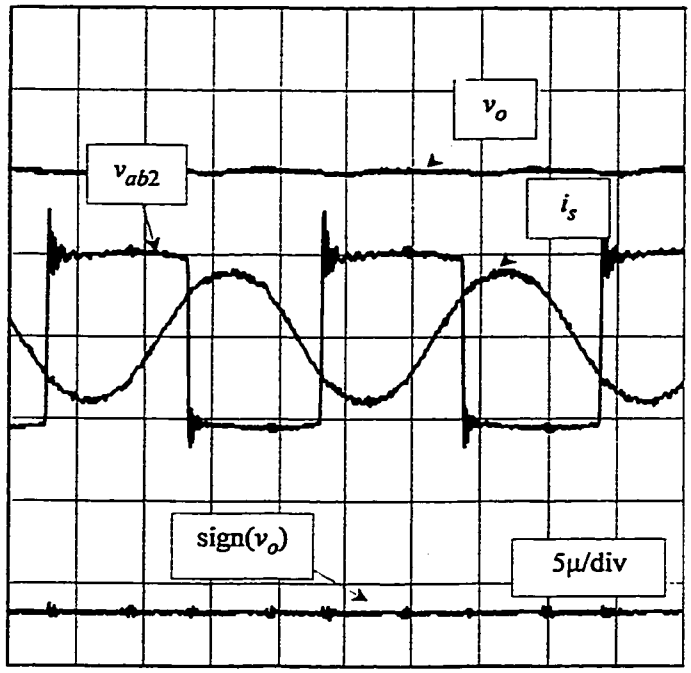


Fig. 5.14 Experimental results of the isolated dc-to-ac converter.
P_o=210W, v_b=50 V, v_o=70.7Vrms. Vertical scales: 50V/div.and 25A/div. Horizontal scale:5μs/div.
L_s=55μH, C_s=250nF, n_1/n_2=1.2.

In the next section, the concepts developed so far are extended to a fully isolated ZVS UPS topology.

5. 4 ZERO VOLTAGE SWITCHING UPS TOPOLOGY

Fig. 5.15 shows an UPS topology derived from the concepts developed in this chapter. This UPS is comprised of three converters, a high frequency interface and input and output filters. The input and output filters are used to attenuate the high frequency current components at the low frequency side (or dc side) of the converters of the UPS. For example, the capacitor C_{o1} and C_{o2} and the low pass filter C_b and L_b are used to attenuate the high frequency voltage and current components of v_o and i_b respectively. In addition, the parameters of the filter at the input of the line side converter (LSC) are selected so that the high frequency current components generated by LSC are

significantly attenuated, and the low frequency voltage components resulted from rectification of the incoming ac line are not attenuated. As a result, it is possible to operate with high input power factor, and to meet the requirements imposed by international regulatory agencies regarding the amplitude of the low order current harmonic injected by equipment connected with the utility supply system. On the other hand, a high frequency interface which consists of passive components is used to provide galvanic isolation among the terminals of the UPS and the required impedance to interface the LSC, battery side converter (BSC) and the output side converter (OSC). The inductor L_s and capacitor C_s form a resonant branch that operates above its resonant frequency, and as a result, provides the required impedance to interface the LSC, BSC and OSC. All the converters of the UPS operate at high frequency, usually at hundreds of kHz, and their operating principle are descried below.

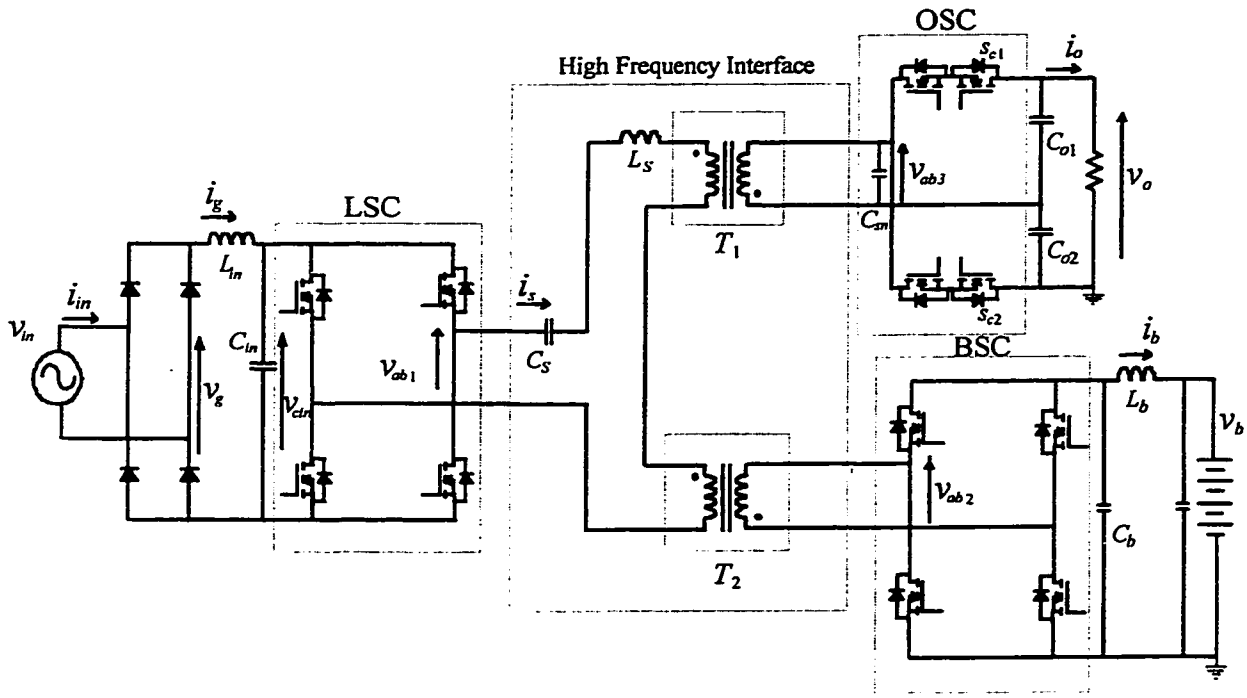


Fig. 5.15 Power circuit of the proposed series resonant based UPS.

5.4.1 Converters Operation

The LSC is used to interface the incoming input ac supply and the high frequency current link. A full bridge inverter was selected for the implementation of the LSC which makes possible the operation with phase shift modulation. In order to operate with ZVS in phase shift modulation, the inverter output current should cross zero inside the non-zero inverter output voltage pulse. This requirement can be achieved by adopting the self-sustained oscillation controller proposed in Chapter 2. The angle γ_{1a} is kept constant at a value close to 180°. This ensures that the current crosses zero inside the output voltage pulse. On the other hand, the angle γ_{1b} is used to control the pulse width of the quasi-square waveform produced at the ac terminals of the LSC. Therefore, for a given current i_s by increasing angle γ_{1b} towards 180° the power transfer from the input ac supply to the resonant circuit increases.

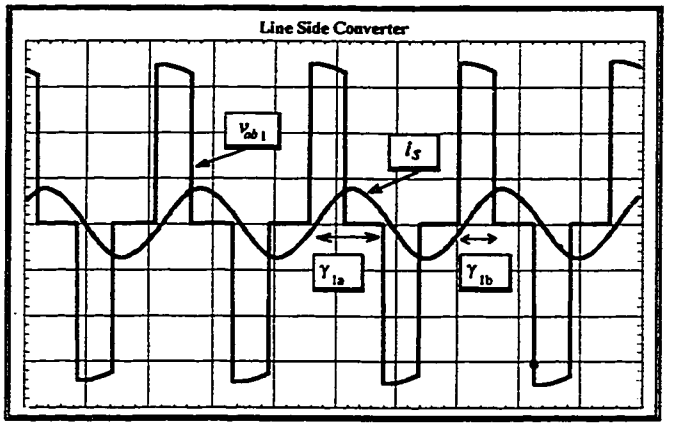


Fig. 5.16 Main waveforms of the line side converter during the line operating mode.

On the other hand, the BSC and the OSC operate as described in sections 5.2 and 5.3.

5.4.2 Stability of the Self-Sustained Oscillation

The high frequency ac current that circulates through the resonant circuit will be generated using the concept of self-sustained oscillation. In order to investigate the existence and stability of the self-sustained oscillation, the LSC, BSC and OSC are represented by a single nonlinearity. This representation is possible since these converters are connected in series and their output waveforms are generated from the same variable ($-i_s$). In this way, the UPS can be interpreted as a single-input/single-output system driven by a nonlinearity which represents the series connection of the LSC, BSC and OSC, as shown in Fig. 5.6 (a). The intersection point of the loci in Fig. 5.6 (b) can be found analytically by solving (5.6). Equation (5.6) can be represented by two non-linear equations, one of them is associated with the real part of (5.6) and the other with the imaginary part, that are:

$$\mathrm{Re}(N_e(.)) = -r \tag{5.14}$$

and

$$\mathrm{Im}[N_e(.)] = \frac{(1-\alpha^2)}{\alpha}\omega_o L_s \tag{5.15}$$

where α is the ratio between the switching frequency ω_s and the resonant frequency ω_o. The real and imaginary part of describing function $N_e(.)$ are given by:

$$\mathrm{Re}(N_e(.)) = \frac{2}{\pi \hat{i}_s}\left\{v_g\left[\cos(\gamma_{1a})+\cos(\gamma_{1b})\right]+v_b\left[\cos(\gamma_{2a})+\cos(\gamma_{2b})\right]+2|v_o|\cos(\gamma_3)\right. \tag{5.16}$$

$$\mathrm{Im}(N_e(.)) = \frac{-2}{\pi \hat{i}_s}\left\{v_g\left[\sin(\gamma_{1a})+\sin(\gamma_{1b})\right]+v_b\left[\sin(\gamma_{2a})+\sin(\gamma_{2b})\right]+2|v_o|\sin(\gamma_3)\right. \tag{5.17}$$

where the turns ratio of the transformers T_1 and T_2 where made 2:1 and 1:1 respectively.

By solving (5.6) for α greater than one results in a possible operating point of the converter. In addition, taking into account that for operation in self-sustained operation mode the angle of $N_e(.)$ must be smaller than -90° and greater than -180° from (5.16) and (5.17) it is found that:

$$v_g[\cos(\gamma_{1a}) + \cos(\gamma_{1b})] + v_b[\cos(\gamma_{2a}) + \cos(\gamma_{2b})] + 2|v_o|\cos(\gamma_3) \le 0 \qquad (5.18)$$

$$v_g[\sin(\gamma_{1a}) + \sin(\gamma_{1b})] + v_b[\sin(\gamma_{2a}) + \sin(\gamma_{2b})] + 2|v_o|\sin(\gamma_3) \ge 0 \qquad (5.19)$$

The left side of (5.18) becomes zero when resonant circuit has no losses, and this equation can also be obtained from the input-output power balance of the converter.

5.4.3 Control Angles and Switching Frequency

In this section the control angles and the switching frequency required to operate with a given input and output power profile will be derived.

Taking into account that the UPS of Fig. 5.15 does not have any large energy storage element, and by assuming that the resonant circuit is loss-less and operates in sinusoidal steady state, the sum of the instantaneous power absorbed by the converters equals the power delivered by the converters. As a result, the input-output power balance can be expressed as:

$$p_{in} = p_o + p_b \qquad (5.20)$$

where p_{in} is the power absorbed by the LSC from the ac line, and p_o and p_b are the power sent to the output load and the battery respectively. For the UPS of Fig. 5.15 the power at the input and output are given by:

$$p_{in} = v_g i_g, \quad p_b = v_b i_b, \quad p_o = v_o i_o. \qquad (5.21)$$

The voltages v_g, v_b, and v_o as well as the power p_{in}, p_b, and p_o are well known quantities in given implementation. Therefore, the currents i_g, i_b, and i_o can be easily found by using (5.15). On the other hand, by considering the operation of the LSC, BSC and OSC as explained in sub-section 5.4.1, and by neglecting the effect of the input and output filters, since switching frequency is very high, the currents i_g, i_b, and i_o can also be expressed as:

$$i_g = -\frac{\bar{i}_s}{\pi}(\cos(\gamma_{1a}) + \cos(\gamma_{1b})) \tag{5.22}$$

$$i_b = \frac{\bar{i}_s}{\pi}(\cos(\gamma_{2a}) + \cos(\gamma_{2b})) \tag{5.23}$$

$$i_o = \frac{2\bar{i}_s}{\pi}\mathrm{sgn}(v_o)\cos(\gamma_3) \tag{5.24}$$

It is concluded from (5.22)-(5.24) that for proper operation of the converter the amplitude of the current i_s must satisfy the following inequality:

$$\bar{i}_s \geq \max\left[\frac{\pi i_g}{2}, \frac{\pi|i_b|}{2}, \frac{\pi|i_o|}{2}\right] \tag{5.25}$$

The equation (5.25) can be used to establish the amplitude of the resonant circuit current i_s. Once the amplitude of the current i_s is defined, the control angles of the LSC, BSC, and OSC can be found using (5.22)-(5.24). For example, let us assume that the parameters of Table 5.1 are known. By making the amplitude of the current i_s equal to $(P_{in}\pi)/(2v_{gm})$, the control angles required to operate with the given voltage and power can found. Fig. 5.17 shows the control angle during the backup mode with and inductive output load. It is also shown in this figure how the switching frequency changes along the output voltage cycle for three values of $\omega_o L_{s2}$.

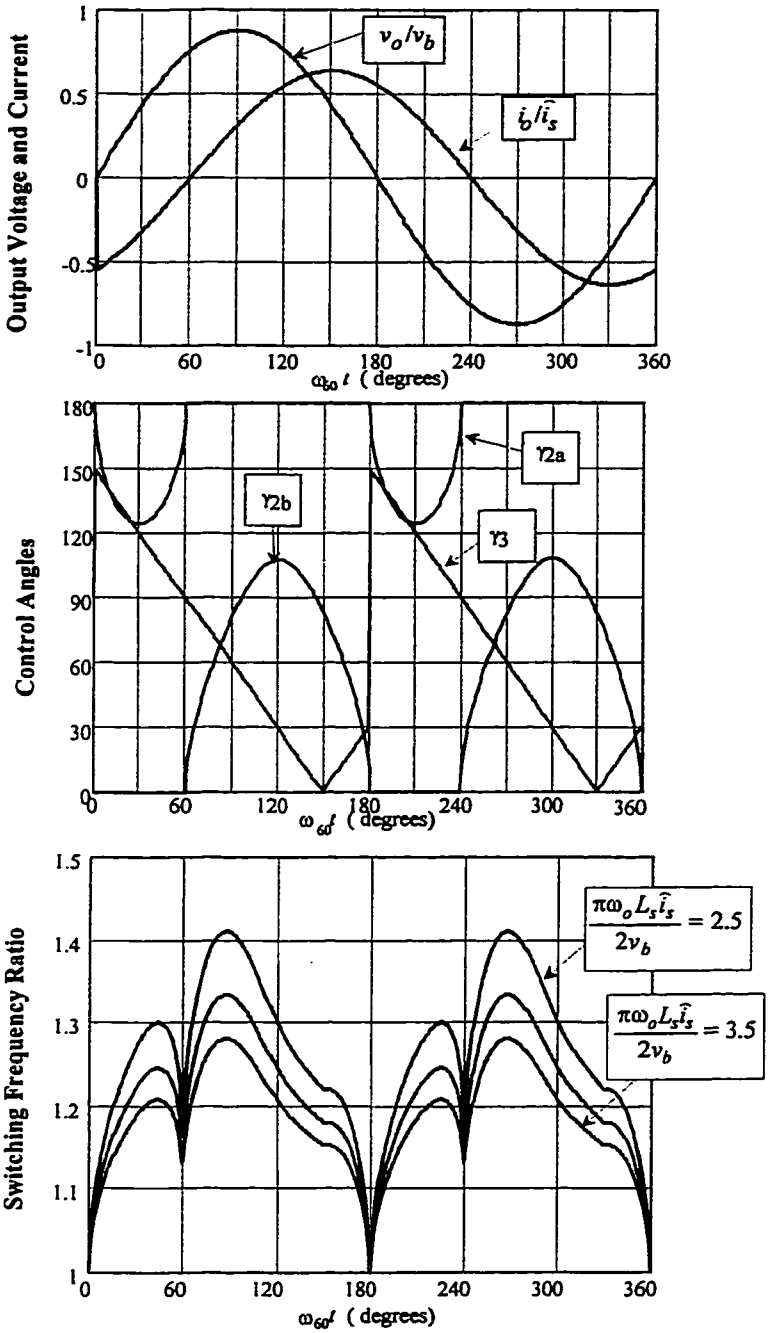


Fig. 5.17 Analytical results for the backup mode of operation

Top: Output voltage and current for operation with a inductive output load along one output voltage cycle; **Middle**: Control Angles of the BSC and OSC; Bottom: Switching frequency ratio for different values of the power circuit parameters.

It is concluded from Fig. 5.17 that for a given application by increasing the value of $\omega_o L_s$, the range of switching frequency is reduced. However, by increasing $\omega_o L_s$ the

rating of the resonant circuit also increases. Therefore, a trade-off between switching frequency range and the volt-ampere rating of the resonant components must be considered when selecting $\omega_o L_s$.

5.4.4 Experimental Results

In order to validate the concepts developed in this Section a prototype of the proposed UPS has been implemented. The main parameters the implemented UPS are given in Table 5.1 and a detailed description of the power circuit is given in Appendix 5.

TABLE 5.1 UPS MAIN PARAMETERS

Rated Power	400 W
Input Voltage	120 V
Output Voltage	100 V (peak)
Battery Voltage	48 V
Resonant Inductor L_S	125 μH
Resonant Capacitor C_S	60 nF
*Transformers turn ratio :	
T_1	1:2.6
T_2	1:1.25

* See Appendix 5.

For the proper operation of the UPS, the amplitude of the current i_s must be selected so that the inequality (5.25) is satisfied. By using power and incoming voltage ac voltage value of Table 5.1 the amplitude of current i_s can be found as follows:

$$\hat{i}_s = \frac{\pi P_m}{2\hat{v}_{gm}} = \frac{\pi 800}{2\sqrt{2}120} = 7.4 \text{ A} . \tag{5.26}$$

In the implemented setup the amplitude of the current i_s is regulated at 8 A. The first set of measurements carried out aimed to determine if the UPS operates as predicted analytically. To demonstrate that, Table 5.2 summarizes the operating conditions obtained experimentally. It was found that the proposes UPS topology allows the synthesis of high quality output waveforms while charging the battery and drawing from the incoming ac line a current with low total harmonic distortion as illustrated in Fig. 5.18.

TABLE 5.2 OPERATING CONDITIONS.

v_{in}	v_o	v_b	P_{in}	P_o	P_b
120 V	100 V (peak)	55 V	450 W	319 W	50 W

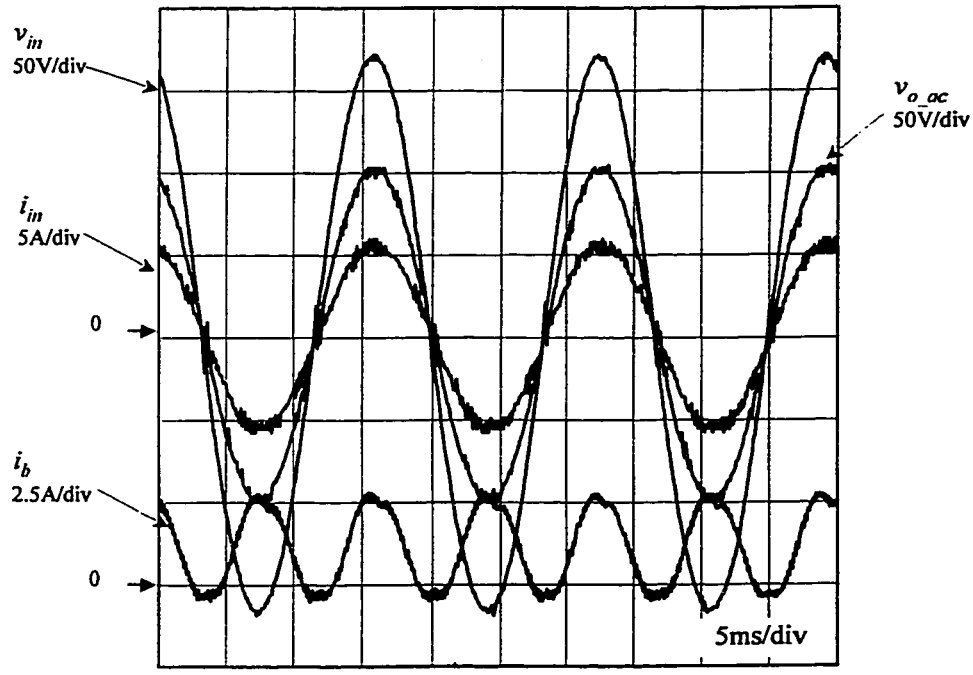


Fig. 5.18 Experimental Results. Line operating mode.
Operating conditions given in Table 5.2.

On the other hand, Fig. 5.19 to Fig. 5.21 show typical waveforms of the current and voltage at the high frequency terminals of the LSC, OSC, and BSC. Fig. 5.19 shows that voltage v_{ab1} has a high frequency quasi-square waveform whose amplitude follows the absolute value of the low frequency sine waveform which results from the rectification of the incoming ac line. It is also shown in this figure that the current i_s lags the voltage v_{ab1} and it crosses zero inside of the non-zero voltage pulse of v_{ab1} at the different instant along the incoming ac voltage cycle.

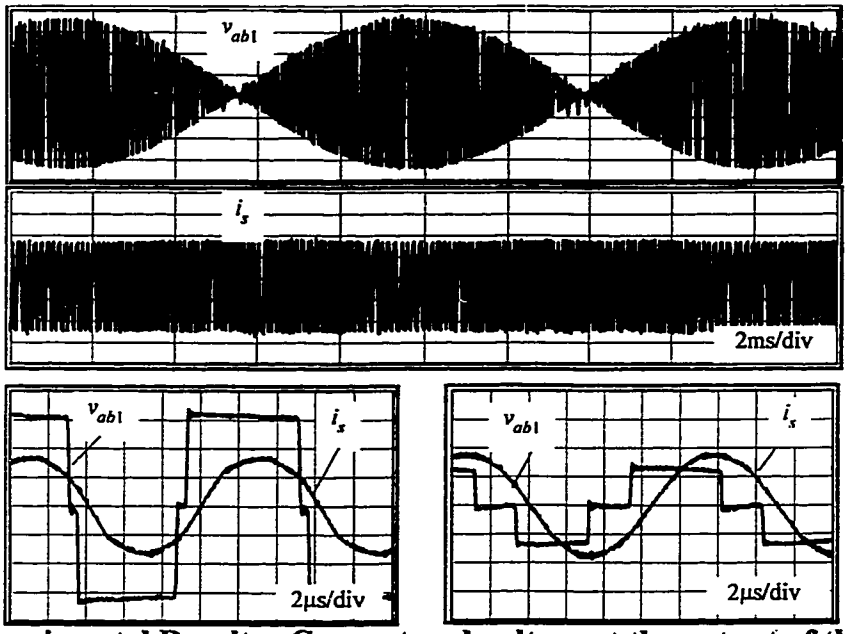


Fig. 5.19 Experimental Results. Current and voltage at the output of the LSC.
P_o=319 W and P_b=50 W. Vertical scales: 50V/div, and current 5.0 A/div. Horizontal scales: 2ms/div and 2μs/div.

Similarly, Fig. 5.20 shows the voltage across the high frequency terminals of the OSC, v_{ab3}, and the current i_s. This figure shows that the voltage v_{ab3} has a square waveform with amplitude equal to half the output voltage, v_{o_ac}. In addition, this figure shows that the current i_s lags the voltage v_{ab3} in more than 90° indicating that power is been transferred from the resonant circuit to the output side.

Typical waveforms of the voltage across the high frequency terminals of the BSC are shown in Fig. 5.21. The voltage v_{ab3} has a quasi-square waveform, which results from the operation with VFPSM. During the line operating mode, when the battery is been charged, the current i_s lags voltage v_{ab3} in more than 90° as illustrated in Fig. 5.21 (a). However, during the backup mode the i_s lags voltage v_{ab3} in less than 90°, Fig. 5.21 (b), since power is transferred from the battery to the output.

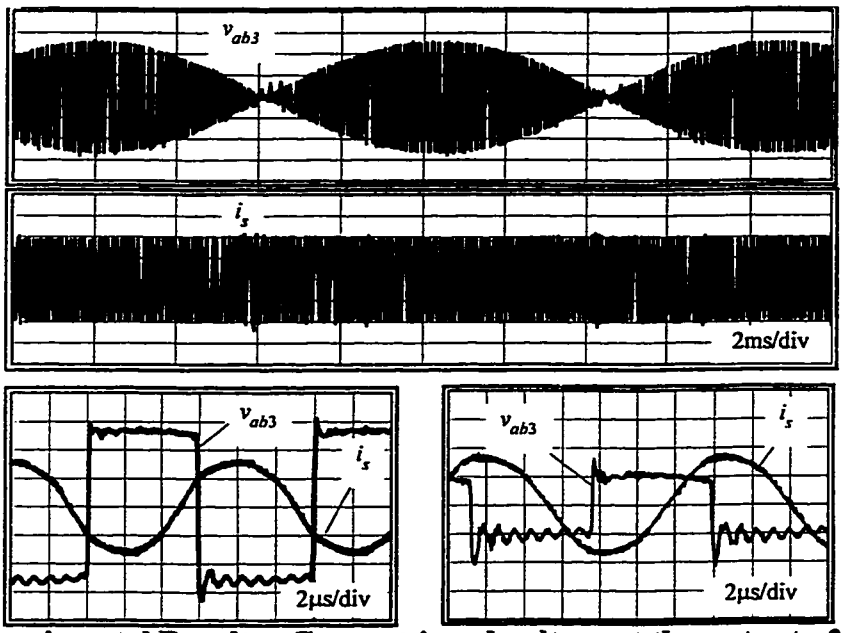
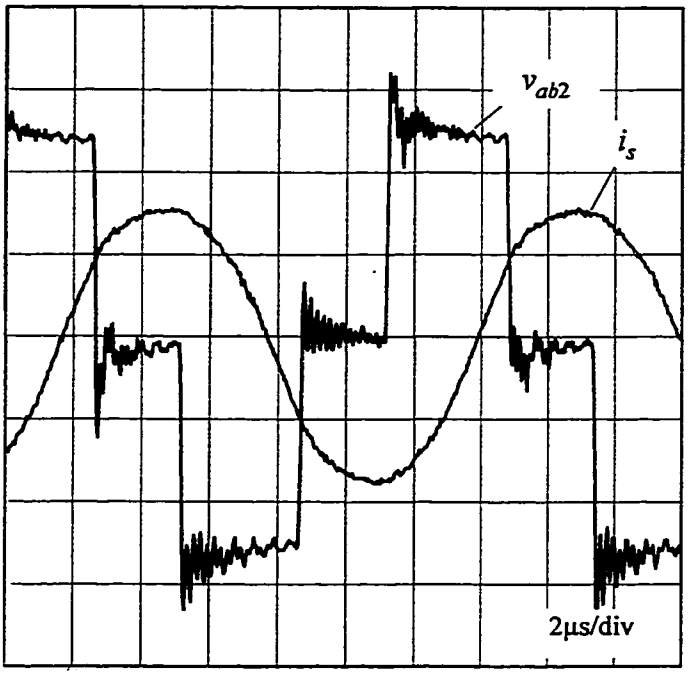
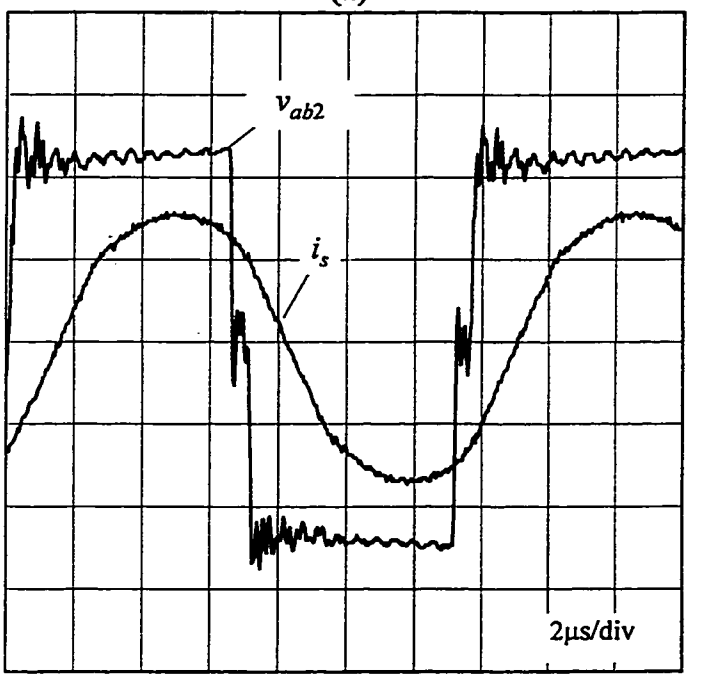


Fig. 5.20 Experimental Results. Current i_s and voltage at the output of the OSC.
P_o=319 W and P_b=50 W. Vertical scales: 20V/div, and current 5.0 A/div. Horizontal scales: 2ms/div and 2μs/div.



(a)



(b)

Fig. 5.21 Experimental Results. Current i_s and voltage at the output of the BSC.
(a) Line Operating mode. (b) Backup mode. Vertical scales: 20V/div, and current 5.0 A/div. Horizontal scales: 2ms/div and 2μs/div.

Finally, the static and the dynamic performances of the UPS were obtained from the implemented setup. The UPS overall efficiency, input power factor, and THD of the input current are summarized in Fig. 5.22. The input power factor is close to unity and the THD of the input current is close to 10% from half of full load to full load. The overall efficiency of the UPS is 82% during the line operating mode and 83.5% during the backup mode. The efficiency is slightly lower during the line operating mode due to losses associated with the input diode rectifier. Among the losses, the conduction losses are predominant, since the current i_s circulates through all converters and its amplitude is kept constant along the entire input (output) cycle. On the other hand, Fig. 5.23 illustrates the transient response of the UPS due a step change in the load. It is seen that the voltage v_{o_ac} is virtually undisturbed by the load change.

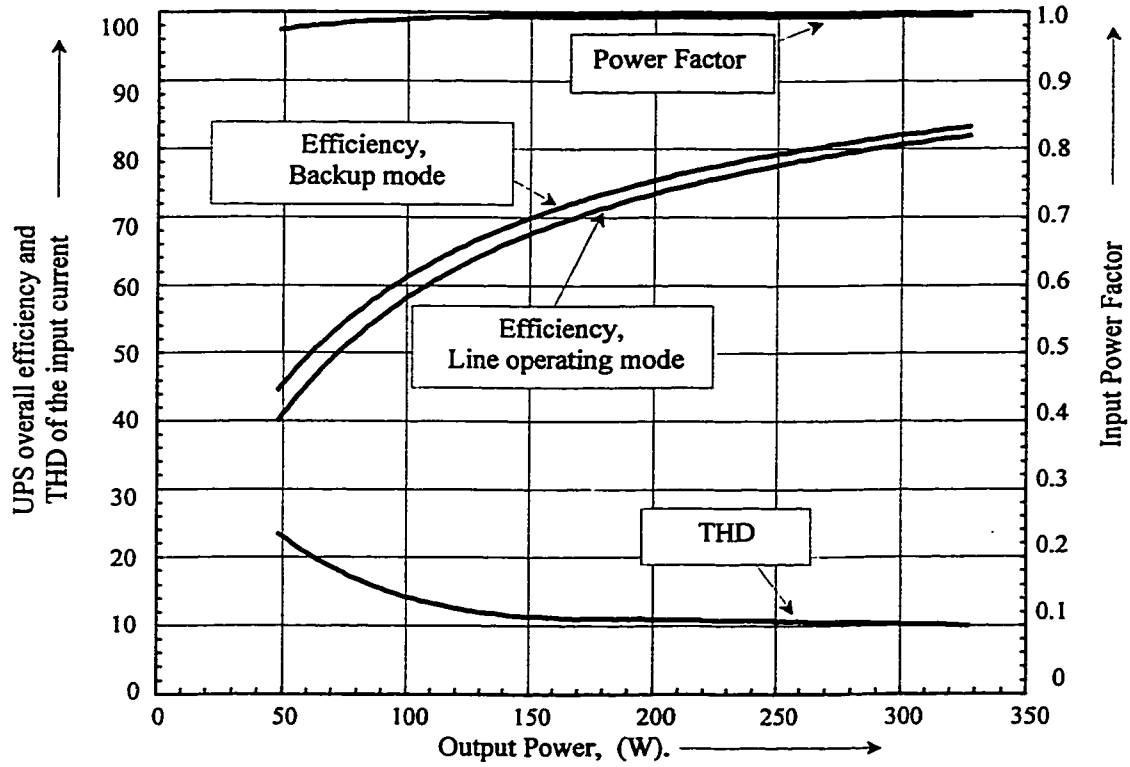


Fig. 5.22 Experimental Results. Static performance of the UPS.
v_{in}=120V, v_b=50V, v_{o_ac}=100V (peak).

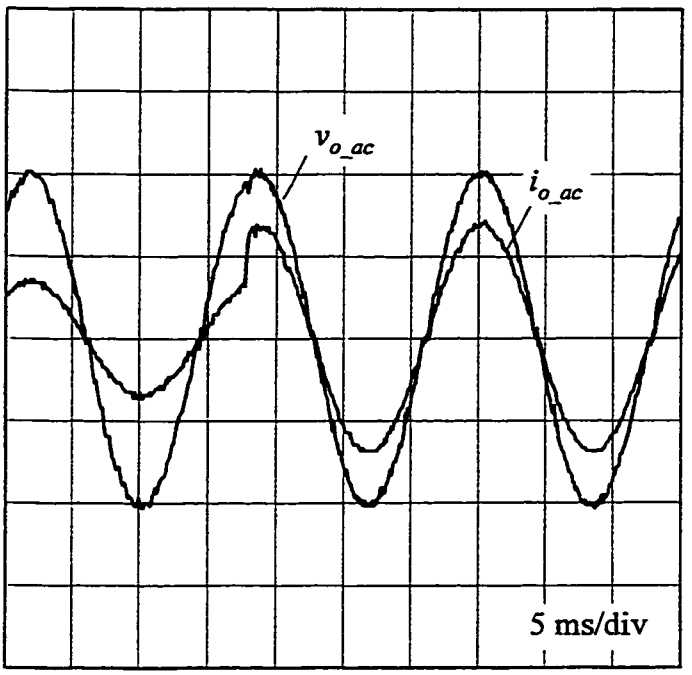


Fig. 5.23 Experimental Results. Transient response due to a step change in the load from 175 to 350 W.
v_{in}=120V, v_b=50V.

5. 5 SUMMARY AND CONCLUSIONS

In this chapter a ZVS bidirectional converters operating in self-sustained oscillation suitable for UPS applications have been introduced. The operating principle of the converters have been presented and the main characteristics given. Experimental results are presented to validate the concepts developed. An UPS topology have been proposed and analyzed. In summary, the main features of the proposed UPS are: (i) operation with zero voltage switching at all operating conditions, (ii) isolation of the input, output and battery from each other using high frequency transformers, (iii) the output load is inherently protected against short circuit since the high frequency link current is regulated, (iv) the input has close to unity power factor independent of the output load, and (v) the UPS maintains uninterrupted output voltage upon the failure of the incoming ac line.

CHAPTER 6: SUMMARY AND CONCLUSIONS

6. 1 SUMMARY

The challenge found in designing isolated UPSs is to keep the size small while producing high quality input and output waveforms without degrading the overall efficiency of the UPS. This is emphasized in those applications that require isolation between the input, the output and the battery. This thesis addresses this problem by proposing a single high frequency transformer UPS topology. This UPS topology presents high input power factor, without dedicate power factor correction stage, and it has few converter stages in cascade between the input and output. When operating at high switching frequency the switching losses limit overall efficiency of the UPS. Aiming to mitigate the switching losses a control technique, which ensures operation with ZVS, is developed. In addition, the proposed control technique allows the operation with variable frequency plus phase shift modulation, which reduces the stresses in the UPS. In the thesis analysis and design procedures are developed and experimental results are presented to validate the concepts developed and to demonstrate the feasibility and performance of the proposed converters.

6. 2 CONTRIBUTIONS

The main contributions of this thesis are as follows:

(i) A fully isolated UPS topology based on series-parallel resonant converters has been proposed. The main features of the proposed UPS topology are: (a) the use

of a single high frequency transformer to provide galvanic isolation between the input, the output and the battery from each other; (b) the operation with high input power factor without requiring a dedicated power factor correction stage.

(ii) A control technique for resonant converters has been developed. This control technique, which is named self-sustained oscillation control, allows the operation with ZVS at different loads and input voltage values. Therefore, the switching losses can be eliminated making it possible to operate at high switching frequencies and to use smaller isolation transformer and filters without degrading the overall efficiency of the converter. It has been shown in the thesis that the proposed control technique can be applied to series, parallel, series-parallel, and bidirectional resonant converters.

(iii) It has been demonstrated in the thesis that the proposed self-sustained oscillation control technique can produce the combination of variable frequency and phase shift modulation. As a result, reduction of the switching frequency range and current stresses in the power circuit are achieved when compared with conventional variable frequency control, and ZVS is extended to the entire load range when compared with phase shift modulation.

(iv) A modified control action approach for single stage ac-to-dc series-parallel resonant converters operating in self-sustained oscillation mode has been proposed. This approach improves the input power factor without requiring active control of the input current. As a result, the limits on the low frequency current harmonics drawn by the equipment connected to the utility grid, which are

imposed by regulatory agencies, can be satisfied without increasing the complexity of the converter's circuitry.

(v) A design procedure for the selection the resonant circuit parameters of the proposed UPS operating with both inductive and capacitive output dc-bus filters has been developed. With this design procedure, the parameters of the power circuit of the proposed series-parallel resonant based UPS are selected to allow operation with a high input power factor and a constant output dc bus voltage under different battery charging conditions.

In addition, the following related contributions are made in the thesis:

(i) An isolated bidirectional dc-to-dc converter operating with the proposed controller has been investigated and it is demonstrated that bidirectional power transfer can be achieved while ensuring ZVS.

(ii) It is shown in the thesis that isolated dc-to-ac converters can also be implemented with the proposed self-sustained controller. Both the analytical and the experimental results demonstrate the feasibility of the proposed converter.

(iii) A ZVS series resonant based UPS has been proposed. It consists of three ZVS high frequency converters, one series resonant circuit, and two high frequency transformers. This UPS can operate with high input power factor and provide full isolation between the input, output, and battery while operating with ZVS under all load and input voltage conditions.

6. 3 CONCLUSIONS

The following conclusions can be reached regarding the proposed controller and converters:

(i) The proposed self-sustained oscillation controller ensures operation with a lagging power factor at different load and input (output) voltages since the angle between the current and the voltage at the converter's high frequency terminals is controlled directly, thereby, providing a means to achieve ZVS. This controller can replace the conventional variable frequency control.

(ii) Ac-to-dc series-parallel resonant converters can operate with ZVS and a high input power factor even without active control of the input current. It is demonstrated in the thesis that by the appropriate modification of the control angle the THD of the input current is reduced significantly (11%).

(iii) The proposed series-parallel resonant based UPS topology can operate with both inductive and capacitive output dc bus filters. The operation with capacitive output dc bus filter results in reduced current stresses and higher efficiency during the backup mode.

6. 4 SUGGESTIONS FOR FUTURE WORK

Future work related with the subject dealt in thesis could be in following topics:

(i) The proposed series-parallel resonant based UPS topology requires resonant inductors and a high frequency transformer. Research could be carried out to investigate the possibility of integrating these components in a single magnetic structure.

(ii) The ZVS series resonant based UPS, which is proposed in Chapter 5, operates with constant amplitude current in the resonant circuit. Research can be done to study the possibility of varying the amplitude of this current in order to reduce the conduction losses in the power circuit.

(iii) The isolated ZVS dc-to-ac converter, which is proposed in Chapter 5, operates with a half bridge cycloconverter. Research could be carried out to investigate the advantages of operation with a full bridge cycloconverter where VFPSM can be adopted.

(iv) The overall performance of the implemented laboratory setup could be improved. For example, ultrafast diodes were used to implement the output rectifier of the implemented series-parallel resonant based UPS with capacitive output dc bus filter, however, schottky diodes could be used, which would lead to lower conduction losses. In addition, the layout of the power circuit could be improved, for instance by the appropriate design of print circuit boards, which can reduce the losses in the power circuit.

REFERENCES

[1] *IEEE Recommended Practice for Emergency and Standby Power Systems for Industrial and Commercial Applications*, New York, 1996.

[2] D.C. Griffith, *Uninterruptible Power Supplies Power Conditioners for Critical Equipment*, New York: Marcel Dekker Inc., 1989.

[3] *IEC 1000-3-2: International Standard, IEC Electromagnetic compatibility (EMC), Part 3: Limits - Section 2: Limits of harmonic current emissions*, First edition, 1995.

[4] R. Redl, "Power Electronics and Electromagnetic Compatibility," *in Proc. PESC'96*, 1996, pp. 15-21.

[5] R. Redl, A.S. Kislovski, "Telecom Power Supplies and Power Quality," *IEEE INTELEC'95 Conf. Rec.*, 1995, pp.13-21.

[6] M.Qiu, *Performance Analysis of Power Distribution System for Hybrid Fiber/Coax Networks*, Master Thesis at Concordia University, 1996.

[7] K. Mistry, T, Taylor, "Hybrid Fiber/coaxial Systems: Powering Issues," In Proc. IEEE INTELC'94, 1994, pp. 75-82.

[8] P.Jain, "Powering the Information Superhighway of the Future," *IEEE-IEC Conference Records*, 1995.

[9] C.J. Brunet, "Hybridizing the local loop," *IEEE Spectrum*, June 1994, pp.28-32.

[10] D. Large, "Creating a Network for Interactivity," *IEEE Spectrum*, April 1995, pp.58-63.

[11] L.Cividino, "Power System Architecture's for the Emerging Information Highway," *IEEE- INTELEC Conf. Rec.*, 1994, pp. 90-97.

[12] T.H. Sloane, F. Mekanik, "Effects of Line-Failure Phase Angle in Ferroresonant UPS," in *Proc. IEEE- APEC'96,* 1996, p.716-721.

[13] H. Pinheiro, P. Jain, G. Joos "A Comparison of AC Power Supplies to Power Fiber/Coaxial Networks", *IEEE INTELEC'97*, 1997, p. 73-79

[14] G.J. Smollinger, W.J. Raddi, "Reverse Energy Transfer Through an AC Line Synchronized Pulse Width Modulation Sinewave Inverter," *IEEE-INTELEC Conf. Rec.*, 1981, pp.126-131.

[15] W.J. Raddi, R.W. Johnson, "A Utility Interactive PWM Sinewave Inverter Configured as a High Efficiency UPS," *IEEE-PESC Conf. Rec.*, 1982, pp.42-48.

[16] S. Manias, P.D. Ziogas, G. Olivier, "Bilateral DC to AC Converter Employing a High Frequency Link", *IEEE-IAS 1985 Annual Meeting Conf. Rec.*, 1985, pp. 1156-1161.

[17] T. Kawabata, Y. Shikano, S. Higashino, Y. Yamamoto, M. Udaka, K. Kawagishi "Chargeless UPS Using Multi-functional BIMOS Inverter - Sinusoidal Voltage waveform inverter with current minor loop," *IEEE-IAS 1986 Annual Meeting Conf. Rec.*, pp. 513-520, 1986.

[18] I. Yamato, N. Tokunaga, Y. Matsuda, H. Amano, Y. Susuzi, "New Conversion System for UPS using High Frequency Link," *IEEE-PESC Conf. Rec.*, 1988, pp.658-662.

[19] K. Harada, H. Sakamoto, M. Shoyama "Phase Controlled Dc-Ac Converter with High Frequency Switching," *IEEE-PESC Conf. Rec.*, 1987, pp.13-19.

[20] I. Yamato, N. Tokunaga, Y. Matsuda, Y. Suzuki, H. Amano, "High Frequency link DC-AC Converter for UPS with a New Voltage Clamper," *IEEE PESC Conference Record*, pp.749-756, 1990.

[21] D. Alexa, M. Florea, "Uninterrupted power supply with intermediate HF circuit" *Arch fur Elektrotechnik*, no.5, 1992, pp.341-344.

[22] D. L. Vidor, A.J. Perin "A Soft Commutation Constant High frequency Link DC/AC Converter Operating with Sinusoidal Output Voltage," *IEEE-PESC Conf. Rec.*, 1994, pp.637-643.

[23] S. J. Jeon, G. H. Cho, " A series-parallel compensated uninterruptible power supply with sinusoidal input current and sinusoidal output voltage," *IEEE-PESC Conf. Rec.*, 1997, pp. 297-303.

[24] P.Jain, D. Vincenti, H. Jin, "An Optimized Single-Phase Ac Power Supply with DC bus synchronization," *IEEE- APEC'96 Conf. Rec,* pp.905-910, 1996.

[25] P.Jain, J.R.Espinoza "Transient Performance of a Single-Stage UPS System Single-Phase Trapezoidal-Shaped ac Voltage Supplies," *IEEE-APEC'96 Conf. Rec,* pp.832-838, 1997.

[26] T. Kagotani, K. Kuroki, J. Shinohara, A. Misaizu, "A Novel UPS Using High-Frequency Switch-Mode Rectifier and High-Frequency PWM Inverter," *IEEE-PESC Conference Record*, 1989, pp.53-57.

[27] D. M. Divan, "A New Topology for Single Phase UPS Systems," *IEEE-IAS'89 Annual Meeting Conf. Rec.*, 1989, pp. 931-936.

[28] I. Ando, I. Takahashi, Y. Tanaka, M. Ikchara, " Development of a high efficiency UPS having active filter ability composed of a three arms bridge," in *Proc. IECON'97*, 1997, pp.804-809.

[29] R. Yamada, K. Kuroki, J. Shinohara, T. Kagotani, "High-Frequency Isolation UPS with Novel SMR," *IEEE-IECON Conf. Rec.*, 1993, pp.1258-1262.

[30] K. Hirachi, M. Sakane, S. Niwa, T. Matsui, "Development of UPS Using New Type of Circuits," *IEEE-INTELEC Conf. Rec.*, 1994, pp.635-642.

[31] K. Hirachi, et al, "Cost Effective Practical Developments of High Performance and Multi-functional UPS with New Configurations and Their Specific Control Implementations," *PESC Conference Record*, 1995, pp.480-485.

[32] G.J. Su, T. Ohno, "A Novel Topology for Single Phase UPS Systems," *IEEE-IAS 1997 Annual Meeting Conf. Rec*, 1997, pp. 1376-1382.

[33] R. Caceres, et al, "A high performance uninterruptible power supply with power factor correction," *PESC Conference Record*, 1997, pp. 304-309.

[34] R.L. Steigerwald, R.E. Tompkins, "A Comparison of High-Frequency Link Schemes for Interfacing a DC source to a Utility Grid," *IEEE-IAS 1982 Annual Meeting Conf. Rec.*, 1982, pp. 759-766.

[35] W.J. Gu, R. Lui, "A Study of Volume and Weight vs. Frequency for High-Frequency Transformers," *IEEE-PESC Conf. Rec.*, 1993, pp.1123-1129.

[36] M.F. Schlecht, B.A. Miwa, "Active power factor correction for switching power supplies," IEEE Trans. Power Electronics, vol.2, no.4, pp.273-281, Oct.1987.

[37] D. Chambers "A new high frequency resonant techniques for dynamic correction of offline converter input current waveforms," *Proceedings of Powercon 10*, F-1, 1983, pp.1-10.

[38] M. Madigan, R. Erickson, E. Ismail, "Integrated High Quality Rectifier Regulators," in *Proc. of PESC'92*, 1992, pp. 1043-1051.

[39] Y. Jiang, F.C. Lee, G. Hua, W. Tang, "A novel single-stage single phase parallel power factor correction scheme," in *Proc. of PESC'94*, 1994, pp. 569-575.

[40] O. Garcia, J. A. Cobos, P. Alou, R. Prieto, J. Uceda, "A new family of single-stage isolated power factor correction with fast regulation of the output voltage," in *Proc. of PESC'94*, 1994, pp. 1137-1144.

[41] M. Qiu, G. Moschopoulos, H. Pinheiro, P. Jain, "A PWM full-bridge converter with natural input power factor correction," in *Proc. of PESC'98*, 1998, pp. 1605-1611.

[42] J.G. Cho, G.Y. Jeong, J.W. Baek, G.H. Rim, "Novel zero-voltage-transition isolated PWM boots converter for single stage power factor correction," in *Proc. of PESC'98*, 1998, pp. 1023-1029.

[43] R.J. King, T.A. Stuard, "Inherent overload protection for series resonant converter," *IEEE Trans. on Aerospace and Electronics Systems*, pp.820-830, Nov. 1983.

[44] K. Lui, F.C. Lee, "Resonant Switch –A unified approach to improve the performances of switching Converters," *IEEE International Telecommunications Energy Conf. Rec.*, 1984, pp.344-351.

[45] W.A. Tabisz, F.C. Lee, "Zero-Voltage-Switching multi-resonant technique- A novel approach to improve performance of high frequency quasi-resonant topologies," *IEEE PESC Conf. rec.*, 1988, pp. 9-17.

[46] P.Jain, "A phase-shift modulated double tuned dc/dc converter: Analysis and experimental results," *IEEE APEC Conference Records*, 1992, pp 90-97.

[47] P.Jain, J.Valerio, "A Review of Single Phase Power Factor Correction Circuit for Telecommunications Applications," *Conf. Rec. INTELEC'94*, pp 334-338, 1994.

[48] O.D. Patterson, D.M.Divan, "Pseudo-resonant full bridge dc-dc Converter," *IEEE Trans. on Power Elect.*, vol. 6, no.4 , pp. 671-678, Oct. 1991.

[49] G. Hua, C.S. Leu, F.C. Lee "Novel zero-voltage Transition" *IEEE Trans. on Power Electronics*, vol. 9, no.2, pp. 213-219, Mar. 1994.

[50] G. Hua, E.X. Yang, Y. Jaing, F.C. Lee, "Novel Zero-Current Transition PWM converters," *IEEE PESC Conf. rec.*, 1993,pp. 538-544.

[51] D.M.Divan, "The Resonant DC Link Converter - A new concept in Static Power Conversion," *IEEE- IAS Conference Records*, 1986, pp. 648-656.

[52] P.K. Sood, T.A. Lipo, "Power Conversion Distribution System Using A Resonant High Frequency AC Link," *IEEE-IAS 1986 Annual Meeting Conf. Rec.*, pp. 533-541, 1986.

[53] M. Matsui, Y.Y. Yang, "Macroscopic Modeling of a parallel Resonant Link Converter and Its Application to Closed-loop Link Voltage Control," *IEEE-IAS 1997 Annual Meeting Conf. Rec.*, 1997.

[54] G.B. Joung, C.T. Rim, G.H. Cho, "Integral cycle Control of the series resonant converter," *IEEE Trans. Power Electron.*, vol.4, pp.83-91, 1989.

[55] P.Bidan, M. Valentin, L. Martinez, "Modeling and Current-mode control of a zero-current switching resonant converter used for Ac side voltage generation," *IEEE PESC'93 Conf. Rec.*, pp.636-640, 1993.

[56] R. Oruganti and F.C. Lee, "Resonant Power Processors: Part I -Methods of Control," *IEEE-IAS 1984 Annual Meeting Conf. Rec.*, 1984, pp. 860-867.

[57] R.L. Steigerwald, "A comparison of Half-bridge resonant converter topologies," *IEEE Trans. Power Electron.*, vol. 3, pp. 174-182, April 1988.

[58] M.J.Schutten, R.L.Steigerwald and M.H. Kheraluwala, "Characteristics of Load Resonant Converters Operated in a High-Power Factor Mode," *IEEE Trans. Power Electron.*, vol. 7, pp. 304-314, April 1992.

[59] J. He and N. Mohan, "Input-current shaping in line rectification by resonant converters," *IEEE Industry Applications Society Conference Record*, 1987, pp.991-995.

[60] A.K.S. Bhat, "Operation of High-Frequency resonant Converters on the Utility Line with Improved Characteristics," *IEEE Trans. Power Electronics*, vol.12, no.4, July 1997.

[61] H. Fujite, H. Akagi, "A 2 MHz, 2KW Voltage –Source inverter for low-Temperature Plasma Generators: Implementation of Fast Switching with a Third-Order Resonant Circuit," *IEEE Industry Applications Society Conference Record*, 1997.

[62] R.L Sterigerwald, "Analysis of a resonant transistor dc-dc converter with captive output filter," *IEEE Transaction on Industrial Electronics*, vol. IE-32, no.4, pp.439-444, Nov. 1985.

[63] A.K. Bhat, "Analysis and design of series-parallel resonant converter with capacitive output filter," *IEEE Transactions on Industry Applications*, vol.27, no.3, pp. 523-530, May/June 1991.

[64] A.K. Bhat and M. M. Swamy, "Loss Calculation in Transistorized Parallel resonant Converters Operating Above Resonance," *IEEE Trans. Power Electron.*, vol 4, pp. 391-401, October 1989.

[65] R. Oruganti and F.C. Lee, "Resonant Power Processors: Part II -Methods of Control ," *IEEE-IAS 1984 Annual Meeting Conf. Rec.*, pp. 860-867, 1984.

[66] V. Sendanyoye, K. Al-Haddad, V. Rajagopalan, "Optimal Trajectory Control Strategy for Improved dynamic response of series resonant converter," *IEEE-IAS 1990 Annual Meeting Conf. Rec.*, 1990, pp. 1237-1242.

[67] M.G. Kim, D.S. Lee, M.J.Youn, "A New State Feedback Control of Resonant Converters," *IEEE Trans. Industrial Electronics.*, vol 38, pp. 178-178, June 1991.

[68] J. Hong, D. Maksimovic, R.W. Erickson and I. Khan, "Half-Cycle Control of Parallel Resonant Converter Operated as a High Power Factor Rectifier," *IEEE Trans. Power Electron.*, vol. 10, pp. 13, January 1985.

[69] K. Al-Haddad, A. Bellahnid, V. Rajagopalan, Y. Cheron, H. Foch, "Novel Control Strategy to Improve the Dynamic Performance of Series Resonant Converters," *IEEE-IAS 1988 Annual Meeting Conf. Rec.*, 1988, pp. 806-812.

[70] L. Rossetto, "A simple Control Technique for Series Resonant Converters," *IEEE Trans. Power Electron.*, vol 11, no.4, pp.554-560, July 1996.

[71] J.J.E. Slotine, W. Li, *Applied Nonlinear Control*, New Jersey: Prentice Hall, 1991.

[72] R.J. King, T.A. Stuart, "A Large-Signal Dynamic Simulation for Series Resonant Converter," *IEEE Trans. on Aerospace and Electronics Systems*, vol. AES-19, no.6, pp.859-870, Nov.1983.

[73] G. C. Verghese, M. E. Elbuluk, J. G. Kassakian, "A General Approach to Sampled-Data Modeling for Power Electronics Circuits," *IEEE Trans. on Power Electron.*, vol. PE-1, no.2, pp. 76-89, April 1986.

[74] J.L. Duarte, J.M.A. Willaert, "A full digitized phased-shift modulated LCC resonant converter," *PESC Conference Record*, 1994, pp.1303-1308.

[75] C.T. Rim, G.H. Cho, "Phasor Transformation ant its Application to the DC/AC Analyses of frequency Phase-Controlled Series Resonant Converters (SRC)," *IEEE Trans. Power Electron.*, vol, 5, n. 2, pp. 201-211, April 1990.

[76] E.X. Yang, F.C. Lee and M.M. Jovanovic, "Small-Signal Modeling of LCC Resonant Converter," *PESC Conference Record*, 1992, pp.941-948.

[77] V. Belaguli, A.K.S. Bhat, "A Hybrid Resonant Converter Operated as a Low Harmonic Rectifier With and Without Active Control," *PESC Conference Record*, 1996, pp.720-726.

[78] V. Belaguli, A.K. Bhat, "High Power Factor Operation of Discontinuous Current Mode Series-Parallel Resonant Converter," *INTELEC Conf. Rec.*, 1994, pp.359-366.

[79] H.Pinheiro, P.Jain, G. Joos, "Series-Parallel Converter in the Self-Sustained Oscillating Mode for Unity Power Factor Applications," *Conf. Rec. of APEC 97*, vol.1, pp. 477-483, 1997.

[80] A.P. Loh, V.U. Vasnani, "Necessary Conditions for Limit Cycles in Multiloop Relay System," *IEE Proc. Control Theory Appl.*, vol.141, no.3, May 1994.

[81] Tsypkin, YA. Z.: "Relay Control Systems," (Cambridge University Press, Cambridge, 1984).

[82] H.Pinheiro, P.Jain, G.Joos "Self-Sustained Oscillating Resonant Converters Operating above the Resonant Frequency," *Conf. Rec. of APEC'97*, vol. 2, 1997, pp. 993-999.

[83] H.Pinheiro, P.Jain, G. Joos, "Series-Parallel Converter in the Self-Sustained Oscillating Mode for Unity Power Factor Applications," *Conf. Rec. of APEC 97*, vol.1, 1997, pp 477-483.

[84] H.Pinheiro, P. Jain, G. Joos, "Performance Characterization of two Self-Oscillating Controllers for Parallel Resonant Converters Operating with Unity Power Factor, "*Conf. Rec. of PESC'97*, vol.1, 1997, pp. 692-698.

[85] H.Pinheiro, P. Jain, G. Joos, "A New AC Power Supply based on Series-Parallel Resonant Converter," *Conf. Rec. of PESC'97*, vol.1, 1997, pp. 310-316.

[86] R. Lai, K.D.T.Ngo, "A PWM Method for Reduction of Switching Loss in a Full-Bridge Inverter," *IEEE Trans. Power Electron.*, vol.10, no.3, pp.337-343, .

[87] M. H. Kheraluwala, R. W. Gascoigne, D.M. Divan, E.D. Baumann, "Performance Characterization of High-Power Dual Active Bridge dc-to-dc Converter," *IEEE Trans. Industry Applications*, vol. 28, no.6, Nov. 1992.

[88] N. H. Kutkut, G. Luckjiff, D. M. Divan, "A dual Bridge high current dc-to-dc converter with soft switching capability," *IEEE-IAS 1988 Annual Meeting Conf. Rec.*, 1997, pp. 1396-1405.

[89] H. Pinheiro, P. Jain, G. Joos "Zero Voltage Switching Series Resonant Based UPS", *Proc. IEEE PESC' 98*, 1998, pp.1879-1885.

[90] J.L. Duarte, J.M.A. Willard, "A fully digitized phase-shift modulated LCC resonant converter," *Proc. IEEE PESC'94*, 1994, pp.1303-1307.

[91] S.D. Johnson, R. W. Erickson, "Stead-State Analysis and Design of the Parallel Resonant Converter," *IEEE Trans. Power. Electron.*, vol. 3, no. 1, pp. 93-104, Jan. 1988.

[92] A.K.S. Bhat, "Analysis and Design of a Series-Parallel Resonant Converter with Capacitive Output Filter," *IEEE Trans. Industry Applications*, vol. 27, no. 3, pp. 523-530, May/June. 1991.

[93] C. Loef, "Analysis of a full-bridge LCC-type parallel resonant converter with capacitive output filter," in *Proc.PESC'97*, 1997, p. 1402.

[94] B. Yaakov, G. Rahav, "Average modeling and simulation of series-parallel resonant converters by SPICE compatible behavioral dependent sources," in *Proc. APEC'96*, 1996, p. 116-120.

APPENDIX 1: IMPACT OF THE SOC ON THE DYNAMIC BEHAVIOR OF RESONANT CONVERTERS

In Chapter 2 the range of control angle for operation with ZVS in self-sustained oscillation mode was found using the describing function method based on the first harmonic approximation, and by considering that the control angle was directly controlled. Here these assumptions are relaxed and as an example, the impact of the SOC on the dynamic behavior of the series-parallel resonant converters is investigated in detail. In order to accurately model the converter with the SOC the sampled-data modeling approach is adopted [72-74]. The model derived includes the states associated with the power circuit, as well as the states associated with the proposed SOC, allowing, in this way, to investigate how the parameters of the SOC affects the overall performance of the converter.

A.1 MODES OF OPERATION

Since the main goal of this appendix is to investigate the resonant converter with SOC, ideal voltage and current sources are used to represent the input voltage source and output load respectively. In this case, the series-parallel resonant converter with a SOC that uses the current through the resonant inductor as the feedback variable assumes the form as shown in Fig. A1.1.

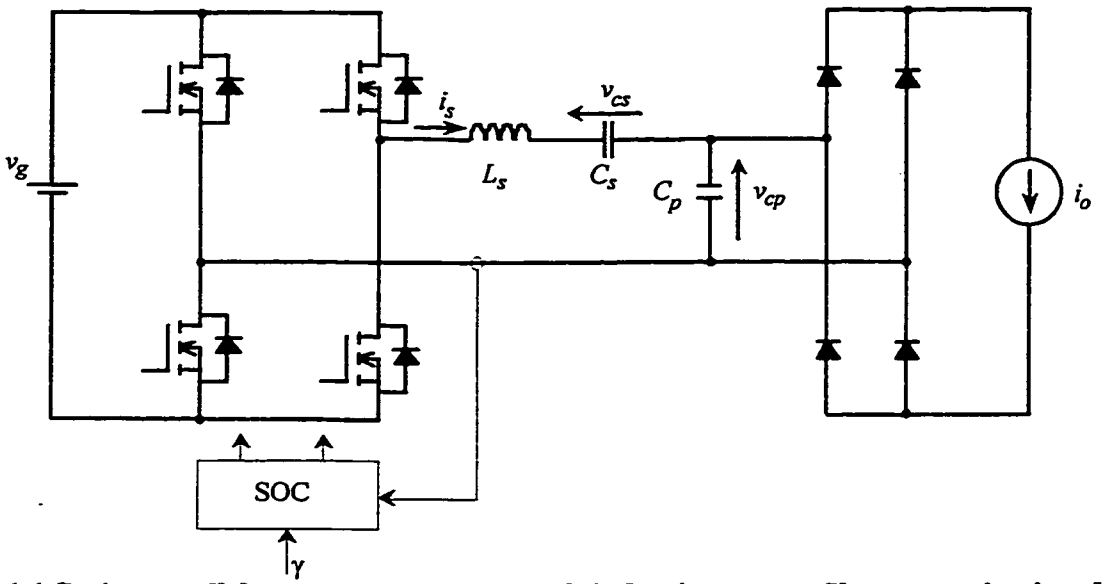


Fig. A1.1 Series-parallel resonant converter with inductive output filter operating in self-sustained oscillation mode.

Let us consider that the series-parallel resonant converter operates cyclically with a succession of n linear time invariant circuit configurations in each cycle. By piecing together the solution of each circuit configuration the converter can be described by a non-linear sampled-data model of the form

$$x_{k+1} = f(x_k, u_k) \tag{A1.1.a}$$

$$\sigma(x_k, u_k) = 0 \tag{A1.1.b}$$

where $f(.)$ and $\sigma(.)$ are vector functions whose entries are scalar functions with the vector arguments x_k and u_k. The vector x_k is the state vector whose entries are the states of the converter sampled at the time instant t_k. For the converter of Fig. A1.1 the state vector can be selected as $x_k = [i'_s(t_k)\ v'_s(t_k)\ v'_{cp}(t_k)\ x_s(t_k)\ s_t(t_k)]^T$. The symbol ' marks the normalized variables. The base quantities required to obtain the normalized values are: $i_{base}=v_g/\omega_o L_s$, $v_{base}=v_g$, and the time is normalized with $t_{base}=1/\omega_o$. On the other hand, the

input vector $\boldsymbol{u}_k$ is comprised of two vectors, that is, $\boldsymbol{u}_k = [\boldsymbol{p}_k , \boldsymbol{w}_k]$. The entries of the vector $\boldsymbol{w}_k$ are the indirectly-controlled-transition-times [73]. The indirectly-controlled-transition-times define the time instants when the circuit configurations change inside of a switching cycle. The indirectly-controlled-transition-times, here named τ_i, are characterized by at least one of the following events:

(i) Commutation of output diode rectifier, either due to zero crossing of the voltage v_{cp} or when the current i_s becomes greater than the load current.

(ii) Transition of the inverter output voltage, when v_{ca} becomes greater than s_t.

(iii) Reset of the sawtooth signal s_t, when the inductor current crosses zero.

When the converter operates cyclically with n circuit configurations within a switching cycle the vector $\boldsymbol{w}_k$ is defined as $\boldsymbol{w}_k = [\tau_1 \ \tau_2 \ .. \ \tau_n]^T$. Finally, the vector $\boldsymbol{p}_k$ contains the independent sources of the circuit. For the converter of Fig. A1.1 $\boldsymbol{p}_k = [v'_g \ i'_o \ V_p]^T$, where the two first entries are independent sources of the power circuit while the last entry, V_p, is the reference voltage, that is used to set the amplitude of the sawtooth signal s_t.

In order to derive the functions f (.) and σ (.) an operating mode with a specific switching sequence must be considered. The series-parallel resonant converter of Fig. A1.1 can operate with continuous capacitor conduction mode (CCVM) or with discontinuous capacitor voltage mode (DCVM) depending on the output load. Fig. A1.2 shows typical waveforms that are found during cyclic steady-state operation of the circuit of Fig. A1.1.

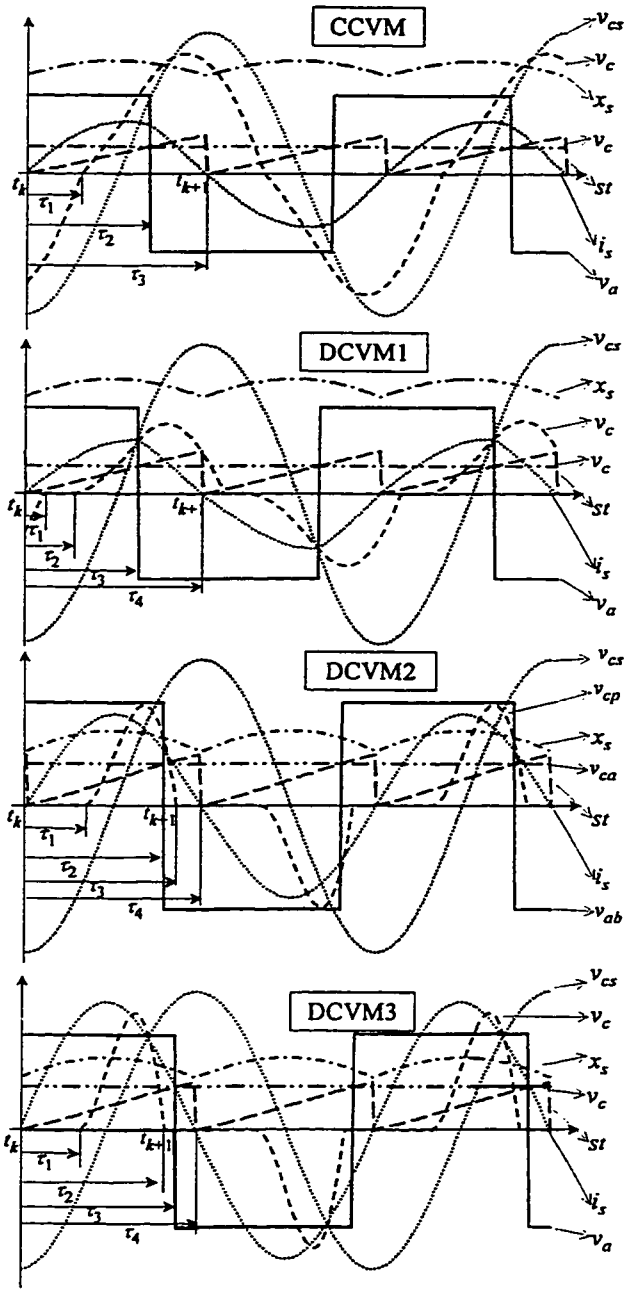


Fig. A1.2 Main waveforms of the series-parallel resonant converter at different operating modes.

The function $f(.)$ and $\sigma(.)$ usually are different at each mode of operation. For operation with CCVM the vector function $f(.)$ is given by

$$f(x_k,u_k)=\Phi(\tau_3-\tau_2)\{\Phi(\tau_2-\tau_1)[(\Phi(\tau_1)\Phi_0 Wx_k+\Psi(\tau_1)I_1p_k]+\Psi(\tau_2-\tau_1)I_2p_k\}+\Psi(\tau_3-\tau_2)I_3p_k \tag{A1.2}$$

where $\Phi(.)$ is the expositional matrix associated with the state space description of the resonant circuit and the SOC. and $\Psi(.)$ is a function of the integral of exponential matrix. These functions are given by:

$$\Phi(t)=\begin{bmatrix} \cos(\sqrt{1+\beta}t) & \frac{-\sin(\sqrt{1+\beta}t)}{\sqrt{1+\beta}} & \frac{-\sin(\sqrt{1+\beta}t)}{\sqrt{1+\beta}} & 0 & 0 \\ \frac{\sin(\sqrt{1+\beta}t)}{\sqrt{1+\beta}} & \frac{\beta+\cos(\sqrt{1+\beta}t)}{1+\beta} & \frac{-1+\cos(\sqrt{1+\beta}t)}{1+\beta} & 0 & 0 \\ \frac{\beta\sin(\sqrt{1+\beta}t)}{\sqrt{1+\beta}} & \frac{-\beta+\beta\cos(\sqrt{1+\beta}t)}{1+\beta} & \frac{1+\beta\cos(\sqrt{1+\beta}t)}{1+\beta} & 0 & 0 \\ 0 & 0 & 0 & \cos(\upsilon t) & -\frac{\upsilon\omega_o}{k_{p2}}\sin(\upsilon t) \\ 0 & 0 & 0 & \frac{\upsilon\omega_o}{k_{p1}}\sin(\upsilon t) & \cos(\upsilon t) \end{bmatrix} \tag{A1.3}$$

where υ is the ratio between ω_{sr} and ω_o. β is the ratio between the series and the parallel resonant capacitors, that is $\beta=C_s/C_p$. On the other hand, the integral function of the exponential matrix,$\Psi(.)$, is given by:

$$\Psi(t)=\begin{bmatrix} \frac{\sin(\sqrt{1+\beta}t)}{\sqrt{1+\beta}} & \frac{\beta-\beta\cos(\sqrt{1+\beta}t)}{1+\beta} & 0 \\ \frac{1-\cos(\sqrt{1+\beta}t)}{1+\beta} & \frac{\beta(\sqrt{1+\beta}t-\sin(\sqrt{1+\beta}t))}{(1+\beta)^{3/2}} & 0 \\ \frac{\beta-\beta\cos(\sqrt{1+\beta}t)}{1+\beta} & \frac{-\beta(\sqrt{1+\beta}t+\beta\sin(\sqrt{1+\beta}t))}{(1+\beta)^{3/2}} & 0 \\ 0 & 0 & \frac{\sin(\upsilon t)}{\upsilon}\frac{k_{p1}}{\omega_o} \\ 0 & 0 & 1-\cos(\upsilon t) \end{bmatrix} \tag{A1.4}$$

The matrices I_1, I_2 and I_3 are diagonal matrices with 1's and –1's on its diagonals. These matrices are used to provide the correct polarity the voltage applied by the inverter in resonant circuit as well as the current drawn by the output rectifier from the resonant circuit during each circuit configuration within a switching cycle. These matrices are given by:

$$I_1 = \begin{bmatrix} 1 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \quad I_2 = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \quad I_3 = \begin{bmatrix} -1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \qquad \text{(A1.5), (A1.6),(A1.7)}$$

It is worth mentioning that the sawtooth signal is reset whenever the current i_s crosses zero by the reset pulse ***RP***. Here the reset pulse ***RP*** will be represent by an impulse function at $t = t_k$. Therefore, an additional circuit configuration can be used to represent the transition of the states of the converter from $t = t_{k-}$ to $t = t_{k+}$. It is possible demonstrate that the matrix Φ_0, which is defined as

$$\Phi_0 = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \qquad \text{(A1.8)}$$

maps the converter states from $t = t_{k-}$ to $t = t_{k+}$. Finally, the matrix W is used to exploit the half-wave symmetry of the resonant circuit variables. If the matrix W is defined by

$$W = \begin{bmatrix} -1 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \qquad \text{(A1.9)}$$

then the resonant circuit variables are represented as unidirectional quantities, therefore simplifying the converter representation.

On the other hand, the entries of the vector function $\sigma(.)$ are the constraint equations related with the event that characterizes the end of each circuit configuration. For operation in CCVM the function $\sigma(.)$ is given by

$$\sigma(x_k,u_k)=\begin{bmatrix} [(\Phi_1(\tau_1)\Phi_0 W x_k+\Psi_1(\tau_1)I_1 p_k]_3 \\ [\Phi_1(\tau_2-\tau_1)[(\Phi_1(\tau_1)\Phi_0 W x_k+\Psi_1(\tau_1)I_1 p_k]+\Psi_1(\tau_2-\tau_1)I_2 p_k]_5-v_{ca} \\ [\Phi_1(\tau_3-\tau_2)\{\Phi_1(\tau_2-\tau_1)[(\Phi_1(\tau_1)\Phi_0 W x_k+\Psi_1(\tau_1)I_1 p_k]+\Psi_1(\tau_2-\tau_1)I_2 p_k\}+\Psi_1(\tau_3-\tau_2)I_3 p_k]_1 \end{bmatrix} \quad \text{(A1.10)}$$

where the notation $[\ ]_i$ is used to extract the i-th entry of the vector within the brackets. The first entry of $\sigma(.)$ is a function that defines the zero crossing of the voltage across the parallel resonant capacitor and it characterizes the instant that the output diode rectifier commutates. The second entry defines the instant that the sawtooth signal and the control voltage v_{ca} are equal. At this instant, the inverter voltage commutates from v_g to $-v_g$. The third entry is a function that defines the zero crossing of the current i_s. This function characterizes the (i) time instant that the sawtooth signal is reset and (ii) the end of a half-cycle of operation.

A similar procedure can be used to obtained the functions $f(.)$ and $\sigma(.)$ for the DCVM1, DCVM2 and DCVM3. Taking into account that the converter behaves distinctly in each operating mode it is advisable to obtain the boundary between the different mode of operation before deriving the small signal models of the converter. The boundary between the CCVM and DCVM1 can be obtained by equating the indirectly-controlled-transition-times τ_1 and τ_2 for the DCVM1 and solve the associated equation

(A1.1) for its steady state operating point. A similar procedure can be applied to find the boundary between DCVM1 and DCVM2, as well as to find the boundary between DCVM2 and DCVM3. The boundaries between the different modes of operation are shown in Fig. A1.3. It is also indicated in this figure operating points obtained from the simulation of the circuit of using the PSIM simulator. From this figure, it is concluded that there is a good agreement between the simulation and the analytical results.

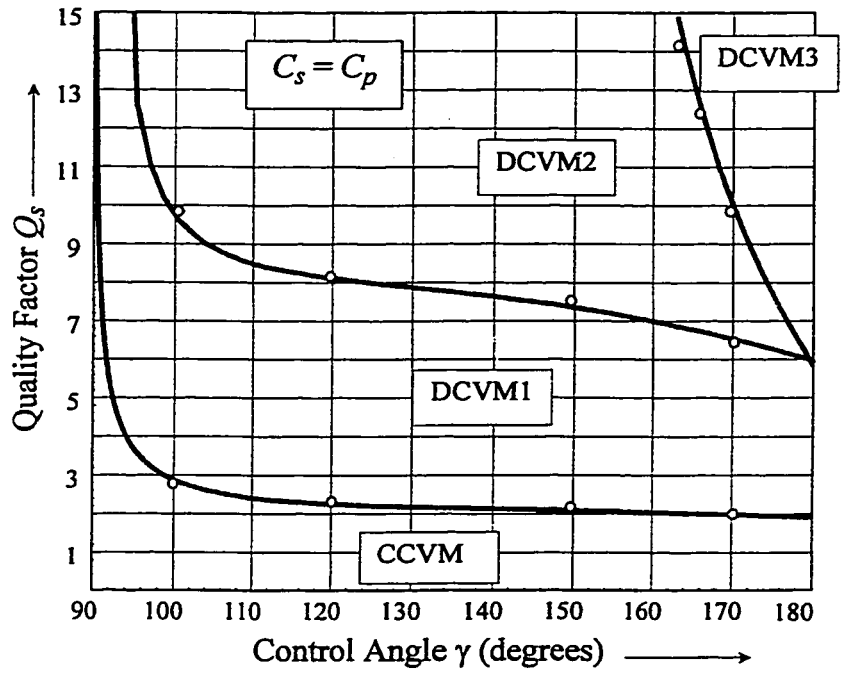


Fig. A1.3 Operation modes. Series-parallel resonant converter with inductive output filter.

Circles indicate simulation results. Solid lines are obtained from analytical results.

Once the boundaries between the different mode are identified, the small signal models of converter can be derived. The next sub-section addresses this issue.

A1.2 SMALL SIGNAL MODELS

In order to derive the small signal model an equilibrium point of (A1.1) must be found. The equilibrium point can be found by solving the following equations:

$$f(x_k, u_k) - x_k = 0 \tag{A1.11.a}$$

$$\sigma(x_k, u_k) = 0 \tag{A1.11.b}$$

Let us consider that the converter of Fig. A1.1 operates cyclically in CCVM mode and that a small perturbation applied to it does not make the converter to move to another mode of operation. Then, by linearizing the nonlinear sampled-data model (A1.1) around a given operating point results in a linear time invariant model that can be used to investigate the stability of the converter with the proposed controlled. Such a linear time invariant model assume the form

$$\tilde{x}_{k+1} = A\,\tilde{x}_k + B\,\tilde{p}_k \tag{A1.12}$$

where the matrices A and B are given by

$$A = \frac{\partial f}{\partial x} - \frac{\partial f}{\partial w}\left[\frac{\partial \sigma}{\partial w}\right]^{-1}\frac{\partial \sigma}{\partial x} \tag{A1.13.a}$$

$$B = \frac{\partial f}{\partial p} - \frac{\partial f}{\partial w}\left[\frac{\partial \sigma}{\partial w}\right]^{-1}\frac{\partial \sigma}{\partial p}. \tag{A1.13.b}$$

In order to validate the derived small signal model (A1.12) a small perturbation is applied to both (A1.1) and (A1.12), and their transient responses are then compared. Fig. A1.4 shows the result of this procedure when step changes of small amplitude are added to the control voltage, v_{ca}. It was found that the transient responses of all the state variables of both models are in good agreement as long as the amplitude of the step

changes are kept small. The nonlinear sample data model (A1.1) can be used for simulation of the converter. On the other hand, the small signal model (A1.12) can be used to investigate the stability of the resonant converter with the proposed controller.

Fig. A1.5 illustrates how the poles of the system change for various amplitudes of the control voltage and for various values of the controller parameters. Two poles of (A1.12) are at the origin. These poles at the origin are attributed to the synchronization of the sawtooth signal with the current i_s and to the reset of the sawtooth signal at each half-cycle. The remainder poles are well damped and they are inside of the unity circle, consequently, indicating that the system is stable. This confirms the stability prediction carried out in Chapter 2. Fig. A1.5 (b) shows the locus of the poles of (A1.12) as the parameter ω_{sl}, that defines the gain of the SOC, changes. From Fig. A1.5(b) it is concluded that by increasing ω_{sl} towards ω_o the modes of the system become faster since the poles are shifted toward the origin. Therefore, ω_{sl} can be selected equal to the minimum expected value of ω_o. In this way, the inequality (2.22) is satisfied and good transient responses are achieved. For example, let us consider that series resonant inductor and the series resonant capacitor have a tolerance of +/-20 %. Therefore, ω_{sl} should be selected at 83% of the nominal value of ω_o, since in this way (2.22) is satisfied for all expected values of L_s and C_s.

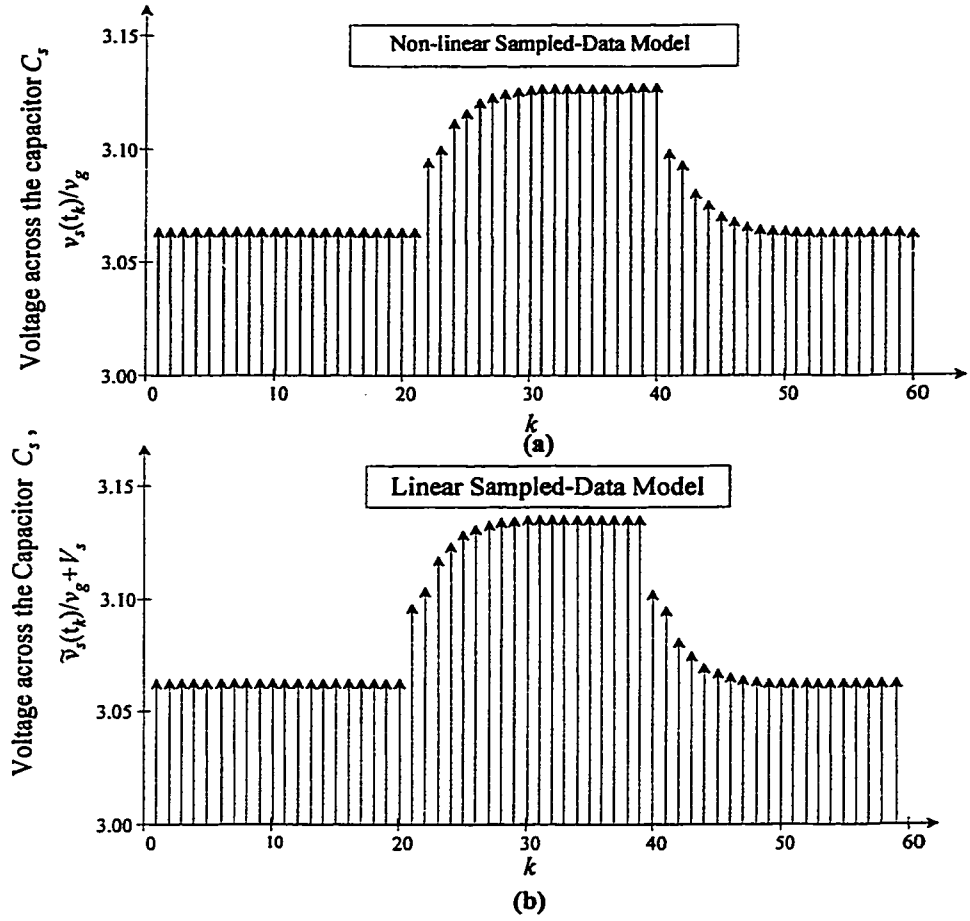
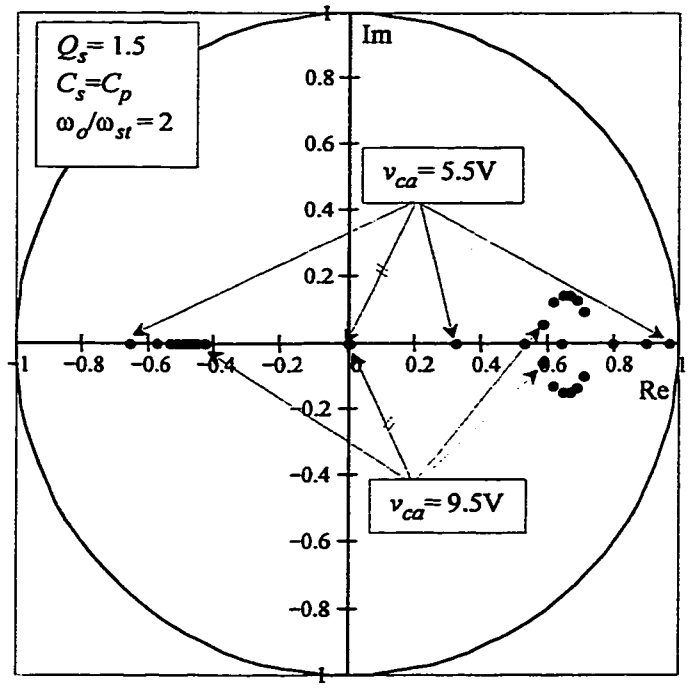
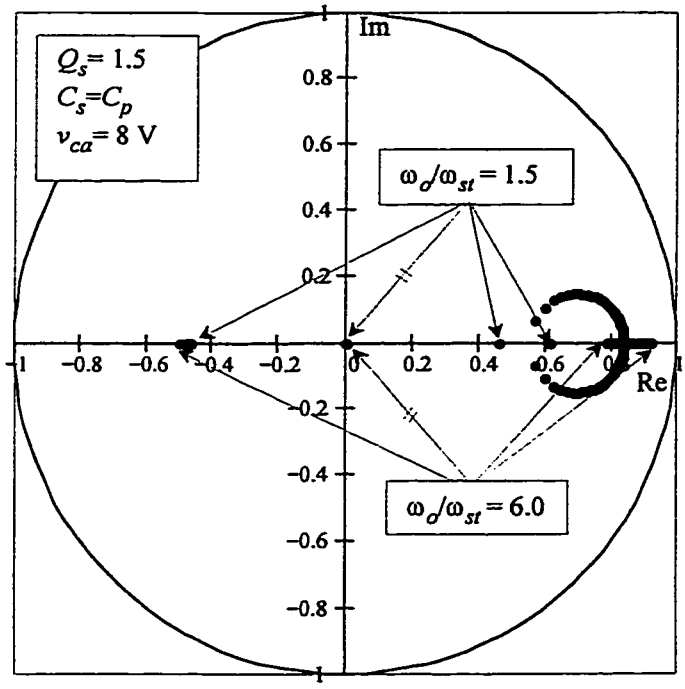


Fig. A1.4 Comparison between the non-linear model (a) and the linear model (b).
Transient caused by step changes in the control voltage between 9V and 9.25V. V_p=10, v_g=1, i_o=1.88, ω_o/ω_{sl}=2. Operation in CCVM with Q_s=1.5.



(a)



(b)

Fig. A1.5 Locus of the sampled-data model poles.
(a) Locus as the control voltage varies. **(b)** Locus as the gain of the self-sustained controller varies.

APPENDIX 2: GENERALIZED SAMPLED-DATA MODEL FOR SERIES-PARALLEL RESONANT CONVERTERS WITH INDUCTIVE OUTPUT FILTER.

This appendix presents the analysis of a series-parallel resonant converter with inductive output filter using the generalized sampled-data modeling approach of static converters. The main goal of this analysis is to obtain the peak value of the voltage across the parallel resonant capacitor, which is a key information for the design the of the UPS topology proposed in Chapter 4.

A2.1 CHARACTERIZATION OF THE MODES OF OPERATION UNDER VFPSM

Before presenting the different modes of operation, the events that characterize the transitions from one circuit configuration to the next, within a switching semi-cycle of the converter of Fig. A2.1, are enumerated. It is assumed that the input voltage source v_g, the output current source i_o, and semiconductors are ideal and that the leg A of the inverter commutes at the zero crossing of the current i_s. In this case, the transition events for the converter of Fig. A2.1 are:

(i) The transition of the voltage v_{ab} from the non-zero to the zero voltage level when the control voltage v_{ca} becomes greater than the sawtooth signal s_t.

(ii) Commutation of the output diode rectifier when the voltage v_{cp} crosses zero with the current i_s greater than i_o. For instant the diodes D_3 and D_2 turn-off and the diodes D_1 and D_4 turn-on when the voltage v_{cp} crosses zero from the negative to

the positive semi-cycle.

(iii) Commutation of the output diode rectifier when the voltage v_{cp} becomes zero and i_s is smaller than i_o. For example, the diodes D_3 and D_2 were previously conducting and D_1 and D_4 turn-on assuming part of the load current and clamping the voltage v_{cp} at zero. This characterizes the beginning of the output load freewheeling interval.

(iv) Commutation of the output diode rectifier characterizing the end of freewheeling interval when the current i_s becomes greater than i_o.

(v) Reset of the sawtooth signal s_t when the current i_s crosses zero.

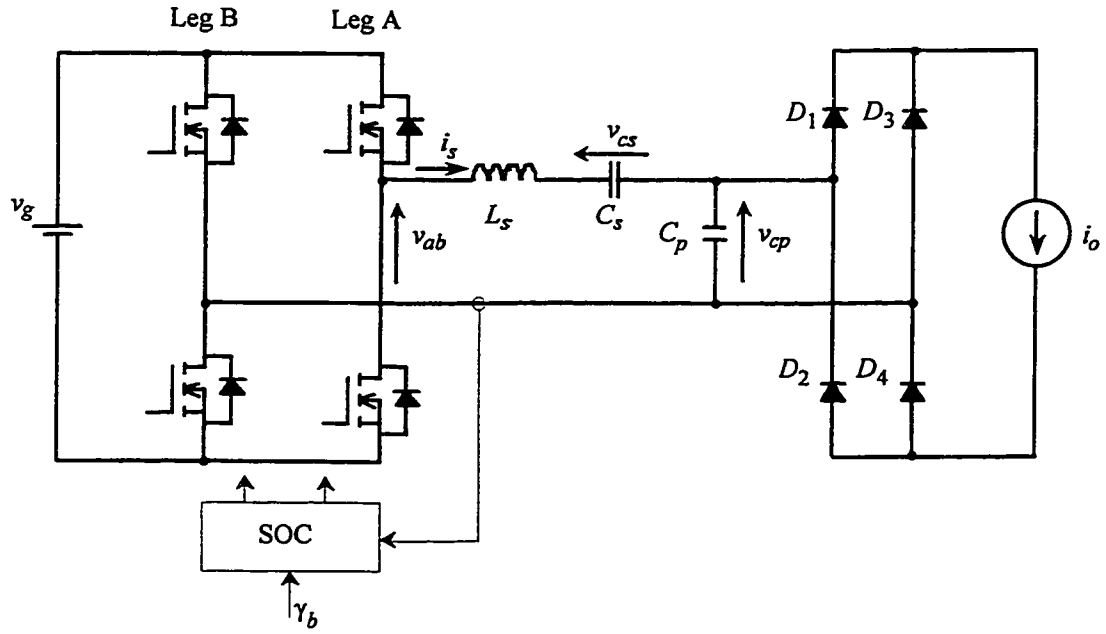


Fig. A2.1 Series-parallel resonant converter with inductive output filter operating in self-sustained oscillation mode

If the current i_s is greater than i_o at the instant that the voltage v_{cp} crosses zero the events (iii) and (iv) do not occur and the converter is said to operate in the continuous capacitor voltage mode, CCVM. Therefore, only the events, (i) and (ii), occurs within a

switching semi-cycle. Two continuous capacitor voltage modes can be characterized depending on the way that the events (i) and (ii) are distributed within the switching semi-cycle. These modes are shown in Fig. A2.2.

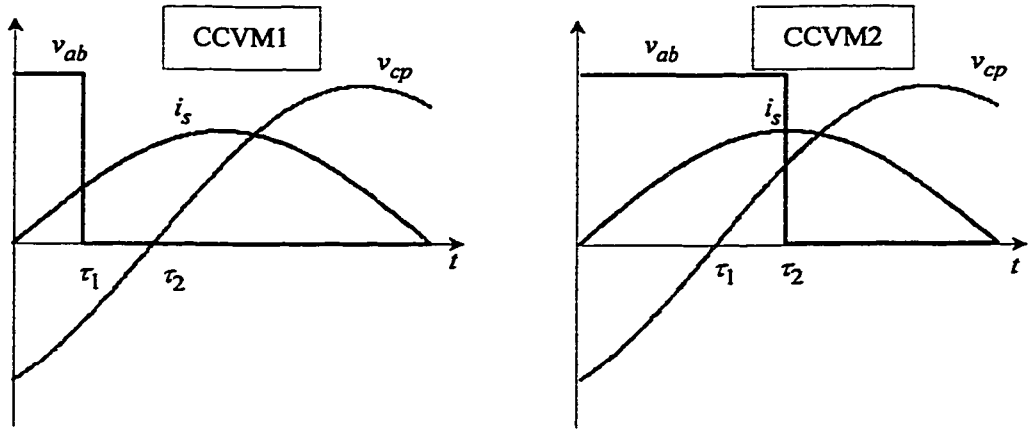


Fig. A2.2 Continuous capacitor voltage modes.

On the other hand, if i_s is smaller than i_o when the voltage reaches zero the voltage v_{cp} will be kept at zero for a finite time interval. This is due to the simultaneous conduction of all diodes of the output rectifier. Therefore, the event (ii) does not occur and the remainder events (i), (iii) and (iv) are distributed within the switching semi-cycle. Six modes of operation can be characterized depending on the order that these three events are distributed within the switching semi-cycle. These modes are called discontinuous capacitor voltage mode 1 to 6 and they are depicted in Fig. A2.3.

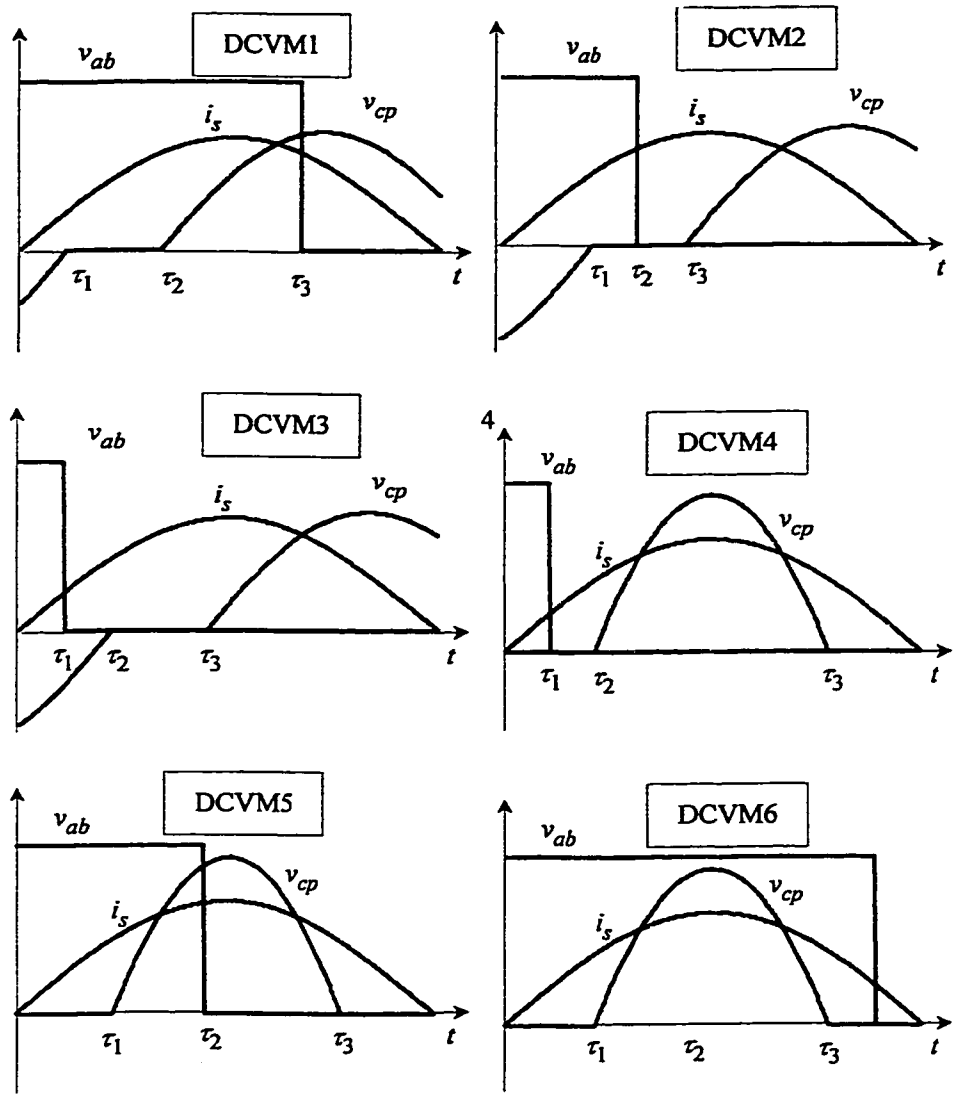


Fig. A2.3 Discontinuous Capacitor Conduction Mode.

A2.2 DESCRIPTION OF THE MODES OF OPERATION

Each one of the eight operating modes can be represented by the sampled-data model (A1.1). In order to simply the derivation of the functions $f(.)$ and $\sigma(.)$ of (A1.1) for each mode of operation, the solution of the two basic circuit configurations will first be presented. The basic circuit configurations of the converter of Fig. A2.1 are given in Fig. A2.4.

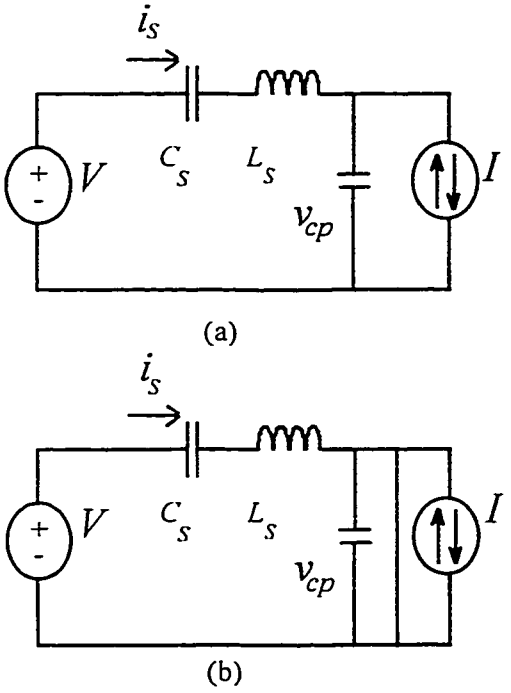


Fig. A2.4 Basic circuit configurations.
(a) Circuit configuration I. (b) Circuit configuration II

Further simplification can be achieved by defining the following base quantities: (i) base time = $\sqrt{L_s C_s}$, (ii) base voltage = v_g. (iii) base current $= v_g/\sqrt{L_s/C_s}$. With these base quantities the following state-space representation for the circuit configuration I can be found:

$$\begin{bmatrix} \frac{di_s'}{dt'} \\ \frac{dv_s'}{dt'} \\ \frac{dv_{cp}'}{dt'} \\ \frac{dx_s}{dt'} \\ \frac{ds_I}{dt'} \end{bmatrix} = \begin{bmatrix} 0 & -1 & -1 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ \beta & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-k_{p1}}{\omega_n} \\ 0 & 0 & 0 & \frac{k_{p2}}{\omega_n} & 0 \end{bmatrix} \begin{bmatrix} i_s' \\ v_s' \\ v_{cp}' \\ x_s \\ s_I \end{bmatrix} + \begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 0 \\ -\beta & 0 & 0 \\ 0 & 0 & \frac{k_{p1}}{\omega_n} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V' \\ I' \\ I_p' \end{bmatrix} \qquad \text{(A2.1)}$$

where the symbol ′ is used to denote normalized quantities. Note that the states of the

SOC. x_s and s_t. were also included in (A2.1). Similarly, the sate-space equation that describes the circuit configuration II is:

$$\begin{bmatrix} \frac{di_s'}{dt'} \\ \frac{dv_s'}{dt'} \\ \frac{dv_{cp}'}{dt'} \\ \frac{dx_s}{dt'} \\ \frac{ds_t}{dt'} \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-k_{p1}}{\omega_n} \\ 0 & 0 & 0 & \frac{k_{p2}}{\omega_n} & 0 \end{bmatrix} \begin{bmatrix} i_s' \\ v_s' \\ v_{cp}' \\ x_s \\ s_t \end{bmatrix} + \begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & \frac{k_{p1}}{\omega_n} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I'' \\ I' \\ I_p' \end{bmatrix} \tag{A2.2}$$

The solution of the state space equations (A2.1) and (A2.2) can be expressed as:

$$\begin{bmatrix} i_s'(t') \\ v_s'(t') \\ v_{cp}'(t') \\ x_s(t') \\ s_t(t') \end{bmatrix} = \Phi_1(t'-t_0') \begin{bmatrix} i_s'(t_0') \\ v_s'(t_0') \\ v_{cp}'(t_0') \\ x_s(t_0') \\ s_t(t_0') \end{bmatrix} + \Psi_1(t'-t_0') \begin{bmatrix} I'' \\ I' \\ I_p' \end{bmatrix} \tag{A2.3}$$

$$\begin{bmatrix} i_s'(t') \\ v_s'(t') \\ v_{cp}'(t') \\ x_s(t') \\ s_t(t') \end{bmatrix} = \Phi_2(t'-t_0') \begin{bmatrix} i_s'(t_0') \\ v_s'(t_0') \\ v_{cp}'(t_0') \\ x_s(t_0') \\ s_t(t_0') \end{bmatrix} + \Psi_2(t'-t_0') \begin{bmatrix} I'' \\ I' \\ I_p' \end{bmatrix} \tag{A2.4}$$

where the matrices $\Phi_1(.), \Psi_1(.)$ and $\Phi_2(.), \Psi_2(.)$ are given by

$$\Phi_1(\tau) = \begin{bmatrix} \cos(\sqrt{(1+\beta)}\,\tau) & \frac{-\sin(\sqrt{(1+\beta)}\,\tau)}{\sqrt{1+\beta_2}} & \frac{-\sin(\sqrt{(1+\beta)}\,\tau)}{\sqrt{1+\beta}} & 0 & 0 \\ \frac{\sin(\sqrt{(1+\beta)}\,\tau)}{\sqrt{1+\beta}} & \frac{\beta+\cos(\sqrt{(1+\beta)}\,\tau)}{(1+\beta)} & \frac{-1+\cos(\sqrt{(1+\beta)}\,\tau)}{(1+\beta)} & 0 & 0 \\ \frac{\beta\sin(\sqrt{(1+\beta)}\,\tau)}{\sqrt{1+\beta}} & \frac{-\beta+\beta\cos(\sqrt{1+\beta}\,\tau)}{(1+\beta)} & \frac{1+\beta\cos(\sqrt{(1+\beta)}\,\tau)}{(1+\beta)} & 0 & 0 \\ 0 & 0 & 0 & \cos(\upsilon\tau) & \frac{-\upsilon\omega_n}{k_{p2}}\sin(\upsilon\tau) \\ 0 & 0 & 0 & \frac{\upsilon\omega_n}{k_{p1}}\sin(\upsilon\tau) & \cos(\upsilon\tau) \end{bmatrix} \tag{A2.5}$$

$$\Psi_1(\tau)=\begin{bmatrix} \frac{\sin(\sqrt{(1+\beta)}\,\tau)}{\sqrt{1+\beta}} & \frac{\beta-\beta\cos(\sqrt{(1+\beta)}\,\tau)}{(1+\beta)} & 0 \\ \frac{1-\cos(\sqrt{(1+\beta)}\,\tau)}{(1+\beta)} & \frac{(\sqrt{1+\beta}\tau-\sin(\sqrt{1+\beta}\tau))\beta}{(1+\beta)^{3/2}} & 0 \\ \frac{\beta(1-\cos(\sqrt{(1+\beta)}\,\tau))}{(1+\beta)} & -\frac{(\sqrt{1+\beta}\tau+\sin(\sqrt{1+\beta}\tau))\beta}{(1+\beta)^{3/2}} & 0 \\ 0 & 0 & \frac{k_{p1}}{\upsilon\omega_o}\sin(\upsilon\tau) \\ 0 & 0 & 1-\cos(\upsilon\tau) \end{bmatrix} \tag{A2.6}$$

$$\Phi_2(\tau)=\begin{bmatrix} \cos(\tau) & -\sin(\tau) & 0 & 0 & 0 \\ \sin(\tau) & \cos(\tau) & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & \cos(\upsilon\tau) & \frac{-\upsilon\omega_o}{k_{p2}}\sin(\upsilon\tau) \\ 0 & 0 & 0 & \frac{\upsilon\omega_o}{k_{p1}}\sin(\upsilon\tau & \cos(\upsilon\tau) \end{bmatrix} \tag{A2.7}$$

$$\Psi_2(\tau)=\begin{bmatrix} \sin(\tau) & 0 & 0 \\ 1-\cos(\tau) & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & \frac{k_{p1}}{\upsilon\omega_o}\sin(\upsilon\tau) \\ 0 & 0 & 1-\cos(\upsilon\tau) \end{bmatrix} \tag{A2.8}$$

Table A2.1 summarizes the main information required to derive the functions *f(.)* and *σ(.)* for each mode of operation.

	Circuit configurations, parameters, and transition events.															
	V	I	Basic Circ.	τ_1	V	I	Basic Circ.	τ_2	V	I	Basic Circ.	τ_3	V	I	Basic Circ.	τ_4
CCVM1	v_g	$-i_o$	I	$s_1=v_{ca}$	0	$-i_o$	I	$v_{cp}=0$	0	i_o	I	$i_s=0$	-	-	-	-
CCVM2	v_g	$-i_o$	I	$v_{cp}=0$	v_g	i_o	I	$s_1=v_{ca}$	0	i_o	I	$i_s=0$	-	-	-	-
DCVM1	v_g	$-i_o$	I	$v_{cp}=0$	v_g	$-i_o$	II	$i_s=i_o$	v_g	i_o	I	$s_1=v_{ca}$	0	i_o	I	$i_s=0$
DCVM2	v_g	$-i_o$	I	$v_{cp}=0$	v_g	$-i_o$	II	$s_1=v_{ca}$	0	$-i_o$	II	$i_s=i_o$	0	i_o	I	$i_s=0$
DCVM3	v_g	$-i_o$	I	$s_1=v_{ca}$	0	$-i_o$	I	$v_{cp}=0$	0	$-i_o$	II	$i_s=i_o$	0	i_o	I	$i_s=0$
DCVM4	v_g	$-i_o$	II	$s_1=v_{ca}$	0	$-i_o$	II	$i_s=i_o$	0	i_o	I	$v_{cp}=0$	0	i_o	II	$i_s=0$
DCVM5	v_g	$-i_o$	II	$i_s=i_o$	v_g	i_o	I	$s_1=v_{ca}$	0	i_o	I	$v_{cp}=0$	0	i_o	II	$i_s=0$
DCVM6	v_g	$-i_o$	II	$i_s=i_o$	v_g	i_o	I	$v_{cp}=0$	v_g	i_o	II	$s_1=v_{ca}$	0	$-i_o$	II	$i_s=0$

TABLE A2.1 SUMMARY OF THE PARAMETERS AND TRANSITION EVENTS FOR THE DIFFERENT MODES OF OPERATION.

For the operation in CCVM1 the functions $f(.)$ and $\sigma(.)$ can be found as:

$$f(x_k, u_k) = \Phi_1(\frac{T_s}{2} - \tau_2)\{\Phi_1(\tau_2 - \tau_1)[(\Phi_1(\tau_1)\Phi_0 W x_k + \Psi_1(\tau_1) I_1 p_k] + \Psi_1(\tau_2 - \tau_1) I_2 p_k\} + \Psi_1(\frac{T_s}{2} - \tau_2) I_3 p_k \tag{A2.9}$$

where the vectors x_k, u_k, p_k, and the matrices W and Φ_0 are defined as in the Appendix 1, while the matrix I_1, I_2 and I_3 are given by:

$$I_1 = \begin{bmatrix} 1 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \qquad I_2 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \qquad I_3 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{A2.10), (A2.11), (A2.12),}$$

On the other hand, the entries of the vector function $\sigma(.)$ are the constraint equations related with the event that characterizes the end of each circuit configuration. For CCVM 1 the vector function $\sigma(.)$ is given by

$$\sigma(x_k, u_k) = \begin{bmatrix} [(\Phi_1(\tau_1)\Phi_0 W x_k + \Psi_1(\tau_1) I_1 p_k]_3 - v_{cm} \\ [\Phi_1(\tau_2 - \tau_1)[(\Phi_1(\tau_1)\Phi_0 W x_k + \Psi_1(\tau_1) I_1 p_k] + \Psi_1(\tau_2 - \tau_1) I_2 p_k]_3 \\ [\Phi_1(T_s/2 - \tau_2)[\Phi_1(\tau_2 - \tau_1)[(\Phi_1(\tau_1)\Phi_0 W x_k + \Psi_1(\tau_1) I_1 p_k] + \Psi_1(\tau_2 - \tau_1) I_2 p_k] + \Psi_1(Ts/2 - \tau_2) I_2 p_k]_3 \end{bmatrix} \tag{A2.13),}$$

Similarly for the CCVM2 the functions $f(.)$ and $\sigma(.)$ given by:

$$f(x_k, u_k) = \Phi_1(\frac{T_s}{2} - \tau_2)\{\Phi_1(\tau_2 - \tau_1)[(\Phi_1(\tau_1)\Phi_0 W x_k + \Psi_1(\tau_1) I_1 p_k] + \Psi_1(\tau_2 - \tau_1) I_4 p_k\} + \Psi_1(\frac{T_s}{2} - \tau_2) I_3 p_k \tag{A2.14}$$

$$\sigma(x_k, u_k) = \begin{bmatrix} [(\Phi_1(\tau_1)\Phi_0 W x_k + \Psi_1(\tau_1) I_1 p_k]_3 \\ [\Phi_1(\tau_2 - \tau_1)[(\Phi_1(\tau_1)\Phi_0 W x_k + \Psi_1(\tau_1) I_1 p_k] + \Psi_1(\tau_2 - \tau_1) I_4 p_k]_3 - v_{cm} \\ [\Phi_1(T_s/2 - \tau_2)[\Phi_1(\tau_2 - \tau_1)[(\Phi_1(\tau_1)\Phi_0 W x_k + \Psi_1(\tau_1) I_1 p_k] + \Psi_1(\tau_2 - \tau_1) I_4 p_k] + \Psi_1(Ts/2 - \tau_2) I_2 p_k]_3 \end{bmatrix} \tag{A2.15),}$$

where the matrix I_4 is given by:

$$I_4 = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{A2.16),}$$

Similar equations $f(.)$ and $\sigma(.)$ can be found for the DCVM1 to DCVM6.

A2.3 BOUNDARY BETWEEN THE MODES OF OPERATION

Once the equation that describe the evolution of the states variables from the beginning to the end of each semi-cycle are derived the steady state operating points can be found from the solution of the following equation:

$$f(x_k, u_k) - x_k = 0 \qquad \text{(A2.17 a)}$$

$$\sigma(x_k, u_k) = 0 \qquad \text{(A2.17 b)}$$

with $0>\tau_1>\tau_2...>T_s/2$.

In order to compute the peak value of the voltage across the parallel resonant capacitor, it is necessary to know the boundary between the modes of operation in the circuit parameter space. For example the boundary between CCVM1 and CCVM2 can be found by solving (A2.17) with $0>\tau_1=\tau_2>T_s/2$ for different circuit parameters. The boundary between CCVM2 and DCVM1 can be found by solving (A2.17), which is associated with DCVM1, with $0>\tau_1>\tau_2=\tau_3>T_s/2$. The results of this procedure for different circuit parameters are shown in Fig. A2.5 to Fig. A2.8.

A2.4 PEAK VALUE OF THE VOLTAGE ACROSS THE PARALLEL RESONANT CAPACITOR

The peak value of the voltage across the parallel resonant capacitor can be found from the solution of the following equation:

$$\hat{v}_{cp} = g(x_k, u_k) \qquad \text{(A2.18 a)}$$

$$0 = \sigma_1(x_k, u_k) \qquad \text{(A2.18 b)}$$

where the functions $g(.)$ and $\sigma_1(.)$ can be derived using the same procedure used for $f(.)$ and $\sigma(.)$. The peak value of the voltage across the parallel resonant capacitor for different values of circuit parameter is plotted in Fig. A2.9 to Fig. A2.12.

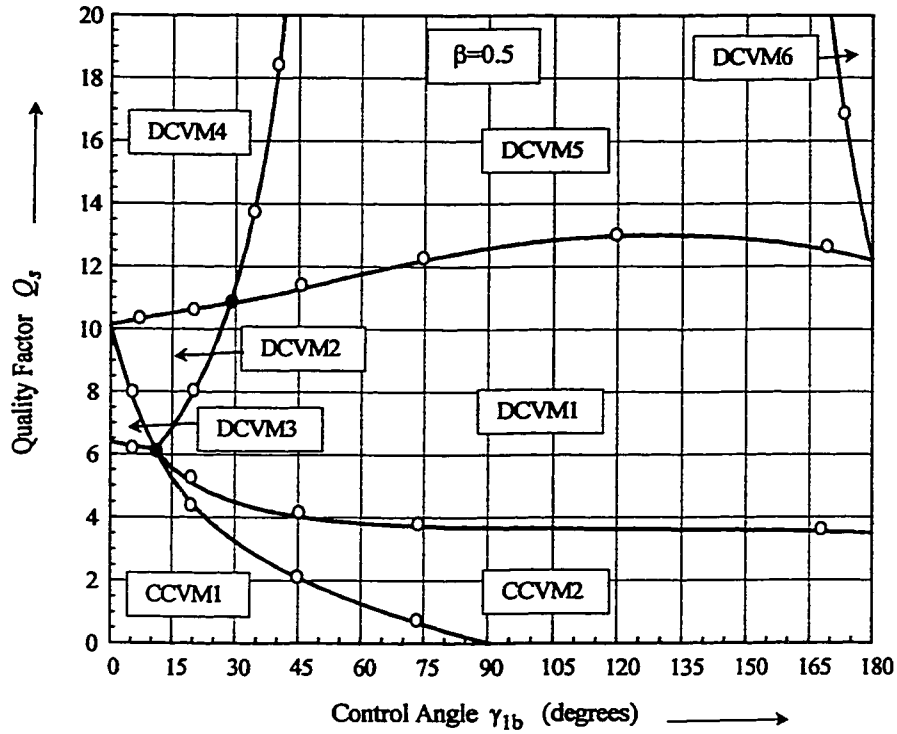


Fig. A2.5 Boundaries between the modes of operation. VFPSM .

$\gamma_{1a}=180^{o}$, $\beta=0.5$. Solid lines are analytical results. Circles represent simulation results.

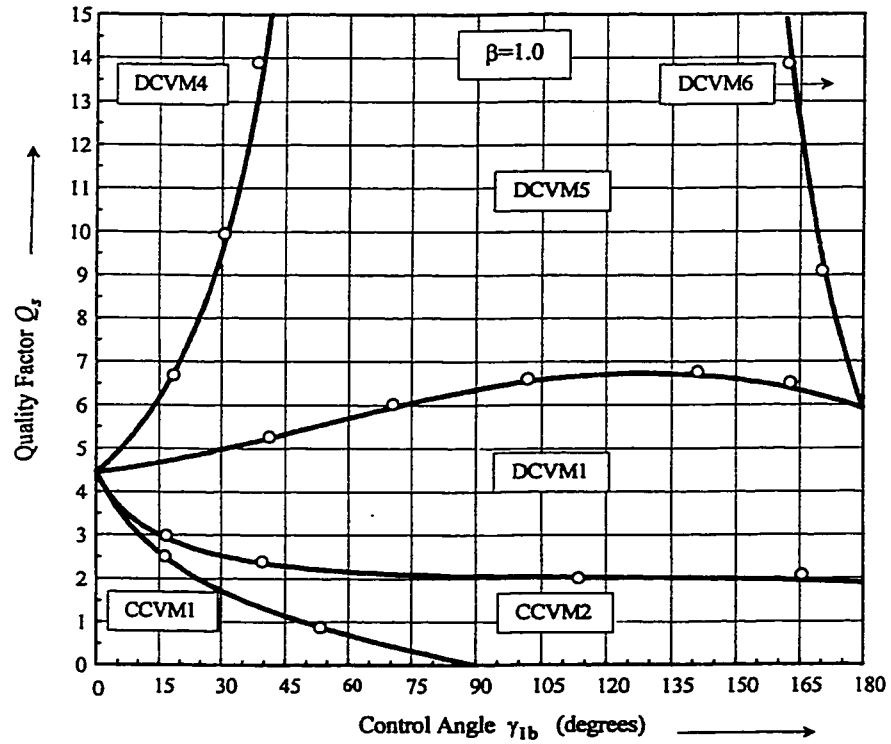


Fig. A2.6 Boundaries between the modes of operation. VFPSM .

$\gamma_{1a}=180^{o}$, $\beta=1.0$. Solid lines are analytical results. Circles represent simulation results.

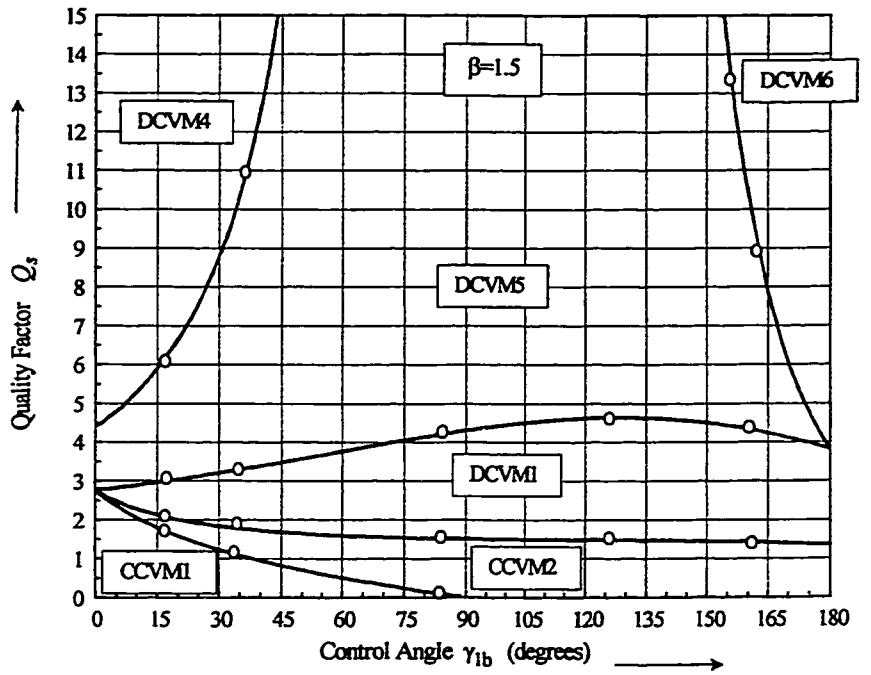


Fig. A2.7 Boundaries between the modes of operation. VFPSM .

$\gamma_{1a}=180^{o}$, $\beta=1.5$. Solid lines are analytical results. Circles represent simulation results.

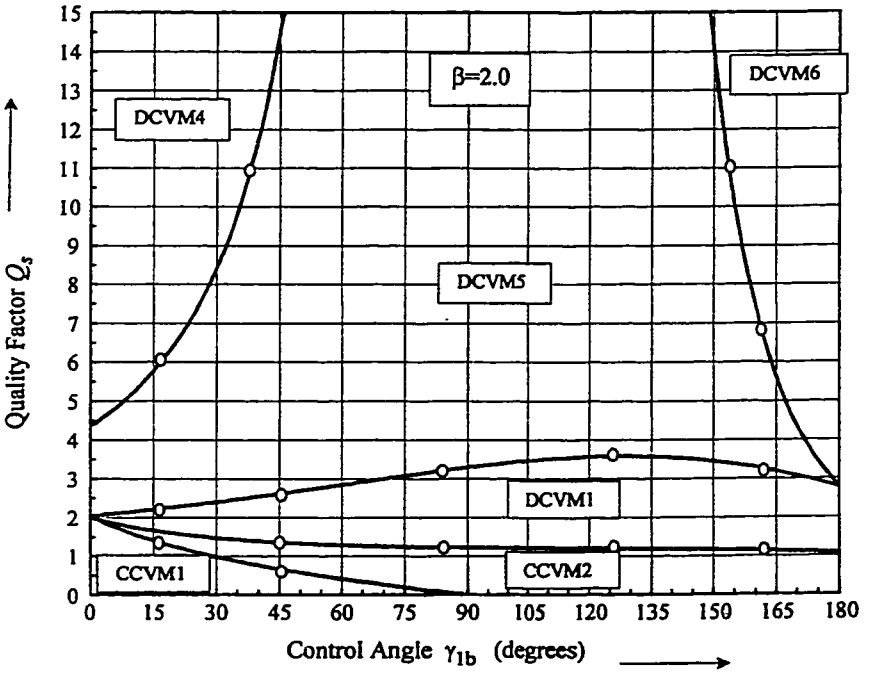


Fig. A2.8 Boundaries between the modes of operation. VFPSM .

$\gamma_{1a}=180^{o}$, $\beta=2.0$. Solid lines are analytical results. Circles represent simulation results.

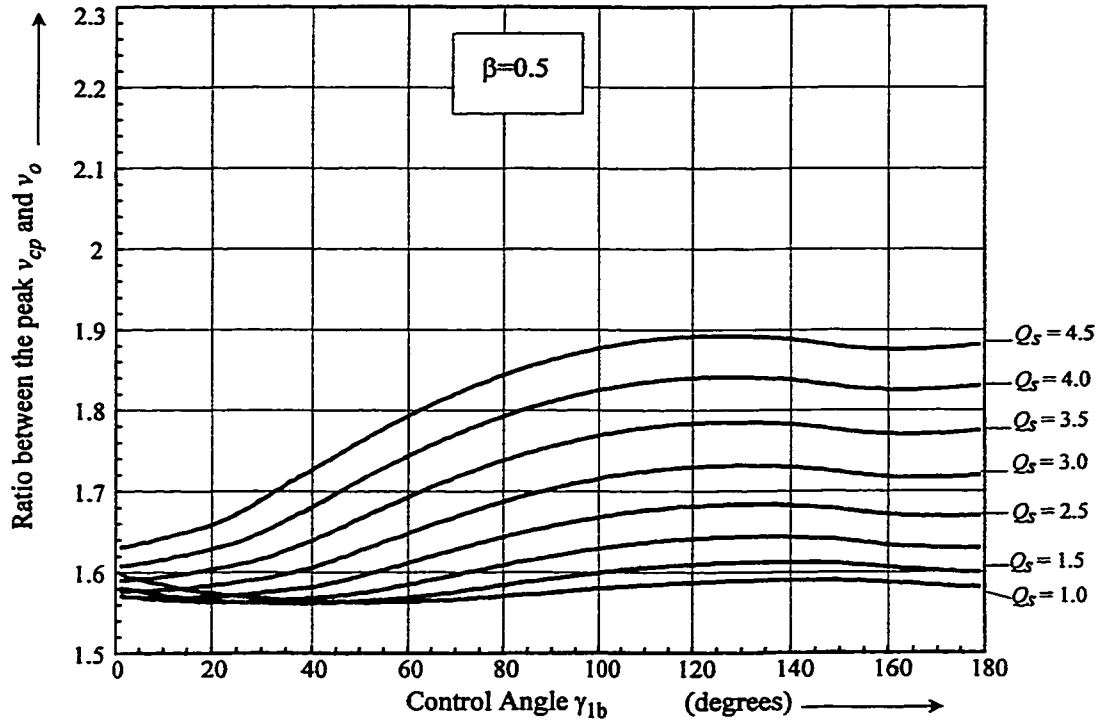


Fig. A2.9 Ratio between the peak value of v_{cp} and the average value of v_o for operation with VFPSM.

(γ_{1a}=180°, β=0.5)

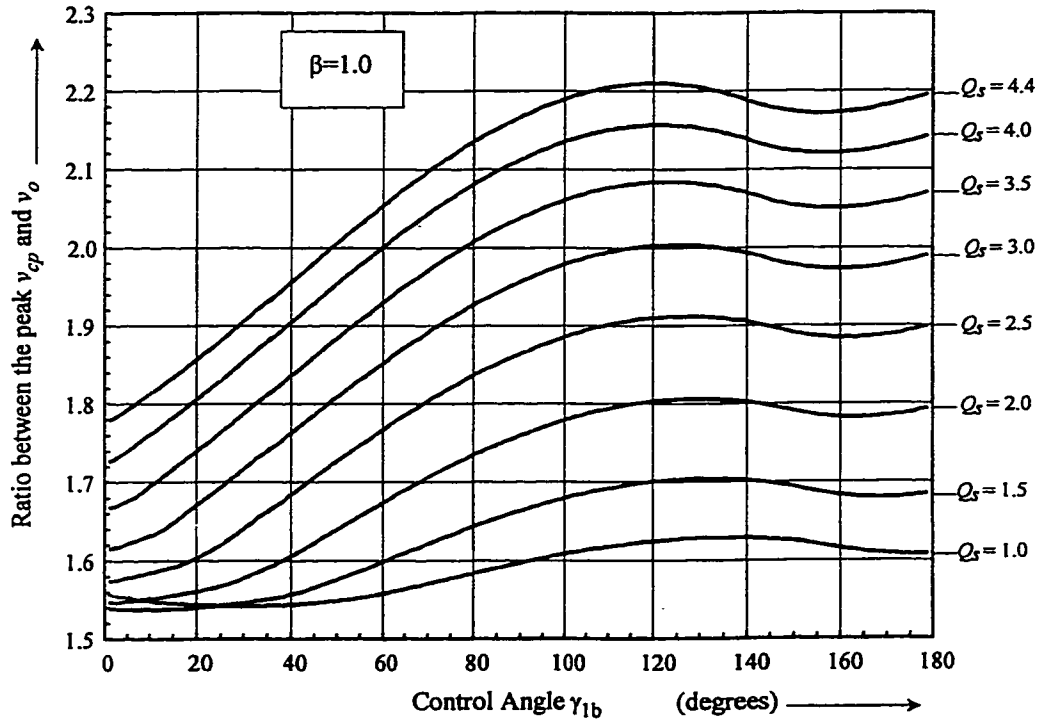


Fig. A2.10 Ratio between the peak value of v_{cp} and the average value of v_o for operation with VFPSM.

(γ_{1a}=180°, β=1.0)

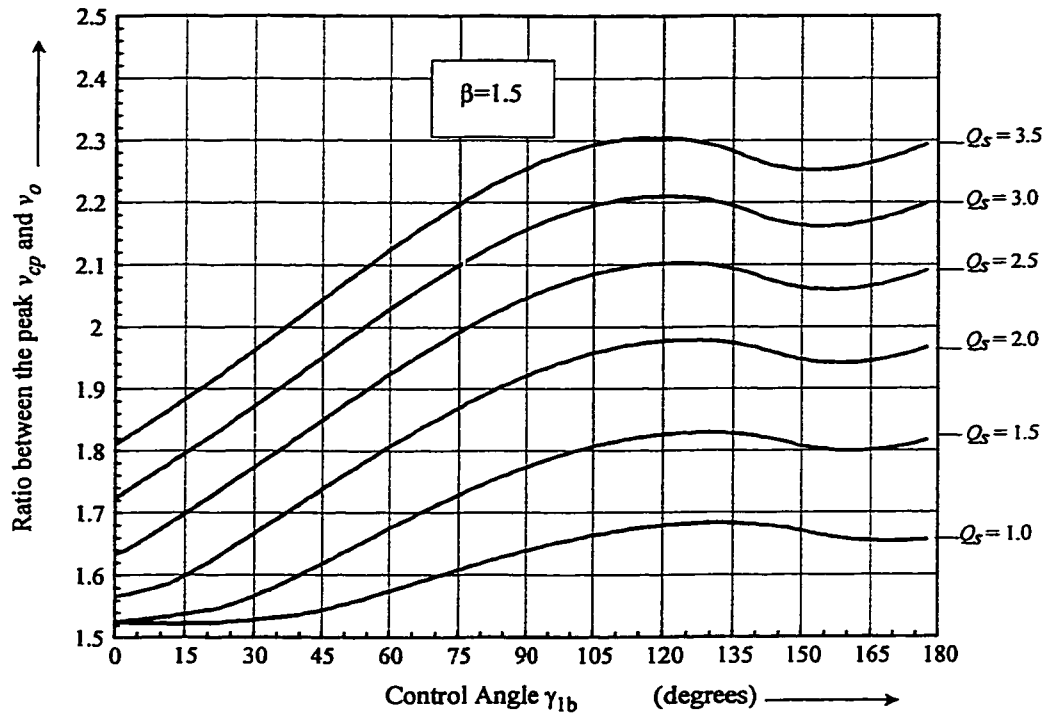


Fig. A2.11 Ratio between the peak value of v_{cp} and the average value of v_o for operation with VFPSM.

(γ_{1a}=180°, β=1.5)

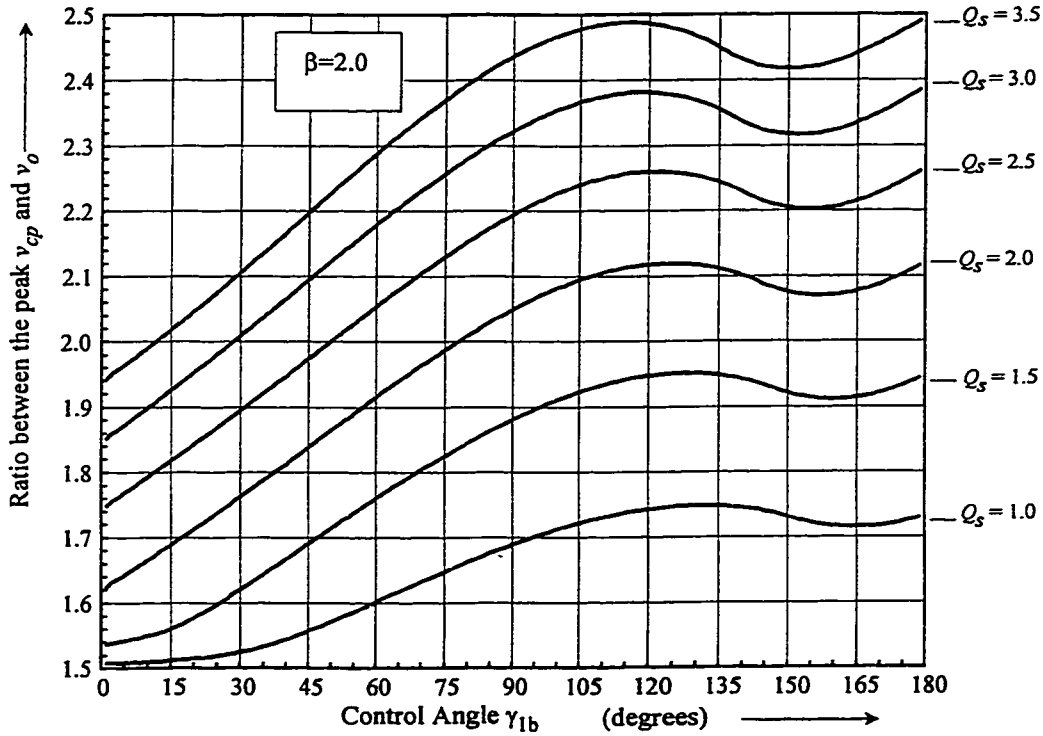


Fig. A2.12 Ratio between the peak value of v_{cp} and the average value of v_o for operation with VFPSM.

(γ_{1a}=180°, β=2)

APPENDIX 3: HIGH FREQUENCY EQUIVALENT CIRCUIT FOR THE UPS TOPOLOGY BASED ON SERIES-PARALLEL RESONANT CONVERTER WITH INDUCTIVE OUTPUT FILTER

In this appendix the solution of a high frequency equivalent circuit for the UPS topology based on series parallel resonant converters with inductive output filter is presented. The analysis carried out is based on the first harmonic component and phasor diagrams are used to illustrate the relation among the resonant circuit variables for both the line operating mode and backup mode.

A3.1 LINE OPERATING MODE

Fig. A3.1 shows the high frequency equivalent circuit that represents the operation of the LSC and BSC during the line operating mode for the UPS topology of Fig. 4.1. The transformer turns ratios are made to be equal to one and an equivalent load resistor R_{eq} is used to represent the output stage. The equivalent load resistor R_{eq} is the resistor that if connected across the primary side of the high frequency transformer would dissipate the same power that is sent by the resonant circuit to the output stage. The equivalent load resistor is given by

$$R_{eq} = \frac{\pi^2}{8}\frac{v_o^2}{P_o} \qquad \text{(A2.1)}$$

where P_o is the power sent by the resonant circuit to the output stage and the voltage v_o is the voltage across the dc output filter capacitor [57,94]. In addition, the resonant branches connected to the LSC and BSC (L_{s1}, C_{s1}, and L_{s2}, C_{s2}) have the same resonant frequency. This resonant frequency is named ω_o. In this way, both resonant branches have inductive characteristic for switching frequencies greater than ω_o. The series resonant branches at the battery side and at the input side will be represented by the equivalent inductances. For instance, the and series resonant branches at the LSC will be represented by:

$$L_{eq1} = \frac{\alpha^2 - 1}{\alpha^2} L_{s1} \tag{A3.2}$$

where α is the switching frequency ratio. The switching frequency ratio α is considered to be greater than one, which means that the converter operates above the resonant frequency of the series resonant branches. Therefore, the equivalent impedance of both the series resonant branches are inductive. In the same manner, the equivalent parallel resonant capacitor is given by

$$C_{eq} = \alpha C_p \tag{A3.3}$$

In the equivalent circuit of Fig. A3.1 the voltages developed by the LSC and BSC are represented by their fundamental components V_{ao1} and V_{ao2} respectively.

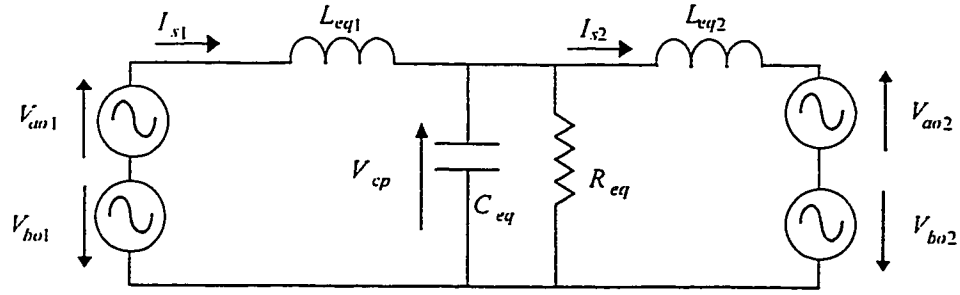


Fig. A3.1High frequency equivalent circuit of the LSC and BSC during the line operating mode.

By applying the Kirchhoff's law to the high frequency equivalent circuit of Fig. A3.1, the equations that define the relationship among the resonant circuit variables can be found, and are given below

$$\frac{4}{\pi}v_g\cos(\frac{\gamma_{1a}-\gamma_{1b}}{2}) = \frac{\pi}{2}v_o\cos(\beta) - I_{s1}\sin(\frac{(\gamma_{1a}+\gamma_{1b})}{2}-\pi)\alpha\omega_o L_{eq1} \quad \text{(A3.4)}$$

$$0 = \frac{\pi}{2}v_o\sin(\beta) + \quad I_{s1}\cos(\frac{(\gamma_{1a}+\gamma_{1b})}{2}-\pi)\alpha\omega_o L_{eq1} \quad \text{(A3.5)}$$

$$I_{s1}\cos(\frac{(\gamma_{1a}+\gamma_{1b})}{2}-\pi) = \frac{\frac{\pi}{2}v_o\cos(\beta)}{R_{eq}} - \frac{\frac{\pi}{2}v_o\sin(\beta)}{(\omega_o C_{eq})^{-1}} + I_{s2}\cos(\sigma) \quad \text{(A3.6)}$$

$$I_{s1}\sin(\frac{(\gamma_{1a}+\gamma_{1b})}{2}-\pi) = \frac{\frac{\pi}{2}v_o\sin(\beta)}{R_{eq}} + \frac{\frac{\pi}{2}v_o\cos(\beta)}{(\omega_o C_{eq})^{-1}} + I_{s2}\sin(\sigma) \quad \text{(A3.7)}$$

$$\frac{\pi}{2}v_o\cos(\beta) = \frac{4}{\pi}\frac{v_b}{2}\cos(\frac{(\gamma_{1a}+\gamma_{1b})}{2}-\pi-\gamma_{2a}) + \frac{4}{\pi}\frac{v_b}{2}\cos(\sigma) - I_{s2}\sin(\sigma)\alpha\,\omega_o L_{eq2} \quad \text{(A3.8)}$$

$$\frac{\pi}{2}v_o\sin(\beta) = \frac{4}{\pi}v_b\sin(\frac{(\gamma_{1a}+\gamma_{1b})}{2}-\pi-\gamma_{2a}) + \frac{4}{\pi}\frac{v_b}{2}\sin(\sigma) + I_{s2}\cos(\sigma)\,\alpha\omega_o L_{eq2} \quad \text{(A3.9)}$$

where the angles in the above equations are defined by means of a phasor diagram in Fig.A3. 2.

The simultaneous solution of equations (A3.4) to (A3.9) gives the possible operating points of the converter. In order to avoid those solutions that do not represent the operation above the resonance frequency of the converter the following constraints are included:

$$\alpha > 1 \quad \text{(A3.10)}$$

$$\gamma_{1a} = \pi \tag{A3.11}$$

$$0 < \gamma_{1b} < \pi \tag{A3.12}$$

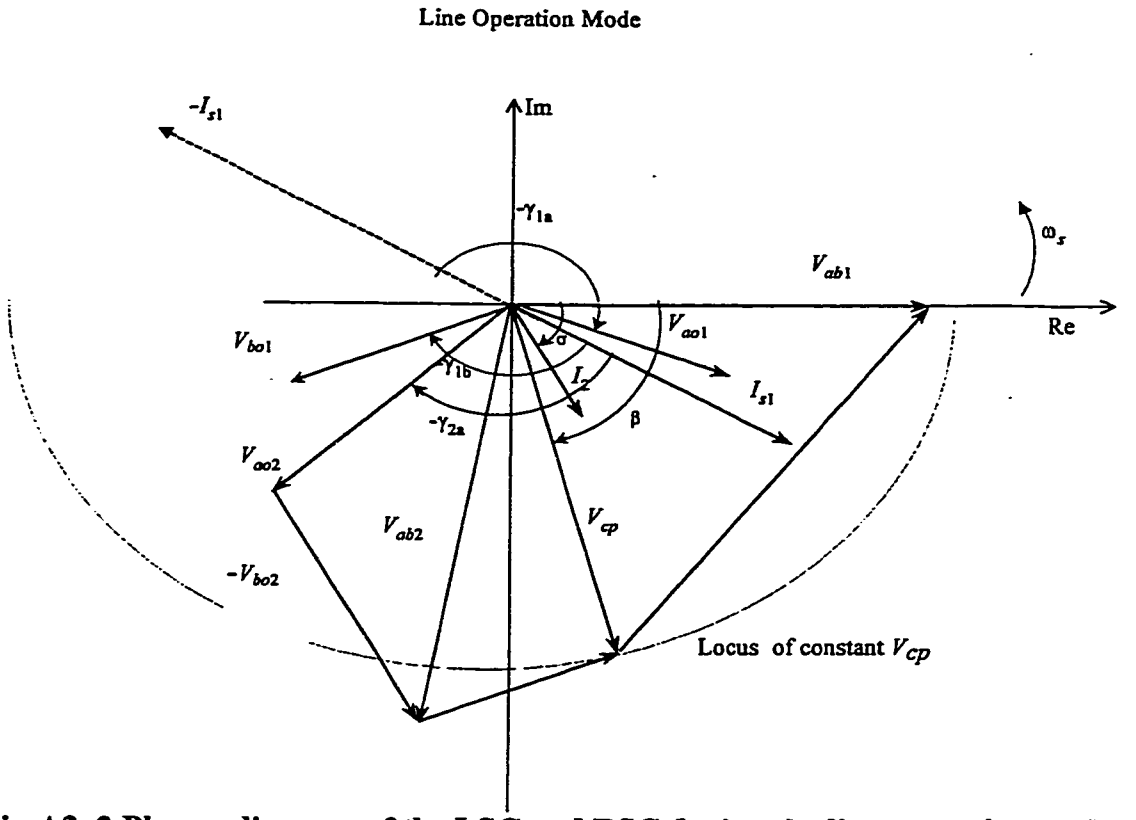


Fig.A3. 2 Phasor diagram of the LSC and BSC during the line operating mode.

$$P_{in} = \frac{v_g \frac{4}{\pi} \cos(\frac{\gamma_{1a} - \gamma_{1b}}{2}) I_{s1} \cos(\frac{(\gamma_{1a} + \gamma_{1b})}{2} - \pi)}{2} \tag{A3.13}$$

$$0 < \gamma_{2b} < \pi \tag{A3.14}$$

$$-\gamma_{2a} < -\arccos(\frac{\frac{\pi}{2} v_o}{v_b}) + \beta - \frac{(\gamma_{1a} + \gamma_{1b})}{2} + \pi \tag{A3.15}$$

The inequality (A3.10) limits the possible solutions to those associated with operation above the resonant frequency. On the other hand (A3.11-A3.13) are associated to the

operation of the line side converter while (A.3.15) is introduced to avoid complex solutions.

An additional constraint is considered to satisfy the input-output power balance. This constraint is given by

$$p_{in} = p_o + p_b \tag{A3.16}$$

where p_{in} is the power at the input of the LSC and p_b is the power sent to the batteries. When operating with unity power factor, the input power is expressed as

$$p_{in} = P_{in} \sin(\omega_{60} t)^2 \tag{A3.17}$$

where $P_{in}/2$ represents the average power absorbed by the converter from the ac mains over one input line cycle. Moreover, the presence of a diode rectifier at the output side requires that

$$p_o \geq 0 \tag{A3.18}$$

In order to simplify the solution the power sent to the battery and to the output side are also considered to follow a sine square profile.

The solution of the equivalent circuit for different points along half period of the input line is given in Fig.4.17 and Fig.4.18 .

A3.2 BACKUP MODE

The operation of the converter in the backup mode can also be represented in terms of ac equivalent circuit. The equivalent circuit for the backup mode is shown in Fig. A3.3 and the equations associated with it are

$$\frac{4}{\pi} v_h \cos\left(\frac{\gamma_{2a} - \gamma_{2b}}{2}\right) = \frac{\pi}{2} v_o \cos(\beta_2) + I_{s2} \sin\left(\frac{(\gamma_{2a} + \gamma_{2b})}{2} - \pi\right) \alpha \omega_o L_{eq2} \tag{A3.19}$$

$$0 = \frac{\pi}{2} v_o \sin(\beta_2) - I_{s2} \cos(\frac{(\gamma_{2a} + \gamma_{2b})}{2} - \pi)\alpha\omega_o L_{eq2} \tag{A3.20}$$

$$-I_{s2}\cos(\frac{(\gamma_{2a} + \gamma_{2b})}{2} - \pi) = \frac{\frac{\pi}{2} v_o \sin(\beta_2)}{R_{eq2}} - \frac{\frac{\pi}{2} v_o \sin(\beta_2)}{(\omega_o C_{eq})^{-1}} \tag{A3.21}$$

$$-I_{s2}\sin(\frac{(\gamma_{2a} + \gamma_{2b})}{2} - \pi) = \frac{\frac{\pi}{2} v_o \cos(\beta_2)}{R_{eq2}} + \frac{\frac{\pi}{2} v_o \cos(\beta_2)}{(\omega_o C_{eq})^{-1}}. \tag{A3.22}$$

The simultaneous solution of equations (A3.19) to (A3.22) results in a possible operating point of the converter during the backup mode. In order to avoid those solutions that do not represent the operating points of the converter in the backup mode, the following constraints should be included:

$$\alpha > 1 \tag{A3.23}$$

$$\gamma_{2a} = \pi \tag{A3.24}$$

$$0 < \gamma_{2b} < \pi \tag{A3.25}$$

$$P_o = \frac{-v_b \frac{4}{\pi} \cos(\frac{\gamma_{2a} - \gamma_{2b}}{2}) I_{s2} \cos(\frac{(\gamma_{2a} + \gamma_{2b})}{2} - \pi)}{2} \tag{A3.26}$$

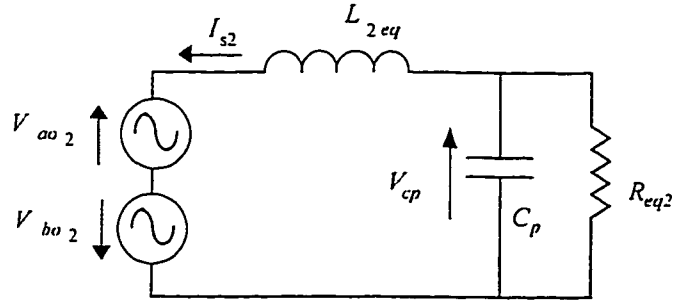


Fig. A3.3 High frequency equivalent circuit of the BSC during the backup mode.

APPENDIX 4: AC-TO-DC SERIES-PARALLEL RESONANT CONVERTER WITH CAPACITIVE OUTPUT FILTER OPERATING WITH UNITY INPUT POWER FACTOR

In this appendix it is derived the design curves for the selection of the resonant circuit parameters of ac-to-dc single stage series-parallel resonant converter with capacitive output filter operating with unity input power factor. The generalized sampled-data modeling approach is used to derive static characteristics of the converter as well as the design curves. The procedure adopted to generate the design curves is similar to the one presented in Section 3.3.

A4.1 MODES OF OPERATION

Let us consider the series parallel-resonant converter with capacitive output filter of Fig. A4.1. In order to derive the sampled-data model(s) for the series parallel resonant converter of Fig. A4.1 it is necessary to consider that the converter operates cyclically taking a succession of configurations within the switching cycle. Before doing so, the events that characterize the transition between the circuit configurations are enumerated. For the converter of Fig. A4.1 these events are:

(a) The turning on of two diodes of the output rectifier when the voltage v_{cp} becomes greater then v_o.

(b) The turning off of two diodes of the output rectifier when the current i_s crosses zero.

(c) The transition of the voltage v_{ab} from non the zero voltage level to the zero voltage level when the control signal v_{ca} becomes greater than the sawtooth signal s_t.

(d) The transition of the voltage v_{ab} from zero to non-zero voltage level when the current i_s crosses zero.

By assuming that the current i_s crosses zero at t=0, just two events occurs within the rest of the semi-cycle, that are the events (a) and (c). As a result, two modes of operation are characterized depending on the distributions of these events within the semi-cycle. Typical waveforms of these modes of operation are shown in Fig. A4.2. Once the modes of operation are identified, exact sampled-data models can be derived and they can be used to obtain the main characteristics of the converter.

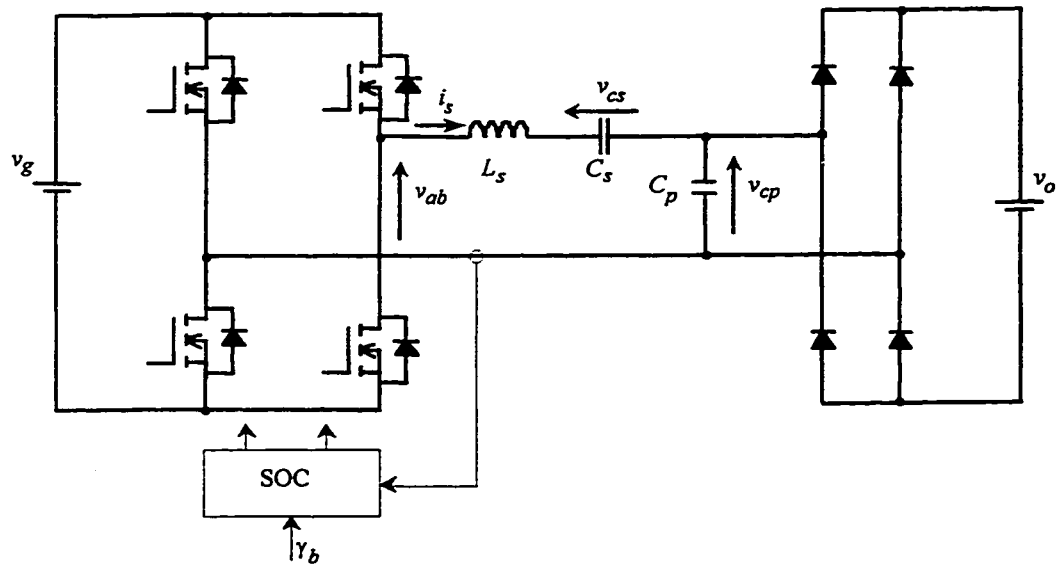


Fig. A4.1 Series-parallel resonant converter with capacitive output filter operating in self-sustained oscillation mode.

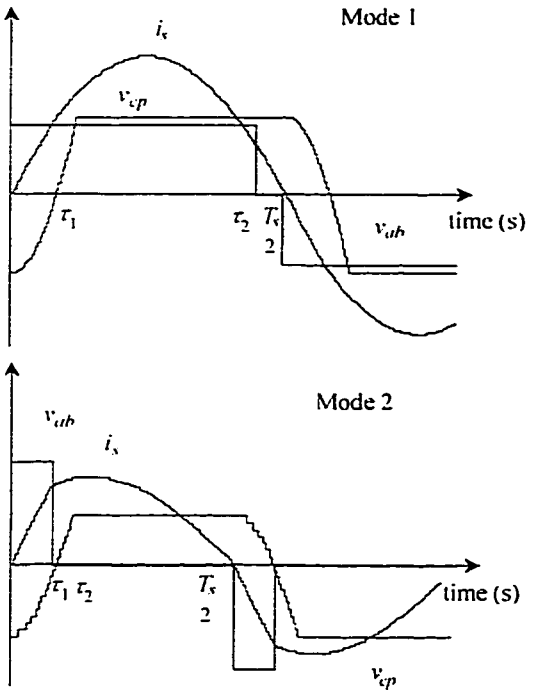


Fig. A4.2 Modes of operation

Let us consider that the series-parallel resonant converter operates cyclically with a succession of linear time invariant circuit configurations in each cycle. By piecing together the solution of each circuit configuration, the converter can be described by a non-linear sampled-data model of the following form:

$$x_{k+1} = f(x_k, u_k) \tag{A4.1a}$$

$$\sigma(x_k, u_k) = 0 \quad . \tag{A4.1b}$$

The entries of the vector x_k are the variables of the converter sampled at the instant that the current i_s crosses zero, and it is given by $x_k = [i'_s(t_k)\ v'_s(t_k)\ v'_{cp}(t_k)\ x_s(t_k)\ s_f(t_k)]^T$. The symbol ' marks the normalized variable as defined in Appendix 2. On the other hand, the input vector u_k is comprised of two vectors, that is, $u_k = [\ p_k\ ,\ w_k\ ]$. The entries of the vector w_k are the indirectly-controlled-transition-times. For the modes of operation of

Fig. A4.2 the vector w_k is defined as $w_k = [\tau_1 \ \tau_2]^T$. Finally, the vector p_k contains the independent sources of the circuit, that is, $p_k = [v'_g \ v'_o \ V_p]^T$.

The function $f(.)$ for the Mode 1 operation can be found as:

$$f(x_k, u_k) = \Phi_2(\frac{T_s}{2} - \tau_2)\{\Phi_2(\tau_2 - \tau_1)[(\Phi_1(\tau_1)\Phi_0 W x_k + \Psi_1(\tau_1) I_1 p_k] + \Psi_2(\tau_2 - \tau_1) I_1 p_k\} + \Psi_2(\frac{T_s}{2} - \tau_2) I_2 p_k \tag{A4.2}$$

where the matrices Φ_0, Φ_1, Φ_2 and W are defined as in Appendix 2. The other matrices are given by:

$$\Psi_1(\tau) = \begin{bmatrix} \frac{\sin(\sqrt{(1+\beta)}\,\tau)}{\sqrt{1+\beta}} & 0 & 0 \\ \frac{1-\cos(\sqrt{(1+\beta)}\,\tau)}{(1+\beta)} & 0 & 0 \\ \frac{\beta(1-\cos(\sqrt{(1+\beta)}\,\tau))}{(1+\beta)} & 0 & 0 \\ 0 & 0 & \frac{k_{p1}}{\upsilon\omega_0}\sin(\upsilon\tau) \\ 0 & 0 & 1-\cos(\upsilon\tau) \end{bmatrix} \tag{A4.3}$$

$$\Psi_2(\tau) = \begin{bmatrix} \sin(\tau) & -\sin(\tau) & 0 \\ 1-\cos(\tau) & -1+\cos(\tau) & 0 \\ 0 & 0 & 0 \\ 0 & 0 & \frac{k_{p1}}{\upsilon\omega_0}\sin(\upsilon\tau) \\ 0 & 0 & 1-\cos(\upsilon\tau) \end{bmatrix} \tag{A4.4}$$

$$I_1 = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \quad I_2 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{A4.5}$$

(A4.6), (A4.7), (A4.8),

On the other hand, the entries of the vector function $\sigma(.)$ are the constraint equations related with the event that characterizes the end of each circuit configuration. For Mode 1 of operation the vector function $\sigma(.)$ is given by:

$$\sigma(x_k, u_k) = \begin{bmatrix} [(\Phi_1(\tau_1)\Phi_0 W x_k + \Psi_1(\tau_1) I_1 p_k]_3 - v_0 \\ [\Phi_2(\tau_2 - \tau_1)[(\Phi_1(\tau_1)\Phi_0 W x_k + \Psi_1(\tau_1) I_1 p_k] + \Psi_2(\tau_2 - \tau_1) I_1 p_k]_5 - v_{ca} \\ [\Phi_2(T_s/2 - \tau_2)[\Phi_2(\tau_2 - \tau_1)[(\Phi_1(\tau_1)\Phi_0 W x_k + \Psi_1(\tau_1) I_1 p_k] + \Psi_2(\tau_2 - \tau_1) I_1 p_k] + \Psi_2(Ts/2 - \tau_2) I_2 p_k]_1 \end{bmatrix} \tag{A4.9}$$

In the same manner, for the Mode 2 of operation the functions $f(.)$ and $\sigma(.)$ are given by:

$$f(x_k,u_k)=\Phi_2(\frac{T_s}{2}-\tau_2)\{\Phi_2(\tau_2-\tau_1)[(\Phi_1(\tau_1)\Phi_0 Wx_k+\Psi_1(\tau_1)I_1p_k]+\Psi_2(\tau_2-\tau_1)I_2p_k\}+\Psi_2(\frac{T_s}{2}-\tau_2)I_2p_k \quad \text{(A4.10)}$$

and

$$\sigma(x_k,u_k)=\begin{bmatrix}[(\Phi_1(\tau_1)\Phi_0 Wx_k+\Psi_1(\tau_1)I_1p_k]_5-v_{co}\\ [\Phi_2(\tau_2-\tau_1)[(\Phi_1(\tau_1)\Phi_0 Wx_k+\Psi_1(\tau_1)I_1p_k]+\Psi_2(\tau_2-\tau_1)I_2p_k]_3-v_0\\ [\Phi_2(T_s/2-\tau_2)[\Phi_2(\tau_2-\tau_1)[(\Phi_1(\tau_1)\Phi_0 Wx_k+\Psi_1(\tau_1)I_1p_k]+\Psi_2(\tau_2-\tau_1)I_2p_k]+\Psi_2(Ts/2-\tau_2)I_2p_k]_1\end{bmatrix} \quad \text{(A4.11)}$$

A4.2 STATIC CHARACTERISTICS AND BOUNDARY

The boundary between the Mode 1 and 2 of operation in the circuit parameter space can be found by solving (A4.10) and (A4.11) for its steady-state solution with $0>\tau_1=\tau_2>T_s/2$ using different circuit parameters. The result of this procedure is plotted in Fig. A4.3. Once the boundary between the modes of operation are found the static characteristics of the converter can be obtained. The voltage conversion ratio for the series-parallel resonant converter operating with capacitive output filter under VFPSM is given in Fig. A4.4 and Fig. A4.5.

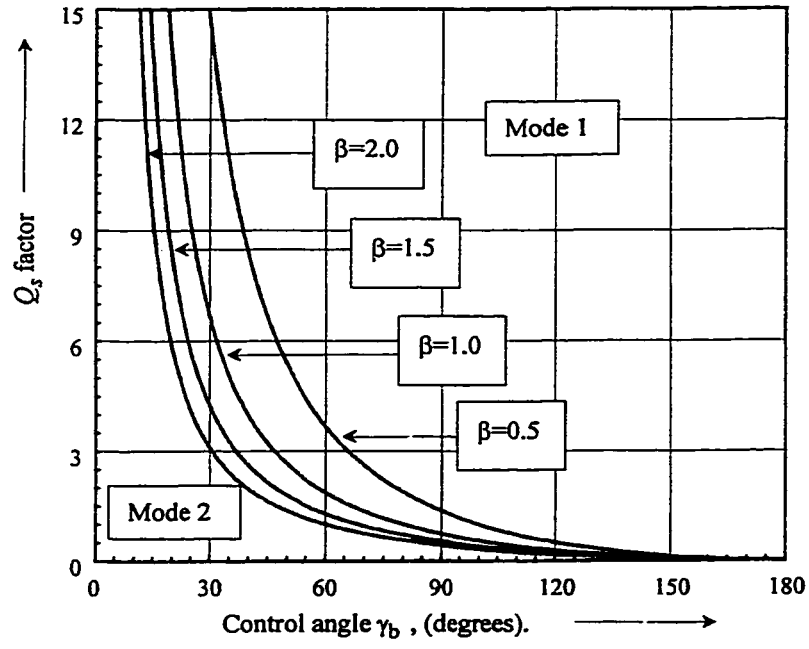


Fig. A4.3 Boundaries between the modes of operation. VFPSM .
$\gamma_a=180^o$.

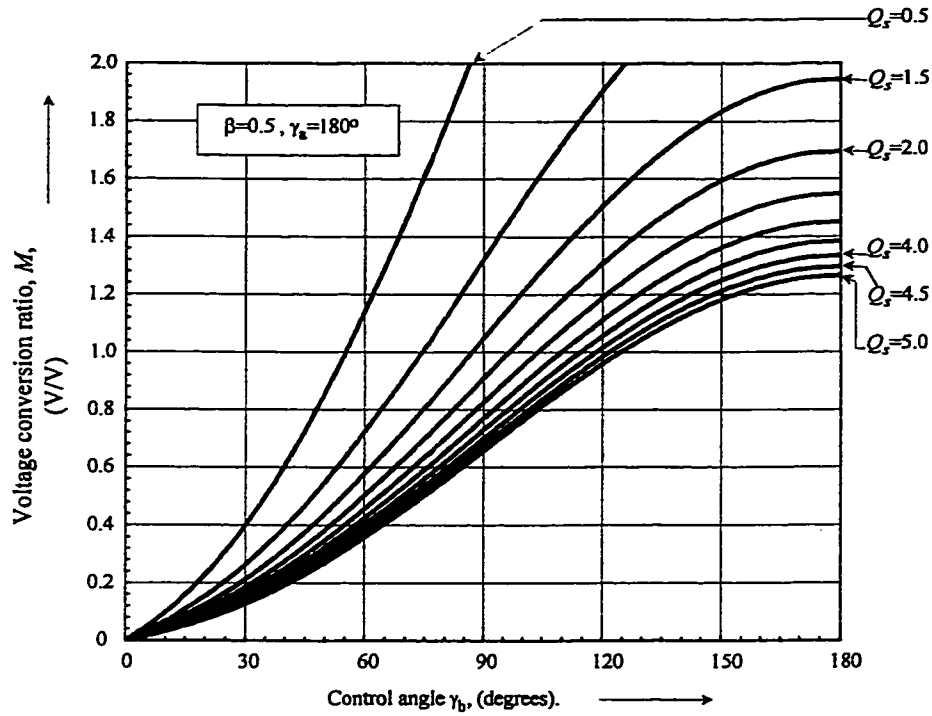


Fig. A4.4 Voltage conversion ratio as a function the control angle.
VFPSM with capacitive output filter.

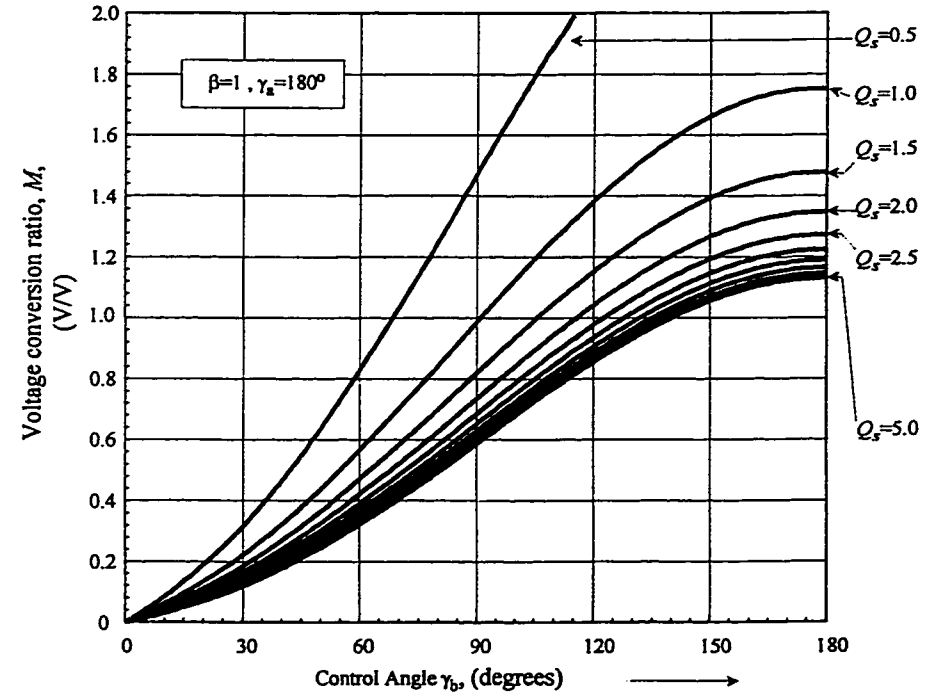


Fig. A4.5 Voltage conversion ratio as a function the control angle.
VFPSM with capacitive output filter.

A4.3 Operation with Unity Input Power Factor

In order to find the maximum voltage conversion ratio of the ac-to-dc converter the same procedure presented in Section 3.3 is adopted. The first step is to find the control angle at the resonance frequency. Then in a second step, the maximum voltage conversion ratio of the dc-to-dc converter is represented in terms of a map from Q_s to M. This map for typical values of β is shown in Fig. A4.7. Finally, the ac-to-dc maximum voltage conversion ratio is found from the minimum of the product defined by (3.14), which is illustrated Fig. A4.8. Fig. A4.9 summarizes the maximum voltage conversion ratio for operation with unity power factor and constant output voltage. Furthermore, Fig. A4.10 presents the switching frequency ratio at the peak of the input of the incoming ac line, which together with Fig. A4.9 constitute the key information for the selection of the resonant circuit parameters as demonstrated in Section 3.7.

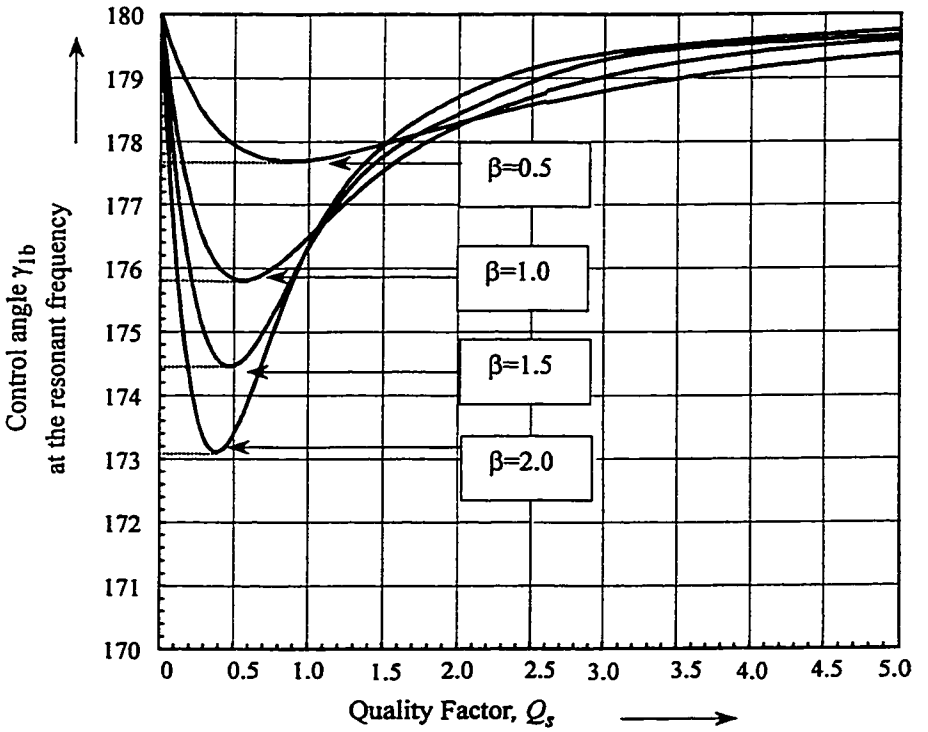


Fig. A4.6 Control angle γ_{1b} at the resonant frequency for operation with VFPSM and with capacitive output filter.

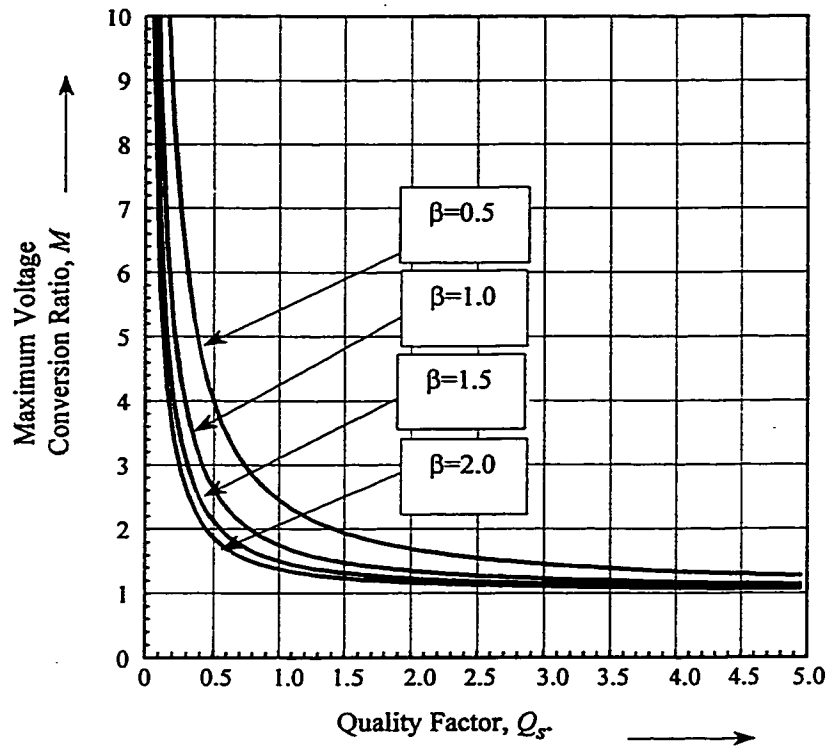


Fig. A4.7 Maximum gain of the converter for operation with VFPSM.
(γ_a=180°. γ_b=178.6° for β=0.5. γ_b=175.8° for β=1. γ_b=174.4° for β=1.5. γ_b=173.1° for β=2)

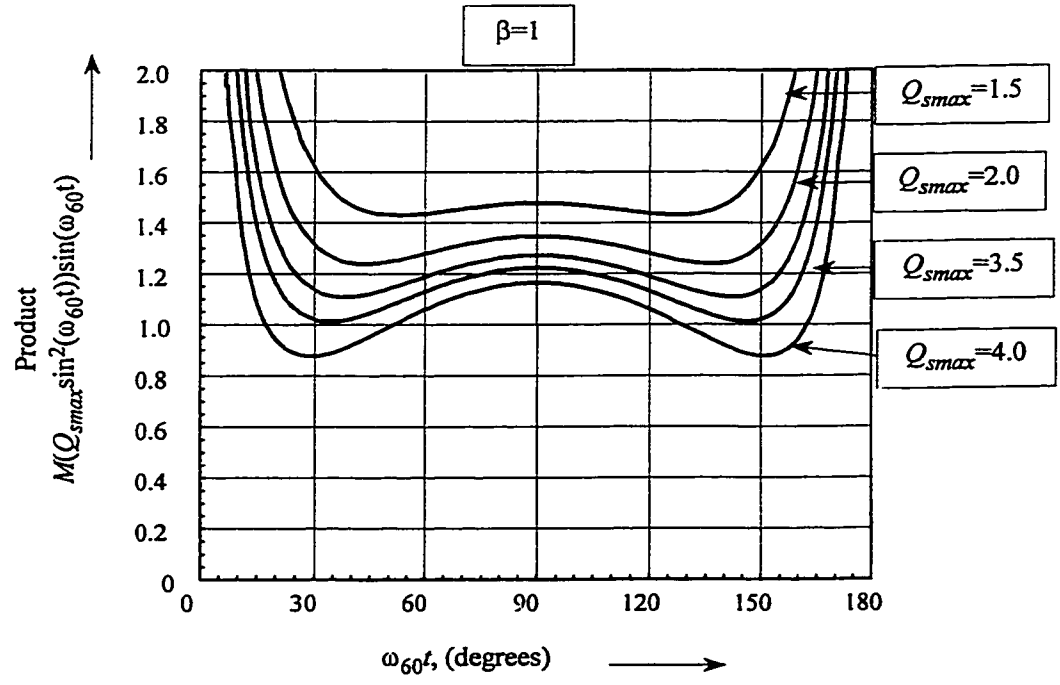


Fig. A4.8 Product $M(Q_{smax}\sin^2(\omega_{60}t))\sin(\omega_{60}t)$ for different values of Q_{smax}.
(γ_a=180°, γ_b=174°,β=1)

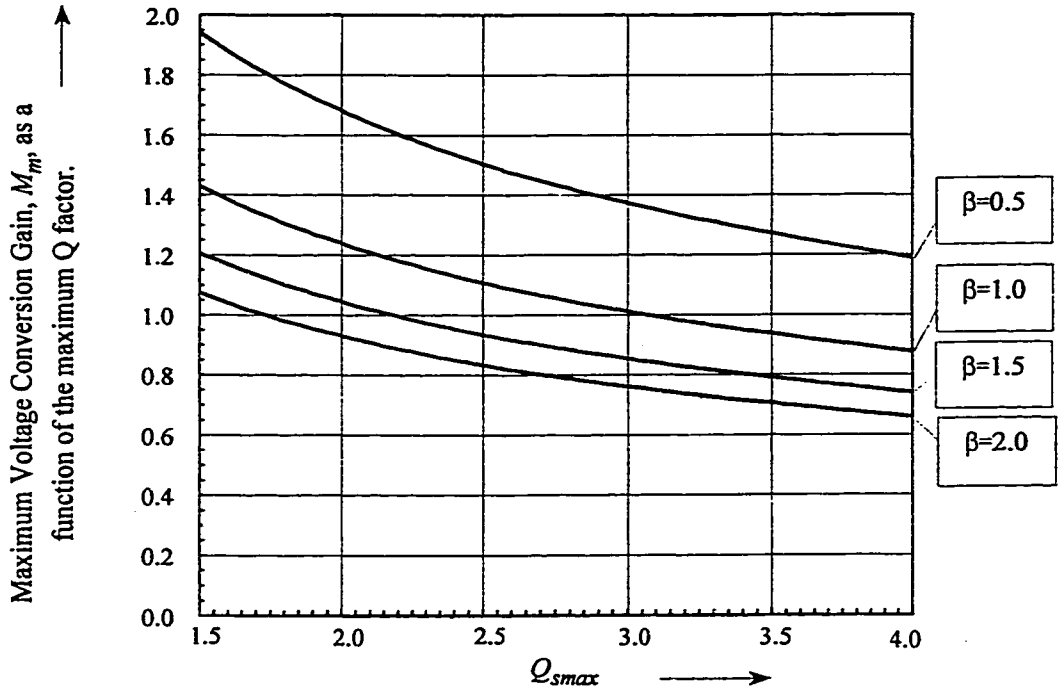


Fig. A4.9 Maximum voltage conversion ratio for operation with constant output voltage and unity input power factor. Operation with capacitive output filter.

(γ_a=180°, γ_b=176° for β=0.5, γ_b=174° for β=1, γ_b=172° for β=1.5, γ_b=170.5° for β=2)

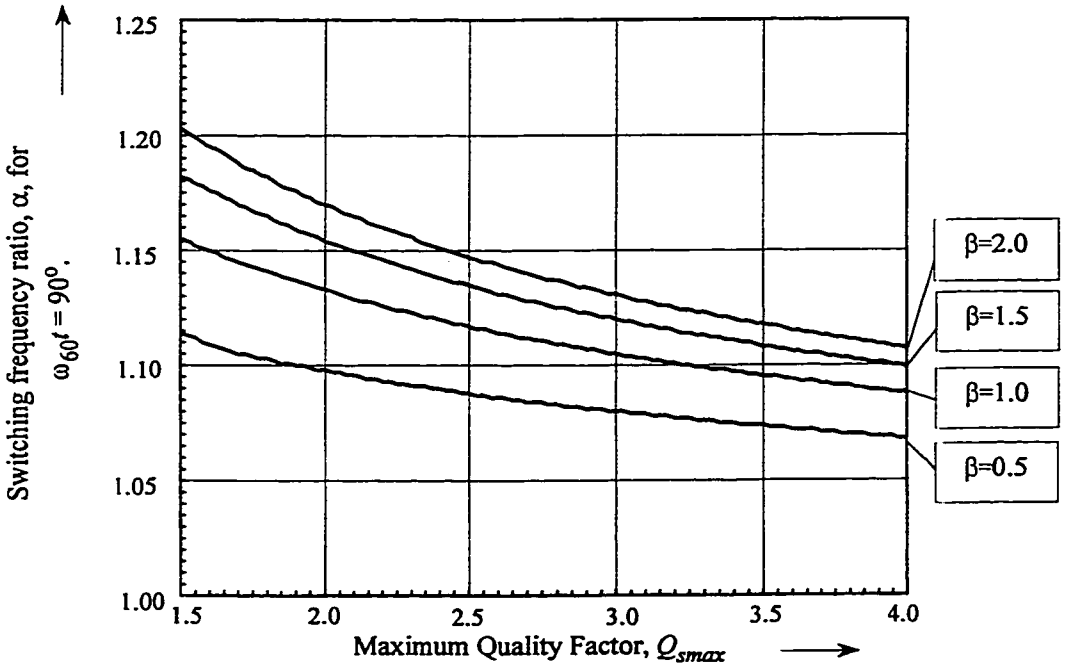


Fig. A4.10 Switching frequency ratio at $\omega_{60}t$=90°. Operation with VFPSM and with capacitive output filter.

(γ_a=180°, γ_b=176° for β=0.5, γ_b=174° for β=1, γ_b=172° for β=1.5, γ_b=170.5° for β=2)

APPENDIX 5: CIRCUIT DIAGRAMS

A5.1 SERIES-PARALLEL BASED UPS WITH INDUCTIVE OUTPUT FILTER

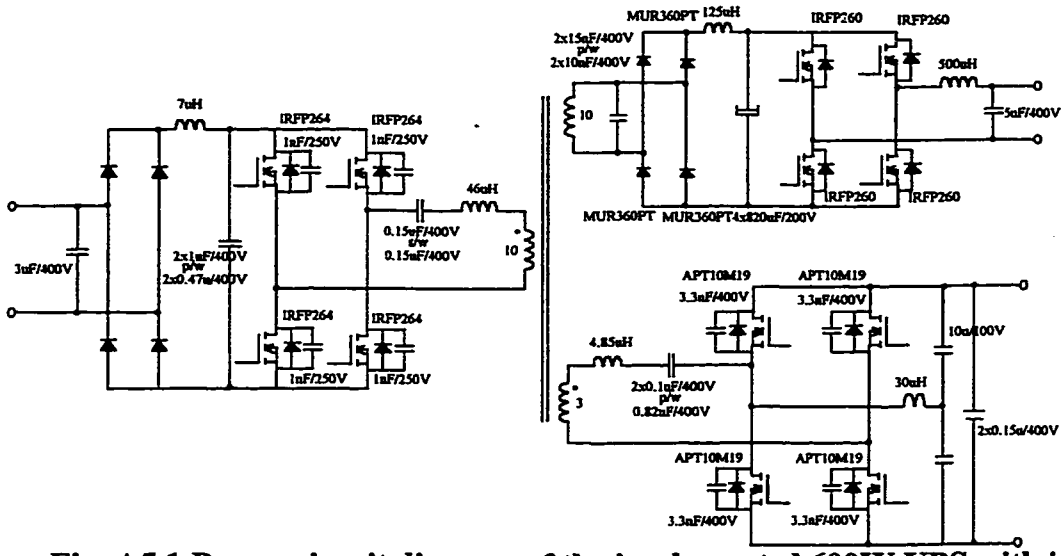


Fig. A5.1 Power circuit diagram of the implemented 600W UPS with inductive output dc bus filter.

s/w stands for "in series with" and p/w for "in parallel with".

A5.2 SERIES-PARALLEL BASED UPS WITH CAPACITIVE OUTPUT FILTER

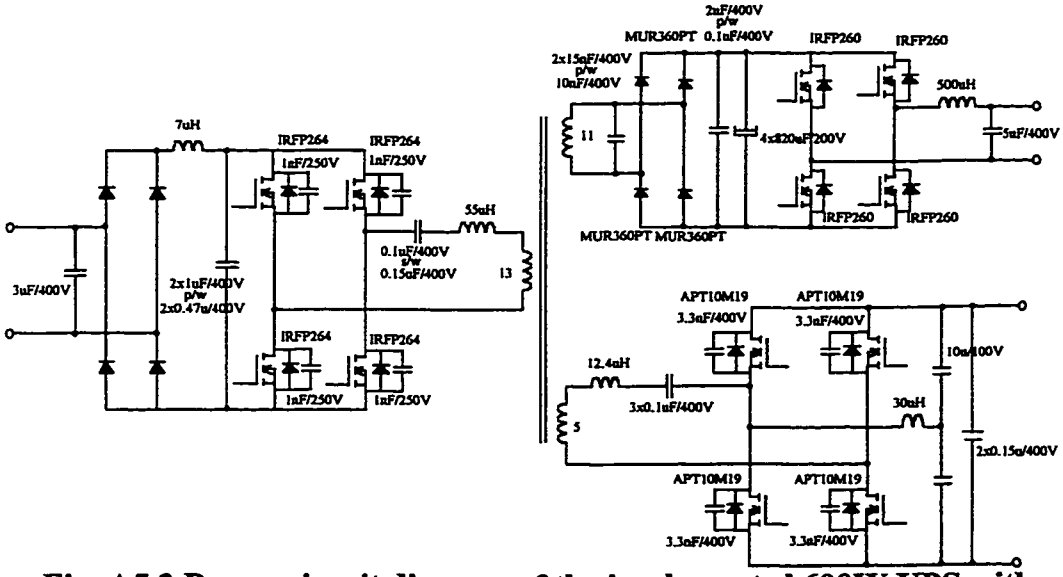


Fig. A5.2 Power circuit diagram of the implemented 600W UPS with capacitive output dc bus filter.

s/w stands for "in series with" and p/w for "in parallel with".

A5.3 SERIES RESONANT BASED UPS

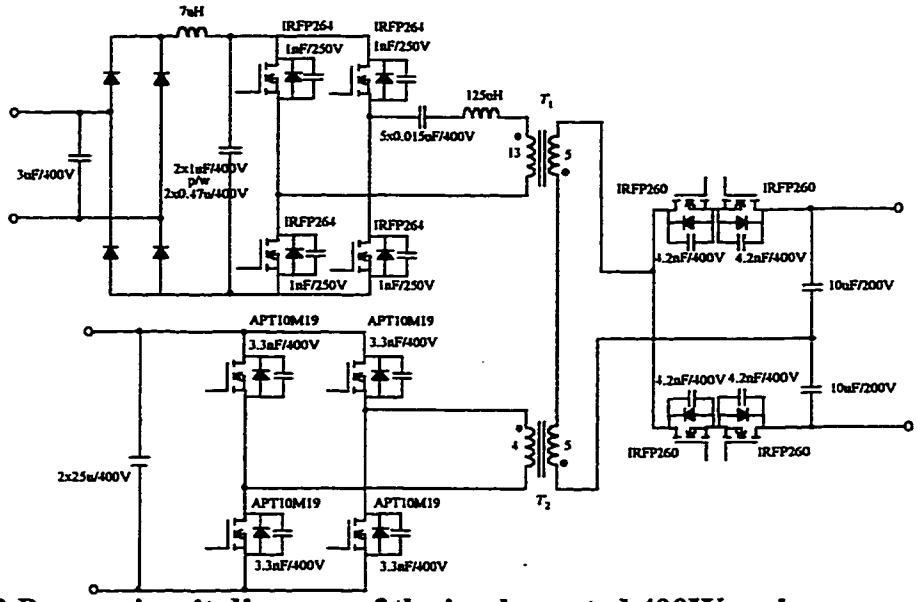


Fig. A5.3 Power circuit diagram of the implemented 400W series resonant based UPS.

A5.4 SELF-SUSTAINED CONTROLLER

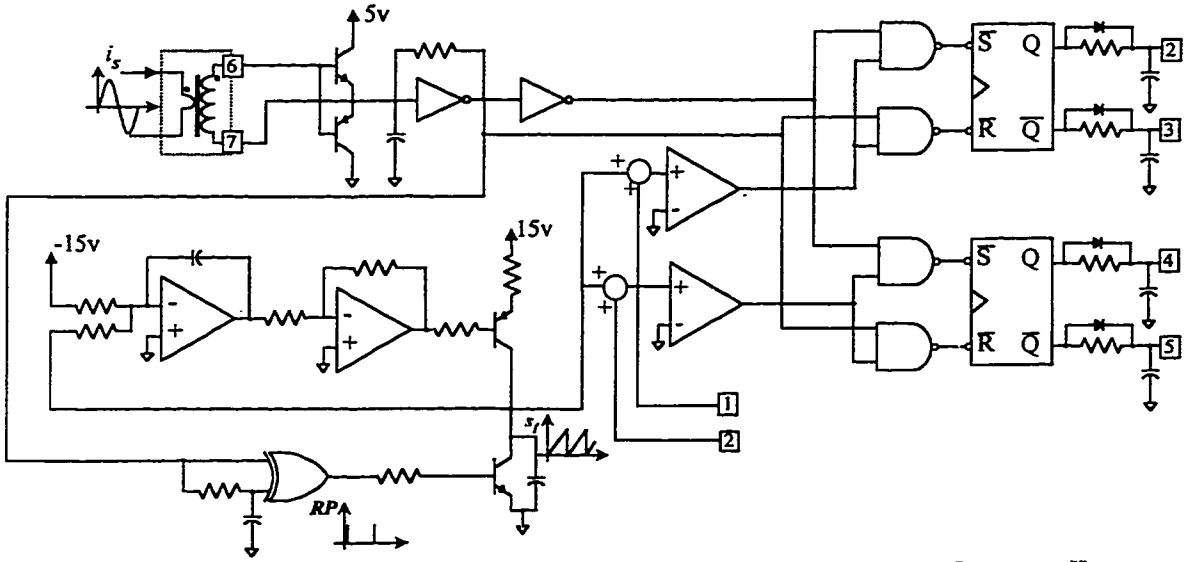


Fig. A5.4 Circuit diagram of the inplemented self-sustained controller.

Pins 1,2: Control voltage for the converter's legs A and B respectively. **Pins 2,3:** Output voltage required to generate the gate signals of the leg A. **Pins 4,5:** Output voltage required to generate the gate signals of the leg B. **Pins 6,7:** Terminals for the connection of the current transformer.

APPENDIX 6: HYBRID FIBER-COAXIAL NETWORKS

Fig. A6.1 shows a typical hybrid fiber-coaxial network, which can carry video, telephony, and broadband signals to the subscribers. This network consists of (i) headend and fiber cable, (ii) coax node and power insert node, (iii) drop boxes and drop cables, and (v) home termination units.

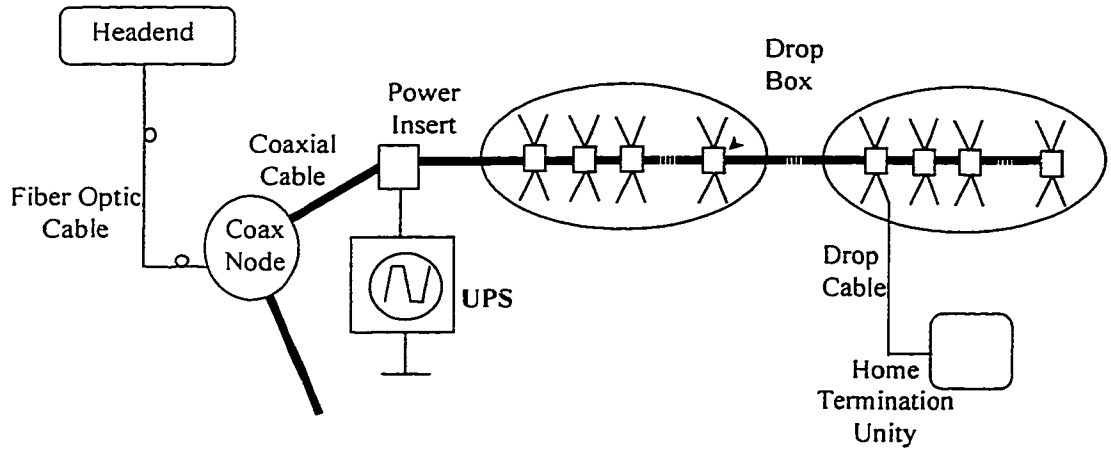


Fig. A6.1 Hybrid Fiber/coaxial network.

In the headend stations the communication signal are received and converted into optical signals [6]. Then, fiber optic cables are used to carry the communication signals between the headend and the coax nodes. At the coax node the communication signals are converted from optical to electrical form and then they are distributed to the subscribers over the coaxial cable. In addition to the communication signals, the coaxial cable can also carry power, which is required to provide the basic telephony services.

Different alternatives for powering hybrid fiber-coaxial networks have been considered in the literature [6-8]. Among the factors that bound the selection of the

distribution voltage, frequency and power are: (i) loading capability, (ii) safety and code compliance, and (iii) corrosion.

Powering hybrid fiber-coaxial networks with 90V trapezoidal voltage at 60 Hz (or 1Hz) has been demonstrated to be an optimal compromise between the above mentioned factors. This is because the loading capability of the network increases with the amplitude of the distribution voltage. However, the maximum amplitude of the distribution voltage is limited at 90V by safety codes (National Electrical Safety Code, Bellcore). On the other hand, the factors that determine the selection of the distribution frequency are safety and corrosion. Higher frequency minimizes the weight losses of the coaxial cable, however the safety voltage reduces with the frequency [7]. As a result, both 60 Hz and 1Hz have been adopted. Finally, trapezoidal waveform has been selected since it results in higher network loading capability when compared with the sinusoidal waveform. This is due to the fact that the network is loaded with nonlinear loads which are associated with the amplifiers and the power supplies at the home termination units.

Table A6.1 summarizes the main output features of a UPS for powering hybrid fiber/coaxial networks.

TABLE A6.1 UPS REQUERIEMENTS

Output Voltage	90 V rms
Output Voltage Waveform	Trapezoidal with rising and falling-edge slew rate of 100 +/- 50 mV/μs.
Frequency	60 Hz
Input Voltage	92V - 138 V rms
Maximum Power (limited by Bellcore)	1350 W

APPENDIX 7: COMPARISON OF VARIOUS UPS TOPOLOGIES

In this appendix four distinct uninterruptible power supply topologies for powering fiber-coaxial networks are compared. Three of these UPS are described and their performances presented in the next sections. The fourth UPS topology is the series-parallel resonant based UPS, which is described in detail in Chapter 4.

A7.1 FERRORESONANT-BASED UPS (TOPOLOGY A).

A7.1.1 Circuit Description

Fig. 1.1 shows the main elements of the ferroresonant-based UPS. The UPS is comprised of a ferroresonant transformer, an inverter, and a battery charger. The ferroresonant transformer has three windings, the line side winding, the battery side winding and the output side winding and it couples the input ac line and battery side inverter to the load. In addition, the ferroresonant transformer has a magnetic shunt that provides a path for the leakage flux between the line side winding (or the inverter side winding) and the output side winding. The inverter operates at low frequency. an it produces a quasi-square ac waveform that drives the ferroresonant transformer during the failure of the incoming ac voltage.

A7.1.2 Operating Principle

When the input voltage is within the acceptable input voltage range, usually +/- 20% of its nominal value, power is transferred from the incoming ac line to the output.

(the switch S_1 is closed and the switch S_2 is open). At the same time, an external battery charger provides the required voltage (or current) to charger the battery. During this mode, the leakage inductance of the transformer combined with the output capacitor form a resonant circuit at the incoming ac line frequency. The limiting action of the saturation characteristics of the ferroresonant transformer provides a way to regulate the output voltage over the acceptable input voltage range. Upon the failure of the incoming ac line, the states of the switches S_1 and S_2 are reversed and then the inverter is activated. During this mode, the leakage inductance of the transformer combined with the output capacitor is used to filter the harmonics generated by the inverter.

A7.1.3 Converter Performance

In order to evaluate the performance of the ferroresonant-based UPS a π model of the ferroresonant transformer is used [12]. The π-model of the ferroresonant transformer is shown in Fig. A7.1. The inductor L_s, of the π model, is associated with the flux through the magnetic shunt of the ferroresonant transformer while the non-linear inductance L_2 is associated with the saturable secondary magnetic path that is used to regulate the output voltage. The nonlinear inductor L_2 was simulated using the Jiles-Atherton model where the parameters are the ones given in [12]. The parameter used in the Pspice simulation are: L_1=345mH; R_1=0.1Ω; L_s=5.7mH; R_2=0.05; R_s=0.05; C_f=1200μF. The parameters of the nonlinear inductor L_2 are: magnetization saturation MS = 1.5 10^6, thermal energy A = 150, Area = 29, Path = 23.

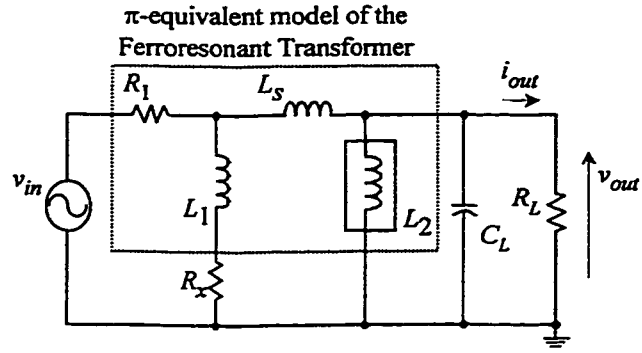


Fig. A7.1 Pspice circuit model used for simulation of the ferroresonant UPS.

Based in this model the transient response of the ferroresonant-based UPS due to a step change in the load was obtained, and it is shown in Fig. A7.2. It is possible to see that the output voltage drops during the load transient and restores to the nominal value with in one cycle.

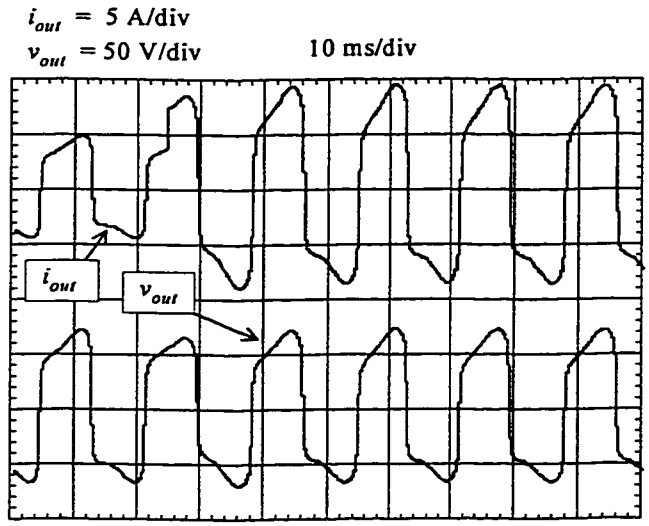


Fig. A7.2 Simulation results. Load step transient from 185 to 370 W.

Fig. A7.3 shows the transient in the output voltage during a swell in the input ac line. It is possible to see that the output voltage during the transient reaches almost two times its nominal value. After the transient, that lasts about five cycles, the rms value of

the output voltage returns to its nominal value as a result of the regulating action of the ferroresonant transformer.

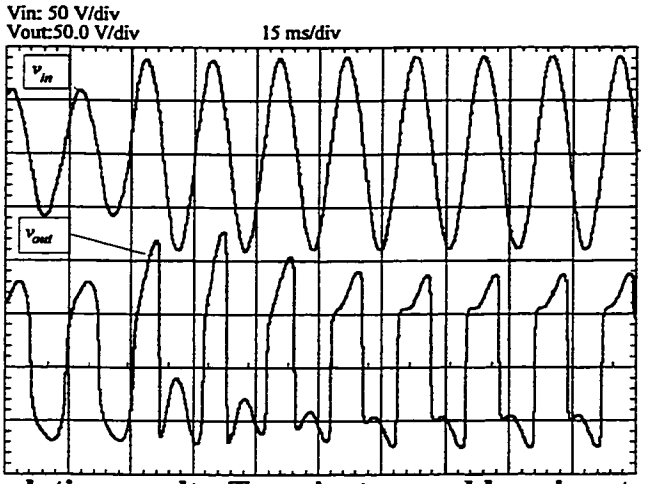


Fig. A7.3 Simulation results. Transient caused by a input voltage swell.
Top: Ac input voltage transient, v_{in} changes from -20 % to +20% of its nominal value; Bottom: Output voltage transient due to the variation in the input voltage.

The steady-state characteristics of the ferroresonant-based UPS are shown in Fig. A7.4. The efficiency approaches 88% as the load increases. However, the efficiency at a fraction of full load is considerable lower. The input power factor is acceptable, however the total harmonic distortion of the input current is high, especially when operating with a fraction of the full load.

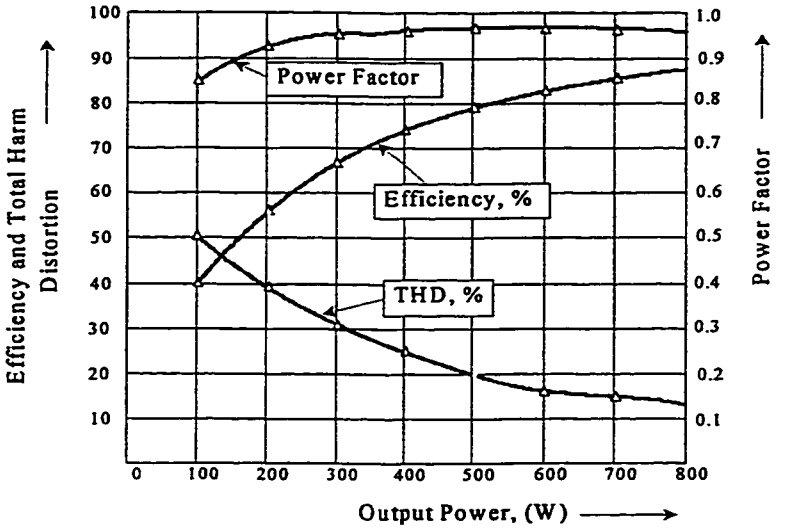


Fig. A7.4 Input power factor, efficiency, and total harmonic distortion of the input current as a function of the output power for the UPS topology A.

A7.2 LINEAR 60 HZ TRANSFORMER BASED UPS (TOPOLOGY B).

A7.2.1 Circuit Description

Fig.1.2 shows the power circuit diagram of the linear 60 Hz transformer based UPS. The main elements of this UPS are: (i) a single phase full wave diode bridge rectifier, located at the incoming line side, (ii) a PWM inverter with a second order low pass output filter, (iii) a 60 Hz transformer, (iv) a battery disconnect (S_1), and (v) a battery charger.

A7.2.2 Operating principle

This topology operates in two different modes depending on the regulation of the ac input voltage, v_{in}. The first one occurs when the input voltage is within the acceptable range. In this mode, the incoming ac line supplies the load power through the PWM inverter while the switch S_1 is kept opened to avoid the discharge of the battery. In

addition. in order charger the battery. an external battery charger is used. On the other hand. the second mode starts upon the failure of the incoming ac line. At this instant the switch S_1 is closed connecting the battery to the input dc bus. Therefore. during this mode, the battery supplies power to the load though the inverter, ensuring, in this way, continuous operation to the output load.

In order to operate with high input power factor. without additional power factor correction stage or other circuitry. it was propose in [24] to use a small capacitor in the input dc bus. In this way, when the input ac line is normal, the input dc bus voltage is pulsating. as it assumes the shape of an absolute value of a sine wave resultant of the rectification of the incoming ac line. In order to avoid the adverse effect of the dc bus voltage pulsation on the output voltage, the output voltage is synchronized with the incoming ac line. In this way, it is possible to achieve a high quality output voltage waveform by the active control the output voltage. It has been demonstrated in [24] that when operating with resistive output load the resulting input power factor is high, and the requirements. which are imposed by regulatory agencies. limiting the low frequency harmonics injected in the utility grid can be easily satisfied. It is worth mentioning that to ensure the proper operation of the output inverter the output voltage has to be smaller than the dc bus voltage. However, this does not represent a limitation since the turns ratio of the output transformer can be adjusted to result in the required output voltage level.

A7.2.3 Converter performance

The transient performance of the UPS under the input supply and load transient conditions are given in Fig. A7.5 and Fig. A7.6. For the results shown in these figures, the voltage across the inverter terminals is actively controlled. An integral type controller

with a trapezoidal reference voltage in phase with the ac input line voltage has been adopted. With this controller the fluctuations and disturbances coming from the ac line are attenuate. From Fig. A7.5 it is possible to observe that the output voltage presents an oscillation that features an undershoot of 25 % and a settling time of about 500 μs. On the other hand, Fig. A7.6 shows that even with a supply step change of 50 % the output voltage presents a small oscillation.

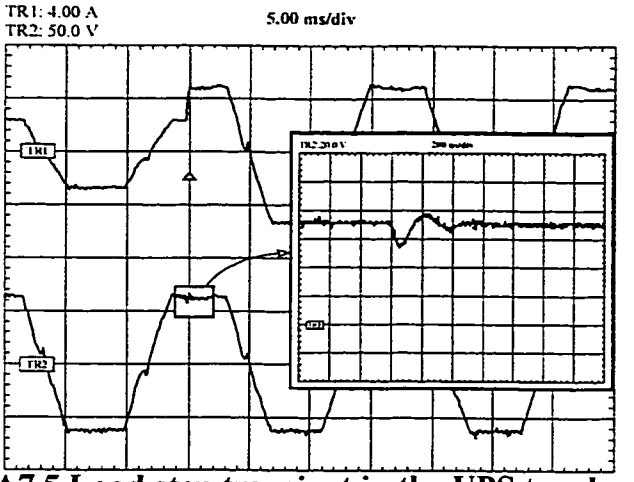


Fig. A7.5 Load step transient in the UPS topology B.
(Transient from 200 to 400 W - experimental waveforms).
TR1: Output current. TR2: Output voltage.

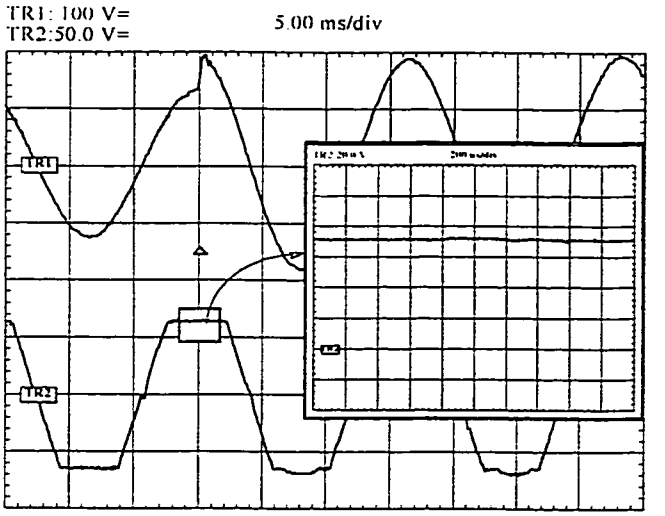


Fig. A7.6 Ac supply voltage transient in the UPS topology B
(85 to 135 V step increase at 400 W output - experimental waveforms). TR1: Supply voltage. TR2: Load voltage.

On the other hand, Fig. A7.7 shows the static performance of UPS topology. From this figure, it is possible to conclude that:

(i) the input power factor is acceptable, around 0.93, and the of the input current is THD high around 40%.

(ii) the efficiency is very high 93%, and it is almost constant for a wide range of output load.

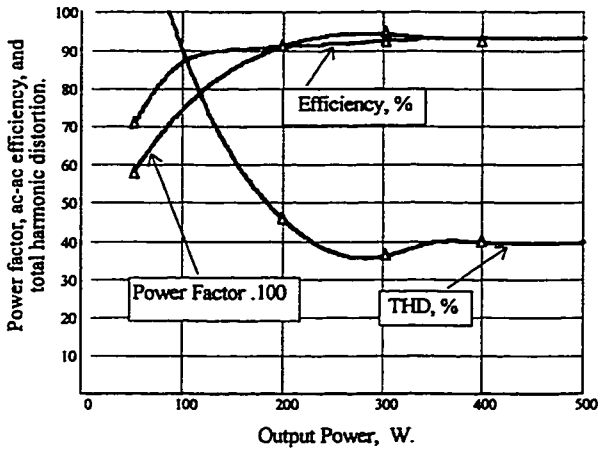


Fig. A7.7 Static performance as a function of the load. UPS topology B. v_{in}=110 V.

A7.3 CONVENTIONAL HIGH FREQUENCY TRANSFORMER UPS (TOPOLOGY C)

A7.3.1 Circuit description

Fig. 1.3 shows the power circuit diagram of a conventional rectifier-inverter UPS based on high frequency transformer. The rectifier consists of a boost pre-regulator cascaded with an isolated dc-to-dc converter. At the output side another boost converter is used to step-up the battery voltage to a value higher than the peak of the output voltage.

Finally, a PWM inverter generates the output trapezoidal ac waveform from the output dc bus voltage.

A7.3.2 Operating principle

The converter connected to the incoming ac line is a boost pre-regulator, which is comprised of the inductor at the ac line side, the switch S_1, the diode D_1, and the boost capacitor, Fig. 1.3. The boost pre-regulator has been widely used for power factor correction because of its simplicity. In addition, when it operates in continuous conduction mode of the input inductor current the THD of the input current is very low and the input power factor is close to one. On the other hand, the average value of the output of the boost pre-regulator (the input dc bus voltage) is regulated at a value that is larger than the peak of the incoming ac line voltage. This voltage is used to feed an isolated dc-to-dc converter that interfaces the input dc bus and the battery. Whenever the incoming ac voltage is within the acceptable voltage range the dc-to-dc converter keeps the battery current at the required value against variations in the input dc bus voltage and output load current. The dc-to-dc resonant converter, which is described in [47], was selected for this UPS topology. The dc-to-dc resonant converter consists of an inverter, a series parallel tuned resonant circuit, and an output diode rectifier. The inverter (S_2, S_3, S_4, S_5) operates at high frequency and it is controlled using phase-shift modulation, therefore, its output voltage is a high frequency quasi-square voltage. The application of this high frequency quasi-square voltage across the combination of the series and parallel branches of the resonant circuit allows the operation of the inverter's switches with ZVS in a wide range of phase shift angle, and results in a stiff almost sinusoidal voltage across the high frequency transformer. A detailed description of the operating intervals of the

dc-to-dc resonant converter and the design guidelines for the selection of the resonant circuit parameters are found in [47]. However, here, just its main characteristics will be pointed out, i.e.: (i) the circulating currents are confined within the parallel branch of the resonant circuit resulting in high converter efficiency from full-load to reduced-load, (ii) the switching losses are near zero, since the turn-on and turn-off of the switches occurs under zero voltage over a wide range of phase-shift angle, and (iii) the voltage stresses across the output diode rectifier are reduced due to the parallel resonant capacitor.

In the rectifier-inverter type of UPS, the battery is placed between the input rectifier and the output inverter stage. Usually, the battery voltage is smaller than the value required for the synthesis of the output voltage using a conventional PWM inverter. In order to step-up the battery voltage to the required value a boost converter can be used. Therefore, this boost interfaces the battery and the output inverter. In Fig.1.3, this boost converter consists of the inductor L_3, the switch S_6, the diode D_2, and an output boost capacitor. The operation in continuous conduction mode of the current through the inductor L_3 was selected since it results in smaller current stresses. The duty cycle of the output boost is almost constant since neither the battery voltage nor the output dc bus voltage vary significantly. Finally, the PWM inverter (S_7, S_8, S_9, S_{10}) generates the desired trapezoidal output waveform from the output dc bus voltage, and a second order low pass filter attenuates the high frequency components produced by the PWM inverter.

A7.3.3 Converter performance

The output transient performance of the UPS topology depends primarily on the output inverter design. For the design purpose, first the switching frequency is defined to keep the switching losses at acceptable value. Aiming to limit the switching losses at a

reasonable value the switching frequency of the output inverter was selected to be 20 kHz. The efficiency of the output inverter as well as the efficiency of the output boost converter as a function of the load are given in Fig. A7. 8.

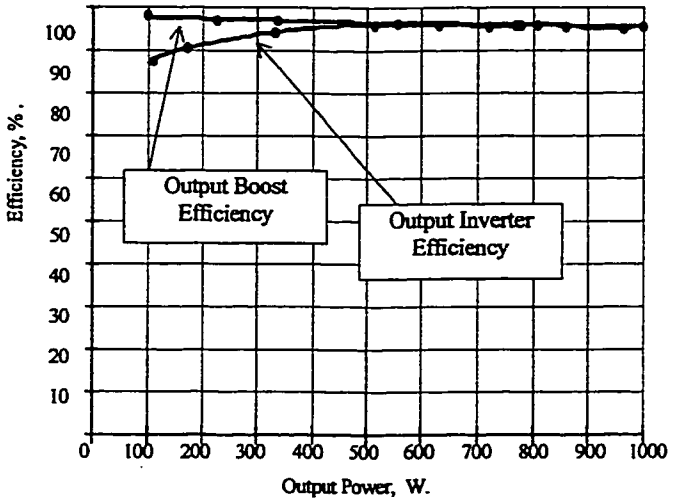


Fig. A7. 8 Output boost and output inverter efficiencies as a function of the load. Switching frequency 20 kHz.

The selected transistor for the implementation of these converters was the IRFP250 and the boost diode the MUR 1504. v_o = 110 V, v_{bat}=56 V.

The output inverter of this topology is identical to the one described in Section 4.5, therefore, the output transient response follows the one presented in Section 4.6.4. On the other hand, the static performance of the conventional high frequency transformer based UPS was found by combining the static characteristics that define the performance of the boost pre-regulator and the dc-to-dc resonant converter given in [47] with the efficiency of the output boost and inverter obtained from a experimental setup. The overall static performance of the conventional high frequency transformer based UPS is shown in Fig. A7.9. From this figure, it is possible to conclude that: (i) the input power factor is high, around 0.99, for operation at full load. (ii) the full-load overall efficiency of the UPS is about 81%.

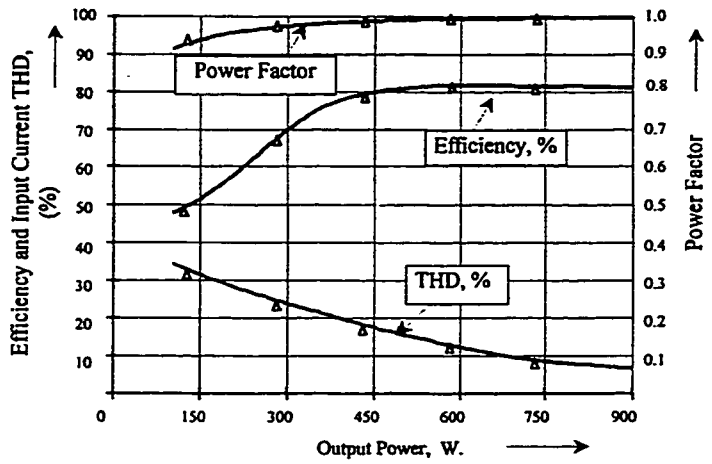


Fig. A7.9 Efficiency, power factor and total harmonic distortion as a function of the load for the UPS topology C.

v_{bat}= 56V.

A7.4 DISCUSSION

The results obtained in the previous sections are summarized in Table A1.1. In addition, the performance of the series-parallel UPS, which is described in Chapter 4, is included under the name of Topology D. It is possible to conclude from this table that the UPS topologies based on low frequency transformer present higher efficiency at full load than the one based on high frequency transformer. However, the transient response, the input power factor and total harmonic distortion of the input current of the high frequency based UPS topologies are superior than their counterpart based on low frequency transformer. This is because in the high frequency transformer based UPS topologies the input power factor is actively corrected and the intermediate energy storage elements provide an excellent buffer from the ac voltage transients to the output load. In addition, the size and weight of the high frequency UPS are much smaller and lighter than the low frequency transformer based UPS.

Fiber-coaxial networks can also be fed from power supplies that produce trapezoidal waveform of 90 V at 1Hz. In this case the UPS topologies based on low frequency transformer can no longer be used, since the isolation transformer becomes prohibitively bulky and heavy. Among the high frequency topologies, the series-parallel resonant based UPS offers a higher efficiency, during the line-operating mode, and the opportunity to simultaneously grounding the battery and the output.

TABLE A7.1 COMPARISON OF THE UPS TOPOLOGIES.

	Topology A	Topology B	Topology C	Topology D
Efficiency (*)	88%	93%	81%	87%
Power Factor (*)	0.95	0.93	0.99	0.99
THD (*)	13%	40%	7%	7 %
Quality of the output voltage	Poor	Very good	Excellent	Excellent
Transient Response	Poor	Good	Very good	Very good
Weight (approximate)	25 kg	15 kg	6 kg	5 kg
Volume (approximate)	1400 in^3	900 in^3	500 in^3	400 in^3
Isolation	Full	Partial	Partial	Full

(*) Operation at full load. The topology D is the series-parallel resonant based UPS of Chapter 4.

Topology A- Ferroresonant based UPS

Topology B- Linear 60 Hz transformer based UPS

Topology C- Conventional High Frequency Transformer UPS

Topology D- Series-parallel resonant based UPS