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A Bulk-Driven CMOS Voltage-to-Current Transconductor and its Applications

Yingtao Jiang

A Thesis

in

The Department

of

Electrical and Computer Engineering

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Abstract

A Bulk-Driven CMOS Voltage-to-Current Transconductor and its Applications

Yingtao Jiang

Techniques that can provide non-degraded performance at low power supply voltages and consuming less power are demanded and will continue to evolute. In this thesis a novel bulk-driven CMOS voltage to current transconductor (VCT) is introduced. In contrast with the conventional gate-driven transconductors, this new transconductor (called bulk-driven VCT) has great potential to be used in low power low voltage supply system. Characteristics (DC, AC, etc.) related to this VCT circuit have been investigated. Noise performance of the circuit has been studied as well. Simulation and test results on several prototype chips fabricated in a 1.5 micron CMOS process show close agreements between the theoretical and test results. The functional parameters versus power consumption of the new VCT is very impressive compared with similar gate-driven VCTs that have been reported in the literature.This bulk-driven VCT can be further used to synthesize many components (like resistors and inductors). Using VCT-based inductors, a large system (filter) has been built. Advantage and disadvantage of the synthesized filter system have been shown through simulation and test results respectively. This VCT circuit may find its applications in audio devices and biomedical equipment, in which a modest working frequency band and efficient power consumption are required.

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I would like to express my deep gratitude to my thesis supervisor, Dr. R. Raut, for his continual interest and insightful guidance during the course of this work. His great generosity and kindness have substantially improved the working environment during my past two studying years at Concordia. Also I want to gratefully acknowledge the VLSI Design Lab staff D. Hargreaves for his assistance. During my two-year stay in Montreal, I received enormous help from my friends and colleagues. I owe big thanks to them. Finally, I want to thank my beloved mother who really gives me the perspective I need the most for my future.

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Chapter 1

Introduction

Looking back to the history of microelectronics, we find that low power microelectronics was conceived through the invention of the transistor in 1947 and enabled by the invention of the integrated circuit in 1958. Through the following 39 years, low power design is one of the most active research areas and will keep on attracting huge attention in the foreseeable future. Bipolar is still the dominant technology in very high frequency applications. A bipolar transistor, compared to a MOS transistor, usually has an intrinsically higher transconductance; the silicon area required is less, therefore, resulting in less parasitics. However, in many systems power consumption is more important than area. CMOS offers very low standby currents and transistors with full capabilities at very low bias currents; thereby, leading to less power consumption. Not only does the CMOS distinguish itself in terms of lower power dissipation, but its ability to accommodate high performance analog devices and dense digital circuits on the same chip may prove to be an even more significant advantage in the future [1]. These advantages, combined with a lot more not mentioned here, provide the explanations why CMOS technology has been a major process technology in the past several decades and will continue its dominance in the foreseeable future. In this thesis, we will confine our focus only on CMOS technology used in

analogue signal processing.

1.1 Trends in Low Power Low Voltage Circuit Design

Trends in analog integrated circuit design unexceptionably have been employing low power design. Laptop computer disk drives, cellular telephone handsets, portable communicators and other applications mandate design for battery longevity [2]. These trends propose significant design challenges to the integrated circuit design engineer. Some analogue design techniques for low-voltage operation of CMOS continuous time filters [3], CMOS op amps with 3, 2 or even 1V with standard digitally-oriented process has been reported. This trend for lower supply voltages is giving rise to new design techniques for analogue circuits.

Generally, there are three possible approaches to achieve high performance analog circuits in CMOS technology at low power supply voltages. One is to multiply the lower voltage dc to larger values. Another is to modify existing CMOS digitally-oriented fabrication processes to accommodate low-voltage analog circuits. The third is to stay with the existing fabrication technology by using new circuit techniques [4]. Obviously, the last approach is more efficient since its compatibility with existing fabrication processes will drastically reduce the cost of designing, prototyping, and fabricating. We will stick to the third approach in this thesis as well.

1.2 Bulk-driven Operation of the MOSFETs

As we know, a MOSFET has four terminals: gate, source, drain and substrate (also called bulk). Almost all of the proposed circuit configurations are only using gate, source and drain terminals and keeping the bulk terminal connected to the most positive/negative

potentials, or to its corresponding source terminal if applicable. This technique thereafter will be named gate-driven. With the rising concern of the low voltage supplies and low power requirements, we have to unfold every possible approach that is available. As a matter of fact, the signal could be fed not only to the gate terminal, but to the bulk terminal as well. Consequently, a bulk-driven technique emerges.

Among the many possibilities to implement the third approach suggested in the previous section, bulk-driven MOSFET exhibits the potential in low power and low voltage analogue signal processing. It has been claimed that a current mirror using bulk-driven MOSFETs can have input voltages of 0.1-0.3 V and saturation output voltages similar to gate-driven MOSFET mirrors [4]. Some researchers even incorporate bulk-driven techniques to MOSFETs biased in weak inversion and the linear range has been extended by almost 100% [5].

1.3 Voltage to Current Transconductor (VCT)

Current-mode circuits [6] provide attractive and elegant solutions for analogue computation and signal processing, particularly when the voltage supplies shrink to 3.3V, 3V, or below. Linear transconductors or voltage-to-current converter (VCT: transconductor/ transducer) circuits are fundamental building blocks of current-mode analog circuits and systems. VCTs can convert real-life voltage signals into current representations to be further processed by the current mode integrated circuit techniques. They are used in interface circuits, D/A and A/D converters, instrumentation amplifiers, and continuous-time filters. When the transconductance is electronically variable they can also be applied in operational transconductance amplifiers (OTA's), gain control circuits, and analog multipliers.

During the last two decades, various transconductor circuits based on the square law

[1, 7, 8] or linear [9, 10] or expotential characteristic [5] of MOS transistors biased in all the three operating regions (i.e., saturation, triode, and weak inversion) have appeared. Almost all of these proposed VCT configurations use gate-driven techniques; that is, all the input signals are fed to the gate terminals of MOS transistors. However, in 1996, in order to increase the linear range of MOS transconductors operating in weak inversion, Fried et. al. described a new technology by using the bulk as an active terminal [5]. It has been reported that the linear range can be increased by close to 100%. However, none of the literature deals with a bulk-driven VCT with the MOS transistors operating in the saturation region. This issue will be addressed in quite a lot of detail and constitutes the major part of the thesis. First, let us review some published VCTs to enhance our basic understanding of this important analogue circuit.

1.3.1 Gate-Driven VCT with MOSFETs Operating in Saturation Region[1]

The majority of proposed VCTs, and also the most successful ones, are based on the intrinsic square-law I-V characteristics of MOS transistors operating in the saturation region. Through linearizing a CMOS differential stage by various clever circuit techniques or simply differencing current the nonlinear term of the transistor I-V curve is eliminated.These circuits share the common principle as reported in [11, 12] (see Fig.1.1).

1. If not otherwise specified, a "VCT" refers to a gate-driven VCT. For VCTs using bulk-driven technologies, "bulk-driven" will be put before the "VCT" in order to distinct the simulation.

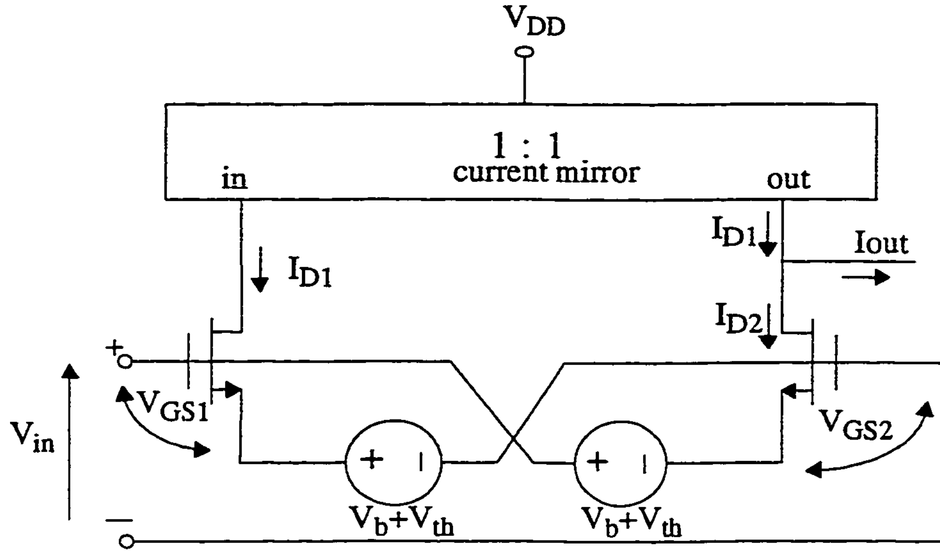

Fig. 1.1 Linear MOS Transconductor Circuit Principle [11, 12]. $I_{out} = I_{D1} - I_{D2}$

Assuming that *i)* the MOS Transistors are matched, *ii)* the transistors are operating in the saturation mode, *iii)* channel modulation effect is absent, we can use the square law dependence and arrive at

$$I_{D1} = \frac{1}{2}\beta\,(V_{GS1} - V_{th})^2 \tag{1.1}$$

$$I_{D2} = \frac{1}{2}\beta\,(V_{GS2} - V_{th})^2 \tag{1.2}$$

where β is the transconductance of the signal-input transistors. Using basic current law, and taking eqs. (1.1) and (1.2) into account. we further can arrive at

$$I_{out} = I_{D1} - I_{D2} = \beta\,(V_{GS1} + V_{GS2} - 2V_{th})\,\left(\frac{V_{GS1} - V_{GS2}}{2}\right) \tag{1.3}$$

The circuits referred to are arranged in various ways to make the last term in eq. (1.3) equal to the applied differential input voltage V_{in} and in addition to make the term

$V_{GS1} + V_{GS2} - 2V_{th}$ equal to a constant voltage; thereby, a linear voltage-to-current conversion is achieved:

$$I_{out} = g_m V_{in} \tag{1.4}$$

where

$$\begin{aligned} g_m &= 2\beta (V_{GS1} + V_{Gs2} - 2V_{th}) = const \qquad (a) \\ &\qquad and \\ V_{in} &= \frac{V_{GS1} - V_{GS2}}{2} \qquad (b) \end{aligned} \tag{1.5}$$

Following the suggestion of this principle, researchers proposed various new configurations. Seevinck et al. [11] extended the above-mentioned principle from single-channel MOS to CMOS. One more current mirror was adopted into their circuit (see. Fig.1.2).

The linearity characteristic governed by eq. (1.4) is still held in Seevincick's VCT, with a different transconductance representation if transistors are ideally matched. It has been shown that apart from the linear applications, such circuit may implement many analogue computational functions such as squaring, square rooting, vector summing and vector differencing, precision rectification, and rms-dc conversion. Note that such versatility is associated with one distinct feature of the circuit: the output current $I_{out} = I_1 - I_2$ is provided in two complementary ways thanks to the use of an extra current mirror. Note that only like-polarity transistors need be matched; no matching of p- to n-Channel transistors is required, a very desirable property.

Nevertheless, this circuit may experience the difficulty while used in a low power voltage supply circuit. The reason is quite obvious: the presence of stacked gate-source voltages requires a higher supply voltage. That is, since at least four series-connected transistor must all be biased in strong inversion region at all times, if large signal swing is expected (notice that the reduction in dynamic range due to the V_{GS} of a CMOS pair is

twice that due to an NMOS transistor) the voltage power applied may not be able to be reduced to below 3 volt with the absolute values of threshold voltages of MOSFETs around several hundred minivolts up to about 1 volt in a standard digital process. Furthermore, the extra circuitry introduced in Seevinck's VCT brings more freedom than the simple circuit suggested by the principle at a cost of more power dissipation. This problem can be serious because low voltage supply is preferred to avoid hot electron problems in MOS transistors [7].

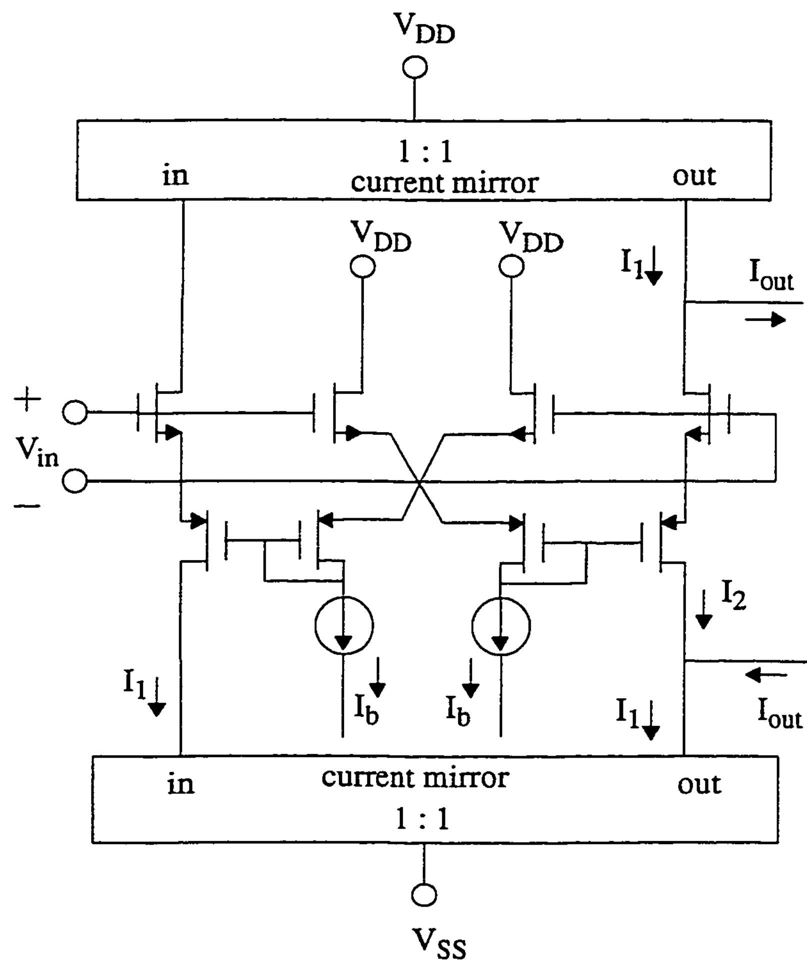

Fig. 1.2 Seevincick's CMOS transconductor circuit [11].

According to the analysis stated above, it turns out that we should stick to the basic principle as shown in Fig.1.1 and use less stacked configurations in terms of stringent low power supplies. Nedungadi et al. [12] have suggested use of a crosscoupled quad cell (CCQC) to linearize the voltage-current transfer function. Based on the cross-coupling ideas, Li et al. [7] further proposed a linearity improvement technique by adding two symmetrical current bootstrapping loops (see Fig.1.3). Simulation result verifies that such method can improve the linearity of the transconductor with small quiescent current and without sacrificing dynamic range. Thus it is claimed that the improved circuit is suitable for low voltage supply applications.

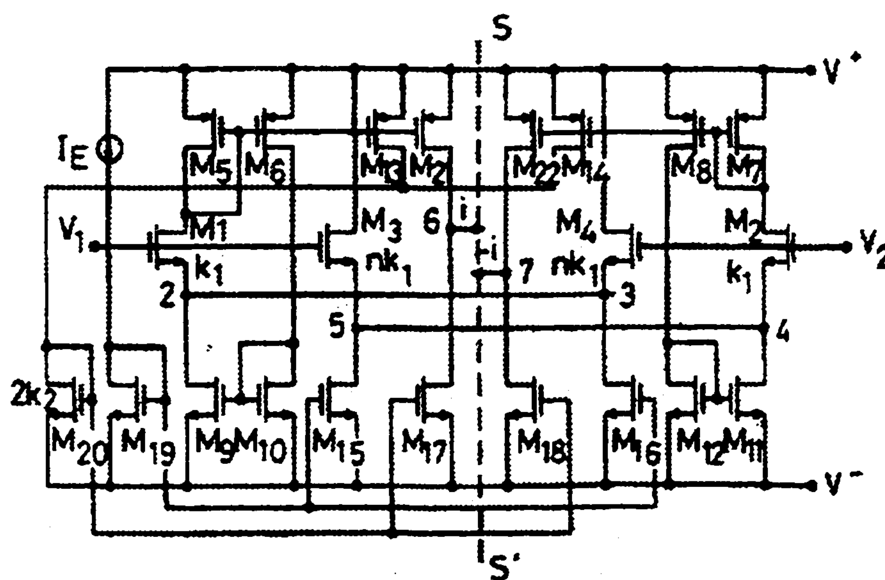

Fig. 1.3 Li's VCT [6].

Even though the promises made by the circuit bring some hope to low power designs, the circuit is too complicated and may lose its justification if applied in a real sig-

nal processing system. Once the bootstrapping loops are removed, a large value of n (transistor size ratio among transistors), maybe as large as 20, has to be chosen in order to keep the gate-to-source voltage drops of two input transistors almost identical. It is apparent that this also causes area overhead.

In 1992, Dr. Raut [8, 13] proposed a CMOS VCT, also based on the principle introduced above (see Fig.1.4) with an interesting variation. This new VCT uses two positive voltage supplies with different values. The output short circuit current, with the channel length effect ignored, is given by

$$\begin{aligned} i_{out} &= i_{01} + i_{02} \\ &= K'_P (V_{C1} - V_{C2})\,(V_1 - V_2) = g_{VCT}(V_1 - V_2) \end{aligned} \tag{1.6}$$

where K'_P is the transconductance parameter for the PMOS transistors. Eq. (1.6) manifests itself that the transconductance can be controlled by adjusting the difference of two positive voltage power supplies, assumed all the eight transistors will not change their operating modes when such adjustment happens. This programmability (easy and simple tunability as well) is one of the major advantages of this configuration.Unlike some other published VCTs, Raut's architecture has the capability of performing a real four-quadrant trans-multiplier since the difference of two positive voltage supplies (i.e., value of $V_1 - V_2$) can easily be made either positive or negative, as indicated by the eq. (1.6). Since i_{out} is only dependent on $V_1 - V_2$ (first order analysis), the response will be unaffected by common-mode signals. Furthermore, the output is not influenced by the V_{TH} of the transistors, at least to the extent of first-order analysis using the square law model equation as well. These improved features have determined its successful applications towards implementing inductors, positive conductances, and particularly negative conductances, which can be used in current mode analogue LSI/VLSI systems [8, 13].

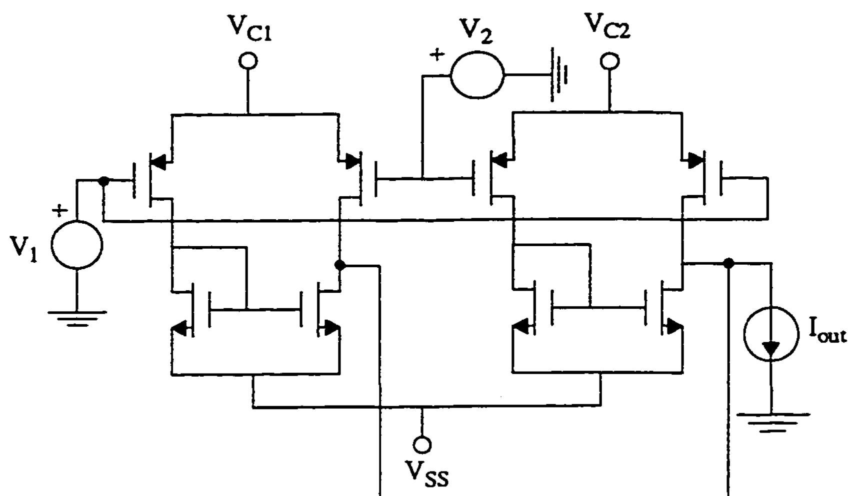

Fig. 1.4 Raut's VCT [8, 13].

As usual, nothing is perfect. Again, if we try to use such configuration to a low power voltage supplied circuit, we have to render that such two positive power supplies are not desirable in some cases, due to the voltage overhead introduced by the difference of two positive voltage supplies. However, if on-site programmability is required, this bright idea, double positive (or even theoretically double negative) voltage supplies, can be employed to many VCT configurations that have been proposed (note this approach can not be applied to Park's VCT described next, since the transconductance is independent of the voltage power supplies).

As shown by both experiments and simulation, a simple CMOS inverter has sound frequency response and relatively low distortion. However, a VCT using just a simple CMOS inverter suffers poor power supply rejection (PSR); what is more, the linear behavior depends critically on the obtainable matching between a PMOS and an NMOS transistor, i.e., the parameter $\mu_{eff}C_{ox}\frac{W}{L}$ has to be the same for the n-channel and p-channel

devices (W/L is the width-to-length ratio of the gate area and C_{ox} is the gate oxide capacitance per unit area). Such matching, although possible, will be very difficult to achieve in practice. To alleviate this difficulty, Park et al. [14] obtained a new VCT by replacing each transistor in the CMOS inverter by a p-channel-n-channel pair. The method used by Park et al. involves no current mirror at all (see Fig.1.5).

The operation of Park's VCT resembles in most respects of a CMOS inverter. Assuming matching between the geometrically identical n-MOS devices, M_1, M_3, and between the p-MOS devices M_2, M_4, using the standard square-law model for MOS devices operating in the saturation region, and taking $I_o = I_a - I_b$ into consideration, the output current is ready to be derived as

$$I_o = -2K_{eff}[V_{G1} + V_{G4} - \Sigma V_T]V_i + K_{eff}[V_{G1} + V_{G4} - \Sigma V_T]\Delta V_T \tag{1.7}$$

where the abbreviations are represented as[2]

$$K_{eff} = \frac{K_n K_p}{(\sqrt{K_n} + \sqrt{K_p})^2} \tag{1.8}$$

$$\Sigma V_T = V_{Tn1} + V_{Tn3} + |V_{Tp2}| + |V_{Tp4}| \tag{1.9}$$

$$\Delta V_T = (V_{Tn3} - V_{Tn1}) + (|V_{Tp4}| - |V_{Tp2}|) + (V_{G1} - V_{G4}) \tag{1.10}$$

If body effect can be neglected in this architecture and one makes $V_{G1} = V_{G4}$, the circuit will implement an ideal voltage-to-current transform function, $I_o = -g_{mT}V_i$, where

$$g_{mT} = 2K_{eff}(2V_G - \Sigma V_T) \tag{1.11}$$

2. The meanings of K_m and K_p are similar as mentioned before.

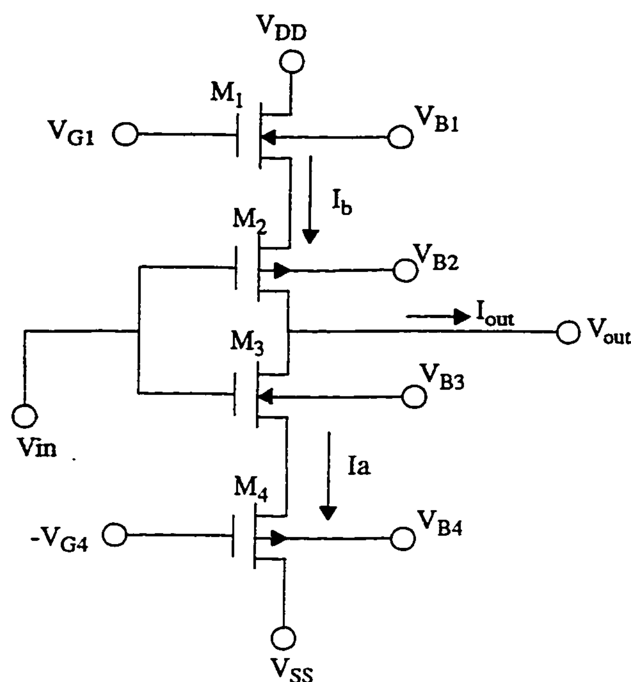

Fig. 1.5 Park's VCT [14].

This configuration is particularly suitable to a SOS (Silicon-on-Sapphire) process. However to a common single well process, body effect will definitely impact the performance. For instance, If a Park's VCT is designed in a P-well process, M_1 and M_3 will reside on their own wells; and therefore, ideally body effect related to these two transistors can be ignored. However, the bulk terminal of transistor M_2 must be connected to the most negative voltage, making the condition $V_{Tn3} = V_{Tn1}$ no longer valid or existent[3]. Similar impact will happen in an N-well process. Park et al. suggested that to keep eq. (1.7) still valid V_{G1} can be used for transconductance control and V_{G4} for ΔV_T nulling. In practice, this approach has the problem that the voltage value of V_{G1} may be larger than

3. The equations governing the behaviors of a bulk terminal in a MOS transistor will be given later.

V_{DD}. Fortunately, through sizing optimization, body effect can be drastically reduced. The price paid here is that more complex voltage reference networks have to be brought in.

Since no current mirror is involved in this configuration, the circuit avoids some high resistance node associated with a current mirror; and therefore, sound high frequency response is possible. Matching among p- and n-transistors is desired in order to achieve high linearity. As already alluded before, this transconductance of this architecture is independent of the supply voltages, leading to the improved PSRR.

Although this approach does provide advantages in terms of high linearity and wide working band, it does not work for low power circuit. The major contributing factors of the problem are that all the transistors are simply connected in series as a column (i.e., this is a quite stacked architecture) and some transistor has higher V_{th} due to inherently unavoidable body effect associated to this configuration.

1.3.2 VCT with MOSFETs Operating in Triode and Saturation Regions

Coban and Allen [10] proposed a low-voltage CMOS transconductance cell in 1994 (see Fig.1.6). The operating condition of their architecture is slightly different from those introduced above.

The operating principle of the transconductor is based on the fact that distortion terms of saturation and triode region implementations have opposite signs. It was recommended by Coban and Allen that for the same values of common mode input voltage V_C and mobility reduction coefficient θ, triode region transconductors have much higher linearity than those of saturation region transconductors. Actually, controversy exists regarding to these claims. Some researchers argue that such sign change does not happen in the low

voltage region, even though that is the case from the view point of SPICE simulation. However, as a linearizing technique, Coban and Allen's discovery deserves a closer look. We will not pursue this approach further for the time being.

Fig. 1.6 Coban's VCT.

Nabicht et. al [9] proposed a linear CMOS transconductor, where part of the transistors operating (M_2 and M_3) in the saturation mode, and some transistors (M_1's) in the triode mode (see Fig.1.7).

This circuit consists of two identical transconductors whose current sources are implemented through a diode-connected p-MOS transistor, M_3 and a p-MOS transistor M_4, where M_3-M_4 form a current mirror. Since some transistors are operating in the triode region, it is possible this circuit can use small voltage source. It is shown that this circuit

can be used in low voltage (with voltage supplies only in the range ±1 V) high frequency (up to several tens of MHz) and high linearity applications. To our knowledge, it is one of the best gate-driven VCT realizations so far reported in terms of low voltage operation. However, there is a tiny problem related to this circuit. It usually requires a level shift circuit to bring the input signal to the desired level. The level shift circuit is suggested as a construct with a capacitor and a transistor connected in series. This level shifting problem may relate to the fact that the signal is inputted to the gate terminal through a MOSFET operating in the triode region. If single output is desired, the current should be rearranged in the way like the one shown in the previous circuits.

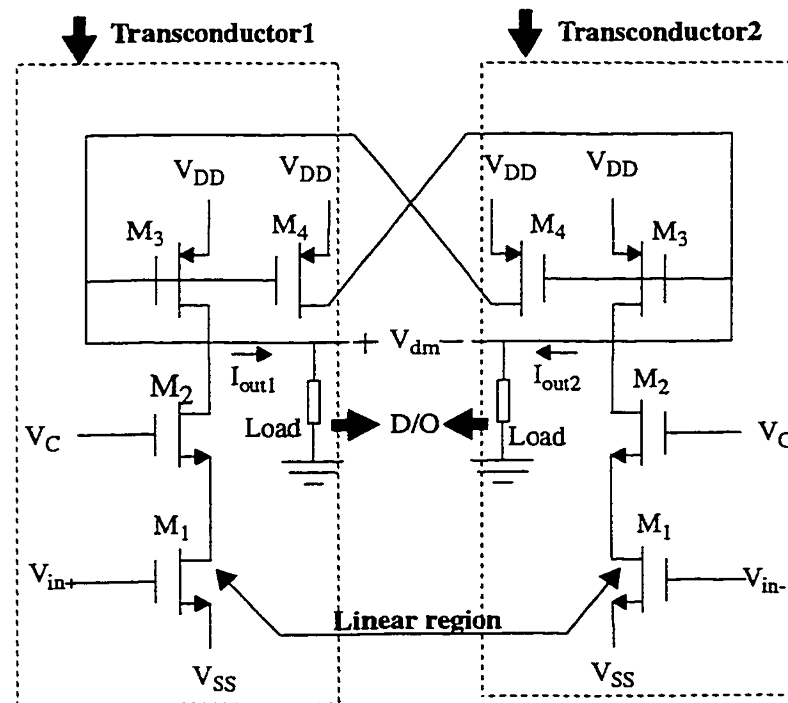

Fig. 1.7 Nabicht's fully differential transconductor circuit [9].

1.3.3 General Review

VCT is a very versatile building block. The first ever book thoroughly committed to current mode signal processing techniques [6], as its name indicates, contribute 5 chapters to the topic of transconductors (decades of different architectures proposed by various researchers are reviewed) and their even more impressive and complicated applications. It is appropriate to mention that the book was published in 1990. Since then, the research has proceeded to the stage that efficient power use and shrunk voltage became more concerned than ever before. Half of the VCT architectures were published in the most recent years, with more emphasis on the power consumption and voltage supplies while in the meantime pursuing high linearity, dynamic range, etc. It is also our orientation and initiative of this research to seek new architecture to achieve less power consumption and use reduced voltage supply. Therefore, we adopted different taxonomy from what was done in [6] to categorize various VCTs to suit our best concerns.

For the sake of convenience and simplicity, a table listing some features of above mentioned VCTs is given (see Table 1). A simple inspection to the table will unveil that how versatility of these architectures can be, even not mentioning their differences in terms of performance and characteristics.

Table 1 Various VCTs

VCT	Number of Transistors	Number of voltage supplies	Number of current reference	Number of voltage reference	Operating conditions	Configuration	V_T dependence for transconductance
Basic Circuit [11, 12]	≥ 4	2	0	0	saturation	DISO	Yes
Seevinck's VCT [11]	≥ 8	2	2	0	saturation	DISO	Yes
Li's[7]	≥ 20	2	1	0	saturation	DISO	Yes

Table 1 Various VCTs

VCT	Number of Transistors	Number of voltage supplies	Number of current reference	Number of voltage reference	Operating conditions	Configuration	V_T dependence for transconductance
Raut's[8]	8	3	0	0	saturation	DISO/ DIDO	No
Park's [14]	4	2	0	2	saturation	SISO	Yes
Coban's [10]	>16	2	0	1	saturation + linear	SISO	Yes
Nabicht's [9]	>5	2	1	1	saturation + linear	SISO/ DIDO	Yes

1.3.4 Practical Concerns Regarding Low Voltage and Low Power VCT Operation

Low power and small chip area are well-known desirable features for any integrated circuit. In this section, some practical concerns on developing a VCT with low power consumption are to be addressed.

Linear transconductor (g_m) circuits, like all other analogue and digital building blocks, are being influenced by reduced supply voltage requirements. Unfortunately such trend brings extreme difficulty in terms of linearity, harmonic distortion and dynamic range [15]. For low voltage operation, source coupled transconductors are more suitable.

MOSFETs operating in the saturation region can be used in low power low voltage circuits. However, extra care should be taken and new circuit configurations are sometimes essential. To facilitate the design, the circuit should be as simple as possible to minimize the power and area overhead while maintaining the specified requirements for linearity, frequency response, and so on.

Generally, a transistor column should consist of no more than 3 transistors. With special circuit configurations, such as bootstrapping, a circuit using 4 enhancement MOS tran-

sistors connected in series is possible with extreme difficulty. In a word, a differential pair with a less-stacked transistor structure is suitable for low-voltage operation.

To reduce the unintended body effect, the configuration should insure that as many as possible transistors should reside in their own wells (i.e., try to make the source and bulk terminals connected when it is possible).

It is more appropriate to just use two power supplies. And using the circuit with higher CMRR (Common Mode Rejection Ratio) and PSRR (Power Supply Rejection Ratio) will definitely be an advantage. High PSRR is achievable if the transconductance is just weakly dependant (the best will be no dependence). When programmability (or easy tunability in the field) is required, Raut's approach will be one of the simple and elegant solutions to many circuit configurations.

It is more desirable to use the configurations that only require the matching of polarity-like transistors. This is particularly true for a VLSI system, where matching principle is always one of the key issues.

Due to the shrinkage of voltage supplies, the noise becomes a real problem to the circuit designers that they can never afford to overlook. Therefore, noise situation should be treated in an even more serious manner. Disciplined design rules have to be followed in order to achieve a workable circuit.

1.4 A Novel Bulk-Driven VCT Architecture

Based on the knowledge we have acquired on published VCT architectures and bulk-driven techniques, both briefly mentioned in the previous sections, we are proposing a bulk-driven CMOS VCT with all transistors operating in the saturation regions. This

architecture has quite simple circuitry and can work with voltage supplies as low as 2 Volts. The biasing current (quiescent current) required to drive the circuit is very small; and hence, the power dissipation is in low, normally about several decades of microwatts. The power consumption efficiency of the proposed bulk-driven VCT is further evaluated by using the criteria of $g_m/Power$ and alike. Generally, this VCT cell, therefore, places itself as a candidate for low power applications. The proposed VCT has modest frequency response; thus it is a fine and appropriate architecture for a low frequency application, as most biomedical signal processing units, usually fully- or semi-implanted instruments, which demand low power dissipation and operating in the low frequency region.

Throughout the following chapters, we will deal with the proposed VCT in a great detail. Chapter 2 presents a widely used MOSFET model for analyzing both the large signal and ac small signal characteristics; a physical bulk-driven MOSFET model is also presented as well. Some problems related to modelling in analog circuit design and analysis are addressed. Chapter 3 deals with the bulk-driven VCT through a completed analyses and simulation at large. Apart from the DC and AC equations regarding to the circuit, noise analysis has been conducted. Some evaluation and optimization techniques that can be applied to the proposed circuit are discussed. As an application of this VCT, a large scale system (filter) using the VCT is introduced in chapter 4. Features and characteristics of various components associated with the filter are exhibited. Chapter 5 dedicates itself to the layout generation and post layout simulation; measurements on a fabricated chip are given. Chapter 6 concludes the work by highlighting the advantages and disadvantages of bulk-driven techniques and by suggesting future direction of work.

Chapter 2

Modeling Bulk-Driven MOSFETs

In this chapter, a MOSFET model will be shown. Modeling approach will be introduced. This approach will be applied to the proposed bulk-driven circuit to develop an appropriate bulk-driven MOSFET model. Operating mechanism of bulk-driven technology will be discussed in detail. Some advantages and disadvantages of the model being used will also be addressed.

2.1 Modeling Approach

The fundamental goal in device modeling is to obtain the functional relationship among the terminal electrical variables of the device to be modeled. These electrical characteristics depend on a set of parameters including both geometrical variables and variables related to the device physics [16]. Fortunately, for most physical electrical devices, at best only a good approximation to the actual relationship of the electrical variables can be obtained. Obviously, tradeoffs are often made between the quality of the approximation and its complexity. A very simple model is generally necessary to provide insight for

design and facilitate symbolic hand manipulations whereas a more accurate and correspondingly more sophisticated model is generally preferred for computer simulations of circuits employing these devices. The general modeling approach adopted in this thesis is illustrated in Fig.2.1.

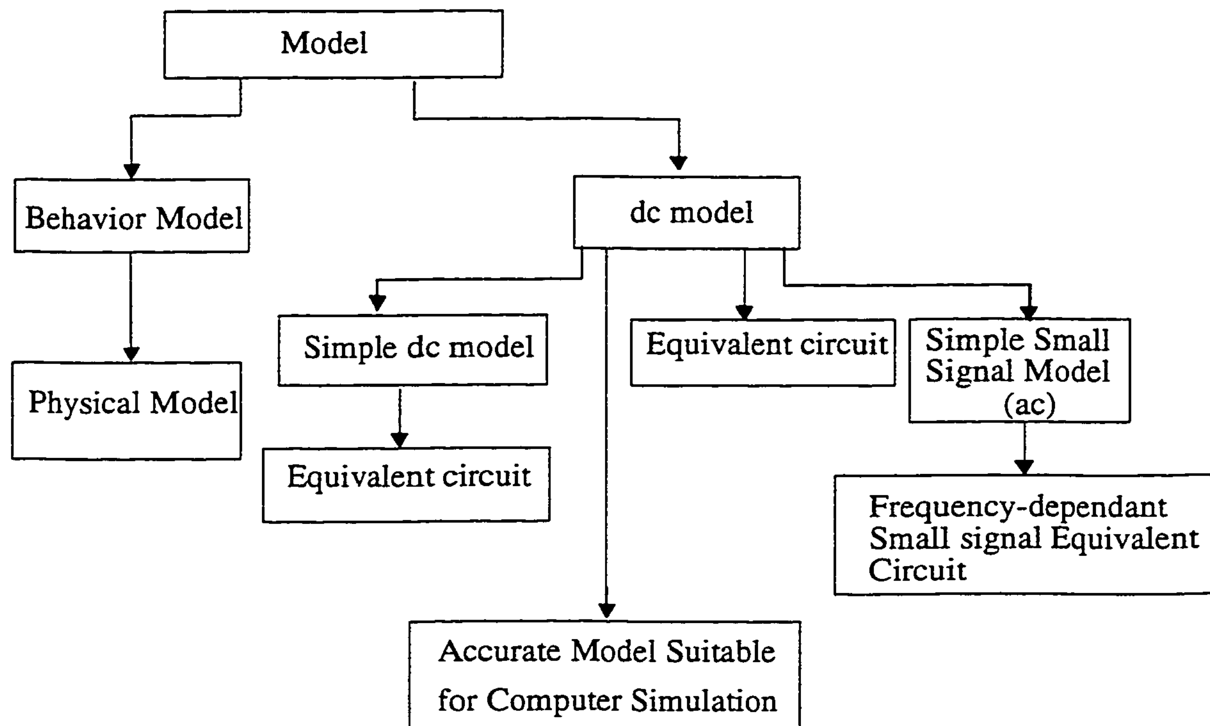

Fig. 2.1 Approach to device modeling.

According to the modeling approach suggested in [16], we shall start the modeling for DC signal. From this DC model, a linear small signal model and equivalent simplified ac and dc circuits will be derived. The method will then be expanded upon to provide better agreement between the theoretical and experimental results for use in computer simulation. This general modeling approach will be applied to the proposed bulk-driven VCT as

well.Before we go to the mathematical watershed, in the next subsections, we will first discuss a behavior model of a Bulk-driven MOSFET, which empowers us to better understand the operational principle of such a bulk-driven MOSFET, and perceive its advantages over the conventional gate-driven MOSFET systems.

2.2 Bulk-Driven MOSFETs - Operation and Advantages

Since the bulk terminal of a MOSFET will be used as an input terminal in the bulk-driven techniques, this bulk terminal will no longer be able to connect to the most positive, or most negative, or its corresponding source terminal; consequently, the bulk-driven technique can only be applied to the MOSFETs that have their own separate wells. Such arrangement will, theoretically to say, free the bulk terminal from the impacts of other terminals or voltage sources, and is ready to receive voltage stimuli. That is, a p-type MOSFET in an n-well process may be a candidate to the so called bulk-driven techniques. Same philosophy applies to an n-type MOSFET in a p-well process. Of course, if a twin-well process is available, theoretically, both n- and p-type transistors will have the same access to bulk-driven techniques.

Through the following, we will look at a bulk-driven p-MOS transistor in an n-well process. Note that a bulk-driven n-MOS transistor in a p-well process is every similar to what we see here except polarity changes in power supplies. A cross-section view of such a p-MOS is shown as Fig.2.2. In the graph, one parasitic lateral (QP) and one vertical (QV) bipolar junction transistors are also presented.

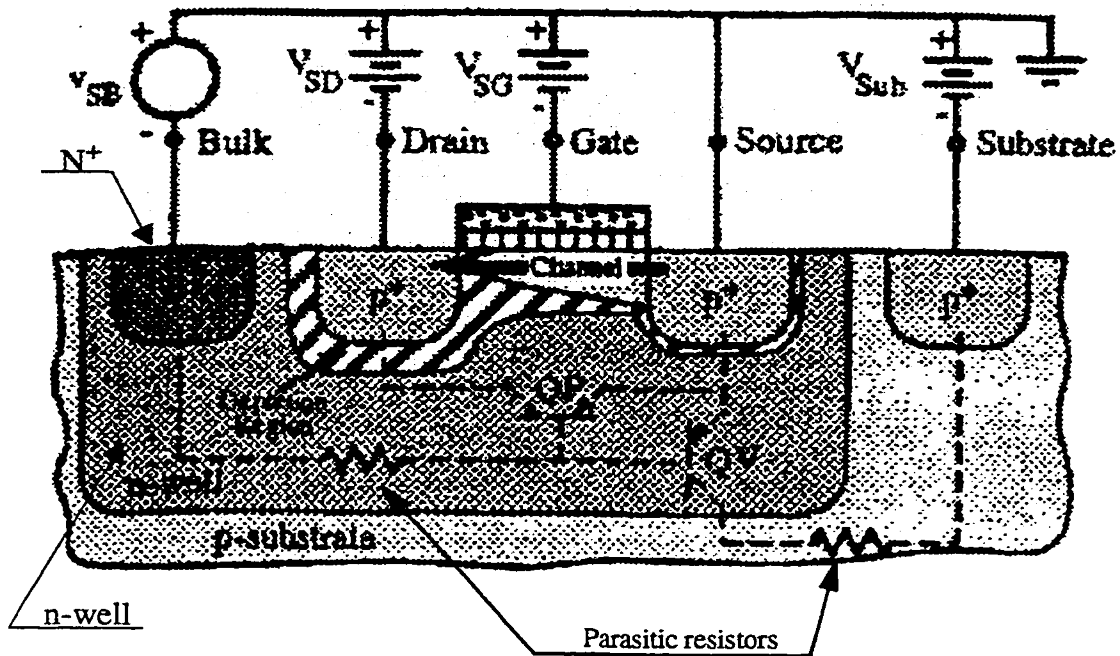

Fig. 2.2 Cross-section of a PMOS transistor and terminal voltages for bulk-source operation.

The operation of the bulk-driven MOSFET is much like a JFET (Junction FET) [4]. If sufficiently high voltage is applied to the gate terminal of a MOSFET, an inversion layer forming the conduction channel beneath the gate will be established. Usually, in a bulk-driven case, a fixed reference voltage is connected to the gate terminal of the MOSFET. Such voltage reference insures that the conductance channel is well formed at all times[4]. The thickness of the depletion layer beneath the source, inversion layer, and drain of the MOSFET is determined by the bulk potential. By varying the voltage between the source and bulk terminals, this depletion layer thickness changes accordingly; as a consequence,

4. We restrict our attention to the MOSFET operating in the saturation region and triode region as well. MOSFET operating in weak inversion region will not be pursued.

the inversion layer through which the drain current flows can be modulated. The major advantage of a bulk-driven circuit can be attributed to the fact that with very small dc values of the bulk-source potential, the channel current can be modulated.

Even though the threshold voltage (see Fig.2.3) will increase as a result of the potential difference between the source and substrate terminals[5] introduced by the bulk-driven techniques, with low DC current required, the power consumption is quite small as a result. Also with higher V_{TH}, the V_{DS} can be smaller because of the saturation condition needed to be satisfied, $V_{DS} \geq V_{GS} - V_{TH}$. This leads to operation with lower supply voltage. Obviously, such claim is not very true if the gate-driven technology were used, since the minimum allowed V_{GS} has to be increased to satisfy another operating condition $V_{GS} - V_{TH} > 0$. However, for a bulk-driven circuit, the gate terminals of corresponding MOSFETs are always connected to a voltage reference(s) (practically, this value of the voltage reference can be as high/low as the most positive/negative sources.); therefore, the $V_{GS} - V_{TH} > 0$ condition is almost insured at all the time.

Above discussion is based on the observation of a single MOSFET. However, if we connect several transistors to form a signal processing unit, it turns out that the minimum voltage supply should be greater than the sum of the threshold voltages (absolute values) of the p- and n- devices that may constitute the column of the unit. For the sake of simplicity, we assume that we only have one PMOS and one NMOS transistors at one column. Therefore, the voltage supply in this simple case will be

$$V > V_{Tn} + |V_{Tp}| \tag{2.1}$$

5. If the substrate and source terminals are lightly forward biased, the threshold voltage will actually be reduced. Here, we are talking about these terminals are reverse biased. Forward biasing definitely will make the reduction of the voltage supplies reduced.

To illustrate what eq. (2.1) really means to us, we will give an example here. Assuming that the threshold voltages for NMOS and PMOS are 0.8 volt and -0.8 volt respectively, we can draw some interesting comparison between a gate-driven and a bulk-driven circuit, regarding to low voltage low power operation.

For a bulk-driven, with 1 volt DC swing (from -0.5 volt to 0.5 volt), the voltage supply needed is less than 1.8 volts[6] (see Fig.2.3). If the bulk-source p-n junction can be forward-biased, the voltage supply can be even reduced to 1.3 ~1.4 volts[7]!

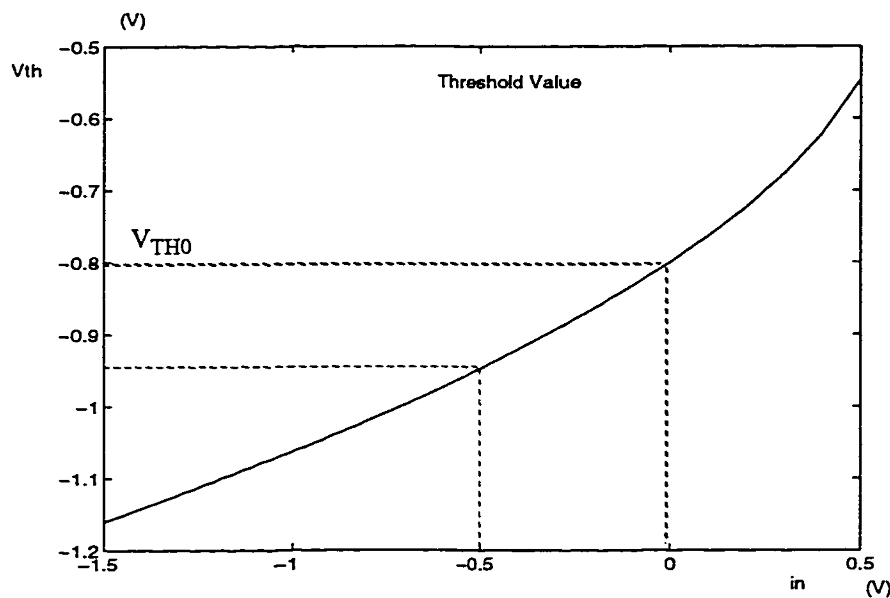

Fig. 2.3 Threshold change in accordance with the change of V_{SB} (p-type device used).

For a gate-driven circuit, on the other hand, there is no way to reduce the voltage supply to the level of 1.6 volts even though no signal is applied. To handle the same DC swing applied to a gate-driven VCT, the voltage supply required is 2.1 volts[8]. Above

6. The threshold voltage of one transistor remains 0.8volt, and the other one may jump to 0.9 ~1.0volt. Altogether, the voltage supply will be 1.7 ~ 1.8 volts.

7. In this case, the threshold voltage drops to around 0.5 ~ 0.6 volt in absolute value.

example clearly clarifies that bulk-driven can be used in the low voltage supply situations. Its advantage while being used in a forward-biased situation is even more drastic, although we are a little hesitant to pursue this goal in this thesis. However, the door is still open, and it might need some research to substantially explore this plausibility. It may be noted that a current mirror has been built so far using the forward-biased bulk-driven technique[4].

If we further look at any CMOS gate-driven architecture that has three or more transistors connected in series in one column[9], and if we assume the use of single well technology, we can conclude that the body effect is likely unavoidable for at least one transistor. In simple words, at least one transistor has larger threshold voltage due to the body effect. Since this unavoidable effect exists, we may use the bulk terminal of that "problematic" transistor as the one receiving the signal input. The gate terminals, therefore, can only commit themselves to one single task, insuring all the transistors operating at the right mode. In traditional gate-driven techniques, gate input signals have to carry on two duties: feeding the input signal and maintaining the proper biasing of the whole circuit simultaneously. However, once the voltage of the power supply drops, it is difficult to achieve both goals, keeping the operating mode when a signal with large swing is applied. Feeding in large signal to a gate-driven circuit put the requirements on higher DC voltage biasing and higher power supplies, leading to large DC current flows in the circuit. The bulk-driven techniques can reduce the input signal's biasing voltage; and thus, the power consumption is reduced accordingly.

If in the future, some circuit architectures can fully take advantage of the observations mentioned above, it is possible to lower down the voltage supplies to an even lower stage. Bulk-driven techniques have offered such possibilities.

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8. This value is calculated by adding 0.5volt to equ. (2.1), i.e., 0.8+0.8+0.5=2.1Volts.

9. Strictly speaking, both n- and p-type devices should appear in that column.

2.3 Mathematical Model of MOSFET for Hand Calculation

A summary of the MOSFET model for both n-channel and p-channel devices are presented below (in Table 2). This model is based on the long-channel characteristics of MOSFETs. That is the channel length is much larger than the sum of the source and drain depletion layer widths [17]. This model is simple and physically meaningful; therefore, it is good and adequate for hand calculations.

Table 2 MOSFET Model for Hand Calculation.[a]

Transistor Type	Operation Region	Conditions	Equations
N-MOS	Cutoff	$V_{GS} < V_T$ and $V_{DS} \geq 0$	$I_D = 0$
	Linear[b]	$V_{GS} > V_T$ and $V_{DS} \leq V_{GS} - V_T$	$I_D = \frac{K'W}{L}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS}$
	Saturation	$V_{GS} > V_T$ and $V_{DS} > V_{GS} - V_T$	$I_D = \frac{K'W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$
P-MOS	Cutoff	$V_{GS} > V_T$ and $V_{DS} \leq 0$	$I_D = 0$
	Linear	$V_{GS} < V_T$ and $V_{DS} \geq V_{GS} - V_T$	$I_D = \frac{K'W}{L}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS}$
	Saturation	$V_{GS} < V_T$ and $V_{DS} < V_{GS} - V_T$	$I_D = \frac{K'W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$

a. Design parameters:
- **W = channel width**
- **L = channel length**

Process parameters:
- K' **= transconductance parameter**
- V_{T0} **= threshold voltage for** $V_{BS} = 0$
- γ **= bulk threshold parameter**
- ϕ **= strong inversion surface**
- λ **= channel length modulation parameter**

K', γ, ϕ, *and* λ **are positive for both n-channel and p-channel transistors. N-channel transistors are termed enhancement if** $V_{T0} > 0$ **and depletion if** $V_{T0} < 0$**. P-channel transistors are termed enhancement if** $V_{T0} < 0$ **and depletion if** $V_{T0} > 0$

b. Also known as triode or ohmic region.

In many cases, for the sake of simplicity, the channel length effect is ignored (i.e., $\lambda = 0$ is assumed); and therefore, the impact of V_{DS} will disappear from the equations modeling saturated transistors. As a matter of fact, to the first approximation $1/\lambda$ is prop-

ositional to L (that is why $1/\lambda$ is considered to be the "Early voltage V_A" in MOSFETs) and such effect of the channel-length modulation can be reduced by applying the large channel length of some μm orders [20].This approximation is good for hand calculation and simulation of verifying the principle of the prototype circuit.

2.4 AC Model for MOSFET

AC small signal model is conventionally derived from the DC model by assuming small variations around a given (DC) operating point. For AC analysis, the region of operation is assumed to be the saturation region.

A MOS transistor has four terminals; consequently, a large number of AC parameters could be defined by considering a pair of terminal at a time. The most prominent DC component in the MOSFET is the drain to source current controlled by v_{gs}, v_{ds} and v_{bs}. As we can see from the proposed bulk-driven VCT, the drain to source current is modulated by v_{bs}. In the model introduced here, three conductances are used. They are[10]

$$g_m = \left.\frac{\partial i_D}{\partial V_{gs}}\right|_{operating\ point} = \sqrt{\frac{2K'W}{L}|I_{DQ}|} \tag{2.2}$$

$$g_{mbs} = \left.\frac{\partial i_D}{\partial V_{bs}}\right|_{operating\ point} = \frac{\gamma}{2\sqrt{\phi - V_{BSQ}}} g_m \tag{2.3}$$

$$g_{ds} = \left.\frac{\partial i_D}{\partial V_{ds}}\right|_{operating\ point} \approx \lambda|I_{DQ}| \tag{2.4}$$

In the above, g_m is the transconductance, g_{mb} is the bulk transconductance and

10. Operating point are represented by V_{dsQ}, V_{bsQ} and V_{gsQ}.

g_{ds}. is the output conductance of the MOSFET. For a simplified model, these three parameters are good enough to describe the behavior of a MOSFET; however, for a more accurate model description (see Fig.2.4), parasitic components should be taken into considerations. To accomplish both the simplicity and completeness simultaneously, the parasitic resistors (i.e., R_d and R_S from the Fig.2.4) will be ignored. Besides, some other parasitic components, like the parasitic diodes associated with the field effect devices are of no concern in Fig.2.4, either. Such omission will reduce the complexity of the model to a manageable level with sufficiently enough accuracy maintained.

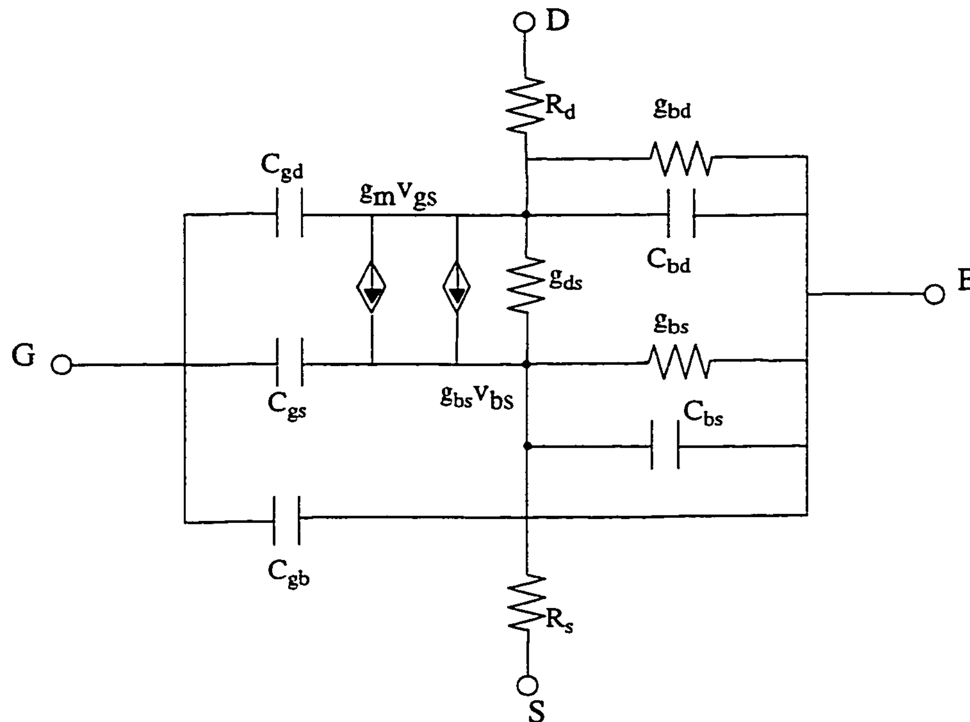


Fig. 2.4 AC model for the MOSFET.

The AC model will be used in the next chapter while deriving the ac equivalent circuit of the proposed bulk-driven VCT.

2.5 Second Order Effects

In the previous sections, simple MOSFET models were suggested. The basic device characteristics were derived under the following assumptions [17]:

(1) only drift current is considered;

(2) carrier mobility in inversion layer is constant;

(3) doping in the channel is uniform;

(4) reverse leakage current is negligible;

(5) drain-to-source voltage is small compared to surface potential for strong inversion;

(6) the transverse field in the channel is much larger than the longitudinal field.

The last condition corresponds to the gradual channel approximation. However, the short channel effects, arising as a result of a two dimensional potential distribution and high electric fields in the channel region, make one or more of the above mentioned assumptions invalid. This two dimensional potential results in degradation of the subthreshold behavior, dependence of the threshold voltage on device dimensions and biasing voltages, and failure of current saturation due to punchthrough [17]. The concerns have been incorporated into various MOSFET models in the SPICE by modifying different terms of the basic device model, using theoretical, empirical or semi empirical equations.

Because short channel effects complicate device operation and degrade device performance, these effects, such as the threshold voltage shift, mobility reduction, velocity saturation, channel length modulation, oxide charging [17] and many more, should be eliminated or minimized so that a physical short channel device can preserve the behavior of the electrically long channel device.

2.6 Modeling for Analog Applications

The MOSFET is no longer a device mainly used for digital applications. many MOS chips are now designed combining digital and analog functions. Most of the available models are suitable for digital designs. Hence, analog circuits are often designed very conservatively and the full potential of the technology is not realized [17].

The small signal drain conductance (g_{ds}) in saturation is one of the most poorly modeled parameters. That may cause problems in our bulk-driven VCT by introducing some DC offset at the output terminal. Another problem in modelling for analog applications is the failure of the quasi-static approximation. For digital circuits, the devices usually operate in one of the regions and the model equations do produce the device characteristics with acceptable accuracy. However, in analog applications, neither the strong inversion nor the weak inversion approximation is valid. Furthermore, the small signal conductances and capacitances are obtained by differentiating the large signal drain current and terminal charge equations designed to perform efficient dc and transient simulations. The advantage here is the distortion behavior, which is related to the large signal device characteristics, of the circuit can be determined in this way. The disadvantage, again, comes from its inaccuracy.

We have addressed the modeling for analog circuits in this chapter because modeling is an essential issue for analog circuit design and analysis. We are going to stick to the models given in the previous sections, even though some problems might occur as mentioned. The reason is obvious: simple but accurate enough model for each particular design case is preferred for guiding a designer to accomplish the design task.

The lesson that can be learned is that the design should always be conservative to make room for unpredictable variances and modeling inaccuracy. In the following chapter, we will show how a Monte Carlo analysis can be performed to evaluate the yield and vari-

ances associated with the process. However, fabrication prototypes is necessary since no model presently available can really describe a real silicon in a convincing fashion.

Chapter 3

A Novel CMOS Bulk-Driven VCT

In this chapter, a novel bulk-driven voltage-to-current transconductor (VCT) is introduced first, followed by the DC and AC analyses of the proposed configuration. HSPICE simulation results exhibit the features that this bulk-driven VCT configuration carries. Noise characteristics are discussed in a great detail. Some optimization techniques are suggested.

3.1 A Novel Bulk-Driven VCT

Inherently, a MOSFET consists of four terminals. Body effect in most cases are not desired; quite a number of methods have been proposed to evaluate and eliminate this disgusting effect[11]. However, body effect is not always a negative factor. Occasionally, it may happen to do something good. As already mentioned before, bulk-driven technique has its own potential privileges in low power and low voltage circuit family. We have proposed a

11. Note that some circuit designers used bulk terminals in their architectures to improve some electrical characteristics. This situation is beyond our consideration and will be excluded from our considerations.

novel bulk-driven VCT with the transistors operating in the saturation region. We will examine this proposal in the following chapters. Applications using this new VCT will be given. Some advantages and disadvantages will be discussed.

The basic circuit of the bulk-driven voltage-to-current transconductor is shown as Fig.3.1. This circuit has 6 transistors for a DISO (Differential In and Single Out) configuration. Two voltage references are needed in this scheme.

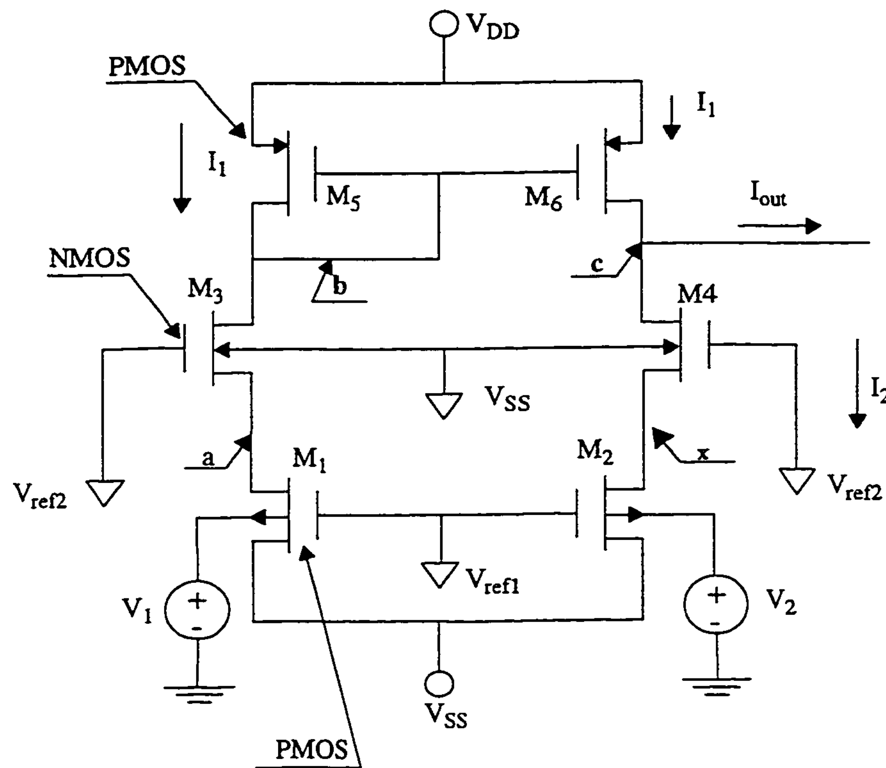


Fig. 3.1 **Bulk-Driven VCT (N-well).**

The use of an n-well process is assumed in the proposed circuit. If the current mirror

is assumed to be ideal, basically, then the operation of this circuit is totally controlled by the transistor pairs M_1/M_3 and M_2/M_4 and the two reference voltages. The reason that we incorporate cascoded transistors M_3 and M_4 is that separation of the current output node (node *c* in Fig.3.1) from node *x* is strongly desired. Such separation will simplify the DC common mode biasing for the two signal input terminals. For example, we may need to ground the current output I_{out}. Thanks to the voltage drop between the drain and source terminals, V_x (the voltage at node *x*) can be set to a negative voltage. As a result, the input V_2 can be grounded and at the same time, still keeping the source and substrate terminals reverse biased. Briefly, it is always desirable to make the DC potential of the bulk terminals higher than those of both source and drain terminals respectively so that all the diodes of the transistor will remain reverse-biased. Further, take a notice that cascode architecture always provides higher output impedance (i.e., lower output conductance) [18]. This is achieved without any noise penalty, and with only a very small reduction of phase margin.

If a p-well process is used (like the 1.5 micron ISO-HCMOS process of Mitel Semiconductor Components Division, Canada), the bulk-driven VCT will have to be modified accordingly in concert with the p-well transistors (see Fig.3.2). Although the small-signal model is exactly same for an n-device and its p- counterpart, due to the fact that the holes have lower mobility than electrons, an n-type device usually has higher transconductance than a p-type device with same size. Since the transconductance is strongly related to the size of transistors M_3 and M_4, and to realize relatively higher transconductance with a smaller size, an n-well process will be preferred. Except this concern, these two configurations (see Fig.3.1 and Fig.3.2) are considered to be analogous.

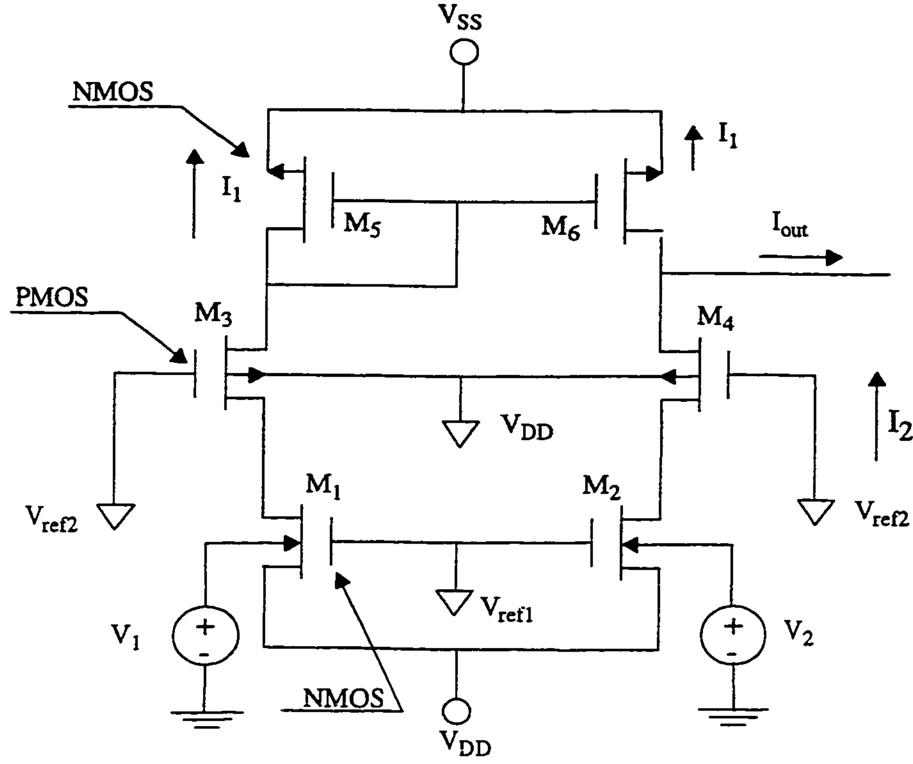


Fig. 3.2 Bulk-Driven VCT (P-well).

3.2 Basic Operations

A bulk-driven VCT with the differential-in, single-out (DISO) configuration has been shown in Fig.3.1. Assuming that all the transistors operate in the saturation region, and channel length effect is ignored, we will have

$$I_1 = \frac{\beta_1}{2}(V_{ref1} - V_a - V_{Tp})^2 = \frac{\beta_3}{2}(V_{ref2} - V_a - V_{Tn})^2 \tag{3.1}$$

$$I_2 = \frac{\beta_1}{2}(V_{ref1} - V_x - V_{Tp})^2 = \frac{\beta_3}{2}(V_{ref2} - V_x - V_{Tn})^2 \tag{3.2}$$

where β_1 and β_3 are the transconductances of transistor pairs of M_1/M_2 and M_3/M_4 respectively.

$$V_{Tp} = V_{Tp0} - \gamma_p(\sqrt{\phi_p - V_a + V_1} - \sqrt{\phi_p}) \tag{3.3}$$

Since an n-well process is assumed, the bulk terminal of transistors M_3 and M_4 (NMOS transistors on a P-substrate) are connected to the most negative voltage source V_{SS}. Thereby, the threshold voltage of V_{Tn} is given as follows (derived from eq. (2.4))

$$V_{Tn} = V_{Tn0} + \gamma_n(\sqrt{\phi_n + V_a - V_{ss}} - \sqrt{\phi_n}) \tag{3.4}$$

From the eqs. (3.1) through (3.4), we can see that the difficulty to deduce the large signal operation equation lies in how to determine an explicit expression of V_a (the voltage at node a, same problem applies to derive the expression regarding to the voltage at node x, V_x). To facilitate the analysis, we can approximate V_a by a polynomial; that is

$$V_a = V_{A0} + a_1 V_1 + a_2 V_1^2 + a_3 V_1^3 + \dots \tag{3.5}$$

where V_{A0} is the voltage at node a when V_1 is zero.

Extensive simulations using different sizes and biasing conditions led to the conclusion that V_a is very closely proportional to the first degree on V_1; thus we may use the linear approach to evaluate V_a. Thus,

$$V_a \approx V_{A0} + a_1 V_1 \tag{3.6}$$

Generally, a relationship $V_\alpha \approx V_{\alpha 0} + a_1 V_i$ holds for the voltage at nodes a and x (see Fig. 1, i = 1, 2). Applying the series expansion approximation $\sqrt{x + x_0} = x_0 + \frac{1}{2}\frac{x}{x_0}$, we will arrive at

$$\gamma_n\sqrt{\phi_n + V_{A0} + (1+a_1)V_1 - V_{ss}} \approx \gamma_n\left[(\phi_n - V_{A0} - V_{ss}) + \frac{(1-a_1)V_1}{2(\phi_p - V_{A0} - V_{ss})}\right] \tag{3.7}$$

To minimize the error of eq. (3.7) to a negligible level, we have try to make the value of $\phi_p - V_{A0}$ far greater than V_1. If extreme high linearity is not required, such condition could be relaxed.

If same assumptions and manipulations are applied to transistors M_2 and M_4, and assuming the perfectness of the current mirror consisting of transistors M_5 and M_6, after fancy mathematical manipulation, finally we arrive at the following

$$\begin{aligned} I_{out} &= I_1 - I_2 \\ &= \beta_1(V_C + \gamma_p\phi_p - \gamma_p V_{A0})(k_2 - \gamma_p k_2 - \gamma_p)(V_2 - V_1) \end{aligned} \tag{3.8}$$

where β_1 is the transconductance for transistors M_1 and M_2, and

$$V_C = V_{SS} - V_{A0} - V_{Tp0} - \gamma_p\sqrt{\phi_p} \qquad and \tag{3.9}$$

$$V_{A0} = \frac{\sqrt{\frac{\beta_3}{\beta_1}}\left(V_{ref2} - V_{Tn0} - \gamma_n\sqrt{\phi_n + k_1\phi_n - V_{ref1}} + k\gamma_n\sqrt{\phi_n}\right)}{1+\sqrt{\frac{\beta_3}{\beta_1}}} + \frac{V_{ref1} - V_{Tp0} + \gamma_p\sqrt{\phi_p - k_1\phi_p} - \gamma_p\sqrt{\phi_p}}{1+\sqrt{\frac{\beta_3}{\beta_1}}} \tag{3.10}$$

Note that when deducing eq. (3.10), we made an approximation again; that is $|V_{A0}| \approx k_1\phi_p \approx k_1\phi_n$. In most available technologies, ϕ_n and ϕ_p can be made quite close; therefore, such $\phi_n = \phi_p$ prevails in our manipulation. k_1 is a constant and usually it has

the range, $0.5 < k_1 < 1$. In an actual design, $k_1 = \frac{2}{3}$ will be quite acceptable in terms of accuracy and simplicity. More accurate value of k_1 can be obtained by extensive SPICE simulation. Note that a_1 has disappeared from the final equation and actually its impact is somehow reflected in k_1.

If p-well process is assumed (see Fig.3.2), the dc characteristics can be represented by the following design equations, using the same philosophy employed while deducing the equations for an n-well process:

$$\begin{aligned} I_{out} &= I_1 - I_2 \\ &= \beta_1 (V_C + \gamma_n \phi_n - \gamma_n V_{A0}) (k_2 - \gamma_n k_2 - \gamma_n) (V_2 - V_1) \end{aligned} \tag{3.11}$$

where β_1 is the transconductance for transistors M_1 and M_2, and

$$V_C = V_{DD} - V_{A0} + V_{Tn0} + \gamma_n \sqrt{\phi_n} \qquad and \tag{3.12}$$

$$\begin{aligned} V_{A0} = {} & \frac{\sqrt{\frac{\beta_3}{\beta_1}} \left(V_{ref2} - V_{Tp0} + \gamma_p \sqrt{\left| \phi_p + k_1 \phi_p - V_{ref1} \right|} + k \gamma_p \sqrt{\phi_p} \right)}{1 + \sqrt{\frac{\beta_3}{\beta_1}}} + \\ & + \frac{V_{ref1} - V_{Tn0} - \sqrt{\left| \phi_n - k_1 \phi_n \right|} + \gamma_n \sqrt{\phi_n}}{1 + \sqrt{\frac{\beta_3}{\beta_1}}} \end{aligned} \tag{3.13}$$

3.3 Channel Length Modulation Effect

The finite output conductance of MOS transistors operating in the saturation region is due to the spreading of the depletion region near the drain which results in a reduction of the channel length. Calculation presented above did not consider the channel length modu-

lation effect (usually accounted for by the parameter λ). In the following we will take this effect into our considerations and we assume that all the n- and p- transistors have the same channel length modulation factor respectively (see Fig.3.1).

$$\begin{bmatrix} I_1 = \frac{\beta_1}{2}(V_{ref1} - V_a - V_{Tp})^2[1 + \lambda_p(V_a - V_{ref1})] & (a) \\ I_1 = \frac{\beta_3}{2}(V_{ref2} - V_a - V_{Tn})^2[1 + \lambda_n(V_b - V_a)] & (b) \\ I_1 = \frac{\beta_5}{2}(V_b - V_{DD} - V_{Tp0})^2[1 + \lambda_p(V_{DD} - V_b)] & (c) \end{bmatrix} \tag{3.14}$$

If we size the transistors in such a way that $V_b \approx V_c$ (see Fig.3.1). the impact of λ_p on the current mirror is negligible. And also note that $V_{A0} \approx V_{X0}$. Therefore,

$$\begin{bmatrix} I_2 = \frac{\beta_1}{2}(V_{ref1} - V_x - V_{Tp})^2[1 + \lambda_p(V_x - V_{ref1})] \\ I_2 = \frac{\beta_3}{2}(V_{ref2} - V_x - V_{Tn})^2[1 + \lambda_n(V_x - V_a)] \\ I_2 = \frac{\beta_5}{2}(V_c - V_{DD} - V_{Tp0})^2[1 + \lambda_p(V_{DD} - V_b)] \end{bmatrix} \tag{3.15}$$

$$I'_{out} = I_1 - I_2 = (1 + \lambda_p V_{ref1} + \frac{\beta_1}{2}\lambda_p V_{A0}) I_{out} + I_{offset} \tag{3.16}$$

where I_{out} is same as given as eq. (3.8), and

$$I_{offset} = \frac{\beta_1}{2}\lambda_{p1}k[V_1(V_{ref1} - V_a - V_{Tp1})^2)] - V_2(V_{ref1} - V_x - V_{Tp2})^2 \tag{3.17}$$

where k is regarded as a constant, based on the assumption that we made before that $V_\alpha \approx V_{\alpha 0} + a_1 V_i$ (i = 1, 2) holds for nodes a and x (see Fig.3.1). Eq. (3.17) shows that the major contributor of the offset is the λ_p of transistors M_1 and M_2, where the signals are fed in. It also can be seen that the offset is somehow dependent on the input signal level. Small

voltage level shift to the input signals will diminish the impact of the dc offset. However, this may never be completely removed.

3.4 Output-Voltage Limitation

Our previous discussions on the output current excluded implicitly the impacts of the output voltage. That is, we did not mention where the current I_{out} goes and how far we can trust this current I_{out} to be independent of V_{out}. Obviously, unlimited variation of V_{out} definitely will result in the departure of I_{out} from its expectations. In [20], it has been shown that two limits (identified as upper and lower limits) exist regarding to a transconductance amplifier scheme. A illustrative curve of showing the dependence of output current of the simple transconductance amplifier on output voltage is given in Fig.3.3. Basically, the curve shows that there is an upper limit, where the output current increases rapidly (region I in the curve). There is also a lower limit, below which the output current decreases rapidly (region III in the curve). In between (region II in the curve), the output current is closely independent of the output voltage, although due to the finite output conductance, a slight slope does exist, meaning some dependance of output current on the output voltage. This slope can be greatly reduced by applying the cascode technique [16], which is the case in the proposed bulk-driven VCT circuit. Note that these limits are the circuit limits always existing.

We are not supposed to expect that the output voltage can exceed the most positive voltage source or has lower voltage value than the most negative voltage source. These are the soft limitations of the output voltage. Table 3 gives these limits in the form of soft and hard limits. It can be seen that some limits really depend on the input voltage.

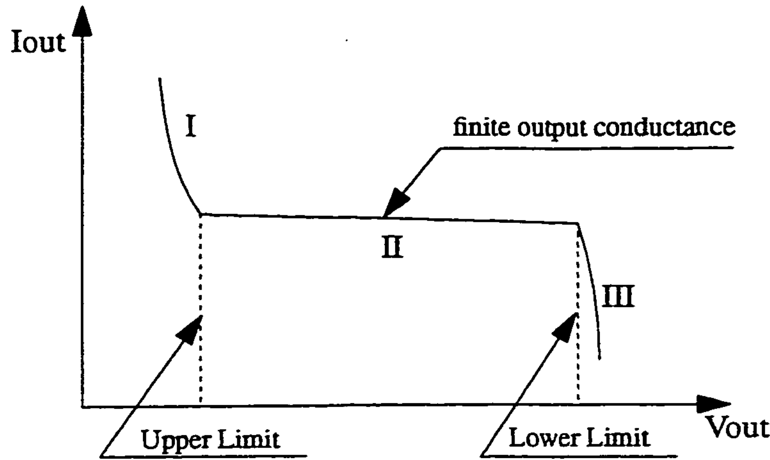


Fig. 3.3 Dependence of output current of the simple transconductance unit on output voltage.

Table 3 Voltage Output Limitations

Technology	Soft Upper Limits	Soft Lower Limits	Hard Upper Limits	Hard Lower Limits[a]
P-Well Process	V_{SS}	V_{DD}	V_{SS}	$V_{DD} - \lvert V_x \rvert$
N-Well Process	V_{DD}	V_{SS}	V_{DD}	$-(\lvert V_{SS} \rvert - \lvert V_x \rvert)$

a. Even we put "hard" there, such bounds given here can not be viewed as an explicit representations of the hard lower limits. These *hard lower limits* (better approximation than their soft counterparts, and therefore named hard) below which the circuit does not work, indicate that acceptable output voltage is really dependent on the input signal levels. V_X is the voltage at node x shown in Figs.3.1 and 3.2.

Here to calculate the lower limit to V_{out} (output voltage), we take the observation that if V_{out} is lower than V_x, after which the output node becomes the source of M_4, and node x becomes the drain. The interchange of source and drain of M_4 results in a reversal of current through M_4 - I_2 becomes negative instead of positive. In this case, the output current increases from two equal contributions of the same sign. The performance of the VCT now will drift from it is expected. Therefore, it is the limitation on the operation and

we put it into Table 3. Once the design parameter is given (transistor dimensions and the values of reference voltages), V_X can be determined either roughly by hand calculation using the method we introduced in previous section or more accurately by HSPICE simulation. As Vx is known, these output voltage limits will serve as part of the specifications for interconnection of VCT and following signal processing stages.

3.5 Common Mode Range

As we assumed that all the transistors are operating in the saturation region, here we attempt to determine the common mode range (CMR) of voltages at input. As a matter of fact, both M_1 and M_2 transistors should operate in the saturation region at all the time, transistors M_3 and M_4 can be operate in either linear or saturation region, even though we assumed that they were saturated for the sake of a simpler mathematical operations (actually, it is the case most of the time when the circuit is operating). Consequently, the range of input voltages V_1 and V_2 can be obtained by just considering the conditions that

$$\begin{aligned} &V_{DS1} < V_{GS1} - V_{Tp} \qquad (a) \\ &V_{GS1} - V_{Tp} < 0 \qquad (b) \end{aligned} \tag{3.18}$$

Dynamic range can also be determined by using the equations shown in Table 2. As stated above, transistors M_3/M_4 can operate in either the saturation region or the linear region as long as the current can pass through. Therefore,

$$V_{supply} > |V_{DS5}| + |V_{DS1}| \tag{3.19}$$

where $V_{supply} = |V_{DD} - V_{SS}|$. Since transistor pair M_5/M_6 constitutes a current mirror, we may make a simple assumption that $|V_{DS5}| = |V_{Tp0}|$. Then the eq. (3.19) will be rewritten as

$$|V_{DS1}| < V_{supply} - |V_{Tp0}| \tag{3.20}$$

To insure the p-device operating in the saturation mode, a condition that $V_{DS1} > V_{GS1} - V_{Tn}$ has to be satisfied. We will not consider the lower bound, since the lower bound definitely will be the case where the bulk terminal is forward-biased. We would assume that this value may happen when $|V_{BS}| < 0.5$ volt.

Using the combination of strategies introduced while deriving the DC characteristics and eqs. (3.18) to (3.20), we can arrive at the following

$$\frac{C}{\left[|a_1| + \frac{(1-|a_1|)}{2(\phi_p - V_{A0})}\right]} < V_1 < \frac{C}{\left[-|a_1| + \frac{(1-|a_1|)}{2(\phi_p - V_{A0})}\right]} \tag{3.21}$$

where

$$C = 2V_{ss} - V_{ref1} + V_{Tp0} - V_{A0} + \sqrt{\gamma_p \phi_p} + \gamma_p (V_{A0} - \phi_p) \tag{3.22}$$

Basically, the common mode range should be in the range of 20% to 50% of voltage supply as the equations above suggest.

3.6 Numeric Simulation for DC Analysis

Derivation of the operating DC equations of the VCT has not been very straightforward. We had to make several approximations and assumptions to overcome the difficulty. In order to get more accurate values from the circuit, we may go for a numeric computation applying a simple algorithm in a computer. The flow chart of the numerical simulation algorithm is given as Fig.3.4.

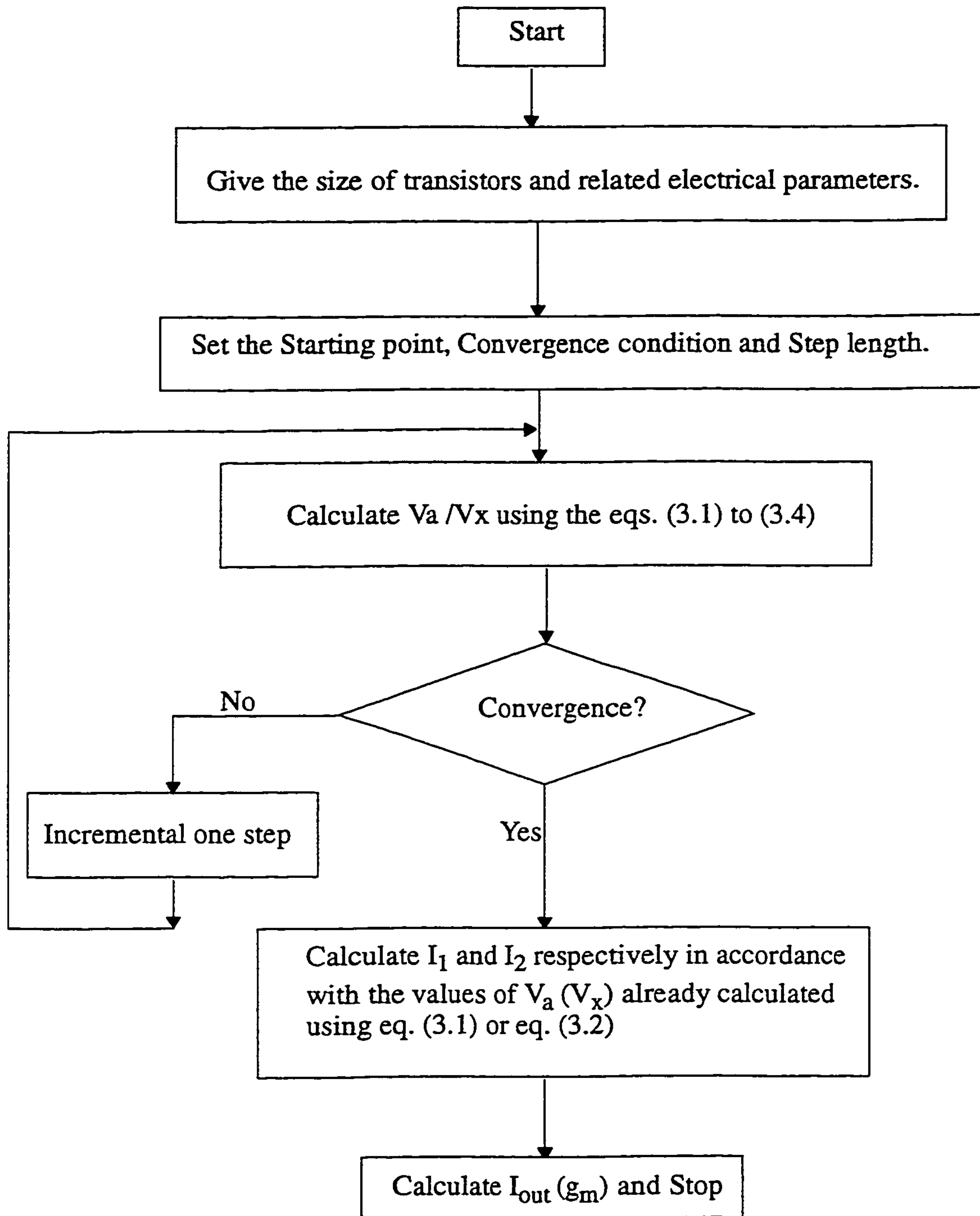


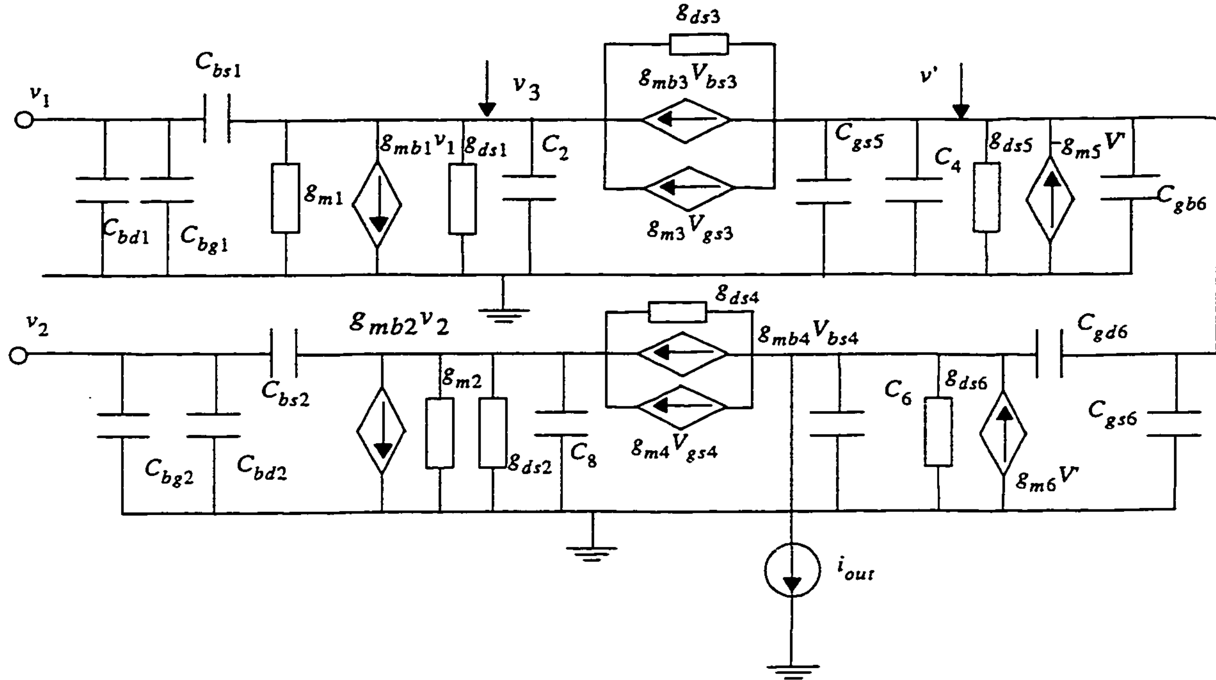
Fig. 3.4 Determining DC operating point (a numeric approach flowchart).

Through observation and simulation, we found that the functions were well behaved (mathematically); therefore, we may use Newton-Raphson (also called Secant) Method[21] which has a fast convergence rate. The Newton-Raphson technique demands the computation of first derivatives. These derivatives are usually computed analytically. In some cases, however, the model equations are so complicated that it is tedious, cumbersome and error prone to compute analytical derivatives. Numerical derivatives using the finite difference method may be used in these situations, but this increases the model computation time. During the Newton-Raphson iterations, it is possible to encounter wide variations in the terminal voltages [17, 21]. Therefore, it is important to consider the entire voltage range while formulating the model equations even though the device will not encounter these voltages in practical circuits [17].

3.7 AC Characteristics

The ac small signal model introduced in the chapter 2 will be applied to construct the ac equivalent circuit of the proposed bulk-driven VCT (see Fig.3.5). The two-port nodal admittance matrix (NAM) for the VCT can be derived through inspection, simplification, and node suppression.

To alleviate massive math manipulation, we may assume that $g_{ds3} = g_{ds4} = 0$; as a result, the ac small signal equivalent circuit can be simplified as shown as Fig.3.6.

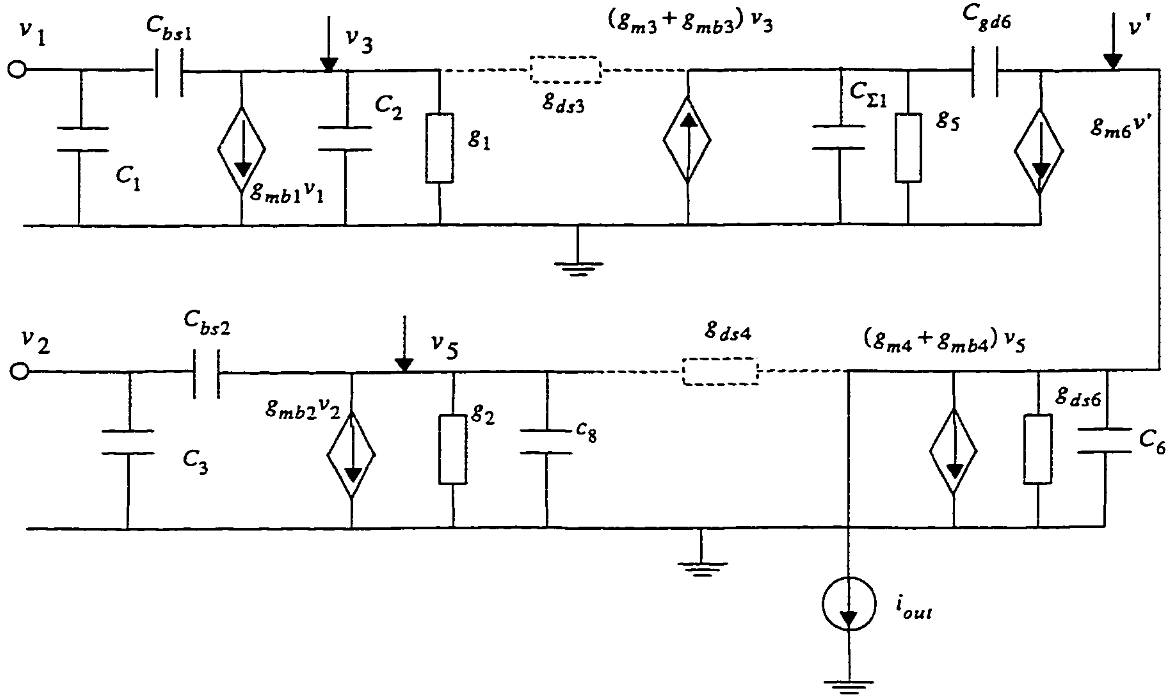


$C_2 = C_{gd1} + C_{gs1}$ $\quad$ $C_6 = C_{bd6} + C_{bs6}$

$C_4 = C_{bd5} + C_{bs5}$ $\quad$ $C_8 = C_{gd2} + C_{gs2}$

$v_{gs3} = v_{ds3} = v_3$

Fig. 3.5 AC equivalent circuit of the proposed bulk-driven VCT.



$C_2 = C_{gd1} + C_{gs1}$ $\qquad$ $C_6 = C_{bd6} + C_{bs6}$

$C_4 = C_{bd5} + C_{bs5}$ $\qquad$ $C_8 = C_{gd2} + C_{gs2}$

$C_1 = C_{bd1} + C_{bg1}$ $\qquad$ $C_{\Sigma 1} = C_4 + C_{gs5} + C_{gs6}$

$g_1 = g_{m3} + g_{mb3} + g_{ds1} + g_{m1}$ $\qquad$ $g_2 = g_{m4} + g_{mb4} + g_{ds2} + g_{m2}$

$g_5 = g_{ds5} + g_{m5}$

Fig. 3.6 Simplified AC small signal equivalent circuit of the VCT.

Using routine nodal analysis technique to the circuit, we arrive at

$$i_{out} = (g_{m4} + g_{mb4}) \frac{C_{bs2}S - g_{mb2}}{(C_8 + C_{bs2})S + g_2} v_2 + (-g_{m6} + C_{gd6}S) \frac{g_{m3} + g_{mb3}}{(C_{gd6} + C_{\Sigma 1})S + g_5} \frac{C_{bs1}S - g_{mb1}}{(C_2 + C_{bs1})S + g_1} v_1 \tag{3.23}$$

where those clustered representations of capacitors and transconductances are given in Fig.3.6.

When the proposed VCT is used in the low frequency applications, we may further ignore the impact of the parasitic capacitors; thereby, we land on

$$i_{out} = (g_{m4} + g_{mb4}) \frac{g_{mb2}}{g_2} (v_1 - v_2) = g_{ac}(v_1 - v_2) \tag{3.24}$$

where

$$\begin{aligned} g_1 &= g_{m3} + g_{mb3} + g_{ds3} + g_{m1} \\ g_2 &= g_{m4} + g_{mb4} + g_{ds2} + g_{m2} \\ &\quad and \\ g_{ac} &= (g_{m4} + g_{mb4}) \frac{g_{mb2}}{g_2} = (g_{m3} + g_{mb3}) \frac{g_{mb1}}{g_1} \end{aligned} \tag{3.25}$$

Note that transistor pairs matching are implicitly assumed in eq. (3.25). That is $\frac{g_{m4} + g_{mb4}}{g_2} = \frac{g_{m3} + g_{mb3}}{g_1}$.

Above equations clearly show that the ac transconductance of bulk-driven VCT is relatively small compared to that in a normal gate-driven device, since bulk transconductance (g_{mb}) is generally smaller than transconductance (g_m). To boost the value of transconductance, an easy and intuitive way is to increase the dimensions (ratio of width to length) of transistors M_1 through M_4. Obviously, such increase will introduce higher parasitic capacitors, resulting to reduced working bandwidth. Therefore, it is recommended

that the bulk-driven VCT to be used in low frequency applications. It is important to note that the critical frequency of a g_m-C filter depends on the ratio of g_m/C. For low frequency applications, the value of g_m can be small so that the value of the capacitor can be made reasonably small, because it is not easy to integrate a large capacitor. As a matter of fact, high transconductance is not desired in a low frequency application; only the opposite is true.

3.8 CMRR Analysis

The signals that are fed to the two input terminals of the proposed VCT can be decomposed into a difference-mode signal, V_D, and a common-mode signal, V_C. This is illustrated by the following relations, where V_1 and V_2 are two arbitrary input signals.

$$\begin{aligned} V_1 &= \frac{V_D}{2} + V_C \qquad (a) \\ V_2 &= \frac{V_D}{2} - V_C \qquad (b) \end{aligned} \tag{3.26}$$

As to a VCT, the ratio of the differential-mode gain (transconductance, g_D) to the common-mode gain (transconductance, g_C) is defined as the common-mode rejection ratio (CMRR), namely

$$CMRR = 20lg\frac{g_D}{g_C} \tag{3.27}$$

Ideally, the CMRR should be as large as possible. Consider the eq. (3.24) and Fig.3.6, we may approximate the CMRR as follows:

$$CMRR \approx 20lg\left|(g_{m4} + g_{mb4})\frac{g_{mb2}}{g_{\Sigma}}\right| \quad (3.28)$$

where

$$g_{\Sigma} = g_{m4} + g_{mb4} - g_{m3} + g_{mb2} + g_{m6} - g_{m5} + g_{m2} - g_{m1} \quad (3.29)$$

Eq. (3.28) clearly manifests itself that if the transistor pairs are perfectly matching to each other and biasing for the two columns of the transistor is exactly the same, infinite CMRR is achievable. This observation is totally based on the theoretical viewpoint. However, to achieve matching in terms of biasing is not easy in reality.

3.9 PSRR Analysis

The variation of the power supplies will in some way impact the performance of a circuit, since many of the input signals are coupled to the circuit through the power supply lines (e.g., spikes due to switching of digital circuit on the same chip). To evaluate the impact of the power lines to a VCT circuit, the power supply rejection ratio (PSRR) is defined as the ratio of the transconductance to the change in the output current of the VCT caused by the change in the power supply. Ideally, VCT should have an infinite PSRR. Practically, it is important that the VCT should exhibit good power supply rejection. The PSRRs for positive and negative voltage sources (V_{DD} and V_{SS}) are defined by equations (3.30) and (3.31) respectively.

$$PSRR\,(V_{DD}) = \frac{\Delta V_{DD}}{\Delta i_{out}} g_m \quad (3.30)$$

$$PSRR\,(V_{SS}) = \frac{\Delta V_{SS}}{\Delta i_{out}} g_m \tag{3.31}$$

The PSRRs can be calculated in such a way that from the transconductance equation, we assume V_{DD} (or V_{SS}) is a variable and calculate the first partial derivative of V_{DD} (or V_{SS}) over the current output. It can be viewed from eq. (3.8) that the output current is not related to the value of the most positive voltage source V_{DD} for a n-well process. As a result, the $PSRR\,(V_{DD})$, theoretically, can be as large as infinity. On the other hand, the output current is related to the V_{SS} (equations (3.8), (3.12), and (3.10)) and therefore, the PSRR for the negative voltage source (positive voltage source) for an n-well process (p-well process) is poorer.

3.10 Noise Analysis

Noise in integrated circuits is one of the most important factors that determines the performance of low level integrated signal processing systems such as a transducer [15]. It represents a lower limit to the size of the electrical signal that can be handled by an integrated circuit without significant deterioration in signal quality.

In this section the noise behaviors of the proposed VCT are investigated in detail. For each noise source, physical origins and mechanisms are discussed and the relationships to the process, and particularly to the design parameters are studied. These relationships form the foundation for a practical design.

3.10.1 Noise Sources

Noise Sources related to a bulk-driven circuit[12] can be distinguished as four major categories:

(1) thermal noise associated with the conducting resistive channel.

(2)flicker or 1/f noise.

Above two noise sources are the major noise contributors for MOS transistors. To our particular circuit, two more noise resources have to be taken into our considerations. They are

(3) the noise associated with the resistive poly-gate, and

(4) the noise due to the distributed substrate resistance.

It can be found from the SPICE documentation that four mechanisms are listed as the primary contributors to the presence of noise in MOSFETs [16]. Two noise-current generators are modeled in the same way as the first two in our noise generator category. The other two are associated with the parasitic series resistances in the drain and source terminals. These two noise sources will not be pursued here since they are strongly connected with the values of the parasitic resistors with respect to their terminals and are difficult to be evaluated from a designer's point of view. Basically, these two noise resources provide some noise as a normal resistor does.

3.10.2 Thermal Noise

The thermal noise (also called channel thermal noise) of a MOSFET is associated with the conducting resistive channel. The inverse resistive channel is formed by the

12. Since all the transistors of the proposed bulk-driven VCT are operating in the saturation region, the noises introduced will be concentrated on saturated transistors only.

minority carriers in the substrate under the appropriate control of the gate voltage. The noise is generated due to the random motion of free carriers within the channel, analogous to that in a normal resistor. To predict the channel thermal noise behavior of MOSFETs with negligible substrate effect, a simple and also widely used expression is given as follows,

$$i_d^2 = 4kT\frac{2}{3}g_m \tag{3.32}$$

where g_m is the transconductance of the MOSFET, k is the Boltaman constant, and T is the absolute temperature. However, equation (3.32) does not take the dependency of V_T on the channel potential (i.e., along the channel, the threshold voltage V_T is not a constant since for each position of the channel, the voltage is slightly different due to the voltage drop) into account. Apart from the impact of the channel potential, since we are dealing with the bulk-driven circuit, the dependence of V_T on the channel potential also comes from the depletion charge variation due to the substrate effect. Therefore, in order to predict the noise performance of a bulk-driven MOSFET in a more accurate way, we have to modify the eq. (3.32) with a factor γ. Now we proceed to

$$i_d^2 = 4kT\gamma g_m \tag{3.33}$$

where γ is a very complex function of the basic transistor parameters and bias conditions. For modern CMOS processes, the factor γ is situated between $0.67 < \gamma < 1$ [18]. Notice that when $\gamma = 0.67$, eqs. (3.33) and (3.32) are the same.

3.10.3 1/f Noise

The 1/f noise has been observed in almost all kinds of devices. The mechanism of

producing this noise is not quite understood very well now and intensive research is still on its way. Among all active integrated devices, MOS transistors show the highest 1/f noise of all due to their surface conduction mechanism. Some practical models have been presented by semiconductor physicists. Among them, McWhorter's number fluctuation model shows sound agreement between the theoretical predictions and experiments. The mean square current for 1/f noise is given by

$$i_d^2(f) = \frac{K_F I_{DS}}{C_{ox} L^2 f} \tag{3.34}$$

where K_F is a constant, C_{ox} is the gate oxide capacitance per unit area, I_{DS} is the drain source current through the transistor. Furthermore, the mean square voltage for 1/f noise is also given by

$$v_f^2(f) = \frac{K_f}{C_{ox}^2 W L f} \tag{3.35}$$

where $K_f = K_F/2\mu$. Eqs. (3.34) and (3.35) are widely used in low noise CMOS amplifier design. These equations suggest that larger area might be helpful to reduce the 1/f noise, since $v_f^2(f) \propto \frac{1}{WL}$.

Generally speaking, by applying larger MOSFETs and high dc bias levels, low noise (*1/f*) circuit is possible. This suggestion is purely coming from the viewpoint of reducing the *1/f* noise. Since the proposed bulk-driven VCT is mainly working in the low frequency range, this relationship is a good news for us. That is we may use larger transistor to get higher transconductance; at the mean time, the *1/f* noise is lowered. Nevertheless, area and even more concerned power penalties are obvious to follow this suggestion.

For most practical cases, the use of these two noise sources is sufficient enough to conduct the noise analysis and direct circuit design. Apart from these two noise sources,

their still exist some minor noise sources and we will go over to have a look at them in the following two subsections.

3.10.4 Resistive Ploy-Gate Noise

The resistive poly-gate related noise is a layout-oriented noise source [15]. In the proposed bulk-driven circuit, large MOSFETs are more often encountered so as to meet the requirement for the transconductance; the layout design, thus, deserves a closer attention. Usually, for MOS transistors with large *W/L* ratio, a popular finger structure has to be employed to keep the resistive poly-gate noise to a reasonable low level. This finger structure divides the total width of a transistor into n poly stripes with an equal width. That is, a fat MOS transistor can be replaced by n smaller parallel connected transistors with equal dimensions. In addition, these n transistors should be able to reside in one single well. The total output drain noise spectrum due to all the n gates is given as [15]

$$i_d^2 = 4kT\frac{R_g}{12n^2}g_m^2 \tag{3.36}$$

where R_g is the total gate resistance (for n gates) and g_m is the total transconductance of the MOSFET under consideration. It has been shown [15] that if no care is taken in the layout design stage, i.e., n=1, this noise may even dominate the channel thermal noise for a transistor with the size like 3000u/3u (W/L). Eq. (3.36) clearly manifests itself that larger n (like 10) will drastically reduce the noise to a negligible level.

3.10.5 Substrate Resistive Noise

A lumped resistor R_b will be used to describe the nature of the substrate resistances.

The dominant factor can be viewed as the resistor lumped from the equivalent distributed resistance between the point underneath the channel and the bulk contact on the top of the wafer. If the device layout is a finger structure composed of n poly stripes, the total noise current due to all stripes is given by [15]

$$i_{dB}^2 = 4kTB\frac{b}{W}g_{mb}^2 \tag{3.37}$$

where B is a proportionality constant, g_{mb} is the bulk transconductance, b is the distance between the channel and the substrate pole connecting to the outside. Eq. (3.37) attests that the layout structure plays little impact on the noise contribution. To a bulk-driven circuit, the transconductance of the overall circuit is heavily relying on g_{mb}; therefore, values of g_{mb} in these cases are higher than those of normal gate-driven circuits. As a result, bulk-driven circuits have higher substrate resistance noise level. Note that $i_{dB}^2 \propto \frac{b}{W}$, which means increasing the width W has no impact on the noise reduction since b will increase the same magnitude with respect to the increase of width W accordingly. We, thereby, can not diminish this kind of noise by some technical means, like some particular layout structure. To a gate-driven device, this resistance noise related to the substrate can be minimized by making g_{mb} minimal through smart and careful biasing on the potential difference between the bulk and source terminals. Unfortunately, to a bulk-driven circuit, small or modest g_{mb} seems to be the only appropriate solution in terms of reduced substrate noise. This is particularly true for a ultra low-noise requirement.

On the other hand, compared to the thermal noise and *1/f* noise, this noise source is quite small. Therefore, we will not be bothered to consider this noise source at all in most design cases. Only when an ultra low-noise design is required will drag a designer to look at this noise source.

3.10.6 Small Signal Model and Noise Sources of one MOS Transistor

The ac equivalent circuit of a MOSFET can be extended to include the noise sources described above. This is presented in Fig.3.7, shown below. This work is helpful to determine the minimal input signal which can be handled by the circuit before the noise degrades the signal quality.

These two equivalent noise generators are ready to be derived by using the approach as follows. First short circuit all input terminals of Fig.3.7.a, Fig.3.7.b (bulk is the input terminal), and Fig.3.7.c (gate is used as the input terminal) and equate the total output noise i_0^2 to obtain the v_i^2. To obtain i_i^2, just open all the circuit inputs and equate the total output noise i_0^2. After a straightforward calculation the three equivalent input noise generators for a MOSFET (gate-driven) are given by[13]

$$v_{ig}^2 = \frac{(i_d^2 + i_f^2 + i_{dB}^2)}{|g_m - j\omega C_{GD}|^2} + 4kTR_g \tag{3.38}$$

$$i_{ig}^2 = |j\omega(C_{GS} + C_{GD})|^2 \frac{(i_d^2 + i_f^2 + i_{dB}^2)}{|g_m - j\omega C_{GD}|^2} \tag{3.39}$$

where i_{dB}^2 represents the noise contribution of the substrate resistance and is given by equation (3.37). i_d^2 and i_f^2 are given by equations (3.33) and (3.34), respectively. Note that $g_m/2\pi C_{GD}$ is much smaller than the transistor cut off frequency f_T, the term $j\omega C_{GD}$ can be neglected with respect to g_m for practical cases of interest [15].

13. For clear representation, the noise generators which uses gate as the input terminal will be assigned a "g" in the corresponding subscripts, and generators which uses bulk as the input terminal will be assigned a "b" in the corresponding subscripts as well.

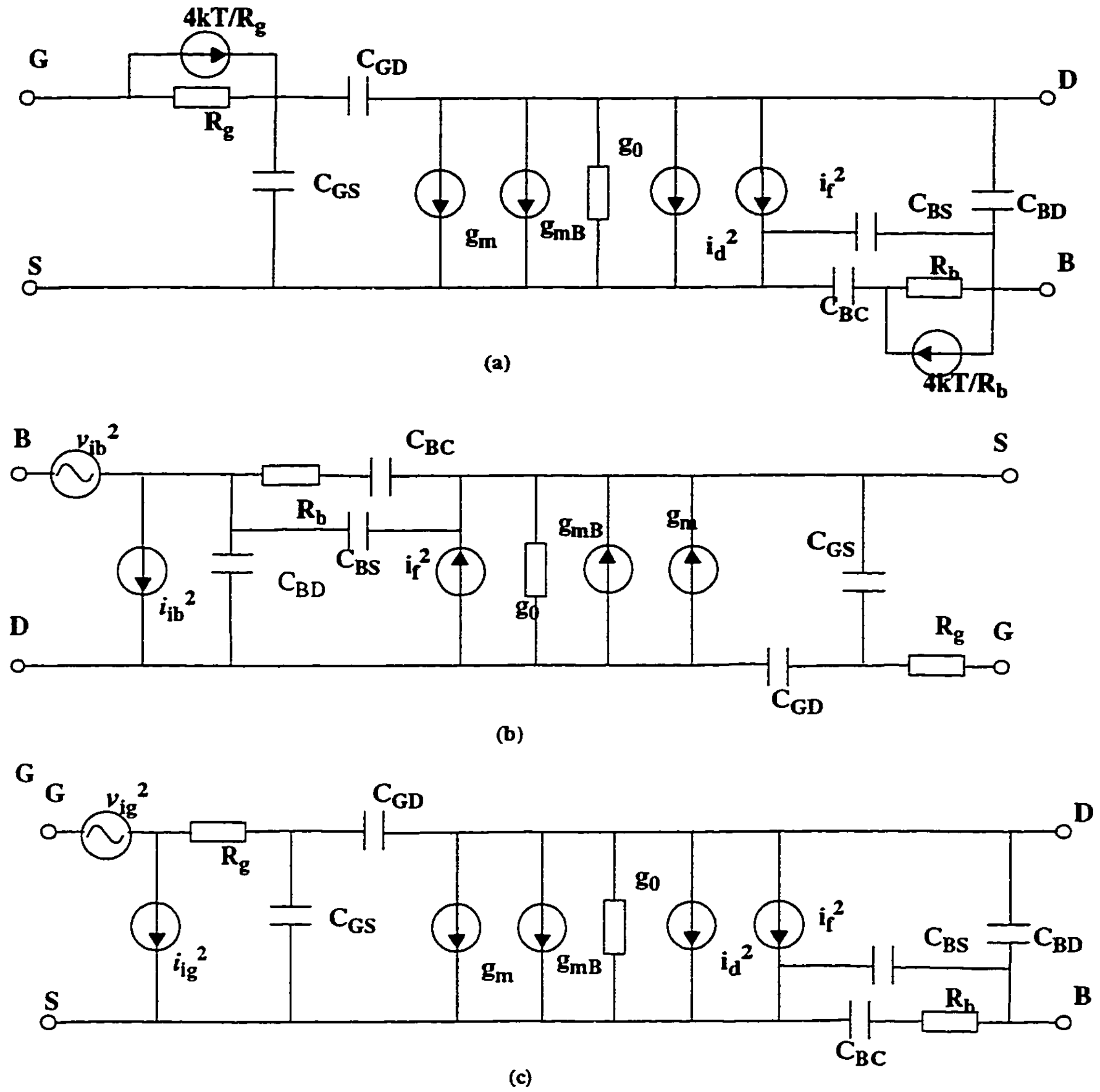


Fig. 3.7 (a) Small Signal Model and Noise Sources of a MOS Transistor.

(b) The equivalent input noise generator model with the bulk terminal used as the input.

(c) The equivalent input noise generator model with the gate terminal used as the input.

Note that there is no special significance for direction for those i_d^2, i_f^2, and i_{ig}^2/i_{ib}^2, even though we drew the arrows for the sake of representation.

Similarly, if the C_{BS} can be ignored for simplicity,

$$v_{ib}^2 = \frac{(i_d^2 + i_f^2 + i_{dB}^2)}{|g_m - j\omega C_{GD}|^2} + 4kTR_b \tag{3.40}$$

$$i_{ib}^2 = |j\omega(C_{BD} + C_{BC})|^2 \frac{(i_d^2 + i_f^2 + i_{dB}^2)}{|g_m - j\omega C_{BC}|^2} \tag{3.41}$$

From a designer's point of view working on a particular CMOS circuit, like the proposed bulk-driven VCT, it is necessary to optimize the design parameters (e.g., W, L and I_{DQ}) for each of transistors. Such optimization will reduce the noise generated by the noise source i_d^2 and i_f^2, since they are strongly dependent on these design parameters. On the other hand, optimal layout of the transistors may be required to minimize the impact from the noise sources $4kT/R_b$ and $4kT/R_b$, which are mainly concerned with the physical layout design.

We may further simplify the scheme shown in the Fig.3.7 into a block representation. See Fig.3.8.

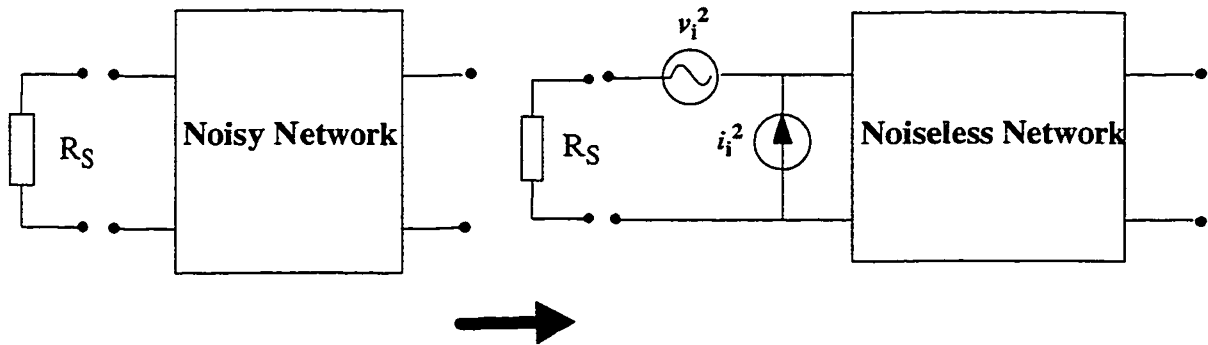


Fig. 3.8 Noise source equivalent representation from a system's view.

By using the approach introduced from the Fig.3.8, we may arrive at what is given in the Fig.3.9. Here i_i^2 noise source has been ignored.

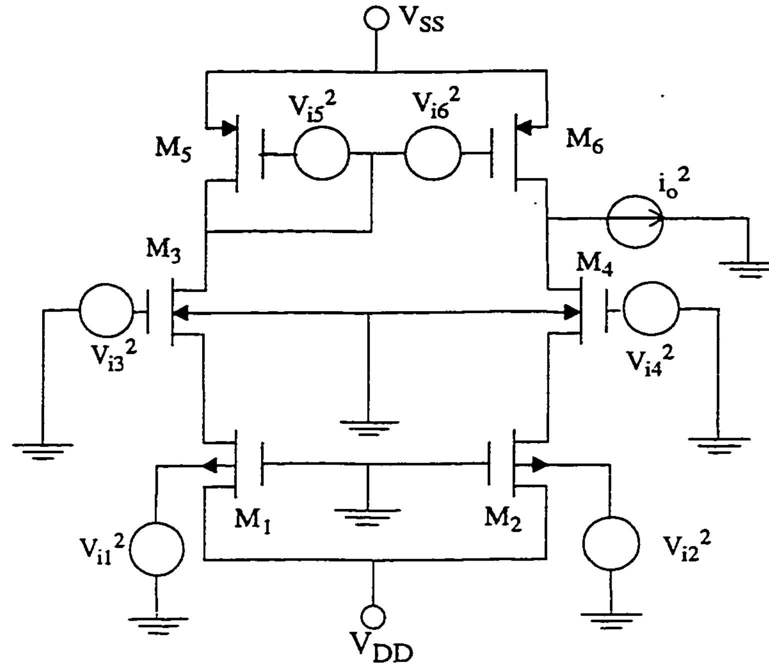


Fig. 3.9 Equivalent noise circuit of the proposed bulk-driven VCT.

The ac equivalent network for the bulk-driven VCT at the input is shown in Fig.3.10. Note that such equivalence is not valid for large signal MOSFET operation (input-referred noise source). The equivalent input noise voltage generator V_{eqT}^2 is given by

$$V_{eqT}^2 = V_{i1}^2 + V_{i2}^2 + \left(\frac{g_{m3}}{g_{mb1}}\right)^2 (V_{i3}^2 + V_{i4}^2) + \left(\frac{g_{m5}}{g_{mb1}}\right)^2 (V_{i5}^2 + V_{i6}^2) \tag{3.42}$$

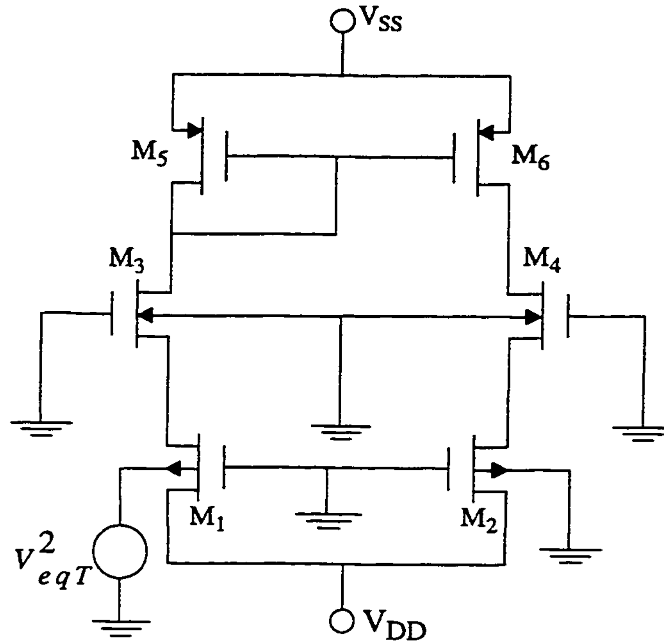


Fig. 3.10 AC equivalent noise voltage generator for proposed bulk-driven VCT.

Therefore, from the system's view point, in order to achieve low noise design, the transconductance, g_{mb1} should be made as large as possible[14], and the transconductances of M_3 trough M_6 should be small as eq. (3.42) suggests. Obviously, as already alluded previously, optimizing each individual transistor is also critical to accomplish the low noise requirement. In most design work, wider transistors M_1 and M_2 are adopted, based on such considerations. However, if they are too fat in terms of dimensions, special layout considerations must prevail, like using the finger structure to minimize the gate resistance noise introduced before.

It is always claimed that a current-mode signal processing unit exhibits higher noise level than its voltage-mode counterpart. In the physical world, particularly most of the interface circuits are using voltage signals; VCT as the interface between the voltage input

14. Note that this is the signal input transistor. It really tells us we would use a transistor with large transconductance to receive the voltage signal input and transform it to a current representation.

to further current-mode signal processing units, should take the noise into a serious consideration. Low noise design is possible if cautions are taken at the early stage. Again, it is always the specification of a particular design determines which parameter or parameters command special considerations (e.g., linearity, low voltage power, low noise, frequency response, etc.).

3.11 HSPICE Simulation Results

HSPICE simulations have been performed to test the bulk-driven VCT. The basic parameters of the circuit is shown in the Table 4.

Table 4 Simulation Parameters

<table>
<tr><td rowspan="3">Transistor size (μm)</td><td>M1/M2</td><td>150/3</td></tr>
<tr><td>M3/M4</td><td>10/3</td></tr>
<tr><td>M5/M6</td><td>5/6</td></tr>
<tr><td>Voltage supplies (V)</td><td colspan="2">3V (±1.5)</td></tr>
<tr><td rowspan="2">Reference Voltages (V)</td><td>Vref1</td><td>0.8</td></tr>
<tr><td>Vref2</td><td>-1.5</td></tr>
<tr><td>Technology</td><td colspan="2">ISO-HCMOS (see Appendix A)</td></tr>
</table>

3.11.1 DC Characteristics

The test bench of testing the DC characteristics is shown in Fig.3.12. The test result is shown in the form of V_{in} vs. I_{out} in Fig.3.12.

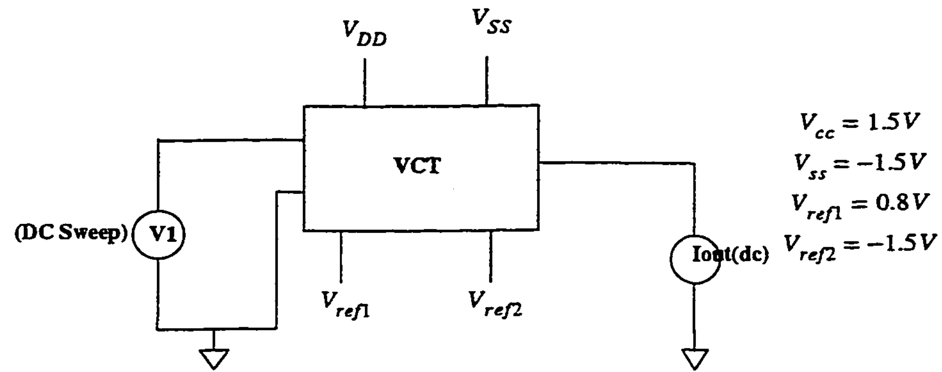


Fig. 3.11 DC characteristics of the bulk-driven VCT: test bench construction

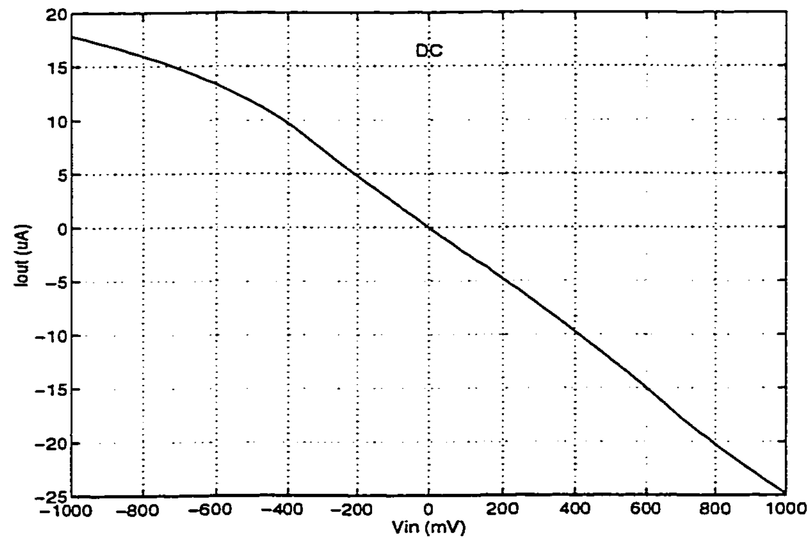


Fig. 3.12 DC characteristics of the bulk-driven VCT: HSPICE simulation result

It can be shown that the linear region spans from almost half of the rail-to-rail voltage (i.e., good large signal handling capability) and the negative and positive sides are not strictly symmetrical to the zero point (input voltage is zero). Also note that the proposed

VCT does not show any clipping outside its linear range. Instead, the output current varies parabolically with respect to the input voltage in this region.

3.11.2 AC Characteristics

Test bench of testing AC characteristics is built as shown in Fig.3.13. Graphical exhibition of the simulation results is given as Fig.3.14. All the hardware condition is same as those of the DC analysis (listed in Table 4 (see page 63)). The frequency sweep is from 1Hz to 100 MHz.

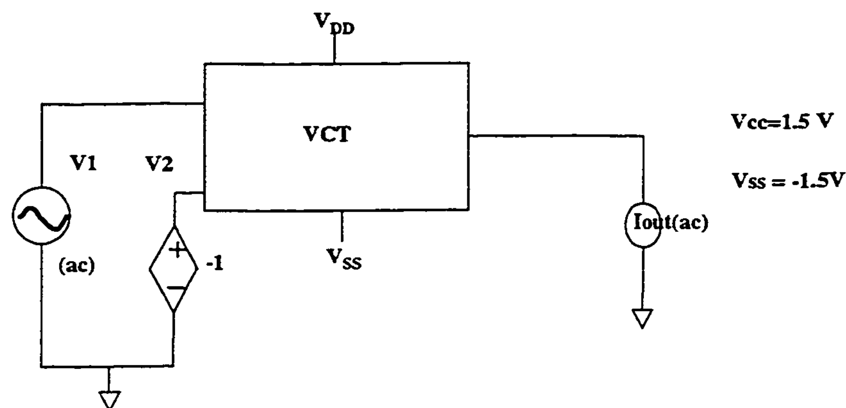
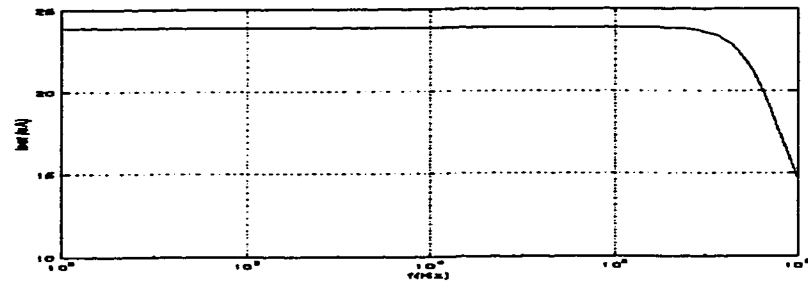
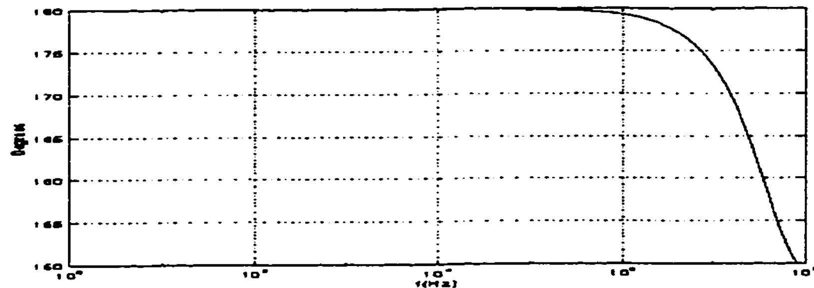


Fig. 3.13 AC analysis of the proposed VCT: test bench.



(a) Magnitude response



(b) Phase response

Fig. 3.14 AC analysis of the proposed VCT: simulation results.

It can be viewed from the curves that the frequency characteristics of output current. Below 1.5 MHz, the phase shift is less than 1°.

3.11.3 Statistical Characteristics

As it is known, an electrical circuit must be designed to lead to maximum process yield. This implies the number of parts (as a %) that passes the given specifications. HSPICE can be used to analyze the effects of elements and model parameter variation via Monte-Carlo analysis.

The iteration number (i.e., independent samples) is set to 30; this value is derived based on the fact that the statistical significance of 30 iterations is quite high. It has been shown that if the circuit operates correctly for all 30 iterations, there is a 99% probability that over 80% of the samples will operate correctly[19]. Here we will consider DC sweep and AC sweep analyses in terms of the statistical variations of the channel length, threshold voltages, and lithography of each MOSFET. Each MOSFET is assumed to have a random Gaussian characteristic for the variation of its channel length. It is assumed to be 5% of the ±3 sigmal level. Similarly, the threshold voltage and the lithographic variations are assumed to have the same characteristic.

Comparing Fig.3.16 with Fig.3.12, we may find some variations in terms of DC characteristics as expected. Some nonlinearity my be introduced close to the ±1 Volt end. AC transconductance may vary with the variation of the process parameters. The phase response is quite immune to the variation of the process parameters (see Fig.3.14 and Fig.3.16 respectively).

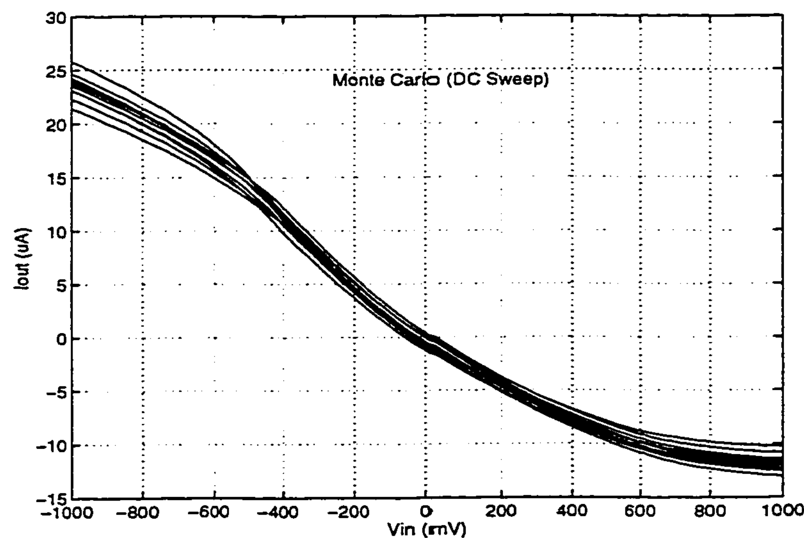
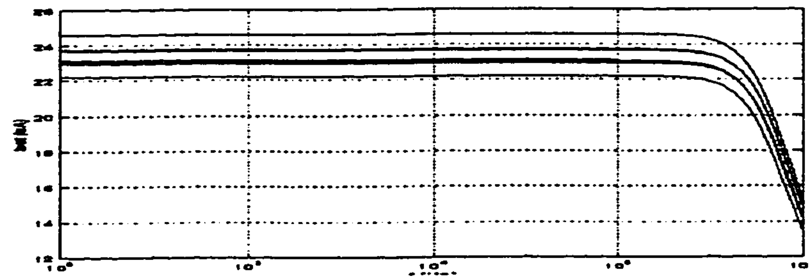
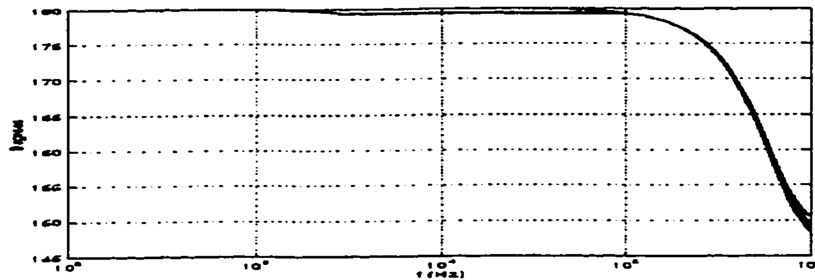


Fig. 3.15 Statistic characteristics of the VCT: DC Sweep.



(a) Magnitude response



(a) Phase response

Fig. 3.16 Statistic characteristics of the VCT: AC Sweep.

3.11.4 Other Characteristics

The HSPICE simulation result on CMRR of the circuit is shown in Fig.3.17. The sizes of the transistors are same as before. Basically, this circuit has good CMRR. At low frequency range (below 100 KHz), the CMRR is above 55 dB. When the frequency goes up to 1 MHz, the CMRR is over 40 dB.

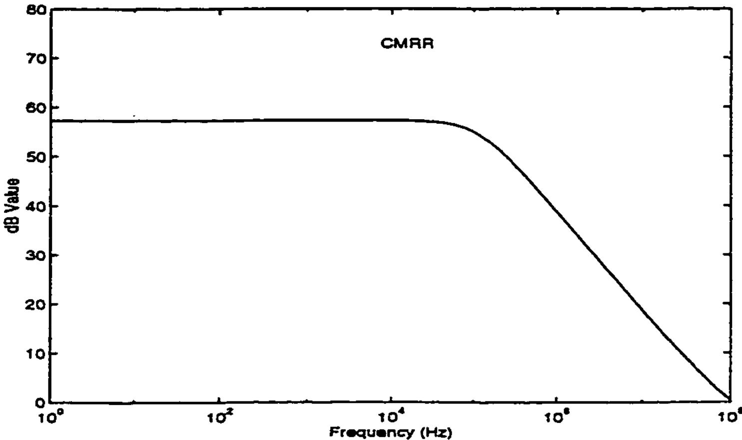


Fig. 3.17 CMRR of the bulk-driven VCT.

The test bench of testing the PSRR (for both V_{DD}) is shown in Fig.3.18 (Note that test bench for testing PSRR (Vss) should be similar to the one shown here), and Fig.3.19 shows the HSPICE simulation results regarding to the PSRR characteristics of the bulk-driven VCT, where curve I shows the PSRR(V_{DD}) and curve II the PSRR(V_{SS}). It can seen PSRRs are quite stale in the whole testing frequency range.

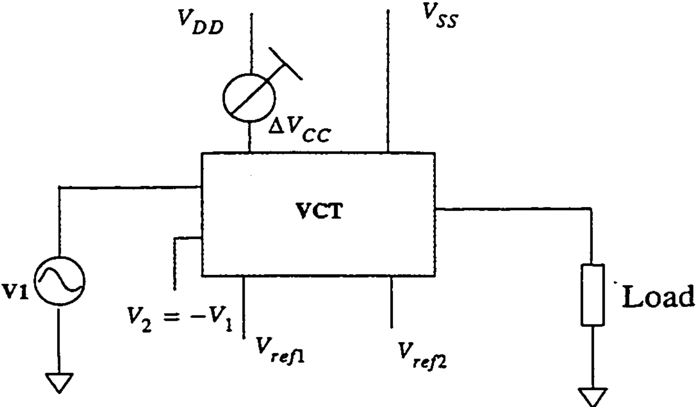


Fig. 3.18 Test bench construction for testing PSRR (V_{DD}).

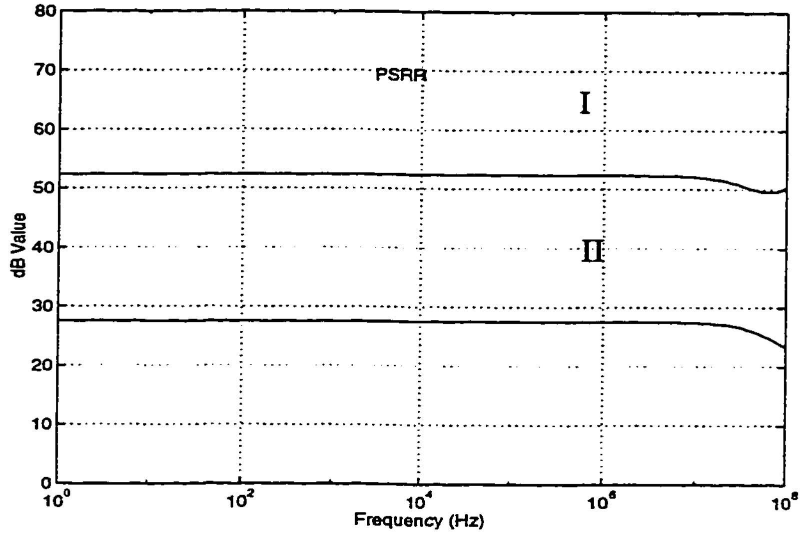


Fig. 3.19 PSRR characteristics for the bulk-driven VCT.

Noise simulation has been performed in HSPICE (same simulation conditions shown in Table 2). The normalized total output noise level (with respect to the square root of the noise bandwidth) is 1.28×10^{-10} $volts/\sqrt{Hz}$ (up to 10 MHz). The simulation results are summarized in Table 5.

Table 5 Noise Characteristics Simulation

Frequency (Hz)	Total Output Noise Voltage (V)	Total Equivalent Voltage Noise[a] (V)	Normalized Output Noise Level $(volts/\sqrt{Hz})$
1 - 1K	4.06 n	169.7 u	1.28×10^{-10}
<100K	38.50 n	1.61 m	
<1M	121.73 n	5.09 m	
<10M	384.96 n	16.1 m	

a. That is at the node where current is outputted (node I_{out} in Figs.3.1 and 3.2).

Note that the total output noise voltage is the RMS (Root Mean Square) sum of the individual noise contributions:

$$outnoise = \sum_{n=1}^{N} |Z_n I_n|^2 \tag{3.43}$$

where I_n refers to equivalent current due to thermal noise, shot or flicker noise, Z_n is the equivalent transimpedance between noise source and the output, and n shows the number of associated noise sources.

3.12 Performance Evaluation / Comparison

We have already seen that several versatile CMOS VCTs have been proposed so far. They vary from the architecture, size of transistors, numbers of voltage and current sources, the power supplies, and so on and so forth. How to justify the "goodness" of all these amazing circuits lies on how we choose the appropriate criteria applicable. Quite a number of criteria have been suggested and applied, such as linearity, noise level, matching, voltage supply level, etc. At the home university, Dr. Raut presents a brand new idea by using the ratio of transconductance of a VCT circuit to its power consumption as the criterion to optimize his VCT circuit (see Fig.1.4). Therefore, the evaluation of the power efficiency for the circuit boils down to looking at the transconductance level of the target circuit for each unit power consumed in the transducer circuit component. This criterion is based on the observation that the two major parameters of a VCT cell are the value of transconductance and the power consumption; and more important, this criterion links the two parameters in a mathematically-simple, but practically meaningful fashion.

Furthermore, Dr. Raut extends the idea of $g_m/Power$ to $BW/Power$, and alike. It

thus appears that a meaningful criterion for evaluation of the performance of a VCT would be $X/Power$, where X can be, for example, transconductance, bandwidth, and so on so forth. This power-based set of criteria can be used while making comparison between the bulk-driven VCT and a gate-driven VCT which has emphasized very low-voltage low-power operation [9]. To facilitate the calculation, the static power is used. Bear in mind that the major design parameters available for a designer to play with are the dimensions of transistors M_1 through M_4 (see Figs.3.1 and 3.2). The dimensions of the other two transistors, namely M_5 and M_6, are quite independent from the transconductance.

Table 6 A Comparison between the proposed VCT and the VCT reported in [9].

Parameters	VCT in [9] I[a]	Bulk-Driven VCT[b]	VCT in [9] II[c]
Power supplies (V)	3	3	2
Area (μm^2)[d]	260	510	2700
No. of Reference Voltages	1	2	1
g_m (μs)	25[e]	25	70[f]
Power dissipation (μW)	480	40	32
Dynamic range (mv)	180	450	100
area/power ($\mu m^2/\mu s$)	0.1	0.05	0.026
Dynamic range / Power (mv/μW)	0.37	11	1.2
g_m / Power ($\mu s/\mu W$)	0.052	0.62	0.2
Intrinsic Frequency (3dB) (MHz)[g]	80	80	80
BW/Power (MHz/μW)	0.17	2.0	0.22

a. The design parameters are derived by using the transconductance equation given in [9] and iterative HSPICE simulations.
b. For the sake of comparison, we used the design parameter of the fabricated chip presented in Table 9 (see page 91) in a later chapter.
c. The design parameters are directly adopted from [9].
d. Area is coarsely estimated based on the dimensions of transistors used.
e. The reference voltage, shown in Fig.1.7 (see page 15), is 0 V.
f. Again, the reference voltage is 0 volt.
g. The output of the VCTs is connected to a 1 ohm resistor in each case.

Table 6 gives a detailed comparison between VCT in [9] and the bulk-driven VCT, which reflects part of the fact that the proposed bulk-driven VCT is suitable for low power applications. However, while in low frequency (which requires low transconductance value) applications, our proposed VCT will show its advantage in terms of lower power dissipation.

It can be seen from the comparison drawn from Table 6, that $g_m/Power$, $BW/Power$ as well, is a very good indicator to guide the design. HSPICE simulation will be very helpful to determine the maximal $g_m/Power$ value while maintaining desirable value of g_m.

3.13 Optimization and Tunability

The ultimate goal of the circuit designer is not a clever circuit schematic or a computer simulation that predicts the circuit works as anticipated, but an efficiently designed physical piece of silicon that satisfies the original specifications [21].

Optimization is always one of the major concerns regarding to VLSI design and implementation. In order to enhance the performance of the VCT, some optimization strategy has to be adopted. As can be seen that the proposed bulk-driven VCT has four terminals controlled by the reference networks (see Fig.3.2). In order to simplify the design, we only came out with two voltage references (also see Fig.3.1, V_{ref1} and V_{ref2}). However, such arrangement assumes that both two columns of transistors are symmetric. In some critical design, we may use four voltage reference network to fully balance the two columns. Now the circuit will look like Fig.3.20 (in a P-well technology). That is, all the gate terminals of the transistors M_1 through M_4 are now available to be controlled by independent voltage references.

In order to simplify the circuit, the reference voltage source V_{ref1} and V_{ref3} can be connected as one, and therefore, leave only three voltage references being used. This strategy is particularly useful when several stages need to be cascaded to realize, for example, a high order filter.

Fig. 3.20 Bulk-driven VCT with 4 voltage references.

One obvious drawback of this scheme is that the area overhead is caused due to introduction of an additional voltage source. However, with the third voltage sources available, it is still desirable to have the extra voltage resource to make the designing and tuning a lot easier.

Also note that since the transconductance of the circuit is the function of the reference

voltages. Therefore, the circuit is electronically tunable by controlling the references.

3.14 Summary

It can be found that the proposed bulk-driven VCT architecture has advantages while used in a low power circuit (operating as the voltage source is only 3 volts or even lower). In this chapter, the DC analysis, both by simulation and analytic deduction, shows that the circuit is able to transfer voltage input to a current output in a linear fashion. AC analysis verifies that this circuit has modest frequency response. This VCT has high CMRR. The PSRR is high for one voltage supply and a little poorer for the other one. Noise analysis shows that in order to reduce the noise generated, it is necessary to optimize each of the transistors and the layout design as a whole. This bulk-driven VCT is electronically tunable.

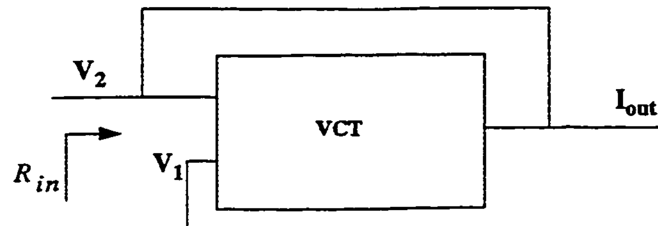
Chapter 4

Applications of the Bulk-Driven VCT

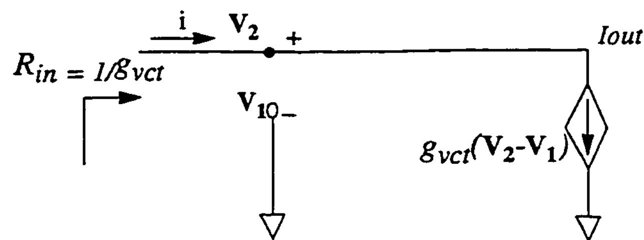
In this chapter, applications of the bulk-driven VCT as a building block for large integrated system is addressed. Thus the case of implementation of a resistance using the VCTs is illustrated. Further, a larger system, namely a third-order low pass filter, using the basic bulk-driven VCT is constructed. In order to integrate a filter architecture in one single chip, a synthesized inductor is necessary. We shall use the knowledge that both grounded and floating inductors can be built systematically with four VCTs and a capacitor using gyrator-capacitor approach. These inductors are used to realize the counterpart of a passive LC filter. In the simulation, model parameter of a 1.5 μm CMOS technology (Mitel's ISO-HCMOS) has been used. The geometrical and electrical parameters of the VCT are shown in Table 4 (see page 63).

4.1 Resistance Realization

The proposed VCT can be used as a basic circuit to perform some other analogue functions. By connecting the circuit as shown in Fig.4.1, a grounded resistor is ready to be derived.



(a) Construct of a floating resistor



(b) A simple ac equivalent circuit of the synthesized grounded resistor

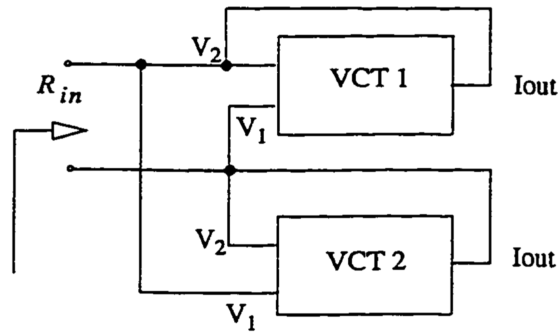
Fig. 4.1 A grounded resistor realization.

Again, if we assume low frequency applications and ignore channel length modulation effect, one can derive that

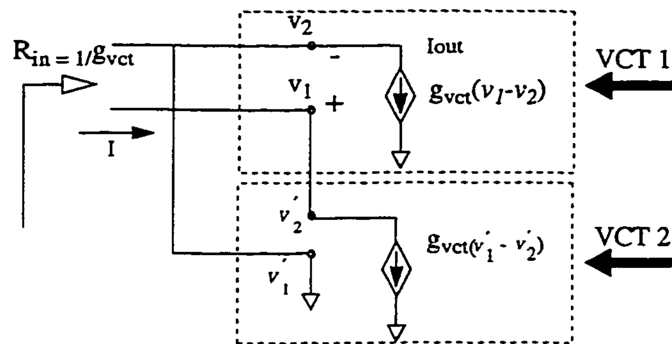
$$i_x / v = g_{VCT} \tag{4.1}$$

$$i_z / \hat{v} = -g_{VCT} \tag{4.2}$$

A floating components may be the ones that we meet in the daily design life.A floating resistor can be built B by having two VCTs connected as shown in the Fig.4.2.



(a) Realization of a floating resistor



(b) A simple ac equivalent circuit of the synthesized grounded resistor

Fig. 4.2 Realization of a floating resistor.

To simulate the performance of the VCT-based floating resistor implementation, a test bench can be constructed as shown in Fig.4.3. The simulation results are shown in Fig.4.4 and tabulated in Table 7 (see page 80).

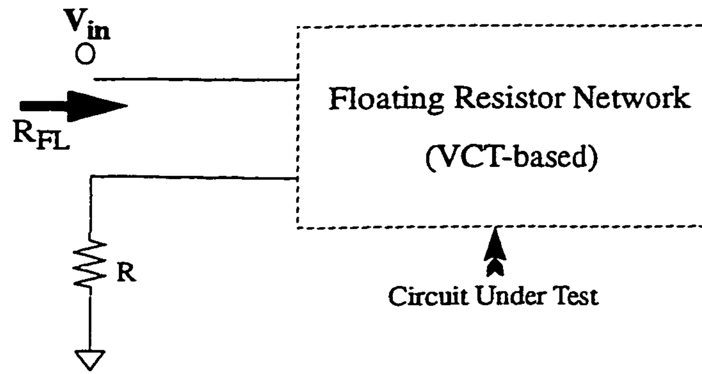


Fig. 4.3 Floating resistor implementation: test bench.

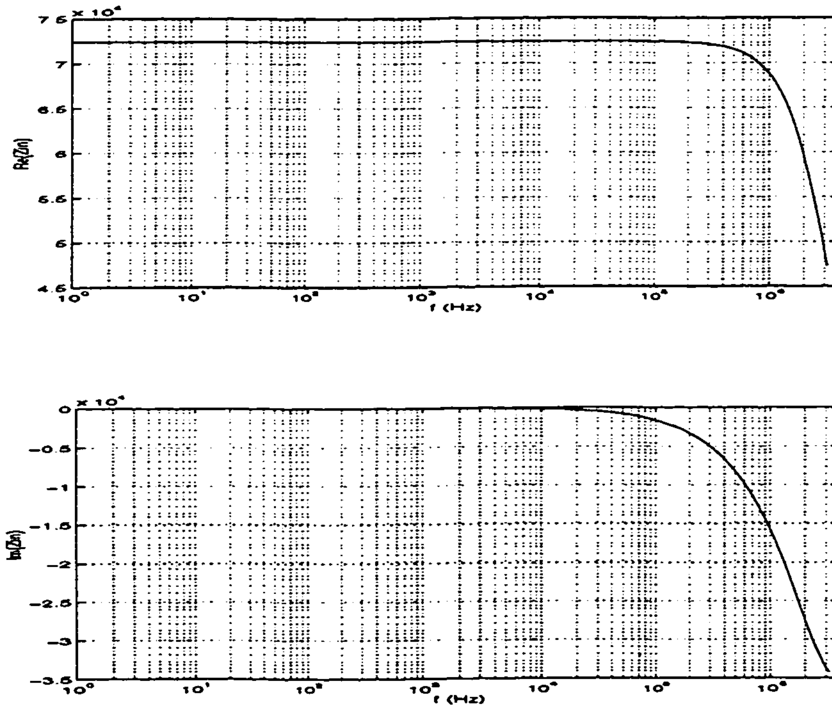


Fig. 4.4 Floating resistor implementation: simulation results.

Table 7 Floating Resistor Implementation: Simulation Results

Frequency (Hz)	Real Part of R_{FL} ($K\Omega$)	Imaginary Part of R_{FL} (Ω)	Expected Value of the Resistor ($K\Omega$)
1.0	72.42	-16.68m	71.90
10.0	72.42	-166.81m	
100.0	72.42	-1.69	
1.0K	72.42	-16.68	
10.0K	72.42	-166.81	
20.0K	72.42	-332.82	
35.5K	72.42	-591.82	
50.1K	72.41	-835.91	
79.4K	72.40	-1.32K	
100.0K	72.39	-1.67K	
199.5K	72.27	-3.32K	
316.2K	72.04	-5.25K	
501.2K	71.46	-8.25K	
707.9K	70.53	-11.50K	
1.0M	68.75	-15.83K	
2.0M	59.73	-27.40K	
3.16M	47.25	-34.28K	

HSPICE simulation results show that at low frequency, with the imaginary part of the impedance being very small compared to its real part, (i.e., negligible), the VCT-based floating resistor realization is a sound approximation to a passive resistor prototype with high accuracy. Since the VCT is electronically tunable, it is easy to tune the synthesized resistor into the desired value.

4.2 Using VCT's to Realize a Grounded Inductor

It is extremely difficult to integrate an inductor in VLSI if not impossible. Instead,

there are some ways that a synthesized inductor can be built by using the integrable components, like capacitors. Also a major problem encountered by filter designers is caused by the need for inductance at low frequencies. A concept that will enable the designer to dispense with inductors for certain applications by using what is referred to in the literature as the passive network simulation method. Central to the basis of the design is a device referred to as a gyrator whose principle of operation was outlined by Tellegan. Here we will look at an inductor realization by using several VCT's and capacitor(s).

An ideal gyrator may be represented by the parallel connection of two oppositely directed transconductance components, one with 180 degrees phase shift and the other with 0 phase shift. The ideal gyrator is a four-terminal (two-port) network which presents, at either port, an input impedance which is proportional to the admittance connected across the other port. Thus one can write

$$Z_{11} = r^2 Y_{22} \tag{4.3}$$

likewise

$$Y_{11} = g^2 Z_{22} \tag{4.4}$$

where g is defined as the gyration conductance:

$$g = \frac{1}{r} \tag{4.5}$$

Observation of eqs. (4.3) and (4.4) suggests that if the termination is a pure resistor then the input impedance is also a pure resistor. If the terminating component is a pure capacitor, however, then the input impedance is a pure inductor and vice versa. Therefore, it can be concluded that the device inverts the impedance connected to it.

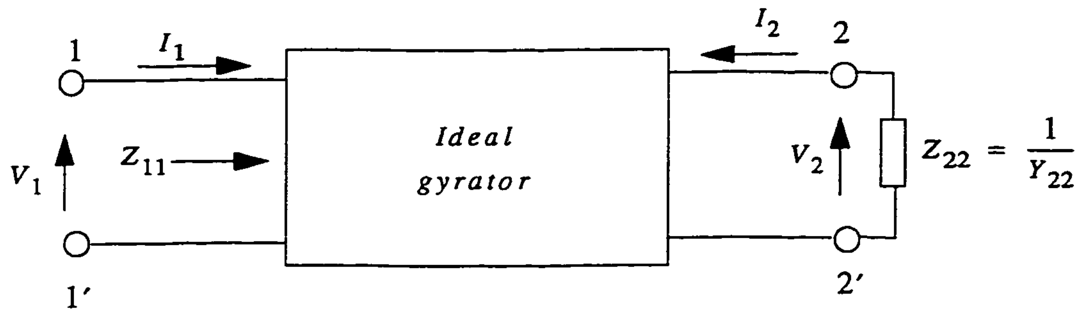


Fig. 4.5 Two-port network terminated in Z_{22}.

Consider that impedance Z_{22} is a pure capacitor $Z(j\omega) = 1/j\omega C$. Using equation (4.3) produces

$$Z_{11} = r^2 j\omega C = j\omega(r^2 C) \tag{4.6}$$

Therefore, a gyrator can be realized systematically by connecting two transconductance blocks of opposite polarities back-to-back in parallel (see Fig.4.6). With a capacitive load, this gyrator can implement a grounded inductor.

At low frequencies and with the channel length factor ignored, one has the approximate value

$$Z_{IN} = \frac{sC_L}{g^2_{VCT}} \tag{4.7}$$

which represents an ideal inductance of value

$$L = \frac{C_L}{g^2_{VCT}} \tag{4.8}$$

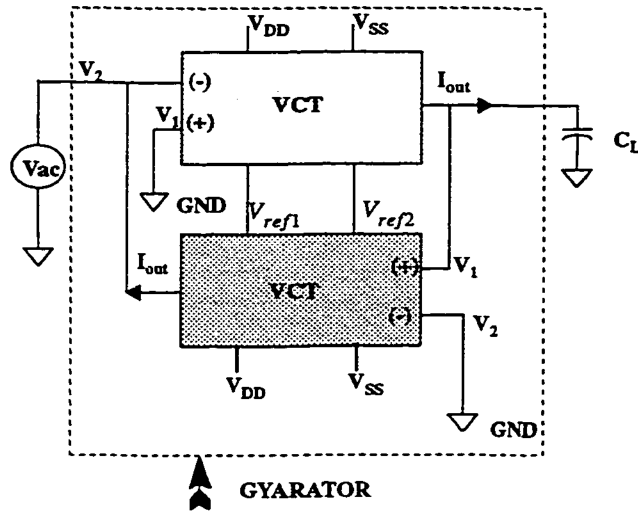


Fig. 4.6 Grounded inductor (gyrator) realization.

In practice, both real and imaginary parts of Z_{IN} are frequency-dependent. Using the configuration proposed in the Fig.4.6, we performed HSPICE simulation to justify the validity of a grounded inductor. The size of the transistors and the power sources are same as those given in Table 4 (see page 63). A load capacitance with the value of 10 pf has been employed. The simulation result is tabulated in Table 8 and also given in Fig.4.7 in a graphic representation.

The simulation results show that, at frequencies below 3 MHz, the driving point impedance can be expressed as $Z_{IN} = R + j\omega L$, where R and L are both exhibiting positive numbers.Therefore, the driving point impedance can be viewed as a series combination of an inductor and resistor. A quick look at Fig.4.7 (b) reveals that the imaginary part of the admittance is very linear to the frequency. The value of synthesized inductor is very close to that expressed by applying eqs. (4.7) and (4.8).

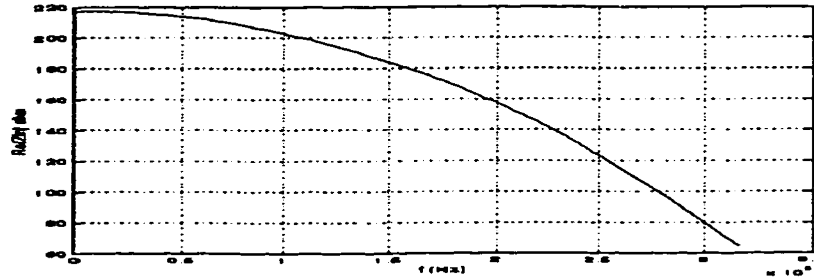
The frequency dependence of Z_{IN}, as mentioned above, is revealed in the simulation results (see Table 8 and Fig.4.7). At high frequency, Z_{IN} appears as a resistance in series with a capacitance, because of the negative imaginary part of the driving point impedance. This effect is not shown in the Table 8 and Fig.4.7.

Generally speaking, this gyrator-based grounded inductor can work as high as several hundred KHz with quite stable and predictable inductance value. The series connected resistor is in the range of several hundred ohms (can be reduced through a deliberate design and careful simulation).

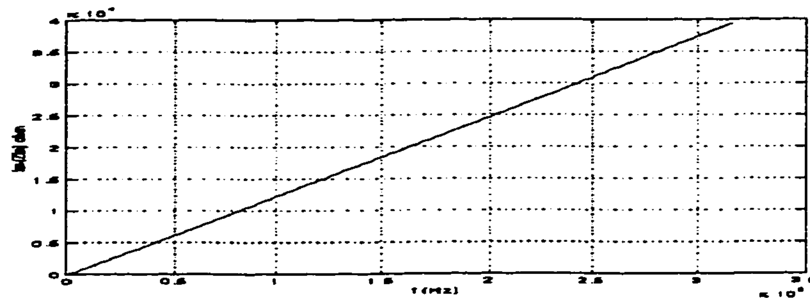
Note that two VCT's are used to build a gyrator, the power dissipation is slightly less than 80 uw, double that of just single VCT.

Table 8 Impedance of the Grounded Inductor.

Frequency (Hz)	Real Part (Ω)	Imaginary Part (Ω)	Simulated Value of Inductance (mH)	Expected Value of Inductance (mH)
1.0	217.3	121.994m	19.4	19.6
10.0	217.3	1.2199	19.4	
100.0	217.3	12.1994	19.4	
1000.0	217.3	121.99	19.4	
10.0K	217.2	1.2200K	19.4	
19.95K	216.7	2.4343K	19.4	
31.6K	215.8	3.8587K	19.4	
39.8K	215.0	4.8584K	19.4	
50.1K	213.6	6.1176K	19.4	
100.0K	202.6	12.2269K	19.5	
$Z_{in} = R + jX_L$				



(a) Real part of Z_{in}.



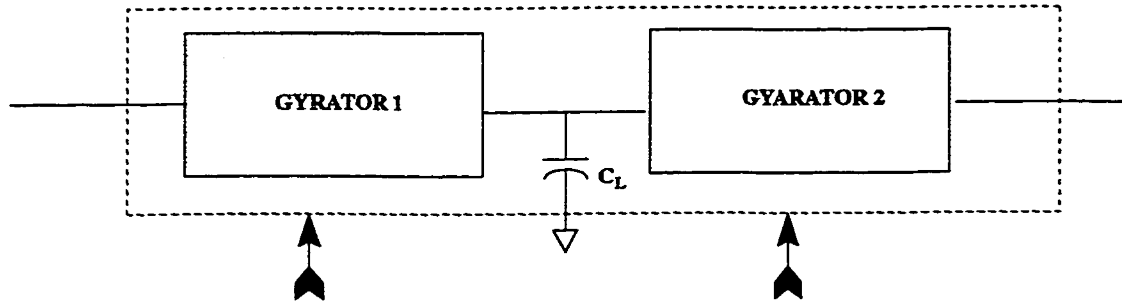
(b) Imaginary part of Z_{in}.

Fig. 4.7 Grounded inductor realization: simulation result.

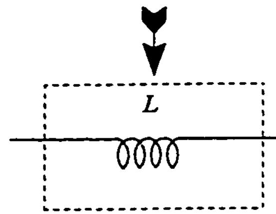
4.3 Floating Inductor Realization

In this part, we will use VCT-based inductors to build a voltage-mode LC filter. In actual signal processing, more often a floating inductor is needed. A floating inductor will be built in this section. Reference [13] shows the system configuration of a VCT-based floating inductor, and is redrawn in Fig.4.8(a). Fig.4.8 (b) gives the transformation of a floating inductor. Such transformation is based on the assumption that all the gyrators are ideal components. The inductance of the system is given by

$$L = \frac{C_L}{g_{VCT1} g_{VCT2}} \tag{4.9}$$



(a) Floating inductor realization.



(b) Transformation of (a).

Fig. 4.8 Floating inductor realization. $L = \frac{C_L}{g_{VCT1} g_{VCT2}}$.

4.4 Active Filter Implementation Using VCT's

Analog filters have always been among the key components of telecommunication, radar, biomedical instruments, and control systems. They often have very exacting specifications, and hence require complex structures, accurate (often tuned or trimmed) components, carefully arranged physical realization, as well as complicated design, testing and tuning procedures [23]. Active filters (especially those used at low frequencies) could reduce the size and weight by replacing inductors by active elements, usually operational amplifiers. Also, active filters could be fabricated using hybrid construction from thick-film resistors, chip capacitors and integrated operational amplifiers. The resulting circuit

may have required only a small fraction of the volume occupied by an equivalent reactance filter. However, analog integrated circuits, much more than digital ones, depend critically on the characteristics and imperfections of the fabrication process [23]. It is obvious that familiarity to the limitations of a fabrication process is necessary for a designer working on an active filter design.

One practical method to design active filters based on double-terminated LC ladder lossless prototype is the component simulation approach. This approach is based on simulating the ladder inductances and employs various devices such as gyrators [24], generalized-immittance converters (GIC's) and frequency-dependent negative resistances (FDNR's) [25]. Using such synthesized inductor, we can implement an LCR filter function in a straightforward fashion by just replacing the inductances by capacitance-loaded gyrators. In the following, a third-order low-pass filter is shown in Fig.4.9 and the synthesized network using the VCT approach is given as Fig.4.10. The floating inductance L is implemented using the structure shown in Fig.4.8.

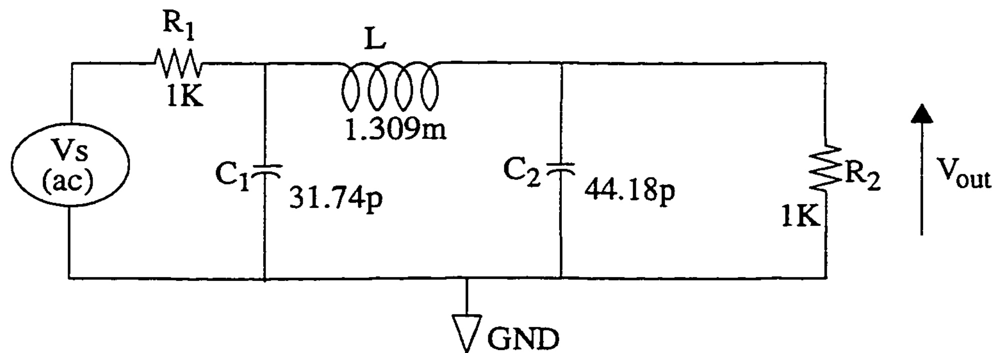


Fig. 4.9 A third-order low-pass filter.

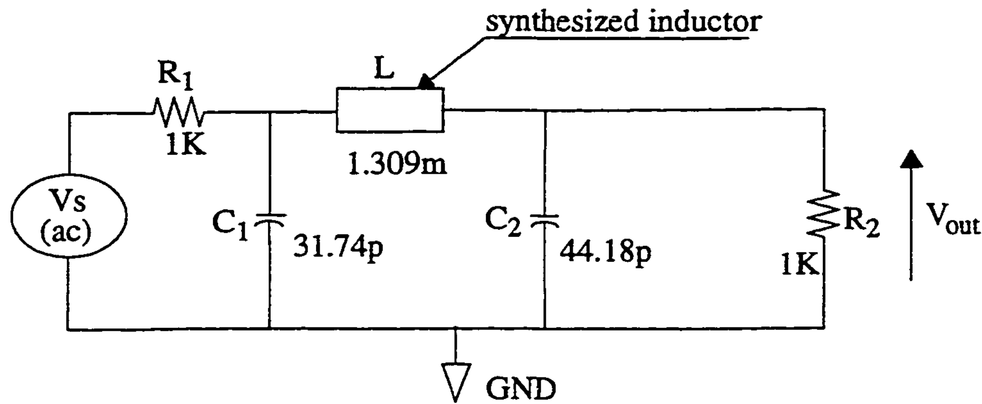


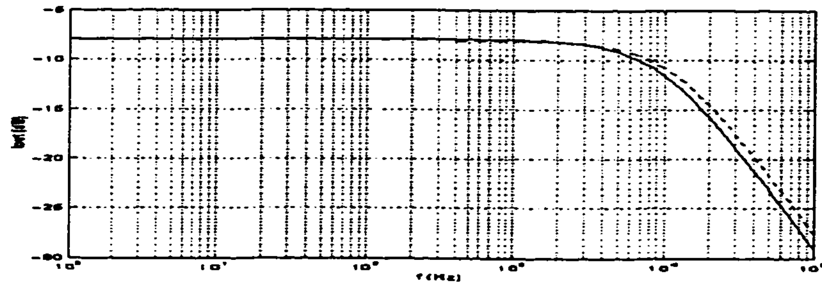
Fig. 4.10 A third-order filter realization using gyrator-based floating inductors.

The simulation results on both passive network and the synthesized network are shown in Fig.4.11 for the sake of comparison. The solid lines exhibit the frequency and phase responses of the filtering network using passive components, while the broken lines represent the frequency and phase responses of filtering network using VCT-based components and capacitors. The reference voltages here are 1.0 Volt and -1.3 Volt, respectively. The sizes of the transistors are exactly the same as those given in Table 4 (see page 63).

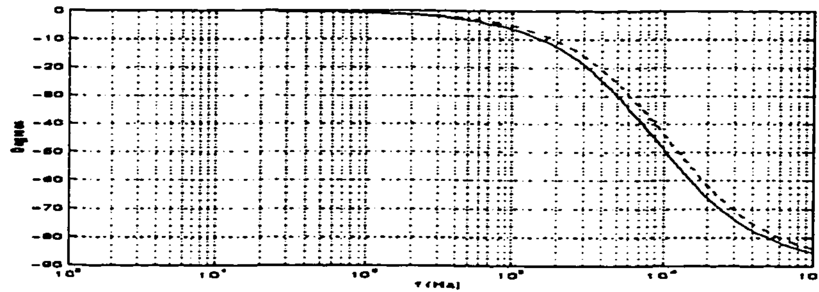
It has been shown above that synthesized inductors work quite good in the passband (around 10 KHz for 3dB bandwidth), but some deterioration in the transition and stop bands. This may attribute t o the nonideal characteristics of the gyrators. The major problem related to this scheme is the parasitic resistor associated with the inductor. The value is several hundred ohms or above. Some kind of compensation techniques, like an NII (Negative Impedance) suggested in [13], may be employed to improve the performance of the VCT-based gyrators if necessary.

It can be seen that the methodology shown here for the design of an inductorless fil-

ter is simple, and more important it is quite practical. The power dissipation for the synthesized network is just 182.7 uW (i.e., 60.9 $\mu W/pole$).



(a) Magnitude response



(b) Phase response

Fig. 4.11 Simulation result of a synthesized 3rd order filter.

Chapter 5

Layout Fabrication and Testing

Fabrication is an essential step in the design of an integrated circuit. Accordingly, a fabrication was made to test the performance of the proposed bulk-driven VCT circuit. DC and AC characteristics have been tested. A second order low pass filter has been realized, mainly based on the VCTs integrated in the chip.

5.1 Physical Layout of the Chip

The technology being used in the physical layout design is the ISO-HCMOS process of Mitel Semiconductor Co. (Bromont, Quebec, Canada) with the feature size 1.5 μm. Note that ISO-HCMOS process is a p-well process, and therefore, the VCT scheme used is the one shown in Fig.3.2. In terms of the physical layout design of the bulk-driven VCT circuit, no particular optimization techniques have been applied.

As a general rule, matched transistor networks are very often desired and used in analog design. However, it is not a general practice to fully characterize the matching characteristics of analog CMOS processes. To determine the appropriate transistor operating

point, its parasitics and its behavior for specific applications, analog simulation is still the best approach to verify heuristic designs [1]. This is also the case in our layout design. During the phase of various simulations, it has been found that this VCT has the ability to operate with the voltage sources as low as ±1 volt. We, therefore, used this ±1 volt as the voltage supplies as one of the design parameters. The dimensions of the transistors (see Fig.3.2), determined after several iterations of hand calculation, HSPICE simulation and parameter modification, are listed in the Table 9.

Table 9 Design parameters of the bulk-driven VCT.

CMOS technology being used	Mitel's ISO-HCMOS process (P-well, 1.5μm)	
Transistor size (μm)	M1/M2	200/3
	M3/M4	550/3
	M5/M6	30/3
Voltage supplies (V)	±1	
Reference Voltages (V)	Vref1	1
	Vref2	-1

A single bulk-driven VCT mask layout is shown in Fig.5.1. The area for the single cell is roughly 830 μm * 64.8 μm, that is 0.0538 mm^2. The whole die area is 3000 μm * 3000 μm with the pad frame included and 2460 μm * 2460 μm with the pad frame absent. The total pin number is 40 with a DIP (Dual In-line Package) packaging. Mainly owing to the finite pin counts, we only integrated 4 VCTs and 3 gyrators (two VCTs connected together in the way shown in Fig.4.6) into one chip. The layout view of the chip is shown in Fig.5.2. The pin enumeration mapping is shown in Appendix A. A view with pins labelled as in the enclosed diagram (drawn by CMC, Canadian Microelectronic Corporation) is exhibited in Appendix A as well.

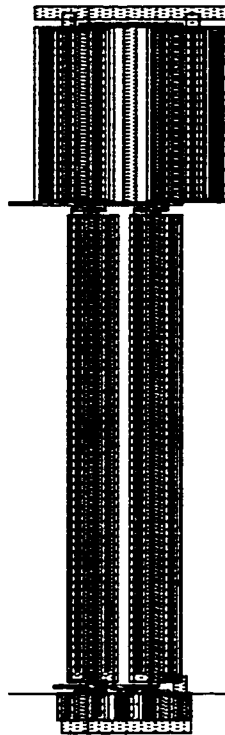


Fig. 5.1 Physical layout of the proposed bulk-driven VCT.

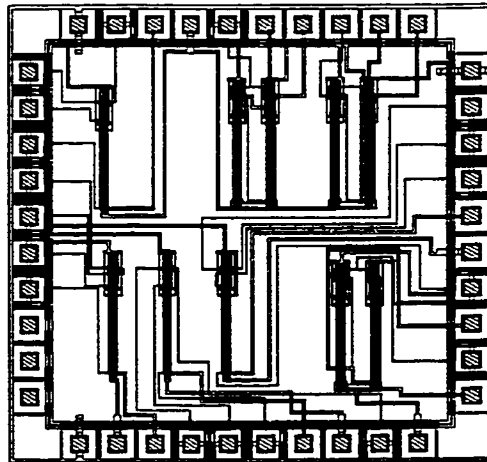


Fig. 5.2 Physical layout of the fabricated chip.

5.2 DC Characteristics

The test bench we used to test the DC characteristics is given in Fig.5.3, which is similar to the one shown in Fig.3.12 (a). The probe is a voltage meter to detect the output voltage. Through measuring the voltage, we may easily derive the output current accordingly.

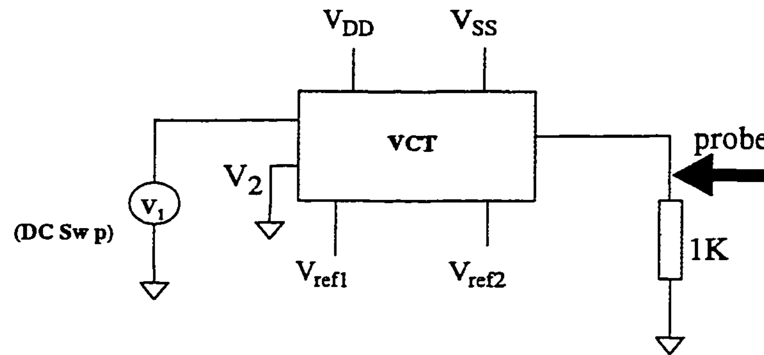


Fig. 5.3 The DC characteristic of the fabricated VCT.

The parameters employed are given in Table 9 (see page 91). HSPICE simulation result on this design is given in Fig.5.4. The test curve showing the relationship of the output current (of the VCT) vs. the input voltage is given in the Fig.5.3. The reason that we gave these two curses separately lies in the fact that there is an DC offset for our testing curve. To put these two curves together into one figure will make it very inconvenient to read.

Based on the test results, we can see that the linearity of the transconductance is quite good. Due to the variable electrical parameters, the transconductance is higher than the simulation values. The lesson we learned from the results is that the model we used in our

simulation is not accurate enough to determine the actual values of the transconductance. However, since we have two reference voltage inputs available, we may use these two terminals as the tuning terminals.

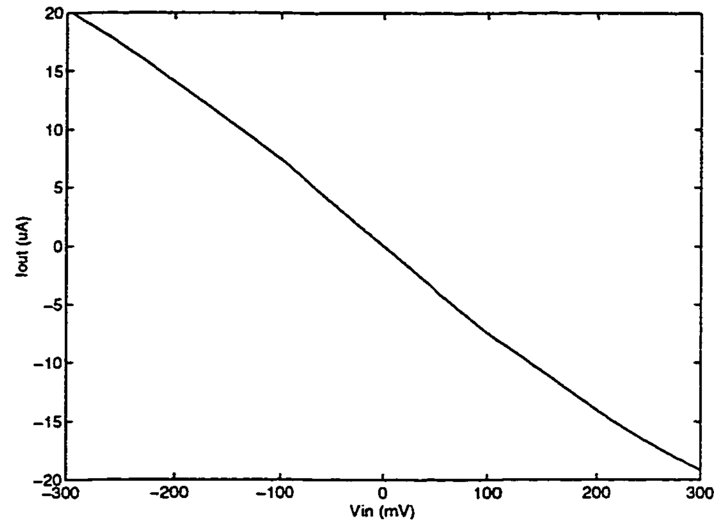


Fig. 5.4 HSPICE simulation result of the designed VCT.

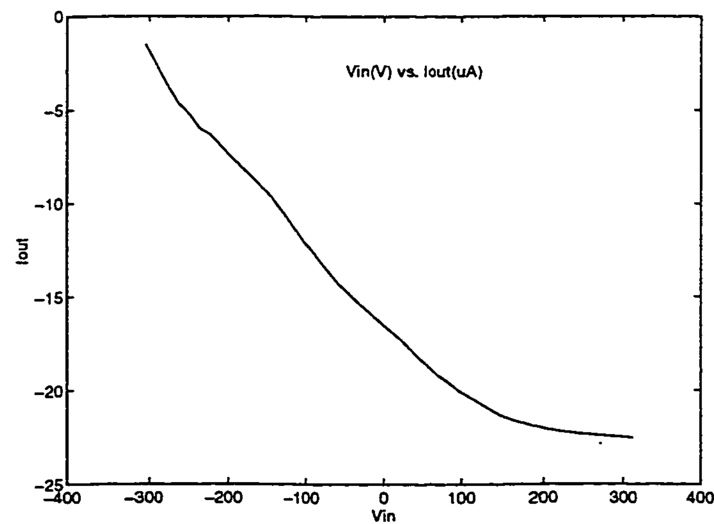


Fig. 5.5 The DC characteristic of the fabricated VCT.

Obviously, the characteristics reveal small variations from sample to sample as a result of statistical tolerance which exists in an integrated circuit process technology. The results are shown in Fig.5.6. From the figure, the linear relationship between the input voltage and the output current is observable, particularly when the input signal is in the range of -100 mV to 100 mV. A small DC offset was observed in all three cases. However, such offset is pretty stable in three cases.

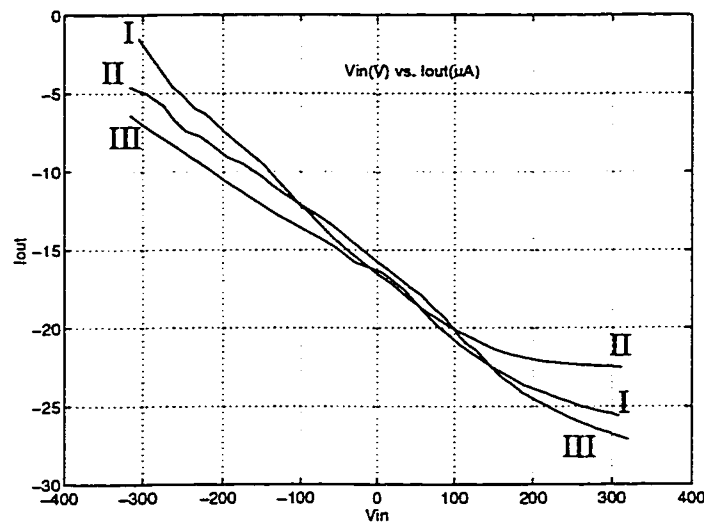


Fig. 5.6 DC characteristics of fabricated VCTs.

5.3 AC Characteristics

The test bench we used to test the AC characteristics is shown in Fig.3.13, which is similar to the one shown in Fig.3.13. Again, we measure the output voltage and converts to the voltage signal to its corresponding current representations.

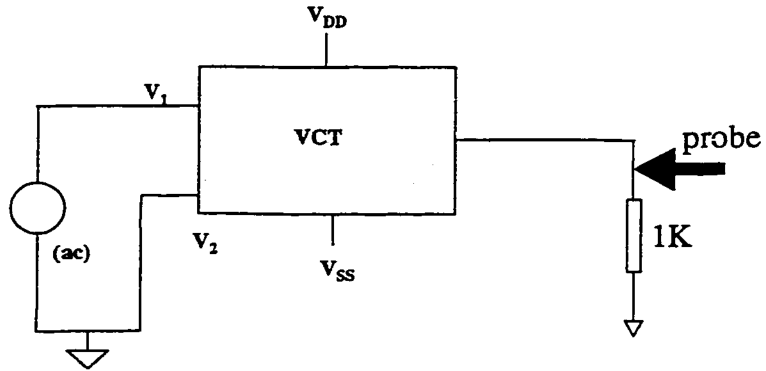
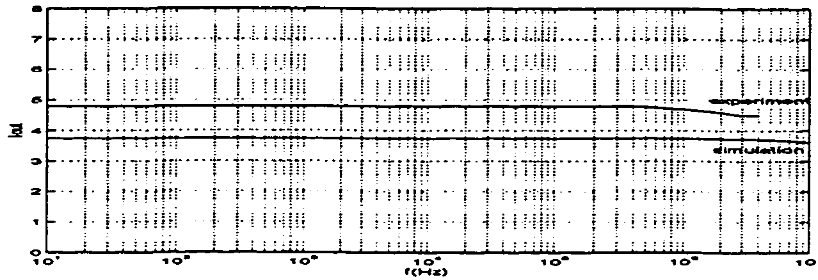
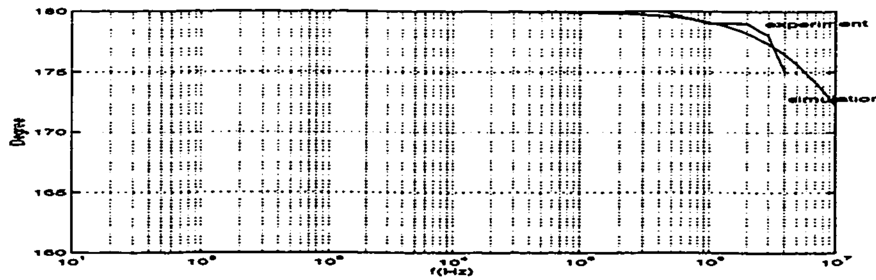


Fig. 5.7 AC analysis of the proposed VCT: Test Bench.



(a) Magnitude response



(b) Phase response

Fig. 5.8 Testing results on the fabricated chip: AC characteristics.

The parameters employed are given in Table 9 (see page 91). Fig.5.8 shows the AC

characteristics by HSPICE simulation and the test results. It has been shown in the simulation curve that the phase shift is less than 1 degree when the system is operating in the frequency range up to 1 MHz. Again, quite good agreements between the simulation and test results can be viewed from the figure. We tested the circuit using sine signal with frequency from almost DC up to 4 MHz. Here 3 chips were tested as well. All the three chips showed very alike AC response. Therefore, the characteristics of just one single chip is given in the figure.

5.4 Low-Pass Filter

As shown in the previous chapter, VCTs can be used to realize many electrical components, such as a floating inductor. Floating inductor can be used in a filter scheme to replace a passive inductor. Also in previous chapter, simulation results on a third order low-pass filter using VCT-based inductor were presented. In this section, we shall present test results on a second order low pass filter using the fabricated chip. The scheme of the filter is given as Fig.5.9.

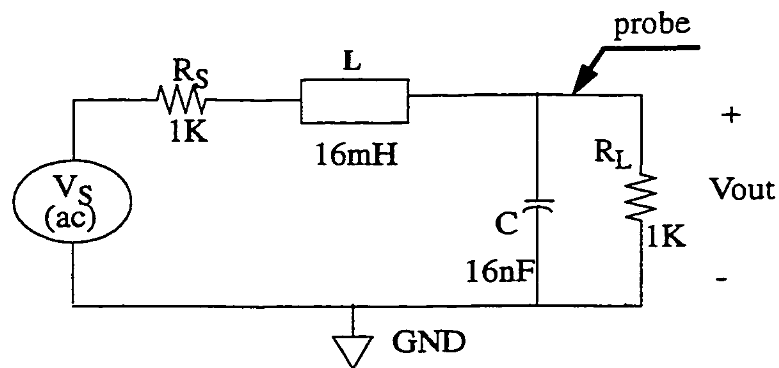


Fig. 5.9 A second order low pass filter.

Elementary analysis yields the expression:

$$\frac{V_o(s)}{V_i(s)} = \frac{\frac{1}{LC}}{s^2 + s\left(\frac{L + CR_LR_S}{LCR_L}\right) + \frac{R_L + R_S}{LCR_L}} \tag{5.1}$$

The 3dB frequency is given by

$$\omega_{3dB} = 2\pi f_{3dB} = \omega_0\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}} \tag{5.2}$$

where ω_0 is the undamped natural frequency and Q is the quality factor; they are governed by

$$\omega_0 = \sqrt{\frac{R_L + R_S}{LCR_L}} \tag{5.3}$$

and

$$Q = \frac{\sqrt{(R_L + R_S)\,LCR_L}}{L + CR_LR_S} \tag{5.4}$$

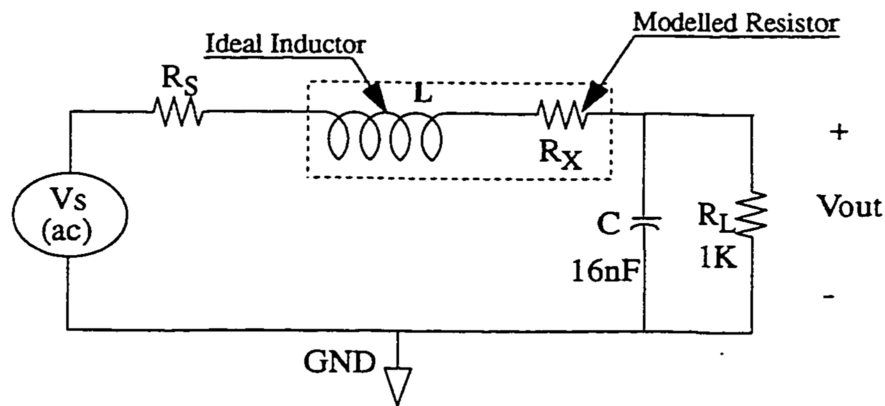


Fig. 5.10 Model of the synthesized low pass filter.

Simulation results have shown the existence of parasitic resistance in series with the inductance. Thus the synthesized inductor can be modelled as an ideal inductor with a series connected resistor (see Fig.5.10).

Now the transfer function will be slightly different from what is given in eq. (5.1), rather it is like

$$\frac{V_o(s)}{V_i(s)} = \frac{\frac{1}{LC}}{s^2 + s\left(\frac{L + CR_L R'_S}{LCR_L}\right) + \frac{R_L + R'_S}{LCR_L}} \tag{5.5}$$

where $R'_S = R_X + R_S$.

The 3-dB frequency representation is very similar to the one given in equations (5.2), (5.3), and (5.4) with R_S replaced by R'_S.

Above equations (equations (5.2) through (5.5)) clearly indicate that if the values of capacitor and resistors are kept unchanged, the impact of R_X will cause the frequency response of the synthesized network somehow different from that of the passive prototype. Even the undamped frequency will be slightly higher than that of the prototype network. This is verified in Table 10, where different values of R_X are used to perform the HSPICE simulation on a passive prototype network (see Fig.5.10). The passive network has a 3dB frequency of 14.1 KHz. If the R_X is considered (modeled as a resistor varying from 10 ohms to 280 ohms, which is close to the case happened in the IC realization of the network, some magnitude degradation happens at the pass band.

Table 10 The Impact of R_X to the Magnitude/Phase Responses

Frequency (Hz)	R_X 0	Magnitude[a]	Phase (degree)[b]	3-dB Frequency (KHz)
10	280	0.88	4.41×10^{-3}	15
1K		0.88	0.47	
14.1K		0.93	11.79	
100 K		0.83	2.52	
10	80	0.96	4.4×10^{-3}	14.4
1K		0.96	0.39×10^{-3}	
14.1K		1.04	8.84	
100 K		1.21	1.16	
10	10	1.00	5.0×10^{-3}	14.2
1K		1.00	0.50	
14.1K		1.09	7.45	
100 K		1.21	0.61	

a. We take the values of passive prototype ($R_X = 0$) at each particular frequency as one, and normalize the output magnitude of the simulated filter accordingly.

b. The data entries are the phase difference between the prototype without R_X and the filter network with R_X modeled as given at given frequency.

Following the analysis given as above, we conducted experiments on the fabricated chip to build the filter shown in Fig.5.9 (f_p = 14.1KHz and Q_p = 0.71). The inductance has a value of 16 mH. This floating inductance has been realized using two gyrators built from the bulk-driven VCTs (see Fig.4.8). The magnitude response of the filter realized using the VCT-based inductance and the ideal expected response (i.e., of the prototype filter) are shown in Fig.5.11. The solid lines show the magnitude response in (a), and the phase response in (b) of the passive filter network. The dash-dot lines show the test results of a synthesized network, where the inductor is replaced by a synthesized inductor and all the rest components are left untouched. The agreements are very good. Power supply values of ±1 volt have been used for the simulation and the lab bench test. The power consumption for the second order filter is 192.6 μW, i.e., 96.3 μW per pole (simulation results[15]).

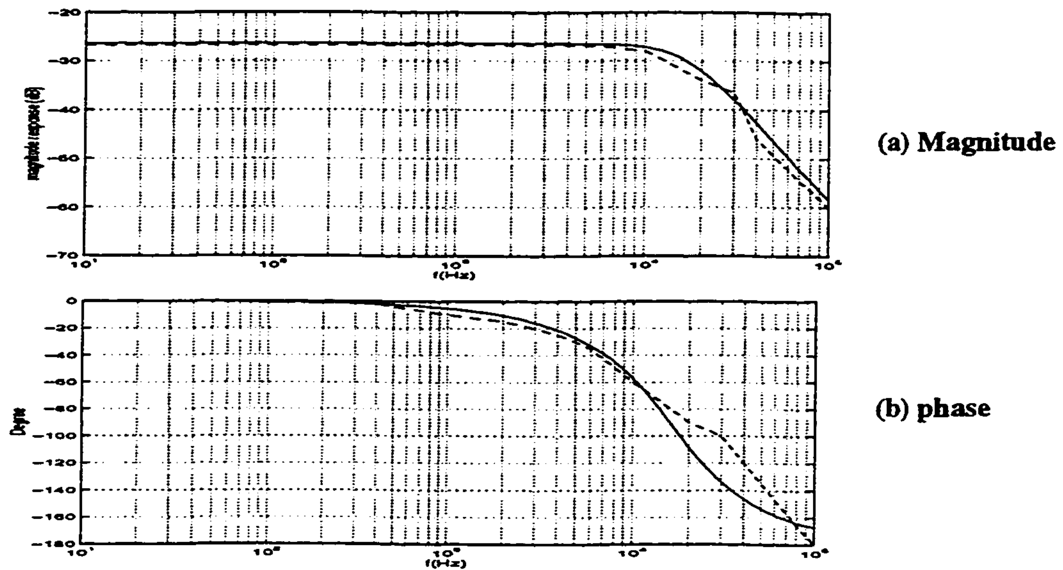


Fig. 5.11 Simulation and test results of a second order filter using synthesized inductor.

In the design of such filter using the inductor-capacitor synthesis approach, it is essential to take the R_X into consideration and try to minimize it. The model that we present here, modelling the synthesized inductor connected with a series resistor, is accurate enough to evaluate the behaviors of the active component.

No capacitors and resistors were incorporated into the chip[16], and all of these passive components were connected externally. We just simply connected the reference voltages to their corresponding voltage sources in the layout design. However, if such reference voltage terminals can be controlled electrically, we may further tune the value of the induc-

15. It is very difficult to measure the power dissipation for the fabricated chip, due to the way the chip has been fabricated: more than one VCT operates when the circuit is powered.

16. Actually, it is impossible to integrate the capacitors we used in the filter scheme since they are too large to be integrated.

tance so that we may land on a more desirable filtering response. We emphasize this point again since such flexibility is there and we should be able to take advantage of it if it is desired.

Chapter 6

Conclusions and Suggestions for Further Research

The evolution of digital processes and techniques will shift the boundary between digital and analog circuits. However, analog circuits will remain irreplaceable components of systems-on-a-chip[18]. Besides the A/D conversion, there still exists quite a number of demands to implement signal processing functions in an analog manner. Techniques that can provide non-degraded performance at low power supply voltages and consuming less power are demanded and will continue to evolute.

6.1 Concluding Remarks

Here a bulk-driven VCT has been proposed. Basic operating conditions are examined. The VCT has been used to constitute several important analog building blocks, like gyrators and inductors. HSPICE simulation further determines its usefulness in building a larger system, such as a monolithic filter using either inductor-capacitor network or $g_m - C$ network. Several VCTs have been fabricated in a chip using Mitel's ISO-HCMOS technology (Mitel, 1.5 μm, p-well). Test results have verified many aspects of the theoretically

expected characteristics of the proposed VCT. This circuit has the potential to be applied in low power systems. The power consumption of the proposed bulk-driven VCT is one magnitude of order less that of a conventional gate-driven VCT, shown in Table 6 (see page 72).

This circuit shows quite good CMRR. In addition, PSRR is good for one voltage source and a little poorer for the other.

As it is known, current-mode signal processing units are troubled by higher noise level. VCT as the first stage for the transformation unit from the physical voltage signal to the current signal used by the next current-mode signal stages, some design guidelines to design low noise bulk-driven circuit must be followed. That is, not only the transistor size ratios are essential, but the layout plays a very important role as well.

The proposed bulk-driven VCT is electronically tunable. Since there are two voltage references in this circuit, it is possible to use these reference voltages as the tuning parameters. In order to reduce the burden of the tuning circuit, we may connect one of the voltage references to a fixed voltage reference circuit and only adjust the value of another voltage reference. This strategy is essential to tune a larger network (e.g., a high order filter). Obviously, if it is allowed, we may have both voltage references controllable by the tuning circuits. Thus, the circuit will be tuned in the way that we may adjust the voltage reference networks jointly. Such freedom comes with the cost of area and power overhead, obviously.

Once again, we have to stress that bulk-driven techniques will not replace the dominant gate-driven circuits; at least at this moment and foreseeable future. Rather we view the bulk-driven techniques as the complementary to the present gate-driven ones. This VCT is mainly restricted to low frequency applications and has relative low transconductance value.

Nevertheless, this bulk-driven VCT, with its ability of being applied to the low power design in a modest frequency range and large DC operating range, is likely to be used to a biomedical instrumentation or audio equipment demanding sound low frequency response and efficient power use.

6.2 Scope for Future Research

VCT architectures have been under intensive research for almost two decades (accompanied with the popularity of the CMOS and current mode signal processing). With more and more stringent power dissipation requirement and further reduction in voltage supply values, one day we may have to fully land ourselves onto current mode signal processing if there is no major breakthrough in the semiconductor material/process level. A VCT will show its increasing importance, thereby. Obviously, the VCTs are also subject to the problems arising from the low power and low voltage trend.

As we know, bulk-driven techniques have attracted some attention in the past few years. Some promising circuit architectures have been proposed. Design models have been suggested as well. However, the research is still far from a concluding phase. We, therefore, believe that the model proposed in chapters 2 and 3 may be a little oversimplified from the actual situations, particularly if we use the forward-biased bulk-source diode to modulate the input signal. To fully understand the bulk driven techniques and use these techniques more efficiently, a more comprehensive and concrete model will be very helpful.

Secondly, we believe that the low power low voltage trend in the signal processing field also poses a question in terms of circuit tuning. In this thesis, we proposed a tuning guideline for the proposed circuit. As a matter of fact, to implement an auto tuning circuit

to tune the VCT proposed here requires extra effort to minimize the power and area penalties on those tuning circuits, even again not mentioning that those tuning circuits themselves are subject to the reduced voltage supplies.

Testing is an essential part in terms of a functionally and electrically successful silicon fabrication. Design for testability (DFT) may be applied to the circuit proposed here. It should be noticed that testing a circuit, like a VCT, is not a trivia work, where two different electrical parameters involved in a VCT-related circuit, namely, the current and the voltage. One testing scheme is suggested in Fig.6.1. Since most of the time, more likely there exist more than one current mode signal processing units functioning in one single chip, we would then use a multiplexer to select the specific circuit under test (CUT) at a time. This will lead to a reduction of the pin count at a cost of longer testing time. If the circuit employs some feedback(s) to the input terminal of the VCT, the feedback branch(es) should be capable of being selected/deselected. The load illustrated in the figure can be either a resistor, or a capacitor, or just a floating node (viewed as a resistor with infinite resistance). Input signal should be a slow ramp (i.e., viewed as a DC swing). Another input testing signal may be a sine wave signal, generated by either a digital way (probably for a mixed mode chip) or a system crystal or directly input from the external. Test Circuit unit may comprise of several current amplification/attenuation mechanism to bring the input current to the desired range for the sake of comparison. Also inside the testing circuit, some transimpedance component such that the input current will be transformed to a voltage signal may be incorporated. If that is the case, the *Reference Current* shown in the Fig.6.1 will be changed to *Reference Voltage* accordingly. Boundary scan technique (using *IEEE std. 1149.1*) is possible to be adopted in the testing scheme. It will be very interesting to explore some methods to perform on-line testing in a current-mode signal processing unit.

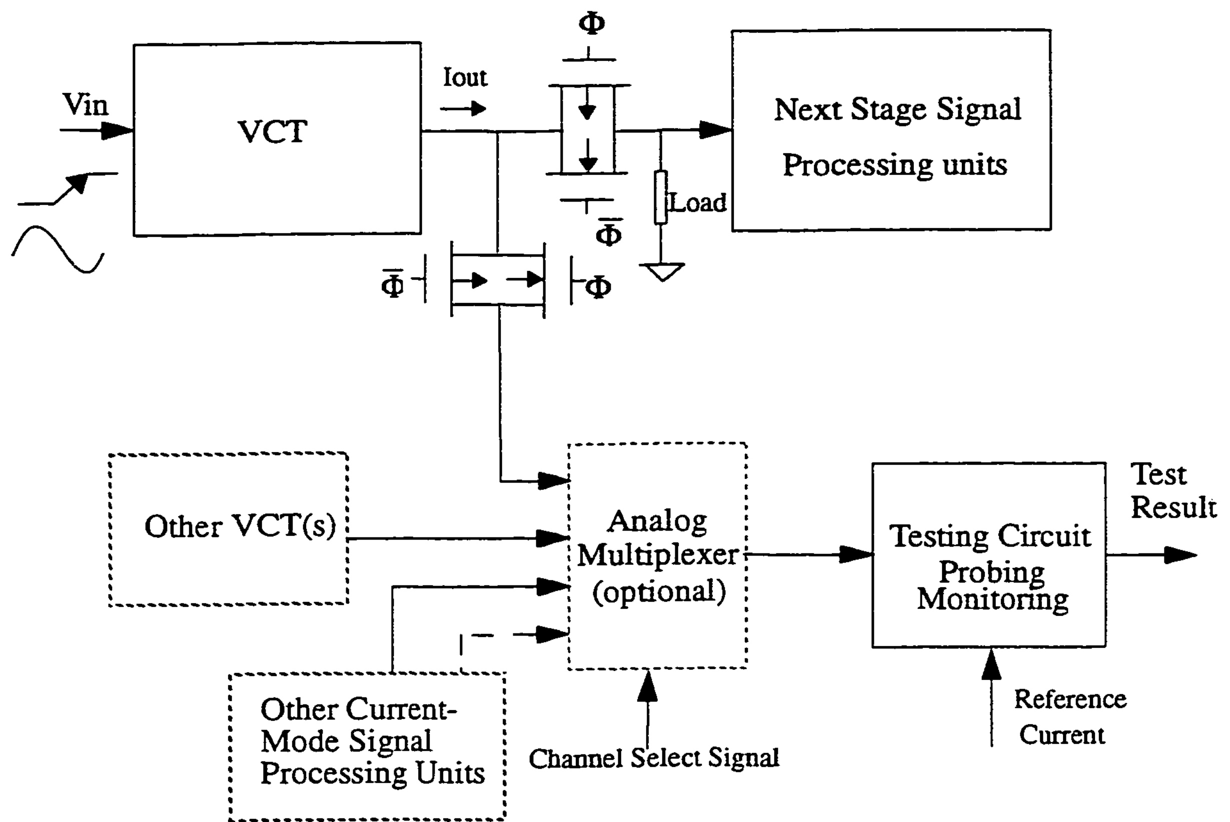


Fig. 6.1 General testing scheme of the circuit.

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Appendix A

Pin Enumeration of the Fabricated Chip

Table 11 Pin Enumeration of the Fabricated Chip

Component Name	Node Name	Pin Number	Component Name	Node Name	Pin Number
VCT1	V1	16	VCT2	V1	19
	V2	14		V2	20
	Vref1	18		Vref1	21
	Vref2	17		Vref2	22
	Iout	13		Iout	28
VCT3	V1	29	VCT4	V1	4
	V2	34		V2	3
	Vref1	30		Vref1	2
	Vref2	31		Vref2	39
	Iout	32		Iout	38
Gyrator1	Gnd	11	Gyrator2	Gnd	8
	In	10		In	7
	Cout	9		Cout	6

Component Name	Node Name	Pin Number	Component Name	Node Name	Pin Number
Gyrator1	Gnd	36	Sources	Vdd	5, 15, 26
	In	37		Vss	27, 33, 35, 40
	Cout	38			

Diagram of bonding of the Fabricated Chip from CMC.

Appendix B

Collections of Simulation Files

B.1 DC Analysis (see Fig.3.12)

```
*********************************************
*
* -- This is a SPICE Netlist for a bulk-driven VCT
*
* -- DC Characteristics
*
* Yingtao Jiang
*
* June 1, 1997
*
*********************************************


.SUBCKT VCT1 VDD VSS VREF1 VREF2 V1 V2 IOUT

MQ1 VREF2 VREF2 V3 V1 mitelpmos L = 3u W = 150u AD = 1p AS = 1p NRD = 1 NRS = 1
MQ2 VREF2 VREF2 V4 V2 mitelpmos L = 3u W = 150u AD = 1p AS = 1p NRD = 1 NRS = 1

MQ3 VY VREF1 V3 VSS mitelnmos L = 3u W = 10u AD = 1p AS = 1p NRD = 1 NRS = 1
MQ4 IOUT VREF1 V4 VSS mitelnmos L = 3u W = 10u AD = 1p AS = 1p NRD = 1 NRS = 1

MQ5 VY VY VDD VDD mitelpmos L = 5u W = 6u AD = 1p AS = 1p NRD = 1 NRS = 1
MQ6 IOUT VY VDD VDD mitelpmos L = 5u W = 6u AD = 1p AS = 1p NRD = 1 NRS = 1

.ENDS VCT1


XVCT1 VDD VSS VREF1 VREF2 V1 V2 IOUT VCT1
```

```
VPOS VDD 0 DC
VNEG VSS 0 -1.5

VR1 VREF1 0 0.80V
VR2 VREF2 0 -1.5V

VINPUT1 V1 0 0.1
EV V2 0 V1 0 -1

ROUT IOUT 0 1

.LIB '$HOME/sim/model_file' nominal

.TEMP 25

.OP

.DC VINPUT1 -1V 1V 0.01V

.OPTION POST


.END
```

B.2 AC Analysis (see Fig.3.14)

```
*********************************************
*
* -- This is a SPICE Netlist for a bulk-driven VCT
*
* -- AC Characteristics
*
* Yingtao Jiang
*
* June 1, 1997
*
*********************************************


.SUBCKT VCT1 VDD VSS VREF1 VREF2 V1 V2 IOUT

MQ1 VREF2 VREF2 V3 V1 mitelpmos L = 3u W = 150u AD = 1p AS = 1p NRD = 1 NRS = 1
MQ2 VREF2 VREF2 V4 V2 mitelpmos L = 3u W = 150u AD = 1p AS = 1p NRD = 1 NRS = 1

MQ3 VY VREF1 V3 VSS mitelnmos L = 3u W = 10u AD = 1p AS = 1p NRD = 1 NRS = 1
MQ4 IOUT VREF1 V4 VSS mitelnmos L = 3u W = 10u AD = 1p AS = 1p NRD = 1 NRS = 1

MQ5 VY VY VDD VDD mitelpmos L = 5u W = 6u AD = 1p AS = 1p NRD = 1 NRS = 1
```

```
MQ6 IOUT VY VDD VDD mitelpmos L = 5u W = 6u AD = 1p AS = 1p NRD = 1 NRS = 1

.ENDS VCT1


XVCT1 VDD VSS VREF1 VREF2 V1 V2 IOUT VCT1


VPOS VDD 0 1.5
VNEG VSS 0 -1.5

VR1 VREF1 0 0.80V
VR2 VREF2 0 -1.5V

VINPUT1 V1 0 AC
EV V2 0 V1 0 -1

ROUT IOUT 0 1

.LIB '$HOME/sim/model_file' nominal

.TEMP 25

.OP

.AC DEC 20 1 100Meg

.OPTION POST


.END
```

B.3 Monte Carlo Analysis -- DC Sweep (see Fig.3.15)

```
**********************************************
*
* -- This is a SPICE Netlist for a bulk-driven VCT
*
* -- Monte Carlo Analysis (Statistical)
*
* -- DC Sweep
*
* Yingtao Jiang
*
* June 1, 1997
*
**********************************************

.DC VINPUT1 -1 1 0.01 SWEEP Monte = 30

.PARAM L1 = 3u
```

```
.PARAM LEFF1 = GAUSS(L1, .05, 3)

.PARAM L2 = 5u
.PARAM LEFF2 = GAUSS(L2, .05, 3)

.PARAM Vthn = GAUSS( 0.8404, .05, 3)
.PARAM Vthp = GAUSS(-0.7281, .05, 3)

.PARAM Lith = GAUSS(-1.269e-07, .05, 3)


.SUBCKT VCT1 VDD VSS VREF1 VREF2 V1 V2 IOUT

MQ1 VREF2 VREF2 V3 V1 mitelpmos L = 3u W = 150u AD = 1p AS = 1p NRD = 1 NRS = 1
MQ2 VREF2 VREF2 V4 V2 mitelpmos L = 3u W = 150u AD = 1p AS = 1p NRD = 1 NRS = 1

MQ3 VY VREF1 V3 VSS mitelnmos L = 3u W = 10u AD = 1p AS = 1p NRD = 1 NRS = 1
MQ4 IOUT VREF1 V4 VSS mitelnmos L = 3u W = 10u AD = 1p AS = 1p NRD = 1 NRS = 1

MQ5 VY VY VDD VDD mitelpmos L = 5u W = 6u AD = 1p AS = 1p NRD = 1 NRS = 1
MQ6 IOUT VY VDD VDD mitelpmos L = 5u W = 6u AD = 1p AS = 1p NRD = 1 NRS = 1

.ENDS VCT1


XVCT1 VDD VSS VREF1 VREF2 Vin V2 IOUT VCT1

VPOS VDD 0 1.5
VNEG VSS 0 -1.5

VR1 VREF1 0 0.80V
VR2 VREF2 0 -1.5V

VINPUT1 Vin 0 AC
VV V2 0 0

ROUT IOUT 0 1


.TEMP 25
.OP

.OPTION LIST POST = 2
.PRINT DC Ioutdiff = par(" 2*I(ROUT)")
+ GM = par("I(ROUT) / (V(V1) - V(V2))")
+ va = par("v(xvct1.v3) / v(v1)")


.model mnmos nmos
+ level = 3.0
+ ld = 1.941e-07
+ dw = -1.279e-07
+ xl = Lith
+ vto = Vthn
+ tpg = 1.0
+ nsub = 1.345e+16
+ cgdo = 2.716e-10
+ cgso = 2.716e-10
+ capop = 4.0
+ tox = 2.671e-08
+ acm = 0.0
+ js = 2.50e-03
+ cj = 3.161e-04
```

```
+ cjsw = 2.145e-10
+ mj = 0.3570
+ mjsw = 0.2847
+ pb = 0.7191
+ rsh = 202.6
+ gap1 = 4.73e-04
+ gap2 = 6.36e+02
+ delta = 1.721
+ eta = 2.223e-02
+ kappa = 0.2620
+ nfs = 5.161e+11
+ theta = 4.090e-02
+ vmax = 2.383e+05
+ xj = 2.197e-07
+ uo = 527.2
+ tref = 25.0
.model mpmos pmos
+ level = 3.0
+ ld = 1.735e-07
+ dw = -2.179e-07
+ xl = Lith
+ vto = Vthp
+ tpg = -1.0
+ nsub = 3.947e+16
+ cgdo = 2.534e-10
+ cgso = 2.534e-10
+ capop = 4.0
+ tox = 2.672e-08
+ acm = 0.0
+ js = 2.50e-03
+ cj = 2.898e-04
+ cjsw = 2.052e-10
+ mj = 0.3566
+ mjsw = 0.2450
+ pb = 0.2259
+ rsh = 393.4
+ gap1 = 4.73e-04
+ gap2 = 6.36e+02
+ delta = 1.829
+ eta = 1.522e-02
+ kappa = 9.994
+ nfs = 9.275e+10
+ theta = 0.1049
+ vmax = 2.795e+05
+ xj = 1.762e-07
+ uo = 193.7
+ tref = 25.0

.END
```

B.4 Monte Carlo Analysis -- AC Sweep (see Fig.3.16)

```
*********************************************
*
* -- This is a SPICE Netlist for a bulk-driven VCT
*
* -- Monte Carlo Analysis (Statistical)
```

```
*
* -- AC Sweep
*
* Yingtao Jiang
*
* June 1, 1997
*
**********************************************

.ac dec 20 1 100meg sweep monte = 30


.PARAM L1 = 3u
.PARAM LEFF1 = GAUSS(L1, .05, 3)

.PARAM L2 = 5u
.PARAM LEFF2 = GAUSS(L2, .05, 3)

.PARAM Vthn = GAUSS( 0.8404, .05, 3)
.PARAM Vthp = GAUSS(-0.7281, .05, 3)

.PARAM Lith = GAUSS(-1.269e-07, .05, 3)


.SUBCKT VCT1 VDD VSS VREF1 VREF2 V1 V2 IOUT

MQ1 VREF2 VREF2 V3 V1 mitelpmos L = 3u W = 150u AD = 1p AS = 1p NRD = 1 NRS = 1
MQ2 VREF2 VREF2 V4 V2 mitelpmos L = 3u W = 150u AD = 1p AS = 1p NRD = 1 NRS = 1

MQ3 VY VREF1 V3 VSS mitelnmos L = 3u W = 10u AD = 1p AS = 1p NRD = 1 NRS = 1
MQ4 IOUT VREF1 V4 VSS mitelnmos L = 3u W = 10u AD = 1p AS = 1p NRD = 1 NRS = 1

MQ5 VY VY VDD VDD mitelpmos L = 5u W = 6u AD = 1p AS = 1p NRD = 1 NRS = 1
MQ6 IOUT VY VDD VDD mitelpmos L = 5u W = 6u AD = 1p AS = 1p NRD = 1 NRS = 1

.ENDS VCT1


XVCT1 VDD VSS VREF1 VREF2 V1 V2 IOUT VCT1

VPOS VDD 0 1.5
VNEG VSS 0 -1.5

VR1 VREF1 0 0.80V
VR2 VREF2 0 -1.5V

VINPUT1 V1 0 AC
EV V2 0 V1 0 -1

ROUT IOUT 0 1

.TEMP 25
```

```
.OP

.OPTION LIST POST = 2

.model mnmos nmos
+ level = 3.0
+ ld = 1.941e-07
+ dw = -1.279e-07
+ xl = Lith
+ vto = Vthn
+ tpg = 1.0
+ nsub = 1.345e+16
+ cgdo = 2.716e-10
+ cgso = 2.716e-10
+ capop = 4.0
+ tox = 2.671e-08
+ acm = 0.0
+ js = 2.50e-03
+ cj = 3.161e-04
+ cjsw = 2.145e-10
+ mj = 0.3570
+ mjsw = 0.2847
+ pb = 0.7191
+ rsh = 202.6
+ gap1 = 4.73e-04
+ gap2 = 6.36e+02
+ delta = 1.721
+ eta = 2.223e-02
+ kappa = 0.2620
+ nfs = 5.161e+11
+ theta = 4.090e-02
+ vmax = 2.383e+05
+ xj = 2.197e-07
+ uo = 527.2
+ tref = 25.0
.model mpmos pmos
+ level = 3.0
+ ld = 1.735e-07
+ dw = -2.179e-07
+ xl = Lith
+ vto = Vthp
+ tpg = -1.0
+ nsub = 3.947e+16
+ cgdo = 2.534e-10
+ cgso = 2.534e-10
+ capop = 4.0
+ tox = 2.672e-08
+ acm = 0.0
+ js = 2.50e-03
+ cj = 2.898e-04
+ cjsw = 2.052e-10
+ mj = 0.3566
+ mjsw = 0.2450
```

```
+ pb = 0.2259
+ rsh = 393.4
+ gap1 = 4.73e-04
+ gap2 = 6.36e+02
+ delta = 1.829
+ eta = 1.522e-02
+ kappa = 9.994
+ nfs = 9.275e+10
+ theta = 0.1049
+ vmax = 2.795e+05
+ xj = 1.762e-07
+ uo = 193.7
+ tref = 25.0

.END
```

B.5 CMRR Characteristics (see Fig.3.17)

```
**********************************************
*
* -- This is a SPICE Netlist for a bulk-driven VCT
*
* -- CMRR (Common Mode Reject Ratio) Test
*
* Yingtao Jiang
*
* June 1, 1997
*
**********************************************


.SUBCKT VCT1 VDD VSS VREF1 VREF2 V1 V2 IOUT

MQ1 VREF2 VREF2 V3 V1 mitelpmos L = 3u W = 150u AD = 1p AS = 1p NRD = 1 NRS = 1
MQ2 VREF2 VREF2 V4 V2 mitelpmos L = 3u W = 150u AD = 1p AS = 1p NRD = 1 NRS = 1

MQ3 VY VREF1 V3 VSS mitelnmos L = 3u W = 10u AD = 1p AS = 1p NRD = 1 NRS = 1
MQ4 IOUT VREF1 V4 VSS mitelnmos L = 3u W = 10u AD = 1p AS = 1p NRD = 1 NRS = 1

MQ5 VY VY VDD VDD mitelpmos L = 5u W = 6u AD = 1p AS = 1p NRD = 1 NRS = 1
MQ6 IOUT VY VDD VDD mitelpmos L = 5u W = 6u AD = 1p AS = 1p NRD = 1 NRS = 1

.ENDS VCT1


XVCT1 VDD VSS VREF1 VREF2 V1 V2 IOUT1 VCT1

XVCT2 VDD VSS VREF1 VREF2 V1 V1 IOUT2 VCT1
```

```
XVCT3 VDD VSS VREF1 VREF2 V3 V3 IOUT3 VCT1

VPOS VDD 0 1.5
VNEG VSS 0 -1.5

VR1 VREF1 0 0.80V
VR2 VREF2 0 -1.5V

VINPUT1 V1 0 AC 1
EV V2 0 V1 0 -1

ROUT1 IOUT1 0 1
ROUT2 IOUT2 0 1

VINPUT2 V3 0 DC 0
*VINPUT3 V4 0 AC 1
*V3 and V4 are common mode input.

.LIB '$HOME/sim/model_file' nominal

.TEMP 25

.OP

.AC DEC 20 1 100Meg

.OPTION POST

.END
```

B.6 PSRR -- V_{DD} Characteristics (see Fig.3.19)

```
T***********************************************
*
* -- This is a SPICE Netlist for a bulk-driven VCT
*
* -- PSRR (Power Supply Reject Ratio)
*
* -- for PSRR(Vdd) -- Vdd can be varied by some
* -- assumptions. here is an
* -- example how to do it.
*
* -- for Vss, using same strategy by varying its
*
* -- value by some
*
* Yingtao Jiang
*
```

```
* June 1, 1997
*
**********************************************


.SUBCKT VCT1 VDD VSS VREF1 VREF2 V1 V2 IOUT

MQ1 VREF2 VREF2 V3 V1 mitelpmos L = 3u W = 150u AD = 1p AS = 1p NRD = 1 NRS = 1
MQ2 VREF2 VREF2 V4 V2 mitelpmos L = 3u W = 150u AD = 1p AS = 1p NRD = 1 NRS = 1

MQ3 VY VREF1 V3 VSS mitelnmos L = 3u W = 10u AD = 1p AS = 1p NRD = 1 NRS = 1
MQ4 IOUT VREF1 V4 VSS mitelnmos L = 3u W = 10u AD = 1p AS = 1p NRD = 1 NRS = 1

MQ5 VY VY VDD VDD mitelpmos L = 5u W = 6u AD = 1p AS = 1p NRD = 1 NRS = 1
MQ6 IOUT VY VDD VDD mitelpmos L = 5u W = 6u AD = 1p AS = 1p NRD = 1 NRS = 1

.ENDS VCT1


XVCT1 VDD1 VSS VREF1 VREF2 V1 V2 IOUT1 VCT1
XVCT2 VDD2 VSS VREF1 VREF2 V1 V2 IOUT2 VCT1

VPOS1 VDD1 0 1.55
VPOS2 VDD2 0 1.50
VNEG VSS 0 -1.5

VR1 VREF1 0 0.80V
VR2 VREF2 0 -1.5V

VINPUT1 V1 0 AC
EV V2 0 V1 0 -1

ROUT1 IOUT1 0 1
ROUT2 IOUT2 0 1

.LIB '$HOME/sim/model_file' nominal

.TEMP 25

.OP

.AC DEC 20 1 100Meg

.OPTION POST

.PRINT AC IM(ROUT)
+ IP(ROUT)
+ PSRR =
+ par("0.05 / ((I(ROUT1) / (V(V1) * 2)) - (I(ROUT2) / (V(V1) * 2))) * (I(ROUT2) / (V(V1) * 2))")

.END
```

B.7 Noise Characteristics (see Table 5)

```
*********************************************
*
* -- This is a SPICE Netlist for a bulk-driven VCT
*
* -- Noise Characteristics
*
* -- Frequency dependent
*
* Yingtao Jiang
*
* June 1, 1997
*
*********************************************


.SUBCKT VCT1 VDD VSS VREF1 VREF2 V1 V2 IOUT

MQ1 VREF2 VREF2 V3 V1 mitelpmos L = 3u W = 150u AD = 1p AS = 1p NRD = 1 NRS = 1
MQ2 VREF2 VREF2 V4 V2 mitelpmos L = 3u W = 150u AD = 1p AS = 1p NRD = 1 NRS = 1

MQ3 VY VREF1 V3 VSS mitelnmos L = 3u W = 10u AD = 1p AS = 1p NRD = 1 NRS = 1
MQ4 IOUT VREF1 V4 VSS mitelnmos L = 3u W = 10u AD = 1p AS = 1p NRD = 1 NRS = 1

MQ5 VY VY VDD VDD mitelpmos L = 5u W = 6u AD = 1p AS = 1p NRD = 1 NRS = 1
MQ6 IOUT VY VDD VDD mitelpmos L = 5u W = 6u AD = 1p AS = 1p NRD = 1 NRS = 1

.ENDS VCT1


XVCT1 VDD VSS VREF1 VREF2 V1 V2 IOUT VCT1

VPOS VDD 0 1.5
VNEG VSS 0 -1.5

VR1 VREF1 0 0.80V
VR2 VREF2 0 -1.5V

VINPUT1 V1 0 AC 1
EV V2 0 V1 0 -1
*VV2 V2 0 0

ROUT IOUT 0 1

.NOISE V(Iout) VINPUT1 Iout

.LIB '$HOME/sim/model_file' nominal

.TEMP 25
.OP
.AC DEC 20 10K 10meg
```

```
.OPTION POST
.PRINT NOISE onoise

.END
```

B.8 Floating Resistor Implementation (see Table 7 and Fig.4.4)

```
**********************************************
*
* -- This is a SPICE Netlist for a bulk-driven VCT
*
* -- Floating Resistor Implementation
*
* -- Two VCTs are used to build a floating
* -- resistor.
*
* Yingtao Jiang
*
* June 1, 1997
*
**********************************************


.SUBCKT Flt_Resistor Vnet1 Vnet2

XVCT1 VDD VSS VREF1 VREF2 Vnet2 Vnet1 Vnet2 VCT1
XVCT2 VDD VSS VREF1 VREF2 Vnet1 Vnet2 Vnet1 VCT1

Vpos VDD 0 1.5V
Vneg VSS 0 -1.5V

Vr1 VREF1 0 0.8V
Vr2 VREF2 0 -1.5V

VV2 V2 0 0V

.ENDS Flt_Resistor


.SUBCKT VCT1 VDD VSS VREF1 VREF2 V1 V2 IOUT

MQ1 VREF2 VREF2 V3 V1 mitelpmos
+ L=3u W=280u AD=1p AS=1p NRD=1 NRS=1
MQ2 VREF2 VREF2 V4 V2 mitelpmos
+L=3u W=280u AD=1p AS=1p NRD=1 NRS=1
MQ3 VY VREF1 V3 VSS mitelnmos
+ L=3u W=10u AD=1p AS=1p NRD=1 NRS=1
MQ4 IOUT VREF1 V4 VSS mitelnmos
+ L=3u W=10u AD=1p AS=1p NRD=1 NRS=1
MQ5 VY VY VDD VDD mitelpmos
+ L=5u W=6u AD=1p AS=1p NRD=1 NRS=1
```

```
MQ6 IOUT VY VDD VDD mitelpmos
+L=5u W=6u AD=1p AS=1p NRD=1 NRS=1

.ENDS VCT1


XFlt_Resistor V1 V2 Flt_Resistor


VIN V1 V2 AC 1

Rx V2 0 1K


.LIB '$HOME/sim/model_file' nominal


.TEMP 25

.OP

.NET VIN RIN = 1

.AC DEC 20 1 3Meg

.OPTION POST

.PRINT AC ZIN(R) ZIN(I)


.END
```

B.9 Grounded Inductor Realization (see Table 8 and Fig.4.7)

```
**********************************************
*
* -- This is a SPICE Netlist for a bulk-driven VCT
*
* -- Grounded Inductor Realization
*
* -- Two VCTs are used.
*
* -- Frequency dependent
*
* Yingtao Jiang
*
* June 1, 1997
*
**********************************************

.SUBCKT GYRATOR V1 IOUT
```

```
XVCT1 VDD VSS VREF1 VREF2 V1 V2 IOUT VCT1
XVCT2 VDD VSS VREF1 VREF2 V2 IOUT V1 VCT1

Vpos VDD 0 1.5V
Vneg VSS 0 -1.5V

Vr1 VREF1 0 1.0V
Vr2 VREF2 0 -1.3V

VV2 V2 0 0V

.ENDS GYRATOR

.SUBCKT VCT1 VDD VSS VREF1 VREF2 V1 V2 IOUT

MQ1 VREF2 VREF2 V3 V1 mitelpmos L=3u W=280u AD=1p AS=1p NRD=1 NRS=1
MQ2 VREF2 VREF2 V4 V2 mitelpmos L=3u W=280u AD=1p AS=1p NRD=1 NRS=1
MQ3 VY VREF1 V3 VSS mitelnmos L=3u W=10u AD=1p AS=1p NRD=1 NRS=1
MQ4 IOUT VREF1 V4 VSS mitelnmos L=3u W=10u AD=1p AS=1p NRD=1 NRS=1
MQ5 VY VY VDD VDD mitelpmos L=5u W=6u AD=1p AS=1p NRD=1 NRS=1
MQ6 IOUT VY VDD VDD mitelpmos L=5u W=6u AD=1p AS=1p NRD=1 NRS=1

.ENDS VCT1

******* SUBCKT VCT ENDS HERE. ***********

XGYRATOR V1 IOUT GYRATOR


VIN V1 0 AC 0.1

C11 IOUT 0 5pF

.LIB '$HOME/sim/model_file' nominal

.TEMP 25

.OP

.NET VIN RIN = 1

.AC DEC 20 1 300K

.OPTION POST

.PRINT AC ZIN(R)
+ ZIN(I)

.PRINT AC VR(IOUT)
+ VM(IOUT)
```

```
.END
```

B.10 A Third Order Filter Realization Using VCT-Based Floating Inductor (see Figs.4.10 and 4.11)

```
**********************************************
*
* -- This is a SPICE Netlist for a bulk-driven VCT
*
* -- Floating Inductor Realization
*
* -- Further, this floating inductor is used
* -- to build a 3rd order filter.
*
* Yingtao Jiang
*
* June 1, 1997
*
**********************************************

xvct1 vdd vss vref1 vref2 v1 v2 iout vct1
xvct2 vdd vss vref1 vref2 v2 iout v1 vct1

vpos vdd 0 1.5v
vneg vss 0 -1.5v

vr1 vref1 0 1.0v
vr2 vref2 0 -1.28v

vv2 v2 0 0v

.ends gyrator

.subckt vct1 vdd vss vref1 vref2 v1 v2 iout

mq1 vref2 vref2 v3 v1 mitelpmos l=3u w=280u ad=1p as=1p nrd=1 nrs=1
mq2 vref2 vref2 v4 v2 mitelpmos l=3u w=280u ad=1p as=1p nrd=1 nrs=1
mq3 vy vref1 v3 vss mitelnmos l=3u w=10u ad=1p as=1p nrd=1 nrs=1
mq4 iout vref1 v4 vss mitelnmos l=3u w=10u ad=1p as=1p nrd=1 nrs=1
mq5 vy vy vdd vdd mitelpmos l=5u w=6u ad=1p as=1p nrd=1 nrs=1
mq6 iout vy vdd vdd mitelpmos l=5u w=6u ad=1p as=1p nrd=1 nrs=1

.ends vct1

.subckt float_inductor in out cload
xgyrator1 in cload gyrator
xgyrator2 cload out gyrator
.ends float_inductor

xfloat_inductor n2 n3 cc float_inductor
```

```
cin cc 0 10.0pf

rin n1 n2 1k
c1 n2 0 1.89pf
*li n2 n3 37.74mh
c2 n3 0 1.89pf
rl n3 0 1k

vs n1 0 ac 1v

.temp 25

.op

.LIB '$HOME/sim/model_file' nominal

.option post

.ac dec 20 1 100k

.print ac vm(n3) vp(n3) vdb(n3)

.end
```

B.11 A Second LP Filter Implementation using 2 Volts Voltage Supplies (see Figs.5.9 and 5.11)

```
***********************************************

*

* -- This is a SPICE Netlist for a bulk-driven VCT

*

* -- 2nd order filter LP using postlayout

* -- data.

*

* -- Vdd = -Vss = 1Volt

*

* Yingtao Jiang

*
```

```
* June 1, 1997
*
**********************************************

.subckt gyrator in out
xota1 in 0 out ota
xota2 0 out in ota
.ends gyrator

.subckt inductor in out
xgyrator1 in Cload gyrator
xgyrator2 cload out gyrator
C1 cload 0 15pf
.ends inductor

.subckt OTA Vpos Vneg Iout

xi10 IOUT Vpos Vneg g2 g3 sub1

v5 g2 0 -1.0
v2 g3 0 1.0
.ends OTA

.LIB '$HOME/sim/model_file' nominal

.subckt sub1 iout v1 v2 vref1 vref2
vpos g3 0 1.0
```

```
vneg g2 0 -1.0

c3 n2 g3 1.31843505212593e-15 m=1.0
c4 n2 vref2 808.499989115604e-18 m=1.0
c5 vref1 n1 808.499989115604e-18 m=1.0
c6 n0 vref2 1.35019497599971e-15 m=1.0
c7 v2 g3 4.52674481693548e-15 m=1.0
c8 iout g3 2.35876504722928e-15 m=1.0
c9 g2 g3 16.9739998559558e-15 m=1.0
c10 vref2 g3 22.8748802939913e-15 m=1.0
c11 n2 g3 2.03073904466908e-15 m=1.0
c12 n1 g3 2.82175495026438e-15 m=1.0
c13 n0 g3 1.40207997918377e-15 m=1.0
c14 v2 g3 298.079999742971e-18 m=1.0
c15 g2 iout 165.59999691612e-18 m=1.0
c16 n2 v2 331.199993832239e-18 m=1.0
c17 n1 g2 315.330011002262e-18 m=1.0
c18 v1 g3 298.079999742971e-18 m=1.0
c19 vref1 g3 77.6249977272505e-18 m=1.0
c20 n0 v1 331.199993832239e-18 m=1.0
c21 vref2 g3 19.2404618170987e-15 m=1.0
c22 vref1 g3 13.0342725883901e-15 m=1.0
c23 vref2 v2 967.85997371864e-18 m=1.0
c24 n1 g2 1.72799803437561e-15 m=1.0
c25 v1 vref2 967.85997371864e-18 m=1.0
c26 v1 g3 4.67944198743585e-15 m=1.0
c27 n1 g3 4.12585682849423e-15 m=1.0
```

```
m28 iout vrefl n2 g3 mitelpmos l=3.00000010611257e-6 w=549.999997019768e-6
+ad=2.9700000236943e-9 as=2.9700000236943e-9 pd=1.11079995986074e-3
+ps=1.11079995986074e-3 nrd=+4.09090911e-03 nrs=+4.09090911e-03 m=1.0
m29 n0 vrefl n1 g3 mitelpmos l=3.00000010611257e-6 w=549.999997019768e-6
+ad=2.94250002141894e-9 as=2.99750002596966e-9 pd=1.11069995909929e-3
+ps=1.11089996062219e-3 nrd=+4.09090911e-03 nrs=+4.09090911e-03 m=1.0
m30 iout n1 g2 g2 mitelnmos l=3.00000010611257e-6 w=29.9999992421363e-6
+ad=161.999996750595e-12 as=161.999996750595e-12 pd=70.8000006852672e-6
+ps=70.8000006852672e-6 nrd=+7.50000019e-02 nrs=+7.50000019e-02 m=1.0
m31 n1 n1 g2 g2 mitelnmos l=3.00000010611257e-6 w=29.9999992421363e-6
+ad=161.999996750595e-12 as=161.999996750595e-12 pd=70.8000006852672e-6
+ps=70.8000006852672e-6 nrd=+7.50000019e-02 nrs=+7.50000019e-02 m=1.0
m32 n0 vref2 g3 v1 mitelnmos l=3.00000010611257e-6 w=199.999994947575e-6
+ad=1.0799999783373e-9 as=1.0799999783373e-9 pd=410.800013924018e-6
+ps=410.800013924018e-6 nrd=+1.12500003e-02 nrs=+1.12500003e-02 m=1.0
m33 g3 vref2 n2 v2 mitelnmos l=3.00000010611257e-6 w=199.999994947575e-6
+ad=1.0799999783373e-9 as=1.0799999783373e-9 pd=410.800013924018e-6
+ps=410.800013924018e-6 nrd=+1.12500003e-02 nrs=+1.12500003e-02 m=1.0
.ends sub1

Vi1 n1 0 ac 1
Rs1 n1 n2 800

xinductor1 n2 n3 inductor

Cc1 n3 0 16nf
```

```
Rl1 n3 0 1k

Rs2 n1 n5 1K

xinductor2 n5 n6 inductor

Cc2 n6 0 16nf

Rl2 n6 0 1k

.AC DEC 20 1.00000 300K

.temp 25.0000

.op

.option acout = 0 POST

.PRINT AC VM(n3) VP(n3) VDB(n3) VM(n6) VP(n6) VDB(n6)


.end
```

Appendix C

Model Parameters of Mitel's ISO-HCMOS (P-well, 1.5 micron) Technology (Nominal Model)

NMOS

ld=1.941e-07 dw=-1.279e-07 xl=-1.269e-07 vto=0.8404 tpg=1.0 nsub=1.345e+16
cgdo=2.716e-10 cgso=2.716e-10 capop=4.0 tox=2.671e-08 acm=0.0 js=2.50e-03
cj=3.161e-04 cjsw=2.145e-10 mj=0.3570 mjsw=0.2847 pb=0.7191 rsh=202.6
gap1=4.73e-04 gap2=6.36e+02 delta=1.721 eta=2.223e-02 kappa=0.2620
nfs=5.161e+11 theta=4.090e-02 vmax=2.383e+05 xj=2.197e-07 uo=527.2 tref=25.0

PMOS

ld = 1.735e-07 dw = -2.179e-07 xl = -1.267e-07 vto = -0.7281 tpg = -1.0
nsub = 3.947e+16 cgdo = 2.534e-10 cgso = 2.534e-10 capop = 4.0 tox = 2.672e-08
acm = 0.0 js = 2.50e-03 cj = 2.898e-04 cjsw = 2.052e-10 mj = 0.3566 mjsw = 0.2450
pb = 0.2259 rsh = 393.4 gap1 = 4.73e-04 gap2 = 6.36e+02 delta = 1.829
eta = 1.522e-02 kappa = 9.994 nfs = 9.275e+10 theta = 0.1049 vmax = 2.795e+05
xj = 1.762e-07 uo = 193.7 tref = 25.0