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# A SINGLE STAGE FULL BRIDGE POWER FACTOR CORRECTED AC/DC CONVERTER

**Nasser Ismail**

**A Thesis**

**in**

**The Department**

**of**

**Electrical and Computer Engineering**

**Presented in Partial Fulfillment of the Requirements**
**for the Degree of Master of Applied Science at**
**Concordia University**
**Montreal, Quebec, Canada**

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# ABSTRACT

## A Single Stage Full Bridge Power Factor Corrected AC/DC Converter

Nasser Ismail

Conventional single phase AC/DC converters use a two stage power configuration to provide a regulated DC power supply at high input power factor. Elimination of one of these stages can reduce the cost, weight, size, complexity and increase the overall reliability of this converter. This thesis proposes a single stage power factor correction converter circuit. This proposed converter circuit uses the traditional non-power-factor corrected circuit configuration with only few additional components. These are: an additional winding on the high frequency transformer, a small high frequency inductor and three diodes. The topology allows the output voltage regulation and input current shaping with a single power processing stage and one control chip. In addition, it is shown that this converter can be designed to offer soft switching of the full bridge switches. The operating principles of the proposed converter are discussed and its performance characteristics under steady state conditions are examined. A design procedure is illustrated to select the components of the converter for a 500 W power supply operating at 50 kHz. Theoretical results are verified with simulation and experimental tests on a 500 W laboratory prototype.

## ACKNOWLEDGMENTS

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## LIST OF ACRONYMS

| | |
|---|---|
| AC | Alternating Current |
| CACM | Continuous Auxiliary Inductor Current Mode |
| COCM | Continuous Output Inductor Current Mode |
| DACM | Discontinuous Auxiliary Inductor Current Mode |
| DC | Direct Current |
| DOCM | Discontinuous Output Inductor Current Mode |
| FB | Full Bridge DC/AC Converter |
| IGBT | Insulated Gate Bipolar Transistor |
| MOSFET | Metal-Oxide-Semiconductor Field Effect Transistor |
| PFC | Power Factor Correction |
| PWM | Pulse Width Modulation |
| RMS | Root Mean Square |
| SMPS | Switch-Mode Power Supply |
| SS | Single Stage |
| THD | Total Harmonic Distortion |
| uF | Micro Farad |
| uH | Micro Henri |
| ZCS | Zero Current Switching |
| ZVS | Zero Voltage Switching |

# LIST OF PRINCIPAL SYMBOLS

| | |
|---|---|
| $C_{bl}$ | Dc Blocking Capacitor |
| $C_{dc}$ | Dc Link Capacitor |
| $C_o$ | Output Filter Capacitor |
| $D$ | Duty Cycle - Charging Time of auxiliary and Output Inductors |
| $D'$ | Discharging Time of Auxiliary Inductor |
| $D_{aux1}$, $D_{aux2}$ | Diodes of the Auxiliary Diode Rectifier |
| $D_{max}$ | Maximum Duty Cycle |
| $D_o^{'}$ | Discharging Time of Output Inductor |
| $D_{o1}$, $D_{o2}$ | Diodes of the Output Diode Rectifier |
| $D_{su}$ | Start-up Diode |
| $f_L$ | Line Frequency |
| $f_{sw}$ | Switching Frequency |
| $f_{sn}$ | Number of Switching Periods in one line frequency period |
| $i_{aux}$ | Auxiliary Inductor Current |
| $i_{aux,n}$ | N-th Component of the Auxiliary Current |
| $i_{Cdc}$ | DC Link Capacitor Current |
| $i_{Cdc\_1n}$ | N-th Component of the DC Link Capacitor Current During On Time |
| $i_{Cdc\_1n}$ | N-th Component of the DC Link Capacitor Current During Off Time |
| $i_{Cdc\_n}$ | N-th Component of the Overall DC Link Capacitor Current |
| $I_{Cdc,rms}$ | DC Link Capacitor RMS Current |

| | |
|---|---|
| $i_{Co\_1}$ | Output Filter Capacitor Current During Charging Time |
| $i_{Co\_2}$ | Output Filter Capacitor Current During Discharging Time |
| $I_{co,rms}$ | Output Filter Capacitor RMS Current |
| $i_{in\_1n}$ | N-th Component of the Input Current During On Time |
| $i_{in\_2n}$ | N-th Component of the Input Current During Off Time |
| $i_{in\_n}$ | N-th Component of the Overall Input Current |
| $I_{in,rms}$ | Input RMS Current |
| $i_{Lo}$ | Output Inductor Current |
| $I_{Lo,p}$ | Peak Output Inductor Current |
| $i_M$ | Magnetizing Current |
| $i_o$ | Instantaneous Output Current |
| $I_{o,avg}$ | Average Output Current |
| $I_p$ | Primary Current |
| $i_{sw}$ | Current through Full Bridge Switches |
| $I_{sw,rms}$ | RMS Switch Current |
| $K_{ripple}$ | Ratio of Output Inductor Ripple to The Rated Output Current |
| $L_{aux}$ | Auxiliary Inductor |
| $L_o$ | Output Filter Inductor |
| $n_{aux}$ | Turns Ratio of Primary to Auxiliary Windings |
| $n_s$ | Turns Ratio of Primary to Secondary Windings |
| $N_{aux}$ | Auxiliary Winding Number of Turns |
| $N_p$ | Primary Winding Number of Turns |

| | |
|---|---|
| $N_s$ | Secondary Winding Number of Turns |
| $P_{(B)}$ | Base Power |
| $P_o$ | Output Power |
| $P_{o,disc}$ | Output Power For Discontinuous Output Inductor Current |
| $P_{sw,loss}$ | Switching Losses |
| $Q_1$-$Q_4$ | Switches of The Full Bridge |
| $R_o$ | Output Load Resistance |
| $t_{on}$ | On Time |
| $t_{off}$ | Off Time |
| $t_1$-$t_{10}$ | Switching Instants of The full Bridge switches |
| $T_L$ | Line Frequency Period |
| $T_s$ | Switching Frequency Period |
| $T_s'$ | Half Switching Frequency Period, or Auxiliary Current Waveform Period |
| $V_{aux}$ | Auxiliary Added Voltage |
| $V_{(B)}$ | Base Voltage |
| $V_{dc}$ | DC Link Voltage |
| $V_{laux}$ | Voltage Across the Auxiliary Inductor |
| $V_o$ | Output Voltage |
| $V_p$ | Primary Voltage |
| $V_s$ | Peak Input Voltage |
| $V_{s,rms}$ | RMS Input Voltage |
| $V_{s,max}$ | Maximum Value of Line Voltage |

| | |
|---|---|
| $V_{s,min}$ | Minimum Value of Line Voltage |
| $V_{sn}$ | Value of Input Voltage at the n-th Switching Period |

# CHAPTER 1

# INTRODUCTION

## 1.1 General Introduction

A desired feature in most of today's switch-mode power supplies (SMPS) is to improve power factor and thereby to comply with various national and international regulations on harmonic pollution of the utility (such as IEC 555-2 , IEC 1000-3-2 and IEEE 519) in line operated electronic equipment [1]-[2].

Power factor is defined as the ratio of the real power measured in Watts to the apparent power which is the product of the RMS current multiplied by the RMS voltage. However, it has been historically defined in terms of a phase-shift between the voltage and current waveforms. In a SMPS, shown in Fig. 1.1, which uses a front-end diode rectifier to provide a dc voltage across a bulky dc link capacitor, poor input power factor does not come from the phase-shift between the line voltage and current. Rather it is the discontinuous charging of the dc link filter capacitor, which results in a narrow pulse of high peak current as shown in Fig. 1.2. This leads to a low input power factor ( $< 0.65$ ) [3] and high total harmonic distortion.

High harmonic content of the input current causes a voltage distortion at the point of common coupling causing over-voltages. This is unacceptable especially if sensitive equipment such as mainframe computers and telecommunication equipment are connected to the same point of common coupling.

Traditionally their are two ways of shaping the input current waveform so that the overall off-the-line AC/DC converter is seen as a resistive load by the ac mains. The first is the passive approach in which a 60 Hz inductor connected to the ac mains is used, but this is not a practical solution, as it adds to the size and weight of the power supply, in a time when these parameters are minimized by the use of higher switching frequencies. The second is the active approach, where a DC/DC converter is used to shape the input current waveform.

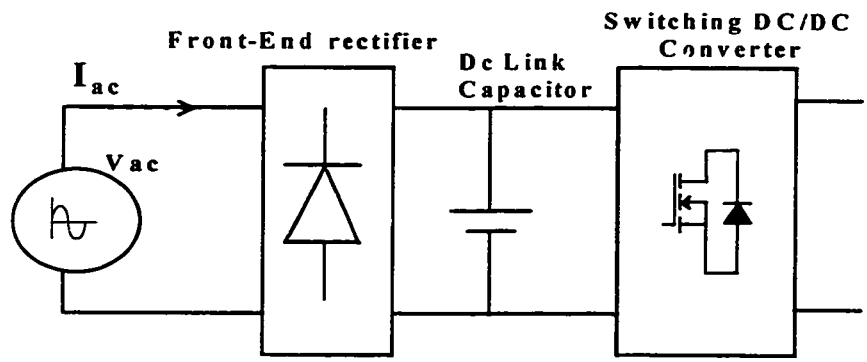


**Fig. 1.1** Traditional Switch-Mode Power Supply (SMPS)

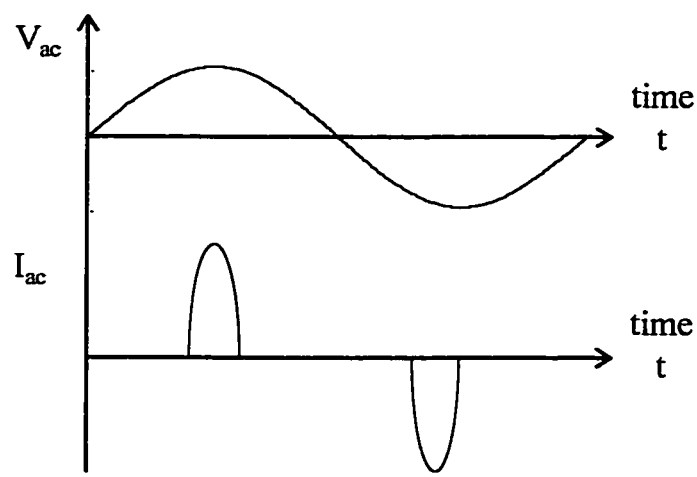


**Fig. 1.2** Input voltage and current waveforms for a traditional SMPS

## 1.2 Literature Review

Active power factor correction techniques which are used to provide a sinusoidal input current for SMPS that use a front-end diode rectifier have been widely reported in the literature. The two stage technique which uses a separate DC/DC converter to perform the input current shaping is shown in Fig 1.3, [4]-[5]. This approach which is presented in Fig 1.4 is mostly used with a boost converter in the role of wave-shaper [6]-[7]. The boost converter has an output voltage across the DC capacitor, which is higher than the peak input voltage. When the switch is on, current rises and flow through the switch. When the switch is off, current falls and flow through the diode to the output. The input current is shaped to be sinusoidal if the rise and fall times are programmed to track a sine wave. The boost converter might operate in continuous mode for high power or in discontinuous mode for lower power applications [8]. Although the two-stage PFC approach has many advantages, it has some drawbacks. For instance, it has two power stages and two control circuits are therefore needed, it is inefficient and is not cost effective [9] as in the case of low power applications.

The drawbacks associated with two-stage PFC methods motivated several researchers to find other ways to provide both input current shaping and output voltage regulation. Thus, a new class of new single stage PFC (SS-PFC) topologies have been proposed [10]-[20].

The use of the boost converter topology to perform both functions of current shaping and output voltage regulation was reported in [6]-[7], and [11]-[13]. However

this approach has a main drawback: that is bandwidth of the output voltage regulation is limited to few Hertz [14].

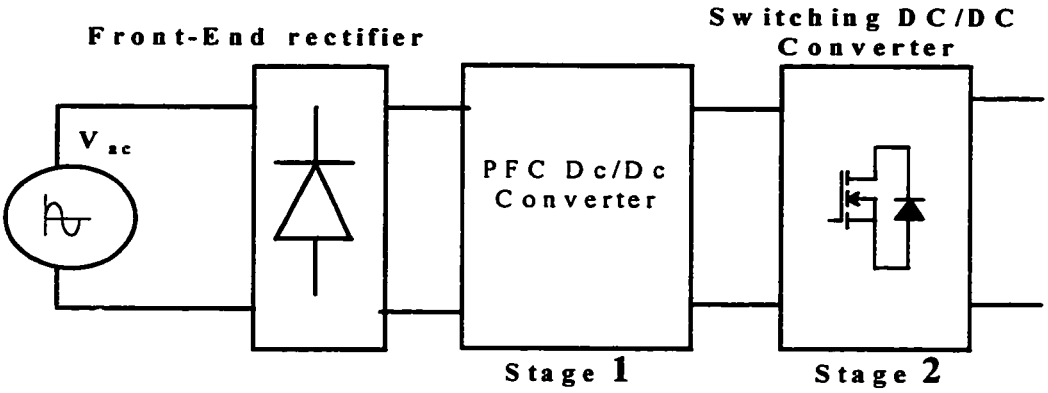


**Fig. 1.3** Two-Stage power factor correction circuit

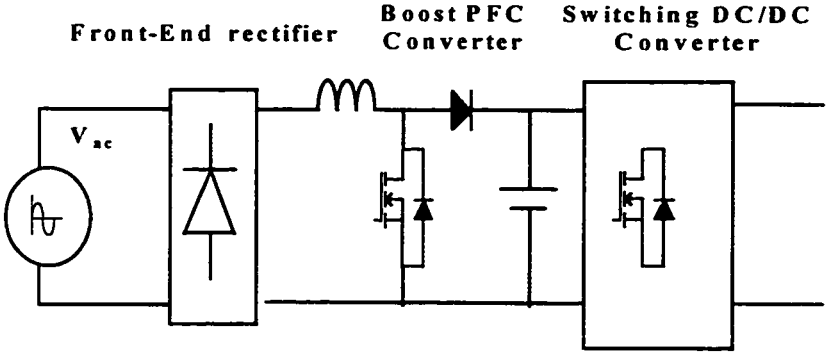


**Fig. 1.4.** Boost converter in the role of PFC converter

The buck-boost derived topologies were proposed to perform PFC mainly because they emulate a natural resistor when operating in discontinuous conduction mode (DCM) [15]-[16]. They can also offer an output voltage less or higher than the input voltage [8].

Other topologies such as forward derived topologies were also presented in [11]-[12] and [17]-[20]. These topologies are appropriate for low power levels up to 250 watts.

A new family of isolated power factor corrected switching power supplies have been proposed in [21] and design considerations for these converters have been presented in [22]. In these topologies, the power factor correction cell is followed by a DC/DC converter cell, and both cells are operated in DCM. The voltage across the energy storage capacitor is independent of the load, but still increases with line voltage and decreasing ratio of input and output stage inductance. When the DC/DC cell is operated in continuous conduction mode (CCM), which is preferable for low output voltage, light load current applications. The negative effect is a load dependent variation of the energy storage capacitor voltage [23]-[24].

The use of magnetic amplifiers (magamps) for PFC has also been reported, where the magamp controls the rectified line current, while the fast output regulation is provided independently. This is done through pulse width modulation (PWM) of the active switch of the Cuk converter as shown in [25] or PWM of the bridge switches as shown in [14]. The use of magamps with DCM provide input current shaping with fast voltage regulation, while keeping constant the voltage on the energy storage capacitor regardless of load and line eliminating the increased voltage stress on the transistors and diodes.

A boost supply using resonant techniques might be used in series with the energy storage capacitor to provide high input power factor in a single stage configuration [26]. Other resonant SS-PFC circuits based on the half bridge converter [3] and forward converter topologies [20]. The Characteristics of full bridge parallel and series-parallel

converters operating in high power factor mode were presented in [27]. These converters offer a power factor up to 0.96. Unfortunately, the resonant converters use resonant techniques, with variable frequency operation which leads to higher circulating currents and variable frequency operation that complicates EMI filter design.

## 1.3 Thesis Objectives and Scope

The objectives of this thesis are to propose and analyze a new single stage power factor corrected AC/DC converter which overcomes several of the drawbacks mentioned in the previous section. The scope of this thesis is limited to the analysis of the characteristics of the proposed converter topology under steady-state conditions. Emphasis is given on demonstrating the operating principle, modes of operation, and derives circuit equations .

The major contributions of this thesis are:

(1) Proposing a new single stage power factor corrected AC/DC converter topology that features simple power and control circuitry .

(2) Performing steady state analyses of the proposed converter in both continuous and discontinuous modes of operation.

(3) Selection of a proper control technique to modulate the full bridge to provide close to zero switching losses.

(4) Development of a design procedure to choose circuit components.

(5) Experimental verification of the proof-of-concept of the proposed converter.

The contents of this thesis are organized as follows:

In Chapter 2, a general description of the new single-stage power factor corrected full-bridge converter is provided. The principle of operation is explained in details and the operation of the converter over a switching period is described in terms of nine operating modes. The issue of switching losses and requirements for soft switching are given in this chapter as well.

In Chapter 3, the steady state analysis of the proposed converter for continuous output current is performed. The steady state operation analysis is based on three different states of the auxiliary inductor current waveform. An alternative method to find the value of the auxiliary inductance necessary for proper operation of the circuit is proposed. The method also provides a way of finding the turns ratios of the high frequency transformer. The Dc link voltage depends on the duty cycle, load, output and auxiliary inductances. Performance characteristics of the converter such as RMS current through the switches, capacitors, RMS. input current, output voltage and current ripples and power factor are also presented.

In Chapter 4, the operation of the converter with discontinuous output inductor current mode (DOCM) is proposed. This mode of operation reduces the dc link voltage value to acceptable levels. The steady state analysis of the converter in this mode is provided. A comparison of performance characteristics for the converter operating in both COCM and DOCM is presented and results are illustrated in the form of graphs.

In Chapter 5, the design issues of the SS-FB-PFC converter are considered. The choice of operating switching frequency is explained and the auxiliary inductor is chosen. The design procedure is presented and verified with simulated and experimental results.

In Chapter 6, the conclusions of this thesis are given and suggestions for future work are presented.

# CHAPTER 2

# DESCRIPTION OF THE PROPOSED CONVERTER CIRCUIT AND MODES OF OPERATION

## 2.1 Introduction

This chapter provides a general description of the proposed single stage high power factor full bridge AC/DC converter topology. Details of the circuit and its operation principle are presented.

Description of the proposed circuit is given in section 2.2. In Section 2.3 the principle of operation is described. Modes of operation of the circuit are discussed in section 2.4. In Section 2.5 the issues and requirements for loss-less switching operation are discussed.

## 2.2 Description of the Proposed Converter Circuit

The proposed single-stage PFC full bridge AC/DC converter is shown in Fig. 2.1, which consists of:

**(a)** Front-End Diode Rectifier ($FB_{FE}$) which is used to convert the ac input voltage to an uncontrolled DC voltage across the DC link capacitor,

**(b)** DC Link Capacitor ($C_{dc}$) which provides the filtering action for the 120 Hz component and hold-up time,

**(c)** Full Bridge DC/AC Inverter (FB) which consists of four MOSFET switches that have built-in anti-parallel diodes. Phase shift control is used to control the switching action of the full bridge switches.

**(d)** DC Blocking Capacitor ($C_{bl}$) which is used to block any net dc component that might saturate the high frequency transformer.

**(e)** High Frequency Transformer ($TR_{HF}$) which has three windings: The primary winding (with $N_P$ turns) is connected to the FB legs, the secondary winding (with $N_s$ turns) is connected to the Output Full-Wave Diode Rectifier ($HB_o$), and the third auxiliary winding ( with $N_{aux}$ turns ) is connected to the Auxiliary Full-Wave Diode Rectifier ($HB_{aux}$).

**(f)** Auxiliary Circuit which includes the Auxiliary Transformer Winding (with $N_{aux}$ turns), $HB_{aux}$ and Auxiliary Inductor ($L_{aux}$). This auxiliary circuit is the key to the proper operation of the proposed circuit as a power factor correction circuit. A proper design of $L_{aux}$ will cause the input current to be discontinuous and follow a sinusoidal shape, as the net positive voltage applied across this inductor during the conduction of any diagonal pair of the FB switches is necessarily the rectified ac mains voltage.

**(g)** Output Filter which consists of Output Filter Capacitor ($C_o$ ) and Inductor ($L_o$ ) which might operate in continuous conduction mode (COCM), or in discontinuous current mode (DOCM) to reduce the dc link voltage to acceptable levels.

## 2.3 Principle of Operation

The sinusoidal mains voltage is rectified through the front end bridge diode rectifier. A voltage from the auxiliary transformer winding which is rectified using half bridge diode rectifier is added to the rectified voltage. This forces the input current to follow a sinusoidal shape and flow in discontinuous manner. The full bridge phase shifted PWM converter topology provides a good choice to control the converter. Its control features are similar to regular PWM converter.

Four MOSFET switches ($Q_1$ - $Q_4$) and a high frequency power transformer are used to form the full bridge. The capacitor $C_{b1}$ is used to block any net dc voltage from appearing across the transformer primary and saturating it. A center-tapped secondary is used with ultra-fast rectifiers at the output. The gate drives of both legs, $Q_1$, $Q_4$ or $Q_2$, $Q_3$ are complementary with duty cycle close to 50%. However a known delay is introduced between turn-off of one switch and the turn-on of the other switch of the same leg to avoid simultaneous conduction of any two switches from the same leg. This delay also allows the capacitor across the switch to discharge to zero so that the switch is turned on at zero voltage.

The output voltage regulation is achieved by phase modulation, that is by adjusting the amount of time the right and left legs of the full bridge are in phase or out of phase with each other. When both legs are in phase, no power is transferred to the load. If they are out of phase full power is transferred or delivered. When $Q_1$, $Q_3$ are conducting, positive voltage is applied to the primary and when $Q_2$, $Q_4$ are conducting, negative

voltage is applied to it. During other periods the primary voltage is zero and energy stored in the output filter inductor free-wheels through the secondary.

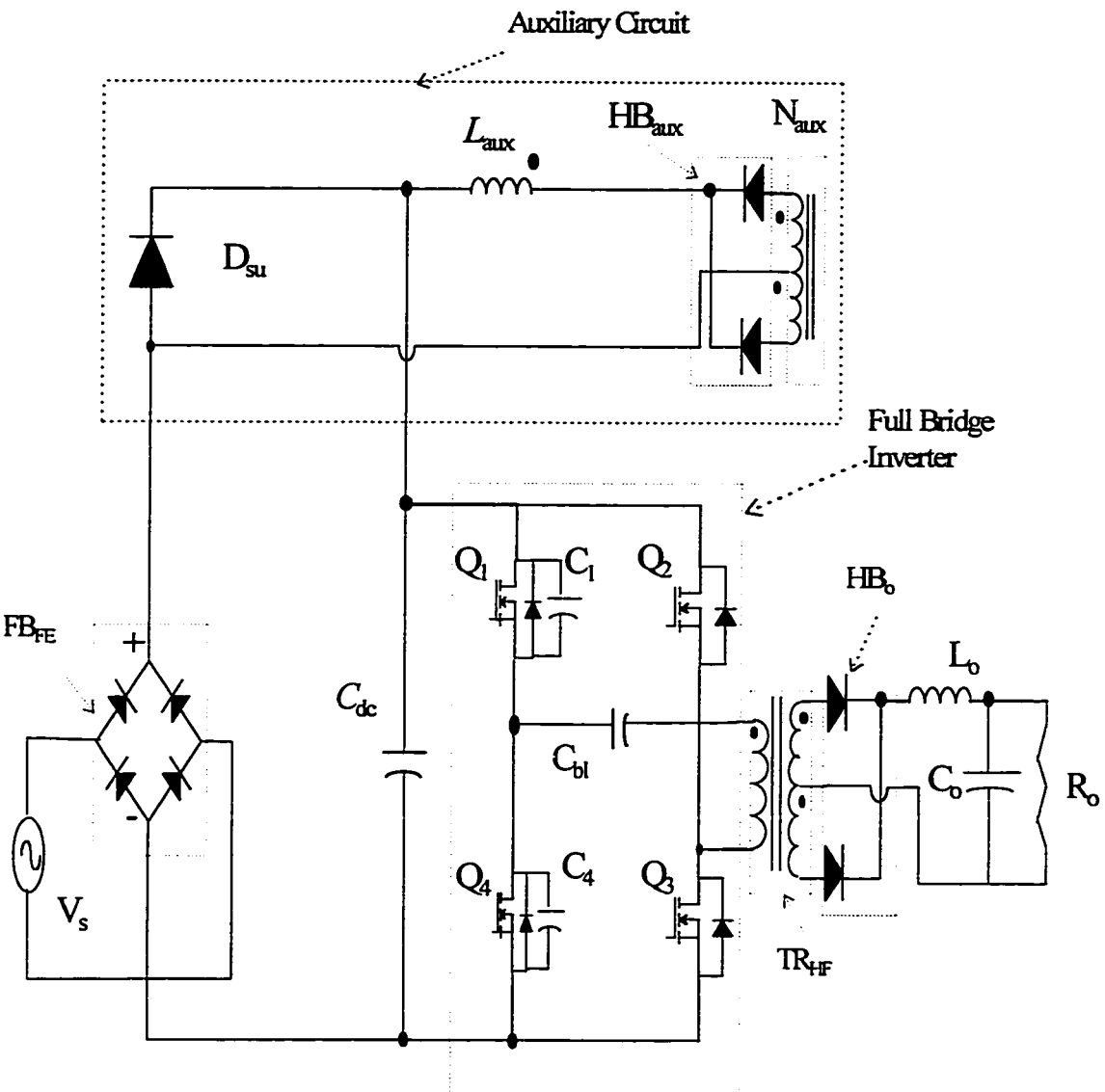


**Fig. 2.1** Power circuit of the New Single Stage Full-Bridge Power Factor Corrected AC/DC Converter

## 2.4 Circuit Modes of Operation

The analysis of circuit operation and its topological modes are presented in this section. To be able to perform this analysis, the operating waveforms are presented in Fig. 2.2.

These waveforms show the gating signals of the FB switches. The amount of phase shift between the left and right legs is adjusted to keep the output voltage constant with changing line and load. Pulse duration of each switch is slightly less than 50 % of the switching period due to the time delay introduced between the gating signals of any two switches from the same leg. The effective duty cycle is defined as the time during which a diagonal pair conducts ($Q_1$, $Q_3$ or $Q_2$, $Q_4$). This duty cycle is maximum for minimum line voltage and maximum load. Also the current through the primary winding of the high frequency transformer and voltage across it are shown in this figure.

The operation of the circuit over a cycle of switching frequency could be explained in terms of the following topological modes of operation

### 2.4.1 MODE 1, Interval [t1, t2]: $Q_1$, $Q_3$ Conduction

The circuit representing this topological mode of operation is shown in Fig 2.3. During this mode: At time $t = t_1$, $Q_3$ is turned on and power is transferred to the secondary winding as the diagonal pair of switches $Q_1$ and $Q_3$ are both conducting. The dc link capacitor discharges during this mode as the current flows in the negative direction, and the output inductor current reaches peak value at $t = t_2$.

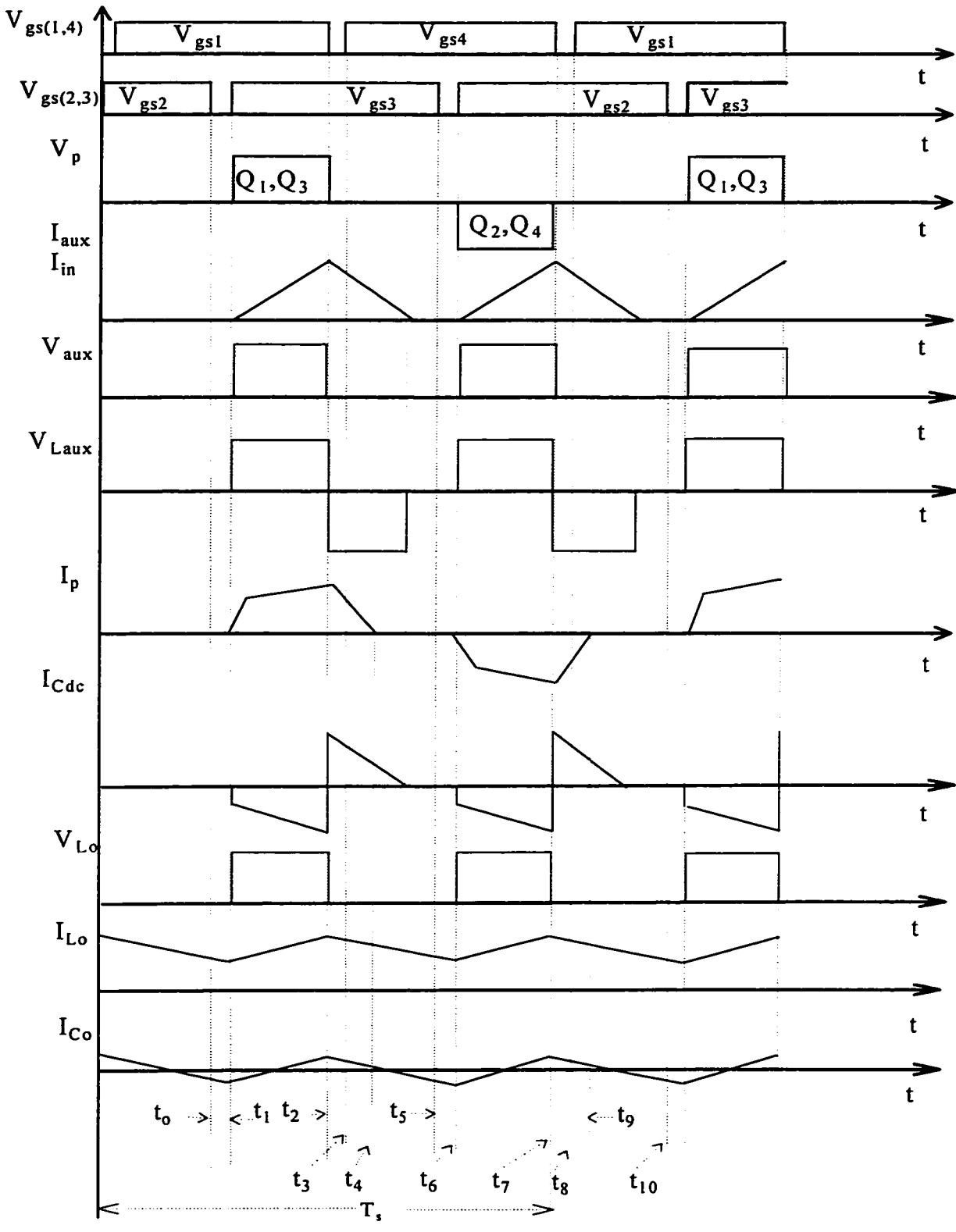


**Fig. 2.2** Operating Waveforms of the converter

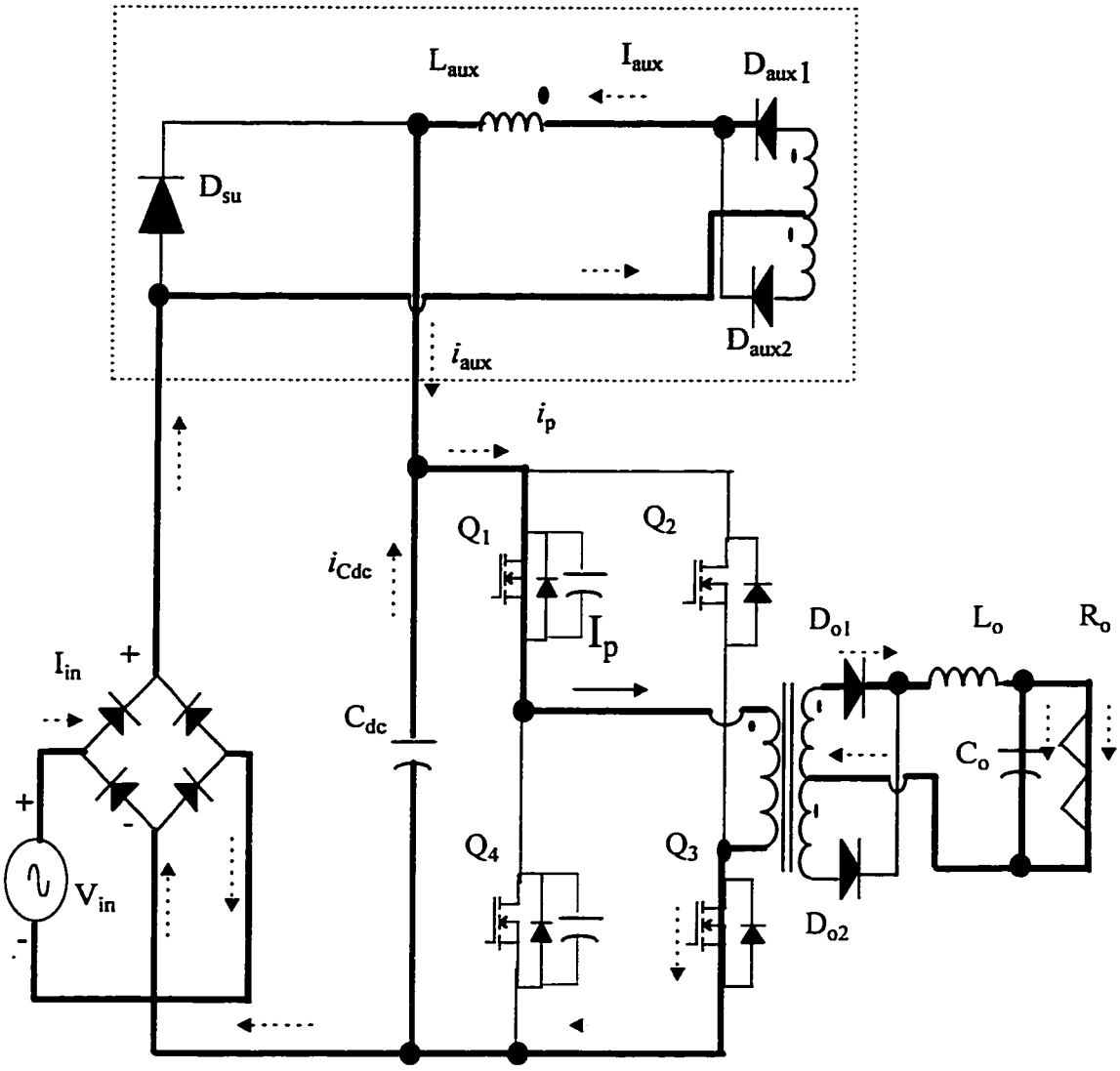


**Fig. 2.3** Mode I, Power Transfer Cycle: $Q_1$ and $Q_3$ are conducting

Conducting Elements: $Q_1$, $Q_3$, $D_{o1}$, $D_{aux1}$

Final Conditions:

$$i_p = \frac{I_o}{n_s} + i_{aux} \tag{2.1}$$

$$v_{ds1} = v_{ds3} = 0$$
$$v_{ds2} = v_{ds4} = V_p \quad (2.2)$$

The primary current is the sum of the reflected load current and the auxiliary current. Auxiliary current is linearly rising until it reaches its peak value. At the end of this interval switch $Q_1$ is turned off at zero voltage.

### 2.4.2 MODE 2, Interval t = [$t_2$, $t_3$]: Left leg Transition

Mode 2 is shown in Fig. 2.4. When $Q_1$ is turned off, the primary current, $i_p$, starts discharging $C_4$ and charging $C_1$ in a linear fashion. At time $t_3$, the voltage across $Q_4$ reaches zero while the voltage across $Q_1$ reaches $V_{dc}$. If $Q_4$ is turned on after $t_3$, then it will turn on at zero voltage, thus reducing the switching losses. The rate of discharge is defined by the MOSFET capacitance and the primary current in the circuit. Thus, at higher load currents it is easy to achieve ZVS. The magnetizing current is assumed to be constant and very small and could be neglected during this interval as any change would be a negligible second-order effect. This mode ends when $D_4$ starts conducting after $v_{ds4}$ had reduced to zero voltage.

Conducting elements: $Q_3$, $C_1$, $C_4$, $D_{o1}$, $D_{o2}$, $D_{aux1}$

Initial conditions: $v_{ds1} = v_{ds3} = 0$

$v_{ds2} = v_{ds4} = V_{dc}$

Final Conditions:

$$t_3 = \frac{(C_1 + C_4)V_{dc}}{i_P} \quad (2.3)$$

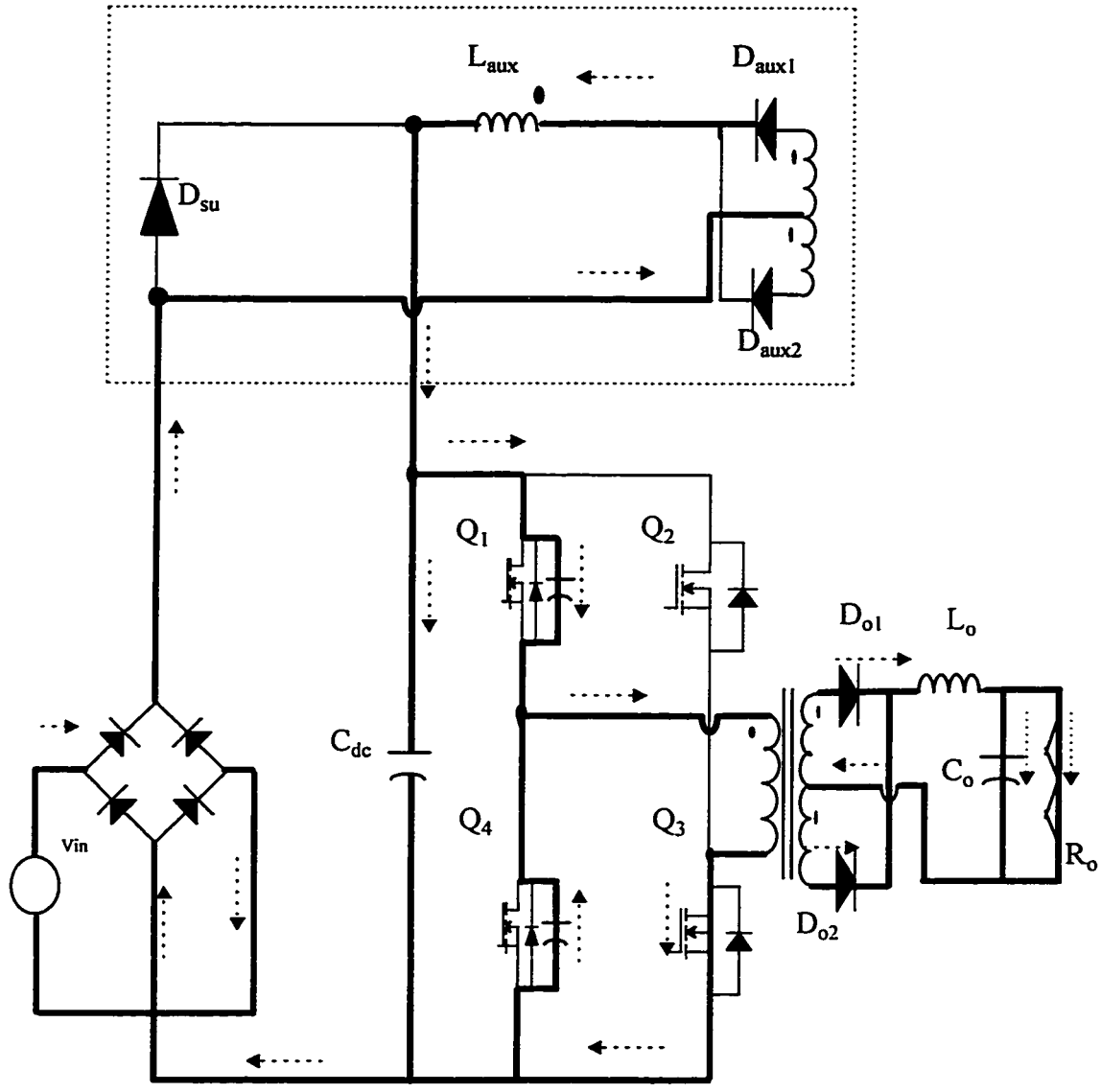


**Fig. 2.4** Mode 2: left leg Transition

State Equations:

$$v_{ds1} = \frac{i_P}{(C_1 + C_4)} t \tag{2.4}$$

$$V_{ds4} = v_p = V_{dc} - v_{ds1} = V_{dc} - \frac{i_P}{(C_1 + C_4)} t \tag{2.5}$$

### 2.4.3 MODE 3, Interval t = [$t_3$, $t_4$]: Primary and Secondary Free-wheeling

This mode starts with $v_{ds4}$ going to zero and $D_4$ turning on. During this mode, the primary current free-wheels through $Q_3$ and $D_4$. All variables remain unchanged during this interval. Switch $Q_4$ can be turned on at zero voltage at any time during this interval. Turning $Q_4$ on will divert the current from $D_4$ to $Q_4$. The voltage across the primary is zero. The load current also free-wheels through the shorted secondary winding. Fig. 2.5 demonstrates the events during this mode.

Conducting elements: $Q_1$, $D_2$ / $Q_2$, $D_{o1}$, $D_{o2}$, $D_{aux1}$

Initial conditions:

$$v_{ds1} = v_{ds2} = V_{dc} \text{ and } v_{ds3} = v_{ds4} = 0$$

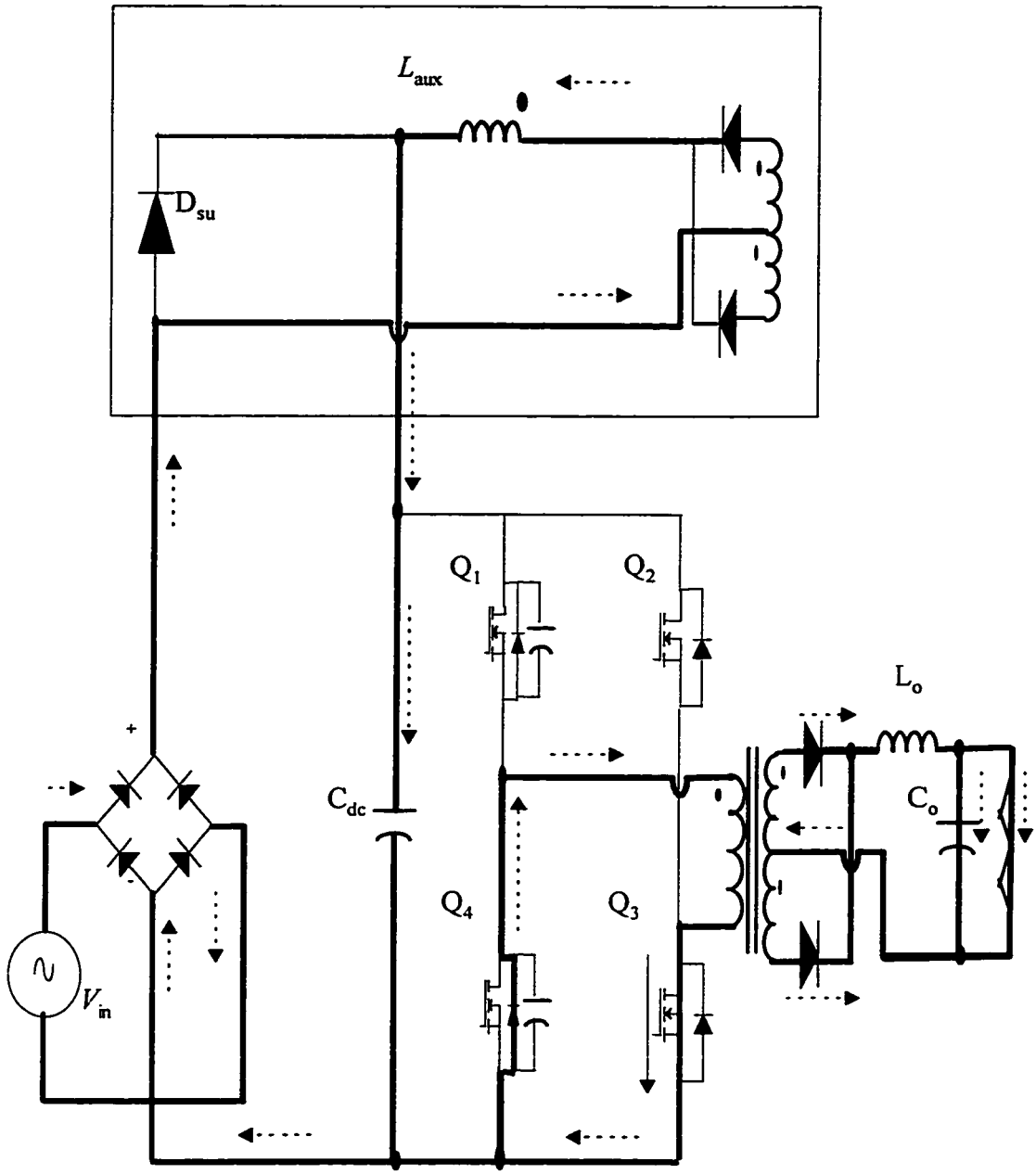


**Fig. 2.5** Mode 3: Primary freewheeling

### 2.4.4 MODE 4, Interval $t = [t_4, t_5]$: Primary Current is zero, $I_{aux}$ is charging $C_{dc}$

This mode starts when no switch is conducting and primary voltage and current are zero. The auxiliary current will charge the dc link capacitor. Secondary is freewheeling. Mode 4 is shown in Fig 2.6

Conducting Elements: $D_{o1}$, $D_{o2}$, $D_{aux1}$

$$v_{ds1} = v_{ds2} = V_{dc}$$

$$v_{ds3} = v_{ds4} = V_p = 0$$

Final Conditions: $v_{ds4} = 0$, $v_{ds1} = V_{dc}$

### 2.4.5 Mode 5, Interval $t = [t_5, t_6]$: Turning on $Q_2$ at zero current

At instant $t = t_6$, $Q_2$ is turned on at zero current as the current ramps slowly due to leakage and auxiliary inductance and the voltage across the drain to source of $Q_2$ becomes zero.

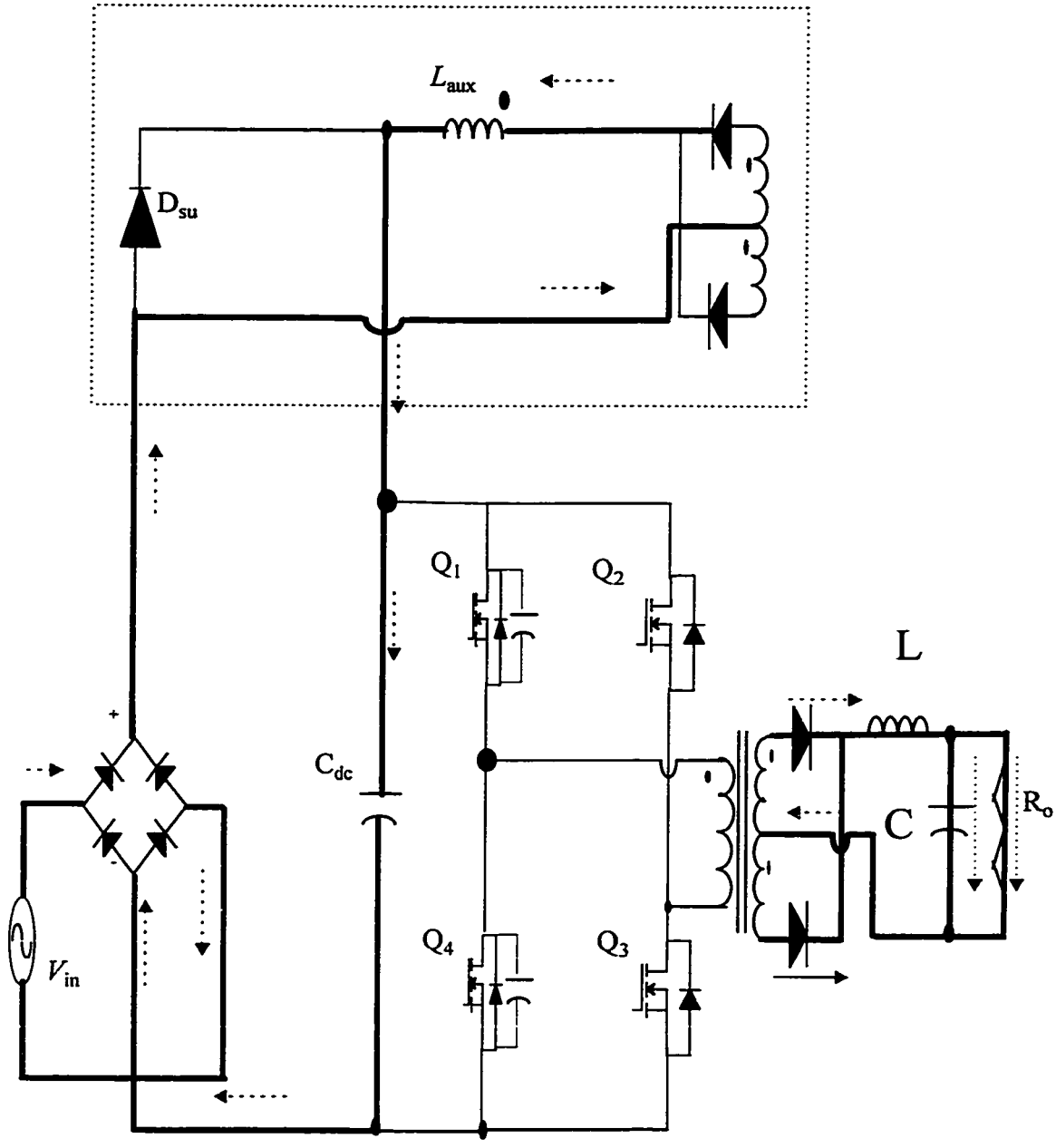


**Fig. 2.6** Mode 4: Zero primary current

### 2.4.6 Mode 6, Interval t = [$t_6$, $t_7$]: Power Cycle, Linear Current Ramping

During this mode, the primary current ($i_p$) falls down linearly and goes negative. Once the current reverses direction, (assuming $Q_4$ has been turned on by then) the circuit remains in this mode until the primary current can support the load current through $D_{o1}$. At this point, $D_{o2}$ turns off, $Q_4$ and $Q_2$ conduct and the dc link voltage appears across the primary winding of the transformer. The circuit representing this mode is shown in Fig. 2.7

Conducting Elements: $Q_2$, $Q_4$, $D_{o2}$, $D_{aux2}$

$$v_{ds1} = v_{ds3} = V_{dc}$$

$$v_{ds2} = v_{ds4} = V_p = 0$$

Final equations:

$$i_L = \frac{-I_o}{n_s} + i_{aux} \tag{2.6}$$

$$V_p = -V_{dc}$$

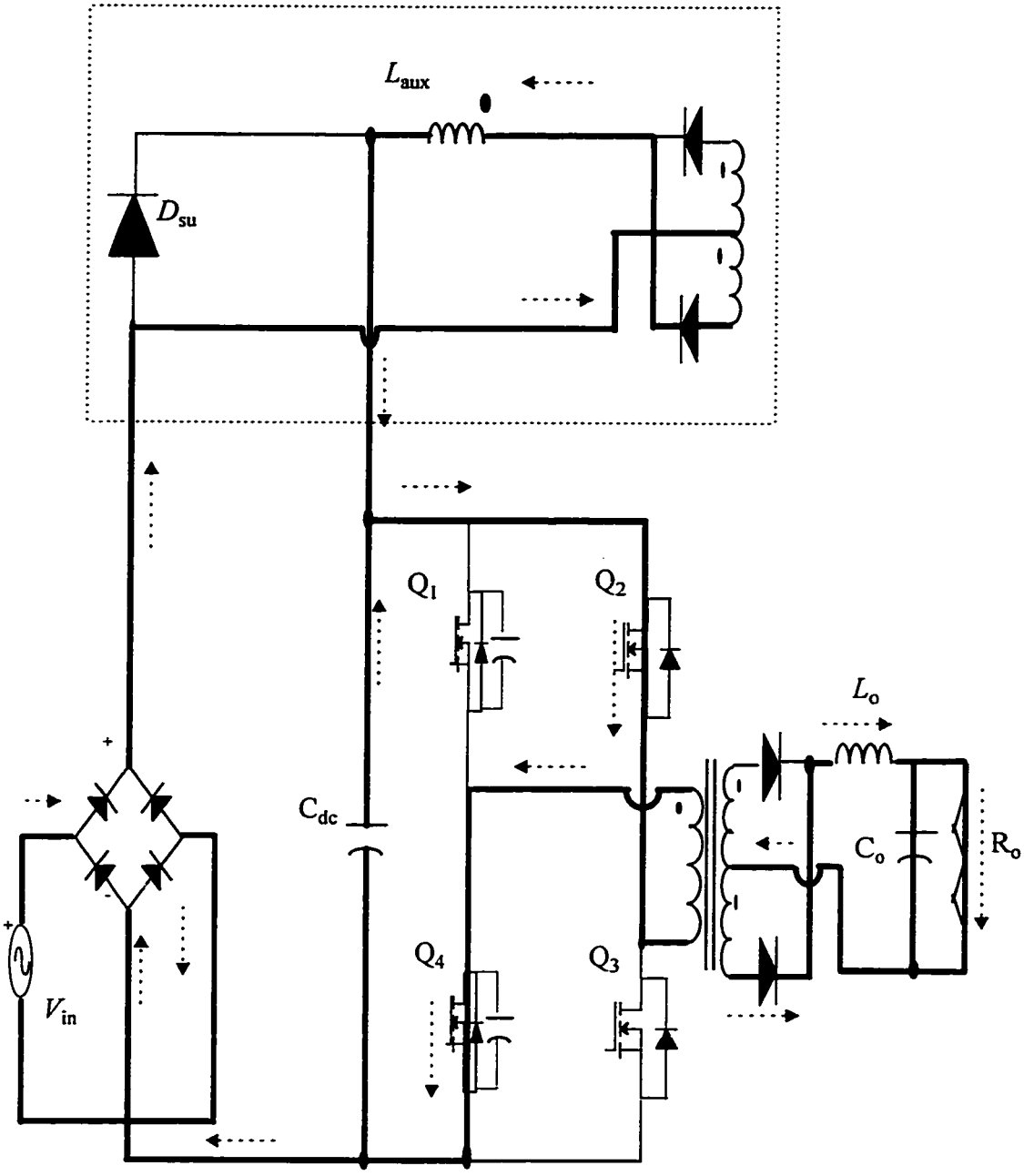


**Fig. 2.7** Mode 6: Linear Current Ramping

### 2.4.7 Mode 7, Interval $t = [t_7, t_8]$: Transition of the left leg, $Q_4$ turn off.

At instant $t = t_7$, $Q_4$ is turned off at zero voltage, $C_1$ is discharged to zero volts and $C_4$ is charged to $V_{dc}$. After this instant $Q_1$ can be turned on at zero voltage. Fig. 2.8 shows the circuit during this mode of operation

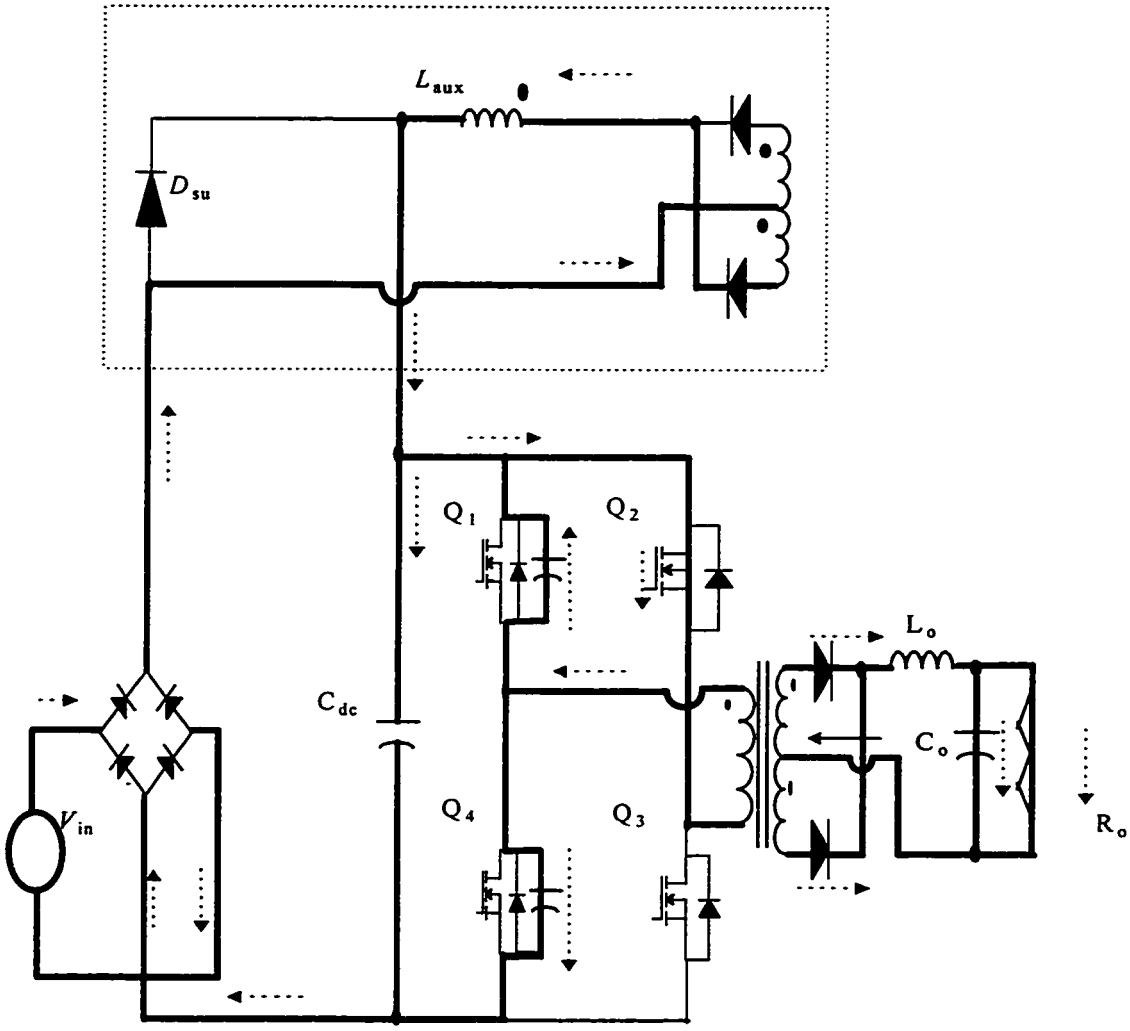


**Fig. 2.8** Mode 7, left leg transition

### 2.4.8 Mode 8, Interval t = [$t_8$, $t_9$]: $Q_1$ turn on

At instant t = $t_8$, $Q_1$ is turned on at ZV as $C_1$ was fully discharged. $D_1$ and $Q_2$ are conducting during this interval which is similar to mode 3. This mode is shown in Fig. 2.9.

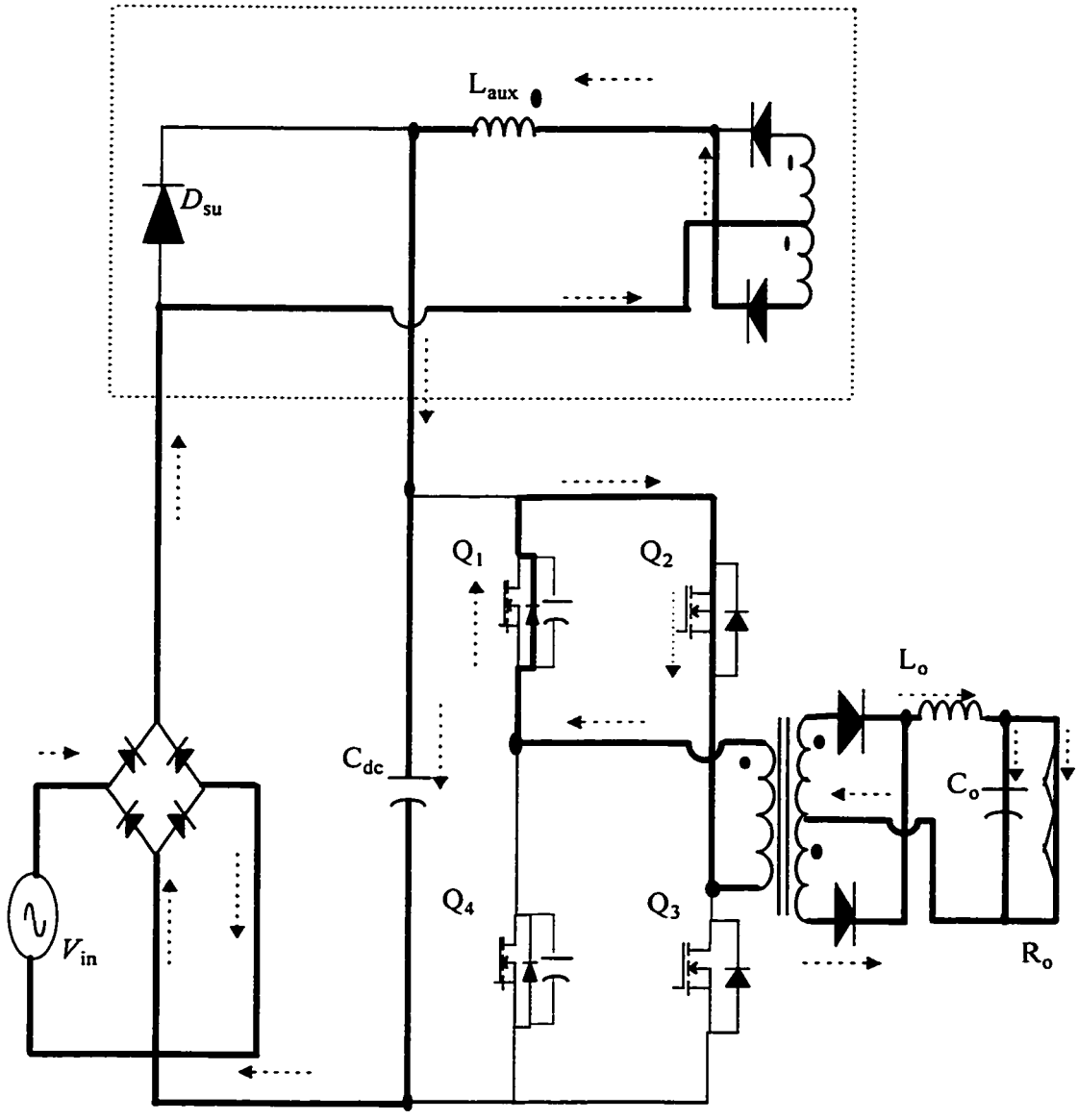


**Fig. 2.9** Mode 8 - t = [$t_8$, $t_9$]

### 2.4.9 Mode 9, Interval $t = [t_9, t_{10}]$: $Q_2$ turn off

At instant $t = t_{10}$, switch $Q_2$ is turned off at zero current (ZC). This mode is similar to mode 4 with zero primary current and auxiliary current charging the dc bus capacitor. This mode ends when $Q_2$ is turned off and a complete cycle of operation ends at this point.

## 2.5 Losses During Switching Operation

As was seen from the analysis of various modes of operation presented in section 2.3, the left leg switches are switched with zero voltage and those of the right leg with zero current.

The peak auxiliary current plays an important role in zero voltage switching as when one of the left leg switches turns off, its capacitor starts charging and the capacitor of the other switch in the same leg starts discharging. If the voltage becomes zero before the switch is turned on, then we achieve zero voltage switching, if not switching will be with some losses.

The energy stored in the auxiliary and leakage inductors at the time when $Q_1$ is turned off should be equal to or greater than the energy stored in the output capacitance of the switch.

$$\frac{1}{2}(C_{ds} + C_{sn})V_{dc}^{\ 2} \leq \frac{1}{2}(L_{aux} + L_{leak})i_p^{\ 2} \tag{2.7}$$

As the leakage inductance is very small compared to the auxiliary inductance, it is ignored in later discussions. Also, as we consider the most severe conditions for

switching ( with maximum losses), which occur close to no load condition, the primary current will be equal to the auxiliary current.

The auxiliary current is ac modulated, as shown in Fig. 2.10, so at the beginning of line frequency it has smaller values.

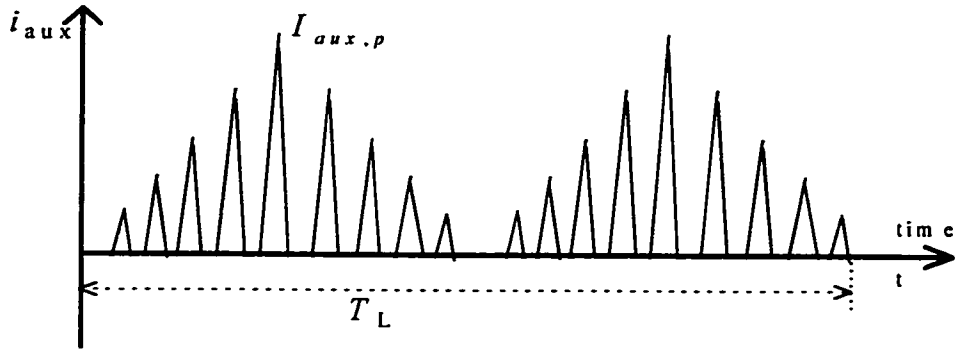


**Fig. 2.10** Current through the auxiliary inductor

The instantaneous value of the auxiliary current in each n-th auxiliary current period

$$i_{aux,n} = I_{aux,p} Sin\left(\frac{nT_s/2}{T_L} 2\pi\right) \tag{2.8}$$

where $V_{dc}$ is the dc link voltage which appears across the primary and any switch of the full bridge when it is off.

$T_L$ is the line frequency period.

$T_s$ is the a period of switching frequency, and $\frac{T_s}{2} = T_s'$ is a period of the auxiliary current and equal to half a switching period.

The peak auxiliary current $I_{aux,p}$ is written as:

$$I_{aux,p} = \frac{V_{s,\max}}{L_{aux}} \frac{DT_s}{2} \tag{2.9}$$

Replacing $\left(C_{ds} + C_{sn}\right)$ by $C_1$ and $i_p$ by $i_{aux}$ in (2.7) yields

$$\frac{1}{2} C_1 V_{dc}^{\ 2} \leq \frac{1}{2} \left(L_{aux} + L_{leak}\right) i_{aux}^{\ 2} \tag{2.10}$$

For known values of inductance, capacitance and dc link voltage, the minimum required current for fully discharging the capacitance is calculated as:

$$i_{aux,\min} \geq \sqrt{\frac{4C_1}{L_{aux}} V_{dc}^{\ 2}} \tag{2.11}$$

When the instantaneous value of the auxiliary current ($i_{aux,n}$) is less than $i_{aux,\min}$ for the whole line period, then switching losses exist and are expressed as:

$$P_{sw,loss} = \frac{1}{2} C_1 V_{dc}^{\ 2} f_{sw} \tag{2.12}$$

This is valid in case the auxiliary current is less than the minimum during the whole line frequency period, otherwise only a portion of these losses exist whenever $i_{aux,n} < i_{aux,\min}$.

The value of the losses could be approximated by the following expression:

$$P_{sw,loss} = \frac{1}{2} C_1 V_{dc}^{\ 2} f_{sw} \frac{\left(\sin^{-1}\left(\frac{i_{aux,n}}{i_{aux,\min}}\right)\right)}{\pi / 2} \tag{2.13}$$

## 2.6 Conclusions

This chapter presented the topological modes of operation of the proposed converter circuit. In each switching frequency period, nine distinctive modes were explained. It is noted that the left leg switches have ZV turn on and turn off, a small snubber capacitor is added to achieve ZVS at turn off if the parasitic capacitance value is not enough. Due to the presence of the auxiliary inductor, the right leg switches have a natural ZCS at both turn on and turn off.

The following conclusions about the switching losses are made: when operating at full load, the $1/2CV^2$ losses negligible, but at light loads these losses tend to increase depending on the amount of peak energy stored in both the leakage and auxiliary inductors, whether it is enough to discharge the switch output capacitance before it turns on. This is the case for the left leg switches, but the right leg switches always have $1/2CV^2$ losses.

# CHAPTER 3

# STEADY STATE ANALYSIS OF THE CIRCUIT FOR CONTINUOUS OUTPUT CURRENT

## 3.1 Introduction

In this chapter steady state analysis of the single stage power factor corrected converter described in chapter two is presented in detail. This analysis is important to predict steady state performance and to develop necessary equations for the proper choice of converter components.

The steady state analysis is carried out for continuous conduction mode of the output filter inductor (COCM) and the discontinuous conduction mode of the auxiliary inductor (DACM).

The steady state analysis of this converter is more complicated than that of the conventional converters due to the nature of current and voltage waveforms. Some of these waveforms have a switching frequency period ($T_s = 1/f_{sw}$), while others have half switching frequency period ($T_s/2$). This fact complicates the steady state analysis. For example, to obtain the value of the RMS current through the auxiliary inductor, the area under the $I_{aux}$ curve in each cycle is found ( these waveforms repeat in shape, but differ in value or amplitude). Then all these areas are summed and averaged over the line frequency and the square root is taken for this sum.

In this chapter the circuit equations are derived and used to describe the proposed circuit. The schematic shown in Fig 2.1 represents the main power circuit. Simplified

equivalent circuits are used in the analysis as well. Section 3.2 presents the states (intervals) of operation. Section 3.3 shows how to find the turns ratio of the high frequency transformer. In Section 3.4 modes of conduction of the auxiliary current are discussed and its value is found. In Section 3.5 DC link voltage value is found as a function of duty ratio, output load and auxiliary inductance.

Performance characteristics of the converter such as RMS current through the switches, RMS input current, dc link capacitor current, output filter capacitor RMS current, input power factor, total harmonic distortion and the output current ripple are developed in Section 3.6.

## 3.2 States of Operation

The steady state analysis of the circuit is conducted using equivalent simplified circuits and using the following simplifying assumptions:

(1) Magnetizing current is neglected due to the high value of magnetizing inductance.

(2) The rectified line voltage $|V_s|$ is constant during the switching period.

(3) DC link voltage $V_{dc}$ is constant during a switching period.

Circuit operation is better described in terms of the auxiliary current waveform during one cycle of operation, which is equal to half the switching period. The waveform is shown in Fig. 3.1.

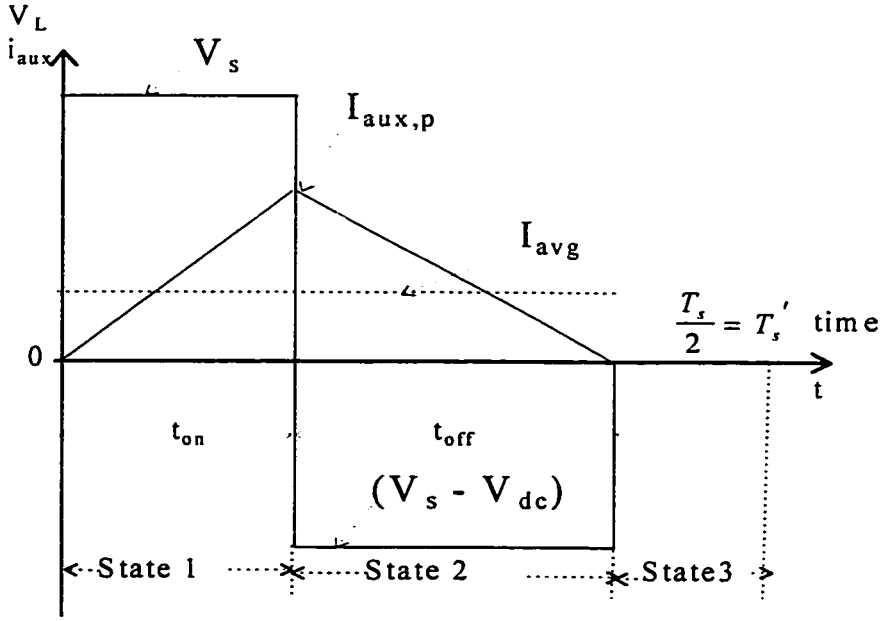


**Fig. 3.1** Auxiliary Current waveform

This waveform clearly shows three states or intervals of operation:

(1) State One: The on-time interval: Linear Rise of the Auxiliary Current- $t_{on}$

(2) State Two: The off-time interval: Linear fall of the Auxiliary Current- $t_{off}$

(3) State Three: The dead-band interval: Auxiliary current is zero- $T_s/2-(t_{on}+t_{off})$

### 3.2.1 State One: Auxiliary Current linearly Rising

In this state current is rising as the net voltage across the inductor is positive. The circuit representing this state is shown in Fig. 3.2. During this interval the operation of the circuit is explained by the following events:

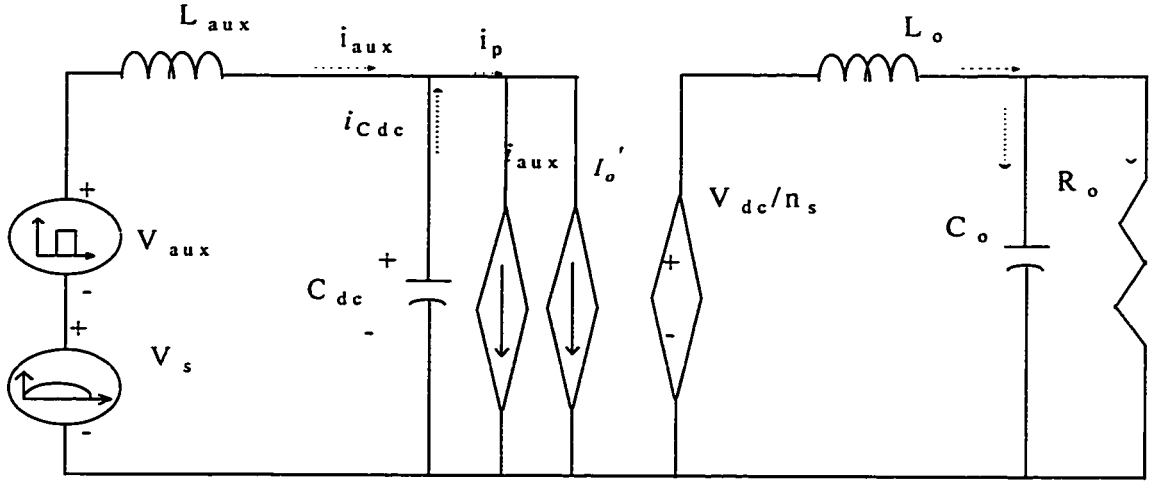


**Fig. 3.2** State One Equivalent circuit- on time

a) Auxiliary current increases linearly with the net positive voltage applied across $L_{aux}$ equal to $|V_s|$ as shown in Fig. 3.3.

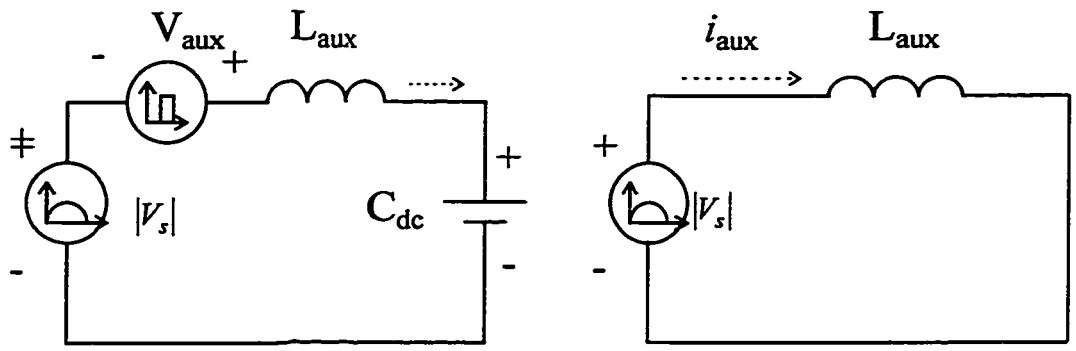


**Fig. 3.3** State one a) Linear Rise of Auxiliary Current

$$V_{aux} = V_{dc}\frac{N_{aux}}{N_p} \tag{3.1}$$

Applying KVL to Fig. 3.3 yields

$$V_{Laux} = |V_s| + V_{aux} - V_{dc} \tag{3.2}$$

Assuming $N_{aux} = N_p$

In a power transfer cycle, during first state $V_{aux}$ equals $V_{dc}$ and they cancel each other as they have different signs, this yields

$$V_{Laux} = |V_s| \tag{3.3}$$

and the auxiliary current is:

$$i_{aux} = \frac{|V_s|}{L_{aux}}.t_{on} \tag{3.4}$$

b) Primary current is the sum of auxiliary current and load current reflected to the primary.

$$i_p = I_o^{'} + i_{aux} \tag{3.5}$$

Also the primary current is the sum of the auxiliary inductor current and the dc link capacitor current:

$$i_p = i_{Cdc} + i_{aux} \tag{3.6}$$

By equating the two expression for the primary current (3.5) and (3.6)

$$i_{Cdc} + i_{aux} = I_o' + i_{aux} \tag{3.7}$$

By eliminating $i_{aux}$ from both sides, (3.7) becomes

$$i_{Cdc} = I_o' \tag{3.8}$$

This means that in this state the load draws the current from the dc link capacitor $C_{dc}$ and discharges it.

c) Power is transferred to the load as a voltage is applied across the primary. This voltage is transferred to the secondary and then rectified. This mode is explained in Fig. 3.4 & 3.5

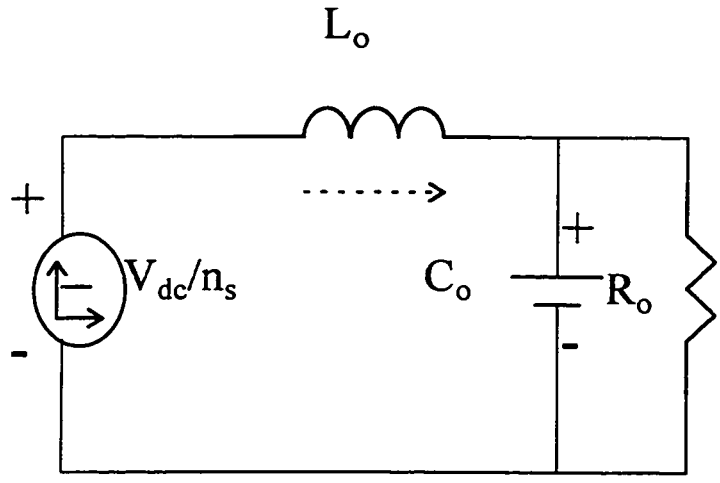


**Fig. 3.4** State one c) Power transfer to the load

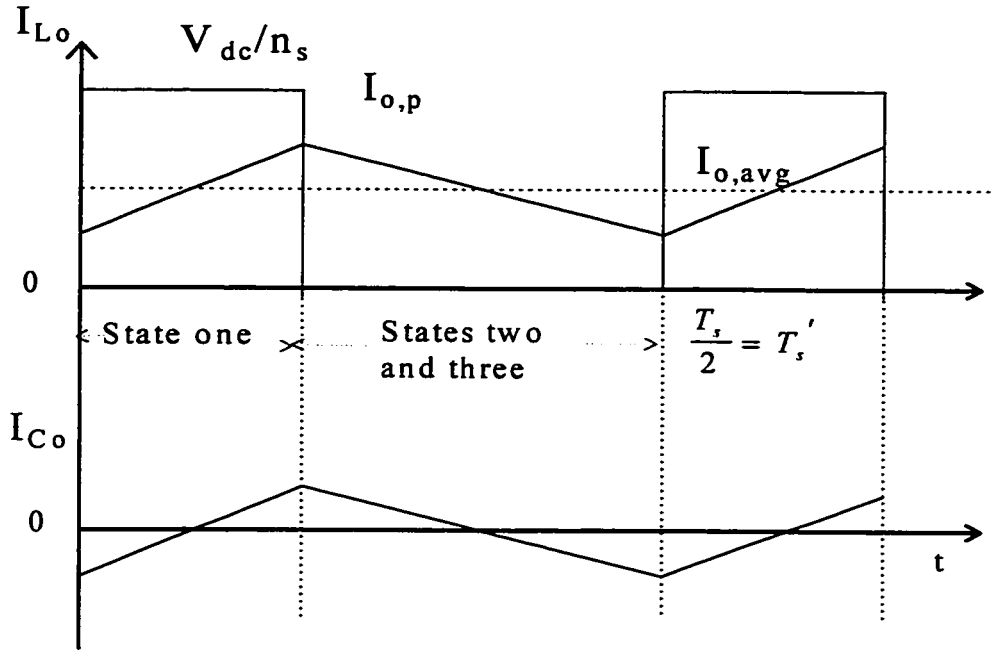


**Fig. 3.5** Output filter inductor and capacitor currents

The duration of this period is the duty cycle

$$D = \frac{t_{on}}{T_s'} \tag{3.9}$$

### 3.2.2 State Two: Auxiliary Current Linearly decreasing

In this state auxiliary current is decreasing (falling) as the net voltage across the auxiliary inductor is negative. The auxiliary voltage is zero and the following events take place:

a) The voltage across $L_{aux}$ is negative dc voltage according to the following considerations

$$V_{Laux} = |V_s| + V_{aux} - V_{dc} \text{ and } V_{aux} = 0$$

$$V_{Laux} = |V_s| - V_{dc} \tag{3.10}$$

The value of the dc link voltage which ensures the discontinuous operation for the auxiliary inductor could be found as follows.

The peak value of the auxiliary current is

$$I_{Laux,p} = \frac{V_s}{L_{aux}} t_{on} \tag{3.11}$$

Also it could be written as

$$I_{Laux,p} = \frac{V_{dc} - V_s}{L_{aux}} t_{off} \tag{3.12}$$

The auxiliary current has to be discontinuous for proper operation of the circuit, so the following relationship has to be satisfied:

$$t_{on} + t_{off} \leq T_s' \tag{3.13}$$

The time scale is normalized to simplify the presentation

$$D = \frac{t_{on}}{T_s'} \tag{3.14}$$

and

$$D' = \frac{t_{off}}{T_s'} \tag{3.15}$$

Substituting (3.14) and (3.15) in (3.13) yields:

$$D + D' \leq 1 \tag{3.16}$$

By equalizing (3.11) and (3.12) and substituting $D' \leq 1 - D$ in these equations, we have

$$\frac{V_s}{L_{aux}} DT_s' = \frac{(V_{dc} - V_s)}{L_{aux}} D'T_s' \tag{3.17}$$

And substituting (3.16) for $D'$ in (3.17) yields

$$V_s D = (V_{dc} - V_s)D' \leq (V_{dc} - V_s)(1 - D) \tag{3.18}$$

Equation (3.18) might be simplified and give the following expression

$$V_{dc} \geq \frac{V_s}{1 - D} \Rightarrow V_{dc} > V_s \tag{3.19}$$

Substituting (3.19) in (3.10) shows that the voltage across $L_{aux}$ during this state is negative and current $i_{aux}$ is decreasing.

2) The dc link capacitor is charged as the auxiliary current flows through it. Current in the secondary is freewheeling through the output diodes and load. At the end of this state auxiliary current becomes zero.

$$i_{aux} = i_{Cdc} \tag{3.20}$$

Fig. 3.6 shows the equivalent simplified circuit representing this state.

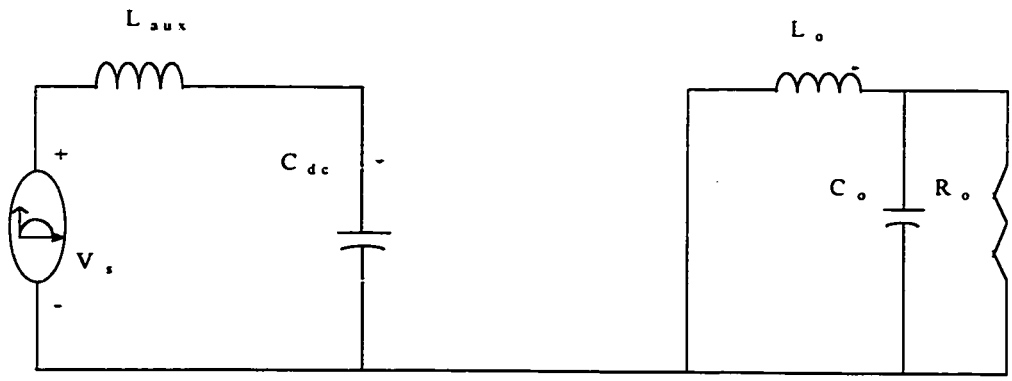


**Fig. 3.6** State Two Equivalent Simplified Circuit

### 3.2.3 State Three: Auxiliary Current is zero [$T_s/2-(t_{on}+t_{off})$]

In this state the auxiliary current is zero as all the energy stored in the auxiliary inductor has been used to charge the dc link capacitor and the net dc voltage across the auxiliary inductor is also zero. The equivalent simplified circuit could be represented as shown in Fig. 3.7.

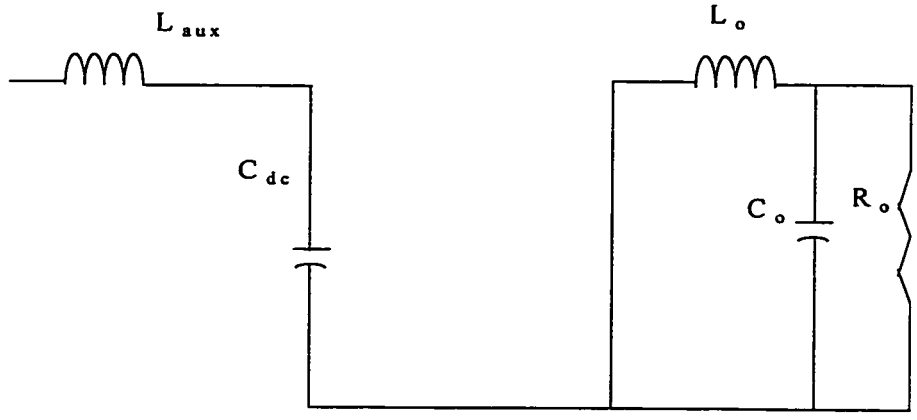


**Fig. 3.7** State Three: Zero auxiliary current

During this state the output current is freewheeling through the output diodes and the load, auxiliary current is zero. This state continues until another power cycle starts.

## 3.3 Turns Ratio of the High Frequency Transformer

The turns ratio of the high frequency transformer is found using the value of minimum input voltage, maximum duty cycle and the rated output voltage.

For proper operation of the circuit the maximum pulse width ($t_{on}$ ) should not exceed 90° which results in a maximum duty cycle of 50% ($D = 2t_{on}$)

$$D=\frac{V_o}{V_{dc}}\frac{N_p}{N_s}=\frac{V_o}{V_{dc}}n_s$$

$$n_s = \frac{DV_{dc}}{V_o} \tag{3.22}$$

Also, the value of dc link voltage is found from (3.19) as

$$V_{dc} = \frac{V_s}{1-D} \tag{3.23}$$

Using these equations the value of the turns ratio of the transformer is found

Example:

$D_{max} = 0.45$

$V_{s,min} = 248.902$ V

$V_o = 50$ V

The value of the dc link voltage is found from (3.23)

$$V_{dc} = \frac{Vs}{1-D} = \frac{248.902}{1-0.45} = 452.55 \text{ V}$$

$$n_s = \frac{DV_{Cdc}}{V_o} = \frac{0.45 * 452.55}{50} = 4.07$$

we chose $n_s = 4$ and the maximum duty cycle becomes:

$$D = \frac{V_o}{V_{Cdc}} n_s = \frac{50}{452.55} 4 = 0.442$$

## 3.4 Modes of Conduction and the Value of the Auxiliary Inductor

### 3.4.1 Value of the Auxiliary Inductor

The dc link capacitor current waveform is shown in Fig. 3.8. This waveform is used to find the value of the auxiliary inductor.

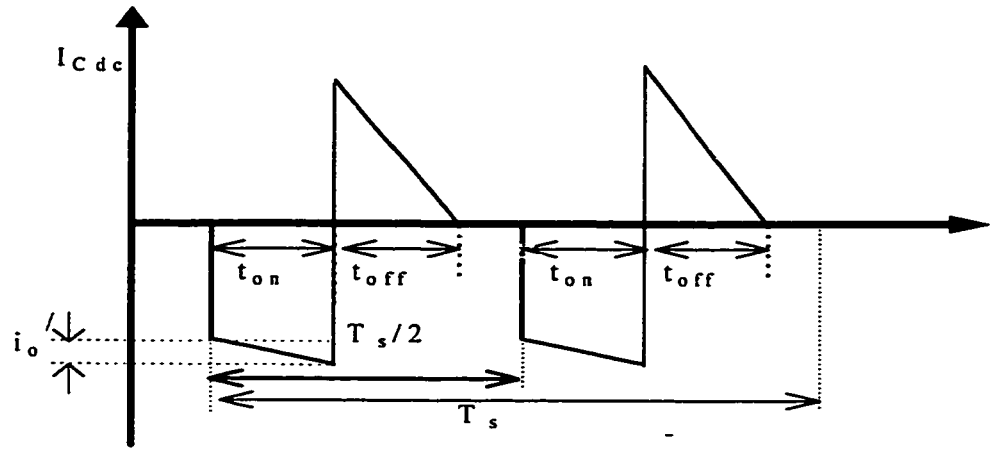


**Fig. 3.8** Dc link capacitor current

It is well known that in steady state the average current through the dc link capacitor is equal to zero. This fact is used to find the value of the auxiliary inductor.

$$i_{Cdc} = \frac{1}{T_L}\int_0^{T_L} i_{Cdc}.dt = 0$$

$$= \frac{1}{T_L}\left(-\sum_{n=1}^{f_{sn}} \frac{DT_S}{2}\frac{V_o}{R_o}\frac{1}{n_s} + \sum_{n=1}^{f_{sn}} \frac{D'T_S}{4}\frac{V_{sn}}{L_{aux}}\frac{DT_s}{2}\right) = 0 \qquad (3.24)$$

Solving equation (3.24), $L_{aux}$ is expressed as:

$$L_{aux} = \frac{R_o}{V_o'}\frac{1}{T_L}\frac{\left(\frac{T_s}{2}D\right)^2}{2}\sum_{n=1}^{f_{sn}} \frac{V_{sn}^{\,2}}{\left(1-V_{sn}/V_{dc}\right)} \qquad (3.25)$$

The value of the inductance as a function of input voltage and switching frequency is plotted in Fig. 3.9

The per unit inductor value could be expressed as:

$$L_{aux} = \frac{24.4\pi}{2\pi f_{sw} R_{o(Rated)}} \qquad (3.25.a)$$

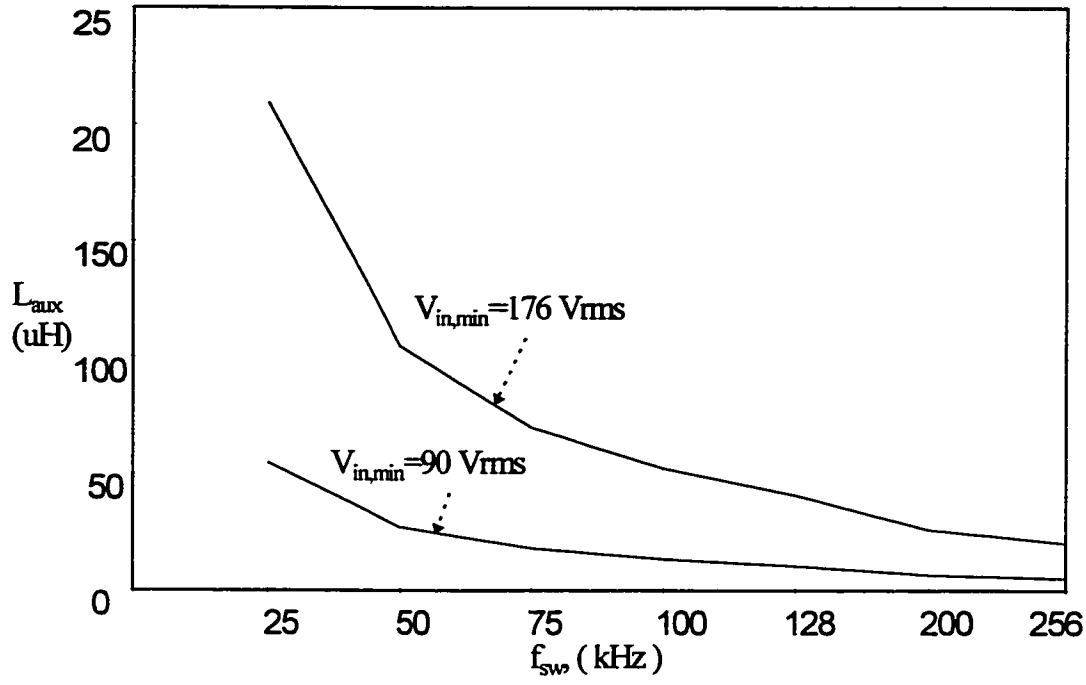


**Fig. 3.9** The value of the auxiliary inductor for different switching frequencies and input voltage levels

### 3.4.2 Modes of Conduction of the Auxiliary Inductor

The auxiliary inductor is a key element in the operation of this circuit, it might even be considered the most important component. As any inductor it might operate in two modes of conduction:

I) Continuous Auxiliary Inductor Conduction Mode (CACM); when there is no time interval where the current passing through it drops to zero. With higher inductance values we operate in CACM.

II) ) Discontinuous Auxiliary Inductor Conduction Mode (DACM), when in some time intervals the current passing through it drops to zero. With lower inductance values we operate in DACM. There is a value of inductance, which gives an operation on the boundary between these two modes.

As was mentioned before, for the proper operation of the circuit we must operate in DACM all the time, independent of the line and load conditions. The inductor should be designed for extreme conditions of low line voltage and full load.

The boundary is drawn using calculations for different input voltage ranges and switching frequencies. It is observed that maximum load and low input voltage are the extreme conditions which define where this boundary occurs.

Fig. 3.10 shows the boundary between these two modes for input voltage range Vin = 85-135 volts.

Fig. 3.11 shows the boundary between these two modes for input voltage range Vin = 176-266 volts.

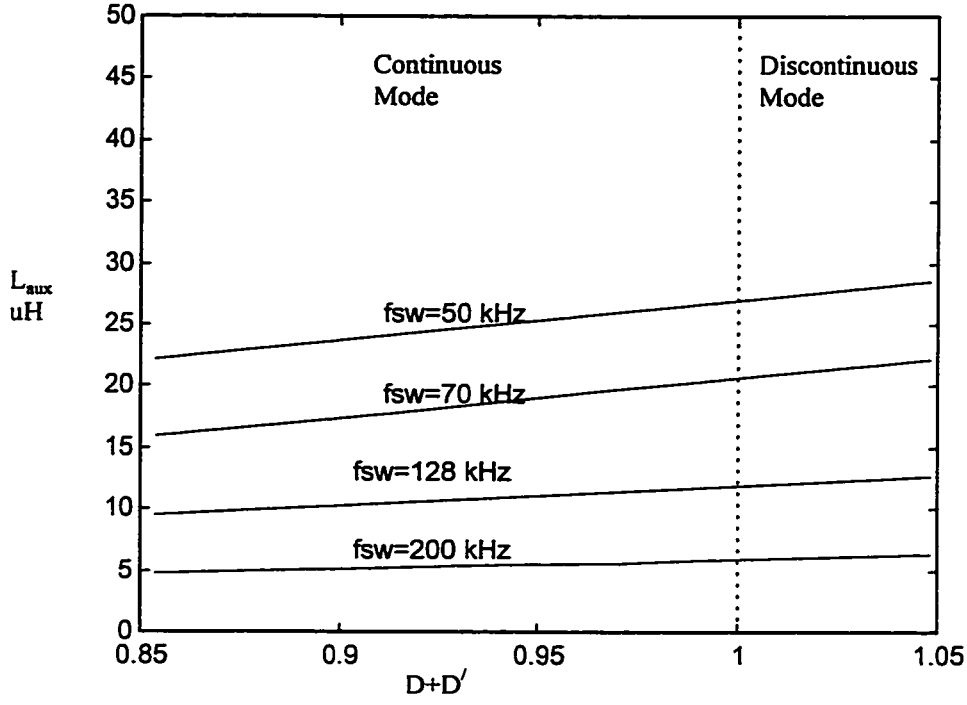


**Fig. 3.10** Boundary of CCM and DCM for $V_{in}$ = 85-135 volts

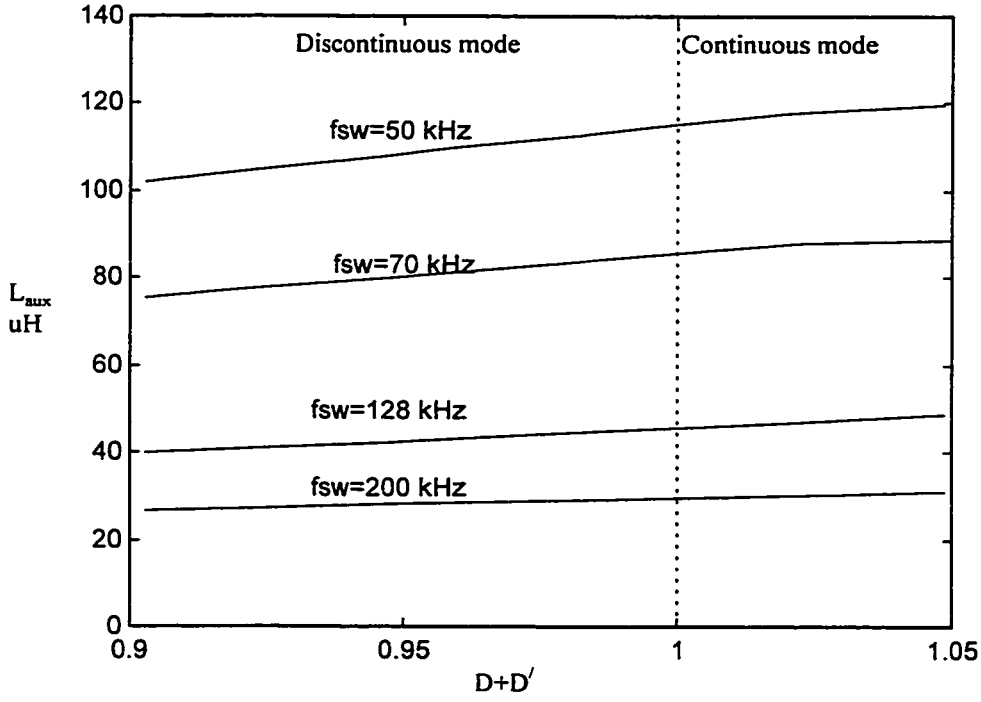


**Fig. 3.11** Boundary of CCM and DCM for $V_{in}$ = 176-266 volts

## 3.5 Dc Link Voltage

The waveforms of the auxiliary current and voltage during a switching period are shown in Fig. 3.12.

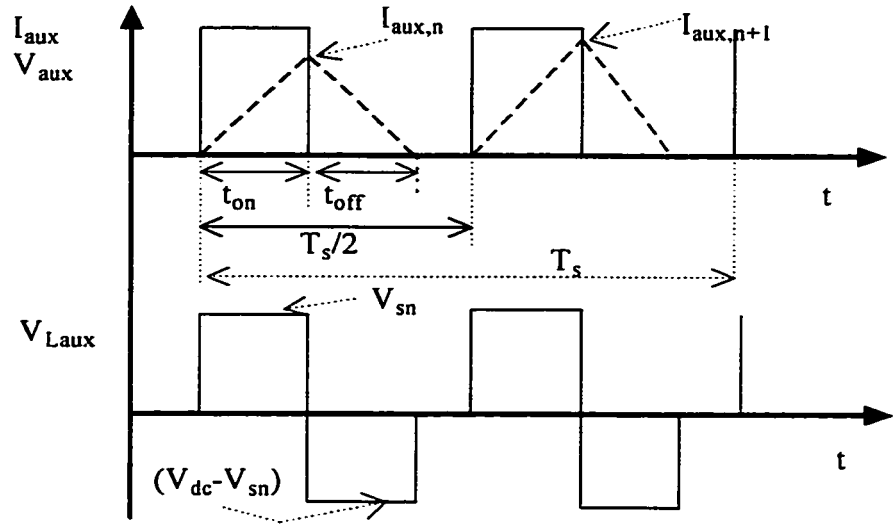


**Fig. 3.12** Current through the auxiliary inductor

The peak current of the auxiliary inductor in each period, 'n', could be expressed as:

$$i_{aux,n} = \frac{V_{sn}}{L_{aux}} t_{on} \tag{3.26}$$

or as:

$$i_{aux,n} = \frac{V_{dc} - V_{sn}}{L_{aux}} . t_{off} \tag{3.27}$$

where

$$t_{on} = \frac{DT_s}{2}. \text{ and } t_{off} = \frac{D'T_s}{2}$$

Where, $V_{sn}$ is the value of line voltage at the beginning of each power transfer cycle.

$$V_{sn} = V_s \sin\left(2\pi.\frac{n}{2T_L/T_s}\right) \tag{3.28}$$

Using equations (3.26) - (3.27) and the energy balance between the average input and output power, the value of the auxiliary inductor could be found. The input power in each half switching cycle could be found as:

$$P_{in,n} = \frac{1}{2L_{aux}}.t_{on}^{\,2}.\left(\frac{(V_{sn})^2}{\left(1-\frac{V_{sn}}{V_{dc}}\right)}\right) \tag{3.29}$$

and the overall average power is found by the summation of all these average power components over a line frequency cycle ($T_L = 1/f_L$ ), where $t_{on}$ - is the power cycle duration and $T_s$ - is the switching frequency.

The output power (averaged over a line frequency cycle) could be expressed as:

$$P_o = \frac{t_{on}^2}{2.T_L.L_{aux}} \sum_{n=1}^{f_{sn}} \left(\frac{V_{sn}^{\,2}}{1-\left(V_{sn}/V_{dc}\right)}\right) \tag{3.30}$$

$$D = \frac{V_o}{V_{dc}} \frac{N_p}{N_s} \tag{3.31}$$

where, D - is the duty cycle, or power transfer period. The value of dc link capacitor voltage and the required duty cycle can be found by solving the equations (3.30) and (3.31) numerically. $V_{dc}$ is a function of load, duty cycle and output current.

## 3.6 Performance Characteristics - Ratings Of The Components

### 3.6.1 RMS Current Through The Switches

The current passing through any of the full bridge switches is the sum of three components:

1. Reflected load current

$$i_o' = \frac{1}{n_s}\left[\frac{V_o}{R_o} + \frac{V_{dc}/n_s - V_o}{L_o}t - \frac{V_{dc}/n_s - V_o}{L_o}\frac{DT_s}{4}\right] \tag{3.32}$$

This expression is valid for continuous current mode of the output filter inductor.

2. Magnetizing current

$$i_M = \frac{V_{dc}}{L_M}t - \frac{V_{dc}}{L_M}\frac{DT_S}{4} \tag{3.33}$$

3. Auxiliary current

$$i_{aux} = \frac{V_{sn}}{L_{aux}}t \tag{3.34}$$

The expression for the switch current is:

$$i_{sw} = i_o' + i_M + i_{aux} \tag{3.35}$$

And its RMS value over a period of $T_S/2$ is found by integrating the expression for $i_{switch}^2$ from 0 to $T_S/2$. This is the RMS current for half a switching period and the RMS switch current is found by averaging all these particular areas over the line frequency period.

$$i_{sw}(t)=\frac{1}{n_s}\left[\frac{V_o}{R}+\frac{V_{dc}/n_s-V_o}{L_o}t-\frac{V_{dc}/n_s-V_o}{L_o}\frac{DT_s}{4}\right]+\frac{V_{dc}}{L_M}t-\frac{V_{dc}}{L_M}\frac{DT_S}{4L_M}+\frac{V_S}{L_S}t \quad (3.36)$$

The following expression is used to find the RMS value of the switch current:

$$I_{sw,rms}=\sqrt{\frac{1}{T_L}\int_o^{T_L} i_{sw}^2(t)dt} \quad (3.37)$$

This expression is valid for the case when the current waveform has an analytical-continuous expression in the line frequency period. In the given topology the switch current consists of a discrete waveform which repeats itself over switching frequency period with a difference in amplitude between each cycle. So the RMS switch current is found by using a modified formula of (3.37)

$$I_{sw,rms}=\sqrt{\frac{1}{T_L}\sum_{n=1}^{f_{sn}}\int_0^{DTs} i_{sw}^2(t)dt} \quad (3.38)$$

where

$f_{sn}=\frac{2T_L}{T_S}$, number of auxiliary current periods in a line frequency period.

$$i_{sw}^2(t)=\left(\frac{1}{n_s}\frac{V_{dc}/n_s-V_o}{L_o}\left[\frac{V_o}{R_o}\frac{L_o}{V_{dc}/n_s-V_o}+t-\frac{dT_s}{4}\right]+\frac{V_{dc}}{L_M}\left(t-\frac{DT_S}{4}\right)+\frac{V_{sn}}{L_{aux}}t\right)^2 \quad (3.39)$$

We know that

$$V_o = \frac{V_{dc}}{n_s} D \tag{3.40}$$

Substituting the expression for the output voltage from (3.40) in (3.41) yields

$$i_{sw}{}^2(t) = \left( \frac{1}{n_s} \frac{V_{dc}/n_s (1-D)}{L_o} \left[ \frac{V_o}{R} \frac{L_o}{V_{dc}/n_s (1-D)} + t - \frac{DT_s}{4} \right] + \frac{V_{dc}}{L_M} \left( t - \frac{DT_S}{4} \right) + \frac{V_{sn}}{L_{aux}} t \right)^2 \tag{3.41}$$

And by integrating (3.41) we obtain

$$\int_0^{DT_s} i_{sw}{}^2(t)dt = \int_0^{DT_s} \left( \frac{1}{n_s} \frac{V_{dc}/n_s (1-D)}{L_o} \left[ \frac{V_o}{R} \frac{L_o}{V_{dc}/n_s (1-D)} + t - \frac{DT_s}{4} \right] + \frac{V_{dc}}{L_M} \left( t - \frac{DT_s}{4} \right) + \frac{V_{sn}}{L_s} t \right)^2 dt$$

$$= \frac{\left[ \left( \frac{1}{n_s} \frac{V_{dc}/n_s (1-D)}{L_o} \left[ \frac{V_o}{R_o} \frac{L_o}{\left( V_{dc}/n_s (1-D) \right)} + t - \frac{DT_s}{4} \right] + \frac{V_{dc}}{L_M} \left( t - \frac{DT_S}{4} \right) + \frac{V_{sn}}{L_{aux}} t \right) \right]^3}{3 \left( \frac{V_{sn}}{L_{aux}} + \frac{V_{dc}}{L_M} + \frac{V_{dc}(1-D)}{n_s{}^2 L_o} \right)} \Bigg|_0^{\frac{DT_s}{2}} \tag{3.42}$$

Expression (3.42) is substituted in (3.38) and the result is used to plot the value of the switch RMS current versus the output load as will be shown in later parts of this thesis.

### 3.6.2 RMS Input Current

The waveform of the input current is shown on Fig. 3.13

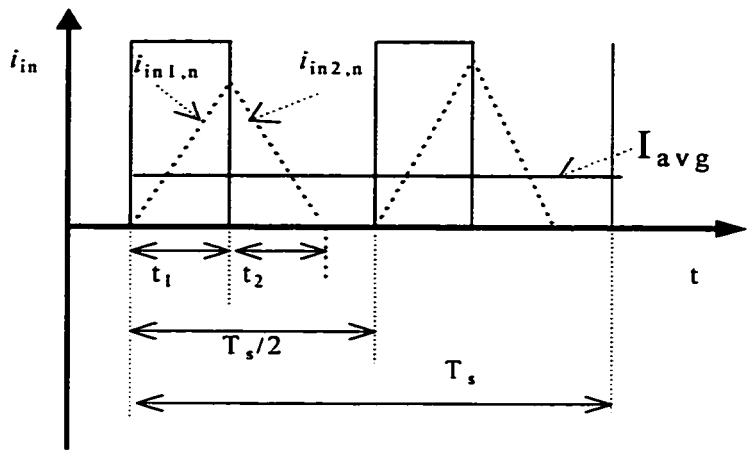


**Fig. 3.13** Input current and auxiliary voltage waveforms

The rms. value of the input current is expressed as

$$I_{in,rms} = \sqrt{\frac{1}{T_L}\int_0^{T_L} i_{in}^2(t)dt} = \sqrt{\frac{1}{T_L}\sum_1^{f_{sw}}\left(\int_0^{DT_s/2} i_{in1}^2(t)dt + \int_0^{D'T_s/2} i_{in2}^2(t)dt\right)} \tag{3.44}$$

The first increasing part of the input current $i_{in1}$ is

$$i_{in1,n}(t) = \frac{V_{sn}}{L_{aux}}t \tag{3.45}$$

and its square is

$$i_{in1,n}^2(t) = \frac{V_{sn}^2}{L_{aux}^2}t^2 \tag{3.46}$$

The corresponding area under this curve is found as

$$\int_0^{DT_S/2} i_{in1}^2 dt = \int_0^{DT_S/2} \left(\frac{V_{sn}}{L_{aux}} t\right)^2 dt = \left(\frac{V_{sn}}{L_{aux}}\right)^2 \frac{t^3}{3}\Big|_0^{DT_S/2} = \left(\frac{V_{sn}}{L_{aux}}\right)^2 \frac{\left(DT_S/2\right)^3}{3} \tag{3.47}$$

The second decreasing part of the input current $i_{in2}$ is

$$i_{in2,n}(t) = \frac{V_{sn}}{L_{aux}} \frac{DT_S}{D'T_S} t = \frac{V_{sn}}{L_{aux}} \frac{D}{D'} t \tag{3.48}$$

The corresponding area under this curve is found as

$$\int_0^{D'T_S/2} i_{in2}(t)^2 dt = \int_0^{D'T_S/2} \left(\frac{V_{sn}}{L_{aux}} \frac{D}{D'} t\right)^2 dt = \left(\frac{V_{sn}}{L_{aux}} \frac{D}{D'}\right)^2 \frac{t^3}{3}\Big|_0^{\Delta_1 T_S/2} = \left(\frac{V_{sn}}{L_{aux}} \frac{D}{D'}\right)^2 \frac{\left(D'T_S/2\right)^3}{3}$$

$$= \left(\frac{V_{sn}}{L_{aux}}\right)^2 \left(\frac{V_{dc} - V_{sn}}{V_{sn}}\right)^2 \frac{\left(D'T_S/2\right)^3}{3} \tag{3.49}$$

where

$$D' = D \frac{V_{sn}}{V_{dc} - V_{sn}} \tag{3.50}$$

Using the following relationship (3.50) in (3.49) yields

$$\int_0^{D'T_S/2} i_{in2,n}^2(t) dt = \left(\frac{V_{sn}}{L_{aux}}\right)^2 \left(\frac{V_{dc}}{V_{dc} - V_{sn}}\right)^2 \frac{\left(DT_S/2\right)^3}{3} \tag{3.51}$$

and the expression for the overall RMS input current before filtering is obtained by substituting (3.47) and (3.51) in (3.44):

$$I_{in,rms} = \sqrt{\frac{1}{T_L} \sum_{n=1}^{L_m} \int_0^{DT_S/2} i_{in,1}^2(t) dt + \int_0^{\Delta_1 T_S/2} i_{in2}^2 dt} \tag{3.52}$$

Using these equations, the current RMS value is plotted in later chapters.

The expression for input current after filtering could be found by averaging the waveform of the current

$$I_{in,avg} = \frac{1}{T_S/2}\int_0^{T_S/2} i_{avg}(t)dt$$

$$= \frac{1}{T_S/2}\frac{(DT_s/2)^2}{2L_{aux}}\frac{V_{sn}}{1-\left(V_{sn}/V_{dc}\right)} \tag{3.53}$$

and the RMS value of this current is found as:

$$I_{in,rms} = \sqrt{\frac{1}{T_L}\sum_{n=1}^{f_{sn}}\left(\frac{1}{T_S/2}\frac{(DT_s/2)^2}{2L_{aux}}\frac{V_{sn}}{1-V_{sn}/V_{dc}}\right)^2} \tag{3.54}$$

### 3.6.3 DC Link Capacitor Current

Based on the waveform of the current passing through the dc link capacitor, shown in Fig. 3.8, during the first period $t_{on} = DT_S/2$ the expression for the current is:

$$i_{Cdc\_1n} = \frac{I_o}{n_s} + \frac{V_{dc}/n_s - V_o}{L_o n_s}t - \frac{V_{dc}/n_s - V_o}{L_o n_s}\frac{DT_S}{4} \tag{3.55}$$

During the second period $t_{off} = D'T_S/2$ the expression for the current is:

$$i_{Cdc\_2n} = \frac{-V_{sn}}{L_{aux}}\frac{2DT_S}{2D'T_S}t + \frac{-V_{sn}}{L_{aux}}\frac{DT_s}{2} = \left(-\frac{V_{dc}-V_{sn}}{L_{aux}}t + \frac{V_{sn}}{L_{aux}}\frac{DT_s}{2}\right) \tag{3.56}$$

The RMS current is defined by the following formula:

$$I_{Cdc,rms} = \sqrt{\frac{1}{T_L}\int_0^{T_L} {i_{Cdc\_n}}^2 dt} \tag{3.57}$$

where,

$$i_{Cdc\_n}{}^2(t) = i_{Cdc\_1n}{}^2(t) + i_{Cdc\_2n}{}^2(t) \tag{3.58}$$

First integrals of both dc capacitor currents in expressions (3.55) and (3.56) are found as:

$$\int_0^{DT_S/2} i_{Cdc\_1n}{}^2 dt = \int_0^{DT_S/2} \left( \frac{I_o}{n_s} + \frac{V_{dc}/n_s - V_o}{L_o n_s} t - \frac{V_{dc}/n_s - V_o}{L_o n_s} \frac{DT_s}{4} \right)^2 dt$$

$$= \frac{1}{3\left( \frac{V_{dc}/n_s - V_o}{L_o n_s} \right)} \left( \frac{I_o}{n_s} + \frac{V_{dc}/n_s - V_o}{L_o n_s} t - \frac{V_{Cdc}/n_s - V_o}{L_o n_s} \frac{DT_S}{4} \right)^3 \Bigg|_0^{DT_S/2}$$

$$= \frac{1}{3\left( \frac{V_{dc}/n_s - V_o}{L_o n_s} \right)} \left\{ \left( \frac{I_o}{n_s} + \frac{V_{dc}/n_s - V_o}{L_o n_s} \frac{DT_S}{4} \right)^3 - \left( \frac{I_o}{n_s} - \frac{V_{dc}/n_s - V_o}{L_o n_s} \frac{DT_S}{4} \right)^3 \right\} \tag{3.59}$$

and the area for the second current component is:

$$\int_0^{D'T_s/2} i_{Cdc\_2n}{}^2 dt = \int_0^{D'Ts/2} \left( -\frac{V_{dc} - V_{sn}}{L_{aux}} t + \frac{V_{sn}}{L_{aux}} \frac{DT_S}{2} \right)^2 dt$$

$$= \frac{1}{3\left( \frac{V_{sn} - V_{dc}}{L_{aux}} \right)} \left( -\frac{V_{dc} - V_{sn}}{L_{aux}} t + \frac{V_{sn}}{L_{aux}} \frac{DT_S}{2} \right)^3 \Bigg|_0^{D'T_s/2}$$

$$= \frac{1}{3\left( \frac{V_{sn} - V_{dc}}{L_{aux}} \right)} \left( \frac{V_{sn}}{L_{aux}} \frac{DT_S}{2} \right)^3 \tag{3.60}$$

where

$$D' = D\frac{V_{dc}}{V_{dc} - V_{sn}} \tag{3.61}$$

The RMS current through the dc link capacitor is:

$$I_{Cdc,rms} = \sqrt{\frac{1}{T_L}\sum_{n=1}^{f_m}\int_0^{DT_S/2} i_{Cdc\_1n}{}^2(t)dt + \int_0^{D'T_s/2} i_{Cdc\_2n}(t)^2 dt} \tag{3.62}$$

### 3.6.4 Output Filter Capacitor RMS Current

The RMS current through the output filter capacitor is a function of the allowed current ripple which is in turn a function of the inductor value. Fig 3.14 shows the theoretical waveforms of the current through the output filter components.

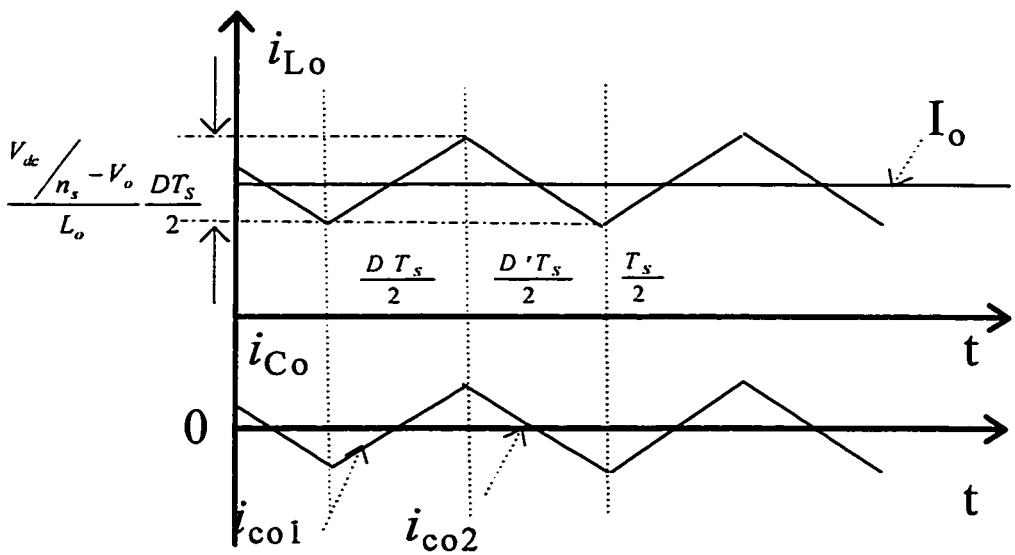


**Fig. 3.14** Current through the output filter components

During the on time interval t = [0, $DT_S/2$] the expression for the output capacitor current is:

$$i_{C_{o\_1}} = \left( \frac{V_{dc}/n_s - V_o}{L_o} t - \frac{V_{dc}/n_s - V_o}{L_o} \frac{DT_S}{4} \right) \tag{3.63}$$

And the area under the square value of this current component is

$$\int_0^{DT_S/4} i_{Co\_1} = \int_0^{DT_S/4} \left( \frac{V_{dc}/n_s - V_o}{L_o} t - \frac{V_{dc}/n_s - V_o}{L_o} \frac{DT_S}{4} \right)^2 dt$$

$$= \frac{1}{3} \left( \frac{\left(V_{dc}/n_s - V_o\right)}{L_o} t - \frac{\left(V_{dc}/n_s - V_o\right)}{L_o} \frac{DT_S}{4} \right)^3 \cdot \frac{1}{\frac{\left(V_{dc}/n_s - V_o\right)}{L_o}} \Bigg|_0^{DT_S/4}$$

$$= \frac{2}{3} \left( \frac{\left(V_{dc}/n_s - V_o\right)}{L_o} \frac{DT_S}{4} \right)^3 \frac{L_o}{\left(V_{dc}/n_s - V\right)_o} \tag{3.64}$$

During the remainder of the half switching period, t = [0, $(1-D)T_S/4$], the expression for the output capacitor current is:

$$i_{C_{o\_2}} = \left( \frac{-V_o}{L_o} t + \frac{V_o}{L_o} \frac{(1-D)T_S}{4} \right) \tag{3.65}$$

and the area under the square value of this current component is

$$= \int_0^{(1-D)T_S/4} \left( \frac{-V_o}{L_o} t + \frac{V_o}{L_o} \frac{DT_S}{4} \right)^2 dt$$

$$= \frac{1}{3}\left(\frac{-V_o}{L_o}t + \frac{V_o}{L_o}\frac{(1-D)T_S}{4}\right)^3 \frac{1}{\frac{-V_o}{L_o}}\Bigg|_0^{(1-D)T_S/4}$$

$$= \frac{1}{3}\left(\frac{-L_o}{V_o}\right)\left(\frac{V_o}{L_o}\frac{(1-D)T_S}{4}\right)^3 \tag{3.66}$$

and the overall RMS current of the output filter capacitor is

$$I_{co\_rms} = \sqrt{\frac{1}{T_L}\left[\int_0^{DT_S/4} i_{Co\_1}(t)dt + \int_0^{(1-D)T_S/4} i_{Co\_2}(t)dt\right]} \tag{3.67}$$

### 3.6.5 Output Filter Inductor And Current Ripple

The output voltage is expressed in terms of the dc link voltage and the duty cycle

$$V_o = \frac{V_{dc}}{n_s}D \tag{3.68}$$

The current ripple of the output filter inductor was shown in Fig. 3.5 and equals

$$\Delta i_{Lo} = \frac{V_{dc}/n_s - V_o}{L_o}\frac{DT_S}{2} = \frac{\frac{V_{dc}}{n_s} - \frac{V_{dc}}{n_s}D}{L_o}\frac{DT_S}{2}$$

$$= \frac{V_{dc}/n_s(1-D)}{L_o}\frac{DT_S}{2} \tag{3.69}$$

Also,

$$\Delta i_{L_o} = \frac{V_o(1-D)}{L_o}\frac{DT_S}{2} \tag{3.70}$$

and the ripple factor is defined as:

$$K_{ripple\cdot} = \frac{\Delta i_{L_o}}{I_o} = \frac{V_o(1-D)}{I_o L_o}\frac{T_S}{2} = \frac{V_o^2(1-D)}{P_o L_o}\frac{T_S}{2} \tag{3.71}$$

The value of the output filter inductor is found for a given ripple factor by solving (3.71)

$$L_o = \frac{V_o^2(1-D)}{P_o K_{ripple}}\frac{T_S}{2} \tag{3.72}$$

### 3.6.6 Output Voltage Ripple

The output voltage ripple is found to be

$$\Delta V_{C_o} = \frac{\left(T_S/2\right)^2(1-D)}{8L_o C_o} \tag{3.73}$$

Then for a known value of allowed voltage and current ripple, the output filter capacitor is found from (3.73)

### 3.6.7 Input Power Factor

The input power factor is defined as the turns ratio of the real power to the apparent input power. As was assumed in previous sections if the system has 100 % efficiency and the apparent input power equals the average output power, then power factor could be expressed as:

$$pf = \frac{P_o}{V_{s,rms\cdot} I_{in,rms}} = \frac{V_o . I_o}{V_{s,rms\cdot} I_{in,rms}} \tag{3.74}$$

All variables in equation (3.73) could be defined either from circuit specification or the performance characteristics of the circuit, as in the case of the input RMS current defined in section 3.5.2.

### 3.6.8 Total Harmonic Distortion

Total harmonic distortion is represented by the following expression

$$THD = \sqrt{\frac{1}{pf^2} - 1}.100\ \% \tag{3.75}$$

## 3.7 Conclusions

The steady state analysis of the proposed converter have been performed in this chapter. The operation of the circuit was described based on three States of operation of the converter. A method for calculating the auxiliary inductance, turn ratios of the high frequency transformer, RMS currents in the circuit, and the DC link voltage value have been presented. It is concluded that the DC link Voltage value is load dependent for the COCM and varies in a wide range of 5 to 1 from 10 % to 100% load. This is why the use of this converter in this mode is recommended for operation from input line voltage of (85-135) V, while operating from 30-100 % rated load.

# CHAPTER 4

# STEADY STATE ANALYSIS OF THE CIRCUIT FOR DISCONTINUOUS OUTPUT CURRENT

## 4.1 Introduction

In Chapter 3 the operation of the circuit was analyzed for continuous output current mode. This operation leads to a variable dc link voltage depending on the load. A high value of dc link voltage leads to higher ratings of the full bridge switches. A good compromise (solution) to this problem is to operate with discontinuous output current while keeping the auxiliary inductor in discontinuous operation

Discontinuous output current mode (DOCM) results in lower dc link voltage and makes it load independent. Also, a mixed mode of operation is possible where the converter is operated in continuous output current mode (COCM) at high loads, as the dc voltage level is lower, and in DOCM at light loads when high dc link voltage occurs.

Section 4.2 provides some important facts about the steady state analysis for Continuous output current mode. In Section 4.3 the steady state analysis is performed for output current in discontinuous mode. This mode enables us to reduce the dc link voltage level and consequently the voltage ratings of the full bridge switches. The value of the critical inductance which enables operation in DOCM for a given output power level is derived.

The performance characteristics of the converter are affected by this mode of operation (DOCM) and the new performance characteristics are presented in Section 4.4,

where the RMS values of currents through the switches, the dc link and output capacitors. Also, the expression for the output voltage ripple is derived for DOCM.

Comparative plots showing some of the performance characteristics for these two modes of operation is presented in section 4.5.

## 4.2 Summary of Steady State Analysis for DACM and COCM

The full steady state analysis for COCM was presented in chapter three, here we only mention some important facts. The waveform of the auxiliary current and voltage during a switching period were shown in Fig. 3.12.

The peak current through the auxiliary inductor in the n-th switching period is expressed as:

$$I_{aux,n} = \frac{V_{sn} + n_{aux}V_{dc} - V_{dc}}{L_{aux}}.t_{on} = \frac{V_{dc} - V_{sn}}{L_{aux}}.t_{off} \tag{4.1}$$

Where, $V_{sn}$ is the value of line voltage at the beginning of each power transfer cycle.

$$V_{sn} = V_s \sin\left(2\pi \frac{n}{2T_L / T_s}\right) \tag{4.2}$$

Using equations (4.1) - (4.3) and the energy balance between the average input and output powers, the value of the auxiliary inductor could be found. The power in each half switching cycle could be found as:

$$P_o = \frac{n_{aux}}{2L_{aux}} . t_{on}^{\ 2} . \left( \frac{V_{sn} . \left( V_{sn} + n_{aux} V_{dc} - V_{dc} \right)}{1 - \frac{|V_{sn}|}{V_{dc}}} \right) \tag{4.3}$$

where, $t_{on}$ is the power cycle duration and $T_s$ is the switching frequency.

The output power (averaged over a line frequency cycle) could be expressed as:

$$P_o = \frac{n'_{aux}}{L_{aux} T_L} \frac{(DT_s / 2)^2}{2} \sum_{n=1}^{f_{sn}} \frac{V_{sn} . \left( V_{sn} + n'_{aux} V_{dc} - V_{dc} \right)}{1 - \frac{|V_{sn}|}{V_{dc}}} \tag{4.4}$$

$$D = \frac{V_o}{V_{dc}} n'_s \tag{4.5}$$

where D is the duty cycle, or power transfer period.

$n'_s = \frac{1}{n_s} = \frac{N_s}{N_p}$ is the turns ratio of the secondary winding.

$n'_{aux} = \frac{1}{n_{aux}} = \frac{N_{aux}}{N_p}$ is the turns ratio of the auxiliary winding.

The value of dc link capacitor voltage and the required duty cycle can be found by solving the equations (4.4) and (4.5) numerically. $V_{dc}$ is a function of load, duty cycle and input current.

## 4.3 Steady State Analysis For DACM And DOCM

As a starting point for the analysis, we consider the operation at the edge of continuous output current mode (COCM) and discontinuous output current mode (DOCM). The current and voltage waveforms are shown in Fig. 4.1.

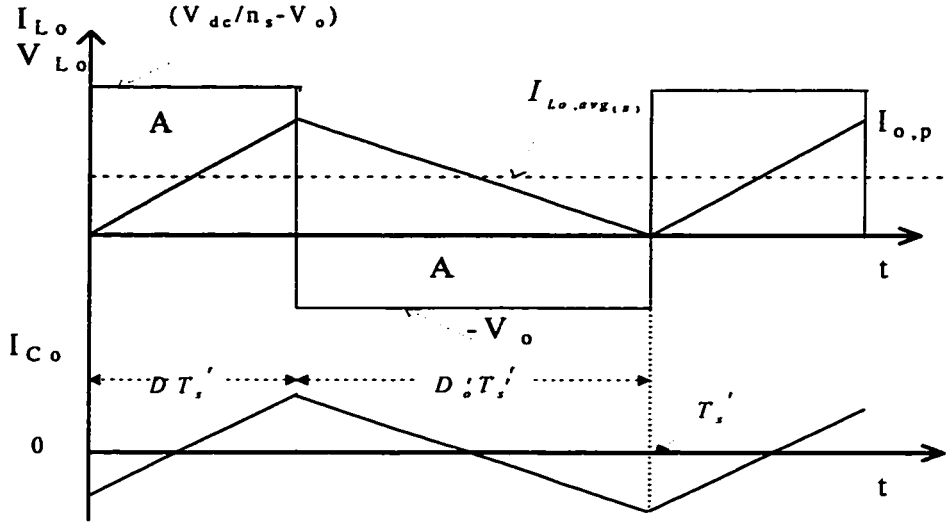


**Fig. 4 1** Output filter current and voltage waveforms for operation at the edge of COCM and DOCM

The peak value of the ac current component $I_{o,p}$ is

$$I_{o,p} = \frac{\left(V_{dc}/n_s - V_o\right)}{L_o} DT_s' = \frac{A}{L_o} \tag{4.6}$$

where A is the voltage-time integral of the positive (or negative) half period of the ripple voltage.

The average value of the load current at the edge of COCM and DOCM is

$$I_{Lo,avg(B)} = \frac{1}{2}\frac{\left(V_{dc}/n_s - V_o\right)}{L_o}\frac{DT_s'}{2} = \frac{1}{2}\frac{V_o}{L_o}\frac{D_o' T_s'}{2} \tag{4.7}$$

where $D_o'$ is the free-wheeling period and is equal to

$$D_o' = 1 - D \tag{4.8}$$

Equation (4.8) is true for operation at the edge, but if we operate the DOCM, then it becomes

$$D_o' = 1 - D - \Delta_o \tag{4.9}$$

where $\Delta_o$ is the zero current period, D is the pulse duration or duty cycle.

The value of the output inductor for operation at the edge of COCM and DOCM is:

$$L_o = \frac{V_o^2 (1-D) T_s'}{2 P_{o,disc}} \tag{4.10}$$

For any value of output load less than the $P_{o,disc}$ value in (4.10), the operation will be in DOCM.

The expression for the output power in DOCM is derived using Fig. 4.1 as follows:

The average voltage across the output inductor is equal to zero in steady state. This yields the following expression for the output inductor discharging time, $D_o'$:

$$D_o' = \frac{\left(\frac{V_{dc}}{n_s} - V_o\right)}{V_o}.D \tag{4.11}$$

The mean value of the output current is found by finding the overall area under the current waveform and then dividing the result over half switching period, this results in

$$I_o = \frac{1}{T_s'} \frac{(D + D_o')T_s'}{2} \frac{V_o}{L_o} D_o' T_s' \tag{4.12}$$

Substituting the value of $D_o'$ from (4.11) in (4.12) and multiplying the result by $V_o$ yields the following expression for the output power:

$$P_o = V_o.I_o = \frac{D^2.T_s'.V_{dc}}{2.L_o.n_s}\left(\frac{V_{dc}}{n_s} - V_o\right) \tag{4.13}$$

In COCM the output voltage is expressed as:

$$V_o = \frac{DV_{dc}}{n_s} \tag{4.14}$$

Expression (4.14) is not valid anymore for DOCM, but rather it becomes

$$V_o = \frac{DV_{dc}}{(D + D_o')n_s} \tag{4.15}$$

When the output inductor current reaches zero the output filter capacitor provides the load current. In order to decrease the dc link voltage value, the output is operated in DOCM for the maximum load power or any other desired value of the output power.

## 4.4 Performance Characteristics Of The Converter For DACM And DOCM

Due to the discontinuous nature of the output inductor current, some of the performance characteristics of the converter will vary from those presented in Chapter three as will follow in the following sections.

### 4.4.1 RMS Current Through The Switches

The current passing through any of the full bridge switches is the sum of three components:

1. Reflected load current

$$i_o' = \frac{1}{n_s}\left[\frac{V_{dc}/n - V_o}{L_o}t\right] \tag{4.16}$$

This expression is valid for discontinuous current mode of the output filter inductor.

2. Magnetizing current which remains the same as in (3.33).

3. Auxiliary current which remains as in (3.34).

The expression for the switch current is found by using (3.35).

Its RMS value over a period of $T_S/2$ is found by integrating the expression for $i_{switch}^2$ from 0 to $T_S/2$, i.e. the RMS current for half a switching period and the RMS switch current over the line frequency period is found by averaging all these particular areas

$$i_{sw} = \frac{1}{n_s}\left[\frac{V_{dc}/n_s - V_o}{L_o}t\right] + \frac{V_{dc}}{L_M}t - \frac{V_{Cdc}}{L_M}\frac{DT_S}{4} + \frac{V_{sn}}{L_{aux}}t \tag{4.17}$$

The following expression is used to find the RMS value of the switch current for DOCM

$$I_{sw,rms(disc)} = \sqrt{\frac{1}{T_L}\sum_{n=1}^{f_{sn}}\int_0^{DT_s} i_{sw\_disc}^2\,dt} \tag{4.18}$$

where

$f_{sn} = \frac{2T_L}{T_s}$ , number of auxiliary current periods in a line frequency period.

$$i_{sw\_disc}^2 = \left(\frac{1}{n_s}\frac{V_{dc}/n_s - V_o}{L_o}t + \frac{V_{dc}}{L_M}\left(t - \frac{DT_S}{4}\right) + \frac{V_{sn}}{L_{aux}}t\right)^2 \tag{4.19}$$

We know that

$$V_o = \frac{DV_{dc}}{n_s} \tag{4.20}$$

Using expression (3.20) in equation (3.19) yields

$$i_{sw\_disc}{}^2 = \left( \frac{1}{n_s} \frac{\frac{V_{dc}}{n_s}(1-D)}{L_o} t + \frac{V_{dc}}{L_M}\left(t - \frac{DT_S}{4}\right) + \frac{V_{sn}}{L_{aux}} t \right)^2 \tag{4.21}$$

And by integrating (4.21) we obtain

$$\int_0^{DT_S} i_{sw\_disc}{}^2 dt = \int_0^{DT_S} \left( \frac{1}{n_s} \frac{V_{dc}/n_s (1-D)}{L_o} t + \frac{V_{dc}}{L_M}\left(t - \frac{DT_S}{4}\right) + \frac{V_{sn}}{L_S} t \right)^2 dt \tag{4.22}$$

And the area for the n-th switching period is found as a result from (4.22) and equals:

$$\int_0^{DT_S} i_{sw\_disc}{}^2 dt = \frac{1}{3}\left[ \left( \frac{1}{n_s} \frac{V_{dc}/n_s (1-D)}{L_o} t + \frac{V_{dc}}{L_M}\left(t - \frac{DT_S}{4}\right) + \frac{V_{sn}}{L_{aux}} t \right) \right]^2 \frac{1}{\frac{V_{sn}}{L_{aux}} + \frac{V_{dc}}{L_M} + \frac{V_{dc}(1-D)}{n_s{}^2 L_o}}$$

$$= \frac{1}{3}\left[ \left( \frac{1}{n_s} \frac{\frac{V_{dc}}{n_s}(1-D)}{L_o} \frac{DT_s}{2} + \frac{V_{dc}}{L_M}\frac{DT_s}{2} + \frac{V_{sn}}{L_{aux}}\frac{DT_s}{2} \right) \right]^3 \frac{1}{\frac{V_{sn}}{L_{aux}} + \frac{V_{dc}}{L_M} + \frac{V_{dc}(1-D)}{n_s{}^2 L_o}} \tag{4.23}$$

Equation (4.18) could be rewritten as:

$$I_{sw,rms(disc)} = \sqrt{\frac{1}{T_L} \sum_{n=1}^{f_{sn}} \int_0^{DT_S} i_{sw\_disc}{}^2(t) dt} \tag{4.24}$$

### 4.4.2 DC Link Capacitor RMS Current

The waveform of the current passing through the dc link capacitor is shown in Fig. 4.2.

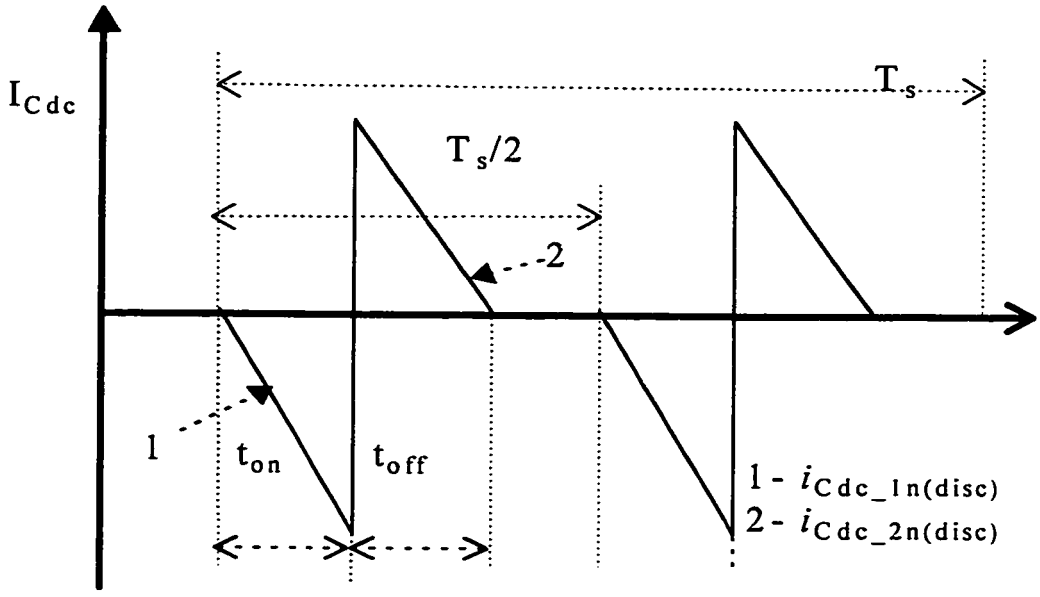


**Fig. 4.2** Dc Link Capacitor Current during DOCM

During the first on period, $t_{on} = DT_s/2$, the expression for the current is:

$$i_{Cdc\_1n(disc)} = \frac{V_{dc}/n_s - V_o}{L_o n_s} t \tag{4.25}$$

During the second off period, $t_{off} = D'T_S/2$, the expression for the current is similar to that for COCM in (3.57)

$$i_{Cdc\_2n(disc)} = \frac{-V_{sn}}{L_{aux}} \frac{2DT_S}{2D'T_S} t + \frac{-V_{sn}}{L_{aux}} \frac{DT_S}{2} = \left( -\frac{V_{dc} - V_{sn}}{L_{aux}} t + \frac{V_{sn}}{L_{aux}} \frac{DT_S}{2} \right) \tag{4.26}$$

The RMS current is defined by the following formula:

$$I_{Cdc,rms(disc)} = \sqrt{\frac{1}{T_L}\int_0^{T_L} i_{Cdc\_n(disc)}{}^2 dt} \tag{4.27}$$

where,

$$i_{Cdc\_n(disc)}{}^2 = i_{Cdc\_1n(disc)}{}^2 + i_{Cdc\_2n(disc)}{}^2 \tag{4.28}$$

First integrals of both dc capacitor currents in expressions (4.25) and (4.26) are found as:

$$\int_0^{DT_S/2} i_{Cdc\_1n(disc)}{}^2 dt = \int_0^{DT_S/2} \left(\frac{V_{Cdc}/n_s - V_o}{L_o n_s} t\right)^2 dt$$

$$= \frac{1}{3\left(\frac{V_{dc}/n_s - V_o}{L_o n_s}\right)} \left(\frac{V_{Cdc}/n_s - V_o}{L_o n_s} t\right)^3 \Bigg|_0^{DT_S/2}$$

$$= \frac{1}{3\left(\frac{V_{dc}/n_s - V_o}{L_o n_s}\right)} \left(\frac{V_{Cdc}/n_s - V_o}{L_o n_s} \frac{DT_s}{2}\right)^3 \tag{4.29}$$

And the area for the second current component is:

$$\int_0^{DT_s/2} i_{Cdc\_2n(disc)}{}^2 dt = \int_0^{DT_S/2} \left(-\frac{V_{dc} - V_{sn}}{L_{aux}} t + \frac{V_{sn}}{L_{aux}} \frac{DT_S}{2}\right)^2 dt$$

$$= \frac{1}{3\left(\frac{V_{sn} - V_{dc}}{L_{aux}}\right)} \left(-\frac{V_{dc} - V_{sn}}{L_{aux}} t + \frac{V_{sn}}{L_{aux}} \frac{DT_S}{2}\right)^3 \Bigg|_0^{DT_s/2}$$

$$= \frac{1}{3\left(\frac{V_{sn}-V_{dc}}{L_{aux}}\right)}\left(\frac{V_{sn}}{L_{aux}}\frac{DT_S}{2}\right)^3 \tag{4.30}$$

where

$$D' = D\frac{V_{dc}}{V_{dc}-V_{sn}} \tag{4.31}$$

The RMS current through the dc link capacitor is expressed as:

$$I_{Cdc,rms(disc)} = \sqrt{\frac{1}{T_L}\sum_{1}^{f_{sn}}\left(\int_0^{DT_S/2} i_{Cdc\_1n(disc)}{}^2(t)dt + \int_0^{D'T_S/2} i_{Cdc\_2n(disc)}{}^2(t)dt\right)} \tag{4.32}$$

### 4.4.3 Output Voltage Ripple

The output voltage ripple is written as:

$$\Delta V_{o(disc)} = \frac{\Delta Q}{C_o} = \frac{A_1 + A_2}{C_o} \tag{4.33}$$

where

$$A_1 = \frac{1}{2}\left(DT_s' - \frac{P_o}{V_o}\frac{L_o}{\left(\frac{V_{dc}}{n_s}-V_o\right)}\right)\cdot\left(\frac{\frac{V_{dc}}{n_s}-V_o}{L_o}DT_s' - \frac{P_o}{V_o}\right) \tag{4.34}$$

and

$$A_2 = \frac{1}{2}\left(\frac{\left(\frac{V_{dc}}{n_s}-V_o\right)DT_s' - L_o\frac{P_o}{V_o}}{V_o}\right)\cdot\left(\frac{\frac{V_{dc}}{n_s}-V_o}{L_o}DT_s' - \frac{P_o}{V_o}\right) \tag{4.35}$$

Areas $A_1$ and $A_2$ in (4.33) are shown in Fig. 4.3. After simplifications, the voltage

ripple is written as:

$$\Delta V_{o(disc)} = \frac{V_{dc}}{2C_o V_o^2 n_s}\left(\frac{\left(\frac{V_{dc}}{n_s} - V_o\right)}{L_{o(disc)}} DT_s' - I_o\right)\left(DT_s' - \frac{1}{\left(\frac{V_{dc}}{n_s} - V\right)_o} I_o L_{o(disc)}\right) \qquad (4.36)$$

### 4.4.4 RMS Current Through The Output Filter Capacitor

The waveform of the current through the output filter capacitor for DOCM is shown in Fig. 4.3. From this it is shown that the capacitor maintains the output current at its average value while operating in the zero inductor current region.

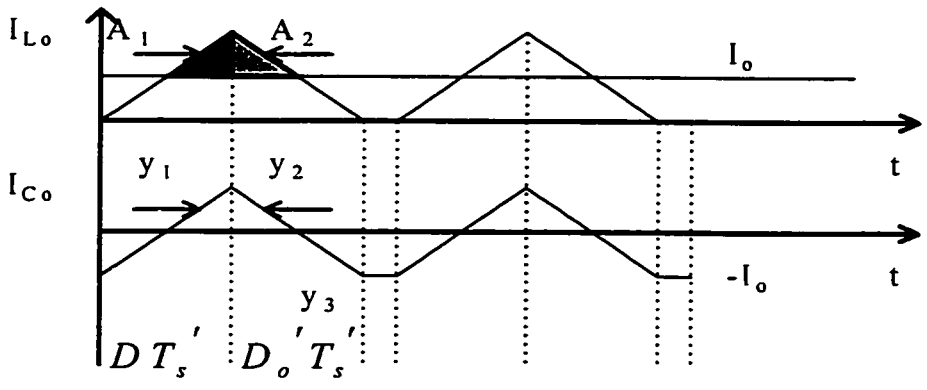


**Fig. 4.3 Current through the output filter capacitor for DOCM**

The curve of the current through the output capacitor could be broken up into three linear lines. In the first part $y_1$ the current is increasing. It decreases in $y_2$ and is constant and equal to - $I_o$ in the third part $y_3$.

$$y_1 = \frac{\frac{V_{dc}}{n_s} - V_o}{L_o} DT_s' - I_o \tag{4.37}$$

The area under the square value of $y_1$

$$\int_0^{DT_s'} y_1^2 dt = \frac{1}{3} \frac{L_o}{\left(\frac{V_{dc}}{n_s} - V_o\right)} \left( \frac{\left(\frac{V_{dc}}{n_s} - V_o\right)}{L_o} t - I_o \right)^3 \Bigg|_0^{DT_s'}$$

$$= \frac{1}{3} \frac{L_o}{\left(\frac{V_{dc}}{n_s} - V_o\right)} \left( \frac{\left(\frac{V_{dc}}{n_s} - V_o\right)}{L_o} DT_s' - I_o \right)^3 + I_o^3 \tag{4.38}$$

The second linearly decreasing curve:

$$y_2 = \frac{-V_o}{L_o} t + \frac{\left(\frac{V_{dc}}{n_s} - V_o\right)}{L_o} DT_s' - I_o \tag{4.39}$$

and the area under $y_2$

$$\int_0^{D_o' T_s'} y_2^2 dt = \frac{1}{3} \frac{-V_o}{L_o} \left( \frac{-V_o}{L_o} t + \frac{\left(\frac{V_{dc}}{n_s} - V_o\right)}{L_o} DT_s' - I_o \right)^3 \Bigg|_0^{D_o' T_s'}$$

$$= \frac{L_o}{V_o} \left( I_o^3 + \left( \frac{\frac{V_{dc}}{n_s} - V_o}{L_o} DT_s' - I_o \right)^3 \right) \tag{4.40}$$

The third is a constant value equal to the negative value of the average output

current

$$y_3 = -I_o \tag{4.41}$$

and the area under this curve is:

$$\int_0^{(T_s'(1-D-D_o'))} y_3^2 dt = I_o^2 (1 - D - D_o')T_s' \tag{4.42}$$

And the overall RMS current through the output filter capacitor for DOCM is expressed as:

$$I_{C_o,rms(disc)} = \sqrt{\frac{1}{T_s'}\left( \int_0^{DT_s'} y_1^2 dt + \int_0^{D_o'T_s'} y_2^2 dt + \int_0^{(1-D-D_o')T_s'} y_3^2 dt \right)} \tag{4.43}$$

## 4.5 Comparison Of Performance Characteristics Of COCM And DOCM

In Chapter 3, the expressions for the important performance characteristics for operation in COCM were presented. The performance characteristics for operation with DOCM were presented in the previous sections of this chapter. Based on that information this section shows some comparative performance curves for these two modes of output inductor conduction as follows:

In Fig. 4.4 the dc link voltage is shown which clearly shows that the dc link voltage value is reduced and kept constant by operating in DOCM.

Fig. 4.5 shows the RMS current through the dc link capacitor which increases slightly while operating in DOCM.

Fig. 4.6 shows the output filter capacitor RMS current which clearly increases in DOCM due to the peak to peak current passing through it and due to the fact that this capacitor maintains the load current during the zero inductor current intervals.

Fig. 4.7 shows the per unit RMS current through the full bridge switches. The current ratings of the switches increase when operating in the DOCM. In Fig. 4.8 the per unit peak output inductor current is shown. Fig. 4.9 presents the per unit ripple factor for both modes of operation. Fig. 4.10 presents the input peak current for both modes of operation.

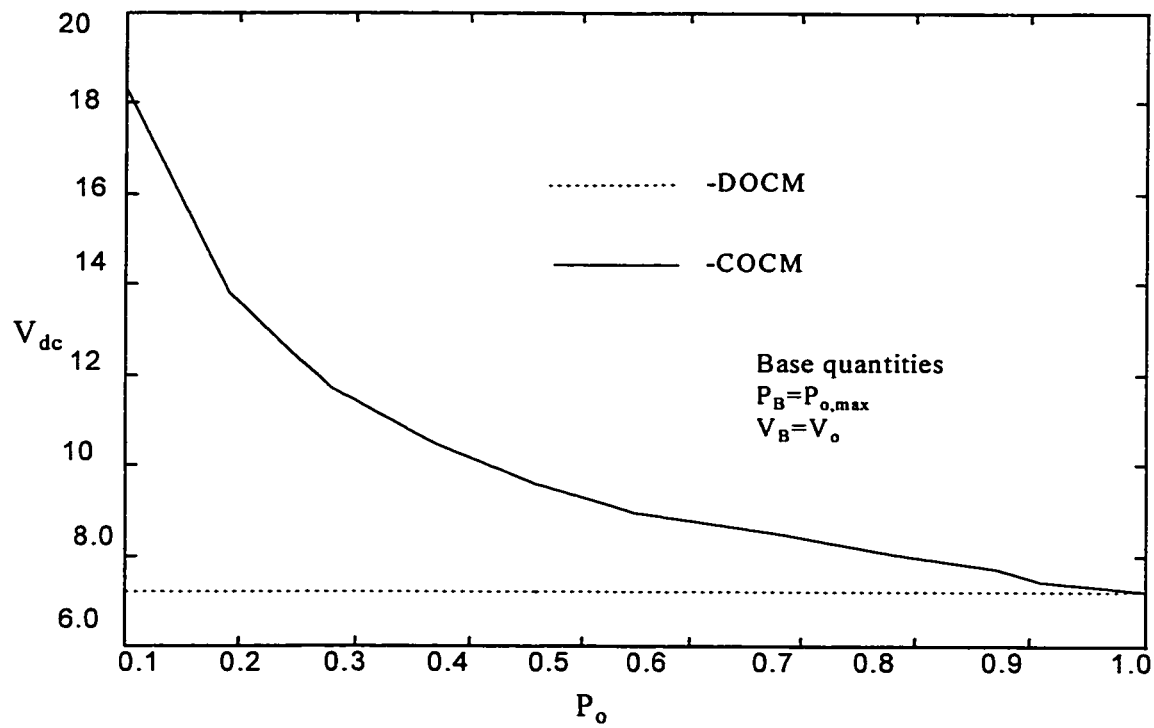


**Fig. 4.4** Per unit dc link voltage

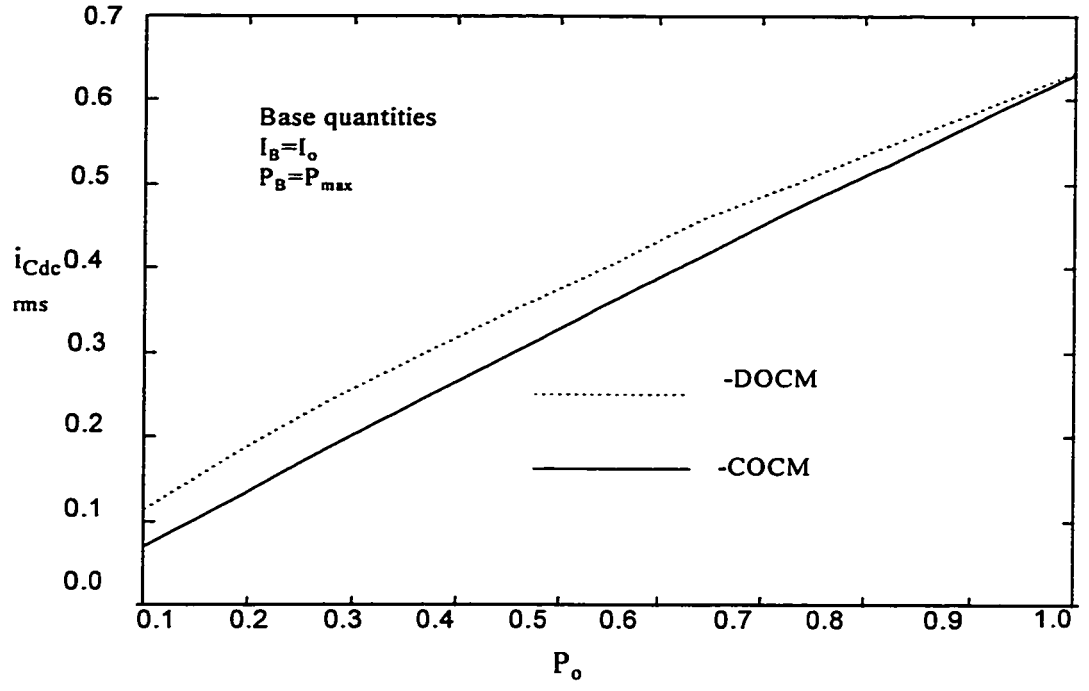


**Fig. 4.5** Per Unit DC Link Capacitor RMS Current

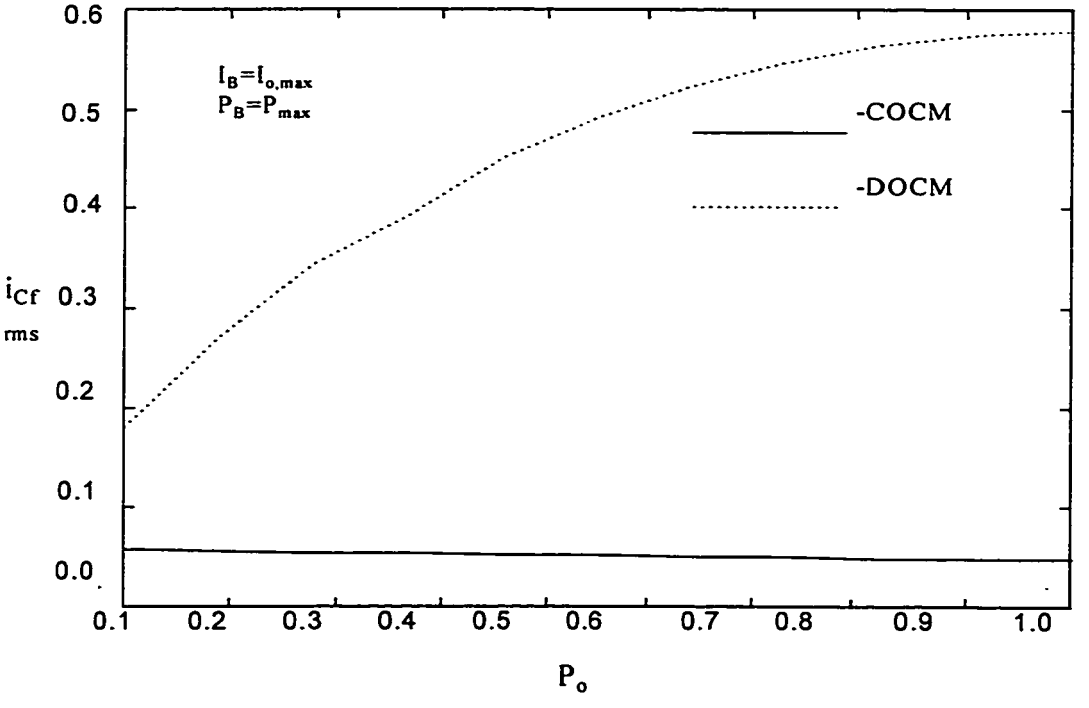


**Fig. 4.6** Per unit RMS filter capacitor current

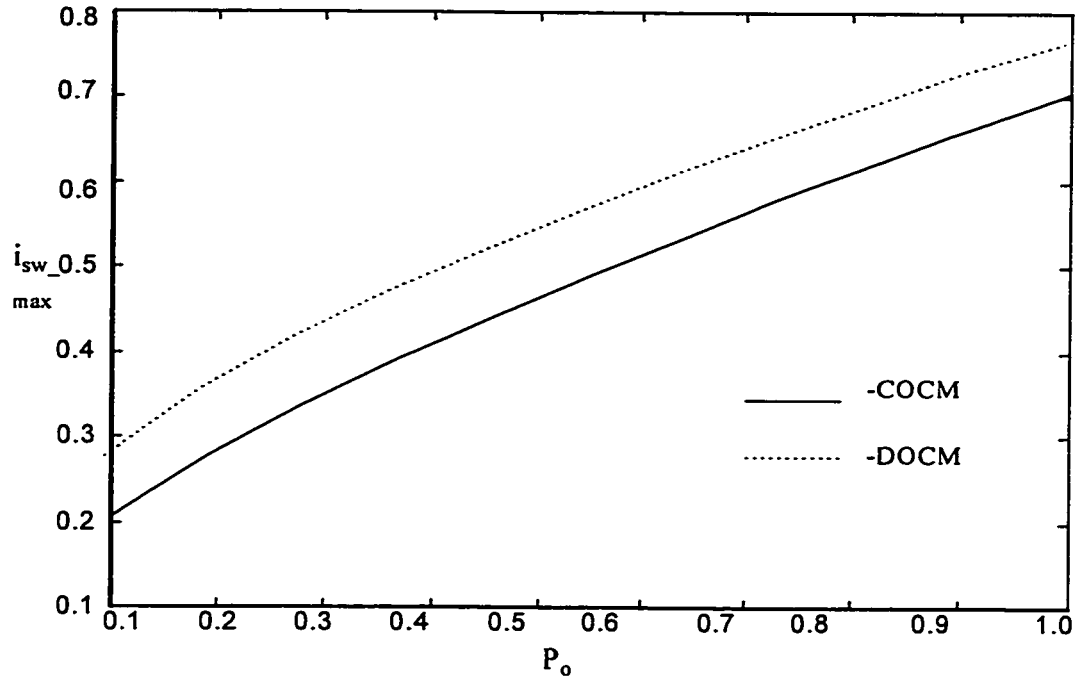


**Fig. 4.7** Per unit switch RMS current

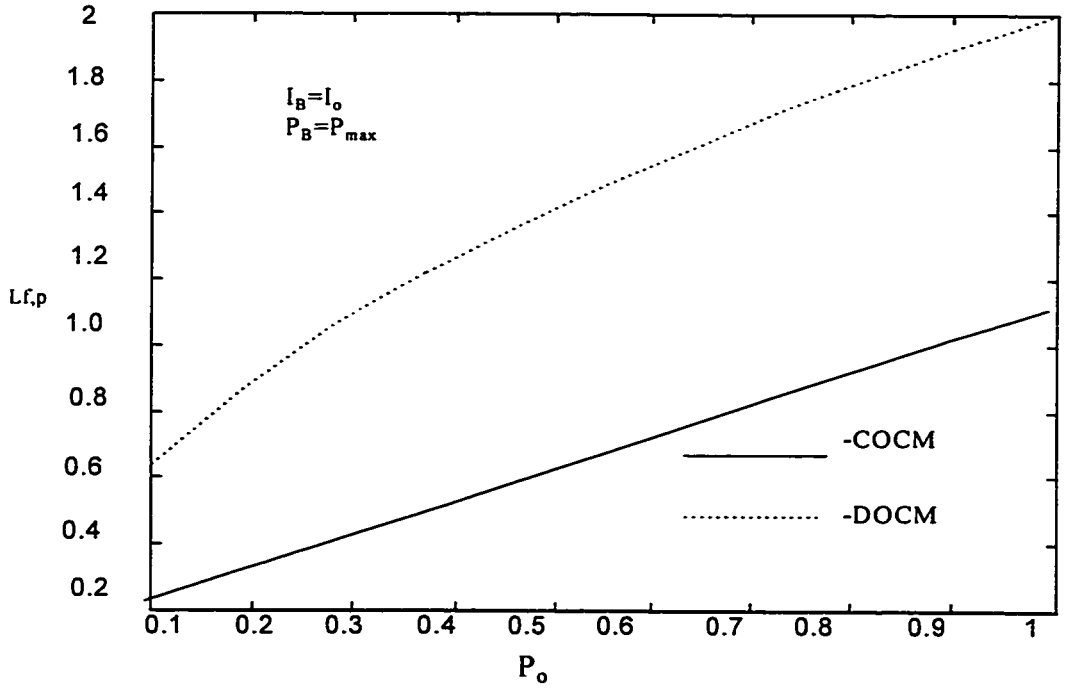


**Fig. 4.8** Per unit peak output inductor current

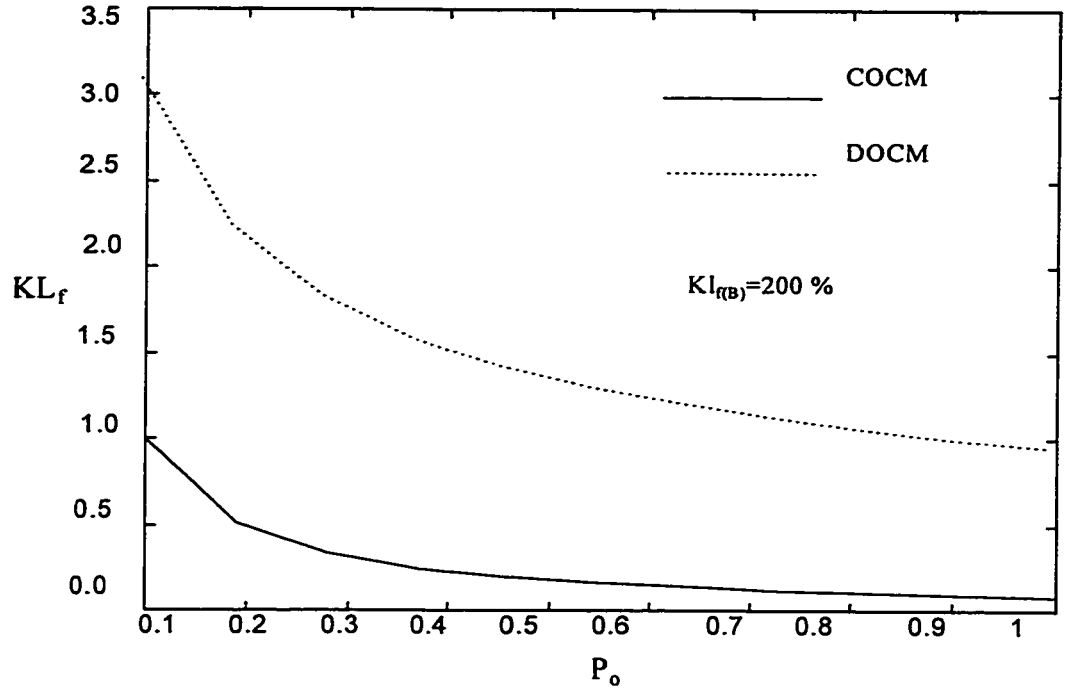


**Fig. 4.9** Per unit ripple factor

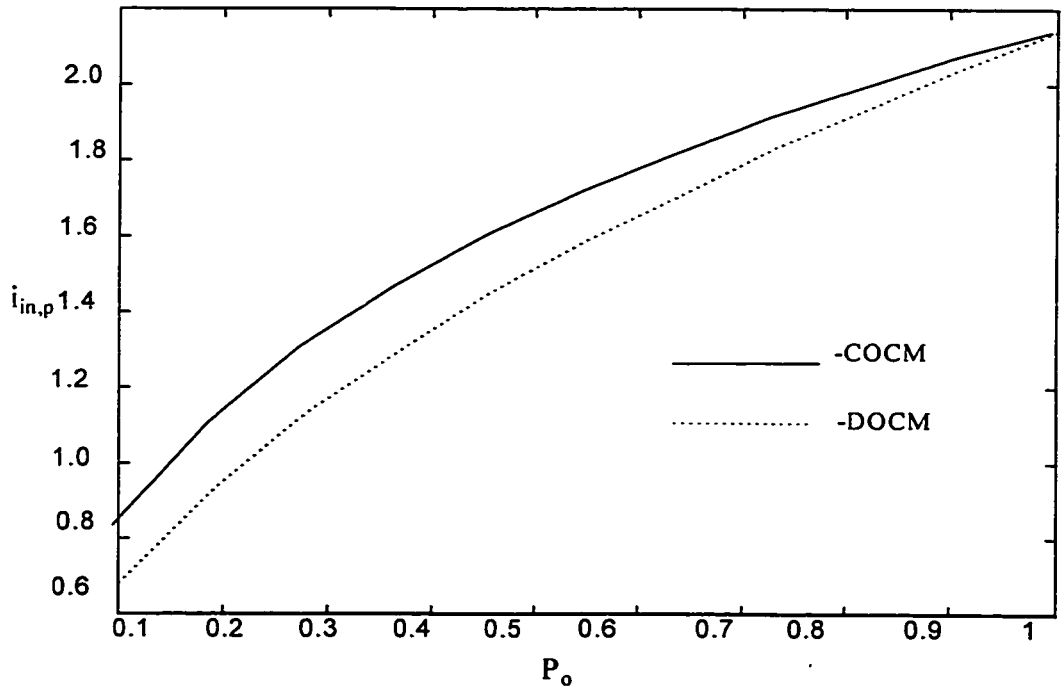


**Fig. 4.10** Per unit input peak current

## 4.6 Conclusions

In this chapter the steady state analysis of the converter for discontinuous input and output current modes has been presented. This operation reduces the voltage ratings of the full bridge switches while enabling operation from full load to 10 % load, Reduces $1/2CV_{dc}^{2}$ losses, and permits the use of high switching frequencies while keeping a close to unity power factor at the input, independent of the load.

# CHAPTER 5

# DESIGN PROCEDURE AND GUIDELINES

## 5.1 Introduction

This chapter considers the design issues of the single stage full bridge power factor corrected AC/DC converter. The equations and performance characteristics derived in Chapter 3 and 4, are used to choose the circuit components. In determining the suitable input line voltage level and switching frequency for the operation of this circuit some new graphs are developed and presented in Section 5.1 A design example for a 500 W AC/ DC converter operated with DACM and COCM is presented in Section 5.2. Section 5.3 presents the simulation and experimental results for the design example in section 5.2.

The single stage power factor corrected topology presented in this thesis has several advantages over the traditional two stage circuits in terms of simplicity of control, cost and weight of magnetic components. But it has still some limitations operating from high input voltage levels. It is found that the presented topology is suitable for operation in the (85-135) V input voltage range. This is due to the high dc link voltage level which might go up to more than 1.8 kV at light loads when operating from (176-266) V line voltage. An increase in the auxiliary inductance value leads to lower dc link voltage, but at the same time we approach the boundary between continuous and discontinuous conduction modes for the auxiliary inductor. Operation in discontinuous output inductor current mode limits the dc link voltage value and makes it load independent and lowers the voltage rating of the full bridge switches. In Figs. 5.1 and 5.2 the influence of $L_{aux}$ on

the dc link voltage value and the mode of conduction is investigated for different input voltage values and various switching frequencies.

1. The influence of $L_{aux}$ is considered for operation at 50 kHz when operating from line voltage which could vary from 176-266 volts. The results are shown in Fig. 5.1

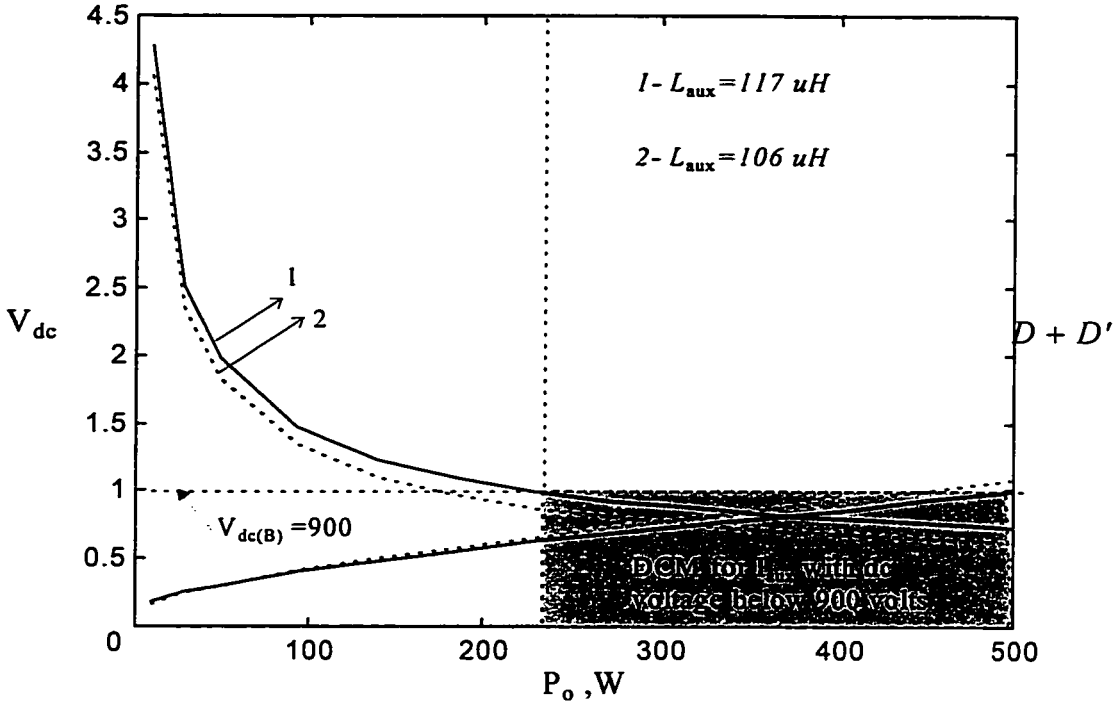


**Fig. 5.1** Influence of the value of $L_{aux}$ on Vdc and conduction mode of $I_{aux}$ for $V_{s,rms}$ = 176 - 266 volts, $f_{sw}$ =50 kHz

Fig 5.1 shows that for an increase in inductance value for the same $V_s$, the dc link voltage value will decrease, but at the same time will approach the operation in CCM for the auxiliary inductor.

2. The influence of $L_{aux}$ is considered for operation at 50 kHz when operating from line voltage which could vary from (85-135) volts input. The results are shown in Fig. 5.2.

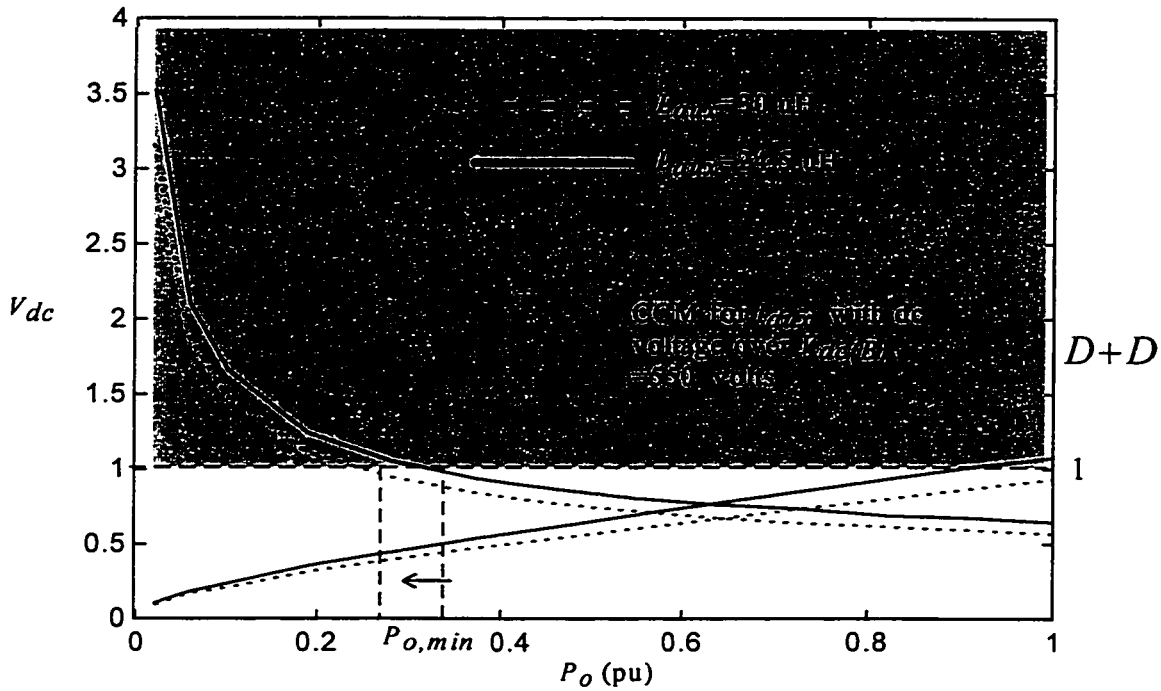


**Fig. 5.2** Influence of the value of $L_{aux}$ on Vdc and conduction mode of $I_{aux}$ for $V_{s,rms}$ =85-135 volts, $f_{sw}$ =50 kHz

Fig 5.2 shows that for an increase in inductance value for the same $V_s$, the dc link voltage value will decrease, but at the same time will approach the operation in CCM for the auxiliary current. Higher value of $L_{aux}$ also results in lowering the minimum required load from 165 W for $L_{aux}$ = 24.5 uH to 133 W for $L_{aux}$ = 30 uH.

## 5.2 Design Procedure And Example

In this section a design example is given to illustrate the choice of circuit components for the converter circuit. The equations developed in previous chapters, as well as the design considerations in section 5.1 are used to determine the suitable switching frequency.

### 5.2.1 Design Specifications

It is required to design a 500 W output, single stage power factor corrected power supply with the following specifications:

Input supply voltage = 110±20%

Output voltage $V_0$ = 50 V

Maximum Load Current $I_0$ =10 A.

Switching frequency $f_{sw}$: high

Using the equations and analysis presented previously and the fact that the on time should not exceed 50 % for proper operation of the circuit, the circuit parameters are chosen as follows:

The maximum duty cycle $D_{max}$ = 0.45

The minimum peak line voltage

$$V_{s,\min} = 85\sqrt{2} = 120.2\ \text{V}$$

### 5.2.2 The Dc Link Voltage Value

The minimum dc link voltage is found as

$$V_{dc} = \frac{V_{s,\min}}{1-D} = \frac{120.2}{1-D_{\max}} = 218.6\,\mathrm{V}$$

### 5.2.3 The Turns Ratio Of the High Frequency Transformer

The high frequency transformer turns ratio is

$$n_s = \frac{N_p}{N_s}$$

which could be found as

$$n_s = D_{\max}\frac{V_{dc}}{V_o} = 1.97 \cong 2$$

### 5.2.4 Switching Frequency Considerations

The higher the value of $f_{sw}$, the better it is in terms of the size and weight of magnetic components. But, it is well known that with an increase in switching frequency the switching losses increase. From loss calculations at different frequencies it is seen that a frequency equal to $f_{sw}$ =50 kHz is a good compromise in terms of lower switching losses and lower dc link voltage level. If we use MOSFET switches for the full bridge, then the dc voltage is better to be kept below 550 volts and a minimum load is required at the output side equal to 165 W or 33 % of the rated load.

### 5.2.5 The Auxiliary Inductor

The auxiliary inductor value is calculated using formulae from Chapter 3, in particular (3.25), or is chosen from Fig. 5.2 so that the operation will stay in DCM for auxiliary inductor. A value of $L_{aux} = 24.5$ uH will minimize $V_{dc}$ and keep the operation in DACM, as shown in Fig. 5.2, where the per unit conduction time is less than 1 over the whole load range. This enables the inductor to charge and discharge within the specified half switching period.

### 5.2.6 The Switch RMS Current

The switch rms. current is found from section 3.5.1. The maximum value occurs at low line voltage and maximum load condition. It is found to have a maximum value of $I_{sw,rms\_max} = 0.7\ I_{o(B)} = 0.7 \cdot 10 = 7$ A, as shown in Fig. 4.7.

The voltage rating of the switch is the dc link voltage. It is limited to 550 V. Two MOSFET switches might be paralleled to lower the $R_{DS,ON}$ value and thereby decrease conduction losses. But, this might affect the switching losses as the output capacitance of the switch will increase and discharging this capacitance will need more energy from the circuit inductance.

### 5.2.7 Output Filter Inductor

The value of the output filter inductor will affect its mode of operation, continuous or discontinuous. For continuous mode, it is required by the design specifications to have a ripple factor less than 20 %, which means that the allowed filter

inductor current ripple is 2 Amperes at $P_0$ =50 W. Equation (3.72) is used to find the value of the output inductor which meets the design specifications for the output current ripple

$$L_o = \frac{V_o^2(1-D)}{P_{o\_disc} K_{ripple} i_{Lo}} \frac{T_s}{2} = \frac{50^2(1-0.107)10e-06}{100} = 223 \quad uH$$

### 5.2.8 Input RMS Current

Input RMS current is necessary to determine the current ratings of the front end diode rectifier. This current is found from equation (3.53) in section 3.5.2. Fig 4.10 shows the per unit input RMS current as a function of the per unit output load. This plot shows that maximum current occurs at full load and low line. The current rating of the front end diode rectifier is 0.6 pu.

### 5.2.9 Output Filter Capacitor

The output voltage ripple is found from (3.73) and equals

$$\Delta V_{C_o} = \frac{\left(T_s'\right)^2(1-D)}{8 L_o C_o}.100$$

Then for a known value of allowed voltage ripple, equal to 50 mV, the output filter capacitor is found using the expression for output voltage ripple

$C_0$ = 100 uF

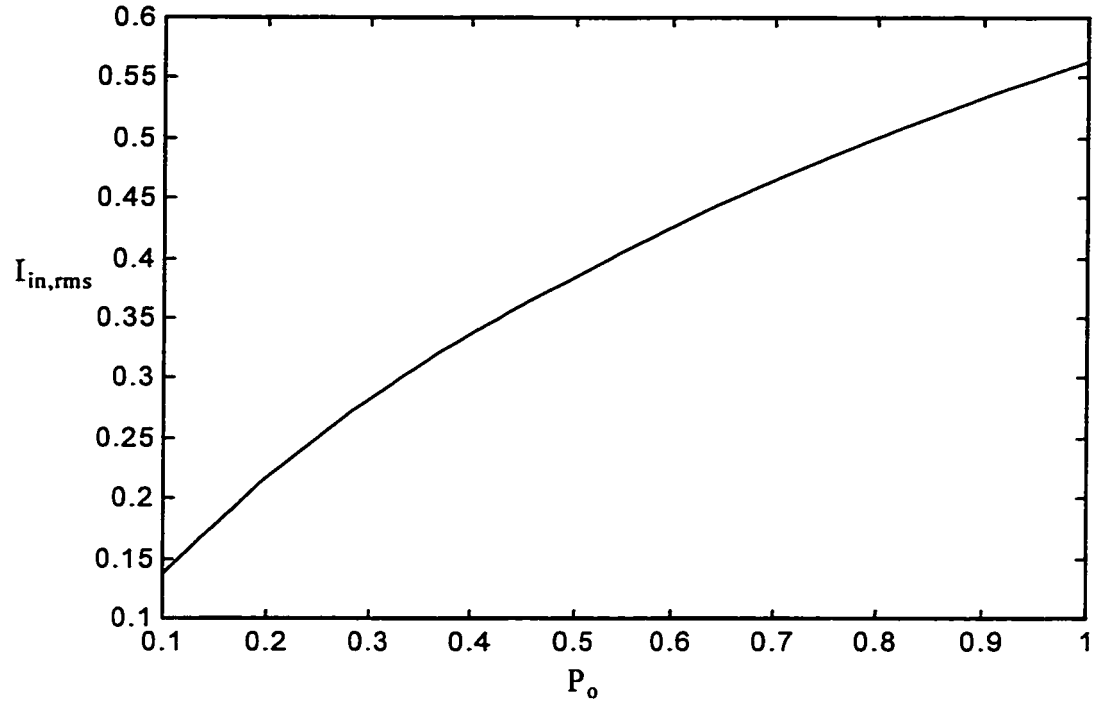


**Fig. 5.3** Per Unit Input RMS Current for $V_{s,rms}$ = (85-135) V

### 5.2.10 DC Link Capacitor RMS. Current

The dc link capacitor rms. current was shown in the previous chapter in Fig 4.5 and indicates that the current rating of the dc link capacitor is 0.64 pu.

## 5.3 Simulation And Experimental Results Of The Designed Converter

The full bridge converter circuit was simulated using PECAN and PSIM simulation packages for the given design example and the simulation results are provided which verify the proper design and choice of circuit components. Also a laboratory prototype was built and tested.

### 5.3.1 Simulated Input Current Waveform

The input current waveform is presented for operation at 50 kHz and 500 W output power. The resulting waveform is shown in Fig. 5.5 and the harmonic spectrum of this waveform is shown in Fig. 5.6 and 5.7.

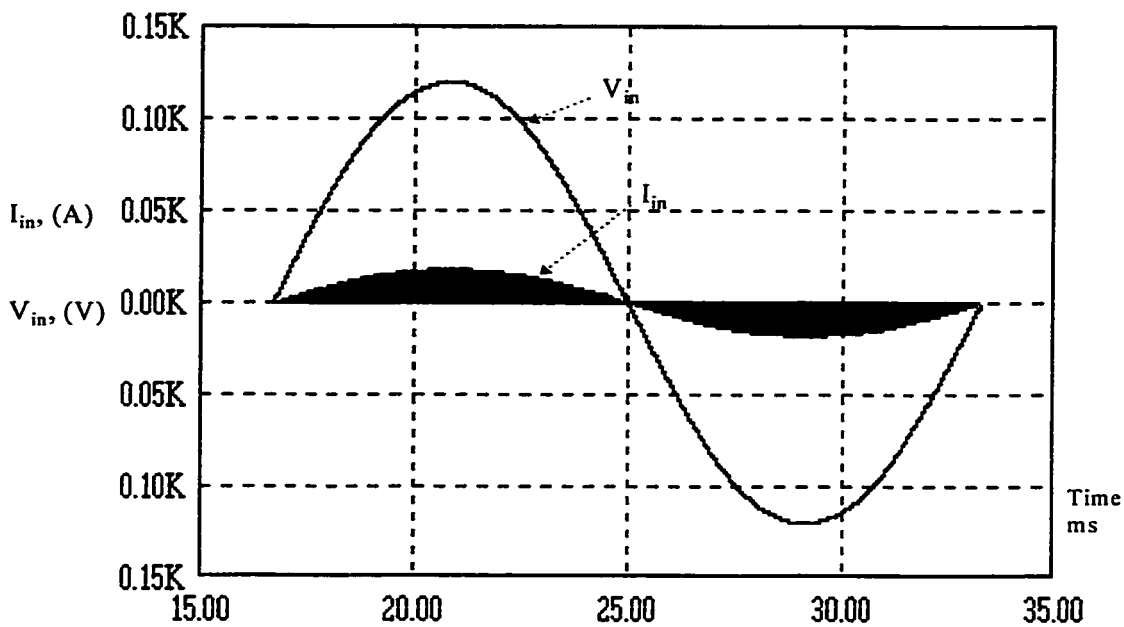


**Fig. 5.4** Simulated Input Current and Voltage Waveforms for a 500 W Converter with $D_{max}$ =0.45 and $f_{sw}$ =*50* kHz

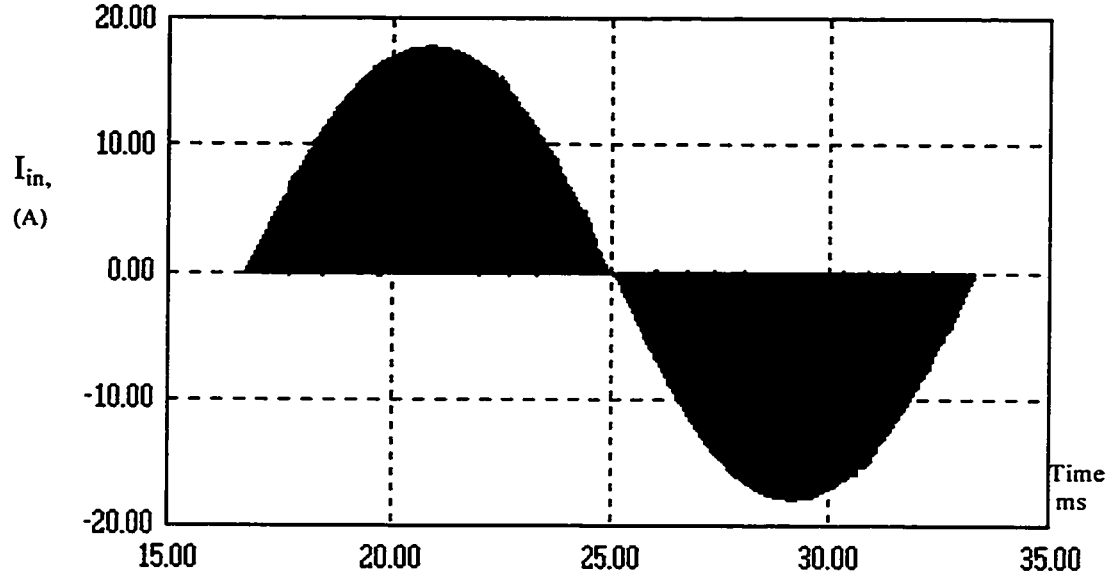


**Fig. 5.5** Simulated Input Current Waveform for a 500 W Converter with $D_{max}$ =0.45 and $f_{sw}$ =50 kHz and $V_{s,rms}$ = 85 V

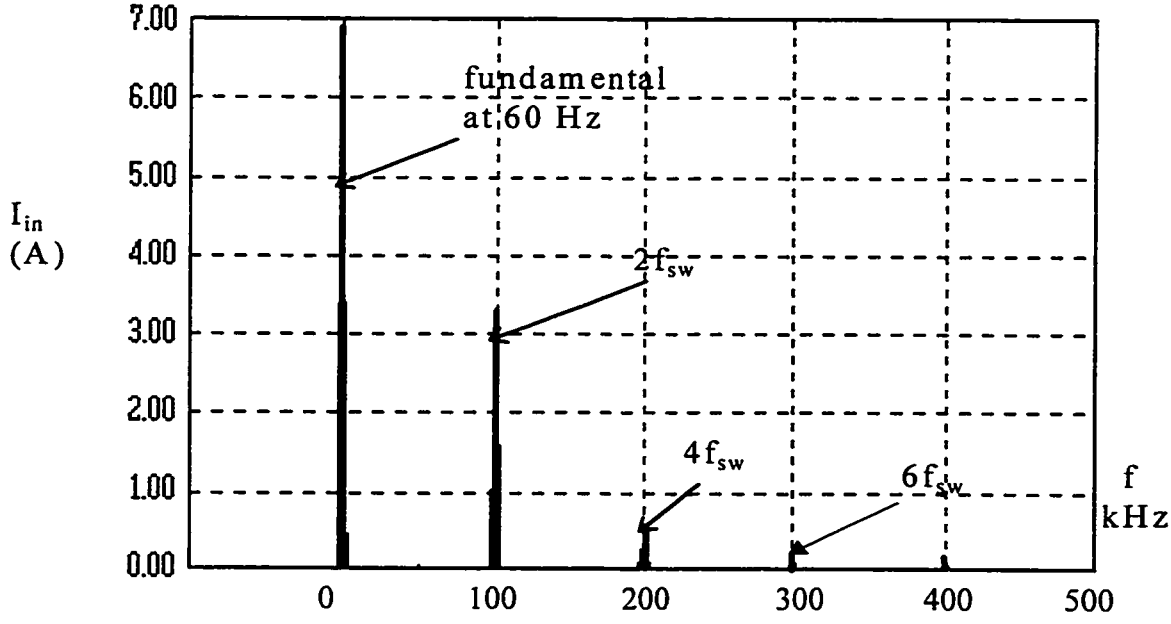


**Fig. 5.6.** Simulated Input Current Harmonic Spectrum for a 500 W Converter with $D_{max}$ =0.45 and $f_{sw}$ =*50* kHz and $V_{s,rms}$ = 85 V

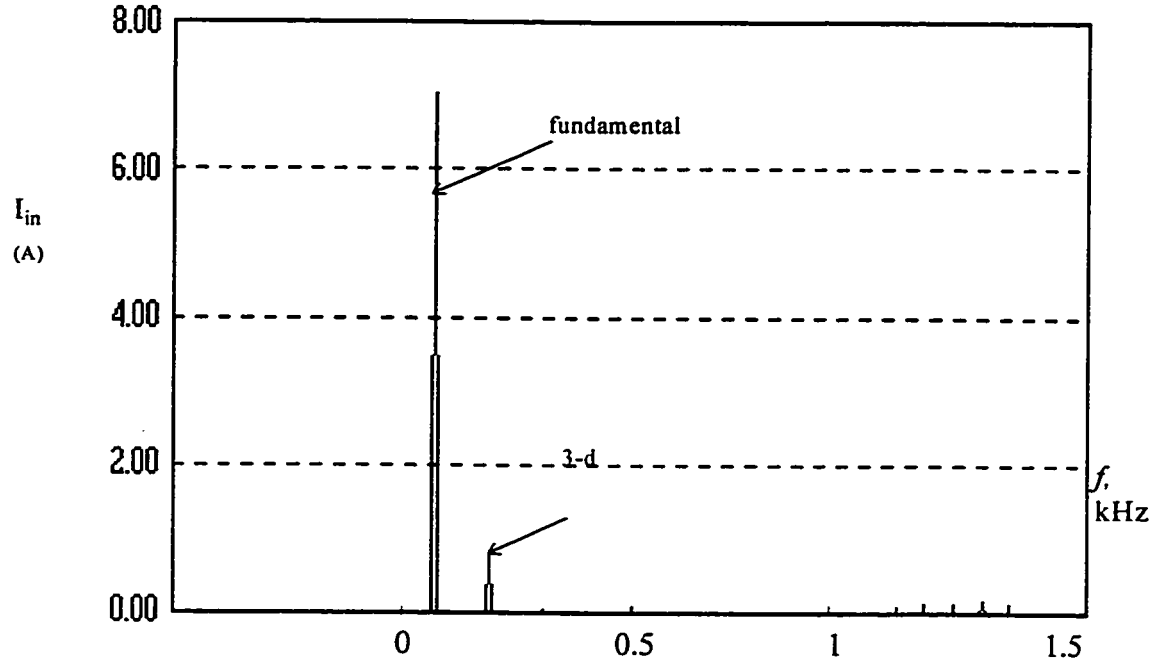


**Fig. 5.7.** Simulated Input Current (Low Frequency) Harmonic Spectrum for a 500 W Converter with $D_{max} = 0.45$ and $f_{sw} = 50$ kHz and $V_{s,rms} = 85$ V

### 5.3.2 Simulated Voltage At The Front - End Diode Rectifier Output

This voltage is the sum of the rectified input voltage and the auxiliary voltage which is added from the auxiliary winding to shape the input current waveform.

### 5.3.3 Simulated Dc Link Voltage

The simulated waveform of the dc link voltage is provided in Fig. 5.11

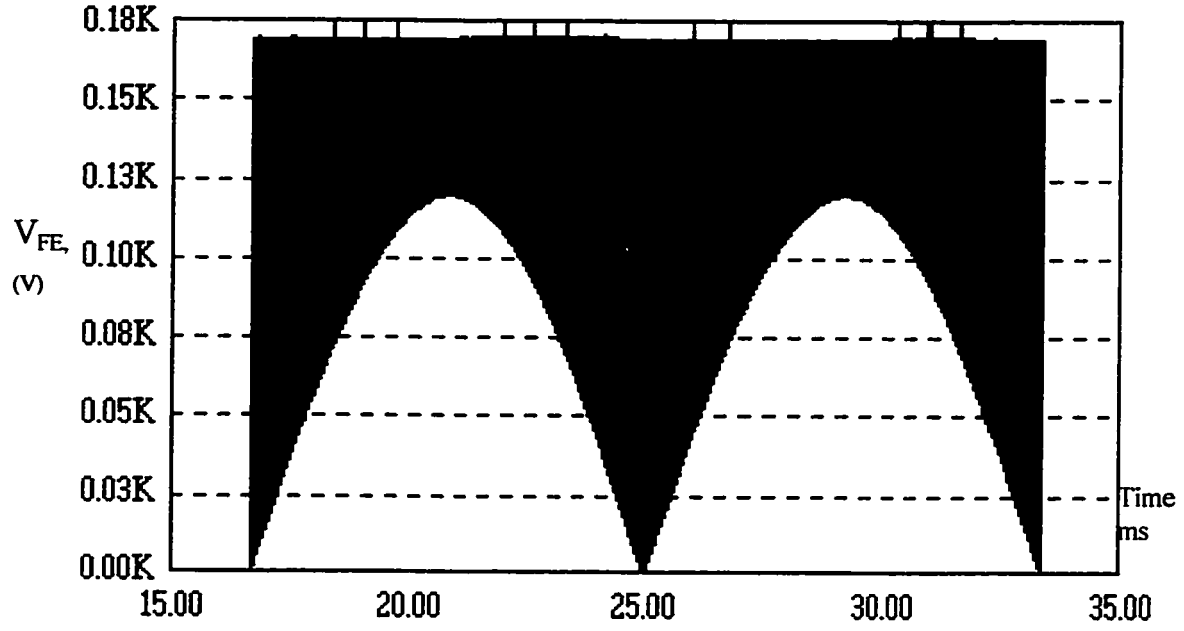


**Fig. 5.8** Simulated Voltage at the Front End Rectifier Output for a 500 kW Converter with $D_{max}$ =0.45 and $f_{sw}$ =*50* kHz and $V_{s,rms}$ = 85 V

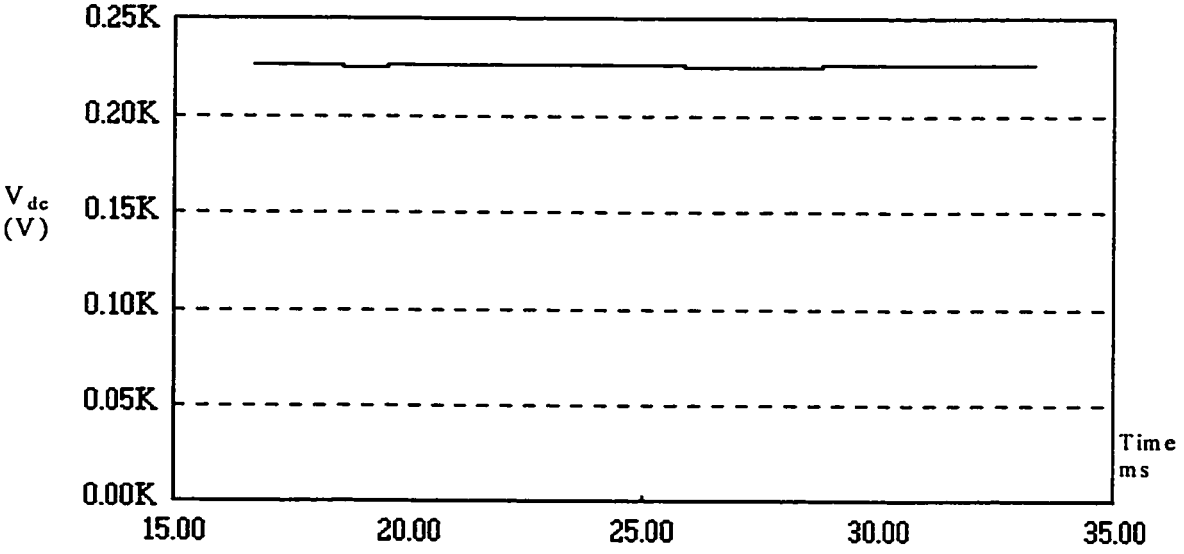


**Fig. 5.9**. Simulated Dc link Capacitor Voltage Waveform for a 500 W Converter with $D_{max}$ =0.45 and $f_{sw}$ =*50* kHz and $V_{s,rms}$ = 85 V

### 5.3.4 Experimental Results

A 500 Watt laboratory prototype was built and tested for operation at low input voltage. The experimental results confirm the high power factor and sinusoidal input current shape. Experimental current waveforms before filtering are shown in Fig 5.10 and in Fig. 5.11 after the filtering action. The phase shift control techniques is used to control the two legs of the full bridge converter. This technique was implemented using the ML4818 control chip.

The power factor is load dependent and its experimental value is shown as follows:

| $V_{in}$ (V) | $I_o$ (A) | pf |
|---|---|---|
| 85 | 3.3 | 0.992 |
| 85 | 10 | 0.997 |
| 135 | 3.3 | 0.989 |
| 135 | 10 | 0.995 |

## 5.4 Conclusions

A design procedure for the proposed converter circuit has been presented in this chapter. This procedure has been demonstrated on a 500 W power supply example. The simulation and experimental results has been given as well. These results confirm the theoretical considerations and thereby, features such as a close to unity power factor with a fast output voltage regulation are obtained.

**Fig 5.10** Experimental input current waveform before filtering for operation at 50 kHz and $V_{s,rms}$ = 85 V ( 5 A/10 mV)

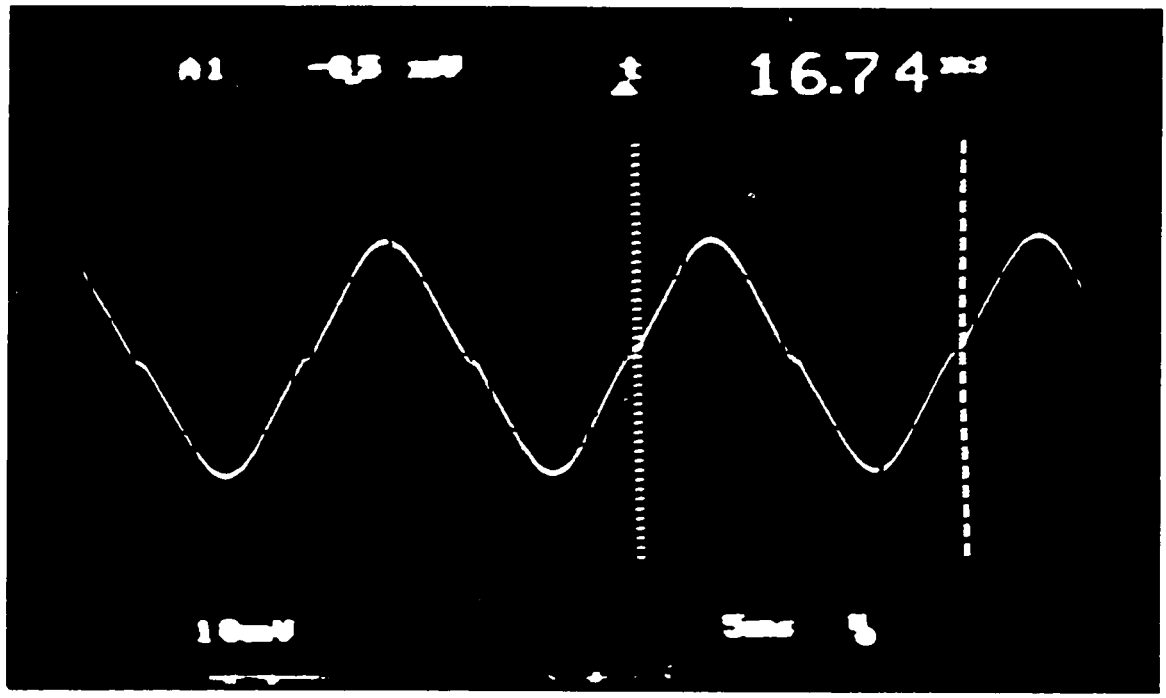


**Fig 5.11** Experimental input current waveform after filtering for operation at 50 kHz and minimum input voltage $V_{s,min}$ =85 V

# CHAPTER 6

# CONCLUSIONS

## 6.1 Summary

In this thesis a new single phase single stage power factor corrected AC/DC converter topology is presented. The converter uses a diode rectifier as a front-end converter, a full wave inverter to supply the load power, and an auxiliary circuit to shape the supply line current. The analysis of the converter, the operating principles and operating modes are given. A steady state analyses of the converter for both continuous and discontinuous modes of the load inductor is performed. Steady state analysis leads to design equations as well as an optimum operating mode. Theoretical considerations are tested on a 500 W laboratory prototype.

## 6.2 Conclusions

A new single stage power factor correction AC/DC converter has been studied and analyzed for operation in both continuous and discontinuous current modes. The features of the proposed converter topology confirmed by design, simulation and experimental results can be summarized as follows:

(1) The supply current can be sinusoidal shaped by means of the auxiliary circuit.

(2) Line input harmonics are mainly at twice the switching frequency.

(3) The discontinuous load inductor current allows the operation at reduced dc link voltages.

(3) The independent and high frequency operation of the load inverter allows the design of control loops with wide band width.

(4) The applicability is for low-medium power ranges.

The above features lead to the following improved characteristics:

(a) Unity displacement power factor operation.

(b) Minimum line current harmonic distortion.

(c) Reduced switch voltage ratings.

(d) Negligible load voltage harmonics.

(e) Light converter and easy control circuitry.

## 6.3 Suggestions for Future Work

The following work is proposed for the future research on this topic:

(1) Development of IGBT based AC/DC converter for higher power levels.

(2) Investigation of resonant mode auxiliary circuits in the proposed converter structure.

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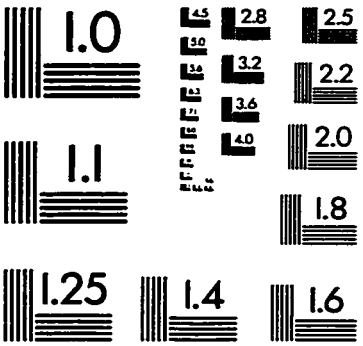
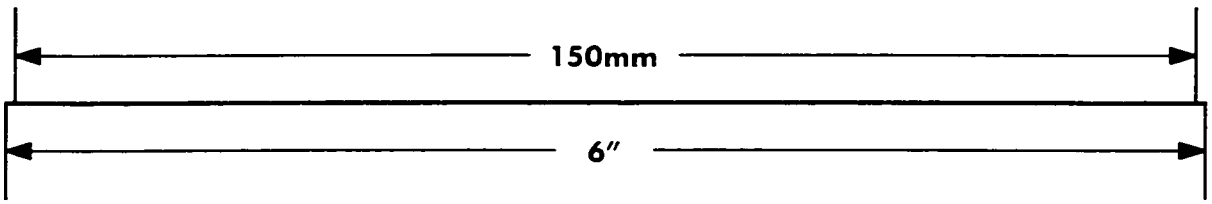
TEST TARGET (QA-3)

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