

Faculty of Health, Engineering and Sciences

Overcoming Asymmetrical Communication Delays in Line Current Differential Protection Circuits

Dissertation submitted by

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ABSTRACT

Communications asymmetry leads to current differential protection relay misoperation by causing relays at either end of a power line to sample load current waveforms at different moments in time. The increased use of current differential protection and developments in communication technologies in power systems has led to the increase likelihood of relay misoperation due to communication delay asymmetry.

The main cause of communication delay asymmetry is split-path-communications, whereby transmit and receive directions of a communications channel take separate paths with different delays. Split-path-communications are the result of faults in one direction of a communications channel, causing that direction only to switch from main to alternate paths.

This project studies AusNet Services' communications network and those similar to it, to find the typical sources of communication delays. Delays are measured between a variety E1 interfaces in the AusNet Services network, and the results used to calculate the per unit delays through given types of cross-connections. These are used in conjunction with a current differential relay response calculator, to create a model that displays a relay's response to a communications channel with specified attributes.

The chance of split-path-communications can be avoided by using communications equipment with bidirectional switching capabilities. The Avara DB4 family of branching E1 cards have this capability; however, this project reveals that a fault in the DB4 firmware code means that they may still cause protection relays to misoperate due to asymmetry. The DB4 firmware was updated, and further testing proved that it now prevented relay misoperation.

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Nomenclature and Acronyms

The following abbreviations have been used throughout this report:

μs	Microsecond		
87L	Segregated Line Current Differential (ANSI standard)		
AC	Alternating Current		
AER	Australian Energy Regulator		
ACM	Adaptive Coding and Modulation		
AIS	Alarm Indication Signal		
ANSI	American National Standards Institute		
AU	Administrative Unit		
AUG	Administrative Unit Group		
СВ	Circuit Breaker		
CT	Current Transformer		
CWDM	Coarse Wave Division Multiplexing		
DIU	Digital Interface Unit		
DTE	Data Terminal Equipment		
DWDM	Dense Wave Division Multiplexing		
Gbps	Gigabits per Second		
GIS	Geographic Information System		
GPS	Global Positioning System		
Hz	Hertz		
IED	Intelligent Electronic Device		
IEEE	Institute of Electrical and Electronics Engineers		
kbps	Kilobits per Second		
Mbps	Megabits per Second		
ms	Millisecond		
MSP	Multiplexer Section Protection		
OTDR	Optical Time Domain Reflectometer		
PDH	Plesiochronous Digital Hierarchy		
РОН	Path Overhead		
PRC	Primary Reference Clock		
Rx	Receive		
SCADA	Supervisory Control and Data Acquisition		
SDH	Synchronous Digital Hierarchy		

SECV	State Electricity Commission of Victoria
SNCP	Sub Network Connection Protection
SONET	Synchronous Optical Networking
STM	Synchronous Transport Module
TDM	Time Domain Multiplexing
Telco	Telephone Company
TU	Tributary Units
TUG	Tributary Unit Group
Tx	Transmit
VC	Virtual Container

CHAPTER 1 - Introduction

The increased speed and availability of digital communications channels in electricity transmission and distribution networks has resulted in an increased use of line current differential relays. Current differential relays depend heavily on reliable communications with low, symmetrical propagation delays. Much research and development has resulted in highly reliable communications networks utilising protective switching. This project will explain that if not carefully managed, this communications network switching can result in the misoperation of current differential relays due to asymmetrical communication channel delays.

1.1 Company Information

This research project is supported by my employer, AusNet Services, Victoria.

AusNet Services (formally SP AusNet) is the publicly listed company which owns and operates almost all of Victoria's electrical transmission network and the majority of its sub-transmission and distribution networks. It also owns and operates a portion of Victoria's gas distribution network. As of March 2016 it owns and operates approximately \$11 billion of electricity and gas assets, connecting to more than 1.3 million Victorian homes and businesses. It services over 700,000 electricity customers and over 600,000 gas customers. The extent of AusNet Services' coverage is illustrated in Figure 1.1.

AusNet Services' electricity transmission network consists of 49 terminal stations, 13,000 towers and 6,500 kilometres of high voltage powerlines operating between 110 and 500 kV. Its electricity sub-transmission and distribution networks consist of more than 380,000 power poles and 49,816 kilometres of powerlines operating between 415 V and 66 kV.

AusNet Services is a regulated network business, meaning its revenue is capped by the Australian Energy Regulator (AER) so as to prevent monopoly pricing. It also owns two unregulated businesses, Select Solutions and Geomatic Technologies. These businesses provide a range of services to the energy and other industries including water, transportation, telecommunications, finance and property.



AusNet Services' Electricity and Gas Networks

Figure 1.1: AusNet Services Electricity and Gas Network Coverage (AusNet Services, 2016).

The Victorian electricity generation, transmission and distribution was formally owned and operated by the State Electricity Commission of Victoria (SECV). In 1994, Victoria's electricity network was privatised and its transmission and distribution networks were bought by separate companies. The networks have changed hands several times since, and AusNet Services now owns and operates both transmission and distribution assets.

1.2 Project Justification

Line current differential protection plays a vital role in today's electrical power systems. Its failure or misoperation can have severe impacts on the power system and on public safety. An integral component of line current differential protection systems are the communications channels between ends of powerlines. These communications channels are most often multiplexed fibre and/or radio systems that have the potential for asymmetrical delays in transmit and receive directions. This asymmetry can cause differential protection circuits to fail or misoperate.

AusNet Services has several line current differential protection circuits in service with the potential for asymmetrical communication delays. There have been several transmission line current differential protection false-trips, suspected to be a direct result of communications channel asymmetry.

Prior to the commencement of this project very little had been done by the company to determine the cause of, or the magnitude of the asymmetry in its communications network. Recent acquisitions of GPS-synchronised communications network test equipment have made it possible to accurately measure the one-way time delay and asymmetry across various points in the network.

1.3 Project Objective

The objective of this project is to measure the time delay across a variety of AusNet Services' communications network nodes, and to use this data to identify sources of latency and asymmetry. The Literature Review will be used to help determine possible sources of asymmetry, and ways to minimise or compensate for it.

The measured data will also be used to develop a model to estimate the latency between any two points in AusNet Services' communications network. If proven accurate, this model can be used by communications design engineers to predict the latency of proposed communications routes prior to them being established.

Latency testing was conducted using the following test equipment:

- Albedo Ether.Genius communications test set
- Net Research NetProbe 2000 communications test set
- Anritsu MT1000A Network Master Pro OTDR with transport module
- Hioki MR8847 memory recorder

The Albedo was the test set most used due to its GPS synchronised end-to-end delay functionality. The other testers were used at various stages throughout the project, as they each possess their own unique desirable functionality.

The general layout of the AusNet Services communications network is described in Section 3. To find the true latency between ends of a line current differential circuit as seen by the

Intelligent Electronic Devices (IEDs) would require testing at the 64 kbps interface. However, it is simpler to setup and measure at the 2 Mbps (E1) level, and preliminary testing revealed that the multiplexing delay between 64 kbps and E1 levels were practically equal across all circuits. Additionally, the 64 kbps interface is common to both primary and backup paths of protected E1 circuits, so its delay affects both paths. Thus, there was nothing to be gained by testing at the 64 kbps interface.

1.4 Dissertation Structure and Content

The chapter structure and the contents within the thesis are outlined in the following list.

Chapter 1 – Introduction: Outlines the justification and objectives of the project, briefly describing the motivations and desired outcomes.

Chapter 2 – Literature Review: Details the theory behind current differential protection and provides an overview of the PDH/ SDH communications standards. Studies previous works relating to asymmetrical communications delays and their effects on current differential protection circuits.

Chapter 3 – AusNet Services' Communications Network: Provides an overview on the types and configurations of communications equipment used by AusNet Services.

Chapter 4 – Methodology: Describes the planning steps and the tasks that were undertaken to achieve the project aims.

Chapter 5 – Results: Details and discusses the results of the project testing and calculations.

Chapter 6 – Conclusions and Further Work: Summarises the project findings and proposes possible further works.

CHAPTER 2 – Literature Review

This section gives an overview of current differential protection and how it is affected by communications channel delays and asymmetry. It explains the communications technologies used to transport current differential signals and their potential causes of asymmetry. It includes a review of the 2015 IEEE Guide for Application of Digital Line Current Differential Relays Using Digital Communication.

2.1 Current Differential Protection Overview

Current differential line protection is a form of protection whereby current vectors are measured at either end of a power line. A current difference greater than a predetermined value indicates a fault on the line, and circuit breakers (CBs) are opened by IEDs to isolate the fault from the rest of the network.

Because the power network operates at 50 Hz ac, to compare the waveforms at either end of a line they must be sampled at precise intervals in time. It would be worthless comparing the peak of one end with the zero-crossing of the other. It is for this reason that it is of critical importance to have reliable communications with stable, predictable propagation delays.

Because power line protection is so critical, the communication system that it relies on should have built-in diversity so that, wherever possible, there is no single point-of-failure that would render it inoperable. To achieve this diversity, the communications equipment used is able to switch automatically from communications path A to path B in the event of a fault on path A. This switching between communications paths can result in differences in propagation delays between transmit and receive directions, which can lead to protection system misoperation.

The basic operating principle of current differential relaying is to calculate the difference between the currents entering and leaving the protected zone (Brunello et al. 2004). Figure 2.1 below shows the typical arrangement for two current differential IEDs protecting a power line using multiplexed communications.



Figure 2.1: Typical Line Current Differential Protection Arrangement (Antonova et al. 2014).

To measure the current at each end of a line, line current differential IEDs use current transformers (CTs) which provide a scaled-down (secondary) version of the actual (primary) current. Scaling factors based on the CT ratios are used by the IEDs to calculate primary currents from the secondaries. Figure 2.2 below shows the current vectors at either end of an ideal healthy line.



Figure 2.2: Current Vectors on an Ideal Healthy Line (Siemens AG, 2009).

In mathematical terms, for an ideal healthy line

$$I_{Diff} = \left| \sum_{i=0}^{N} \underline{I}_{A} \underline{I}_{B} \right| = 0 \tag{2.1}$$

Differential current is never zero on real power lines due to capacitive losses. On a real and healthy line, the differential current is equal to the capacitive load current of the line (Siemens AG, 2009). So the differential current becomes

$$I_{Diff} = \left| \sum_{i=0}^{N} \underline{I}_{A} \underline{I}_{B} \right| = I_{C}$$

$$(2.2)$$

2.1.1 Effects of Communications Delays on Current Differential Protection

The currents waveforms at each end of a healthy line will be 180° out of phase. Adding the two waveforms together gives the differential current which should be close to zero. If the waveform sampling times are not synchronised, different sampling points will be compared and wrong tripping decisions will be made. Figure 2.3 below shows the apparent differential current caused by misaligned sampling. In this example a false-trip would occur since the magnitude of I_{diff} is greater than I_{dmin} .



inne(s)

Figure 2.3: Misaligned Current Waveforms (Antonova, Colmenares & Jankovic 2013).

2.1.2 Communications Delay Compensation

One method of compensating for communication delay when it is not feasible to use GPS reference clocks, is to use the '*ping-pong*' algorithm. This algorithm uses four time measurements collected in a round trip pair of messages between IEDs to synchronise their clocks. These round trip messages are continually exchanged to maintain synchronism between ends. The four time measurement events are shown in Figure 2.4.



Figure 2.4: Communications Delay Compensation using Ping-Pong (IEEE 2015).

Time stamps t_0 and t_3 are measured by relay A, t_1 and t_2 are measured by Relay B. The following will be true with regard to the first message:

$$t_1 - t_0 = t_f + T_{21} \tag{2.3}$$

where T_{21} = offset of clock at relay B with respect to clock at relay A, and t_f = communications delay in transmitting the first message.

The following will be true for the second message

$$t_3 - t_2 = t_r - T_{21} \tag{2.4}$$

where $t_r =$ communications delay in transmitting the return message.

The estimated communications delay, \hat{T}_{21} can then be estimated by

$$\hat{T}_{21} = \frac{t_1 - t_0 + t_2 - t_3}{2} = T_{21} + \frac{t_f - t_r}{2}.$$
(2.5)

In the equation above, $t_f - t_r$ is equal to the communications channel asymmetry. The *pingpong* estimate of the clock offset is equal to the actual clock offset plus one half of the channel asymmetry (Brunello et al. 2004). This highlights a major shortfall of the *ping-pong* method – that there will always exist an error time equal to half the communication channel asymmetry. Without GPS reference clocks this error is undetectable by the IEDs, and can lead to misoperation.

2.2 Synchronous and Plesiochronous Digital Hierarchies

Synchronous Digital Hierarchy (SDH) and Plesiochronous Digital Hierarchy (PDH) are two standards for Time Domain Multiplexing (TDM) communications over optic fibre. Both systems are commonly used for power system communications. The United States / Canadian equivalent of SDH is SONET, which is essentially the same. The hierarchy of a typical PDH structure is shown in Figure 2.5.



Figure 2.5: PDH Hierarchy (Wells 2001).

As the name suggests (plesiochronous), the timing in a PDH system can vary slightly from one piece of equipment to the next. To compensate, a process known as *bit-stuffing* is used, which adds extra bits to bring all input signals up to some common bit-rate. This *plesiochronous* timing and associated bit-stuffing is the reason that, as shown above, to extract a 2 Mbps signal from a 565 Mbps requires 'steps' of 565-34, 34-8 then 8-2 Mbps.

The main limitations of PDH are:

- Inability to identify individual channels in a higher-order bit stream.
- Insufficient capacity for network management.
- Most PDH network management is proprietary.
- There is no standardised definition of PDH bit rates greater than 140 Mbps.
- There are different hierarchies in use around the world. Specialised interface equipment is required to interwork two hierarchies.

Despite its limitations, PDH is still used for power system communications due to its interoperability with a wide range of end equipment and protocols. It is most often used to multiplex between E1 (2 Mbps) interfaces of SDH equipment, and lower bit rate (e.g. 64 kbps) Data Terminal Equipment (DTE) such as IEDs.

The main advantage of SDH over PDH is the fact that it is synchronous. This means that a signal can be multiplexed into and out of a higher bit-rate bearer of any level without having to use multiplexing *steps* like PDH. This is possible because the SDH standard specifies extremely precise timing across nodes in a network. Most SDH networks use a single Primary Reference Clock (PRC) which is propagated throughout the network from node to node. The Primary Reference Clock is usually derived from GPS. Care needs to be taken when designing SDH networks, not to create timing loops.

Another advantage of SDH over PDH is that it is capable of much higher bit rates. Table 2.1 outlines the PDH and SDH/SONET transmission level bit rates.

Designation	Bit Rate	Abbreviated	Capacity
PDH			
E0	64 kbps	64 kbps	One 64 kbps
E1 (D2)	2.048 Mbps	2 Mbps	32 E0
E2	8.448 Mbps	8 Mbps	128 E0
E3 (D34)	34.368 Mbps	34 Mbps	16 E1
E4 (D140)	139.264 Mbps	140 Mbps	64 E1
SDH/SONET			
STM-0 (SONET only)	51.84 Mbps	51 Mbps	21 E1
STM-1	155.52 Mbps	155 Mbps	63 E1 or 1 E4
STM-4	622.08 Mbps	622 Mbps	252 E1 or 4 E4
STM-16	2488.32 Mbps	2.4 Gbps	1008 E1 or 16 E4
STM-64	9953.28 Mbps	10 Gbps	4032 E1 or 64 E4
STM-256	39813.12 Mbps	40 Gbps	16128 E1 or 256 E4

 Table 2.1: PDH / SDH / SONET Transmission Hierarchies.

Figure 2.6 shows the organisation of the SDH multiplexing structure. The PDH tributary signals are framed in Containers (C-x), then Path Overheads (POH) are added to form Virtual

Containers (VC-*x*). Pointers are added to VCs to map their phase differences relative to the higher order SDH frame to form Tributary Units (TU), and TUs are interleaved byte-wise to form Tributary Unit Groups (TUG). Administrative Unit (AU) pointers are added, then AUs are interleaved into Administrative Unit Groups (AUG) which are framed into the STM-*n* bearer.



Figure 2.6: SDH Multiplexing Structure.

2.2.1 PDH / SDH Protection Switching

One desirable feature of PDH/SDH networks is their ability to quickly and automatically switch to alternate paths in the event of disruption to their primary paths. Protective switching can be applied at either the path or the circuit level by the SDH and/or PDH equipment.

Figure 2.7 shows an SDH path switched ring, whereby protection switching occurs at the VC level. VCs enter the ring at a node and are simultaneously transmitted in both directions. One direction will be designated the primary path, the other direction the secondary or protection

path. If a signal path failure is detected, switching occurs at the local multiplexer and the service is restored.

Figure 2.8 shows an SDH line switched ring. Line switching occurs at the STM-*n* level, which means that half of the available bandwidth must be reserved to provide the protected path. Restoration times and propagation delays are generally longer in line switched rings than in path switched.



Figure 2.7: SDH Path Switched Ring (Michel et al. 2004).



Figure 2.8: SDH Line Switched Ring (Michel et al., 2004).

Path level protection by SDH equipment occurs at the STM-n level, and is referred to as Multiplexer Section Protection (MSP). MSP is seldom used in modern SDH networks. More commonly used is the circuit level protection known as Sub Network Connection Protection (SNCP). SNCP carries out the protective switching within the SDH cross connect. It transmits signals in both the main and alternate directions, but under normal conditions only receives from the main. One advantage of SNCP is that it enables a single optical bearer to carry a combination of protected and unprotected circuits.

PDH protection is most commonly applied at the E1 level using protective E1 switching. Overhead bits in the E1 frame are used to trigger switching events. It is also possible to apply circuit level protection using protective 'Y' branches, which switch individual timeslots or groups of timeslots.

AusNet Services uses a combination of SDH SNC Protection at the VC-12 signal level, and PDH E1 protective switching in its communications network. Communications and protection equipment are duplicated for redundancy with separate X and Y equipment. X and Y communications equipment and routes are separated wherever practicable. Where this is not viable, X and Y communications nodes are connected together in single protective rings.

Although the SDH standards were developed to alleviate interoperability issues, vendors continue to add their own proprietary data to frames so that certain features will not work between vendors. Due to vendor interoperability issues, SNC Protection is not always possible when interfacing SDH nodes produced by different manufacturers. This is one of the contributing factors affecting asymmetrical communications delays described next.

2.2.2 Causes of Asymmetrical Communications Delays

The primary cause of asymmetrical communications delay is what is known as '*split path communications*'. Split path communications are the situation where the transmit (Tx) direction of a channel take a different path to the receive (Rx) direction. A simple example is illustrated by figure 2.9.



Figure 2.9: Split Path Communications Example (Carroll et al. 2002).

In this example, the primary path Rx direction has been disrupted at Site #1, causing it to switch to its alternate path, which traverses the long way around the ring. Because only a single fibre has been cut, Site #2 continues to receive from its primary (direct) path. The communications asymmetry is caused by the direct path having a shorter propagation delay than the long path. Table 2.2 outlines the propagation time for various fibre and microwave paths lengths.

Kilometres	Fibre	Microwave
1	4.9	3.3
10	48.9	33.3
20	97.8	66.7
50	244.6	166.7
100	489.2	333.3
250	1223.1	833.3
500	2446.2	1666.7
1000	4892.3	3333.3

Table 2.2: Medium Propagation Time (µs) (Michel et al. 2004).

Fibre and microwave propagation often account for only a small portion of the total propagation time. The total end-to-end delay between current differential relays includes:

• Relay interface, typically 1000 µs to 5000 µs

- Fibre propagation delay, 5 µs per km (as above)
- Through delays of intermediate devices (multiplexers), typically
 - 1. E1 substation multiplexer 370 µs
 - 2. Telephone company (telco) channel bank 1000 µs to 100 ms
 - 3. SDH multiplexers 200 µs.

The times quoted above are meant as very rough guidelines, taken from the IEEE guide. Equipment-specific delays are seldom documented by manufacturers. Of all the communications equipment tested in this project, the only documented delays found were those through Ceragon IP10G microwave radios. The delay figures listed in table 2.3 are taken from the Ceragon IP10G latency guide. The highlighted figures show the delays through Ceragon radios as configured in the AusNet Services communications network.

ACM working point	Modulation	Fixed Mode (µ	Modulation us)	ACM M	lode (µs)
		First hop in TDM trail	Any additional hop in TDM trail	First hop in TDM trail	Any additional hop in TDM trail
0	QPSK	663	426		
1	8 PSK	598	361		
2	16 QAM	533	296		
3	32 QAM	493	256	971	624
4	64 QAM	502	265	0/1	034
5	128 QAM	491	254		
6	256 QAM (Strong FEC)	496	259		
7	256 QAM (Light FEC)	485	248		

 Table 2.3: Ceragon IP10G E1 Latency – 28 MHz Channel Bandwidth.

In so-called *substation-class* SDH networks, long-term channel asymmetry is alleviated through the use of *bi-directional switching* which automatically switches both Tx and Rx directions in the event of a one-directional fault. Bi-directional switching is applied in SDH SNCP switching, but is not applied in early PDH E1 protective switching. Even when bi-directional switching is applied, there always exists a small switching delay between ends, meaning there is always a period of potential asymmetry when differential relays *may* misoperate. Whether or not this switching time is long enough to cause relay misoperation, is investigated as part of this project.

2.3 IEEE Recommendations

In June 2015 the *IEEE Guide for Application of Digital Line Current Differential Relays Using Digital Communication* was released. This document is intended as a guide to designers of line current differential protective relaying systems and their communications network.

2.3.1 Relay Recommendations

The guide covers the following pertinent points on current differential protection relaying:

- Dual slope restraint characteristic
- Alpha plane differential characteristic.

The dual slope restraint characteristic is illustrated by figure 2.10.



Figure 2.10: Dual Slope Restraint Characteristic (IEEE 2015).

The vertical axis represents the differential current I_d , the horizontal axis the restraint current I_r . The restraint current is that which the differential current must exceed before a trip will

occur. The minimum operating current I_{s1} is the minimum restraint current. It increases linearly with differential current, up to the cross over threshold I_{s2} . Above the crossover threshold the slope increases, so that the relays are more sensitive for low loads and less sensitive for higher loads when differential current errors are likely to be greater.

The alpha plane depicts the complex ratio I_R/I_L , where I_R and I_L are the remote and local currents. The IEEE guide states that *under balanced conditions, the two currents of the zone* $(I_L \text{ and } I_R)$ are equal in magnitude and opposite in phase. This yields an operating point on the alpha plane of $r = 1 \ge 180^\circ$. Under internal faults, the complex current ratio, r, departs from this ideal blocking point, allowing the alpha plane element to operate. The horizontal axis in Figure 2.11 represents the real part of the ratio, the vertical axis the imaginary part.



Figure 2.11: Current Ratio Plane (IEEE 2015).

The restraining region lies within the area formed by the blocking radius, R and its reciprocal 1/R, and the blocking angle, α . The blocking radius determines the sensitivity of the relays in terms of restraint current. Increasing R decreases the relays' sensitivity to current differential. The blocking angle represents the sensitivity to phase shift between relays.

The blocking angle component of the restraining region adds a degree of immunity to communication channel asymmetry. As described in section 2.1.1, when channel delay cannot be compensated for, it results in a phase shift between local and remote sensed currents. Increasing angle α de-sensitises the relays to this apparent phase shift.

2.3.2 Communications Network Recommendations

The IEEE guide notes that timing issues are of particular concern for relay communications over digital channels. It lists the following timing issues:

- End-to-end delay; excessive delay due to intermediate devices
- Variable delay, referred to as jitter or wander; changes in delay time from one period to another
- Asymmetry; different transmit and receive delay paths
- Interruptions and re-synchronisation delays following a switching operation on the communications network.

The guide recommends that *when using a multiplexed channel, the number of intermediate devices should be kept to a minimum*, and that *substation-class network equipment* may need to be deployed to support protective relay application. There is no mention of what constitutes 'substation-class' network equipment. Table 1 from the IEEE guide compares the requirements of data, voice and line differential relay data. It is reproduced below.

	Data (not time-critical)	Voice	Line differential relay
Delay (latency) tolerance	High	Moderate/low (50-100 ms)	Very low (<20 ms)
Jitter (variation in delay) tolerance	High	Moderate	Very low
Stream/burst transmission	Bursts	Stream	Stream
Error tolerance	Low	High	Very low
Packet/data loss tolerance	Moderate, by the application requesting retransmission	Some data loss is acceptable until voice quality becomes too low	No
Interruption tolerance	Yes, by the application requesting retransmission	Moderate (0.1 s)	None/very low
Protocol standard	Proprietary/standardised	Standardised	Proprietary

Table 2.4: Comparison between Data, Voice, and Line Differential Relay Data (IEEE, 2015).

Although the table states few real values, it does give an appreciation of the strict requirements imposed on communications channels carrying line current differential protection traffic.

Section 6.5.2 of the guide discusses the bi-directional switching method used to eliminate the chance of split-path-communications, as described in section 2.2.2 of this document. Figure 10 from the IEEE guide illustrates the concept of bi-directional switching. It is reproduced below.



Figure 2.12: SONET Bi-Directional Switching (IEEE, 2015).

In the event of a one-way fault in the primary path, both Rx and Tx directions will switch to the back-up path. The guide points out that bi-directional switching can result in increased channel delay, but that it is more important to ensure equal channel delay times between relays.

One potential shortfall of bi-directional switching is that the Tx and Rx directions do not switch at exactly the same time. Following the one-way failure on the primary path in figure 2.12, the SONET node in Substation A will switch to the back-up path almost immediately. The node in Substation A must then send an Alarm Indication Signal (AIS) to the SONET node in Substation B to instruct it to switch to the alternate path. The AIS signal takes a finite

time to propagate from Substation A to Substation B, thus for a short period there will be asymmetrical delays.

The guide discusses the use of GPS synchronisation to line current differential relays for systems where asymmetrical communications delays are unavoidable. It states that GPS synchronisation is a viable option to add some immunity to asymmetrical delays, however it stresses that care needs to be taken when designing GPS synchronisation systems. It states that poor GPS clocking designs have resulted in false tripping.

2.4 Summary

When used to transport line current differential protection signals, the symmetry of communications channel delays is critical. Asymmetrical communications delays cannot be accurately detected by IEDs without GPS reference clocks, meaning they can lead to false-trips. Substation-class SDH communications systems are supposed to avoid the possibility of asymmetrical delays by using bi-directional switching to switch both Tx and Rx directions in the event of unidirectional disruptions.

It is predicted that relays may still misoperate from asymmetrical communication channel delays in systems with bidirectional-switching, due to the communications nodes switching at slightly different times. This situation was not covered in any of the research material reviewed. Its potential impact will be investigated through testing as part of this project.

There appears to be little published research material on multi-vendor SDH/PDH communications networks used in power systems. As described above, there still exists some interoperability problems when interfacing equipment from different vendors, even when using supposedly standardised SDH equipment. These networks create unique challenges for designers of power system communications networks, who must consider not only the technical, but also the economic feasibility of their designs.

Microwave radio links are often used in power system communications networks in areas where it is impractical or uneconomical to run fibre cables. There is little modern published literature on power system microwave communication systems and the effects of their errors on line current differential protection relays.

CHAPTER 3 - AusNet Services' Communications Network

This chapter provides an overview of AusNet Services' communications network. It details the equipment vendors, technologies and physical transport media used, and provides examples of the types of topologies used in its transmission and distribution communications networks. For security reasons, some details have been deliberately omitted.

The AusNet Services communications network covers most of Victoria, using a combination of fibre optic cable and microwave radio links. It is used to transport a range of traffic types including protection, SCADA, operational telephone and third-party circuits.

3.1 Backbone Network

As of 2016, the majority of AusNet Services' communications backbone is a ring/mesh network made up of SDH STM-n bearers over fibre and OFDM microwave radio links. The system is almost completely duplicated, with X and Y equipment running independently. Single points-of-failure are avoided wherever possible using duplicated equipment, power supplies, cables and radio links.

There is one communications network used for power transmission circuits and one used for power distribution circuits. Interconnections between the two networks are kept to a minimum. The backbone transmission network is made up of predominately Siemens and Ericsson Marconi SDH equipment and Ceragon microwave radios. The distribution network is made up of mainly ZTE SDH equipment and Ceragon microwave radios. Figures 3.1 and 3.2 below are representations of small sections of the transmission and distribution networks.

The transmission network and the communications that support it are generally considered more important than the distribution network. Thus, much more time, effort and money are spent ensuring the security and dependability of the transmission communications network. At the time of writing, the cost of an Ericsson Marconi SDH node is around 15 times that of a ZTE SDH node. As shown in figure 3.2, transmission communications equipment is sometimes used to carry distribution circuits. Distribution communications equipment is never used to carry transmission circuits, since it does not meet the transmission security or dependability requirements.

The DWDM and CWDM equipment shown in figure 3.2 are used to congregate more circuits onto less fibres, when using third-party fibre cables to transport traffic. AusNet Services owns much of the state's power poles and towers, making it relatively cheap to install overhead fibre optic cables. Thus there is generally little need to minimise the number of fibre cores used in cables.



Figure 3.1: Section of Transmission Communications Network.



Figure 3.2: Section of Distribution Communications Network.

3.2 Digital Interface Equipment

There still exists a need to use what is now considered *legacy* PDH equipment, as the lowest level interface on the SDH equipment used by AusNet Services is the electrical E1 (2 Mbps) interface, and most end equipment used requires a 64 kbps interface. The PDH / digital interface equipment used by AusNet Services has been exclusively Nokia Siemens equipment for many years. Nokia Siemens have stopped making and supporting their PDH equipment so it is gradually being replaced by Avara equipment.

Figure 3.3 below is an example of how PDH equipment typically interfaces with SDH in the transmission communications network. The coloured lines represent STM-*n* optical connections, the thin black lines are electrical E1 connections.



Figure 3.3: Typical Transmission PDH Connections.

The green icons represent Nokia DB2T or Avara DB4 branching cards - they can be considered the same at this point. As configured by AusNet Services, they have one main and one standby E1 connection. The main connections are indicated by the black dots in figure 3.3. Both connections are monitored, and under normal conditions the main connection will be the active. If a fault is detected on the main connection, the card will automatically switch to the standby. The cards pass the E1 signals to the frame backplane, to which up to 14 digital interface unit (DIU) cards are connected. The DIUs multiplex/ demultiplex the lower level (usually 64 kbps) signals into and out of the 2 Mbps E1 signal and encode them using the desired protocol. An E1 signal can carry up to 30 64 kbps channels, referred to as *timeslots*. The DIUs are not shown in figure 3.3.

The Avara DB4 cards have several features which the older Nokia DB2T cards do not.

- Up 4 E1 interfaces plus backplane. DB2Ts gave 2 E1 interfaces plus backplane, or 3 E1 interfaces without a backplane connection.
- Ability to interface with and carry Ethernet traffic.
- Ethernet/ serial management connectivity.
- User upgradable firmware.
- *Bi-directional switching* capability, eliminating the chance of long-term split-path-communications resulting in channel asymmetry.
The addition of bi-directional switching is the most attractive feature of the Avara DB4 cards when used to transport current differential protection circuits. No testing has yet been conducted by AusNet Services to prove its effectiveness. Testing will be carried out as part of this project.

The typical PDH connections used in the distribution communications network are shown in figure 3.4. They are slightly different to those in the transmission network.



Figure 3.4: Typical Distribution PDH Connections.

The first difference is that Nokia DB2B E1 branching cards are used rather than DB2Ts. Instead of having a main and standby E1 interface, DB2B cards have interfaces designated *direction 1* and *direction 2*. Direction 1 is indicated by the black dot in figure 3.4. The backplane is given the designation *direction3*. Timeslots can be programmed to pass between any two of the three directions in what are known as *branching tables*.

Because DB2B cards do not have protective switching capability, CO2 change-over cards are used to achieve this function. CO2 cards are similar to DB2Ts, but instead of passing the active E1 signal to the backplane they pass it to another E1 interface, which is connected to a direction of the DB2B card in this configuration. As with DB2Ts, CO2s do not have bi-directional switching capability.

An SDH node failure will not result in loss of E1 traffic in the transmission configuration, but will in the distribution configuration. Distribution E1 connections are configured this way because it is not usual to have more than one fibre cable between any two distribution sites, so the SDH nodes are connected in a predominately ring network. An X E1 circuit would generally use the most direct path between sites for its main interface, and use the long way around the loop for its alternate. Its equivalent Y E1 circuit would use the long way around the loop as its main path, and the direct as its alternate. This way a single fibre break will not disrupt the main path of both X and Y circuits. It is acceptable to have less redundancy in the distribution communications network as its traffic is not considered as critical as that in the transmission network.

CHAPTER 4 - Methodology

This chapter outlines the methodology used to complete this project. It details the various project phases and tasks within each phase. It explains the test equipment and testing methods used to measure the required delay and asymmetry figures.

4.1 **Project Structure**

The project was conducted in the following phases:

Research -	Research was conducted on line current differential protection,
	SDH/PDH communications, past causes and remedies to communications
	channel asymmetry.
Preparation -	Study AusNet Services' communications network and its defect history to
	identify potential testing paths. Obtain authorisation to access sites and create testing trails.
Measurement -	Use test equipment to measure actual communications channel delays and
	their effect on current differential protection relays.
Data analysis -	Compile and analyse the measured and theoretical data. Create and test a
	model to be used to predict the latency between any given points on
	AusNet Services' communications network.
Write-up -	Compile all results into dissertation and presentation.

Table 4.1 outlines the individual tasks to be carried out in each phase.

The timing of each project task is shown on the project timeline in Appendix C. This was the *planned* timeline created in late 2015 as part of the project proposal. The *actual* project timings were very close to those planned. The main differences were some last-minute DB4 switching and relay response tests requested by Avara staff to test their latest firmware build.

Phase 1	Research Phase
1A	Gather Resource Literature – Search libraries, databases, manuals and company
	documentation for material relating to the project. This activity will likely
	continue throughout the life of the project to varying degrees.
1B	Sort and Study Literature – Sort literature into subject areas. Highlight and take
	notes on important points. Gain a thorough understanding of pertinent points.
Phase 2	Preparation Phase
2A	Study Communications Network – Study AusNet Services' communications
	network and its defect history to identify existing/potential sources of
	asymmetrical delays and potential testing paths.
2B	Obtain Authorisation to Test – Contact relevant stakeholders to obtain
	authorisation to access sites and create/test communications paths.
Phase 3	Measurement Phase
3A	E1 Delay Testing – Measure propagation delays at the E1 level using Albedo
	Ether.Genius communication system testers.
3B	<u>C37.94 Delay Testing</u> – Measure propagation delays at the C37.94 level using
	Ether.Genius testers.
3C	<u>DB4 Testing</u> – Connect two Avara DB4 cards via test E1 circuits to measure
	their bi-directional switching performance.
3D	<u>Relay Testing</u> – Connect two current differential relays using a communication
	channel with variable asymmetry and observe its effects on relay performance.
3E	<u>Relay Testing through DB4s</u> – Connect two current differential relays through
	communications circuits using DB4s to measure the effects that the bi-
	directional switching has on relay performance.
Phase 4	Data Analysis Phase
4A	<u>Compile Measured Data</u> – Compile all measured delay data in a logical way.
4B	Analyse Measured Data – Analyse measured data to determine sources of delay
	and find any delay anomalies. Create a model to predict delays across points on
	AusNet Services' communications network.
4C	Compare Data – Compare measured and researched data to compare AusNet
	Sevices' network with those of other utilities and with industry standards.
Phase 5	Write-Up Phase
5A	Draft Dissertation – Compile all findings into a draft dissertation. Submit to
	supervisor for review and feedback.
5B	Finalise Dissertation – Make necessary changes based on supervisor feedback
	and submit finalised dissertation.

4.2 Test Equipment

The test equipment predominately used was the Albedo Ether.Genius, shown in figure 4.1. This unit is primarily an Ethernet tester, but also has Datacom capabilities which include the G.703 and C37.94 protocols. The features that makes the Ether.Genius particularly suited to this project are its ability to measure one-way delay and asymmetry using GPS synchronisation.



Figure 4.1: Albedo Ether.Genius Ethernet, E1 and Datacom Tester.

The Net Research NetProbe 2000 does not have one-way delay or asymmetry testing functionality, which makes it unsuitable for the delay measurements required for the project. What it can do is monitor bit statuses within individual timeslots of E1 bearers. This was used in later stages of the testing, to monitor switching statuses of DB4 E1 branching cards.



Figure 4.2: Net Research NetProbe 2000 Communications System Tester.

The Anritsu MT1000A Network Master Pro OTDR with transport module was used to inject known signals into single timeslots of E1 bearers, while passing all overhead signals without change. This was used in conjunction with the NetProbe 2000 testers, to monitor DB4 switching statuses.



Figure 4.3: Anritsu MT1000A Network Master Pro OTDR.

The Hioki MR8847 Memory HiCorder event recorder was used to monitor the DB4 switching statuses directly using the header pin breakout cables supplied by Avara Technologies engineers during the later stages of testing. This method of monitoring made the Anritsu and NetProbe 2000 testers unnecessary.



Figure 4.4: Hioki MR8847 Memory HiCorder Event Recorder.

4.3 Communications Tests

4.3.1 E1 One-Way Delay

Two Ether.Genius testers were connected to each other through the communications circuit under test. As outlined in section 1.2, the majority of the testing was conducted at the E1 level. Figure 4.5 shows a typical test setup. In this simple example the tester at site A traverses site B to connect to site C. The lines between SDH nodes are fibre-connected STM-n bearers, the lines inside the nodes are VC12 cross-connects. Using this method, the testers could be connected between any two sites on the network simply by programming the necessary SDH cross-connects.



Figure 4.5: Typical E1 Test Setup.

The first stage of E1 testing was conducted across the same equipment types through varying fibre and microwave radio link lengths. The resulting data was used to calculate the perkilometre delays through fibre and microwave radio links.

Delay testing was then carried out across as many different types of communications equipment as practicable. Since the delays through the transmission media were already calculated, it was now possible to estimate the delays caused by the communications equipment. The data was used to create a model to estimate the delay between any two points in the AusNet Services communications network.

With the estimated communications delays calculated it was then possible to estimate the potential delay asymmetry due to split-path-communications between any two points. As detailed in section 3.2, all E1 bearers carrying protection traffic are protected by an alternate route, so that a single link loss will not result in loss of E1 traffic. The potential asymmetry of an E1 circuit was estimated by calculating the difference between its main and alternate routes.

4.3.2 C37.94 One-Way Delay

Due to the limited number of available C37.94 interfaces in the AusNet Services communications network, there will be few delay tests conducted through C37.94 channels. As mentioned in section 1.2 there is little to be gained by testing at the C37.94 level, as preliminary testing revealed that there is a practically constant delay between the C37.94 and E1 levels across all circuits. Some C37.94 delay testing was carried out however, because this is the interface to which most new current differential protection relays connect. A simple C37.94 delay test setup is shown in figure 4.6.



Figure 4.6: C37.94 Test Setup.

The Ether.Genius testers connect via fibre to the Avara C37.94 DIU cards. The C37.94 signals are passed to the DB2 branching cards via the backplane of the frames. The DB2s multiplex the signals into E1 bearers which are cross-connected through SDH nodes the same as before, to pass them between ends.

4.3.3 DB4 Switching Performance

As outlined in section 3.2, AusNet Services is beginning to replace Nokia DB2T cards with Avara DB4s, as Nokia cards are no longer being supported. The DB4's ability to perform bidirectional switching make them an attractive alternative. The test setup shown in figure 4.7 was used to test how the DB4 cards perform when subjected to E1 faults in one direction only. Note that logical representations of the PDH/ DIU equipment are now used.

The Albedo Ether.Genius testers were used to monitor delay and asymmetry as before. The Anritsu OTDR with transmission module was added to inject a known signal (all ones) into

timeslots 29 and 31 of the backup E1 bearers, and the Net Research NetProbe 2000 testers were added to monitor these timeslots to identify which direction of the DB4 cards were active at any given time.



Figure 4.7: Short Term Asymmetry Test Setup.

4.4 Relay Tests

4.4.1 Relay Response to Asymmetrical Communications

The next stage of testing involved connecting pairs of L90 line current differential protection relays via a communications path with variable asymmetry to record the effect that long-term asymmetry had on relay performance. The variable asymmetry was achieved by directly connecting one direction of the E1 bearer between branching cards, and passing the other direction through a variable number of SDH nodes. Figure 4.6 illustrates how this was done. Note that the two black lines connecting to the DB2 cards represent the two directions of a single E1 bearer.

The ring-connected SDH nodes are part of the AusNet Services communications network. The PDH frames, relays and testers make up a laboratory test setup. The asymmetry was increased by programming SDH cross-connects to increase the number of times the E1 signal loops around the SDH ring. The tester and relay C37.94 signals are multiplexed into different timeslots of the same E1 bearer, so that they are both subjected to the same asymmetry. This way the asymmetry was monitored on the testers while its effects were observed on the relays.



Figure 4.8: Relay Asymmetry Response Test Setup.

The effects of communications asymmetry were also tested on a pair of SEL 311L relays. Because the SEL relays make their trip decision based on the alpha plane, no practical amount of communication asymmetry would cause them to trip when using relay restraint settings used by AusNet Services. Thus, no further tests were carried out using SEL relays.

4.4.2 Relay Response to DB4 Switching

To measure the effects of DB4 bi-directional switching on L90 current differential relays, the test setup shown in figure 4.9 was used. Not shown in the figure was a Doble protection tester

connected to the relays to provide simulated line loads. A photograph of the test setup, excluding the SDH equipment, is shown in figure 4.10. Note that the Hioki memory recorder is now used to monitor DB4 switching times.



Figure 4.9: Relay DB4 Switching Response Setup.



Figure 4.10: Photograph of Relay Test Setup.

If it performs perfectly, bi-directional switching should result in no false differential current seen by the relays during a DB4 switch-over due to link failure on the main communications path. However, this had not been tested by AusNet Services before, so the relay response to DB4 switching was unknown at that point in time. The Hioki memory recorder was included in this test setup to record the DB4 switching statuses and relay CB trip commands, so that the timing of any relay false trips could be captured during simulated communications faults.

4.5 Calculating and Documenting Results

The testing resulted in a large amount of data. Microsoft Excel was used to store, manipulate and plot the testing data. The layout and inbuilt functions of Excel made it ideally suited for this type of application. The simultaneous equations required to estimate per-unit communications delays were calculated using both Excel and MATLAB. The calculated values from Excel and MATLAB were compared, and the results deemed most accurate were used in the delay model.

The testing data alone did not provide many meaningful results. AusNet Services documents its communications network using a geographic information system (GIS) application made by General Electric called Smallworld SDMT. Information such as fibre/ microwave radio routes, circuit paths and programming sheets was extracted from SDMT and combined with the testing data to calculate useful results. Current differential relay settings and response templates were used to help calculate the theoretical response of relays to communication channels with asymmetrical delays.

Certain information such as site names and locations were omitted from the documented results to comply with privacy, security and marketing constraints imposed by AusNet Services. This did not detriment the project, as all technical data was maintained.

CHAPTER 5 – Experimental Results and Discussion

This section presents the results of all project measurements and calculations. It outlines delay results and relay responses to communications asymmetry. It lists the results of DB4 E1 protective switching tests and its effects on L90 relay performance. It then shows the results of DB4 tests using an updated firmware build that Avara engineers released in response to identified design flaws.

5.1 Communications Test Results

5.1.1 E1 Delays

The results of E1 delay tests and calculations are summarised in table 5.1. Some characters are omitted from site names to anonymise them. Fibre and radio link lengths are taken from documented OTDR test results. When these results could not be found, OTDR traces where run at the time of delay testing. Each delay measurement was run for approximately five minutes. When there was a difference between the maximum and minimum delay measured, the average value was taken.

Table 5.1 shows only a short summary of the E1 delay tests carried out. It was identified early that there appeared to exist delay asymmetry within nodes. E.g., the delay from an E1 to an STM-n port of an SDH node appeared to be different to the delay in the other direction. The exact difference in delays was difficult to measure, since the testers used can only interface at the E1 ports of SDH nodes. To estimate asymmetry within nodes, multiple tests were carried out between nodes of different types. Figure 5.1 shows example asymmetry results from such tests. All delay results were tabled together as matrices to be solved using Excel and MATLAB.



Figure 5.1: Example Mixed-Equipment Delay Test Setup and Results.

	Distanc	e (km)	Forward	Return		
	Fibre	Radio	Delay (ms)	Delay (ms)		
ZTE - ZTE SDH						
H***3-H***7	0.003		0.173	0.158		
H***3-T**	28,138		0.321	0.293		
T**-S**	55.582		0.468	0.474		
S**-M**	20.823		0.329	0.336		
M**-B**	68.000		0.554	0.552		
B**-B***	12.016		0.293	0.307		
S**-F** (via MRV)	134.000		0.848	0.832		
F**-1**	45,480		0.405	0.404		
_ ·	58,500		0.470	0.471		
H***7-M***3	3,330		0.184	0.193		
M***-M*N	5.085		0.224	0.228		
M*N-Y****	11.388		0.244	0.255		
Y****-M*W	20.489		0.286	0.288		
M*W-H***	11.252		0.241	0.249		
M*W-M*S	7.759		0.217	0.223		
M***-M*E	2.057		0.199	0.194		
H***3-T**-S**	81.286		0.575	0.620		
H***3-T**-S**-M**	102.224		0.749	0.804		
H***3-T**-S**-M**-B**	171.208		1.073	1.126		
H***3-T**-S**-M**-B**-B***	183.355		1.204	1.244		
H***3-T**-S**-M**-B**-B***-M**L	183.355	13.738	1.907	1.867		
H***3-T**-S**-M**-B**-B***-M**L-S**	183.355	73.685	2.459	2.674		
H***3-T**-S**-M**-B**-B***-M**L-S**-F**	317.200	73.685	3.532	3.428		
H***3-T**-S**-M**-B**-B***-M**L-S**-F**-L**	362.303	73.685	3.821	3.757		
H***3-T**-S**-M**-B**-B***-M**L-S**-F**-L**-W**	420.214	73.685	4.138	4.052		
Ericsson - Ericsson SDH						
H***5-H***6	0.008		0.177	0.163		
H***-L****	20.539		0.278	0.266		
H***-J***	0.966		0.182	0.187		
J***-M***	3.250		0.193	0.179		
M***-Y****	12.829		0.240	0.264		
H***5-J***-M***	4.216		0.188	0.175		
H***5-J***-M***-Y****	17.045		0.224	0.226		
H***5-J***-M***-Y****1-Y****2	17.045		0.326	0.324		
H***5-J***-M***-Y****1-Y****2-Y***A-J***(Y)	17.045		0.354	0.339		
H***5-J***-M***-Y****1-Y****2-Y***A-J***(Y)-J***	17.045	22.000	1.049	0.927		
H***5-J***-M***-Y****1-Y****2-Y****A-J***(Y)-	47.045	22.000	1 200	4 470		
J***-J***(H)-H***r	17.045	22.000	1.208	1.176		
H***5-J***-M***-Y****1-Y****2-Y****A-J***(Y)-	17.445	30.110	1.877	1.734		
Ceragon - Ceragon Microwave Radio						
B***-M***		15.400	0.620	0.612		
M**L-S**		60.000	0.814	0.785		
		8.110	0.534	0.540		
J***-L***A		13.800	0.558	0.554		
J***-Y****A	1	22.000	0.584	0.585		

 Table 5.1: Summary of Measured E1 Delays.

To create a delay model for the whole AusNet Services communications network, delays had to be estimated through certain key interface points. The first delays to be estimated were the per unit distance delays through air and fibre, which could be calculated from the speed of light. The speed of light in a vacuum is 299,792,458 m/s. It is slowed at sea level by the refractive index of air, which at standard temperature and pressure is n = 1.0002926. This is close enough to unity to be ignored, thus the per metre delay of microwave radio links through air could be calculated as

$$\Delta t_{radio} = 299,792,458^{-1} = 3.33564 \, ns/m. \tag{5.1}$$

To make values more easily recognisable, the base units used throughout the project were kilometres and milliseconds. Thus, the figure for radio delay becomes

$$\Delta t_{radio} = 3.33654 \times 10^{-9} \times 10^{6} = 3.33654 \, ms/m$$
$$= 0.00333654 \, ms/km. \tag{5.2}$$

The refractive index of the single-mode fibre optic cable used by AusNet Services is n = 1.4677. The signals passing through the fibre are slowed down by this factor, so the per kilometre delay through optic fibre could be calculated as

$$\Delta t_{fibre} = 0.00333654 \times 1.4677 = 0.00489572 \, ms/km. \tag{5.3}$$

These delay figures were compared with measured values and were deemed accurate.

The next delays to be calculated were those through cross-connections of communications nodes. It was decided that there were nine types of node delays to be considered:

- From an E1 to an STM-n port of a ZTE SDH node
- From an STM-n to an E1 port of a ZTE SDH node
- Between STM-n ports of a ZTE SDH node
- From an E1 to an STM-n port of an Ericsson SDH node
- From an STM-n to an E1 port of an Ericsson SDH node
- Between STM-n ports of an Ericsson SDH node
- From an E1 to the radio port of a Ceragon microwave radio
- From the radio to an E1 port of a Ceragon microwave radio
- Between STM-n and radio ports of a Ceragon microwave radio.

Dist	ance		ZTE			ERI			Rad			
2100		F1-	STM-	STM-	F1-	STM-	STM-	F1-	Rad-	STM-	Measured	
Fibre	Radio	STM	F1	STM	STM	F1	STM	Rad	F1	Rad	Delay	
0.003	nauto	1	1	0	0	0	0	0	0	0	0.1725	
28.138		1	1	0	0	0	0	0	0	0	0.3210	
55.582		1	1	0	0	0	0	0	0	0	0.4680	
20.823		1	1	0	0	0	0	0	0	0	0.3285	
68.000		1	1	0	0	0	0	0	0	0	0.5540	
12.016		1	1	0	0	0	0	0	0	0	0.2930	
134.000		1	1	0	0	0	0	0	0	0	0.8480	
45.480		1	1	0	0	0	0	0	0	0	0.4050	
58,500		1	1	0	0	0	0	0	0	0	0.4700	
3.330		1	1	0	0	0	0	0	0	0	0.1840	
5.085		1	1	0	0	0	0	0	0	0	0.2240	
11.388		1	1	0	0	0	0	0	0	0	0.2435	
20.489		1	1	0	0	0	0	0	0	0	0.2860	
11.252		1	1	0	0	0	0	0	0	0	0.2405	
7.759		1	1	0	0	0	0	0	0	0	0.2170	
2.057		1	1	0	0	0	0	0	0	0	0.1990	
	15.400	0	0	0	0	0	0	1	1	0	0.6200	
	60.000	0	0	0	0	0	0	1	1	0	0.8140	
	8.110	0	0	0	0	0	0	1	1	0	0.5335	
	13.800	0	0	0	0	0	0	1	1	0	0.5575	
	22.000	0	0	0	0	0	0	1	1	0	0.5840	
0.008		0	0	0	1	1	0	0	0	0	0.1830	
20.539		0	0	0	1	1	0	0	0	0	0.2665	
0.966		0	0	0	1	1	0	0	0	0	0.1760	
3.250		0	0	0	1	1	0	0	0	0	0.1935	
12.829		0	0	0	1	1	0	0	0	0	0.2480	
4.216		0	0	0	1	1	1	0	0	0	0.2240	
17.045		0	0	0	1	1	2	0	0	0	0.3260	
17.045		0	0	0	1	1	3	0	0	0	0.3540	
17.045	22.000	0	0	0	1	0	4	0	1	1	1.0490	
17.045	22.000	0	0	0	1	1	4	0	0	2	1.2080	
17.045	30.110	0	0	0	1	0	5	0	1	3	1.8765	
17.445	30.110	0	0	0	1	1	5	0	0	4	2.0390	
81.286		1	1	1	0	0	0	0	0	0	0.5745	
102.224		1	1	2	0	0	0	0	0	0	0.7485	
171.208		1	1	3	0	0	0	0	0	0	1.0725	
183.355		1	1	4	0	0	0	0	0	0	1.2035	
183.355	13.738	1	1	4	0	0	0	1	1	0	1.9070	
183.355	73.685	1	1	4	0	0	0	2	2	0	2.4585	
317.200	73.685	2	2	4	0	0	0	2	2	0	3.5315	
362.303	73.685	2	2	5	0	0	0	2	2	0	3.8210	
420.214	73.685	2	2	6	0	0	0	2	2	0	4.1380	
0.003		1	0	0	0	1	0	0	0	0	0.1050	
0.003		0	1	0	1	0	0	0	0	0	0.2735	
0.011		1	0	0	0	1	1	0	0	0	0.1325	
0.011		0	1	0	1	0	1	0	0	0	0.2650	
0.011		1	0	1	0	1	0	0	0	0	0.1385	
0.011		0	1	1	1	0	0	0	0	0	0.2825	
0.014		1	0	1	0	1	1	0	0	0	0.1610	
0.014		0	1	1	1	0	1	0	0	0	0.2720	

 Table 5.2: Measured Delays and Distances/ Nodes Traversed.

Table 5.2 shows only the measured forward delays. For calculation purposes, the return delay results were also included. The numbers in the cross-connection columns show how many of the various types of cross-connections are traversed by the circuits under test.

The cross-connection delays were calculated independently using both Excel and MATLAB. In Excel using the inbuilt *Solver* add-in, and in MATLAB using the *pinv* (Moore-Penrose pseudoinverse) function.

The delays were calculated in Excel as follows:

- All distance, nodes traversed and delay data tabled together in a logical manner.
- Initial estimations of node delays tabled.
- Estimated per-node delay values used to calculate the estimated end-to-end delays.
- Percentage differences between estimated and measured delays calculated and tabled.
- GRG Nonlinear solver applied, setting it to minimise the objective cell being that containing the average percentage error between estimated and actual delays, and setting the changed variables to the cells containing the estimated node delays. Figure 5.2 is a screenshot showing how this was achieved.

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-	kr	n 0	SED	Rnd-tri	n delav	Forwar	delav	Av	Calc	n	4	Return	delay	Av	Calc	<u>u</u>	~	Asym	netry	0		Start Time
	Meas	SDMT		Min	Max	Min	Max	- direct	fwd	Diff	Err	Min	Max	- direct	rtn	Diff	Err	Min	Max			June
ver Pa	aramete	rs												×								
_		_			_				-	-					A	Actual De	lay	Estimate	d Delay	Di	ff	
															Up		Back	Up	Back	Up	Back	Up
Set	Objectiv	e:		ŚW	\$111								- 1		0.575		0.620	0.633	0.633	0.059	0.013	10
															0.749		0.804	0.777	0.777	0.029	0.027	3
Tor									0						1.0/3		1.126	1.157	1.157	0.084	0.031	
10.	0) <u>M</u> ax		🔘 Mij	<u>n</u>	© <u>∨</u> a	lue Of:		0					E	1.204		1.244	1.258	1.258	0.055	0.014	4.
															1.907		1.86/	1.865	1.817	0.044	0.050	2
<u>B</u> y	Changing) Variab	le Cells	:										Ľ	2.459		2.6/4	2.376	2.022	0.082	0.052	3
ŚR	\$112:\$R	\$114.\$F	(\$117:	sR\$119	.\$R\$122	2:\$R\$124							1		3.552		3.428	3.4/1	3.4/1	0.061	0.043	1
							•								5.021		5./5/	5.755	5.755	0.088	0.025	2
cb	viact to t	ha Canr	trainte												4.150		4.052	4.055	4.055	0.075	0.007	1
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										^		Add										
											()	Change			Estimated	d delays						Average % E
															ZTE							5
												Delete			E1-STM		0.072460					
												Delete			STM-E1		0.120960					Av Difference
															STM-STM		0.041765					0.
											R	eset All	_									
															ERI							
															E1-STM		0.133962					
										÷	Lo	aujsave			STM-E1		0.043462					
V	Ma <u>k</u> e Ur	nconstra	ained V	ariables	Non-Ne	gative									STM-STM		0.023181					
Sele	ect a Sol	ving Me	thod:		GRG	Nonlinea	ar .			-	(Dotions			IP10							
															E1-Rad		0.258561					
Se	olvina Me	thod													Rad-E1		0.300561					
Se	elect the	GRG No	nlinea	engine	for Solv	er Probl	ems tha	at are sm	nooth na	nlinear.	Select t	he LP Sim	plex		STM-Rad		0.382029					
er	ngine for	linear S	olver P	roblems	, and se	elect the	Evoluti	ionary er	ngine for	Solver	problem	s that are	2		PDH							
no	on-smoot	h.													F1.52		0.0060					
															F1-F2-F2		0.0060					
															-1-62-65		0.0005					
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	Ticib								201/6			CIOS			Per and							
			/												Eibre		0.004896					

Figure 5.2: Screenshot of Excel Solver Method of Node Delay Calculation.

To calculate the cross-connection delays using MATLAB, the following script was written.

The Excel worksheet read by the script is similar to that shown in table 5.2.

```
clear all
close all
clc
xlsdata = xlsread('F:\ERP2016\Delays to MATLAB.xlsx','B3:M94');
fibre dist = xlsdata(:,1);
radio dist = xlsdata(:,2);
fibre per km = (1./299.792) . *1.4677;
radio per km = 1./299.792;
fibre delay = fibre dist.*fibre per km;
radio_delay = radio_dist.*radio_per_km;
A = xlsdata(:, 3:11);
delay = xlsdata(:,12)-fibre delay-radio delay;
per km delays = pinv(A)*delay;
fprintf('\n')
fprintf('\tZTE SDH\n')
fprintf('\t\tE1-STMx:\t%.8f ms\n',per km delays(1))
fprintf('\t\tSTMx-E1:\t%.8f ms\n',per km delays(2))
fprintf('\t\tSTMx-STMx:\t%.8f ms\n',per km delays(3))
fprintf('\n')
fprintf('\tEricsson SDH\n')
fprintf('\t\tE1-STMx:\t%.8f ms\n',per km delays(4))
fprintf('\t\tSTMx-E1:\t%.8f ms\n',per km_delays(5))
fprintf('\t\tSTMx-STMx:\t%.8f ms\n',per km delays(6))
fprintf('\n')
fprintf('\tCeragon Radio\n')
fprintf('\t\tRadio-E1:\t%.8f ms\n',per km delays(7))
fprintf('\t\tE1-Radio:\t%.8f ms\n',per km delays(8))
fprintf('\t\tSTMx-Radio:\t%.8f ms\n',per km delays(9))
```

The script works as follows:

- The *xlsread* command extracts the relevant delay data from the specially formatted Excel delay worksheet.
- Fibre and radio distance measurements are extracted from the first two columns and stored as separate arrays.
- Fibre and radio delays are calculated and then subtracted from the measured delays to find the delays due only to cross-connections through nodes.
- The *pinv* command is used to calculate the Moore-Penrose pseudoinverse of the node cross-connection and delay data, to estimate the delay for each type of cross-connection.
- Results are displayed.

The results of the Excel solver and MATLAB pseudoinverse methods of node delay calculations are shown in table 5.3. The fact that the two independent methods provided such similar values helped to validate the results.

Calculated Delays (µs)										
	Excel Solver	MATLAB pinv								
ZTE SDH										
E1-STM	63.4488	72.4600								
STM-E1	121.576	120.960								
STM-STM	33.4602	41.7648								
Ericsson SDH										
E1-STM	137.052	133.962								
STM-E1	40.5365	43.4617								
STM-STM	23.4753	23.1805								
Ceragon Radio										
E1-Radio	257.204	258.561								
Radio-E1	303.170	300.561								
STM-Radio	378.331	382.029								

Table 5.3: Excel and MATLAB Calculated Node Delays.

The average percentage error calculated by the Excel worksheet using the node delay values calculated by its solver was 4.435%. When using the MATLAB calculated node delays, the average percentage error was 5.621%. However, a plot of calculated and actual delays showed a better fit using the MATLAB calculated values. The MATLAB code also uses far more sophisticated algorithms to calculate best-fit than the relatively simplistic average error target using the Excel solver. For these reasons, the MALAB calculated values were those chosen to create the delay model. Figure 5.3 shows the difference between the predicted and actual forward delays, using the total distance traversed by the circuits (fibre + radio) as a reference. A plot of return delays was almost identical.



Figure 5.3: Predicted and Measured Forward E1 Delays.

Before the introduction of SDH, the AusNet Services communications backbone network was made up of entirely PDH equipment. E2 (8 Mbps) and E3 (34 Mbps) were the most common bearer speeds between stations. There remains a small number of E2/E3 bearers that are yet to be replaced by SDH STM-n. To factor these legacy links into the delay model, two types of delays were considered:

- E1 E2 and
- E1 E2 E3.

The measure and calculate these delays, the following circuit configurations were created:

- E1 E2 E2 E1 and
- E1 E2 E3 E3 E2 E1.

Delays were measured across each configuration and then divided by two. Asymmetry within the equipment did not need to be considered, since the cards are always used in pairs

The figures used to create a delay model for the whole AusNet Communications network are summarised in table 5.4. A visual representation is shown in figure 5.4.

Equipment	Connection	Delay (µs)
	E1-STM	72.4600
ZTE SDH	STM-E1	120.960
	STM-STM	41.7648
	E1-STM	133.962
Ericsson SDH	STM-E1	43.4617
	STM-STM	23.1805
	E1-Radio	258.561
Ceragon Radio	Radio-E1	300.561
	STM-Radio	382.029
וותם	E1-E2	6.00000
РОП	E1-E2-E3	6.50000
Dor km Through Madia	Fibre	4.89572
Per kin mrougn Media	Radio	3.33564

Table 5.4: Figures used to Create Delay Model.



Figure 5.4: Visual Representation of Delays.

It is immediately obvious that the delays through SDH nodes are much longer than the delays through the PDH equipment that they replace. They are in fact between 16.68 and 127.96 milliseconds longer. It was also observed that the delay between E1 and radio ports of a legacy radio system was between 0.179 and 0.194 milliseconds – around 258 to 382 milliseconds less than newer microwave radio systems. These legacy radio delays were not factored into the overall delay model, as there was only one of these type links in the test area, and only three in the whole network. The much longer delays through newer high-bandwidth equipment explains why asymmetrical communications delays are causing problems with current differential relays now where they were not in the past.

To create the AusNet Services communications network E1 delay database, circuit details were first extracted from SDMT. Circuits were systematically scanned to identify and highlight all E1 bearers carrying current differential protection signals. Delays over E1 bearers not used to carry current differential protection signals were not calculated. Distance and node cross-connection numbers were tabled for the main and alternate paths of all current differential carrying E1 bearers and, together with delay figures in table 5.5, used to calculate the main and alternate path delays. The timing difference between main and alternate paths gave the potential asymmetry of the E1 bearers. Figure 5.5 is an excerpt of the tabled data. Bearer names and descriptions have been omitted. The source database contains delay and asymmetry data on 195 current differential carrying E1 bearers. The calculated asymmetry figures would be used later in the project to help identify the at-risk current differential protection circuits.

				Main Path														Alte	rnate	Path								
Main	Alt	Potential		7TF			FRI		PD	н	Cera	igon R	adio	kı	ms		7TF			FRI		рг	эн	Cera	gon R	oihe		
Delav	Delav	Asvm.				L				E1-													E1-					
		- 1	E1 to STM	to E1	STM-	E1 to STM	to E1	STM- STM	E1- E2	E2- E3	El to Rad	Rad to E1	Rad	Rad	Fibre	E1 to STM	to E1	STM-	E1 to STM	to E1	STM-	E1- E2	E2- E3	El to Rad	Rad to E1	Rad	Rad	kms
0.214	0.593	0.379				1	1								7							2		1	1		6	0
0.580	0.226	-0.354									1	1		6					1	1		2						8
0.341	2.958	2.617				1	1								33				1		4							558
3.002	0.341	-2.660				1	1	4							558				1	1								33
0.234	0.997	0.763				1	1							1	11				1	1	3	2		1	1		6	32
1.544	0.265	-1.279				1	1	12			1	1		6	104				1	1		2						15
4.968	0.669	-4.299				1	1	8			3	2	5	275	82				1	1								100
0.253	0.252	-0.001	1	1											12	1	1											12
0.252	0.253	0.001	1	1										1	12	1	1											12
0.219	0.346	0.127	1	1											5	1	1	1										23
0.346	0.219	-0.127	1	1	1										23	1	1											5
0.283	2.310	2.027				1	1								22				1	1	3					4	89	49
2.310	0.283	-2.027				1	1	3					4	89	49				1	1								22
0.250	0.339	0.088				1	1	1							10				1	1	1							28
0.339	0.250	-0.088				1	1	1]	28				1	1	1							10
0.137	4.381	4.243								2					25				1	1	14							792
3.873	0.137	-3.736				1	2			2	4	3	1	177	150								2					25
0.253	0.940	0.687				1	1							1	16				1	1	12							99
1.848	0.253	-1.594				1	1	12							284				1	1								16
0.228	0.336	0.108				1	1								10				1	1	2							23
0.336	0.228	-0.108				1	1	2							23				1	1								10
0.209	0.355	0.146				1	1								7				1	1	2							27
0.355	0.209	-0.146				1	1	2							27				1	1								7
0.338	4.153	3.815								2					66				1	1	13							751
2.066	0.338	-1.728				1	1	2					4	89	4								2					66
0.204	1.013	0.808				1	1								6				1	1	12							114
0.422	0.204	-0.217				1	1	3						1	36				1	1								6
0.245	0.790	0.545	1	1		1									11	1	1	5										79
0.790	0.245	-0.545	1	1	5										79	1	1											11
0.220	0.581	0.361				1	1								9				1	1	6							54
0.906	0.220	-0.686				1	1	10							101				1	1								9
0.438	0.303	-0.135	1	1	2									1	33	1	1	1										14
0.303	0.438	0.135	1	1	1										14	1	1	2										33
0.776	3.904	3.127				1	1								122				1	1	13							700
3.218	0.776	-2.442				1	1			2	4	3	1	177	52				1	1								122
0.230	0.571	0.340				1	1								11				1	1	6							52
0.887	0.230	-0.656				1	1	10							98				1	1								11
0.373	1.121	0.748				1	1								40				1	1	1					2	47	
1.121	0.373	-0.748				1	1	1					2	47					1	1								40
0.228	0.841	0.613	1	1											7	1	1	6										81
0.799	0.228	-0.571	1	1	5										81	1	1											7
2.786	0.403	-2.383				1	1	5	2	2	3	3		140	66				1	1								46
0.773	4.393	3.620				1	1								122				2	2	5	2		4	4	2	178	64
4.564	0.785	-3.779				2	2	6		2	4	4	2	186	89				1	1		2						122
0.356	0.679	0.323	1	1		1								1	33	1	1	5										57
		8			_	8			1		(8					1			8					()	

Figure 5.5: Excerpt of Calculated E1 Delays.

5.1.2 C37.94 Delays

The test setup shown in figure 4.3 was used to measure delays at the C37.94 interfaces. Measurements at the E1 interfaces of the same test circuit were taken immediately after the C37.94 tests. By subtracting the delays at the E1 interfaces from those at the C37.94 and dividing by two, the delays due to each of the DB2/ C37.94 DIU combinations could be found. The results are summarised in table 5.5. Since these delays affect the main and alternate E1 paths equally, they do not influence the potential asymmetry of a protected bearer.

	Delay (µs)
SDH-SDH	262
C37.94 DIU-DB4-SDH-SDH-DB4-C37.94 DIU	1931
Difference / 2	834.8

 Table 5.5: Delays through DB2 and C37.94 DIU Cards.

5.1.3 DB4 Performance

The test setup shown in figure 4.3 was used to test the switching response of Avara DB4 cards, with DB4s in place of DB2s. The Albedo testers were configured to log the measured delays and asymmetry while E1 faults were simulated by removing a single direction of an E1 connection. The Albedo tester are only capable of logging measurements at one-second intervals, meaning they may not capture some momentary responses.

The recorded asymmetry from a DB4 switchover remained for much longer than was expected. It was predicted that asymmetry would exist for up to around 10 ms, due mainly to the time taken for signals to propagate from one DB4 to the other. The asymmetry observed by the Albedo testers typically occurred for around five seconds, ranging randomly between around one and ten seconds. Figure 5.6 represents a typical response, showing little or no asymmetry when switching from main to alternate paths, but several seconds of asymmetry when switching from alternate back to the main.



Figure 5.6: Typical DB4 Switching Asymmetry.

The DB4 switching performance as measured above was deemed unacceptable for use in current differential protection signal carrying circuits. When used on bearers with the potential for large asymmetry, it was predicted that they would almost certainly result in a false current differential trip in the event of an E1 protective switchover.

It was not yet known whether the delay asymmetry captured by the Albedo testers was due to differences in DB4 switching times or some other reason. The test setup described in section 4.3.3 and shown in figure 4.5 was used to ascertain that the asymmetry was in fact due to the two DB4s switching at different times, when reverting from the alternate E1 path back to the main. The findings of these tests were relayed back to Avara Technologies engineers, who carried out their own bench-top testing to verify the results.

With proof that the asymmetry during an E1 revert was due to delays in DB4 switching, Avara Technologies staff were asked to provide a solution. They created a new DB4 firmware build and travelled to the AusNet Services Hazelwood Terminal Station to evaluate it using the test circuits created as part of this project. The Avara staff brought with them breakout cables that connect to header pins on the DB4 circuit board. These cables were used to monitor the switching statuses of the two DB4s directly using voltage recording equipment, which negated the need for the Anritsu OTDR and NetProbe 2000 testers.

Avara's first attempt at a firmware revision appeared initially to rectify the asymmetry problem. A storage oscilloscope provided by Avara was used to monitor the DB4 switching statuses during E1 protective switchovers and reverts. The oscilloscope showed that the two DB4s were switching simultaneously to within around 10 milliseconds. It was noted, however, that the Albedo testers were still detecting asymmetry for several seconds. It was only after the Avara staff had left, that the Hioki recorder was used to find that the DB4s were switching simultaneously, but then one end was switching back to the alternate path for a number of seconds before settling back to the main. This 'bounce' was not captured by Avara's oscilloscope because the time scale used to capture the small time difference in initial reverts was too small to capture subsequent switches a few seconds later.

Figure 5.7 shows the Hioki capture of this 'bouncing' revert. The green and yellow lines represent the switching status of each DB4. A low voltage level indicates that a DB4 has switched to the main E1 path; a high level indicates the alternate path. The yellow signal plot has been shifted up slightly so that the two plots can be distinguished from each other. It can be seen that both DB4s revert together at the trigger point (time = 0), but then around 1

second later one end flips back to the alternate for roughly 4.5 seconds, before settling back to the main again. The time length of this 'bounce' appeared to vary randomly between around 1 and 10 seconds.



Figure 5.7: Hioki Capture of a DB4 'Bouncing' Revert.

These latest set of results were communicated to Avara Technologies staff who verified it with their own testing. They amended their previous DB4 firmware revision and travelled to Hazelwood once again to test it. By this time, two L90 current differential relays had been sourced, and were connected to each other through the communications test setup at Hazelwood. This meant that the effects of the DB4 firmware revision could be simulated properly using relay settings from an in-service 500 kV protection circuit. The results of this testing are described in section 5.2.2.

5.2 Relay Test Results

The next step was to measure the effects that communications channel faults had on current differential protection relays. Two L90 relays were connected via the communications equipment in the previously configured test setup to measure these effects.

5.2.1 Asymmetry Effects

Prior to any practical relay testing, work was carried out to calculate the theoretical relay responses to asymmetrical communications channel delays. These responses were found by

manipulating and adding to Excel worksheets provided by relay manufacturers. GE L90 and MiCOM P546 were the relay types considered, as these were known to have cause line trips due to communications faults in the past. The worksheets were modified to display restraint curves, maximum permissible asymmetry and asymmetry responses for any given current differential setting.

Figures 5.8 and 5.9 show the L90 restraint curves and maximum permissible asymmetries displayed using two groups of relay settings:

- Breakpoint (A): 8.5 and 10
- Slope 1 (%): 20 and 30
- Slope 2 (%): 50 and 70
- Pickup (A): 0.85 and 1.0



Figure 5.8: L90 Restraint using 8.5 A, 20%, 50% and 0.85 A.



Figure 5.9: L90 Restraint using 10 A, 30%, 70% and 1.0 A.

The maximum permissible communications asymmetry is calculated by finding the minimum angle formed by the restraint curve. When using realistic relay settings, this point will always be at the breakpoint load current. The difference, I_{Diff} between two 50 Hz load current waves, I_L separated by delay, d in milliseconds, is given by

$$I_{Diff} = 2I_L \sin(9d). \tag{5.1}$$

As described in section 2.1.2, current differential relays using the ping-pong method are able to compensate for half of the communications channel asymmetry. Thus, the equation relating communications asymmetry, t_{asym} in milliseconds, to the resulting differential current seen by the relay is

$$I_{Diff(relay)} = 2I_L \sin(4.5t_{asym}).$$
(5.2)

Rearranging, this can be used to find the communications asymmetry that would cause a relay to see the current differential, $I_{Diff(relay)}$ at load current I_L .

$$t_{asym} = \frac{\sin^{-1}(l_{Diff(relay)}/2I_L)}{4.5}.$$
 (5.3)

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When load and differential currents at the minimum angle point of the restraint curve are used, this equation gives the maximum permissible communications channel asymmetry for that relay.

The trip/ no-trip responses of L90 and P546 relays are also displayed by the modified relay worksheets. Figures 5.9 and 5.10 show the displayed responses with the same relay settings used to produce the restraint curves in shown in figures 5.10 and 5.11. Figure 5.12 is a mesh plot produced in MATLAB, showing the likelihood of an L90 false trip due to communications asymmetry and line load.



Figure 5.10: L90 Response using 8.5 A, 20%, 50% and 0.85 A.



Figure 5.11: L90 Response using 10 A, 30%, 70% and 1.0 A.



Figure 5.12: Likelihood of L90 Trip due to Asymmetry.

The relay test setup described in section 4.4.1 and shown in figure 4.6 was used to measure the effects of long-term communications asymmetry on both L90 and P546 protection relays. The relay settings were taken from in-service relays on AusNet Services 500 kV and 220 kV lines. A single Doble was used to pass the same three phase current through both relays to simulate a perfect, lossless line. The trip responses of the relays were recorded under varying line loads and communications asymmetry, and the results compared with predicted responses.

Figure 5.13 shows that the displayed restraint currents and observed trip/ no-trip responses of the L90 relays was very close to those predicted. It was observed that the local, remote and differential currents reported by the relays became more unstable as the load current simulated by the Doble was increased. This was likely due to errors in

- Doble current waveforms
- Relay load current measurement
- Relay differential current processing
- Variances in communications delays.

Together, all of these errors account for the slight differences between predicted and observed relay responses at higher simulated line loads.

Figure 5.14 shows the accuracy of the relay response model on P546 relays. Again, the model loses accuracy under heavy simulated line load conditions.

It may be possible to build into the model a margin of error on the load current, to compensate for the apparent error under high simulated loads. However, as the source of the error was not yet known, it was decided not to implement this error margin. It would be pointless modifying the model to account for errors in the test environment, only to find that the errors do not apply to real-world conditions. It may be possible to find the source of the errors as part of future work.



Figure 5.13: Predicted and Observed L90 Relay Responses.



Figure 5.14: Predicted and Observed P546 Relay Responses.

With relay responses verified, an asymmetry threshold of 2.4 milliseconds was chosen based on the calculated likelihood of false trip due to asymmetry. Any E1 bearer carrying current differential traffic with predicted potential asymmetry greater than the threshold was flagged as potentially at-risk. Momentary fading of microwave radio links mean that they are more likely than fibre, to disrupt E1 circuits in one direction only. Hence, bearers with at least one radio link in their main path are at higher risk of asymmetry than those with only fibre, and were flagged as such. These checks identified that out of 333 current differential circuits, 14 were potentially at high risk of misoperation and a further 37 were at medium risk.

Restraint settings of the relays used in the potentially at-risk current differential circuits were recorded and, using the modified relay response worksheets, used to calculate the maximum permissible asymmetry for each circuit. Any circuits with potential asymmetry 1 or more milliseconds less than the permissible, were deemed not at risk. This further check identified that 10 of the 37 potentially medium risk circuits were not at risk of misoperation. Table 5.6 lists the identified at-risk current differential circuits, ranked from most to least at-risk. Bearer names have been hidden and their descriptions omitted.

Namo	Relay	Potential	Permissible	Potential -					
Nume	Туре	Asymmetry	Asymmetry	Permissible					
1**001	P546	4.299	2.564	1.735					
1**205	P546	3.221	2.564	0.657					
1**206	P546	3.221	2.564	0.657					
1**207	P546	3.221	2.564	0.657					
1**208	P546	3.221	2.564	0.657					
1**403	P546	3.056	2.564	0.492					
1**303	L90	3.221	2.826	0.395					
1**304	L90	3.221	2.826	0.395					
1**702	L90	4.202	3.936	0.266					
1**001	P544	2.785	2.564	0.221					
1**002	P544	2.785	2.564	0.221					
1**A03	P546	3.056	2.890	0.166					
1**A04	P546	3.056	2.890	0.166					
1**201	P546	2.442	2.546	-0.104					
1**101	P543	4.243	2.564	1.679					
1**001	P543	3.878	2.564	1.314					
1**002	P543	3.878	2.564	1.314					
1**201	P546	3.861	2.564	1.297					
1**501	P546	3.815	2.564	1.251					
1**301	P543	3.362	2.564	0.798					
1**201	P546	3.318	2.564	0.754					
1**202	P546	3.318	2.564	0.754					
1**401	P546	3.127	2.564	0.563					
1**208	P546	3.127	2.564	0.563					
1**101	P543	3.121	2.564	0.557					
1**102	P546	2.995	2.564	0.431					
1**303	L90	4.731	4.304	0.427					
1**304	L90	4.731	4.304	0.427					
1**501	P546	2.576	2.240	0.336					
1**001	P546	2.617	2.564	0.053					
1**502	L90	2.576	2.604	-0.028					
1**504	L90	2.576	2.604	-0.028					
1**002	L90	2.660	2.722	-0.062					
1**004	L90	2.660	2.722	-0.062					
1**005	L90	2.660	2.722	-0.062					
1**003	P546	2.617	2.722	-0.105					
1**006	L90	2.617	2.722	-0.105					
1**001	LFCB	3.008	3.217	-0.209					
1**002	LFCB	3.008	3.217	-0.209					
1**B02	P546	2.849	3.217	-0.368					
1**402	P546	2.702	3.217	-0.515					

Table 5.6: At-Risk Current Differential Circuits.



High Risk (radio in main path)

Medium Risk (no radio in main path)

5.2.2 DB4 Switching Effects

As detailed in section 5.1.3, it was found that the DB4s as configured in AusNet Services' communications network would not switch from alternate to main E1 paths simultaneously in a protective revert, which resulted in several seconds of delay asymmetry. While it had been suspected that this had been the cause of extra high voltage line trips, it had not yet been proven.

The test setup described in section 4.4.2 and shown in figures 4.7 and 4.8 was used to observe the response of L90 current differential relays during DB4 protective E1 switchovers. The Hioki memory recorder was configured to capture the two DB4 E1 switching statuses, as well as any CB trip commands from the L90 relays. Figure 5.15 is a typical Hioki capture from such tests, when using DB4s with the production firmware currently used in the AusNet Services network. The green and yellow lines show DB4 switching statuses as before, the blue and orange lines show the L90 CB trip outputs. A high level represents a trip command. Again, the yellow signal has been shifted up slightly to distinguish it from the green. A Doble was used to provide a 5 A secondary load, which simulated a 900 A primary line load. The capture shows that the L90 relays would definitely trip under normal conditions with this version of DB4 firmware. They would output a CB trip command roughly 2.5 seconds after the first DB4 had switched. This timing was not precise; it varied randomly between around 2.4 and 2.8 seconds.



Figure 5.15: Hioki Capture showing L90 CB Trip Commands.
The L90 relays were configured to store log files of analogue signals and digital statuses for several seconds before and after each CB trip command. Of interest were the differential and restraint currents signals and any statuses relating to the 87L signal. Figure 5.16 shows a typical response.



Figure 5.16: L90 Differential Current and Statuses.

The L90 record shows that the 87L function is blocked at various stages throughout each test. This is due to the 87L channel being briefly interrupted as the E1 bearers change paths and resynchronise. It can be seen that at around 8 seconds before the trip command, when the DB4s switched to the alternate E1 path, the differential current rises quickly and may have resulted in a trip if the restraint did not also rise. The capture shows that the restraint increases each time the L90 detects excessive 87L channel asymmetry. This adds a level of immunity to momentary bursts of channel asymmetry, but it cannot prevent misoperation during prolonged asymmetry, without GPS compensation. With GPS, the L90 is quoted as being able to compensate for up to 10 milliseconds of asymmetry, which is well above anything measured or predicted in the AusNet Services network.

Having established that DB4s with the latest production version of firmware could cause current differential misoperation, it was now time to test the L90 response to E1 switchovers with Avara's improved (evaluation) DB4 firmware. Albedo communications testers and Hioki memory recorders were again used to measure delays and E1 switching times at the same time as the L90 response. The measured delays and switching times are shown in figures 5.17 and 5.18.



Figure 5.17: Improved DB4 Firmware Delays.



Figure 5.18: Improved DB4 Firmware E1 Switching.

The delay measurements show that brief moments of asymmetry of between 1 and 2 seconds still exist at the time of an E1 switchover and revert. This is a vast improvement on the asymmetry for up to 10 seconds that was being seen using the production DB4 firmware. These brief bursts of asymmetry would be very hard or even impossible to avoid, given the resynchronisation time required for such large differences in path delays.

The E1 switching capture shows that both DB4s now switch to the alternate, and revert to the main path almost simultaneously. Precise measurements revealed that both ends would always switch within around 4 and 150 milliseconds of each other. The test was repeated using a range of simulated line loads and communication fault types, and the L90s did not once output a CB trip command.

Figure 5.19 shows an L90 response during a DB4 E1 switchover using the improved firmware, figure 5.20 shows the revert. As part of the firmware upgrade, the minimum programmable Wait To Restore (WTR) time of the DB4 was changed from 0 to 60 seconds. This meant that the E1 switchover and revert could not be recorded on the same L90 capture, where they could be before.



Figure 5.19: L90 Response to Improved DB4 E1 Switchover.



Figure 5.20: L90 Response to Improved E1 Revert.

The captures show that with the improved DB4 firmware, the differential current measured by the L90s rises very little during an E1 switchover and revert. They still detect an 87L delay time change and increase their restraint current accordingly, but now the asymmetry does not exist for long enough for the L90s to see the ramping differential current that they did before.

5.3 Final Product

The final model brings together the communications delay and current differential relay response calculators, to predict the potential asymmetry of E1 bearers and display their effects on P54x or L90 relays. The user enters the distances and cross connections traversed by the main and alternate paths of an E1 bearer, the differential settings used in the relays connected to the bearer, and the charging reactive power and voltage of the line. The model outputs the differential current restraint curve of the relay and displays the maximum

permissible and actual asymmetries. It also plots the relay trip response to asymmetry and highlights the portion relevant to the calculated asymmetry. It takes into account the charging of the line, calculated by dividing the line charging reactive power by the line voltage. Figure 5.21 shows the output of the model with settings and configurations taken from an AusNet Services 220 kV line protection circuit using P546 relays. It can be seen that the P546 relays in this circuit will trip if asymmetry exists with a line load current between around 540 and 2,250 A. Figure 5.22 shows the output from a 66 kV line protection circuit using L90 relays. These relays will trip due to asymmetry only when the line current is between around 720 and 900 A. Enlarged versions of figures 5.21 and 5.22 are in Appendix D.



Figure 5.21: Delay Model Output of AusNet Services P546 Protection Circuit.



Figure 5.22: Delay Model Output of AusNet Services L90 Protection Circuit.

Note that the model does not consider the direction of cross-connections through nodes. I.e. the delays from E1 to STM-n interfaces are considered the same as from STM-n to E1. The same applies through radio nodes. This was done to make the model simpler to use without any real reduction in accuracy. It will result in a negligible error in the rare case that a circuit begins and ends with two different types of nodes. This error is likely to be well within the model's margin of error.

5.4 Assumptions

The model does make the following assumptions regarding the AusNet Services electricity and communications networks:

- That the Siemens and the newer type Ericsson SDH nodes used in transmission sites create the same delays as the Ericsson nodes used to measure E1 delays.
- That all microwave radio nodes create the same delays as those measured/ calculated.
- That the calculated fibre and radio link lengths reported by SDMT are accurate.
- That there is no actual current differential on the lines protected by current differential protection.

The first assumption is the most likely potential source of error. There are several AusNet transmission sites that still use the older Siemens SDH equipment, or have been upgraded to Ericsson SDH equipment different to those used to measure E1 delays. While it is likely that the delays through these nodes are similar to those through the measured nodes, it is unlikely that they are the same. The Siemens nodes are gradually being replaced by Ericsson, so no time will be spent on these nodes. The newer Ericsson equipment is planned to replace around half of the existing Ericsson nodes. Delays will be measured through the newer nodes when they are rolled out in the local region. If the delays are notably different, the model will be updated to include the newer nodes as cross-connection types.

Table 2.3 in section 2.2.2 shows that the E1 delays through Ceragon radios vary substantially with modulation type. Testing also revealed that the delays through older model Ceragon radios are much lower than through new radios. These older radios are ignored, as there are very few left and they will eventually be replaced by the newer types. Further testing may prove that a single figure for radio delays results in unacceptable errors when different modulation types are used, in which case the model will be amended to include radio modulation types.

SDMT is the application used to record physical and logical details of the AusNet Services communications network. It uses a georeferenced overlay map to calculate fibre and radio link lengths. It includes fibre service loop locations and adds a set length for each loop. OTDR measurements in the local area showed that the lengths reported by SDMT were reasonably accurate. However, the location data in SDMT was entered manually from a central site, and is as such subject to human error.

The relay response model considers line charging current, but does not factor in any other potential sources of 'normal' differential current. One such source is current transformer non-linearity at high loads when they approach saturation. When designed properly, the differential current caused by CT saturation should be negligible, and it was therefore considered acceptable not to account for it.

CHAPTER 6 – Conclusions and Further Works

6.1 Conclusions

Current differential communications channel asymmetry presents a very real risk of relay misoperation in modern power system protection systems. Increased used of current differential protection and the replacement of communications nodes with higher capacity equipment with higher latency, has meant that channel asymmetry problems are more prevalent now than they were in the past. Hence, the need to consider communications delay asymmetry is more critical now than it has ever been.

The most likely cause of asymmetry is split-path-communications brought about by faults in one direction only. These single direction faults are more likely to occur in microwave radio than through fibre optic links. Thus, protected E1 bearers with radio links in their main path are especially vulnerable to delay asymmetry.

Delay testing revealed that there were no abnormally long delays through the AusNet Services communications network. This indicates that the delays are inherent to the communications equipment, and not due to any type of fault that could be rectified.

The research, delay measurements and relay testing all culminated to produce a model that will predict E1 delays with around 94% accuracy, and predict L90 and P54x relay trip response to asymmetry with around 95% accuracy. These accuracy figures will likely come down with further testing, but they are promising results nonetheless.

With the advertised capabilities, Avara Technologies DB4 switching E1 card should have been able to use bidirectional switching to alleviate the problem of delay asymmetry. Testing revealed, however, that two connected DB4s did not switch E1 paths simultaneously; resulting in asymmetry for long enough that connected current differential relays would potentially misoperate. Avara Technologies staff admitted that the mistimed switching was due to a bug in the DB4 firmware. The firmware code was updated, and tests with L90 relays proved that updated DB4s would not cause relay misoperation due to asymmetry. A production version of the firmware was yet to be released at the time of writing.

6.2 Further Works

Delay testing was carried out through only around one eighth of AusNet Services' E1 bearers. Per-node delays were calculated using estimated distances reported by SDMT. Further testing over a broader range of SDH equipment and microwave radio modulation types, with calculations using OTDR measured distances would result in a more refined delay model with a higher degree of accuracy. The layout of the delay data spreadsheets is such that they can be easily built upon as further delay measurements are recorded.

Only GE L90 and MiCOM P546 protection relays were modelled in this project. SEL 311L relays were tested but not studied in detail, as it was found that they would never trip due to asymmetry in the configuration used by AusNet Services. The SEL alpha plain method of differential current detection uses relatively simple vector calculations. Future work could include modifying the combined model to include SEL, and possibly other types of protection relays.

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APPENDIX A – Project Specifications

FOR:	JUSTIN DORTMANS
TOPIC:	OVERCOMING ASYMETRICAL COMMUNICATION DELAYS IN LINE CURRENT DIFFERENTIAL PROTECTION CIRCUITS
SUPERVISOR:	Dr Narottam Das
ENROLEMENT:	ENG4111 – S1 2016 ENG4112 – S2 2016
PROJECT AIM:	To analyse and propose ways to overcome asymmetrical communications delays on line current differential protection circuits
SPONSORSHIP:	AusNet Services Ltd. & School of Mechanical and Electrical Eng.

PROGRAMME:

- 1. Research on fibre / microwave communications area to determine causes and typical values of latency in communication systems.
- 2. Research and investigate line current differential protection relays to determine how they work and what design principles are implemented to add immunity to communication system faults.
- 3. Use communication network test equipment to measure the latency through a variety of fibre and microwave links.
- 4. Set up a pair of line current differential relays in a test environment to make a correlation between communications channel asymmetry and false current differential detected by the relays.
- 5. Analyse the measured communication delays to try to make a correlation between physical link length/ network elements traversed and latency for both fibre and microwave link circuits, and identify potential causes of any abnormally long delays.
- 6. Compare the reported (i.e., existing researched) and measured data to determine ways to overcome the line current differential faults caused by asymmetrical communication system delays.
- 7. Compile all findings into the dissertation.
- 8. Prepare an accurate and precise documented report for my dissertation and submit to the HES, USQ.

As time / resources permit:

- 9. Implement the proposed techniques on a real-life line current differential protection circuit to determine if they do rectify the asymmetrical communications fault.
- 10. Expect to report the results to conference or in journal papers.

APPENDIX B - Risk Assessments

Two risk assessments are shown in Tables B.2 and B.3. Table B.2 was carried out from a personal perspective, B.3 considers the hazards which may pose risks to the network or the successful completion of the project. Table B.1 shows the risk matrix used to determine the personal risk level of each activity. The task numbers refer to those listed in table 4.1.

		Consequence				
		A Minor First aid or medical attention	B Moderate Increased medical attention	C Major Severe health outcome or injury	D Extreme Intensive care or death	
<u>ئ</u> ے	1 Rare	A1	B1	C1	D1	
nood of	2 Unlikely	A2	B2	C2	D2	
Likelił Occur	3 Likely	A3	В3	C3	D3	
	4 Almost Certain	A4	B 4	C4	D4	
ŗ						
	Legend	Low Risk	Medium Risk	High Risk		

	Table B	3.1 :	Personal	Risk	Matrix.
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Task	Hazard	Risk	Minimisation
3A/	Slips/trips/strains	A2	1. Use correct, approved manual handling techniques
B/C			2. Maintain neat workspace
3A/	Laser exposure	C1	1. Avoid looking directly into fibre connectors
B/C			2. Implement Auto Laser Shutdown (ALS) on equipment
3A/	Electric shock	D1	1. Maintain clearance around live terminals
B/C			2. Wear appropriate Personal Protective Equipment (PPE)
3A/	Traffic collision	D1	1. Drive defensively
3B	(long distances)		2. Take breaks when fatigued

Task	Hazard	Risk	Minimisation
1A/	Lack of previous research	Medium	1. Evaluate current literature to determine
1B			level of cover and identify "gaps" in
			research
2A	Insufficient time to study	Low	1. Obtain manager approval to study
	network due to work		network during working hours
	commitments		2. Attend work after hours to study
			network
			3. Study network after hours from home
		2.6.11	using remote desktop
2A	Reluctance of designers to	Medium	1. Ensure designers that discretion will be
	disclose network shortfalls		used as to what details are divulged to
		т	
2B	Insufficient access granted	Low	1. Obtain preliminary approval to access
24/		N 1'	and modify communications network
3A/	lest equipment/personnel	Medium	1. Begin planning and communicate test
3B/	not available when required		2 Diag angles tradition and the string around
			2. Plan project related testing around
21/	Test equipment	Madium	1. Study test equipment specifications
3A/ 2D/	Test equipment	Medium	1. Study test equipment specifications
30/	issues		2. Carry out company the checks prior to
2 \ /	Connot replicate delay	Madium	1. Conduct tests across a wide range of
3A/ 3D		Medium	1. Conduct tests across a while range of network nodes under verying conditions
$\frac{3D}{3\Lambda/}$	Inadvertent disruption to	Low	1. Do not make changes to
3R/	communication/protection	LOW	communications network without a
3D/	circuits		thorough understanding of potential
50	eneurs		impacts
			2 Ensure that personnel that are assisting
			are suitably trained and instructed
			3. Isolate protection circuits if there is any
			chance of disruption to protection traffic
4B/	Cannot create delay model	High	1. Take as many measurements as
4C	due to randomness of	0	practicable
	measured data		2. Ignore data that is obviously influences
			by external disturbances
4B/	Cannot determine causes of	High	1. Study relevant equipment manuals
4C	abnormal delays	Ŭ	2. Seek guidance from specialist engineers
			3. Record as many conditions during
			testing as possible
5A/	Reluctance of the company	High	1. Obtain guidance as to what detail can
5B	to have network details		and cannot be published
	made public		2. Generalise published network details if
			necessary
			3. If necessary, obtain written declaration
			from the university that the dissertation
			will not be published

 Table B.3: Project/Network Risk Assessment.

APPENDIX C – Project Timeline



APPENDIX D – Delay Model Outputs



Figure D.1: Delay Model Output of AusNet Services P546 Protection Circuit.



Figure D.2: Delay Model Output of AusNet Services L90 Protection Circuit.