University of Southern Queensland

Faculty of Health, Engineering and Science

Develop Process Bus Architecture for integrating sampled value IEDs

A dissertation submitted by

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Abstract

The recent interest within the power industry for the use of the IEC61850 standard has meant that the technology needed to implement this standard is at the forefront of most manufactures development projects. The most recent development are for devices used to implement the process bus component of the standard, described in part 9 of the standard. The implementation of this new technology into a Distribution Network Service Provider's substation has additional challenges compared to that of a Transmission Network service Provider.

The implementation of a process bus architecture is a significant change from the existing practice. The critical nature of the system in which this change is occurring means that the impact of the technology will be heavily scrutinised by end users. Two key technical issues were identified that would arise from the introduction of process bus technology into a substation.

The impact on the reliability of the system caused by replacing a simple connection practice between the instrument transformer and the protection relay with a communication network is one of the issues. Appropriately designing the process bus architecture by utilising redundancy has provided a means so that the reliability of the process bus system exceeds that of the existing conventional system. The analyses of two-process bus architectures has been constructed as part of this project to demonstrate the reliability improvement.

The performance of the new devices introduced into the network needs to be understood so that any effect on the overall system is known. It has been identified that the merging unit that was tested as part of this project has shown a reduction in the performance of the analogue to digital conversion of measured data based on transient response criteria.

To describe the performance of a merging unit such that the end user can predict the output of the device for different inputs, a mathematical model was developed. This model is a second order transfer function approximation obtained from the transient response test results for a merging unit subjected to a DC step input. Minor gain errors were observed when testing the model with typical system signals such as the unsaturated sine waveform and a saturated CT waveform.

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Chapter 1

Introduction

1.1 Existing Ergon Energy Architecture

Ergon Energy as a Distribution Network Service Provider (DNSP) is responsible for constructing and maintaining electrical assets to supply electricity to both low and medium voltage customers in Queensland. Zone Substations are a combination of various pieces of primary plant such as circuit breakers, transformers and secondary system equipment such as protection relays, local control facilities to transform the voltage levels to distribute power. These substation are key infrastructure to provide connection from a Transmission Network Service Provider (TNSP) i.e. Powerlink Queensland, to distribute electricity efficiently to a geographically disperse customer base.

Australian Energy Regulator (AER) and the Australian Energy Market Commission (AEMC) set the requirements of the DNSP. The criterion focuses on the reliability and safe operation of the electrical network. Therefore, to operate the network to comply with the criteria, Ergon Energy has continually improved their technology and infrastructure.

The secondary system equipment is responsible for the general control of the primary plant, for example regulating the system voltages. The secondary system is also tasked with maintaining the safe operation of the network by isolating a faulty part of the electrical network. The connection between the two systems has not changed significantly since the conception, with the use of copper wiring connecting directly between two points.

The architecture shown in Figure 1 is constructed using predominately-analogue systems to connect from the primary plant to the secondary system equipment. Copper cables are used to connect point to point with analogue to digital converters within the IEDs or control signals converted to DC outputs to control mechanical contacts to operate the primary plant. An example of this would be the AC signal from the current transformer to the protection Intelligent Electronic Devices (IEDs). The DC signals are typically indications or instructions such as open or close of the circuit breaker.

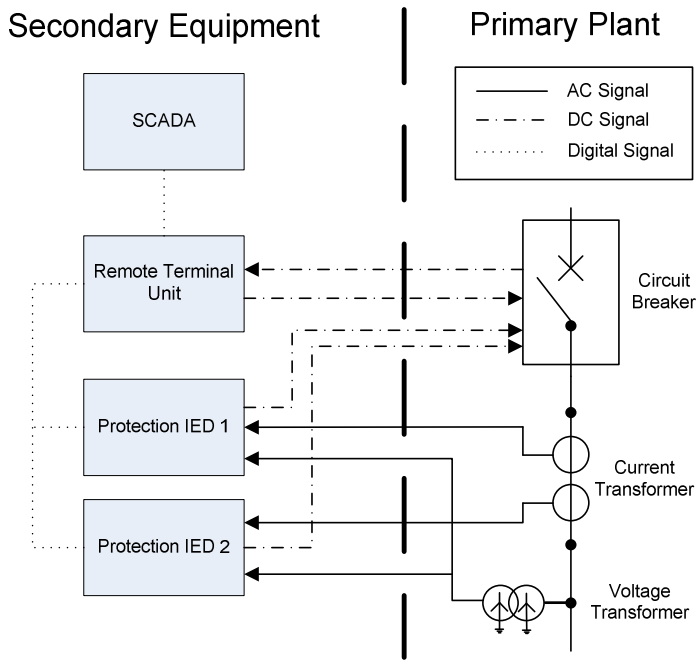

Figure 1 – Conventional connection between primary plant and secondary equipment

The digital signal part of the architecture consists of the transmission of information gathered via the IEDs through a remote terminal unit (RTU) to be made available on SCADA. The technology that is within the zone substation has allowed more information to be available to remote control centres to monitor the network's condition. An example of this would be power flow during planned or unplanned outages on the network. Having the visibility of power flow and ratings of the primary plant allows the remote operator to open or close switches within the network so that the system operates safely within its limit.

In summary, the architecture that is presently deployed into Ergon Energy's network is a mixture of protocols and limited in its distribution of measured values from a particular instrument transformer, as will be discussed later on.

1.2 Development of new Technology

The International Electrotechnical Commission (IEC) recognised that within the power industry there were wide varieties of proprietary communication protocols within a typical substation architecture. This brought about the development of the *IEC 61850 Power Utility Automation* suite of standards. This standard can be split into two main categories with reference to the development of new technology, Station Bus and Process Bus.

1.2.1 Station Bus

The Station Bus conveys control and condition messages between the secondary system equipment. Information such as open/close indication from circuit breakers and information from Protection IEDs to remote locations through SCADA are typical communication signals assigned to Station Bus. The majority of the signalling that is transported over this level already exists in a non-proprietary communication medium, which therefore can be deemed common practice. The Digital and some DC signals shown in Figure 1, which illustrates the conventional system connections, will be replaced by Station Bus architecture.

The advancement and use of this technology is already being implemented within the power industry. The deployment of this technology is due to the overlying architecture being very similar to that of the existing practices. The introduction of primary plant, which publishes condition-based information in a digital format, meant that having a system that can transmit this information would have known quantifiable benefits.

A single communication protocol with the main advantage of interoperability such as IEC 61850 is the reason for equipment with these abilities being developed. It can be noted that the equipment that is being developed is predominately the same with the addition of a module to allow an IEC 61850 communications capabilities.

Interoperability at the station bus is the main driver for the introduction of IEC 61850. The ability at this level to be interoperable has not been as complex due to the information that is being transmitted. Different manufactures using this information are not using proprietary algorithms that are dependent on the quality of the information.

1.2.2 Process Bus

Process Bus is used to transport the measured values taken by an instrument transformer and other primary plant condition status over a communication medium to an IED. The conventional medium for the transportation of this information is via a copper wire connected directly between the two devices.

The measurement process within a substation's protection system is typically made up of three (3) components:

1. Transformation
2. Analogue to digital conversion
3. Protection Algorithm

The first component is completed by a conventional instrument transformer to a level that can be used by sensitive equipment. This information is then transported to a device that converts the signal to a format that can then be used in the following component. With the introduction of numerical relays, the signal would need to be in a digital format. The numerical relays then implement a protection algorithm specific to the information that is available to identify when there is a system abnormality.

The conventional system has had both the second and third component built into the same IED. The new technology is now moving the second component physically closer to the first. The measured values are now being sampled by an IED separate to the protection relay. The new IED then broadcasts the measured values now referred to as "Sampled Values" onto a communication bus (Process Bus) for protection IEDs to use.

Although the end-to-end measurement process has not changed, the connection between each component will with the introduction of IEC61850-9-2. The protection system is critical to ensure the safe operation of an electrical network and any change to this system is heavily scrutinised.

Interoperability of the Process Bus is quite complex due to the requirement of the sampled value. Presently the protection relay is only responsible to sample the analogue signal to ensure the correct operation of its own protection algorithm. The system's interoperability means that different manufactures protection IEDs will need to be able to use sampled values from other manufacturer's IEDs to function correctly.

1.3 Project Rationale

The electricity industry like most other industries over time has evolved with the development of new technology. Ergon Energy is obligated as Distribution Network Service Provider (DNSP) to ensure that the infrastructure installed within their network is safe, reliable and the most cost effective and efficient. The Substation Standards group within Ergon Energy is tasked with continually reviewing the standards that our design teams use to both repair/replace and augment Ergon Energy's network. With the development of IEC 61850 and the possible impact the standard can have on the way in which Ergon Energy works, it is prudent for further investigation of IEC 61850 use in Ergon Energy's network is undertaken.

Ergon Energy's network has evolved over time; this included the development of the company's protection standards to comply with Australian standards and regulatory requirements. Ergon Energy's network consists of a number of substations that have limited protection schemes and aging protection relays. Given the expected life of a protection relay is less than half that of the primary system means that during the substation's life cycle the protection systems will be replaced and need to utilise existing measurement equipment.

The technology presently used to replace the protection relays has particular requirements of the instrument transformers. These requirements limit the ability of the instrument transformer to share the measurement to allow additional protection schemes to be implemented without the need to make changes to the instrument transformer. Development of technology such as process bus, which allows measured values to be shared amongst multiple intelligent devices, provides an engineering solution to remove the limited protection scheme issue within Ergon Energy's network.

1.4 Project Aim

The aim of this project is to objectively assess the impact of introducing process bus into Ergon Energy's substations. This assessment will include two main components of a process bus system: Network Architecture and Sampled Values.

The network architecture for process bus has a direct impact on the operation of the protection system within the Ergon Energy substation. The adoption of such a network would be a significant change from what is presently installed: hardwired connection between the instrument transformer and the protection IED. The process bus architecture is a communication network and therefore has the flexibility in the topology due to the introduction of new redundancy communication protocols. The aim of this section of the project is to assess the possible topologies to understand:

- a comparison to the conventional architecture
- how improvements can be made

The sampled values assessment is based on the introduction of the IED termed "Merging Unit". The functionality of the merging unit for use in this project is to perform the sampling of an analogue measurement and then convert it to a digital format and publish it on a communication network. The physical location of these devices has an impact on the performance of an instrument transformer, given reason to the assessment of their impact on Ergon Energy's network.

1.5 Project methodology

Process bus is still in development with very few known systems that have been implemented. The two main parts to process bus are Sampled Values and the Communication Network. The project will look into both parts analytically and practically where possible due to limited accessibility to IEC61850 process bus compliant equipment.

1.5.1 Process Bus Architecture

The methodology adopted for determining the architecture of the process bus network for a recently commissioned Ergon Energy substation in a staged process. The initial stage of the assessment will isolate a section of the ultimate arrangement so that a strategy can be developed to apply to a larger scale. The criteria to which this will be assessed, is based on the comparison of the reliability and availability of the existing versus the new architecture.

The assessment will use the proven methodology of IEEE 493 standard by deriving reliability and availability block diagrams and then simplifying down to single block. Although this methodology is proven, the extension of this to the next stage of applying to the ultimate arrangement with the integration of multiple smaller networks to construct the total network will require the development of a new process to assess the network.

The ultimate arrangement will then require a number of topologies to be assessed to fully understand the advantages and disadvantages of each topology. The topologies will be based on the learnings from the isolated case.

The final architecture is then to be deconstructed so that using the logic used to develop it that smaller blocks can be created. These smaller blocks can then be used to implement the process bus architecture for different substation configurations.

It should be noted that this methodology would only be completed analytically, as the hardware that is IEC61850 compliant presently does not support any redundancy protocol.

1.5.2 Sampled Values

The methodology adopted for accessing the impact of sampled values into Ergon Energy's network will utilise both numerical modelling and practical testing of existing and new hardware. The use of medium voltage equipment to simulate primary system conditions is not possible due to safety concerns therefore a numerical model of the primary system will be used in the test equipment.

To understand the change in the systems performance it required an assessment of conventional protection relays and the new process bus devices. The tests were carried out using following equipment:

Test Equipment

- Doble F6150 Power System Simulator – This device has been used to provide the analogue test signal
- Omicron CMC850 – This device has been used to provide the sampled value test signal
- SAT Sync test kit – This was used to provide a GPS signal to the Doble F6150 for time synchronisation
- ALSTOM MICOM P594 – This device produces IRIG-B and 1 Pulse Per Second signalling to be used in the tested devices for time synchronisation.
- Personal computer – This is used to control the test, communicate with relays and capture test data

Test Software

- MATLAB® R2013b – This software was used to produce the saturated second test signal
- Microsoft Excel 2013 – This software converted the MATLAB® saturated waveform model output into COMTRADE format for use in the test device.
- Protection Suite v2 – This software controls the Doble F6150
- Test Universe – This software controls the Omicron CMC850
- Manufacture “X” configuration software
- Manufacture “Y” configuration software
- Manufacture “Z” configuration software
- Wireshark v1.8.15 – This software captured the sampled value messages on the network

Tested Devices

- Manufacture “X” relay- This is a conventional multifunction relay
- Manufacture “Y” relay - This is a conventional multifunction relay
- Manufacture “Z” merging unit – This is an analogue merging unit compliant with IEC61850-9-2LE
- Manufacture “Z” relay – This is IEC61850-9-2LE compliant Current Differential with Distance Backup relay

- Manufacture “W” Ethernet Switch – This device allowed the establishment of a process bus.

To derive the impact of each device and it’s response to different inputs, four different test plans were required. The following are the test name and the general purpose:

- **Conventional Relay Base Test** – Determine the system response of a conventional relay.
- **Process Bus Devices including Ethernet Switch Test** - Determine the system response of the Merging unit and Process Bus relay. Record the response with the sample values having to pass through an Ethernet Switch.
- **Process Bus Devices excluding Ethernet Switch Test** - Record the response with the sample values not having to pass through an Ethernet Switch to then compare with other test results to determine the delay created by an Ethernet switch.
- **Process Bus Relay Test** – Use generated sample values to assess the system response of the Process Bus relay.

Each test was subject to three different types of types signals:

- Unsaturated single phase current input
- Saturated single phase current input
- DC Step single phase current input

Figure 2 below is a signal flow diagram that has summarised all four tests into one diagram.

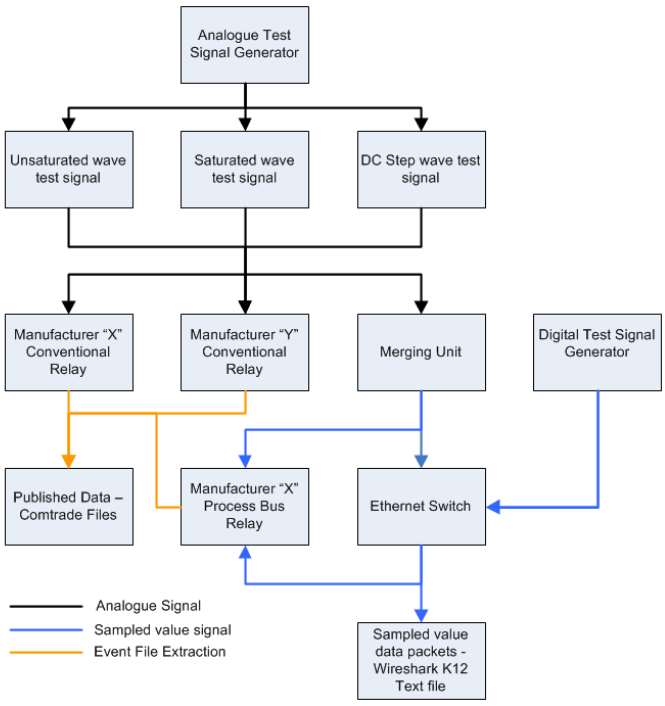

Figure 2 – Connection and signal flow diagram for the test methodology

Chapter 2

Literature Review

2.1 Relevant Standards

2.1.1 IEC61850

2.1.1.1 Part 7

The IEC61850 standard consists of a number of parts to address different applications of this communication standard. The standard was developed to address a number of communication requirements between IEDs to improve the automation and interoperability of devices within a substation. Figure 3 below has been taken from IEC 61850-7-1 section 5 that describes the overview of the 61850 series concepts.

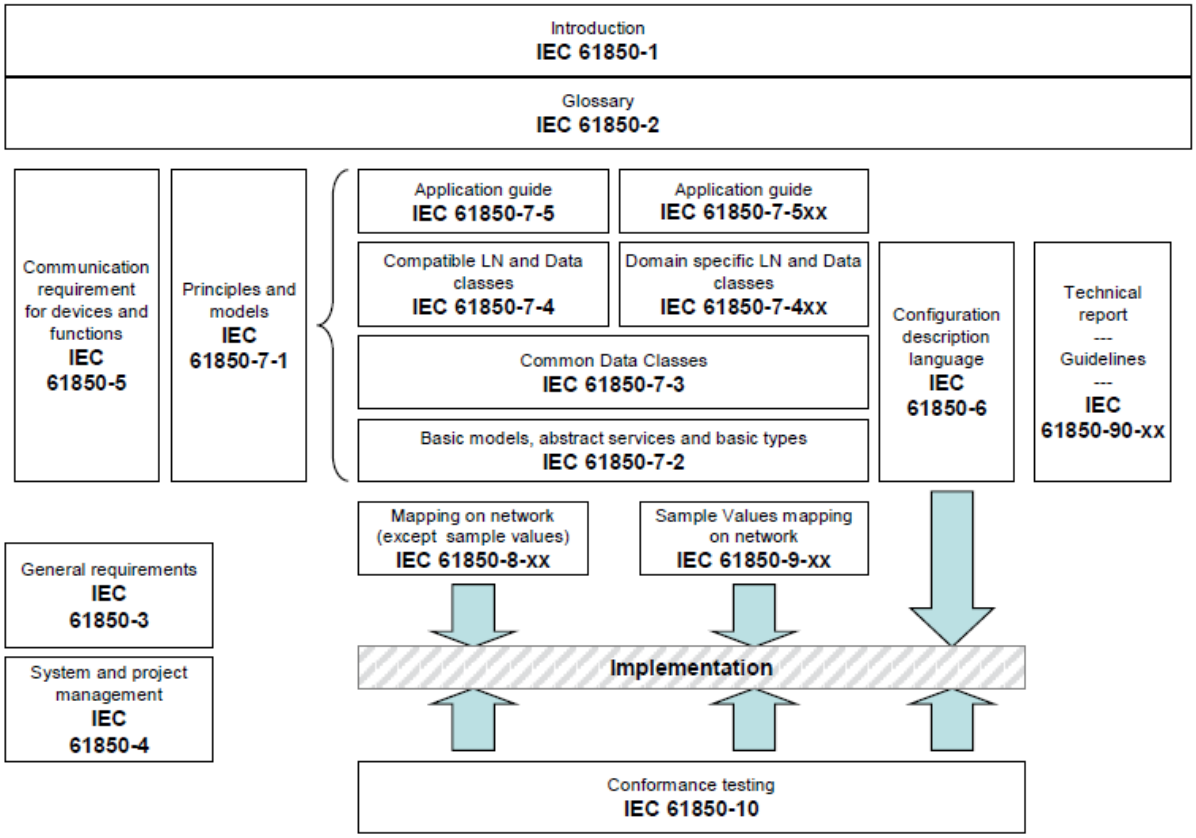

Figure 3 – Relations between modelling and mapping parts of the IEC 61850 series (International Electrotechnical Commission, 2013)

Part 7 is primarily focused on constructing data models for transportation of information over the station bus whilst maintaining the conventional connection between the instrument transformers and protection relays. The critical information that is discussed within part 7 of the series is the introduction of logical nodes and the naming convention associated with the functionality of the node. Throughout Part 7, there is regular reference to a communication path for condition and control signalling for primary plant using Generic Oriented Object System Event (GOOSE) data structure to assist with determining priority.

With reference to a number of manufacturers, these GOOSE messages are used by IEDs referred to as bay controllers to perform logical actions. The location of these bay controllers has led to the development of IEDs that accept both station and process bus information. For the purpose of this dissertation, it will be assumed that these forms of communication will occur over physically separate communication mediums.

2.1.1.2 Part 9

The transportation of measured values from the instrument transformer to an intelligent electronic device is the reason for the development of Part 9 of the IEC61850 standard. The concept of Specific Communication Service Mapping (SCSM) set outs the data structure for transporting sample values was defined within this part. This standard is targeted to set key requirements of components within the process bus of the substation automation.

Implementation of this standard has brought about discussions within the industry to refine the standard. Through industry workshops, an IEC61850-9-2LE version or also known as *Implementation Guideline for Digital Interface to Instrument Transformers Using IEC 61850-9-2* was published. In this publication, the areas that were targeted towards the implementation of this standard have been addressed.

The limitation to part 9 and IEC61850 in general is the information required to develop a product that is compliant and practicable. In particular is the IED referred to as the Merging Unit (MU). Within the IEC61850-9-2LE document, there is an analysis of an example of implementing the use of a logical device. It illustrates by using a sliding rule to show how the resolution of the Analogue to Digital affects the replication of measured value.

Although the standard has worked to develop the data structure and key requirements such as sample rates that ultimately effect the process down the chain, it still lacks more detail as to the application. The sampling frequency is only one criterion that can define the quality of the information that is to be received by an IED to use. Other criteria such as resolution, peak range and any filtering performed prior to the conversion would be needed to allow full interoperability. This will be discussed later in the dissertation.

2.1.2 IEC 61869

The implementation of process bus has a significant impact on the protection and metering system of the substation. The IEC61869 standard is in place to define the technical requirements for instrument transformers, which includes their performance and test requirements. The key component of the systems mentioned is their associated instrument transformers; the IEC61869 series is in the process of being extended to included two additional parts to cover the introduction of IEC 61850. These two parts are:

IEC 61869 Instrument Transformers - Part 9: Digital Interface for Instrument Transformers

IEC 61869 Instrument Transformers - Part 13: Standalone Merging Unit

Part 9 is presently in draft release that allowed a copy to be obtained for review from a standards body within a particular country. A review of this standard has reproduced the development of IEC61850-9-2LE version that looked more into the requirements of the logical devices. By defining specific technical requirements based on their application is important to allow different manufactures to develop such devices.

The previous parts were inadequate in defining the operation of the main logical device that will enable process bus to be used within conventional medium voltage substation. The uses of non-conventional instrument transformers, which publish the measured value in a digital format within a medium voltage substation, are not cost effective. The merging unit performs the sampling of the analogue system and publishes the information on to the network; therefore, these devices are critical to the operation of the new system. Consulting with the IEC representatives, Part 13 is not due to be released in a draft version until late 2014 with the final publication due January 2015.

2.1.3 Ergon Energy

Developing a standard design will ensure that what is designed and constructed will consistently comply with Australian standards, AER and AEMC within Ergon Energy's network infrastructure. The company standards in all cases either meet or exceed legislative requirements, these requirements are typical safety clearance or ratings.

The introduction of sampled values and process bus architecture into the substation will have considerable impact on the protection and metering standards. Within the standards, they clearly define the requirements of the equipment. The protection standards *STNW1002 – Standard for Substation* Protection defines the requirements of the protection systems for Ergon Energy assets.

The architecture has been defined based on the use of either "X" and "Y" or "Main" and "Backup" configuration to support the criticality of the asset that was being protected. The connection of these configurations is predominantly independent of one and other. This means that each protection scheme requires separate instrument transformers, protection relays, DC supplies etc. The duplication is to ensure that in the event of a common mode failure of an individual part it does not compromise the overall system; an example of this is to use different relay manufacturers.

The protection system is not only designed to isolate a faulty part of the network but also to reduce the number of customers impacted by the fault. The protection system may cover a larger customer base, in particular for back up protection that may rely on a remote location to isolate a fault in the event of the primary protection failing to operate.

The development of the process bus architecture must demonstrate that the reliability and availability of the system is adequate to be implemented as a company standard. The rules set throughout the existing standard in reference to main and back up protections will be maintained within the development of the new architecture.

Ergon Energy has also developed standard full substation designs to accommodate the needs of the business. These designs were developed to allow future infrastructure to be built without the need to complete full design from the ground up. Given the diverse requirements throughout their network, these designs ranged from a single 6.3MVA substation to a dual 32MVA substation. For the purpose of this project, the Z6-32D was used. To simplify the process a recently constructed version of this standard, Oonoonba substation, was used as there were information regarding the full primary and secondary systems.

A simplified single line diagram showing the primary system's connection can be seen in Figure 4 .This single line diagram will be used to develop the ultimate arrangement of the proposed process bus architecture and allow for comparison of the two systems.

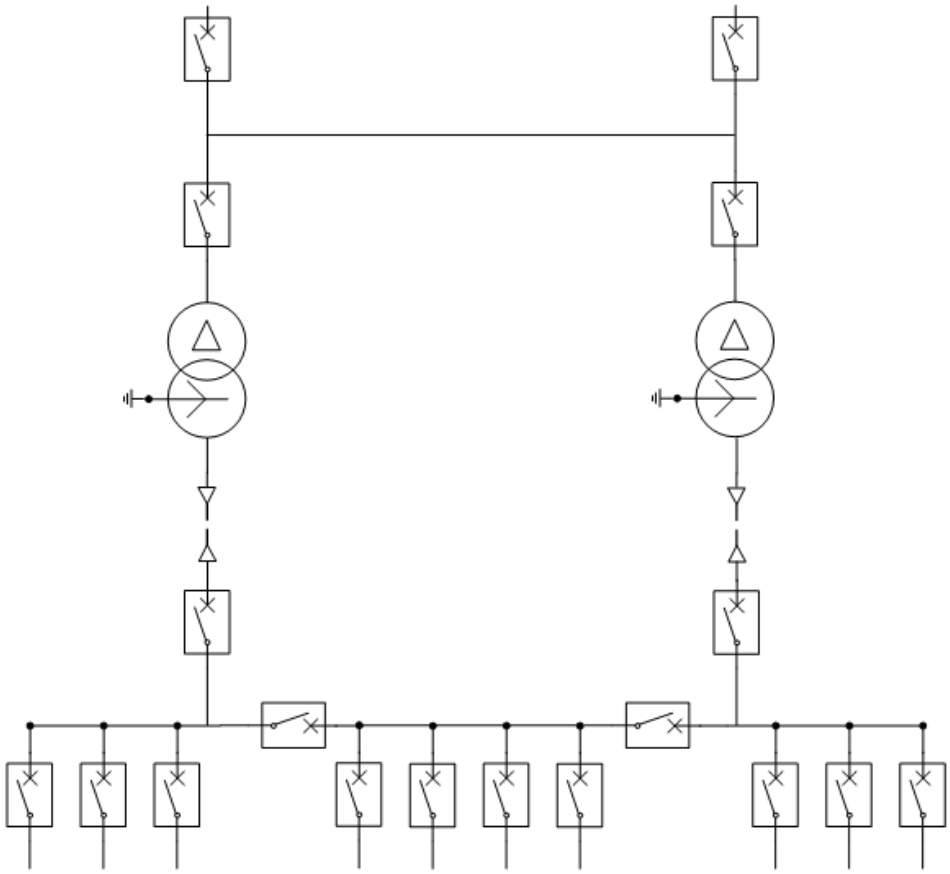

Figure 4 – Simplified Operating Single Line Diagram of Oonoonba Substation

2.2 Measured Values

2.2.1 Sampled Value

Sampled values is the term given to the data set that was produced from an analogue to digital conversion. Existing numerical relays presently perform the analogue to digital conversion within the single case unit and use a data bus to transfer the information to the logical part of the device to perform the appropriate algorithm. The introduction of IEC61850-9-2 has brought about a standard in which these sampled values are now to be shared amongst other multifunction IEDs. To allow this, the standard defines the application of a new device "Merging Unit" which is tasked with gathering information and broadcasting it over a communication bus.

A recent paper by *Alexander (2010)* stated important differences between the sampled data presently being performed in a numerical relay and that of a merging unit. These were:

- While in the relays the sampling is controlled by the IED and is usually using frequency tracking, in IEC 61850 all interface or merging units are time synchronised with an accuracy better than 1 microsecond and use a fixed number of samples per cycle at the nominal frequency
- The sampled values in the IED are exchanged directly between the A/D converter and the processor, while IEC 61850 they are transmitted using typically multicast from the merging unit(publisher) to all IEDs (subscribers) that need these sampled values
- The sampled values in IEC are primary quantities

This author has thought about the differences in the transportation of these measurements rather than the measurement itself. Given the process in which a sample is taken can ultimately influence the system's design to use it; this brings about the appreciation of this impact.

Alexander (2010) and Benton & Alexander (2006) discussed the impacts that a merging unit could have on the system using measured values. The introduction of the merging unit meant that, protection device which were dependant on a number of measured values would be receiving sampled data from multiple merging units. *Benton & Alexander (2006)* proposed a simple block diagram showing the process within a merging unit, which can be seen in Figure 5. The delay within this system has the potential to impact on a protection schemes that are dependent on a number of sampled values. Also extracted from the same paper is an illustration of this delay as shown in Figure 6, if poorly dealt with it could be seen as a phase shift.

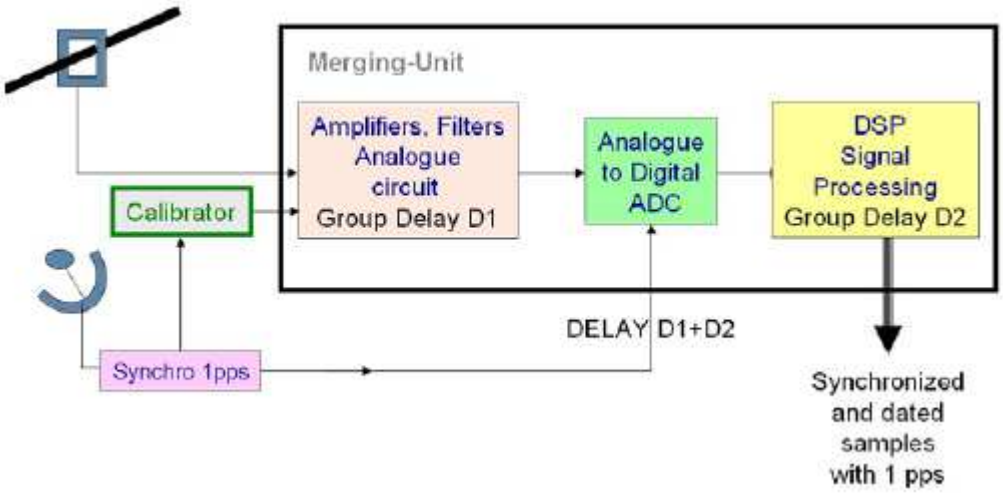

Figure 5 – Simplified block diagram of a merging unit (Vandiver & Apostolov, 2006)

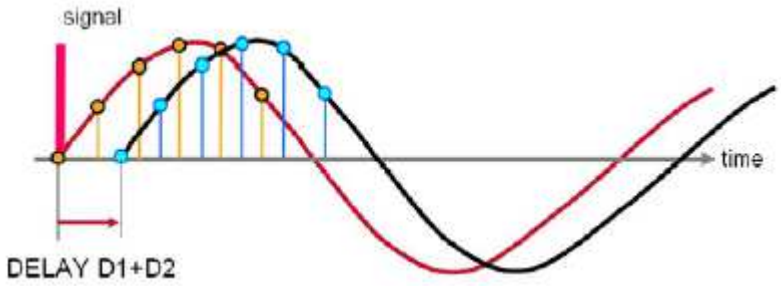

Figure 6 – Analogue signal phase shift due to not compensating for the delay (Vandiver & Apostolov, 2006)

Throughout my review I had found a number of articles which analysed the use of non-convention instrument transformers and very few for the implementation of analogue merging units. The impact studies that showed how the introduction of the merging unit had on the change in requirements of the primary systems would only be included as an insert similar to section 3 of *IEC 61850 Process Bus benefits of IEC 61850 9-2 Process Bus Applications and Benefits*. A. Apostolov *(2010)* discusses the removal of the lead resistance from the secondary burden due to the merging unit being located near to the instrument transformer.

The literature review identified that there is limited information regarding the impact of the sampled data resolution on the protection device. Given the difference in present practices of different relay manufacturers, these sampled value qualities have the ability to impact on the interoperability of the IEC61850 standard.

2.2.2 Current Transformer Models

The measured value that is produced by the instrument transformer is critical in determining the performance requirements of the secondary systems. The performance criteria for new instrument transformers are dictated by the requirements of the intelligent devices, which uses the measurement. Existing substations where the secondary systems are to be replaced are governed by the existing primary plant's performance qualities.

A review of *Network Protection & Automation Guide (2011)* described the requirements for protection applications. This has revealed that the main criteria for a current transformer is it saturation characteristics. The simulation of a saturated current transformer has been discussed in numerous papers for the development of a mathematical model for a current transformer. The initial stage of developing a mathematical model was to understand the components and connection of the system, a simple transformer equivalent circuit will not conform to the actual operation of a current transformer.

Amongst the journals that were reviewed, *Noshad*, et al. (2013) illustrated the model in a simplistic form that connected the system to a current source, which is equivalent to the primary side being replicated ideally on the secondary side of the current transformer as shown in Figure 7. The key feature is the identification of the non-linear inductor for the magnetising arm of the transformer and the introduction of the magnetising current (i_μ).

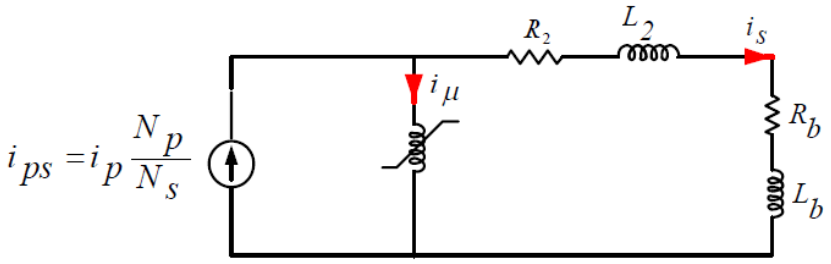

Figure 7 – Current Transformer model referred to the secondary side (Noshad, et al., 2013)

Noshad, et al. (2013) went on to develop a MATLAB® model based on the relationship of the flux linkage and magnetising current. To determine the relationship that this model was based on, the information regarding the material with which the current transformer was constructed of and the way in which it was constructed is required.

In January 2000, Working group C-5 of the Systems Protection Subcommittee of the IEEE Power System Relaying Committee published a paper *Mathematical Models for Current, Voltage, and Coupling Capacitor Voltage Transformers*. This paper explored the use of existing Power System Simulation software, such as Electromagnetic Transients Program (EMTP) to determine guidelines for the physical elements within an instrument transformer that are impacted by transient conditions. This paper is similar to the previous paper, as it too required specific construction details about the current transformer to complete the model.

The limitation of the information known about the current transformer is the determining factor in the construction of the mathematical model. The available literature required more detail regarding the construction of the instrument transformer. Within the industry, there has been an identification of this need to produce wave files to test protection relays. In 2003, a company named NxtPhase developed a model within Microsoft Excel to produce a waveform for a protection class CT operating in a saturated state.

The review of the information within this model, which refers to as an IEC Version referencing IEC 44-1 First edition 1996-12, has revealed that it was developed to use data known about a "P" class current transformer. Within Ergon Energy and for the purpose of this dissertation a "Px" class current transformer is to be used. The accuracy of the model for the purpose of this project is not significant and that the error will be common to all analysis.

The review of literature available for developing a mathematical model for a current transformer has been covered extensively. The area with which for the purpose of my dissertation is lacking and that there is no clear literature covering the application that is needed.

2.3 Communication Network Architecture

2.3.1 Network Designs

Oxford University Press (2014) defines "Network" as "A group or system of interconnected people or things". The design of a network is determined by the application and its dependencies. Two networks that have similar application and dependencies would be the electricity and telecommunication networks. Both of these networks are critical to the way in which society can function in today's environment. Therefore, government agencies or regulators place certain conditions on the availability of these networks.

To assist with designing reliable networks the industry working groups develop standards that assist these companies to comply or improve the way in which they design and construct their infrastructure. One such guide was developed by the Institute of Electrical and Electronics Engineers (IEEE) to assist the power industry; this was *IEEE Recommended Practice for the Design of Reliable Industrial and Commercial Power Systems*. Of particular use is "*Chapter 2 Basic concepts of reliability"* that sets out the terminology, common equations and relationships for reliability evaluations. These evaluations included the construction of either an Availability or Reliability Block Diagram. With these diagrams, the system can be simplified or altered to determine the impact or overall reliability of a complex network. The reduction of a whole system to a single block is process to determine the reliability of a system. The reduction method is best represented by the basic operation of reducing two nodes into one, with two initial configurations of nodes in either series or parallel as shown in Figure 8 and Figure 9 respectfully.

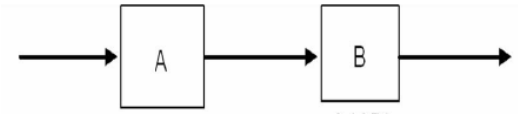

Figure 8 - Series Reliability Block Diagram

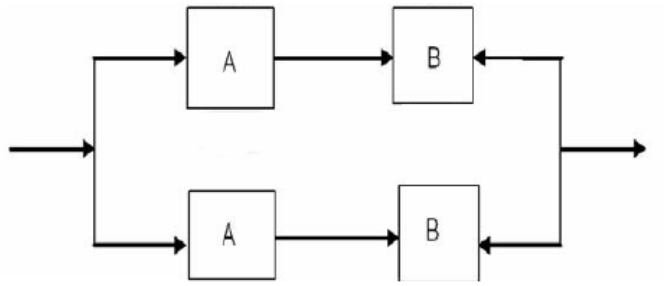

Figure 9 - Parallel Reliability Diagram

Simplifying Figure 8 could be done two ways; the preferred method is to multiply the availability values of each block in series by each other, as per equation (2-1). Simplifying Figure 9 is a little more complicated with the need to determine the probability when both branches will fail. To determine the probability of failure (POF) for a single branch is done using equation (2-2) and then multiply the result for each branch, in this case they are identical, to get the probability of both branches failing at the same time. The availability of the system is then obtained by using equation (2-3.

$$A_{series} = \prod_{i=0}^{n} A_n \qquad (2\text{-}1)$$

$$POF_{\ branch} = 1\text{-}A_i \qquad (2\text{-}2)$$

$$A_{parallel} = 1\text{-}(POF_{\ branch1} \times POF_{\ branch2}) \qquad (2\text{-}3)$$

The application of this type of analysis on a communication network has been best shown by *Babbitt & Pollock (2008)*. Their analysis was conducted on the topology of telecommunication service providers. They started by explaining the need for such an assessment with the introduction of availability being specified in Service Level Agreements (SLAs).

Babbitt & Pollock (2008) introduced the methodology of accessing the topology of a communication network. Throughout the journal, it focuses mainly on the availability, which used an equation that was also stated in IEEE 493 guide, this equation required two parameters of the system to determine the availability of a single component within the system. These parameters are; Mean Time between Failures (MTBF) and Mean Time to Repair (MTTR). Equation (2-4) is the combination of these variables to determine the availability. This paper then discusses the impact these variables have and the way in which a design could improve availability of the network. The concept to take from this is that with an increase in MTBF there will be an increase in Availability, an increase in MTTR results in a decrease in Availability.

$$A = \frac{MTBF}{MTBF + MTTR} \qquad (2\text{-}4)$$

The variation in topology that is available to this type of communication network has been assessed to derive a function, which approximates the cost per 9's. 9's is the terminology given to the reliability of the system, in their journal it is stated that the required number of 9's was four. There were no discussions of communication protocols that could limit the way in which the network nodes can be connected to each other, this limited the use of a similar type of topology for the Process Bus communication network.

The technical journals that assessed the reliability design for common networks shows well-structured procedures however, they lacked the direct application to this project. The reliability and availability assessment is relevant and will be adopted in this project to assess the process bus network.

2.3.2 Process Bus Network

Process bus network plays a significant role in transportation of sampled values enabling the operation of a substation. The key dependants of this information are the protection relays. These devices are part of safety system that is governed by the National Electricity Rules. The system that this bus network is designed to replace is an analogue system that in a traditional application is well known and is a proven method. Therefore, the conversion to a new architecture that is communication based will be heavily scrutinised.

Similar to other networks that were discussed in section 2.3.1 the process bus network is best described by its reliability and availability. To improve the networks reliability and availability the design would incorporate a level of redundancy to reduce the probability of failure to the network. This redundancy is not only considered by the communication paths but also the hardware that is connected.

Tournier & Werner (2010) discuss a number of topologies, which can provide redundancy for the process bus network. The interconnections were based on two basic connection types, Star and Ring connection. To implement these connections a specific communication protocol is required given that in an Ethernet network ring or parallel connections can cause significant data traffic issues and can cause the system to fail. A typical Ethernet network installation uses Rapid Spanning Tree Protocol (RSTP) to identify loops within the network and configure the network so that these loops are eliminated. In the event of a failed link, the system is able to reconfigure itself to take advantage of the redundant path. Figure 10 has been taken from their paper showing the two connection types.

The reliability of the network topology is dependent on how it functions when there is a failure of one component. RSTP is effective for implementation in a typical Ethernet network however; the process bus has a time requirement. A typical RSTP time to restore the redundant path is dependent on the size and complexity of the network but typically can be in the order of over 100ms and very rarely around the low millisecond range. The process bus typically functions on a time precision in the order of microseconds, therefore it can be seen that this protocol does not provide adequate redundancy.

The IEC have published IEC62439 *Industrial communication networks – High availability automation networks* to define the protocols to address the need for reliability protocols for substation automation. In particular, Part 3 of the series is designed specifically for the application of IEC61850-9-2. The two protocols are Parallel Redundancy Protocol (PRP) and High-availability Seamless Redundancy (HSR). The two protocols are used for star and ring topologies respectively, with no time required for the system to correct itself in the event of a failure within the network.

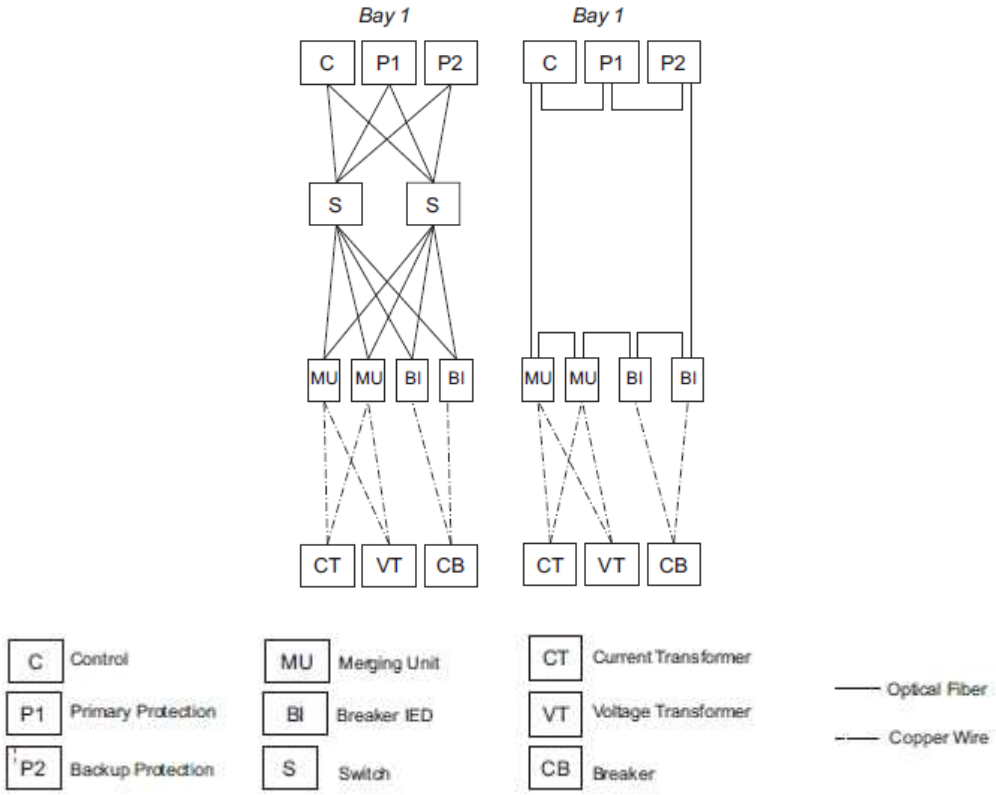

Figure 10 – Star and Ring Network Topology for Process Bus of a Single Bay (Tournier & Werner, 2010)

The mechanics that these redundancy protocols use requires a level of redundancy within the devices. The standard refers to these as singly and doubly attached nodes. The doubly attached nodes are device with redundant ethernet ports. Both protocol uses these ports to send the same message at the same time.

The PRP messages are sent on two separate networks wether this is via physical or virtual separation. In the case of the process bus, the merging unit would send a sampled value message with a prescribed header as per the protocol standard out of each port. Another device, in this case a protection relay with redundant ports, would receive the same message in each port and with an appropriate algorithm be able to reject the duplicate message. Hence, if there is a failure on one network the system is able to continue without interruption.

HSR protocol as previously mentioned is used in a ring type topology. To create the ring all devices are required to have redundant ports as described for a doubly attached node. Using the process bus as an example to describe how this protocol works we start with the merging unit. The merging unit sends a sampled value messages each with the same information with the appropriate suffix out of each port. If a device such as a protection relay, which has subscribed to this sampled value stream, will need to use an algorithm to eliminate the duplicate message.

The other devices in the ring are required to ensure that the message continues around the ring so that all devices see both messages. Therefore, the message is maintained all the way around the ring and then rejected once the sender receives the message on the other port. This has meant that a ring type network has twice as much traffic.

A number of other authors of journals discussing the impact and determine criteria to assess these impacts all follow similar logic. The common analysis is performed on single bay with switches and merging units performing the function for one application within the primary system. This functionality is similar to the architecture that we have in service today. Utilising this arrangement is typically deployed in transmission substations where such things as non-conventional instrument transformers are a cost effective solution and where cost of redundancy due to the criticality of the plant being monitored is allowed at a higher value.

The implementation of process bus into a medium voltage substation such as the type Ergon Energy construct would require a network that has a higher utilisation. The analysis shown in most papers are relevant although the direct application has not been completed. There has also been no identified assessment of the process bus reliability or availability versus that of the system in service today.

Chapter 3

Secondary System Architecture

3.1 Overview

The secondary system architecture has a number of components. These components are responsible for conveying information between different devices to monitor and control the primary system. The introduction of Process Bus as part of the IEC 61850 standard has brought about a new way of conveying that information.

The component of the secondary system that this project is assessing is in respect to the transportation of the measured value. This value has been transformed by a conventional instrument transformer to a level that can be used in sensitive electronic devices. The change to this component is that what is presently being done via a hardwired connection will now be replaced by a communication network.

It should also be noted that the term LV has been used to describe the low voltage plant in a substation. This could be either 11 or 22kV within an Ergon Energy substation. The HV plant has a voltage rating of 33kV, 66kV, 110kV or 132kV.

3.2 LV Feeder Protection Architecture

3.2.1 Change In Architecture Impact Assessment

The LV feeder bay's secondary system network architecture has been selected to perform a case study to assess the impact of the new network architecture. The case study will observe the impact that changing from the conventional hardwire point-to-point system to a communication-based system has on the secondary system's availability.

This selection was based on a block reduction of an ultimate substation secondary system's architecture to a practical solution. The protection for a single LV feeder is a multifunction relay connected to a CT in the feeder bay and a VT selector switch that is connected to two VTs in separate LV bus riser panel on the LV bus. The conventional network architecture of this system and an equivalent Process Bus network architecture have been illustrated in Figure 11.

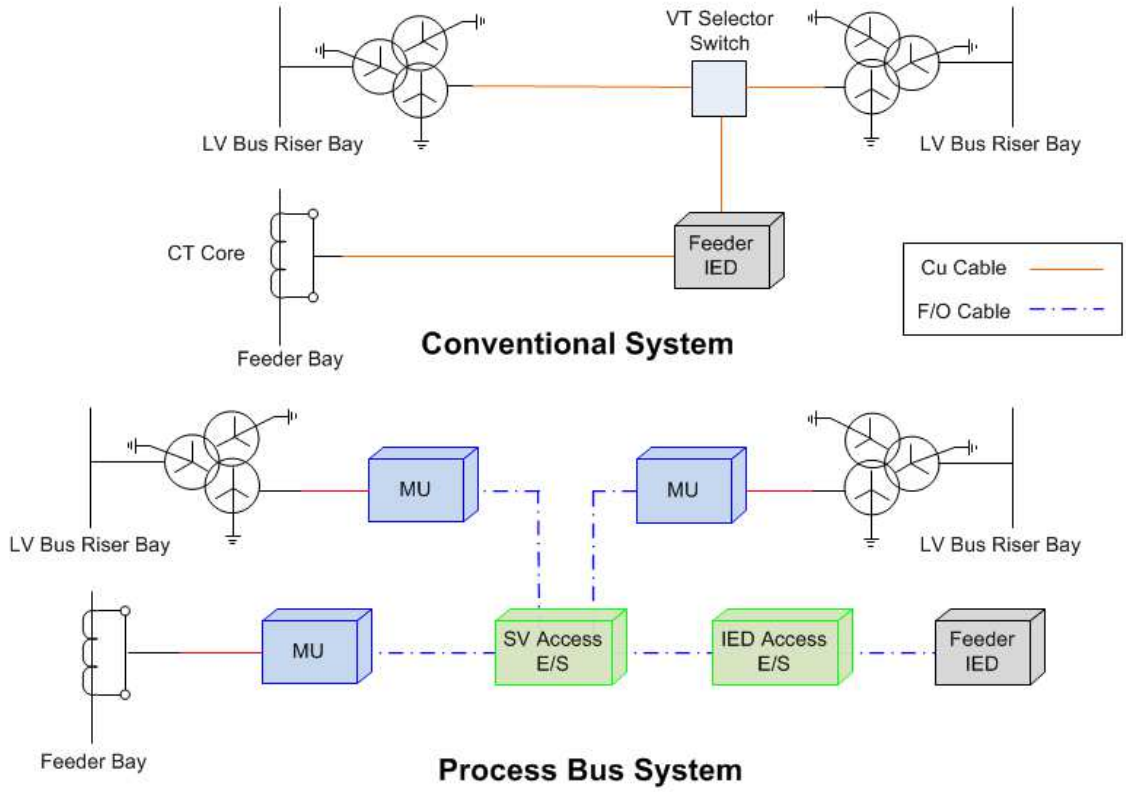

Figure 11 – LV Feeder Secondary System Network Architectures

The process bus system shown in Figure 11 consists of four (4) new components, these are:

- Merging unit (MU) – Creates the Sampled Values (SV) to be published on the Process Bus
- SV Access Ethernet switch – Used to collate multiple SV data streams to be distributed over the Process Bus network
- IED Access Ethernet Switch – Used to allow multiple protection IEDs to access the Process Bus network
- Fibre Optic (F/O) cable – Used for the connection of all the electronic devices communication paths

Both the MU and F/O cables are common to all Process Bus network architectures. The Ethernet switches are considered variables within the construction of the network architecture. The selection of this equivalent network architecture in Figure 11 incorporates a number of assumptions:

- The Sample Values will be shared amongst multiple subscribing protection IEDs
- A separate Ethernet switch will be used for connecting MUs and Protection IEDs to the process bus network

Assessing the change in the system's availability will determine the impact that the changes to the system's components has had. *Tournier & Werner* (2010) and *Schweitzer, et al.* (1997) both completed a similar type assessment on different process bus architectures, these assessments required knowledge of the MTBF for each component within the system. Table 1 below is a collation of data from these journals and *IEEE 493* for the MTBF of components for both systems. The MTTR in Table 1 has been estimated based on:

- The criticality of the system
- The ability of Ergon Energy tradesmen to respond and correct the failure
- The substation is located in an urban location with workshops and strategic spares located within a 50km radius

Device	MTBF (years)	MTTR (hours)	Availability (%)
Protection IED (PIED)	100	12	99.9986
Merging Unit (MU)	150	12	99.9991
Ethernet Switch (ES)	50	12	99.9972
DC Power System (UPS)	100	12	99.9986
DC Cables (DCC)	150	12	99.9991
Optic Fibre Cable (OFC)	50	12	99.9972

Table 1 – Reliability data for components of a protection system (Tournier & Werner, 2010) (Schweitzer, et al., 1997) (Institute of Electrical and Electronics Engineers, Inc., 2007)

The existing and new systems in Figure 11 consist of two main connections, CT to IED and VT to IED. The connection of a VT to the IED incorporates redundancy with the ability to select between two possible VTs. Therefore, a loss of a single component in the CT to IED connection results in a complete system failure and it would take the failure of both VT connections to have a complete system failure. Using equations (2-1), (2-2) and (2-3) from section 2.3.1 both systems can be reduced to a single availability value for comparison purposes. The availability of the existing system as shown in Figure 11 is given by:

$$A_{existing} = {A_{DCC}}^2 \times [1 - (1 - A_{DCC})^2] \times A_{PIED} = 99.9968\% \ (four\ 9's)$$

In addition, the availability of the new system is given by:

$$A_{new} = A_{MU} \times {A_{OFC}}^3 \times [1 - (1 - A_{OFC} \times A_{MU})^2] \times A_{PIED} \times {A_{ES}}^2 = 99.9895\% \ (three\ 9's)$$

The results of the availability assessment have shown a reduction of one 9's. The reduction of protection system's availability should not be considered best practice. The reduction in availability can be linked to the number of additional electronic devices required in the Process Bus network architecture such as the Merging Unit and Ethernet Switches.

Improving the availability of a Process Bus system can be done by two means:

- Install devices which have higher availability
- Incorporate redundancy in to the network architecture

The first option to utilise devices with higher availability would still mean that the introduction of new electronic devices would reduce the availability. However, the overall impact might not be as significant, it is expected that there will still be a reduction in the system's availability. Given that Table 1 defines the availability of these device based on industry experience this option will not be further explored.

The development of the communication protocols such as PRP and HSR, explained in section 2.3.2, allows redundant communication paths to be incorporated into the network. Duplicating electronic devices and utilising redundant communication paths allows the system's availability to be improved.

3.2.2 Process Bus Network Architecture Redundancy

Process Bus network architecture's redundancy is limited by the functionality of the IEDs within the network. The main limiting factor is the inability of a process bus protection IED to be configured such that if it loses the current-sampled values from one merging unit it is unable to automatically change over and use of the current-sampled values from another merging unit.

The Protection IEDs do have the ability to switch voltage-sampled values, ALSTOM (2013) technical manual for a protection IED that is IEC 61850 -9-2LE compliant is an example of this restricted functionality. Given this restricted functionality, the duplication of a merging unit will not be considered unless it is for use in a second protection IED.

3.2.2.1 Singly Attached Node (SAN) IED Redundant Network

This level of redundancy maintains a similar communication structure as the Process Bus network architecture in Figure 11 with all electronic devices being SAN and maintaining the same network utilisation assumptions. Figure 12 below is the network configuration with only the protection IED being duplicated.

The system shown in Figure 12 introduces another parallel path into the availability block diagram due to the redundant protection IEDs. Utilising all three availability equations given in section 2.3.1 the – LV Feeder Process Bus Network Redundancy Architecture 1 has an availability of 99.9918%

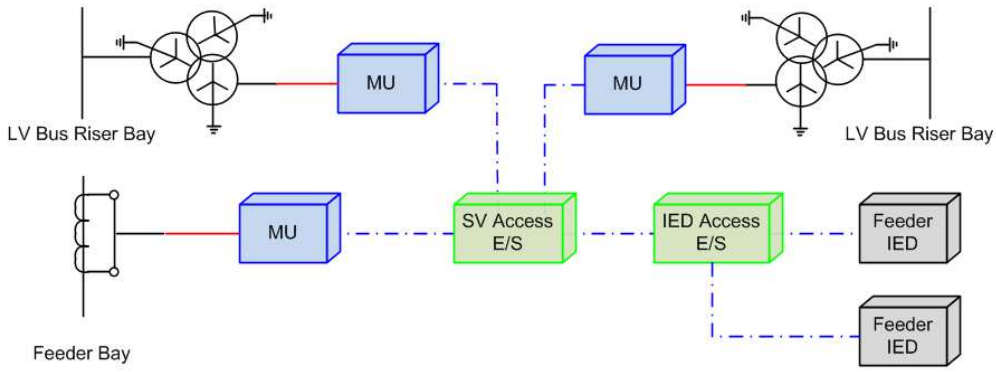

Figure 12 – LV Feeder Process Bus Network Redundancy Architecture 1

A system comprising of two protection IEDs such as the one in Figure 12 is able to utilise a second merging unit. Figure 13 shows the connection of this system with each protection IED subscribing to a separate merging unit's sampled value data stream.

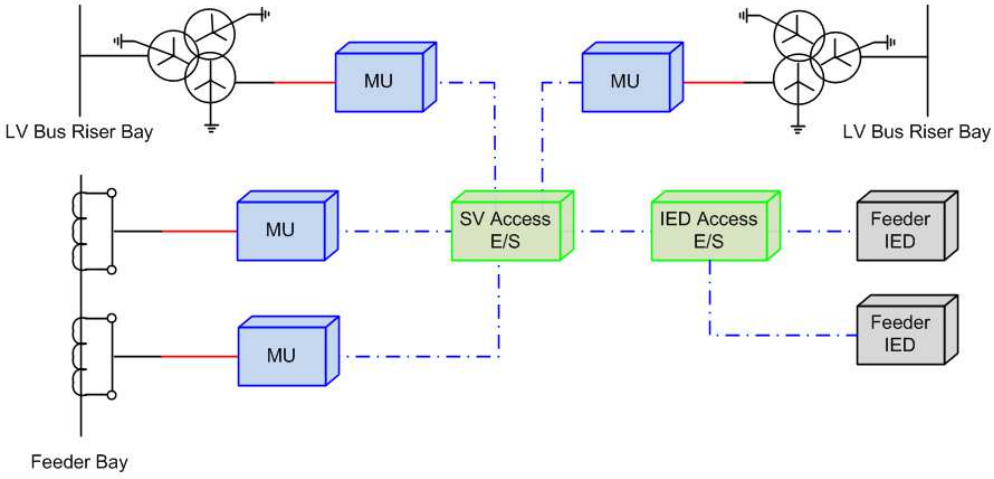

Figure 13 – LV Feeder Process Bus Network Redundancy Architecture 2

The full redundancy of the IEDs within the system has resulted in availability of 99.9936%. It can be seen from the assessment that communication pathway between the SV access points and the IED access point has a significant impact on the overall system availability.

3.2.2.2 Doubly Attached Node implementing PRP (DANP) Redundant Network

A redundant communication path can be created using a combination of software and hardware based networks. The software component can occur within the Ethernet Switches using Virtual Networks known as VLANs. Throughout the following assessments, it is assumed that all Ethernet switches have the following functionality:

- They are manageable – Allows for Multiple VLAN configuration
- Capable of performing the tasks of a RedBox as defined in IEC62439-3

The Process Bus network architecture shown in Figure 11 has the ability of utilising PRP to create redundant communication pathway between the Merging units and protection IED. Figure 14 below shows the connection of the network with redundant communication paths.

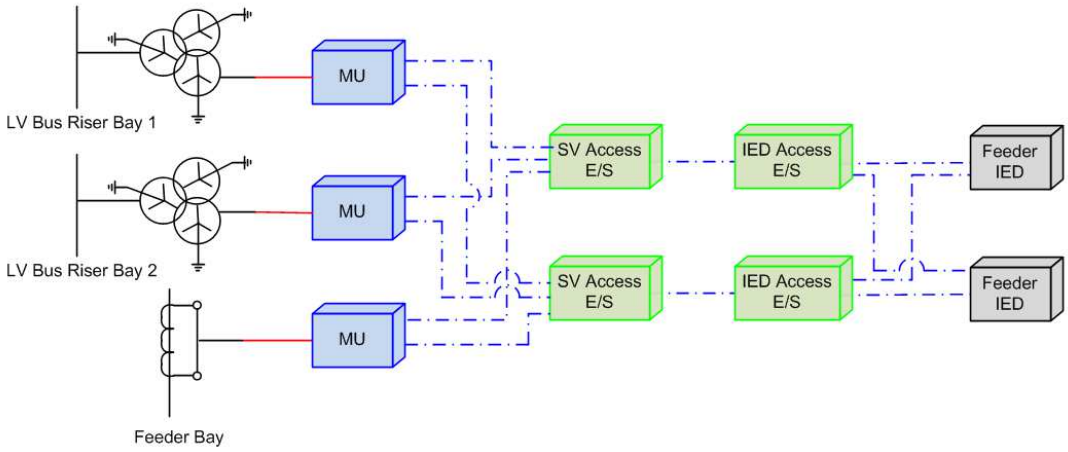

Figure 14 – LV Feeder Process Bus Network Redundancy Architecture 3

The implementation of PRP utilising doubly attached nodes has introduced another level of redundancy for the VT signal. An assessment of the availability of the connection between the voltage transformer merging units and the SV access Ethernet switches has resulted in the availability being 100%. Having this high availability is the reason for this part of the network being omitted for the remaining of this case study.

A single branch of the parallel communication pathways for the CT signal consists of three Fibre optic cables and two Ethernet switches. With the redundancy in the communication path and maintaining the original number of IEDs, the network's availability is 99.9977%. The introduction of the redundant communication path has increased the availability of the process bus network to that of the original network architecture.

The network's availability can be further increased by introducing redundancy of the IEDs connected as seen in section 3.2.2.1. Given the network is already configured for DANP the second protection IED will utilise this as the option as a SAN protection IED would not be the preferred solution. Figure 15 shows the inclusion of a second DANP Protection IED.

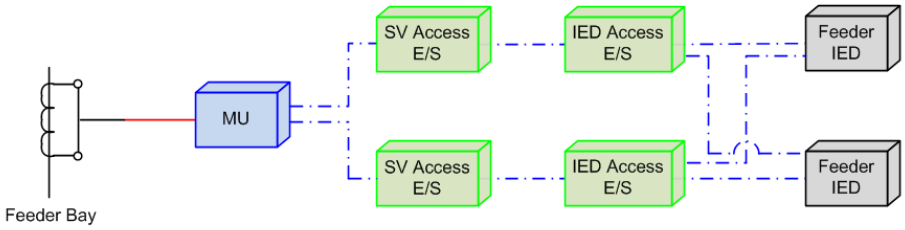

Figure 15 – LV Feeder Process Bus Network Redundancy Architecture 4

Having both a redundant communication path and protection IEDs has resulted in the availability of the process bus network increasing to 99.9990%. This new availability exceeds the original network architecture's availability and increases the number of 9's to five (5).

3.2.2.3 Doubly Attached Node implementing HSR (DANH) Redundant Network

HSR requires the use of a new type of Ethernet switch referred to as "RedBox" or "QuadBox" in the IEC62349-3 standard. These types of Ethernet switches allows the interconnection of the multiple HSR networks or connecting a SAN to either a PRP or HSR network to utilise the redundant communication paths. The availability of a HSR network is dependent on the number of IEDs within the ring. Figure 16 below shows the typical connection that would be utilised between the SV access network and the IED access network, it should be noted that the dotted line indicates that more IEDs can be added or removed from the network. This configuration also does not allow for redundancy of the communication link between the different access networks.

The system's availability is dependent on the number of other IEDs on the ring. The network architecture has been assessed for a range of IEDs in each ring ranging from the minimum number of IEDs required to perform the protection function up to eight (8) additional IEDs split evenly on each parallel path.

$$A_{sys5}(\mathrm{n}) = A_{MU} \times [1-(1-A_{OFC})^2]^2 \times [1-[1-(A_{MU}{}^n \times A_{OFC}{}^n)]^2] \times A_{RED}{}^2 \times A_{OFC} \times [1-[1-(A_{PIED}{}^n \times A_{OFC}{}^n)]^2] \times A_{PIED} \quad (3\text{-}1)$$

Where: $n = Number\ of\ additional\ IEDs\ in\ a\ parallel\ path$

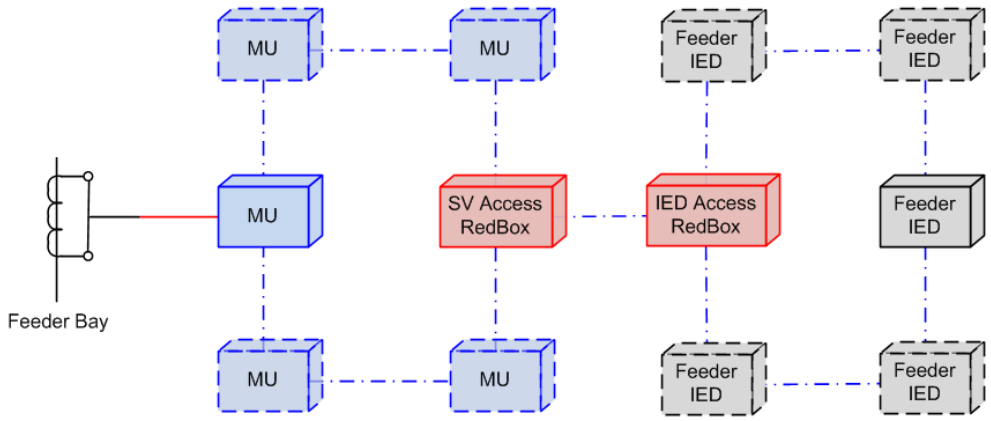

Figure 16 - LV Feeder Process Bus Network Redundancy Architecture 5

Equation (3-1 above describes the availability function for the Process Bus network architecture shown in Figure 16. The results from the above analysis show that by increasing the number of IEDs in each parallel path has minimal effect on the overall network availability. The results for the network's availability with the minimum number of IEDs being 99.99477% and the worst-case scenario resulting in an availability of 99.99476%.

The availability of the network is still below the original network architecture. To improve the availability of the system the connection between the two access networks will incorporate redundancy. This is achieved by using additional RedBoxes as described in *IEC62439-3* (International Electrotechnical Commission, 2012). The new Process Bus network architecture can be seen in Figure 17 below.

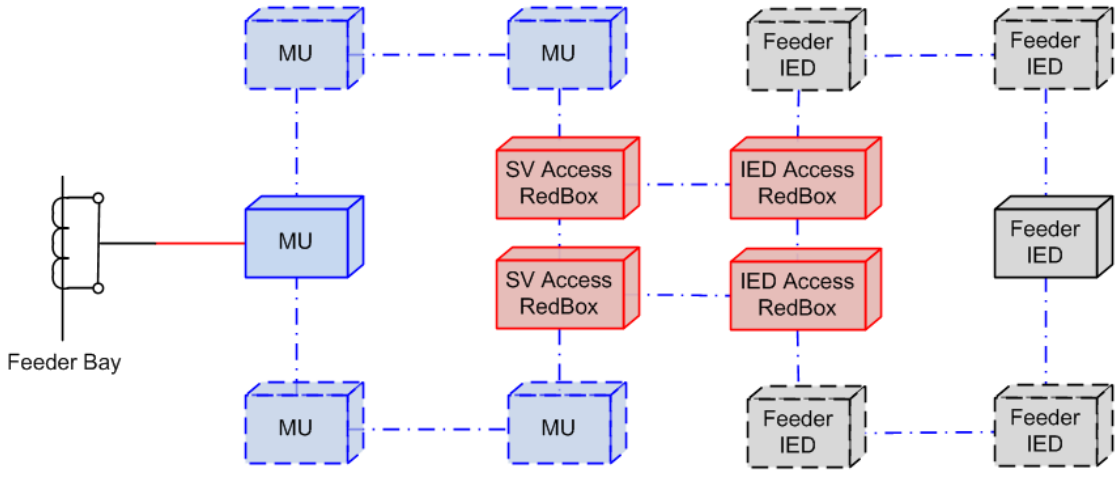

Figure 17 - LV Feeder Process Bus Network Redundancy Architecture 6

The additional IEDs in the parallel paths have no impact on the network's availability when interpreting the result with precision to the fourth decimal place. Therefore, the assessment of the availability for the network shown in Figure 17 is based on the worst-case scenario of four additional IEDs in each parallel path. The result obtain for this network was 99.9977%, which when compared with the original network architecture is the same.

The combination of redundant communication paths utilising HSR and redundant protection IEDs similar to that for the DANP assessment conducted in section 0 is an option to improve the network's availability. The inclusion of the redundant protection IED increases the system's availability to 99.9990%. This availability of a system with both a redundant communication path and protection IED has the same improvement in availability whether HSR or PRP has been used.

3.2.2.4 Combination of DANP and DANH Redundant Network

Process Bus network architectures that combine different redundancy protocols, such as HSR and PRP, into one network are heavily dependent on the functional ability of the RedBox. The ability to configure the RedBox to appropriately filter the redundant packets, then apply the appropriate new redundancy protocol suffix into the packet so that the subscriber can identify the redundant packets. Figure 18 below consists of two network topologies using the combination of the two types of redundant protocols. In these cases, the SV access network and IED access network would be opposite to the other.

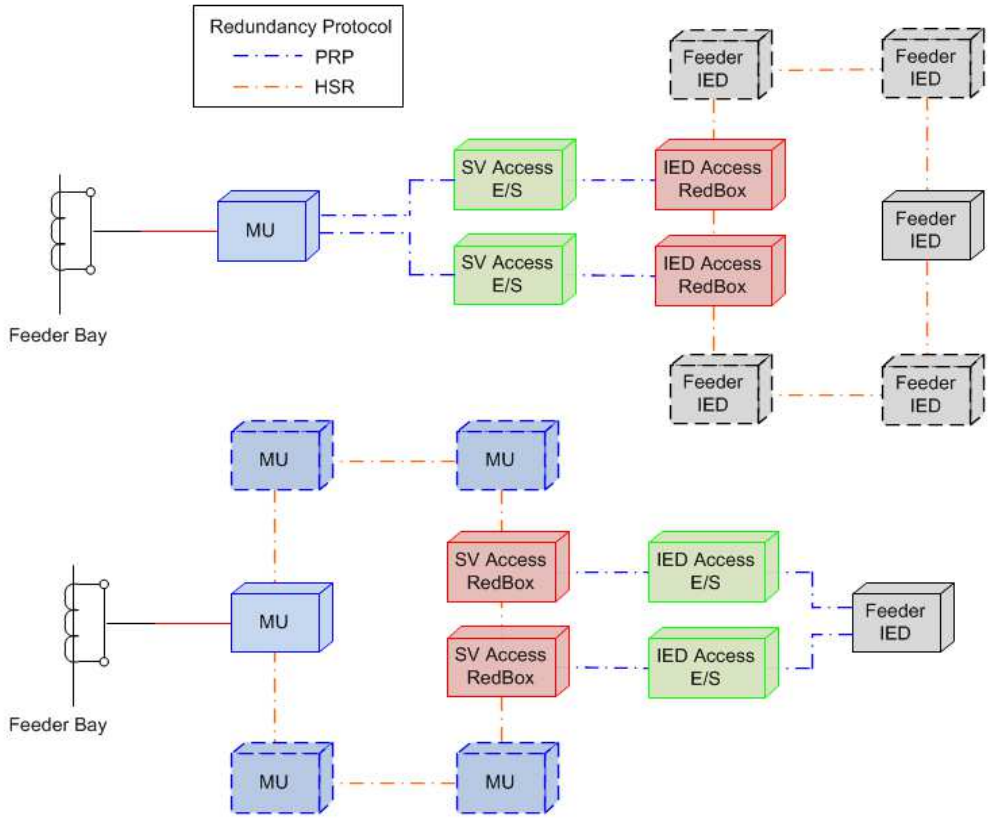

Figure 18 – LV Feeder Process Bus Network Redundancy Architecture 7

The two network topologies shown in Figure 18 are very similar with the creation of parallel communication paths. The difference will only be seen when adding redundant protection IEDs. The availability assessment confirmed this with only a slight increase when the HSR ring consisted of Merging Units given their higher availability compared to that of the protection IED. The availability of the network that used the combination of DANP and DANH devices was the same as the networks utilising only one type with an availability of 99.9977%.

3.2.2.5 Sensitivity Analysis

The values of MTBF for the new devices introduced into the network have been taken from previous bodies of work for assessing the availability of a Process Bus system. Manufacturer supplied MTBF values are based on the number of units sold verse the number of units that had reported failures. These devices are new to the industry and using actual data to determine the MTBF can lead to a miss representation of what can be expected.

A sensitivity analysis has been conducted on the impact that these inaccuracies for the MTBF of a merging unit, optical Fibre cable and ethernet switch will have. The methodology adopted for this uses the Monte Carlo method, which is defined as:

"A Technique in which a large quantity of randomly generated numbers are studied using a probabilistic model to find an approximate solution to a numerical problem that would be difficult to solve by other methods." (Oxford University Press, 2014)

The sensitivity analysis will be conducted so that the relative error in the MTBF for the three new components of the Process Bus are assessed individually. The relative error will only be looking at the minus component, as this analysis will assume worst case that the specified values for the MTBF used in the previous assessments is the upper limit.

Figure 19 below shows the process flow for determine the probability that the systems availability will be greater than equal to that of the existing network's availability as the relative error is increased.

The sensitivity test for the MTBF value of the merging unit has shown that when the relative error is less than -55% the networks availability will be either equal to or greater than the existing network's availability. This means that the MTBF could range from approximately 67 to 150 years. Figure 20 below is a plot showing this result.

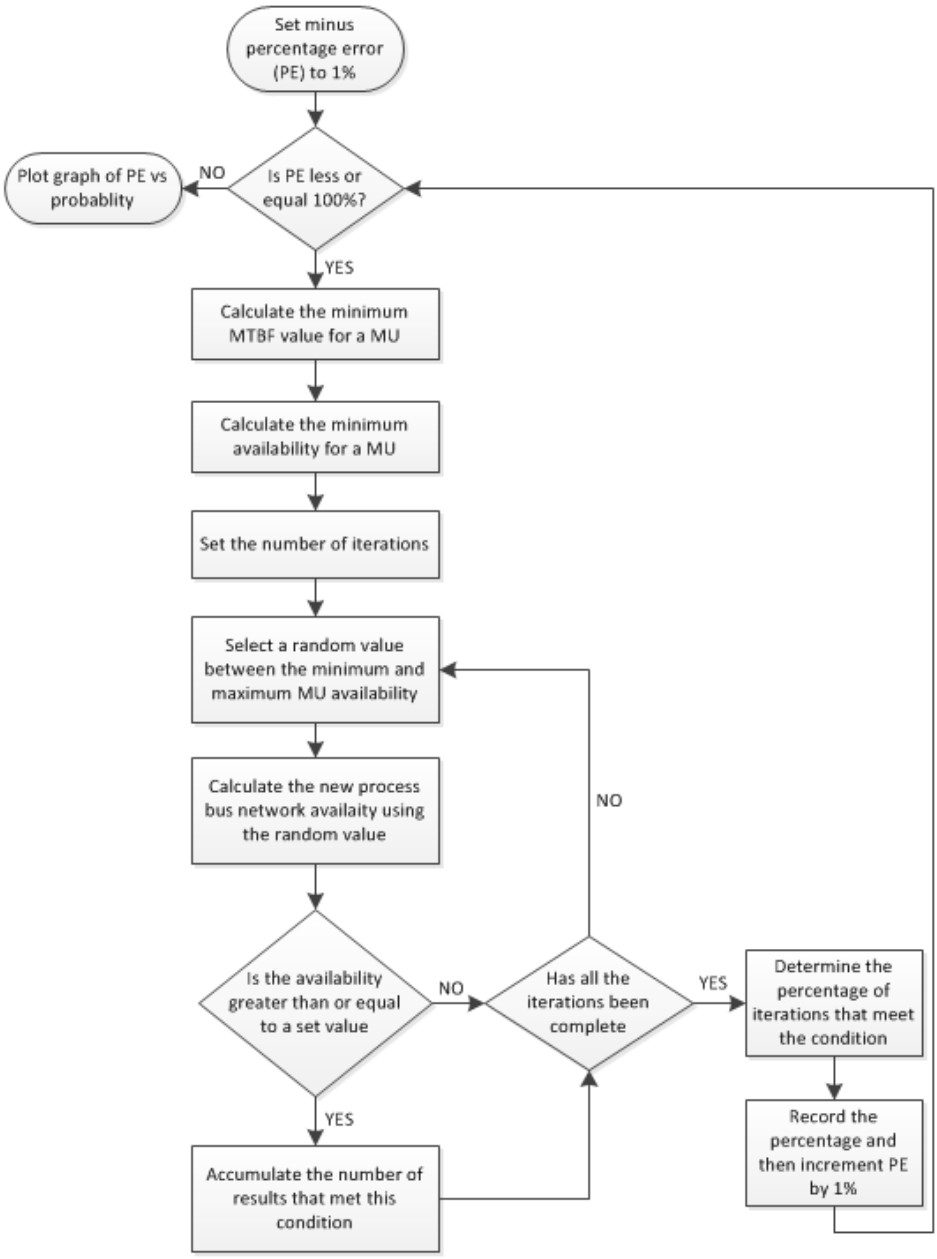

Figure 19 – Process flow diagram for assessing the sensitivity of the Merging Unit's MTBF on the network's availability

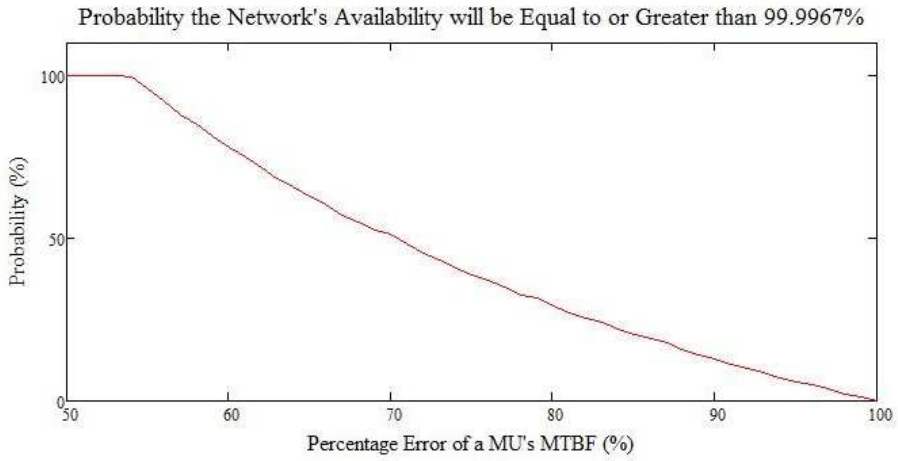

Figure 20 – Sensitivity analysis results for a merging unit's MTBF

The sensitivity test for the MTBF value of both the ethernet switch and fibre optic cable has shown that the relative error has little impact on the network's availability. Both components could have a relative error of -97% before the network's availability is impacted. Figure 21 below is a plot showing this result.

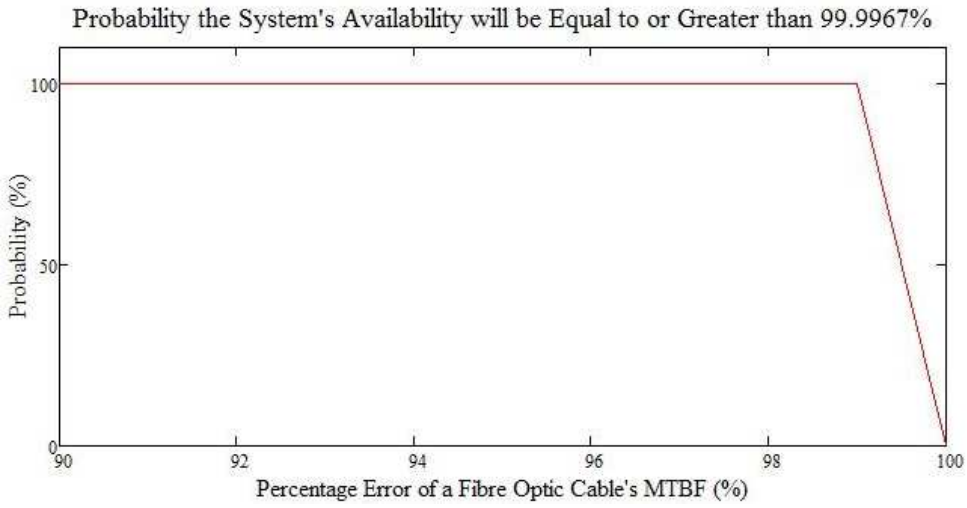

Figure 21 – Sensitivity analysis results for a fibre optic cable's MTBF

These results have concluded that the use of the MTBF values defined in Table 1 for these new devices is an acceptable practice.

3.3 Ultimate Process Bus Architecture

3.3.1 Conventional Substation Secondary System Architecture

The conventional architectures shown previously in Figure 11 consist of the following components: CT core, VT winding, control cables and the protection relay. This architecture is very simplistic due to the limitations of the components within the network; these limitations will been discussed later in this dissertation. Section 2.1.3 outlined Ergon Energy standards that included both an ultimate substation design for a two-32MVA transformer zone substation and specific standards that defined the requirements of subsystems with in the standard design. The main standard that influences the secondary system architecture is the Protection Standard STNW1002.

To implement the protection standard for the ultimate arrangement it required the use of multiple CT cores in individual bays throughout the substation, individual control cables from the CT marshalling boxes directly to each protection relay and the inclusion of redundant protection schemes to provide the appropriate level of backup protection deemed best practice based on the Nation Electricity Rules.

The analysis of the system's availability for the ultimate substations secondary system is quite complex. The complexity lies in the analysis of all the different functionalities that occur within the system. This project is focused on the impact that the implementation of sampled values has on the system. Therefore, the availability of the system is limited to the devices in the network that are responsible for the transfer of the secondary measurement obtained by the instrument transformer to the protection relays that uses this information to make a decision.

The key factors in assessing the systems availability is to identify smaller system's within the network that do not directly influence each other's individual availability. This breakdown will identify where parallel paths occur and allow the block reduction procedure to be used to determine the complete system's availability. Please note that a failure of the whole system as part of this analysis does not imply that all protection functionality of the safety system is breached.

3.3.1.1 LV Protection

The LV protection consists of two main protection schemes, these are:

- Feeder protection, &
- Bus Protection

Due to the nature of the equipment being protected, the standard does not require that the protection be duplicated. Instead the backup protection can be performed in a more cost effective/ practicable way.

For reliability purposes through studies of distribution loading for feeders, Ergon Energy has adopted a three-bus section arrangement for the LV component of the substation. The single line diagram in Figure 4 illustrates that the two outer sections support three outgoing feeders and the middle section supports four. Each feeder consists of a secondary system as shown in Figure 11.

Each section of the LV bus is also protected using a high impedance differential protection scheme. This scheme requires an electrical summation of all currents entering or leaving this bus section hence a control cable from all bays is needed. The two outer bays have the same configuration; they both use a CT core from three feeder bays, one incomer bay and one bus section bay. The inner section is slightly different with the use of a CT core in four feeder bays and a core in each bus section bay. These two networks can be seen in Figure 22 below.

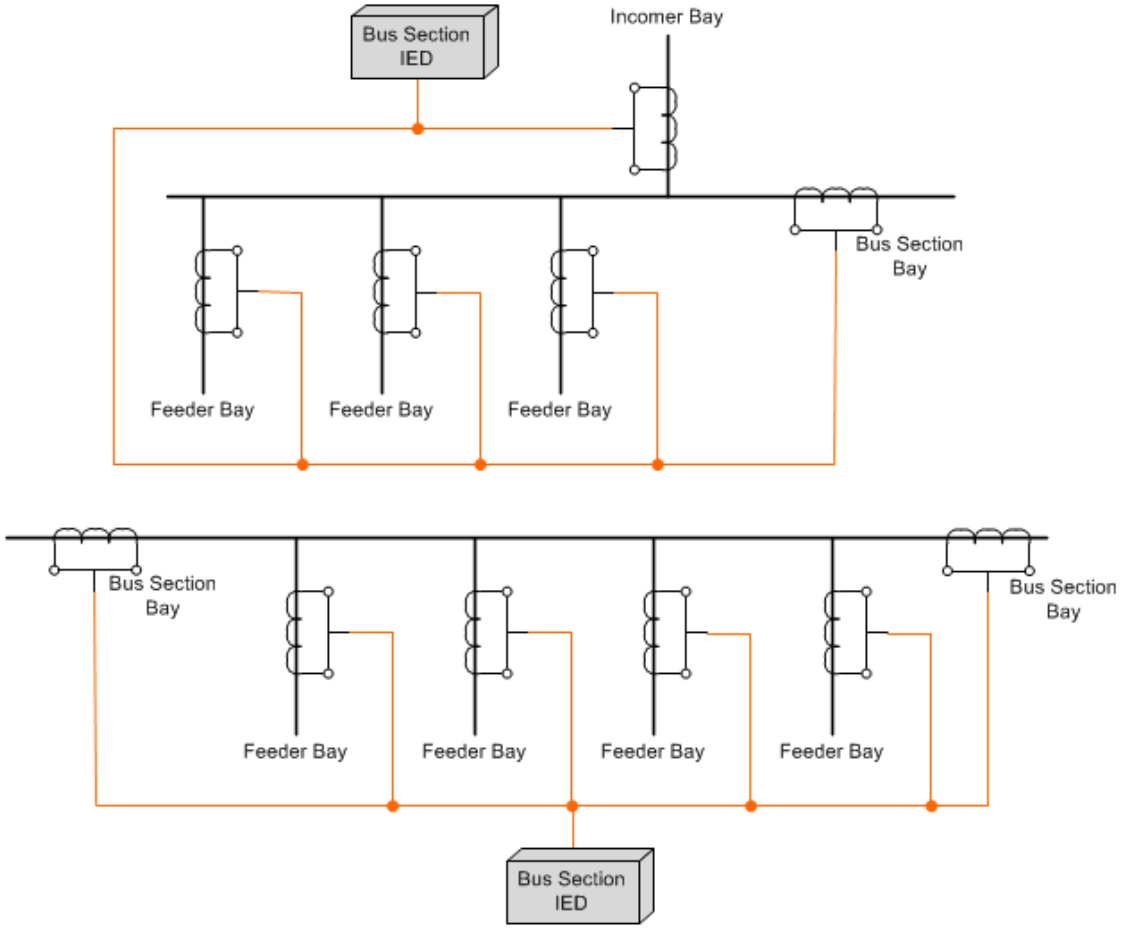

Figure 22 – A Conventional LV Bus section's protection connection diagram

The bus section and feeder protection schemes are backed up using a summated overcurrent protection scheme. The method for this scheme is to summate the CT measurements of the bays that has the potential to supply current to the faulty section of the network.

Similar to the bus protection schemes shown in Figure 22 the current from the CT Cores used to supply the measured values are electrically summated. The two outer sections have similar connections that electrically summate a CT core from the Incomer bay and the Bus section bay. The middle section summates the measurement from a CT core in each of the Bus section bays.

The Availability block diagram for the LV component of the substation can be seen below in Figure 23. Using block diagram reduction the LV secondary system component of the substation has been evaluated to having an availability of seven 9's.

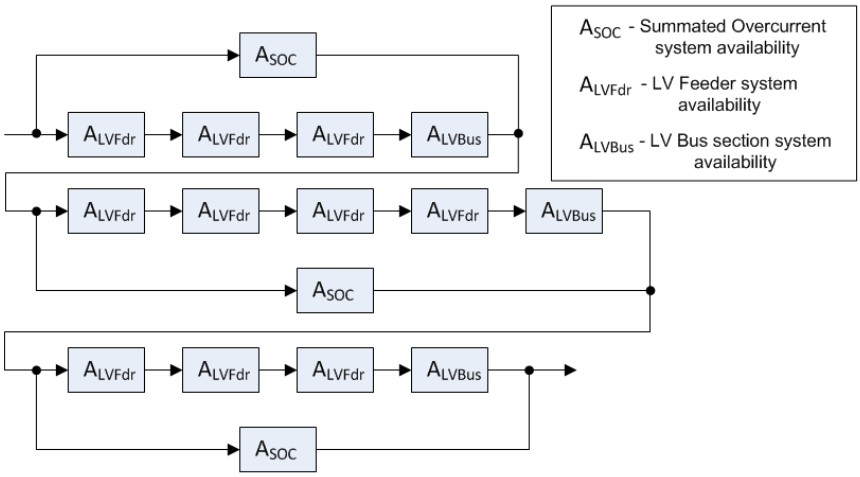

Figure 23 – Ultimate substation's LV secondary system availability block diagram

3.3.1.2 Transformer Protection

The ultimate substation arrangement consists of two power transformers. Due to the criticality and cost associated with this type of equipment the protection standard defined the requirement for the protection scheme to be duplicated. The protection scheme selected for protecting a power transformer is a low impedance differential scheme. The benefit of this scheme is its ability to use the intelligence of the protection relay to adjust both the mismatch in current magnitude and phase angle due to the effect the power transformer has on the primary current of the system. The relays used for this protection also have the added function of not just a differential pickup but also pickups for both HV and LV over current.

The connection of the protection schemes for each transformer is the same. Given this, Figure 24 below shows the secondary connection for a single transformer.

The connection diagram shown in Figure 24 can be converted into an availability block diagram similar to the LV part of the substation. This block diagram would show two parallel systems in series. Each branch of the parallel path would have equal availability given that the protection systems a duplicated. Therefore, the availability of the transformer secondary system component of the substation has been determined to be eight 9's.

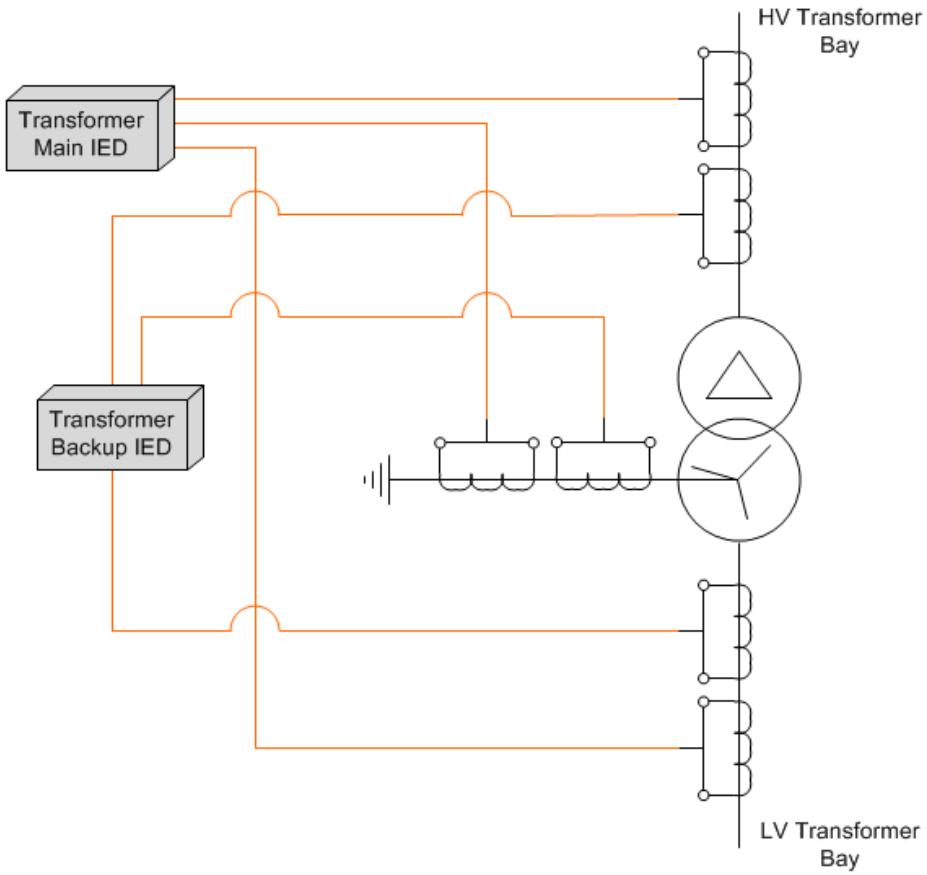

Figure 24 – A Conventional transformer's protection connection diagram

3.3.1.3 HV Protection

The HV protection architecture is similar to the LV protection architecture, the difference being the level of redundancy that has been built into the system. The primary system that these protection schemes are used for can cause significant damage and have the potential to cause serious harm, Ergon Energy has deemed that there shall be duplicate protection schemes similar to the requirements of the transformer protection. This duplication is similar to the conditions that the National Electricity Rules place on a Transmission Network Service Provider.

The protection of a HV feeder can be done in a variety of ways, for the purpose of this analysis a non-communicating distance protection scheme has been used for both the main and back up protection schemes. Figure 25 below shows the typical connection of the HV feeder protection.

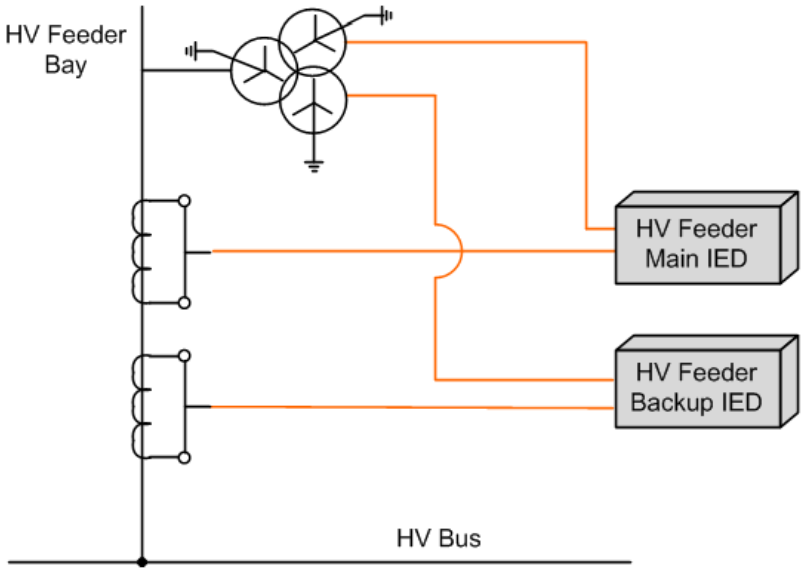

Figure 25 – Conventional HV Feeder's protection connection diagram

The example used to perform a base analysis on consists of a single HV bus section with two HV feeders and two transformer bays connections. The HV bus is protected using the same type of protection as the LV bus, High Impedance differential protection. The back-up protection is a duplication of the main protection scheme. Figure 26 below shows the typical connection of a HV Bus protection system.

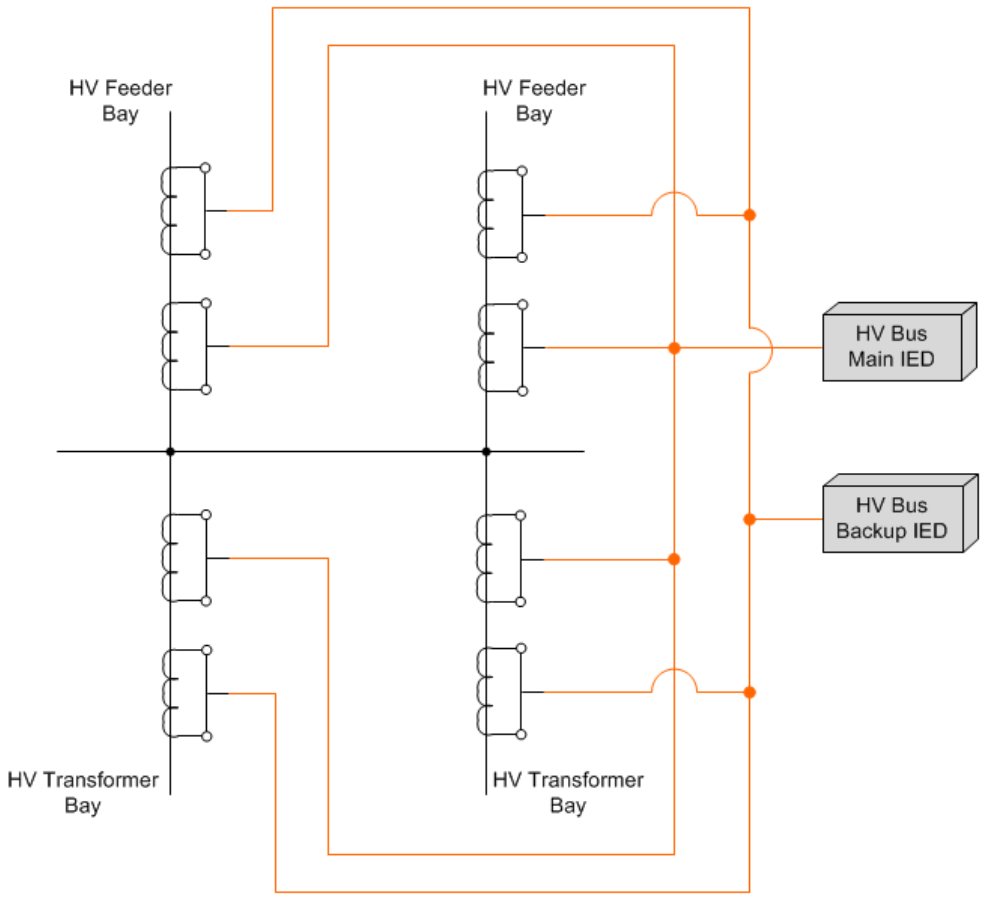

Figure 26 - Conventional HV Bus secondary system's protection connection diagram

The HV secondary network architecture consists of two HV feeder bays and one HV bus protection systems. Performing an availability block analysis similar to that permed for the LV secondary network architecture returns an availability of eight 9's.

3.3.1.4 Complete System Availability

The complete substations secondary network architecture is a combination of all three components; LV, Transformer and HV protection. Each of these three networks are independent of one another. Therefore, the reduction of these three network's availability to one single availability figure would be calculated as if they are in series.

The availability of the complete substation secondary network architecture is seven 9's. The high value for the network's availability is due to the level of redundancy that has been incorporated into the complete network.

3.3.2 Process Bus Substation Secondary System Architecture

3.3.2.1 General Characteristics

The process bus secondary system has increased the flexibility with the way in which the protection relays receive the measured value. Section 2.2.1 defines the introduction of the merging unit; this device is what allows for the flexibility. The conventional system required that the protection relay be connected directly to the instrument transformer, in a process bus system the relay subscribes to a sampled value data stream on a communication network. This means that the measured value from a single merging unit can be used in multiple protection relays.

Figure 27 below shows the location of the merging units in relation to the primary system's single line diagram. Each bay typically consists of two merging units, main and backup. This has replaced the need for multiple CT cores. A single bay in the conventional system would have four CT cores with two lots of main and backup for two different types of protection i.e. HV feeder and HV bus protection.

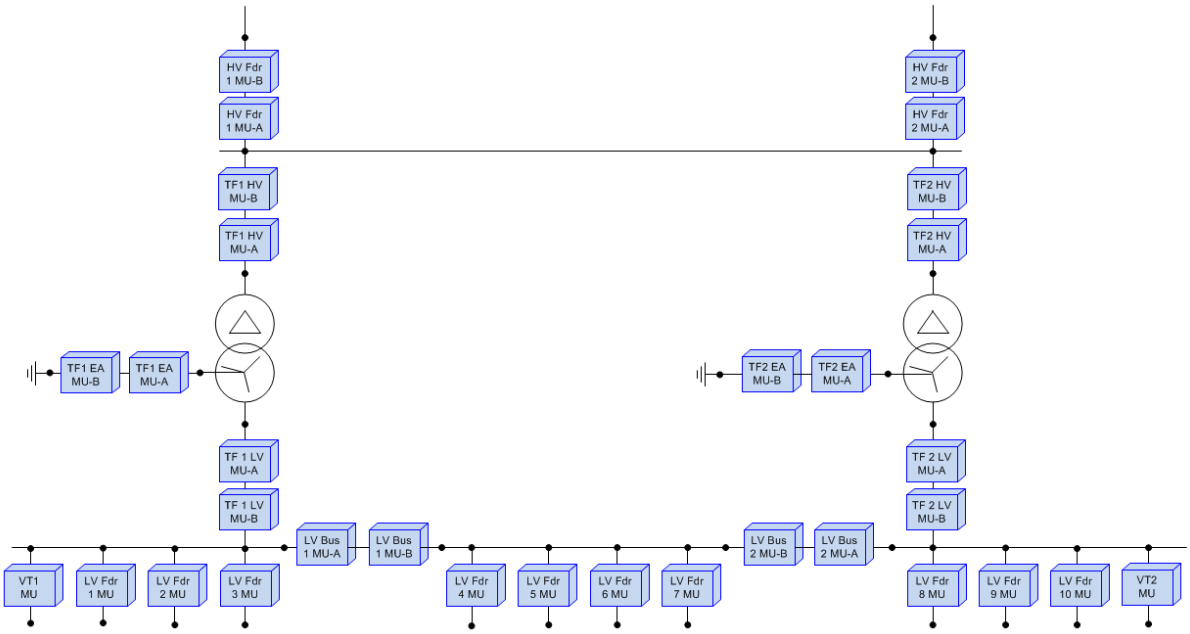

Figure 27 – Placement of Merging Units within the Ultimate Substation Layout

The protection relay is critical to the operation of the secondary system. The assessment of the LV feeder bay determined that the system's availability does not require the duplication of any IEDs to equal or exceed the conventional system. This has meant the process bus secondary system will consist of the same protection relays as the conventional ultimate arrangement.

Figure 28 below defines the merging units that each protection relay needs to subscribe too. This dependency does not change with the development of different process bus architecture.

The process bus network's configuration requirements were discussed in section 3.2.1. The key requirements and limitations to note are:

- Merging units and protection IEDs will not be connected to the same ethernet switch
- All devices have redundant communication ports that are capable of IEC62439-3 compliant.
- Ethernet switches can be managed
- All data ports are 100Mb/s
- Merging Unit publishes 5Mb/s and can be defined by a VLAN
- Each port's bandwidth should not exceed approximately 50% utilisation

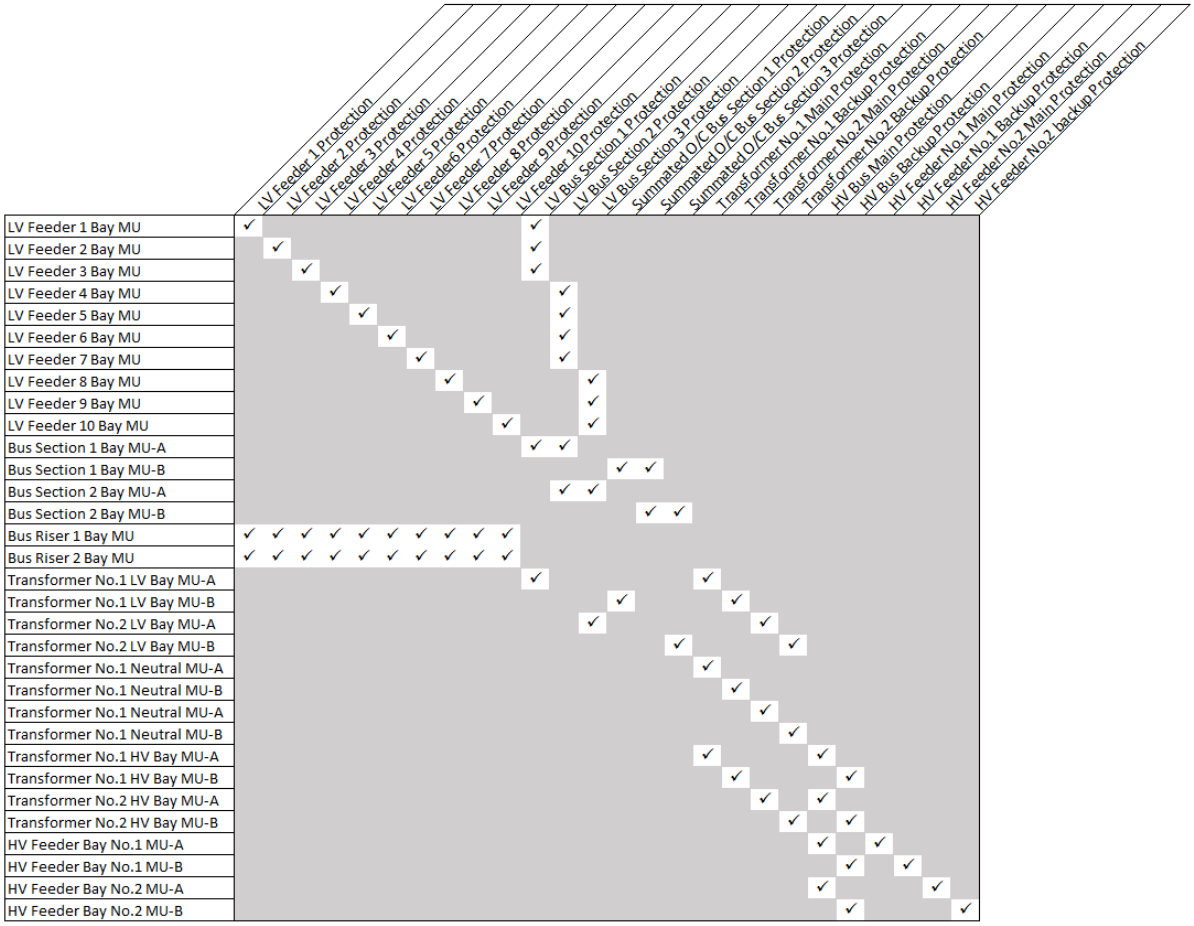

Figure 28 – Protection Relays dependency on a particular Merging Unit

The process bus network requires that there be duplicated communication paths. This requirement introduces redundancy that will result in the appropriate level of system availability. The two types of redundancy protocols discussed in the assessment of the LV feeder bay protection could be used. A further assessment of the two protocols has highlighted that the use of HSR is targeted at specialised cases. The HSR redundancy has a patented algorithm to deal with the duplicate packets of data.

Based on the above assessment this project will utilise the Parallel Redundancy Protocol for the implementation of a redundancy into the process bus architecture. The following architectures will only show one connection to improve the readability of the diagram.

3.3.2.2 Ultimate Process Bus Network Architecture 1

The concept for this architecture is to establish sections within the complete network. The sections were based on the ability to isolate a certain section of the primary system and still maintain limited operation of the substation. This resulted in five sections:

- LV Bus Section 1 – This section incorporates the merging units for LV feeder bays 1 – 3, transformer No.1 LV bay and transformer No.1 neutral bay
- LV Bus Section 2 – This section incorporates the merging units for LV feeder bays 4 – 7, bus section No.1 bay and bus section No.2 bay
- LV Bus Section 3 – This section incorporates the merging units for LV feeder bays 8 – 10, transformer No.2 LV bay and transformer No.2 neutral bay
- HV Section 1 – This section incorporates the merging units for the transformer No.1 HV bay and HV feeder No.1 bay
- HV Section 2 – This section incorporates the merging units for the transformer No.2 HV bay and HV feeder No.2 bay

Figure 29 below shows the interconnections between the sample value access ethernet switches and the protection IED access ethernet switches. This architecture abides by the limitations for the process bus network defined in section 3.3.2.1.

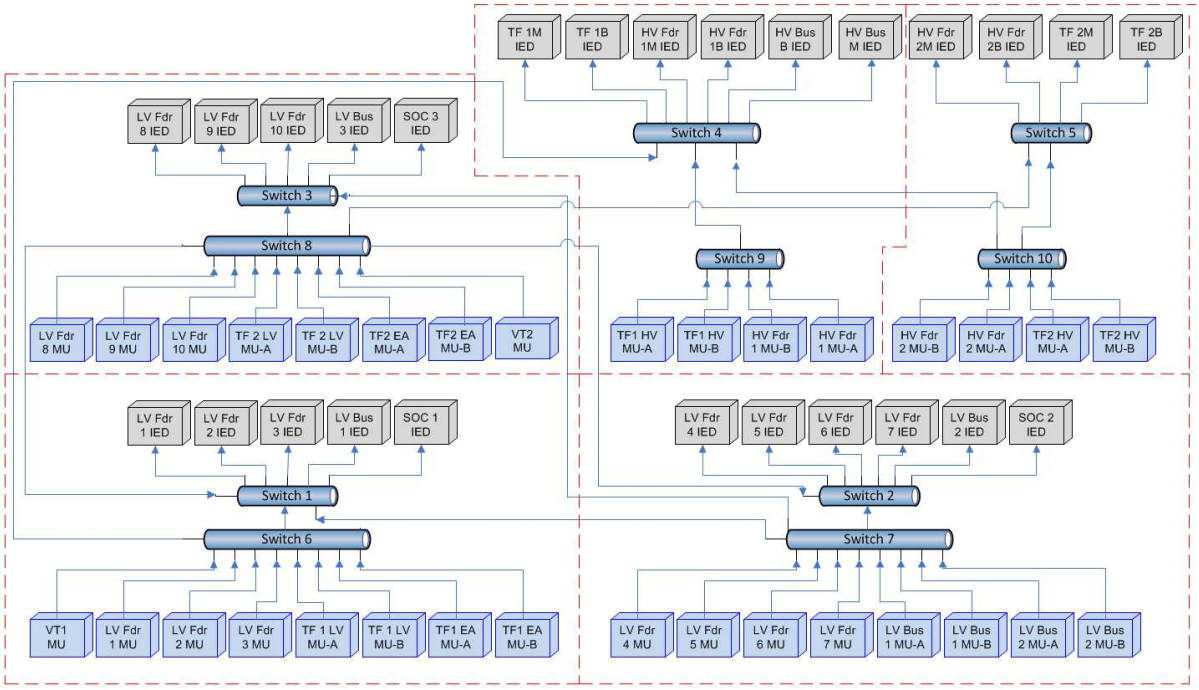

Figure 29 – Ultimate Process Bus Architecture based on Section of the Primary System

An availability assessment of a process bus architecture is more complicated than of the conventional architecture. The interconnection of multiple networks due to the sharing of the measured value means that you can no longer simply isolate different protection schemes to simplify the process.

To simplify this process the removal of the only measured value that can be used from two access switches is the VT measurement, which can come from either Switch 6 or Switch 8. The insignificant impact of doing this was discussed in section 0.

The availability assessment was then conducted so that the only possible parallel path was created by either a redundant merging unit or protection IED. This resulted in the process bus architecture shown in Figure 29 having an availability of seven 9's.

A practical assessment of this architecture has a number of possible issues. The main issue is that both the main and back up protections are dependent on the same communication path. The shared communication network incorporates redundancy that deals with the common mode of failure. The flexibility of architecture will be determined by the length of time that it is deemed acceptable to have one part of the network out of service for either routine maintenance or due to a fault.

3.3.2.3 Ultimate Process Bus Network Architecture 2

The previous process bus architecture had the possibility of issues with its operational flexibility. The second process bus architecture to be assessed is based on the existing protection principles that the main and backup protections are to be completely separate. This architecture is also based on the minimum substation configuration. The minimum substation configuration is to have a single incoming HV feeder, one Power transformer and one LV bus section.

Figure 30 below shows the connection of the process bus architecture based on this concept. Similar to the first process bus architecture, this architecture can be broken into four sections. These sections are:

- Section 1 – This section consists of all the main IEDs and merging units for HV feeder 1, transformer No.1 and the LV section 1.
- Section 2 – This section consists of all the main IEDs and merging units associate with the LV bus section 2.
- Section 3 - This section consists of all the main IEDs and merging units for HV feeder 2, transformer No.1 and the LV section 2.
- Section 4 – This section consists of all the backup IEDs and merging units for the complete architecture.

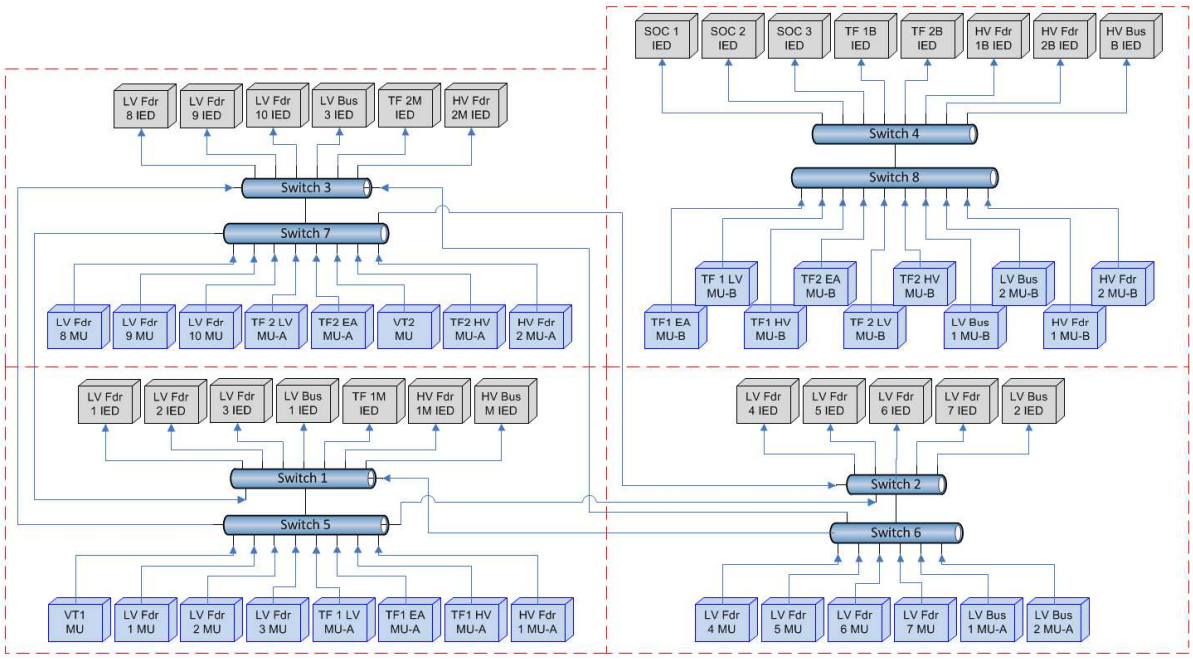

Figure 30 - Ultimate Process Bus Architecture based on Segregating Main and Backup Protection

The same approach for assessing the availability as used in section 0 can be applied to this architecture. This has resulted in the architecture shown in Figure 30 having an availability of seven 9's.

The practical assessment for this architecture highlights a number of good aspects. The most important being the clear separation of the main and backup systems. This allows for the same flexibility when performing maintenance or dealing with unexpected failures as could be done with the existing system.

3.4 Summary

The case study of the LV feeder bay confirmed that the change in the network architecture would have an impact on the system's availability. The reduction in the system's availability was due to the communication path. The introduction of redundant IEDs although had a positive impact on the system's availability it was not able to return the availability to the required level. However, by duplicating the communication path and maintaining the base number of IEDs, the system's availability was able to exceed the required availability.

The comparison between the two redundancy protocols PRP and HSR returned no significant difference in the availability benefit of either protocol. The PRP redundancy protocol that is used to establish a star type topology was chosen as the preferred solution. This allows for greater flexibility and does not restrict the operation of the system when routine maintenance is required on a merging unit or protection relay.

The assessment of the ultimate architecture based on the recently constructed Ergon Energy Oonoonba Substation, identified that the network responsible for the transportation of the measured value had a very high availability of seven 9's. This assessment formed the base to compare the ultimate process bus architectures that could be implemented. The two architectures that were developed both had the same number of 9's as the conventional network.

The two ultimate process bus architectures meet the minimum requirement, which was to have an availability equal to or greater than the convention network. It was also identified that there was operational flexibility issues with the first network. Having both the main and backup dependant on the same communication paths meant that if there is an abnormality on the network then there would be a reduction to the availability of both main and back up protection. With the redundancy incorporated into the communication network it is possible that this architecture can still comply with the "no single mode of failure" requirement.

The second ultimate process bus architecture not only allowed for the operational flexibility but also allowed for scalability. Scalability is an important aspect of the process bus architecture. This allows for a standard approach when building different types of substations. An example would be a single transformer substation that only has one HV and one LV bus section. The network architecture for this type of substation would only require Sections 1 & 4 from section 3.3.2.3.

Chapter 4

Technical Specification of the Sampled Value Methodology

4.1 Overview

The methodology description in section 1.5.2 was at a high-level to describe how the impact of sampled values will be assessed. There were five tests listed that would allow data to be obtained from all the devices to complete an assessment of the overall affect. The only technical requirement that was mentioned was the type of inputs that the test devices would be subjected too during each test.

The technical specification of these test signals and the test equipment that is used to produce them, is critical to understand how the test is performed. The time synchronisation of all the devices with in the system being tested is critical to establishing a time line for each test result. These technical requirements will be covered in this chapter with its technical requirements.

The five tests required a number of software tools to be developed. The software tools were used to create test signals and change data into useful information. The development of these tools utilised both MATLAB® and Microsoft Excel programs. The use of Microsoft Excel to develop engineering tools has become a common practice within the industry due to its flexibility and availability for general users.

4.2 Test apparatus

4.2.1 General Characteristics

Two types of test equipment were used as part of this project and were responsible for producing the test signal (single-phase current) to be put into the test circuit to observe how the system responds. The test signals needed to be in two formats, analogue for an input to the conventional relay and merging unit and digital for use in the 9-2LE compliant protection relay.

The manufacturer and model type of the two test devices used were listed in the test equipment in section 1.5.2. Figure 31 below shows the user interface of Doble F6150. The Doble test device was only used when the test required an analogue signal. To control the test signal output of this device required Protection Suite software to be installed on a personal computer. A more detailed look at this interface will be discussed in the sections detailing the test signal requirements.

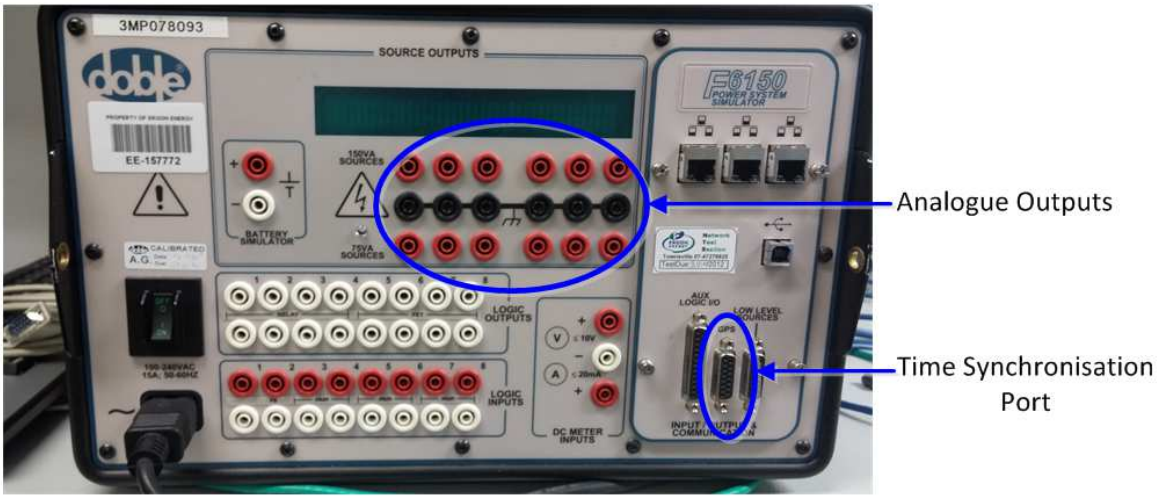

Figure 31 – Doble F6150 User Interface Panel Layout

The Omicron CMC850 test device is specifically designed to test only IEC61850 equipment. It has the ability to broadcast three sampled value streams onto a process bus network. The output port for this device as shown in Figure 32 is via an RJ45 copper ethernet port.

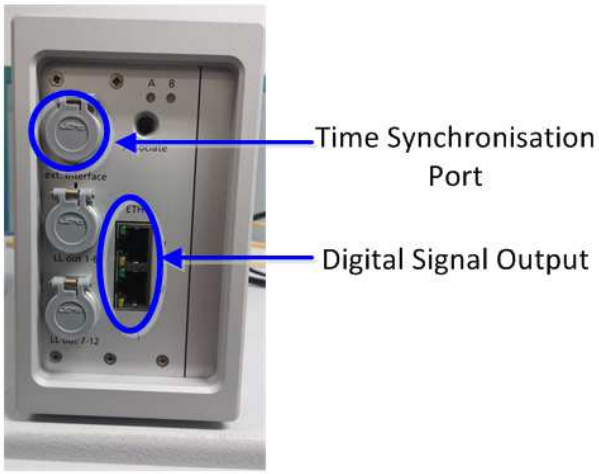

Figure 32 – Omicron CMC850 User Interface Panel Layout

The protection relay's communication port used to connect to the process bus are ST type Optic fibre cable connection. To enable the protection relay to subscribe to the Sampled Value stream generated by the Omicron CMC850 meant that an ethernet switch consisting of a mixture of copper and fibre communication ports was needed to establish an interface between the two devices.

4.2.2 Test Signal

4.2.2.1 Unsaturated Test Signal

The unsaturated test signal has been selected to determine the operation of the system under normal conditions. The magnitude of this waveform (10Arms) has been selected so that the test signal is within the peak-to-peak range of all the test devices. Figure 33 below shows the configuration of a "State Simulation" in Protection Suite to control the Doble F6150 to produce the appropriate test signal.

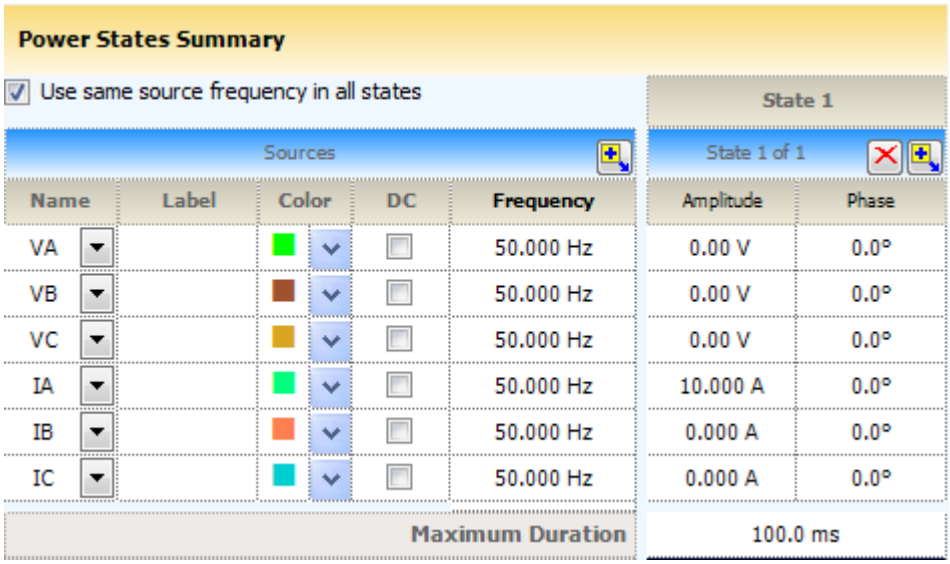

Figure 33 – State Simulation settings for an unsaturated test signal

The initiation of this state simulation is the same for all test signals. The use of the GO AT function allows the test signal to have a set start time, relative to UTC. This start time for each test was always the start of a new minute. By using this functionality, a test could be given a specific start to the test time line. The test signal is shown in Figure 34 with particular note of the start time. The Omicron CMC850 test software has a similar function for starting a test at a known time.

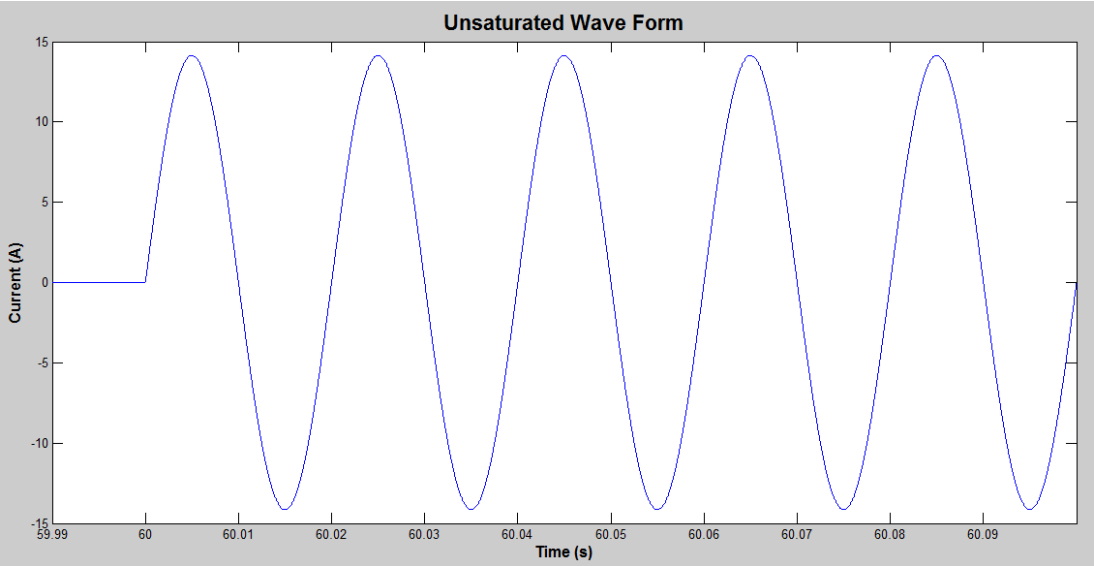

Figure 34 – Unsaturated Test Signal

4.2.2.2 Saturated Test Signal

The saturated test signal is used to replicate the secondary system during a fault on the primary system and observe how each component responds. During a fault condition on the primary system, the primary system current is only limited by the impedance between the source and the fault.

The fault current varies from site to site and for this reason the analysis will use the rated fault current for the primary equipment, which is 25kA for both the high and low voltage plant. The primary system's transient component to a fault current due to the inductive and resistive components of the primary system between the source and fault location has a significant impact on the fault current. The instantaneous current is shown in equation (4-1 has the transient component due to inductive and resistance ratio (X/R).

$$i_{primary} = \sqrt{2} I_{fault} \times [e^{-\frac{T}{\tau}} - \cos(\omega T + \varphi)] \qquad (4\text{-}1)$$

Where,

$I_{primary}$ = Instantaneous value for the primary current (A)

I_{fault} = Primary side rated maximum fault current (A)

T = Time (s)

τ = Primary system time constant (X/R)

ω = Angular velocity (rad/s)

φ = phase shift angle (radians)

The instantaneous value for the primary current has to be transformed to a level appropriate for use in a sensitive piece of equipment. The detailed characteristics of the current transformer used to perform this task will be discussed later in the dissertation. However, the key factor to understand here is that depending on these characteristics the transformation of the primary current can be distorted on the secondary side of the current transformer. The most common distortion is referred to as saturation. For the purpose of this section, the saturated signal has been generated using a MATLAB® script.

Both test devices have the ability to replay either recorded events or computer-generated waveforms to test a protection relay. The recorded or generated waveform data structure has been standardised by the IEEE. *C37.111-1999 - IEEE Standard Common Format for Transient Data Exchange (COMTRADE) for Power Systems* is a standard that defines the data structure of the file used in the test device. The limitation of this file structure is that the data within the files cannot be interpreted easily by a user.

Simulation of specific conditions is common when testing relays. These system conditions are typically created using software to create the transient data, this allows a way that the data can be easily understood. As previously mentioned the saturated wave used for this project is generated by MATLAB® and exported as a Microsoft Excel file. This data is then manipulated by a software tool, used in the protection group of Ergon Energy, to create the .CFG and .DAT files.

Protection suite and Test universe both have an option to simulate using a COMTRADE file. The secondary current as shown in Figure 35 has a peak current of 120A. The Doble F6150 device has built in protection that prevents the test from starting if it detects a test signal that could cause damage. The test signal for this project is of a transient nature that has a high output but for a short period, this period is not long enough to cause damage. Therefore, to run the saturated wave test signal the source was changed to a transient source inside Protection Suite.

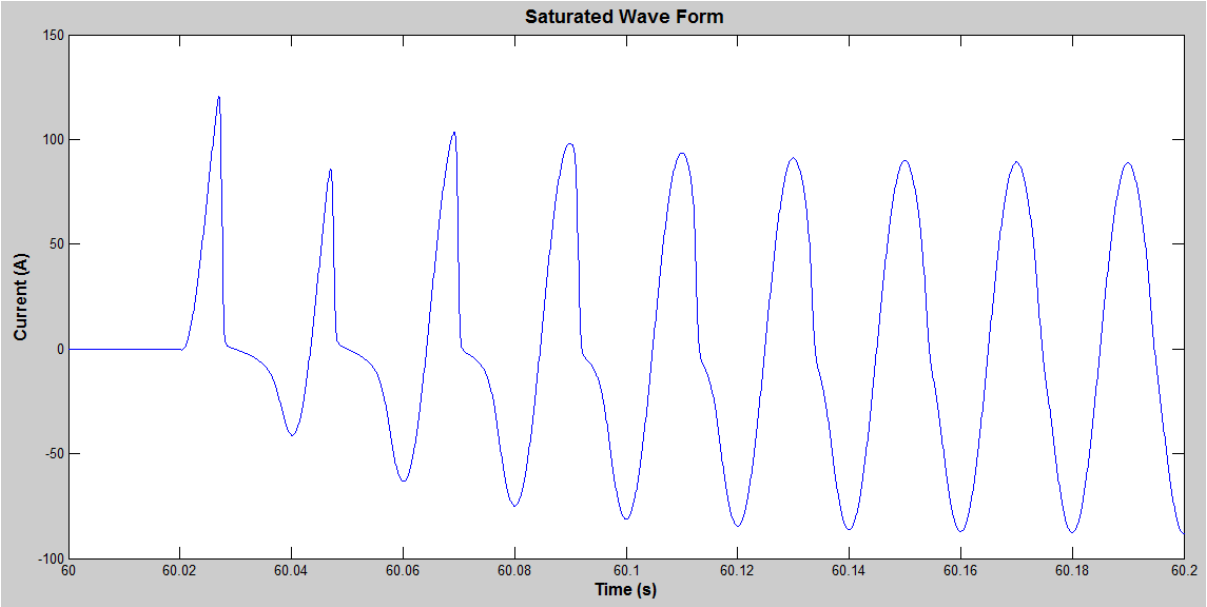

Figure 35 – Saturated Test Signal

4.2.2.3 DC Step Test Signal

The system that is being assessed is considered as a control system. Each component therefore has an impact on the output when subjected to a particular input. To understand this impact an analysis of the transient response of each device to a known input was conducted as part of the project.

Nise (2007) established a number of steps to assess a control system. This process is used to develop a mathematical model to understand what can be changed or additional components added so that the system operates within the specified way. The last step in the process is to subject the system to different types of inputs and then monitor and measure the transient response; this is the reason for the selection of a DC Step input.

The DC Step started at zero current and using the GO AT in the Doble and similar application in the Omicron software the current was stepped up to 10A and held at this level for 100ms. Figure 36 below shows the configuration of a State Simulation in Protection Suite to control the Doble F6150 to output the appropriate test signal.

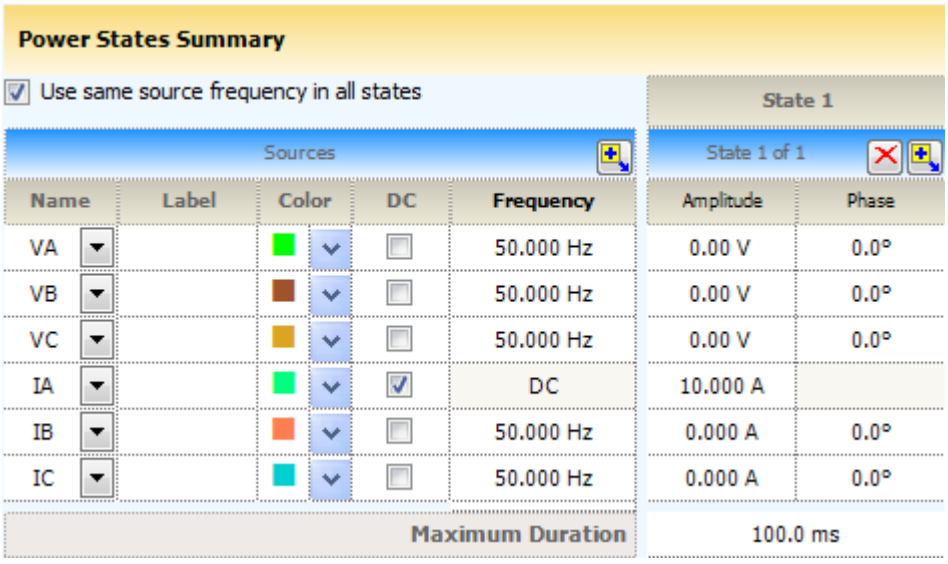

Figure 36 - State Simulation settings for a DC Step test signal

The above simulation results in a test signal as shown in Figure 37 below.

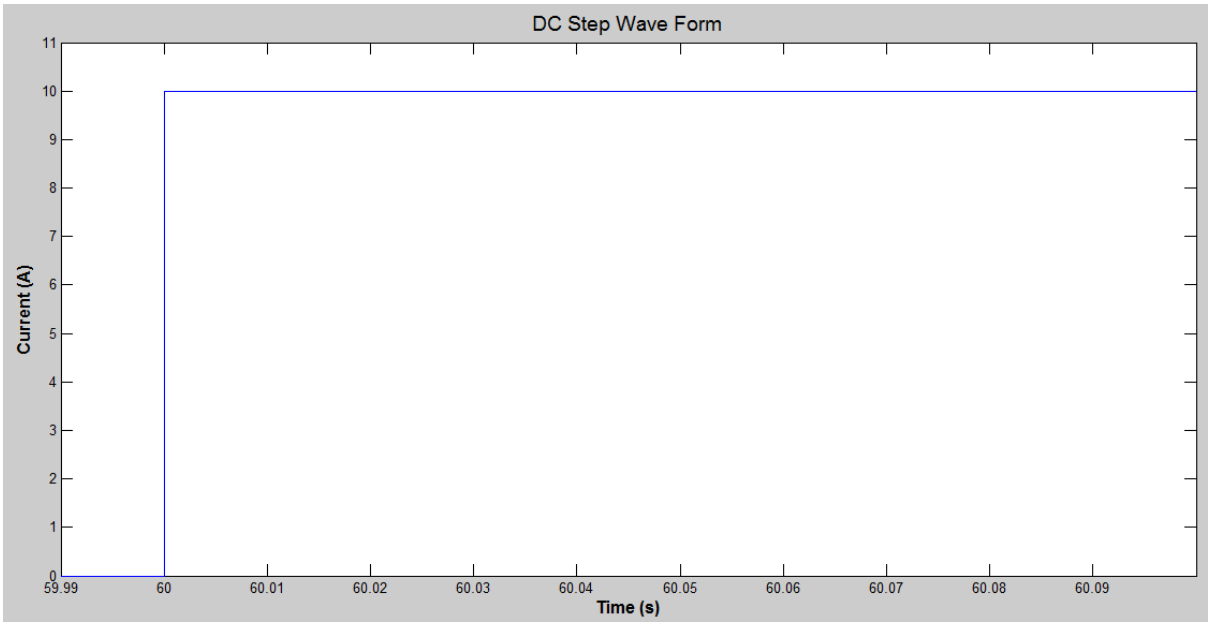

Figure 37 – Theoretical DC Step Test Signal

4.3 Merging Unit

The impact assessment of sampled values requires that data from the output of each device. The protection relays record events that are initiated by a trigger; in this case, the trigger was the instantaneous over current. These records contain the system conditions i.e. voltage and current values and any relay input conditions for a number of cycles pre and post the trigger. This data can be extracted from each protection relay via a communications port in an ASCII COMTRADE file format.

The merging unit does not have this recording functionality. The output of a merging unit is a multicast sample value stream of data, which means the data is capable of being captured by any device connected to the same network. A popular network analyser program Wireshark allows a user to monitor the information on a particular communication network, including the sampled value protocol.

Brunner,et al. (2004) and *International Electrotechnical Commission* (2011) establish that for a protection application the merging unit samples the analogue system at 80 samples/cycle. This sample rate means that every second there has been 4000 samples broadcasted onto the network. Each one of those samples has the data structure as shown in Figure 38 below.

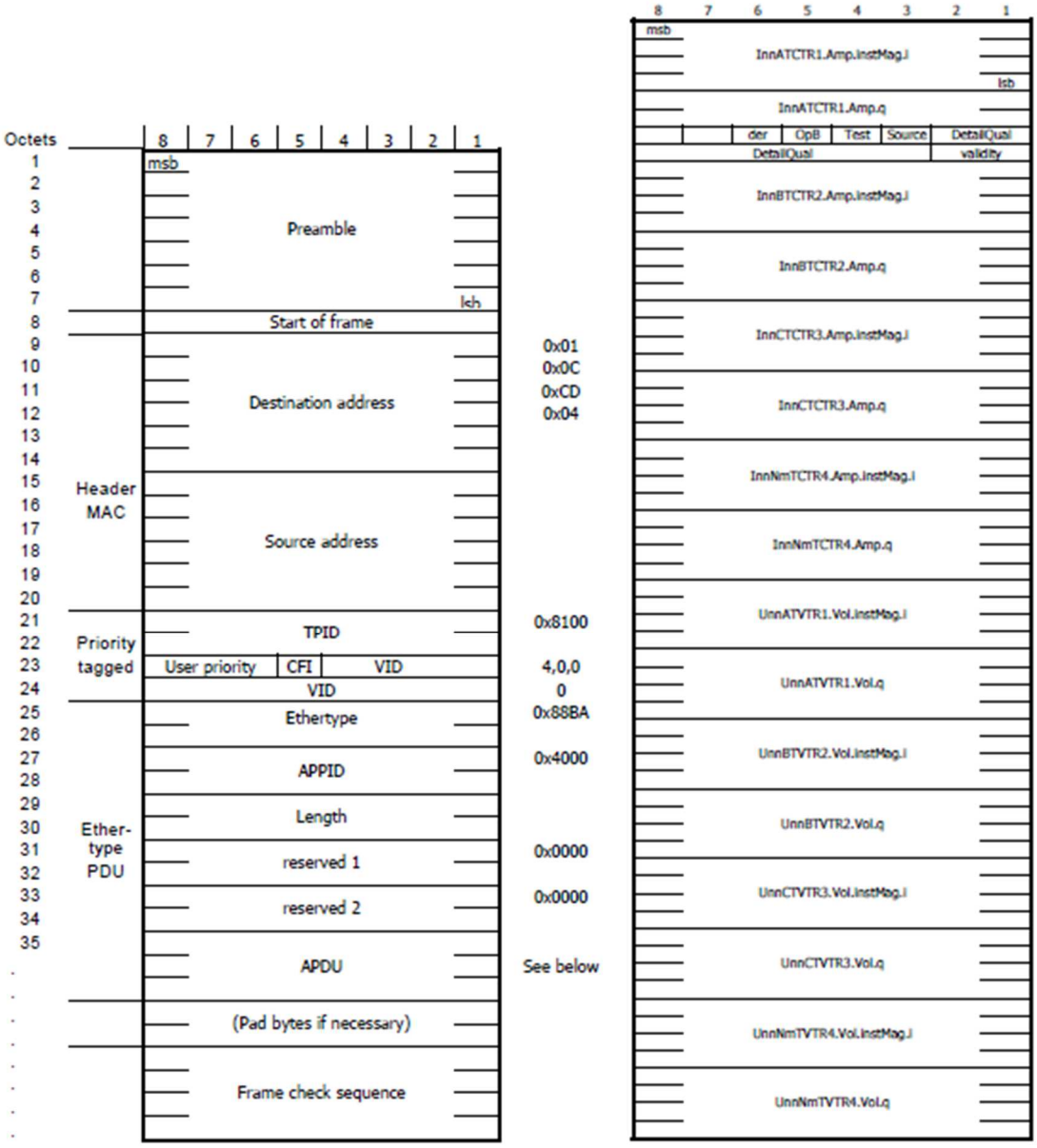

Figure 38 – Content of a Sampled Value messages Ethernet frame and Data set

Wireshark has built in intelligence to identify the Ether type of each packet on the network. The sampled value packet has an Ether type of “88BA”. It is then possible to set up filters in Wireshark so that it only captures these particular types of packets. Figure 39 below shows a capture with this filter on and an example of the information in one sampled value packet.

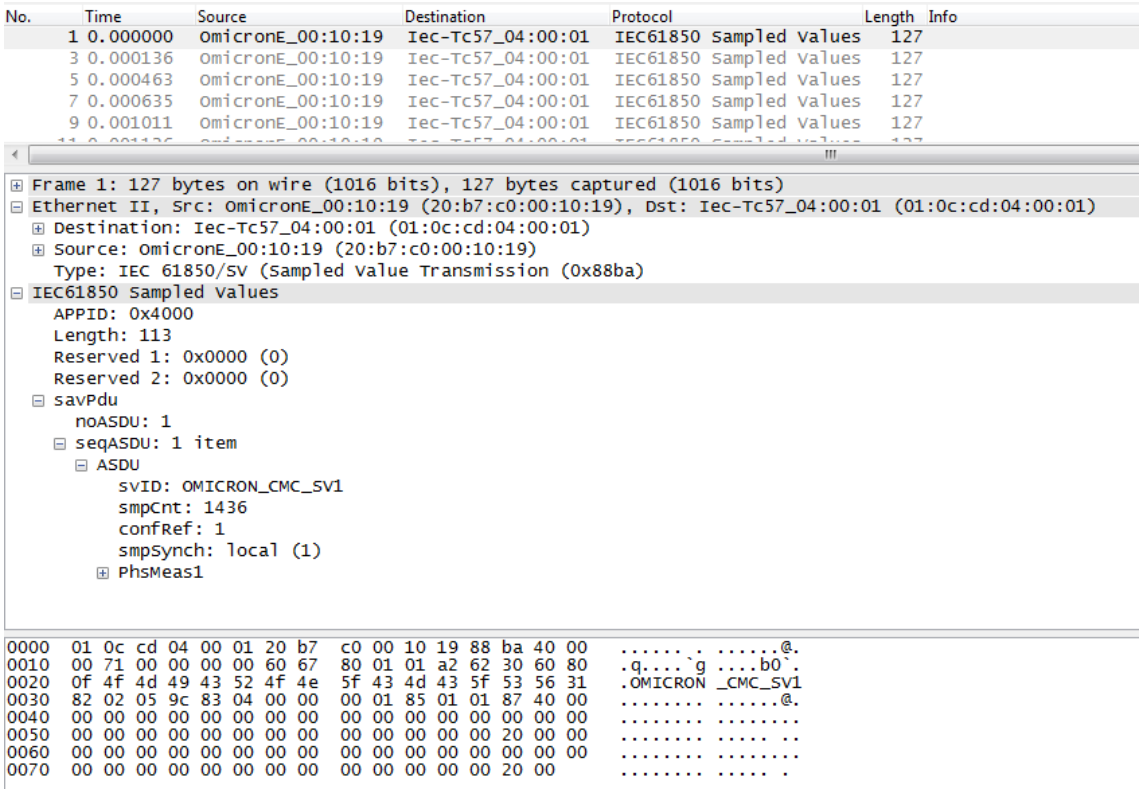

Figure 39 – Wireshark Capture of a Process Bus Network

Wireshark presents this information in a way that the information within a packet can be easily read. For example, it is clear from sampled value packet shown in Figure 39 that the sampled value ID is “OMICRON_CMC_SV1”; a protection relay will need to subscribe to this sampled value ID to enable it to receive these sampled value packets. However, the output of Wireshark to allow further analysis is in the form of a K12 text file. Each packet of information adds a single line of information that consists of the Hexadecimal information shown in the bottom of Figure 39 to the K12 text file.

The information that needs to be recorded for the assessment of the impact of sampled values is the following:

- SVID – Sampled Value ID so that if there is more than one sampled value stream on they can be isolated
- smpCnt – Sample Count is used to establish when a particular sample was taken
- PhysMeas1 – This will consist of eight measurements, four currents and four voltages.

A typical data capture for a single test would have up to thirty to forty thousand sampled value packets. Using Microsoft Excel a software tool was developed to convert this data into useful information. The program flow chart that the Visual Basic for Applications (VBA) code is based on can be seen in Figure 40 below.

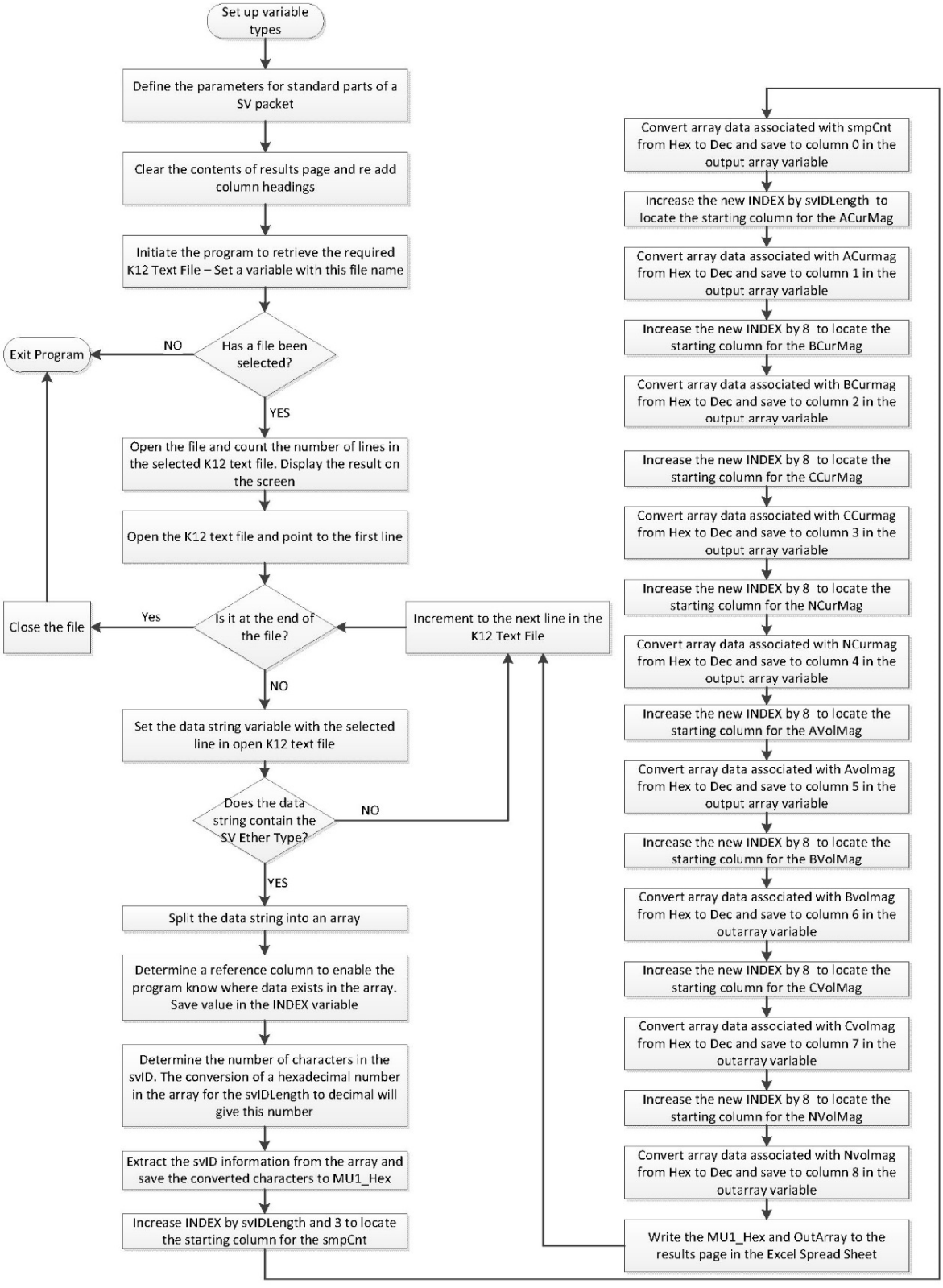

Figure 40 – Program flow diagram for sampled value data conversion

4.4 Time Synchronisation

4.4.1 Signals

Time synchronisation can be done by a number of different types of signals. The signals used to synchronise the devices within the tests conducted as part of this project can be categorised into two types, IRIG-B and one pulse per second (1PPS).

These signals were produced by an Alstom MiCOM P594 device. This device needed to be synchronised with a GPS signal utilising a minimum of four satellites before it could provide the time sync signals for the tests. The interface for the distribution of these devices were via a ST fibre optic communication port for the 1PPS and either a BNC coaxial connector or a RS-422 connector for the IRIG-B signal. These ports can be seen in Figure 41 below.

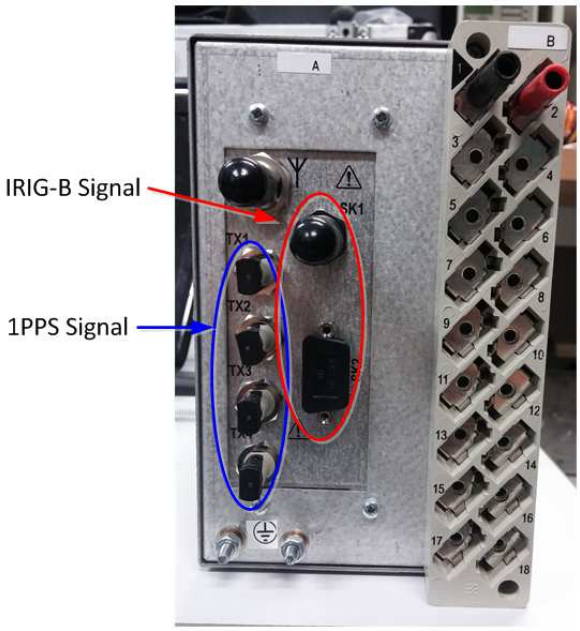

Figure 41 – Alstom MiCOM P594 Interface panel for time Synchronisation signal outputs

The standard that defines the technical specification for IRIG-B is *200-04 IRIG Serial Time Code Formats. Timing Committee Telecommunications and Timing Group Range Commanders Council (2012)* has defined that the IRIG-B can be sent in 3 ways, pulse width code (Unmodulated), Sine Wave (Amplitude Modulated) or Manchester modulated. If a modulation is used, than the carrier frequency as defined in the standard is to be a 1kHz frequency, this is shown in Figure 42.

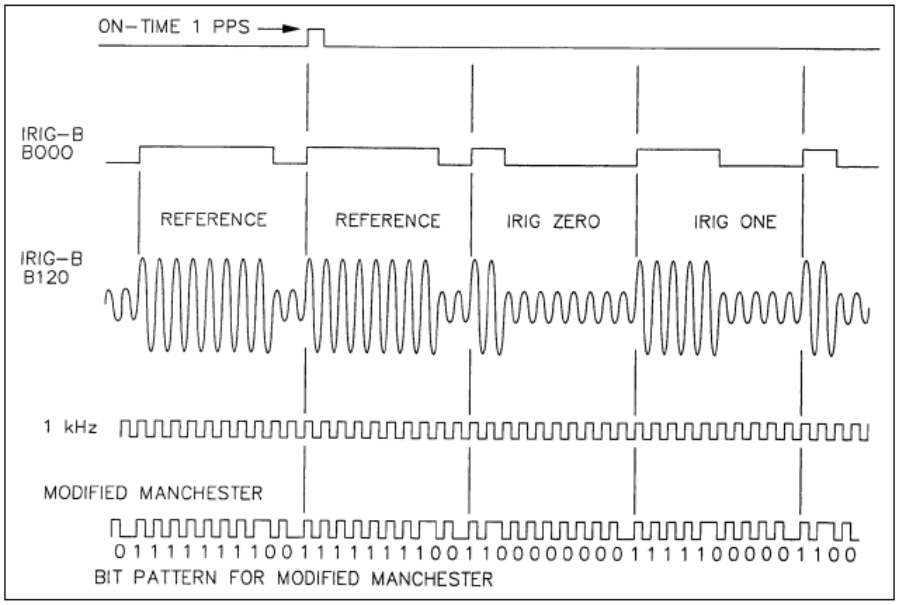

Figure 42 – IRIG-B signal modulations (Timing Committee Telecommunications and Timing Group Range Commanders Council, 2012)

The Alstom MiCOM P594 used to produce the IRIG-B can be configured to produce two of the three ways shown above, Unmodulated and Amplitude Modulated. The BNC port can be configured to output either of the two formats and the RS-422 port can only be used for an unmodulated signal.

The 1PPS time synchronisation signal is also shown Figure 42. The two reference markers can be futher defined with the first being the “Position Indentifer” and the second being the “Reference” bit. The rise of the 1PPS signal is to occur at the same time as the rise of the “Reference” bit. To confirm that the Alstom MiCOM P546 conforms with the standard I converted the 1PPS into an electrical signal using a fibre optic reciever and reverse engineering an output. The output of the receiver and the output of the BNC from the Alstom MiCOM P594 were used to confirm synchronisation as shown in Figure 43.

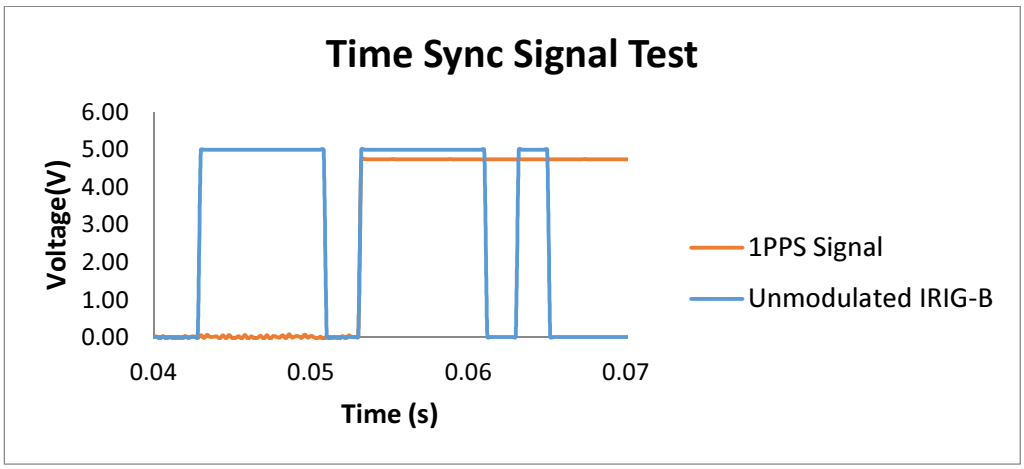

Figure 43 – Conformation Test result for the MiCOM P546 IED

4.4.2 Test Equipment

To establish an accurate time line for each test requires that the tests start precisely at a known time. Section 4.2.2 that defined the test signals introduced the built in functionality of the Doble and Omicron test equipment that allowed the test to start at a known time. To enable this functionality required that the test equipment be in a synchronised state.

4.4.2.1 Doble F6150

The GO AT function previous described allows the user to set a time for when the test will start. A GPS signal is used to time synchronise this test device. The input for the GPS signal is via a 15-pin D-type female connector on the user interface panel as shown in Figure 31.

The GO AT time selected for each test was the start of a new minute and requires sub millisecond accuracy to meet the minimum time stamping of the devices tested in the system. To confirm that the test signal occurs as specified in the test procedure, a test was conducted that observed only the output of the test equipment with a time reference.

The unmodulated IRIG-B signal from the BNC connector of the Alstom MiCOM P594 was put into one of the sampling ports of the oscilloscope, used to create a reference for time. The output of the Doble was put into another sampling port of the oscilloscope. A trigger was set in the oscilloscope to record when the channel with the Doble signal was above a predefined level. The result of the test can be seen in Figure 44.

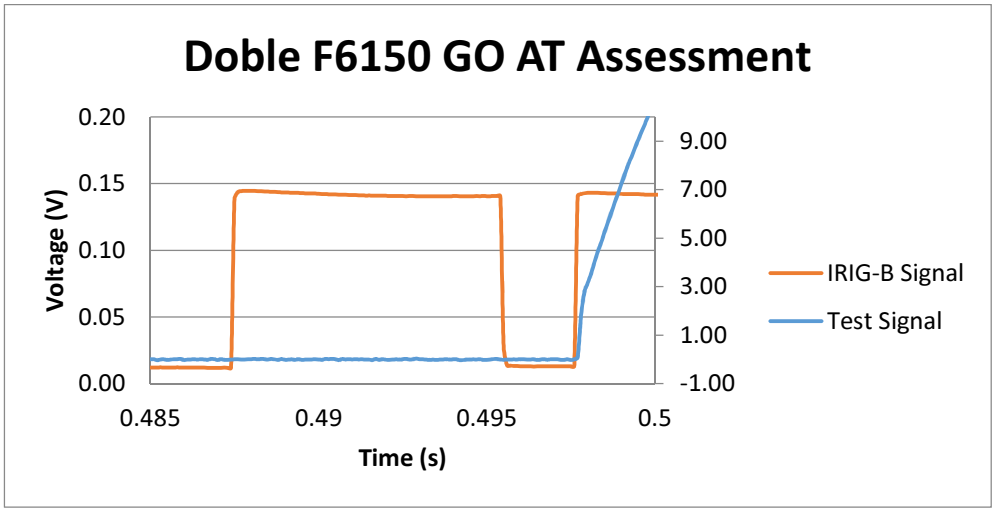

Figure 44 – Doble F6150 Test Signal's start time confirmation test result

The result shown in Figure 44 confirms that the test signal starts with the rising edge of the reference bit as described in section 4.4.1. The test equipment meet the required accuracy for the start time to develop an accurate time line.

4.4.2.2 Omicron CMC850

Similar to the Doble F6150, Omicron CMC850 has the ability to allow a test to be started at a predetermined time. The output of this device is a generated stream of sampled values. The Omicron is responsible for time stamping the sampled value messages that it will publish onto the network.

To enable the Omicron to start a test at a known time also required being in a synchronised state. The source used for this project was an unmodulated IRIG-B signal generated by the Alstom MiCOM P594 using the BNC connection type to synchronise the Omicron CMC850.

A test was conducted that observed the output of the Omicron with reference to the start time of the test signal. Data was captured on the process bus network that the Omicron CMC850 was publishing sampled values onto when a test was conducted. The sample count of each sampled value packet was used to determine the timing of the test signal. Figure 45 below shows the result of this test.

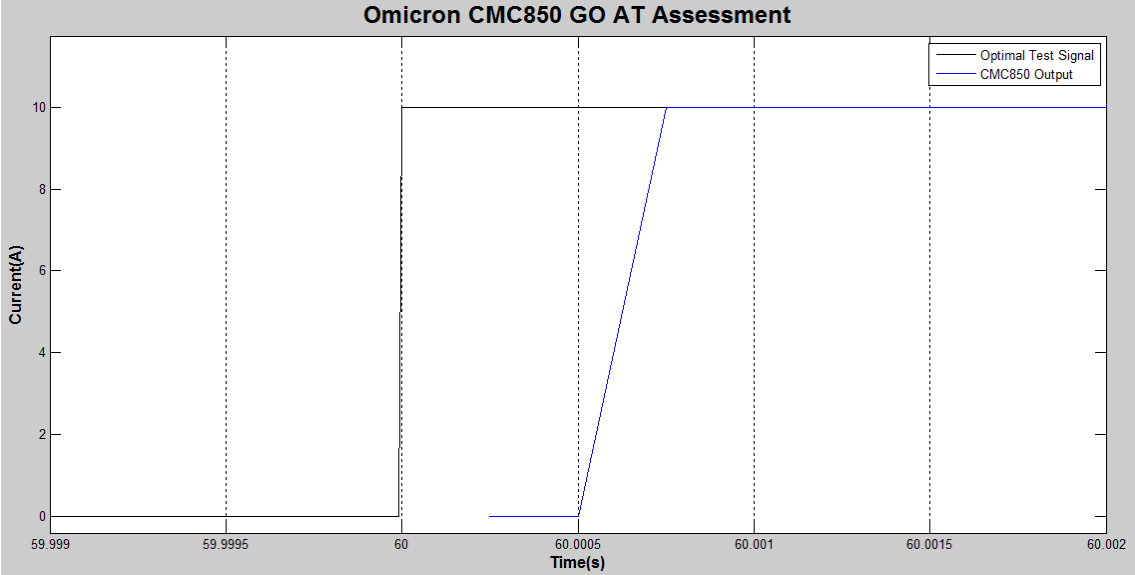

Figure 45 – Omicron CMC850 Test Signal's start time confirmation test result

The Omicron has an inaccuracy with the GO AT functionality as per the result shown in Figure 45. The inaccuracy of this result is that the start time has been delayed by 500µs, which equates to two samples. This error can be extend to when the test signal reaches the predefined value; this means that the test signal does not reach its required value until 750µs after it was initiated. This error has been factored into the assessment of the results for the process bus relay.

4.4.3 Tested Devices

4.4.3.1 Manufacturer “Y” Relay

The test data obtain from this device is an event file that consists of conditions when a triggered event occurred. The information that is of importance in the event file for this project is the current measurements and the time at which they occurred. The relay typical has the ability to have the time and date set by an operator through its user interface. This setting over time can slightly drift away from the actual time.

To ensure that the data within the event file can be compared against other devices output as well as the test signal it is critical that they all have the same time. Therefore, the drift that was mentioned and the human factor of the input could have the potential to introduce significant amount of error when needing sub millisecond accuracy.

The relay used in this project has the additional functionality that allowed for time synchronisation that was performed by an unmodulated IRIG-B signal. To check the accuracy of this time synchronisation three test were conducted for each test signal input. The results from these tests can be seen in Figure 46.

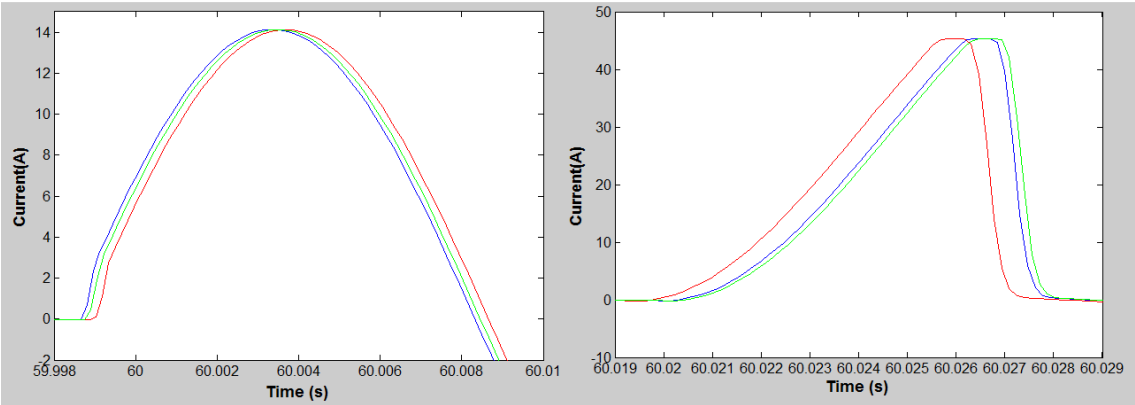

Figure 46 – Results of multiple test for Manufacturer “Y” relay showing time stamping comparison

The results shown in Figure 46 show that there are slight inaccuracies with the time synchronisation. The greatest difference measured between the three test results was 400µs. Manufacturer “Y” instructional manual for the IED defines the accuracy of the time synchronisation using the IRIG-B signal for the test conducted is ±5ms. Therefore, the result shown here is well with the predefined limits. This error needs to be accounted for when assessing the data from this manufacturer with other data from different devices.

4.4.3.2 Manufacturer "X" Conventional relay

The event data is recorded in the same way as the previous manufacturer's relay. It has the same time setting abilities and the same associated issues. Too accurately time synchronise manufacturer "X" relay requires an amplitude modulate IRIG-B signal. Three tests of each signal were also conducted on this relay with results shown in Figure 47 below.

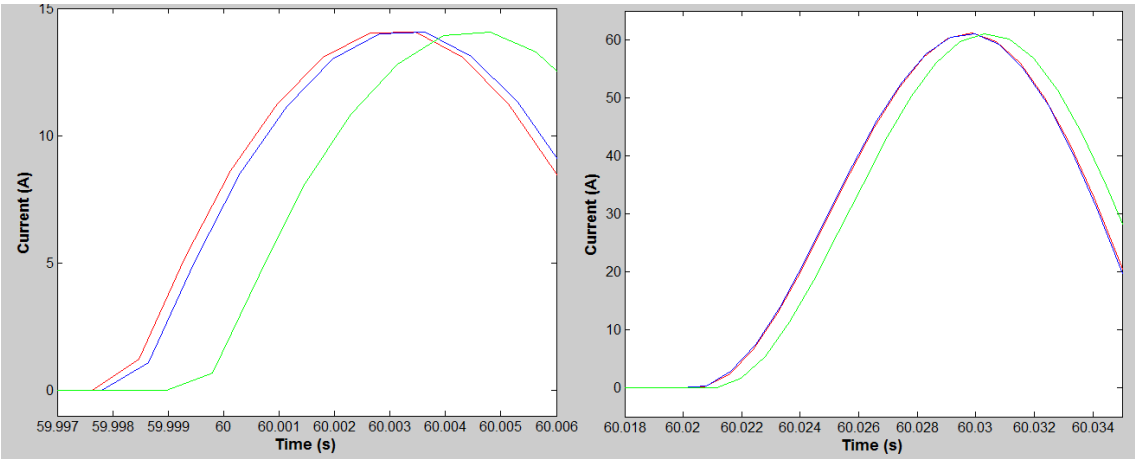

Figure 47 - Results of multiple test for Manufacturer "X" relay showing time stamping comparison

The results shown in Figure 47 show that there are inaccuracies with the way in which the Manufacturer "X" time stamps. The greatest difference between two results is 1.2ms. The technical manual for the Manufacturer "X" relay states that the accuracy for IRIG-B should be less than ±2ms. Therefore, the relay is operating with the manufacture's specifications. However, when comparing values this inaccuracy needed to be accounted for.

4.4.3.3 Manufacturer "Z" Process Bus Relay

The data extracted from the Manufacturer "Z" relay is conducted in the same way as a conventional relay. The event file from this relay is subjected to the same time synchronisation as both the conventional relays, which means the way its time is set can influence the accuracy of the time stamping. This relay manufacturer has used an amplitude modulated IRIG-B signal to synchronise the relay's time.

This device was also tested with the three test signals multiple times to observe any difference that could occur, which included the consistency of the time stamping. Figure 48 below shows the results obtained as part of the testing.

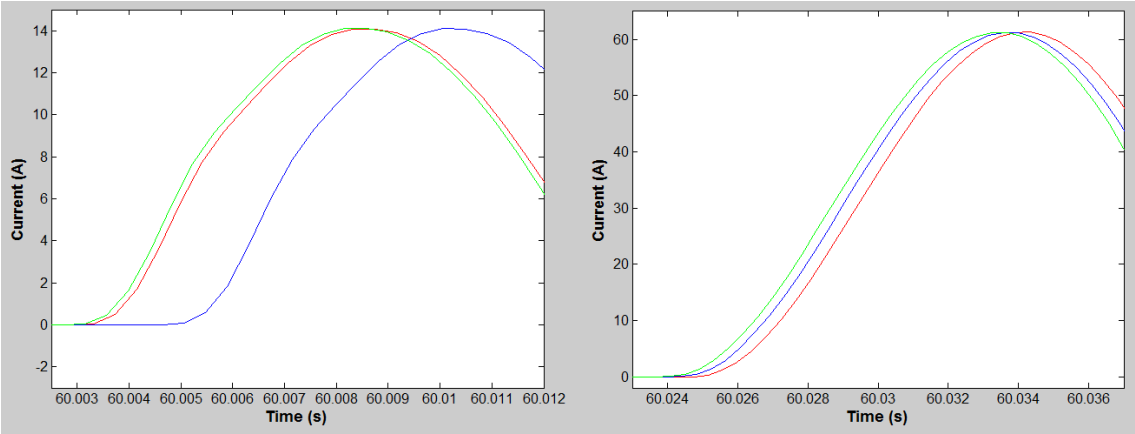

Figure 48 - Results of multiple test for Manufacturer "Z" relay showing time stamping comparison

The results obtained indicate that there is an inconsistency in the time stamping of the recorded data. The greatest difference between two results for the Manufacturer "Z" relay was 1.5ms. The difference recorded here conforms to the technical manual for the relay.

4.4.3.4 Manufacturer "Z" Analogue Merging Unit

The time synchronisation of the analogue merging unit is critical to the operation of the device when used in a protection scheme that utilises measurements from more than one independent merging unit i.e. differential protection. Each measurement in a typical protection system is taken every 250µs as explained in section 4.3, this means that that the time synchronisation requires microsecond accuracy.

The time synchronisation of the Manufacturer "Z" merging unit used in the testing for this project is done via a 1PPS signal from the Alstom MiCOM P594. Section 4.3 introduced the concept of the sample count for each sampled value message; the sample count goes from 0 to 3999. This information is used to convey the time that the sample was taken in reference to other sampling devices on the same system.

The 1PPS signal is used in the relay to align the sample with the sample count value of "0" to the start of every second. This knowledge allows the user to observe the output of the merging unit with reference to the test signal. Figure 49 below shows the test results for Manufacturer "Z" merging unit being subjected to the different test signals multiple times.

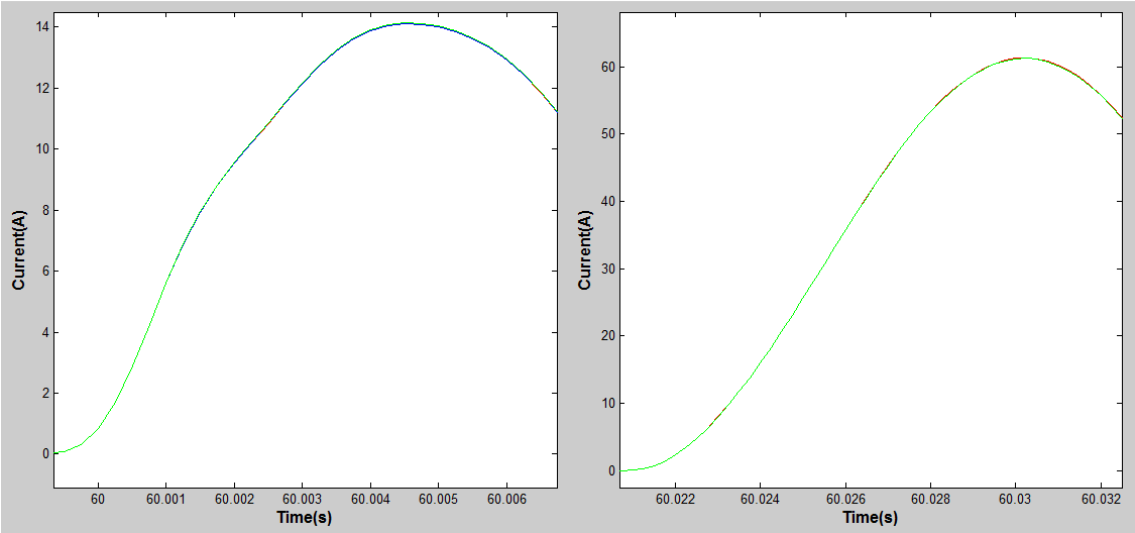

Figure 49 - Results of multiple test for manufacturer "Z" merging unit showing time stamping comparison

The results shown in Figure 49 confirm that the time synchronisation of the sampled values meet the required microsecond accuracy.

4.5 Summary

A number of key considerations were discussed in this chapter such as the way the testing and specific parameters will be conducted, new software tools and time synchronisation. The test signals, in particular the DC step test signal, are important to allow the appropriate results to be obtained to determine the impact on the system performance. The DC step test will allow the user to observe the transient response of the system due to a known change to the system input as per the standard procedure for analysing a control system.

The development of a tool that can handle a large amount of network data is critical to the final analysis of the merging unit. The structure of the program designed and the implementation into VBA allows for a text file of considerable size obtained using Wireshark to be converted in a timely manner.

Time synchronisation is critical to the development of an accurate time line for each test. The accuracy of each device being time synched has been analysed and the relative error identified. The two types of IRIG-B signals, Unmodulated and Amplitude Modulated, have differing accuracies as observed between Manufacturers "X" and "Y" relays test data. The results for Manufacturer "Z" merging unit has confirmed the required time stamping accuracy of such a device.

Chapter 5

Sampled Value Performance Characteristics

5.1 Overview

To allow integration of process bus devices into the secondary systems of Ergon Energy the performance needs to be assessed. The assessment undertaken was based on three criteria:

- Current Transformer performance
- Analogue to digital conversion
- Time Delays

The three criteria would require an assessment of the conventional system as well as the process bus system. The first criteria is assessed by manipulating the current transformer model to represent the change to the current transformer circuit. The output of this model will also be used to perform an assessment of the other two criteria for the current and future devices.

To obtain the appropriate data for the devices being tested to assess the performance of each device against two of the three criteria needed a number of test setups. The connection diagrams for the four tests listed in section 1.5.2 are located in Appendix F.

Chapter 4 defines a number of specifications and formats that are needed to assess the data obtained from the four test procedures. To enable ease of handling of the data obtained from all the tests, a MATLAB® script has been compiled to assist with the analysis. The main functions of the MATLAB® script are:

- Develop the test signals to be used for the analysis
- Import and convert the COMTRADE files of both of the conventional relays for different test signals
- Import and convert the COMTRADE files of the Process bus relay for the different network configurations and test signals
- Import the Excel files for the captured sampled values from the Merging Unit
- Determine the overshot and delay times of the tested devices
- Produce Plots for visual analysis

5.2 Current Transformer Performance

5.2.1 Current Transformer Theory

The existing current transformers and Ergon Energy period contract current transformers are constructed using independent secondary windings or cores. The number cores is dependent on the location of the current transformer within the power system and the need for back up protection.

A typical 66kV current transformer consists of four protection class cores and one metering class core. The technical constraint that exists to restrict the use of one protection core to be used for multiple protection schemes will be explained later.

The construction standard of a current transformer is defined in the IEC 61869-2 or the Australian standard 60044. These standards also defines the information that is to be recorded on the nameplate of the current transformer. The information given for a Px class current transformer should be:

- The rated turns ratio
- The rated knee point e.m.f. (E_k)
- The upper limit of exciting current (I_e) at the rated knee point e.m.f. and/or at the stated percentage thereof;
- The upper limit of secondary winding resistance (R_{ct})
- The dimensioning factor (K_x)
- The rated resistive burden (R_b)

The performance requirement of an instrument transformer is to replicate accurately the primary system conditions at a level that can be used by sensitive electronic equipment. The condition in section 4.2.2.2 is due to a current with a very high magnitude that has a decaying DC component. The performance of the instrument transformer during these conditions are determined by the saturation characteristics of the instrument transformer.

A saturated current transformer is that when it is in its saturated state the system acts like there is a short circuit across the current transformer's magnetising branch. The short-circuit means that the protection relay that is dependent on this signal will see the primary system as if there is reduced or no current flowing. This prevents the relay from accurately detecting the fault and denying it the opportunity to react and isolate the faulted network. Figure 50 below shows a general example of this occurrence.

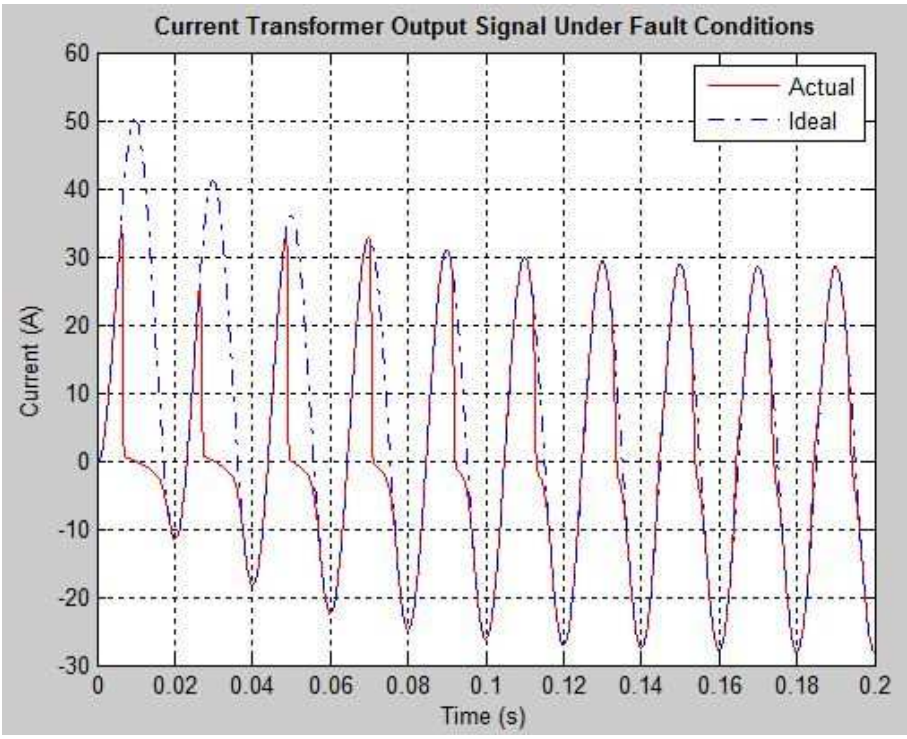

Figure 50 – Output of the Secondary current signal for the MATLAB® Model

Figure 50 shows the output of a current transformer when it is saturating in the positive half cycle. The flux within the core is proportional to the integral secondary voltage. The voltage known as the Knee point voltage of the current transformer is defined in the IEC 61869-2 as "r.m.s. value of the sinusoidal voltage at rated frequency applied to the secondary terminals of the transformer, all other terminals being open-circuited, which, when increased by 10 %, causes the r.m.s. value of the *exciting current to increase by 50 %"*. The type test results for a 66kV CT installed at the Oonoomba substation that was used for the availability assessment can be seen in Figure 51 below.

Present practice is to specify an over dimensioning factor when ordering a CT to match the requirement of the protection relay. This over dimensioning factor can be as high as 250 for the 66kV CTs as per a period contract specification. Equation (5-1) shows how the over dimensioning factor is used to determine if the system is going to apply. It should be noted that numerical relays now have the ability to deal with a certain level of saturation.

$$V_k > \frac{I_{fault}}{N} \times (R_{CT} + R_b) \times \left(1 + \frac{X}{R}\right) \qquad (5\text{-}1)$$

Where,

V_k = Rated Knee point voltage of the CT
I_{fault} = Primary side rated maximum fault current
N = CT ratio
R_{CT} = CT secondary winding resistance
R_b = Load burden
$\left(1 + \frac{X}{R}\right)$ = Over dimensioning factor

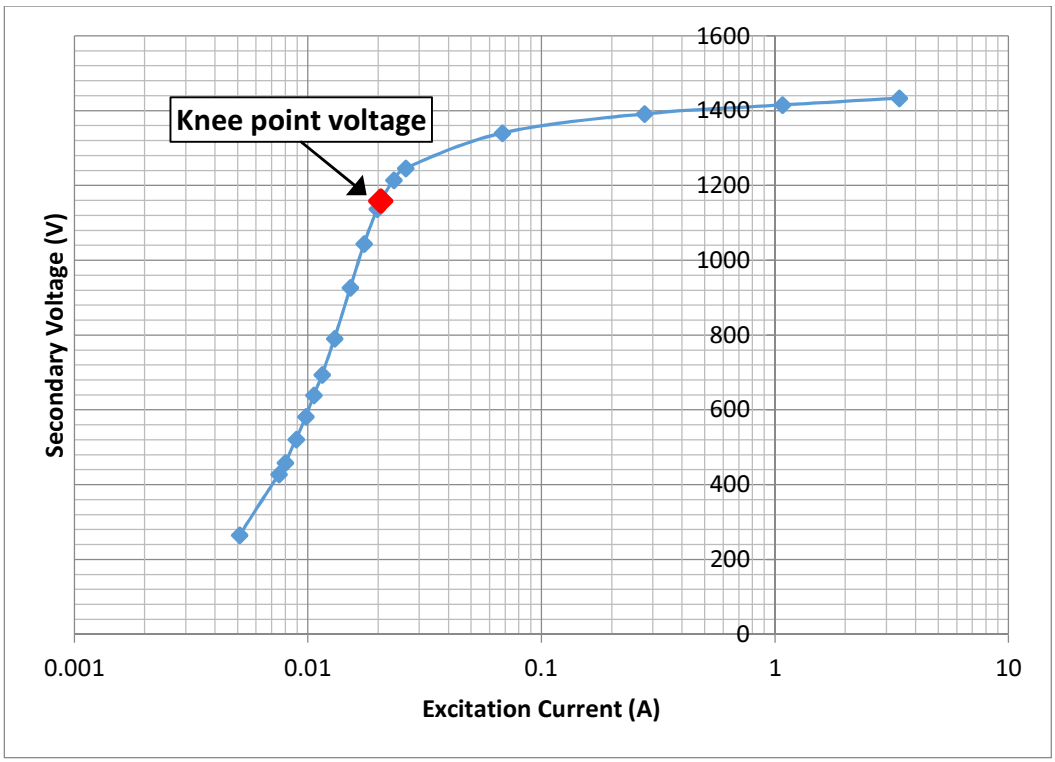

Figure 51 – Existing Ergon Energy 66kV 1200/1 Current Transformer Type Test Data

5.2.2 Current Transformer Model

As described above the performance of a current transformer during a network fault condition is critical to allowing the protection device to act accordingly, an assessment of the impact of the merging unit on this performance criteria needed to be done. To undertake this task a MATLAB® model has been developed to observe the change in the performance by adjusting the appropriate parameters.

The construction of the model meant that the information that is available for current transformers that are in-service could be used. This information is on the nameplate of the instrument transformer. Therefore, the model requires the following inputs:

- Knee Point Voltage (V)
- Accuracy Limit Factor
- Rated primary current (A)
- Rated secondary current (A)
- Secondary burden rating (VA)
- Percentage error when at the limits
- CT winding resistance at the given CT ratio (Ω)
- Secondary burden (Ω)

It should be noted that the above inputs are obtained from a P class CT rating nameplate. In the case of the current transformer with a PX class rating, then this can be converted to a P class by performing the following equations as derive by *P. Fonti (2000)*.

$$VA = \frac{1.6}{1.4}\left(\frac{V_s \times I_n}{ALF}\right) - R_{ct} \times I_n \quad (5\text{-}2)$$

And

$$V_k = \frac{1.6}{1.4} \times V_s \quad (5\text{-}3)$$

Where,

VA = Rated secondary Burden

V_s = the knee point voltage as recorded in the name plate of the CT

I_n = the rated secondary current

ALF = this has been assumed as 20 given this is the standard value for a P class CT

R_{ct} = CT winding resistance at the used CT ratio

V_k = the knee point voltage of a P class CT

The current transformer model that has been developed in MATLAB® to simulate the impact of the new technology on the performance of a current transformer can be seen in Appendix G.

5.2.3 Impact of the New Technology

The limitation of the existing system is determined by the secondary burden. The voltage across the secondary terminals that influences the saturation voltage is proportional to the secondary burden. This means that an increase in the secondary burden will increase the secondary voltage with respect to the same current. This is the reason why each core can only typically support one protection relay.

The introduction of the merging unit has had a positive theoretical effect on this component of the system's performance. The reason for this is that the merging unit is located in the near vicinity, typical in the marshalling cubical located on the piece of equipment. Therefore, the secondary burden has been reduced significantly. The true impact of the new devices with the reduction of the secondary burden can be seen in Figure 52 below.

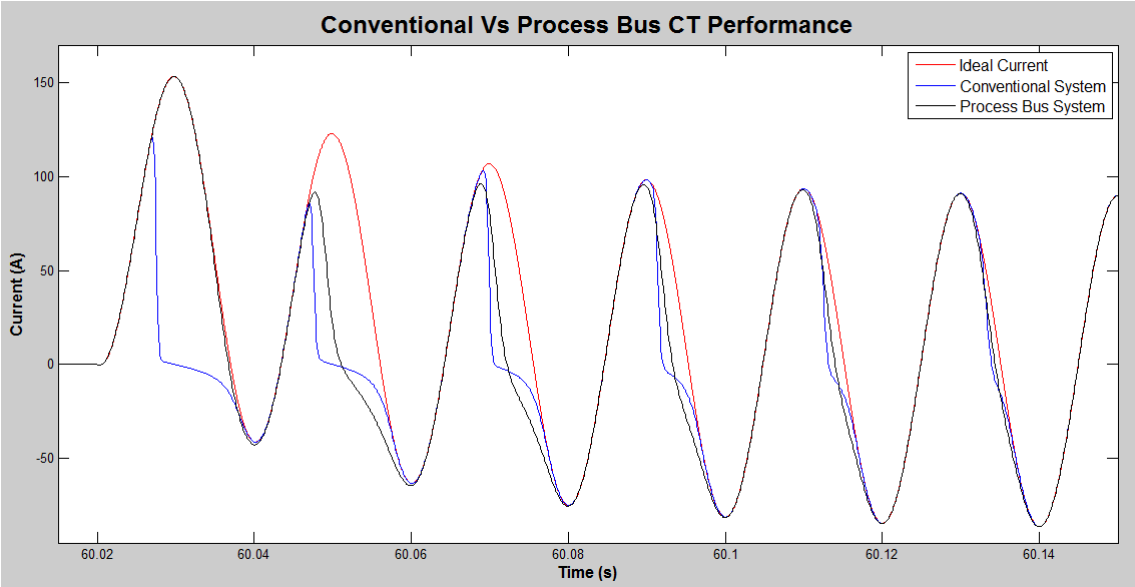

Figure 52 – Secondary current with respect to secondary burden change

From Figure 52 it can be concluded that there has been an improvement in the performance of the current transfer circuit. The particular improvement is its ability to replicate the ideal wave for the first cycle of the fault current before the flux builds up and causes the current transformer to saturate. However, after one and a half cycles the two systems are beginning to produce the same output.

5.3 Conventional Relay performance

5.3.1 General Characteristics

The conventional relay has advanced in technology from the electromechanical to the most recent the numerical relay. To establish the base level to compare the performance of the latest technology against, two manufacturers relays have been selected and subjected to the same test signals. The primary performance that is being assessed is the measured value/ analogue to digital converter component of the relay. The secondary performance is the transmission of the measured values to the protection function. Figure 53 below shows a simplified diagram of the flow of information.

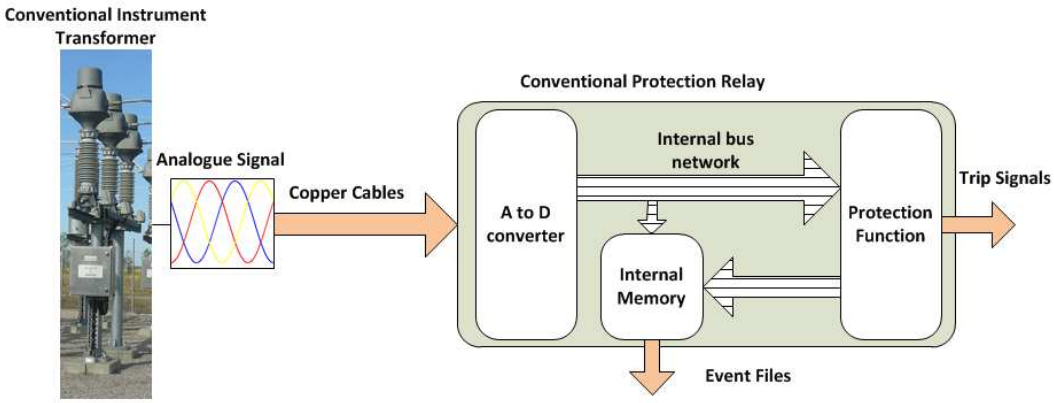

Figure 53 – Conventional relay information flow diagram

The first part of the information flow diagram is the analogue signal from the instrument transformer to the protection relay. As previously mentioned that the instrument transformer is used to convert the primary system conditions to a level that can be used in sensitive electronic devices. However, due to the sensitivity of these devices the relay further converts this to a small value using an internal transformer. A DC source can cause this internal transformer to saturate. Shown in Figure 54 is the two different manufacturers' relays that have been subjected to a DC step input of 10A for 100ms.

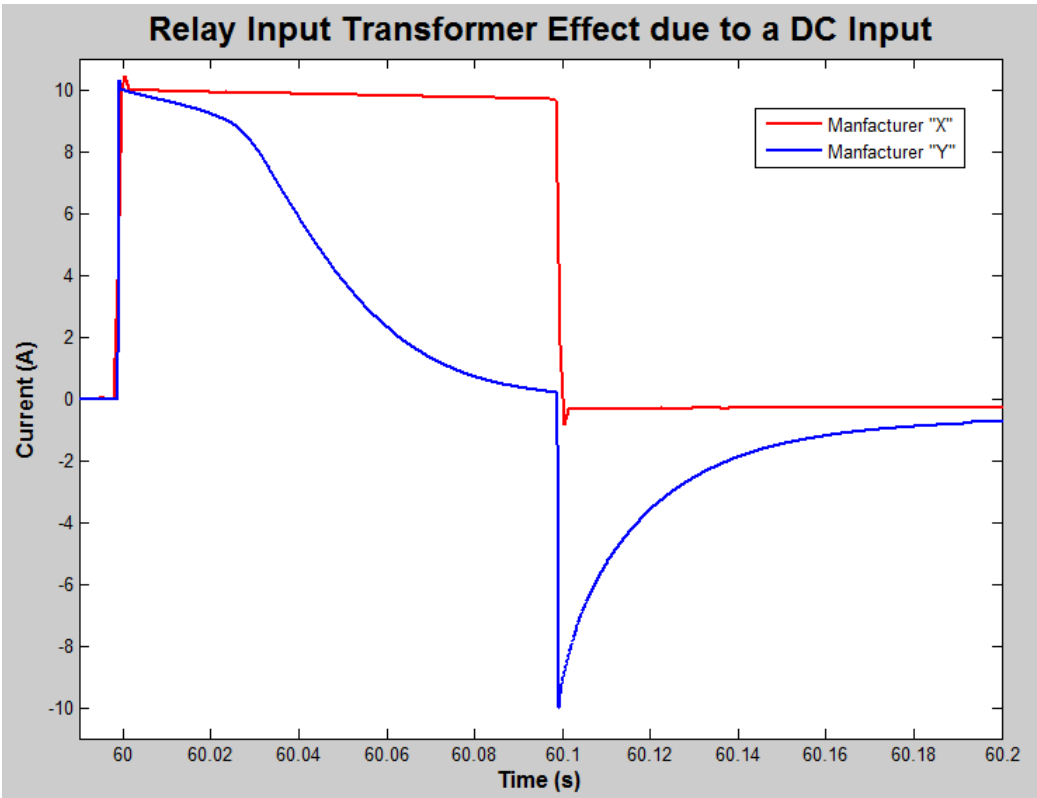

Figure 54 – Effect of the relay's input transformer on the output data

The results shown in Figure 54 illustrate the difference of two different manufactures relay performance due to their construction. The way it is constructed has a significant impact on the transient response of the relay. The remaining analysis on the test devices will be focused on the initial transient response until it is within plus or minus two percent of the input signal.

The quality of the sampled value produced by the analogue to digital converter is impacted by the following three characteristics:

1. Sample rate – The number of conversions per cycle
2. Measurement range – This is the allowable peak to peak measurement
3. Resolution – This is the smallest change in the input that the relay can record

The impact of each of these characteristics will be discussed when looking at the performance of each particular device. The data that will be used to assess each of the conventional relay is obtained from an event file in a COMTRADE format.

5.3.2 Manufacturer "Y" Protection Relay

The technical manual for manufacturer "Y" relay used in this project defined the recording sampling frequency of 128 samples/cycle, a measurement range of 64pu peak to peak and a 16-bit resolution. The measurement range has restricted the relays ability to replicate a high-level fault. However, the relay has a much better resolution for lower level measurements. The measurement range can be converted to an RMS value of approximately 22pu, if we used a 200:1 CT core this would me that a primary fault current with no transient component of 4.4kA could be replicated if the CT does not saturate. If this current does exceed 32pu peak then the recorded waveform will be clipped as shown in Figure 55.

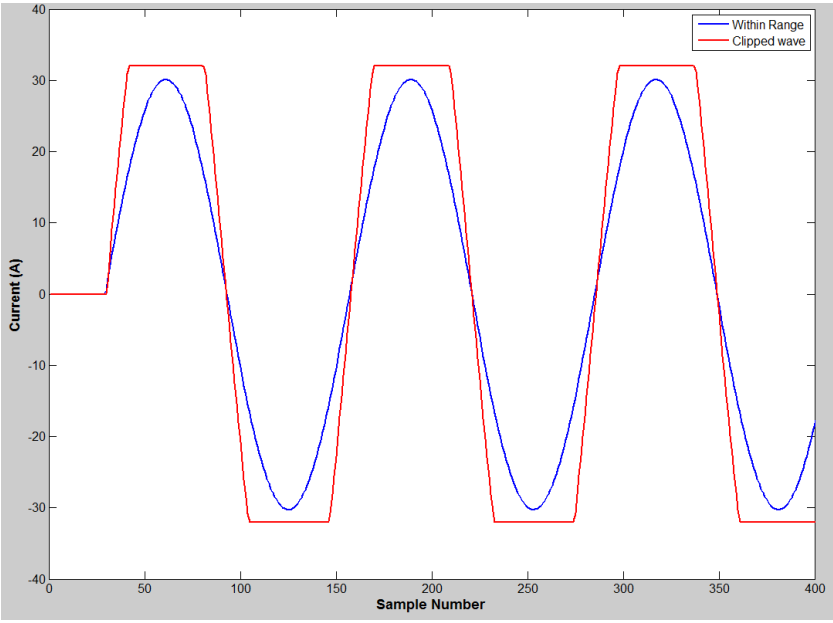

Figure 55 – Clipped Manufacturer "Y" waveform due to input exceeding 64pu peak to peak

Manufacturer “Y” relay was one of the protection relays used in the “Conventional Relay Base Test “as part of sampled value methodology. The transient response of this relay for a 10A DC step input is shown in Figure 56. The same method to check consistency of time stamping was used to check the consistence of the analogue to digital conversion. The sampling rate of the analogue to digital converter has a significant impact on the time to settle and reaction time to a change to the input of the relay. This particular relay has a sampling frequency of 128 samples/cycle, which equates to a sampling being recorded ever 156µs.

The transient response of a device can be categorised by a number of parameters. The performance of the conventional relay will focus on three:

1. Delay
2. Settling time
3. Percentage overshoot

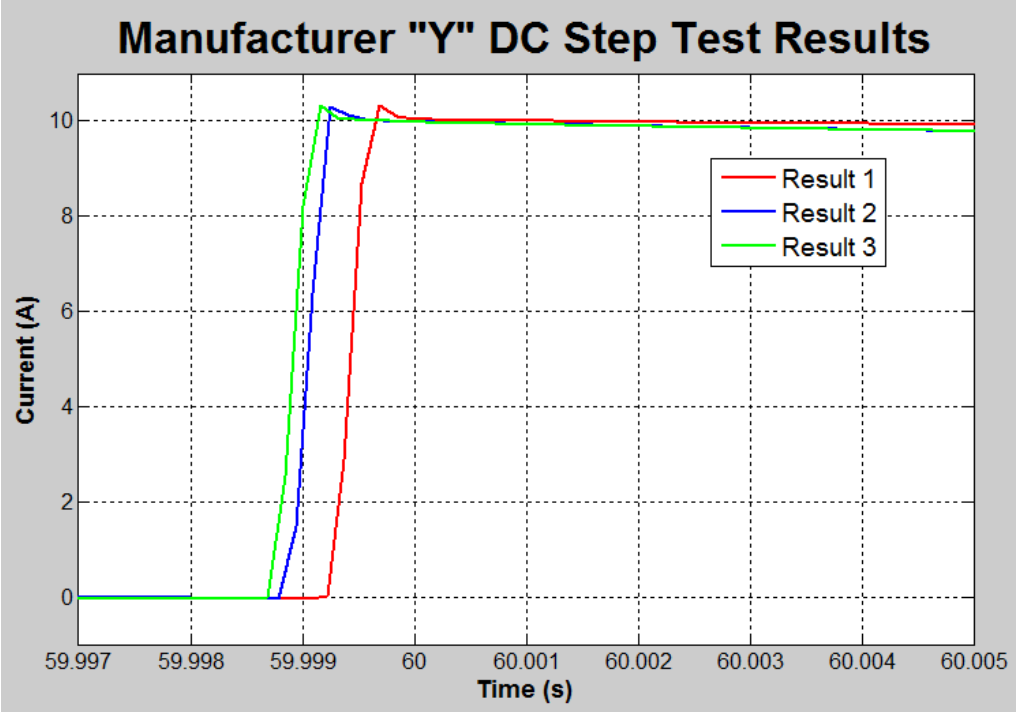

Figure 56 – Transient response of the manufacturer “Y” protection relay for a DC step input

The first point of interest with the results shown in Figure 56 is the delay. It would be expected that the process to perform the analogue to digital conversion should take a finite time hence, introduce a delay into the system. All three-test results indicate that the test signal is applied to the input terminals of the relay before the test signal has been started. Based on the tests results this manufacturer’s relay on average records that it sees the test signal approximately 1ms before the test signal is applied. Based on the sample frequency the relay has over corrected for the inherent processing delay by six sample counts.

The sampling frequency has a significant impact on the relay's settling time. This is due to the length of time between each sample, i.e. a low sampling frequency results in a longer period where the recorded data does not change. The settling time is based on the time for the system to settle to within plus or minus two percent of the test signal and this time is based on the time line of the recorded wave data. Therefore, manufacturer "Y" relay typically has a settling time of 500µs or three samples.

The results shown in Figure 54 indicate that the relay has a high dampening component that has resulted in a fast responding with minimal overshoot characteristics. Based on the three test results the transient response only exhibited on average a 3.126% overshoot. This characteristic has a positive impact on the settling time of the system.

5.3.3 Manufacturer "X" Protection Relay

Manufacturer "X" relay used in this project had a sampling frequency of 24 samples/cycle, a measurement range of 90.5pu peak and a 16-bit resolution. Based on the technical specification of this relay it can be derived that it samples the analogue signal every 833µs. Manufacturer "X" relay's transient response shown in Figure 57 was assessed against the same criteria as discussed in section 5.3.2.

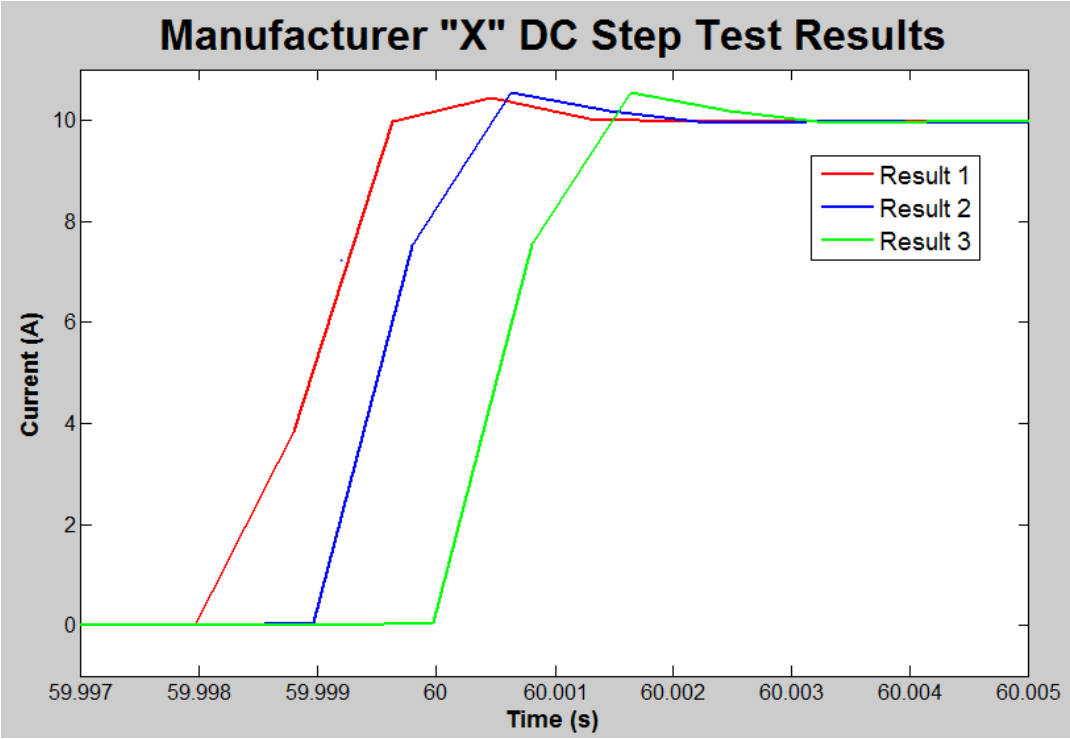

Figure 57 - Transient response of the manufacturer "X" protection relay for a DC step input

Manufacturer “X” relay recorded the input in the event file before the actual test signal was injected. Therefore, it can be concluded that the data processing within the relay has over corrected the internal delay by time stamping the measured value incorrectly. The three result obtained from the DC Step test showed that on average the relay recorded the first sample 900µs before the test signal was injected, which equates to only one sample based on the given sampling frequency.

The reduced sampling rate of this particular relay means that it only records a change in the system every 833µs. The average settling time based on the three results is 2.77ms or approximately 3 samples.

The last of the performance criteria is the amount of overshoot that the transient response includes. Manufacturer “X” relay’s result shown in Figure 54 clearly shows that the input has different characteristics to that of manufacturer “Y” relay, this change in characteristic has also influenced the amount of overshoot that the system experiences. The average overshoot for manufacturer “X” relay is 5.02%.

5.3.4 Conventional Relay Result Comparisons

The technical specification of each relay has defined a number of key differences. These differences have a significant impact on the analogue to digital performance. The range and bit resolution are not identifiable in the step test results. However, these specifications can have an impact on the normal operation of the protection relay.

Manufacturer “X” relay has the ability to record an input signal to nearly 3 times the peak value of manufacturer “Y” relay. By only assessing this specification one might conclude that manufacturer “X” has a better performance particularly with recording high fault currents. The second part to the measurement is its resolution, where both relays have a 16-bit resolution. With the reduced range, manufacturer “Y” has the ability to detect a 1mA secondary current change, where manufacturer “X” only has the ability to detect a 2.8mA secondary current. When using a 1000:1 current transformer ratio then the comparison is 1A verses 2.8A change in the primary system current. The use in protection this might seem an issue. However, for metering purposes such a change might be significant.

The sampling frequency technical specification impacts on the transient response of the protection relay. Figure 58 illustrates the difference between the transient responses of each relay. The analysis of each relay in the previous sections allows for an analytical assessment of the results.

The average delay of each relay was very similar, with manufacturer “X” relay being 900µs and manufacturer “Y” being 1ms. When comparing the delay in relation to number of samples it shows that manufacturer “Y” records the input seven samples before the input signal is inject compared to only one sample for the manufacturer “X”.

The biggest impact due to the sampling frequency was the settling time of the each relay. Both relays had the same number of samples to settle. Manufacturer “X” relay actually settles 5 times slower than manufacturer “Y” relay.

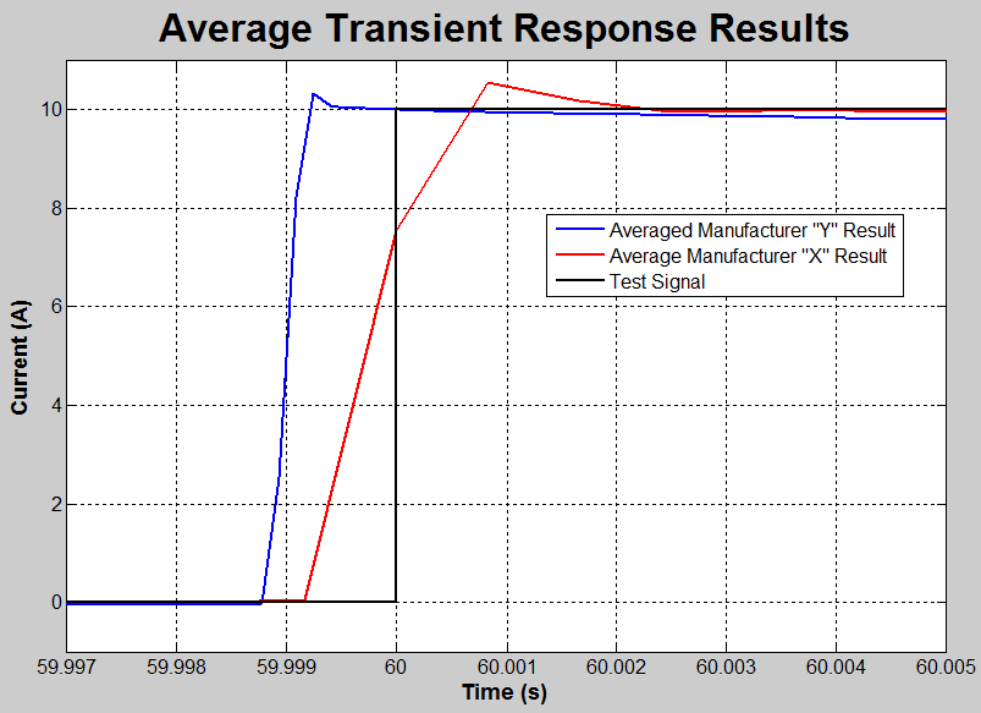

Figure 58 – Average waveform comparison for the Manufacturer “Y” and Manufacturer “X”

5.4 Process Bus performance

5.4.1 General Characteristics

The process bus system consists of three device to perform the same function as the conventional relay. The three devices are:

1. Analogue merging unit – this device replaces the analogue to digital converter component of the conventional relay.
2. Ethernet Switch – this replace the internal bus network shown in Figure 53.
3. 9-2LE Protection Relay – this relace the protection function component of the conventional relay.

To understand how each device impacts on the overall process bus system it requires the results from three different test setups, as shown in Appendix E. The first test is set up such that the sampled values produced by the analogue merging unit are sent via an ethernet switch to the subscribing 9-2LE protection relay.

The data extracted from these tests are the sampled value packets recorded from the network and an event file from the 9-2LE protection relay. The sampled values packets will produce the information required to assess the performance of the analogue merging unit. The event file is critical to determine a time line for key moments to determine time delays of each device.

The next test setup is to connect the analogue merging unit directly to the 9-2LE protection relay. An event file is extracted from the 9-2LE relay for this test setup is to produce another time line that can be used with the time line from the previous set up to determine the impact of the ether net switch.

The final test setup is to use the Omicron CMC850 to generate a sampled value message stream and publish them onto the same network as used in the first test setup. The data extracted from this test setup was the same as the first test set up. However, the sampled value packets were used to confirm the test signal produced by the CMC850 test instrument. The event file was used to observe the performance of the 9-2LE protection relay's sample recording and to establish a time line that could be used to refine the delays due to the network.

5.4.2 Manufacturer "Z" Analogue Merging Unit

Manufacturer "Z" merging unit used in this project had a sampling frequency of 80 samples/cycle, a measurement range of 90.5pu peak and a 24-bit resolution. *Brunner, et al. (2004)* has indicated the impact of varying the resolution has on the performance of the merging unit. However, the only requirement set by the IEC61850-9-2 standard is the 80 samples/cycle. The increased bit resolution allows the merging unit to be able to detect a 10μA change in the secondary current.

Manufacturer "Z" merging unit has time stamped the sampled value such that any internal delay due to converting the analogue to digital and processing the information has been corrected. Given the consistency of the signal time stamping for multiple test, as described in section 4.4.3.4 , the merging unit has consistently recorded that the input starts four samples before the test signal is injected into the system. Table 2 below shows that the first recorded current occurs on a sample count of 3996, hence the four-sample error previously mentioned.

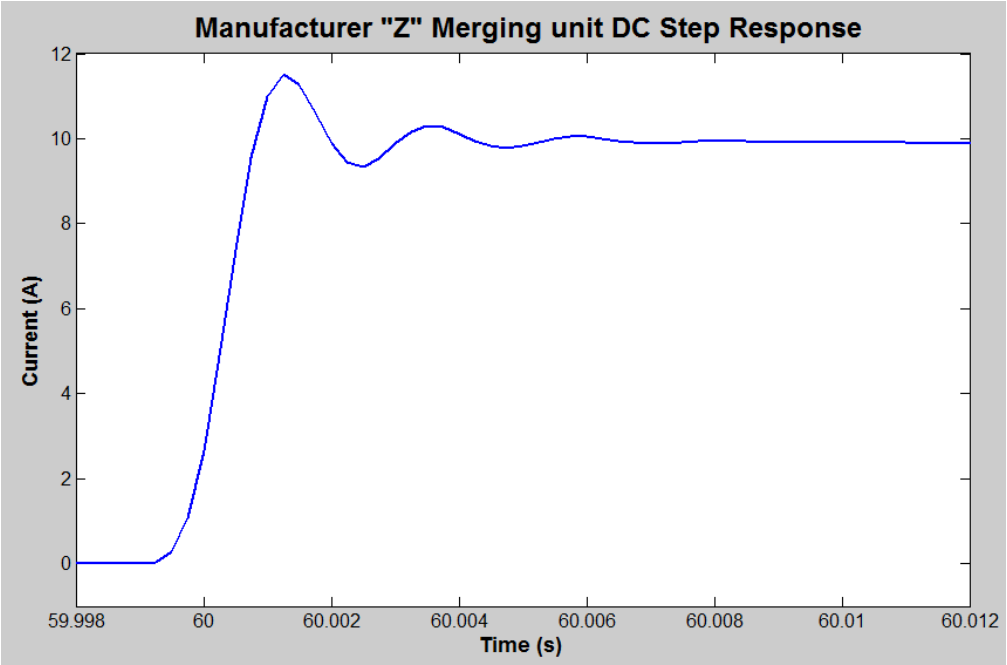

Figure 59 - Transient response of the Manufacturer "Z" merging unit for a DC step input

Logical Node	Sample Count	A-Phase Current (A)	B-Phase Current (A)	C-Phase Current (A)	Neutral Current (A)
Manufacturer Z	3995	0	0	0	0
Manufacturer Z	3996	1	0	0	0
Manufacturer Z	3997	33	0	0	0
Manufacturer Z	3998	288	0	0	0
Manufacturer Z	3999	1095	0	0	0
Manufacturer Z	0	2665	0	0	0
Manufacturer Z	1	4897	0	1	0
Manufacturer Z	2	7376	1	1	0
Manufacturer Z	3	9553	1	1	0
Manufacturer Z	4	10990	1	1	0
Manufacturer Z	5	11518	1	2	0

Table 2 – Manufacturer "Z" merging unit step test recorded data

The transient response shown in Figure 59 above indicates that the rate of change upon the input of the test signal has decreased compared to the conventional relay. The time taken to reach the first peak is impacted by this rate of change. The Manufacturer "Z" merging unit has experienced a time of approximately 2.2ms or nine samples.

The settling time of manufacturer "Z" merging unit has been approximated to be 6ms. Based on this nearly half the time for the system to settle is taken up by the time taken to reach the first peak. The amount of overshoot that is experienced also contributed to the length of time for the system to settle. The tested merging unit experienced approximately 15% overshoot.

5.4.3 Manufacturer “W” Ethernet switch

This device is tasked with routing the broadcasted sampled value packets produced by the Manufacturer “Z” merging unit and the Omicron CMC850. The device does not change any part of the sampled value hence it can be said that an ethernet switch is effectively a time delay. This delay can become critical as each ethernet switch that is added into the network between the output of the merging unit and the input to the protection has a cascading effect.

The observed time delays though out the system are dependent on the time stamping of the data by each test device. The results previously discussed showed that the devices are trying to correct for internal delays. These adjustments are not consistent between manufacturers hence the need to perform two different tests, one with the switch in-service and the other with the switch bypassed.

The event files from manufacturer “Z” relay have been used to determine the delay of the ethernet switch. The assumption made for this assessment is that the processing of the sampled data packets once the information reaches the ethernet port of the relay is consistent with both test procedures. Each of the tests have been conducted three times with a DC step input to check consistence, the inconsistency was discussed in section 4.4.3.3. To derive the approximate time delay the three results for each test type has been averaged back to a single start time. Figure 60 below shows the average result for each of the test connections.

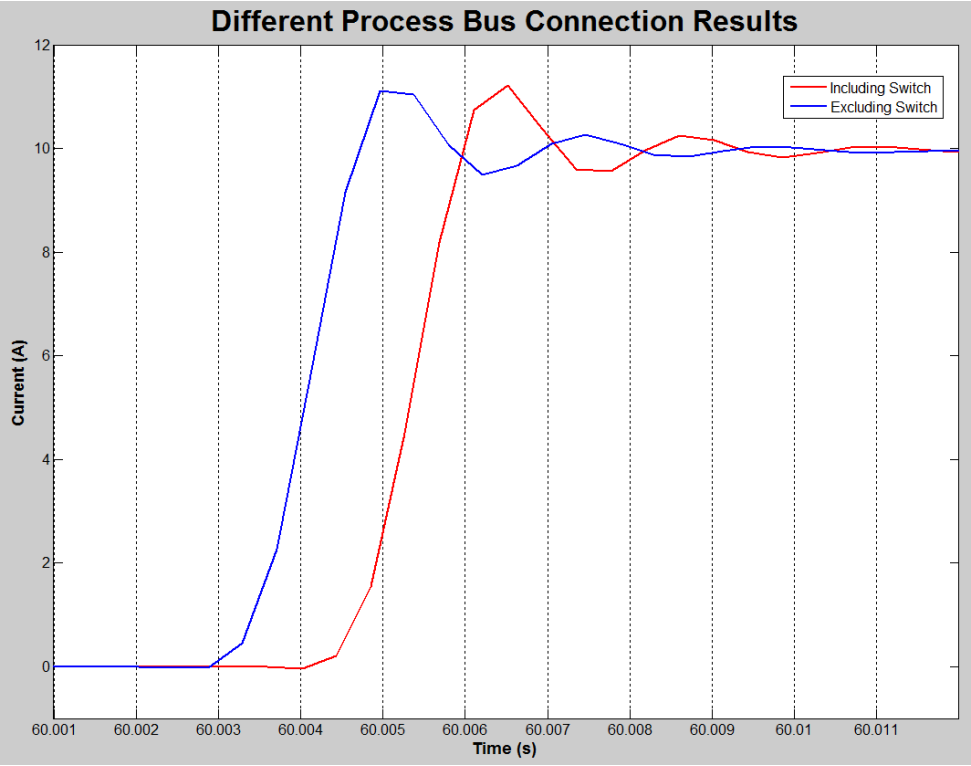

Figure 60 – Comparison of test results for a process bus network with different connections

The results of these two test as shown in Figure 60 resulted in a delay of 1.1ms. *Yang (2012*) defined this delay as "*Ethernet switch latency is defined as the time it takes for a switch to forward a packet from its ingress port to its egress port"*. A review of the manufacturer "W" ethernet switch datasheet revealed that the switch latency should only be 7µs, which is significantly less than what the results have indicated.

The difference in switch latency has not been explored further. This would require additional hardware and knowledge to understand possible switch configurations. This has been included as future works.

5.4.4 Manufacturer "Z" Protection Relay

Manufacturer "Z" relay is a line differential relay that is 9-2LE compliant. This means that the CT and VT module that is in a typical relay has been replaced with an ethernet card. The processor that previously managed the analogue to digital conversion is now used to re-sample the sampled value data stream to which it has subscribed to use.

The sampled value stream is governed by the standard to produce 80 samples per cycle where the relay is free to use as little or as many of those samples, provided it will perform the protection functionality correctly. Manufacturer "Z" relay resamples at a rate of 48samples per cycle.

Having a lower sample rate than that of the data stream provided allows compensation for any packet loss. The reduced sample rate means that the resolution has been impacted and the peak has not been recorded appropriately during the DC step response test, Figure 61 illustrates this issue. Given that, the typical system that this relay will be used in this would not be considered a problem.

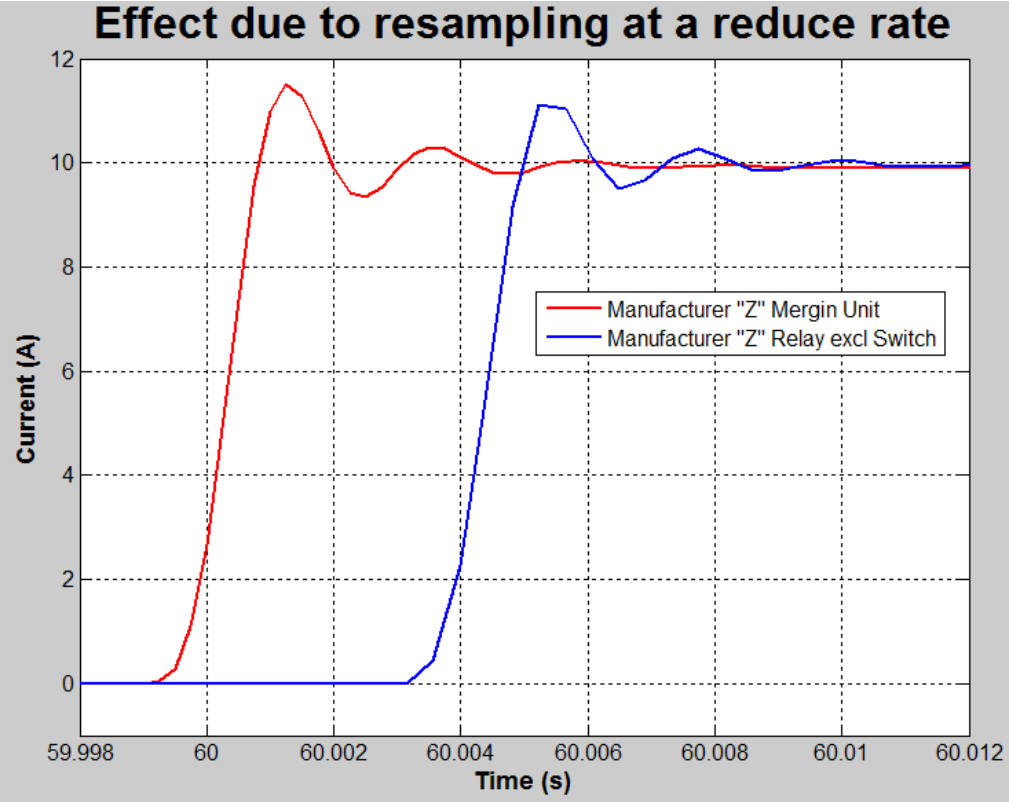

Figure 61 – Effect of the reduced sampling rate between the merging unit and the protection relay

The results shown in Figure 61 are based on manufacturer “Z” relay resampling a sampled valued data stream from a merging unit during a step change. This has meant that the performance of the protection relay could not be correctly observed. However, from those results the relay data showed signs that it would only record data that was in sampled value message.

Using the IEC61850 test equipment manufacturer “Z” relay was subjected to a generated DC step input sampled value stream. Figure 62 below indicates that manufacturer “Z” relay does not only record what it is given in a sampled value packet. This is represent by one sample before the signal is generated being lower than zero and the overshoot of one sample.

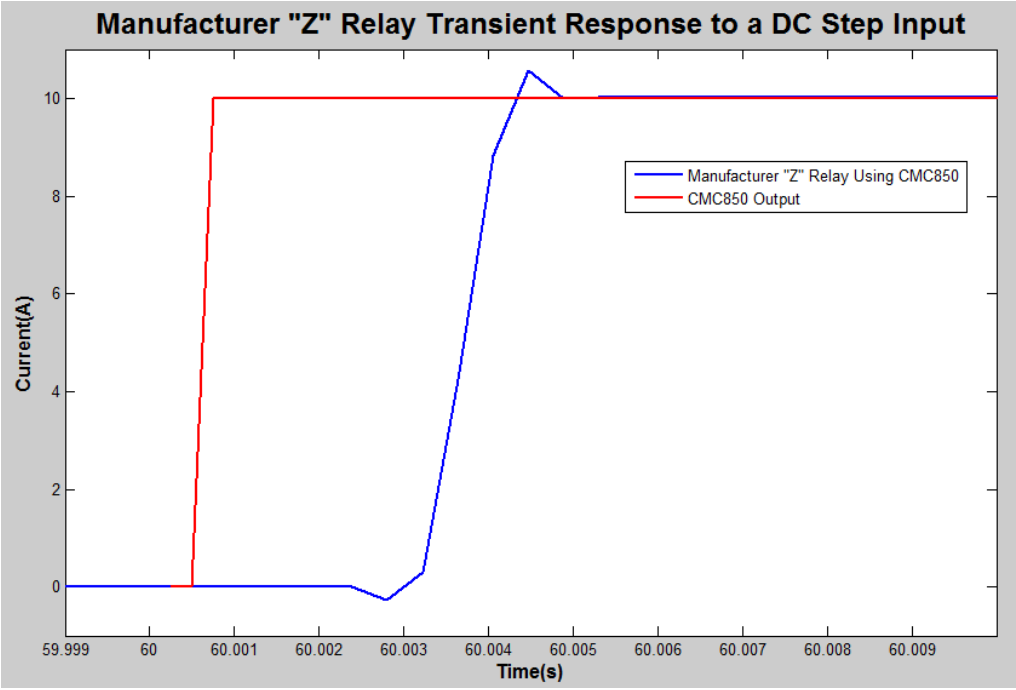

Figure 62 – Manufacturer "Z" relay transient response to a step input

The internal delay due to the resampling process can be approximated based on the results shown in Figure 62. The assumptions that will be made is that the Omicron CMC850 publishes the sampled value packet as per the time stamping i.e. the first sample is published on to the network at 60.0005s. In addition, the other assumption is that the delay due to the transmission over the ethernet cable is insignificant and can be omitted and the ethernet switch introduces 1.1ms delay. Based on the above assumptions the internal delay for manufacturer "Z" relay is approximately 1.4ms.

5.5 Summary

The performance of the each device has an impact on the operation of the whole system. In the case of the conventional protection relays, the impact can be accounted for in the protection algorithms or by specifying the minimum CT specifications. The reason for this is that the manufacturer has developed both components of the protection system and performed multiple tests to understand where improvements are needed.

Most numerical protection relays are designed to operate in such a short time frame, which means that the improvements that are gained by reducing the lead burden would be very beneficial. The results indicate that the CT will begin to saturate after approximately once cycle.

The transient response of the conventional relay to a DC step current input indicates that they have a very short rise time with very little overshoot. The response of the two different manufacturer's relay also highlighted that neither manufacturer performs the analogue to digital part of the process the same.

The process bus equipment that has been tested has shown that the measurable performance of the merging unit to a DC step has reduced than that of previous technology. The overshoot has increased from approximate 3% to 15% and the setting time has increased by nearly five times. The merging unit has also shown the characteristic that it is time stamping the measured values with the internal delay trying to be accounted for.

The ethernet switch and 9-2LE compliant protection relay also has introduced additional delays into the system. The results from the tests also indicate that manufacturer "Z" relay also does not only record the sampled value data produced by the Omicron test equipment. This error can be seen in Figure 62 with the overshoot and pre-test jitter.

Chapter 6

Analogue Merging Unit Transfer Function

6.1 Overview

The relocation of the analogue to digital component of the protection relay into a separate IED has the potential for affecting the performance of the protection function. In section 5.3.4 the comparison of the two different manufactures analogue to digital conversion and recording them has proven that they are not the same. Manufactures in the past has had the ability to develop their protection algorithms based on the known quality of their measured data.

The analysis of the analogue-merging unit in section 5.4.2 has identified that the tested device have corrected the time stamping of the sampled values to compensate for internal delays. The effect of the internal delay of the merging unit could affect a protection schemes such as a low impedance differential protection if the error is not known and dealt with correctly. The intent of the IEC61850 standard is to be interoperable such that in the above example it should be possible to use different manufacturers merging units to perform the appropriate measurements. Based on this if there are differences in the time stamping then there is a possibility that this could be seen as a phase shift and cause an incorrect trip.

The hardware and software used to measure and record the system's conditions consists of a number of components. These components have been simplified into three main functions shown in Figure 63 below. The first component is referred to as the analogue interface. This interface is a combination of a number of passive components to transform the current lower further for use in the relay's sensitive circuitry.

The following two components in the system are digital in nature. The A to D converter uses appropriate transduces to convert the filtered analogue signal into a digital format. Once this has occurred the data is then processed by microprocessor. The microprocessor is then responsible for filtering and creation of the sampled value message that contains all the information that is to be sent to a protection relay.

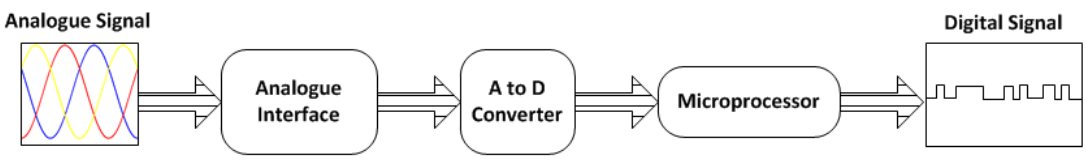

Figure 63 – Simplified block diagram for information flow in a merging unit

To allow the utility companies to use these devices, it would useful if a useable definition that described the performance of the merging unit. A typical system's performance can be represented by a system transfer function. This function allows the user to be able to predict the output of the merging unit for any particular input.

The merging unit was subjected to three different transient response tests, the results of these tests will be used to develop the transfer function for this particular device. These tests are:

1. DC Step response
2. Frequency response, and
3. Impulse response

6.2 DC Step Response

The test signal for a DC step response has been used to develop an understanding of the performance of the device examined as part of this project. This type of response also has known characteristics that can be used to approximate a second order system. Figure 64 below shows a typical response of a second order system to a step input.

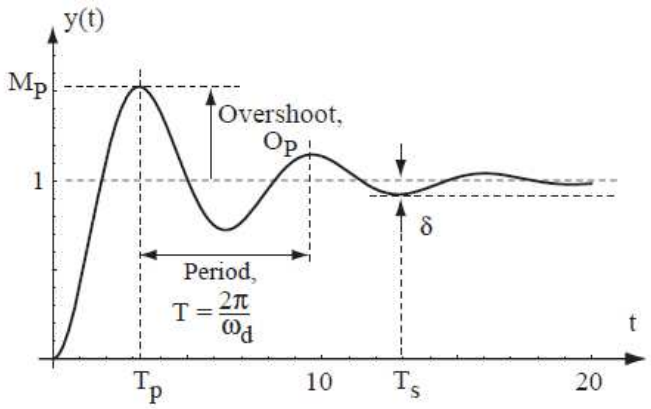

Figure 64 – Underdamped system parameters (Norris, 2009)

The above figure has been theoretically developed based on the assumption that the input signal can go from zero to a known value instantaneously. The DC step signal generated by Doble test equipment was put into an oscilloscope to confirm the test signals characteristics. Figure 65 below clearly indicates that there is a finite time required for the Doble to complete the step change. This characteristic of the test equipment will be used to test the derived system transfer function.

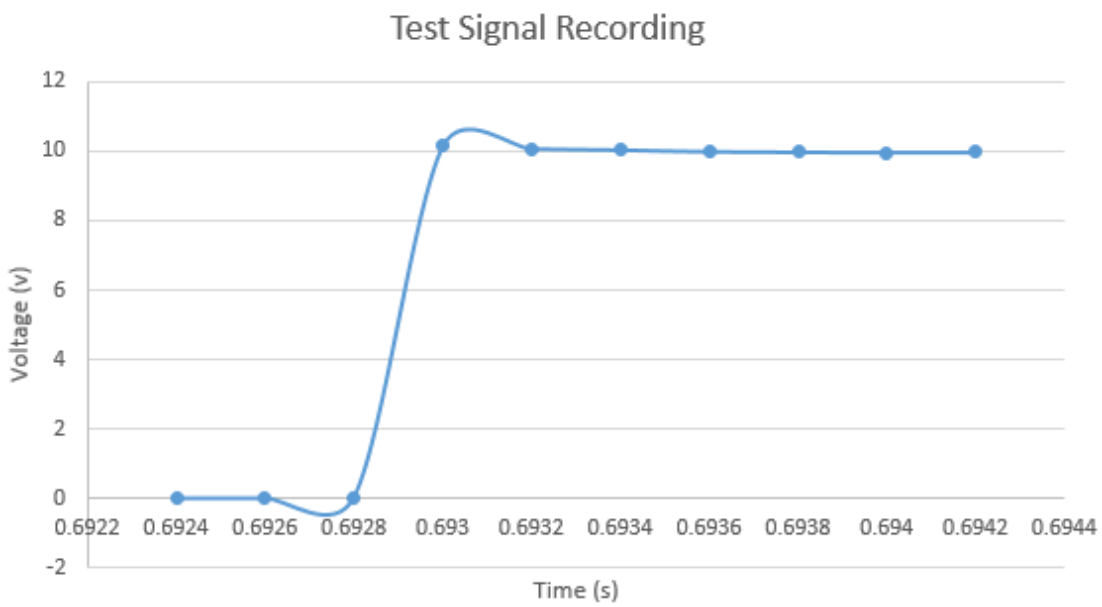

Figure 65 – Doble DC step test signal oscilloscope recording

The second order transfer function approximation is given by equation (6-1. Using the characteristics such as the percentage over shoot and the dampening time constant obtained from the test data an approximate system transfer function can be derived.

$$H(s)=\frac{{\omega_n}^2}{s^2+2\zeta\omega_n s+{\omega_n}^2} \qquad (6\text{-}1)$$

Where,

H(s) = Transfer function

ω_n= Natural frequency

ζ = Dampening coefficient

Figure 64 – Underdamped system parameters

Manufacturer "Z" merging unit had approximately 15% overshoot and had a dampening time of approximately 2.25ms. Using these values the two unknowns in the transfer function can be calculated by solving the equations (6-2) and (6-3).

$$\zeta=-\frac{ln(OP)}{\sqrt{(2\pi)^2+ln^2(OP)}} \qquad (6\text{-}2)$$

$$\omega_n=\frac{2\pi}{T_D\sqrt{1-\zeta^2}} \qquad (6\text{-}3)$$

This resulted in a transfer function of:

$$H(s)=\frac{8.51\times10^{6}}{s^{2}+1686s+8.51\times10^{6}}$$

Figure 66 below shows the Simulink model that has been used to assess the derived transfer function from a step response against actual test data. Figure 67 shows the result of the test data vs that of the transfer function. The transfer function is known to be only a 2nd order approximation hence the error that occurs between the two plots. However, the results of the model has shown that the derived transfer function has the ability to produce an output that is a good representation of the test data.

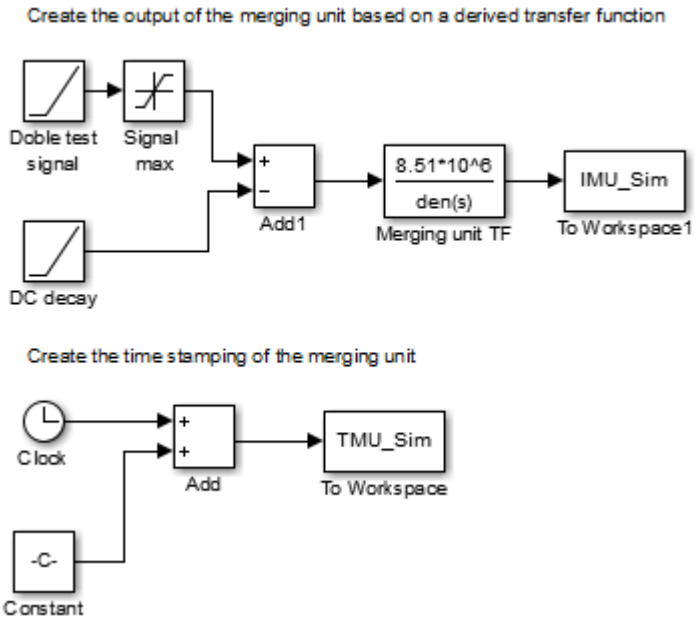

Figure 66 – Step input Simulink model extract

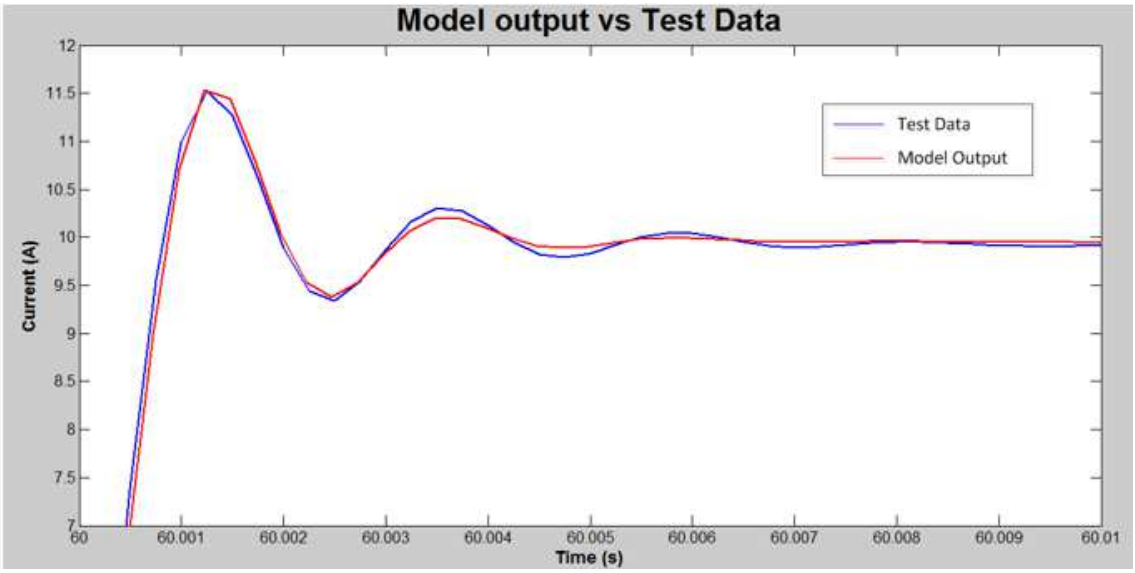

Figure 67 – Comparison of the model out vs actual test data

6.3 Frequency Response

Frequency response testing is one technique used to obtain an understanding of how a system responds to different inputs. The procedure for a frequency response test is to subject the system to range of frequencies, record the steady state gain and phase error. These results are then plotted on semi-log graphs to derive key characteristics that can be used to determine a transfer function of the system.

The Doble test equipment used in this test procedure is accurate for frequencies of 1Hz up to 1000Hz. To enable a relative high resolution for the results the frequency was increased by steps of 10Hz and the results recorded.

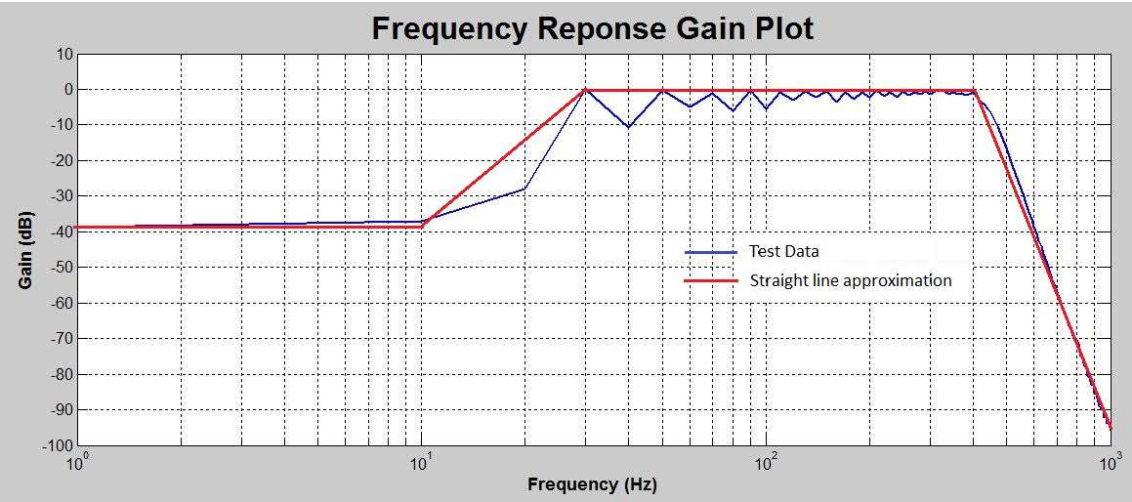

Figure 68 – Frequency response test results in a gain and phase bode plots

The test results obtained from the frequency response shown in Figure 68 above indicate three distinct turning points. These points of interest are referred to as corner frequencies. The rate of change from one corner frequency to the next describes if it corresponds to either a “zero” or a “pole”. The characteristic of a zero is that there is a positive increase in the rate of change of 20dB/decade beginning at that particular frequency. Therefore, based on the straight-line approximation of the test results there is one zero in the frequency response plot, this occurs at 10Hz. The gradient of this line is approximately 160dB/decade; this equates to eight zeros all occurring at 10Hz.

The second corner frequency occurs at 30Hz where the gain levels off at 0dB. For this to occur an equal amount of poles to that of the zeros described above need to occur. The final corner frequency obtained from the testing occurs at 400Hz where a -240dB/decade is being recorded. This has resulted in an additional 12 poles.

The DC gain is located where the result crosses the y-axis, based on the test results this is approximately -40dB. Combining all these known conditions allows a transfer function to be derived.

$$H(s)=\frac{0.01\left(\frac{s}{10}+1\right)^4}{\left(\frac{s}{30}+1\right)^4\times\left(\frac{s}{400}+1\right)^{12}}$$

Using MATLAB® the above transfer functions Gain bode plot was obtained to compare to that of the test data. The result of the gain plot for the derived transfer function can be seen in Figure 69. It is clear that there is considerable error between this plot and the tests results.

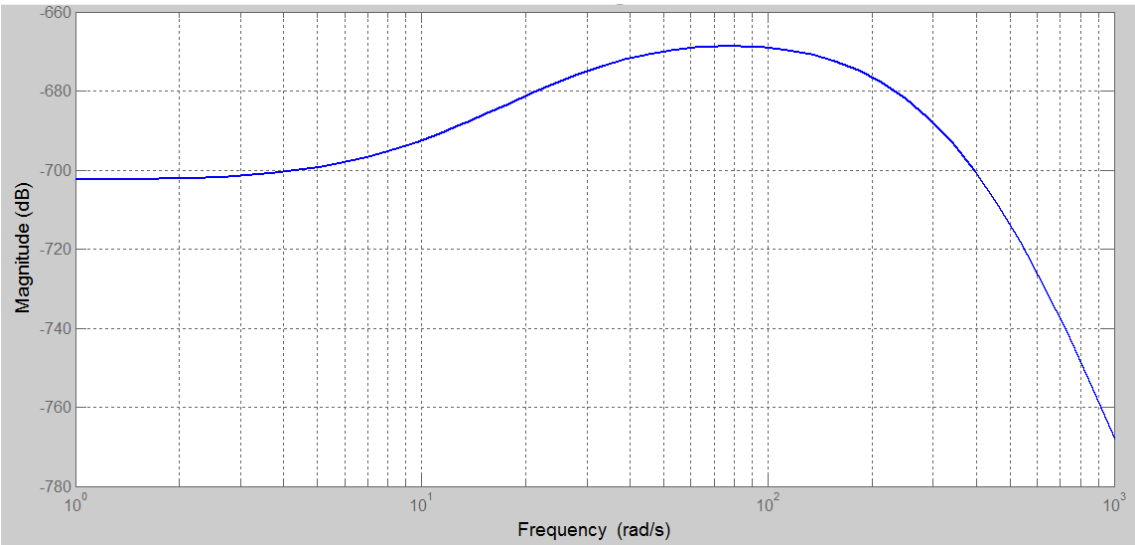

Figure 69 Gain plot of the transfer function based on the Zeros and poles of the test data gain plot

The limited ability to observe the frequency response of the system at higher frequencies could be the reason for this error. The gain bode plot for the transfer function obtained via the step response test only had one corner frequency that occurred at approximately 2300Hz. This indicates that the system has higher frequency components to its response characteristics.

6.4 Impulse Response

An impulse response test subjects the system to a theoretical pulse that is infinite at time zero and zero for all other time. This type of signal is not possible via typical test equipment. The Doble state simulation has a minimum signal duration time of 2ms, hence the response shown in Figure 70.

The two parameters observed for the step response in section 6.2 can also be observed in the impulse response. The percentage overshoot for the impulse test is approximately 13% and the dampening time constant is approximately 2.5ms. This has resulted in a 2nd order transfer function approximation similar two that of the step response. Given this, Figure 70 also includes the transfer function from section 6.2 response to the same impulse test signal.

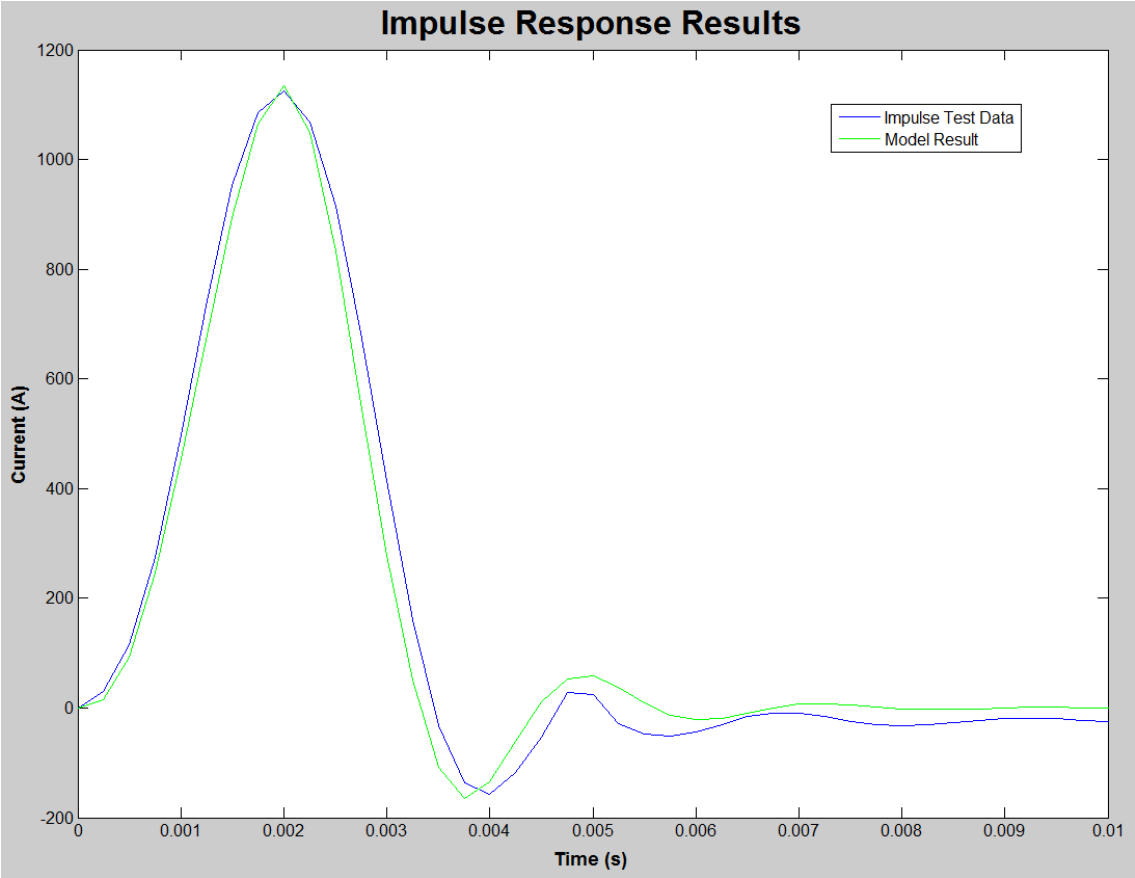

Figure 70 – Impulse response of the Alstom MU Agile

The above result indicates that the transfer function derived from the step response has produced an output that closely matches the impulse test result.

6.5 Summary

The ability to predict how the merging unit will represent the analogue system is important to the overall protection system. In the past, the performance of the analogue to digital component could be tested and designed into the protection algorithms by each manufacturer. This ability has been removed, as the intent of IEC61850 is that a protection relay should now be able to use the sampled values for another manufactures merging unit.

The performance criteria that could affect the protection system not only refers to the differing time delays but the transient response of the merging unit. In a high-speed protection, having differing transient responses could cause inappropriate tripping. Two examples of typical analogue system signals would be the unsaturated (normal) wave and a saturated (fault) wave.

The result of the different transient response tests to determine the transfer function that approximates the merging unit is:

$$H(s)=\frac{8.51\times10^{6}}{s^{2}+1686s+8.51\times10^{6}}$$

The result of subjecting the above transfer function to the typical system signals are show in Figure 71 and Figure 72 below. Also included in the plots are actual test data results. The unsaturated response of the model has resulted in a slight gain error of approximately 1%.

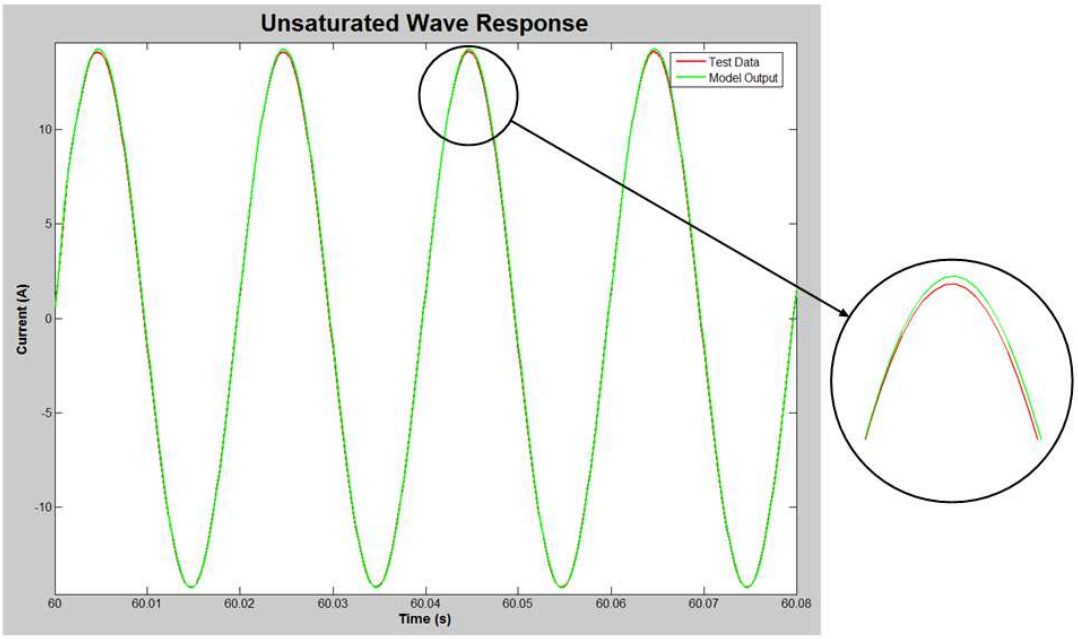

Figure 71 Unsaturated waveform results

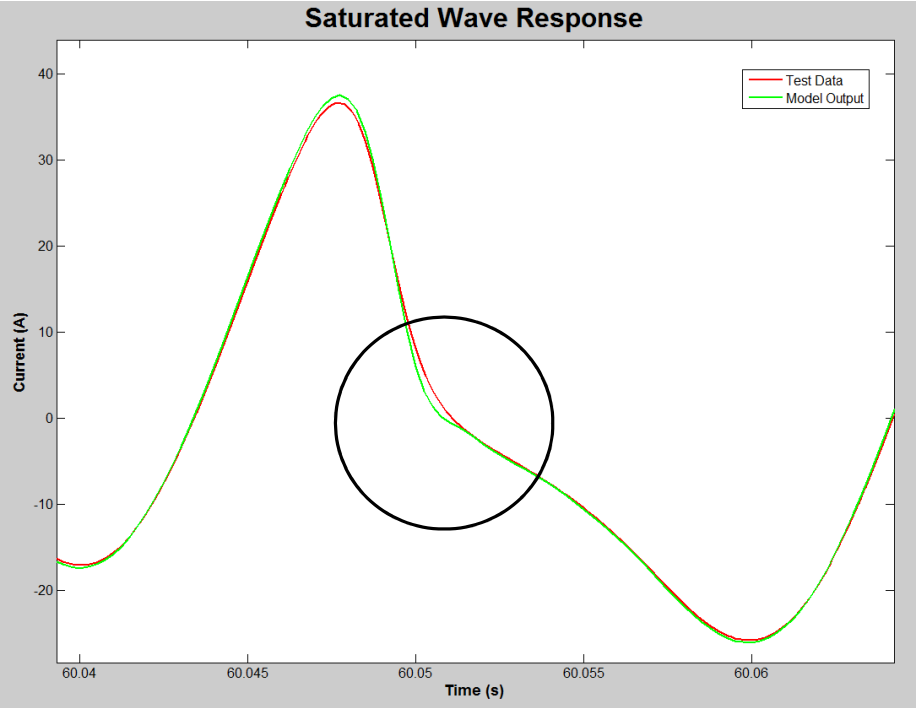

Figure 72 Saturated waveform results

The model's response to a saturated current waveform has shown issues about the x-axis during the most deformed part of the wave. This is shown in the circle section of Figure 72. The derived transfer function for the merging unit is a 2^{nd} order approximation. This has limitations to the frequency response of the system to replicate the actual system, which could be the cause of this error.

Chapter 7

Conclusion

7.1 Project Summary

The development of the process bus architecture to implement sampled value IEDs involves two technical requirements, system availability and system performance.

7.1.1 System's Availability

The system's availability refers to the reliability of the new construction of the communication path between the conventional instrument transformer and the protection. The significance of this component for the operation of a critical safety system in a high voltage electrical network requires that the communication path to be very reliable.

The present construction practice for this communication path is via copper cable that is connected directly from the terminal of the instrument transformer to the rear of the protection relay. This system consists of simple components that makes this construction highly reliable. The development of the process bus has essentially replaced the copper cable with three new components, fibre optic cable, analogue merging unit and ethernet switch.

The process bus components that have been introduced consist of electronic components that exhibit lower reliability attributes. The assessment of the isolated conventional component of a complete substation has determined a system availability that is used to set the minimum requirement for the process bus network. When comparing the minimum process bus network to replace the copper cable it was identified that, the availability reduced from 99.9968% to 99.9895%.

A reduction in the system's availability can be overcome by a number of methods that were discussed in section 3.2. It was concluded that at a minimum the system's availability could meet the required value by having redundant communication paths between the merging unit and protection relay. It is a requirement of the system that there is a very small amount of time to restore the network if there was a failure of a communication; this has meant that the rapid spanning tree protocol would not be adequate and the new Parallel Redundancy Protocol and High-availability Seamless Redundancy IEC62439-3 protocols are to be used.

This logic was applied to the ultimate architecture required for a two by 32MVA transformer substation construction. A number of additional conditions were considered to develop two possibilities for the ultimate architecture. These were scalability of the structure of the process bus and the physical connection arrangement of the main and back up protection schemes.

The ultimate process bus architecture described in section 3.3.2.3 would be the preferred architecture. This process bus architecture achieved the first key requirement of meeting or exceeding the availability of the conventional system. The physical separation of the main and back up process bus architectures allows the system to comply with separate networks when a maintenance or a fault occurs on one of the redundant communication path. The configuration of the ultimate architecture allows for progressive implementation of individual blocks to match a strategic increase in the electrical capacity of the substation.

7.1.2 System's Performance

Having proven that the process bus architecture can conform to the system availability criteria, an understanding of the change in the system's performance with the introduction of new technology. To achieve this a number of specific test configurations were developed to obtain the appropriate data to access the impact of the new technology.

The initial assessment referred to the time delay and process of recording sampled values. The impact of the accuracy and consistency of the time synchronisation for a device identified some clear observations. The first being that the IRIG-B used to synchronised the protection relays consistently had differences between the times stamping of the recorded results. This inaccuracy does not influence the functionality of relay, instead when investigating events and trying to piece together sequence of events could become troublesome.

The analogue merging units time stamping is critical to the correct operation, in particular when multiple merging units are used in one protection scheme. The results for the merging unit that used a one pulse per second was very positive with a consistent time stamping of multiple tests.

The concerning component of the time stamping of the merging unit is the observation that it has adjusted for any internal delays. Although different manufacturers could have different internal delays and if no adjustment is made by any manufacture, than the time stamping could be different and the same effect could occur. The concern is that as the end user this information should be made available such that it can be accounted for when implementing the protection scheme or accounted for by a standard so that the intent of IEC61850 of being interoperable can be achieved.

The location of the merging unit has removed the lead burden from the instrument transformer secondary circuit. This has an impact the performance of the current transformer during high fault current conditions that drives the current transformer into saturation. The conclusion of this assessment is that by removing the secondary lead burden it has delayed the saturation of the core until the start of the second cycle. With the development of electronic relays, such an improvement is considerable with the ability of the relay to identify a fault within the first cycle.

The analogue to digital component of the protection relay has been relocated to a new device that it now needs to subscribe to for the system measurements. The quality of these measurements that are termed “Sampled Values” is important when using different manufacturers for the two devises. The key criteria that was obtained by observing the transient response of the devises to a DC step input were the amount of overshoot, rise time to the first maximum, damping time constant and the settling time.

Two different manufacturers were used to observe a conventional relay’s characteristics to compare with the new technology. The first observation is that each manufacturer has a different response to each other. They both exhibited a quick rise time with very little overshoot and settle within a few samples.

The hypothetical assessment that the analogue to digital module from the conventional relay has simply be relocated to a separate device was not been represented in the test result. The single merging unit that was assessed as part of this project for the same characteristics were not as favourable as the conventional relay. The merging unit exhibited nearly 10 times the amount of overshoot, a much slower rise time and a settling time that was nearly a quarter of a 50Hz cycle time period.

The transportation of the sampled value is through the process bus network that consists of a number of ethernet switches. The typical switch latency that technical documents claim is in the low microsecond range. The particular ethernet switch used in the test process bus is meant to be approximately 7μs. The test results indicate that there is a 1.1ms latency however; further work is required to understand the impact switch configuration has on this result.

The new protection relays that are 9-2LE compliant have replaced the CT/VT module with an ethernet card. The relay used in this project resamples the 80 samples per cycle produced by the merging unit at 48 samples per cycle. The logic that the protection relay would only uses the information within a sampled value message has been disproved via the test performed that used a generated sampled value stream from the Omicron CMC850 test equipment. The relay recorded values that were not within a sampled value message.

If the merging unit were to be implemented into a protection scheme that used multiple units then a way of predicting their performance would be useful. A mathematical model that representing the merging unit would allow the end user to predict the output of device for different input situations. The results obtained via observing the device's transient response allowed for a second order transfer function approximation. This mathematical representation was then tested with typical network signals that resulted in the identification that although close there is still error.

7.2 Further Work

7.2.1 Process Bus Architecture

Process bus architecture will also have the ability to include the control signals for primary plant, such as trip signals. The availability assessment conducted as part of this project only assessed the components associated with the communication path of the measured value between the instrument transformer and protection relay. Recent developments of the merging unit has included additional functionality to control primary plant. This means that the utilisation of the communication path will be increased.

Given this development, a full assessment of the whole protection system, that includes all associated components used, would allow for better understanding of the full impact of implementing process bus with all of the functionality used.

7.2.2 Developing a Mathematical model for a merging unit

The work that has been complete as part of this project has been able to identify a 2^{nd} order approximation for the merging unit. The results show that there is still a consistent level of error in the reproduction of the output verse that of the test data. Developing a method to determine a more accurate model would assist with representing high transient fault conditions and possible condition monitoring situations.

7.3 Merging Unit Assessment

The development of IEC61869 part 13 due for publication in 2015 means that there should be a standard that the performance of a merging unit can be assessed against. Determine if the criteria set within the standard will help improve the transient response of the device. It was identified as part of this project that the transient behaviour of a device is not a typically tested.

The assessment of the interoperability of different manufacturers merging units in a protection scheme that is dependent on a minimum of two merging units i.e. differential scheme.

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Appendix A: Project specification

ENG4111 / ENG4112 – Research Project
Project Specification by Luke Napier
Student Number: 0050065124

Topic:

Develop Process Bus Architecture for integrating sampled value IEDs

Supervisor:
Tony Ahfock

Sponsor:
Ergon Energy

Project Aim
The purpose of the project is to investigate the theoretical performance of measurement systems based on Sampled Values

Programme

ISSUE A: 19th March 2014

1. Research the performance criteria of primary and secondary systems for exist standards and devices.
2. Develop a theoretical model of a Current Transformer and the operation of an IED. Perform test to confirm theoretical model.
3. Analyse the market availability of devices that employ Sampled Value measurement interfaces
4. Assess the functionality of the available devices against performance of the existing devices.
5. Develop a new architecture for the implementation of sampled values into a standard Ergon Energy substation.
6. Deconstruct new architecture into building blocks for application into existing substations
7. Submit an academic dissertation on the research.

As Time Permits:

1. Undertake performance testing of the new hardware.

Appendix B: Chapter 3 Availability Calculations

Component Information

Protection IED (PIED): $MTBF_{PIED} := 100yr$ $MTTR_{PIED} := 12hr$ $A_{PIED} := \frac{MTBF_{PIED}}{MTBF_{PIED} + MTTR_{PIED}}$

Merging Unit (MU): $MTBF_{MU} := 150yr$ $MTTR_{MU} := 12hr$ $A_{MU} := \frac{MTBF_{MU}}{MTBF_{MU} + MTTR_{MU}}$

Ethernet Switch (ES): $MTBF_{ES} := 50yr$ $MTTR_{ES} := 12hr$ $A_{ES} := \frac{MTBF_{ES}}{MTBF_{ES} + MTTR_{ES}}$

DC Power System (UPS): $MTBF_{UPS} := 35yr$ $MTTR_{UPS} := 12hr$ $A_{UPS} := \frac{MTBF_{UPS}}{MTBF_{UPS} + MTTR_{UPS}}$

DC Cables (DCC): $MTBF_{DCC} := 150yr$ $MTTR_{DCC} := 12hr$ $A_{DCC} := \frac{MTBF_{DCC}}{MTBF_{DCC} + MTTR_{DCC}}$

Optic Fibre Cables (OFC): $MTBF_{OFC} := 150yr$ $MTTR_{OFC} := 12hr$ $A_{OFC} := \frac{MTBF_{OFC}}{MTBF_{OFC} + MTTR_{OFC}}$

RedBox (RED): $MTBF_{RED} := 135yr$ $MTTR_{RED} := 12hr$ $A_{RED} := \frac{MTBF_{RED}}{MTBF_{RED} + MTTR_{RED}}$

11kV Feeder Bay Existing System Availaibility

$$A_{11existing} := \left[A_{DCC}^{2} \cdot \left[1 - \left(1 - A_{DCC}\right)^{2}\right] \cdot A_{PIED}\right] \cdot 100$$

$A_{11existing} = 99.996805833$

11kV Feeder Bay New System Availaibility

$$A_{11new} := \left[A_{MU}\left[1 - \left[1 - \left(A_{OFC} \cdot A_{MU}\right)\right]^{2}\right] \cdot A_{OFC}^{3} \cdot A_{PIED} \cdot A_{ES}^{2}\right] \cdot 100$$

$A_{11new} = 99.9895053$

Redundancy Process Bus System 1

$$A_{sys1} := \left[A_{MU}\left[1 - \left[1 - \left(A_{OFC} \cdot A_{MU}\right)\right]^{2}\right] \cdot A_{OFC}^{2} \cdot \left[1 - \left[1 - \left(A_{OFC} \cdot A_{PIED}\right)\right]^{2}\right] \cdot A_{ES}^{2}\right] \cdot 100$$

$A_{sys1} = 99.991786612$

Redundancy Process Bus System 2

$$A_{sys2} := \left[\left[1 - \left[1 - \left(A_{OFC} \cdot A_{MU}\right)\right]^{2}\right]^{2} \cdot A_{OFC} \cdot \left[1 - \left[1 - \left(A_{OFC} \cdot A_{PIED}\right)\right]^{2}\right] \cdot A_{ES}^{2}\right] \cdot 100$$

$A_{sys2} = 99.99361171$

Redundancy Process Bus System 3

VT signal communcition path availability to to the first ethernet switches

$$A_{VT} := 1 - \left[1 - \left[1 - \left(A_{OFC} \cdot A_{MU}\right)\right]^2\right]^2$$

$$A_{sys3} := \left[\left[1 - \left[1 - \left(A_{OFC}^{3} \cdot A_{ES}\right)\right]^2\right] \cdot A_{MU} \cdot A_{VT} \cdot A_{PIED}\right] \cdot 100$$

$A_{sys3} = 99.997718149$

Redundancy Process Bus System 4

$$A_{sys4} := \left[A_{MU} \cdot \left[1 - \left[1 - \left(A_{OFC}^{3} \cdot A_{ES}\right)\right]^2\right] \cdot \left[1 - \left(1 - A_{PIED}\right)^2\right]\right] \cdot 100$$

$A_{sys4} = 99.999087053$

Redundancy Process Bus System 5

$i := 1 .. 5$ $\quad$ ORIGIN $:= 1$

$n_i :=$

0
1
2
3
4

$$A_{sys5_i} := \left[A_{MU} \cdot \left[1 - \left(1 - A_{OFC}\right)^2\right]^2 \cdot \left[1 - \left[1 - \left(A_{MU}^{n_i} \cdot A_{OFC}^{n_i}\right)\right]^2\right] \cdot A_{RED}^{2} \cdot A_{OFC} \cdot \left[1 - \left[1 - \left(A_{PIED}^{n_i} \cdot A_{OFC}^{n_i}\right)\right]^2\right] \cdot A_{PIED}\right] \cdot 100$$

$A_{sys5_i} =$

99.994777839
99.994777754
99.994777498
99.994777071
99.994776474

Redundancy Process Bus System 6

$$A_{s6_i} := \left[A_{MU} \cdot \left[1 - \left(1 - A_{OFC}\right)^2\right]^2 \cdot \left[1 - \left[1 - \left(A_{MU}^{n_i} \cdot A_{OFC}^{n_i}\right)\right]^2\right] \cdot \left[1 - \left[1 - \left(A_{RED}^{2} \cdot A_{OFC}\right)\right]^2\right] \cdot \left[1 - \left[1 - \left(A_{PIED}^{n_i} \cdot A_{OFC}^{n_i}\right)\right]^2\right] \cdot A_{PIED}\right] \cdot 100$$

$A_{s6_i} =$

99.997718345
99.99771826
99.997718004
99.997717577
99.99771698

$$A_{s6b_i} := \left[A_{MU} \cdot \left[1 - \left(1 - A_{OFC}\right)^2\right]^2 \cdot \left[1 - \left[1 - \left(A_{MU}^{n_i} \cdot A_{OFC}^{n_i}\right)\right]^2\right] \cdot \left[1 - \left[1 - \left(A_{RED}^{2} \cdot A_{OFC}\right)\right]^2\right] \cdot \left[1 - \left[1 - \left(A_{PIED}^{n_i} \cdot A_{OFC}^{n_i}\right)\right]^2\right] \cdot \left[1 - \left[1 - \left(A_{PIED}\right)\right]^2\right]\right]$$

$A_{s6b_i} =$

99.99908725
99.999087165
99.999086909
99.999086482
99.999085884

Redundancy Process Bus System 7

$$A_{s7_i} := \left[A_{MU} \left[1 - \left(1 - A_{OFC}^{n_i+3} \cdot A_{ES} \cdot A_{RED} \cdot A_{PIED}^{n_i} \right)^2 \right] \cdot A_{PIED} \right] \cdot 100$$

$A_{s7_i} =$

99.997718027
99.997717679
99.997717227
99.997716671
99.99771601

$$A_{sys7b_i} := \left[A_{MU} \left[1 - \left(1 - A_{OFC}^{n_i+3} \cdot A_{ES} \cdot A_{RED} \cdot A_{MU}^{n_i} \right)^2 \right] \cdot A_{PIED} \right] \cdot 100$$

$A_{sys7b_i} =$

99.997718027
99.997717757
99.99771742
99.997717017
99.997716547

Sensitivity Anlysis

$Iterations := 10000$

$PlusError_{MU} := 0\%$ $\quad MinusError_{MU} := 0\%$

$PlusError_{ES} := 0\%$ $\quad MinusError_{ES} := 0\%$

$PlusError_{OFC} := 0\%$ $\quad MinusError_{OFC} := 0\%$

$$MTBF_{MUmax} := 150 \cdot (1 + PlusError_{MU})\,yr \qquad MTBF_{ESmax} := 50(1 + PlusError_{ES}) \cdot yr \qquad MTBF_{OFCmax} := 150 \cdot (1 + PlusError_{OFC})\,yr$$

$$A_{MUmax} := \frac{MTBF_{MUmax}}{MTBF_{MUmax} + MTTR_{MU}} \qquad A_{ESmax} := \frac{MTBF_{ESmax}}{MTBF_{ESmax} + MTTR_{ES}} \qquad A_{OFCmax} := \frac{MTBF_{OFCmax}}{MTBF_{OFCmax} + MTTR_{OFC}}$$

Senstivity of the MTBF for the merging unit

$Probability :=$ for $p \in 1 .. 100$

- $mn \leftarrow 0$
- $MinusError_{MU} \leftarrow \frac{p}{100}$
- $MTBF_{MUmin} \leftarrow MTBF_{MU} \cdot (1 - MinusError_{MU})$
- $A_{MUmin} \leftarrow \frac{MTBF_{MUmin}}{MTBF_{MUmin} + MTTR_{MU}}$
- $A_{MUran} \leftarrow runif(Iterations, A_{MUmin}, A_{MUmax})$
- for $n \in 1 .. Iterations$
  - $A_{sys} \leftarrow \left[\left[1 - \left[1 - \left[(A_{OFC})^3 \cdot (A_{ES}) \right] \right]^2 \right] \cdot A_{MUran_n} \cdot A_{PIED} \right] \cdot 100$
  - $A_{sys} \leftarrow round(A_{sys}, 4)$
  - $A_{11existing} \leftarrow round(A_{11existing}, 4)$
  - $mn \leftarrow mn + 1$ if $A_{sys} \geq A_{11existing} - 0.0001$
- $Prob_p \leftarrow \frac{mn}{Iterations} \cdot 100$

$t \leftarrow Prob$

Senstivity of the MTBF for the Ethernet Switch

$$
\begin{aligned}
&\text{Probability} := \text{for } p \in 1..100 \\
&\quad mn \leftarrow 0 \\
&\quad \text{MinusError}_{ES} \leftarrow \frac{p}{100} \\
&\quad \text{MTBF}_{ESmin} \leftarrow \text{MTBF}_{ES} \cdot \left(1 - \text{MinusError}_{ES}\right) \\
&\quad A_{ESmin} \leftarrow \frac{\text{MTBF}_{ESmin}}{\text{MTBF}_{ESmin} + \text{MTTR}_{ES}} \\
&\quad A_{ESran} \leftarrow \text{runif}\left(\text{Iterations}, A_{ESmin}, A_{ES}\right) \\
&\quad \text{for } n \in 1..\text{Iterations} \\
&\quad\quad A_{sys} \leftarrow \left[\left[1 - \left[1 - \left[\left(A_{OFC}\right)^3 \cdot A_{ESran_n}\right]\right]^2\right] \cdot A_{MU} \cdot A_{PIED}\right] \cdot 100 \\
&\quad\quad A_{sys} \leftarrow \text{round}\left(A_{sys}, 4\right) \\
&\quad\quad A_{11existing} \leftarrow \text{round}\left(A_{11existing}, 4\right) \\
&\quad\quad mn \leftarrow mn + 1 \quad \text{if } A_{sys} \geq A_{11existing} - 0.0001 \\
&\quad \text{Prob}_p \leftarrow \frac{mn}{\text{Iterations}} \cdot 100 \\
&t \leftarrow \text{Prob}
\end{aligned}
$$

Senstivity of the MTBF for the Fibre optic cable

$$
\begin{aligned}
&\text{Probability} := \text{for } p \in 1..100 \\
&\quad mn \leftarrow 0 \\
&\quad \text{MinusError}_{OFC} \leftarrow \frac{p}{100} \\
&\quad \text{MTBF}_{OFCmin} \leftarrow \text{MTBF}_{OFC} \cdot \left(1 - \text{MinusError}_{OFC}\right) \\
&\quad A_{OFCmin} \leftarrow \frac{\text{MTBF}_{OFCmin}}{\text{MTBF}_{OFCmin} + \text{MTTR}_{OFC}} \\
&\quad A_{OFCran} \leftarrow \text{runif}\left(\text{Iterations}, A_{OFCmin}, A_{OFC}\right) \\
&\quad \text{for } n \in 1..\text{Iterations} \\
&\quad\quad A_{sys} \leftarrow \left[\left[1 - \left[1 - \left[\left(A_{OFCran_n}\right)^3 \cdot A_{ES}\right]\right]^2\right] \cdot A_{MU} \cdot A_{PIED}\right] \cdot 100 \\
&\quad\quad A_{sys} \leftarrow \text{round}\left(A_{sys}, 4\right) \\
&\quad\quad A_{11existing} \leftarrow \text{round}\left(A_{11existing}, 4\right) \\
&\quad\quad mn \leftarrow mn + 1 \quad \text{if } A_{sys} \geq A_{11existing} - 0.0001 \\
&\quad \text{Prob}_p \leftarrow \frac{mn}{\text{Iterations}} \cdot 100 \\
&t \leftarrow \text{Prob}
\end{aligned}
$$

Onoomba Substation

LV Feeder Main protection - CT & VT control cable

$LVFdr := A_{DCC}^{2} \cdot A_{PIED} = 0.999968058$

LV Bus Main protection inc CB fail relay

$LVHZD_{Bus1} := A_{DCC}^{6} \cdot A_{PIED}^{2}$, $LVHZD_{Bus2} := A_{DCC}^{6} \cdot A_{PIED}$, $LVHZD_{Bus3} := A_{DCC}^{6} \cdot A_{PIED}^{2} = 0.999917867$

LV Feeder and Bus Backup protection

$SOC := A_{DCC}^{2} \cdot A_{PIED}$

Transformer Main protection

$DiffM := A_{DCC}^{3} \cdot A_{PIED}$

Transformer Backup protection

$DiffB := A_{DCC}^{3} \cdot A_{PIED}$

HV Bus Main protection

$HVHZDM := A_{DCC}^{4} \cdot A_{PIED}$

HV Bus Backup protection

$HVHZDB := A_{DCC}^{4} \cdot A_{PIED}$

HV Feeder Main protection

$HVFdrM := A_{DCC}^{2} \cdot A_{PIED}$

HV Feeder Main protection

$HVFdrB := A_{DCC}^{2} \cdot A_{PIED}$

LV Bus 1 Reduction

$LVBus_1 := \left[1 - \left[1 - \left(LVFdr^{3} \cdot LVHZD_{Bus1}\right)\right] \cdot (1 - SOC)\right] = 0.999999994$

LV Bus 2 Reduction

$LVBus_2 := \left[1 - \left[1 - \left(LVFdr^{4} \cdot LVHZD_{Bus2}\right)\right] \cdot (1 - SOC)\right] = 0.999999994$

LV Bus 3 Reduction

$LVBus_3 := \left[1 - \left[1 - \left(LVFdr^{3} \cdot LVHZD_{Bus3}\right)\right] \cdot (1 - SOC)\right] = 0.999999994$

Transformer 1 Reduction

$Trans_1 := 1 - \left[(1 - DiffM) \cdot (1 - DiffB)\right] = 0.999999998$

Transformer 2 Reduction

$Trans_2 := 1 - \left[(1 - DiffM) \cdot (1 - DiffB)\right] = 0.999999998$

HV Bus Reduction

$HVBus := 1 - \left[(1 - HVHZDM) \cdot (1 - HVHZDB)\right] = 0.999999997$

HV Feeder 1 Reduction

$HVFdr_1 := 1 - \left[(1 - HVFdrM) \cdot (1 - HVFdrB)\right] = 0.999999999$

HV Feeder 2 Reduction

$HVFdr_2 := 1 - \left[(1 - HVFdrM) \cdot (1 - HVFdrB)\right] = 0.999999999$

$A_{con} := (LVBus_1 \cdot LVBus_2 \cdot LVBus_3 \cdot Trans_1 \cdot Trans_2 \cdot HVBus \cdot HVFdr_1 \cdot HVFdr_2) \cdot 100$

$A_{con} = 99.999997443$

Ultimate Process Bus 1 System Availaibility

The availability has been brken into subsystems which start with the IED and ends at each switch. These subsystem incorporate redundnacy of the ethernet switches. To solve for each subsystem the availability of the the IEDS and communcation paths are done seperately and then combined.

Subsystem - Switch 1

$$A_{IEDSW1} := \left[1 - \left[\left(1 - A_{PIED}{}^{4}\right)\cdot\left(1 - A_{PIED}\right)\right]\right]$$

$$A_{COMSW1} := \left[1 - \left[\left(1 - A_{OFC}{}^{4}\right)\cdot\left(1 - A_{OFC}\right)\right]\right]\cdot A_{ES}$$

$$A_{SW1} := A_{IEDSW1}\cdot\left[1 - \left[\left(1 - A_{COMSW1}\right)^{2}\right]\right] = 0.999999999$$

Subsystem - Switch 2

$$A_{IEDSW2} := \left[1 - \left[\left(1 - A_{PIED}{}^{5}\right)\cdot\left(1 - A_{PIED}\right)\right]\right]$$

$$A_{COMSW2} := \left[1 - \left[\left(1 - A_{OFC}{}^{5}\right)\cdot\left(1 - A_{OFC}\right)\right]\right]\cdot A_{ES}$$

$$A_{SW2} := A_{IEDSW2}\cdot\left[1 - \left[\left(1 - A_{COMSW2}\right)^{2}\right]\right] = 0.999999998$$

Subsystem - Switch 3

$$A_{IEDSW3} := \left[1 - \left[\left(1 - A_{PIED}{}^{4}\right)\cdot\left(1 - A_{PIED}\right)\right]\right]$$

$$A_{COMSW3} := \left[1 - \left[\left(1 - A_{OFC}{}^{4}\right)\cdot\left(1 - A_{OFC}\right)\right]\right]\cdot A_{ES}$$

$$A_{SW3} := A_{IEDSW3}\cdot\left[1 - \left[\left(1 - A_{COMSW3}\right)^{2}\right]\right] = 0.999999999$$

Subsystem - Switch 4

$$A_{IEDSW4} := \left[1 - \left[\left(1 - A_{PIED}\right)^{2}\right]\right]^{3}$$

$$A_{COMSW4} := \left[1 - \left[\left(1 - A_{OFC}\right)^{2}\right]\right]^{3}\cdot A_{ES}$$

$$A_{SW4} := A_{IEDSW4}\cdot\left[1 - \left[\left(1 - A_{COMSW4}\right)^{2}\right]\right] = 0.999999999$$

Subsystem - Switch 5

$$A_{IEDSW5} := \left[1 - \left[\left(1 - A_{PIED}\right)^{2}\right]\right]^{2}$$

$$A_{COMSW5} := \left[1 - \left[\left(1 - A_{OFC}\right)^{2}\right]\right]^{2}\cdot A_{ES}$$

$$A_{SW5} := A_{IEDSW5}\cdot\left[1 - \left[\left(1 - A_{COMSW5}\right)^{2}\right]\right] = 0.999999999$$

Subsystem - Commmuncation network connect between switches

$$A_{COMNET} := \left[1 - \left[\left(1 - A_{OFC}\right)^{2}\right]\right]^{12} = 0.999999999$$

Subsystem - Switch 6

$$A_{IEDSW6} := \left[1 - \left[\left(1 - A_{MU}{}^{4}\right)\cdot\left(1 - A_{MU}\right)\right]\right]\cdot\left[1 - \left[\left(1 - A_{MU}\right)^{2}\right]\right]$$

$$A_{COMSW6} := \left[1 - \left[\left(1 - A_{OFC}{}^{4}\right)\cdot\left(1 - A_{OFC}\right)\right]\right]\cdot\left[1 - \left[\left(1 - A_{OFC}\right)^{2}\right]\right]\cdot A_{OFC}{}^{3}\cdot A_{ES}$$

$$A_{SW6} := A_{IEDSW6}\cdot\left[1 - \left[\left(1 - A_{COMSW6}\right)^{2}\right]\right] = 0.999999997$$

Subsystem - Switch 7

$$A_{IEDSW7} := \left[1 - \left[\left(1 - A_{MU}{}^{4}\right)\cdot\left(1 - A_{MU}\right)\right]\right]\cdot\left[1 - \left[\left(1 - A_{MU}\right)^{2}\right]\right]$$

$$A_{COMSW7} := \left[1 - \left[\left(1 - A_{OFC}{}^{6}\right)\cdot\left(1 - A_{OFC}{}^{2}\right)\right]\right]\cdot A_{ES}$$

$$A_{SW7} := A_{IEDSW7}\cdot\left[1 - \left[\left(1 - A_{COMSW7}\right)^{2}\right]\right] = 0.999999999$$

Subsystem - Switch 8

$$A_{IEDSW8} := \left[1 - \left[\left(1 - A_{MU}{}^{4}\right)\cdot\left(1 - A_{MU}\right)\right]\right]\cdot\left[1 - \left[\left(1 - A_{MU}\right)^{2}\right]\right]$$

$$A_{COMSW8} := \left[1 - \left[\left(1 - A_{OFC}{}^{4}\right)\cdot\left(1 - A_{OFC}\right)\right]\right]\cdot\left[1 - \left[\left(1 - A_{OFC}\right)^{2}\right]\right]\cdot A_{OFC}{}^{3}\cdot A_{ES}$$

$$A_{SW8} := A_{IEDSW8}\cdot\left[1 - \left[\left(1 - A_{COMSW8}\right)^{2}\right]\right] = 0.999999997$$

Subsystem - Switch 9

$$A_{IEDSW9} := \left[1 - \left[\left(1 - A_{MU}\right)^{2}\right]\right]^{2}$$

$$A_{COMSW9} := \left[1 - \left[\left(1 - A_{OFC}\right)^{2}\right]\right]^{2}\cdot A_{ES}$$

$$A_{SW9} := A_{IEDSW9}\cdot\left[1 - \left[\left(1 - A_{COMSW9}\right)^{2}\right]\right]$$

Subsystem - Switch 10

$$A_{IEDSW10} := \left[1 - \left[\left(1 - A_{MU}\right)^2\right]\right]^2$$

$$A_{COMSW10} := \left[1 - \left[\left(1 - A_{OFC}\right)^2\right]\right]^2 \cdot A_{ES}$$

$$A_{SW10} := A_{IEDSW9} \cdot \left[1 - \left[\left(1 - A_{COMSW9}\right)^2\right]\right]$$

Therefore the ultimate process bus system is fully operational when all the the subsystems are functioning.

$$A_{Processbus1} := \left(A_{SW1} \cdot A_{SW2} \cdot A_{SW3} \cdot A_{SW4} \cdot A_{SW5} \cdot A_{SW6} \cdot A_{SW7} \cdot A_{SW8} \cdot A_{SW9} \cdot A_{SW10} \cdot A_{COMNET}\right) \cdot 100$$

$$A_{Processbus1} = 99.999998205$$

Ultimate Process Bus 2 System Availaibility

Subsystem - Switch 1

$$A_{IEDSW12} := A_{PIED}^{7}$$

$$A_{COMSW12} := \left[1 - \left[\left(1 - A_{OFC}^{7}\right)^2\right]\right] \cdot A_{ES}$$

$$A_{SW12} := A_{IEDSW12} \cdot \left[1 - \left[\left(1 - A_{COMSW12}\right)^2\right]\right] = 0.999904178$$

Subsystem - Switch 2

$$A_{IEDSW22} := A_{PIED}^{5}$$

$$A_{COMSW22} := \left[1 - \left[\left(1 - A_{OFC}^{5}\right)^2\right]\right] \cdot A_{ES}$$

$$A_{SW22} := A_{IEDSW22} \cdot \left[1 - \left[\left(1 - A_{COMSW22}\right)^2\right]\right] = 0.999931554$$

Subsystem - Switch 3

$$A_{IEDSW32} := A_{PIED}^{6}$$

$$A_{COMSW32} := \left[1 - \left[\left(1 - A_{OFC}^{6}\right)^2\right]\right] \cdot A_{ES}$$

$$A_{SW32} := A_{IEDSW32} \cdot \left[1 - \left[\left(1 - A_{COMSW32}\right)^2\right]\right] = 0.999917866$$

Subsystem - Commmuncation network connect between switches

$$A_{COMNET2} := \left[1 - \left[\left(1 - A_{OFC}\right)^2\right]\right]^9 = 0.999999999$$

Subsystem - Switch 4

$$A_{IEDSW42} := A_{PIED}^{8}$$

$$A_{COMSW42} := \left[1 - \left[\left(1 - A_{OFC}^{8}\right)^2\right]\right] \cdot A_{ES}$$

$$A_{SW42} := A_{IEDSW42} \cdot \left[1 - \left[\left(1 - A_{COMSW42}\right)^2\right]\right] = 0.99989049$$

Subsystem - Switch 5

$$A_{IEDSW52} := A_{MU}^{7}$$

$$A_{COMSW52} := \left[1 - \left[\left(1 - A_{OFC}^{7}\right)^2\right]\right] \cdot A_{ES}$$

$$A_{SW52} := A_{IEDSW52} \cdot \left[1 - \left[\left(1 - A_{COMSW52}\right)^2\right]\right] = 0.999936117$$

Subsystem - Switch 6

$$A_{IEDSW62} := A_{MU}^{6}$$

$$A_{COMSW62} := \left[1 - \left[\left(1 - A_{OFC}^{6}\right)^2\right]\right] \cdot A_{ES}$$

$$A_{SW62} := A_{IEDSW62} \cdot \left[1 - \left[\left(1 - A_{COMSW62}\right)^2\right]\right] = 0.999945243$$

Subsystem - Switch 7

$$A_{IEDSW72} := A_{MU}^{7}$$

$$A_{COMSW72} := \left[1 - \left[\left(1 - A_{OFC}^{7}\right)^2\right]\right] \cdot A_{ES}$$

$$A_{SW72} := A_{IEDSW72} \cdot \left[1 - \left[\left(1 - A_{COMSW72}\right)^2\right]\right] = 0.999936117$$

Subsystem - Switch 8

$$A_{IEDSW82} := A_{MU}^{10}$$

$$A_{COMSW82} := \left[1 - \left[\left(1 - A_{OFC}^{10}\right)^2\right]\right] \cdot A_{ES}$$

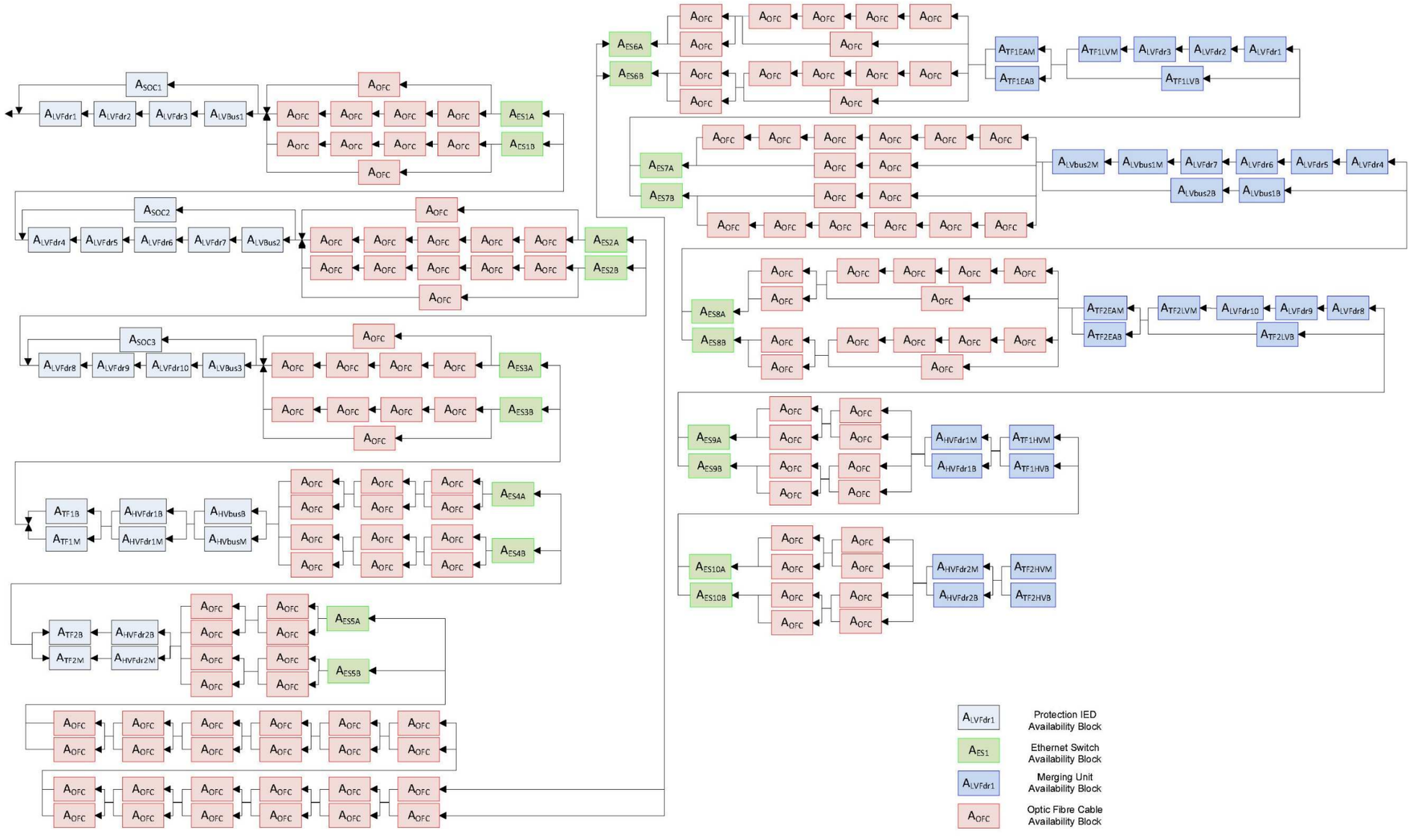
$$A_{SW82} := A_{IEDSW82} \cdot \left[1 - \left[\left(1 - A_{COMSW82}\right)^2\right]\right] = 0.99990874$$

The availbililty of the process bus architecture has switch 4 & 8 in parallel to the other switches. Therefore the availbility of the second process bus system is:

$$A_{Processbus2} := \left[1 - \left(1 - A_{SW12} \cdot A_{SW22} \cdot A_{SW32} \cdot A_{SW52} \cdot A_{SW62} \cdot A_{SW72} \cdot A_{COMNET2}\right) \cdot \left(1 - A_{SW42} \cdot A_{SW82}\right)\right] \cdot 100$$

$$A_{Processbus2} = 99.99999139$$

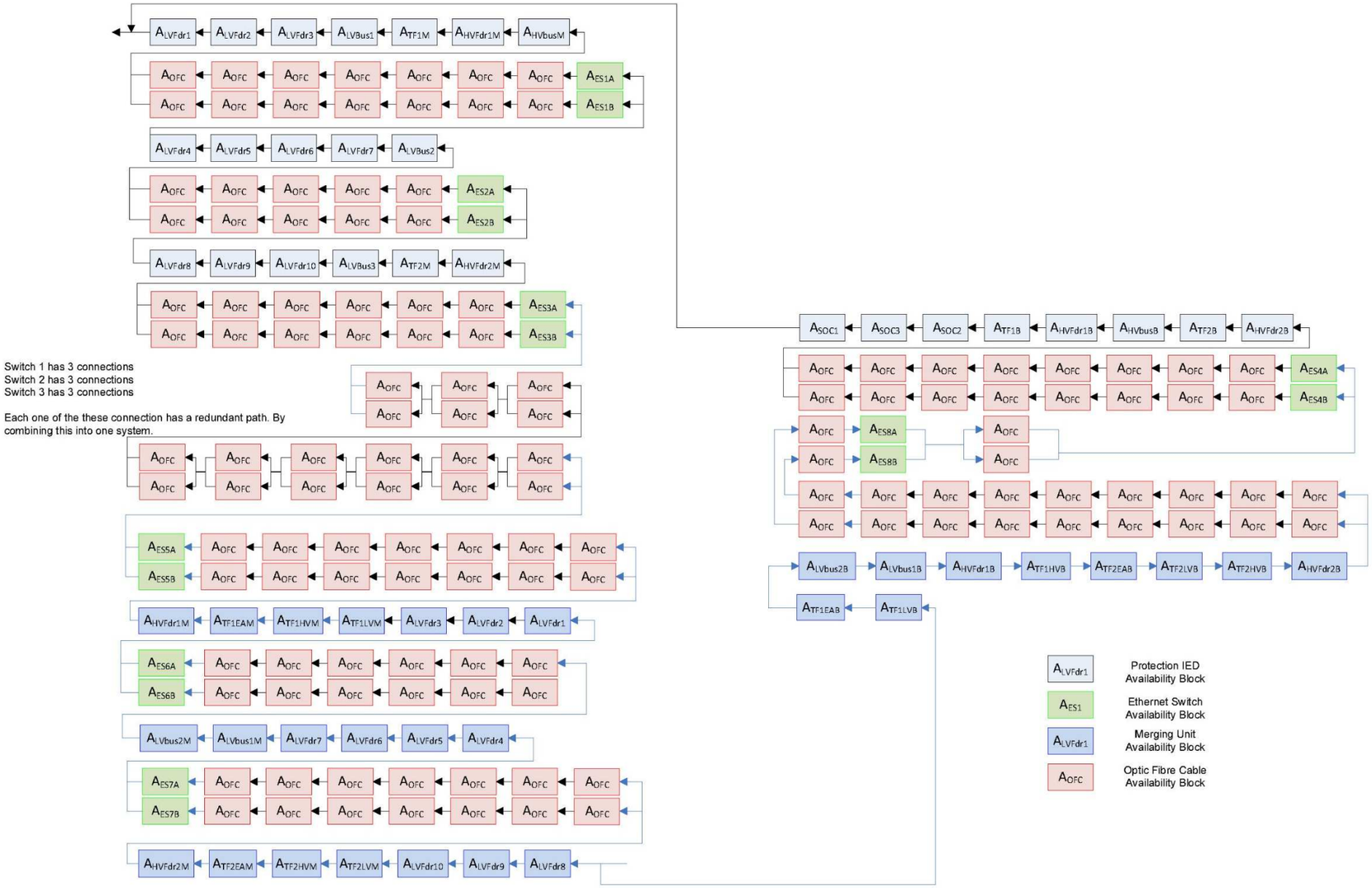
Appendix C: Availability Block Diagram for Section 0



Switch 1 has 3 connections
Switch 2 has 2 connections
Switch 3 has 2 connections
Switch 4 has 3 connections
Switch 5 has 2 connections

Each one of the these connection has a redundant path. By combining this into one system.

Appendix D: Availability Block Diagram for Section 3.3.2.3



Appendix E: VBA Code for Sampled Data Conversion

```
Sub Import()

    Dim DataString, Packet_Preamble, EtherType As String
    Dim svID As String
    Dim MU1_Hex As String
    Dim smpCnt, ACurMag, BCurMag, CCurMag, NCurMag, AVolMag, BVolMag, CVolMag, NVolMag As Long
    Dim arr() As String
    Dim INDEX As Integer
    Dim RowCount, NumberofLines, CurrentLine As Double
    Dim OutArray(10) As Long
' Define the parameters of the standard parts of the packet
    Packet_Preamble = "|0   "
    EtherType = "|88|ba"
    svID = "a2"
    RowCount = 2
' Clear the contents of any previously imported data
    Sheets("MU_1").Select
    Cells.Select
    Selection.ClearContents
' Reset the column headings
    Range("A1").Select
    ActiveSheet.Range("A1") = "Logical Node"
    ActiveSheet.Range("B1") = "Sample Count"
    ActiveSheet.Range("C1") = "A-Phase Current (A)"
    ActiveSheet.Range("D1") = "B-Phase Current (A)"
    ActiveSheet.Range("E1") = "C-Phase Current (A)"
    ActiveSheet.Range("F1") = "Neutral Current (A)"
    ActiveSheet.Range("G1") = "A-Phase Voltage (V)"
    ActiveSheet.Range("H1") = "B-Phase Voltage (V)"
    ActiveSheet.Range("I1") = "C-Phase Voltage (V)"
    ActiveSheet.Range("J1") = "Neutral Voltage (V)"
' Retrieve text file
    MsgBox "Please retreive the K12 Text File"
    Fname = Application.GetOpenFilename()
    If Fname = "False" Then Exit Sub
' Count the number of lines in the text file
    NumberofLines = 0
    Open Fname For Input As #2
    While Not EOF(2)
        Input #2, DataString
        NumberofLines = NumberofLines + 1
    Wend
    Close #2
    MsgBox Format(NumberofLines, "#,###") & " number of lines to process", vbOKOnly, "Data Import"
```

```
' Import text file content for Sampled value data
    Open Fname For Input As #1
    Sheets("MU_1").Activate
    While Not EOF(1)
        Input #1, DataString

        If InStr(DataString, EtherType) > 0 Then ' Check to see if the Ether type for a SV is in the string
            arr() = Split(DataString, "|") ' This will split the string into the two hexadecimal numbers and
                                           ' create an array
            INDEX = Application.Match(svID, arr, False) + 4 ' This will look for the column with fixed bits
                                                            ' for the reference the umber of columns to the
                                                            ' information needed
            svIDLength = CLng("&H" & arr(INDEX)) ' Determine the number for the number of characters in the svID
            MU1_Hex = "" ' Clear out MU1_Hex before use
            For i = 1 To svIDLength
                MU1_Hex = MU1_Hex & Chr("&H" & arr(INDEX + i))
            Next i
            INDEX = INDEX + svIDLength + 3
            smpCnt = CLng("&H" & (arr(INDEX) & arr(INDEX + 1)))
            OutArray(0) = smpCnt
            INDEX = INDEX + svIDLength
            ACurMag = CLng("&H" & (arr(INDEX) & arr(INDEX + 1) & arr(INDEX + 2) & arr(INDEX + 3)))
            OutArray(1) = ACurMag / 1000
            INDEX = INDEX + 8
            BCurMag = CLng("&H" & (arr(INDEX) & arr(INDEX + 1) & arr(INDEX + 2) & arr(INDEX + 3)))
            OutArray(2) = BCurMag / 1000
            INDEX = INDEX + 8
            CCurMag = CLng("&H" & (arr(INDEX) & arr(INDEX + 1) & arr(INDEX + 2) & arr(INDEX + 3)))
            OutArray(3) = CCurMag / 1000
            INDEX = INDEX + 8
            NCurMag = CLng("&H" & (arr(INDEX) & arr(INDEX + 1) & arr(INDEX + 2) & arr(INDEX + 3)))
            OutArray(4) = NCurMag / 1000
            INDEX = INDEX + 8
            AVolMag = CLng("&H" & (arr(INDEX) & arr(INDEX + 1) & arr(INDEX + 2) & arr(INDEX + 3)))
            OutArray(5) = AVolMag / 1000
            INDEX = INDEX + 8
            BVolMag = CLng("&H" & (arr(INDEX) & arr(INDEX + 1) & arr(INDEX + 2) & arr(INDEX + 3)))
            OutArray(6) = BVolMag / 1000
            INDEX = INDEX + 8
            CVolMag = CLng("&H" & (arr(INDEX) & arr(INDEX + 1) & arr(INDEX + 2) & arr(INDEX + 3)))
            OutArray(7) = CVolMag / 1000
            INDEX = INDEX + 8
            NVolMag = CLng("&H" & (arr(INDEX) & arr(INDEX + 1) & arr(INDEX + 2) & arr(INDEX + 3)))
            OutArray(8) = NVolMag / 1000


    Wend
    Close #1

' Unload ProgressForm
    MsgBox "Finished", vbInformation, "Done"

End Sub
```

Appendix F: Test Plan Connection Diagrams

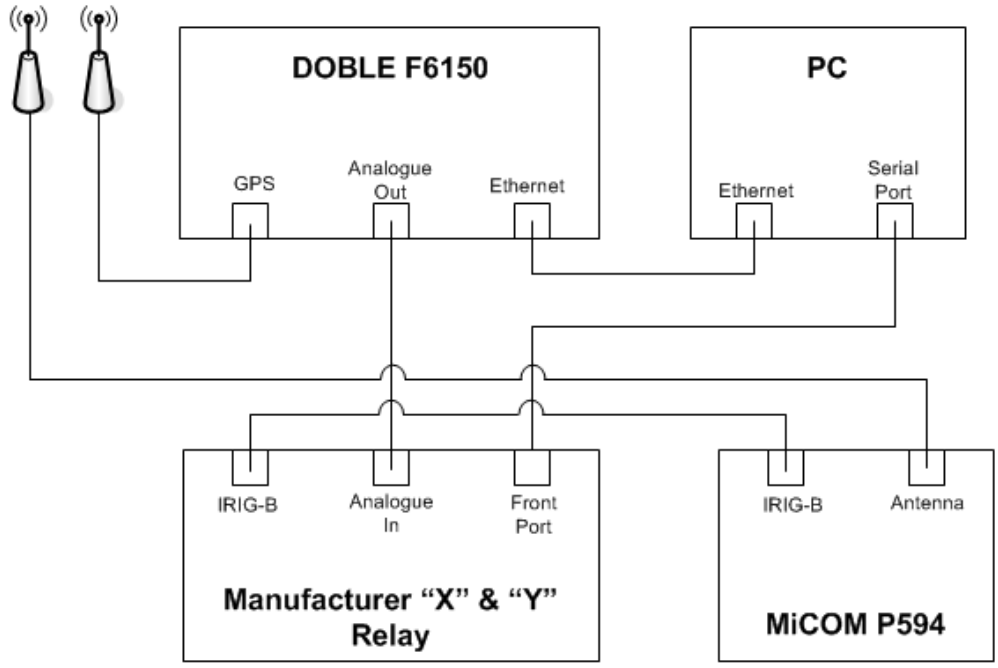


Figure 73 – Conventional Relay Base test connection diagram

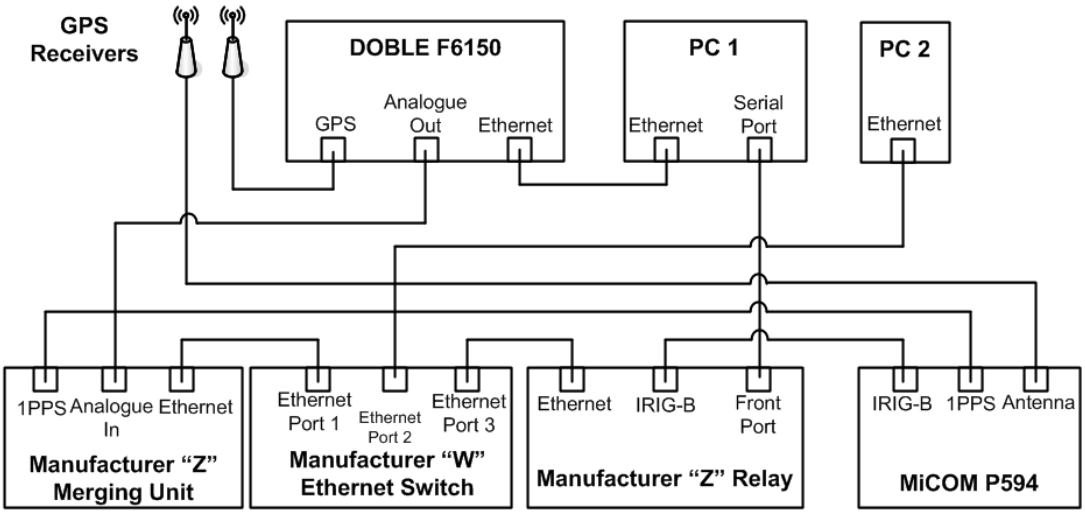


Figure 74 – Process Bus Devices including an Ethernet Switch test connection diagram

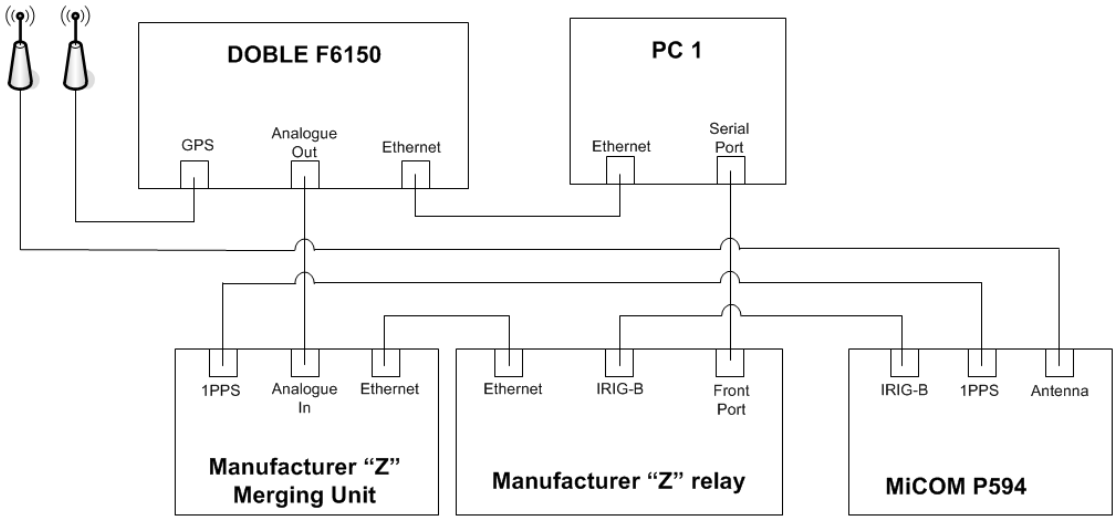


Figure 75 – Process Bus devices excluding an Ethernet switch test connection diagram

Process Bus Relay Test

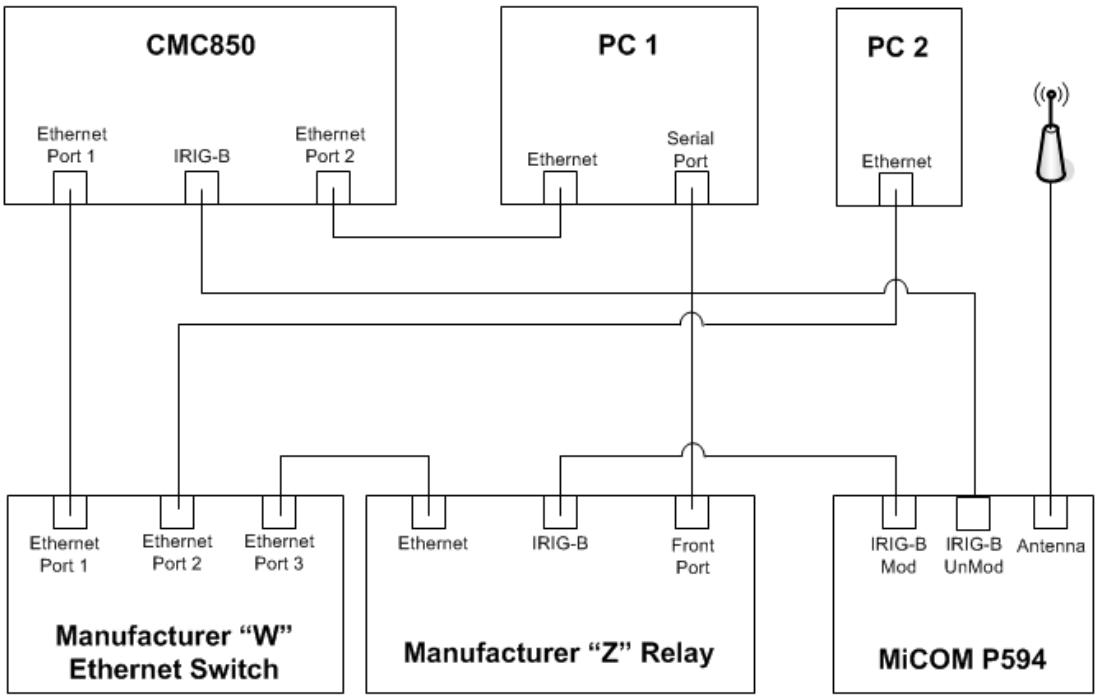


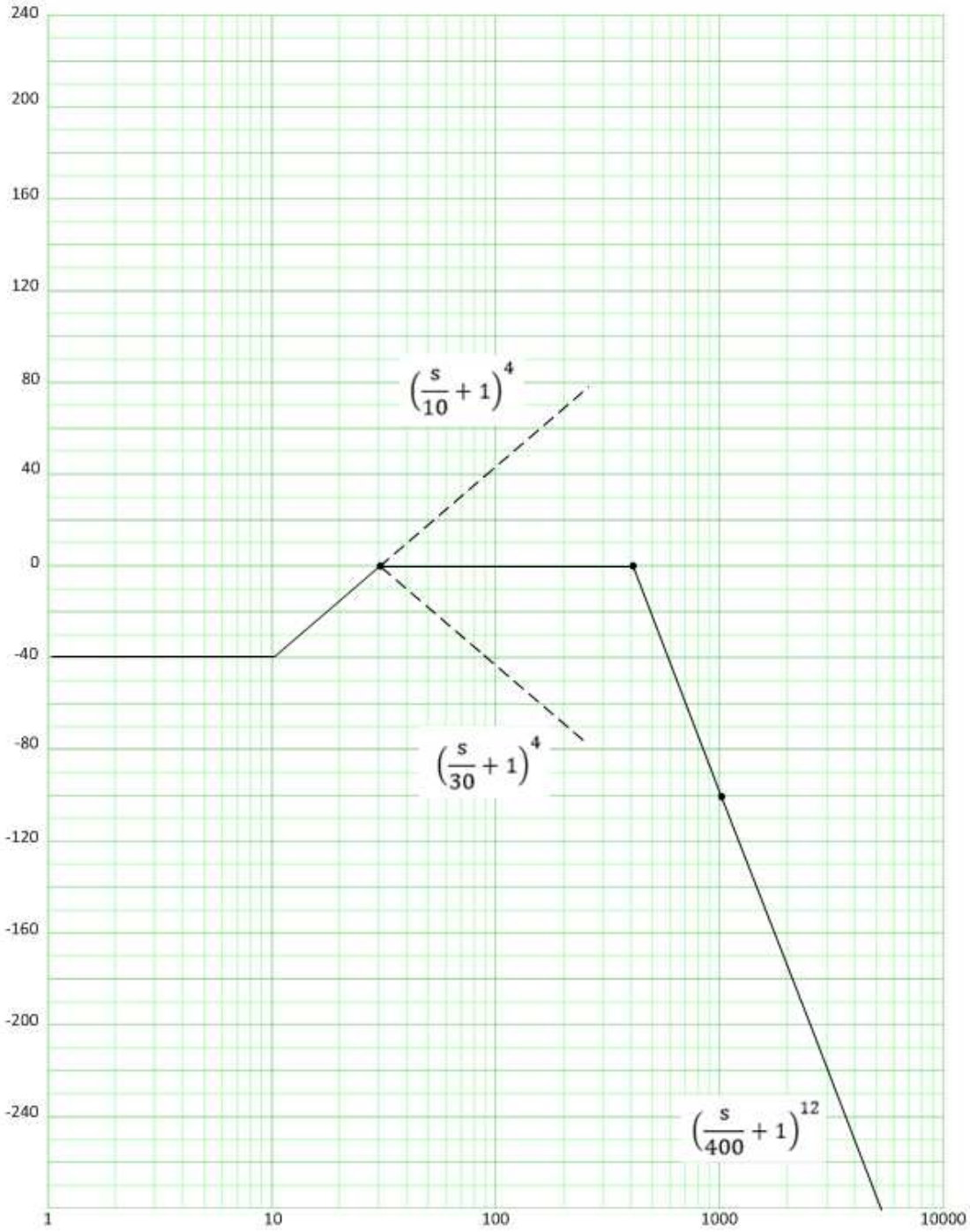
Figure 76 – Process Bus relay test connection diagram

Appendix G: Current Transformer MATLAB® Model

```
%                   Current Transformer Model
%
%% REFRESH MATLAB AND CLEAN BEFORE RUNNING THE ANALYSIS
clear;
close all;
clc;
%% General System parameters
F = 50; % Network frequency (Hz)
%% Current Transformer's Parameters
Vs = 228; % Knee point Voltage at the given ratio
S = 22; % This is the inverse of the slope of the saturated part of
        % the ie vs Vs curve
ALF = 20; % Accuracy limit factor. This factor is applied to
          % the rated secondary current to stay within the percentage
          % accuracy
Ipri = 200; % Primary current rating of the CT
Isec = 1; % Secondary current rating of the CT
VArat = 11; % Secondary burden rating when using a 'P' class CT
CE = 5; % Percentage Error when at the limits
Rw = 0.4; % Secondary winding resistance at the given CT ratio
Rb = 0; % Secondary burden resistance
Xb = 0; % Secondary burden impedance
%% Fault conditions
XoverR = 10; % This is the network X/R ratio
Ip = 25000; % Symmetrical Fault current RMS value
fluxRem = 0; % Remanent Flux
%% Calculated values
Rt = Rw+Rb; % Total burden resistance
omega = 2*pi*F; % Rotational frequency
Tau1 = XoverR/omega; % Primary system time constant
Lb = Xb/omega; % Burden's inductance
Lamsat = sqrt(2)*Vs/omega; % Peak Flux linkages corresponding to
                           % secondary voltage
%% Determine the magnetising RMS to peak ratio by using a form factor
%  calculation
angle2=0;
 for k = 1:1:100;
     angle1=angle2;
     angle2=angle1+(pi/200);
     Angle(k,:)=(angle2); % Sets the array of the k*e(k) for summing
 end
sineS = sin(Angle).^(S*2);
sineSlast=sineS(end);
sineS1 = sineS(1:end-1);
RP = sqrt((sum(sineS1)+sineSlast/2)/100);
%% Determine the secondary current corresponding to saturation
Is = ALF*Isec*CE/100;
%% Determine the coefficient in instantaneous ie vs lambda
A = (Is*omega^S)/((sqrt(2)*Vs)^S*RP);
```

```
%% CT Signal
dt = 0.00001;
m = 0;
T1 = 0;
Lambda = 0.0001;
for T = 0:dt:0.32 % This is time of analysis
    m = m+1; % This used to establish the row number for the column
             % vector
    T1 (m,:) = T;
    isideal = sqrt(2)*Ip/Ipri*(exp(-T/Tau1)-cos(omega*T)); % Determine
                                    % the Primary current at the given
    isidealv(m,:)=isideal; % Save each value for the primary current
                           % at each time interval
    disdt = sqrt(2)*Ip/Ipri*(-1/Tau1*exp(-T/Tau1)+omega*sin(omega*T));
    ie = A*sign(Lambda)*(abs(Lambda)^S); % Excitation current
    iev(m,:)=ie; % Save each value for the excitation current at each
                 % time interval
    Deltalambda = ((Rt*isideal+Lb*disdt-Rt*ie)*dt)…
                                        /(1+Lb*S*A*abs(Lambda)^(S-1));
                                        % Change in flux linkage due
                                         % to change in secondary
                                         % voltage change
    Deltalambdav(m,:)= Deltalambda; % Save each value for the change
                                    % of flux linkage at each time
                                    % interval
    Lambda = Lambda + Deltalambda; % The new vlaue for the flux
                                   % linkage
    Lambdav(m,:) = Lambda;
    i2(m,:) = isideal - ie; % Actual secondary current through the
                            % burden
    end
```

Appendix H: Frequency Response Bode Plot



Appendix I: Risk Assessment

This project consists of predominately-theoretical assessment of the topic. To prove the theoretical models there is a minor amount of laboratory work required. The laboratory is located within Ergon Energy's facilities therefore appropriate procedures are to be followed.

Although the laboratory is located within a typical office, there are still hazards that can occur in this type of workplace. These hazards are typically assigned to "Slips, Trips and Falls". The fore mentioned hazards are evident with the test lab due to the use of external leads required to connect between test equipment and the equipment being tested.

The other hazard present within the lab is electrical shock. The test device use is one that injects current in the order of tens of amps. This hazard has the potential to injure a person.

The two hazards identified above can be assessed for their risk. The assessment use a standard three by three matrix determine the level of risk each hazard poses. The assessment has been conducted with the know methods in place. For example appropriate training, PPE can reduce the likelihood of the consequence. Figure 77 below shows the matrix that has been used to assess the risks.

Consequence ↓	Likelihood →	Rare	Possible	Almost Certain
Catastrophic		MEDIUM	HIGH	HIGH
Moderate		LOW	MEDIUM	HIGH
Insignificant		LOW	LOW	MEDIUM

Figure 77 – 3x3 Risk Matric

From the matrix above for the Slips, trips and falls hazard the consequence is "Insignificant". The reason for this is that if this were to occur it would worst cause some minor medical treatment i.e. for sprained ankle. The likelihood would be "Possible", in some cases it is not possible to eliminate obstacles therefore increasing the likelihood. This has resulted in a Low risk score.

The electric shock hazard has been assessed to have a consequence of "Moderate". This is due to the seriousness of receiving an electric shock. The likelihood of this occurring is "Rare", the test devices are designed to that if it detects a resistance above a certain threshold it does not function. The leads used to connect between devices are fully insulted with very little opportunity to expose live parts. This has resulted in a Low risk score.

The primary focus of this project is the development of the system architecture that is to implemented into the safety system of a medium voltage substation. The reproduction of the resultant architecture into a live substation can influence the safety of the system. The consequence that such a system fails to operate correctly is “Catastrophic” due to possibility of serious injury to the public. The likelihood is “Possible” as it requires the primary system to be faulty and the new architecture to failure concurrently. This has resulted in a High-risk score. However full implementation of such a system based on this project would still require significant design and testing before full serviceability is achieved.