Monte Carlo analysis of the dynamic behavior of InAlAs/InGaAs velocity modulation transistors: a geometrical optimization

B. G. Vasallo*, T. González, D. Pardo, and J. Mateos

Universidad de Salamanca, Plaza de la Merced, s/n, 37008, Salamanca.

*e-mail: bgvasallo@usal.es

***Abstract*—The influence of the geometry on the dynamic behavior of InAlAs/InGaAs Velocity Modulation Transistors (VMTs) is analized by means of a Monte Carlo simulator in order to optimize the performance of this new type of transistor. In VMTs, based on the topology of a Double-Gate High Electron Mobility Transistor (DG-HEMT), the source and drain electrodes are connected by two channels with different mobilities, and electrons are transferred between both of them by changing the gate voltages in differential mode. Consequently, the drain current is modulated while keeping the total carrier density constant, thus in principle avoiding capacitance charging/dis-charging delays. However, the low values taken by the transconductance, as well as the high capacitance between the two gates in differential-mode operation, lead to a deficient dynamic performance. This behavior can be geometrically optimized by increasing the mobility difference between the two channels, by increasing the channel width and, mainly, by reducing the gate length, with a higher immunity to short channel effects than the traditional architectures.**

Index Terms—Monte Carlo simulations, HEMTs, Velocity Modulation Transistor

I. INTRODUCTION

III-V High Electron Mobility Transistors have shown an excellent performance for high-frequency operation [1]. To further improve their behavior, alternative solutions based on an evolution of the standard HEMT design have been proposed, as the Double-Gate (DG) HEMT, a HEMT with two gates placed on each side of the conducting InGaAs channel [2-6]. The progress of the DG-HEMT technology has allowed the design and fabrication of III-V Velocity Modulation Transistors (VMTs) [7,8]. In VMTs [7-15], the conducting channel is divided in two regions, a high-mobility (high-μ) undoped channel and a low-μ channel obtained by compensated doping (N_A=N_D), with two (top and bottom) gates controlling the electron density. Carriers are transferred between the two channels by changing the gate voltages (V_{G1} and V_{G2}) in differential mode (DM), in which a potential $\pm V_{GDIFF}/2$ is added to a bias voltage V_{GOFF} which adjusts the total channel electron concentration ($V_{GDIFF}=V_{G1}-V_{G2}$). Thus, the drain current I_D is modulated while keeping constant the total carrier density, and it is in principle possible to overcome the transit-time limit for high-frequency applications. However, the dynamic behavior of the VMT is not as exceptional as expected [9] due to the low values of the transconductance g_m, and mainly due to the high capacitance between both gates C_{g1g2} [8]. In contrast, this device does not follow the traditional scaling rules for standard FETs and provides a high immunity to short-channel effects [8].

In this work, an optimization of the geometry of recessed short-channel InAlAs/InGaAs VMTs is performed by means of an *ensemble* 2D Monte Carlo (MC) simulator self-consistently coupled with a 2D Poisson solver [16]. This model, which has provided a full microscopic interpretation of its dynamic performance [8], allows a geometrical optimization of VMTs in order to achieve optimal operation frequencies.

II. PHYSICAL MODEL

The validity of the semiclassical MC model used for the simulation of VMTs has been proved for standard [16] and DG [5,6] HEMTs by reproducing their experimental static and dynamic behavior. This technique has been also successfully applied to the study of the static and dynamic behavior of a fabricated VMT [7,8].

The topology of the simulated VMT, similar to that of the fabricated transistors, is sketched in Fig. 1(a). The active layer structure and the technological process for the fabrication were detailed in Ref. 7. Two opposite gate electrodes control the total electron density in the channels as well as the carrier shift between them in DM operation. The only difference with respect to a DG-HEMT [2-6] is that the channel is divided into two regions: a high-μ undoped channel and a low-μ channel with compensated doping. The compensated-doping allows increasing the ionized impurity scattering and thus decreasing the electron mobility. Initially, we analyze a VMT in which the gate length is L_g=100 nm, the channel width d_C=40 nm, and $N_A+N_D=10^{19}$ cm^{-3}. Then, similar structures with different geometrical parameters are studied.

Since the small signal equivalent circuit of VMTs in DM operation is not well established,,in order to carry out the analysis of the dynamic behavior of VMTs an input capacitance C_{IN} is defined as $\mathrm{Im}[Y_{11}]/2\pi f$, being $Y_{11}=\Delta I_{IN}/\Delta V_{IN}$ when V_{DS} remains constant, and f the operation frequency. C_{IN} can be generally considered as the addition of the gate-to-source C_{gs}, gate-to-drain C_{gd} and gate1-to-gate2 C_{g1g2} capacitances. When working in DM, C_{gs} and C_{gd} are practically zero, since the amount of electrons under the gate remains practically constant and there is no need for channel charging/discharging, so that C_{IN} is nearly C_{g1g2}. The cut-off frequency f_C can therefore be calculated as $g_m/2\pi C_{IN}$.

III. RESULTS

Fig. 2 presents the intrinsic MC output characteristics of a VMT with L_g=100 nm,

N_A+N_D=10^{19} cm^{-3}, and L_C=40 nm: (a) I_D–V_{DS} for V_{GDIFF}=0 V (common-mode CM operation), and (b) I_D–V_{GDIFF} for V_{DS} = 0.5 V (DM), for different values of V_{GOFF}. While in CM [Fig. 2(a)] the VMT works as a classic FET device (specifically as a DG-HEMT [2-6]), in differential-mode operation the values taken by I_D depend on V_{GDIFF} due to the velocity-modulation effect: when increasing V_{GDIFF} the electron density is transferred from the low-μ to the high-μ channel, thus increasing the drain current. MC profiles of electron concentration and mean velocity in both high-μ and low-μ channels for different biasings demonstrate the velocity-modulation operation of the proposed transistor [7,8]. Concerning the dynamic performance of the 100 nm-gate device, MC results show that the cutoff frequencies take values much lower than predicted [9] (the maximum value of f_C estimated with the MC model is of the order of 200 GHz for a geometry similar to that of the experimental device [8]) because of the low g_m associated to the VM behavior and, remarkably, to the high geometrical capacitance existing between the two gate electrodes when operating in DM, which is the main contribution to C_{IN} [7,8]. To improve the frequency operation, the VMT geometry must be optimized for an enhanced g_m and reduced C_{IN}.

g_m can be improved by increasing the difference in electron velocity between both channels, which can be achieved by rising the compensated doping N_A+N_D. Fig. 3 presents the MC values of (a) g_m, C_{IN}, and (b) f_C, as a function of N_A +N_D for V_{GDIFF}=0 V, V_{DS}=0.5 V and V_{GOFF} providing the maximum value of f_C. As expected, g_m is improved when increasing N_A+N_D, while C_{IN} remains almost constant. However, for a value of N_A+N_D=5×10^{19} cm^{-3}, μ in the low-μ channel is so small (~840 cm^2/Vs) that a further rise in the value of the compensated doping does not lead to an improvement in f_C. On the contrary, it degrades the charge transfer between channels (lower value in g_m).

In order to diminish C_{IN}, the distance between the gate electrodes must be increased,

for example, by enlarging the channel width d_C. Fig. 4 presents the MC intrinsic results for different values of d_C, showing that a wider channel provides also an improvement in the value of g_m, i.e., a better control on the transfer of electrons between channels. Nevertheless, the improvement of g_m and f_C saturates for a value of about d_C=80 nm.

Finally, in Fig. 5 we show that the most appropriate way to reduce C_{IN} is shortening the gate length L_g. A shorter L_g does not lead to a reduction of g_m (neither to an increase as for traditional FETs), while the value of C_{IN} decreases and thus f_C is remarkably enhanced. As a consequence, because of the different scaling rules of the VMT and the immunity to short-channel effects of the DG architecture [5], the limit for attaining high frequencies of operation comes from the technological difficulties met to achieve a perfect alignment of both gates of so small length.

IV. Conclusions

In this work we have analyzed, by means of a 2D ensemble MC simulator, an InAlAs/InGaAs short-channel VMT based on the DG-HEMT topology. By changing the gate voltages in differential mode, electrons are shifted between two channels with significantly different mobilities. The low values taken by g_m, as well as the high capacitance between the gates C_{g1g2} in DM operation, leads to a deficient dynamic behavior. However, the cutoff frequency of VMTs can be increased by rising the compensated doping N_A+N_D and by enlarging the distance between the gate electrodes. However, given the immunity to short-channel effects of the DG architecture, the most appropriate way to reduce C_{IN} without lowering g_m (thus enhancing f_C) is shortening the gate length L_g.

Acknowledgments

This work has been partially supported by the European Commission through the ROOTHz Project ICT-2009-243845, by the Dirección General de Investigación (MEC)

and FEDER through Project TEC2007-61259/MIC and by the Consejería de Educación, Junta de Castilla y León through Projects SA019A08 and GR270.

REFERENCES

[1] S. Tiwari, *Compound Semiconductor Device Physics*, New York: Academic (1992).

[2] N. Wichmann, I. Duszynski, X. Wallart, S. Bollaert, A. Cappy, *IEEE Electron. Device Lett.* **25**, 354 (2004).

[3] N. Wichmann, I. Duszynski, S. Bollaert, J. Mateos, X. Wallart, A. Cappy, *in IEDM Tech Dig.,* p. 1023 (2004)

[4] N. Wichmann, I. Duszynski, X. Wallart, S. Bollaert, A. Cappy, *IEEE Electron. Device Lett.* **26**, 601 (2005).

[5] B. G. Vasallo, N. Wichmann, S. Bollaert, Y. Roelens, A. Cappy, T. González, D. Pardo, J. Mateos, *IEEE Trans. Electron Dev.* **54**, 2815 (2007).

[6] B. G. Vasallo, N. Wichmann, S. Bollaert, Y. Roelens, A. Cappy, T. González, D. Pardo, J. Mateos, *IEEE Trans. Electron Dev.* **55,** 1535 (2008).

[7] N. Wichmann, B. G. Vasallo, S. Bollaert, Y. Roelens, X. Wallart, A. Cappy, T. González, D. Pardo, J. Mateos, *Appl. Phys. Lett.* **94**, 103504 (1-3) (2009).

[8] B. G. Vasallo, N. Wichmann, S. Bollaert, Y. Roelens, A. Cappy, T. González, D. Pardo, J. Mateos, *IEEE Trans. Electron Dev.* (to be published).

[9] H. Sakaki, *Jpn. J. Appl. Phys.* **21**, L381 (1982).

[10] K. Hirakawa, H,. Sakaki, J. Yoshino, *Phys. Rev. Lett*. **54**, 1279 (1985).

[11] K. Maezawa, T. Mizutani, M. Tomizawa, *Jpn. J. Appl. Phys.* **31**, 757 (1992).

[12] K. Maezawa, T. Mizutani, *IEEE Trans. Electron Devices* **39**, 2438 (1992).

[13] K. J. Webb, E, B, Cohen, M. R. Melloch, *IEEE Trans. Electron Devices* **48**, 2701 (2001).

[14] M. Prunnila, J. Ahopelto, K. Henttinen, F. Gamiz, *Appl. Phys. Lett.* **85**, 5442 (2004).

[15] C. Sampedro, F. Gamiz, A. Godoy, M. Prunnila, J. Ahopelto, *Appl. Phys. Lett.* **86**, 202115 (1-3) (2004).

[16] J. Mateos, T. González, D. Pardo, V. Hoël, A. Cappy, *IEEE Trans. Electron Devices* **47**, 1950 (2000).

FIGURE CAPTIONS

Fig. 1. Schematic topology of the VMT under analysis.

Fig. 2. MC (a) I_D–V_{DS} for V_{GDIFF}=0 V and (b) I_D–V_{GDIFF} for V_{DS}=0.5 V. V_{GOFF} is –0.1 V for the top curves, and the potential step is ΔV_{GOFF}=0.1 V. L_g=100 nm, d_C=40 nm and N_A+ N_D=10^{19} cm^{-3}.

Fig. 3. Intrinsic MC values of (a) g_m and C_{IN}, and (b) f_C as a function of N_A+N_D, for V_{GDIFF}=0 V, V_{DS}=0.5 V and V_{GOFF} providing the maximum of f_C. L_g=100 nm and d_C=40 nm.

Fig. 4. Intrinsic MC values of (a) g_m and C_{IN}, and (b) f_C as a function of d_C, for V_{GDIFF}=0 V, V_{DS}=0.5 V, and V_{GOFF} providing the maximum of f_C. L_g=100 nm and N_A+ N_D=10^{19} cm^{-3}.

Fig. 5. Intrinsic MC values of (a) g_m and C_{IN}, and (b) f_C as a function of L_g, for V_{GDIFF}=0 V, V_{DS}=0.5 V, and V_{GOFF} providing the maximum of f_C. d_C=40 nm and N_A+ N_D=10^{19} cm^{-3}.

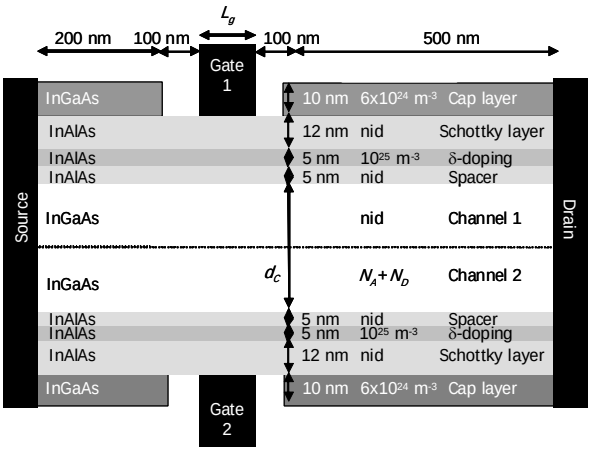

Fig. 1. Schematic topology of the VMT under analysis.

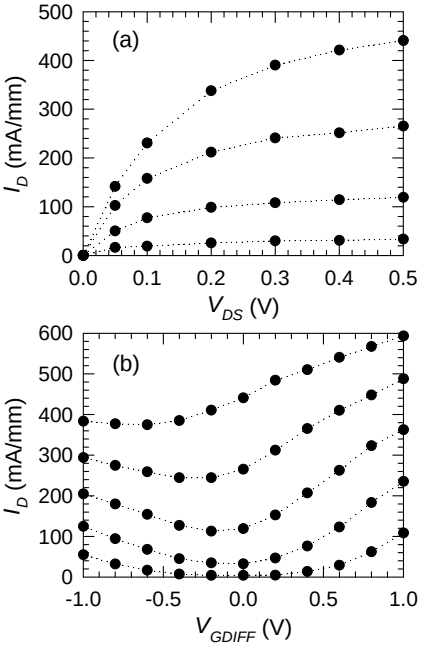

Fig. 2. MC (a) I_D–V_{DS} for V_{GDIFF}=0 V and (b) I_D–V_{GDIFF} for V_{DS}=0.5 V. V_{GOFF} is –0.1 V for the top curves, and the potential step is ΔV_{GOFF}=0.1 V. L_g=100 nm, d_C=40 nm and N_A+ N_D=10^{19} cm^{-3}.

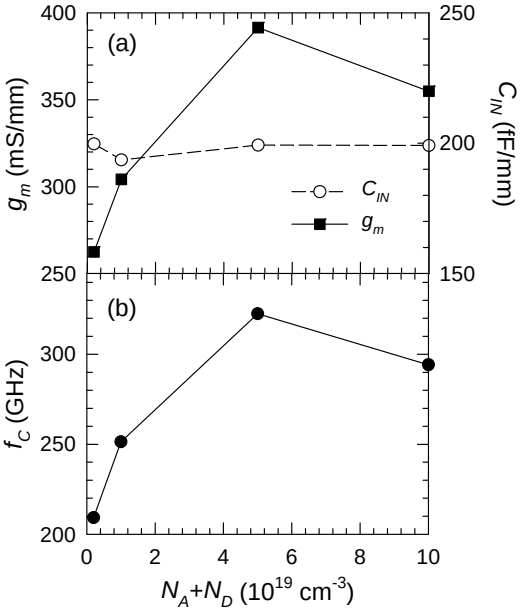

Fig. 3. Intrinsic MC values of (a) g_m and C_{IN}, and (b) f_C as a function of N_A+N_D, for V_{GDIFF}=0 V, V_{DS}=0.5 V and V_{GOFF} providing the maximum of f_C. L_g=100 nm and d_C=40 nm.

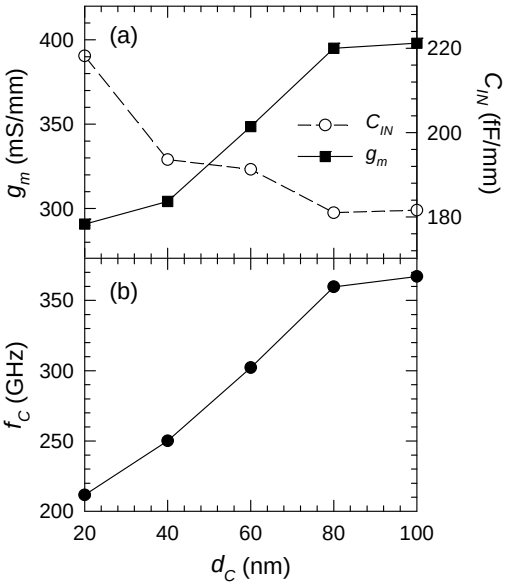

Fig. 4. Intrinsic MC values of (a) g_m and C_{IN}, and (b) f_C as a function of d_C, for V_{GDIFF}=0 V, V_{DS}=0.5 V, and V_{GOFF} providing the maximum of f_C. L_g=100 nm and N_A+ N_D=10^{19} cm^{-3}.

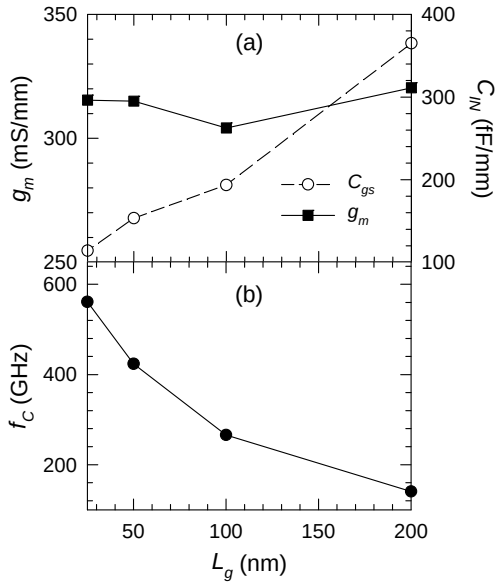

Fig. 5. Intrinsic MC values of (a) g_m and C_{IN}, and (b) f_C as a function of L_g, for V_{GDIFF}=0 V, V_{DS}=0.5 V, and V_{GOFF} providing the maximum of f_C. d_C=40 nm and N_A+ N_D=10^{19} cm^{-3}.