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Design Techniques for Low-power SAR ADCs in Nano-scale CMOS Technologies

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Dedicated to my parents and my wife.

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Design Techniques for Low-power SAR ADCs in Nano-scale CMOS Technologies

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This thesis presents low power design techniques for successive approximation register (SAR) analog-to-digital converters (ADCs) in nano-scale CMOS technologies. Low power SAR ADCs face two major challenges especially at high resolutions: (1) increased comparator power to suppress the noise, and (2) increased DAC switching energy due to the large DAC size. To improve the comparator's power efficiency, a statistical estimation based comparator noise reduction technique is presented. It allows a low power and noisy comparator to achieve high signal-to-noise ratio (SNR) by estimating the conversion residue. A first prototype ADC in 65nm CMOS has been developed to validate the proposed noise reduction technique. It achieves 4.5 fJ/conv-step Walden figure of merit and 64.5 dB signal-to-noise and distortion ratio (SNDR). In addition, a bidirectional single-side switching technique is developed to reduce the DAC switching power. It can reduce the DAC switching power and the total number of unit capacitors by 86% and 75%, respectively. A second prototype ADC with the proposed switching technique is

designed and fabricated in 180nm CMOS technology. It achieves an SNDR of 63.4 dB and consumes only 24 μW at 1MS/s, leading to a Walden figure of merit of 19.9 fJ/conv-step.

This thesis also presents an improved loop-unrolled SAR ADC, which works at high frequency with reduced SAR logic power and delay. It employs the bidirectional single-side switching technique to reduce the comparator common-mode voltage variation. In addition, it uses a V_{cm}-adaptive offset calibration technique which can accurately calibrate comparator's offset at its operating V_{cm}. A prototype ADC designed in 40nm CMOS achieves 35 dB at 700 MS/s sampling rate and consumes only 0.95 mW, leading to a Walden figure of merit of 30 fJ/conv-step.

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Chapter 1

Introduction

1.1 Motivation

The Internet of Things (IoT) is attracting lots of attention from semiconductor industry. It is changing the way how people control their surroundings and environments. In order to provide multiple functions at low cost, a typical IoT system-on-a-chip (SoC) commonly integrates sensor interfaces, analog-to-digital converters (ADCs), local digital processor, embedded memory and multi-protocol wireless transceivers. The integration of ADCs with adequate performance is critical in any IoT SoCs. Since many sensor interfaces and ADCs are battery-powered, low power operation becomes paramount.

Successive approximation register (SAR) ADC is a popular choice due to its simple architecture and short development cycle. It is more digital friendly and does not require any opamps compared to pipeline ADCs or sigma-delta ADCs. SAR ADC can achieve excellent power efficiency of less than one femtojoule (fJ)/conv-step at low resolution with a target effective number of bits (ENOB) below 10 bits. This can be visualized from Fig. 1.1, which shows the Walden figure of merit (FOM) versus the corresponding signal to noise and distortion ration (SNDR) for recently published SAR ADCs in ISSCC and VLSI conferences. The data for the

figure is taken from the survey made available by Dr. Boris Murmann (`http://web.stanford.edu/~murmann/adcsurvey.html`). However, some wireless sensor nodes and biomedical devices [Verma and Chandrakasan [2007]; Van Helleputte et al. [2012]] require low power ADCs with resolution greater than 10 bits. It is nontrivial to maintain such good power efficiency when extending the ENOB beyond 10 bits due to two design challenges. First, designing a low power comparator with low noise is a main challenge since traditional analog scaling requires four times the comparator power for every 1-bit reduction in noise. This places a steep power-noise trade-off. The second challenge for a high-resolution SAR ADC is its exponentially growing capacitive DAC size, which results in greatly increased DAC switching power. Thus, it is highly desirable to develop power efficient techniques to reduce comparator noise and DAC switching power.

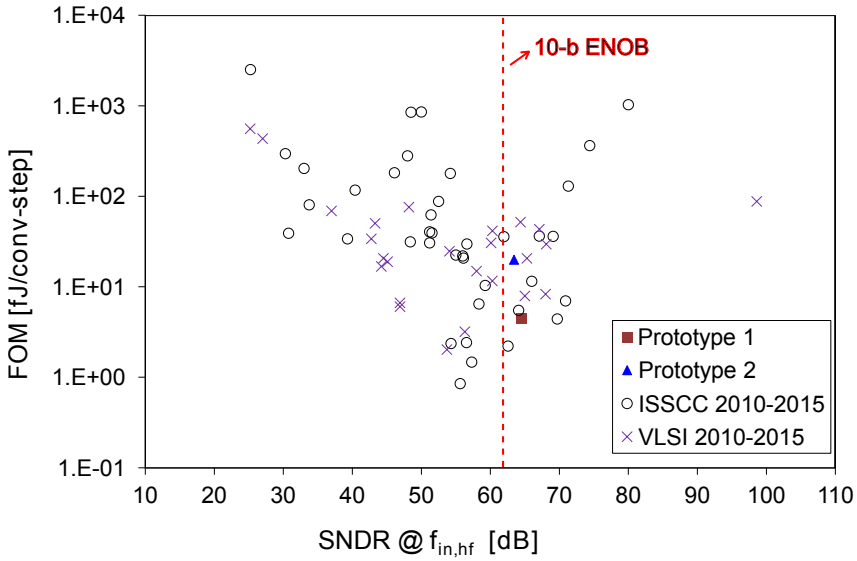

Figure 1.1: FOM versus SNDR plot for recently published SAR ADCs in ISSCC and VLSI conferences.

In this thesis, a statistical estimation based technique is presented which can efficiently reduce comparator noise for SAR ADCs. Instead of designing an accurate comparator with large power consumption, the proposed technique utilizes the low power and noisy comparator and estimates the conversion residue by firing the comparator multiple times for LSB bit comparison. The conversion residue can be estimated by exploring the repeated comparison results. The estimated residue is then subtracted from the ADC output to accurately represent the input. The key challenge here is to build an accurate estimator. It has been proved in statistics that the Bayes estimator achieves lowest estimation error. Thus, Bayes estimator is chosen for the prototype SAR ADC design. The prototype ADC 1 has been implemented in 65nm CMOS and measured in the lab. The measured FOM of the first prototype ADC is 4.5 fJ/conv-step with 64.5dB SNDR, shown in Fig. 1.1. It suits well for the low power applications with low conversion speed.

Another challenge for low power and high resolution SAR ADC design is to reduce the DAC switching energy. The DAC is commonly implemented with binary capacitors in SAR ADCs. To suppress the sampling kT/C noise and provide good matching accuracy in high resolution designs, the capacitive DAC needs to be large, leading to a significant power consumption out of total ADC power. This work proposes a bidirectional single-side switching (BSS) technique, which can save 86% DAC switching power compared to conventional switching technique. Moreover, the comparator input common mode variation is reduced in the technique compared to widely used monotonic switching technique [Liu et al. [2010a]]. The prototype ADC 2 with BSS switching technique is designed in 180nm CMOS. The

measured FOM is 19.9 fJ/conv-step with 63.4dB SNDR. It achieves the state-of-art power efficiency shown in Fig. 1.1, given its relatively old 180nm process.

Modern high speed serial link transceivers and communication systems employ high speed and low resolution ADCs. Although SAR ADC is simple and power efficient, it can not run at a high speed compared to flash ADCs and pipeline ADCs, mainly due to its serial conversion algorithm. This work investigates a loop-unrolled architecture with multiple comparators to increase the speed of SAR ADCs. The loop-unrolled architecture is based on the work of [Jiang et al. [2012]]. However, the linearity in [Jiang et al. [2012]] is not good due to large comparator offset mismatches. This work employs the BSS switching technique and a V_{cm}-adaptive calibration technique to effectively reduce the comparator offset mismatches and improve the linearity. A third prototype 6-bit loop-unrolled SAR ADC is implemented in 45nm CMOS and the measured SNDR is 34.8 dB at a sampling rate of 700 MS/s.

1.2 Organization

Chapter 2 of the thesis presents the low power SAR ADC with statistical estimation based noise reduction. It also includes the measurement results of the first prototype designed in 65nm CMOS technology. Chapter 3 presents the bidirectional single-side switching technique to reduce the DAC switching power. The measurement results for the second prototype designed in 180nm CMOS technology are also discussed. Chapter 4 presents the third 40nm high speed SAR ADC prototype with improved loop-unrolled architecture. The measured results are also

shown in Chapter 4. The conclusion is drawn in Chapter 5.

Chapter 2

Statistical Estimation Based Noise Reduction

This chapter[1] presents a power-efficient noise reduction technique for SAR ADCs based on the statistical estimation theory. It suppresses both comparator noise and quantization error by accurately estimating the ADC conversion residue. It allows a high SNR to be achieved with a noisy low-power comparator and a relatively low resolution DAC. The proposed technique has low hardware complexity, requiring no change to the standard ADC operation except for repeating the LSB comparisons. Three estimation schemes are studied and the optimal Bayes estimator is chosen for a prototype 11-bit ADC in 65nm CMOS. The measured SNR is improved by 7dB with the proposed noise reduction technique.

This chapter is organized as follows: an introduction of existing techniques is first presented. The basic idea of proposed noise reduction technique is studied next. Then the formulation is analyzed. Finally, a prototype ADC implementation is presented, followed by its measurement.

[1] This chapter is a partial reprint of the publication: Long Chen, Xiyuan Tang, Arindam Sanyal, Yeonam Yoon, Jie Cong, and Nan Sun, "A 10.5-b ENOB 645nW 100kS/s SAR ADC with statistical estimation based noise reduction," IEEE Custom Integrated Circuit Conference (CICC), 2015, pp. 1–4. I thank all the co-authors for their valuable advice in designing and testing of the prototype.

2.1 Introduction

Rapid advances in wireless sensor nodes and biomedical devices place demanding requirements on low power and high resolution analog-to-digital converters (ADCs) [Verma and Chandrakasan [2007]; Van Helleputte et al. [2012]]. Successive approximation register (SAR) ADC is a popular choice due to its simple architecture and short development cycle. It consists of only a capacitive DAC, a comparator, and a digital SAR logic. Since it is highly digital, it scales well with technology, and consumes both low power and low area in advanced CMOS processes. By using a low power but relatively noisy dynamic comparator, a SAR ADC does not consume any static current. As a result, it can achieve an excellent power efficiency of only a few femtojoule (fJ) per conversion step, especially at low resolution with a target effective number of bits (ENOB) below 10-bit [Tai et al. [2014a]; Harpe et al. [2014]]. Despite many advantages of SAR ADCs, it is nontrivial to design a high resolution SAR ADC and maintain a high power efficiency when extending the resolution beyond 10 bits. To reach higher signal-to-noise ratio (SNR), the comparator noise needs to be reduced. This can be accomplished by brute-force analog scaling, which is to increase the transistor sizes and power. However, this requires four times the comparator power for every 1-bit reduction in noise, which is a steep power-noise trade-off. The other challenge for a high-resolution SAR ADC is its exponentially growing capacitive DAC size, which results in greatly increased DAC power. In addition, it makes a SAR ADC hard to drive. Facing these challenges, it is highly desirable to develop a more efficient way to increase SAR ADC resolution without significantly increasing the comparator power and the DAC size.

There are several prior SAR ADC works that aim to reduce the comparator power and noise. The technique of [Giannini et al. [2008]] arranges two comparators with different noise and power levels. For a b-bit SAR ADC, it uses a low-power but high-noise comparator during the first $(b-1)$ MSB comparison cycles. To tolerate the resulting comparison errors due to the high noise, a redundant LSB bit is added. A high-power but low-noise comparator is used only for the LSB and the redundant bit. As a result, the overall ADC noise is almost the same as the case where the high-power low-noise comparator is used for every comparison cycle, but the total comparator power is greatly reduced. The limitation of this approach is that the offsets of the two comparators need to be tightly matched, which is non-trivial at high resolution. To address the offset mismatch issue, the majority voting technique is developed [Harpe et al. [2013]]. It uses only one low-power high-noise comparator. When low comparator noise is needed at critical decision point with a small comparator input voltage, the comparator is fired multiple times and the decision is made via majority voting. This technique does not have the comparator offset mismatch problem of [Giannini et al. [2008]], but it requires a carefully tuned metastability detector to sense the comparator input voltage, resulting in increased design complexity. Also, its conversion speed is reduced due to multiple comparisons needed. A similar technique using an optimized vote allocation is reported in [Ahmadi and Namgoong [2013]]. It obviates the need for a metastability detector, however, at the cost of further increased number of comparison cycles.

The majority voting technique of [Harpe et al. [2013]; Ahmadi and Namgoong [2013]] can effectively reduce the comparator noise and power, but they do

not make *full* use of the information embedded in the voting results. It only cares about whether there are more '1's or more '0's, and uses it only to make a 1-bit majority decision. It does not take advantage of the detailed distributions of '1's and '0's, but there is valuable information there that can be exploited. Let us consider an example that the comparator is fired in total 15 times at a given comparison cycle. Let us assume that there are two cases: one is that there are eight '1's and seven '0's, and the other is that there are fifteen '1's and no '0's. Since there are more '1's, there is no difference for majority voting, but there is extra information. The first case indicates that the comparator input is very close to 0, while the second case of fifteen straight '1's means that its comparator input is greater than zero by at least several comparator noise standard deviations. As will be shown later, this extra information can be used to reduce not only the comparator noise but also the quantization error set by the DAC resolution.

This chapter presents a statistical estimation based technique that can reduce both the comparator noise and the quantization error for SAR ADCs. Its circuit implementation is simple. It does not require any change to the standard SAR ADC operation except for repeating the last LSB comparison for multiple times [Chen et al. [2015]]. It exploits *all* the information embedded in the comparator output distribution, not just making a binary majority decision for the LSB bit as in [Harpe et al. [2013]; Ahmadi and Namgoong [2013]], but to estimate the magnitude of the comparator input voltage. A useful property of a SAR ADC is that the comparator input voltage is the ADC conversion residue. If we are able to estimate the residue, we can subtract it from the ADC output to increase the ADC resolution. Note that

this reduces not only the comparator noise, but also the quantization error, which is impossible with prior works [Giannini et al. [2008]; Harpe et al. [2013]; Ahmadi and Namgoong [2013]]. Although a '1'-bit high-noise comparator cannot provide an accurate estimation for its input if used only once, we can improve the estimation accuracy by repeating the comparison for multiple times and examining the number of comparator outputs being '1' or '0'. It turns out that the estimation of an unknown value via multiple noisy binary tests is a classic *statistical estimation problem* [Casella and Berger [1990]]. Thus, we can directly borrow the concepts and theories from *statistics* to solve our estimation problem. Specifically, this chapter discusses three widely used statistical estimators: the averaging based estimator, the maximum likelihood estimator (MLE), and the Bayes estimator. Out of them, the Bayes estimator achieves the lowest estimation error, and thus, is chosen for our proposed SAR ADC. Note that the estimator is essentially a mapping from the comparator output distribution to a digital estimate for the comparator input, which can be easily implemented using a pre-computed look-up table.

This chapter introduces the statistical estimation theory to the field of ADC design and offers a new perspective. In a broad sense, any form of analog-to-digital conversion, regardless of its architecture, can be considered as a statistical estimation problem, as its entire operation is to estimate (or convert) an unknown analog signal by performing a series of comparison tests. The theories from statistics are helpful when we deal with multiple noisy comparator outputs, as in our case. The concept of statistical estimation has been exploited in prior studies. For example, the stochastic flash ADC of [Weaver et al. [2010]] takes advantages of random off-

sets in an array of comparators to obtain a 6-bit estimation of its input. This idea has also been adapted to build a stochastic time-to-digital converter (TDC) [Kratyuk et al. [2009]]. Recently, the stochastic flash ADC has been used as a back-end of a SAR ADC [Verbruggen et al. [2015]]. Though independently developed and published on close dates, the work of [Verbruggen et al. [2015]] shares a similar big picture as our work of [Chen et al. [2015]] as it uses multiple comparison results to estimate the SAR conversion residue. However, there are two key advantages of our work both in the choice of the estimator and the circuit architecture. First, the work of [Verbruggen et al. [2015]] uses MLE, which is a sub-optimal choice compared to the Bayes estimator used in our work. Second, it arranges 16 different comparators for the LSB estimation. Their offsets need to be very carefully calibrated, which is a big design and operation burden especially for high resolution applications and considering process, voltage, and temperature (PVT) variations. By contrast, we just re-use the original comparator in the SAR ADC, and thus, do not have the offset mismatch problem. Our limitation compared to [Verbruggen et al. [2015]] is reduced conversion speed as it requires a larger number of comparison cycles. Yet, for the intended low-speed sensor applications, the speed penalty is a minor issue.

To validate the proposed statistical estimation based noise reduction technique, a prototype 11-bit SAR ADC is implemented in 65nm CMOS. Using the proposed technique, the measured SNR is improved by 7 dB, which matches well with the theoretical prediction. Overall, the prototype ADC achieves an ENOB of 10.5-bit at 100kS/s while consuming 0.6μW of power from a 0.7V supply.

2.2 Proposed Statistical Estimation Based Noise Reduction Technique: Basic Idea

Fig. 2.1 shows the simplified block diagram of a single-ended b-bit bottom-plate sampled SAR ADC. A SAR ADC has a property that its conversion residue V_{res} is readily available at the comparator input. We can derive the following relationship among the ADC input V_{in}, output D_{out}, and V_{res}:

$$D_{out} = V_{in} + n_s + V_{res} \tag{2.1}$$

where n_s represents the kT/C noise directly added to V_{in} during the sampling phase. Here, for simplicity of presentation, we have made the following assumptions that do not undermine the practicality of the proposed technique: a) we assume the parasitic capacitor $C_P = 0$. Since its effect is simply attenuating V_{res}, it can be easily added in (2.1) by applying a scaling factor to V_{res}; b) the comparator offset is assumed to be zero, as it does not affect the ADC SNR; and c) we ignore the effect of capacitor mismatch. In practice, if capacitor mismatch is a problem, classic mismatch calibration technique, such as [Lee et al. [1984]], can be applied jointly with the proposed technique.

As shown in (2.1), the ADC conversion error, defined as $(D_{out} - V_{in})$, consists of n_s and V_{res}. To reduce n_s, the only option is to increase the DAC capacitance C_{DAC}, which is not the focus of this work. In a SAR ADC, its conversion error is typically dominated by V_{res}, not n_s. For example, for a 12-bit SAR ADC with 2V peak-to-peak differential input swing, 420 fF of single-side DAC capacitance is already sufficient to suppress the sampling noise n_s to be less than the quantization

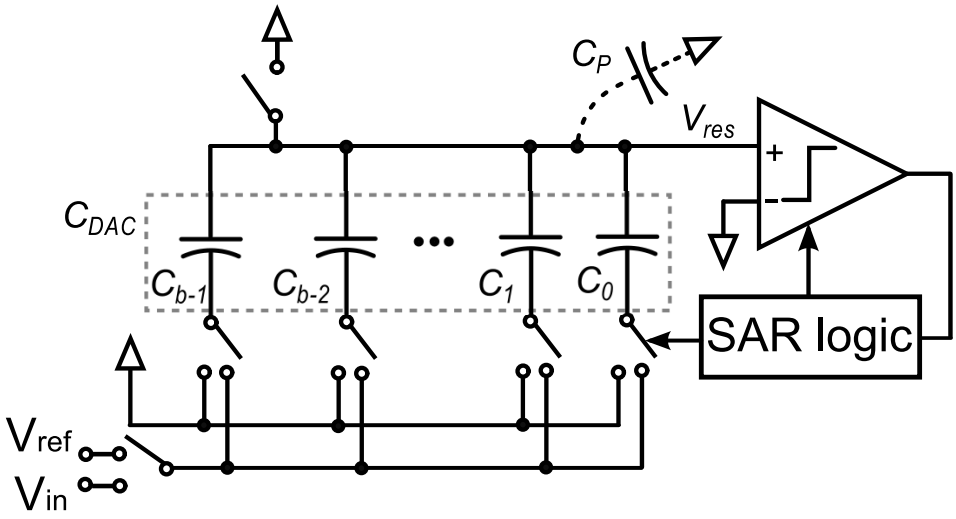

Figure 2.1: Diagram for a b-bit SAR ADC.

error. Note that 420 fF of total capacitance means that the unit capacitor size is only 0.1 fF, which is smaller than what most SAR ADCs use and what matching requires [Tripathi and Murmann [2013]]. In practice, n_s is usually smaller than V_{res}, which is set by the comparator noise and the DAC LSB size. This is especially true for recent SAR ADCs that use low power dynamic comparators without having a pre-amplifier [Harpe et al. [2013]; Lee et al. [2014]; Yip and Chandrakasan [2013]]. As a result, our work focuses on improving ADC SNR by reducing V_{res}.

V_{res} consists of three parts: the ADC quantization error (i.e., DAC LSB step), the comparator noise, and the DAC noise. If the ADC does not have any comparator noise or DAC noise, V_{res} is simply the ADC quantization error and is uniformly distributed between $\pm 1/2$ LSB. By contrast, in the presence of large comparator noise (in a SAR ADC the comparator noise is typically much large than the DAC noise), V_{res} is Gaussian distributed with a standard deviation close to

the comparator noise. To reduce V_{res}, a straightforward way is to use a low-noise comparator and a high-resolution DAC; however, both lead to greatly increased circuit power.

This chapter proposes a simple and power efficient way to reduce V_{res} by using statistical estimation. The core idea is that if we can estimate the value of V_{res}, denoted as $\hat{V}_{res}$, we can increase the ADC SNR by subtracting $\hat{V}_{res}$ from D_{out} as:

$$D^*_{out} = D_{out} - \hat{V}_{res} = V_{in} + n_s + (V_{res} - \hat{V}_{res}) \tag{2.2}$$

which shows that the accuracy of the new ADC output D^*_{out} is limited not by V_{res} but by the estimation error $(V_{res} - \hat{V}_{res})$. An interesting note is that if the estimation error can be made small, the resolution of D^*_{out} can even surpass the limit set by the ADC quantization error, because the subtraction of $\hat{V}_{res}$ reduces both comparator noise and quantization error. This implies that the proposed technique can actually permit, for example, a SAR ADC with a b-bit DAC array to reach more than b-bit resolution.

Now with core idea captured in (2.2), the key question to answer is how we can estimate V_{res}. We prefer performing estimation without incurring large hardware and power cost. Since V_{res} is readily available at the comparator input, we propose to use the original noisy SAR comparator to estimate V_{res}. This may appear counterintuitive because the comparator can only provide a binary decision and its output is error-prone due to its high noise. Certainly 1-time comparison is insufficient. What we propose is to simply repeat the LSB comparison for a total of N times and estimate V_{res} by examining the number of '1's, denoted as k. This is

doable because the comparator output carries information on its input. Qualitatively speaking, if $k = N$, we know that V_{res} is most likely a large positive value; if $k = 0$, V_{res} is most likely negative with a large magnitude; and if $k = N/2$, V_{res} is highly probable to be close to zero.

An intriguing side note is that the estimation of V_{res} is actually *enabled* by the comparator noise. If the comparator does not have any noise, its output would be straight '1's or '0's, and thus, we cannot extract any information about the magnitude of V_{res}, except for its sign. Having noise in the comparator actually enables us to improve our estimation accuracy on V_{res}. This phenomenon is actually an example of *stochastic resonance*, which is observed in a nonlinear system where the presence of a small amount of noise can actually improve the overall system SNR [Harmer et al. [2002]]. Such behavior is impossible in a linear system. In the SAR ADC, the 1-bit comparator is both nonlinear and noisy, which exactly matches the requirement for stochastic resonance.

2.3 Proposed Statistical Estimation Based Noise Reduction Technique: Mathematical Formulation

After presenting the basic idea of our proposed noise reduction technique, we now quantitatively answer what is the optimum choice of the estimator $\hat{V}_{res}$ given the number of LSB comparisons N and the number of '1's k. Let us focus our attention on the repeated LSB comparison, whose model is shown in Fig. 2.2. $d_{0,i}$ presents the i-th LSB comparison result, where i is from 1 to N. n_c represents the total noise referred to the comparator input. It includes both the comparator

noise and the DAC noise. It is typically dominated by the comparator noise. n_c is zero mean, and we denote its standard deviation as σ in the following discussion.

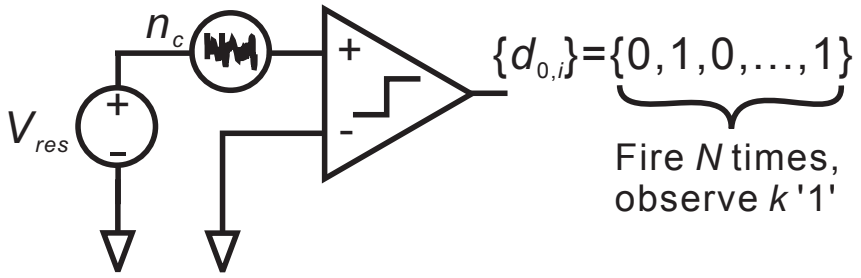

Figure 2.2: Simplified SAR ADC model during the LSB comparison.

Our goal is to form an estimator $\hat{V}_{res}$ that minimizes the mean square error (MSE), defined as:

$$\text{MSE} = Var(V_{res} - \hat{V}_{res}) = E\big[(V_{res} - \hat{V}_{res})^2\big] \tag{2.3}$$

where Var and E stands for statistical variance and expectation, respectively [Casella and Berger [1990]].

It turns out that the estimation of an unknown value out of a series of noisy binary tests is a classic statistical estimation problem [Casella and Berger [1990]]. Therefore, we directly borrow the concepts and theories from statistics to solve our estimation problem. Specifically, we discuss three widely used statistical estimators: the simple averaging based estimator, the maximum likelihood estimator (MLE), and the Bayes estimator. They all can be implemented as digital look-up tables with similar hardware costs.

2.3.1 Estimator based on averaging

One straightforward way to define $\hat{V}_{res}$ is $+1$ LSB for all straight '1's, -1 LSB for all straight '0's, and performing linear interpolation for other values of k. Mathematically speaking, this definition is as follows:

$$\hat{V}_{res,avg} = \frac{2k - N}{N} \cdot LSB \tag{2.4}$$

where $\hat{V}_{res,avg}$ linearly increases with k, and is ± 1 LSB for $k = 0$ and N, respectively. Although $\hat{V}_{res,avg}$ is easy to construct, it has several drawbacks. First, because $\hat{V}_{res,avg}$ is bounded by ± 1 LSB, it cannot accurately approximate V_{res} that is outside of that range due to comparator noise. This can be clearly observed from Fig. 2.3 that plots the MSE of $\hat{V}_{res,avg}$ as a function of V_{res}, N, and the comparator noise σ. If the comparator noise σ is large, there is a high probability for $|V_{res}| > 1$ LSB, and $\hat{V}_{res,avg}$ does not work well.

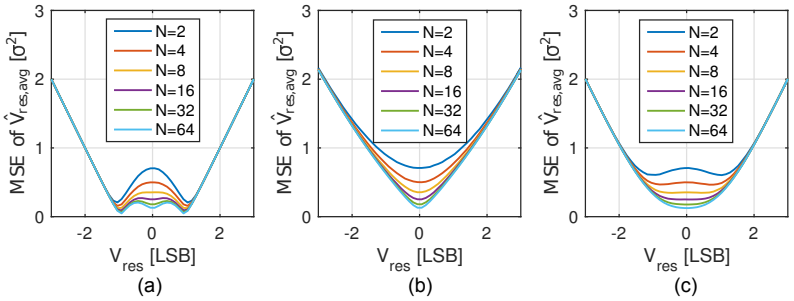

Figure 2.3: MSE of $\hat{V}_{res,avg}$ for various N and (a) $\sigma = 0.5$ LSB, (b) $\sigma = 2$ LSB, and (c) $\sigma = 1$ LSB.

Second, the shape of its MSE curve varies substantially with the comparator noise σ. The reason is that the comparator noise affects the value of k, but such

influence is not captured in (2.4). For example, for a given nonzero V_{res}, if the comparator noise is small, the majority of the comparator outputs would be either all '1's ($k = N$) or all '0's ($k = 0$), leading to $\hat{V}_{res,avg}$ close to ± 1 LSB. This results in a low MSE for $V_{res} = \pm 1$ LSB [see Fig. 2.3(a)], but a large MSE for V_{res} close to 0. On the other hand, if the comparator noise is large, it is highly likely that half of the comparator outputs are '1' ($k = N/2$), leading to $\hat{V}_{res,avg}$ close to 0. This yields a small MSE for $V_{res} = 0$, but a large MSE elsewhere [see Fig. 2.3(b)]. The overall best performance for $\hat{V}_{res,avg}$ in terms of a small and relatively flat MSE is obtained only when the comparator noise σ is close to 1 LSB [see Fig. 2.3(c)]. This limits its applicability.

Furthermore, although its MSE decreases as N increases, the region with a small MSE becomes narrower [see Fig. 2.3]. For a nonzero V_{res}, the MSE of $\hat{V}_{res,avg}$ does not decrease to 0 even if N goes to infinity. The reason is that $\hat{V}_{res,avg}$ is a biased estimator of V_{res}, and the bias does not converge to zero [Casella and Berger [1990]]. As will be shown later, the aforementioned drawbacks for $\hat{V}_{res,avg}$ do not exist for the other two estimators.

2.3.2 Maximum likelihood estimator (MLE)

A key reason that $\hat{V}_{res,avg}$ does not achieve a low estimation error is that it does not assume any prior information on the comparator noise σ. In practice, σ is chosen by the designer. It can be extracted via SPICE simulations with good accuracy. Although σ may change due to process, voltage, and temperature (PVT) variations, we can obtain an accurate value of σ by performing a simple foreground

calibration. We can simply set $V_{in} = 0$ by shorting the ADC input, and monitor the standard deviation of D_{out}. Since we have assumed that comparator noise σ is the dominant random source over the sampling noise n_s, the standard deviation of D_{out} simply reflects the value of σ. Since temperature changes slowly, the foreground calibration does not need to be repeated frequently. In addition, since the statistical estimation is performed at the LSB level, a 10% change in the value of σ only causes minor degradation (e.g., a 0.1 LSB error) in the post-estimation ADC SNR. This greatly relaxes the requirement on the calibration accuracy. Given this, we can treat the value of σ as a known quantity during the estimation process. We can take advantage of it to form a much better estimator, which is the maximum likelihood estimator (MLE).

The definition of MLE is easy to understand. Given the number of comparisons N and the number of '1's k, we define the estimator $\hat{V}_{res}$ to be the value that maximizes the probability of observing k '1's out of N comparisons. MLE has been thoroughly studied in statistics and has several merits. First, it is consistent. As N increases, $\hat{V}_{res,MLE}$ converges to V_{res} and can achieve arbitrary precision [Casella and Berger [1990]]. Second, it is highly efficient from the information usage point of view. It achieves the Cramer-Rao lower bound as N goes to infinity, which means that MLE achieves the lowest asymptotic MSE [Casella and Berger [1990]].

We can derive $\hat{V}_{res,MLE}$ for our problem in the following way. The probability of a comparator output being '1' follows Bernoulli distribution with probability:

$$P(d_0 = 1) = P(V_{res} + n_c > 0) = F(\frac{V_{res}}{\sigma}) \tag{2.5}$$

where $F(x)$ is the cumulative distribution function of normal distribution with mean of 0 and variance of 1, given by:

$$F(x) = \int_{-\infty}^{x} f(x)dt = \int_{-\infty}^{x} \frac{1}{\sqrt{2\pi}} e^{-\frac{s^2}{2}} ds \tag{2.6}$$

where $f(x)$ is its corresponding probability density function. Assuming the comparator hysteresis is negligible, the repeated LSB comparator outputs, $\{d_0\}$ ($i \in [1, N]$), can be considered as independently and identically distributed random variables. Thus, from the probability theory [Casella and Berger [1990]], we know that $k = \sum_{i=1}^{N} d_{0,i}$ follows the binomial distribution $B(N, F(V_{res}/\sigma))$ with the probability given by:

$$P(k|V_{res}) = \binom{N}{k} F(\frac{V_{res}}{\sigma})^k \big(1 - F(\frac{V_{res}}{\sigma})\big)^{N-k} \tag{2.7}$$

where $P(k|V_{res})$ means the probability of having k '1's conditioning on V_{res}. Since $\hat{V}_{res,MLE}$ maximizes $P(k|V_{res})$ by definition, we have:

$$\frac{dP(k|V_{res})}{dV_{res}}\Big|_{\hat{V}_{res,MLE}} = 0 \tag{2.8}$$

From (2.8), we can derive that:

$$F(\hat{V}_{res,MLE}/\sigma) = \frac{k}{N} \tag{2.9}$$

This result is intuitive. $\hat{V}_{res,MLE}$ ensures that the probability of the comparator output being 1 is k/N, and thus, it achieves the highest probability for having in total k '1's out of N trials. From (2.9), we can solve $\hat{V}_{res,MLE}$:

$$\hat{V}_{res,MLE} = \sigma \cdot F^{-1}(\frac{k}{N}) \tag{2.10}$$

It shows that $\hat{V}_{res,MLE}$ is linearly proportional to the comparator noise σ. This is different from $\hat{V}_{res,avg}$ that has no dependence on σ [see (2.4)].

$\hat{V}_{res,MLE}$ defined in (2.10) has one limitation that it does not work for $k = 0$ and $k = N$. If we plug $k = 0$ or $k = N$ into (2.10), $\hat{V}_{res,MLE}$ is $\pm\infty$. This is expected because $\hat{V}_{res,MLE} = -\infty$ achieves the highest probability for $k = 0$, and $\hat{V}_{res,MLE} = \infty$ ensures that $k = N$. This issue may be minor for a large N, because the probability of $k = 0$ and $k = N$ would approach zero. However, for a small N, $k = 0$ and $k = N$ do appear, which causes an estimation failure. To solve this problem, we can re-define:

$$\hat{V}_{res,MLE}(k = 0) = \sigma \cdot F^{-1}(\frac{0.2}{N}) \tag{2.11}$$

$$\hat{V}_{res,MLE}(k = N) = \sigma \cdot F^{-1}(\frac{N - 0.2}{N}) \tag{2.12}$$

For other k lies in $[1, N - 1]$, we still follow the definition of (2.10).

Fig. 2.4 shows $\hat{V}_{res,MLE}$ as a function of k and N. Different from $\hat{V}_{res,MLE}$, the relationship between $\hat{V}_{res,MLE}$ and k is nonlinear. The range of $\hat{V}_{res,MLE}$ expands with N, from $\pm 1.6\sigma$ at $N = 3$ to $\pm 2.3\sigma$ at $N = 15$. This means that $\hat{V}_{res,MLE}$ can approximate a wider range V_{res} as N increases.

To evaluate how accurate $\hat{V}_{res,MLE}$ is, we plot its estimation error as a function of V_{res} and N in Fig. 2.5. In general, its MSE decreases as N increases. For the same N, its MSE is small for a small V_{res}, but increases as the amplitude of V_{res} increases. The reason is that the value of $\hat{V}_{res,MLE}$ is bounded for a given N (see Fig. 2.4), and thus, does not work well for a very large V_{res}. However, unlike $\hat{V}_{res,avg}$, the range of $\hat{V}_{res,MLE}$ increases with N, and thus, its region with a small

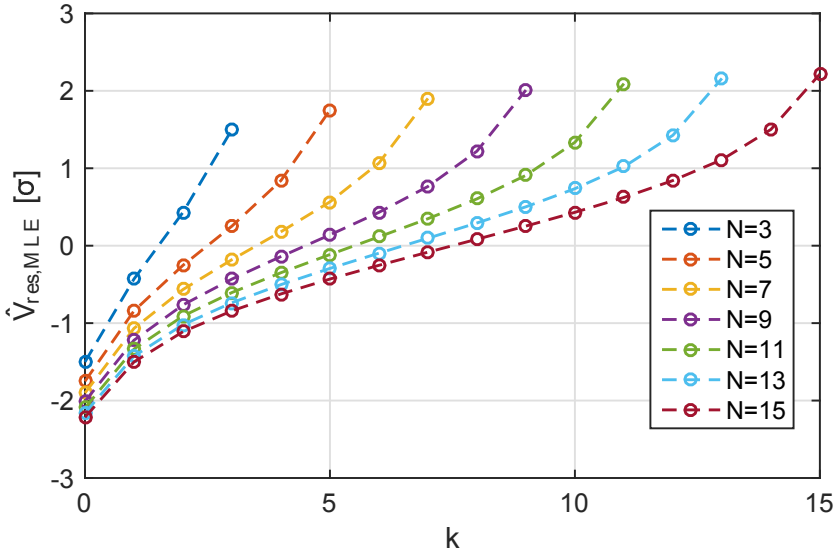

Figure 2.4: Value of $\hat{V}_{res,MLE}$ as a function of N and k.

MSE is broadened. This is a key advantage of $\hat{V}_{res,MLE}$ compared to $\hat{V}_{res,avg}$. It enables $\hat{V}_{res,MLE}$ to accurately estimate a wide range of V_{res} especially for a large N. In fact, we can prove that the MSE of $\hat{V}_{res,MLE}$ goes to zero as N approaches infinity for any V_{res} [Casella and Berger [1990]].

2.3.3 Bayes estimator

MLE is a significant improvement over the simple averaging based estimator, but it still does not achieve the lowest estimation error. There is one extra piece of information that MLE does not make use of, which is the distribution of V_{res}. This extra information can be exploited to construct a better estimator with a lower estimation error than MLE.

Before moving ahead, let us first examine the distribution of V_{res}. Fig. 2.6

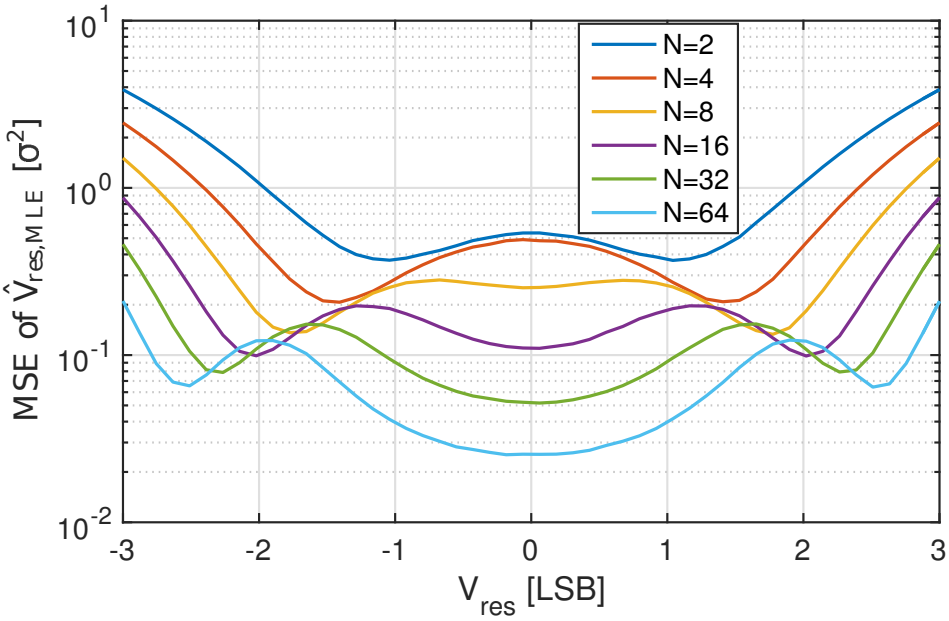

Figure 2.5: MSE of $\hat{V}_{res,MLE}$ for different V_{res}.

shows the simulated histograms of V_{res} for an 11-bit SAR ADC assuming the comparator noise $\sigma = 1$ LSB. Three different input signals are used. Sinusoidal inputs with -6-dBFS and -20-dBFS are used in Fig. 2.6(a) and (b), respectively. A Gaussian random input with a standard deviation of 10% ADC full swing is used in Fig. 2.6(c). As can be seen, there is negligible difference in the V_{res} distribution among the three cases. They are all close to Gaussian distribution with zero mean and a standard deviation of 1 LSB. This shows that the distribution of V_{res} has very weak dependence on the ADC input V_{in}. This is not hard to understand. By the end of the 11-bit SAR conversion, the conversion residue V_{res} is almost completely uncorrelated with V_{in}, and is basically set by the comparator noise. Given this observation, we can confidently approximate V_{res} as a Gaussian random variable and its proba-

bility density function (pdf) $g(V_{res}) \equiv f(V_{res}/\sigma)$, where $f(\cdot)$ is the pdf of Gaussian distribution with zero mean and standard deviation of 1.

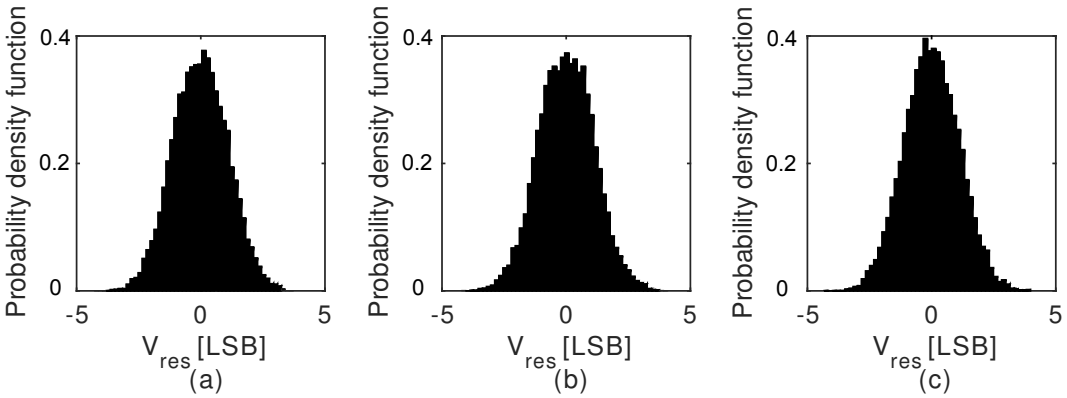

Figure 2.6: Histogram of V_{res} for (a) a -6-dBFS sinusoidal input, (b) a -20-dBFS sinusoidal input, and (c) a Gaussian random input with standard deviation of 10% ADC full range.

Now let us derive the optimum estimator for V_{res} given the prior information on its distribution. This problem has been thoroughly studied in the statistical estimation theory [Casella and Berger [1990]]. It can be rigorously proved that the best estimator that achieves the minimum MSE given the prior distribution is the Bayes estimator (BE), which is defined as the mean of the posterior distribution of V_{res} after observing k '1's out of N trials. To understand it, let us consider a simple example of $N = 3$. We can have 4 different values for k, which is 0, 1, 2, and 3. For each case, we can calculate the posterior distribution $g(V_{res}|k)$ using the Bayes theorem[Casella and Berger [1990]]:

$$g(V_{res}|k) = \frac{P(k|V_{res})g(V_{res})}{\int_{-\infty}^{+\infty} P(k|V_{res})g(V_{res})dV_{res}} \tag{2.13}$$

where $P(k|V_{res})$ is the probability of observing k '1's conditioning on V_{res}. Fig. 2.7 plots the V_{res} prior distribution $g(V_{res})$ together with its posterior distributions $g(V_{res}|0)$, $g(V_{res}|1)$, $g(V_{res}|2)$, and $g(V_{res}|3)$. Bayes rule basically allows us to update the distribution of V_{res} given the observation result k. We can see that the prior and posterior distributions are different, which is enabled by the knowledge of k. For example, compared to $g(V_{res})$, the posterior distribution $g(V_{res}|0)$ is shifted towards the negative side. This is because after observing all '0's from the comparator outputs, we can update the distribution of V_{res}, which should be more negatively biased.

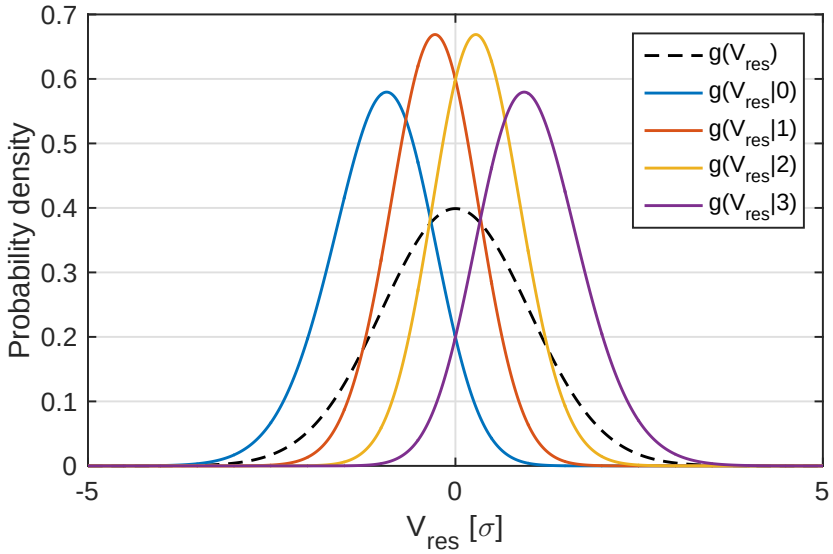

Figure 2.7: Prior distribution $g(V_{res})$ and posterior distribution $g(V_{res}|k)$ for $N = 3$.

The Bayes estimator is defined as the mean of the posterior distribution.

Mathematically, it is given by:

$$\hat{V}_{res,BE}(k) \equiv E(V_{res}|k) = \int_{-\infty}^{+\infty} V_{res} \cdot g(V_{res}|k) dV_{res} \tag{2.14}$$

For the case of $N = 3$, we can calculate that $\hat{V}_{res,BE}(0) = -1\sigma$, $\hat{V}_{res,BE}(1) = -0.3\sigma$, $\hat{V}_{res,BE}(2) = +0.3\sigma$, and $\hat{V}_{res,BE}(3) = +1\sigma$, respectively.

Note that (2.13) and (2.14) are computationally intensive. Fortunately, we do not need to solve $\hat{V}_{res,BE}$ for every ADC output. We only need to compute once, and store the results for all possible k values in a look-up table. This way, once we know k from the comparator outputs, $\hat{V}_{res,BE}$ can be directly obtained from the table.

Fig. 2.8 shows $\hat{V}_{res,BE}$ as a function of k and N. Comparing it carefully with $\hat{V}_{res,MLE}$ shown in Fig. 2.4, we can see that the range of $\hat{V}_{res,BE}$ is smaller than $\hat{V}_{res,MLE}$. The reason is that $\hat{V}_{res,BE}$ makes use of the prior distribution of V_{res}. Since V_{res} is concentrated around zero, $\hat{V}_{res,BE}$ is biased more towards zero.

Fig. 2.9 shows MSE for $\hat{V}_{res,BE}$ as a function of V_{res} and N. Comparing it with Fig. 2.5 of $\hat{V}_{res,MLE}$, we see that the MSE of $\hat{V}_{res,BE}$ is smaller than that of $\hat{V}_{res,MLE}$ for a small V_{res} in $[-2\sigma, +2\sigma]$, but is slightly larger for $|V_{res}| > 2\sigma$. However, because V_{res} is known to concentrate around 0, it is expected that the overall MSE of $\hat{V}_{res,BE}$ is smaller than that of $\hat{V}_{res,MLE}$.

2.3.4 Estimator performance comparison

To compare the estimation error for the three estimators, we compute the MSE of $\hat{V}_{res,avg}$, $\hat{V}_{res,MLE}$, and $\hat{V}_{res,BE}$ for $\sigma = 1$ LSB, and plot them as a function

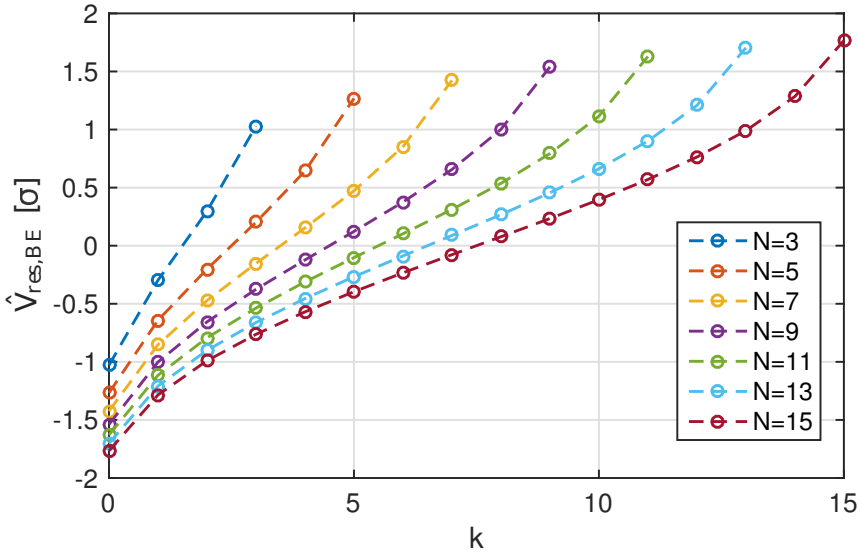

Figure 2.8: $\hat{V}_{res,BE}$ as a function of N and k.

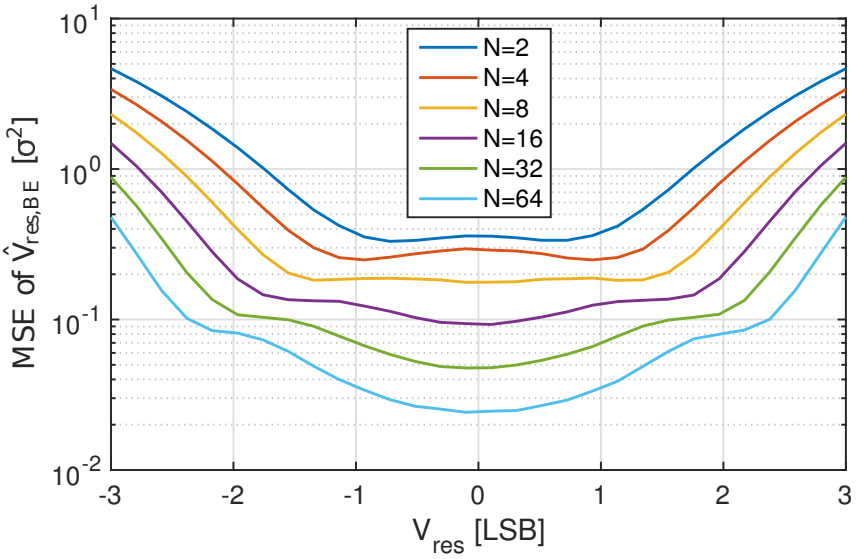

Figure 2.9: MSE versus x for $\hat{V}_{res,BE}$.

of N in Fig. 2.10.

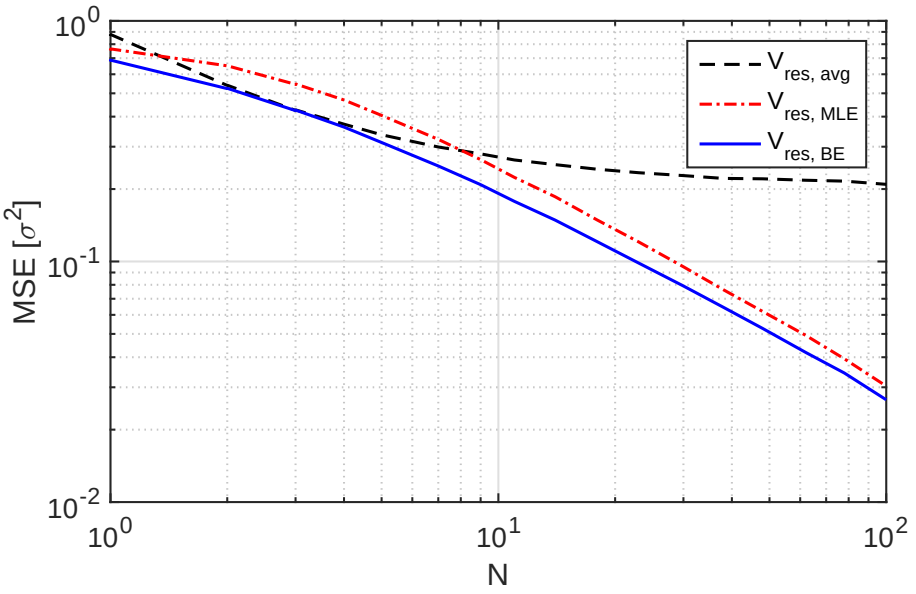

Figure 2.10: MSE versus N for a normal distributed x with $\sigma = 1$LSB.

As expected, the MSE of $\hat{V}_{res,BE}$ is consistently smaller than that of $\hat{V}_{res,avg}$ and $\hat{V}_{res,MLE}$, indicating the highest estimation accuracy. Note that the MSE values for all three estimators are similar for a small N. However, for a large N, there are significant differences. For $\hat{V}_{res,avg}$, its MSE saturates to around $0.2\sigma^2$. By contrast, the MSE of $\hat{V}_{res,MLE}$ and $\hat{V}_{res,BE}$ keep decreasing with N at the slope of 10 dB per decade. This slope is essentially the limit set by Cramer-Rao lower bound [Casella and Berger [1990]], confirming the high efficiency of both $\hat{V}_{res,MLE}$ and $\hat{V}_{res,BE}$. Since $\hat{V}_{res,BE}$ has the lowest MSE, it is chosen for the prototype ADC.

As mentioned earlier, both MLE and Bayes estimators require the knowledge of the comparator noise σ. It is interesting that the extracted comparator

noise does not need to be 100% accurate when estimating $\hat{V}_{res,BE}$. This makes the proposed technique more robust as the comparator noise can drift with Process-Voltage-Temperature (PVT) variation. Let us assume a $\pm 10\%$ noise drifting happens in the prototype ADC. After 1σ=1.0 LSB is extracted, the comparator noise drifts to 0.9 LSB or 1.1 LSB due to PVT variation. However, the comparator noise is supposed to be the same and the 1σ comparator noise of 1.0 LSB is used when performing the Bayes estimation. Fig. 2.11 plots the behavioral simulated SNR improvement for different σs. As can be seen from Fig. 2.11, the SNR is improved effectively even though an inaccurate comparator noise 1σ=1.0 LSB is used to estimate $\hat{V}_{res,BE}$ for 1σ=0.9 LSB and 1σ=1.1 LSB. Note that the SNR differences among three cases result from different comparator noise used in the ADC model. Fig. 2.11 also shows that the proposed technique can be easily extended to achieve re-configurable resolution by adjusting N. In the prototype design, a 7-dB SNR improvement is expected which requires $N = 17$.

2.3.5 Comparison to oversampling and analog scaling

The standard ADC oversampling can also be used to reduce ADC noise by averaging, and the improvement in SNR is also 10 dB per decade. Thus, it is meaningful to compare it to the proposed statistical estimation technique. The merit of oversampling is that it reduces both the sampling noise n_s and the comparison noise n_c, while the proposed technique based on statistical estimation only reduces n_c. However, as mentioned earlier, in a SAR ADC, the noise is typically dominated by n_c, and thus, their effect in total noise reduction is similar. The disadvantage of

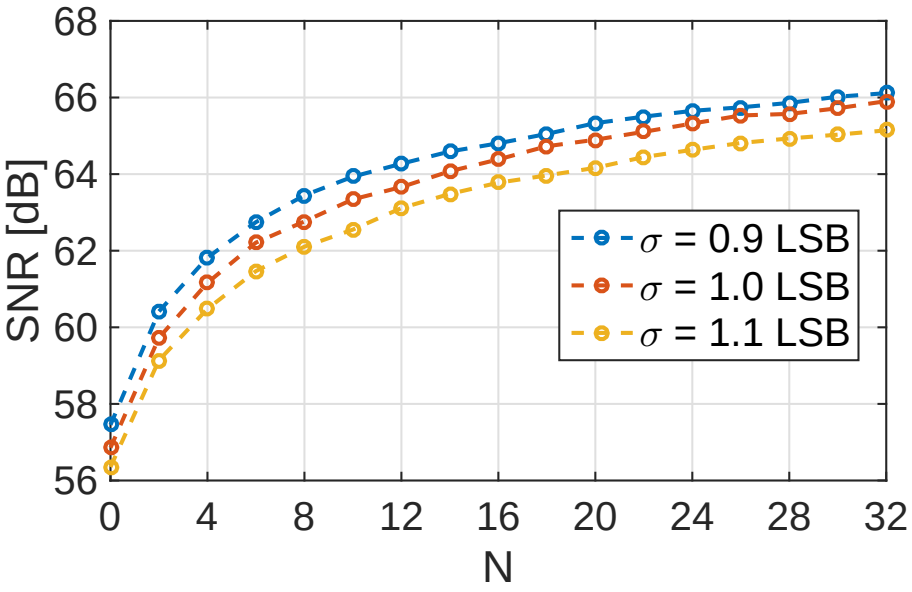

Figure 2.11: Simulated SNR versus N with $\pm 10\%$ variations in the comparator noise σ.

oversampling is that it *cannot* improve the ADC power efficiency. Every doubling of the oversampling ratio (OSR) leads to twice the ADC power, as it requires repeating all the sampling, comparison and DAC switching operations. By contrast, the proposed technique only increases the number of LSB comparisons, so its required total number of comparator operations is much smaller. Additionally, the DAC is not switched, and thus, does not dissipate any extra DAC power. As a result, the power efficiency of the proposed technique is much higher than oversampling.

As in any noise reduction technique, there is always a cost of power. For the proposed technique, the total power of the comparator increases due to extra number of LSB comparisons. Take our 11-bit prototype ADC as an example, to reduce noise by 7 dB, the LSB comparison needs to be fired 17 times, which results

in an increase of total comparator power by $(11+17)/11 \approx 2.5$ times. By contrast, to obtain the same amount of noise reduction for the same 11-bit ADC, if we choose the brute-force way to reduce comparator noise by increasing its size and power, we need to increase the comparator power by 21 times (see Prototype ADC Design section). Thus, the proposed technique is much more power efficient. The tradeoff for the proposed technique is reduced conversion rate due to increased number of LSB comparisons. However, as mentioned earlier, this is only a minor issue for the intended low-to-medium speed sensor applications.

2.4 Prototype ADC Design

2.4.1 Detailed circuit schematics

To verify the proposed statistical estimation based noise reduction technique, a 11-bit prototype SAR ADC is designed, whose architecture is shown in Fig. 2.12. There are only two simple changes made to the standard SAR ADC architecture: 1) the SAR logic is modified to repeat the LSB comparison for $N = 17$ times; and 2) a counter is used to count the number of '1's during LSB comparisons to obtain k. A low power supply voltage of 0.7V is chosen to demonstrate the effectiveness of the proposed technique for low voltage and low power applications.

The DAC is implemented with binary-weighted metal finger (or MoM) capacitors. Since the DAC power is proportional to the total capacitor value, it is desired to reduce the unit capacitor C_u for power saving. Considering the noise and matching requirement, this design chooses C_u = 2 fF. A bidirectional single-side (BSS) switching technique is adopted to further reduce the DAC reference power by

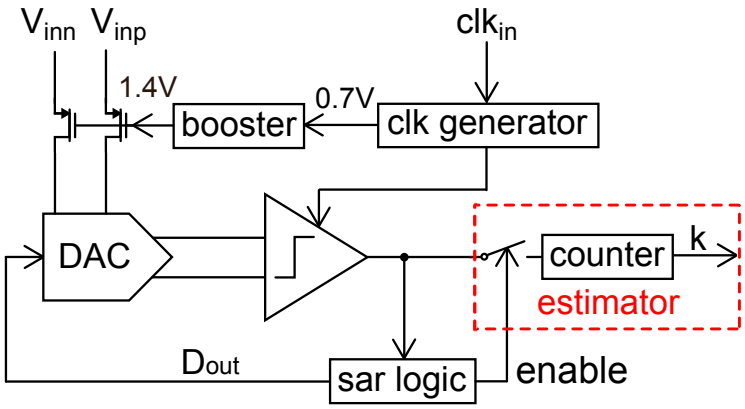

Figure 2.12: Proposed SAR ADC architecture.

86% compared to the conventional switching scheme [Chen et al. [2014a]; Sanyal and Sun [2014]]. BSS reduces the number of unit capacitors by 4 times, leading to a small capacitor array of $\{256, 128, 64, 32, 16, 16, 8, 4, 2, 1, 1\}C_u$ for an 11-bit ADC. Compared to widely used monotonic switching technique of [Liu et al. [2010a]], BSS achieves higher SNDR as the comparator input common-mode voltage V_{cm} variation is reduced and V_{cm} can converge to half V_{dd} instead of ground. A redundant capacitor of $16C_u$ is provided to recover possible errors during the first several MSB comparisons with large V_{cm} variation [Chen et al. [2014a]]. The total capacitance is $528C_u = 1056$fF, leading to 88-μV differential sampling kT/C noise. Since the unit capacitor is only 2 fF, the routing parasitic capacitors have a considerable influence on the capacitor matching accuracy. A segmented common-centroid layout technique is used for better matching. The floor plan for a single side capacitor array is shown in Fig. 2.13. The capacitors are separated into two groups $\{C_8, C_7, ..., C_4\}$ and $\{C_3, C_2, C_1, C_0\}$. The common-centroid rule is applied horizontally for the first group and vertically for the second. Dummy cells, repre-

sented as D, are added for better matching.

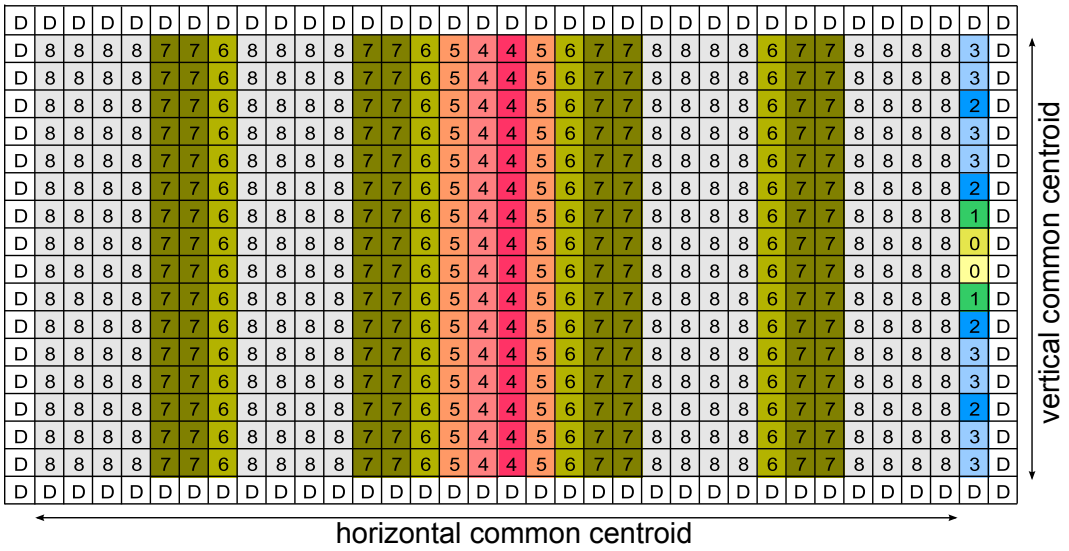

Figure 2.13: DAC capacitor array floor plan.

To ensure good sampling linearity, bottom-plate sampling is used. In addition, a clock booster shown in Fig. 2.14(a) is employed to boost the sampling clock voltage from 0.7V to 1.4V. As a result, simple small NMOS transistors can be used to sample V_{in} instead of an array of bootstrapped switches or large CMOS switches to reduce the design complexity and the switch driving power.

Fig. 2.14(b) shows the dynamic strong-arm latch comparator. It uses a PMOS input pair to minimize the flicker noise and the substrate coupling. Thanks to the proposed noise reduction technique, the comparator thermal noise requirement is relaxed, leading to substantially reduced comparator power. In this design, the SPICE simulated total input referred noise at the comparator input is 480μV or 0.7 LSB. Note that this is much larger than the sampling kT/C noise, and thus, the

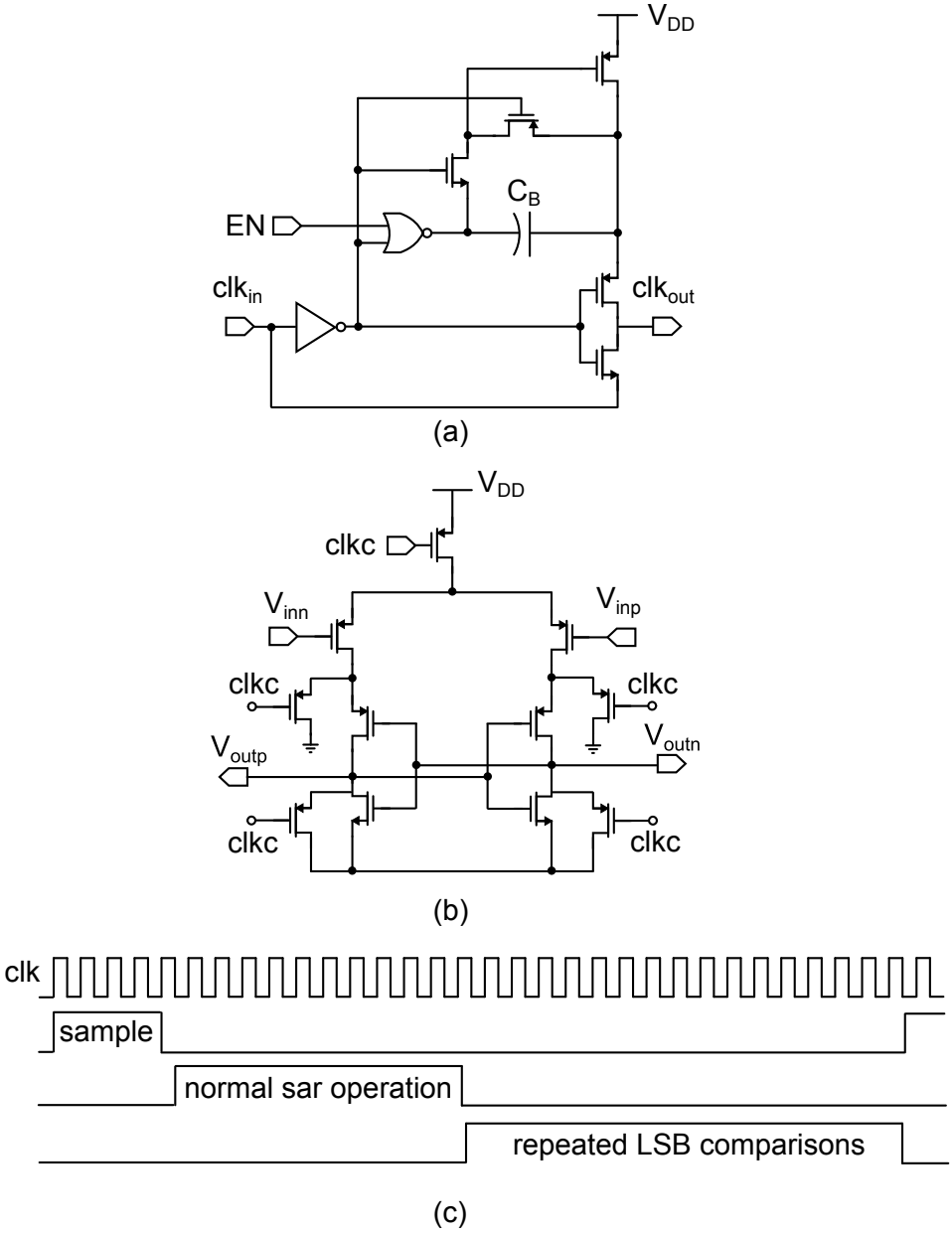

Figure 2.14: Schematic of (a) the clock booster; (b) the comparator; and (c) the timing diagram.

overall ADC noise is dominated by the comparator noise.

The ADC timing diagram is shown in Fig. 2.14(c). It uses a synchronous clocking scheme. The frequency of the master clock is 32 times faster than the sampling rate. The first 4 clock cycles are used for input sampling to ensure high sampling accuracy; the subsequent 11 cycles are used for normal SAR operation; and the final 17 cycles are used for repeated LSB comparisons. This clock allocation scheme can be easily implemented using a ripple counter based clock divider and several AND gates. The SAR logic is built by standard shift registers. When the normal SAR operation finishes, the last shift register makes transition and $ready = 1$ is generated. A 5-bit counter shown in Fig. 2.15 is enabled, which records the number of '1's during the LSB comparisons and obtains k for statistical estimation. The counter consumes no power during normal SAR operation. The counted k is given by:

$$k = 16 \times D4 + 8 \times D3 + 4 \times D2 + 2 \times D1 + D0 \tag{2.15}$$

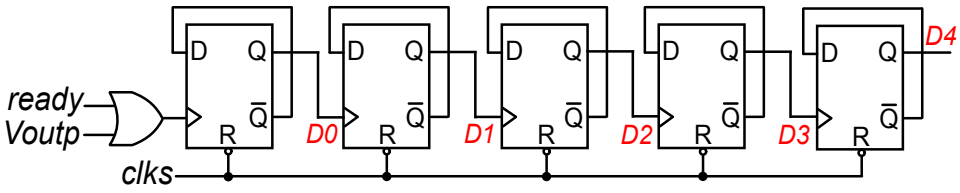

Figure 2.15: 5-bit counter to count k.

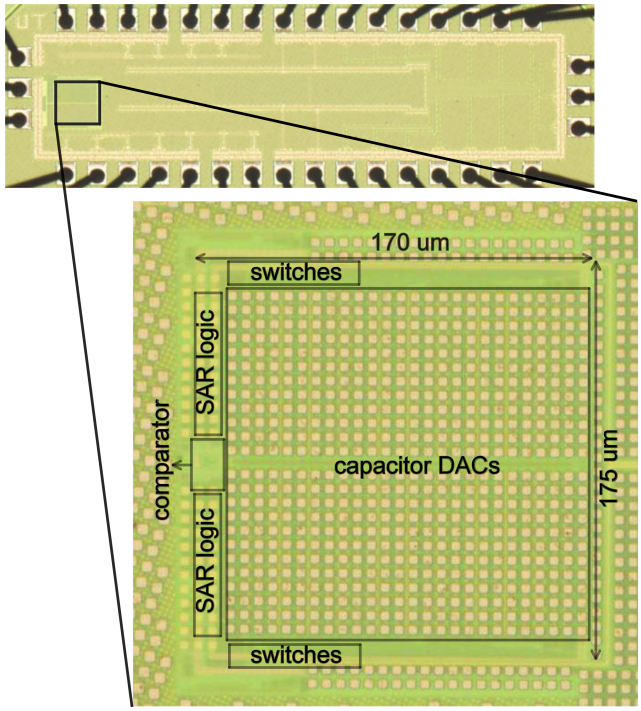

Figure 2.16: Die micrograph.

2.4.2 Measurement Results

The prototype ADC is implemented in 65nm CMOS process. Fig. 2.16 shows the die photo. The ADC occupies an active area of 0.03 mm^2, which is dominated by the DAC. The power supply is 0.7V and the sampling rate is 100kS/s. Fig. 2.17 shows the measured DNL and INL, which are $+1.04/-1$ LSB and $+1.57/-1.23$ LSB. According to the INL plot, there exists a 1-LSB systematic mismatch between the 6 MSB capacitors and the 6 LSB capacitors, which arises from the unmatched surrounding environment due to the segmented layout strategy in Fig. 2.13 and inaccurate parasitic capacitor extraction. A simple foreground calibration similar to [Chen and Brodersen [2006]] is performed and the appreciable

periodic INL transition pattern reduces.

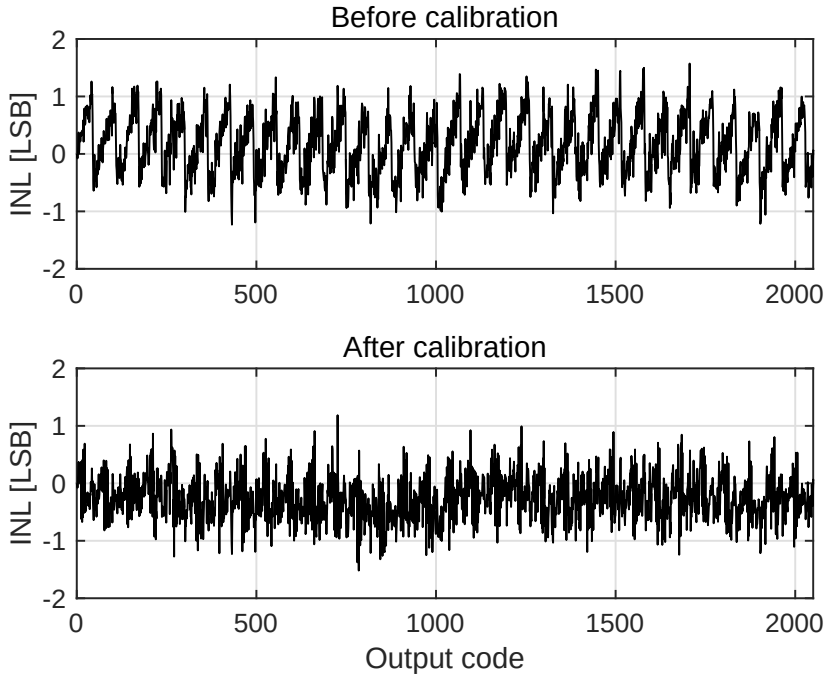

Figure 2.17: Measured DNL and INL.

To verify the proposed noise reduction technique, we first measure the ADC noise (e.g., the variation of D_{out}) at $V_{in} = 0$. The measured probability densities for D_{out} before and after noise reduction are shown in Fig. 2.18 together with fitted normal distributions. Before noise reduction, the standard deviation of D_{out} is 0.73 LSB. It indicates the comparator input referred noise is about 500μV, which is in agreement with SPICE simulation. After noise reduction, the standard deviation of D^*_{out} is reduced by 7 dB to 0.33 LSB, which matches well with the estimation theory. Note that if the conventional SAR ADC design approach is used, the comparator noise needs to be reduced to 0.16 LSB in order for the total ADC noise to

be 0.33 LSB, which also includes the 0.29 LSB quantization error. This means that the total comparator power needs to be increased by 21 times. By contrast, in our proposed noise reduction technique, the total comparator power is only increased by 2.5 times, which firmly proves its higher power efficiency compared to brute-forth analog scaling. Once the comparator noise is extracted, $\hat{V}_{res,BE}(k)$ can be computed using (2.13) and (2.14).

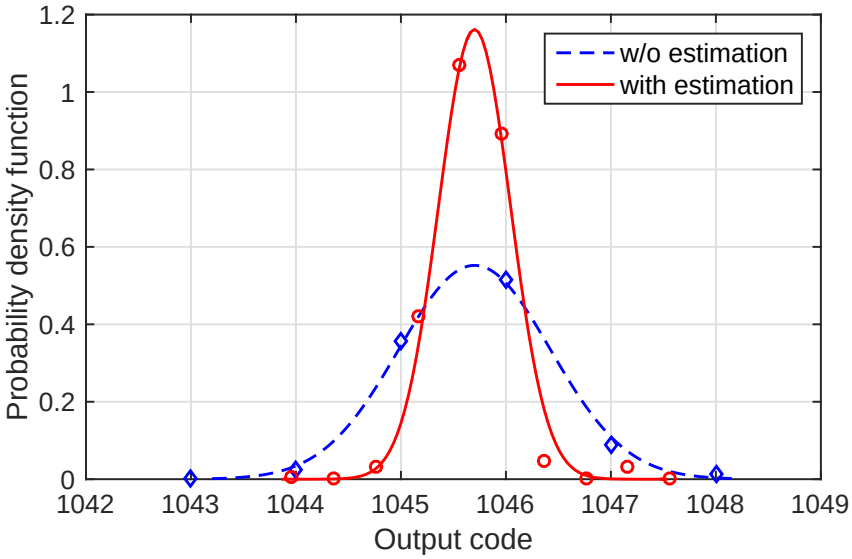

Figure 2.18: D_{out} distribution with and w/o estimation at $V_{in} = 0$.

Fig. 2.19 shows the measured spectrum for a 96-kHz full-scale input sampled at 100kS/s. The reason choosing the 96-kHz frequency input is our high-quality low-distortion band-pass filter has a cut-off frequency at 90 kHz. The measured SNDR and SNR are 59.4 and 59.7 dB for 96-kHz input, respectively. After applying the proposed noise reduction technique, the noise floor is clearly lowered. SNDR and SNR are improved to 64.5 dB and 65 dB, respectively. The correspond-

ing ENOB is 10.5-bit.

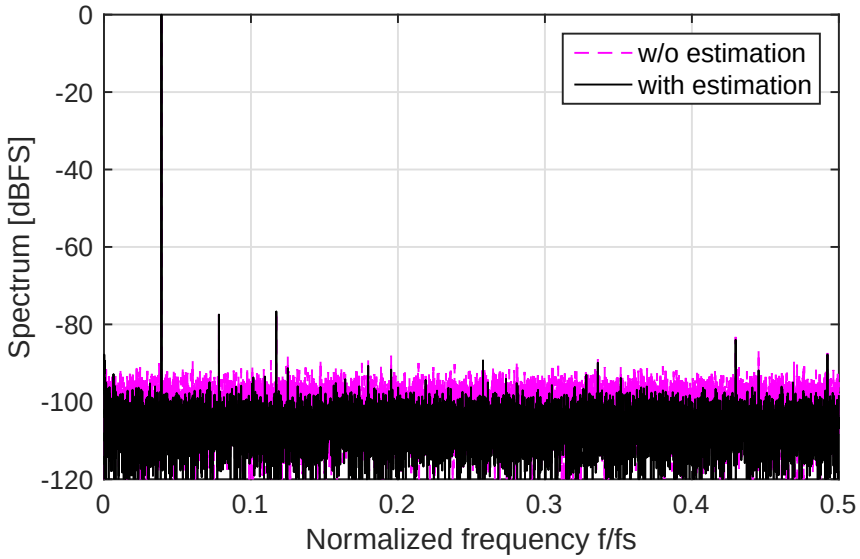

Figure 2.19: Measured 2^{14}-point ADC output spectrum with 96-kHz input.

Fig. 2.20 shows the SNR with varying input amplitudes. The SNR improvement using simple averaging based estimator $\hat{V}_{res,avg}$ is limited to only 2.2dB. Maximum likelihood estimator (MLE) achieves 5.8dB SNR improvement, which is better than averaging based estimator. Using the Bayes estimator $\hat{V}_{res,BE}$, the SNR can be improved by 7dB, which is 4.8dB better than that of averaging based estimator and 1.2dB better than that of MLE. This matches well with the analysis. When the input is very large, the SNR improvement decreases slightly to 5.3 dB, which is caused by the unwanted capacitive coupling from the ADC input to the reference lines, discovered during measurements. Such SNR loss can be recovered by layout optimization to reduce the coupling. To evaluate the robustness of SNR improvement using Bayes estimator, various extracted comparator noise σs, which

can be caused by PVT variation, are used to estimate $\hat{V}_{res,BE}$. Fig. 2.21 shows the measured SNR improvement versus σs. The peak SNR improvement is large in the middle and small at two sides, just like a parabolic distribution. The peak SNR improvement is 6.9 dB at $\sigma = 0.73$ LSB. As long as the extracted $\sigma \in [0.6, 0.86]$ LSB, the SNR improvement is greater than 6 dB and one more effective bit is achieved with Bayes estimation.

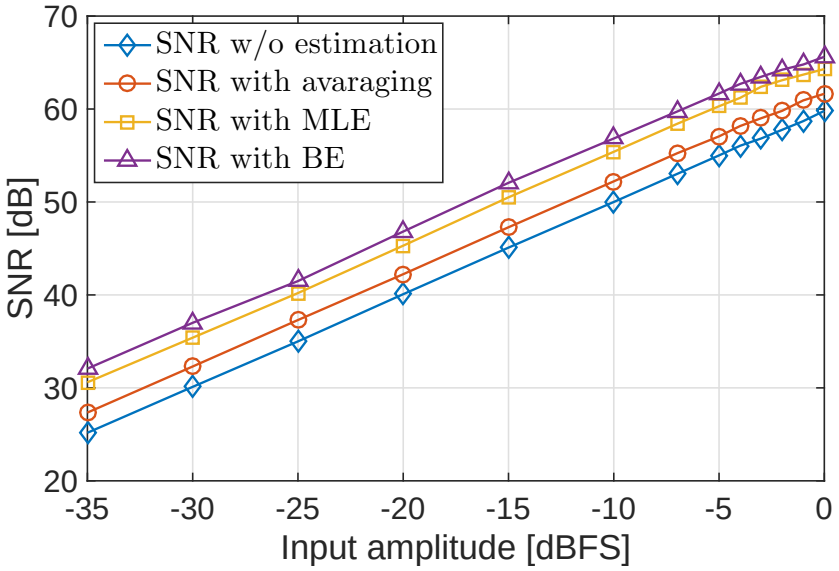

Figure 2.20: Measured SNR versus input amplitudes.

The ADC consumes 0.6 μW from a 0.7 V power supply. The comparator, DAC, clock generator, and SAR logic consume 70 nW, 102 nW, 193 nW and 280 nW, respectively. With the noise reduction technique, the comparator power accounts for only 10% of the total power at the ENOB of 10.5-bit. The digital power, including both clock generator and SAR logic, dominates the overall ADC power. It can be substantially reduced via optimization and/or going to a more

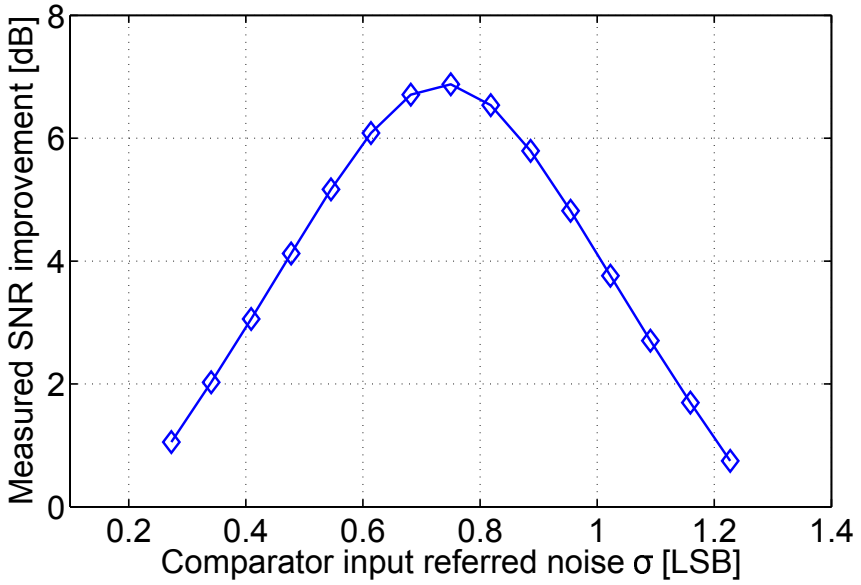

Figure 2.21: Measured SNR improvement versus various comparator noise σ.

advanced technology node, without affecting SNR. The measured figure-of-merit (FOM) for the prototype ADC is 4.5 fJ/conversion-step. The performance of the proposed ADC is summarized in Table 2.1. Fig. 2.22 shows Walden FoM versus SNDR for this work and recently published ADCs in ISSCC and VLSI conferences. The data for the figure is taken from the survey made available by Dr. Boris Murmann (`http://web.stanford.edu/~murmann/adcsurvey.html`). As can be seen, this work achieves the state-of-the-art power efficiency, especially among ADCs with SNDR greater than 64 dB. Note that there is still large space for further performance improvements especially on the design of the clock generator and the SAR logic.

Table 2.1: Measured performance summary

Process [nm]	65	
Sampling rate [kS/s]	100	
Resolution [bit]	11	
Active area [mm^2]	0.03	
Power supply [V]	0.7	
Total power [μW]	0.6	
DNL [LSB]	$+1.04$ / -1.00	
INL [LSB]	$+1.57$ / -1.23	
Noise Reduction?	No	Yes
Dynamic range [dB]	60	67
Peak SNR [dB]	59.7	65
Peak SNDR [dB]	59.4	64.5
ENOB [bit]	9.6	10.5
Walden FoM [fJ/conv-step]	9	4.5

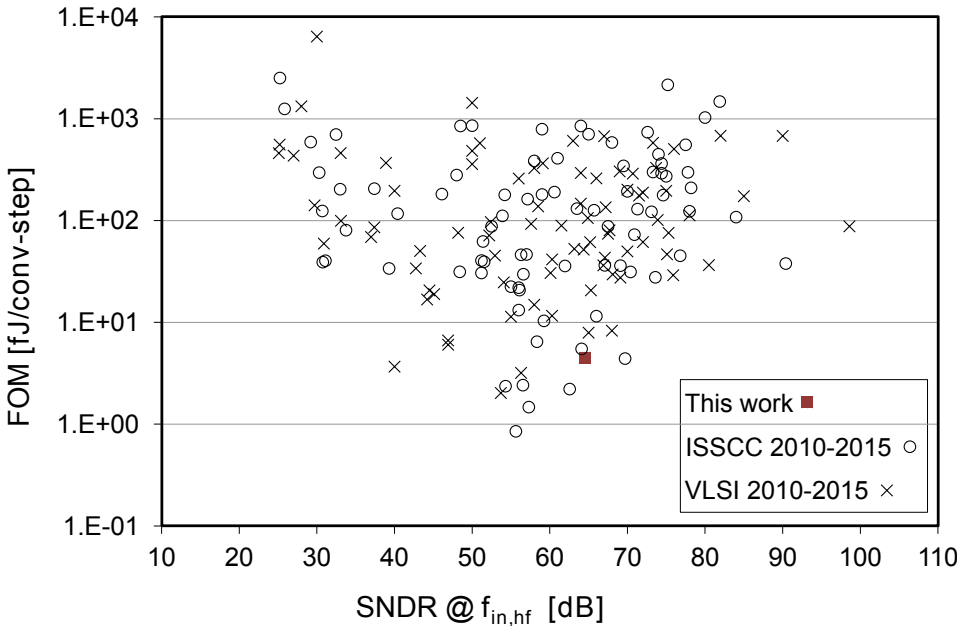

Figure 2.22: FOM versus SNDR plot for this work and recently published ADCs in ISSCC and VLSI conferences.

Chapter 3

Bidirectional Single-side Switching Technique

This chapter[1] presents a low-power SAR ADC with a bidirectional single-side (BSS) switching technique. Compared to the conventional SAR switching scheme, it reduces the DAC reference power and the total number of unit capacitors by 86% and 75%, respectively. It also minimizes the power dissipated in driving DAC switches as it has only one single-side switching event every comparison cycle. Compared to the monotonic switching technique [Liu et al. [2010a]] that also has only one switching event, it reduces the comparator input common-mode voltage variation by 2 times. Moreover, its comparator input common-mode voltage does not converge to ground but to V_{cm}. This greatly reduces the comparator offset and noise. It obviates the need for a specially designed comparator and allows the use of a low-power strong-arm latch. A prototype with proposed technique has been developed in 180nm CMOS.

This chapter is organized as follows: an introduction of existing switching techniques is first presented. The effect of comparator common-mode variation is

[1] This chapter is a partial reprint of the publication: Long Chen, Arindam Sanyal, Ji Ma and Nan Sun, "A 24-uW 11-bit 1-MS/s SAR ADC with a bidirectional single-side switching technique", *IEEE ESSCIRC*, pp. 219–222, 2014. I thank all the co-authors for their valuable advice in designing and testing of the prototype.

analyzed next. Finally, the proposed BSS switching technique is presented, followed by the prototype implementation and measurement.

3.1 Introduction

Successive approximation register (SAR) analog-to-digital converter (ADC) is scaling friendly and power efficient. It is suitable for low power and low voltage applications, such as wireless sensor networks, implantable bio-sensors, and portable medical electronics [Harpe et al. [2013]; Van Elzakker et al. [2010]; Verma and Chandrakasan [2006]; Zhang et al. [2012]]. It consists of a capacitive DAC, a comparator, and a SAR logic block. The DAC can take up a large portion of the total ADC power especially at high resolution with large capacitors. The conventional DAC switching technique based on trial and error is not power efficient. To address this issue, several low-power DAC switching techniques have been developed, including the split capacitor technique [Ginsburg and Chandrakasan [2005]], the V_{cm}-based switching technique [Zhu et al. [2010]], and the monotonic switching technique [Liu et al. [2010a]]. The split capacitor technique reduces DAC reference power by 37% compared to the conventional switching scheme. The V_{cm}-based switching technique reduces DAC reference power by 88%, but it requires additional switches to pass V_{cm}. Due to the reduced overdrive voltage, these switches need to be large, leading to increased power in driving these switches. This limitation is more pronounced at low power supply voltage and high conversion rate [Sanyal and Sun [2014]].

The monotonic switching technique of [Liu et al. [2010a]] has attracted in-

creasing attention as it reduces both the DAC reference power and power dissipated in driving switches. It achieves 81% reduction in DAC reference power. It does not need capacitor splitting or additional large switches. Moreover, it requires only one switching event every comparison cycle. Thus, its switching activity is only 33% of the conventional switching technique and 50% of the V_{cm}-based switching technique. In addition, it reduces the total number of unit capacitors by a factor of 2. Despite the merits mentioned above, monotonic switching has one key limitation. Its comparator input common-mode voltage decreases every comparison cycle and eventually converges to ground. Although a comparator with a PMOS input pair can be used to maintain functionality, the large change in the common-mode voltage causes varying comparator offset, resulting in ADC nonlinearity. In addition, the large overdrive voltage for the input pair leads to increased comparator noise and degrades the SNR. To address these issues, the authors of [Liu et al. [2010a]] designed a special comparator by stacking an extra tail transistor acting like a dynamic current source, so that the input pairs overdrive voltage can be kept relatively constant. However, this solution increases design effort and requires additional bias circuit. In addition, the proposed comparator consumes static power during the evaluation phase. Another approach to address the common-mode variation problem is to split MSB capacitors and switch two half capacitors on both sides of the DAC capacitor array every comparison [Liu et al. [2010b]]. This technique requires additional inverter for each split capacitor, which increases digital power and slows down speed. In addition, the number of switches also needs to be doubled for split bits, resulting in more layout efforts and more power dissipated on driving

the parasitic capacitors.

This chapter presents a bidirectional single-side (BSS) switching technique that maintains all the aforementioned merits of the monotonic switching technique and solves the large common-mode variation issue [Chen et al. [2014a]]. Instead of switching DAC capacitors from V_{ref} to ground monotonically as in [Liu et al. [2010b]], the proposed technique first switches the MSB capacitor from ground to V_{ref}, and then, switches other capacitors from V_{ref} to ground. Consequently, the range of comparator input common-mode variation is reduced by 2 times. More importantly, the common-mode voltage converges to V_{cm} instead of ground, which greatly reduces the comparator noise and offset variation. As a result, the proposed technique obviates the need for the specially designed comparator and permits the use of a low-power strong-arm latch as a comparator. Furthermore, the proposed switching method achieves an additional bit over monotonic switching by using V_{cm} as reference for the LSB capacitor. For the same resolution, the proposed technique reduces the total number of unit capacitors by 2 times compared to monotonic switching and 4 times compared to conventional switching. It reduces the DAC reference power by 86%, which is also more than that for monotonic switching.

An 11-bit prototype ADC using the proposed BSS switching technique is fabricated in 180nm CMOS process. To minimize power and area, the smallest available MIM capacitor of 2 fF is used as the unit capacitor. To ensure good matching, a segmented common-centroid layout with surrounding dummy capacitors is developed, which allows the ADC to achieve 77 dB of SFDR without any calibration. Operating at 1 MS/s, it consumes 24 μW of power under 1 V power

supply. It achieves 10.3-b ENOB and an FOM of 19.9 fJ per conversion step.

3.2 Effect of Comparator Common-Mode Variation

The strong-arm latch comparator in Fig. 3.1 is widely used in ADCs and memory read-out circuits [Kobayashi et al. [1993]; Van der Plas et al. [2006]]. Its input common-mode voltage strongly affects the comparator offset, noise, and speed [Wicht et al. [2004]; Nuzzo et al. [2008]]. Since the common-mode voltage variation is a key issue in both monotonic switching and the proposed BSS switching techniques, let us first analyze its effects on the comparator performance.

Fig. 3.2 shows a typical transient behavior of the comparator with a 1mV input differential voltage. When $clkc$ is low, the comparator is in reset with both $V_{X1,2}$ and $V_{outp,n}$ pulled to V_{DD}. When $clkc$ is high, the comparator is in evaluation mode. Here its operation can be divided into two phases, the pre-amplification phase and the latch regeneration phase as shown in Fig. 3.3, with the turn-on of the PMOS cross-coupled pair separating two phases. During the pre-amplification phase, the PMOS cross-coupled pair is in cut-off and the comparator works as a dynamic integrator. From differential-mode point of view, the comparator input voltage induces a differential drain current, which is integrated on the output capacitive load C_O and produces a differential output voltage V_{out} that grows linearly with time. From the common-mode point of view, $V_{X1,2}$ decrease after $clkc$ goes high. Once they reach $V_{DD} - V_{Tn3,4}$, M3 and M4 are turned on and $V_{outp,n}$ start to decrease. When $V_{outp,n}$ decrease to $V_{DD} - V_{Tp5,6}$, the PMOS crossed coupled pair is turned on and the comparator enters the latch phase. Since the PMOS crossed coupled pair is in

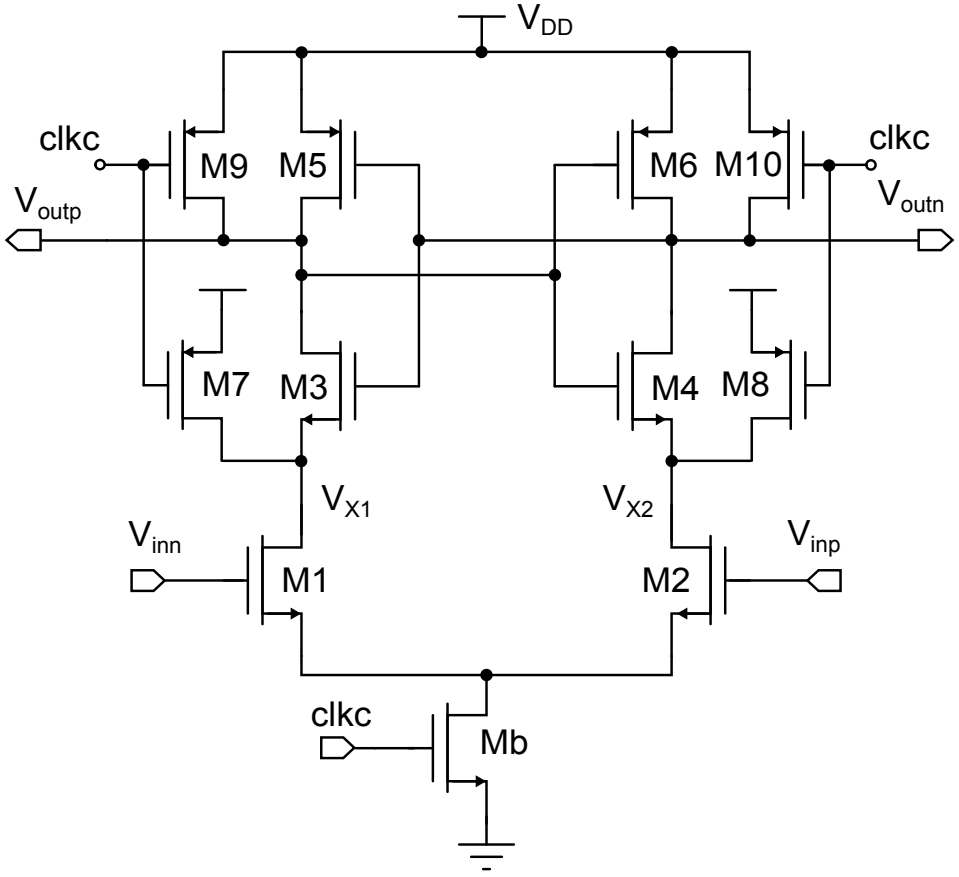

Figure 3.1: Schematic of a strong-arm latch comparator.

positive feedback and provides exponentially growing gain, the PMOS pair dominates the behavior of the comparator in the latch phase, while other transistors can be considered to the first order as a current source before V_{out} grows very large that cuts off a transistor in the PMOS pair or the current source.

A critical parameter that links the two phases is the pre-amplifier gain G, defined as the differential voltage gain of the comparator at the end of the pre-amplification phase. It affects the comparator offset and noise. We can model

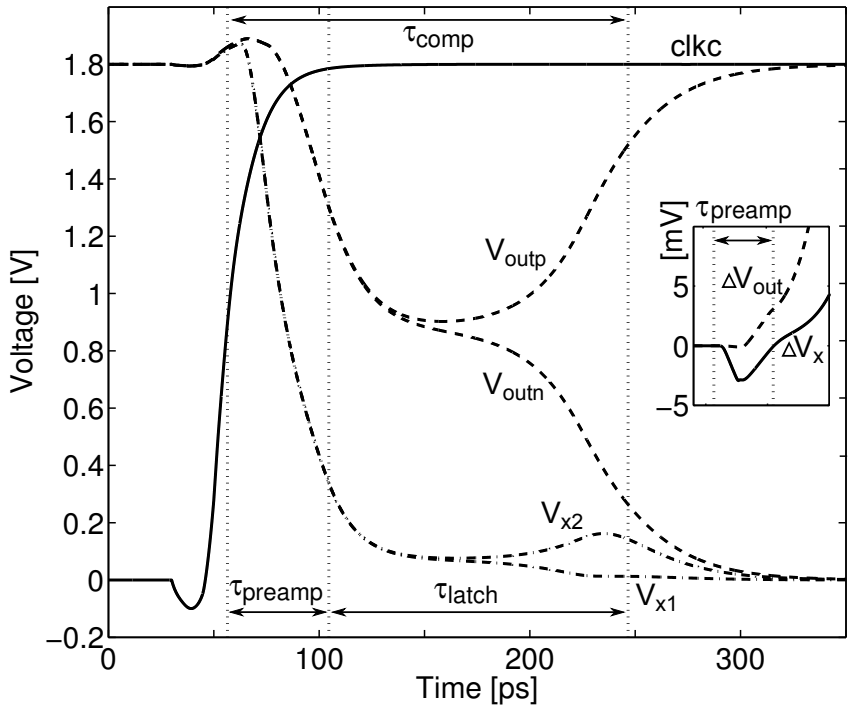

Figure 3.2: Transient behavior of a strong-arm latch comparator.

the input referred offset of the pre-amplification phase as $V_{os,preamp}$, whose main contributor is $V_{Tn1,2}$ mismatch in the input pair. For the latch phase, we can model its offset referred to the output nodes at the beginning of the latch generation phase as $V_{os,latch}$, whose main contributor is $V_{Tp5,6}$ mismatch in the PMOS cross coupled pair. As a result, the input referred offset of the entire comparator, V_{os}, is given by:

$$V_{os} = V_{os,preamp} + \frac{V_{os,latch}}{G} \tag{3.1}$$

In terms of root-mean-square (rms) offset, we have:

$$\sigma_{os} = \sqrt{\sigma^2_{os,preamp} + \frac{\sigma^2_{os,latch}}{G^2}} \tag{3.2}$$

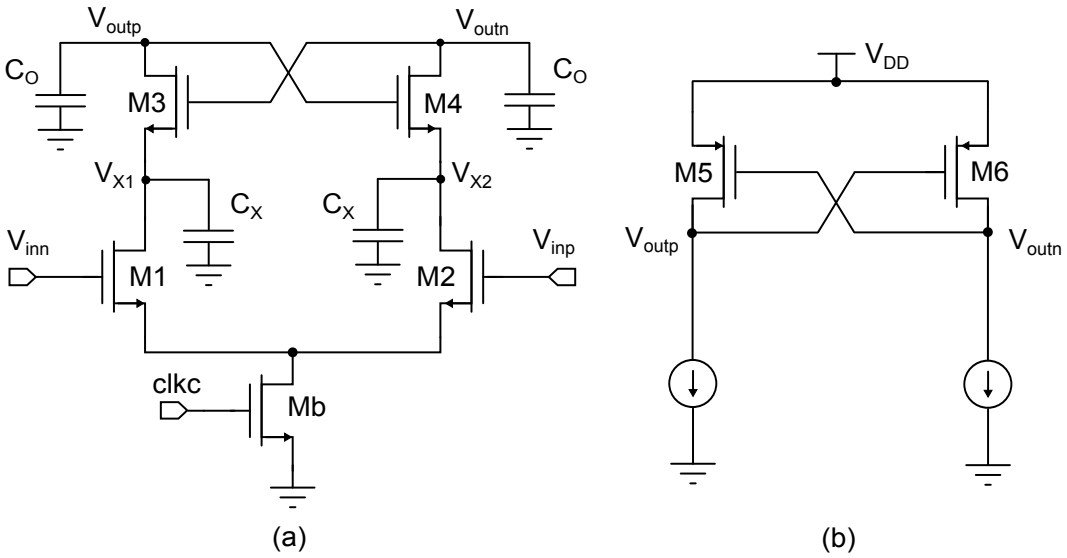

Figure 3.3: Comparator schematic for (a) the pre-amplification phase and (b) the latch regeneration phase.

Similarly, we can also write down the expression for the comparator noise:

$$\sigma_n = \sqrt{\sigma_{n,preamp}^2 + \frac{\sigma_{n,latch}^2}{G^2}} \tag{3.3}$$

From (3.1)-(3.3), we can see that the offset and noise depend strongly on G, and a large G is preferred as it attenuates the contribution from the latch phase. The value of G can be estimated to the first order in the following way. We first calculate the time duration τ_{preamp} of the pre-amplification phase by examining the common-mode voltage change. At the beginning of the pre-amplification phase, the common-mode voltages at $V_{outp,n}$ and $V_{X1,2}$ are both V_{DD}. By the end of the pre-amplification phase, the common-mode voltage at $V_{outp,n}$ and $V_{X1,2}$ are approximately $V_{DD} - V_{Tp5,6}$ and $V_{DD} - V_{Tp5,6} - V_{Tn3,4}$, respectively. For simplicity, assuming that the common-mode drain current of the comparator input pair I_D is

unchanged during the integration, we have:

$$\tau_{preamp} \approx \frac{C_O V_{Tp5,6} + C_X(V_{Tp5,6} + V_{Tn3,4})}{I_D} \tag{3.4}$$

where C_X and C_O are the total capacitive load at $V_{X1,2}$ and $V_{outp,n}$ (see Fig. 3.3). Similarly, assuming g_m of the input pair is unchanged during the integration, the total amount of differential charge ΔQ produced by the input pair with small input voltage ΔV_{in} is:

$$\Delta Q = \Delta I \cdot \tau_{preamp} \approx g_m \Delta V \cdot \tau_{preamp} \tag{3.5}$$

By the end of the integration phase, the majority of the differential charge ΔQ is at the output nodes $V_{outp,n}$ (the amount of differential charge at $V_{X1,2}$ is very small as shown in Fig. 3.2), and thus, we can derive G:

$$\begin{aligned} G &\approx \frac{\Delta V_{out}}{\Delta V_{in}} \approx \frac{\Delta Q / C_O}{\Delta V} \\ &\approx \frac{g_m}{I_D}\left\{ V_{Tp5,6} + \frac{C_X}{C_O}(V_{Tp5,6} + V_{Tp3,4}) \right\} \end{aligned} \tag{3.6}$$

Since the comparator input common-mode V_{cmi} determines g_m/I_D of the input transistor, it has a strong influence on G. To increase G and reduce offset and noise, we prefer a small V_{cmi}. To verify the analysis above, SPICE simulation is performed in 0.18-μm CMOS process with $V_{DD} = 1.8V$. G is extracted by examining the voltage difference at $V_{outp,n}$ when the output common-mode drops to $V_{DD} - V_{Tp5,6}$. Fig. 3.4(a) shows that G depends strongly on V_{cmi}. It decreases from 12.6 at $V_{cmi} = 0.6V$ to 0.6 at $V_{cmi} = 1.8V$. Also, g_m/I_D proportionally decreases as V_{cmi} increases. These results match (3.6). σ_{os} and σ_n are extracted from Monte Carlo and transient noise simulations, respectively. Fig. 3.4(b) shows that they both

increase with V_{cmi} due to the reduction in G. Fig. 3.4(c) plots their square as a function of $1/G^2$. The close linear fitting with a fitting coefficient $r > 0.99$ clearly validates the models of (3.1)-(3.3).

V_{cmi} also strongly affects the comparator resolve time τ_{comp} defined here as the time it takes for the comparator output differential voltage to reach $0.7V_{DD}$. Fig. 3.4(d) shows τ_{comp} as a function of V_{cmi} for a fixed 1mV input. τ_{comp} decreases as V_{cmi} increases, which can be explained by (3.4) as a larger I_D shortens the pre-amplification phase τ_{comp}. An interesting observation is that the minimum τ_{comp} is not obtained at $V_{cmi} = V_{DD}$. The reason is that if V_{cmi} is too large, the time duration of the latch regeneration phase is longer due to the reduction in G [Wicht et al. [2004]]. In addition, the comparator power P_{comp} depends mildly on V_{cmi}, as shown in Fig. 3.4(e). The reason is that a large V_{cmi} leads to increased short circuit current.

Overall, a small V_{cmi} is preferred for small offset, low noise, and low power, but it leads to slow speed. This represents a trade-off in the choice of V_{cmi}. To provide a holistic evaluation of the comparator performance, we can define a comparator figure-of-merit FOM_{comp} shown below:

$$FOM_{comp} = \frac{1}{\sigma_n^{\alpha} \times \tau_{comp}^{\beta} \times P_{comp}^{\gamma}} \tag{3.7}$$

where α, β and γ are weighting factors to be determined by the designer. For example, for noise optimized design, we can give more weight to σ_n by having a larger α. Or if speed is the top priority, we can emphasize τ_{comp} in FOM_{comp} by enlarging β. For a balanced design with $\alpha = \beta = \gamma = 1$, FOM_{comp} is plotted

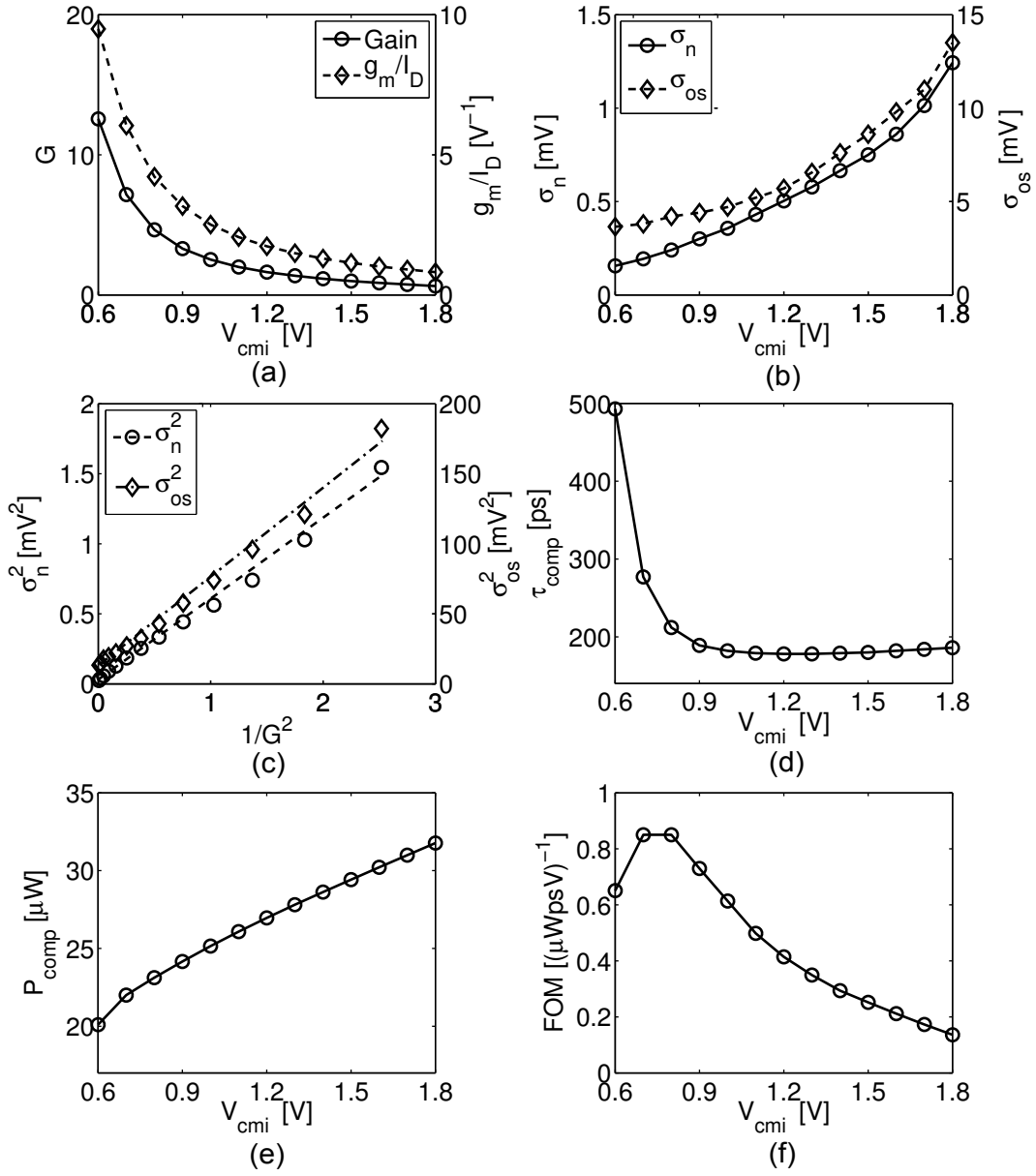

Figure 3.4: Simulated comparator performance: (a) G and g_m/I_D; (b) noise and offset; (c) linear fitting for noise and offset with $1/G^2$; (d) resolve time; (e) power and (f) FOM_{comp}.

shown in Fig. 3.4(f). Its optimum is at around $V_{cmi} = 0.8V$, which is more than 6 times larger than that at $V_{cmi} = 1.8V$.

3.3 Proposed BSS switching technique

Fig. 3.5 shows an example of the proposed bidirectional single-side (BSS) switching technique applied to a 4-bit top-plate sampled SAR ADC. During the sampling phase, the input is sampled onto the DAC array with the $2C$ MSB capacitor connected to ground and other capacitors connected to V_{ref}. Since the input is available at the comparator input, the MSB decision can be made immediately after the sampling phase. Depending on the comparison result, one side of the $2C$ MSB capacitors is switched from ground to V_{ref}. Following the second comparator decision, one side of the second MSB capacitor (the middle capacitor C) is switched from V_{ref} to ground. After the third comparison, one side of the LSB capacitor (the rightmost capacitor C) is switched from V_{ref} to V_{cm}. Finally, the fourth comparison is launched. This operation scheme can be easily generalized for more number of bits and also bottom-plate sampling.

3.3.1 Comparator input common-mode variation reduction

The key limitation for monotonic switching is that its comparator input common-mode voltage V_{cmi} monotonically decreases from V_{cm} to ground, which requires the use of a specially designed comparator with a PMOS input pair. Note that there exists a complementary version for the original monotonic switching by connecting all DAC capacitors initially to ground. This way, V_{cmi} monotonically

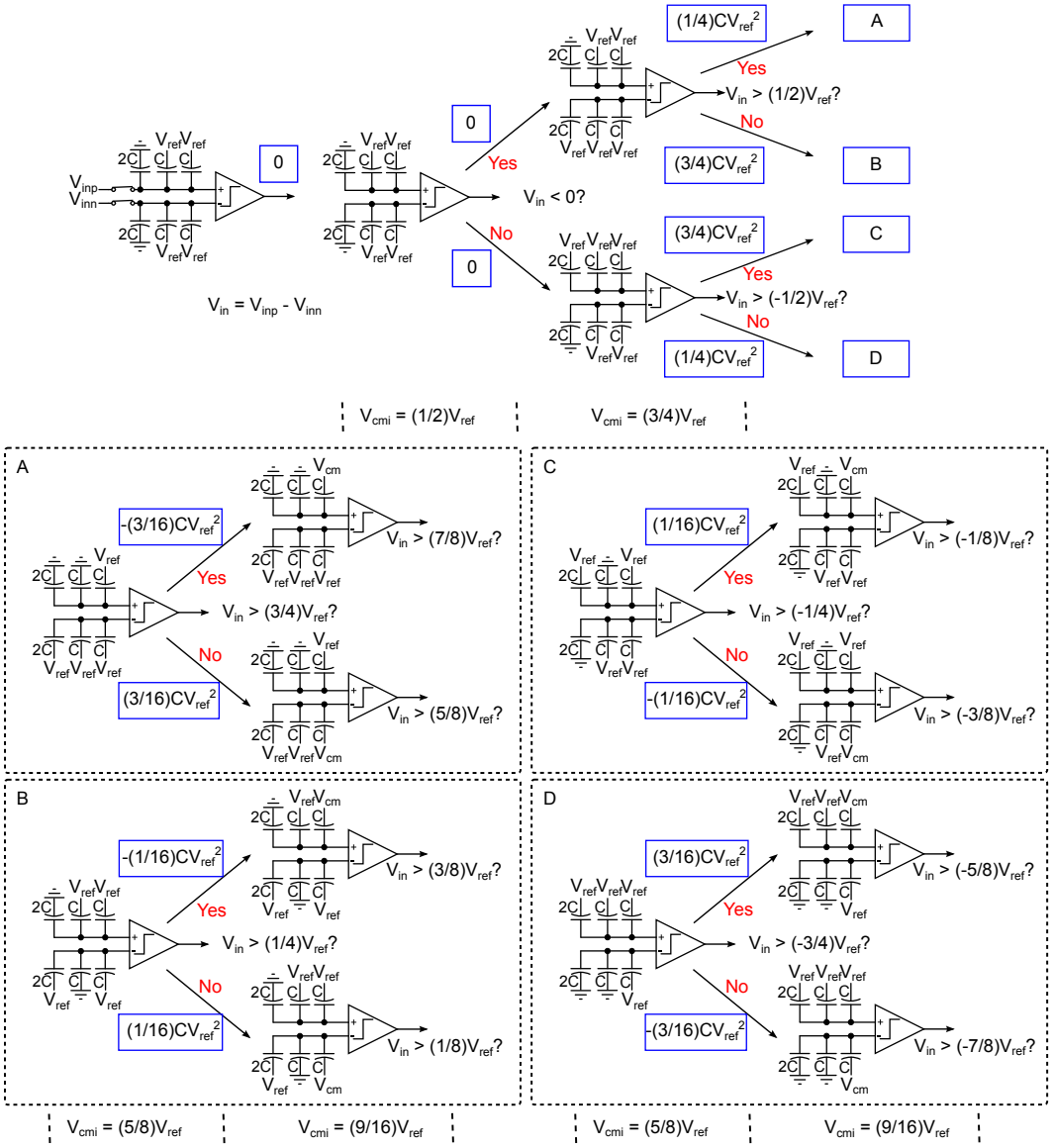

Figure 3.5: Proposed bidirectional single-side switching technique.

increases from V_{cm} to V_{DD}, which permits the use of the strong-arm latch comparator with an NMOS input pair. However, as shown in Fig. 3.4, having $V_{cmi} = V_{DD}$ results in large comparator offset and noise.

Fig. 3.6 shows the variation of V_{cmi} for an 11-bit SAR ADC with different switching schemes. Note that V_{cmi} depends on the comparison cycle but is independent from V_{in}. For the proposed bidirectional up-down switching of Fig. 3.5, V_{cmi} first increases, then decreases, and finally converges to V_{cm}. As a result, compared to monotonic switching, the amount of V_{cmi} variation is reduced by a factor of 2. Furthermore, because V_{cmi} converges to V_{cm}, the comparator noise and offset are significantly reduced. To compare the ADC performance with monotonic up switching and the proposed switching technique, a behavioral model for an 11-bit SAR ADC is built in MATLAB using the strong-arm latch comparator parameters extracted via SPICE simulation (see Fig. 3.4). For simplicity, other components in the SAR ADC are assumed to be ideal.

In a conventional SAR ADC, V_{cmi} is fixed, and thus, the comparator offset is a constant and does not affect the ADC linearity. By contrast, in both monotonic switching and the proposed switching schemes, V_{cmi} changes every comparison cycle, which leads to varying comparator offset (see Fig. 3.4) and degrades the ADC linearity. To examine the influence of offset variation, we first perform 1000-time Monte Carlo simulations for the 11-bit ADC with V_{cmi} dependent offset variation but no noise. The SNDR histograms are shown in Fig. 3.7. Since V_{cmi} in monotonic switching changes from V_{cm} to V_{DD}, it leads to large varying offset, which significantly degrades the ADC SNDR. For the proposed switching scheme, since its V_{cmi} variation is only $V_{DD}/4$ and it starts from V_{cm} and ends at V_{cm}, its SNDR is much higher. However, because V_{cmi} still undergoes large changes in the first several MSB comparisons, there are still appreciable SNDR degradations in cases

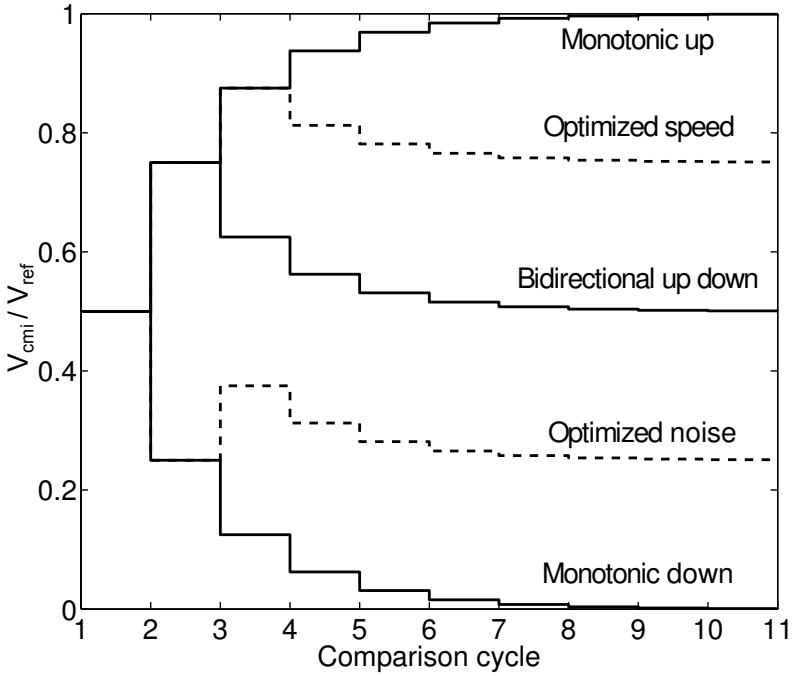

Figure 3.6: Comparator input common-mode variation for different switching techniques.

where the comparator offsets are large and have considerable variations. To solve this problem, a small redundant capacitor can be added after the 6th MSB capacitor, which corrects the errors due to offset variations in the first 6 comparisons. For the comparisons afterwards, the change in V_{cmi} is within $V_{ref}/128$, and thus, the comparator offset variation is negligible and does not degrade SNDR. Fig. 3.8 shows the simulation results with redundancy added. The performance for the ADC with the proposed switching scheme is fully restored. The ADC performance for the monotonic switching is also improved, but there is still about 20% probability for having less than 67 dB SNDR. Although adding redundancy can effectively ad-

dress the offset variation problem, it cannot solve the SNDR loss due to increased comparator noise. For monotonic up switching, because V_{cmi} converges to V_{DD}, its comparator noise is much larger than that for the proposed technique especially for the last several noise sensitive LSB comparisons. This leads to SNDR degradation. Fig. 3.9 shows the simulated SNDR histograms with offset, noise, and redundancy. The average SNDR for monotonic switching is 60 dB, while that for the proposed switching is 67 dB. Note that this 7 dB SNDR improvement comes without any penalty in the comparator power. Moreover, assuming a target SNDR of 63 dB as in our prototype, the proposed switching technique can achieve close to 100% yield, while that for the monotonic switching is less than 10%.

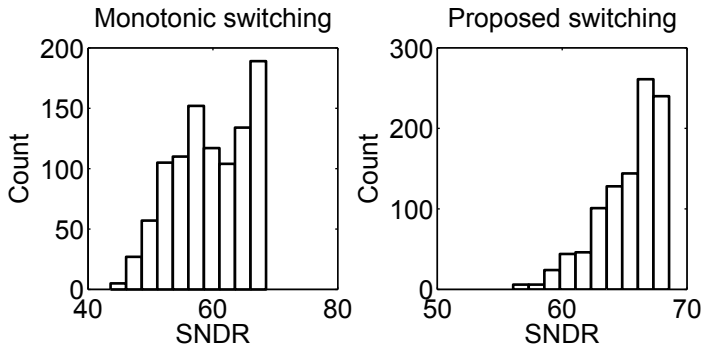

Figure 3.7: Simulated SNDR with comparator offset variation.

3.3.2 Comparator input common-mode voltage optimization

The proposed switching technique can be generalized to allow the comparator common-mode voltage to converge to any desired voltage. It provides designers the freedom to optimize the comparator for different design specifications. For example, for low-speed high-resolution applications, it is desirable to reduce V_{cmi} to

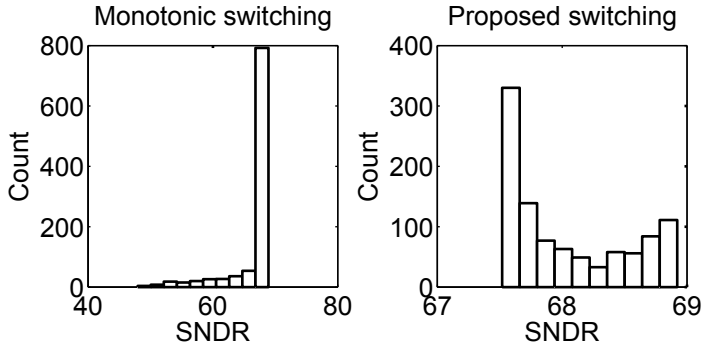

Figure 3.8: Simulated SNDR with both comparator offset variation and a redundant capacitor after the 6th MSB capacitor.

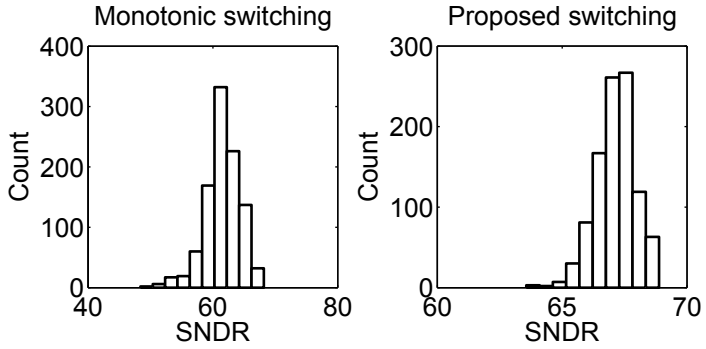

Figure 3.9: Simulated SNDR with comparator offset variation, noise and a redundant capacitor after the 6th MSB capacitor.

minimize the comparator noise (see Fig. 3.4). To this end, we can initialize the DAC array in such a way that the second MSB capacitor is connected to ground while all other capacitors are connected to V_{ref}. As a result, during DAC switching, V_{cmi} first goes down, then goes up, and finally goes down to $0.25 \times 1.8 = 0.45V$ (see Fig. 3.6). In this configuration, the simulated comparator input referred noise is only 100 μV, which is 70% less than that for $V_{cmi} = 0.9V$. For high-speed medium-resolution applications, it is preferred to place V_{cmi} at higher voltages (see

Fig. 3.4). This can be achieved by letting V_{cmi} go up during the first two MSB comparisons and then go down, as shown in Fig. 3.6. This way, V_{cmi} converges to $0.75V_{DD}$, leading to a 10 ps shorter comparator resolve time. Note that the speed improvement by adjusting V_{cmi} can be more significant in advanced technology nodes with low power supply voltage.

3.3.3 Capacitance reduction

For the 4-bit SAR ADC shown in Fig. 3.5, the proposed BSS switching technique requires a total capacitance of only $8C$. By contrast, the conventional switching technique requires in total $32C$ and the monotonic switching requires $16C$. Thus, for a fixed unit capacitor size which is often determined by matching accuracy and/or the fabrication technology, the proposed technique reduces the total DAC capacitance by 4 times, leading to reduced chip area and power. When designed for the same kT/C noise with a fixed total DAC capacitance, the proposed technique allows a 4 times bigger unit capacitor, which provides better matching and simplifies layout design.

3.3.4 Reduced DAC reference energy

The energy required from V_{ref} during each DAC switching is shown in blue boxes along the arrows in Fig. 3.5. The proposed technique consumes zero energy during the switching of the MSB capacitor, as it involves only charge redistribution [Sanyal and Sun [2014]]. For the 4-bit case using the proposed technique, the average reference energy during the comparison phase is $(0.5CV_{ref}^2$. Once all con-

versions finish, the DAC array needs to be reset to initial condition for sampling, which dissipates an additional energy of $1.75CV_{ref}^2$. Thus, the total reference energy is $2.25CV_{ref}^2$. For an n-bit SAR ADC, the total reference energy including both comparison and reset phases is:

$$E_{ref} = (2^{n-3} + \sum_{i=2}^{n-1} 2^{n-3-i} - \frac{1}{2})CV_{ref}^2 \tag{3.8}$$

For an 11-bit prototype ADC, the reference energy for different output codes is plotted in Fig. 3.10. On average, the conventional switching technique consumes $2729CV_{ref}^2$. The monotonic switching technique consumes $512CV_{ref}^2$. The proposed technique consumes $383CV_{ref}^2$, which is 86% and 25% smaller than the conventional and monotonic switching schemes, respectively.

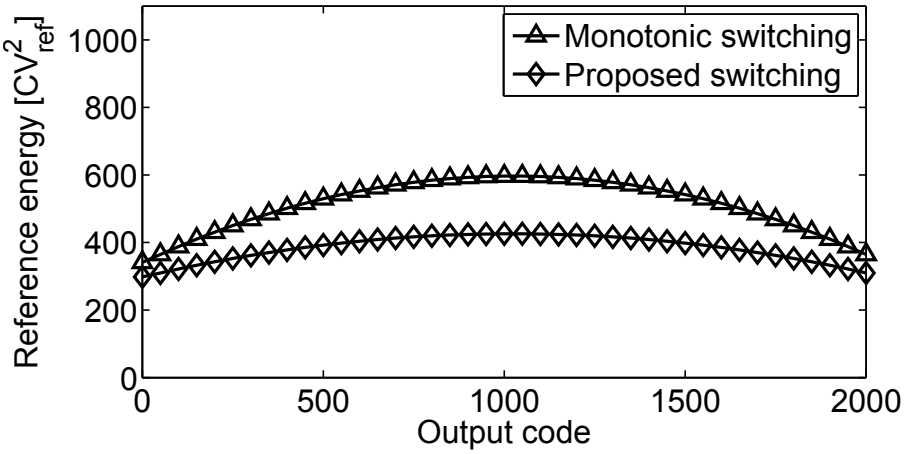

Figure 3.10: DAC reference energy for an 11-bit SAR ADC with different output codes.

Compared to monotonic switching, the proposed BSS switching technique requires an additional reference voltage V_{cm}, but the V_{cm} generator does not need

to deliver a large current as it is only connected to the small LSB capacitor (see Fig. 3.5). It is interesting to note that the averaged energy drawn from V_{cm} is 0. The reason is that V_{cm} sends energy (charge) to the DAC for 50% of the time while it receives energy (charge) from the DAC for the rest of the time. Thus, a large capacitor can be placed at V_{cm} to average out the charges, and output resistance for the V_{cm} generator can be large. This reduces the power and the design effort for the V_{cm} generator. Moreover, since V_{cm} is used only for the LSB comparison, it does not need to be accurate. Simulation shows that 5% deviation in V_{cm} only results in a DNL error of 0.05 LSB. This further simplifies V_{cm} generation.

3.4 Prototype ADC Design

A prototype implementing the proposed bidirectional single-side switching technique was designed in 180nm CMOS process. The following subsections provide detailed description of the prototype.

3.4.1 Detailed circuit schematics

Fig. 3.11 shows an 11-bit SAR ADC using the proposed BSS switching technique.

The capacitive DAC is implemented using binary-weighted capacitors. A redundant capacitor $C_3 = 8C$ is added to recover conversion errors during the first several MSB comparisons with large comparator common-mode variations. The total capacitance including both sides of the DAC array is $1040C$ for the proposed technique, which is 4 times smaller than that for the conventional switching tech-

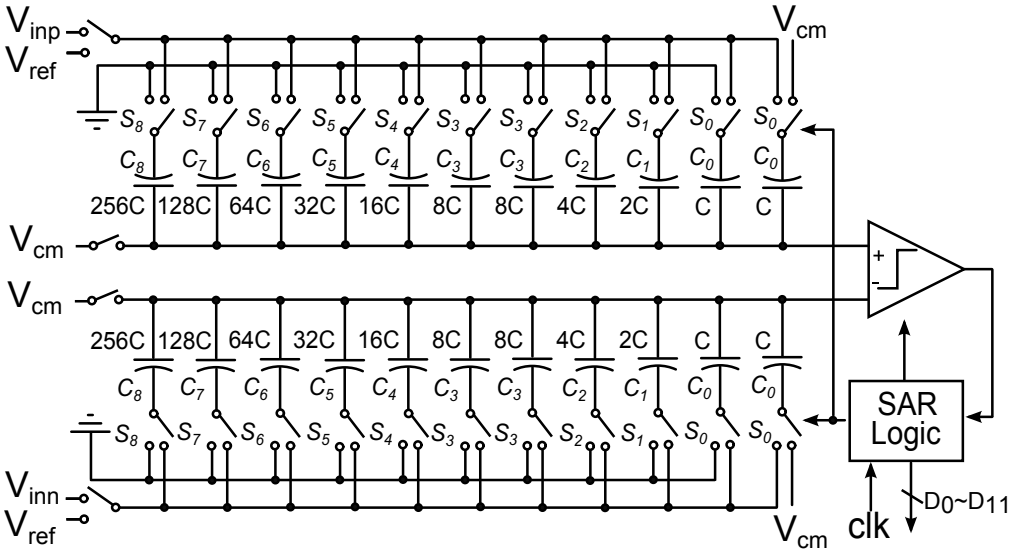

Figure 3.11: Architecture of the 11-bit prototype SAR ADC.

nique that requires $4096C$. In our design, the size of the unit capacitor is limited by matching requirement. For our proposed BSS switching technique, the equivalent LSB capacitor size is $0.5C$ due to the use of V_{cm}. To ensure that the worst case DNL is within 1 LSB, we have [Lin and Bult [1998]; Harpe et al. [2011]]:

$$3\sigma_{DNL} = 3\frac{\sqrt{1040}}{0.5}\sigma_u < 1 \tag{3.9}$$

where σ_u is the unit capacitor mismatch in percentage. From (9), has to be smaller than 0.5%. This translates to the minimum MIM capacitor size of 2 fF based on foundry provided mismatch data. Out of serendipity, the smallest available MIM capacitor is also 2 fF. Thus, it is chosen as the unit capacitor size. The total DAC capacitance is 2 pF. The kT/C noise of about 100 μV does not limit the performance of the ADC with an LSB size of 1.8 mV under $V_{DD} = 1.8V$.

Since the unit capacitor size is only 2 fF, the routing parasitic capacitors

have a considerable influence on the capacitor matching accuracy. Although digital calibration techniques can be used to compensate capacitor mismatches [Chen et al. [2014b]; Ragab et al. [2015]; Chang et al. [2013]], they increase design complexity and digital power. In this design, a segmented common-centroid layout technique is used to simplify the routing, thus minimizing the parasitic capacitors of the routing wires. Fig. 3.12 shows the floor plan for a single side capacitor array. The capacitors are separated into two groups $\{C_8, C_7, ..., C_3\}$ and $\{C_3, C_2, C_1, C_0\}$. The common-centroid rule is applied horizontally for the first group and vertically for the second. The second group is placed at the right side of capacitor array instead of at the center [Liu et al. [2010a]] to simplify routing. Dummy cells, represented as D, are added for better matching. The capacitors' top plates are connected using the highest metal M6 while the bottom plates are connected using a lower metal M2. This minimizes the parasitic capacitors between routing wires. Post-layout simulation shows that with the proposed layout, the ADC is able to achieve an INL within ± 0.5 LSB and an SFDR of 79 dB.

Bottom plate sampling is used to ensure high linearity. The sampling switch is implemented as a transmission gate, and an NMOS switch is used to pass V_{cm}. Both the transmission gate and NMOS switch are sized large enough to reduce resistance and ensure linearity.

The comparator is a strong-arm latch (see Fig. 3.1). No pre-amplifier is used. Based on simulation, the comparator rms input referred noise is 300 μV at $V_{cmi} = 0.9V$ under 1.8 V power supply. The comparator outputs are connected to two nearby inverters that isolate the comparator output nodes from other loading

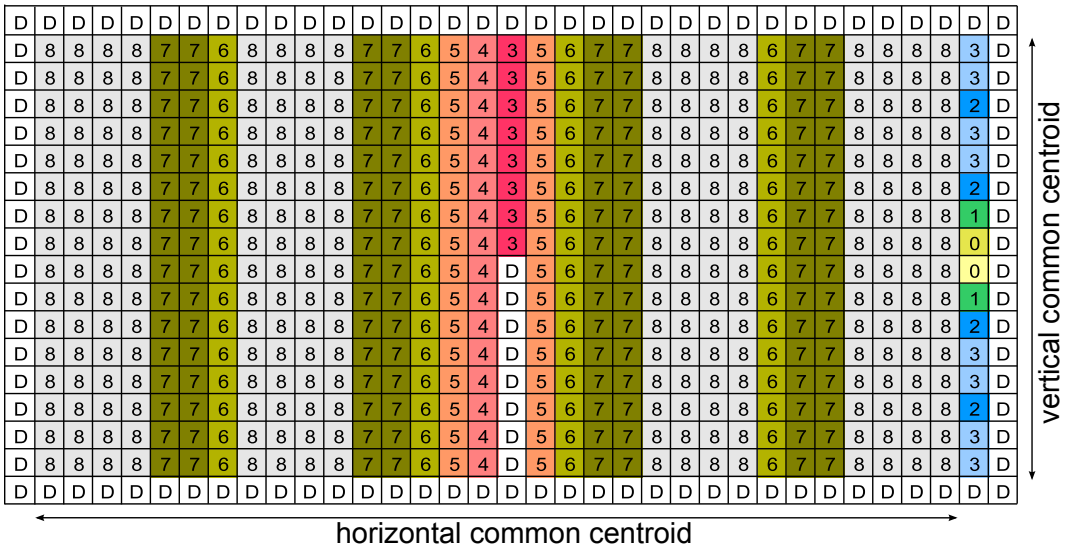

Figure 3.12: DAC capacitor array floor plan.

components, which reduces offset due to load mismatch. An XOR gate follows the inverters to generate a valid signal to trigger the SAR logic.

Since the target ADC sampling rate is low, a synchronous SAR logic is used for simplicity and robustness. Similar to [Zhang et al. [2012]], a 4-bit counter and a decoder are used to generate the sampling clock $clks$ and comparator clock $clkc$. To perform the proposed switching technique, a modified SAR logic is developed as shown in Fig. 3.13(a). It is built with a ring counter and a data register. It produces the initial control sequence of $\{0, 1, 1, ..., 1\}$ for the DAC at the end of the sampling phase. Once the comparator resolves after the first comparison, a valid signal is generated and triggers the ring counter. It then triggers the corresponding DFF in the data register to store the comparator output, which also serves as the DAC control signal to perform the proposed switching technique until the last

comparison.

As shown in Fig. 3.13(b), a gated inverter is used as the DAC control switch. During the sampling phase with $clks$ being high, the DAC switch is disabled, and thus, it does not disturb the bottom plate sampling. During the comparison phase with $clks$ being low, the capacitor is switched between V_{ref} and ground depending on the control signal. The sizes of the top three MSB switches are scaled according to their connected capacitor sizes. The LSB switch is sized 4 times the minimum size due to its reduced overdrive voltage when passing V_{cm}. Other switches have the same minimum size since the settling requirements are relaxed with small capacitors. All digital gates are optimized based on the method of logical efforts.

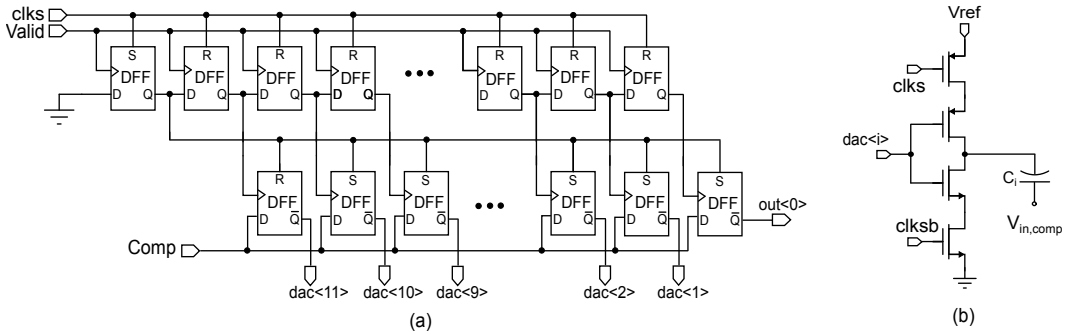

Figure 3.13: Schematic for (a) the SAR logic and (b) the DAC switch.

3.4.2 Measurement Results

The prototype SAR ADC is fabricated in 0.18-μm CMOS process. Fig. 3.14 shows the die photo. The active area is 0.1 mm^2. The rest of the chip area is filled with de-coupling capacitors and metal fills. The power supply is 1.8V and the sampling rate is 1.05 MS/s. Fig. 3.15 shows the measured DNL and INL,

which are $+0.56/-0.83$ LSB and $+0.64/-0.69$ LSB. The major INL jumps occur at first and second MSB transitions, which are due to capacitor mismatches. The measured SNDR and SFDR are 64.3 dB and 78.7 dB, respectively. No calibration is performed. To evaluate the influence of process variation, 4 chips are randomly picked and tested. Their measured SNDR and SFDR are consistently beyond 64 dB and 78 dB. The measured total power consumption is 60.4 μW at $V_{DD} = 1.8$V.

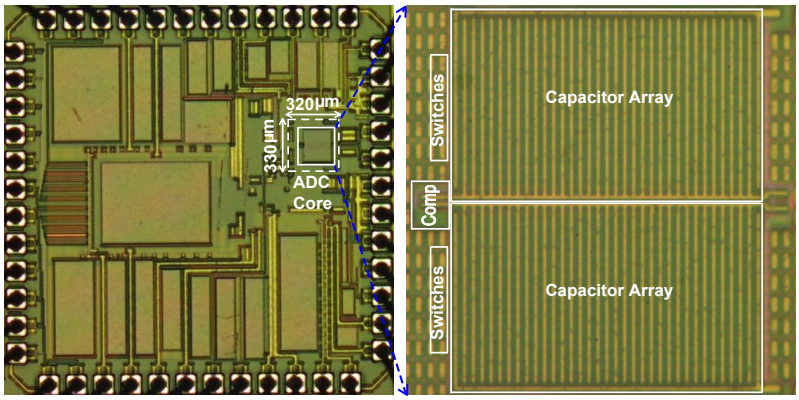

Figure 3.14: Die micrograph and zoomed view.

To reduce the power consumption, the measurements are repeated with a reduced power supply of 1V while maintaining the same sampling rate of 1.05 MS/s. Fig. 3.16 shows the measured spectrum with 500 kHz full-scale input at $V_{DD} = 1V$. SNDR and SFDR are 63.4 dB and 76.6 dB, respectively.

Fig. 3.17 shows the measured SNDR and SFDR versus the input amplitude. The SNDR is limited by noise rather than distortion. Fig. 3.18 shows the SNDR and SFDR versus the input frequency. The SNDR stays almost constant at 63 dB.

Comparator noise plays a key role in the resolving accuracy. To verify the

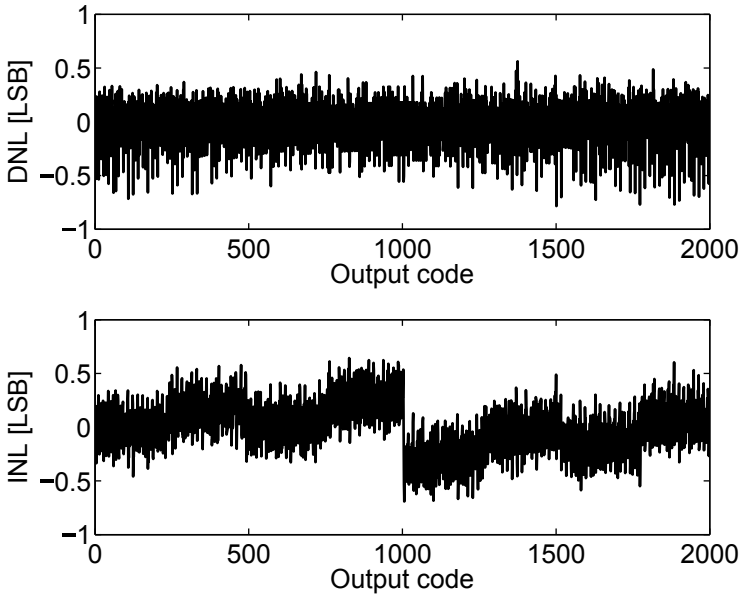

Figure 3.15: Measured DNL and INL.

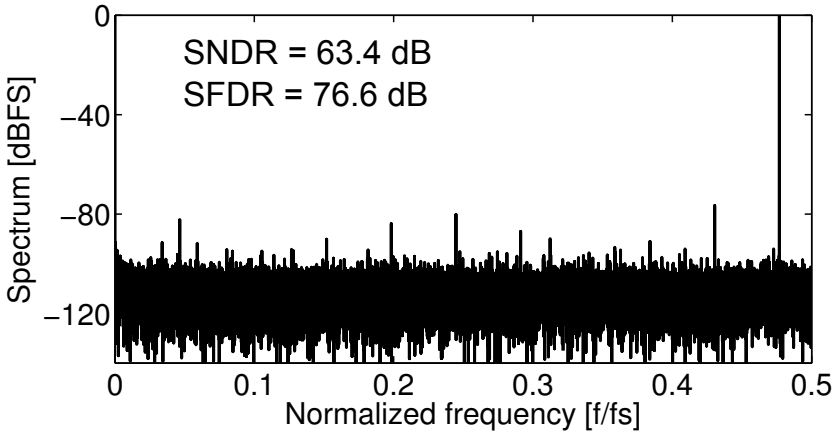

Figure 3.16: Measured 65536-point FFT spectrum with V_{DD} = 1V.

analysis, we vary the comparator input common-mode voltage V_{cmi} and measure ADC output D_{out} at $V_{in} = 0$V. The measured probability densities for D_{out} at

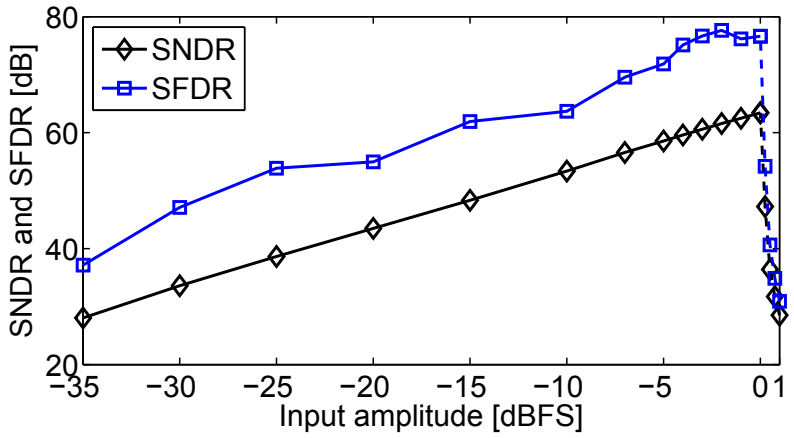

Figure 3.17: Measured SNDR and SFDR versus input amplitudes.

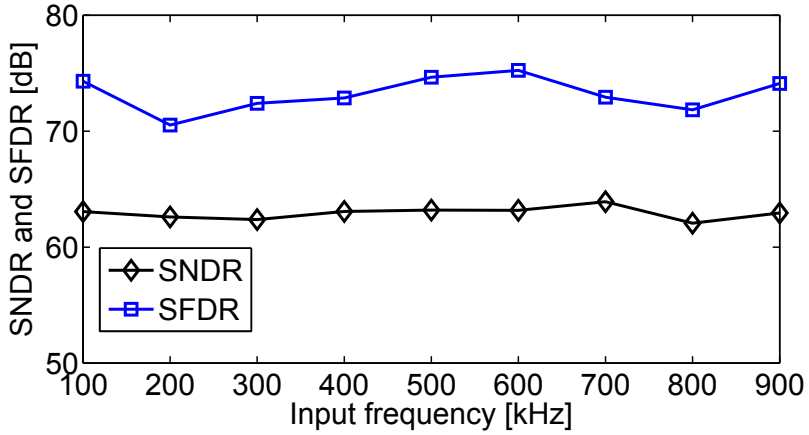

Figure 3.18: Measured SNDR and SFDR versus input frequencies.

$V_{DD} = 1$V with $V_{cmi} = 0.4$V and $V_{cmi} = 0.9$V are shown in Fig. 3.19 together with the fitted normal distributions. When $V_{cmi} = 0.4$V, D_{out} is centered at code 1051 and spread over only 3 bins with a standard deviation of 0.36 LSB. By contrast, when V_{cmi} is increased to 0.9V, D_{out} is centered at code 1049 and spread over 8 bins with a standard deviation of 0.70 LSB. The shift of D_{out} center indicates the

comparator offset variation, which is due to V_{cmi} induced preamplifier gain change as explained in (3.1). The increase in the ADC noise, which is dominated by the comparator, is also the result of preamplifier gain reduction as explained in (3.3). Fig. 3.20 shows the measured ADC rms noise with different V_{cmi}. It clearly shows that a larger V_{cmi} leads to increased comparator noise, which matches well with the analysis.

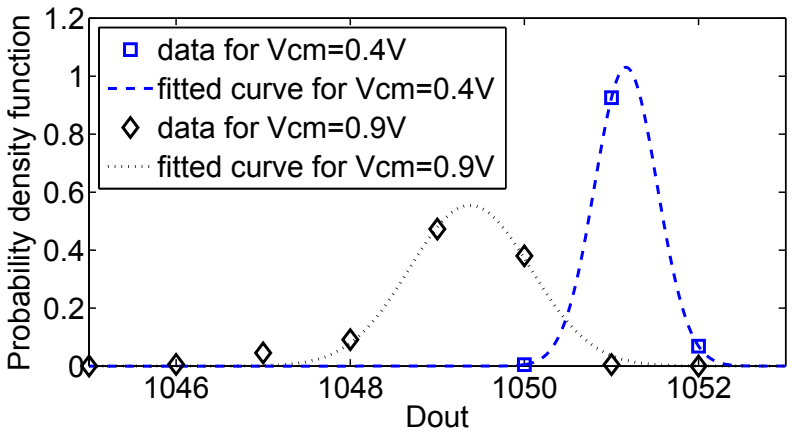

Figure 3.19: Measured D_{out} distribution with $V_{cmi} = 0.4V$ and $V_{cmi} = 0.9V$.

The measured total ADC power is 24 μW at $V_{DD} = 1$V. The DAC, the comparator, and the SAR logic consume 5.8 μW, 8 μW, and 10.2 μW, respectively. The DAC reference power accounts for 24% of the total power. This compares favorably to other works with conventional switching technique, such as [Zhang et al. [2012]] whose DAC power is 62% of the total power. The figure-of-merit (FOM) is 19.9 fJ/conversion-step.

Table 3.1 summarizes the ADC performance under both 1.8V and 1V power supplies. Table 3.2 compares it with recent works with similar power supply volt-

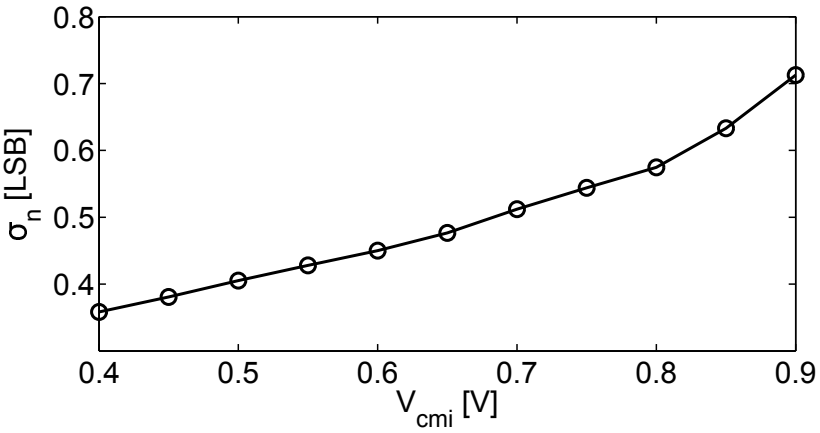

Figure 3.20: Measured D_{out} standard deviation with different V_{cmi} at $V_{in} = 0$V.

ages and sampling rates. This prototype ADC achieves the state-of-the-art performance, especially considering its relatively old 180 nm process.

Table 3.1: Measured performance summary

Process [nm]	180	
Sampling rate [MS/s]	1	
Resolution [bit]	11	
Input capacitance [pF]	2.1	
Active area [mm^2]	0.1	
Power supply [V]	1.8	1.0
DNL [LSB]	+0.56/-0.83	+0.53/-0.85
INL [LSB]	+0.64/-0.69	+0.68/-0.91
SNDR [dB]	64.3	63.4
SFDR [dB]	78.7	76.6
ENOB [bit]	10.4	10.3
Power breakdown		
DAC power [μW]	11.5	5.8
Comparator power [μW]	20.1	8.0
SAR logic power [μW]	28.8	10.2
Total power [μW]	60.4	24.0

Table 3.2: Performance comparison

	Liu et al. [2010a]	Liu et al. [2010b]	Huang et al. [2013]	Harpe et al. [2011]	Chang et al. [2013]	Kuo and Hsieh [2011]	This work
Process [nm]	130	180	90	90	65	180	180
Supply voltage [V]	1.2	1.0	1.0	1.0	1.2	0.9	1.0
Sampling rate [MS/s]	50	10	30	10	50	1	1
Resolution [bit]	10	10	10	8	12	10	11
ENOB [bit]	9.2	9.8	9.2	7.8	10.9	8.4	10.3
Power [μW]	826	98	980	26.3	2090	7.2	24
FOM [fJ/conv-step]	29	11	57	12	21.9	21.6	19.9

Chapter 4

Low-power and High-speed Single-channel SAR ADC

This chapter presents a low-power and high-speed single-channel SAR ADC. It uses a loop-unrolled architecture with multiple comparators. Each comparator is used not only to make a comparison but also to store its output and generate an asynchronous clock to trigger the next comparator. The SAR logic is significantly simplified to increase speed and reduce power. The comparator offset and decision time are optimized with a bidirectional single-side switching technique by controlling the input common-mode voltage V_{cm}. To remove the nonlinearity due to comparators' offset mismatch, a simple and effective V_{cm}-adaptive offset calibration technique is proposed. A 40nm prototype ADC achieves 35dB SNDR and 48dB SFDR at 700MS/s sampling rate. It consumes 0.95mW, leading to a Walden FOM of 30fJ/conv-step.

This chapter is organized as follows: an introduction of existing high speed SAR ADC design techniques is first presented. The proposed SAR ADC architecture is shown next. Finally, the detailed prototype ADC implementation and

[0]This chapter is a partial reprint of the publication: Long Chen, Kareem Ragab, Xiyuan Tang, Jeonggoo Song, Arindam Sanyal, and Nan Sun, "A 0.95-mW 6-b 700-MS/s single-channel loop-unrolled SAR ADC in 40-nm CMOS," to appear in IEEE Transactions on Circuits and Systems II (TCAS–II). I thank all the co-authors for their valuable advice in designing and testing of the prototype.

measurement are presented.

4.1 Introduction

High-speed low-resolution analog-to-digital converters (ADCs) are required by many demanding applications, such as high speed serial link transceivers and communication systems. Compared with pipelined and $\Delta\Sigma$ ADCs, SAR ADCs are more power efficient and scaling friendly due to their mostly digital architecture. Several techniques have been developed to increase the speed of SAR ADCs [Jiang et al. [2012]; Chen and Brodersen [2006]; Yang et al. [2010]; Wei et al. [2012]; Hong et al. [2015]; Kull et al. [2013]; Tai et al. [2014b]; Lin et al. [2010]; Chen et al. [2013]; Rahman et al. [2014]; Verbruggen et al. [2012]]. The first asynchronous SAR ADC was proposed in [Chen and Brodersen [2006]] to shorten the time duration of each comparison cycle. The SAR ADC speed can also be improved by using multi-bit-per-cycle architectures to reduce the number of comparisons, however at the cost of increased hardware complexity [Wei et al. [2012]; Hong et al. [2015]]. Other effective high-speed techniques include using alternate comparators to save the comparator reset time [Kull et al. [2013]] or pipelining two-stage SAR ADCs [Tai et al. [2014b]]. Recently, several works arrange multiple comparators to further increase the speed [Jiang et al. [2012]; Lin et al. [2010]; Chen et al. [2013]; Rahman et al. [2014]; Verbruggen et al. [2012]]. A binary-search ADC was proposed in [Lin et al. [2010]], which describes a transitional structure between flash and SAR ADCs. However, the hardware cost is high in [Lin et al. [2010]] as this technique requires additional switching networks and $2N-1$ comparators for an N-

bit design. The loop-unrolled architecture of [Jiang et al. [2012]; Verbruggen et al. [2012]] employs a dedicated comparator for each comparison cycle. The comparison result is stored directly at the comparator output. As a result, the SAR logic is greatly simplified, leading to reduced power and delay. Although more comparators are used compared to the conventional SAR architecture, the total comparator power does not increase since each of them is fired only once during the whole conversion. Nevertheless, the comparator common-mode voltage V_{cm} varies significantly and eventually goes to V_{DD} in [Jiang et al. [2012]; Verbruggen et al. [2012]], resulting in large comparator offsets and reduced linearity. Both work [Verbruggen et al. [2012]] and [Jiang et al. [2012]] require complicated calibrations for comparators' offset mismatches, which increase both the power consumption and the design complexity.

This work proposes a novel loop-unrolled SAR ADC with two new key techniques to improve the linearity and the power efficiency. First, in order to address the large V_{cm} variation issue, a bidirectional single-side switching technique is employed. It reduces the comparator offset by appropriately controlling V_{cm}. The comparator decision time is also optimized. In addition, it allows a reduced number of DAC unit capacitors, which reduces the DAC area and the routing parasitics. Second, to further improve the linearity, a novel V_{cm}-adaptive offset calibration technique is proposed to calibrate the comparators' offset mismatch. The proposed calibration technique has very low hardware complexity. It can calibrate the comparator offset at its operating V_{cm} following the proposed switching procedure. A prototype ADC is implemented in 40nm CMOS. It achieves 34.8dB SNDR

and 47.8dB SFDR at a sampling rate of 700MS/s, while consuming only 0.95mW power from a 1.2V supply.

4.2 Proposed SAR ADC Architecture

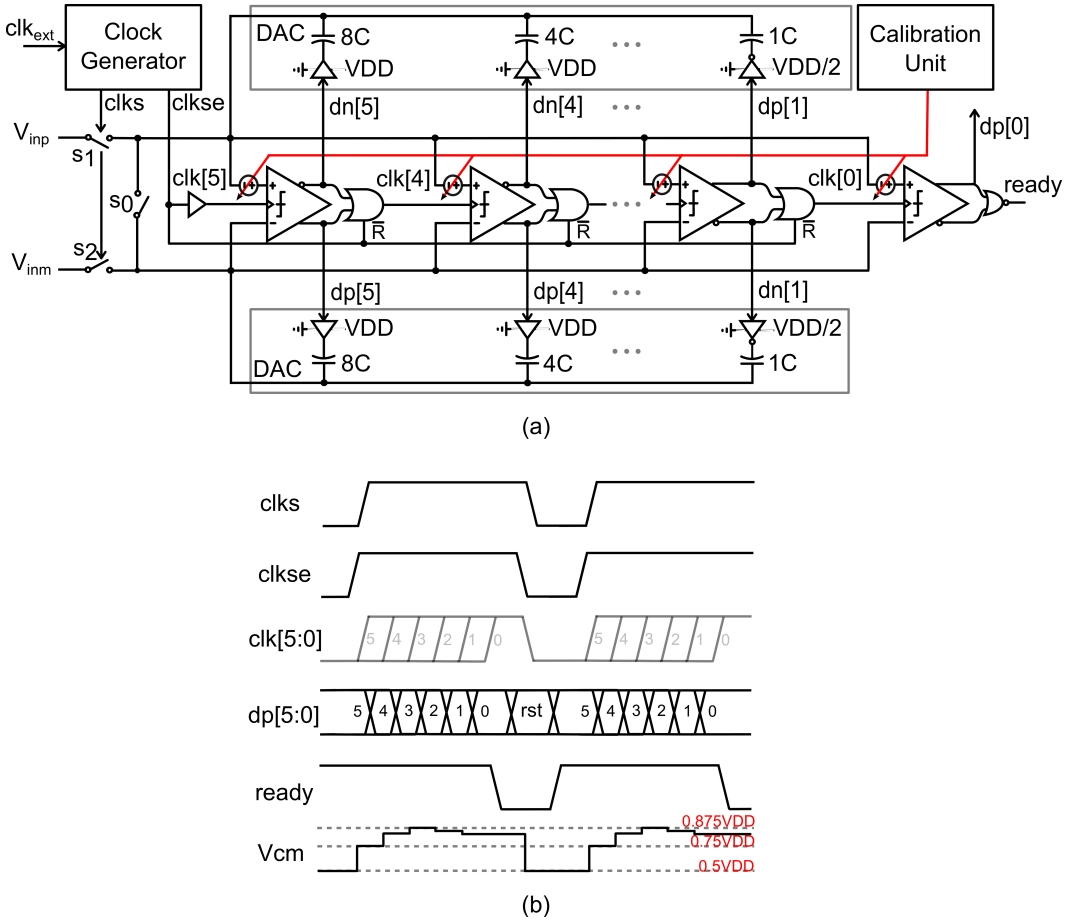

Figure 4.1: (a) Architecture and (b) timing diagram of the proposed SAR ADC.

The proposed 6-bit SAR ADC architecture is shown in Fig. 4.1(a). It consists of a clock generator, a sampling network, 2 capacitive DACs, 6 comparators,

and a calibration unit. The clock generator generates the required timing phases. The sampling switches $S1$ and $S2$ are bootstrapped to ensure high sampling linearity at high input frequencies. The DACs are implemented using binary weighted capacitors. Small dynamic comparators with offset calibration are used to minimize power consumption. Dynamic OR gates with reset and controlled delay are used to generate the asynchronous clocks. The comparator offset mismatch is foreground calibrated by the calibration unit. The LSB comparator outputs are combined by a NOR gate to generate a ready signal, which indicates the end of the whole ADC conversion.

The timing diagram is shown in Fig. 4.1(b). When $clks$ is low, the input voltages are top-plate sampled on the DACs through S_1 and S_2. All comparators' outputs are reset to low through dynamic OR gates controlled by $clkse$. The ready signal is reset to high. When the sampling phase ends, both $clkse$ and $clks$ go to high. The MSB comparator is triggered by $clk[5]$ which is two gates delay of $clkse$. Depending on the sampled input voltages, the MSB comparator makes its decision $dp[5]$ and $dn[5]$, which directly control the capacitive DACs to perform the proposed switching technique without the need for any shift register based SAR logic. The dynamic OR gate delay is controlled to provide adequate time for DAC settling. It generates $clk[4]$ to trigger the second MSB comparator. This procedure propagates in a 'domino' fashion until the LSB comparison finishes. The ready signal goes to low. The next sampling phases starts after the comparator outputs are latched by the falling edge of $clkse$.

Compared to the conventional SAR ADC, the SAR logic is greatly sim-

plified in this loop-unrolled architecture. There is no need for any shift register based sequencer or DFF based data storage because all comparator results are directly stored at the comparator outputs. The comparators are not reset during the ADC conversion process. The asynchronous clock is generated easily by ORing the comparators' outputs. The reduced logic complexity reduces the circuit power, minimizes the chip area, and increases the speed. In the proposed architecture, the conversion time is reduced in three ways compared to the conventional asynchronous SAR ADC [Chen and Brodersen [2006]]. First, no DFF or latch delay is needed to store the comparator output in our critical path. Second, comparators are reset simultaneously, and thus, no comparator reset time is needed for every comparison cycle. The comparator reset time can be a speed bottleneck especially in most advanced technology node where both logic delay and DAC settling time are small [Kull et al. [2013]]. Third, the proposed design allows independent optimization for each comparison cycle. In other words, each OR gate delay can be adjusted based on the corresponding DAC settling time. The comparator power can also be optimized using the technique in [Ahmadi and Namgoong [2015]]. Overall, the optimized critical path for each comparison cycle in the proposed design can be represented as:

$$T = t_{comp,decision} + \max\{t_{DAC}, t_{OR}\} \tag{4.1}$$

This design optimizes $t_{comp,decision}$ by optimizing comparator input common-mode voltage with a bidirectional single-side switching technique. t_{DAC} and t_{OR} are optimized by using small unit capacitor and specially designed dynamic OR gate, respectively. Based on SPICE simulation, t_{DAC} is greater than t_{OR} for the

first 2 MSB bits where the DAC capacitors are large. t_{OR} dominates over t_{DAC} for the last 4 LSB bits.

4.3 Prototype ADC Design

4.3.1 Detailed circuit schematics

Fig. 4.2 shows the dynamic comparator with offset calibration. Two variable MOS capacitors are added at the drain of input transistors $M1$ and $M2$ for calibration purpose. Comparator offset and decision time are two key parameters in this design. Unlike the conventional SAR ADC with one single comparator, the loop-unrolled architecture employs 6 comparators. All comparators have offsets and their offset mismatches degrade the ADC linearity. Comparator decision time is in the critical timing path as shown in (4.1). Thus, it is desirable to design comparator with small offset and fast decision time. One important factor that influences both offset and decision time is the comparator input common-mode voltage V_{cm} [Wicht et al. [2004]]. A small V_{cm} is preferred to reduce the offset. The reason is that the pre-amplification gain is larger at small V_{cm}, which suppresses the offset contribution from the latch. A large V_{cm} helps reduce the pre-amplification time but the time duration of the latch regeneration phase is longer due to the reduction in the pre-amplification gain [Wicht et al. [2004]]. There exists an optimized V_{cm} for decision time. The simulated 1σ offset and decision time are shown in Fig. 4.3. Here the decision time is defined as the time it takes for the comparator output differential voltage to reach $0.7V_{DD}$ given 1mV differential input. It suggests the optimal value of V_{cm} is around 0.8V, where the decision time is minimized and the

offset is also small.

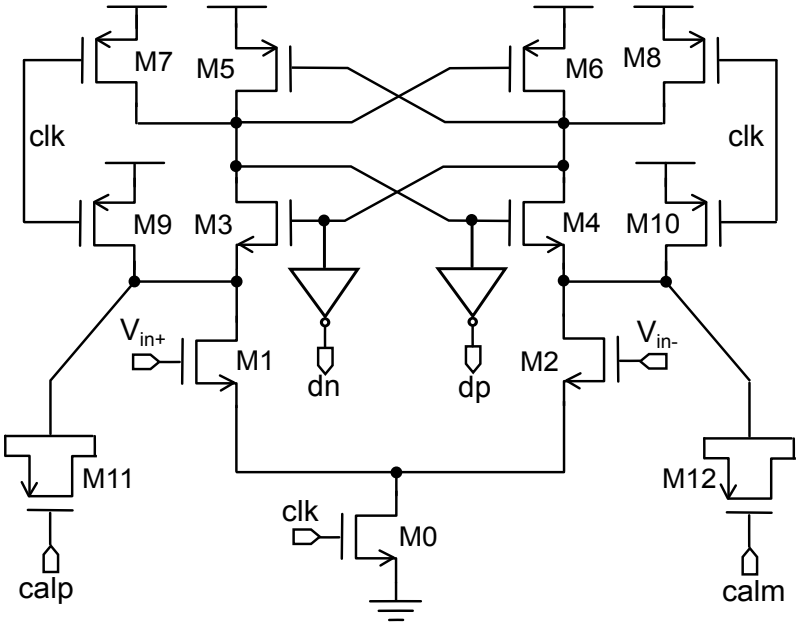

Figure 4.2: Dynamic comparator with varactor loading.

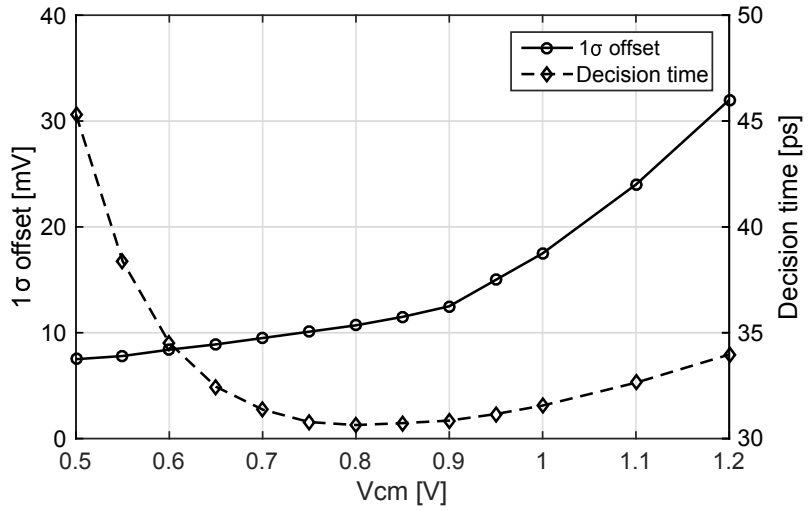

Figure 4.3: Simulated comparator offset and decision time at different V_{cm}.

A modified bidirectional single-side (BSS) switching technique based on [Chen et al. [2014a]; Sanyal and Sun [2014]] is employed in the design. The BSS technique can reduce the number of unit capacitors by 4 times compared to conventional switching technique and 2 times compared to monotonic switching technique [Jiang et al. [2012]; Verbruggen et al. [2012]]. The binary capacitors used in the DAC are $[8C_U, 4C_U, 2C_U, C_U, C_U]$ for 6-bit implementation, with a unit capacitor C_U of 1.9fF. Thanks to the small unit capacitor, the DAC settling time t_{DAC} is short and it is easy to guarantee the settling error to be within 1/2 LSB. No redundancy is provided to avoid additional comparison cycles. The reduced number of unit capacitors reduces the layout complexity since fewer interconnections are needed. The measured result shows the capacitors are matched well for 6-bit accuracy with a similar layout strategy in [Chen et al. [2014a]]. Unlike prior loop-unrolled works [Jiang et al. [2012]; Verbruggen et al. [2012]], no capacitor calibration is needed here.

The proposed BSS switching scheme is shown in Fig. 4.4. DAC is connected to [0, 0, 0, 1, 1/2] when sampling the inputs, where 0, 1 and 1/2 indicate ground, V_{DD} and $V_{DD}/2$, respectively. Instead of switching DAC capacitors from ground to V_{DD} monotonically, the proposed technique switches the first 3 MSB capacitors $[8C_U, 4C_U, 2C_U]$ from ground to V_{DD}, and then, switches the left side C_U capacitors from V_{DD} to ground.

The simulated V_{cm} variation is shown in Fig. 4.5. In the proposed switching scheme, V_{cm} stays close to 0.8V after the first comparison cycle, where the optimized decision time is achieved and comparator offset is kept small [Chen et al.

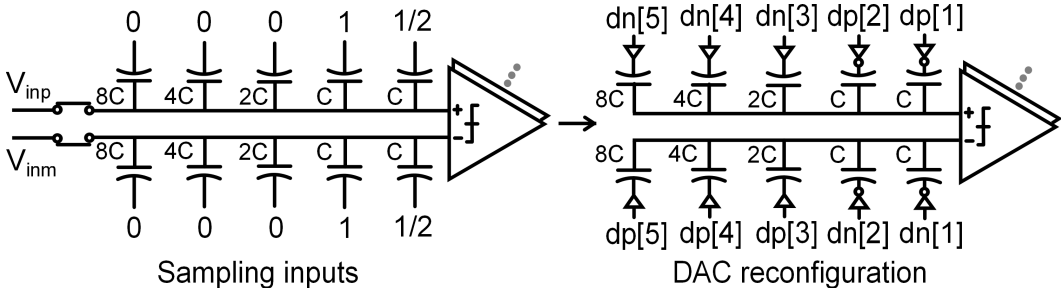

Figure 4.4: BSS switching scheme.

[2016]]. Compared with monotonic switching scheme in [Jiang et al. [2012]; Verbruggen et al. [2012]], where V_{cm} can converge to V_{DD}, the 1σ offset can be reduced from 32mV to 10mV and decision time can be reduced by 10% in the proposed switching technique. Note that V_{cm} decreases slightly when the comparators are fired due to the comparator kick-back noise. The kick-back noise is a common-mode noise to the first order, which does not disturb the settling of the comparator differential mode voltage V_{dm} (see Fig. 4.5). Thus, the kick-back noise does not degrade the linearity for this 6-bit ADC.

In the prototype ADC, the full-scale differential input swing is 1.4V and 1 LSB size is about 20mV. The optimized comparator 1σ offset is 10mV, which is comparable to the LSB size. To avoid linearity degradation due to offset mismatch, a V_{cm}-adaptive offset calibration technique is proposed. The calibration technique works as follows. When the ADC is in the calibration mode, the calibration control switch $S0$ is on and a zero differential input voltage is sampled through $S1$ and $S2$ (see Fig. 4.1). A low-frequency external clock clk_{ext} is provided. Each OR gate's delay is set large enough such that before each comparator is triggered, its differential inputs settle well and stay close to zero. If there is no offset, each comparator's

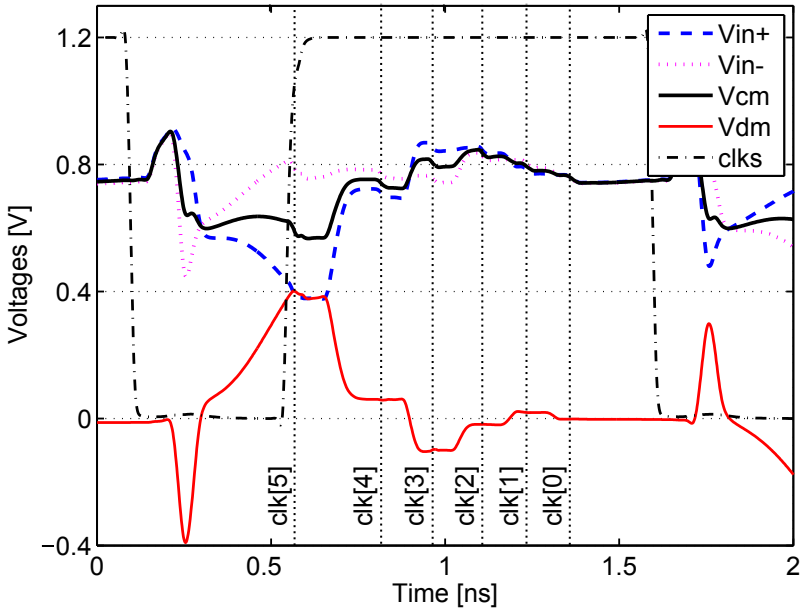

Figure 4.5: Simulated time-domain waveforms for comparator inputs Vin+/Vin-, its common mode voltage V_{cm} and its differential mode voltage V_{dm}.

output jumps between "1" and "0" due to thermal noise. Comparator thermal noise in the design is about 400μV, which is much smaller than the offset. With a large offset in presence, the comparator's output keeps staying at either "1" or "0". The offset can be calibrated by tuning the MOSFET based varactors shown in Fig. 4.2, whose values are controlled by its gate voltage $calp/calm$. The calibration range is designed to be 30mV which is 3 times the simulated 1σ offset. By observing the comparator's output, we can tell whether the comparator offset has been calibrated or not. The calibration is finished when the comparator output is evenly distributed between "1" and "0". 1024 ADC outputs are captured by a logic analyzer during the calibration. The comparator offset is removed when the probability that its

output code equals to "1" is around 50%. Note that the probability does not need to be exactly 50% since the calibration accuracy is relaxed for a 6-b design. The measured probability of comparator outputs being "1" versus its calibration voltage $calm$ for the MSB comparator is plotted in Fig. 4.6. The proposed calibration is simple as it only requires one additional switch $S0$. It does not require special DAC patterns to generate the operating V_{cm} in [Verbruggen et al. [2012]] or special input voltages that cause metastability at different comparators in [Jiang et al. [2012]]. Furthermore, since the same DAC switching procedure happens during calibration, each comparator offset is calibrated at the same V_{cm} as that of the normal ADC operation. This is necessary in BSS or monotonic switching technique since V_{cm} varies in each comparison cycle and the comparator offset depends strongly on V_{cm} [Chen et al. [2014a]; Wicht et al. [2004]].

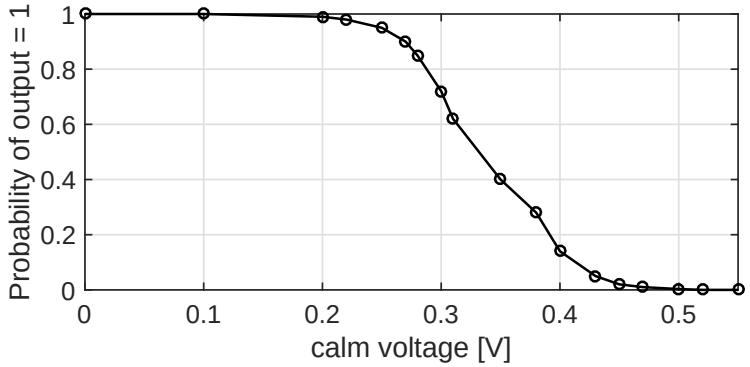

Figure 4.6: Probability of MSB comparator output being '1' versus its $calm$ with $calp$ fixed at 1.2V.

A clock generator similar to [Chen and Brodersen [2006]] is used. The input sampling switches $S1$ and $S2$ are bootstrapped with the circuit shown in Fig. 4.7(a) [Siragusa and Galton [2004]]. It is simple and does not require two complementary

clock phases [Jiang et al. [2012]]. A thick-oxide device provided in the process is used to tolerate a potential voltage higher than 1.2V. OR gate needs to have a reset function together with controlled delay with the aim to provide enough time for DAC settling. Since the unit capacitor employed in this design is quite small (1.9fF), the DAC settling time is comparable with the CMOS logic gate delay. To minimize the number of logic gates and their delay, a dynamic OR gate shown in Fig.4.7(b) is used instead of traditional CMOS gates. VB is used to control the current flowing through OR gate, thus tuning the gate delay.

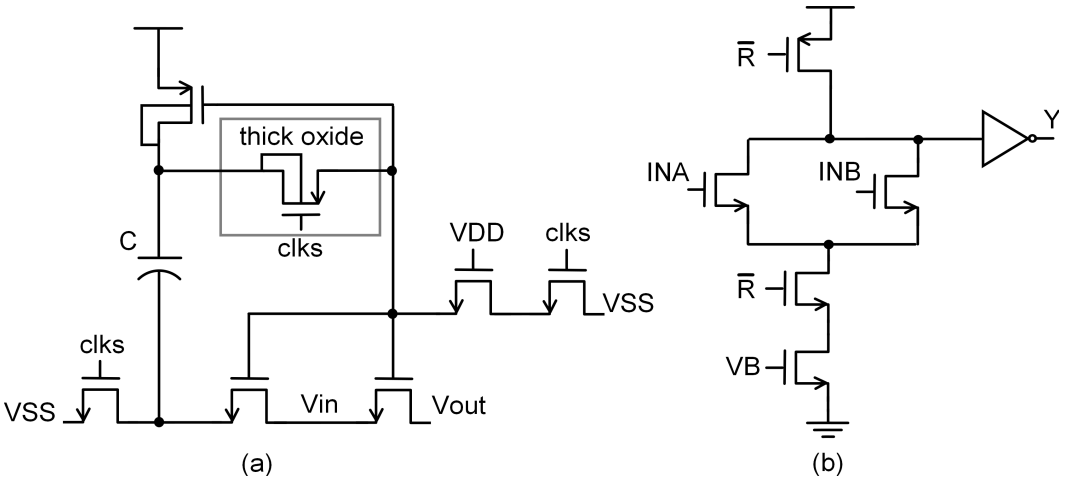

Figure 4.7: Schematic of (a) bootstrapped sampling switch and (b) dynamic OR gate.

4.3.2 Measurement results

The prototype ADC is fabricated in 40-nm CMOS and occupies an active area of only 0.004mm^2, as shown in Fig. 4.8. Unlike the floor plan in [Jiang et al. [2012]], where the DAC and SAR logic are placed side by side, SAR logic

is placed between two CDACs in our design. By doing this, long routing wires are avoided, which saves both area and power. The outputs are decimated by 32 using 5 divide-by-2 toggle flip-flops to facilitate ADC measurements. All measurements are performed under 1.2V power supply.

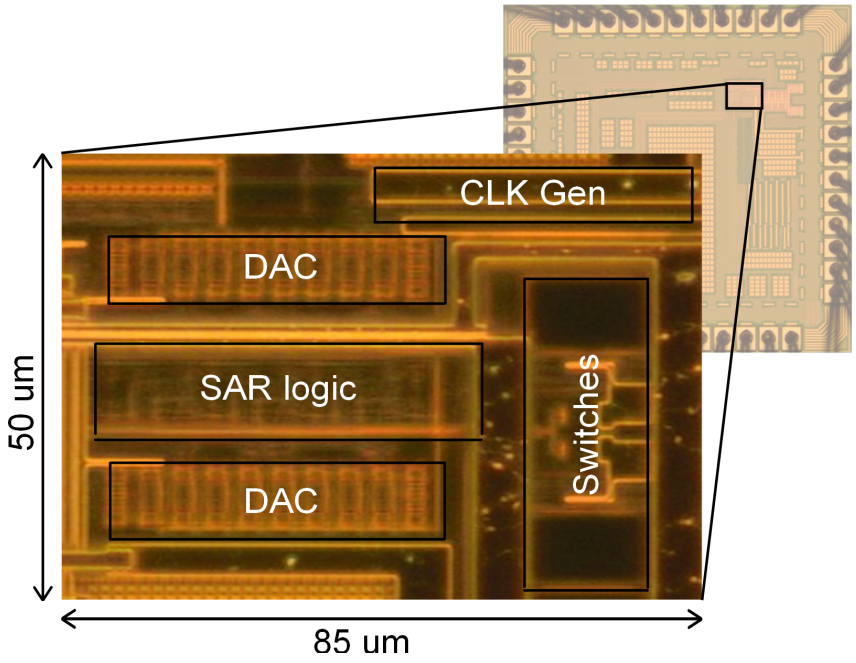

Figure 4.8: Chip micrograph.

Fig. 4.9 shows the measured DNL and INL before and after performing the proposed comparator offset calibration. Before calibration, large DNL and INL jumps happen due to comparator offset mismatches. After performing the V_{cm}-adaptive offset calibration, DNL and INL are reduced significantly to -0.4LSB/0.9LSB and -0.3/0.6LSB, respectively. The effectiveness of the calibration can also be observed from the measured spectrum shown in Fig. 4.10, where 4.3dB SNDR and 8.5dB SFDR improvements are achieved after calibration.

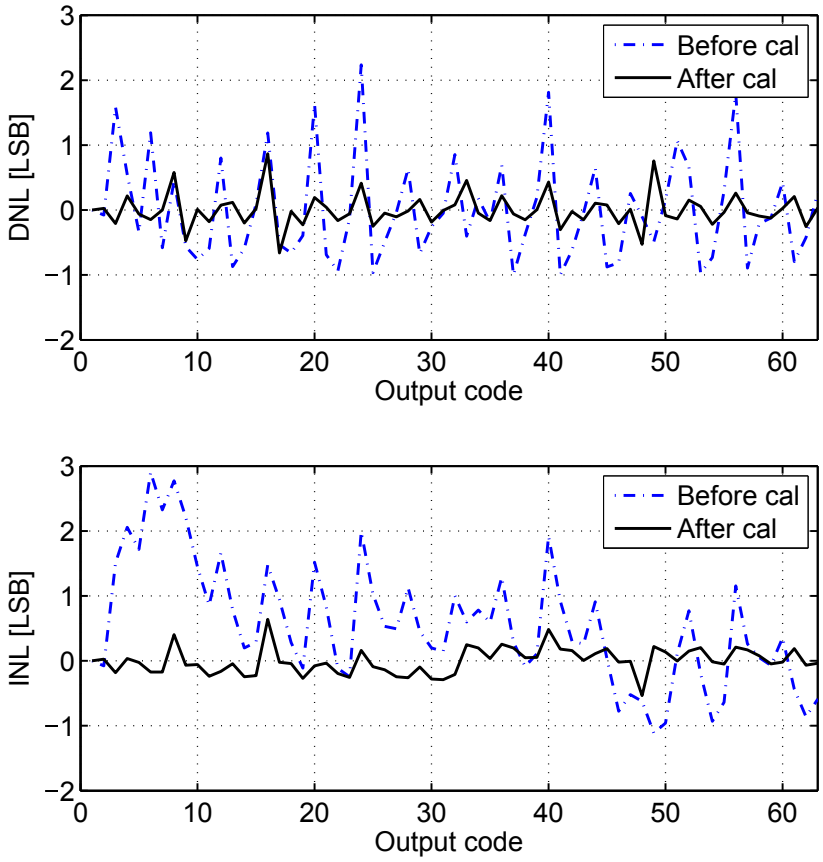

Figure 4.9: Measured DNL/INL before calibration (dotted line) and after calibration (solid line).

Fig. 4.11 shows the measured FFT spectrum with 700MS/s sampling rate and 300MHz input. The measured SNDR and SFDR are 34.8dB and 47.8dB, respectively, leading to 5.5-bit ENOB. When the input frequency is reduced to 10MHz, the measured SNDR and SFDR are 35.1dB and 49.5dB, respectively. Fig. 4.12 shows SNDR and SFDR at different sampling frequencies with a 50MHz in-

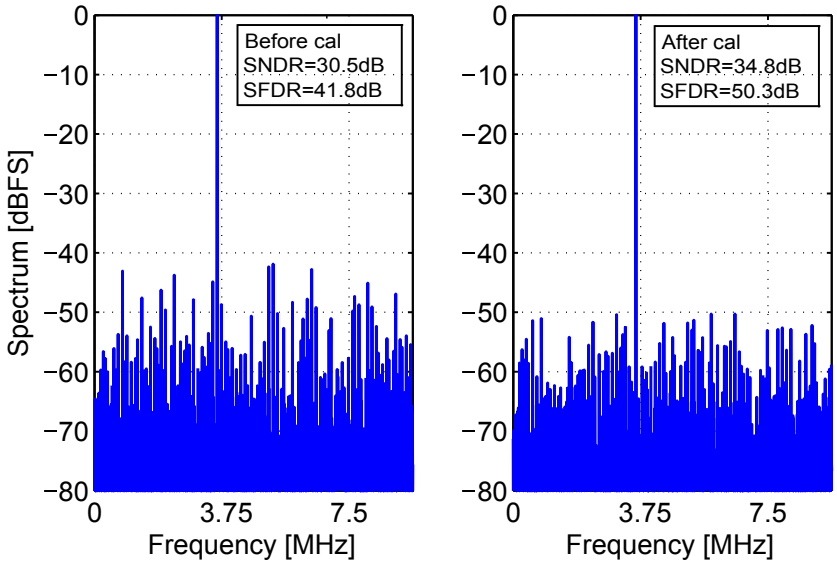

Figure 4.10: Measured 1024p FFT spectrum before calibration and after calibration with 600MS/s sampling rate and 100MHz input.

put, at different input frequencies with 700MS/s sampling rate, and at different input amplitudes with 300MHz input and 700MS/s sampling rate. The measured SNDR is above 34.7dB across the whole Nyquist band. The maximum sampling rate of 700MS/s is limited by insufficient sampling time discovered during chip measurements. When $clkse$ goes low, it takes longer time to reset comparators in measurements than that in simulation, which reduces the effective sampling time. The total power consumption at 700MS/s is 0.95mW, whose breakdown is: 0.84mW used by SAR logic and comparator, 0.09mW used by DAC, and 0.02mW used by clock generator. The measured Walden figure-of-merit (FOM) [Walden [1999]] at Nyquist rate is 30fJ/conversion-step and Schreier FOM [Schreier and Temes [2005]] is 153.4dB. Table 4.1 compares the performance of the prototype ADC

with other recently published high-speed 6-bit SAR ADCs. As shown in Table 4.1, this work achieves the highest SNDR and the best Walden FOM with the smallest chip area among them.

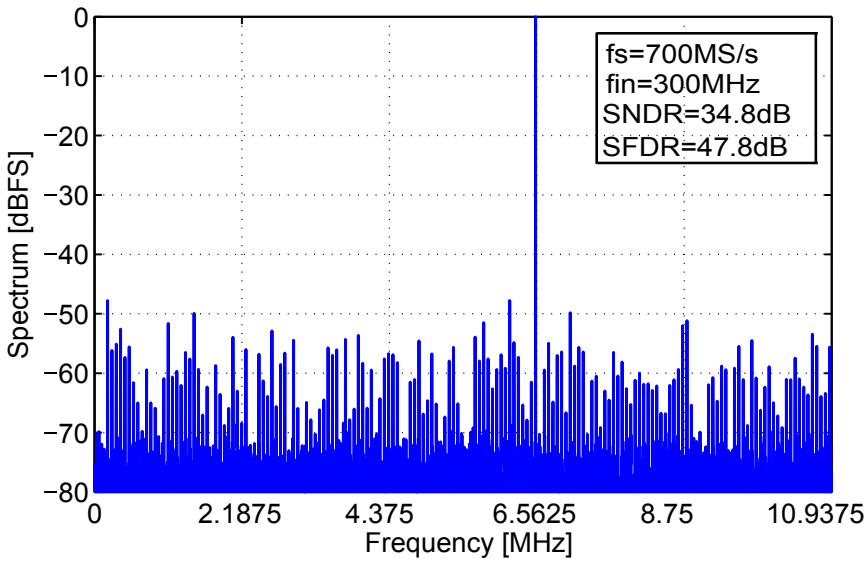

Figure 4.11: Measured 1024p FFT spectrum with 700MS/s sampling rate and 300MHz input.

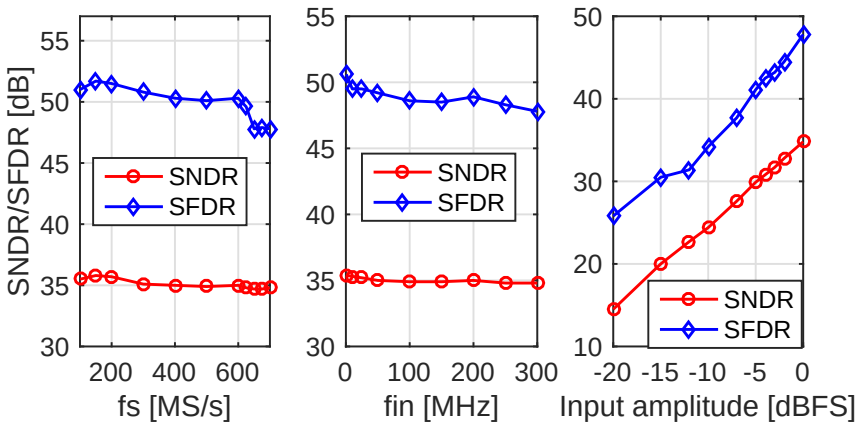

Figure 4.12: Measured SNDR/SFDR under different sampling rates with 50MHz input (left), under different input frequencies with 700MS/s sampling rate (middle), and under different input amplitudes with 700MS/s sampling rate and 300MHz input (right).

Table 4.1: Performance comparison

	Chen and Broder-sen [2006]	Yang et al. [2010]	Tai et al. [2014b]	Jiang et al. [2012]	This work
Resolution [bit]	6	6	6	6	6
Process [nm]	130	65	40	40	40
Supply voltage [V]	1.2	1.2	1.2	1.0	1.2
Active area [mm^2]	0.060	0.110	0.009	0.014	0.004
Number of channels	2	2	1	1	1
Sampling rate [GS/s]	0.6	1	1	1.25	0.7
SNDR(Nyq) [dB]	32	29	31.2	26.8	34.8
ENOB [bit]	5.0	4.5	4.9	4.1	5.5
Power [mW]	5.3	6.7	5.3	6.08	0.95
FOM [fJ/conv-step]	276	290	180	272	30

Chapter 5

Conclusion and Future Directions

5.1 Conclusion

This thesis focuses on improving the power efficiency of SAR ADCs. Three prototype ADCs have been developed to validate the proposed techniques. Chapter 2 presents a novel noise reduction technique for SAR ADC based on statistical estimation. To the authors' best knowledge, this is the first work that comprehensively introduces the statistical estimation theory to the field of ADC design. The proposed technique requires minimum change to the original SAR ADC design. It can significantly reduce both the comparator noise and the quantization error. It is suitable for applications that require low-power high-resolution SAR ADCs.

Chapter 3 presents a low-power ADC with a bidirectional single-side switching technique. It solves the linearity degradation problem due to comparator input common-mode voltage variation. The proposed switching technique provides designers the freedom to choose where the comparator common-mode voltage converges to. It is suitable for applications that require both low power and high resolution.

Chapter 4 presents a high-speed and low-power single-channel loop-unrolled SAR ADC. It proposed a simple method to calibrate the comparator offsets. The

proposed switching technique allows the designers to control comparator input common-mode voltage for comparator offset and speed optimization. It can be easily time-interleaved (TI) for even higher speed applications.

5.2 Future Directions

The proposed statistical estimation based noise reduction technique requires the knowledge of the comparator noise. Since comparator noise is sensitive to PVT variation, an interesting direction is to build a comparator noise extraction circuit on chip. Thus, the look up table of the estimator can be updated when the noise changes. It is also desirable to implement a fully reconfigurable SAR ADC by providing the ability to change the estimation times N.

In the second prototype ADC, a unit capacitor of 2fF is used, which is the minimum MIM capacitor provided in the PDK. Since the DAC switching power is proportional to the unit capacitor size, a smaller unit capacitor is desired. This can be achieved by custom designing the unit capacitor with metal wires. It is also interesting to investigate low power calibration techniques to calibrate the capacitor mismatch with aim to use ultra small unit capacitor. Another interesting path to reduce the DAC size is to use hybrid architecture, such as [Sanyal et al. [2014]]. By doing this, the first stage SAR ADC only needs to resolve less number of bits, leading to reduced DAC size and power. During the measurement, we learned that the SAR logic consumes a significant power out of total ADC power. Although the power of logic circuits reduces in more advanced technologies, it is still desirable to explore circuits design techniques to optimize the logic power.

Although the power and linearity of the loop-unrolled SAR ADC have been improved by using optimized switching technique and V_{cm}-adaptive calibration technique, there is still some work which can be done in the future. One possible direction is to design the background calibration technique to calibrate the comparator offset mismatches. The other direction could be time-interleaving the single channel ADC to achieve higher speed.

Appendix

Appendix 1

List of publications

1. Long Chen, Kareem Ragab, Xiyuan Tang, Jeonggoo Song, Arindam Sanyal, and Nan Sun, "A 0.95-mW 6-b 700-MS/s single-channel loop-unrolled SAR ADC in 40-nm CMOS," accepted in IEEE Transactions on Circuits and Systems II (TCAS–II).

2. Long Chen, Arindam Sanyal, Ji Ma, Xiyuan Tang, and Nan Sun, "Comparator common-mode variation effects analysis and its application in SAR ADCs," accepted in 2016 IEEE International Symposium on Circuits and Systems (ISCAS).

3. Long Chen, Xiyuan Tang, Arindam Sanyal, Yeonam Yoon, Jie Cong, and Nan Sun, "A 10.5-b ENOB 645nW 100kS/s SAR ADC with statistical estimation based noise reduction," IEEE Custom Integrated Circuit Conference (CICC), 2015, pp. 1–4.

4. Yeonam Yoon, Koungtae Lee, Sungjin Hong, Xiyuan Tang, Long Chen, and Nan Sun, "A 0.04-mm^2 modular $\Sigma\Delta$ ADC with VCO-based integrator and 0.9-mW 71-dB SNDR distributed digital DAC calibration," IEEE Custom Integrated Circuit Conference (CICC), 2015, pp. 1–4.

5. Arindam Sanyal, Long Chen, and Nan Sun, "Dynamic element matching with signal-independent element transition rates for multibit delta sigma modulators," IEEE Transactions on Circuits and Systems I (TCAS–I), vol. 62, no. 5, pp. 1325–1334, 2015.

6. Kareem Ragab, Long Chen, Arindam Sanyal, and Nan Sun, "Digital background calibration for pipelined ADCs based on comparator decision time quantization", IEEE Transactions on Circuits and Systems II (TCAS–II), vol. 62, no. 5, pp. 456–460, 2015.

7. Arindam Sanyal, Kareem Ragab, Long Chen, T. R. Viswanathan, Shouli Yan and Nan Sun, "A hybrid SAR-VCO $\Delta\Sigma$ ADC with first-order noise shaping", IEEE Custom Integrated Circuit Conference (CICC), pp. 1–4, 2014.

8. Long Chen, Arindam Sanyal, Ji Ma and Nan Sun, "A 24-uW 11-bit 1-MS/s SAR ADC with a bidirectional single-side switching technique", IEEE European Solid-State Circuit Conference (ESSCIRC), pp. 219–222, 2014.

9. Long Chen, Ji Ma, and Nan Sun, "Capacitor mismatch calibration for SAR ADCs based on comparator metastability detection," IEEE International Symposium on Circuits and Systems (ISCAS), pp. 2357–2360, 2014.

10. Manzur Rahman, Long Chen, and Nan Sun, "Algorithm and implementation of digital calibration of fast converging radix-3 SAR ADC," IEEE International Symposium on Circuits and Systems (ISCAS), pp. 1336–1339, 2014.

11. Long Chen, Manzur Rahman, Sha Liu, and Nan Sun, "A fast radix-3 SAR analog-to-digital converter," IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), pp. 1148–1151, 2013.

Future publications

1. Long Chen, Xiyuan Tang, Arindam Sanyal, Yeonam Yoon, Jie Cong, and Nan Sun, "A 0.7V 0.6μW 100kS/s low-power SAR ADC with statistical estimation based noise reduction," submitted to IEEE Journal of Solid-State Circuits (JSSC).

Bibliography

Naveen Verma and Anantha P. Chandrakasan. An Ultra Low Energy 12-bit Rate-Resolution Scalable SAR ADC for Wireless Sensor Nodes. *Solid-State Circuits, IEEE Journal of*, 42(6):1196–1205, 2007.

Nick Van Helleputte, Sunyoung Kim, Hyejung Kim, Jong Pal Kim, Chris Van Hoof, and Refet Firat Yazicioglu. A 160μW biopotential acquisition ASIC with fully integrated IA and motion-artifact suppression. In *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, pages 118–120, 2012.

Chun-Chen Liu, Soon-Jyh Chang, Guan-Ying Huang, and Ying-Zu Lin. A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure. *Solid-State Circuits, IEEE Journal of*, 45(4):731–740, 2010a.

Tao Jiang, Wing Liu, Freeman Y. Zhong, Charlie Zhong, Kangmin Hu, and Patrick Yin Chiang. A Single-Channel, 1.25-GS/s, 6-bit, 6.08-mW Asynchronous Successive-Approximation ADC With Improved Feedback Delay in 40-nm CMOS. *Solid-State Circuits, IEEE Journal of*, 47(10):2444–2453, 2012.

Hung-Yen Tai, Yao-Sheng Hu, Hung-Wei Chen, and Hsin-Shu Chen. A 0.85fJ/conversion-step 10b 200kS/s subranging SAR ADC in 40nm CMOS. In *Solid-State Circuits Conference, 2014. Digest of Technical Papers. ISSCC. 2014 IEEE International*, pages 196–197, 2014a.

Pieter Harpe, Eugenio Cantatore, and Arthur Van Roermund. An oversampled 12/14b SAR ADC with noise reduction and linearity enhancements achieving up to 79.1dB SNDR. In *Solid-State Circuits Conference, 2014. Digest of Technical Papers. ISSCC. 2014 IEEE International*, pages 194–195, 2014.

Vito Giannini, Pierluigi Nuzzo, Vincenzo Chironi, Andrea Baschirotto, Geert Van der Plas, and Jan Craninckx. An 820μW 9b 40MS/s Noise-Tolerant

Dynamic-SAR ADC in 90nm Digital CMOS. In *Solid-State Circuits Conference, 2008. Digest of Technical Papers. ISSCC. 2008 IEEE International*, pages 238–610, 2008.

Pieter Harpe, Eugenio Cantatore, and Arthur Van Roermund. A 10b/12b 40 kS/s SAR ADC with data-driven noise reduction achieving up to 10.1b ENOB at 2.2 fJ/Conversion-Step. *Solid-State Circuits, IEEE Journal of*, 48(12):3011–3018, 2013.

Mahdi Ahmadi and Won Namgoong. A 3.3fJ/conversion-step 250kS/s 10b SAR ADC using optimized vote allocation. In *Custom Integrated Circuits Conference (CICC), 2013 IEEE*, pages 1–4, 2013.

Long Chen, Xiyuan Tang, Arindam Sanyal, Yeonam Yoon, Jie Cong, and Nan Sun. A 10.5-b ENOB 645 nW 100kS/s SAR ADC with statistical estimation based noise reduction. In *Custom Integrated Circuits Conference (CICC), 2015 IEEE*, pages 1–4, 2015.

George Casella and Roger L. Berger. *Statistical inference*. Duxbury Press, 1990.

Skyler Weaver, Benjamin Hershberg, Peter Kurahashi, Daniel Knierim, and Un-Ku Moon. Stochastic Flash Analog-to-Digital Conversion. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 57(11):2825–2833, 2010.

Volodymyr Kratyuk, Pavan Kumar Hanumolu, Kerem Ok, Un-Ku Moon, and Kartikeya Mayaram. A Digital PLL With a Stochastic Time-to-Digital Converter. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 56(8):1612–1621, 2009.

Bob Verbruggen, Jorgo Tsouhlarakis, Takaya Yamamoto, Masao Iriguchi, Ewout Martens, and Jan Craninckx. A 60 dB SNDR 35 MS/s SAR ADC With Comparator-Noise-Based Stochastic Residue Estimation. *Solid-State Circuits, IEEE Journal of*, 50(9):2002–2011, 2015.

Hau-Seung Lee, Hodges David A., and Paul R. Gray. A self-calibrating 15 bit CMOS A/D converter. *Solid-State Circuits, IEEE Journal of*, 19(6):813–819, 1984.

Vaibhav Tripathi and Boris Murmann. Mismatch characterization of small metal fringe capacitors. In *Custom Integrated Circuits Conference (CICC), 2013 IEEE*, pages 1–4, 2013.

Sunghyuk Lee, Anantha P. Chandrakasan, and Hae-Seung Lee. A 1GS/s 10b 18.9mW time-interleaved SAR ADC with background timing-skew calibration. In *Solid-State Circuits Conference, 2014. Digest of Technical Papers. ISSCC. 2014 IEEE International*, pages 384–385, 2014.

Marcus Yip and Anantha P. Chandrakasan. A Resolution-Reconfigurable 5-to-10-Bit 0.4-to-1 V Power Scalable SAR ADC for Sensor Applications. *Solid-State Circuits, IEEE Journal of*, 48(6):1453–1464, 2013.

Gregory P. Harmer, Bruce R. Davis, and Derek Abbott. A review of stochastic resonance: circuits and measurement. *IEEE Transactions on Instrumentation and Measurement*, 51(2):299–309, 2002.

Long Chen, Arindam Sanyal, Ji Ma, and Nan Sun. A 24-μW 11-bit 1-MS/s SAR ADC with a bidirectional single-side switching technique. In *Solid-State Circuits Conference, 2014. ESSCIRC 2014. Proceedings of the 40th European*, pages 219–222. IEEE, 2014a.

Arindam Sanyal and Nan Sun. An Energy-Efficient Low Frequency-Dependence Switching Technique for SAR ADCs. *Circuits and Systems II: Express Briefs, IEEE Transactions on*, 61(5):294–298, 2014.

Shuo-Wei Michael Chen and Robert W. Brodersen. A 6-bit 600-MS/s 5.3-mW Asynchronous ADC in 0.13-μm CMOS. *Solid-State Circuits, IEEE Journal of*, 41(12):2669–2680, 2006.

Michiel Van Elzakker, Ed Van Tuijl, Paul Geraedts, Danil Schinkel, Eric A. M. Klumperink, and Bram Nauta. A 10-bit charge-redistribution ADC consuming 1.9 μW at 1 MS/s. *Solid-State Circuits, IEEE Journal of*, 45(5):1007–1015, 2010.

Naveen Verma and Anantha P. Chandrakasan. A 25 μW 100kS/s 12 bit ADC for wireless micro-sensor applications. pages 822–831, Feb 2006.

Dai Zhang, Ameya Bhide, and Atila Alvandpour. A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13- μm CMOS for medical implant devices. *Solid-State Circuits, IEEE Journal of*, 47(7):1585–1593, 2012.

Brian P. Ginsburg and Anantha P. Chandrakasan. An energy-efficient charge recycling approach for a SAR converter with capacitive DAC. In *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*, pages 184–187. IEEE, 2005.

Yan Zhu, Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U Ben, Rui Paulo Martins, and Franco Maloberti. A 10-bit 100-MS/s Reference-Free SAR ADC in 90 nm CMOS. *Solid-State Circuits, IEEE Journal of*, 45(6):1111–1121, 2010.

Chun-Cheng Liu, Soon-Jyh Chang, Guan-Ying Huang, Ying-Zu Lin, and Chung-Ming Huang. A 1V 11fJ/conversion-step 10bit 10MS/s asynchronous SAR ADC in 0.18μm CMOS. In *VLSI Circuits (VLSIC), 2010 IEEE Symposium on*, pages 241–242. IEEE, 2010b.

Tsuguo Kobayashi, Kazataka Nogami, Tsukasa Shirotori, and Yuihiro Fujimoto. A current-controlled latch sense amplifier and a static power-saving input buffer for low-power architecture. *Solid-State Circuits, IEEE Journal of*, 28(4):523–527, 1993.

Geert Van der Plas, Stefaan Decoutere, and Stphane Donnay. A 0.16pJ/Conversion-Step 2.5mW 1.25GS/s 4b ADC in a 90nm Digital CMOS Process. In *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International*, pages 2310–2312. IEEE, 2006.

Bernhard Wicht, Thomas Nirschl, and Doris Schmitt-Landsiedel. Yield and speed optimization of a latch-type voltage sense amplifier. *Solid-State Circuits, IEEE Journal of*, 39(7):1148–1158, 2004.

Pierluigi Nuzzo, Fernando De Bernardinis, Pierangelo Terreni, and Geert Van der Plas. Noise Analysis of Regenerative Comparators for Reconfigurable ADC Architectures. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 55 (6):1441–1454, 2008.

Chi-Hung Lin Lin and Klaas Bult. A 10-b, 500-MSample/s CMOS DAC in 0.6 mm^2. *Solid-State Circuits, IEEE Journal of*, 33(12):1948–1958, 1998.

Pieter J. A. Harpe, Cui Zhou, Yu Bi, Nick P. Van der Meijs, Xiaoyan Wang, Kathleen Philips, Guido Delmans, and Harmke De Groot. A 26 μW 8 bit 10 MS/s Asynchronous SAR ADC for Low Energy Radios. *Solid-State Circuits, IEEE Journal of*, 46(7):1585–1595, 2011.

Long Chen, Ji Ma, and Nan Sun. Capacitor mismatch calibration for SAR ADCs based on comparator metastability detection. In *Circuits and Systems (ISCAS), 2014 IEEE International Symposium on*, pages 2357–2360, 2014b.

Kareem Ragab, Long Chen, Arindam Sanyal, and Nan Sun. Digital Background Calibration for Pipelined ADCs Based on Comparator Decision Time Quantization. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 62(5): 456–460, 2015.

Albert H. Chang, Hae-Seung Lee, and Duane Boning. A 12b 50MS/s 2.1mW SAR ADC with redundancy and digital background calibration. In *Solid-State Circuits Conference, 2013. ESSCIRC 2013. Proceedings of the 39th European*, pages 109–112, 2013.

Guan-Ying Huang, Soon-Jyh Chang, Chun-Cheng Liu, and Ying-Zu Lin. 10-bit 30-MS/s SAR ADC Using a Switchback Switching Method. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 21(3):584–588, 2013.

Chien-Hung Kuo and Cheng-En Hsieh. A high energy-efficiency SAR ADC based on partial floating capacitor switching technique. In *Solid-State Circuits Conference, 2011. ESSCIRC 2011. Proceedings of the 37th European*, pages 475–478, 2011.

Jing Yang, Thura Lin Naing, and Robert W. Brodersen. A 1 GS/s 6 Bit 6.7 mW Successive Approximation ADC Using Asynchronous Processing. *Solid-State Circuits, IEEE Journal of*, 45(8):1469–1478, 2010.

Hegong Wei, Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, Rui Paulo Martins, and Franco Maloberti. An 8-b 400-MS/s 2-b-Per-Cycle SAR ADC With Resistive DAC. *Solid-State Circuits, IEEE Journal of*, 47(11):2763–2772, 2012.

Hyeok-Ki Hong, Hyun-Wook Kang, Dong-Shin Jo, Dong-Suk Lee, Yong-Sang You, Yong-Hee Lee, Ho-Jin Park, and Seung-Tak Ryu. A 2.6b/cycle-architecture-based 10b 1 JGS/s 15.4mW 4x-time-interleaved SAR ADC with a multistep hardware-retirement technique. In *Solid-State Circuits Conference, 2015. Digest of Technical Papers. ISSCC. 2015 IEEE International*, pages 1–3, 2015.

Lukas Kull, Thomas Toifl, Martin Schmatz, Pier Andrea Francese, Christian Menolfi, Matthias Brandli, Marcel Kossel, Thomas Morf, Toke Meyer Andersen, and Yusuf Leblebici. A 3.1 mW 8b 1.2 GS/s Single-Channel Asynchronous SAR ADC With Alternate Comparators for Enhanced Speed in 32 nm Digital SOI CMOS. *Solid-State Circuits, IEEE Journal of*, 48(12):3049–3058, 2013.

Hung-Yen Tai, Cheng-Hsueh Tsai, Pao-Yang Tsai, Hung-Wei Chen, and Hsin-Shu Chen. A 6-bit 1-GS/s Two-Step SAR ADC in 40-nm CMOS. *Circuits and Systems II: Express Briefs, IEEE Transactions on*, 61(5):339–343, 2014b.

Ying-Zu Lin, Soon-Jyh Chang, Yen-Ting Liu, Chun-Cheng Liu, and Guan-Ying Huang. An Asynchronous Binary-Search ADC Architecture With a Reduced Comparator Count. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 57(8):1829–1837, 2010.

Long Chen, Manzur Rahman, Sha Liu, and Nan Sun. A fast radix-3 SAR analog-to-digital converter. In *Circuits and Systems (MWSCAS), 2013 IEEE 56th International Midwest Symposium on*, pages 1148–1151, 2013.

Manzur Rahman, Long Chen, and Nan Sun. Algorithm and implementation of digital calibration of fast converging Radix-3 SAR ADC. In *Circuits and Systems (ISCAS), 2014 IEEE International Symposium on*, pages 1336–1339, 2014.

Bob Verbruggen, Masao Iriguchi, and Craninckx Jan. A 1.7 mW 11b 250 MS/s 2-Times Interleaved Fully Dynamic Pipelined SAR ADC in 40 nm Digital CMOS. *Solid-State Circuits, IEEE Journal of*, 47(12):2880–2887, 2012.

Muhammad Ahmadi and Won Namgoong. Comparator Power Minimization Analysis for SAR ADC Using Multiple Comparators. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 62(10):2369–2379, 2015.

Long Chen, Arindam Sanyal, Ji Ma, Xiyuan Tang, and Nan Sun. Comparator common-mode variation effects analysis and its application in SAR ADCs. In *Circuits and Systems (ISCAS), 2016 IEEE International Symposium on*, 2016.

Eric Siragusa and Ian Galton. A digitally enhanced 1.8-V 15-bit 40-MSample/s CMOS pipelined ADC. *Solid-State Circuits, IEEE Journal of*, 39(12):2126–2138, 2004.

Robert H. Walden. Analog-to-digital converter survey and analysis. *IEEE Journal on Selected Areas in Communications*, 17(4):539–550, 1999.

Richard Schreier and Gabor C. Temes. *Understanding delta-sigma data converters*. Wiley-IEEE Press, 2005.

Arindam Sanyal, Kareem Ragab, Long Chen, T. R. Viswanathan, Shouli Yan, and Nan Sun. A hybrid SAR-VCO $\Delta\Sigma$ ADC with first-order noise shaping. In *Custom Integrated Circuits Conference (CICC), 2014 IEEE Proceedings of the*, pages 1–4, 2014.

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