Comment on "Assessment of field-induced quantum confinement in heterogate germanium electron–hole bilayer tunnel field-effect transistor" [Appl. Phys. Lett. 105, 082108 (2014)]

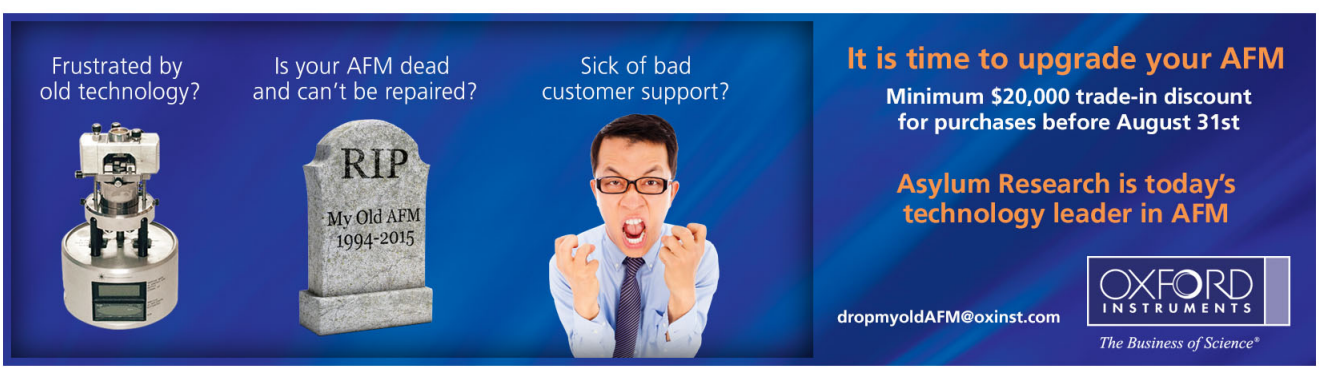
William Hsu, Jason Mantey, Leonard F. Register, and Sanjay K. Banerjee

Citation: Applied Physics Letters **106**, 026102 (2015); doi: 10.1063/1.4905865

View online: http://dx.doi.org/10.1063/1.4905865

View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/106/2?ver=pdfcov

Published by the AIP Publishing



Comment on "Assessment of field-induced quantum confinement in heterogate germanium electron–hole bilayer tunnel field-effect transistor" [Appl. Phys. Lett. 105, 082108 (2014)]

William Hsu,[a] Jason Mantey, Leonard F. Register, and Sanjay K. Banerjee
Department of Electrical and Computer Engineering and Microelectronics Research Center, The University of Texas at Austin, Austin, Texas 78758, USA

(Received 22 October 2014; accepted 31 December 2014; published online 15 January 2015)

[http://dx.doi.org/10.1063/1.4905865]

In a recent letter, Padilla *et al.*[1] pointed out the importance of the diagonal tunneling current in the Ge electron-hole bilayer tunnel field-effect-transistor (EHBTFET), which was previously proposed with favorable ON-current and subthreshold swing (SS) based on simulations.[1] This parasitic diagonal tunneling current is exacerbated by the built-in horizontal field along the channel due to different field-induced quantum confinement (FIQC) between the gate overlap and underlap regions, resulting in SS degradation of a EHBTFET. To address the issue, they proposed a heterogate design which employs substantially different metal gate work functions for the gate overlap and underlap regions to reduce the horizontal field and thus the diagonal tunneling (Fig. 1(a)).[1] The work function difference, 0.5 eV or larger, was optimized for an OFF-state drain voltage, specifically $V_D = 0.5$ V.[1] However, the use of such a large work function difference could have potentially deleterious effects on the ON-state performance with low-V_D CMOS logic.

To examine the performance of the heterogate Ge EHBTFET under different drain bias, a full quantum mechanical (QM) simulation[2] is carried out to evaluate the potential difference/barrier between the gate overlap and underlap regions. The QM (2D subbands) study is performed by solving the Schrödinger and Poisson equations self-consistently in all the 1D slices (y direction) along the channel (x direction) without the incorporation of band-to-band tunneling (BTBT). Here, we define the gate voltage, V_G, at the eigenstate alignment of the first electron and hole subbands in the gate overlap region as $V_{G,align}$. It is assumed that the change of the carrier density in the channel due to BTBT is too low to introduce band modification at $V_G = V_{G,align}$, particularly given the abrupt turn-on predicted by Padilla *et al.*[1] The performance evaluation is conducted by investigating the eigenenergy difference, ΔE, because we only focus on the magnitude of the barrier between the gate overlap and underlap regions induced by work function differences. The magnitude of the barrier at $V_G = V_{G,align}$ is determined using $|\Delta E| = |E_{1e,UL} - E_{1e,OL}| = |E_{1e,UL} - E_{1h,OL}|$, where the $E_{1e,UL}$ and $E_{1e,OL}$ are the electron eigenenergies of the first subbands in the gate underlap and overlap regions, respectively, and $E_{1h,OL}$ is the hole eigenenergy of the first subband in the gate overlap region. Note that the magnitude of the subband overlap, $|E_{1e,UL} - E_{1h,OL}|$, is related to the diagonal tunneling current. For simplicity, the eigenenergies are all extracted at the midpoints of their respective regions. The midpoints also serve as good reference points for estimating built-in electric fields from the simulated band diagrams (not shown).

The basic heterogate Ge EHBTFET device structure from Ref. 1 is shown in Fig. 1(a), although parameters vary in this work. High-κ gate oxides (0.6 nm equivalent oxide thickness) are used. The gate overlap length ($L_{g,OL}$), gate underlap length ($L_{g,UL}$), and the distance between the gate and source (L_s) are all set to 50 nm. A Ge (100) channel thickness of $T_{ch} = 10$ nm is considered. The device consists of an intrinsic Ge region

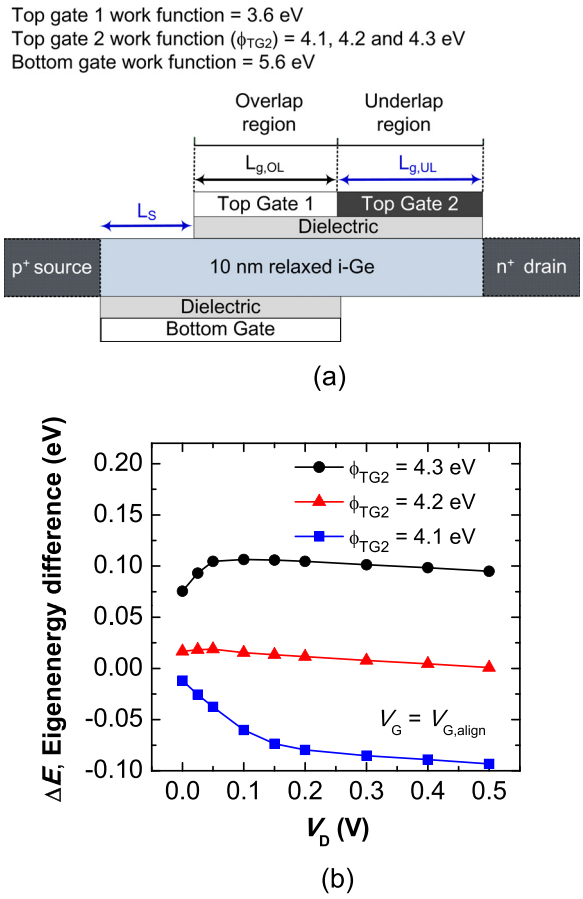


FIG. 1. (a) Schematic cross section of the simulated heterogate Ge EHBTFET ($L_{g,OL} = L_{g,UL} = L_s = 50$ nm, equivalent oxide thickness = 0.6 nm), and (b) eigen energy difference, ΔE, as a function of V_D with the work functions of top gate 2, $\phi_{TG2} = 4.1$, 4.2, and 4.3 eV.

[a]Author to whom correspondence should be addressed. Electronic mail: william.hsu@utexas.edu

(modeled as $N_D = 1 \times 10^{15}\,cm^{-3}$) with heavily doped source and drain ($N_A = N_D = 1 \times 10^{19}\,cm^{-3}$). With the work function of the portion of the top heterogate that covers the gate overlap region (top gate 1) set to 3.6 eV, and the work function of the bottom gate set to 5.6 eV, three different values are considered for the work function of the portion of the heterogate above the gate underlap region (top gate 2) in our simulations, $\phi_{TG2} = 4.1$, 4.2, and 4.3 eV.

Figure 1(b) illustrates the $\Delta E - V_D$ relation with different ϕ_{TG2} at $V_G = V_{G,align}$. For $\phi_{TG2} = 4.1$ eV, the ΔE varies quickly with increasing V_D in the low-V_D regime and nearly saturates in the high-V_D regime. In addition, the ΔE shows a smaller shift with increasing ϕ_{TG2} in the low-V_D regime as compared to the high-V_D regime. Both these behaviors can be explained by drain-induced barrier modification (DIBM),[3] where the channel potential is more strongly controlled by the drain than by the gate at lower drain bias. In the high-V_D regime, where the gate dominates the drain with respect to the channel potential, the change in ΔE with different ϕ_{TG2} become very close to the change in ϕ_{TG2}. Ultimately, there exists an ideal value for ϕ_{TG2} that results in a low and near-constant $|\Delta E|$ as a function of V_D. The optimum ϕ_{TG2} is found to be close to 4.2 eV in simulations (Fig. 1(b)). These results suggest that the heterogate EHBTFET, which can eliminate parasitic tunneling utilizing work function difference between the two top gates without degrading the ON-state performance in the low-V_D regime, also is a promising TFET design. Note that although the evaluation results in this comment are performed with EHBTFETs, the heterogate design concept should be considered to be general for all the TFETs based on 2D-2D or 3D-2D tunneling.

This work was supported in part by the NRI SWAN program and NSF NASCENT ERC.

[1]J. L. Padilla, C. Alper, F. Gamiz, and A. M. Ionescu, Appl. Phys. Lett. **105**, 082108 (2014).
[2]Sentaurus Device, version G-2012.06 (Synopsys, Inc., Mountain View, CA, 2012).
[3]W. Hsu, J. Mantey, L. F. Register, and S. K. Banerjee, Appl. Phys. Lett. **103**, 093501 (2013).