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Advanced III-V MOSFET

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Advanced III-V MOSFET

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Dedication

All my families and my love, Jeong Min Hyun

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Advanced III-V MOSFET

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The University of Texas at Austin, 2016

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As scaling of silicon-based CMOS devices approaches its end, there is an ever increasing interest in high mobility materials. Among potential candidates for future CMOS devices, III-V materials are the most promising option due to their superior carrier transport properties. Despite their attractive material properties, they face several critical challenges that need to be resolved. The main limitation in III-V MOSFETs is lack of a good native oxide. Recently, devices utilizing a gate stack formed with high-κ and metal gate electrode are being explored for EOT scaling. Compared to Si MOSFETs, the surfaces of III-V channel materials are prone to deteriorate, resulting in degradation threshold voltage control, subthreshold characteristics, and overall device performance.

The purpose of this dissertation is to address improvement of surface characteristics of III-V materials, especially, InGaAs. First of all, beryllium oxide (BeO) is considered as interface passivation layer for InGaAs MOSFETs. In order to apply BeO onto InGaAs, the chemical and mechanical properties are first studied. Liquid BeO precursor is never used in ALD systems. The chemical properties of ALD BeO film are revealed from AES, XPS, NRA, RBS, and REELS. Using nano-indentation, the mechanical characteristics of ALD BeO are investigated.

The second part of the study focuses on the application of ALD BeO to InGaAs MOSFETs. The surface channel MOSFET is employed to understand BeO dielectric with III-V channel. The quantum well (QW) structure is known to withstand InGaAs intrinsic material properties from a device point of view. ALD BeO is applied to QW InGaAs MOSFETs as an interface passivation layer below HfO_2. The impact of ALD BeO application for interface passivation is presented using the improvement in device characteristics, for example, drive current (I_{ON}), low leakage current (I_{OFF}), effective mobility (μ_{eff}), and interface trap density (D_{it}).

The third and final part are about process research for InGaAs surface quality. III-V channel materials are inherent to create notorious native oxide that needs to be treated before the fabrication process. In order to protect pristine III-V surface, *in-situ* Ar treatment is studied and used before high-κ deposition. In addition, deuterium (D_2) high-pressure annealing is considered to passivate III-V interface with high-κ. To demonstrate the efficacy of these treatment processes, InGaAs MOSCAPs are fabricated, and capacitance characteristics are analyzed and compared. The C-V hysteresis and multi-frequency C-V are measured, and the interface trap density (D_{it}) is extracted using the C-V result.

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Chapter 1: Introduction

1.1 History of MOSFETs Technology

Metal-oxide-semiconductor field effect transistors (MOSFETs) have played a pivotal role as the main component of integrated circuits (ICs). For over 40 years, the semiconductor industry has maintained Moore's law where the number of transistors on a chip doubles every two years [1, 2].

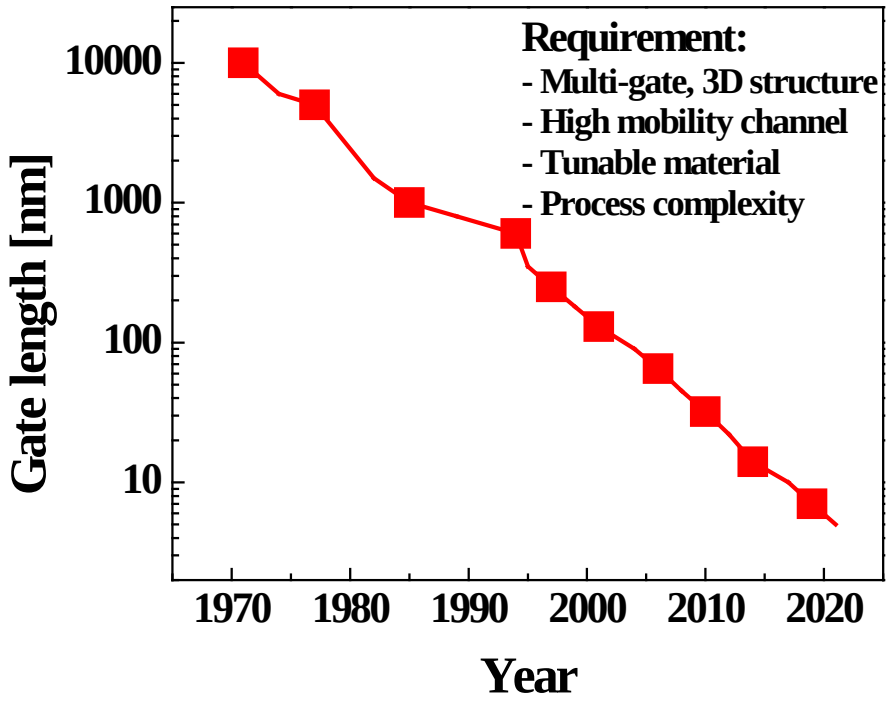


Figure 1-1: Historical trend of Si CMOS technology development in transistor gate length [2].

The key aspect of success in silicon MOSFETs is SiO_2 gate oxide. It is no controversy that SiO_2 is excellent material in silicon CMOS industry, because SiO_2 is well controllable material in thickness and uniformity. First, low defect density is achieved when SiO_2 is used as gate insulator since it forms very stable interface with silicon surface. The P_{b0} center (trivalent Si dangling bond) considering one of the crucial defects is easily passivated after annealing in hydrogen ambient [3-5]. In addition, the band gap of SiO_2 is large (around 9 eV), which can be considered that it is superior in electrical isolation in gate stack.

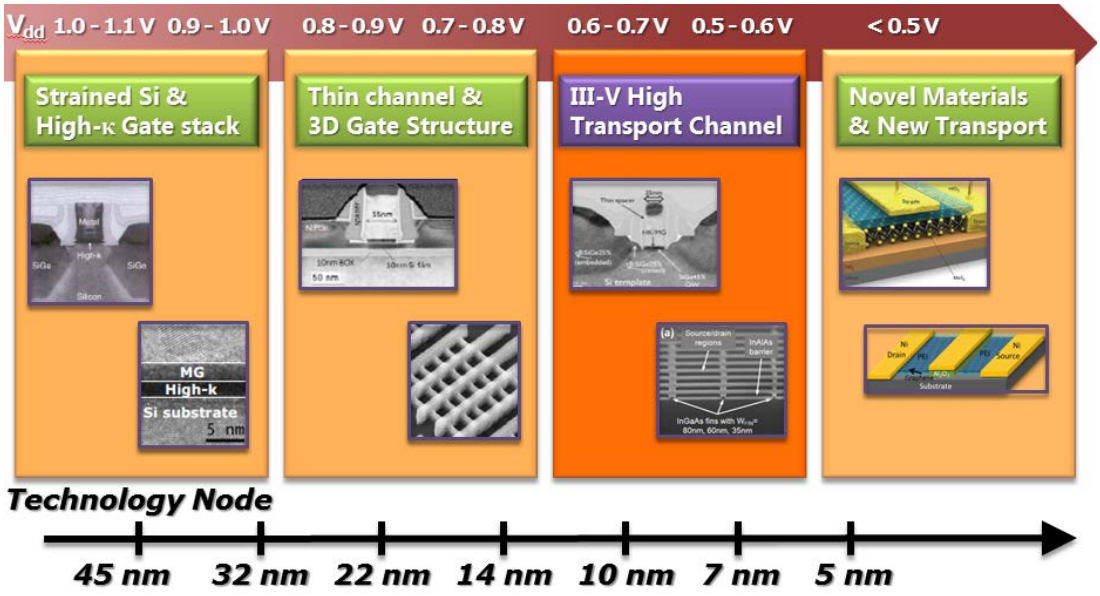


Figure 1-2: Technology innovation toward 22nm node: Strained silicon, high-κ/metal gate stack, and non-planar structure [6].

Owing to prominent properties of SiO_2, this tremendous growth in the semiconductor industry can be realized. It is closely related with the continuous enhancement of integrated circuit performance. The increase packing density by reducing dimension of chip size is key component of success. There are a few of the enabling technologies behind this success in Si CMOS technology, as shown in Figure 1.2 [6]. Nano-lithography, high-κ/metal gate, and 3D device structures lead remarkable growth in semiconductor industry. Although the highly developed lithography processes allow nano-sized device features, scaling of the oxide thickness in MOSFETs faces an inherent challenge [7, 8], due to high gate leakage currents through SiO_2 and poly-Si gate stacks. Thus, SiO_2 and poly-Si gate stacks are replaced with high-κ dielectric materials and metal gates in order to reduce gate leakage while maintaining the same effective oxide thickness [7]. Further scaling of feature sizes can also be achieved by utilizing non-planar device structures as shown in Figure 1.2. A multi-gated structure, for example, brings immense benefits to the chip maker, such as fast throughput, and reduction of power consumption [6].

	Si	Ge	GaAs	InP	$In_{0.53}Ga_{0.47}AS$	$In_{0.7}Ga_{0.3}As$	InAs
Lattice Constant (Å)	5.431	5.658	5.653	5.869	5.869	5.937	6.058
Electron Effectiv Mass (m^*/m_0)	0.19	0.082	0.067	0.077	0.041	0.034	0.023
Electron Affinity (eV)	4.05	4	4.07	4.38	4.5	4.65	4.9
Band-gap (eV)	1.12	0.66	1.42	1.35	0.74	0.58	0.35
Electron mobility ($cm^2/V\cdot s$)	**1500**	**3900**	**8500**	**4600**	**12000**	**20000**	**33000**
Hole mobility ($cm^2/V\cdot s$)	450	1900	400	150	300	400	460
Saturation velocity at low field (cm/s)	$1 X 10^7$	$6 X 10^6$	$2.1 X 10^7$	$2.5 X 10^7$	$3.1 X 10^7$	$6.1 X 10^7$	$7.7 X 10^7$

Table 1-1: Intrinsic material property comparison of several semiconductors

It is hard to continuously maintain Moore's law beyond the 7 nm technology node using just the current silicon technology. Revolutionary advances in materials are inevitable to keep increasing chip density and improving performance. In agreement with necessity of further scaling, high mobility channel materials have also been in the limelight for post-Si CMOS devices. III-V materials, such as InGaAs, InAs, or InP have inherent extraordinary transport properties, as highlighted in Table 1.1 [9, 10].

1.2 MOTIVATION OF III-V MOS DEVICE STUDY

The interest in III-V CMOS comes from the outstanding electron transport properties in these materials, which leads to higher electron velocity, and mobility [11]. This results in devices with both a high ON-state current and transconductance [12]. It can be clearly seen in table 1-1 that III-V materials have higher electron mobility and

smaller effective mass compared to Si. It can be easily compared in equation (1.1), (1.2) and table 1-1.

$$I_D = C_{OX} \cdot \mu \cdot \frac{W}{2L}(Vg - V_{th})^2 \qquad (1.1)$$

$$\mu = \frac{q \cdot \tau_c}{m^*} \qquad (1.2)$$

According to equation (1.1) and (1.2), it can be explained the relation between drive current and effective mass. Considering this relationship, III-V materials produce high drive current in device.

Especially, InGaAs with higher In content shows high electron mobility. This in turn translates into reduced power consumption and gate delay because high electron mobility can lead to a higher drive current at a low supply power, which is described in Figure 1.3.

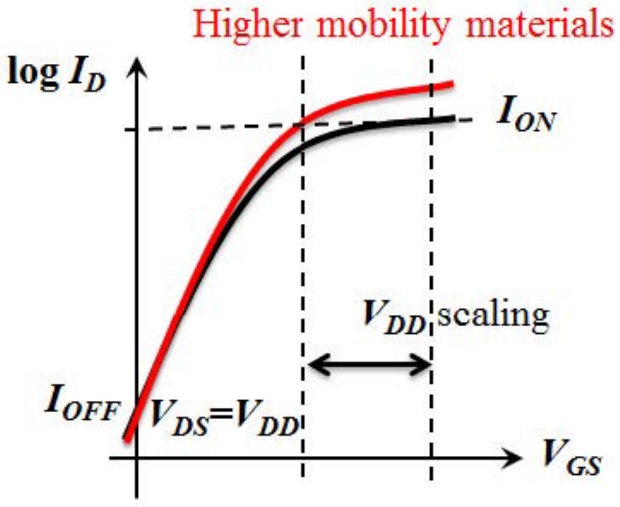


Figure 1-3: The advantage of transfer characteristic in III-V MOSFETs

As device gate lengths are further shrunk down below 100 nm in Si SCMOS, two main issues, power consumption and gate delay, are on the rise. Power consumption consists of active power (P_{active}) and standby power ($P_{standby}$), which can be written as equation (1.3) and (1.4). Low OFF-state current (I_{OFF}) and low supply voltage (V_{DD}) are required to increase performance while the gate length of MOSFETs is decreased following Moore's Law.

$$P_{active} = a \cdot f \cdot C_{load} \cdot V_{DD}^{\ 2} \qquad (1.3)$$

$$P_{standby} = I_{off} \cdot V_{DD}^{\ 2} \qquad (1.4)$$

The decrease of intrinsic gate delay time follows with equation (1.5) [13], which explains that the intrinsic gate delay is proportional to gate length. However, the intrinsic gate delay time doesn't decrease proportionally following the decrease in gate length below the 45 nm technology node, as shown in Figure 1.4.

$$\tau = \frac{(1-\delta)V_{DD} - V_T + \left(C * f \cdot V_{DD} / C_{inv} \cdot L_G\right)}{(3-\delta)V_{DD}/4 - V_T} \frac{L_G}{v} \qquad (1.5)$$

A continuous increase in carrier velocity is hard to achieve because of short channel effects, which are strongly detrimental for device performance in short channel devices [13, 14]. In other words, carrier velocity is expected to increase as gate length decreases, so the term L_G/v in equation (1.3) is expected to decrease, but in reality, the carrier velocity does not further increase due to short channel effects.

In fact, as the gate length is reduced below 45 nm node, reduction of L_G is not the dominant factor because of increase in L_G/v. Therefore, in order to achieve next

generation, higher performance CMOS devices, higher mobility materials should be studied and developed.

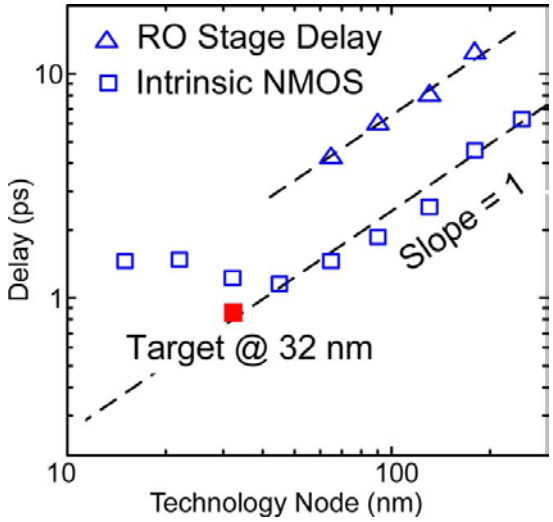


Figure 1-4: The trend of intrinsic transistor delay for benchmark technologies. Gate delay commensurate with until 45 nm technology node, but it shows discrepancy from 45 nm node [14].

In addition, high-κ dielectric material is inevitable not only to maintain Moore's Law, but also to improve device performance. Although III-V materials are attractive materials for future CMOS technology, there is a critical issue of interface layers in III-V channel materials. Either native oxide, or SiO_2 on III-V channel substrate results in Fermi level pinning which results in a poor gate modulation [15, 16]. Thus, forming a better interface layer is an important issue in III-V CMOS technology.

As for the gate dielectrics, high-κ materials require 1) a large band gap with sufficient band offsets for both electrons and holes, 2) thermodynamically stable and low

interface trap density with channel layer, 3) compatibility with current gate electrode, as well as with conventional CMOS processing [17-19].

Properties	**SiO_2**	**Al_2O_3**	**HfO_2**	**ZrO_2**	**La_2O_3**	**BeO**
Dielectric Constant (κ)	3.9	8~9	18~25	18~30	20~36	6~7
Bandgap	9	8.8	6.0	5.8	4.3	7.9
Band offset for electron (eV)	3.5	2.8	1.5	1.4	2.3	2.6
Band offset for holes (eV)	4.4	4.9	3.4	3.3	0.9	4.1

Table 1-2: Material properties comparison of several gate oxides

The main challenge in III-V MOSFETs with a higk-κ gate oxide is formation of a high quality interface between the oxide and the III-V channel substrate. Generally, III-V materials form an unstable and poor quality interface with oxygen [7]. A large amount of In-O, Ga-O, or As-O bonds are observed on the interface between high-κ and III-V surfaces which leads to Fermi level pinning and thereby, a high interface trap density due to oxygen diffusion [20-22]. Therefore, in order to improve interface quality, an interface passivation layer, or additional chemical treatment is necessary during device processing [23, 24].

Current silicon device architecture is pursuit the non-planar structure, such as FinFETs. For FinFET device process, source and drain formation is processed with ion implantation. However, ion implantation leads to damage on the S/D region, and it can be

leakage current path during device operation. Also, it gives rise to doping uniformity problem, since it has shadow effect when ion implantation is carried out.

1.3 CRITERIA OF HIGH-K GATE DIELECTRIC

As shown in table 1-2, it is seen that many dielectrics with high-κ values exist. However, to select suitable high-κ dielectric is quite complicated. As for the gate dielectrics, high-κ materials require several aspects to utilize as gate dielectric.

1) Permittivity: It is necessary to have higher permittivity than that of SiO_2. It is preferred to use one with high dielectric constant, 20~40. Basically, however, it is considered that there is tradeoff between the dielectric constant and bandgap. In the other words, high-κ value dielectric materials are usually inherent low bandgap.

2) Bandgap and band offset: Typically, it is required to be over 5 eV in bandgap. The Schottky emission of electron or holes into the oxide bands can be prevented when the band offset with silicon is over 1.0 eV. For SiO_2 and Si substrate, the conduction band and valance band offsets with silicon present 3.0 eV and 4.8 eV. If the conduction band offsets is not over 1.0 eV, undesired leakage current can be achieved and these oxide will be disregard in gate dielectric application [25].

3) Thermodynamic stability: It is obvious to acquire the good interface between all gate dielectric with silicon substrate. The interface property is critical factor in general device performance. High stability in gate oxide represents less reaction with silicon substrate, so that less produce interfacial SiO_2. It is inevitable to regrow interfacial layer

when high-κ oxide deposit on silicon substrate since inter-diffusion or chemical reaction occurs. Therefore, the high-κ dielectric inherent high Gibbs free energy can keep from reaction with silicon [26, 27]. Due to its low-κ property, the interfacial SiO_2 tends to compromise the total capacitance density of the gate capacitor, and, eventually, it screens out an advantage of high-κ application.

IA												IIIA	IVA	VA	VIA	VIIA	O
*																	*
H	IIA																He
1	1											*	*	*	*	*	*
Li	Be											B	C	N	O	F	Ne
1	1											Al	Si	*	*	*	*
Na	Mg	IIIB	IVB	VB	VIB	VIIB	VIII			IB	IIB			P	S	Cl	Ar
1	Ca	1	2	1	1	1	1	1	1	1	1	1	1	*	*	*	*
K		Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	As	Se	Br	Kr
*	Sr	Y	Zr	1	1	Θ	1	1	1	*	1	1	1	1	1	*	*
Rb				Nb	Mo	Tc	Ru	Rh	Pd	Ag	Cd	In	Sn	Sb	Te	I	Xe
*	3	&	Hf	1	1	1	1	1	*	*	*	*	1	1	Θ	Θ	Θ
Cs	Ba			Ta	W	Re	Os	Ir	Pt	Au	Hg	Ti	Pb	Bi	Po	At	Rn
Θ	Θ	&&	Θ	Θ	Θ	Θ	Θ	Θ									
Fr	Ra		Rf	Db	Sg	Bh	Hs	Mt									

Θ	= Not a solid at 1000 K
*	= Radioactive
1	= Si + MO_x -> M + SiO_2
2	= Si +MO_x -> MSiy + SiO_2
3	= Si + MO_x -> M + Si_xO_y

&	La	Ce	Pr	Nd	Θ Pm	Sm	Eu	Gd	Td	Dy	Ho	Er	Tm	Yb	Lu
&&	Θ	Θ	Θ	Θ	Θ	Θ	Θ	Θ	Θ	Θ	Θ	Θ	Θ	Θ	Θ
	Ac	Th	Pa	U	Np	Pu	Am	Cm	Bk	Cf	Es	Fm	Md	No	Lr

Table 1-3: Thermodynamic stability of binary oxides incorporating with silicon

4) Film morphology: Basically, rapid thermal annealing at 1000 C is necessary in Si CMOS process [28]. The gate dielectric materials must stand this process without crystallization. This is severe ambient for high-κ dielectric materials not to change its crystallinity since their crystalline temperature is low and it can be affected in RTA [25]. Typically, some high-κ materials can easily crystallize at lower temperature condition,

which results in high leakage path through crystallized grain boundaries, and failure with EOT scaling [29].

5) CMOS process compatibility: The deposition method of the high-κ dielectric should be compatible with current CMOS process. The high-κ oxide is required to be grown with good thickness uniformity, interfacial properties, and thermal stability. The atomic layer deposition (ALD) is known as the most excellent deposition system for thin gate dielectrics [17-19].

The high-κ gate application has several limitations due to its chemical bonding, such as, structural defects, mobility degradation, threshold voltage degradation, and reliability issues. Unfortunately, these challenges are more worse in III-V channel devices because III-V materials are not able to form better interfacial oxide layer compared SiO_2 in silicon substrate [7].

Briefly, high-κ valued oxides have intrinsic defects like oxygen vacancies, oxygen interstitials, or oxygen deficiency [30]. Basically, it is the fact that oxygen vacancy is considered as a main reason for oxide traps. Due to the thermal stability in high-κ oxides, the inter-diffusion occurs, resulting to electrical degradation in device electrical characteristics [31]. Another concern is the carrier mobility degradation. Generally, the channel mobility in the high-κ on silicon is dramatically degraded because higher oxide traps and interface trap densities exist. These defects contribute to Coulomb scattering because defects tend to be an acceptor, thus, these can occupy not only within the bandgap, but also at the energy sites aligned with III-V materials' conduction band [32-34]. Furthermore, the soft optical phonons can be problematic in high-κ oxides

because of their ionic bonds. Moreover, threshold voltage degradation should be concerned. Inside high-κ materials, large amount of fixed charges present and they are responsible for charge trapping sites which affect V_{th} control. In addition, fermi pinning effect pinning (FLP) affects also threshold voltage, because oxygen vacancy, especially, produce charges to metal gate electrode [35-38]. For III-V channel device, a large amount of In-O, Ga-O, or As-O bonds are observed on the interface between high-κ and III-V surfaces which leads to Fermi level pinning and thereby, a high interface trap density due to oxygen diffusion [20-22]. Therefore, in order to improve interface quality, an interface passivation layer, or additional chemical treatment is necessary during device processing [23, 24].

1.4 OUTLINE

The objective of this work is to study the improvement of III-V interfaces by applying various scientific processes, as well as III-V device engineering. Among III-V materials, In-rich InGaAs channel material is selected due to its high electron mobility and high drive current capability [39]. As an interface passivation layer, Beryllium oxide (BeO) is employed to InGaAs MOSFETs. BeO is known to have a wide bandgap, high thermal stability, and sufficient valence and conduction band offsets [19, 40-42]. For interface passivation process, the impact of *in-situ* Argon (Ar) ion plasma treatment is studied by fabricating InGaAs MOSCAPs.

In chapter 2, the material properties of Atomic Layer Deposition (ALD) BeO are investigated to reveal its chemical, physical, electrical, and mechanical properties [43]. With ALD BeO, Rutherford backscattering (RBS) and nuclear reaction analysis (NRA) measurement is carried out to quantify the hydrogen content in quantitatively. Also, the band gap of ALD BeO is evaluated using reflection electron energy loss spectroscopy (REELS). The mechanical properties of ALD BeO like the Young's modulus and hardness are evaluated by a nanoindentation measurement.

In Chapter 3, to demonstrate the potent of BeO gate stack, surface channel structure has been applied. InGaAs surface channel MOSFETs with Al_2O_3 or BeO gate dielectric is studied [19]. By comparing BeO with Al_2O_3 gate stack with XPS, TEM, and MOS capacitance, the interface quality of BeO and InGaAs is investigated. Long channel BeO MOSFETs is analyzed with transfer and output characteristics and effective mobility by comparing with Al_2O_3 MOSFETs.

Chapter 4 introduces Quantum Well (QW) InGaAs MOSFETs employing an interface passivation layer (IPL) with BeO [44]. Quantum Well MOSFETs are designed to be immune to short channel effect [45-47]. Device performance including drive current, transconductance, subthreshold swing and effective mobility of devices are examined. Additionally, BeO MOSCAPs are studied to observe the interface property when BeO is applied as an IPL. MOSCAP characteristics are investigated and compared between devices with and without a BeO IPL.

In chapter 5, as a device fabrication approach for interface improvement, *in situ* Ar ion plasma treatment is considered [48]. This process comes from Ar ion

bombardment in a plasma sputtering system. It is done in a plasma enhanced ALD (PEALD) system which allows remote generation of a low-power plasma MOS capacitance characteristics are examined to study the electrical effect of interface property. X-ray photoelectron spectroscopy (XPS) is used to observe chemically changes.

Summary of this dissertation and future work is addressed in chapter 6. Especially, as process development for high-κ improvement deuterium (D_2) high-pressure annealing is utilized on InGaAs substrate. It is reported that D_2 can improve hot carrier injection reliability to compensate Si dangling bond better than hydrogen in Si device process [49, 50]. By measuring general C-V characteristic and comparing interface trap density (D_{it}), the effect of D_2 high-pressure annealing is examined, and future action items are suggested. In addition, the solid phase doping is introduced as 3D doping application [51]. Basically, solid phase doping is that dopant film is deposited on substrate and activated by RTA process. It is observed that the change in I-V characteristics after doped InGaAs substrate. In order to uniform dope on 3D device structure, this novel doping method is tried to apply to 3D structure.

Chapter 2: Atomic layer deposition Beryllium oxide on III-V materials

It is reported that bulk crystalline and ceramic forms of BeO have many excellent materials properties as described in Table 2.1. Unlike other alkaline earth oxides and candidate high-κ gate dielectrics with significant ionic character, [7, 52] the chemical bonding in BeO exhibits significant covalent character. Unfortunately, aside from these basic thin film and interfacial electrical properties, many of the interesting properties for bulk crystalline and ceramic BeO have yet to be reported or are still uncertain for ALD BeO thin films. [1]

2.1 LIQUID TYPE BERYLLIUM OXIDE ALD

Previous ALD BeO was grown with solid-type beryllium source, called dimethylberyllium ($(Be(CH)_3)_2$). It is synthesized with $BeCl_2$ using Grignard metathesis [53]. Generally, the solid type precursor requires relatively high-temperature to sublimate, even overdrive system limitation. The solid typed ALD source remains some white colored solid in deposition system, which may BeO or dimethylberyllium itself transporting by carrier gas. It can be source of contamination to substrate. Thus, liquid type beryllium precursor is developed lead by Prof. Todd Hudnall in Texas State University.

[1]This chapter is based on reference [43]: **D. Koh**, J. H. Yum, S. K. Banerjee, W. A. Lanford, B. L. French, M. French, P. Henry, H. Li, M. Kuhn, S. W. King. "**Investigation of ALD BeO Material Properties for High-κ Dielectric Applications**", *J. Vac. Sci Technol. B***32**,03D117 (2014).
D.Koh contributed to BeO film on Si sample preparation, topological measurement, optical index extraction, and CV measurement.

In this chapter, to observe chemical composition in ALD BeO, Auger Electron Spectroscopy (AES), X-ray Photoelectron Spectroscopy (XPS), Rutherford backscattering (RBS), and Nuclear Reaction analysis (NRA) are carried out with 124 nm bulk BeO on Si substrate. As well as material chemical properties, the experimental work.

Crystal Structure	Wurtzite
Lattice Constant (nm)	a=0.2698, c=0.4378
Melting point (℃)	2530 ± 10
Mass density (g/cm^3)	3.001 ± 0.001
ΔH_F^{291} (KJ/mol)	-616.2 ± 2.4
ΔS^{298} (J/mol K)	14.1 ± 0.2
Heat capacity – C_p^{298} (J/mol K)	25.3 ± 0.2
Refractive index – n	1.719 ⊥ c-axis 1.733, ∥ c-axis
Static/low frequency dielectric constant – k	6.94, ⊥ c-axis 7.65, ∥ c-axis
Band gap (eV) - E_g	10.6
Thermal conductivity (W/mK) – k	370 (@300K)
Volume thermal expansion coefficient (10^{-5}/K)	2.66 ± 0.1
Linear thermal expansion coefficient (10^{-6}/K)	5.99, ⊥ c-axis
Bulk modulus (GPa)	212 ± 3
Young's modulus (GPa)	369.6, ⊥ c-axis 418.9 ∥ c-axis
Sound velocity (m/s)	12370, longitudinal 7449, tranverse
Poisson's ratio – v	0.2, ν_{112} = 0.38,ν_{13}= 0.25
Piezoelectric constant (10^{-12} C/N) – d_{33}	0.24
Pyoelectric constant (10^{-6} C/m^2℃)	-0.34

Table 2-1: Summary of properties for crystalline and ceramic/poly-crystalline BeO.

2.2 BERYLLIUM OXIDE CHEMICAL COMPOSITION INVESTIGATION

To observe chemical composition in ALD BeO, various chemical analysis, such as AES, XPS, NRA, and RBS is carried out with 124 nm bulk BeO on Si substrate. The surface composition and chemical bonding in ALD BeO film is observed with AES and XPS. Figure 2-1 shows an AES spectrum acquired from the ALD BeO film as-loaded and after 60 s Ar+ sputtering. The AES spectra clearly show the presence of a trace level of surface carbon contamination that disappears after light Ar+ sputtering. The remaining features in the sputtered ALD BeO AES spectrum include Be KVV and O KLL Auger peaks whose line shapes are consistent with those obtained from BeO thin films formed via *in-situ* oxidation of metallic Be surfaces or bulk BeO ceramics [54-56].

The higher peak-to-peak ratio for oxygen relative to Be in the AES spectrum is due to the higher sensitivity of AES to the O KLL relative to the Be KVV and is not indicative of an oxygen rich BeO film.

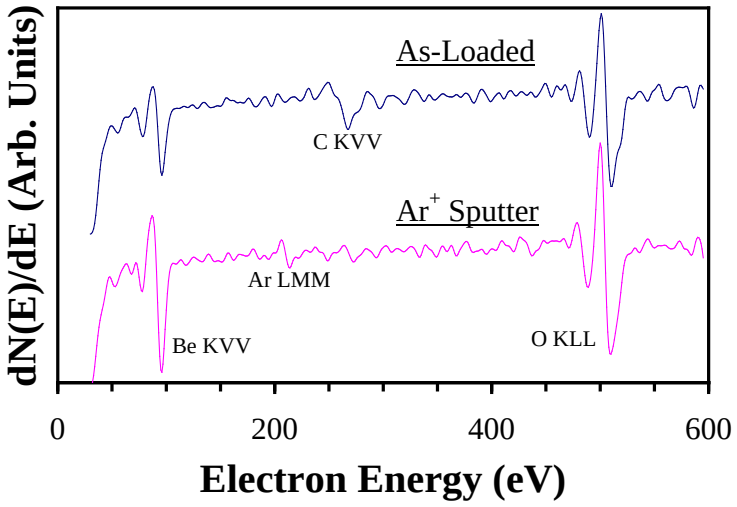


Figure 2-1: AES spectra of ALD BeO before and after Ar+ sputtering.

The surface composition and chemical bonding for the ALD BeO film were additionally investigated using XPS. Similar to AES, an XPS survey spectrum of the as-loaded ALD BeO film showed the presence of a surface carbon contamination layer that was reduced by Ar+ sputtering.

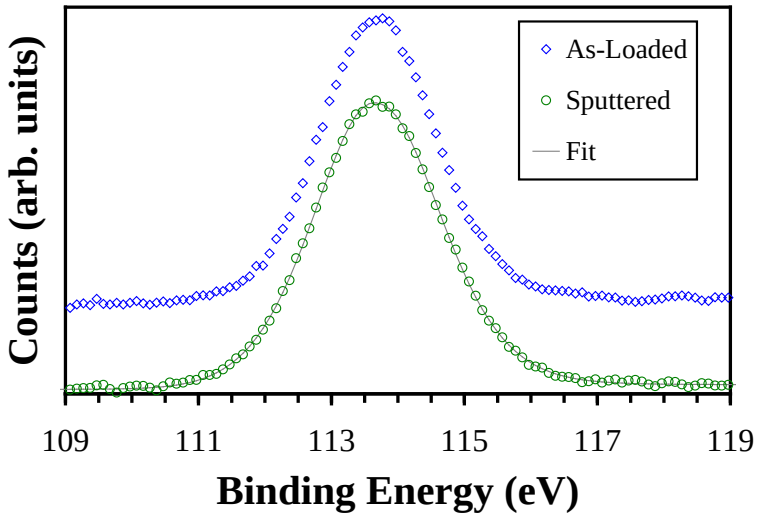


Figure 2-2: XPS spectra of ALD BeO Be 1s core level before and after Ar+ sputtering.

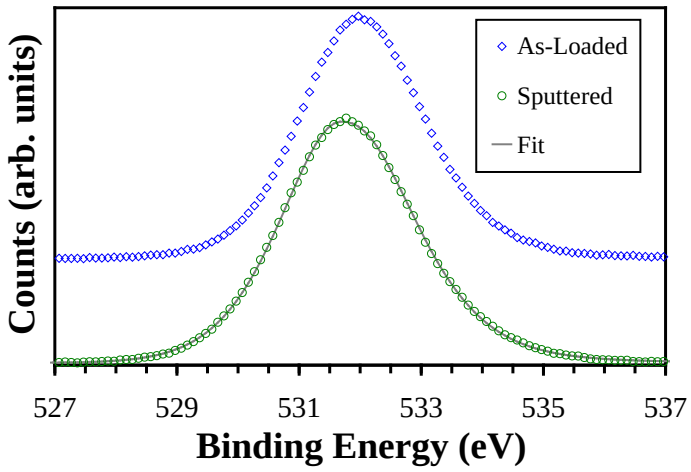


Figure 2-3: XPS spectra of ALD BeO O 1s core level before and after Ar+ sputtering.

Figures 2-2 and 2-3 show XPS spectra for the Be 1s and O 1s core levels of the ALD BeO film before and after sputtering. These spectra were corrected for charging by aligning the C 1s core level pre-sputtering to 285.0 eV. The centroid of the Be 1s and O 1s core levels was determined via fitting to a mixed Gaussian–Lorentzian line shape with a Shirley background. As shown in Figure 2-2 and 2-3, the core levels were well fitted using single peaks centered at 113.6 and 531.7–532.0 eV, respectively. These energy positions are consistent with Be–O bonding and other XPS measurements of BeO ceramics [57]. Ar+ sputtering was observed to have minimal effect on the Be 1s position but did result in a slight increase in the full width half maximum (FWHM) from 2 to 2.2 eV. For the O 1s, Ar+ sputtering also resulted in a slight broadening of the FWHM from 2.2 to 2.4 eV but also induced a slight decrease in the O 1s position from 532.0 to 531.7 eV. The large FWHM and slight broadening of the Be 1s and O 1s core levels can be attributed to a combination of the amorphous structure of the ALD BeO film, charging, and sputtering induced surface disorder. The decrease in the O 1s core level position is likely due to the removal of some surface carbonate or adsorbed oxygen species not deconvoluted in fitting the as-loaded O 1s spectra.

To investigate the bulk composition of the ALD BeO film and more closely check the stoichiometry and presence of residual carbon and hydrogen contamination, additional RBS and NRA measurements are performed. The deuteron induced NRA measurements are shown in Figure 2-4 where a number of strong peaks from nuclear reactions can be observed. Close examination of Figure 2-4 reveals that the carbon peak

is actually a doublet, with the lower energy C peak at channel 198 being an order of magnitude stronger than the higher energy C peak at channel 202. This is indicative of carbon present both at the film/substrate interface (lower energy) and the surface (higher energy). These observations are also consistent with the prior AES and XPS measurements that showed the presence of some surface carbon on the ALD BeO film.

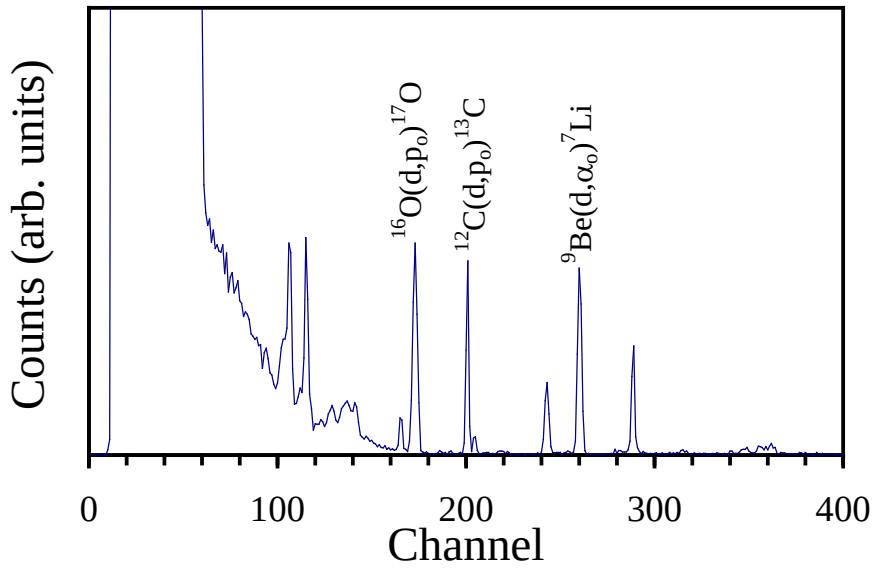


Figure 2-4: Nuclear Reaction Analysis (NRA) spectrum of ALD BeO.

For Be analysis, the strong peak at channel 257 from the $^{9}Be(d,\alpha_0)^{7}Li$ reaction was used. To establish the nuclear reaction cross section/calibration constant for Be, the calibration constant was varied until the Si substrate edge in the RUMP simulation matched the measured RBS spectrum shown in Figure 2-5.

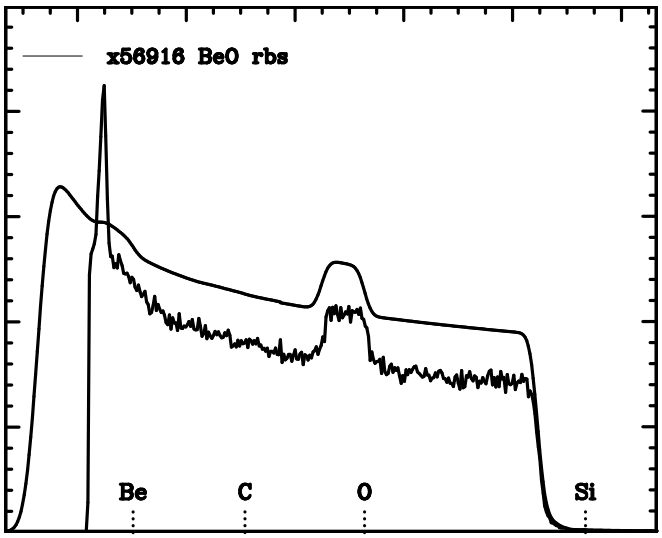


Figure 2-5: Rutherford Backscattering Spectrometry (RBS) spectrum of ALD BeO.

This procedure relies on the energy loss rate of He in the target material. The concentration of Be, O, and H were then determined from RUMP RBS simulations. These simulations yielded concentrations of 7.2, 6.3, and 0.6×10^{22} atoms/cm^3 for Be, O, and H, respectively. The combined NRA–RBS results indicate the film is slightly Be rich (Be/O = 1.1 ± 0.05) with a low but significant hydrogen content of 4%. However, the slight deviation from Be/O stoichiometry is nearly within the error bar for Be content. The full elemental composition from RBS also allows the mass density to be estimated at 2.8 ± 0.1 g/cm^3 which is substantially less than the value determined by XRR, but within the XRR error bars and still close to the theoretical density of 3.0 g/cm^3. The lower RBS

value for mass density is consistent with the as deposited amorphous structure of ALD BeO as confirmed by separate x-ray diffraction measurements [58, 59].

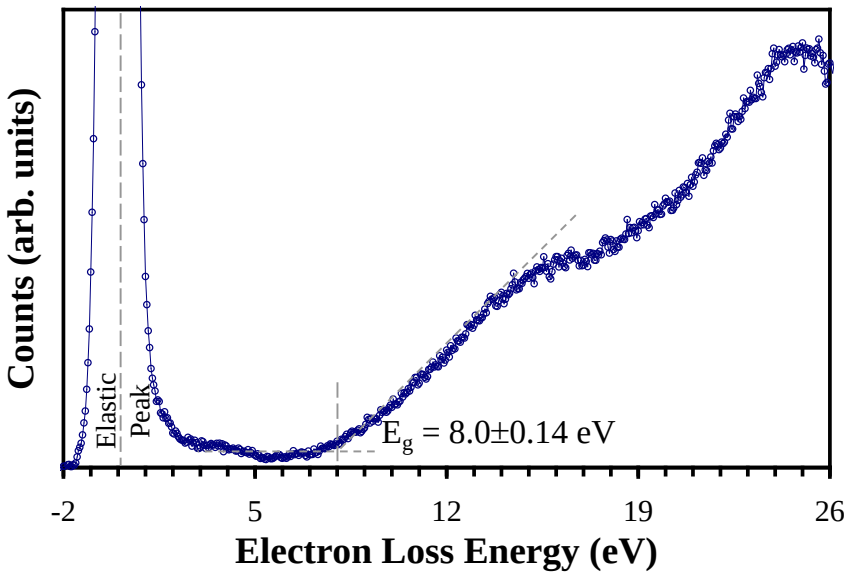


Figure 2-6: REELS spectrum of as-loaded ALD BeO collected using a 2.5 keV electron beam.

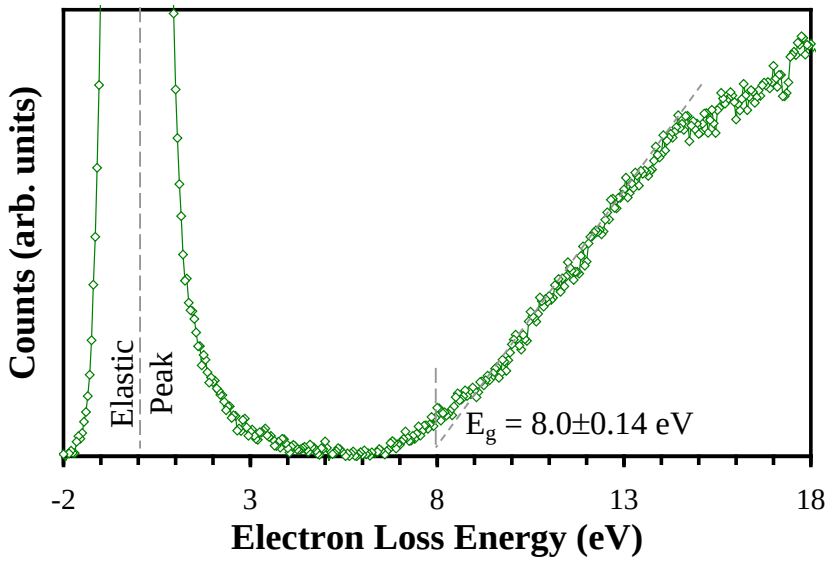


Figure 2-7: REELS spectrum of ALD BeO collected after Ar^+ sputtering using a 2.5 keV electron beams.

Figures 2-6 and 2-7 show 2.5 keV REELS spectra acquired from the ALD BeO film before and after Ar^+ sputtering, respectively. The REELS spectrum in Figure 2.6 shows a maximum in loss intensity at approximately 24.6 ± 0.1 eV. The position of this maximum is consistent with prior EELS measurements on single crystalline BeO and BeO thin films where a maximum at 24.5 eV has been observed and attributed to the excitation of a bulk plasmon [60-63].

The position of this plasmon is also consistent with a thin film mass density [60, 62] of 3.0 g/cm^3 which is in excellent agreement with the theoretical density for crystalline BeO. However, ALD BeO has only been observed to crystallize after rapid thermal annealing at temperatures of 600 ~ 900℃ and such films are not investigated here. Based on the combined XRR, RBS, and REELS mass density measurements, it is revealed that the mass density for as-deposited ALD BeO is 3.0 ± 0.3 g/cm^3.

2.3 ALD BERYLLIUM OXIDE MECHANICAL PROPERTIES

The mechanical properties of ALD BeO were also investigated via nano-indentation. The Young's modulus and hardness values determined from these measurements are summarized in Table III. As can be seen, a high Young's modulus and hardness of 330 ± 30 and 33 ± 5 GPa were, respectively, determined. The Young's modulus value is lower but close to the values of 380 ~ 420 GPa reported for BeO single crystals and ceramics [64]. These values are also substantially higher than those reported for other amorphous ALD high-κ dielectrics. Specifically, the Young's modulus and

hardness values reported in the literature for ALD Al_2O_3 are 180 ~ 220 and 10 ~ 12 GPa [65, 66], respectively, and for HfO_2, similar values of 150 ~ 220 and 9 ~ 11 GPa have been reported [66, 67]. For additional comparison, nanoindentation measurements performed on the same 1 lm diamond film utilized in the XRR measurements indicated a Young's modulus and hardness of 500 ± 50 and 35 ± 5 GPa, respectively. These results are consistent with BeO being one of the hardest materials next to diamond[64].

In summary, an array of thin film metrologies has been utilized to investigate the material properties of BeO films prepared by ALD. The as-deposited films show a low H and C content and are nearly stoichiometric. Based on combined XRR, RBS, and REELS measurements, the mass density of ALD BeO was concluded to be 3.0 ± 0.3 g/cm^3 and similar to the theoretical value of 3.0 g/cm^3 for crystalline wurtzite BeO. ALD BeO was also found to exhibit a wide band gap of 8 eV and high Young's modulus of 330 ± 30 GPa. Both of these properties are slightly reduced relative to the reported values for single crystalline wurtzite BeO but are substantially higher than those reported for SiO_2 and other high-κ dielectrics (Al_2O_3 and HfO_2). These results support both the excellent device and reliability performance reported for Si and III-V MOSFET devices fabricated with ALD BeO as the gate dielectric.

Chapter 3: Surface Channel InGaAs MOSFETs with BeO

In previous chapter, chemical and mechanical properties of liquid source ALD BeO were investigated, presenting its possibility of high-κ application. To exam the potent of ALD BeO as high-κ for III-V channel, surface channel InGaAs MOSFETs are fabricated and characterized in this chapter. The interface quality of ALD BeO is evaluated using XPS, TEM, and MOS capacitance. BeO surface channel InGaAs MOSFETs are fabricated to understand electrical properties. [2]

3.1 Surface stoichiometry of ALD BeO on InGaAs

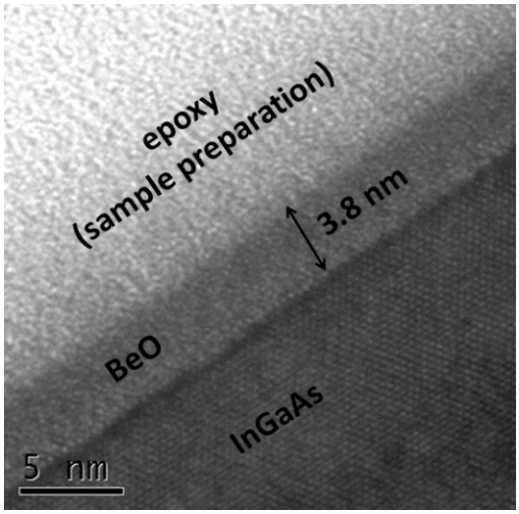


Figure 3-1: High resolution cross-sectional TEM analysis of ALD BeO grown on InGaAs

[2]This chapter is based on reference [19]: **D. Koh**, J-H. Yum, T. Akyol, D. A. Ferrer, M. Lei, T. W. Hudnall, M. C. Downer, C. W. Bielawski, R. Hill G. Bersuker, S. K. Banerjee. "**Novel Atomic Layer Deposited Thin Film Beryllium Oxide for InGaAs FETs**", Aug. 27-30, ***IPRM 2012***, Santa Barbara, CA, USA.
J.-H. Yum and T. Akyol designed this experiment and transferred to D. Koh. D. Koh reproduced metrology measurement (AFM and TEM), as well as capacitance characterization.

Cross-sectional Transmission Electron Microscopy (TEM) images of BeO on InGaAs are indicated in Figure 3-1, demonstrating a sharp interface with InGaAs surface. Surface Atomic Force Microscope (AFM) images of ALD grown BeO and Al_2O_3 films on InGaAs substrate in Figure 3-2 compare surface roughness values. BeO film presents a low RMS surface roughness of 0.19nm in 3×3 μm sized scan area.

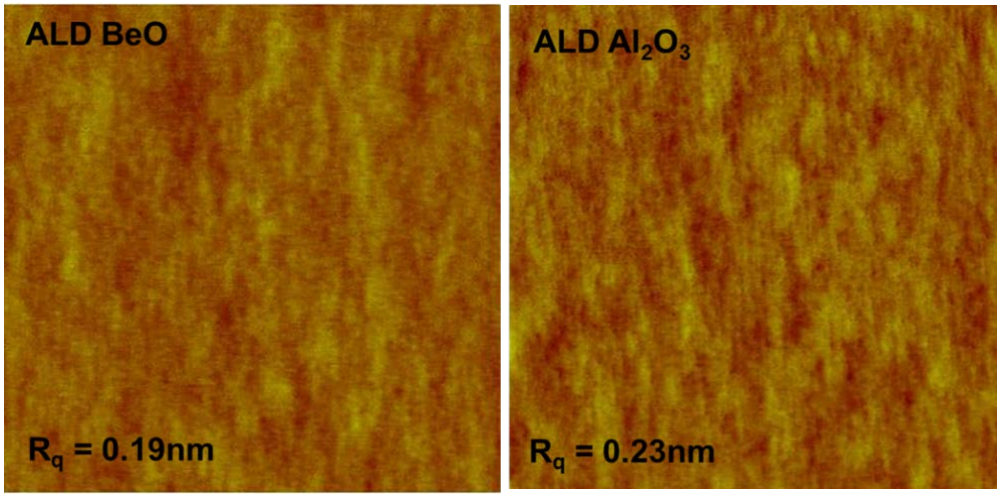
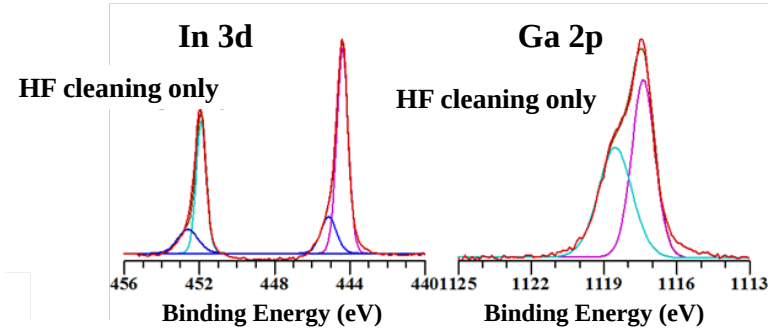


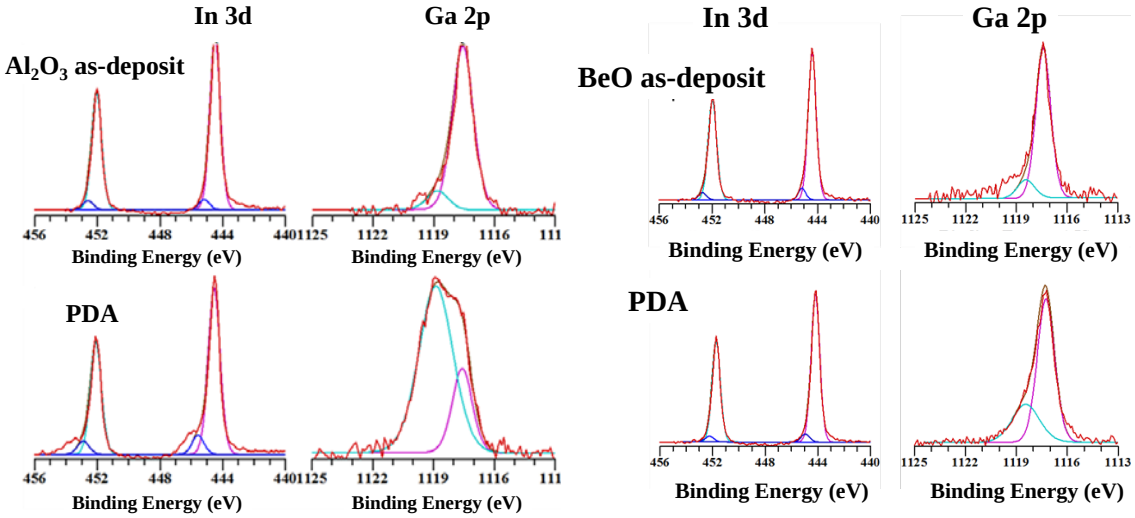
Figure 3-2: AFM and surface roughness analysis of ALD BeO and Al2O3 grown on InGaAs

X-ray photoelectron spectroscopy (XPS) demonstrates the interface quality comparison between Al_2O_3 and BeO film before and after without post-deposition annealing (PDA) as shown in Figure 3-3. Comparing as-deposited XPS result, the self-cleaning effect is observed on BeO deposited InGaAs surface by showing native oxides

reduction (In_xO_y, Ga_xO_y and As_xO_y). After post deposition annealing (PDA), XPS presents that the native oxide on BeO deposited InGaAs surface is less grown than that of Al_2O_3 deposited InGaAs surface. It is because BeO has better thermal stability leading less oxide out-diffusion during PDA.



(a)

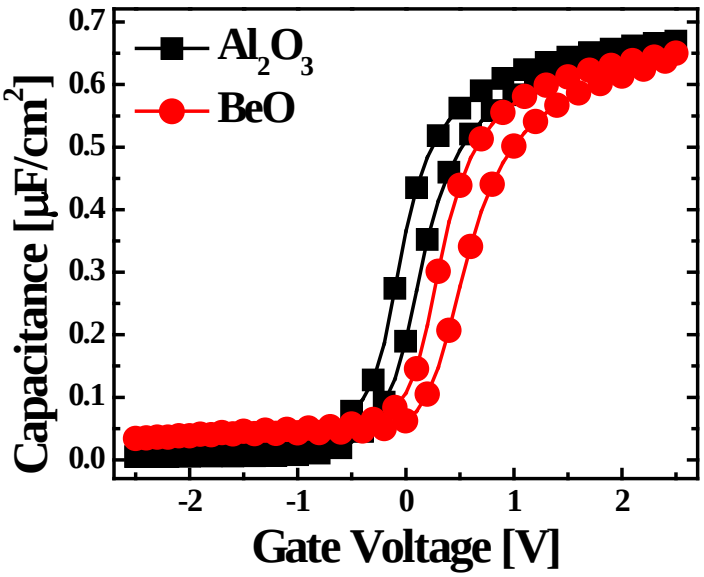


(b) (c)

Figure 3-3: XPS spectrum comparison of ALD Al_2O_3 and BeO film deposited InGaAs substrate. (a) XPS spectra of initial InGaAs surface, (b) Al_2O_3 deposited InGaAs surface before and after PDA, and (c) BeO deposited InGaAs surface before and after PDA.

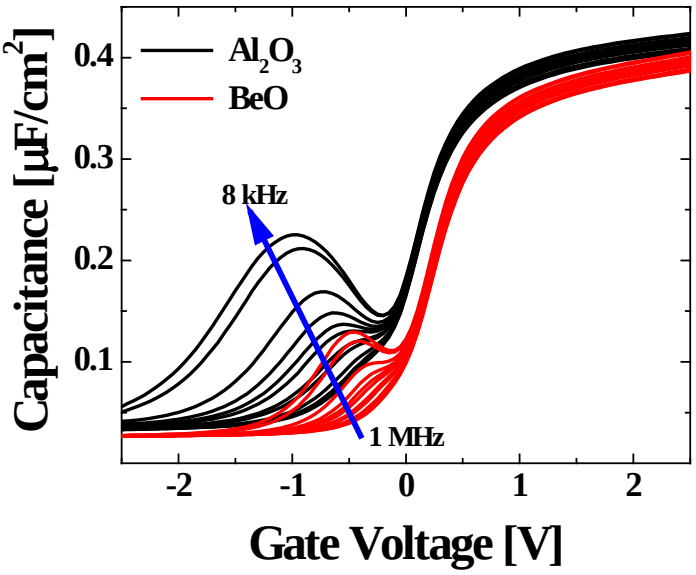
3.2 MOS CAPACITANCE CHARACTERISTIC COMPARISON

MOS capacitor is simple experimental structure to estimates the dielectric properties and interface quality with substrate. Before transistor characterization, MOS capacitance is fabricated and compared with Al_2O_3 MOSCPAs. For MOS capacitor fabrication, InGaAs grown on semi-insulating InP is used for substrate. Initial cleaning with diluted HF is carried out. ALD Al_2O_3 or BeO is deposited up to around 10nm and 9 m, respectively, to adjust the same EOT (5 nm). TaN is deposited as gate metal pad and then residual area is etched by using TaN as a hard mask.

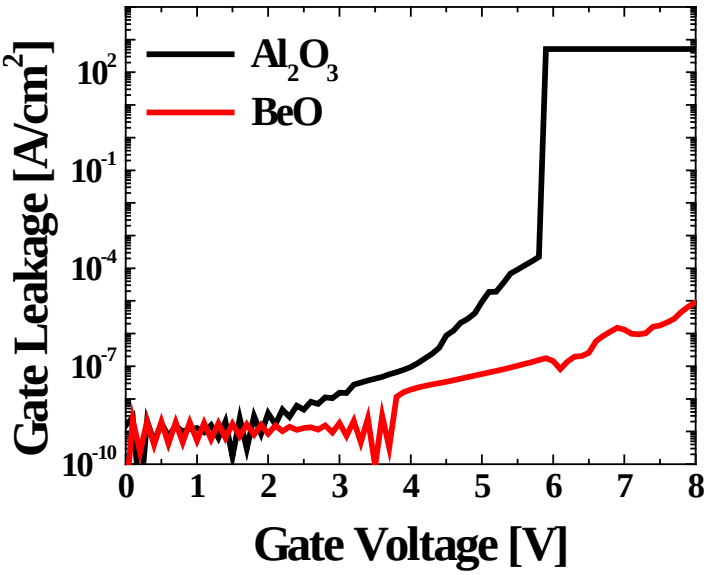


(a)

Figure 3-4

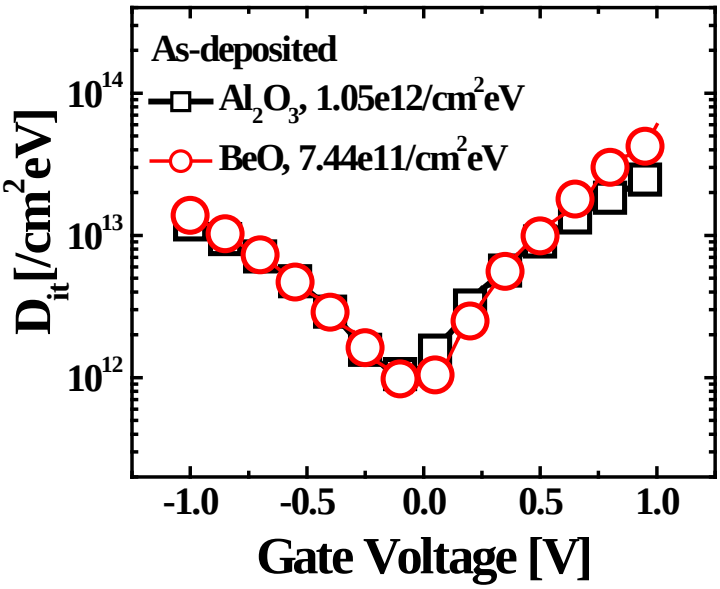

Capacitance [μF/cm²]
0.4
0.3
0.2
0.1
Al2O3
BeO
8 kHz
1 MHz
-2
-1
0
1
2
Gate Voltage [V]

(b)


Gate Leakage [A/cm²]
10²
10⁻¹
10⁻⁴
10⁻⁷
10⁻¹⁰
Al2O3
BeO
0
1
2
3
4
5
6
7
8
Gate Voltage [V]

(c)

Figure 3-4



(d)

Figure 3-4: The MOS C-V characteristic comparison between Al_2O_3 and BeO MOSCAPs. (a) C-V hysteresis (b) frequency dispersion (c) gate leakage current density, (d) interface trap density

BeO InGaAs MOS capacitor demonstrates that the threshold voltage shifts in positive direction. It means that BeO includes less interface charges because the ideal threshold voltage equation is calculated with metal-semiconductor work function (Φ_{ms}), interface charge (Q_i), depletion charge (Q_d), and the surface potential (ϕ_B) shown in equation (3.1).

$$V_{th} = \Phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_d}{C_i} + 2\phi_F \qquad \text{eq. (3-1)}$$

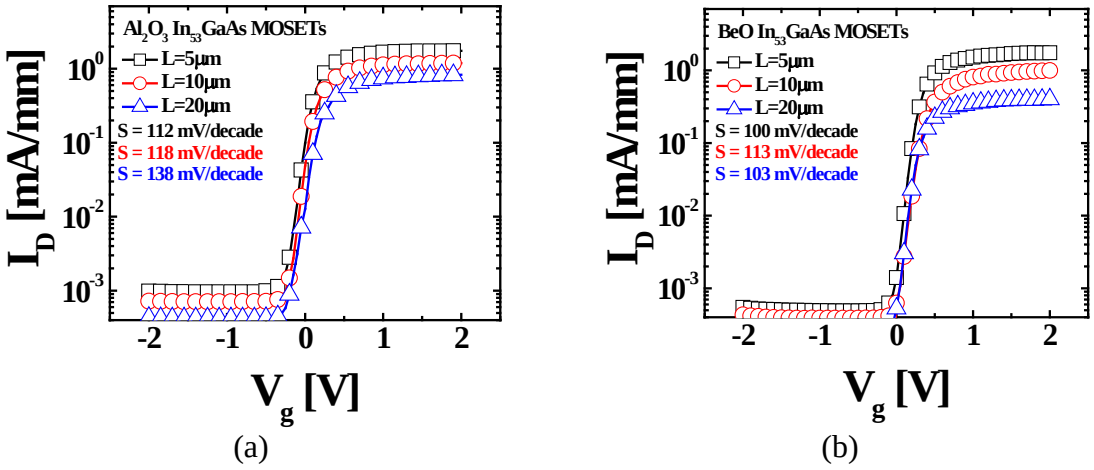
It is assumed that the work function, depletion charge, and surface potential are the same since MOSCAPs are fabricated on the same substrate, but positive charged interface trap is only different parameter. Therefore, the positive shifted threshold voltage indicates the

less interface trap density. The C-V frequency dispersion in Figure 3-4 (c) is in agreement with interface trap density shown in Figure 3-4 (d) by demonstrating less dispersion. Since the band-gap of BeO is larger than Al_2O_3, lower gate leakage current density is measured at BeO MOSCAPs.

3.3 SURFACE CHANNEL INGAAS MOFETS FABRICATION AND CHARACTERIZATION

Based on BeO film properties on InGaAs substrate and MOS capacitance characteristic, surface channel InGaAs MOSFETs is fabricated and characterized. The gate last MOSFET process is employed with 200 nm undoped $In_{0.53}Ga_{0.47}As$ epi-layer which is grown on semi-insulating (100) InP wafers. The native oxide on InGaAs surface was cleaned in 1% HF solution for 1 min. A capping layer of 100Aº ALD Al_2O_3 dielectric was deposited to prevent As-out-diffusion and surface degradation during the S/D activation annealing. Based on align mark, S/D regions were defined and doped with Si ion implantation at 35 keV, $5 \times 10^{14}/cm^2$. After removal of photoresist, S/D activation annealing was done at 700 ºC for 10 ~15 s and Al_2O_3 capping layer was etched off using buffered oxide etchant (BOE). Surface was cleaned and passivated in 1% HF solution for 1 min, and then in 20% $(NH_4)_2S$ solution for 10 min at room temperature. Subsequently, 100 cycle BeO and 90 cycle Al_2O_3 gate dielectrics were grown in the ALD system at 250°C in order to achieve the same EOT. Next, a post-deposition (rapid thermal) annealing (PDA) step was performed at 500 ºC for 2 min in N_2 ambient, followed by a 2000 Å thick TaN metal-gate deposition using a dc magnetron sputtering system. TaN

gate was patterned and etched by CF_4 plasma RIE process. For S/D contacts, BeO/Al_2O_3 dielectric layer where covered on S/D region is etched in BOE after S/D patterning. S/D metallization was finished with AuGe/Ni/Au (40/10/50 nm) lift-off process.



(a) (b)

Figure 3-5: I-V characteristics of n-InGaAs MOSFETs with (a) Al_2O_3 and (b) BeO gate dielectric

The minimum subthreshold swing (SS) of InGaAs MOSFETs (L=5μm) with BeO dielectric is 100 mV/decade, comparing to that with Al_2O_3 (112 mV/decade). It is notable that BeO MOSFETs have positive threshold voltage and lower off-state current, which is in agreement with the result from BeO MOSCAPs as shown in Figure 3-4. Since BeO is able to form better interface with InGaAs in terms of low roughness and less interface trap density, BeO MOSFETs also show better performance characteristics in terms of low resistance in linear region presenting in Figure 3-6.

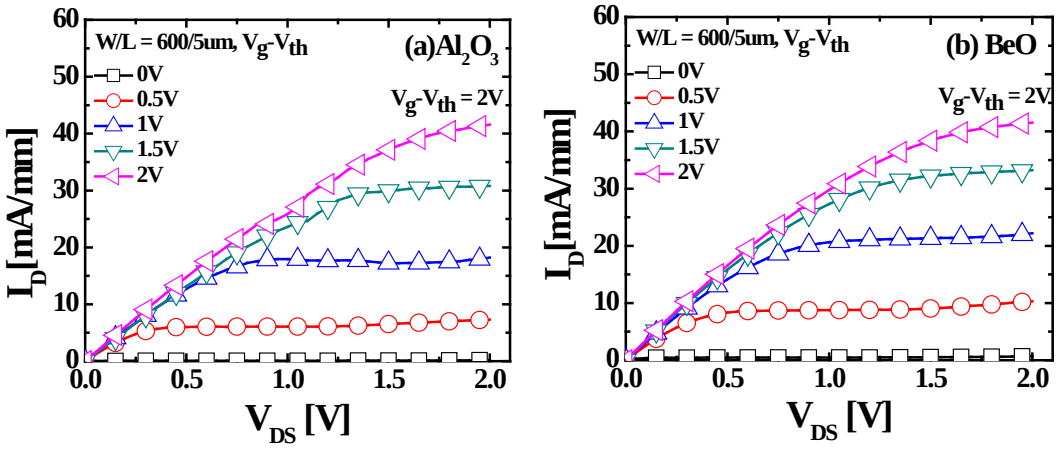


Figure 3-6: Output characteristic of InGaAs MOSFETs with (a) Al_2O_3 and (b) BeO gate dielectric

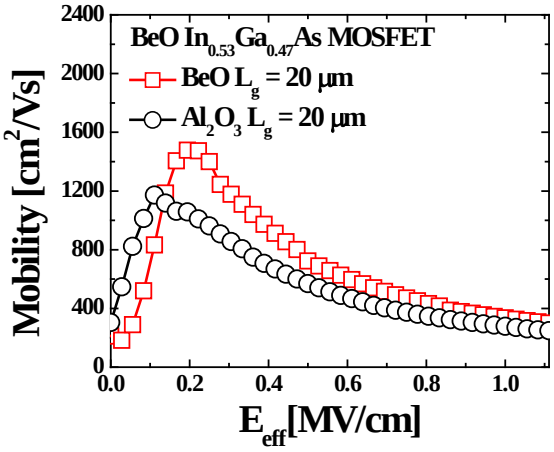


Figure 3-7: Effective mobility comparison between BeO and Al_2O_3 MOSFETs

Figure 3-7 illustrates the effective electron mobility using split C-V method. The peak mobility of BeO MOSFET is 1477 cm^2/Vs, and that of Al2O3 MOSFET is 1172 cm^2/Vs. BeO gate stack MOSFET performs 26% higher effective mobility.

In summary, InGaAs surface channel n-MOSFETs with ALD BeO dielectric is fabricated and characterized. By comparing with Al_2O_3 gate stack in MOSCAPs and MOSFETs, BeO gate dielectric shows better interface properties in low roughness, less interface trap density, and low gate leakage current in MOSCAPs. For device performance, BeO MOSFETs indicates low off-state current, positive shifted threshold voltage, low resistance in linear region, and higher effective mobility.

Chapter 4: Introduction of Quantum Well (QW) III-V MOSFETs

In device characterization point of view, InGaAs Quantum Well (QW) structure is a promising for device performance, because it is still hard to achieve intrinsic carrier mobility in III-V MOSFETs. Quantum well structure indicates that the channel layer is located in a distance from top surface where touches with high-κ gate oxide. By inserting an InP buffer layer between the high-κ and channel layer, it prevents the channel layer from creating notorious interface with high-κ dielectric layer. In order to fully benefit from its intrinsic electrical properties in aggressively scaled III-V devices, it is imperative to adopt a quantum-well QW) design to mitigate the short-channel-effects (SCEs), similar to ultra-thin-body architecture (UTB) in Si MOSFETs. Especially, the movement of electrons under the gate, easily turns into ballistic transport in a quantum well structure [45].[3]

4.1 BeO IPL for Quantum well (QW) InGaAs MOSFETs

Although InP buffer layer is employed to protect the channel layer, InP, itself is also one of the III-V materials. It has the possibility to form poor interface property with high-κ gate dielectric layer. Therefore, BeO is considered as an IPL, because it has

[3]This chapter is based on reference [44]: **D. Koh**, H. M. Kwon, T.-W. Kim, D.-H. Kim, T. W. Hudnall, C. W. Bielawski, W. Maszara, D. Veksler, D. Gilmer, P. D. Kirsch, and S. K. Banerjee. "**L_g = 100 nm $In_{0.7}Ga_{0.3}As$ Quantum Well MOSFETs with Atomic Layer Deposited Beryllium Oxide as interfacial layer**", *Appl. Phy. Lett.***104**, 163502 (2014)
D.Koh designed experiments. D.Koh carried out fabrication BeO/HfO_2 IPL MOSFETs and electrical measurement.

including high melting point,[40, 68, 69] large dissociation energy,[70] high thermodynamic chemical stability,[71, 72] high thermal conductivity,[73-75] high bulk modulus,[76-79] and high electrical resistivity,[80, 81] in addition to a large band gap of 10–10.6 eV (Refs. [60, 82, 83]), and low interfacial trap density with III-V channel. $In_{0.53}Ga_{0.47}As$ MOS capacitors with ALD BeO as gate dielectric and IPL are fabricated to evaluate interface improvement. Electrical characteristics of nanometer-scale $In_{0.7}Ga_{0.3}As$ QW MOSFETs with ALD BeO IPL are observed.

4.2 Device Process of QW InGaAs MOSFETs

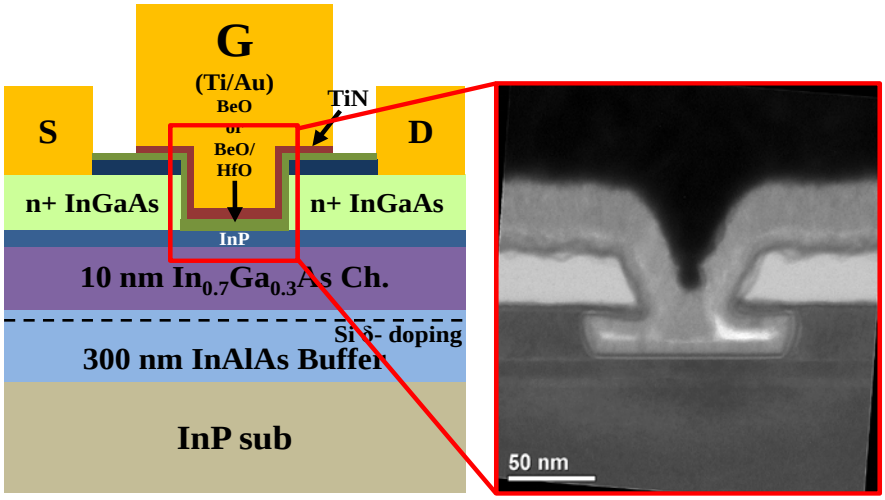


Figure 4-1: Schematic and TEM images of QW MOSFET device structure with BeO or BeO/HfO_2 as gate dielectric or interfacial layer, respectively. Especially, the TEM image indicates 1/1.5 nm BeO/HfO_2 deposited gate stack.

The cross-sectional view of $In_{0.7}Ga_{0.3}As$ QW MOSFET is shown in Figure 4-1. The layer structure is grown by molecular beam epitaxy (MBE) on an InP substrate. A

300 nm $In_{0.52}Al_{0.48}As$ is grown on InP substrate as a backside barrier layer. The quantum well channel consists of a 10 nm thick $In_{0.7}Ga_{0.3}As$ channel and an $In_{0.52}Al_{0.48}As$ barrier layer with inverted Si δ-doping. Subsequently, a 2nm undoped InP barrier and 20nm n+ $In_{0.53}Ga_{0.47}As$ capping layer are sequentially grown. The capping layer decreases the potential barrier through both InP layers in the source and drain access region, and increases the electron concentration in the channel [47].

In order to achieve well-functioning device with this QW wafer structure, the device fabrication process is required to optimize, especially, the process for gate definition, and high-κ/metal gate stack. Therefore, fundamental experiments are conducted for process optimization.

4.3 FUNDAMENTAL EXPERIMENT FOR DEVICE

The quantum well InGaAs MOSFETs consists of raised n^+ InGaAs layer, InP buffer layer, channel InGaAs layer, and InAlAs buffer layer on InP substrate, sequentially. To define gate region, the recess process is considered to be suitable, since the recess process is wet chemical etching which forms less damaged InP surface where is behavior as stopping layer as well as buffer layer for carrier mobility [84]. In order to obtain proper etching rate and good quality etched surface, the gate recess process should be optimized and it is necessity to confirm with electrical measurement.

4.3.1 The Gate recess process

To etch n^+ InGaAs S/D layer, phosphoric acid (H_3PO_4) and peroxide (H_2O_2) are selected since they are popular chemical etchant for InGaAs. Based on general etching information [85], The chemical composition of etchant is started from H_3PO_4:H_2O_2:DI (1:1:32), which is reported to etch InGaAs on InP 120 nm/min. Since n+ InGaAs layer is 40 nm above the InP layer, and slow etching is more controllable, highly diluted H_3PO_4:H_2O_2 in DI (1:1: 80) is used.

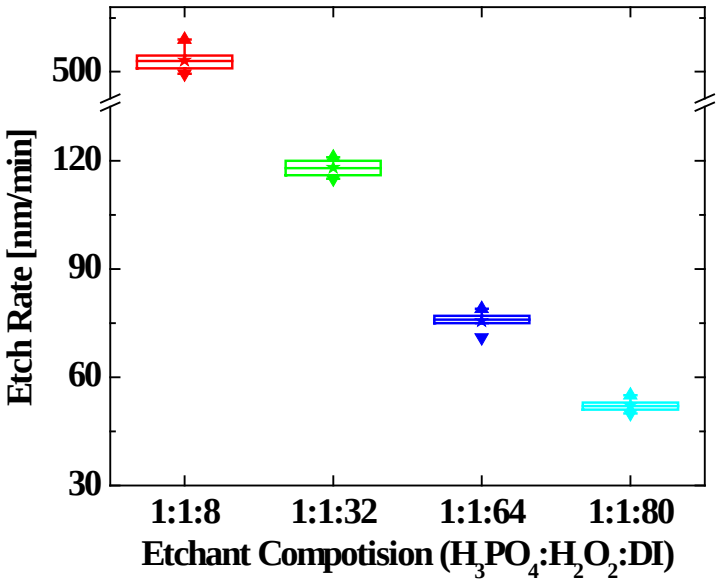


Figure 4-2: The etch rate of InGaAs in based H_3PO_4: H_2O_2 etchant, which is carried out in room temperature for 1 min.

Figure 4-2 indicates that InGaAs etch rate in different composition of H_3PO_4: H_2O_2 in DI water. Each etching experiment is conducted 7 times each and Atomic Force Microscopy (AFM) is used to measure etching profile. All measured etching depth

profile is compared with mean etching rate. The highly diluted etchant produces stable and constant result. The etchant composition, 1:1:64 is selected for gate recess.

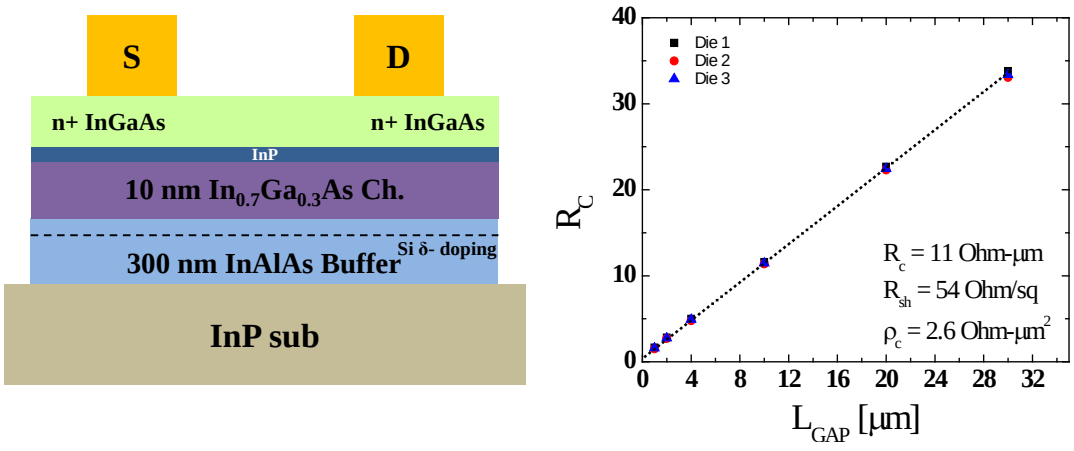


Figure 4-3: The etch rate of InGaAs in based H_3PO_4: H_2O_2 etchant, which is carried out in room temperature for 1 min.

After MESA isolation, ohmic contact is completed with Mo/Ti/Au, and contact resistance and specific contact resistivity is extracted using TLM structure. The contact resistance of 11 Ω-μm is achieved, and the specific contact resistivity is about 2.6 Ω-μm^2, which is comparable result with ref. [86].

For short channel gate definition, n^+ InGaAs is covered by SiO_2 which is deposited as a hard mask. The SiO_2 is grown by 25 nm in PECVE system and etched up to expose n+ InGaAs surface using dry etch process. The SiO_2 etching profile is shown in Figure 4-4. The 25 nm thick SiO_2 is well etched with plasma dry etch process.

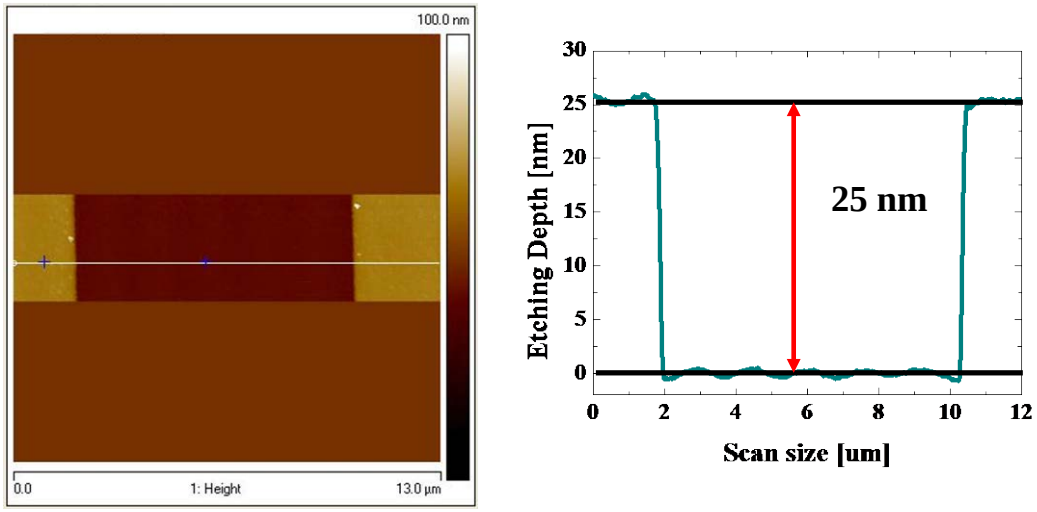


Figure 4-4: The AFM profile after SiO_2 hard mask dry etching, where SiO_2 is grown 25 nm using PECVD.

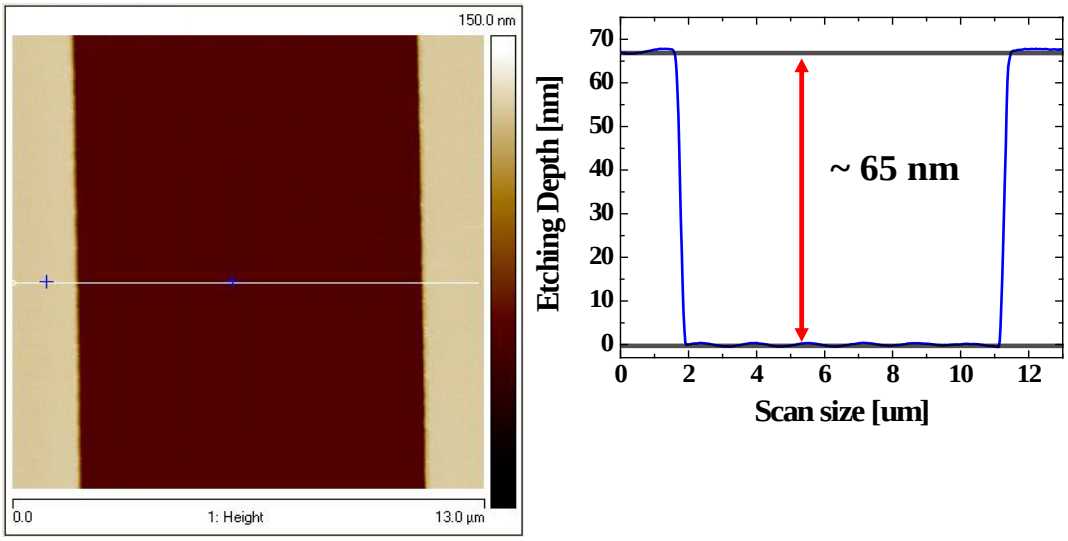


Figure 4-5: The AFM profile of etched surface where includes SiO_2 as hard mask above the n^+ InGaAs capping layer.

Based on InGaAs etching rate, 40nm thick n^+ InGaAs S/D layer is etched away for 30 sec. Figure 4-5 presents the gate recess profile after 30 sec etching. The etching profile

in Figure 4-5 includes etching SiO_2, hard mask which is shown Figure 4-4. Since gate recess means that highly doped InGaAs layer is electrically shorted, the current measurement is another way to investigate the gate recess process. After the InGaAs etching, electrical measure is carried out to observe current lowering. In Figure 4-6, very low current through shorted S/D layer is obtained. According to recess current measurement, the level of resistance in the shorted S/D region is close to insulator range where is around ~10^6 Ω order.

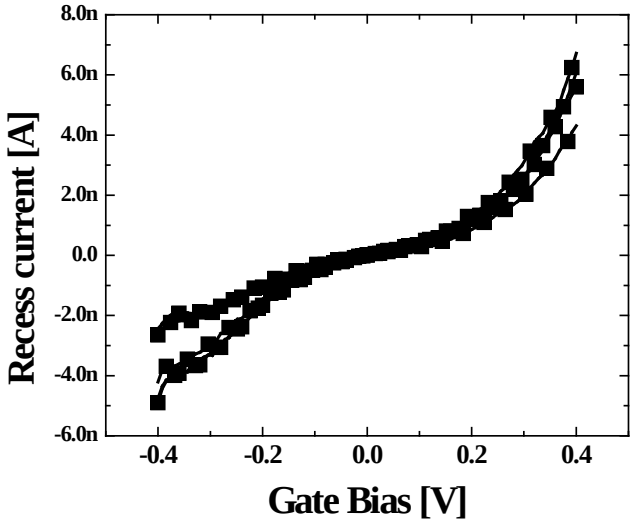


Figure 4-6: The recess current after InGaAs etching in S/D region.

The H_3PO_4:H_2O_2 based etching rate is implement by changing composition and measuring depth profile using AFM, and constant etching rate is accomplished in lower concentration of H_3PO_4:H_2O_2 etchant. The recess current measurement is useful to monitor and confirm the gate recess accomplishment.

4.3.2 Electrical analysis of BeO QW InGaAs MOS capacitance

Figure 4-6 presents comparison of capacitance-voltage (C-V) and gate leakage current density characteristics of $In_{0.53}Ga_{0.47}As$ MOS capacitors with ALD Al_2O_3 and BeO. C-V Hysteresis in BeO MOSCAPs is slightly larger than that in Al_2O_3 MOSCAPs, possibly due to the presence of carbon impurities in the beryllium precursor used for ALD, as reported in ref. [40].

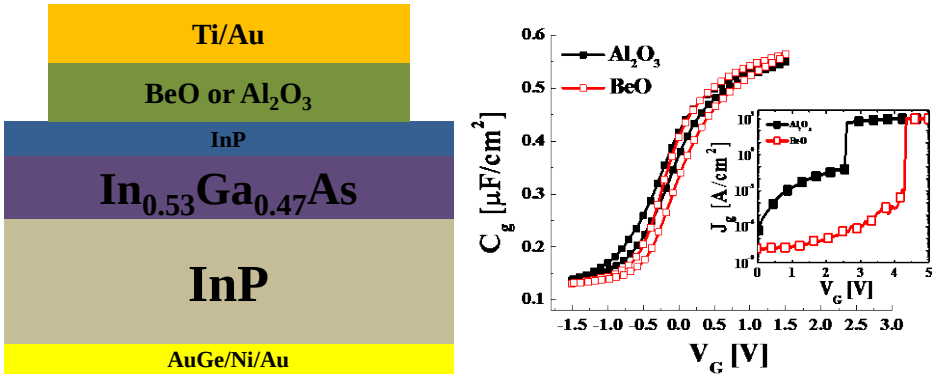


Figure 4-6: Comparison of C-V characteristics and gate leakage current (inset). 10 nm Al_2O_3 and BeO is grown using the same ALD system at 250℃. The MOSCAP structure consists of n+ InP, 20 nm of $In_{0.53}Ga_{0.47}As$, and 2 nm of undoped InP layer.

However, the MOSCAP with BeO exhibits better modulation behavior of channel carriers than one with Al_2O_3. As gate bias swipes, the capacitance curve of BeO transits shows shaper than that of Al_2O_3 due to interface trap density difference. The interface traps created by high-κ deposition usually affect C-V characteristics, resulting in that C-V curves is distort. More importantly, a remarkable reduction in the gate leakage current density (~ 10^{-7} A/cm^2) is observed at forward bias region, as shown in Figure 4-6

(inset). This is due to not only large energy band-gap of BeO [87] , but also higher conduction band offset between BeO and $In_{0.53}Ga_{0.47}As$ channel material than one with Al_2O_3 [88, 89].

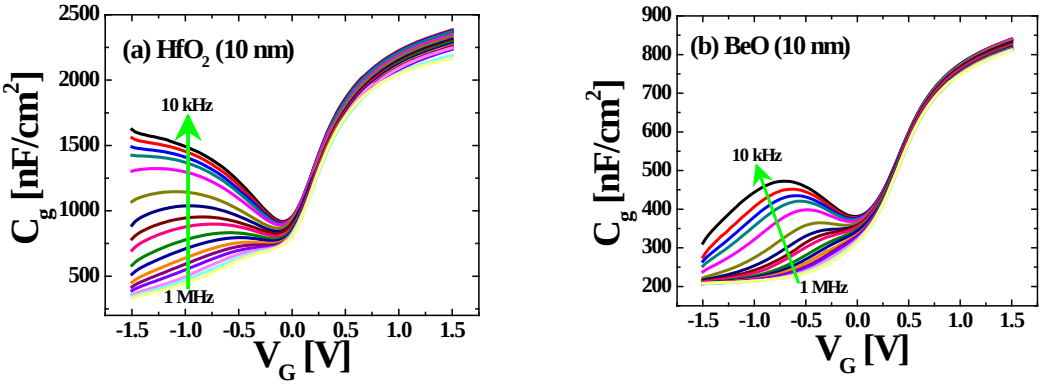


Figure 4-7: The comparison of frequency dispersion characteristic between HfO_2 and BeO MOSCAP

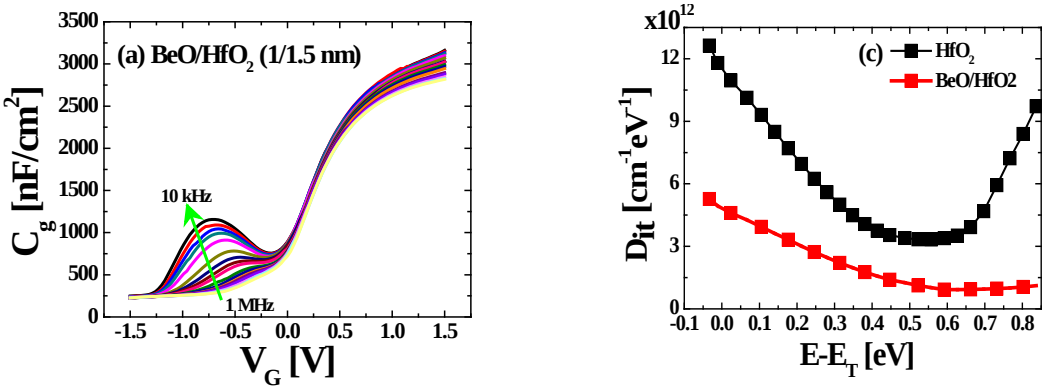


Figure 4-8: Frequency dispersion for InGaAs MOSCAP with 1nm BeO/ 1.5nm HfO_2 thickness gate dielectric.

Figure 4-7 compare C-V frequency dispersion characteristics for $In_{0.7}Ga_{0.3}As$ QW MOS capacitor with single dielectric, (a) HfO_2 or (b) BeO, which are deposited 10 nm each. The device with 10 nm HfO_2 in Figure 4-7 (a) shows worse frequency

dispersion than one with 10 nm BeO in Figure 4-7 (b), since HfO_2 film contains large defect sites inside film and forms poor interface with InGaAs. When BeO interface passivation layer is inserted between channel and high-κ, the large stretch-out shown at HfO_2 single MOSCAP is alleviated in Figure 4-8 (a), while BeO/HfO_2 bi-layer dielectric MOSCAPs is maintaining similar interfacial trap density as single BeO and improving EOT scalability, as shown in Figure 4-8 (a). D_{it} distribution in Figure 4-8 (b) is extracted by conductance method with split C-V. The devices with BeO and BeO/HfO_2 yields a fairly low value of $D_{it} = 2\times10^{12}$/ eV·cm and 1×10^{12}/ eV·cm at mid-gap, whereas one with HfO_2 yields larger frequency dispersion and higher value of D_{it}. This indicates that BeO acts as a good interfacial-layer for $In_{0.53}Ga_{0.47}As$ channel material.

4.3.3 Device analysis of InGaAs QW MOSFETs with BeO IPL

With those fundamental experiment results, BeO interface passivated InGaAs QW MOSFETs is fabricated and characterized. Firstly, electrical isolation of the active region is carried out using an H_3PO_4 based wet etchant. Source and drain ohmic contacts to the n^+ InGaAs are made using e-beam evaporation and subsequent lift-off of Mo/Ti/Au metal stack. PECVD-grown SiO_2 layer is used to form a hard mask and the gate pattern is defined with ZEP-520A by JEOL 6000FX e-beam lithography. Then, CF_4–based plasma dry etching is used to transfer the defined pattern onto the n^+ InGaAs capping layer. According to etching experiment result with H_3PO_4:H_2O_2 based solution, the n^+ InGaAs capping layer is etched for 30 sec to expose the InP layer. ALD BeO/HfO_2 is deposited at

250 °C 1/1.5 nm for IL and 5 nm BeO is grown for gate dielectric layer in Cambridge Nano ALD system. Subsequently, TiN metal gate is deposited with ALD system in an *in situ* manner. Finally, Ti/Au gate metal pad is deposited by e-beam evaporation.

Figure 4-9 shows the electrical characteristics of $In_{0.7}Ga_{0.3}As$ QW MOSFET with BeO/HfO_2 composite gate dielectric layers. Figure 4-9 displays subthreshold and transconductance (g_m) behavior of $In_{0.7}Ga_{0.3}As$ QW MOSFETs with three different values of gate length (L_g = 200 nm, 150 nm and 100 nm).

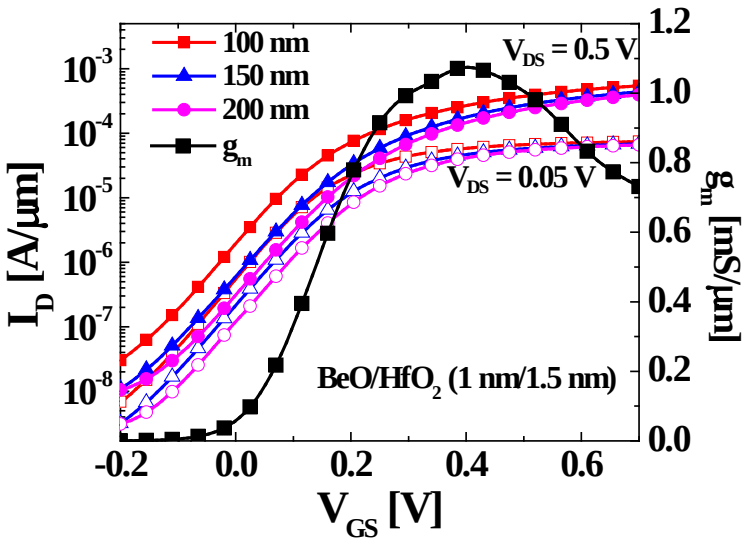


Figure 4-9: Subthreshold characteristic with different channel length and transconductance (gm) of L_g = 100 nm of QW MOSFETs with BeO/HfO_2 (1/1.5 nm) gate stack.

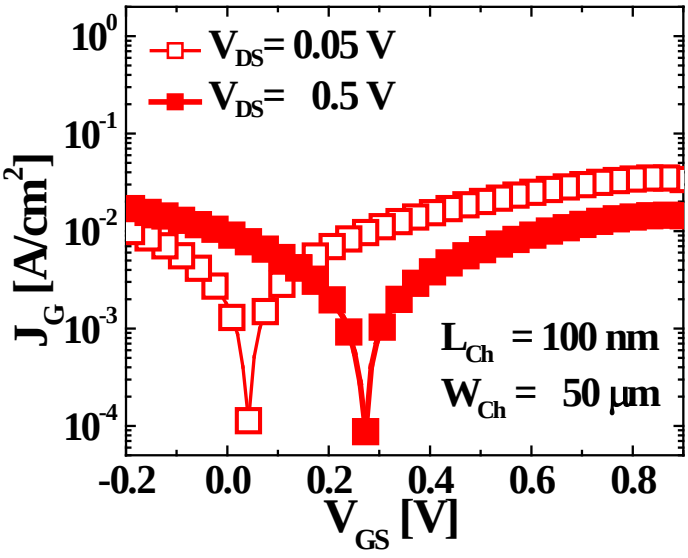


Figure 4-10: The gate leakage current density of L_g = 100 nm QW MOSFETs with BeO/HfO_2 (1/1.5 nm) device at applied drain voltage 0.05 V and 0.5 V.

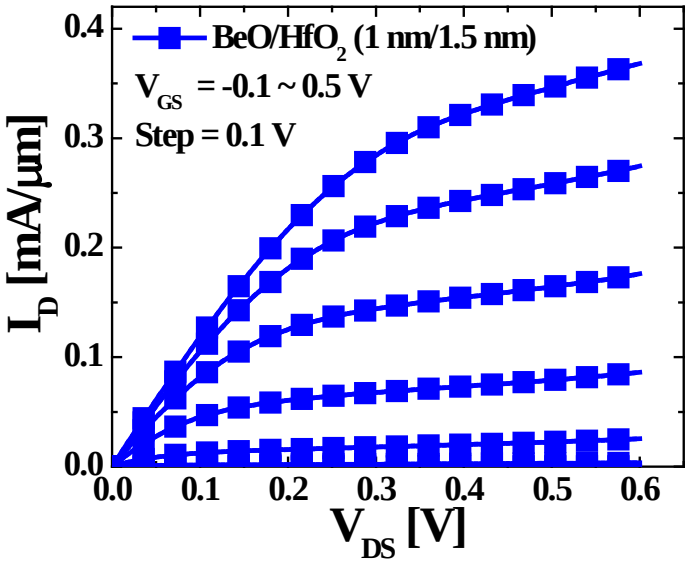


Figure 4-11: The output characteristic of L_g = 100 nm QW MOSFET with BeO/HfO_2 (1/1.5 nm) gate dielectric.

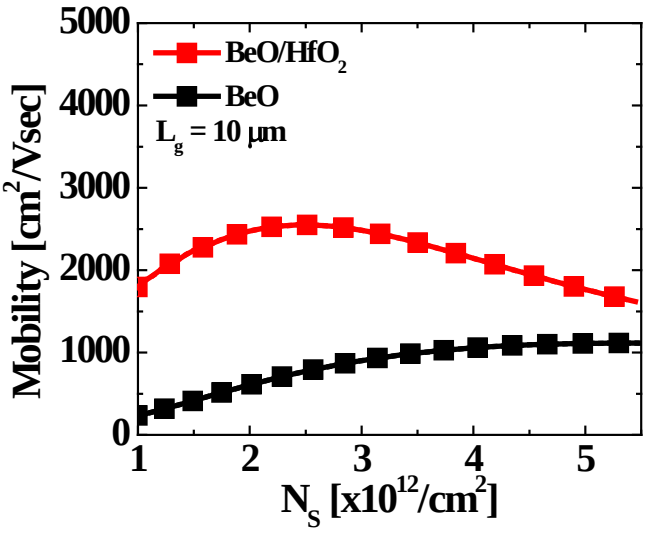


Figure 4-12: The mobility enhancement of L_g = 10 μm BeO/HfO_2 QW MOSFETs

The maximum transconductance (g_{m_max}) for the 100 nm gate length QW MOSFET is 1.1 mS/μm at V_{DS} = 0.5 V. Low interface trap density in Figure 4-8 (b) leads to excellent subthreshold-swing (SS) of 100 mV/dec at L_g = 100 nm. A fairly low value of gate leakage current density is observed as shown in Figure 4-10, which is around ~ 10^{-2} A/cm^2 at a drain bias V_{DS}= 0.5 V, arising from the fact that BeO is very strong oxygen diffusion barrier and a dense oxide layer. Output characteristics of L_g = 100 nm QW MOSFET are shown in Figure 4-11. The device with L_g = 100 nm shows excellent current driving capability, such as I_D = 0.35 mA/μm at V_{GS} = 0.6 V. The bilayer oxide stack consists of a 1nm BeO and 1.5 nm HfO_2, yielding an effective oxide thickness (EOT) of 0.93 nm. Excellent effective mobility ($\mu_{e,eff}$) of 2500 cm^2/V·sec is extracted from long-channel QW MOSFETs with the same BeO/HfO_2 composite dielectric layers.

These results highlight that the BeO forms excellent interface with InGaAs channel material.

In summary, we have demonstrated L_g = 100 nm $In_{0.7}Ga_{0.3}As$ QW MOSFET with ALD BeO. The MOSCAPs with BeO exhibit reduced C-V stretch-out and yield fairly low values of $D_{it} \sim 1\times10^{12}$ /eV·cm^2, since BeO is a dense oxide material and serves as a strong oxygen diffusion barrier. Besides, low gate leakage characteristic is a very attractive advantage of BeO. L_g = 100 nm $In_{0.7}Ga_{0.3}As$ QW MOSFET with BeO/HfO_2 composite dielectric layers represent promising results at V_{DS} = 0.5 V, such as $g_{m,max}$ = 1.1 mS/μm, SS = 100 mV/dec, DIBL = 100 mV/V, and $\mu_{e,eff}$ = 2500 cm^2/V·sec, with EOT = 0.93 nm.

Chapter 5: Process development for interface improvement

While the InGaAs QW MOSFETs is fabricated and studied, it is found that the channel interface property is dramatically degraded either within process system, or of course atmosphere.

Basically, III-V native oxide is known for chemically unstable, and these notorious native oxides can contain high interface trap density (D_{it}). Therefore, it affects gate modulation and ON-state current. The interface trap density (D_{it}), generally, leads to Fermi level pinning (FLP), which causes improper gate modulation [90-92]. To passivate III-V surface, various surface treatments for III-V channel surface are developed, such as using sulfur, HBr, diluted HCl, or HF, and Si, Ge, Si_xN_y, Ge_xN_y or Al_2O_3 interfacial passivation layers [24, 93, 94]. These treatment methods have been reported promising improvement of device performance. Mainly these additional processes are aimed to mitigate Fermi level pinning effect. However, most of them are implemented *ex-situ* experimental condition, which means that the surface of III-V materials can be exposed atmosphere, resulting to create unintentional native oxide.

Thus, *In-situ* Ar ion plasma treatment is considered as surface treatment before high-κ deposition.[4] The influence of these processes are analyzed with MOSCAP characteristics, such as C-V hysteresis, multi-frequency C-V dispersion, and interface trap density, and so on [48].

[4]This chapter is based on reference [48]: **D. Koh**, S.-H. Shin , J.-H. Ahn , S. Sonde , H.-M. kwon , T. Orzali , T.-W. Kim , D.-H. Kim , S. K. Banerjee. "**Damage free Ar ion plasma surface treatment on $In_{0.53}Ga_{0.47}As$-on-Silicon MOS device**", *Appl. Phys. Lett.* 107, 183509 (2015)
D.Koh designed this experiment, optimized Ar plasma power and treatment time. D.Koh conducted fabrication and analysis interface properties.

5.1 In-situ Ar Plasma Treatment for InGaAs surface

An Ar ion plasma surface treatment is evaluated for surface cleaning and curing using Ar ion bombardment on the InGaAs surface before high-κ deposition. This surface treatment was carried out in-situ and at low plasma power to avoid surface damage. The effect of plasma Ar ion treatment is studied by analyzing the XPS spectra data collected ex-situ for surface chemical specimen change and by comparing the characteristics of MOSCAPs, interface trap density (D_{it}), and threshold voltage (V_{th}) degradation.

5.2 Argon Ion Plasma Treatment Process

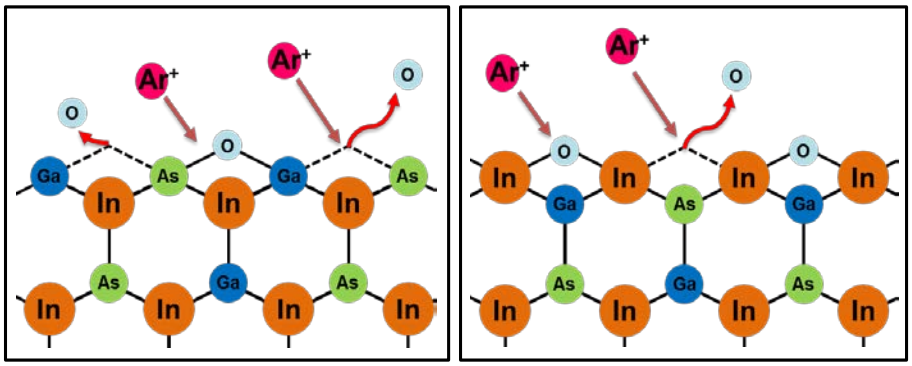


Figure 5-1: The conceptual diagram of Ar ion plasma treatment on $In_{0.53}Ga_{0.47}As$. Note that $In_{0.53}Ga_{0.47}As$ on Silicon MOS capacitor with Al_2O_3/HfO_2 bi-layer high-κ dielectric layer is fabricated in-situ

The epitaxial $In_{0.53}Ga_{0.47}As$ layer is grown on a Si (100) substrate in the MOCVD reactor. The concept of Ar ion plasma treatment is presented in Figure 5-1. The MOS

capacitor is fabricated with Al_2O_3/HfO_2 (6/30 cycle) bi-layer stacks in order to represent a functionally scaled down MOS device. Initial chemical cleaning is carried out on both control and experimental wafers. They are soaked in diluted hydrochloric acid (HCl) with deionized water (DI) for 1 min. Then, an Ar ion treatment is applied at 20 W plasma power within the Oxford Fiji plasma-enhanced atomic layer deposition (ALD) system, and bi-layer high-κ dielectric and titanium nitride (TiN) gate metal are deposited in-situ. An overall Ti/Au metal stack is deposited on the backside (in the e-beam evaporation system) and provides the backside contact. Then, the front-side gate pad is patterned and lifted-off using photolithography and metallized with Ti/Au. XPS is then used to observe any change in the surface chemical composition both with and without Ar ion plasma treatment on samples without metallization. For XPS sample preparation, 8 cycles of TiN are deposited to passivate the surface right after the Ar ion plasma treatment.

5.2 RESULT OF AR ION PLASMA TREATMENT WITH MOSCAPS

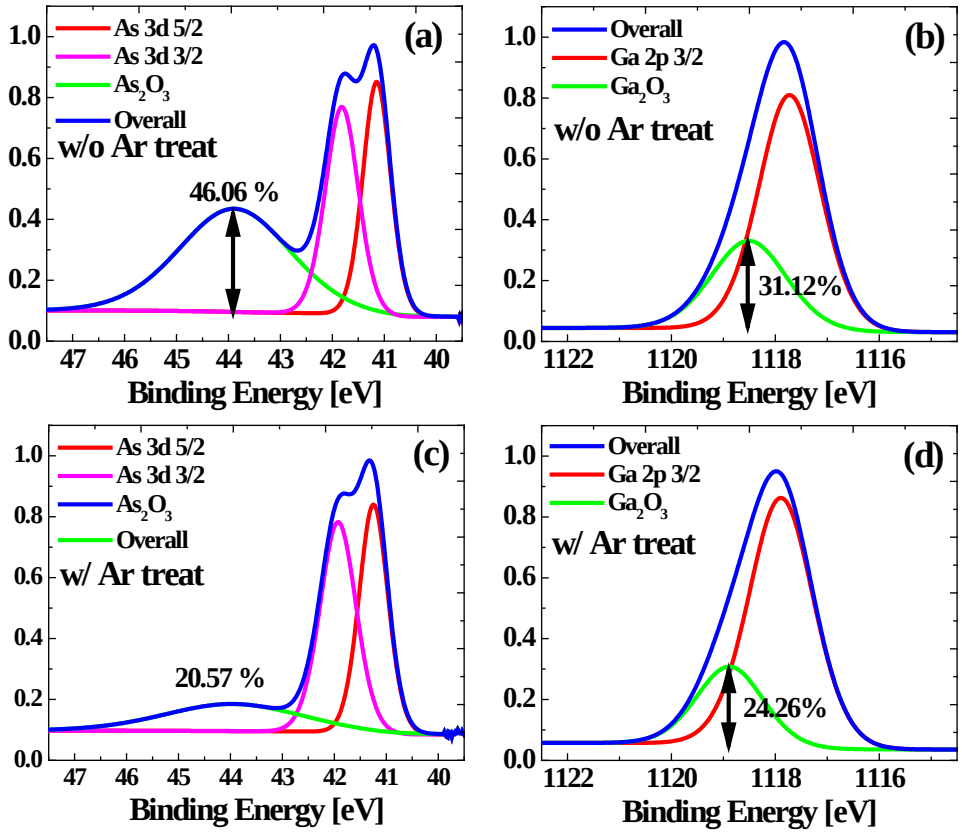


Figure 5-2: The XPS spectra with and without Ar ion plasma treatment. (a) and (b) present non-treatment As and Ga spectra, respectively. (c) and (d) indicate Ar ion-treated As and Ga spectra.

In order to avoid exposing the treated surfaces to oxygen, the samples were covered in-situ with a TiN passivation layer rather than an Al_2O_3/HfO_2 stack. The thickness of the TiN is around 1 nm in order to facilitate observation by X-ray penetration. Figure 5-2 shows the relevant XPS spectra for non-treated Ar ion plasma treated surfaces in Figure 5-2 (a) and (b) as well as treated surfaces in Figure 5-2 (c) and (d).

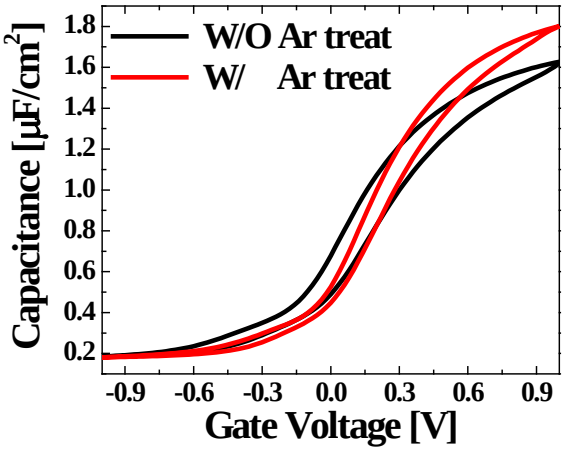


Figure 5-3: The comparison of the C-V hysteresis with and without surface treatment measured in 1 MHz.

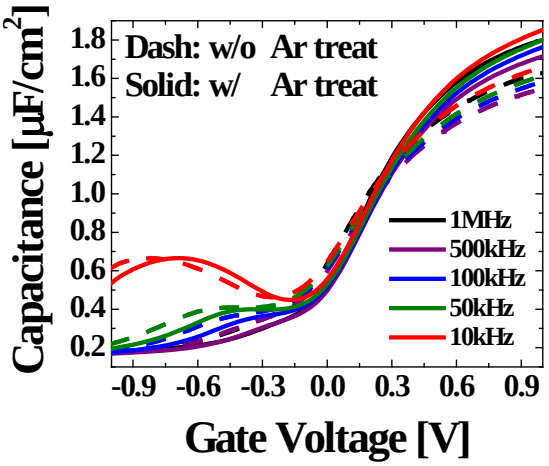


Figure 5-4: The comparison of frequency dispersion characteristic between with and without surface treatment. (Dash line: without Ar treatment, Solid line: with Ar treatment)

The surface native oxide of $In_{0.53}Ga_{0.47}As$ can be prominently seen in Figure 5-2 (a) and (b) for non-treated samples. AsO_x and GaO_x concentrations, as evaluated by normalized XPS spectra, are reduced by 25.49 % and 6.86 % respectively after Ar ion

plasma treatment. This indicates that Ar ion bombardment can easily remove AsO_x and GaO_x bonding. Since it is reposted, AsO_x is the most unstable in a III-V sub-oxide and has weak bonding energy, the dramatic reduction of AsO_x is observed [95].

Figure 5-3 and Figure 5-4 present the C-V characteristics of $In_{0.53}Ga_{0.47}As$ MOSCAPs with and without Ar ion plasma treatment. Because plasma-enhanced Ar ion bombardment can remove native oxide on $In_{0.53}Ga_{0.47}As$ surfaces without damage, Ar ion plasma treated MOCAPs had a higher accumulation capacitance (C_{acc}). The increase of accumulation capacitance is evidence of the sub-oxide reduction on $In_{0.53}Ga_{0.47}As$ surface, which is agreement with Figure 5-2. Also, the capacitance transition of Ar ion treated MOSCAPs is steeper than that of non-treated MOSCAPs shown in Figure 5-3, which is in agreement with Ref. [96]. Because of the low power (20 W) and remote plasma, less damage occurs to the $In_{0.53}Ga_{0.47}As$ surface, resulting in less charging effect which leads to similar gate leakage property [97, 98].

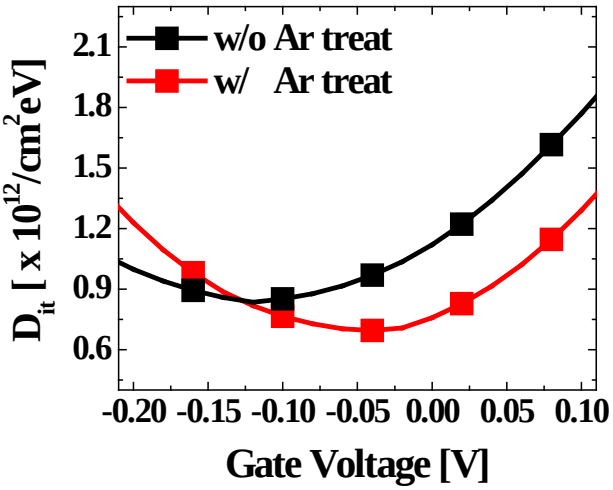


Figure 5-5: The comparison of the interface trap density between with and without Ar treatment. The interface trap density is extracted by conductance method.

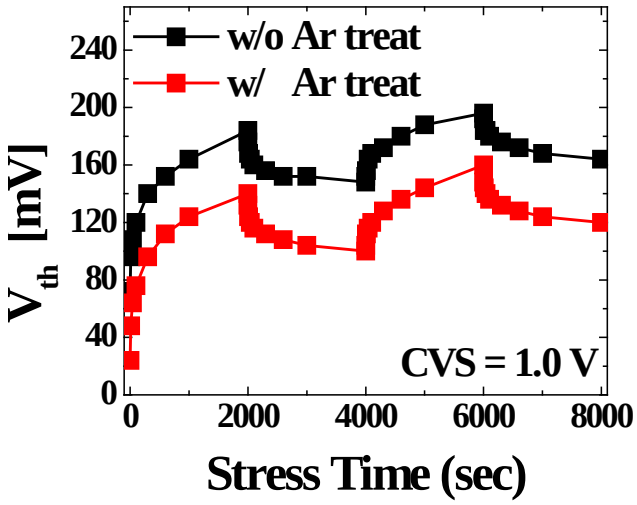


Figure 5-6: The comparison of constant voltage stress induced threshold voltage shift between with and without Ar treatment.

The MOSCAPs with Ar ion treatment in Figure 5-3 also presents a flat-band voltage shift, indicating less interface charge (also known as a positive (+) charge) [99]. The multiple frequency C-V dispersion in Figure 5-4 reveals that the MOSCAPs with treatment have less stretch-out, meaning less interfaces trap density (D_{it}). D_{it} is extracted using a conductance method at near the mid-gap shown in Figure 5-5. The D_{it} without Ar ion plasma treatment is approximately $9\times10^{11}/cm^2$ eV, which is a very low value [8, 14, 18]; this means the $In_{0.53}Ga_{0.47}As$ layer is well grown on the Si substrate. However, when enhanced Ar ion is exposed on the $In_{0.53}Ga_{0.47}As$ surface, the interface trap density (D_{it}) decreases to $6\times10^{11}/cm^2$ eV. Plasma Ar ion bombardment not only removes native oxide, but also induces a better interface between the high-κ dielectric layer and the $In_{0.53}Ga_{0.47}As$ As surface. Hence, the reduction of the multiple frequency C-V dispersion

in MOSCAP with Ar ion treatment can be related to D_{it} as shown in in Figure 5-5. In addition, threshold voltage (V_{th}) degradation is evaluated to explain the improvement in the interface property. The electron trapping behavior is observed under the effective stress field [$E_{eff} = (V_g - V_{th} / EOT]$, where a 1.0 V bias is applied as the constant voltage stress (CVS) and the relaxation occurs by applying 0 V bias. The electrons from the $In_{0.53}Ga_{0.47}As$ channel are trapped into a defect site near the interfacial region at positive stress voltage and de-trapped at opposite polarity. This result is another piece of evidence supporting the theory that the Ar ion plasma process improves the $In_{0.53}Ga_{0.47}As$ interface. Figure 5-6 indicates mitigation of V_{th} degradation is obtained from Ar ion plasma treated MOSCAPs. Ar treatment leads to a smaller defect site near the interface layer. In other words, this treatment can achieve surface reconstruction, with a reduced defect site at the $In_{0.53}Ga_{0.47}As$ surface, thus threshold voltage shift (V_{th}) is suppressed as shown in Figure 5-6 [100-102].

The damage free in-situ Ar ion plasma treatment is developed and analyzed using $In_{0.53}Ga_{0.47}As$ MOSCAPs. The concept of this treatment is to use plasma enhanced Ar ion bombardment onto the surface, but is generated at a distance from the substrate to decrease plasma damage. The Ar ion treatment can remove native oxide, which is explained in the XPS spectra by indicating the reduction of AsO_x, and GaO_x concentration. More evidence of its impact was revealed by the C-V characteristics of the $In_{0.53}Ga_{0.47}As$ MOSCAPs. Higher accumulation capacitance (C_{acc}), less frequency dispersion, and low interface trap density (D_{it}) supported the influence of Ar ion treatment. Furthermore, there was not only an improvement of the interface property, but

also a reduction of defect sites inside the high-κ. The observation of threshold voltage (V_{th}) degradation indicated well-grown high-κ on the $In_{0.53}Ga_{0.47}As$ surface. The result provides a compatible surface treatment and suggests a treatment useful for non-planar structures that causes no damage.

Chapter 6: Summary and Future work

6.1 SUMMARY

As an alternative to CMOS devices, III-V materials have been attractive. Especially, higher indium (In) content III-V alloy channel offers outstanding carrier transport characteristics, resulting in higher drive currents at a lower supply voltage. However, these III-V group materials have several big challenges in channel surface characteristics that need to be overcome. In this dissertation, surface improvement of InGaAs is the main focus for enhancement of device performance. Research about high-κ material for channel, surface treatment, and post high-κ annealing is conducted.

First, the high-κ application has been studied to utilize interface passivation layer for InGaAs channel device. Liquid source ALD BeO has been investigated for its chemical properties using AES, XPS, RBS, and NRA analysis. Based on these combined measurements, liquid source ALD BeO revealed amorphous film, low hydrogen (H) contents, and nearly stoichiometric (Be/O ≅ 1.1 ± 0.05) film quality. The slightly lower band-gap of 8.0 ± 0.14 eV was exhibited due to hydrogen (H) and carbon (C) contamination. The nanoindentation measurement showed that ALD BeO has a high Young's modulus and hardness of 330 ± 30 and 33 ± 5 GPa, respectively.

Second, ALD BeO characteristics which were measured from several measurements showed potential for use as gate oxide or an interface passivation layer on InGaAs channel FETs. Based on our results, ALD BeO was applied to surface channel MOSFETs as a gate oxide. By comparing with Al_2O_3 surface channel MOSFETs, ALD

BeO performed better subthreshold swing, low gate leakage current, and higher effective mobility. As a interface passivation layer, ALD BeO was used to QW InGaAs MOSFETs and the device performance was characterized. Foremost, the interface properties were investigated using InGaAs MOS capacitor with and without BeO IPL incorporated with HfO_2. The low interface trap density (D_{it}) in BeO IPL MOSCAPs was obtained as indicated by less hysteresis and frequency dispersion in the CV measurements. Furthermore, the low gate leakage current characteristic was observed in BeO/HfO_2 InGaAs MOSCAPs. For BeO IPL application in MOSFETs, quantum well InGaAs structure was employed to study the impact of BeO IPL by comparing with non-IPL device. The InGaAs channel contained 70% indium since the higher mobility can be produced in the higher In content material. 100 nm gate length MOSFETs were fabricated using gate recess etching technique and gate last process. By inserting BeO IPL between InGaAs and HfO_2, its influence on BeO IPL was proved with an enhanced electrical performance.

Third, the interface improvement process was developed using InGaAs on Si substrate. *In situ* Ar plasma treatment was applied to $In_{0.53}Ga_{0.47}As$ channel before Al_2O_3/HfO_2 deposition. Optimized Ar pre-treatment was developed to remove native oxide on InGaAs surface without plasma damage. It was experimentally revealed that the pre-treatment effectively removed native oxide on the surface, which was ascertained with increased accumulation capacitance, and similar gate leakage level. A low interface trap density (D_{it}) was achieved. It improved high-κ film properties by showing better CVS reliability measurement.

6.2 SUGGESTION FOR FUTURE WORK

As interface improvement process development, deuterium high pressure annealing (D_2 HPA) is considered since in Si device, it is known that D_2 can improve device instability by creating 'hard' interfacial bonding of Si-D. Applying this process to InGaAs substrate, the effect of D_2 HPA is investigating. Basic C-V and conductance measurement is discussed and future studies are suggested.

In current device process, ion implantation for doping of 3-D structures suffers from shadowing effects of the ion beam, because ion implantation is a line-of-sight process. Non-uniform doping leads to the S/D junction leakage current, which is considered as a source of power consumption in CMOS technology [103]. To overcome these limitations, solid phase doping method are introduced in ref [51]. With this doping method, contact resistance is investigated using a TLM structure. Non-planar device architecture with solid phase doping is discussed.

6.2.1 Concept of D_2 High-Pressure Annealing (HPA)

In Si MOSFETs, the deuterium (D_2) high-pressure-annealing (HPA) has been reported to improve hot carrier reliability, lifetime improvement, and electrical performance at the Si-high-κ interface, because D_2 tends to be easily incorporated at the Si/SiO_2 interface during HPA step and Si-D bonds are more resistant to hot-electron excitation than Si-H bonds [49, 50]. In addition, a high pressure system is a lot more efficient in making D_2-rich environment than any other annealing toolsets, which

shortens the overall annealing time. However, passivation effects of the D_2 HPA on the InGaAs MOSCAPs have not yet been reported. Therefore, we study FETs with InGaAs channel material to improve surface characteristics with the $In_{0.53}Ga_{0.47}As$ MOSCAPs on Si substrate with Al_2O_3/HfO_2 (1/3 nm) bilayer gate stack, and to investigate the impact of the D_2 HPA on capacitance-voltage (C-V) characteristics of the InGaAs MOSCAPs with attention to the interfacial state density (D_{it}).

6.2.2 D_2 High-Pressure Annealing for InGaAs surface

A MOSCAP epitaxial wafer was grown by using metal-organic-chemical-vapor-deposition (MOCVD), and consisted of a 300 nm GaAs strain-relaxation buffer (SRB), an 850 nm InP strain relaxation buffer, a 100 nm n-$In_{0.53}Ga_{0.47}As$ with 5×10^{17} cm^{-3}, and an 150 nm n-$In_{0.53}Ga_{0.47}As$ with 1×10^{17} cm^{-3} on an n-type Si substrate, from bottom to top. A device fabrication process began with oxide removal using diluted Hydrochloric Acid (HCl) with deionized water (DI), and 10 cycles of a trimethylaluminum (TMA) pretreatment were used to clean the InGaAs surface prior to the deposition of $Al_2O_3/HfO_2/TiN$ (1/3/5 nm) stacks by using ALD [104]. Subsequently, the D_2 HPA with various process conditions was performed using a “Poongsan GENI-SYS” equipment, such as process temperatures between 300 ℃ and 400 ℃, and pressures between 10 and 20 atm. We also carried out the H_2 HPA process in comparison to our previous work [105]. Finally, we finished the device fabrication by defining a back-side electrode of Ti/Au (10/50 nm), and a front-side electrode of Ti/Au (20/50 nm), respectively.

6.2.3 The impact of D_2 HPA on InGaAs surface

In order to evaluate the impact of the D_2 HPA process and its dependency upon the HPA process conditions, we have measured bidirectional capacitance-voltage (C-V) characteristics of the fabricated MOSCAPs with frequency of 100 kHz, as shown in Figures 6-1. There are three types of the InGaAs MOSCAPs. One is a control MOSCAP without HPA, another with H_2 HPA at 300 °C and 20 atm, and the other with D_2 HPA at 400 °C and 20 atm. It is known that the C-V hysteresis reflects the amount of oxide trap densities and oxide/semiconductor interfacial trap densities [106].

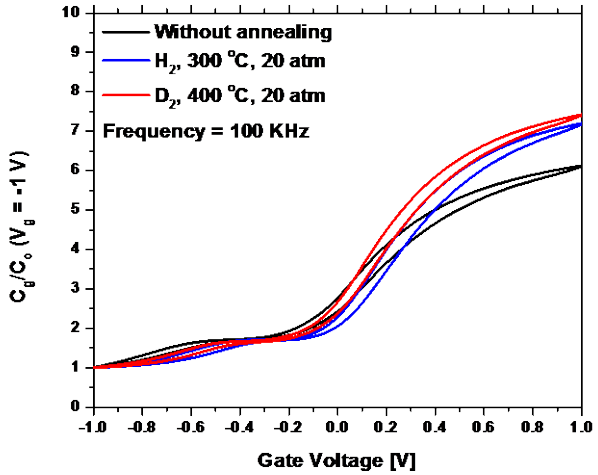
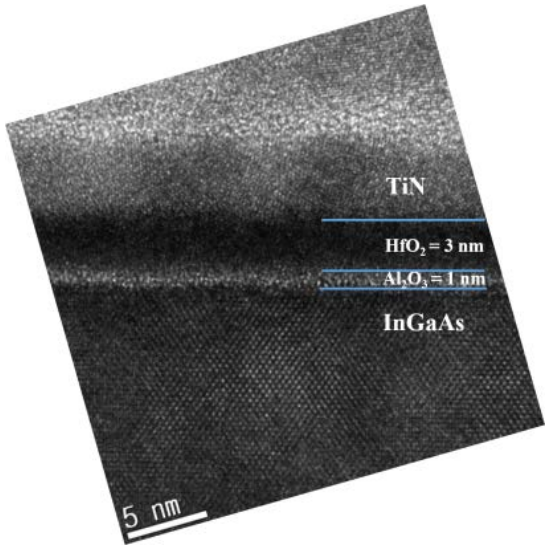


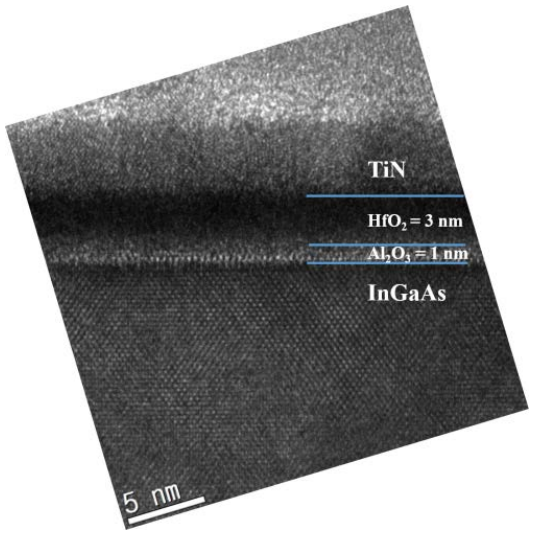
Figure 6-1: The Cg/Co (gate voltage = -1 V) of the bidirectional capacitance-voltage (C-V) characteristics of the $In_{0.53}Ga_{0.47}As$ MOSCAPs on Si without HPA (black), H_2 HPA MOSCAP with 300 °C and 20 atm for 30 min (blue) and D_2 HPA MOSCAP with 400 °C and 20 atm for 30 min (red).

Note that both H_2 and D_2 HPA help to reduce the C-V hysteresis in the InGaAs MOSCAPs. In fact, the D_2 HPA yields more than 26 % reduction of the C-V hysteresis

from the control MOSCAP without HPA. In addition, the MOSCAP with D_2 HPA exhibits the highest value of an accumulation capacitance (C_{acc}), indicating a reduction of the effective-oxide-thickness (EOT) after the D_2 HPA.



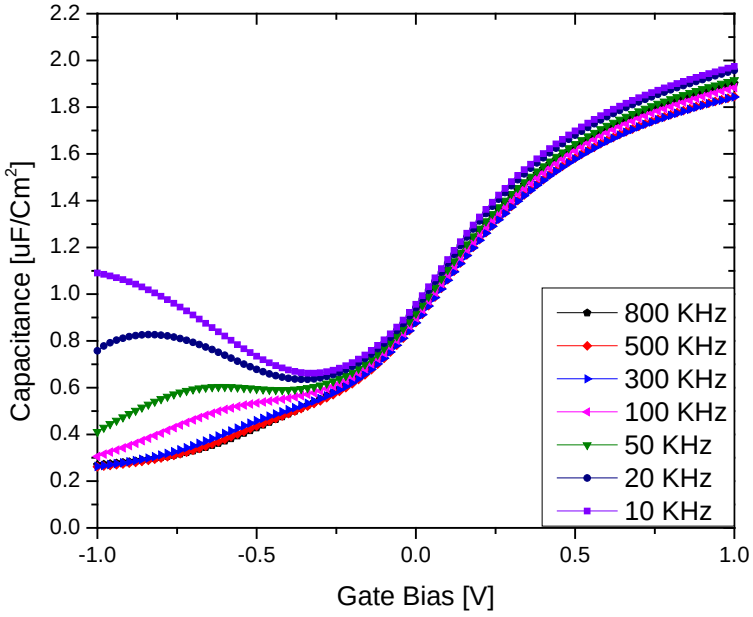
(a)



(b)

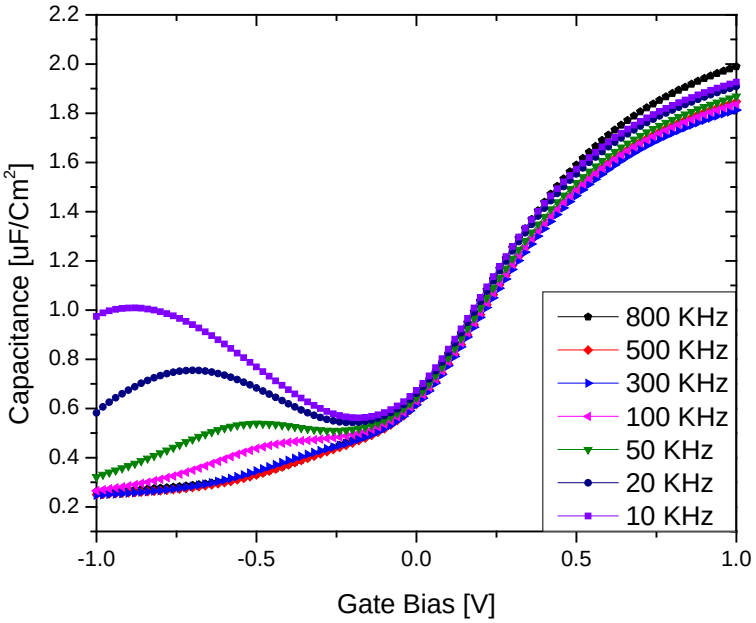
Figure 6-2: Cross sectional TEM images for the $In_{0.53}Ga_{0.47}As$ gate stacks: (a) MOSCAP without HPA and (b) D_2 HPA MOSCAP with 400 °C and 20 atm for 30 min

To examine the physical quality at the interface in the $In_{0.53}Ga_{0.47}As$ MOSCAPs after HPA process step, Figure 6-2 compares cross-sectional TEM images for the $In_{0.53}Ga_{0.47}As$ MOSCAPs before (Figure 6-2 (a)) and after the D_2 HPA (Figure 6-2 (b)). As can be seen, there is no clear evidence for the deterioration of the interface between $In_{0.53}Ga_{0.47}As$ layer and Al_2O_3 high-κ dielectric after the D_2 HPA process. We also observed no deterioration at the interface between $In_{0.53}Ga_{0.47}As$ and Al_2O_3 layer after the H_2 HPA in our previous work [105].

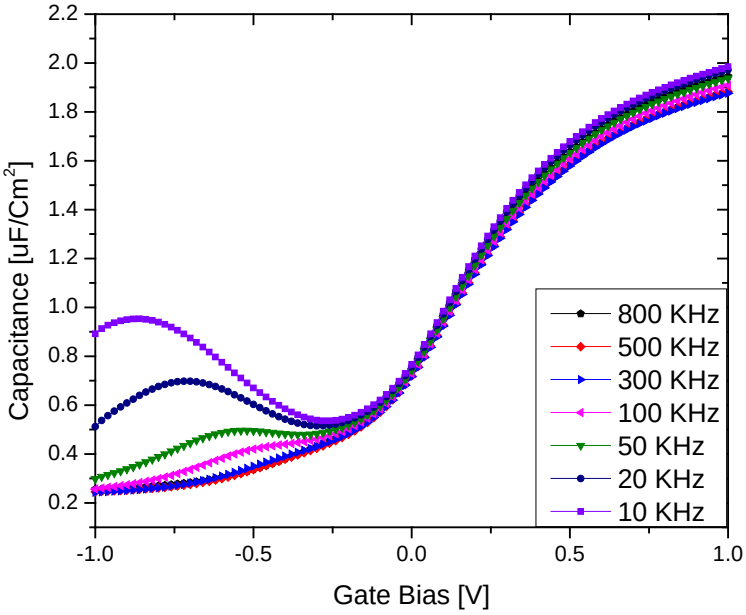


(a)

Figure 6-3



(b)

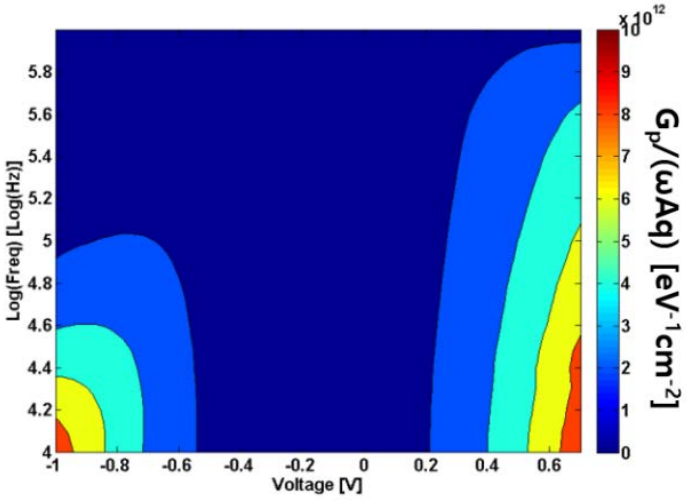


(c)

Figure 6-3: Multi-frequency capacitance-voltage (C-V) characteristics for the $In_{0.53}Ga_{0.47}As$ MOSCAPs on Si: (a) MOSCAP without HPA, (b) H_2 HPA MOSCAP with 300 °C and 20 atm for 30 min, and (c) D_2 HPA MOSCAP with 400 °C and 20 atm for 30 min.

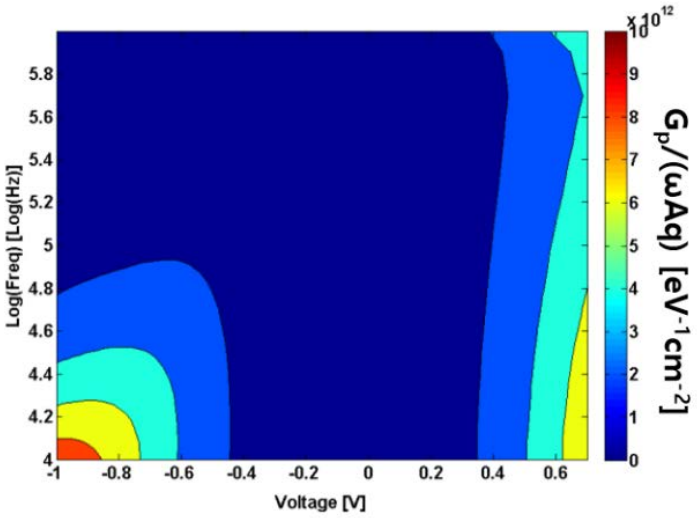
Figure 6-3 shows measured multi-frequency capacitance-voltage (C-V) characteristics for the $In_{0.53}Ga_{0.47}As$ MOSCAPs on Si without annealing, with H_2 HPA at 300 °C and 20 atm, and with D_2 HPA at 400 °C and 20 atm. The MOSCAP with D_2 HPA exhibits the lowest frequency dispersion of 5.5 % among them. The control MOCAP without HPA shows 8.9 % and the MOSCAP with H_2 HPA 6.8 %, indicating that the D_2 HPA process is the most effective in reducing traps inside the high-κ layer [107].

Next, we try to evaluate the quality of the interface between InGaAs channel and Al_2O_3 high-κ dielectric layer. To do so, we have used a conductance method to extract the interface-state density (D_{it}) in three different types of the InGaAs MOSCAPs on Si. First, the normalized conductance values, $G_p/(\omega Aq)$, where G_p is a parallel conductance, ω is an angular frequency, A is a capacitor area, and q is an elemental charge are plotted in Figure 6-4.

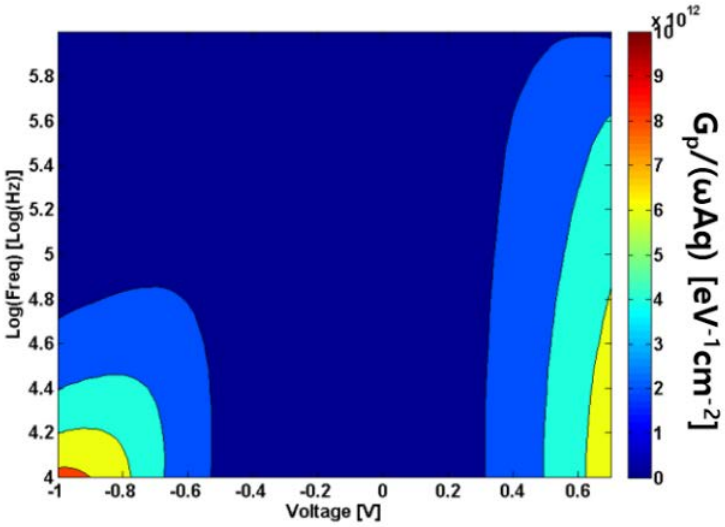


(a)

Figure 6-4



(b)



(c)

Figure 6-4: The normalized conductance value, $G_p/(\omega Aq)$, as a function of gate voltage. (a) $In0._{53}Ga_{0.47}As$ MOSCAP without HPA, (b) H_2 HPA $In0._{53}Ga_{0.47}As$ MOSCAP with 300 °C and 20 atm for 30 min, and (c) D_2 HPA $In0._{53}Ga_{0.47}As$ MOSCAP with 400 °C and 20 atm for 30 min.

From this plot, the maximum position of the conductance peak for three types of the MOSCAPs on Si shifts more than two orders of magnitude in frequency as the gate bias changes between -0.5 V and -1 V. This strongly indicates efficient movements of the Fermi-level (E_F) around the mid-gap in the InGaAs MOSCAPs [17]. Also, the lower value of the normalized conductance peak in the D_2 HPA MOSCAPs reveals the lowest D_{it}, because D_{it} is directly proportional to the normalized conductance peak value by approximately a factor of 2.524.

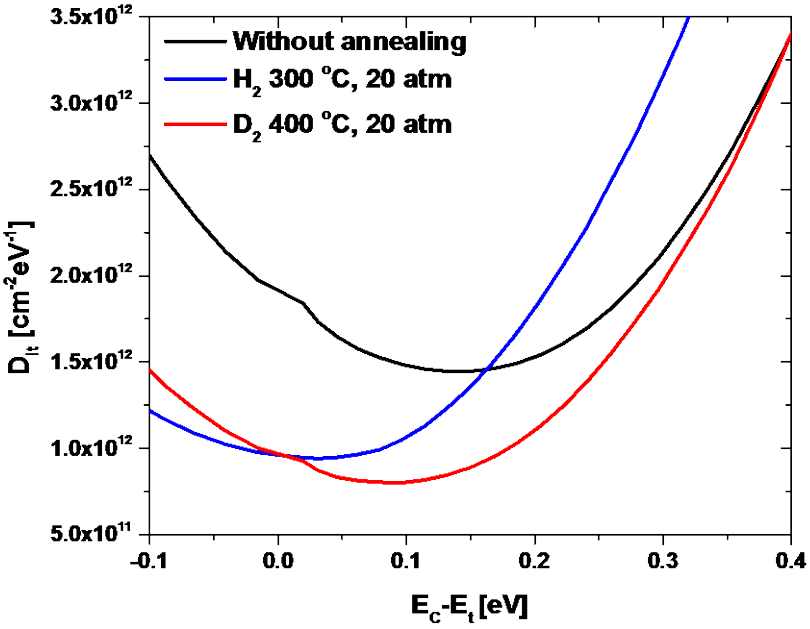


Figure 6-5: Interface trap density (D_{it}) for three types of $In_{0.53}Ga_{0.47}As$ MOSCAPs on Si as a function of energy by using the conductance method: MOSCAP without HPA (black), H_2 HPA MOSCAP with 300 °C and 20 atm for 30 min (blue), and D_2 HPA MOSCAP with 400 °C and 20 atm for 30 min (red).

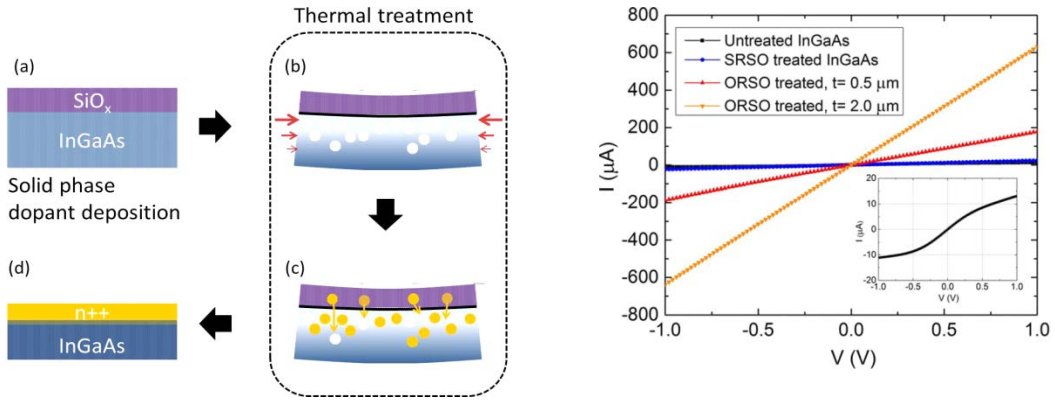
Figure 6-5 summarizes the extracted D_{it} for three types of the $In_{0.53}Ga_{0.47}As$ MOSCAPs on Si as a function of energy using the conductance method aforementioned. Consistent with the improvement of the frequency dispersion of the capacitance in the accumulation regime, the MOSCAP with D_2 HPA exhibits the lowest value of D_{it} = 8×10^{11} $cm^{-2}eV^{-1}$, in comparison to D_{it} = 1.5×10^{12} $cm^{-2}eV^{-1}$ for the MOSCAP without HPA and D_{it} = 9.4×10^{11} $cm^{-2}eV^{-1}$ for the MOSCAP with H_2 HPA. We believe that these improvements are attributed mainly to the effective passivation of the interface traps during the D_2 HPA process.

For scientific support of the effect of D_2 HPA on InGaAs, instability of high-κ should be investigated. Since main advantage of D_2 annealing is for hot carrier injection and lift time improvement, therefore, instability measurement is necessary to proceed. By comparing with H_2 HPA regarding to device reliability, the influence of D_2 HPA can be proposed.

6.3.1 Concept of Solid phase doping on InGaAs

The non-planar device is now the main stream of CMOS technology. 3D gated III-V MOSFETs are being researched. Also, non-planar III-V MOSFETs on Si substrate are needed to be realized to commercialize III-V device. Aside from the gate interface challenge, the junction leakage current is mainly considered as a source of high off-current for InGaAs channel MOSFETs. The degradation of subthreshold characteristic and increase power consumption is caused by junction leakage [108-110].

The solid phase doping can be effective to form S/D region on InGaAs channel, especially, non-planar device architecture.[5] The Figure 6-1 (a) indicates solid phase doping method which is oxygen atoms from a deposited SiO_x layer on InGaAs can diffuse into InGaAs during post-deposition annealing, naming ORSO doping. Non-stoichiometric silicon dioxide (SiO_x) can be an effective doping source for InGaAs by in-diffusion of oxygen or silicon [51]. Since III-V materials are easily damaged by ion implantation for S/D doping, and low contact resistance is pursued, MBE epitaxial grown S/D formation is popular to use. However, ion implantation or raised S/D presents process challenges in the non-planar device.

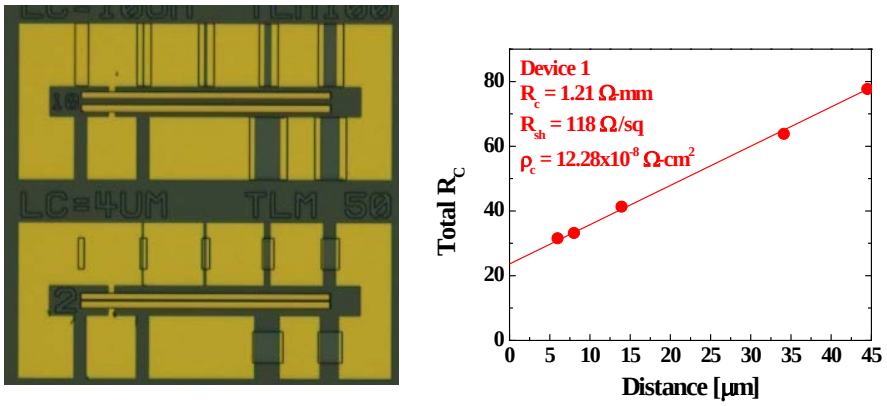


(a) (b)

Figure 6-6: The schematic diagram of solid phase doping process on substrate shown in (a) and I-V characteristics for InGaAs layer after solid phase doping process. The inset shows the result from the untreated InGaAs as a reference with a magnified scale (b)

[5]This chapter is based on reference [51]: [2] J. Ahn, H. Chou, **D. Koh**, T. Kim, J. H. Song, S. K. Banerjee, "**Nanoscale doping of compound semiconductors by solid phase dopant diffusion**", Appl. Phys. Lett.108, 1220107 (2016)
J. Ahn designed experiment and analyzed result. D.Koh designed measurement structure and fabricated ORSO TLM structure. D.Koh conducted hall measurement and TLM measurement.

Figure 6-6 (b) presents the current change after ORSO doping and activation in RTA. Basically, untreated InGaAs substrate shows high resistance of around ~10^5 Ω, however it reduces substrate resistance to ~10^3 Ω. Interesting result is that the reduction of resistance depends on thickness of dopant film.



(a) (b)

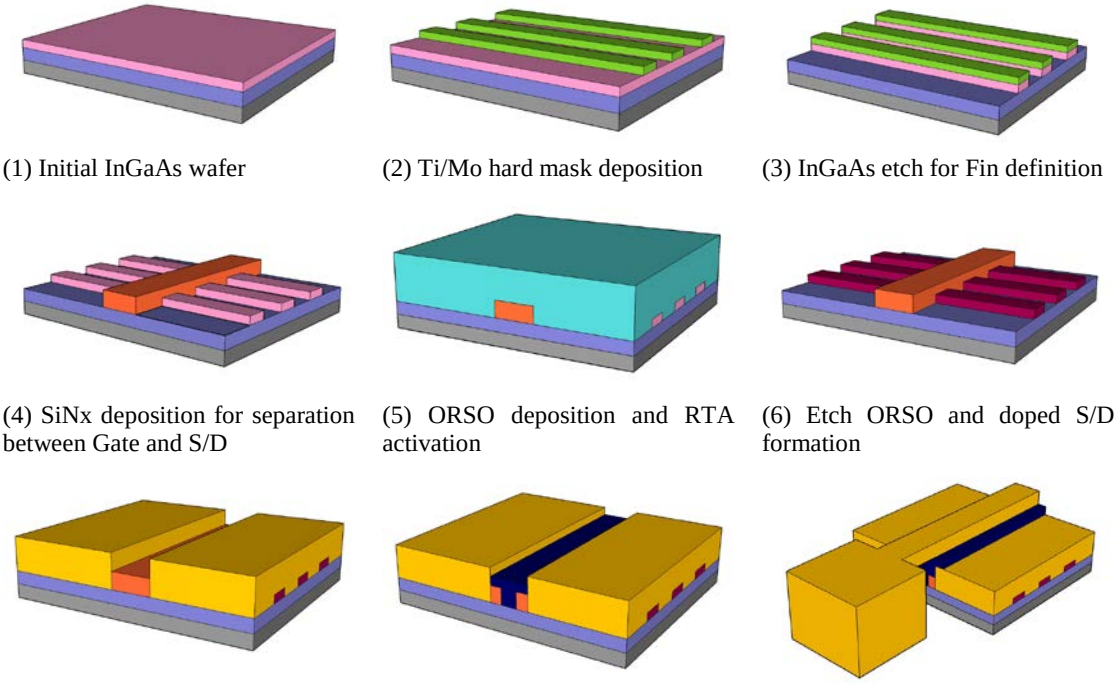
Figure 6-7: The transfer length measurement for ORSO doped InGaAs. (a) optical image of TLM structure, (b) total resistance as a function of pad distance

In order to observe contact resistance and specific contact resistivity, transfer length method is employed and fabricated as shown in Figure 6-7 (a). 20 um thickness ORSO is deposited and annealed at 700 °C for 10min. The Figure 6-7 (b) presents the contact resistance is 1.21 Ω-mm, and specific resistivity of 12.28 ×10^{-8}Ω-cm^2 is extracted. The resistance result is higher than that of QW wafer which is shown in chapter 4.

The solid phase doping can realize nanoscale doped S/D for the 3D device, for example, FinFET, Tri-gate, or Nanowire since this doping mechanism can be controlled by film thickness and activation time or temperature. Therefore, non-planar InGaAs MOSFETs with shallow S/D junction can be demonstrated with solid phase doping method following fabrication step shown Figure 6-3.

For solid phase doped InGaAs FinFET process, the process wafer consists of intrinsic InP capping layer, undoped InGaAs channel, a Si δ-doped InAlAs on InP substrate. The first e-beam lithography can be used to fin line patterning. Metal (Ti/Mo) hard mask for fin S/D area is formed by a lift-off process. Critical fin etching step is implemented in ICP dry etching system. After fin S/D area definition, the metal hard mask is stripped off clearly in CF_4 based RIE system. In order to dope only S/D region, PECVD SiN_X is grown to protect gate region and passivate over etched S/D underneath area where can be a junction leakage path. By patterning S/D area with e-beam lithography, the doping region is exposed to etch SiNx in RIE system. As S/D region is opened for solid phase doping, oxygen rich silicon dioxide (ORSO) is deposited and annealed at 700 °C for 10 min. Once n-type dopant activates into S/D region during annealing, ORSO film is etched away in diluted HF, and S/D is metallized by Mo/Ti/Au lift-off process. For gate stack, InGaAs channel layer is covered by SiN_x, which is used as doping hard mask. Gate line is patterned onto SiN_x, and then, etching is carried out to remove SiN_x at active region. Using digital etching method, InGaAs channel surface is cleaned to be deposited with high-κ. Al_2O_3/HfO_2 is incorporated for the gate dielectric,

and TiN is deposited gate metal and high-κ passivation. Using Ti/Au gate metal stack, solid phase doped FinFET is finalized.



(1) Initial InGaAs wafer

(2) Ti/Mo hard mask deposition

(3) InGaAs etch for Fin definition

(4) SiNx deposition for separation between Gate and S/D

(5) ORSO deposition and RTA activation

(6) Etch ORSO and doped S/D formation

(7) S/D contact metallization with Mo/Ti/Au

(8) Gate formation and HK deposition

(9) Gate contact metallization with Ti/Au

Figure 6-2: The device process flows for solid phase doped InGaAs FinFETs

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