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Monolithic Integration of Crystalline Oxides on Silicon and Germanium using Atomic Layer Deposition

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Monolithic Integration of Crystalline Oxides on Silicon and Germanium using Atomic Layer Deposition

by

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Dedication

To my family and friends, and especially my loving wife

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Monolithic Integration of Crystalline Oxides on Silicon and Germanium using Atomic Layer Deposition

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The University of Texas at Austin, 2015

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Inside your microelectronic devices there are up to a billion transistors working in flawless operation. Silicon has been the workhorse semiconductor used for the transistor; however, there must be a transition to materials other than silicon, such as germanium, with future device sizes. In addition, new dielectric oxide materials are needed. My research has examined a type of crystalline oxide, known as a perovskite, which is selected for its ability to bond chemically to Si and Ge, and eliminate the electrical defects that affect performance. Many perovskite oxides are lattice-matched to the Si (001) and Ge (001) surface spacing, enabling heteroepitaxy. To date, the majority of research on crystalline oxides integrated with semiconductors has been based on strontium titanate, $SrTiO_3$, epitaxially grown on Si (001) by molecular beam epitaxy. Alternative low-temperature growth methods, such as atomic layer deposition (ALD), offer both practical and economic benefits for the integration of crystalline oxides on semiconductors.

My initial research informed the broader community that four unit cells (~1.5 nm) of $SrTiO_3$ are required to enable heteroepitaxy on Si. The research has also shown that heteroepitaxial layers can be monolithically integrated with Si (001) without the formation of a SiO_x interlayer between the Si (001) surface and the $SrTiO_3$ layer because

ALD is performed at lower temperatures than are typical for MBE. Thus, a combined MBE-ALD growth technique creates possible advantages in device designs that require the crystalline oxide to be in contact with the Si (001) surface.

In recent work, I have demonstrated a method for integrating crystalline oxides directly on Ge by ALD. Germanium is being explored as an alternative channel material due to its higher hole and electron mobilities than Si, potentially enabling device operation at higher speed. This all-chemical growth process is expected to be scalable, is inherently less costly from a manufacturing cost of ownership, and is based on current manufacturing tool infrastructure. The impact of my research will be in continued scaling of device dimensions with novel materials that will provide faster speed and lower power consumption for microelectronic devices.

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Chapter 1: Introduction

Atomic layer deposition (ALD) is a proven technique for thin film oxide deposition. Most successful industrial applications have been through binary oxides, such as Al_2O_3 and HfO_2. However, there has been much effort to deposit ternary oxides, such as perovskites (ABO_3), with desirable properties for advanced thin film applications. Distinct challenges are presented with the deposition of multi-component oxides by ALD. This introduction is intended to highlight the research of the many groups that have deposited perovskite oxides by ALD methods. Several commonalities between the studies are discussed. Special emphasis is put on precursor selection, deposition temperatures, and specific property performance (high-*k*, ferroelectric, ferromagnetic, etc.). Lastly, the monolithic integration of perovskite oxides with semiconductors by ALD is reviewed. High-quality epitaxial growth of oxide thin films has traditionally been limited to physical vapor deposition techniques (*e.g.*, molecular beam epitaxy). However, recent studies have demonstrated that epitaxial oxide thin films may be deposited on semiconductors using ALD. This presents an exciting opportunity to integrate functional perovskite oxides for advanced semiconductor applications in a process that is economical and scalable.

1.1. Overview of Current Research

The semiconductor industry faces new challenges in the sub-10 nm era as scaling will no longer dominate performance improvement. New materials provide opportunity to improve performance with minimal architectural overhaul. For example, high-mobility channels of Ge and III-V semiconductors can provide both lower power consumption and faster computing speeds.[1-6] The epitaxial integration of crystalline

oxides on semiconductors presents an ideal platform to explore the fundamental materials physics with numerous technological applications.[7,8] Perovskite oxides are particularly important due to their common structure and lattice-matching with common semiconductors. For example, the cubic perovskite strontium titanate, $SrTiO_3$, (a = 3.91 Å) matches reasonably well with the Si (001) surface atomic spacing (d = 3.84 Å). In early works, molecular beam epitaxy (MBE) was used to grow epitaxial $SrTiO_3$ and $BaTiO_3$ on Si and Ge, respectively.[9,10] However, current nanometer length scales with multi-gate architectures of the semiconductor industry require chemical routes, such as atomic layer deposition (ALD), for uniform and conformal thin film deposition.[11]

ALD has a rich history in thin-film deposition for industrial applications, dating back to its early use in electroluminescent flat panel displays.[12] ALD offers controlled, sequential delivery of metalorganic precursors and co-reactants that either adsorb to saturation or undergo selective ligand reactions that are self-limiting.[13-16] ALD is now a commonly used deposition technique, finding common use in microelectronics,[17] photovoltaics,[18] and other advanced material applications.[19,20] The most prominent industrial applications of ALD are based on binary oxides, such as Al_2O_3 or HfO_2. The extension of ALD to ternary oxides is much less developed and requires additional considerations. For example, appropriate cycling conditions must be adjusted to obtain the desired stoichiometric ratio. Possible deviations from ideal ALD behavior may occur due to the inhomogeneity of the surface. However, with adequate cycling conditions and self-limiting behavior, the many benefits of ALD that have been demonstrated for binary oxides hold true for ternary oxides.

Perovskite oxides (ABO_3) are an extremely important class of ternary oxide materials. The ideal perovskite structure is cubic (space group *Pm3m*) with the larger *A* cation having 12-fold coordination and the smaller *B* cation in 6-fold coordination with

an octahedron of O anions. For many perovskites, the high degree of symmetry in the cubic structure is reduced through octahedral distortion and rotation to create pseudocubic phases. The relative size of the *A* and *B* cation has a large impact on these distortions that lead to a wide-array of properties from insulating to metallic, with many also being ferromagnetic,[21,22] ferroelectric,[23,24] multiferroic,[25,26] or superconducting.[27] Simple substitution of the *A* or *B* cation induces new properties in the perovskite structure, as shown in Figure 1.1. Partial substitution of the *A* and *B* lattice sites is also an effective way to enhance desirable properties. For example, partial substitution of Ti atoms in lead titanate, $PbTiO_3$, with Zr atoms to form $Pb(Zr,Ti)O_3$ is common to manipulate the ferroelectric properties.[8] In addition, advancements in thin film growth techniques over the last 20 years have enabled the growth of oxide heterostructures and superlattices with combined functional properties.[28-31]

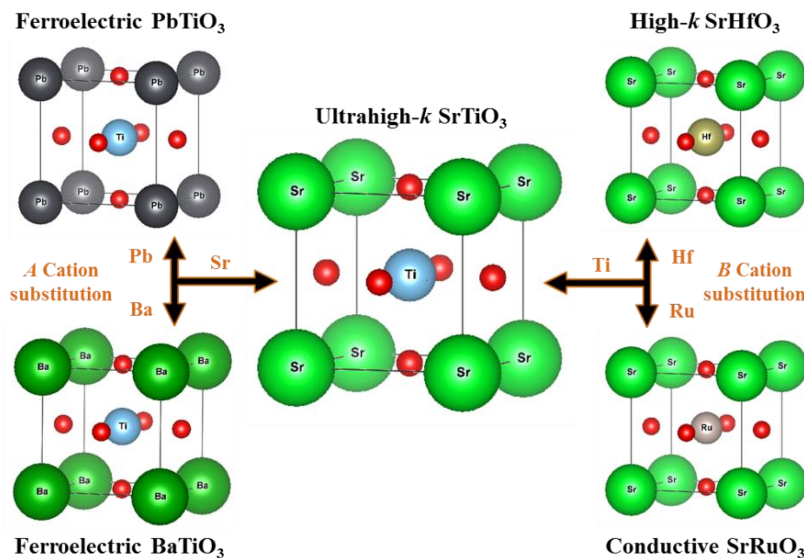


Figure 1.1. The versatility of the perovskite oxide is demonstrated by the simple substitution of the *A* or *B* cation. From ultrahigh-*k* $SrTiO_3$ (center) to ferroelectrics $PbTiO_3$/$BaTiO_3$ (left) and high-*k* $SrHfO_3$ or conductive $SrRuO_3$ (right).

This introduction reviews the many ALD processes that have been developed for perovskite oxides. The vast majority of this work has only been published in the last decade, with increasing knowledge of the complex interactions in multicomponent oxide systems. Tables have been created for easy reference to the known ALD processes for perovskite oxides. Included in these tables are the precursors (reactant *A* and *B*) along with the co-reactant (oxygen source) and deposition temperatures used. Some specific terminology has been used for consistency in reporting of the cycling conditions and growth rates. In this report, the term "supercycle" refers to the entire ALD cycling conditions that includes all of the metalorganic precursors used. The AO (or BO_2) subcycle refers to the common binary oxide ALD cycle, where the metalorganic precursor is exposed and then purged by an inert gas purge, followed by exposure to the co-reactant and subsequent purge. The subcycle ratio refers the ratio of AO:BO_2 subcycles in the overall ALD supercycle.

Finally, this review looks at very recent successes using ALD to integrate thin crystalline oxide perovskites directly on semiconductors. Previous works were limited to MBE techniques to deposit perovskites, such as $SrTiO_3$ and $BaTiO_3$, on Si and Ge substrates.[32-40] Successful growth of crystalline oxides on silicon by MBE requires a surface template (*e.g.*, half-monolayer of Sr) and appropriate deposition conditions that do not disrupt the surface.[41] Extending this concept to ALD is much the same, where a surface template is required and the deposition conditions must not disrupt that surface during oxide growth. Fortunately, the ALD reaction kinetics on appropriate Ge and III-V semiconductor surfaces allow for the deposition of crystalline perovskite oxides. The most recent information on epitaxial oxides grown on Ge will be provided from experiments within our own group.

1.2. PEROVSKITE OXIDES DEPOSITED BY ATOMIC LAYER DEPOSITION

Relevant studies of perovskite oxides deposited by ALD are summarized in this section. The summaries are divided into two major groups: (1) $A^{2+}B^{4+}O_3$ compounds and (2) $A^{3+}B^{3+}O_3$ compounds. Tables for all the ALD perovskite oxide processes are provided at the end of this section for convenient reference. The first group in Table 1 consists of the alkaline-earth containing and lead-based perovskite oxides. The second group in Table 2 consists primarily of La-based perovskite oxides and a series of rare-earth scandates. Details of each ALD process along with key characterization and commonalities can be found in the text below. Specific references are provided for all the work discussed herein.

Recent advancements in the atomic layer deposition of perovskite oxides has benefited from the development and experiments of novel metal precursors, such as those with cyclopentadienyl (Cp) and amidinate (amd) ligands.[42-45] For example, alkaline-earth based perovskites have benefited from the expanded use of the more volatile and reactive cyclopentadienyl precursors versus the traditional β-diketonate complexes. The relatively weak metal-ligand bond of the Cp complexes allows for oxide deposition using water as the co-reactant, while the stability of the Cp ligand itself minimizes decomposition and avoids significant carbon contamination in the deposited film.[45] Within the family of Cp precursors, bulkier ligands provide improved volatility and controllable delivery. Additionally, the relatively low melting points of $Sr(^{i}Pr_3Cp)_2$ and $Ba(^{i}Pr_3Cp)_2$ in particular allow for liquid sources at the sublimation temperature, which is generally preferred for ALD.

Most binary oxide ALD processes have been developed between 200-400 °C. Consequently, many ternary oxides have been deposited in similar temperature ranges within the overlapping temperature window. For example, if the AO and BO_2 processes

show ALD temperature windows of 200-300 °C and 250-350 °C, respectively, then the combined ABO_3 process is studied between 250-300 °C. However, several studies have suggested catalytic effects between the AO and BO_2 layers.[46] Experiments within our own group on $SrTiO_3$ have utilized lower deposition temperatures to achieve more ideal ALD behavior (*i.e.*, saturative growth and uniform composition).[47] Therefore, ternary oxide deposition processes should be developed without assumptions from the binary oxide processes, using the same metrics and evaluation for saturative and conformal growth. In extreme cases, there may be no ALD conditions for the ternary oxide even when using proven precursors for binary oxide deposition. On the other hand, some ALD processes become favorable when depositing the ternary oxide versus the binary oxides. The deposition of $SrTiO_3$ using a β-diketonate precursor with water as the co-reactant is one example.[48]

The ALD supercycle of ternary oxides requires additional considerations over common binary oxides. Generally, the deposition of a ternary oxide involves the intermixing of binary oxide cycles. The most obvious additional parameter is the A:B cycle ratio that is used to adjust the stoichiometry of the ternary oxide. In many cases, the A:B cycle ratio will not correlate exactly with the atomic ratio observed in the film. Additionally, the degree of subcycle intermixing should also be considered. For example, a 4:2 (A:B) cycle ratio may not yield the same composition in the deposited film as a 2:1 (A:B) cycle ratio. Generally, experiments have been performed with the highest degree of cycle intermixing to maximize homogeneity. However, this should not be considered a strict requirement. Extending these concepts to quaternary oxides adds even further complexity. As a result, only a few studies have been attempted to deposit quaternary perovskite oxides by ALD. Deposition processes for both ternary and

quaternary perovskite oxides must be developed such that the benefits of ALD (conformal growth and uniform composition) at the nanometer scale are still attainable.

In addition, the deposition rate of the ternary oxide is generally not a direct summation of the binary oxides. This is exemplified experimentally using different ALD precursors, where vastly different cycle ratios (A:B) lead to stoichiometric film growth. Often, the growth of the ternary oxide leads to an enhanced growth rate (Å/subcycle) over either binary oxide. This is due to the intricacy of ALD surface reactions that include adsorption, diffusion, and desorption of the metalorganic precursor. As a prime example, the growth rate of $SrTiO_3$ is enhanced over the individual binary oxides (SrO and TiO_2).[46] Regardless, the deposition of stoichiometric perovskite oxides can be achieved by tuning the A:B cycle ratio for a given set of ALD precursors.

One key observation from the experimental studies to date is that the intrinsic properties of bulk perovskite oxides that are desired for many applications are not realized in amorphous films. For example, the dielectric properties of high-k $SrTiO_3$ are significantly different for amorphous versus crystalline films. For $SrTiO_3$ grown by ALD, the dielectric constant of amorphous films (k~12-20) is much lower than the bulk single-crystal value of k~300. Two methods have been employed to crystallize the $SrTiO_3$ films and obtain higher dielectric values: (1) the films were post-deposition annealed at temperatures at or above 500 °C, and (2) a crystalline surface, or seed layer, was used to promote *in situ* crystallization of the $SrTiO_3$ when deposited at relatively higher temperatures. Crystallized $SrTiO_3$ films show a significantly increased dielectric constant (k~80-210); however, the leakage current also increases due to grain boundary formation. To fully realize the potential of perovskite oxide films and heterostructures, the crystalline quality and microstructure must be improved coherently.

The substrate plays a critical role in forming the desired crystal structure and potential for epitaxial integration of the crystalline oxide. Typically, amorphous substrates produce films that are amorphous as-deposited, especially at the relatively low temperatures of ALD. Subsequent post-deposition anneals may be employed to crystallize the perovskite films into a random polycrystalline structure. Crystallization improves the intrinsic properties of the perovskite (permittivity, conductivity, etc.); however, for many thin film applications, grain boundaries of polycrystalline structures are detrimental to device performance. Therefore, appropriate choice of a starting substrate, or a surface template, is necessary for integrating crystalline perovskite oxides with enhanced functionality and reduced bulk and interface defects. Epitaxial integration of thin film perovskites may be achieved by choosing a lattice-matched substrate. Fortunately, lattice matching between many perovskite oxides with semiconductor substrates is possible, which has great potential in advanced material applications.

Table 1.1. ALD processes for $A^{2+}B^{4+}O_3$ compounds

Material	Precursors for Atomic Layer Deposition of ABO_3 Perovskite Oxides				
	Reactant A	**Reactant B**	**Co-Reactant**	**T_{dep} (°C)**	**Reference**
$CaMnO_3$	$Ca(thd)_2$	$Mn(thd)_3$	O_3	200-330	78
$CaHfO_3$	$Ca(^{i}Pr_3Cp)_2$	$HfCl_4$	H_2O	225-230	83
$SrTiO_3$	$Sr(^{i}Pr_3Cp)_2$	$Ti(O^{i}Pr)_4$	H_2O	225-325	46,47,69,71,95
	$Sr(^{i}Pr_3Cp)_2$	$Ti(Me_5Cp)(OMe)_3$	*pl*-O_2, H_2O/O_3	250-275	84-87,94
	$Sr(^{i}Pr_3Cp)_2$	$Ti(MeCp)(OMe)_3$	O_3	275	84,85
	$Sr(^{i}Pr_3Cp)_2$	$Ti(Me_5Cp)(NMe_2)_3$	O_3	275	85
	$Sr(^{i}Pr_3Cp)_2$	$Ti(Me_5Cp)(NMe_2)_3$	O_3	275	85
	$Sr(^{i}Pr_3Cp)_2$	$Ti(O^{i}Pr)_2(thd)_2$	H_2O/O_3	370	91,94
	$Sr(^{t}Bu_3Cp)_2$	$Ti(OMe)_4$	H_2O, O_3	250	77,88,90,190
	$Sr(me\text{-}thd)_2$	$Ti(O^{i}Pr)_4$	*pl*-O_2	150-300	79
	$Sr(thd)_2$	$Ti(O^{i}Pr)_4$	H_2O, *pl*-H_2O, O_3	190-325	48,72,73
	$Sr(thd)_2$	$Ti(O^{i}Pr)_2(thd)_2$	H_2O	370	74,75
$(Sr,La)TiO_3$	$Sr(^{i}Pr_3Cp)_2$ / $La(^{i}Pr_2\text{-}famd)_3$	$Ti(O^{i}Pr)_4$	H_2O	225	58
$SrMnO_3$	$Sr(^{n}PrMe_4Cp)_2$	$Mn(Me_4Cp)_2$	H_2O	300	97
$SrFeO_3$	$Sr(thd)_2$	$Fe(thd)_3$	O_3	200-360	76
$SrRuO_3$	$Sr(^{i}Pr_3Cp)_2$	RuO_4*	O_2	230	93
$SrZrO_3$	$Sr(^{i}Pr_3Cp)_2$	$Zr(NEtMe)_4$	O_3	275	101
	$Sr(^{i}Pr_3Cp)_2$	$Zr(CpMe)_2(OMe)Me$	O_3	350	101
$SrHfO_3$	$Sr(^{t}Bu_3Cp)_2$	$Hf(MeCp)_2(OMe)Me$	H_2O	250	92
	$Sr(^{i}Pr_3Cp)_2$	$Hf(MeCp)_2(OMe)Me$	H_2O, *pl*-O_2	250	92
	$Sr(^{i}Pr_3Cp)_2$	$Hf(famd)_4$	H_2O	225	96
$BaTiO_3$	$Ba(Me_5Cp)_2$	$Ti(O^{i}Pr)_4$	H_2O	< 275	44,69
	$Ba(^{i}Pr_3Cp)_2$	$Ti(O^{i}Pr)_4$	H_2O	225	59
	$Ba(^{t}Bu_3Cp)_2$	$Ti(O^{i}Pr)_4$	H_2O	< 350	44
	$Ba(^{t}Bu_3Cp)_2$	$Ti(OMe)_4$	H_2O	300-340	81,82
	$Ba(Me_2NC_2H_4C_5Me_4)_2$	$Ti(O^{i}Pr)_4$	H_2O	unknown	44
$BaZrO_3$	$Ba(^{n}PrMe_4Cp)_2$	$Zr(NMe_2)_4$	H_2O	225-275	98
$PbTiO_3$	$Pb(Ph)_4$	$Ti(O^{i}Pr)_4$	O_3/H_2O	250-300	104
	$Pb(dmamp)_2$	$Ti(O^{i}Pr)_4$	H_2O	200	107
	$Pb(dmamp)_2$	$Ti(O^{t}Bu)_4$	H_2O	200	106,107
	$Pb(dpm)_2$	$Ti(O^{i}Pr)_2(dpm)_2$	H_2O	240	108
$PbZrO_3$	$Pb(Ph)_4$	$Zr(thd)_4$	O_3	275-300	105
$Pb(Zr,Ti)O_3$	$Pb(dpm)_2$	$Zr(dpm)_4$ / $Ti(O^{i}Pr)_2(dpm)_2$	H_2O	240	109
	$Pb(dpm)_2$	$Zr(dpm)_4$ / $Ti(O^{i}Pr)_4$	H_2O	240	109
	$Pb(dpm)_2$	$Zr(dibm)_4$ / $Ti(O^{i}Pr)_4$	H_2O	240	110
	$Pb(thd)_2$	$ZrCl_4$ / $Ti(O^{i}Pr)_2(thd)_2$	H_2O	250	111
	$Pb(thd)_2$	$Zr(thd)_4$ / $Ti(O^{i}Pr)_2(thd)_2$	H_2O	250	112

*CVD of RuO_2 through thermal decomposition of RuO_4 only (no co-reactant)

Table 1.2. ALD processes for $A^{3+}B^{3+}O_3$ compounds

Material	Precursors for Atomic Layer Deposition of ABO_3 Perovskite Oxides				
	Reactant A	Reactant B	Co-Reactant	T_{dep} (°C)	Reference
$LaAlO_3$	$La(^iPr_2\text{-famd})_3$	$Al(CH_3)_3$	H_2O	250-300	[56,128,146]
	$La(^iPr_2\text{-amd})_3$	$Al(CH_3)_3$	H_2O	300-330	[142]
	$La(^iPrCp)_3$	$Al(CH_3)_3$	H_2O, O_3	176-380	[115,147,148]
	$La(thd)_3$	$Al(CH_3)_3$	O_3	250	[149]
	$La(thd)_3$	$Al(acac)_3$	O_3	325-400	[141]
	$La(N(SiMe_3)_2)_3$	$Al(CH_3)_3$	H_2O	225-275	[143-145]
$LaScO_3$	$La(^iPr_2\text{-famd})_3$	$Sc(Et_2\text{-amd})_3$	H_2O	300	[116]
	$La(thd)_3$	$Sc(thd)_3$	O_3	300	[179]
$LaTiO_3$	$La(thd)_3$	$TiCl_4$	O_3/H_2O	225	[165]
$(La,Li)TiO_3$	$La(thd)_3$ / $Li(O^tBu)$	$TiCl_4$	O_3/H_2O	225	[165]
$LaMnO_3$	$La(thd)_3$	$Mn(thd)_3$	O_3	250-300	[155]
	$La(Me_4Cp)_3$	$Mn(Me_4Cp)_2$	H_2O	300	[97]
$LaFeO_3$	$La(thd)_3$	$Fe(thd)_3$	O_3	200-360	[76]
$LaCoO_3$	$La(thd)_3$	$Co(thd)_2$	O_3	200-400	[191]
$LaNiO_3$	$La(thd)_3$	$Ni(thd)_2$	O_3	215-250	[154]
$LaGaO_3$	$La(thd)_3$	$Ga(acac)_3$	O_3	325-425	[159]
$LaYO_3$	$La(^iPr_2\text{-famd})_3$	$Y(^iPr_2\text{-amd})_3$	H_2O	280	[116]
$LaLuO_3$	$La(^iPr_2\text{-famd})_3$	$Lu(Et_2\text{-famd})_3$	H_2O	300-350	[116,117]
	$La(amd)_3$	$Lu(amd)_3$	H_2O	350	[125]
	$La(thd)_3$	$Lu(thd)_3$	O_3	300	[153]
$NdAlO_3$	$Nd(thd)_3$	$Al(CH_3)_3$	H_2O	300	[180]
$GdScO_3$	$Gd(^iPr_2\text{-amd})_3$	$Sc(Et_2\text{-amd})_3$	H_2O	310	[178]
	$Gd(thd)_3$	$Sc(thd)_3$	O_3	300	[177]
$DyScO_3$	$Dy(thd)_3$	$Sc(thd)_3$	O_3	300	[179]
$ErScO_3$	$Er(thd)_3$	$Sc(thd)_3$	O_3	300	[179]
$LuScO_3$	$Lu(thd)_3$	$Sc(thd)_3$	O_3	300	[179]
$YScO_3$	$Y(thd)_3$	$Sc(thd)_3$	O_3	335-350	[176]
	$Y(MeCp)_3$	$Sc(Cp)_3$	H_2O	300	[176]
$YMnO_3$	$Y(thd)_3$	$Mn(thd)_3$	O_3	250-300	[181]
$BiFeO_3$	$Bi(mmp)_3$	$Fe(Cp)_2$	O_3	250-350	[182]
	$Bi(thd)_3$	$Fe(thd)_3$	H_2O	250	[185]
	$Bi(CH_3)_3$	$Fe(C_6H_8)(CO)_3$	H_2O	480-550	[186]
	$Bi(Me_2\text{-}O^tBu)_3$	$Fe(O^tBu)_3$	H_2O	150	[187]

Note: Reactants A/B have been abbreviated for simplicity: acac = pentane-2,4-dionate, amd = acetamidinate, Cp = cyclopentadienyl, dibm = tetrakis(diisobutyrylmethanato), dmamp = 3-N,N-dimethyl-2-methyl-2-propanoxide, dpm = dipivaloylmethanato, Et = ethyl, famd = formamidinate, Me = methyl, mmp = 1-methoxy-2-methyl-2-propoxy, ^iPr = isopropyl, Ph = phenyl, thd = 2,2,6,6-tetramethyl-3,5-heptanedionato ($C_{11}H_{19}O_2$), me-thd = 1-(2-methoxyethoxy)-2,2,6,6-tetramethyl-3,5-heptanedionato

1.2.1. Alkaline-earth perovskite oxides (EBO_3)

Possibly the most well studied perovskites are those containing alkaline earth metals of Ca, Sr, and Ba. In fact, the perovskite name originates from the mineral calcium titanate, $CaTiO_3$, which was discovered in the mountains of Russia in 1839. In the last two decades, it is strontium titanate, $SrTiO_3$, which has been studied extensively for microelectronic applications due to its large dielectric constant and ability to monolithically integrate with silicon.[9] Furthermore, epitaxial $SrTiO_3$ grown on Si allows for large-area 'pseudo-substrates' to be used for the integration of many multi-functional perovskite oxides on a semiconductor platform.[7,32,34,35,40,49-59] Barium titanate, $BaTiO_3$, is a prototypical ferroelectric material that can be monolithically integrated with silicon and germanium.[10,52,60-63] The use of $BaTiO_3$ as a ferroelectric oxide to modulate the charge carriers in a semiconductor channel has extremely high potential for ultralow power switching devices.[64,65] The majority of alkaline-earth perovskites have been grown by MBE or pulsed-laser deposition (PLD); however, a chemical-based deposition process offers both practical and economic benefits that are paramount for implementing these novel oxide materials on an industrial-scale.

Chemical vapor deposition (CVD) of alkaline-earth perovskites (EBO_3, where E = alkaline-earth metals) was limited historically due to low volatility or low reactivity of metalorganic precursors. The commonly used β-diketonate metal complexes were found to be less volatile for alkaline-earth metals than other β-diketonates because of their tendency to cluster as oligomers.[66] However, reasonable volatility can be obtained from several metalorganic compounds containing alkaline-earth metals with cyclopentadienyl (Cp) ligands, which also have good reactivity to air and water. Early work explored using the simplest Cp-based chemistry for atomic layer growth of MgO from bis(cyclopentadienyl) magnesium [$Mg(Cp)_2$] and H_2O.[67,68] However, the simple

compounds of $Ca(Cp)_2$, $Sr(Cp)_2$, and $Ba(Cp)_2$ lack the thermal stability required for ALD growth. Therefore, the larger and heavier alkaline earth metals (Ca, Sr, Ba) require bulkier Cp-based ligands for increased thermal stability and controlled ALD growth.

Early works using Cp-based chemistries

The first deposition of $SrTiO_3$ and $BaTiO_3$ under ALD conditions was reported by Vehkamäki *et al*. at the University of Helsinki in 1999.[69] Their study utilized bis(triisopropylcyclopentadienyl) strontium [$Sr(^iPr_3Cp)_2$] and bis(pentamethylcyclopentadienyl) barium [$Ba(Me_5Cp)_2$] as the alkaline-earth metal precursors, together with titanium tetraisopropoxide [$Ti(O^iPr)_4$] and water. Both $SrTiO_3$ and $BaTiO_3$ were deposited on glass substrates. The Cp compounds were synthesized with tetrahydrofuran (THF) solvent molecules that were coordinated to the metals as adduct ligands, which release during volatilization of the precursor. Our experience with both these cyclopentadienyl compounds has shown that $Sr(^iPr_3Cp)_2$, known commercially as Absolut-Sr,[70] is a low-melting point solid (< 50 °C), in contrast to the much higher melting point (> 300 °C) of $Ba(Me_5Cp)_2$. The liquid state of the Sr precursor may be beneficial if delivery by conventional bubblers is required.

The growth behavior of $SrTiO_3$ was reported in the temperature range of 250-325 °C, with sequential exposures of the SrO and TiO_2 subcycles.[69] The composition could be tuned by the subcycle ratio, where stoichiometric films were found between 0.8:1 to 1:1 (Sr:Ti) subcycle ratios. The growth rate was found to be 0.7 Å/cycle for stoichiometric films, with higher growth rates observed for increasing Sr:Ti subcycle ratio. A high dielectric constant (k~175) was exhibited for polycrystalline $SrTiO_3$ films after post-deposition annealing in air at 500 °C for 1 h, which was nearly double the value in the as-deposited state (k~90). The measured lattice parameter showed a change

from 3.931 Å to 3.917 Å after post-deposition annealing, suggesting densification of the $SrTiO_3$ film may improve the permittivity. However, it is noted by the authors that the dielectric constant continues to decrease with decreasing thickness of the $SrTiO_3$ films, resulting in much lower values than reported for bulk $SrTiO_3$ crystals (k~300). Using silicon test wafers, excellent conformality and trench-filling capability was demonstrated for the $SrTiO_3$ process. The growth of $BaTiO_3$ was examined similarly, but at a lower temperature (275 °C) due to thermal decomposition of the Ba precursor.[69] The $Ba(Me_5Cp)_2$ source was volatilized at a slightly higher temperature of 160 °C due to the lower vapor pressure than $Sr(^iPr_3Cp)_2$. The authors note that the deposition of $BaTiO_3$ was less reproducible than $SrTiO_3$ in terms of film composition and, as a result, film properties. In addition, $BaTiO_3$ was amorphous in the as-deposited state and did not crystallize as easily as $SrTiO_3$. The growth rate was reported to be 0.5 Å/cycle, with a dielectric constant of k~165 for polycrystalline $BaTiO_3$ films after post-deposition annealing at 500 °C for 1 h in air.

A more detailed study of the $SrTiO_3$ process was reported by Vehkamäki *et al.* in 2001.[71] Once again $Sr(^iPr_3Cp)_2$ and $Ti(O^iPr)_4$ were used as the metalorganic precursors, while water was supplied as the co-reactant, at a temperature range of 250-325 °C. $SrTiO_3$ films were deposited on glass substrates at a pressure of 10 mbar using N_2 as a carrier/purge gas. The source temperatures were held at 100 °C and 40 °C for the Sr and Ti precursors, respectively. Higher growth rates (Å/cycle) were observed with increasing the $Sr(^iPr_3Cp)_2$ dosing time from 0.2 to 2.5 s, indicating some thermal decomposition of the Sr precursor. At 250 °C the films appeared amorphous as-deposited, while at 325 °C the polycrystalline perovskite structure was observed. The decomposition is enhanced at a deposition temperature of 325 °C compared to 250 °C; however, it does not lead to any significant carbon accumulation (0.1-0.3 at.%). Capacitor structures of polycrystalline

$SrTiO_3$ revealed a high dielectric constant (*k*~100) for a 50-nm film after post-deposition annealing at 500 °C in air. The permittivity was found to be a strong function of Sr:Ti atomic ratio, decreasing with higher Sr content due to the relatively low dielectric constant of SrO (*k*~15). In contrast, the measured refractive index of the $SrTiO_3$ films was nearly independent of the Sr:Ti ratio.

Details of the growth mechanism of $SrTiO_3$ were characterized using *in situ* quartz crystal microbalance (QCM) and quadrupole mass spectrometer (QMS).[46] Both the QCM and QMS measurements supported that true saturation of the Sr precursor could not be achieved at 325 °C. Using deuterated water (D_2O), the main gaseous byproduct of the SrO cycle was $C_5{}^iPr_3H_2D$ indicating reaction of the $Sr({}^iPr_3Cp)_2$ with the surface causes detachment of at least one of the Cp rings. In fact, on a TiO_2-terminated surface, the QCM mass change indicates that over 90% of the Cp ligands were released during the $Sr({}^iPr_3Cp)_2$ dose at a temperature of 325 °C. Based on our own work using these precursors, the increase in $SrTiO_3$ growth rate is associated with *in situ* film crystallization that promotes decomposition (ligand release) of the Sr precursor.[47] Lower deposition temperatures (< 250 °C) allow for amorphous $SrTiO_3$ films to be deposited with more ideal ALD behavior.

Alkaline-earth β-diketonate complexes for ALD

Despite the limited volatility and reactivity of alkaline-earth complexes with *β*-diketonate ligands, a few groups have shown that ALD of alkaline-earth perovskites is possible using these precursors.[48,72-79] In 2002, Kil *et al.* reported $SrTiO_3$ deposition by using bis(1-(2-methoxyethoxy)-2,2,6,6-tetramethyl-3,5-heptanedionate) strontium [$Sr(me\text{-}thd)_2$] and $Ti(O^iPr)_4$ with remote oxygen plasma as the co-reactant.[79] Thin films were deposited on Si (100) substrates at a deposition temperature of 250 °C. The Sr:Ti

atomic ratio was 1:1 when using a Sr:Ti cycle ratio of 1:1. At lower temperatures than 250 °C the films became Sr-rich, while at higher temperature (300 °C) the film became Ti-rich when using a Sr:Ti cycle ratio of 1:1. The $SrTiO_3$ film was amorphous as-deposited and the carbon content was below XPS detection limit (< 1 at.%). The growth rate was 0.39 Å/subcycle at a substrate temperature of 250 °C.

Kosola *et al.* at the Helsinki University of Technology deposited $SrTiO_3$ films using bis(2,2,6,6-tetramethyl-3,5-heptanedionate) strontium [$Sr(thd)_2$] and $Ti(O^iPr)_4$ as the metalorganic precursors, with ozone and water as the co-reactants for Sr and Ti, respectively.[72] The use of ozone in conjunction with the $Sr(thd)_2$ provides enhanced reactivity over water. For sufficient vapor pressure, the $Sr(thd)_2$ precursor was heated to 220 °C, which is a significantly higher temperature than required for $Sr(^iPr_3Cp)_2$. The films were deposited on Si (100) substrates under a pressure of 1 mbar using N_2 as the carrier and purge gas. The deposition temperature used for $SrTiO_3$ growth was 290 °C and 325 °C. The Sr:Ti atomic ratio could be controlled through the Sr:Ti cycle ratio; however, the growth was dependent on the temperature and cycle ratio. A cycle ratio of 1:1 (Sr:Ti) yielded nearly stoichiometric films with a 0.9:1 (Sr:Ti) atomic ratio. Carbon contamination was problematic using the $Sr(thd)_2$ precursor, as the film growth led to $SrCO_3$ formation instead of SrO. Polycrystalline $SrTiO_3$ films could only be obtained after post-deposition rapid thermal annealing in N_2 atmosphere at 650-900 °C for 3-5 min. The surface roughness of the films increased by a factor of 2-4 with higher annealing temperatures, as the film transitioned from amorphous to polycrystalline. In addition, further characterization of the films suggested that the polycrystalline strontium titanate was actually embedded in amorphous $SrCO_3$.

Several works attempted to expand or improve upon the $SrTiO_3$ deposition using $Sr(thd)_2$ as the Sr source. Kwon *et al*. at Seoul National University used remote-plasma

activated water to improve the reaction between Sr(thd)$_2$ and H_2O at a deposition temperature of 250 °C.[73] Thin films were deposited on Si, Pt-coated Si, and Ru-coated Si substrates. Patterned Si substrates, with contact holes of 0.13 μm diameter and 1 μm depth (aspect ratio of 8), were used to verify thickness and composition uniformity. An improvement in the deposition characteristics, especially composition step coverage, was observed for $SrTiO_3$ by lowering the Sr(thd)$_2$ bubbling temperature below 200 °C to prevent oligomerization and allow for monomer-like adsorption. The excellent step coverage (> 95%) and minimal composition variation (3%) is highlighted in Figure 1.2. However, there was still high residual carbon contamination (> 5%) due to incomplete removal of the 'thd' ligands in the deposited films. The electrical properties of these films were measured from metal-insulator-metal (MIM) structures with a top Pt electrode and bottom Ru electrode.[48] The growth temperature was varied between 190-270 °C, while the Sr(thd)$_2$ and Ti(O^{i}Pr)$_4$ sources were vaporized at 170 °C and 50 °C, respectively. Both plasma-activated and thermal H_2O were studied as the co-reactant. The work confirmed that SrO deposition kinetics are quite sluggish using Sr(thd)$_2$ and water vapor; however, the deposition of $SrTiO_3$ using the same precursors is significantly better due to the improved reactivity on TiO_2 surfaces. The effective dielectric constant of $SrTiO_3$ was relatively low (k~20) for the as-deposited films, but increased to k~80 by post-deposition annealing in N_2 atomsphere to crystallize the films.

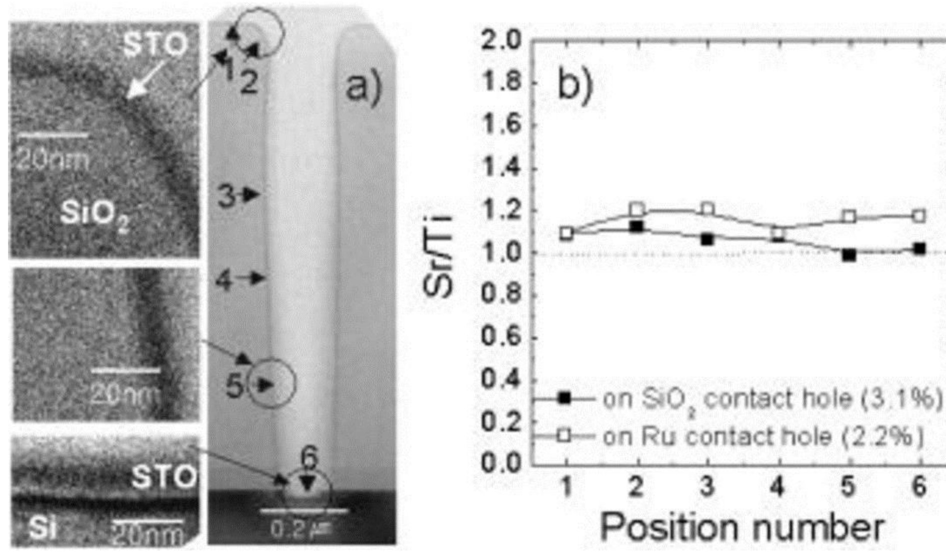


Figure 1.2. (a) Cross-sectional TEM image of $SrTiO_3$ films on SiO_2 contact hole and (b) Sr/Ti atomic ratio at the various points shown in (a). Those on the contact hole having the bottom Ru electrode are also shown.[68] [Reprinted with permission from *J. Electrochem. Soc.*, **152**, C229 (2005). Copyright 2005, The Electrochemical Society.]

A two-step growth and anneal process was explored to optimize the electrical properties (high *k*-value and low leakage) by improving the microstructure of the $SrTiO_3$ films grown on Ru electrodes.[48] The two-step growth and anneal allows for a thin seed layer (~5 nm) to be crystallized, followed by deposition of a thicker film. By using a crystalline seed layer grown by ALD, the final post-deposition anneal temperature could be lowered that led to improved capacitance and leakage current values. In addition, higher ALD temperatures appeared to also improve electrical performance of $SrTiO_3$ films deposited on the crystalline seed layer. The best results yielded a low EOT of 0.45 nm with a leakage current of 10^{-3} A/cm^2 at 1 V. To explore higher deposition temperatures, the same research group deposited $SrTiO_3$ films using $Sr(thd)_2$ and $Ti(O^iPr)_2(thd)_2$ at 370 °C using H_2O as the co-reactant.[74,75] By replacing two of the isopropoxide ligands with 'thd' ligands, the thermal stability of the Ti precursor was

increased to allow ALD at higher temperatures. A thin $SrTiO_3$ seed layer (~3 nm) was again used to promote *in situ* crystallization of the main $SrTiO_3$ film. This higher deposition temperature led to denser $SrTiO_3$ films, which improved the electrical properties. A high dielectric constant (k~108) and low leakage current density (10^{-7} A/cm^2 at 0.8 V) were achieved for a 20-nm-thick $SrTiO_3$ film. The study concluded that a 3-5 nm $SrTiO_3$ seed layer crystallized at 650-700 °C provided optimal electrical performance for their MIM structures of $Pt/SrTiO_3/Ru$.[74]

Beyond $SrTiO_3$, only a few other alkaline-earth perovskite oxide ALD processes have been reported using β-diketonate complexes.[76-78] Nilsen *et al.* deposited thin films of calcium-substituted lanthanum manganite, $La_{1-x}Ca_xMnO_3$, using $La(thd)_3$, $Ca(thd)_2$, and $Mn(thd)_3$ with ozone as the co-reactant at temperatures between 200-330 °C.[78] Interestingly, $La_{1-x}Ca_xMnO_3$ films were low in carbon impurities despite the formation of $CaCO_3$ when only $Ca(thd)_2$ and ozone were used in previous work.[80] The same group deposited thin films of lanthanum strontium ironate, $La_{1-x}Sr_xFeO_3$, using $La(thd)_3$, $Sr(thd)_2$, and $Fe(thd)_3$ with ozone as the co-reactant at temperatures between 185-430 °C.[76] ALD behavior was observed between 200-360 °C for $LaFeO_3$. As before, only a small amount of carbon impurities was observed for $La_{1-x}Sr_xFeO_3$ despite the formation of $SrCO_3$ from $Sr(thd)_2$ and ozone under similar deposition conditions. The ALD cycle ratios of the metalorganic precursors did not correlate well with the resulting atomic composition of the films. These studies demonstrated that multicomponent phases are attainable by ALD, but with increasing complexity.

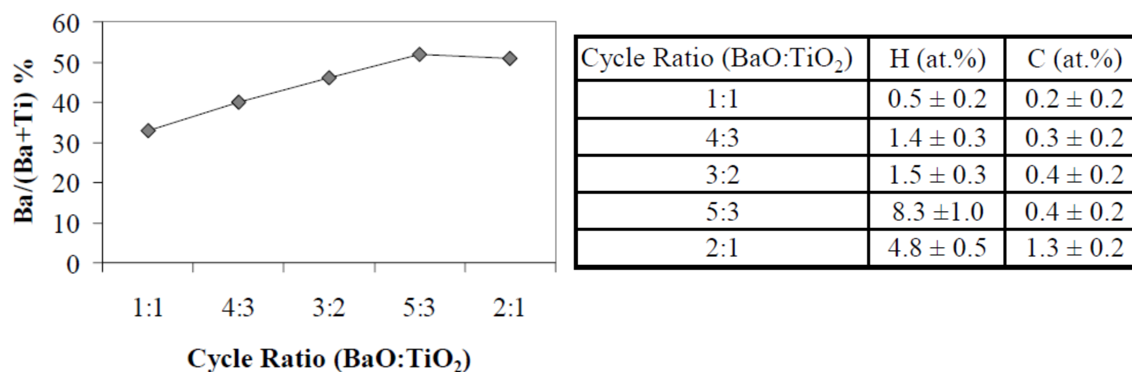
Recent works using Cp-based chemistries

The majority of recent ALD work on alkaline-earth containing perovskite oxides has used the more volatile and reactive cyclopentadienyl (Cp) complexes. In 2004,

studies by Hatanpää *et al.* at the University of Helsinki suggested that Cp-based ligands with *tert*-butyl and isopropyl moieties are the most thermally stable and volatile Ba precursors.[44] In their study, a total of nine Ba complexes were synthesized and compared, from which three were evaluated for ALD of $BaTiO_3$ that included $Ba(Me_5Cp)_2$ and bis(tri-*tert*-butylcyclopentadienyl) barium [$Ba(^tBu_3Cp)_2$] with THF adducts. Evaporation temperatures for $Ba(Me_5Cp)_2$ and $Ba(^tBu_3Cp)_2$ were 160 °C and 120 °C, respectively. Once again, $Ti(O^iPr)_4$ and H_2O were used as the Ti source and co-reactant, respectively. $BaTiO_3$ films deposited at or below 325 °C were amorphous and required post-deposition annealing at 500 °C for crystallization. Interestingly, $Ba(^iPr_3Cp)_2$ with THF adducts has the lowest reported melting temperature (115 °C) of the complexes studied by Hatanpää *et al.*, but the deposition of $BaTiO_3$ using $Ba(^iPr_3Cp)_2$ was not reported until recently by our group.[59]

A few years later Vehkamäki *et al.* reported in detail on the deposition of $BaTiO_3$ using $Ba(^tBu_3Cp)_2$ and $Ti(OMe)_4$ with water as the co-reactant.[81] Both the Ba and Ti precursors were held at 130-140 °C. By mixing the Ba and Ti subcycles as thoroughly as possible, the formation of barium hydroxide is suppressed. The growth rate varied between 0.37-0.5 Å/cycle for Ba:Ti cycle ratios between 1:1 and 3:1. The optimal Ba:Ti cycle ratio for stoichiometric films was found between 3:2 and 2:1. The $BaTiO_3$ thin films were amorphous as-deposited at 340 °C and crystallized into the perovskite structure after post-deposition annealing at 600 °C in O_2 atmosphere for 1 h. The authors note that rapid annealing was beneficial, as slow ramping of the temperature resulted in pinhole formation. Electrical measurements were performed on capacitor structures. Higher device yield (> 90%) was observed when the samples were annealed after the top Pt electrode was deposited by electron beam evaporation. The effective dielectric constant of a 32 nm crystalline $BaTiO_3$ film was k~73, but much lower for a 60 nm

amorphous film (k~15). The scale-up of the $BaTiO_3$ deposition from laboratory scale to 200 mm wafers was demonstrated by the same group.[82] The evaporation temperatures for $Ba(^tBu_3Cp)_2$ and $Ti(OMe)_4$ were 155 °C and 150 °C, respectively. The most stoichiometric films were reported for Ba:Ti cycle ratios of 5:3 and 2:1; however, they also displayed the highest hydrogen impurity of 8.3 at.% and 4.8 at.%, respectively, as shown in Figure 1.3. A cycle ratio of 5:3 (Ba:Ti) showed the highest growth rate of 0.76 Å/cycle and also the best film uniformity (1σ ~ 2.7%). Once again, the as-deposited $BaTiO_3$ films were amorphous and crystallized after post-deposition annealing at 600 °C for 30 min under O_2 atmosphere.



Cycle Ratio ($BaO:TiO_2$)	H (at.%)	C (at.%)
1:1	0.5 ± 0.2	0.2 ± 0.2
4:3	1.4 ± 0.3	0.3 ± 0.2
3:2	1.5 ± 0.3	0.4 ± 0.2
5:3	8.3 ±1.0	0.4 ± 0.2
2:1	4.8 ± 0.5	1.3 ± 0.2

Figure 1.3. (left) Atomic composition, Ba/(Ba+Ti) %, in $BaTiO_3$ films deposited at 300 °C, and (right) hydrogen and carbon impurities measured in the $BaTiO_3$ films under varying Ba:Ti cycle ratios.[79] [Reprinted with permission from *ECS Trans.* **1**, 137 (2006). Copyright 2006, The Electrochemical Society.]

Density functional theory calculations were performed in 2007 by Holme and Prinz at Stanford University to determine optimal ALD precursors for Sr and Ba compounds based on the energy required to break the metal-ligand bonds.[45] The authors evaluated nine Sr and twelve Ba precursors, including *β*-diketonate complexes and several Cp compounds. The energy of the metal-ligand bond was calculated to determine

which precursors would react most readily. In addition, the bond energies within the precursor ligand were studied to determine the potential for carbon contamination during film deposition. The β-diketonate ligands were found to have stronger bonds to the metals than the Cp ligands; however, the bonds within the β-diketonate ligand are much weaker, explaining both the limited reactivity and high carbon content found experimentally. Based on the bond strength analysis, the authors conclude that the optimal Sr and Ba precursors are the Cp complexes of *n*-propyltetramethylcyclopentadienyl (^{n}PrMe$_4$Cp) and pentamethylcyclopentadienyl (Me$_5$Cp) ligands, which had the lowest energy required to break the first metal-ligand bond (2.42 eV).[45] However, ALD experiments using Sr(^{n}PrMe$_4$Cp)$_2$ used a sublimation temperature 190-200 °C, which makes low temperature (< 200°C) ALD impossible. It is noteworthy that the triisopropylcyclopentadienyl (^{i}Pr$_3$Cp) and tri-*tert*-butylcyclopentadienyl (^{t}Bu$_3$Cp) ligands have only slightly higher energies to break the first metal-ligand bond of 2.58 eV and 2.54 eV, respectively, with lower melting points and greater volatilities due to the bulkier ligands. This allows for controlled delivery in ALD over a larger temperature window. For these reasons, the ^{i}Pr$_3$Cp and ^{t}Bu$_3$Cp complexes appear to be the most preferred alkaline-earth precursors for ALD in recent experimental work.[47,81-96]

Nevertheless, Holme *et al.* deposited lanthanum-substituted strontium manganite, La$_x$Sr$_{1-x}$MnO$_3$, from Cp-based chemistries using La(Me$_4$Cp)$_3$, Sr(^{n}PrMe$_4$Cp)$_2$, Mn(Me$_4$Cp)$_2$, and water as the co-reactant.[97] The films were deposited at a substrate temperature of 300 °C using sublimation temperatures of 220 °C (La), 210 °C (Sr), and 180 °C (Mn). The observed growth rate for La$_x$Sr$_{1-x}$MnO$_3$ was 5 Å/subcycle, strongly suggesting the growth was not self-limiting (CVD-like) at a substrate temperature of 300 °C; however, the films were dense and uniform with low impurity levels. The La$_x$Sr$_{1-}$

$_xMnO_3$ films were amorphous as-deposited on Si_3N_4/Si substrates, but crystallized into the polycrystalline perovskite phase after post-deposition annealing at 800 °C for 3 h, with clear faceting of the surface observed. When deposited on a polycrystalline yttria-stabilized zirconia layer, the $La_xSr_{1-x}MnO_3$ was polycrystalline as-deposited. In later work from the same group, An *et al.* reported on the deposition of yttrium-doped barium zirconate, $BaY_xZr_{1-x}O_3$, using Ba(^{n}PrMe$_4$Cp)$_2$, Y(MeCp)$_3$, tetrakis-dimethylamido zirconium [Zr(NMe$_2$)$_4$], and water as the co-reactant.[98] Once again the smaller Cp ligands required high sublimation temperatures of 220 °C and 170 °C for the Ba and Y sources, respectively. Pure $BaZrO_3$ was deposited at a temperature 225-275 °C on 4-inch Si wafers with a Ba:Zr cycle ratio of 1:1. The growth rate was 1.2 Å/cycle under the given conditions. The $BaY_xZr_{1-x}O_3$ films were amorphous as-deposited, but crystallized into the perovskite phase after post-deposition annealing at 800 °C for 2 h in N_2 atmosphere. These two studies demonstrated that ^{n}PrMe$_4$Cp ligands are capable of depositing alkaline-earth perovskites; however, the ALD temperature window appears limited.

Only one Ca-based perovskite oxide has been deposited by ALD using the Cp-based chemistry. The deposition of calcium hafnate, $CaHfO_3$, was explored in 2006 by Kukli *et al.* at the University of Helsinki using Ca(^{i}Pr$_3$Cp)$_2$ and $HfCl_4$ as the metalorganic precursors with water as the co-reactant.[83] Nearly stoichiometric $CaHfO_3$ films were grown on borosilicate glass and Si substrates at 225-230 °C with a 1:1 (Ca:Hf) cycle ratio. Despite equal amounts of Ca and Hf in the deposited film, the $CaHfO_3$ perovskite phase was not observed by XRD after crystallization. A thinner 7 nm film appeared amorphous, while a thicker 40 nm film showed XRD peaks consistent with a Hf-rich phase, $Ca_2Hf_7O_{16}$. It is unclear from the reported study why the polycrystalline $CaHfO_3$ phase could not be obtained.

The deposition of several Sr- and Ba-based perovskite oxides has been demonstrated using the $^{i}Pr_3Cp$ and $^{t}Bu_3Cp$ complexes in the past decade.[47,81,82,84-96] Much of this work attempted to find compatible Ti sources that decomposed at relatively higher temperatures to allow *in situ* crystallization of the oxide film. In 2008, Katamreddy *et al.* reported on the deposition characteristics of $SrTiO_3$ using $Sr(^{i}Pr_3Cp)_2$ with and without stabilizing adducts, along with four heteroleptic Cp complexes of Ti that included trimethoxy-'penta'methylcyclopentadienyl titanium [$Ti(Me_5Cp)(OMe)_3$ / $Ti(MeCp)(OMe)_3$] and tris(diethylamino)-'pentamethyl'cyclopentadienyl titanium [$Ti(Me_5Cp)(NMe_2)_3$ / $Ti(Cp)(NMe_2)_3$].[84,85] ALD behavior was observed at a deposition temperature of 275 °C with ozone as the co-reactant, and the Sr:Ti atomic ratio could be tuned by changing the cycle ratio. Theoretical studies have suggested that the heteroleptic $Ti(Me_5Cp)(OMe)_3$ is more reactive than the homoleptic $Ti(OMe)_4$; however, no deposition occurs when using the heteroleptic Ti complex with water. Theoretical calculations have shown that $Ti(Me_5Cp)(OMe)_3$ does not chemisorb well due to crowding of the Ti atom by the Me_5Cp ligand, which prevents ALD growth.[99] Therefore, the heteroleptic Cp complexes of Ti are not suitable for thermal ALD with water and require a stronger co-reactant, such as ozone or oxygen plasma.

Further ALD studies of $SrTiO_3$ using the $Sr(^{i}Pr_3Cp)_2$ complex with 1,2-dimethoxyethane (DME) adduct and $Ti(Me_5Cp)(OMe)_3$, known commercially as Star-Ti,[70] were reported by Langereis *et al.* at Eindhoven University of Technology using remote-plasma oxygen as the co-reactant instead of ozone.[86,87] The source temperatures were held at 110 and 120 °C, respectively, to maintain vapor pressures 2 torr and 0.05 torr for Sr and Ti, respectively. The films were amorphous as-deposited on Si substrates with native oxide at a temperature of 250 °C. Nearly stoichiometric films were observed for a Sr:Ti cycle ratio of 1:2. The observed growth rate of $SrTiO_3$ using this cycle ratio

was 0.69 Å/subcycle. The $SrTiO_3$ films were post-deposition annealed in N_2 for 10 min at temperatures between 400-650 °C. At anneal temperatures greater than or equal to 500 °C, the films crystallized into the polycrystalline perovskite with a corresponding large change in the dielectric function. Capacitor structures of a 50-nm-thick $SrTiO_3$ revealed a high dielectric constant ($k > 80$) and a low leakage current of $< 10^{-7}$ A/cm^2 at 1 V.[86] Additional work from the same group showed that the Sr:Ti atomic ratio could be tuned between 0.73 and 2.13 for 30 to 40-nm-thick $SrTiO_3$ films by varying the Sr:Ti cycle ratio.[87] The deposition process was developed in a commercial reactor capable of handling 200 mm diameter wafers. Nearly stoichiometric films were deposited on 100 and 200 mm Si wafers with native oxide at Sr:Ti cycle ratios of 2:8 and 2:5, depending on the specifics of the reactor setup. The films were crystallized by rapid thermal anneal (RTA) at 600 °C for 10 min. For Sr:Ti atomic ratios of 0.93 to 1.70, the films crystallized in the polycrystalline perovskite structure; although, the peak intensity was stronger for more stoichiometric films.

In efforts to look at the most thermally stable Sr and Ti precursors using water as the co-reactant, Popovici *et al.* at IMEC Belgium studied the deposition of $SrTiO_3$ using $Sr(^tBu_3Cp)_2$ and $Ti(OMe)_4$.[88] The Sr and Ti sources (both solids) were heated to 180 °C and 160 °C, respectively. $SrTiO_3$ films were deposited on 300 mm wafers of SiO_2(1 nm)/Si (100) and TiN(10 nm)/SiO_2(20 nm)/Si (100). The deposition temperature was 250 °C, where uniformity variation was less than 2.5% across a 300 mm wafer for $SrTiO_3$ thicknesses between 5 and 25 nm. Stoichiometric films were observed for a cycle ratio of 4:3 (Sr:Ti). The composition of Sr/(Sr+Ti) could be tuned between 0.45 to 0.77 by changing the cycle ratio from 1:1 to 10:1 (Sr:Ti), respectively. The onset of crystallization was lowest (540 °C) for stoichiometric $SrTiO_3$. Films crystallized with a post-deposition anneal at 600 °C for 5 min in N_2 atmosphere showed XRD peaks

consistent with the perovskite structure for Sr/(Sr+Ti) ratios between 0.45 to 0.71, although the peak intensities were lower for non-stoichiometric films. Capacitor structures revealed a maximum dielectric constant (*k*~210) for stoichiometric $SrTiO_3$, which reduces rapidly with higher Sr content. More detailed characterization of these MIM capacitors with a TiN bottom electrode were reported for Sr/(Sr+Ti) atomic ratios between 0.45 and 0.67.[89] The extracted dielectric constant of the as-deposited (amorphous) $SrTiO_3$ was *k*~16-18, with only slight dependence on stoichiometry. In contrast, the crystallized $SrTiO_3$ films showed a large dielectric constant that varied with composition, such that *k*~210 for stoichiometric films (50% Sr) and *k*~56 for Sr-rich films (62% Sr). Concurrently, the leakage current is reduced for Sr-rich films due to an increased band gap and apparent reduction in microcracks during crystallization.[89] This becomes an unfortunate trade-off between the high-*k* properties and leakage current of $SrTiO_3$-based structures.

Additional work by Popovici *et al.*, using the same precursors for $SrTiO_3$ deposition, explored the influence of various annealing conditions and seed layer formation on the film morphology and crystallinity.[90] The study verified that the dielectric constant of $SrTiO_3$ films, and consequently the performance of MIM capacitors, is strongly influenced by process conditions. $SrTiO_3$ films were deposited on 300 mm of 20 nm SiO_2/Si (100) wafers capped with 10 nm of TiN deposited by PVD. The films were amorphous as-deposited at 250 °C, but crystallized after post-deposition annealing. The crystallization onset occurred between 500 °C (7 °C/min ramp rate) and 850 °C (laser anneal). The morphology and size of the crystalline grains were related to both the thermal budget and the Sr:Ti atomic ratio. For example, $SrTiO_3$ films spike annealed (ramp rate of ~220 °C/min) between 700-900 °C showed increased fragmentation of the film with higher temperatures, as shown in the SEM images of

Figure 1.4. Stoichiometric $SrTiO_3$ showed large grains (hundreds of nanometers) that were distorted from crystallization and resulted in microcrack formation. Sr-rich films (62% Sr) crystallized in smaller grains (< 50 nm) and could be used as a seed-layer to reduce microcrack formation in stoichiometric films deposited above.

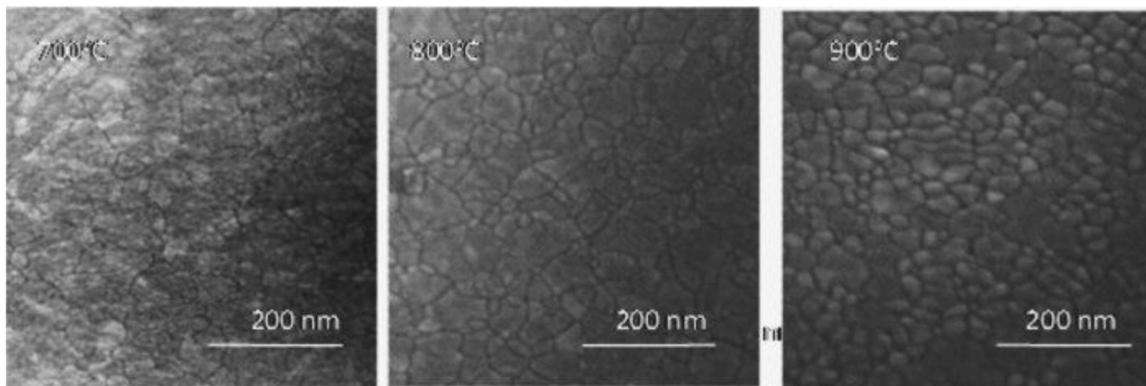


Figure 1.4. SEM plan view images of the $SrTiO_3$ films spike annealed at 700, 800, and 900 °C.[90] [Reprinted with permission from *J. Vac. Sci. Technol. B* **29**, 01A304 (2011). Copyright 2011, American Vacuum Society.]

In 2011, further development of $SrTiO_3$-based capacitors by ALD was reported by Lee *et al.* at Seoul National University using $Sr(^{i}Pr_3Cp)_2$ and $Ti(O^{i}Pr)_2(thd)_2$ with water and ozone as the co-reactants.[91] The Cp-based precursor provides better reactivity than $Sr(thd)_2$, allowing for an enhanced growth rate per cycle at a deposition temperature of 370 °C. In addition, $Sr(^{i}Pr_3Cp)_2$ is liquid at the sublimation temperature, which allows for bubbler delivery with an inert carrier gas (argon). The Sr and Ti bubblers were heated to 110 °C and 130 °C, respectively. For stoichiometric film growth, the Sr:Ti cycle ratio was 1:3 due to higher incorporation of SrO versus TiO_2 per subcycle. This is not unexpected due to the relatively high deposition temperature of 370 °C, which is beyond the reported ALD temperature window for $Sr(^{i}Pr_3Cp)_2$ and H_2O.[84] Nevertheless, at the given parameters, the thickness of the $SrTiO_3$ film was directly proportional to the

number of ALD cycles with a growth rate of 0.107 nm/subcycle.[91] Enhancement of the growth rate was observed on various substrates (Ru, RuO_2, IrO_2), requiring a 5 nm TiO_2 barrier layer to control the initial deposition characteristics. To allow for *in situ* crystallization of the $SrTiO_3$ film during deposition, a crystalline seed layer was used. The main $SrTiO_3$ layer was then crystalline as-deposited with a high dielectric constant of k~146. A minimum EOT of 0.57 nm was obtained for a 10 nm $SrTiO_3$ film with a low leakage current of 3×10^{-8} A/cm^2 at 0.8 V. Extending this work to another heteroleptic Ti precursor, the same group deposited $SrTiO_3$ dielectrics using $Sr(^iPr_3Cp)_2$ and $Ti(Me_5Cp)(OMe)_3$.[94] As before, water and ozone were used as the co-reactant for Sr and Ti, respectively. The source temperatures were 90 °C and 80 °C for the Sr and Ti, respectively. When compared with the previous $Ti(O^iPr)_2(thd)_2$ precursor, the deposition per cycle of TiO_2 with $Ti(Me_5Cp)(OMe)_3$ and ozone was 40% higher. The growth rate of $SrTiO_3$ was 0.123 nm /subcycle at a temperature of 370 °C. Slight improvement in the EOT could be achieved by eliminating the TiO_2 reaction barrier that was employed previously, despite the CVD-like behavior during the initial deposition. A minimum EOT of 0.43 nm was achieved with a low leakage current of 8×10^{-8} A/cm^2 at 0.8 V.

Other Sr-based perovskites, including $SrHfO_3$and $SrRuO_3$, have recently been deposited by ALD methods.[92,93,96] Strontium hafnate, $SrHfO_3$, deposition was first reported by Black *et al.* at the University of Liverpool using $Sr(^iPr_3Cp)_2$, or $Sr(^tBu_3Cp)_2$, and bis(methylcyclopentadienyl)-methoxy-methyl hafnium [$Hf(MeCp)_2(OMe)Me$] with both water and oxygen plasma as the co-reactant.[92] Due to the limited reactivity of the Hf precursor with water vapor, only $SrHfO_3$ films deposited using the oxygen plasma were discussed in detail. At a deposition temperature of 250 °C, a 3:1 (Sr:Hf) cycle ratio yielded stoichiometric $SrHfO_3$ films. The film was amorphous as-deposited on Si (100) substrates and crystallized into the polycrystalline perovskite structure upon post-

deposition annealing in air at 600 °C for 30 min. Capacitor structures for a 57-nm-thick polycrystalline $SrHfO_3$ film showed low frequency dispersion with a dielectric constant of k~21.

Deposition of Hf-based perovskites is also possible by using β-diketonate or amidinate type precursors. The deposition of barium hafnate, $BaHfO_3$, was reported by Lukosius *et al.* (2012) in a study of perovskite-type dielectrics for MIM applications.[77] Pulsed-injection MOCVD was used with traditional β-diketonate precursors, $Ba(thd)_2$ and $Hf(thd)_4$, to deposit thin films of $BaHfO_3$ at 400 °C. Oxygen was added as the co-reactant. In our group, we have recently reported on the deposition of epitaxial $SrHfO_3$ on Ge by ALD, using $Sr(^iPr_3Cp)_2$ and hafnium tetraformamidinate [$Hf(famd)_4$] with water as the co-reactant.[96] Nearly stoichiometric films were achieved using a Sr:Hf cycle ratio of 1:1 at a deposition temperature of 225 °C. The $SrHfO_3$ films are amorphous as-deposited, but become crystalline with epitaxial alignment to the underlying Ge substrate after vacuum annealing at 700 °C for 5 min. More detailed discussion on the monolithic integration of epitaxial oxides on semiconductors by ALD, including $SrHfO_3$ on Ge, is provided in Section 4.

Proper ALD of strontium ruthenate, $SrRuO_3$, has not been achieved due to the lack of a self-limiting Ru precursor. However, the deposition of conductive $SrRuO_3$ was achieved by Han *et al.* at Seoul National University by combining SrO and RuO_2 by ALD and pulsed-CVD, respectively, at a low growth temperature of 230 °C.[93] The SrO was deposited from $Sr(^iPr_3Cp)_2$ with O_2 gas as the co-reactant, while RuO_2 was deposited by thermal decomposition of the RuO_4 precursor. The source temperatures for Sr and Ru were held at 110 °C and 3 °C, respectively. For a fixed dosing time of 2 s for the RuO_4 precursor, stoichiometric $SrRuO_3$ was deposited with a cycle ratio of 6:1 (Sr:Ru) with a growth rate of 0.29 nm/subcycle. Films were deposited on Ta_2O_5(8 nm)/SiO_2(100 nm)/Si

and RuO_2(40 nm)/SiO_2(100 nm)/Si substrates. Different crystallization behaviors were observed depending on the substrate, as shown in the glancing angle XRD spectra in Figure 1.5. On the Ta_2O_5 surface, the annealed $SrRuO_3$ has poor crystalline quality even for stoichiometric films. However, on the RuO_2 surface, the annealed $SrRuO_3$ shows a strong (121) reflection at $2\theta \sim 32.2°$ for Sr concentrations between 47% and 59%. No reflection was observed for lower Sr concentrations (< 46%). The as-deposited film showed high resistivity of 35 m**Ω**-cm, but decreased to a minimum of 2.3 m**Ω**-cm upon crystallization into the polycrystalline perovskite phase during post-deposition annealing at 700 °C in N_2 atmosphere. Subsequent deposition of $SrTiO_3$ films on both amorphous and polycrystalline $SrRuO_3$ revealed dielectric constants of k~12 and k~44, respectively. The difference in the dielectric constant of $SrTiO_3$ is associated with the degree of crystallinity in the deposited film on the amorphous versus polycrystalline $SrRuO_3$ layer.

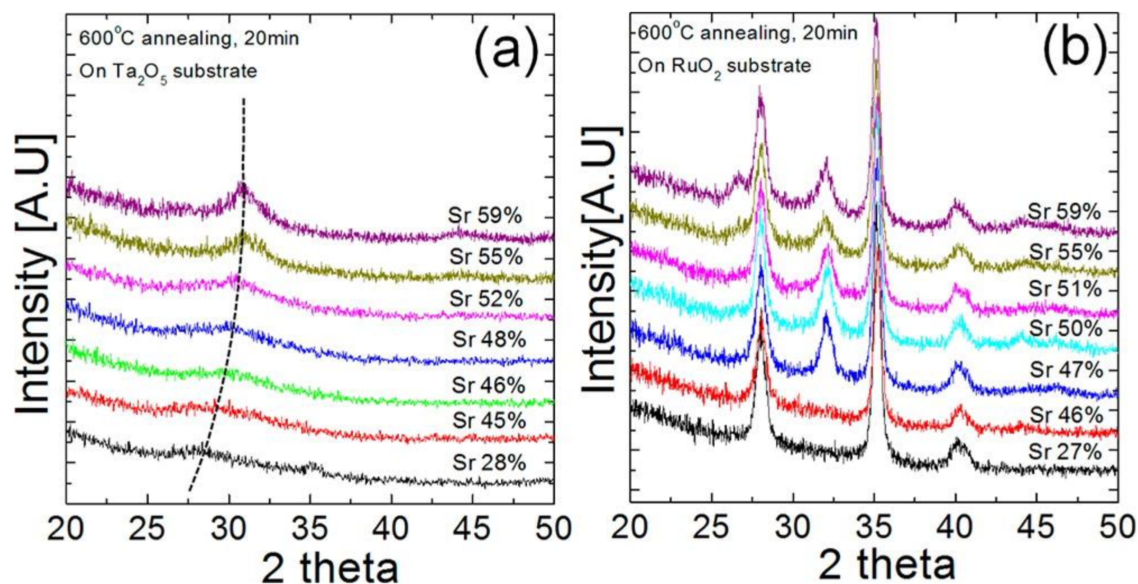


Figure 1.5. Glancing angle XRD spectra of the $SrRuO_3$ films with different Sr concentrations after post-deposition annealing at 600 °C on (a) Ta_2O_5 and (b) RuO_2 substrates. [Reprinted with permission from *Chem. Mater.* **24**, 4686 (2012). Copyright 2012 American Chemical Society.]

1.2.2. Lead-containing perovskite oxides ($PbBO_3$)

Thin films of $PbTiO_3$ and $PbZrO_3$ have attracted attention due to the solid solution of lead zirconate titanate, $Pb(Zr,Ti)O_3$, which has a remarkable piezoelectric response. Integration of $Pb(Zr,Ti)O_3$ thin films on semiconductor substrates can be utilized for ferroelectric random access memory (FeRAM) to enable nonvolatile memory.[8] With current and future generation feature sizes shrinking to increase the FeRAM integration density, growth of the ferroelectric layer by ALD is preferred due to its conformality and precise thickness control. However, there are limited studies on the deposition of quaternary oxide thin films by ALD. Due to the cyclic nature of ALD, there is difficulty in maintaining compositional uniformity throughout the thickness of the film. The increasing complexity of depositing a material such as $Pb(Zr,Ti)O_3$ requires detailed understanding of the deposition characteristics of the parent binary (*e.g.*, PbO, ZrO_2, TiO_2) and ternary (*e.g.*, $PbZrO_3$, $PbTiO_3$) oxides. The deposition of both TiO_2 and ZrO_2 thin films by ALD has been extensively studied for high-k applications;[100-102] whereas, the deposition of PbO by ALD has been limited due to the availability of Pb precursors.[103]

Initial works of lead titanate and lead zirconate

The first reported ALD of lead titanate, $PbTiO_3$, was by Harjuoja *et al.* at the Helsinki University of Technology.[104] Tetraphenyl lead [$Pb(Ph)_4$] was employed as the Pb source at an evaporation temperature of 165 °C, along with $Ti(O^iPr)_4$ as the Ti source evaporated at 40 °C. Ozone and water vapor were used for the co-reactant for $Pb(Ph)_4$ and $Ti(O^iPr)_4$, respectively. The $PbTiO_3$ films were deposited at reactor temperatures of 250 °C and 300 °C on Si (100) substrates. Nearly stoichiometric films were produced for a Pb:Ti cycle ratio of 10:1 and 28:1 when deposited at 250 °C and 300 °C, respectively. Such a high cycle ratio indicates the sluggish kinetics of $Pb(Ph)_4$ despite the use of ozone

as the co-reactant. The $PbTiO_3$ films were amorphous and crystallized into the polycrystalline tetragonal perovskite phase after post-deposition annealing at 600-900 °C in either N_2 or O_2 atmosphere.

Further work by Harjuoja *et al.* reported on the deposition of $PbZrO_3$ using $Pb(Ph)_4$ and $Zr(thd)_4$ with ozone as the co-reactant at 275 °C and 300 °C.[105] The precursors were evaporated inside the reactor at 160 °C and 130 °C for $Pb(Ph)_4$ and $Zr(thd)_4$, respectively. For stoichiometric $PbZrO_3$ films, a Pb:Zr cycle ratio of 3:1 or 7:2 was used at a deposition temperature of 275 °C. At a slightly higher temperature of 300 °C, the Pb:Zr cycle ratio was increased to 6:1 for stoichiometric deposition. The average growth rate of $PbZrO_3$ was 0.15 Å/cycle. Interestingly, films deposited on Si (100) or MgO-buffered Si (100) showed a polycrystalline mix of cubic ZrO_2 and orthorhombic PbO_2 phases without the presence of the $PbZrO_3$ perovskite phase. However, films deposited on single-crystal $SrTiO_3$ (100) were crystallized into the perovskite phase with strong (100) orientation after post-deposition annealing at 600 °C for 10 min in O_2 atmosphere.

A separate study on the ALD of $PbTiO_3$ was reported by Hwang *et al.* at Seoul National University.[106] The precursors used were bis(3-N,N-dimethyl-2-methyl-2-propanoxide) lead [$Pb(dmamp)_2$] and titanium tetra(tert-butoxide) [$Ti(O^tBu)_4$] with water as the co-reactant at a substrate temperature of 200 °C. The Pb and Ti precursors were evaporated at 116 °C and 67 °C, respectively. Thin films of $PbTiO_3$ were deposited on sputtered Ir(100 nm)/IrO_2(30 nm)/SiO_2/Si substrates. Initial growth studies of the binary oxide TiO_2 suggested that $Ti(O^tBu)_4$ has a reduced ALD temperature range (< 200 °C) compared with the more commonly used Ti alkoxides, $Ti(O^iPr)_4$ and $Ti(OMe)_4$. Nevertheless, stoichiometric $PbTiO_3$ films were achieved at a deposition temperature of 200 °C using a Pb:Ti cycle ratio of 3:4. The growth rate of $PbTiO_3$ was 0.64 Å/cycle,

which is notably higher than both PbO (0.1 Å/cycle) and TiO_2 (0.21 Å/cycle) at the same conditions. Seemingly, the TiO_2 surface enhances the deposition rate of PbO using $Pb(dmamp)_2$. The as-deposited $PbTiO_3$ films were amorphous and begin to crystallize into the perovskite structure when annealed for 30 min in O_2 atmosphere at temperatures above 550 °C. Fast annealing rates (~100 °C/min) were necessary for obtaining the pure $PbTiO_3$ perovskite phase without the presence of the pyrochlore or PbO_2 phase. Capacitor structures of a 78 nm $PbTiO_3$ film revealed a peak dielectric constant of k~280 with a remnant polarization of 11.2 μC/cm^2 at an applied voltage of 2.8 eV.

The same group also reported on $PbTiO_3$ deposition using the same Pb precursor, $Pb(dmamp)_2$, with either $Ti(O^iPr)_4$ or $Ti(O^tBu)_4$.[107] This allowed for comparison between the two alkoxide precursors. Once again, the $Ir/IrO_x/SiO_2/Si$ substrate temperature was held at 200 °C and water was used as the co-reactant. The evaporation temperatures for $Pb(dmamp)_2$, $Ti(O^iPr)_4$, and $Ti(O^tBu)_4$ were 126 °C, 65 °C, and 67 °C, respectively. In this work, stoichiometric films were reported for Pb:Ti cycle ratios of 7:4 and 4:5 when using $Ti(O^iPr)_4$ and $Ti(O^tBu)_4$, respectively, with corresponding growth rates of 0.81 Å/cycle and 0.64 Å/cycle, respectively. The $PbTiO_3$ thin films grown using either Ti precursor were amorphous as-deposited and crystallized upon post-deposition annealing at 600 °C for 30 min under O_2 atmosphere. Different surface morphology was observed after post-deposition annealing depending on the Ti precursor used, where films grown with $Ti(O^iPr)_4$ showed the formation of micro-pores and $Ti(O^tBu)_4$ did not. The authors correlate the formation of micro-pores with the higher growth rate of $Ti(O^iPr)_4$ that resulted in less dense films than those grown with $Ti(O^tBu)_4$.

In 2007, the deposition of $PbTiO_3$ was also reported by Watanabe *et al.* at the Center of Nanoelectronic Systems for Information Technology in Germany using a combination of liquid injection ALD of binary TiO_2 and PbO films.[108] The metalorganic

sources were dipivaloylmethanato lead [$Pb(dpm)_2$] and diisopropoxide dipivaloylmethanato titanium [$Ti(O^iPr)_2(dpm)_2$] dissolved in ethylcyclohexane with water as the co-reactant. Thin films of $PbTiO_3$ were deposited at 240 °C on planar Pt-covered and patterned Ir-coated Si substrates. To obtain a Pb:Ti ratio of 1:1, a Pb:Ti cycle ratio of 1:8 was used due to the relatively higher deposition rate of $Pb(dpm)_2$ over $Ti(O^iPr)_2(dpm)_2$ per cycle. The deposition rate of the ternary oxide $PbTiO_3$ was significantly enhanced over the binary ALD processes under the same conditions. Ideal ALD behavior was not achieved for $PbTiO_3$ under the same conditions where self-limiting growth was achieved with the binary oxides of PbO and TiO_2. This indicates the added complexity of surface interactions when depositing multicomponent oxides.

Studies of lead zirconate-titanate (PZT)

Following their initial work on $PbTiO_3$, Watanabe *et al.* deposited $Pb(Zr,Ti)O_3$ using $Pb(dpm)_2$, tetrakis(dipivaloylmethanato) zirconium [$Zr(dpm)_4$], and either $Ti(O^iPr)_2(dpm)_2$ or $Ti(O^iPr)_4$ dissolved in ethylcyclohexane with water as the co-reactant.[109] Once again, the deposition temperature was 240 °C and the dissolved metalorganic precursors were injected into the vaporizer at 200 °C. Thin films were deposited on planar $Pt/TiO_x/SiO_x/Si$ or $Pt/AlO_x/SiO_x/Si$ substrates, as well as patterned Ir-coated Si substrates. Using the $Ti(O^iPr)_2(dpm)_2$, the deposition rate (Å/cycle) of $Pb(Zr,Ti)O_3$ was enhanced by a factor of 2 to 20 times over the binary oxide ALD processes. The deposition rates of Pb and Zr saturated with increasing precursor exposure, while $Ti(O^iPr)_2(dpm)_2$ did not show saturating behavior. To remedy this behavior, the authors examined the pure alkoxide titanium precursor, $Ti(O^iPr)_4$. Unfortunately, saturating behavior was still not observed and the carbon content increased significantly when using $Ti(O^iPr)_4$ due to decomposition of the precursor. The

relative Zr content was quite low in this study due to the poor deposition kinetics of $Zr(dpm)_4$, with an upper limit of about 10% (*i.e.*, $PbZr_{0.1}Ti_{0.9}O_3$). The $Pb(Zr,Ti)O_3$ films were amorphous as-deposited and became weakly polycrystalline after post-deposition annealing in O_2 atmosphere at 400 °C for 30 min followed by 700 °C for 10 min. Electrical measurements did not confirm polarization switching from the polarization-voltage (P-V) hysteresis loop due to the large leakage current. However, some piezoelectric response was observed for the polycrystalline films by piezoelectric force microscopy (PFM).

The same group improved on the deposition of $Pb(Zr,Ti)O_3$ by using an alternative Zr precursor, namely tetrakis(diisobutyrylmethanato) zirconium [$Zr(dibm)_4$].[110] The films were deposited at 240 °C on planar $Pt/AlO_x/SiO_x/Si$ and patterned Ir-coated Si substrates using $Pb(dpm)_2$, $Zr(dibm)_4$, and $Ti(O^iPr)_4$ dissolved in ethylcyclohexane with water as the co-reactant. The higher growth rate of $Zr(dibm)_4$ over $Zr(dpm)_4$ allowed for increased Zr content, up to 50% (*i.e.*, $PbZr_{0.5}Ti_{0.5}O_3$) for a cycle ratio of 1:3:1 (Pb:Zr:Ti). The films appeared amorphous as-deposited and were crystallized in a two-step annealing process as before, 400 °C for 30 min followed by 700 °C for 10 min in O_2 atmosphere. The higher Zr content (x~0.5) reduced the leakage current enough to observe the P-V hysteresis loop at room temperature. The remnant polarization and coercive field were 24 $\mu C/cm^2$ and 200 kV/cm, respectively. Uniform composition and conformal deposition was demonstrated on a hole structure for the as-deposited film, as shown in Figure 1.6. Crystallization did not affect the composition within the hole structure; however, nanosized pores formed during crystallization, especially at the lower part of the hole as can be seen in Figure 1.6(a).

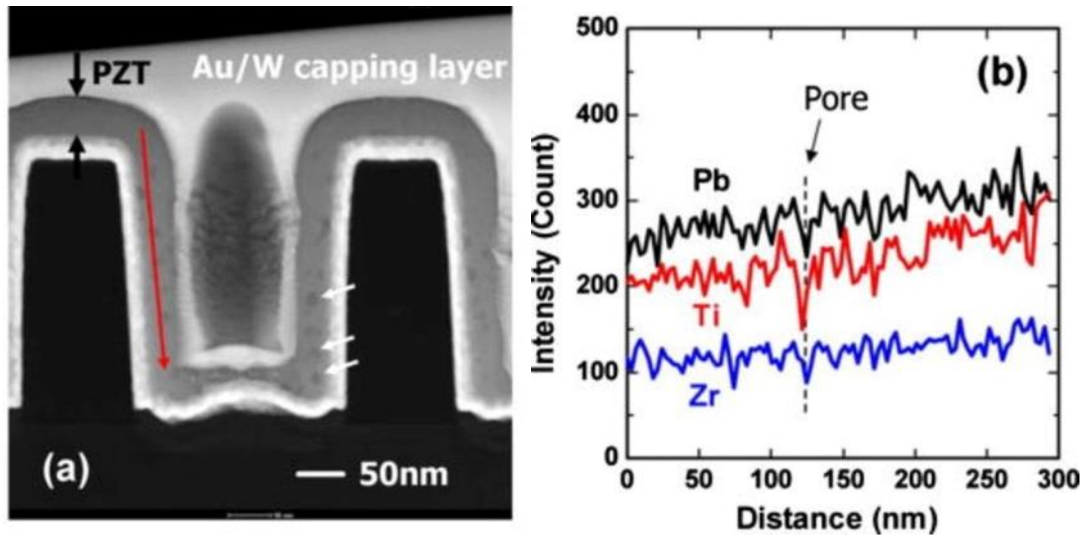


Figure 1.6. (a) STEM cross-sectional image of a PZT film deposited on a hole structure with a diameter of about 0.28μm after annealing at 400°C for 30min and at 700°C for 10min and (b) EDS line-scan profiles at specific positions shown in (a).[108] [Reprinted with permission from *J. Electrochem. Soc.*, **155**, D715 (2008). Copyright 2008, The Electrochemical Society.]

In 2011, Zhang *et al.* at the University of California, Los Angeles (UCLA) reported the ALD of $Pb(Zr,Ti)O_3$ thin films using the traditional β-diketonate lead precursor, $Pb(thd)_2$.[111] The deposition temperature was 250 °C using $Pb(thd)_2$, $Ti(O^iPr)_2(thd)_2$, and zirconium chloride [$ZrCl_4$] with water as the co-reactant. The $Pb(Zr,Ti)O_3$ films were deposited on n-type 4H-SiC (0001) substrates with a 10 nm capping layer of Al_2O_3 deposited by ALD. A cycle ratio of 2:1:1 (Pb:Zr:Ti) was used to obtain optimal piezoelectric performance. The deposited films were amorphous but crystallized into the perovskite phase by rapid thermal annealing at 950 °C for 3 min in N_2 atmosphere. The film composition nearly matched the cycle ratio, leading to a crystallized perovskite film consistent with $PbZr_{0.44}Ti_{0.56}O_3$. MOS capacitor structures revealed an effective dielectric constant of k~50 for a 10 nm $Pb(Zr,Ti)O_3$ film. A low leakage current of 5.5×10^{-6} A/cm^2 at an applied field of 8 MV/cm was demonstrated for a

14 nm $Pb(Zr,Ti)O_3$ film. P-V hysteresis loops were measured at different applied voltages. The remnant polarization, saturation polarization, and coercive field increased with increasing applied voltage from 0-20 V. For 6 nm to 14 nm $Pb(Zr,Ti)O_3$ thicknesses, the remnant polarization increased from 1.3 to 4.3 $\mu C/cm^2$, respectively. PFM image of a polarized $Pb(Zr,Ti)O_3$ film at ± 12 V showed a piezoelectric response of ± 2 mV.

Recent work from the same group at UCLA reported on the deposition of $Pb(Zr,Ti)O_3$ using an alternative Zr precursor, $Zr(thd)_4$, eliminating potential for chlorine contamination.[112] Their goal was to quantify the incubation time for depositing one constituent metal oxide on another using *in situ* FTIR. The films were deposited on Si or Al_2O_3(10 nm)/4H-SiC substrates at 250 °C using $Pb(thd)_2$, $Zr(thd)_4$, and $Ti(O^iPr)_2(thd)_2$ heated to 140, 190, and 100 °C, respectively, with water as the co-reactant. The deposition conditions were set to meet the desired stoichiometry of $PbZr_{0.5}Ti_{0.5}O_3$ for optimal ferroelectric properties. The cycle ratio (Pb:Zr:Ti) to obtain the desired stoichiometry was dependent on the substrate and post-deposition annealing conditions. The so-called incubation times were found between one and four ALD cycle for one constituent metal oxide on another. For example, the incubation period for TiO_2 deposited on PbO required only two ALD cycles compared to four ALD cycles for ZrO_2 on PbO. To avoid interfacial reaction between the $Pb(Zr,Ti)O_3$ film and the Si substrate, a thin Al_2O_3 buffer layer was employed. The desired $Pb(Zr,Ti)O_3$ films were deposited with a cycle ratio of 16:4:7 (Pb:Ti:Zr) and were crystallized into the perovskite structure at temperatures above 600 °C. The piezoelectric properties were studied for a 15 nm $Pb(Zr,Ti)O_3$ film. Again, the remnant polarization, saturation polarization, and coercive field were 1.1 $\mu C/cm^2$, 8.5 $\mu C/cm^2$, and 0.32 MV/cm, respectively, while increasing with applied voltage in the range of ± 20 V.

1.2.3. La-based ternary oxides ($LaBO_3$)

La-based perovskite thin films have attracted much attention recently because of their wide range of properties, such as high-*k* insulating,[54,113-117] conductive,[118-120] antiferromagnetic,[121] and ferromagnetic.[55,122] Lanthanum oxide, La_2O_3, itself is a high-*k* dielectric with a dielectric constant in the range of 20-27.[113,123] However, it is moisture-sensitive and becomes unsuitable for large-scale processes. The dielectric constant of La_2O_3 could increase if it is mixed with some of other oxides forming a perovskite-type structure. It is often mixed with aluminum oxide, Al_2O_3, forming lanthanum aluminate, $LaAlO_3$, which has high immunity against moisture and is more thermally stable in contact with Si compared to La_2O_3.[124] Epitaxial $LaAlO_3$ has a dielectric constant in the range of 25-30, a wide band gap (E_g=5.6 eV), and high band offsets with respect to Si.[113] Therefore, $LaAlO_3$ has been proposed as an alternative to HfO_2 as a high-*k* dielectric material.

Other La-based perovskites, such as $LaYO_3$ and $LaLuO_3$, have also been proposed as alternative high-*k* materials.[116,117,125] La_2O_3 may also be mixed with CoO to form the perovskite $LaCoO_3$, a ferromagnetic oxide that can be monolithically integrated directly on silicon.[55,122] In addition, epitaxial thin films of $(La,Sr)TiO_3$ may serve as a conductive template layer on silicon.[50,58] La-based perovskites, such as $LaGaO_3$, have proven to be suitable substrates for high-temperature superconducting materials.[126,127] The majority of La-based perovskite thin films have been grown by physical vapor deposition methods, such as PLD and MBE. Recent advancements in volatile La precursors have provided additional opportunity to explore the ALD of La-based perovskite thin films,[128,129] especially for applications requiring stringent control of composition and conformality.

Lanthanum aluminate ($LaAlO_3$)

Lanthanum aluminate, $LaAlO_3$, has been one of the most widely studied for La-based perovskites. There has been a considerable amount of work on $LaAlO_3$ thin films grown using both physical and chemical deposition methods, such as MBE,[54,130,131] PLD,[132-134] sputtering,[135,136] and CVD.[137-140] Because of film thickness controllability, uniformity across the wafer, low deposition temperature, and scalability, ALD is a very attractive method for depositing 3-D transistor advanced gate oxides and DRAM insulators. The ALD growth of $LaAlO_3$ has been reported using different types of La precursors, including lanthanum β-diketonates, silylamides, cyclopentadienyls, and amidinates.[56,115,128,141-149] Of these studies, trimethylaluminum [$Al(CH_3)_3$] has been the most common precursor for aluminum owing to its superb ALD behavior.[13,14] The co-reactant used for $LaAlO_3$ growth was either ozone or water, depending on the precursor type. Generally, the β-diketonates have lower reactivity and require a stronger co-reactant, such as ozone.

In 2001, M. Nieminen *et al.* at the Helsinki University of Technology reported the first ALD growth of $LaAlO_3$ using the traditional β-diketonate precursor, $La(thd)_3$.[141] As typical for these precursors, ozone was used as the oxidant since the reactivity of $La(thd)_3$ with water is limited. Thin films of $LaAlO_3$ were deposited on soda lime glass, Si (001), MgO-buffered Si (001) and $SrTiO_3$ substrates using $La(thd)_3$ and $Al(acac)_3$, with O_3 as the co-reactant. The La and Al precursors were evaporated inside the reactor at temperatures of 170 °C and 125 °C, respectively. The influence of the La:Al cycle ratio in the temperature range of 325-400 °C was explored in detail. The growth rates at different temperatures were found to be constant at low La:Al cycle ratios. The growth rate of $LaAlO_3$ decreases with an increase of the relative number of La subcycles was observed. At higher La:Al cycle ratio, a small increase in the growth rate was observed.

The phenomenon was explained by the adsorption of the La precursor, where the Al–O layer diminishes the growth rate of the following La–O layer because the surface sites are not favorable for the adsorption of $La(thd)_3$. Stoichiometric films were obtained using a La:Al cycle ratio of 1.75–2.0. The ALD-grown $LaAlO_3$ films on Si (001) annealed in N_2 atmosphere at 800 °C and 850 °C remained amorphous, while the films annealed at 900 °C for 10 min produced polycrystalline $LaAlO_3$ films. The (110) orientation is preferred if the annealing time increased to 30 min with a slow heating and cooling rate (1 °C/min) for the $LaAlO_3$ films grown on Si (001). The $LaAlO_3$ films grown on MgO-buffered Si (001) show preferred orientation after annealing at 900 °C in a N_2 atmosphere, while the $LaAlO_3$ films grown on $SrTiO_3$ were crystallized with epitaxial alignment after annealing at 900 °C for 30 min.

Sønsteby *et al.* at the University of Oslo reported on epitaxial $LaAlO_3$ thin films grown using the same precursors on $SrTiO_3$ and $LaAlO_3$ substrates, as well as amorphous $LaAlO_3$ films grown on Si (100), soda lime glass, and MgO. The metalorganic sources were $La(thd)_3$ and $Al(CH_3)_3$, with O_3 as the co-reactant at a deposition temperature of 250 °C. Stoichiometric films were achieved using a La:Al cycle ratio of 1:1 despite the large difference in growth rate for the binary oxides of La_2O_3 and Al_2O_3. The growth rate of $LaAlO_3$ films varied between 0.37-0.64 Å/cycle depending on the subcycle mixing conditions. For $LaAlO_3$ thin films grown on $SrTiO_3$ and $LaAlO_3$ substrates, post-deposition annealing at 650 °C for 30 min in O_2 atmosphere was used to crystallize the $LaAlO_3$ with epitaxial registry to the underlying substrate. $LaAlO_3$ films grown on Si and MgO substrates remained amorphous after annealing at 650 °C for 30 min.

The limited reactivity of $La(thd)_3$ with water was overcome by the development of transition metal amidinate precursors by the Gordon group at Harvard University.[42,43] In 2004, Lim *et al.* reported on the growth of $LaAlO_3$ using tris(N,N'-

diisopropylacetamidinate) lanthanum [La(^{i}Pr$_2$-amd)$_3$] and $Al(CH_3)_3$, with water as the co-reactant. The La precursor was held at a temperature of 130 °C, with $Al(CH_3)_3$ and water were held at room temperature. The $LaAlO_3$ films were deposited on HF-etched Si substrates at a deposition temperature of 300-330 °C. Using a La:Al cycle ratio of 1:1 and 3:1, yielded a film composition of $La_{0.5}Al_{1.5}O_3$ and $La_{0.9}Al_{1.1}O_3$, respectively. The films were smooth and amorphous as-deposited, with less than 1 at.% carbon impurity. The growth rate of the $LaAlO_3$ film was approximately 0.94 Å/subcycle for a 1:1 (La:Al) cycle ratio. As expected, the dielectric constant increases with increasing La content. The dielectric constant of a thin (9.8 nm) $La_{0.9}Al_{1.1}O_3$ film was k~13 (EOT = 2.9 nm). The amorphous, as-deposited films had a low leakage current of $< 5\times10^{-8}$ A/cm^2 at 1 MV/cm. No post-deposition annealing was attempted to crystallize the films.

In 2007, Li *et al.* reported on the deposition of $LaAlO_3$ using lanthanum tris(N,N'-diisopropylformamidinate) [La(^{i}Pr$_2$-famd)$_3$], $Al(CH_3)_3$, and water.[128] Among the lanthanum amidinates, La(^{i}Pr$_2$-famd)$_3$ was reported as the most volatile lanthanum precursor, with a vapor pressure of 60 mTorr at 100 °C, approximately 60 times higher than the β-diketonate complex, $La(thd)_3$. $LaAlO_3$ thin films were deposited at a substrate temperature of 300 °C. The films are amorphous as-deposited and remain amorphous even after annealing up to 800 °C for 30 s in N_2 atmosphere. As-deposited films were found to have a dielectric constant of k~14 and a low leakage current of 9.3×10^{-9} A/cm^2 at -1 V with an EOT of 3.15 nm. The impact of low temperature O_2 on the electrical properties of $LaAlO_3$ was explored by Liu *et al.* using the same La and Al precursors.[146] The La(^{i}Pr$_2$-famd)$_3$ source was held at 120 °C, while $Al(CH_3)_3$ and water were again kept at room temperature. Nearly stoichiometric films of $La_{1.1}Al_{0.9}O_3$ were produced using a La:Al cycle ratio of 2:1. The growth rate was 0.93 Å/subcycle at the given conditions with carbon and nitrogen contamination below 1 at.%. Capacitor structures were created

for $LaAlO_3$ films between 5 and 10 nm in thickness. The dielectric constant of the as-deposited films was found to be *k*~15. Post-deposition annealing at 300 °C for 10 min in O_2 atmosphere helped to reduce the interface trap density and leakage current density. The estimated trap density in the as-deposited film is 3.5×10^{12} cm^{-2} eV^{-1}, while the estimated trap density after annealing in O_2 was lowered to 6×10^{11} cm^{-2} eV^{-1}. The leakage current density reduced from 1.1×10^{-4} A/cm^2 to 1.6×10^{-5} A/cm^2 at 1 V bias with an EOT of 2.2 nm.

The formation of epitaxial $LaAlO_3$ on $SrTiO_3$-buffered Si (001) and single-crystal $SrTiO_3$ substrates was also reported by our group using $La(^iPr_2\text{-famd})_3$, $Al(CH_3)_3$, and water.[56,150] A thin (4-unit-cell) $SrTiO_3$ buffer layer was grown on Si (001) by MBE and then transferred *in situ* to the ALD for $LaAlO_3$ deposition. To obtain nearly stoichiometric to slightly La-rich films, a La:Al cycle ratio of 3:2 was used at a deposition temperature of 250 °C. The growth rate was 1.0 Å/subcycle when using a 3:2 (La:Al) cycle ratio. The as-deposited $LaAlO_3$ films on $SrTiO_3$-buffered Si (001) were amorphous and still remained amorphous after a vacuum anneal for 2 h at 550 °C. However, they became crystalline and epitaxial after a vacuum anneal at 600 °C for 2 h. The formation of amorphous interlayer between $SrTiO_3$ and Si was minimized by using the combined MBE-ALD technique. The formation of epitaxial $LaAlO_3$ thin films on single-crystal $SrTiO_3$ was compared for reference. A higher crystallization temperature (750 °C for 2 h in vacuum) was required on the single-crystal substrate versus the $SrTiO_3$-buffered Si. The higher temperature required for crystallization was explained by the larger mismatch between $LaAlO_3$ and $SrTiO_3$ versus Si substrates.

Lanthanum tris(bis(trimethylsilyl)amide) [$La(N(SiMe_3)_2)_3$] has also been reported in several works as an ALD precursor for $LaAlO_3$.[145,151,152] Triyoso *et al.* at Freescale Semiconductor reported on the growth of $LaAlO_3$ on Si substrates by ALD using

$La(N(SiMe_3)_2)_3$, $Al(CH_3)_3$, and water.[151] The La precursor was held at 180 °C, while the $Al(CH_3)_3$ and water were at room temperature. The deposition temperature varied from 200-300 °C, with self-limiting growth behavior between 225-275 °C. A significant amount of Si impurity was reported for films grown at 225 °C, with approximately equal amounts of Al and Si. Further development of $LaAlO_3$ deposition using the same precursors was reported by Kukli *et al.* at the University of Helsinki.[145] Nearly stoichiometric films were achieved using a La:Al cycle ratio of 8:1 at a deposition temperature of 225 °C. The $La(N(SiMe_3)_2)_3$ evaporation temperature was kept above 125 °C (typically 140 °C) for sufficient vapor pressure to stabilize the ALD growth behavior. Using auger electron spectroscopy, the $LaAlO_3$ film was found to have a smaller Si impurity (3 at.%) than reported previously. However, the authors conclude that the ALD growth using these precursors is not reproducible due to considerable variance in the growth rates with deposition parameters. As follow-on work, Triyoso *et al.* compared the growth of $LaAlO_3$ films deposited by ALD and MBE.[152] The same precursors were used as before at a deposition temperature of 225-275 °C, with the $La(N(SiMe_3)_2)_3$ held at 180 °C. The $LaAlO_3$ films were found to be stable against Pt and TiN/W metal gates when annealed to 800 °C for 1 min in N_2 atmosphere. The authors conclude that there is clear interaction between the deposited film and substrate; therefore, $La(N(SiMe_3)_2)_3$ is not a suitable precursor for the deposition of gate dielectrics on silicon.

The ALD growth of $LaAlO_3$ was also performed using tris(isopropylcyclopentadienyl) lanthanum [$La(^iPrCp)_3$] and $Al(CH_3)_3$ as the La and Al precursors, respectively.[115,147,148] In 2008, Eom *et al.* at the Seoul National University reported on the post-deposition annealing effects of $LaAlO_3$ thin films (5-6 nm) on silicon using water as the co-reactant.[147] The $La(^iPrCp)_3$ and $Al(CH_3)_3$ precursors were held at 150 °C and room temperature, respectively. The substrate temperature was varied

from 176 °C to 380 °C during growth, and the films were post-deposition annealed at 800 °C for 30 s in N_2 atmosphere. Regardless of the deposition temperature, post-deposition annealing resulted in significant Si diffusion into the $LaAlO_3$ layer that formed a thin silicate layer. The Si diffusion resulted in La and Al counter diffusion, where Al migrated towards the surface and La migrated to the interface. Further analysis of the high-temperature annealing of $LaAlO_3$ thin films (5-30 nm) on silicon was reported by Congedo *et al.* using the same La and Al precursors with O_3 as the co-reactant. Once again, Si diffusion into the $LaAlO_3$ layer was observed after post-deposition annealing at 900 °C for 60 s in N_2 atmosphere, resulting in the formation of an amorphous La-aluminosilicate ($LaAlSi_2O_5$).

More recently, Sbrockey *et al.* (2012) reported on the growth epitaxial $LaAlO_3$ thin films on TiO_2-terminated $SrTiO_3$ single-crystals using $La(^iPrCp)_3$ and $Al(CH_3)_3$, with water as the co-reactant.[148] The La source was held at 150 °C, while $Al(CH_3)_3$ and water were held at room temperature. At a deposition temperature of 300 °C, nearly stoichiometric $LaAlO_3$ films were grown using a La:Al cycle ratio of 4:1 and 5:1. The growth rate did not saturate with increasing La pulse length, meaning the growth of $LaAlO_3$ was not self-limiting using the $La(^iPrCp)_3$ precursor. However, at fixed pulse lengths for La and Al, the growth was ~0.28 Å/subcycle using a La:Al cycle ratio of 5:1. The $LaAlO_3$ films were amorphous as-deposited, and crystallized after annealing at 900 °C for 60 min in air with epitaxial registry to the $SrTiO_3$ substrate.

Other high-k La-based perovskites ($LaBO_3$)

Thin films of lanthanum lutetium oxide, $LaLuO_3$, deposited by ALD have been explored as gate dielectrics for Si, Ge, and GaAs.[116,117,125,153] In 2008, Roeckerath *et al.* at the Jülich Research Center (Germany) provided the first ALD study of $LaLuO_3$ using

traditional β-diketonate precursors, $La(thd)_3$ and $Lu(thd)_3$, with O_3 as the co-reactant.[153] Thin films were deposited on Si substrates at a temperature of 300 °C. The as-deposited $LaLuO_3$ films were amorphous with an excess of oxygen (*i.e.*, $LaLuO_{5.2}$) and a dielectric constant of k~17. The films remained amorphous even after annealing up to 1000 °C for 10 s in N_2 atmosphere. However, post-deposition annealing at 800 °C for 5 min in O_2 atmosphere crystallized the film into the orthorhombic $LaLuO_3$ phase. The O_2 anneal also reduced the oxygen content to a composition of $LaLuO_{3.6}$ with a corresponding increase in the dielectric constant to k~30. In this case, the increase in dielectric constant appears to be associated with the transition from amorphous to polycrystalline $LaLuO_3$.

More recently, La amidinate precursors have been used for the deposition of lanthanum lutetium oxide, $LaLuO_3$.[116,117,125] Wang *et al.* at Harvard University reported on the deposition of $LaLuO_3$ on Si (001) substrates using $La(^iPr_2\text{-famd})_3$ and tris(N,N'-diethylformamidinate) lutetium [$Lu(Et_2\text{-famd})_3$], with water as the co-reactant.[116] Stoichiometric films are amorphous as deposited at 300 °C using a La:Lu cycle ratio of 1:1. The extracted dielectric constant of amorphous $LaLuO_3$ was k~28, indicating the amidinate precursors provide an advantage over the β-diketonates. Later work by Liu *et al.* demonstrated that $LaLuO_3$ can be grown epitaxially on sulfur-passivated GaAs (111) using the same precursor system at an elevated temperature of 350 °C.[117] This work is discussed further in Section 3 regarding the monolithic integration of oxides on semiconductors. In other work by Gu *et al.*, $LaLuO_3$ was investigated as a gate dielectric for germanium using a Ge-on-insulator (GeOI) substrate.[125] $LaLuO_3$ thin films (5 nm) were deposited at 350 °C using La and Lu amidinate precursors, $La(amd)_3$ and $Lu(amd)_3$. A thermal GeO_2 passivation layer (1.5 nm) was utilized to improve the on-state current and effective hole mobility for p-channel MOSFET devices. A maximum drain current

of 125 μA/μm for a 2 μm device and a maximum effective hole mobility of 260 cm^2/V-s at room temperature was demonstrated.

The deposition of lanthanum yttrium oxide, $LaYO_3$, on Si (100) substrates was also reported by Wang *et al.* using La(^{i}Pr_2-famd)$_3$ and yttrium tris(N,N'-diisopropylacetamidinate) [Y(^{i}Pr_2-amd)$_3$] with water as the co-reactant.[116] The deposition temperature was 280 °C. Using a La:Y cycle ratio of 1:1, produced a composition of $La_{1.23}Y_{0.77}O_3$. Nearly stoichiometric films of $LaYO_3$ may be obtained using a La:Y cycle ratio of 2:3. In contrast to the amorphous as-deposited $LaLuO_3$ thin films, as-deposited $La_xY_{2-x}O_3$ films on Si show a polycrystalline structure over an amorphous layer (3-7 nm). Capacitor structures of $La_{1.23}Y_{0.77}O_3$ revealed a dielectric constant of k~17, which is lower than $LaLuO_3$ films deposited in the same manner. Further characterization of stoichiometric $LaYO_3$ was not reported.

Additional works on La-based perovskites

Thin films of lanthanum cobaltate, $LaCoO_3$, have been explored for use as a ferromagnetic oxide that can be monolithically integrated directly on silicon.[55,122] The deposition of $LaCoO_3$ thin films was first reported by Seim *et al.* (1997) at the Helsinki University of Technology using β-diketonate precursors, La(thd)$_3$ and Co(thd)$_2$, with ozone as the co-reactant. The La and Co sources were evaporated at 190 °C and 100 °C, respectively. The $LaCoO_3$ films were deposited on soda lime and Corning 7059 glass at temperatures between 200-400 °C. One supercycle of $LaCoO_3$ consisted of 15 La subcycles followed by 15 Co subcycles. The mean growth rate was 0.35 Å/subcycle (10.5 Å/supercycle). Carbon content on the surface and in the bulk was measured to be 2–3 at.% and below 0.5 at.%, respectively. Films deposited at 350 °C or lower were

amorphous, but crystallized in the perovskite structure after post-deposition annealing at 600 °C for 12 h in air.

In the same year, Seim *et al.* also reported on the deposition of lanthanum nickelate, $LaNiO_3$, using $La(thd)_3$ and $Ni(thd)_2$ with ozone as the co-reactant.[154] $LaNiO_3$ is a conducting perovskite that may be integrated with other layers in a functional oxide heterostructure. Thin films of $LaNiO_3$ were deposited on Corning 7059 glass substrates at a temperature range of 150-450 °C, achieving saturated ALD growth between 215-250 °C. The $LaNiO_3$ thin films were amorphous as-deposited and crystallized into the polycrystalline cubic perovskite phase (a = 3.809 Å) after annealing at 600 °C for 12 h in O_2 atmosphere. Similar to the previous $LaCoO_3$ growth, one supercycle of $LaNiO_3$ consisted of 15 La subcycles followed by 15 Ni subcycles. The mean growth rate was 0.08 Å/subcycle (2.4 Å/supercycle) in the temperature range of 215-250 °C. The resistivity of the $LaNiO_3$ thin films was reduced by five orders of magnitude after crystallization from 3.2 Ω-m for amorphous $LaNiO_3$ down to 1.8×10^{-5} Ω-m for polycrystalline films.

The deposition of lanthanum manganite, $LaMnO_3$, was reported by Nilsen *et al.* at the University of Oslo in 1999.[155] The structure and magnetic ordering of undoped $LaMnO_3$ has been well established.[156] In addition, $La_{1-x}A_xMnO_3$ (where A is a divalent cation: Ca, Ba, Sr, Pb, Cd) or vacancies introduced at the La sites show colossal magnetoresistance (CMR) properties.[157] For ALD deposition, the traditional β-diketonate precursors, $La(thd)_3$ and $Mn(thd)_3$, were again used with ozone as the co-reactant. The La and Mn sources were evaporated at a temperature of 175 °C and 115 °C, respectively. The films were grown on Si (100), soda lime, and aluminum foil at temperatures between 200-400 °C, where ALD behavior was observed between 250-300 °C. Nearly stoichiometric $LaMnO_3$ films were obtained using a La:Mn cycle ratio of 1:1 at

temperatures above 250 °C, while films became more Mn-deficient at temperatures below 250 °C. Amorphous $LaMnO_3$ films were formed at a temperature of 250 °C, while the deposition of polycrystalline requires temperatures higher than 350 °C. In later works, substituted $LaMnO_3$ films of $La_{1-x}Ca_xMnO_3$ and $La_xSr_{1-x}MnO_3$ were reported by Nilsen *et al.* (2007) and Holme *et al.* (2008).[78,97] Calcium-substituted lanthanum manganite, $La_{1-x}Ca_xMnO_3$, was deposited using the traditional β-diketonates of $La(thd)_3$, $Ca(thd)_2$, and $Mn(thd)_3$ with ozone as the co-reactant.[78] In contrast, lanthanum-substituted strontium manganite, $La_xSr_{1-x}MnO_3$, was deposited from Cp-based chemistries using $La(Me_4Cp)_3$, $Sr(^nPrMe_4Cp)_2$, $Mn(Me_4Cp)_2$, and water as the co-reactant.[97]

Lanthanum gallate, $LaGaO_3$, is another important perovskite that may be used as a substrate for the growth of crystalline high-temperature superconductors.[126,127] $LaGaO_3$ has also been doped with Sr at the A-site and Mg at the B-site exhibiting high oxygen ion conductivity.[158] Thin films of $LaGaO_3$ were deposited by Nieminen *et al.* (2001) at the Helsinki University of Technology using $La(thd)_3$ and $Ga(acac)_3$ with ozone as the co-reactant.[159] The films were grown on soda lime glass, Si (001), MgO-buffered Si (001), MgO (100), $SrTiO_3$ (100) and $LaAlO_3$ (100) substrates at temperatures between 325-425 °C. Stoichiometric $LaGaO_3$ films were deposited at a temperature range of 350–390 °C using a La:Ga cycle ratio of 5:2, with a mean growth rate of 0.38-0.40 Å/cycle. Stoichiometric films contained less than 0.4 at.% carbon impurity. The as-deposited $LaGaO_3$ films were amorphous and required a post-deposition annealing for crystallization. Using Si (001) and MgO-buffered Si (001) substrates, the films were crystallized into the $La_4Ga_2O_9$ phase upon annealing at 850 °C for 10 min in N_2 atmosphere. However, using MgO (100) substrates, the films crystallized into the $LaGaO_3$ phase with (112) preferred orientation after annealing at 850 °C in N_2

atmosphere. Finally, using the lattice-matched substrates of $SrTiO_3$ (100) and $LaAlO_3$ (100), the films were crystallized into the $LaGaO_3$ phase with epitaxial alignment to the substrate upon annealing at 850 °C and above for 10-30 min in N_2 atmosphere. Thus, depositing on the lattice-matched perovskite substrates provides an appropriate template to grow single-crystal $LaGaO_3$ thin films.

Lanthanum ferrite, $LaFeO_3$, is a strong material candidate for solid oxide fuel cell cathodes.[160,161] Thin films of $LaFeO_3$ and lanthanum strontium ferrite, $La_{1-x}Sr_xFeO_3$, were reported by Lie *et al.* (2009) at the University of Oslo using $La(thd)_3$, $Sr(thd)_2$, and $Fe(thd)_3$ with ozone as the co-reactant.[76] Saturative ALD behavior was observed for $LaFeO_3$ films grown between 200-360 °C. At 260 °C, nearly stoichiometric $LaFeO_3$ films were achieved using a La:Fe cycle ratio of 2:3. The $LaFeO_3$ films on Si (001) and soda-lime glass substrates were amorphous as-deposited, but crystallized after annealing at 600 °C for 30 min in O_2 atmosphere. Thin films of $LaFeO_3$ were also deposited on single-crystal substrates of $LaAlO_3$ (012), $SrTiO_3$ (100), and MgO (100) at a temperature of 285 °C. The as-deposited films on $LaAlO_3$ (012) were amorphous and crystallized with (110) preferred orientation due to the in-plane lattice matching. The post-deposition annealed films were dominated by crystals with (110) orientation. The incorporation of Sr to form $La_{1-x}Sr_xFeO_3$ was possible, but again with added complexity as seen with the previous study on $La_{1-x}Ca_xMnO_3$.

Lanthanum titanate, $LaTiO_3$, is another interesting perovskite compound for the application of 2DEG materials in oxide heterostructures.[162-164] The deposition of $LaTiO_3$ was reported Aaltonen *et al.* (2010) at the University of Oslo using $La(thd)_3$ and $TiCl_4$ with ozone and water as the co-reactant, respectively.[165] The β-diketonate, $La(thd)_3$, source was held at 185 °C, while the $TiCl_4$, ozone, and water were at room temperature. The $LaTiO_3$ thin films were deposited at a temperature of 225 °C. Lanthanum lithium

titanate films, $La_{2/3-x}Li_{3x}TiO_3$, were also deposited by introducing a Li source, lithium *tert*-butoxide [LiO^{t}Bu], and water into the ALD supercycle.[165] In general, the perovskite-type structure is exhibited for $La_{2/3-x}Li_{3x}TiO_3$ with $x < 0.16$, which is a desirable material for solid-state lithium batteries.[166] The film composition obtained in the reported work was $Li_{0.32}La_{0.30}TiO_z$. The films crystallized after post-deposition annealing at 800 °C for 3 h in O_2 atmosphere.

1.2.4. Rare-earth scandates (RScO3)

Thin films of rare-earth scandates ($RScO_3$, where R = rare-earth metal) have recently gained attention because of the possibility of using them as high-k gate dielectrics to replace SiO_2 in Si MOSFETs.[167] The scandates have the combination of high dielectric constant and low leakage required of gate dielectrics. In addition, unlike perovskite titanates, they have very large band offsets to silicon in both the valence and conduction bands and are thermally stable to very high temperatures (~900°C).[168] Furthermore, unlike the current high-k material HfO_2, most of the scandates do not crystallize when subjected to prolonged high temperatures when they are grown as amorphous layers.[169] Scandates have also recently been grown as bulk single crystals and are now commercially available as substrates for epitaxial thin film growth of other perovskites.[170,171] Their lattice constants range from 3.93 Å ($HoScO_3$) to 4.05 Å ($LaScO_3$), which make them excellent substrates of choice for straining (mostly tensile) of other functional perovskite oxides. Thin film scandates (in particular $YScO_3$ and $LaScO_3$) were previously grown using sputtering or electron-beam evaporation from the oxide.[172,173] However, these early films are more appropriately characterized as solid solutions of amorphous Y_2O_3 and Sc_2O_3. There is also an additional ternary phase R_3ScO_6 with rhombohedral structure that competes with $RScO_3$ formation making

stoichiometric control important. More recent works have used metal-organic CVD to deposit thin film scandates, such as $DyScO_3$ and $GdScO_3$, demonstrating a high dielectric constant ($k > 20$) and low leakage currents.[174,175] Current microelectronic demands of conformality and thickness control make ALD the most viable deposition technique for integrating scandate thin films into modern semiconductor devices.

The first ALD-grown film of yttrium scandate, $YScO_3$, was reported in 2005 by Myllymäki at the Helsinki University of Technology.[176] The authors investigated the effect on ALD growth when using two different classes of precursors. The first set of precursors used were traditional β-diketonate precursors of both yttrium and scandium, namely $Y(thd)_3$ and $Sc(thd)_3$. The second set of precursors were from the cyclopentadienyl (Cp) family, specifically tris(methylcyclopentadienyl) yttrium [$Y(MeCp)_3$] and tris(cyclopentadienyl) scandium [$Sc(Cp)_3$]. For the β-diketonate precursors, ozone was used as the co-reactant, while for the Cp precursors, water was used. Ultrahigh purity nitrogen was utilized as the carrier and purge gas for both types of precursor. The scandate films were grown on either Si (001) with native oxide or on soda lime glass with the reactor pressure maintained at 2-3 mbar. For $Y(thd)_3$ and $Sc(thd)_3$, the reactor temperature was maintained at 335-350 °C. In the case of the Cp-based process, the reactor temperature was kept slightly lower at 300 °C. The growth behavior for the β-diketonate precursors was consistent with ALD-type growth where the growth rates are mostly independent of the number of cycles. The total growth rate for Y:Sc atomic ratio of 1:1 was found to be 0.18 Å per cycle for both 335 °C and 350 °C. For the Cp-based process, the total growth rate at 300 °C with an Y:Sc ratio of 1:1 was found to be 1.07 Å per cycle. Film composition was measured using x-ray fluorescence. To achieve stoichiometric film growth (Y:Sc ~1:1), the Y:Sc cycle ratio was 10:11 for the β-diketonate precursors and 6:5 for the Cp-based chemistries. A more precise chemical

analysis using elastic recoil detection analysis showed hydrogen impurities of < 0.8% and carbon impurities of < 0.2% for both precursors. XRD analysis shows as-grown films were amorphous. For $YScO_3$ films growth with β-diketonate precursors, crystallization occurred after annealing to 1000 °C; however, the diffraction pattern shows a mixture of Y_2O_3 and Sc_2O_3 rather than the perovskite phase of $YScO_3$. A similar behavior is observed for films deposited with the Cp-based chemistry, but with crystallization occurring at 800 °C.

In 2007, the same group reported on the ALD growth of $GdScO_3$ using the β-diketonate precursors, $Gd(thd)_3$ and $Sc(thd)_3$, with ozone as the co-reactant.[177] The growth was done at a reactor temperature of 300 °C with a Gd:Sc cycle ratio of 5:6, resulting in a mean growth rate of 0.21 Å/subcycle. The composition was determined by XRF and RBS to be close to 1:1. The substrate used was silicon in which the native oxide was removed by dipping in hydrofluoric acid. After film growth, cross-section TEM shows only a very thin SiO_x layer (~1 nm) present between the Si substrate and $GdScO_3$ overlayer. The as-grown films were amorphous and remained amorphous up to 900 °C annealing temperature. Annealing to 1000 °C caused the film to crystallize with perovskite structure (random polycrystalline). Electrical measurements showed very low leakage with a dielectric constant of k~22.

The ALD growth of $GdScO_3$ (2006) and $LaScO_3$ (2009) was reported by the Gordon group at Harvard University.[116,178] They use amidinate-based precursors for all metals, specifically tris(N,N'-diisopropylacetamidinate) gadolinium [$Gd(^iPr_2\text{-amd})_3$], tris(*N*,*N*'-di-*iso*-propylformamidinate) lanthanum [$La(^iPr_2\text{-fmd})_3$], and tris(*N*,*N*'-diethylacetamidinate) scandium [$Sc(Et_2\text{-amd})_3$]. The Gd and Sc precursors were delivered from bubblers held at 140 °C. A reactor temperature of 310 °C and 300 °C was used for $GdScO_3$ and $LaScO_3$, respectively. The films were deposited on hydrogen-

terminated Si substrates using water as the co-reactant. Using a La:Sc cycle ratio of 1:1 resulted in a stoichiometric film as determined by RBS, with C and N impurities being <1% (the detection limit). The growth rate was around 2.0 Å/cycle with slight inhibition during the first few cycles. The films were amorphous as-grown and stayed that way up to 950°C. Cross-section TEM shows very little, if any, (< 0.2 nm) SiO_x interfacial layer. Capacitance-voltage measurements for both $GdScO_3$ and $LaScO_3$ showed very little hysteresis (< 20 mV) with dielectric constants of k~21.5 for $GdScO_3$ and k~23 for $LaScO_3$. The dispersion in the C-V curve was minimal (< 3% in accumulation). Using the scandate thin films, an EOT of ~1 nm was demonstrated while maintaining low leakage current (< 10^{-3} A/cm^2 at 1 V gate bias) with an interface trap density of 3×10^{11} cm^{-2} eV^{-1}.

A systematic study of the ALD-growth of rare earth scandates was reported in 2010 by Myllymäki *et al.* from Aalto University School of Science and Technology with focus on how the rare earth ion size affects growth.[179] Specifically, rare-earth scandate ($RScO_3$) films of La, Gd, Dy, Er, Y, and Lu were grown using β-diketonate precursors (*i.e.*, $R(thd)_3$) with ozone as the co-reactant. The R:Sc cycle ratio was changed until they found one that yielded the closest to a stoichiometric R:Sc composition in the film. With the optimized cycle ratio, films of various thicknesses were grown. The growth rate for the stoichiometric films ranged from 0.18 Å/subcycle for $LuScO_3$ to 0.28 Å/subcycle for $LaScO_3$ at the common growth temperature of 300°C, showing that growth rates are correlated with the rare earth ion size. In terms of carbon impurities, large radius lanthanides (La) showed the highest concentration (~1-3 at.%) compared to the small radius lanthanides (Lu) with < 0.5 at.% of carbon. There is also some hydrogen in the films (1-2 at.%). Using FTIR to determine the nature of the carbon impurity shows that it is likely a unidentate carbonate group. The FTIR signal also decreases with decreasing

rare earth ion size. Annealing of the films also caused a significant reduction in the carbonate FTIR signal, with the signal becoming nearly gone after annealing to 1000°C. All the films were amorphous as grown with the exception of the smallest lanthanide $LuScO_3$, which showed the distorted bixbyite structure. The next smallest lanthanide $ErScO_3$ began to crystallize at 600°C while the larger size ones crystallized at 800-1000°C. $ErScO_3$ and $YScO_3$ crystallized with the bixbyite structure (indicating a mixed phase of R_2O_3 and Sc_2O_3) while $GdScO_3$ and $LaScO_3$ crystallized into the perovskite structure. $DyScO_3$ showed mainly bixbyite structure when annealed at 900°C but converted to perovskite structure when annealed to 1000°C. They also performed C-V and I-V measurements confirming that amorphous rare earth scandates are very promising for use as high-k gate dielectrics on silicon.

1.2.5. Other $A^{3+}B^{3+}O_3$ type perovskite oxides

Outside of the La-based perovskites and scandates, there are only a few ALD studies reported for perovskite oxide compounds of the $A^{3+}B^{3+}O_3$ type. Those studies include neodymium aluminate ($NdAlO_3$),[180] yttrium manganite ($YMnO_3$),[181] and bismuth ferrite ($BiFeO_3$).[182] Aluminates were identified early as alternative high-*k* dielectric materials on silicon.[183] In 2005, Kosola *et al.* at the Helsinki University of Technology reported on the deposition of $NdAlO_3$ using $Nd(thd)_3$ and $Al(CH_3)_3$ with ozone and water as the co-reactant, respectively.[180] $Nd(thd)_3$ was evaporated at 161-164 °C inside the reactor, while $Al(CH_3)_3$ was delivered from outside the reactor at room temperature. The $NdAlO_3$ films were deposited on Si (100) substrates at a temperature of 300 °C. Nearly stoichiometric films were obtained using a Nd:Al cycle ratio of 6:1. The films were post-deposition annealed at 700-950 °C in both O_2 and N_2 atmospheres to study the crystallization effects. The films remained amorphous at temperatures of 700-750 °C, but

crystallized into the perovskite $NdAlO_3$ phase after annealing at 850 °C for 10-30 min. The deposition of the related material, cerium aluminate ($CeAlO_3$), was reported by Lukosius *et al.* (2012) in a study of perovskite-type dielectrics for MIM applications.[77] Pulsed-injection MOCVD was used to deposit thin films of $CeAlO_3$, achieving a dielectric constant of k~60 for the polycrystalline film.

Manganite thin films have attracted interest due to their favorable magnetic properties.[184] The deposition of $YMnO_3$ was reported by Uusi-Esko *et al.* (2009) at the Helsinki University of Technology.[181] Thin films were deposited using β-diketonate precursors, $Y(thd)_3$ and $Mn(thd)_3$, with ozone as the co-reactant at temperatures of 250-300 °C. The metal precursors were evaporated at 123 °C inside the reactor. At a deposition temperature of 275 °C, nearly stoichiometric films were produced using a Y:Mn cycle ratio of 1:1. The films were amorphous as-deposited, but crystallized upon post-deposition annealing at 750-1000 °C. When grown and annealed on Si (001) substrates, the films crystallized into the hexagonal $YMnO_3$ phase; however, on $LaAlO_3$ and $SrTiO_3$ substrates, the films crystallized into the orthorhombic $YMnO_3$ perovskite phase. The crystallinity was improved with increasing the annealing temperature up to 1000 °C for the orthorhombic $YMnO_3$.

$BiFeO_3$ is a promising multiferroic material that is both magnetic and ferroelectric at room temperature.[25] Therefore, the deposition of high-quality crystalline $BiFeO_3$ thin films has numerous applications in advanced electronic applications. Epitaxial thin films of $BiFeO_3$ produced by ALD were reported by Akbashev *et al*. (2013) at Drexel University.[182] The metalorganic precursors were tris(1-methoxy-2-methyl-2-propoxy) bismuth [$Bi(mmp)_3$] and bis(cyclopentadienyl) iron, or ferrocene [$Fe(Cp)_2$], with ozone as the co-reactant. Films were deposited at temperatures between 250-350 °C with $Bi(mmp)_3$ and $Fe(Cp)_2$ evaporated at 135-145 °C and 90 °C, respectively. The $BiFeO_3$

films were post-deposition annealed at 600-740 °C, where epitaxial perovskite films were obtained above 660 °C. The high-quality crystalline $BiFeO_3$ is observed in the cross-sectional TEM image, as shown in Figure 1.7. Strong ferroelectric switching was observed for the ALD-grown $BiFeO_3$ using piezoresponse force microscopy (PFM).

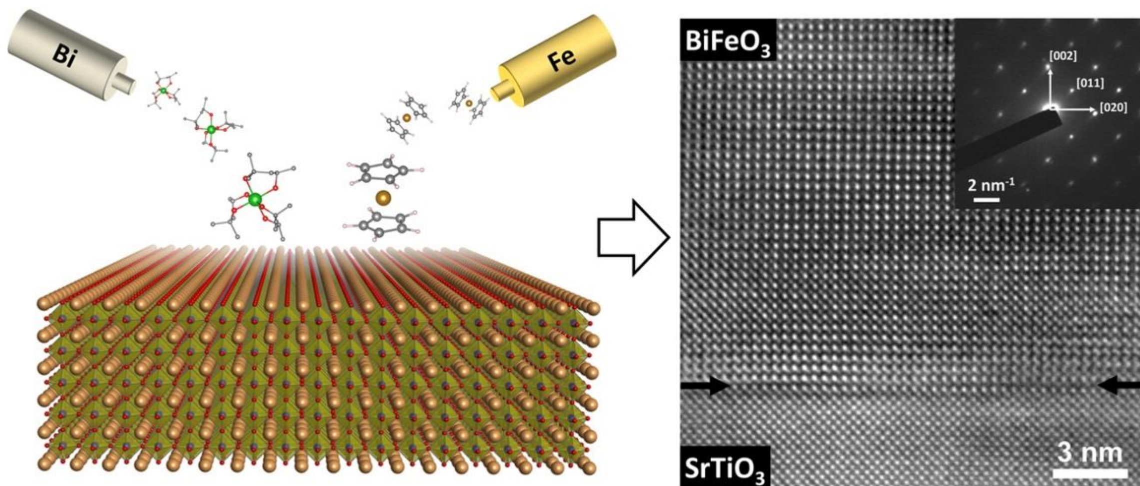


Figure 1.7. (left) Schematic illustration of the ALD process for obtaining heteroepitaxial $BiFeO_3$ on $SrTiO_3$ substrates and (right) high-resolution TEM image of the interface between $BiFeO_3$ and $SrTiO_3$ with (inset) selected-area electron diffraction of the $BiFeO_3$ film. [Reprinted with permission from Nano Lett. **14**, 44 (2014). Copyright 2014, American Chemical Society.]

Simultaneous work on $BiFeO_3$ thin films was reported by Zhang *et al.* of the Chinese Academy of Sciences using β-dikeonates, $Bi(thd)_3$ and $Fe(thd)_3$, with water as the co-reactant.[176] Films were deposited at 250 °C using evaporation temperatures of 140 °C and 120 °C for $Bi(thd)_3$ and $Fe(thd)_3$, respectively. $BiFeO_3$ was deposited using a supercycle that consisted of 10 Bi subcycles followed by 10 Fe subcycles, with a relatively low mean growth rate of 0.05 Å/subcycle. The films crystallized into the rhombohedral $BiFeO_3$ perovskite phase after post-deposition anneal at 650 °C for 60 s in O_2 atmosphere. Polarization of the $BiFeO_3$ film was observed by PFM, where domain

growth was observed with increasing time under the PFM measurement. Further work on $BiFeO_3$ thin films was reported by Liu *et al.* at the National Chiao Tung University.[177] The films were grown on $LaNiO_3$-coated Si substrates using trimethyl-bismuth [$Bi(CH_3)_3$] and cyclohexadiene-tricarbonyl-iron [$Fe(C_6H_8)(CO)_3$] with water as the co-reactant. Ideal ALD growth was not apparent at the growth rate of $BiFeO_3$ was a strong function of temperature between 480-550 °C. Nevertheless, reasonable growth was obtained at 500 °C with low leakage currents (~10^{-4} A/cm^2) and a remnant polarization of 2.0 μC/cm^2 for a 10 nm film. More recently, Jalkanen *et al.* (2014) at the University of Helsinki reported on the magnetic properties of thin polycrystalline films of $BiFeO_3$ grown by ALD.[178] Films were deposited using tris(2,3-dimethyl-2-butoxy) bismuth [$Bi(Me_2\text{-}O^tBu)_3$] and iron *tert*-butoxide [$Fe(O^tBu)_3$] with water as the co-reactant. The films were deposited at 150 °C on $Pt/SiO_2/Si$ substrates. The films were amorphous as-deposited and annealed at 500 °C for 1 h in N_2 atmosphere for crystallization. The magnetic properties were found to be versatile. The $BiFeO_3$ films behaved as a frustrated AFM-FM spin-glass system at low temperatures and a weak magnetic field.

1.3. Objective and Overview of Chapters

The ability to integrate metal oxide thin films on a semiconductor platform is the foundation of modern electronics with metal-oxide-semiconductor field-effect transistor (MOSFET) devices. In such devices, the oxide layer serves as the insulating dielectric material between the metal gate and semiconductor channel. The traditional dielectric material was silicon dioxide (SiO_2) owing to its favorable electronic properties and interfacial quality with silicon. The rapid down-scaling of MOSFET devices has required the integration of new oxides with high dielectric constants, such as hafnium dioxide

(HfO_2), to be integrated with Si. Amorphous oxides are preferred for high-*k* dielectrics to reduce leakage current through crystallographic defects in polycrystalline films. For next-generation high-*k* dielectrics ($k > 100$), perovskite oxides such as $SrTiO_3$ have been proposed. Single-crystal (*i.e.*, crystalline) oxide films often display a higher dielectric constant than their amorphous counterparts and are free of large grain boundaries to reduce leakage pathways. Therefore, methods to grow crystalline oxide films directly on semiconductors are necessary for next-generation high-*k* materials.

In addition, metal oxides display a wide array of other properties (superconductivity, ferroelectricity, magnetism, etc.) that provide an avenue to create novel material structures based on functional metal oxides and semiconductor devices. The majority of these desirable properties can only be realized for crystalline oxide films rather than their amorphous counterparts. The technical challenge becomes integrating crystalline oxide films directly on semiconductor materials with high structural integrity and low interfacial defects. For this reason, the perovskite oxide has been extensively studied due to its numerous properties, common structure, and in-plane lattice matching with common semiconductors. The monolithic integration of crystalline oxides on semiconductors was pioneered by McKee *et al.* (1998) in their early work on a perovskite oxide ($SrTiO_3$) epitaxially grown on Si.[9]

Several groups have since been successful using MBE to monolithically integrate perovskite oxides, such as $SrTiO_3$ and $BaTiO_3$, with Si and Ge substrates.[32-40] However, ALD is a preferred deposition technique for current oxide dielectrics due to its conformal coverage, low thermal budget, scalability, and low cost.[13-16] The key is finding an appropriate surface template that is maintained during ALD such that a crystalline oxide film may form above the semiconductor. Zhang *et al.* at the University of Connecticut successfully formed the half-monolayer Sr coverage on Si (2×1 Sr/Si reconstruction),[188]

which is shown to be a good surface template for MBE growth.[41] However, no further success has been reported for epitaxial oxide growth directly on Si by ALD methods.

Creating a stable surface template on Si for ALD can be overcome by depositing a robust crystalline oxide buffer layer. My initial research explored the use of a thin $SrTiO_3$ buffer layer grown on Si by MBE. This $SrTiO_3$-buffered Si substrate can then be used to grow crystalline oxide films by ALD. Of course, the downfall to this combined ALD-MBE growth technique is that MBE is still needed to deposit the $SrTiO_3$ buffer layer. By replacing Si with other semiconductors, such as Ge, prior thermodynamic limitations to crystalline oxide growth are removed. For example, the instability of GeO_2 versus SiO_2 favors the deposition of alternative oxide films. This has led to stimulating work within our research group to grow epitaxial perovskite oxides directly on Ge.[95,96] In addition, the Gordon group at Harvard University has also demonstrated the growth of an epitaxial perovskite oxide directly on GaAs substrates by ALD.[117]

This dissertation provides detailed growth and characterization of several crystalline oxides monolithically integrated with either $SrTiO_3$-buffered Si (001) or Ge (001) substrates using ALD. Chapter 2 provides an overview of the equipment in the Materials Physics Lab at the University of Texas at Austin where the substrates were prepared and metal oxide films were deposited. Chapters 3 and 4 provide details on the growth and characterization of epitaxial anatase TiO_2 on $SrTiO_3$-buffered Si (001). This initial work provided the foundation of using a 4 unit-cell $SrTiO_3$ layer (1.6 nm) grown on Si as a template for crystalline oxide growth by ALD. The epitaxial $TiO_2/SrTiO_3/Si$ material stack was also explored for resistive memory applications as discussed in Chapter 4. Chapters 5 and 6 discuss the growth and characterization of epitaxial $SrTiO_3$ and $(La,Sr)TiO_3$, respectively, on $SrTiO_3$-buffered Si (001) substrates. This confirmed

the applicability of ALD to deposit ternary and quaternary oxides provided that compatible precursors and processing conditions are developed.

Chapter 7 discusses the first report of an epitaxial perovskite oxide ($SrTiO_3$) grown on Ge by ALD. Amorphous $SrTiO_3$ was deposited by ALD on a clean, 2×1 reconstructed Ge (001) surface and became crystalline with epitaxial registry to the Ge after a post-depostion vacuum anneal. This work demonstrated the monolithic integration of crystalline perovskite oxides directly on semiconductors by ALD, which has great technological opportunity. Chapter 8 reports on the ALD growth of epitaxial $SrHfO_3$ on Ge. This work confirmed that single-crystal oxide films may be grown on Ge by ALD provided an appropriate starting surface (*i.e.*, 2×1 reconstructed Ge (001) surface). Crystalline $SrHfO_3$ was demonstrated as a high-k dielectric material for Ge-based transistors.

1.4. References

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Chapter 2: Deposition and Characterization Equipment of the Materials Physics Laboratory

2.1 Molecular Beam Epitaxy System

The molecular beam epitaxy (MBE) system is a central component of the Materials Physics Laboratory and has been operational since 2009. Images of the MBE system (DCA 600) are provided in Figure 2.1. The MBE is pumped by a cryopump and has a base pressure of 1×10^{-10} torr. It is equipped with six effusion cells (four standard and two high-temperature), a four-pocket electron beam evaporator, a radio frequency (rf) plasma atomic nitrogen source, and an rf plasma atomic oxygen source with a high-precision leak valve. The MBE chamber is also outfitted with a differentially-pumped reflection high energy electron diffraction (RHEED) system for real-time *in situ* monitoring of the growth, and with a quartz crystal microbalance for flux measurement.

The system is capable of handling samples as small as 5×5 mm^2 up to a 2-inch diameter wafer. Samples can be heated up to 1000 °C using the oxygen-resistant silicon carbide DCA sample heater. All metal sources and the sample manipulator have pneumatically actuated shutters. The deposition process can be controlled by computer or manually. The system is also equipped with an ethanol-based cryopanel. The ethanol is regulated and recirculated by a Lauda process thermostat.

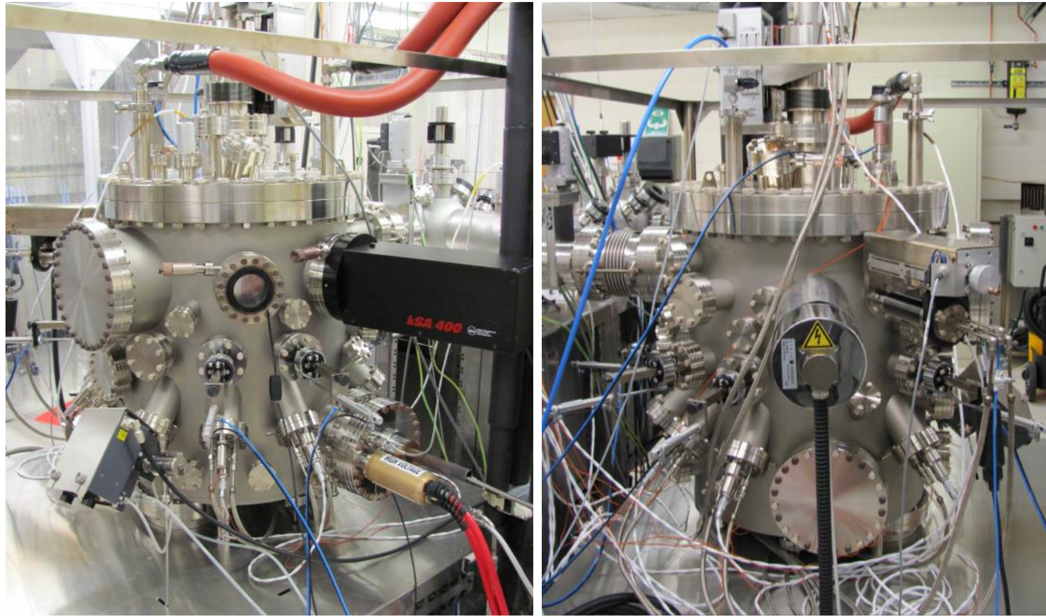

Figure 2.1. Images of the MBE system located in the Materials Physics Lab

2.2 ULTRAHIGH VACUUM TRANSFER LINE

The MBE is connected to the other lab facilities by a 12-foot ultrahigh vacuum (UHV) transfer line allowing for the exchange of samples between other growth and analysis chambers. An inner view of the transfer line is shown in Figure 2.2. This *in situ* sample exchange capability between various systems provides us with a unique capability for complex growth process with characterization at every step of the growth. The transfer line vacuum is maintained by two ion pumps and the transfer mechanism is based on a trolley system. We have the capability of holding up to 20 samples in the transfer line using two trolley carts. The trolley cart moves along rails through the entire length of the transfer line using a rack and pinion mechanism.

The sample disks can be quickly loaded and unloaded without venting the rest of the transfer line through a load lock located at one end of the transfer line. The load lock

is pumped by a turbomolecular pump and is also equipped with halogen lamp heaters capable of heating samples to 150 °C for light outgassing prior to moving into the main transfer line. The load lock end of the transfer line is contained within a Class 100 soft wall clean room ensuring a particulate-free sample environment during sample loading. At the opposite end of the transfer line is a high-temperature heating state with gas flow capability for substrate preparation/cleaning as well as post-deposition annealing. The preparation chamber is capable of heating samples up to 1200 °C and is independently pumped by a high throughput turbopump. The preparation chamber is also equipped with a mass spectrometer for temperature-programmed desorption studies.

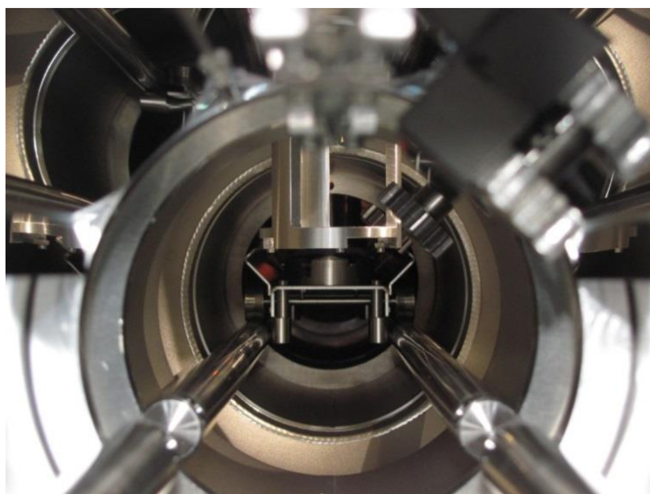

Figure 2.2. Inside view of the UHV transfer line that enables *in situ* transfer between growth and analysis chambers

2.3 ATOMIC LAYER DEPOSITION SYSTEM

The ALD system consists of a custom-built, hot wall stainless steel rectangular chamber with a reactor volume of 460 cm^3. The ALD chamber is pumped by a

turbomolecular pump to a base pressure of 2×10^{-7} torr. The carrier/purge gas (argon) and precursors are introduced through a common manifold at the front of the chamber. The gas manifold allows eight different precursors to be connected at once, which is necessary for studying complex oxide heterostructures. The chamber is continually evacuated during the deposition process by a dual stage rotary vane pump. The ALD system is connected to the high temperature preparation chamber, which also serves as a buffer between the higher pressure ALD system to the UHV transfer line.

Our customized ALD chamber is approximately an 8-inch long rectangular chamber with six ports (shown in Figure 2.3): precursor inlet port (P1), sample transfer port (P2), viewing port (P3), pumping port (P4), power lead port for heater (P5), and a thermocouple port (P6). During ALD growth, the carrier gas is introduced into the chamber from port P1 and pumped out through port P4. Figure 2.3(b) shows an inner schematic of the ALD chamber. The carrier/purge gas in our system is argon. Typically, the metal and H_2O precursor pulsing times are 1-2 seconds with 15 seconds for purging (both metal and H_2O).

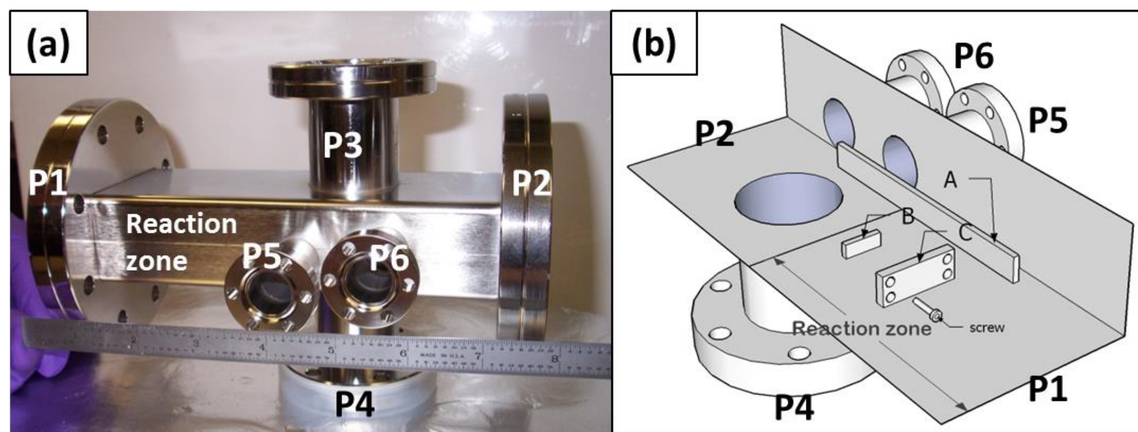

Figure 2.3. (a) Custom-built ALD reactor and (b) inner schematic of ALD reactor

Figure 2.4 shows the assembled ALD reactor, integrated with the existing UHV system for oxide thin film growth and characterization. Swagelok three-way ALD valves with high temperature actuators are used to control the delivery of precursors. This system is composed of eight precursor delivery lines (seven metalorganic precursors and the water oxidant), with the capability of growing binary and ternary metal oxides.

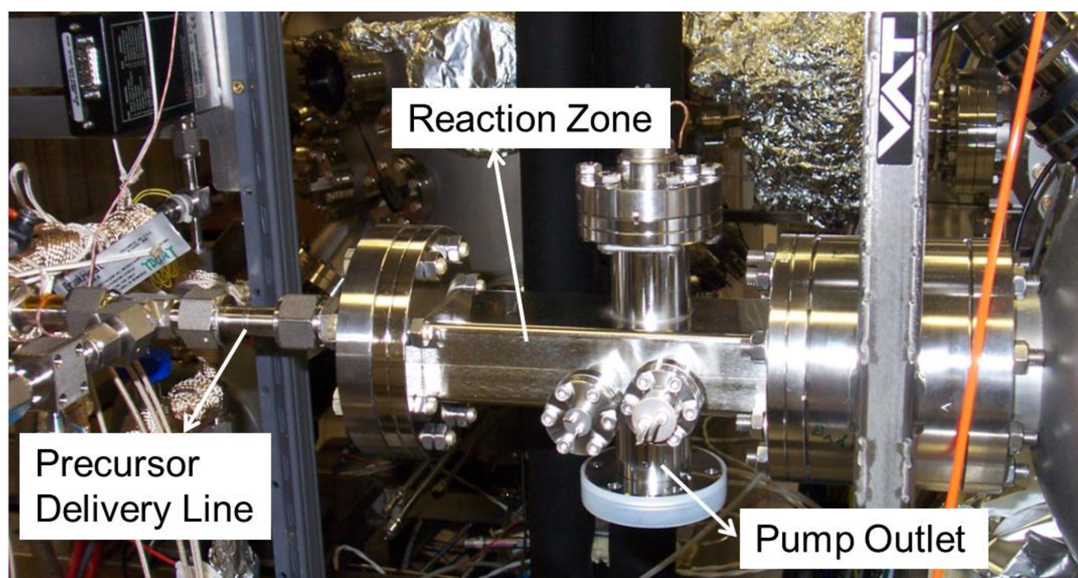

Figure 2.4. Assembled ALD reactor connected to the UHV transfer line

2.4 X-RAY PHOTOELECTRON SPECTROSCOPY SYSTEM

The X-ray photoelectron spectroscopy (XPS) chamber and transfer system was designed by VG Scienta and installed in January 2012. An image of the XPS sytem is provided in Figure 2.5. The system is fully integrated with the vacuum transfer line allowing *in situ* sample exchange with the MBE and ALD deposition systems. The analysis system with a base pressure of 3×10^{-10} torr is equipped with a monochromated Al Kα x-ray source and a high intensity VUV 5000 He plasma-based ultraviolet source.

This allows for high resolution measurements of both UPS valence band spectra and XPS core level spectra for composition and chemical state analysis. Full angular resolution is possible with a five-axis manipulator allowing for valence band mapping and depth profiling measurements. The manipulator can also be cooled down to about 150 K. The system is also equipped with an ion gun that can be used for both sample surface cleaning and depth-profile sputtering, as well as for ion scattering spectroscopy.

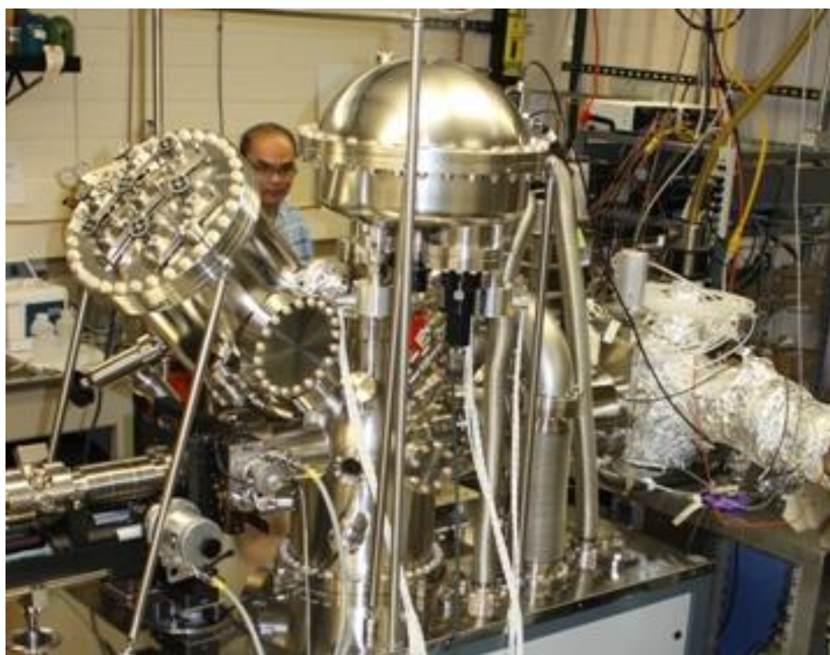

Figure 2.5. Image of the XPS system located in the Materials Physics Lab

Chapter 3: Growth and Characterization of Epitaxial Anatase TiO_2(001) on $SrTiO_3$-buffered Si(001) using Atomic Layer Deposition

Contents of this Chapter were published in Thin Solid Films ***520****, 6525-6530 (2012).*[I]

3.1. Introduction

Development of electronic solid state devices based on oxide thin films has been the subject of much research.[1,2] Many important properties of metal oxides (high temperature superconductivity, ferroelectricity, magnetism, thermal barriers, etc.) have found applications in power transmission,[3] non-volatile memory,[4] magnetic tunnel junctions,[5] and heat resistant coatings.[6] For many of these applications, epitaxial films show better performance than polycrystalline films attributed to their elimination of crystallographic defects, such as high-angle grain boundaries. For example, in gate dielectric applications, these grain boundaries can act as high leakage pathways. Therefore, thin film epitaxial oxide heterostructures present an ideal platform to explore these electronic and magnetic properties, and when integrated with semiconductors, potentially have applications in advanced electronics, hyperspectral sensors, and persistent surveillance and radar technologies.[1-5] However, there is often difficulty with growing epitaxial oxides directly on silicon due to the formation of amorphous SiO_2, as well as silicates and/or silicides at the interface. Strontium titanate (STO) is one of the few oxides that can be grown epitaxially on silicon (001) without interface reaction problems.[7] Therefore, the epitaxial growth of STO on silicon provides a gateway for a multitude of oxide heterostructures to be integrated with silicon.[8-17]

[I] M. D. McDaniel, A. Posadas, T. Wang, A. A. Demkov, and J. G. Ekerdt, "Growth and characterization of epitaxial anatase TiO_2(001) on $SrTiO_3$-buffered Si(001) using atomic layer deposition," Thin Solid Films **520**, 6525-6530 (2012). MDM designed and performed experiments. MDM, AP, AAD, and JGE contributed to the conception and analysis of data. MDM and TW designed and constructed the atomic layer deposition equipment.

Chemical routes for growing epitaxial oxide thin films, such as atomic layer deposition (ALD), need to be explored to enable alternative manufacturing routes, growth over large area substrates, thicker film growth, and potentially easier integration of multifunctional oxide heterostructures on silicon. ALD entails the sequential delivery of precursors or reagents that either adsorb to saturation coverage or undergo selective ligand reactions, which are self-limiting, leading to film growth.[18,19] It is in effect a chemical vapor deposition (CVD) technique based on sequential, self-terminating, gas-solid reactions. Precursor choice has a profound effect on the deposition characteristics of ALD. In many cases, precursors that react with water are preferred to avoid the formation of CO_2 in oxygen and ozone environments that can lead to carbonates in the film.[20] The precursors used in this study, titanium isopropoxide (TTIP) and water, have proven to be effective precursors for the deposition of titanium dioxide (TiO_2).[21,22]

TiO_2 has been one of the most widely studied metal oxides due to its numerous industrial applications.[23–26] TiO_2 has two main polymorphs, anatase and rutile, which both function as a photocatalyst.[27] The relatively low deposition temperature for TiO_2 by ALD typically results in the anatase modification over the more stable rutile structure. In addition, epitaxial stabilization of thin film anatase TiO_2 can be realized on lattice-matched substrates for processing temperatures and conditions where rutile would be preferred in the bulk.[28] Recently, there has been increased interest in controllable synthesis and assembly of anatase TiO_2 with dominant high-energy {001} facets. This may offer potential to exploit enhanced surface properties for photocatalytic and related applications.[29]

Growth of epitaxial anatase TiO_2(001) films has been reported on various single-crystal substrates, including $LaAlO_3$,[28,30-33] (La,Sr)(Al,Ta)O_3,[31,33] and $SrTiO_3$.[31-39] Various deposition techniques have been employed, including molecular beam epitaxy

(MBE),[30–32,34–36,38] reactive sputtering deposition,[28,40] and metal organic CVD.[37,39] Exploration of the physical phenomena and potential applications of the epitaxial anatase TiO_2(001) grown on perovskite structures has been reported, including thermoelectric, memristor, and spintronic applications.[41–45]

The growth of epitaxial STO on Si(001) allows for large area STO pseudo-substrates, which serve as a surface template to integrate functional oxides on Si(001) substrates.[8-11] For example, pure-phase and Co-doped anatase TiO_2(001) films were deposited by MBE on Si(001) substrates using a thin STO buffer layer.[46] The lattice mismatch between STO and Si(001) is relatively small (1.7%) with a 45° in-plane rotation. Anatase TiO_2 exhibits a square surface mesh along the (001) orientation, as does bulk STO, creating a nominal lattice mismatch of (-3.1%). However, since thin epitaxial STO is perfectly strained to the underlying silicon substrate,[47] the lattice mismatch between anatase TiO_2 and the STO-buffered silicon will be smaller (-1.4%).

This study examines the applicability of using a STO pseudo-substrate grown by MBE as a template for the growth of epitaxial oxide films by ALD. In our system, a customized ALD chamber has been integrated with a MBE system, allowing *in-situ* transfer of samples, enabling the study of epitaxial oxide films grown by ALD on surface templates grown by MBE. We are reporting here the growth of epitaxial anatase TiO_2(001) by ALD on STO-buffered Si(001) substrates.

3.2. Experimental Details

The ALD system consists of a custom-built, hot wall stainless steel rectangular chamber that is approximately 20 cm long, with a reactor volume of 460 cm^3. The ALD chamber is pumped by a turbomolecular pump to a base pressure of 2×10^{-4} Pa and is

connected to a transfer chamber that is maintained below 3 × 10^{-7} Pa. The transfer chamber is part of a larger transfer line that allows *in-situ* transfer of samples from the MBE system (DCA 600) to the ALD chamber (Fig. 3.1). Substrate samples are 20 × 20 mm^2 silicon wafers and are held in a molybdenum puck (5 cm diameter) that is used in both the ALD chamber and MBE system, therefore enabling *in-situ* sample transfer and growth on well-characterized and specially prepared surfaces. During ALD growth, the carrier/purge gas (argon) and precursor are introduced through a common manifold at the front of the chamber. The gas manifold allows for seven different precursors to be connected at once. The chamber is continually evacuated during the deposition process by a dual stage rotary vane pump with a peak pumping speed of 6 cfm, which maintains the operating pressure at 130 Pa.

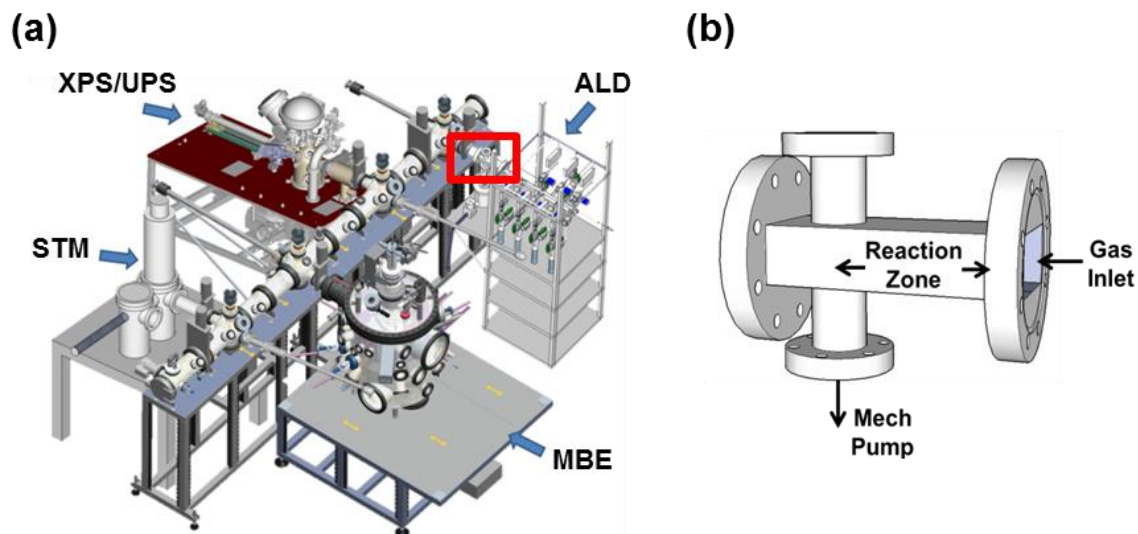

Figure 3.1. Schematic of the MBE and ALD system to allow *in-situ* transfer of samples: (a) system layout including the main transfer line and analysis chambers (location of the ALD chamber is highlighted) and (b) perspective drawing of the ALD chamber. Note: the analysis chambers were not operational during these studies.

The MBE system was used to grow crystalline STO directly on Si(001) using a variation of the Motorola-developed process.[48] The substrates were prime Si wafers with nominal 2 nm of native oxide that were cut to 20×20 mm^2 then ultrasonically cleaned with acetone, isopropyl alcohol, and deionized water for 5 min each, followed by UV/ozone exposure for 15 min to remove residual carbon contamination. The silicon substrate was then loaded into the chamber and the native oxide was desorbed using a Sr-assisted deoxidation process.[49] After achieving a clean Si(001) surface with 2×1 reconstruction, a half monolayer of Sr metal is deposited on the Si substrate at 550 °C forming the strontium silicide template layer. The MBE chamber is equipped with an 18 keV reflection high-energy electron diffraction (RHEED) system to monitor structural morphology during growth. In order to ensure that the underlying Si is not oxidized during the initial STO deposition, the substrate is cooled to below 200°C and molecular oxygen is ramped from 5×10^{-6} Pa to 2×10^{-5} Pa over several minutes. Sr and Ti are co-deposited from effusion cells during the oxygen ramping at a rate of one monolayer per minute to a thickness of four unit cells of STO. Oxygen is then removed and the film is annealed at 550 °C to crystallize the STO layer, as verified by RHEED. For STO thicknesses larger than 4 unit cells, molecular oxygen is re-introduced after crystallization (2×10^{-5} Pa) and additional Sr and Ti are co-deposited to achieve the required film thickness. The film remains crystalline throughout the subsequent growth as observed by RHEED. Upon reaching the desired STO thickness, the substrate is transferred *in-situ* to the ALD chamber.

Epitaxial anatase (TiO_2) thin films were grown by ALD at 225-250 °C using titanium isopropoxide {$Ti[OCH(CH_3)_2]_4$} (TTIP) and water as the co-reactants on MBE-grown single crystal STO/Si(001); the precursors were held at 40 °C and 25 °C, respectively. One deposition cycle consisted of a 1 sec pulse of the Ti precursor, a 10 sec

purge with Ar, a 1 sec pulse of H_2O, and a 10 sec purge with Ar, noted as 1/10/1/10 × N, where N is the number of ALD cycles. Both the Ti precursor (TTIP) and water were found to saturate the substrate surface with 1 sec of dosing time. Argon was used as the carrier gas to deliver the Ti precursor and purge gas between reactant dosing, maintaining the operating pressure at 130 Pa. Post-deposition, samples were annealed at 600 °C for 1-2 hr in vacuum (10^{-7} Pa). Films were characterized using x-ray photoelectron spectroscopy (XPS), x-ray reflectivity (XRR), spectroscopic ellipsometry (SE), atomic force microscopy (AFM), RHEED, and x-ray diffraction (XRD).

XPS was performed *ex-situ* with an Al Kα source at 1486.6 eV using a Physical Electronics 5500 XPS system to determine the film composition and verify the presence of TiO_2. All XPS spectra were analyzed using a uniform shift based on the C 1s peak to 285 eV (unless otherwise noted). Both RHEED and XRD were used to evaluate the orientation and crystallinity of the TiO_2 films. XRD and XRR were conducted with a Bruker-AXS D8 Advance Powder Diffractometer using a sealed tube Cu Kα radiation.

Film thicknesses were determined using XRR analysis, where the plot of log intensity versus 2θ angles from 0° to 6° show oscillations at a frequency that is directly related to the thickness of the deposited film. In addition, film thicknesses were verified by SE using a J.A. Woollam M2000D Spectroscopic Ellipsometer with the WVASE32 software package. Ellipsometric Ψ and Δ data were acquired over the spectral range of 250-1000 nm, using variable angles of incidence between 55° and 75° (every 5°). The model consisted of a three layer TiO_2/STO/Si structure, with fixed optical constants and thicknesses for the STO layer and underlying Si substrate. Both the optical constants and thickness of the TiO_2 layer were allowed to float for optimization of the model to the experimental data.

To establish the TiO_2 ALD growth process, both the saturation behavior and growth rate was evaluated on 20 × 20 mm^2 Si wafers with nominal 2 nm of native oxide that were ultrasonically cleaned with acetone, isopropyl alcohol, and deionized water for 5 min each, followed by UV/ozone exposure for 15 min to remove residual carbon contamination. After deposition, the thickness of the TiO_2 films was measured by XRR and verified by SE. These two methods were found to be in good agreement within experimental error (±1.0 nm for a 20 nm film).

3.3. RESULTS AND DISCUSSION

3.3.1. Formation of anatase-type TiO_2 on SiO_2/Si(001) native oxide

TiO_2 thin films grown on native oxide substrates were used to establish ALD growth rates, film composition, and crystallinity. Compositional analysis of the as-deposited TiO_2 films was completed by *ex-situ* XPS analysis. Figure 3.2 shows the X-ray photoelectron spectra for Ti 2p, where the binding energy for the Ti $2p_{3/2}$ peak is 458.8 eV. This indicates that the titanium ions are in the Ti^{4+} oxidation state. The presence of Ti^{3+} species would have characteristic shifts of ~1.7 eV towards lower binding energy than Ti^{4+} species.[50] Exposure of the as-deposited samples to atmosphere introduced carbon contamination on the surface, indicated by a C 1*s* peak present at 285 eV (not shown). To check the incorporation of carbon in the bulk film, Ar^+ sputtering at 3kV over a 3 × 3 mm^2 area for 90 s was performed. Approximately 3 nm of the topmost surface is removed during the sputtering process. The C 1*s* peak was eliminated during this process, indicating that any C impurities in the bulk film are below the XPS detection limits (< 1 %).

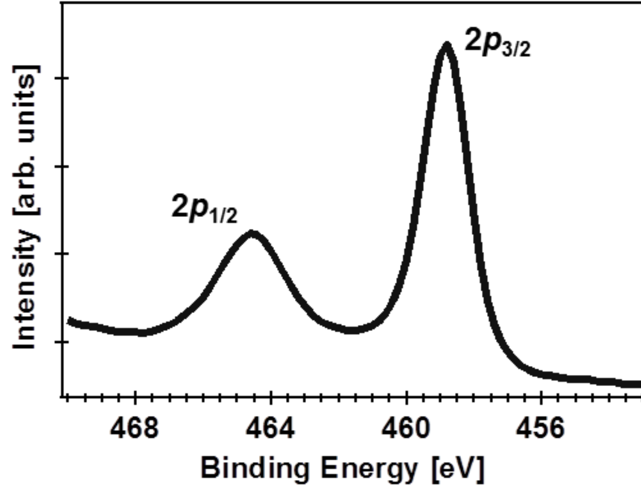

Figure 3.2. Ti 2*p* X-ray photoelectron spectrum for 6 nm of as-deposited TiO_2 on native oxide using TTIP and H_2O precursors at a deposition temperature of 225 °C.

Using XRR and spectroscopic ellipsometry to determine thickness, the growth rate of TiO_2 was 0.31 Å/cycle for $N < 600$ and 0.49 Å/cycle for $N > 1000$ (Fig. 3.3). Previous studies using the same precursors have reported growth rates of 0.30 Å/cycle up to 0.60 Å/cycle.[21,22] The increase in growth rate appeared to have a direct correlation with the number of ALD cycles, *i.e.*, thickness of the film. This behavior has been explained by the development of polycrystalline TiO_2 with increasing thickness, where under the same deposition conditions anatase grows faster than amorphous TiO_2.[51] To verify the development of polycrystalline TiO_2 we utilized *in-situ* RHEED analysis and *ex-situ* XRD.

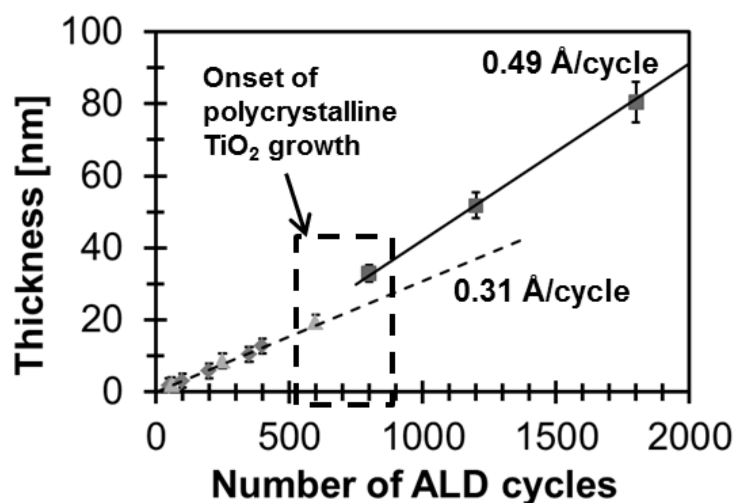

Figure 3.3. Linear growth behavior of TiO_2 films grown using TTIP and H_2O on native oxide at 250 °C. The highlighted area denotes the onset of polycrystalline TiO_2 growth as verified by RHEED and XRD.

XRD analysis (Fig. 3.4), revealed a strong correlation between the TiO_2 film thickness and crystallinity when grown on silicon substrates with native oxide. TiO_2 films on native oxide substrates appeared amorphous at low thicknesses (< 12 nm). However, increasing the thickness of the film (*i.e.*, number of ALD cycles) resulted in a polycrystalline TiO_2 film of anatase structure. This observation is consistent with previous studies using ALD to grow TiO_2 thin films using titanium ethoxide and water.[52] RHEED images did reveal some evidence of polycrystalline TiO_2 at the surface even at lower thicknesses; however films under ~12 nm appeared amorphous by XRD. Films greater than 12 nm showed the anatase (101) peak and to a lesser extent the anatase (200) peak. This is consistent with previous publications on ALD of TiO_2 thin films using silicon substrates.[51–55]

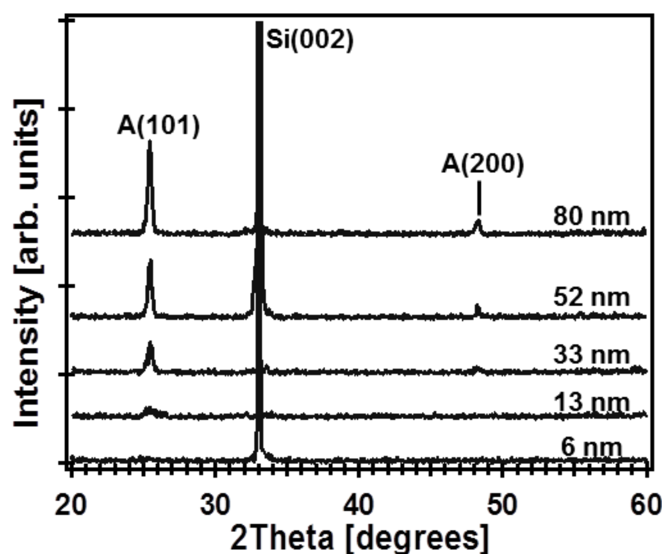

Figure 3.4. X-ray diffraction patterns for TiO_2 films grown using TTIP and H_2O at 250 °C on Si(001) substrate with native oxide. The samples were post-deposition annealed at 600 °C for 1 hr. Thicknesses of 6, 13, 33, 52, and 80 nm were measured for 200, 400, 800, 1200, and 1800 cycles, respectively.

3.3.2. Epitaxial TiO_2 on $SrTiO_3$-buffered Si(001) substrate

In order to explore the growth of epitaxial TiO_2 films on Si(001) substrates by ALD, the MBE system was utilized to create a STO buffer layer to serve as a surface template for ALD growth. Several different thicknesses of the STO template were evaluated for epitaxial ALD growth. The STO maintained a stable template on top of the silicon with a nominal thickness of four unit cells. Less than four unit cells of STO resulted in TiO_2 thin films that were identical to those grown on amorphous SiO_2, where the structure is polycrystalline and does not exhibit preferred orientation in the *c*-axis. These results suggest that less than four unit cells of STO grown on silicon substrates by MBE, does not maintain a suitable surface template for epitaxial TiO_2 growth by ALD.

RHEED served as a quick and effective analysis tool to verify the quality of the surface template. Figures 3.5(a) and 3.5(b) show the RHEED patterns of a typical STO-buffered Si(001) substrate with four unit cells of STO grown by our MBE system; images

are taken along the [100] and [110] direction, respectively. The well-defined streaks in the RHEED images are indicative of a highly crystalline and atomically smooth STO film. This stable template may then be transferred to the ALD system, and the desired thickness of TiO_2 is grown by ALD. Figures 3.5(c) and 3.5(d) show RHEED patterns of the TiO_2 film after ALD at 225 °C and annealing at 600 °C, where the images are also taken along the [100] and [110] direction, respectively. The images have been aligned such that the relationship between the TiO_2 film and the substrate can be observed. The TiO_2 film is highly oriented with the substrate, as can be seen by the alignment of the streaks. Separate studies (not presented) reveal that the as-deposited films are crystalline. The intensity modulation in the streak direction of the TiO_2 RHEED images indicates an increase in surface roughness from the ALD and annealing process.

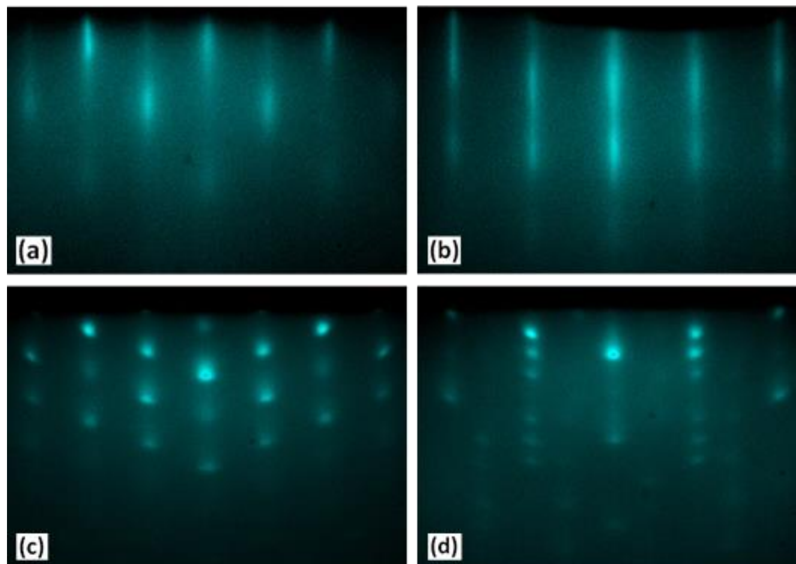

Figure 3.5. RHEED images obtained before [(a), (b)] and after [(c), (d)] ALD growth for 20 nm thick anatase TiO_2 on four unit cell STO-buffered Si(001) at 225 °C. The sample was post-deposition annealed in vacuum at 600 °C for 1 hr. The beam is aligned along the [100] for (a) and (c), and [110] azimuth for (b) and (d).

To determine the surface morphology of the ALD films, AFM measurements were taken on both the as-deposited and annealed films (Fig. 3.6(a) and 3.6(b), respectively). The as-deposited film shows a root-mean-square (RMS) surface roughness of 0.51 nm, while the annealed film shows a slightly reduced RMS value (0.37 nm). Qualitatively, the as-deposited ALD film has a granular-like appearance. After annealing, the film has a relatively smooth surface with distinct features in two perpendicular directions (shown in the highlighted region of Fig 3.6(b)). These features may result from the propagation of crystalline defects (*e.g.*, dislocations) to the surface; this would allow stress relief of the epitaxial film, giving further evidence that the TiO_2 film is constrained to the STO/Si substrate.

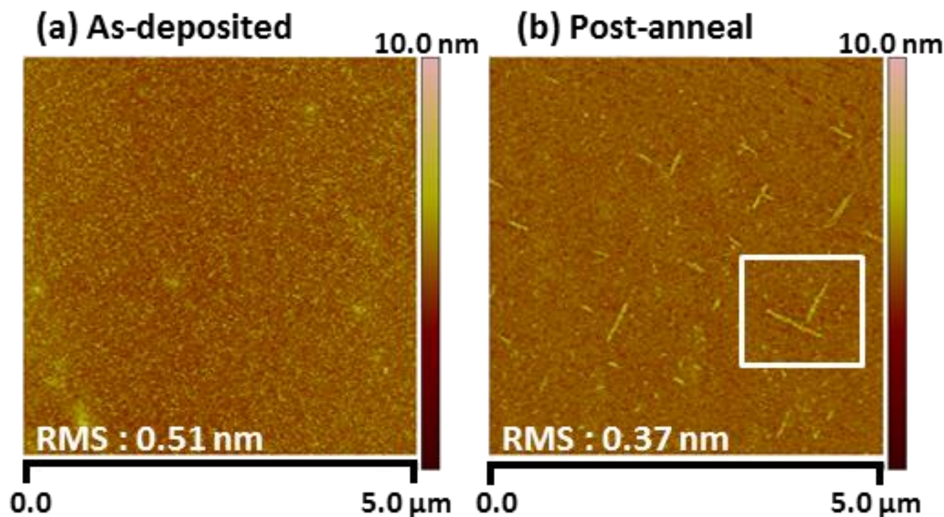

Figure 3.6. AFM image of the as-deposited (a) and annealed (b) film for 10 nm thick anatase TiO_2 on four unit cell STO-buffered Si(001) grown at 250 °C. The sample was vacuum annealed at 600 °C for 1 hr.

XRD patterns verified the crystal structure and preferred orientation of the TiO_2 films. The films grown by ALD were anatase and highly *c*-axis oriented, as indicated by

the sole presence of the (004) reflection. A typical XRD pattern for a 20 nm TiO_2 film grown using the template method is shown in Figure 3.7. The (004) reflection is shifted from that of anatase powder (2θ~37.9°) to a slightly higher value of 2θ~38.2°, indicating that the *c*-lattice constant of the anatase TiO_2 film is 9.42 Å. This is consistent with an increased *a*-axis from that of bulk anatase, which reduces the in-plane lattice mismatch of anatase TiO_2 to the substrate. Similar behavior has been reported for epitaxial anatase TiO_2(001) films grown on STO(100) single crystal by MBE.[35,38] To determine the degree of out-of-plane orientation, a rocking curve was performed around the (004) reflection, which gave a full-width half maximum of 1.4° (Fig. 3.8). The epitaxial relationships between anatase TiO_2 and the substrate were determined by a φ-scan on the {105} reflections of anatase and the {115} reflections of silicon. The anatase film was aligned such that $(001)_{anatase} \| (001)_{STO} \| (001)_{Si}$ and $(100)_{anatase} \| (100)_{STO} \| (110)_{Si}$.

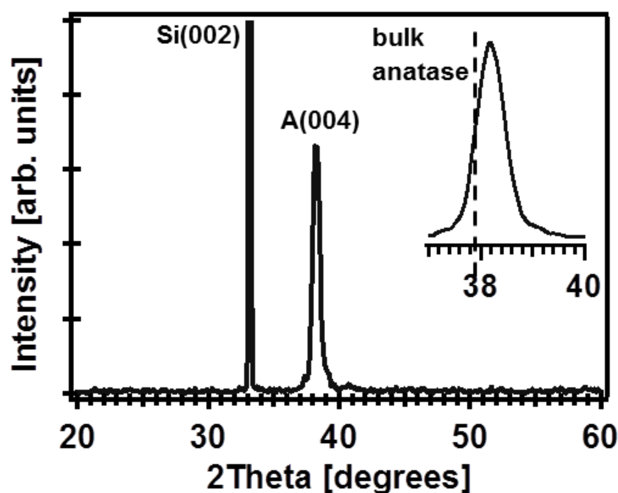

Figure 3.7. X-ray diffraction pattern for a 20 nm thick anatase TiO_2 film grown by ALD on STO-buffered Si(001) at 225 °C. Sample was post-deposition annealed at 600 °C for 1 hr. (inset) Comparison of the anatase (004) reflection with that of bulk anatase.

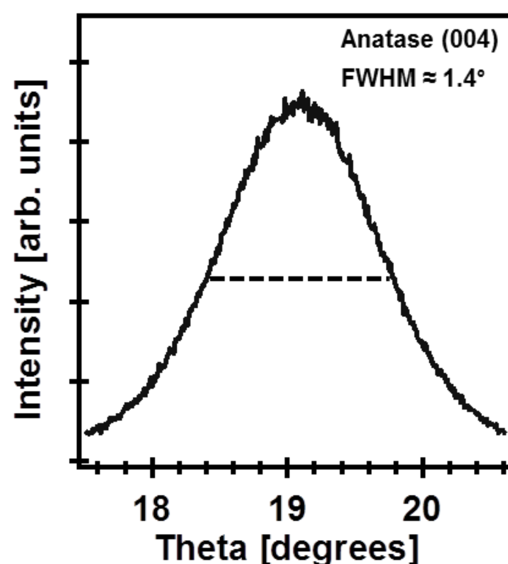

Figure 3.8. Rocking curve of the anatase (004) reflection at a fixed 2θ = 38.2° for a 20 nm thick film grown by ALD on STO-buffered Si(001) at 225 °C and annealed at 600 °C for 1 hr.

3.3.3. Stability of surface template on ALD growth

To test the stability of the surface template, a standard four unit cell STO template was grown on a Si(001) substrate and exposed to ambient conditions for several months. The substrate was then loaded into the ultra-high vacuum system and annealed at 650 °C for 2 hrs to remove residual carbonates and hydroxyls from exposure to atmosphere. The substrate was transferred into the ALD chamber with no further surface treatment or preparation, where TiO_2 was deposited at normal operating conditions. The resulting film was highly crystalline, with preferred orientation in the *c*-axis. The RHEED images and XRD scans from this film (not shown) were indistinguishable from TiO_2 films grown on MBE templates without ambient exposure, such as presented in Figures 3.5(c), 3.5(d), and 3.7. This gives further support that high-quality STO grown on silicon is a stable template for the growth of epitaxial oxides by ALD.

Through *in-situ* transfer between the MBE and ALD system, we explored if other surface templates would allow the growth of epitaxial TiO_2 on Si(001) substrates. One choice is the (2×1) ordered Sr/Si(001) surface, also known as the strontium silicide template layer, which allows the growth of epitaxial STO by MBE.[56] To test this template, we prepared a (2×1) ordered Sr/Si(001) substrate by MBE and transferred it *in-situ* to the ALD chamber, where TiO_2 was deposited. The resulting film was polycrystalline and did not show any sign of preferred orientation. The strontium silicide template prepared in our system appears to be unstable under the ALD TiO_2 growth process.

We expect that the surface template must be able to maintain its structure during each half-reaction of the ALD process. In our system, we anticipate that the H_2O pulse may lead to oxidized silicon species (SiO_x) formation when using silicon substrates despite the care that is taken to prevent SiO_x formation during the MBE growth of STO. Previous work has shown the MBE process to grow high-quality STO on silicon without the formation of SiO_2.[47] To check for formation of SiO_x species after the ALD process, we grew a standard 4 unit cell STO template on a silicon substrate by MBE followed by 60 cycles (~2 nm) of TiO_2 by ALD. The resulting TiO_2 thin film was highly ordered as indicated by the RHEED pattern (not shown). By using XPS (Fig. 3.9) to look at the Si 2p characteristic binding energies, there is clear indication of SiO_x formation ($x < 2$) attributed to the ALD process.

Figure 3.9 shows the Si 2*p* spectrum of this sample with fitted curves to resolve the components, along with a representative spectrum of the Si 2*p* prior to ALD growth. The centroids of the two components are at 99.3 eV and 102.0 eV (after constant shift of the Si 2*p* peak to 99.3 eV), indicate contributions from the bulk Si substrate and amorphous SiO_x, or silicate, species due to the increase in binding energy (~2.7 eV) of

the Si 2*p*-peak. By evaluating the Sr 3*d* before and after annealing, there appears to be no evidence of strontium silicate formation (not shown). Based on the effective attenuation length of Si 2*p* through anatase TiO_2, the thickness of the amorphous SiO_x layer is estimated to be 2-3 nm. Despite the formation of SiO_x, the STO lattice constant should remain strained to silicon because the processing conditions do not allow for both high temperature and large partial pressure of oxygen at the same time. The relatively low temperature of ALD (~250°C) and the absence of oxygen during post-deposition annealing does not allow for significant oxidation of the underlying Si,[57] and consequent relaxation of the STO lattice constant.[58]

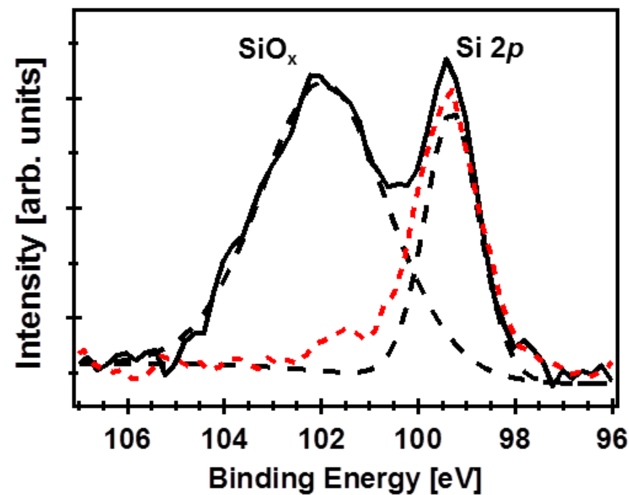

Figure 3.9. Si 2p X-ray photoelectron spectrum after 60 ALD cycles (solid black line) with fitted curves (black dashed lines) and a representative spectrum for the Si 2p prior to ALD growth (dashed red line). A uniform shift of the raw data was applied based on the Si 2p peak (99.3 eV).

Anatase TiO_2 films were grown up to 100 nm using the MBE surface template. All the films remained highly oriented in the *c*-axis; however, for films greater than 20 nm, we observed the presence of anatase (112) reflection in XRD. Figure 3.10 presents

an XRD scan for a 100 nm TiO_2 film grown on STO-buffered Si(001) showing the emergence of the (112) reflection. The relatively low temperature of ALD growth in comparison with MBE likely precludes direct epitaxial growth of TiO_2. Therefore, at increasing thicknesses we observe some deviation from the surface template after annealing. However, the ALD growth does not appear to randomly orient at larger thicknesses due to the absence of the (101) reflection, which is the predominant peak for polycrystalline TiO_2 (Fig. 3.4). The emergence of the (112) direction may be due to the spacing of the Ti atoms on this surface being 5.34 Å and 5.44 Å, which are consistent with the second nearest neighbor Ti-Ti distance in the anatase [001] plane.

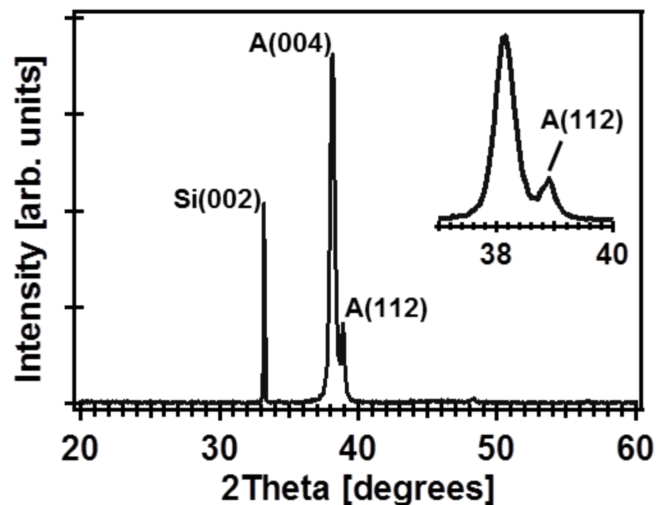

Figure 3.10. X-ray diffraction pattern for a 100 nm thick anatase TiO_2 film grown by ALD on STO-buffered Si(001) at 225 °C. The sample was post-deposition annealed at 600 °C for 1 hr. (inset) Relative positioning between the anatase (004) and (112) reflections.

3.4. SUMMARY

Epitaxial anatase TiO_2(001) thin films were grown on STO-buffered Si(001) by ALD. By using at least 4 unit cells of MBE-grown STO on silicon, a stable template is

created for epitaxial TiO_2 growth by ALD. The STO template remains stable even upon exposure to ambient, provided that surface contamination is removed *in-situ* prior to ALD growth. There is a noticeable shift in the anatase (004) reflection to a higher 2θ-value than that of bulk anatase, indicating that the TiO_2 thin films have a compressed *c*-axis and an expanded *a*-axis, reducing the lattice mismatch to the STO-buffered Si(001) substrate. Using an STO-buffer layer as a surface template should be extendable to other crystalline oxide films to be monolithically integrated with silicon by ALD.

3.5. References

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Chapter 4: Crystallization and Annealing of TiO_2 on $SrTiO_3$-buffered Si(001) substrates

*Contents of this Chapter were published in J. Vac. Sci. Technol. B **30**, 04E111 (2012).*[II]

4.1. Introduction

Large efforts are currently being made to integrate multifunctional complex oxides with advanced semiconductor technology.[1,2] Molecular beam epitaxy (MBE) has been the primary means of growing epitaxial oxides on silicon, largely due to its precise control of atomic layer-by-layer deposition. In the last decade, an increasing number of functional oxides have been grown on silicon by MBE provided an elemental source is available. However, in practice, there are difficulties in growing some oxide heterostructures by MBE. For example, MBE growth requires accurate elemental flux rates, which are typically measured by a quartz crystal microbalance. This measurement can be difficult to make when there is a relatively low flux due to low vapor pressures from the elemental source (*e.g.*, Ti). In addition, high temperature MBE deposition in the presence of oxygen often results in an amorphous SiO_x layer at the STO-Si interface.[3,4]

Atomic layer deposition (ALD) provides a potential chemical route for the growth of epitaxial oxide films. ALD entails the sequential delivery of precursors or reagents that either adsorb to saturation coverage or undergo selective ligand reactions, which are self-limiting, leading to film growth.[5,6] It is in effect a chemical vapor deposition technique based on sequential, self-terminating, gas-solid reactions. Unlike MBE, the surface coverage by a precursor is constrained because the surface reactions are self-

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[II] M. D. McDaniel, A. Posadas, T. Q. Ngo, A. Dhamdhere, D. J. Smith, A. A. Demkov, and J. G. Ekerdt, "Growth of epitaxial oxides on silicon using atomic layer deposition: Crystallization and annealing of TiO_2 on $SrTiO_3$-buffered Si(001)," J. Vac. Sci. Technol. B **30**, 04E111-(1-6) **(**2012**)**. MDM designed and performed experiments. MDM, AP, TQN, AAD, and JGE contributed to the conception and analysis of data. AD and DJS acquired transmission electron microscopy data.

limiting. Under the appropriate operating conditions, this facilitates stoichiometric growth of the desired oxide. Thus, ALD enables alternative manufacturing routes, growth over large area substrates, thicker film growth, and potentially easier integration of multifunctional oxide heterostructures on silicon.

Regardless of the growth method, there are often problems with growing epitaxial oxides directly on silicon due to the formation of amorphous SiO_2, as well as silicates and/or silicides at the interface.[7,8] Strontium titanate (STO) is one of the few oxides that can be grown epitaxially on Si(001) without interface reactions.[9,10] For epitaxial structures to form, the lattice constants of the film and substrate must be reasonably well matched. The lattice mismatch between STO and Si(001) is relatively small (+1.7 %) with a 45° in-plane rotation, with the STO compressively strained to Si. Anatase TiO_2 exhibits a square surface mesh in the (001) orientation, as does bulk STO, creating a nominal lattice mismatch of (-3.1 %). However, since thin epitaxial STO films are perfectly strained to the underlying silicon substrate,[11] the lattice mismatch between anatase TiO_2 and the STO-buffered silicon should be smaller (-1.4 %).

The growth of epitaxial STO on Si(001) allows for large-area STO pseudo-substrates, which serve as surface templates to integrate functional oxides on silicon substrates.[12-21] For example, pure-phase and Co-doped anatase TiO_2 films have been deposited by MBE on Si(001) substrates using thin STO buffer layers.[22] For many applications, such as high-*k* dielectrics or advanced oxide electronics, the existence of an amorphous SiO_x layer at the STO-Si interface is undesirable. MBE growth of epitaxial TiO_2 on STO-buffered Si(001) resulted in an amorphous SiO_x layer,[22] which occurred primarily during deposition of the anatase TiO_2. Both the high temperature and oxygen environment required during MBE deposition contribute to the amorphous SiO_x formation. Since the oxygen environment is necessary for growing an oxide film, a

method for deposition at lower temperature is required for integrating epitaxial TiO_2 on STO-buffered Si(001) without significant SiO_x formation.

In our system, a customized ALD chamber has been integrated with a MBE system, allowing *in situ* transfer of samples, and enabling the study of epitaxial oxide films grown by ALD on surface templates grown by MBE. Our earlier work indicated that an amorphous SiO_x layer existed at the STO-Si interface when TiO_2 films were deposited by ALD and vacuum-annealed at 600 °C.[23] By using *in situ* X-ray photoelectron spectroscopy (XPS) analysis and transmission electron microscopy (TEM), the study herein examines the STO-Si interface before and after the deposition of TiO_2 by ALD, as well as before and after annealing. We report the crystallization and effects of annealing for epitaxial anatase TiO_2 grown by ALD on STO-buffered Si(001) substrates.

4.2. EXPERIMENTAL DETAILS

The ALD system consists of a custom-built, hot-wall stainless steel rectangular chamber that is approximately 20-cm long, with a reactor volume of 460 cm^3, as described in more detail elsewhere.[23] The ALD system is connected to a transfer chamber that allows *in situ* transfer of samples from the MBE system (DCA 600) to the ALD chamber. Substrate samples are 20 × 20 mm^2 silicon wafers held in a molybdenum puck (5 cm diameter) that can be used in both the ALD chamber and MBE system, enabling *in situ* sample transfer and growth on well-characterized and specially prepared surfaces. During ALD growth, the carrier/purge gas (argon) and precursor are introduced through a common manifold at the front of the chamber. The chamber is continually evacuated during deposition by a dual-stage rotary vane pump with a peak pumping speed of 6 cfm, which maintains the operating pressure near 1100 mTorr.

The MBE system was used to grow crystalline STO directly on Si(001) using a variant of the Motorola-developed process.[24] The substrates were prime Si wafers with nominal 2 nm of native oxide that were cut to 20 × 20 mm^2, then ultrasonically cleaned with acetone, isopropyl alcohol, and deionized water for 5 min each, followed by UV/ozone exposure for 15 min to remove residual carbon contamination. The silicon substrate was then loaded into the chamber and the native oxide was desorbed using a Sr-assisted deoxidation process.[25] After achieving a clean Si(001) surface with 2 × 1 reconstruction, a half monolayer of Sr metal is deposited on the Si substrate at 600 °C forming the strontium silicide template layer. The MBE chamber is equipped with an 18 keV reflection high-energy electron diffraction (RHEED) system for monitoring structural morphology during growth. In order to ensure that the underlying Si is not oxidized during the initial STO deposition, the substrate is cooled to below 200 °C and molecular oxygen is ramped from 5×10^{-8} Torr to 2×10^{-7} Torr over several min. Sr and Ti are co-deposited from effusion cells during oxygen ramping at a rate of one monolayer per minute to a thickness of four unit cells of STO. Oxygen is then removed and the film is annealed at 550 °C under vacuum to crystallize the STO layer, as verified by RHEED. The STO-buffered Si(001) pseudo-substrate is then transferred *in situ* to the ALD chamber.

Epitaxial anatase (TiO_2) thin films were grown by ALD at 250 °C using titanium isopropoxide $\{Ti[OCH(CH_3)_2]_4\}$ (TTIP) and water as the co-reactants on the MBE-grown single crystal STO/Si(001) templates; the precursors were held at 40 °C and 25 °C, respectively. Under these conditions, both TTIP and water saturate the substrate surface within 1 sec. One deposition cycle consisted of a 1-sec pulse of the Ti precursor, a 10-sec purge with Ar, a 1-sec pulse of H_2O, and a 10-sec purge with Ar, noted as 1/10/1/10 × *N*, where *N* is the number of ALD cycles. Argon was used as the carrier gas to deliver

the Ti precursor and purge gas between reactant dosing, maintaining the operating pressure at 1.1 Torr. Films were characterized using XPS, X-ray reflectivity (XRR), spectroscopic ellipsometry (SE), RHEED, and X-ray diffraction (XRD).

XPS was performed *in situ* with an Al Kα source at 1486.6 eV using a VG Scienta R3000 XPS system to determine the film composition and to verify the absence or presence of SiO_x at the STO-Si interface. All XP spectra were analyzed using a uniform shift based on the Si $2p_{3/2}$ elemental peak to 99.3 eV. To allow for *in situ* XPS analysis, TiO_2 films grown by ALD had to be sufficiently thin so that the Si 2*p* peaks could still be resolved. Thus, between 100 and 150 ALD cycles were used for the *in situ* XPS studies to give approximately 3 to 5 nm thick TiO_2 films, respectively. The samples could then be annealed *in situ* to examine the effect of annealing on the STO-Si interface.

After deposition, the TiO_2 film thicknesses were measured by XRR and verified by SE. These two methods were found to be in good agreement within experimental error (±0.3 nm for a 5-nm film). The growth rate under these conditions was found to be 0.31 Å/cycle, as reported previously.[23] Both RHEED and XRD were used to evaluate the orientation and crystallinity of the TiO_2 films. XRD and XRR were conducted with a Bruker-AXS D8 Advance Powder Diffractometer using a sealed tube Cu Kα radiation. Film thicknesses were verified by SE using a J.A. Wollam M2000D Spectroscopic Ellipsometer.

Cross-sectional transmission electron microscopy (TEM) was performed on the crystalline TiO_2 film after annealing. The sample was prepared using standard mechanical polishing followed by argon-ion-milling to perforation. Observations were made with a 400-keV high-resolution electron microscope (JEM-4000EX) equipped with a double-tilt specimen holder.

4.3. RESULTS AND DISCUSSION

4.3.1. Crystallization of as-deposited TiO_2 on STO-buffered Si(001)

Figures 4.1(a) and 4.1(b) show the RHEED patterns of a typical STO-buffered Si(001) substrate with four unit cells of STO; as taken along the [100] and [110] directions, respectively. The well-defined streaks in the RHEED images are indicative of a highly crystalline and atomically smooth STO film. This stable template is then transferred to the ALD system, and the desired thickness of TiO_2 is grown by ALD. Figures 4.1(c) and 4.1(d) show RHEED patterns of a 15-nm thick TiO_2 film after ALD, again taken along the [100] and [110] directions, respectively. The patterns have been aligned so that the relationship between the TiO_2 film and the substrate can be observed. The TiO_2 film is highly oriented with the substrate, as shown by the alignment of the streaks. There is a faint appearance of a 2× reconstruction along the [110] azimuth, consistent with previous studies of epitaxial anatase TiO_2 thin films.[26,27] In addition, the increase in intensity modulation along the streak direction in the TiO_2 RHEED patterns indicates an increase in surface roughness due to the ALD process compared with the MBE-grown STO.

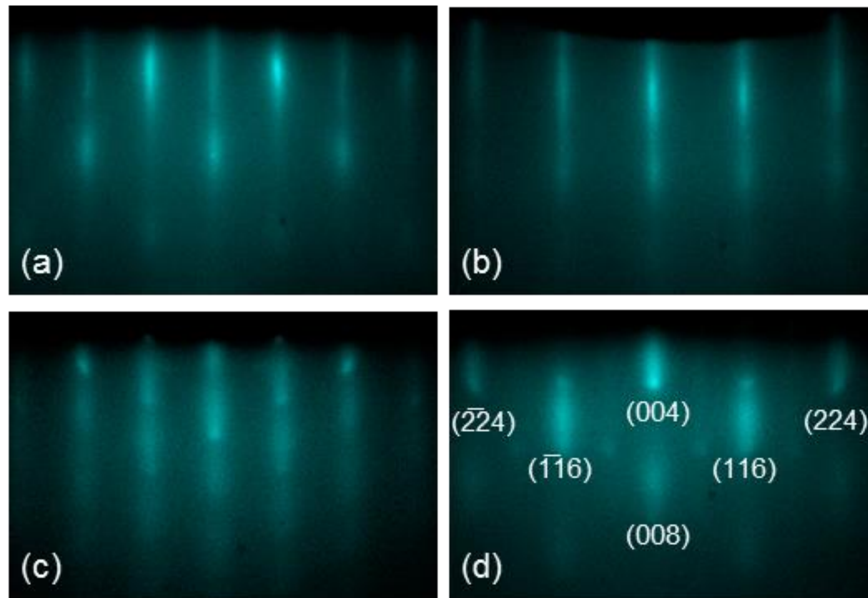


Figure 4.1. RHEED images obtained before [(a), (b)] and after [(c), (d)] ALD growth of a 15-nm thick anatase TiO_2 on four-unit cell STO-buffered Si(001) at 250 °C. The sample was post-deposition annealed in vacuum at 250 °C for 1 hr. The beam is aligned along the [100] for (a) and (c), and [110] azimuth for (b) and (d).

XRD of the as-deposited TiO_2 films verified the crystal structure and preferred orientation of the TiO_2 films. The films grown by ALD were highly *c*-axis oriented anatase, as indicated by the sole presence of the (004) reflection. A typical XRD pattern for a 15-nm thick TiO_2 film grown using the template method is shown in Fig. 4.2. The (004) reflection is shifted from that of anatase powder ($2\theta \approx 37.9°$) to a slightly higher value ($2\theta \approx 38.5°$), indicating that the c lattice constant of this anatase film is 9.346 Å. This value is consistent with an increased a lattice parameter relative to that of bulk anatase, which reduces the in-plane lattice mismatch of anatase TiO_2 with the substrate. Similar behavior has been previously reported for epitaxial anatase TiO_2(001) films grown on STO(100) single crystal by MBE.[28,29] In our case, the TiO_2 is tensile strained to the STO, which is compressively strained to Si. The Poisson ratio, ν, for anatase TiO_2

is not well known experimentally; however, it may be estimated theoretically from the calculated bulk and shear modulus.[30] Using the theoretical value ($\nu = 0.35$), the anatase (004) reflection should be shifted to a value of $2\theta \approx 38.5°$, assuming the TiO_2 is perfectly strained in-plane to the underlying Si (a = 3.84 Å). Therefore, our values obtained experimentally are consistent with full biaxial strain of the 15-nm thick anatase TiO_2 to the Si substrate. For a 20-nm thick anatase TiO_2 film, the anatase (004) reflection is shifted to a value of $2\theta \approx 38.4°$, indicating that thicker films begin to relax towards the bulk value of anatase powder ($2\theta \approx 37.9°$).

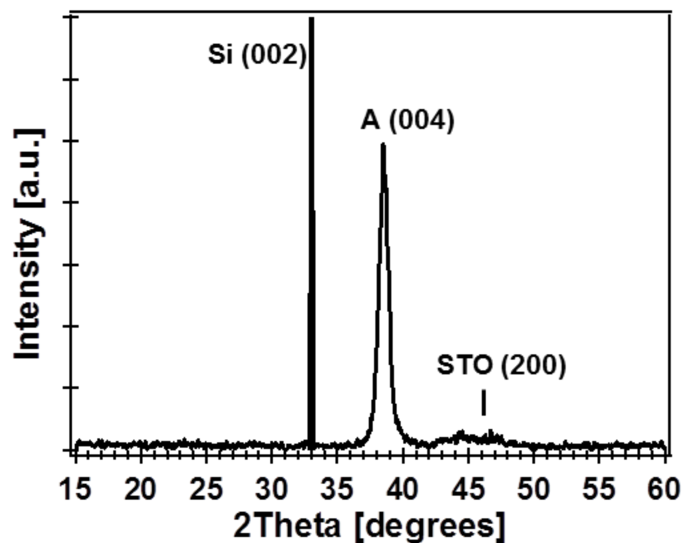


Figure 4.2. X-ray diffraction pattern for a 15-nm thick anatase TiO_2 film grown by ALD on STO-buffered Si(001) at 250 °C. The sample was post-deposition annealed in vacuum at 250 °C for 1 hr.

To determine the degree of out-of-plane orientation, a rocking curve analysis was performed around the (004) reflection, giving a full-width half maximum (FWHM) of 1.9° (Fig. 4.3). The epitaxial relationships between anatase TiO_2 and the substrate were determined by an off-axis φ-scan on the {105} reflections of anatase and the {115}

reflections of silicon. The anatase film was aligned such that $(001)_{anatase}$ $\|(001)_{STO}\|(001)_{Si}$ and $(100)_{anatase}$ $\|(100)_{STO}\|(110)_{Si}$.

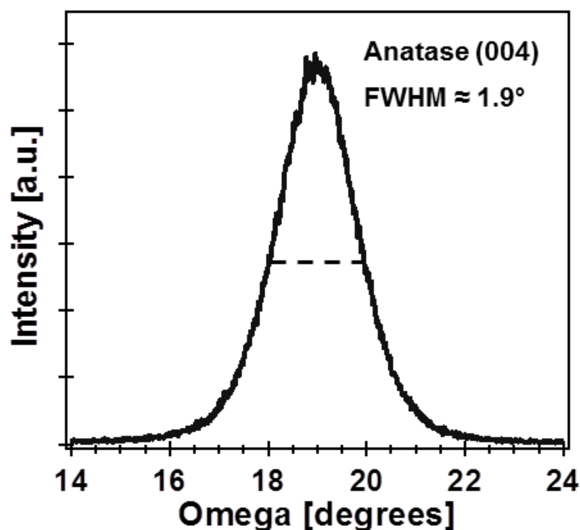


Figure 4.3. Rocking curve of the anatase (004) reflection at a fixed 2θ = 38.5° for a 15-nm thick film grown by ALD on STO-buffered Si(001) at 250 °C. The sample was post-deposition annealed in vacuum at 250 °C for 1 hr.

4.3.2. In situ XPS study of STO-Si interface before and after TiO_2 ALD growth

MBE has been shown to grow high-quality STO on silicon without the formation of SiO_2.[9-11] However, the H_2O pulse during ALD could lead to formation of some oxidized silicon (SiO_x) despite the care taken to prevent SiO_x formation during the STO growth. To examine the impact of the ALD growth on the STO-Si interface, *in situ* XPS analysis was utilized.

A standard four-unit cell STO template was grown by MBE and transferred to the XPS analysis chamber, where XPS scans were collected (Si 2*p*, Sr 3*d*, Ti 2*p*, O 1*s*, and C 1*s*). The sample was then moved to the ALD chamber and exposed to 100 cycles of TiO_2 using the standard dosing conditions. The resulting TiO_2 thin film was highly ordered as indicated by the RHEED pattern (not shown). The total oxide film thickness was

approximately 4.6 nm (1.5 nm STO from MBE plus 3.1 nm TiO_2 from ALD). After TiO_2 deposition, the sample was transferred back into the XPS analysis chamber. The XPS scans of the Si 2*p* peak before and after ALD growth are shown in Fig. 4.4. Suboxides of silicon (SiO_x where $x < 2$) would produce Si 2*p* features between 99.3 eV and 103.3 eV. As can be seen, MBE growth of STO on Si does not result in the oxidation of Si at the STO-Si interface. Surprisingly, no increase in Si-O bonding is observed due to the ALD growth as well. Thus, the relatively low ALD temperature (250 °C) did not cause oxidation of Si at the interface.

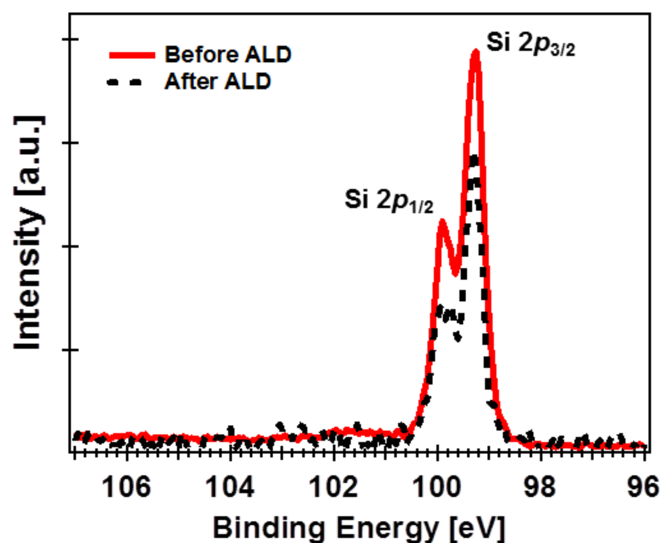


Figure 4.4. X-ray photoelectron spectrum of Si 2*p* shown before (red curve) and after 100 ALD cycles (black curve), indicating negligible Si-O bonding after ALD. (The intensity scaling has been adjusted for clarity.)

These results indicate a potential advantage to integrating epitaxial oxides on silicon when using ALD. Specifically, the formation of amorphous SiO_x may be avoided due to the lower deposition temperature for ALD compared to that required to grow the same film using MBE.

4.3.3. Annealing, crystallization, and in situ XPS of the STO-Si interface after annealing

To improve the crystallinity of the anatase TiO_2 films, *in situ* annealing was done in vacuum (10^{-9} Torr). Initially, films were annealed at a temperature of 600 °C for 1 hr with a ramp rate of 30 °C/min. The (004) reflection of equivalent 18-nm thick anatase films showed a slight increase in sharpness after annealing (Fig. 4.5), where the FWHM of the θ-2θ scan was reduced from 0.69° to 0.64°. Moreover, the anatase (004) reflection is shifted to a lower value ($2\theta \approx 38.2°$). This indicates that the TiO_2 film relaxes towards its bulk value ($2\theta \approx 37.9°$) during high-temperature annealing. Similar effects have been observed for STO thin films on Si(001) substrates.[31] To determine the amount of out-of-plane orientation after annealing, a rocking curve measurement around the (004) reflection of the annealed sample was made, giving a FWHM of 1.4° (not shown). This indicates a slight improvement in crystallinity of the annealed TiO_2 film.

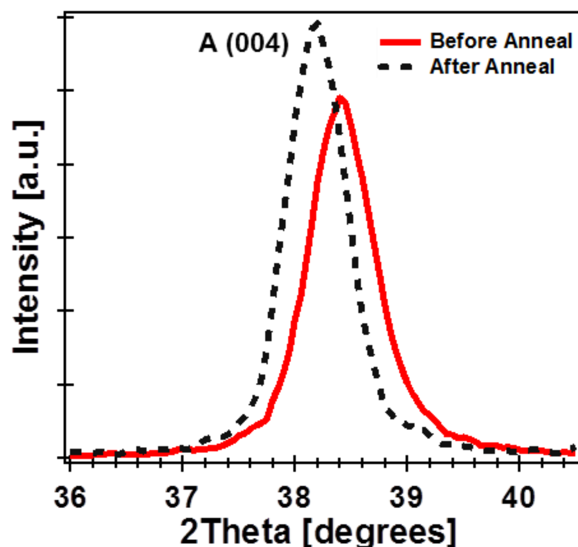


Figure 4.5. X-ray diffraction pattern of the (004) reflection for a 20-nm thick anatase TiO_2 film grown by ALD on STO-buffered Si(001) before (red curve, $2\theta \approx 38.5°$) and after vacuum anneal at 600 °C for 1 hr (black curve, $2\theta \approx 38.2°$). The FWHM before and after annealing is 0.69° and 0.64°, respectively.

Cross-sectional TEM observations of an 18-nm thick TiO_2 film annealed at 600 °C for 1 hr revealed that the TiO_2 was highly-crystallized and well oriented with the substrate (Fig. 4.6 (left)). However, a significant amorphous SiO_x layer was visible at the STO-Si interface with a thickness estimated to be 2.2 nm. The STO-Si interface did not have any SiO_x present after the ALD process (Fig. 4.4). Thus, Fig. 6 suggests that vacuum annealing of the TiO_2 film has resulted in oxidation of the Si, forming an amorphous SiO_x layer at the STO-Si interface. Additional cross-sectional TEM analysis of an as-deposited TiO_2 sample (Fig. 4.6 (right)), shows the ALD film is crystalline as deposited with minimal interfacial oxide (< 2 Å) at the STO-Si interface. The presence of a non-zero amorphous layer may be partially attributed to ion-milling which tends to amorphize materials with weaker bonds during the final thinning to transparency.

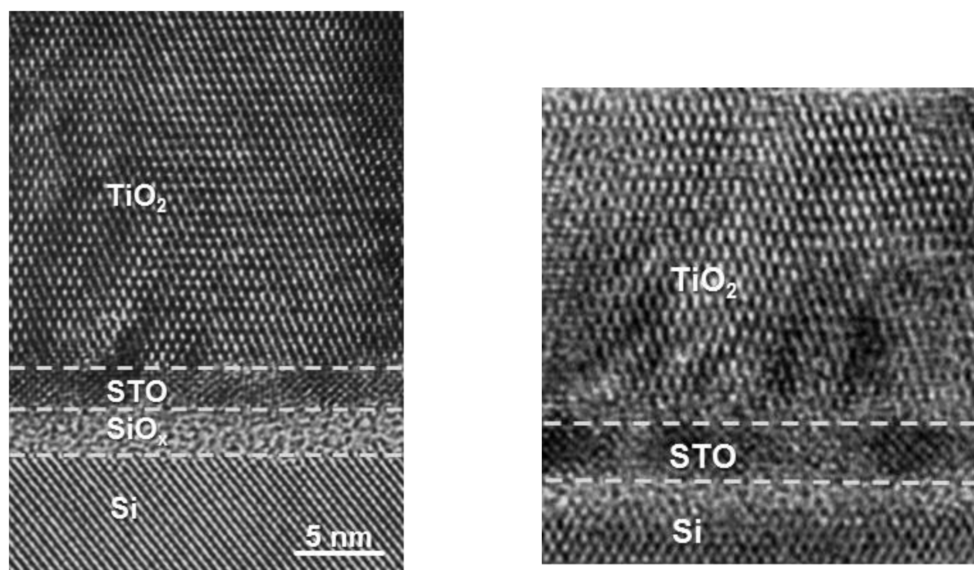


Figure 4.6. High-resolution transmission electron micrographs showing cross section of (left) 18-nm thick anatase TiO_2 film grown by ALD on STO-buffered Si(001) where the sample was post-deposition annealed in vacuum at 600 °C for 1 hr, and (right) an as-deposited 10-nm thick anatase TiO_2 film grown by ALD on STO-buffered Si(001).

In situ XPS analysis verified that the amount of Si-O bonding had increased after annealing. Although the post-deposition processing was done in the absence of oxygen, the TiO_2 film most likely provided sufficient oxygen to favor Si oxidation. To explore this possibility further, additional samples were annealed at temperatures of 450 °C, 300 °C, and 250 °C. Fig. 4.7(a) shows a plot of the Si 2*p* peak after each of the annealing treatments, as well as a representative Si 2*p* peak after 100 cycles of ALD. Even at the moderately low annealing condition of 300 °C for 1 hr, a small peak indicative of Si-O formation is visible. Moreover, XPS analysis verified that oxygen was removed from the TiO_2 film. Figure 4.7(b) shows the Ti 2*p* peak after each of the annealing treatments (450 °C, 300 °C, and 250 °C). The as-deposited film indicates that only the Ti^{4+} species is present, consistent with TiO_2. However, vacuum annealing has induced the presence of Ti^{3+} species, indicating that oxygen has been removed from the TiO_2 film to the STO-Si interface where the Si surface is oxidized. Similar studies (not presented) have shown that pure STO films on Si subjected to similar annealing conditions do not show reduced Ti species.

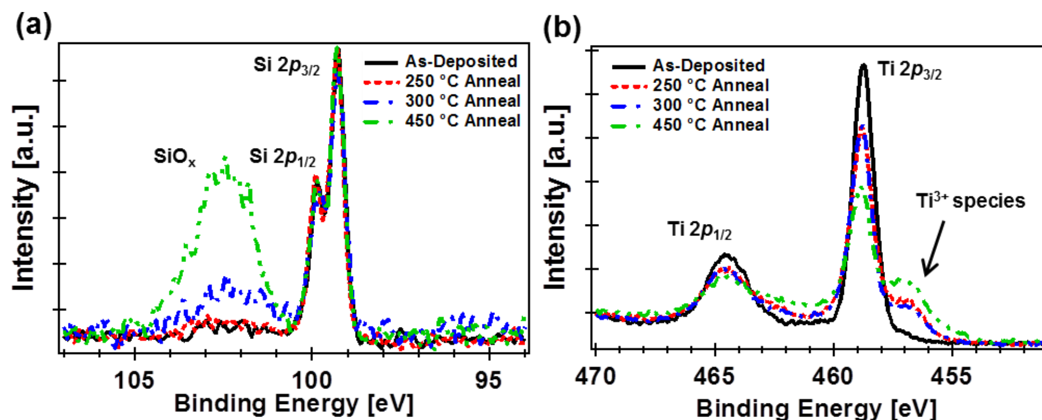


Figure 4.7. X-ray photoelectron spectra of the (a) Si 2p and (b) Ti 2p after annealing at 250 °C, 300 °C, and 450 °C. Samples were exposed to 100 cycles of ALD (3 nm TiO_2) on STO-buffered Si(001).

Therefore, a delicate balance exists in the TiO_2/STO/Si(001) heterostructure. Thermochemical analysis of possible reactions between TiO_2 and Si has shown that reduction of TiO_2 to Ti_2O_3 and Ti_3O_5 is thermodynamically favored,[32] which is consistent with the presence of Ti^{3+} species after annealing. At the low ALD temperature (250 °C), the reduction of TiO_2, and initial oxidation of Si, is most likely limited by the diffusion of oxygen through the STO buffer layer. Once a layer of SiO_x is formed at the STO-Si interface, it is expected that reaction kinetics and/or oxygen ion diffusion across the SiO_x layer limits the total amount of SiO_x formed. Oxygen ion diffusion through single crystal STO is known to increase exponentially with temperature.[33-36] Using the diffusivity relation developed by Paladino *et al.*,[33] the oxygen diffusion length is estimated to increase from 3 nm to over 880 nm for one hour annealing at temperatures of 250 °C and 600 °C, respectively. This is consistent with the results of this study, where the initial oxidation of Si below the STO buffer layer is limited when both the ALD and post-deposition annealing temperatures do not exceed 250 °C.

4.4. Resistive Memory Application

4.4.1. Controllable and stable quantized conductance and resistive switching mechanism in single-crystal TiO_2 resistive memory on silicon

Details of this section are published in Nano Lett. ***14****, 4360-4367 (2014) in collaboration with Chengqing Hu from Prof. Edward Yu's group at the University of Texas at Austin.*

We report a detailed analysis of the resistive switching (RS) characteristics of single-crystal anatase-TiO_2 thin films epitaxially grown on silicon by atomic layer deposition. We demonstrate that although the valence change mechanism is responsible

for the observed RS, single-crystal anatase-TiO_2 thin films show electrical characteristics that are very different from the usual switching behaviors observed for polycrystalline or amorphous TiO_2, and instead very similar to those found in electrochemical metallization memory. In addition, we demonstrate highly stable and reproducible quantized conductance that is well controlled by application of a compliance current and that suggests the localized formation of conducting Magnéli-like nanophases. The quantized conductance observed results in multiple well-defined resistance states suitable for implementation of multilevel memory cells.

Key Results of TiO_2 Resistive Memory

The device structure for the epitaxial TiO_2 resistive RS cells is shown schematically in Fig. 4.8(a). The typical RS *I*–*V* characteristics of such a device, shown in Fig. 4.8(b), exhibits linear *I*–*V* behavior in the low-resistance state (LRS) and abrupt, clean RS for both SET and RESET processes.

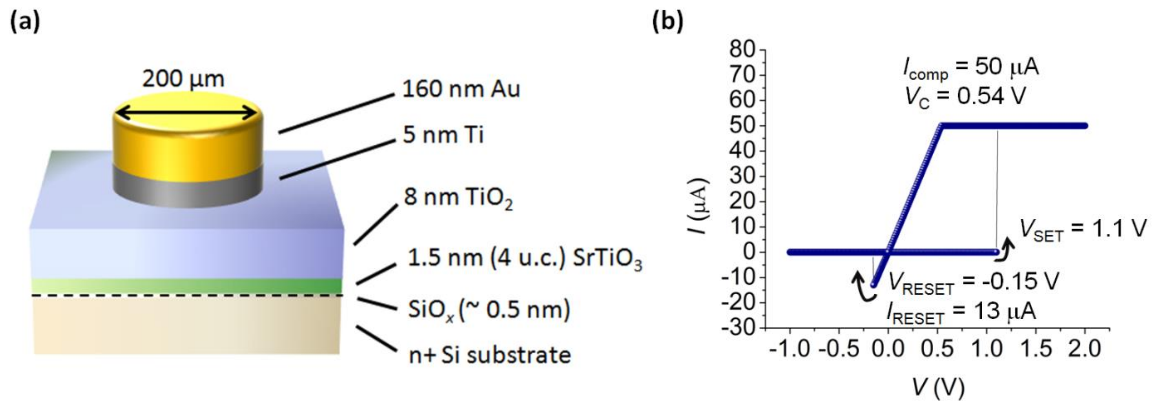


Figure 4.8. (a) Device structure for single-crystal TiO_2 cells; (b) typical *I*–*V* characteristics.

For the TiO_2 devices in this work, however, I_{reset} is smaller than I_{comp} over a wide range of I_{comp}, as shown in Fig. 4.9(a), and the power dissipation at which RESET occurs

is therefore smaller than the power dissipated by the device in the ON state following the SET process for nearly all the different I_{comp} values tested. Fig. 4.9(b) shows the *I–V* characteristics of a set of dc double sweeps (i.e., an upsweep followed by a downsweep), each starting from $V = 0$ V but with I_{comp} increasing in 0.1 mA steps. The first sweep is with $I_{comp} = 0.4$ mA, right after the SET process under the same I_{comp}. It can be seen that for the following sweeps with I_{comp} incrementally increasing, R_{LRS} is always very stable and maintains the same value as that for the first sweep with $I_{comp} = 0.4$ mA. Even with I_{comp} for the last sweep at 1.0 mA, which is much larger than the corresponding $I_{reset} \sim$ 0.38 mA during the follow-up negative voltage sweep (not shown), R_{LRS} remains at the same value, indicating that the conductive filament (CF) formed in the SET process is highly stable against either growing or rupturing. Positive voltage sweeps with $I_{comp} = 10$ mA and the same voltage peak value and sweep rate as for the former SET process (for which $I_{comp} = 10$ μA–1 mA) were also performed (not shown); no unipolar RS (URS) behavior was observed under this condition. This observation together with Figs. 4.9(a) and (b) unambiguously excludes the possibility of interpreting the RESET process as mainly being the result of heat-induced rupturing of the CF. It should be noted, however, that Joule heating could still play a minor role for the RESET processes in this material system, and thermochemical-based URS could potentially be achieved in our system by applying a voltage sweep with I_{comp} much larger than 10 mA.

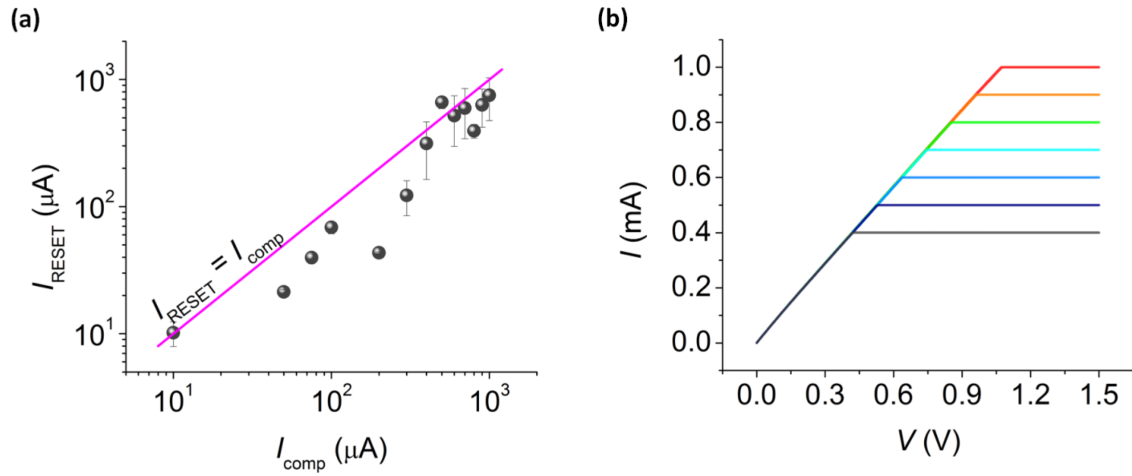


Figure 4.9. Electrical characteristics for the single-crystal TiO_2 device which contradict with those of thermochemical or heat-induced RS mechanism. (a) I_{RESET} vs. I_{comp} for I_{comp} ranging from 10 μA to 1 mA; (b) I–V characteristics of a set of dc double sweeps, each starting from $V = 0$ V but with an incremental I_{comp} (from 400 μA to 1 mA), after the SET process under $I_{\mathrm{comp}} = 400$ μA.

Fig. 4.10(a) compares R_{LRS} (after SET at $I_{\mathrm{comp}} = 500$ μA) for top electrodes of different sizes (80 μm, 100 μm, 150 μm, and 200 μm in diameter, respectively), where R_{LRS} is found to be almost constant over different device sizes, suggesting the filamentary nature of the LRS. Shown in Fig. 4.10(b) is R_{LRS} as a function of temperature (278–338 K) around room temperature for a particular ON-state of the 200 μm device after SET at $I_{\mathrm{comp}} = 500$ μA. R_{LRS} is clearly seen to be essentially constant, increasing by less than 1 Ω when the temperature increases from 278 K to 338 K, indicating that ballistic conduction across a nanoscale channel, with minimal additional series resistance, occurs. Therefore, we conclude that the filamentary-type valence change switching mechanism applies to the RS of our materials stack, i.e., Au/Ti/single-crystal anatase TiO_2/STO/n+ Si.

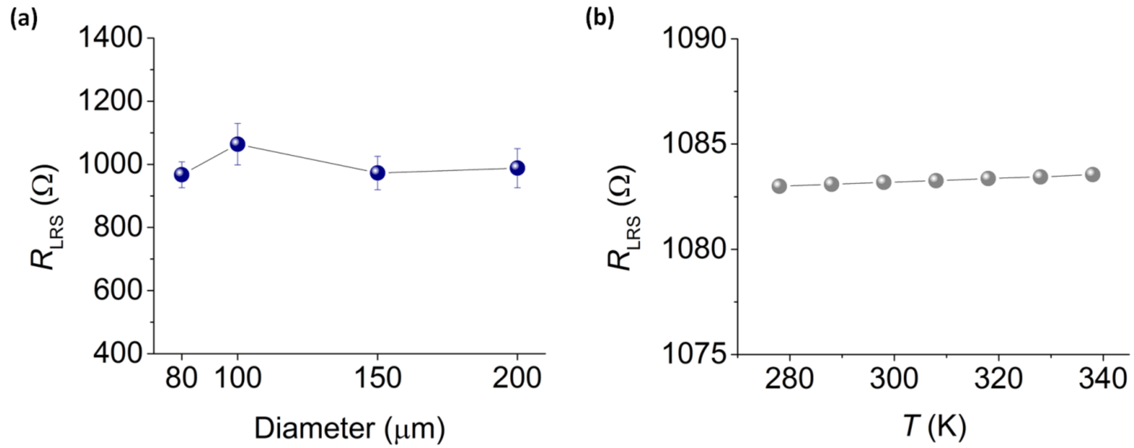


Figure 4.10. (a) R_{LRS} vs. device size (in diameter) after SET processes (30 SET processes for each device size) under I_{comp} = 500 μA, showing no dependence of R_{LRS} on the device electrode area; (b) R_{LRS} vs. T for a particular ON-state of the 200 μm diameter device after SET under I_{comp} = 500 μA, demonstrating a metallic conduction behavior in the LRS.

The filamentary-type valence change based switching mechanism for the single-crystal TiO_2 device is therefore proposed to be as follows. In an as-fabricated TiO_2 device, an oxygen-deficient layer is only present at the top of the TiO_2 layer due to the top Ti metallization, as shown in Fig. 4.11(a). We have determined experimentally that a single-crystal TiO_2 device is not switchable with a pure Au top electrode (specifically, for an 80 s double sweep of voltage with a peak voltage of +5 V). A top oxygen-deficient layer, serving as a reservoir of oxygen vacancies, helps to achieve a very high ON/OFF ratio without causing hard breakdown of the RS active layer.

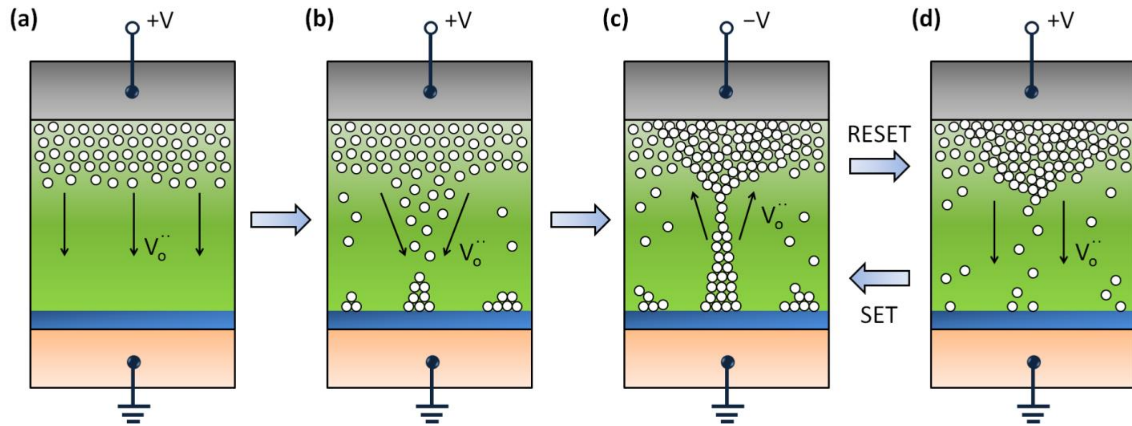


Figure 4.11. Schematic of the proposed RS mechanism based on the *I*–*V* characteristics. Voltage is applied to the top contact after the depicted oxygen vacancy configuration is achieved within the TiO_2 matrix, and the arrows denote moving direction of oxygen vacancies upon application of voltage to the top contact. Oxygen vacancy configuration (a) in the pristine state, (b) during the SET process, (c) in the ON state, and (d) in the OFF state.

By applying a positive bias voltage to the top contact, oxygen vacancies drifting from the top oxygen-deficient layer are partially reduced and re-deposited upward from the bottom, *i.e.*, the TiO_2/STO interface (Fig. 4.11(b)). This process leads to localized formation of a CF, assisted by local roughness of the oxygen vacancy cluster distribution at the bottom that enables CF nucleation at a local asperity, to complete the SET process (Fig. 4.11(c)). During the RESET process, the CF dissolves owing to the electrochemical current through the TiO_2 matrix, followed by the electric-field driven oxygen vacancy drift back to the top, as shown in Fig. 4.11(d). Fig. 4.12(a) shows that the pristine-state current (i.e., OFF-state current before electroforming) is the same order of magnitude as the subsequent OFF-state current. This indicates that during the last stage of the RESET process, most of the dissolved positively-charged oxygen vacancies are driven by the large electric field back toward the top electrode, leaving the single-crystal anatase TiO_2 layer beneath with very few oxygen vacancies. On the other hand, the electroforming

threshold voltage is higher than the SET voltage, as shown for example in Fig. 4.12(a) and also observed for a wide range of SET compliance currents, indicating that during electroforming, additional oxygen vacancies are created by movement of oxygen atoms from the Ti/TiO_2 interface into the Ti electrode, lowering the threshold voltage for the subsequent SET processes. We also note that in Fig. 4.12(a), the *I*–*V* curve after RESET in the regular SET/RESET cycle does not go through the origin.

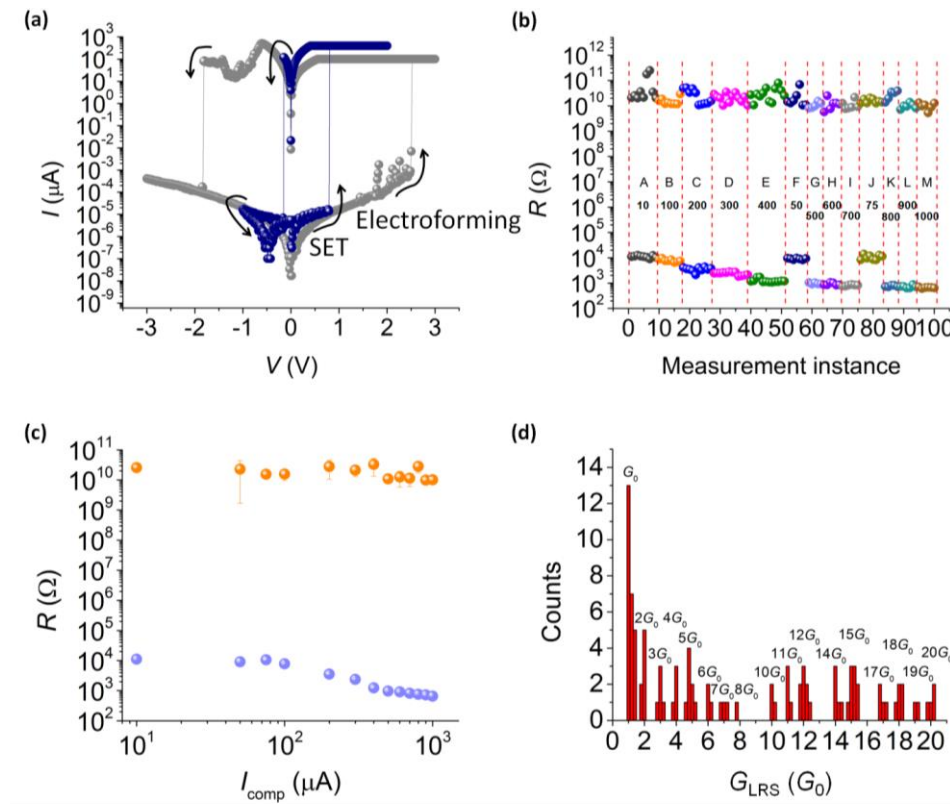


Figure 4.12. Electrical performance of an 8 nm thick single-crystal TiO_2 device. (a) Log *I*–*V* of typical RS characteristics of an electroforming sweep (grey) and a regular RS sweep (blue); (b) R_{HRS} and R_{LRS} over 100 successive switching sweeps, with letters A to M indicating different I_{comp} applied during SET process of those sweeps from 10–1000 μA; (c) R_{HRS} and R_{LRS} vs. I_{comp} based on the data shown in (b), where saturation of the R_{LRS} increase at smaller I_{comp} can be seen; (d) Histogram of G_{LRS} in units of $G_0 = 2e^2/h$ for the 100 successive cycles shown in (b), with discrete peaks for integers of G_0.

Fig. 4.12(b) shows R_{HRS} and R_{LRS} measured over 100 dc sweep cycles under I_{comp} ranging from 10 μA to 1 mA. Here, each R_{LRS} was measured right after a SET process under the corresponding I_{comp}, which is different from the measurement scenario for Fig. 4.9(b). Very high ON/OFF ratios of 10^6–10^7 are observed over the entire range of I_{comp}. This is unusual for filamentary-type valence change memory with a top electrode in the size range employed here (200 μm in diameter), for which the ON/OFF ratio is generally small due to the fact that filamentary RS only affects a tiny portion of the entire electrode area and the remaining electrode area normally contributes to a non-switching parallel resistance by means of electron tunneling or hopping through point defects (e.g., oxygen vacancies and/or reduced metal ions) within the insulating oxide matrix. In this respect, the single-crystal nature of the TiO_2 could play a key role, with high crystallinity and film quality helping to minimize the intrinsic defects, and greatly suppress the background electric current in both states of RRAM operation.

We also observe in Fig. 4.12(b) that while no apparent trend of R_{HRS} over the cycles can be seen, a stable and reproducible modulation of R_{LRS} by over one order of magnitude is achieved by varying I_{comp}, indicating the potential of using the single-crystal anatase TiO_2 material system for implementation of multilevel memory cells. Fig. 4.12(c) shows R_{HRS} and R_{LRS} as a function of I_{comp} in the log R – log I form, summarizing the data from Fig. 4.12(b). R_{HRS} is always above 10^{10} Ω over the entire range of I_{comp}, whereas R_{LRS} increases as I_{comp} decreases and eventually saturates at ~12.9 kΩ. It should be noted that in our measurements, the SET process does not occur for $I_{comp} < 10$ μA, from which we conclude that during the SET process a minimum compliance current is required to form and maintain a conductive nanofilament fully connecting the top and bottom electrodes. The saturation of R_{LRS} occurs at a resistance $R_0 = 1/G_0 = h/(2e^2)$, where h is Planck's constant and e is the magnitude of the electron charge. R_0 corresponds to the

intrinsic contact resistance of a single-mode ballistic conductor sandwiched between two conductive contacts.

The quantized nature of conductance in the LRS is shown more explicitly in Fig. 4.12(d), in which a histogram of the LRS conductance $G_{\mathrm{LRS}} \equiv 1/R_{\mathrm{LRS}}$ for the 100 successive cycles shown in Fig. 4.12(b) reveals a series of discrete peaks around integer multiples of G_0. To further elucidate the role of I_{comp} in determining the number of conductance channels n, histograms of G_{LRS} in units of G_0 for 390 switching cycles (30 cycles for each I_{comp}) performed on the same TiO_2 device as that for Fig. 4.12 are shown in Fig. 4.13 for compliance currents up to 1 mA. At compliance currents of 10–200 μA, histogram peak(s) corresponding to one or two quantized conductance values for each I_{comp} can be seen, and the number of conductance channels n increases with I_{comp}. Within this range of compliance current (10–200 μA), G_{LRS} can be controlled to within a single quantum of conductance by imposing a given I_{comp} during the device SET process. Since G_{LRS} is extracted from linear I–V characteristics in the LRS, good control over n and therefore over the thickness of a conductive nanofilament at or near the atomic scale via I_{comp} is demonstrated. At all of the higher compliance currents tested (300 μA–1 mA), corresponding to larger numbers of conductance channels, n can be controlled to within $\pm(0.5\text{–}1.5)G_0$, with the average number of conductance channels increasing with I_{comp} and reaching $(19\pm0.6)G_0$ for $I_{\mathrm{comp}} = 1$ mA. Fig 4.14(a) summarizes the data in Fig. 4.13 by plotting G_{LRS} vs. I_{comp}, with the mean and standard deviation of G_{LRS} for each I_{comp} shown in Fig. 4.14(b). An almost linear dependence of G_{LRS} on I_{comp} can be observed, indicating that the voltage drop across the TiO_2 RRAM cell at the compliance current, labeled as V_{C} in Fig. 4.8(b), is roughly constant (~0.5 V).

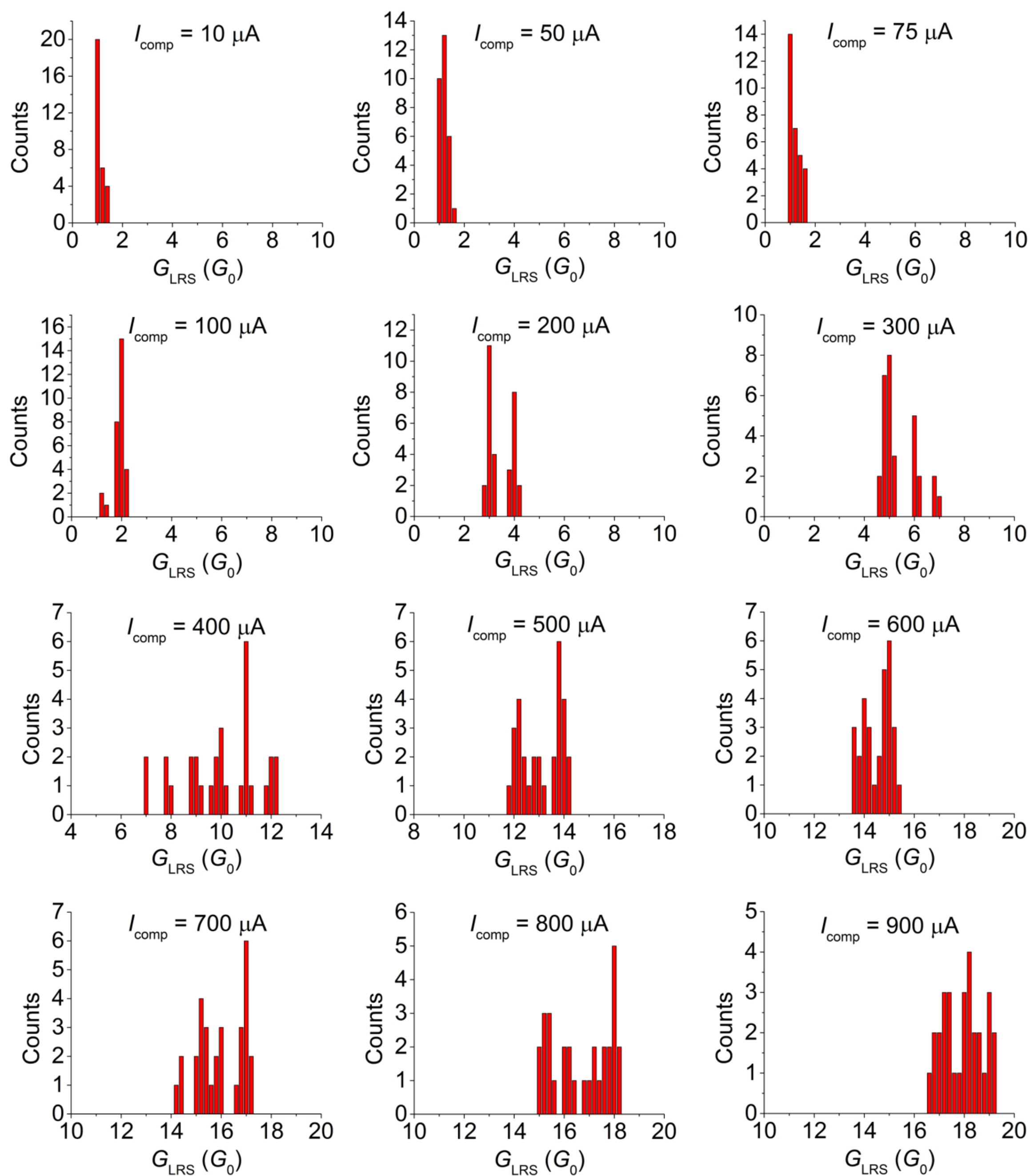
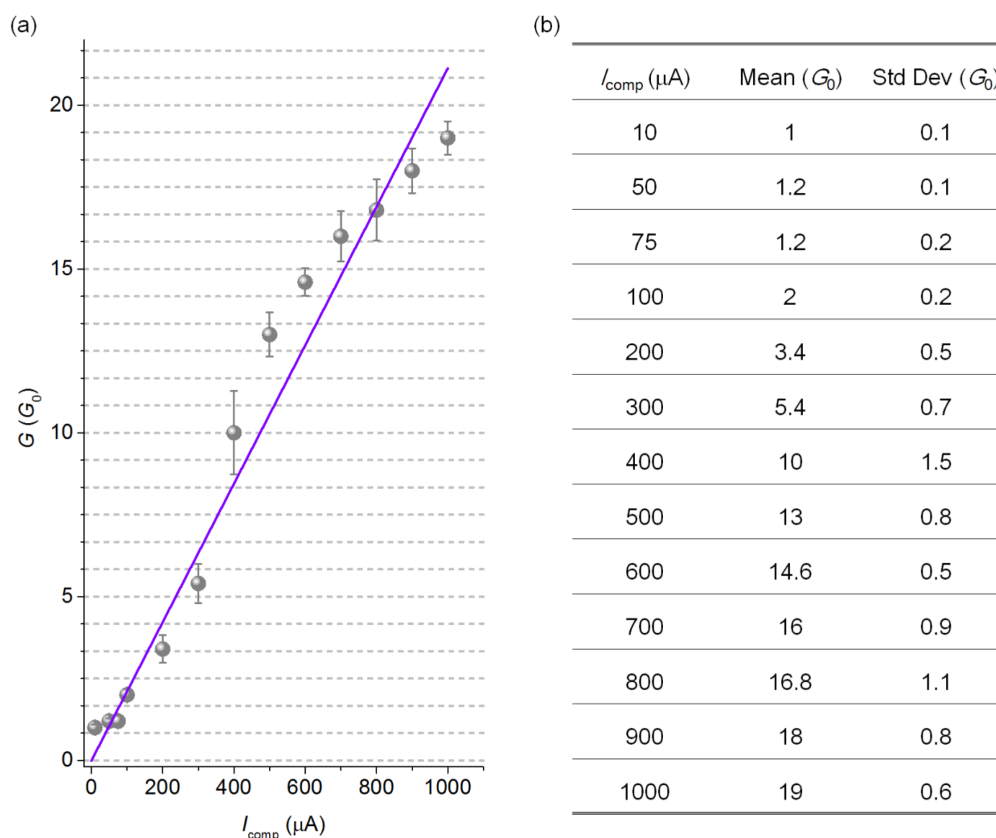


Figure 4.13. Histograms of G_{LRS} in units of $G_0 = 2e^2/h$ for the 390 cycles (including the 100 successive cycles in Fig. 5), with 30 cycles for each I_{comp}, showing effective modulation of the number of quantized channels by varying I_{comp}.

With regard to the formation of a single filament or multiple filaments at high compliance currents, we see in Fig. 4.9(b) that the CF is highly stable against further growth or rupturing at positive voltages once it is formed. In addition, it is widely known that regardless of the detailed RS mechanism, growth of a new CF is significantly suppressed after the cell is SET due to the combination of greatly decreased voltage drop across the cell upon SET and the exponential dependence of the CF growth rate on this voltage drop. Therefore, if a collection of independent nanofilaments were to account for the higher values of G_{LRS}, they would need to form essentially simultaneously at the SET voltage. In this case, however, it is very unlikely that there would be such a clear monotonic dependence of n on I_{comp} (Fig. 4.14), because the number of growing CFs before the cell is ON cannot be determined by I_{comp}. For $I_{\mathrm{comp}} \geq 600$ μA, i.e., $n \geq 14$–16, the observed distribution of values for G_{LRS} begins to become more continuous, as shown in Fig. 4.13. This can be understood as a consequence of the fact that for a thicker conductive nanofilament, the energy spacing between its subbands becomes smaller and eventually is comparable to or smaller than a few k_BT, in which case sharp transitions of conductance over adjacent n's are significantly smeared out. This also suggests the formation of a single thick nanofilament with a large n instead of a collection of several independent thin nanofilaments with small n's. It is therefore highly likely that only a single thick nanofilament is formed for the cases where $n \geq 2$.



I_{comp} (μA)	Mean (G_0)	Std Dev (G_0)
10	1	0.1
50	1.2	0.1
75	1.2	0.2
100	2	0.2
200	3.4	0.5
300	5.4	0.7
400	10	1.5
500	13	0.8
600	14.6	0.5
700	16	0.9
800	16.8	1.1
900	18	0.8
1000	19	0.6

Figure 4.14. (a) G_{LRS} vs. I_{comp} for I_{comp} ranging from 10 μA to 1 mA summarized from each histogram in Fig. 4.13; (b) mean and standard deviation values of G_{LRS} in units of G_0 in (a).

4.5. Summary

Epitaxial anatase TiO_2(001) films have been grown by ALD on Si(001) substrates using STO buffer layers without an amorphous SiO_x layer. *In situ* XPS analysis revealed that the ALD growth did not induce Si-O bonding at the STO-Si interface. However, *in situ* vacuum annealing at temperatures greater than 250 °C produced an amorphous SiO_x layer. *In situ* XPS also revealed that annealing produced Ti^{3+} species, indicating that oxygen was removed from the TiO_2 film and most likely served as the oxygen source for

Si oxidation at the STO-Si interface. ALD growth on the STO-buffered Si(001) template, with annealing at 250 °C for 1 hr, produced crystalline TiO_2 films with minimal SiO_x formation at the STO-Si interface. Suitable combinations of growth temperature and annealing conditions should allow epitaxial oxide films to be grown by ALD on Si(001) substrates without an amorphous SiO_x layer, using STO-buffer layers as surface templates.

Resistive memory applications were explored for epitaxial anatase TiO_2 grown on $SrTiO_3$-buffered Si substrates. Valence change-type bipolar RS (BRS) behavior observed in epitaxial single-crystal anatase TiO_2 thin film integrated on Si has been analyzed in detail, and highly controllable and reproducible quantized conductance has been demonstrated and analyzed. The electrical characteristics of the single-crystal anatase TiO_2 RRAM devices are shown to be very similar to those of electrochemical metallization rather than valence-change memory. Analysis of *I–V* characteristics reveals the metallic filamentary nature of the LRS and that the filamentary-type valence-change effect is responsible for the observed RS behavior. Highly stable quantized conductance (QC) for R_{LRS} was observed, and shown to be highly controllable by varying the compliance current. In this manner, R_{LRS} can be precisely modulated over one order of magnitude, which is indicative of the potential of single-crystal anatase TiO_2 RRAM devices for scaling to atomic dimensions, and their potential suitability for implementation of approaches for increasing memory storage density using multilevel cells. We postulate that the single-crystal nature of the film plays a key role in suppressing the background current and therefore in the emergence of QC, and provide evidence that different values of QC are attained via control over the atomic-scale dimensions of single conducting filaments. These results suggest that single-crystal anatase TiO_2 films epitaxially grown on Si are particularly intriguing and promising as a

platform for memory based on RS, and suggest a variety of directions for future explorations of performance, reliability, and scaling potential of these devices.

4.6. References

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Chapter 5: Epitaxial strontium titanate films grown by atomic layer deposition on $SrTiO_3$-buffered Si(001) substrates

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5.1. Introduction

ABX_3-type materials belonging to the perovskite family possess cubic or pseudocubic crystal structures. The ideal cubic structure has each A cation coordinated with twelve X anions, while each B cation is coordinated to six X anions. In this case, the ideal perovskite structure has a high degree of symmetry (space group Pm3m). Many crystalline oxides adopt the perovskite structure (ABO_3), although octahedral distortion and rotation is common, creating various pseudocubic phases. Their common structure, combined with an array of properties, make perovskite oxides attractive materials to study both theoretically and experimentally. Crystalline perovskites can be insulating or metallic, with many also being ferromagnetic,[1-3] ferroelectric,[4] multiferroic,[5] or superconducting.[6] This wide range of properties, combined with possibilities for lattice-matching during growth, allows for multi-functional heterostructures and superlattices to be engineered.[7-10]

Continuing the pace of growth and innovation in the semiconductor industry requires new materials, such as crystalline perovskite films, to be discovered and efficient processes for their manufacture and integration with silicon to be developed. Epitaxial oxide films and heterostructures integrated with silicon present an ideal platform to explore the fundamental materials physics and have numerous potential technology

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[III] M. D. McDaniel, A. Posadas, T. Q. Ngo, A. Dhamdhere, D. J. Smith, A. A. Demkov, and J. G. Ekerdt, "Epitaxial strontium titanate films grown by atomic layer deposition on $SrTiO_3$-buffered Si(001) substrates," J. Vac. Sci. Tech. A **31**, 01A136-(1-9) (2013). MDM designed and performed experiments. MDM, AP, TQN, AAD, and JGE contributed to the conception and analysis of data. AD and DJS acquired transmission electron microscopy data.

applications.[11-13] Molecular beam epitaxy (MBE) has been the primary means of growing epitaxial oxides on silicon, largely due to its precise control of atomic layer-by-layer deposition. However, alternative growth methods offer both practical and economical benefits for the growth of crystalline oxides on silicon. For example, atomic layer deposition (ALD) provides a chemical route for the growth of epitaxial oxide films at relatively lower temperatures than MBE.

Epitaxial growth of thin films is facilitated by thermodynamic stability between the film and substrate, as well as minimal lattice mismatch. Strontium titanate, $SrTiO_3$ (STO), is one of the few oxides that can be grown epitaxially on Si(001) without interfacial reactions.[14-16] For direct integration of STO with Si(001), there is a relatively small (+1.7%) lattice mismatch with a 45° in-plane rotation, where the STO is compressively strained to Si. In addition, strain relaxation of STO thin films may be provided by annealing in oxygen at elevated temperatures to form amorphous SiO_2 at the interface.[17] Single-crystal STO substrates have been used for the growth of many functional epitaxial oxide films, such as ferroelectric $BaTiO_3$,[18] ferromagnetic $SrRuO_3$,[19] piezoelectric $PbTiO_3$,[20] multiferroic $BiFeO_3$,[21] and superconducting $YBa_2Cu_3O_7$.[22] Therefore, the integration of epitaxial STO on Si(001) allows for large-area STO pseudo-substrates, which have been used as surface templates to integrate multi-functional oxides.[23-33]

Ternary oxides, such as STO, grown by MBE require accurate elemental flux rates for two sources, with precise control of the oxygen environment. Too little oxygen will result in reduced species in the film, such as Ti^{3+} and Ti^{2+} in STO, and excess oxygen during high temperature MBE deposition often results in formation of an amorphous SiO_x layer at the STO-Si interface.[34-37] For many applications, such as high-*k* dielectrics or advanced oxide electronics, the presence of an amorphous SiO_x layer at the STO-Si

interface is undesirable. The ALD method offers controlled, sequential delivery of precursors or reagents that either absorb to saturation or undergo selective ligand reactions, which are self-limiting.[38,39] Under the appropriate operating conditions, this facilitates stoichiometric growth of the desired oxide. Moreover, the relatively low temperature for ALD is likely to inhibit the formation of amorphous SiO_x, silicides, and/or silicates at the STO-Si interface when using a thin STO buffer layer.[40]

ALD of STO thin films has been reported previously.[41-51] The as-deposited films were amorphous to weakly polycrystalline. In most cases, post-deposition annealing at temperatures of 400 °C or higher was used to crystallize the STO films, and provided improvement in the dielectric constant.[43,51] However, epitaxial films are often preferred over polycrystalline films due to their elimination of crystallographic defects, such as high-angle grain boundaries. Several groups have reported on the direct integration of epitaxial STO on Si(001) by MBE,[24-33] but a chemical vapor deposition method is highly desirable due to its potentially easier large-scale production of crystalline oxide films. Recently, formation of the ordered (2×1) strontium silicide template layer by ALD was reported,[52,53] which is known to be an excellent template for the epitaxial growth of STO on Si(001) by MBE. Despite the successful formation of this template, full integration of epitaxial STO films on Si(001) by ALD has not yet been reported.

In this work, an ALD chamber has been integrated with a MBE system, enabling *in vacuo* sample transfer and growth on well-characterized and specially prepared surfaces. The MBE is used to grow the STO surface template used for subsequent ALD growth. We report here the growth and characterization of epitaxial STO films on Si(001) substrates by ALD using an intermediary four-unit-cell STO template grown by MBE.

5.2. EXPERIMENTAL DETAILS

To provide the template surface for ALD growth, the MBE system (DCA 600) was used to grow crystalline STO directly on Si(001) using a variant of the Motorola-developed process.[54] The Si substrates with ~2 nm of native oxide were cut to 20 × 20 mm^2, then ultrasonically cleaned with acetone, isopropyl alcohol, and deionized water for 5 min each, followed by UV/ozone exposure for 15 min to remove residual carbon contamination. The substrates were held in a molybdenum puck (5-cm diameter) that could be used in both the ALD chamber and MBE system, enabling *in vacuo* sample transfer. Upon loading into the MBE chamber, the native oxide was desorbed using a Sr-assisted deoxidation process.[55] After achieving a clean Si(001) surface with 2×1 reconstruction, a half monolayer of Sr metal was deposited on the Si substrate at 550 °C forming the (2×1) strontium silicide template layer. The substrate was cooled to below 200 °C and molecular oxygen was slowly ramped from 5×10^{-8} Torr to 2×10^{-7} Torr over several min to ensure that the underlying Si was not oxidized during the initial STO deposition. Sr and Ti were co-deposited from effusion cells during oxygen ramping at a rate of one monolayer per minute to a thickness of four unit cells of STO. Oxygen was then removed and the films were annealed at 550 °C under vacuum to crystallize the STO layer, as verified by *in situ* reflection high-energy electron diffraction (RHEED). The four-unit-cell STO template grown by this process shows a faint 2× reconstruction along the <210> direction, indicating the film is TiO_2-terminated.[15] The STO-buffered Si(001) pseudo-substrates were then transferred *in vacuo* to the ALD chamber.

The ALD system consists of a custom-built, hot-wall stainless steel rectangular chamber that is approximately 20-cm long, with a reactor volume of 460 cm^3, as described in more detail elsewhere.[56] During ALD growth, the carrier/purge gas (argon) and precursor were introduced through a common manifold at the front of the chamber.

The chamber was continually evacuated during deposition by a dual-stage rotary vane pump with a peak pumping speed of 6 cfm, which maintained the operating pressure near 1 Torr. STO thin films were grown by ALD at 250 °C using strontium bis(triisopropylcyclopentadienyl) [$Sr(^{i}Pr_3Cp)_2$] (HyperSr),[57] titanium tetraisopropoxide [$Ti(O\text{-}^{i}Pr)_4$] (TTIP),[58] and water as co-reactants. HyperSr and TTIP were vaporized at 130 °C and 40 °C, respectively, and water was held at room temperature (26 °C). The water dosing was regulated using an in-line needle valve.

Our previous work showed that TTIP and water saturate the substrate surface within 1 sec of dosing time.[56] Therefore, the TTIP and water dosing times were fixed at 1 sec, while the dosing time for HyperSr was varied to allow for stoichiometric growth of the STO films. Under these conditions, 2 sec dosing time of the Sr precursor provided adequate saturation of the substrate surface. One deposition supercycle of STO consisted of a 2-sec pulse of the Sr precursor, a 10 to 15-sec purge with Ar, a 1-sec pulse of H_2O, and a 10 to 15-sec purge with Ar, for a number of Sr subcycles, followed by a 1-sec pulse of the Ti precursor, a 10 to 15-sec purge with Ar, a 1-sec pulse of H_2O, and a 10 to 15-sec purge with Ar, for b number of Ti subcycles. This is noted as [Sr - 2/10(15)/1/10(15) × a, Ti - 1/10(15)/1/10(15) × b] × N, where a and b represent the number of subcycles for Sr/Ti and N is the number of supercycles. The ratio a:b (Sr:Ti) is used to describe the subcycle ratio per supercycle. Argon was used as the carrier gas, to deliver the Sr and Ti precursors, as well as the purge gas between reactant dosing.

The STO films were characterized using X-ray photoelectron spectroscopy (XPS), X-ray reflectivity (XRR), RHEED, X-ray diffraction (XRD), and cross-sectional transmission electron microscopy (TEM). XPS was performed *in situ* with a monochromatic Al Kα source at 1486.6 eV using a VG Scienta R3000 XPS system to determine the film composition and to verify the absence or presence of SiO_x at the STO-

Si interface. The Sr/(Sr+Ti) composition ratio was calculated using the ratio of the integrated areas of the Sr 3*d* and Ti 2*p* peaks divided by the appropriate atomic sensitivity factor (ASF). For very thin films (< 5 nm), accurate compositional analysis could be obtained using tabulated ASF values of 1.843 and 2.001 for Sr 3*d* and Ti 2*p*, respectively.[59] For thicker films (> 10 nm), it was necessary to account for the sampling depth variation with kinetic energy. This increased the Sr 3*d* ASF value relative to the Ti 2*p* ASF value. For comparison to a standard reference, a 5 × 5 mm^2 single-crystal STO(001) substrate (CrysTec) was analyzed, where the Sr/(Sr+Ti) ratio was assumed to be 0.5. For this case, the effective ASF values were determined to be 2.190 and 2.001 for Sr 3*d* and Ti 2*p*. Additionally, differences in the relative intensities of Sr and Ti peaks between amorphous and crystalline STO films can occur due to photoelectron diffraction effects. To check for these effects, a thin amorphous STO film was grown on clean Si(001) and analyzed using XPS. The same sample was then annealed to form crystalline STO and analyzed using the identical XPS settings. In this case, enhancement was observed for both the Sr and Ti peaks. However, the difference in the relative sensitivities was quite small, yielding only a small error (2.5%) in the Sr/(Sr+Ti) composition ratio. We therefore did not compensate for this error between amorphous and crystalline STO films.

All X-ray photoelectron (XP) spectra were analyzed using a uniform shift based on the Si $2p_{3/2}$ elemental peak to 99.3 eV. To allow for *in situ* XPS analysis of the STO-Si interface, STO films grown by ALD had to be sufficiently thin so that the Si 2*p* peaks could still be resolved. Thus, 15 ALD supercycles with a 1:1 (Sr:Ti) cycle ratio were used for the *in situ* XPS studies to give approximately 5 nm total thickness of the STO film. Additionally, some samples were annealed *in vacuo* to examine the effect of annealing on the STO-Si interface.

To determine the growth rate of the ALD-grown STO, film thicknesses were measured using XRR. For this analysis, the four-unit cell STO template grown by MBE was assumed to be 1.5-nm thick. Therefore, the ALD-grown film was equal to the total STO thickness minus the MBE template. Both RHEED and XRD were used to evaluate the orientation and crystallinity of the STO films. XRD and XRR were conducted with a Bruker-AXS D8 Advance Powder Diffractometer using a sealed tube Cu Kα radiation. For TEM analysis, the sample was prepared using standard mechanical polishing followed by argon-ion-milling to perforation. Observations were made with a 400-keV high-resolution electron microscope (JEM-4000EX) equipped with a double-tilt specimen holder.

5.3. Results and Discussion

5.3.1. Stoichiometry and growth rate of crystalline STO films

Complexity in the ALD growth of ternary oxides versus binary oxides comes from several sources, which include the control of stoichiometry, precursor interactions, and growth on mixed-termination surfaces. To determine the stoichiometry of the as-deposited films, *in situ* XPS was used to analyze the Sr 3*d*, Ti 2*p*, and O 1*s* peaks. Representative Sr 3*d* and Ti 2*p* curves are given in Figures 5.1(a) and 5.1(b), respectively, which were taken after deposition of a 24-nm thick STO film (22.5 nm from ALD plus 1.5 nm from MBE). The ALD cycle conditions were {Sr - 2/15/1/15 × *1*, Ti - 1/15/1/15 × *1*} × *100* supercycles, where film growth occurred through one-hundred alternating exposures of the Sr and Ti precursor on the MBE template. When stoichiometric conditions were met, *i.e.*, Sr/(Sr+Ti) ≈ 0.50, the STO film was crystalline as-deposited. Both Sr and Ti were consistent with fully oxidized species, *i.e.*, Sr^{2+} and

Ti^{4+}, as expected with $SrTiO_3$. For the STO film represented in Figure 5.1, the ratio of Sr/(Sr+Ti) at the center of the sample was found experimentally to be 0.53, indicating that the film was nearly stoichiometric.

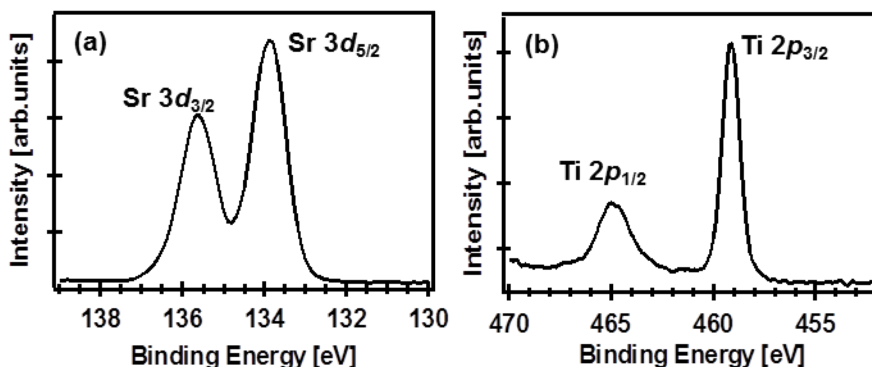

Figure 5.1. X-ray photoelectron spectra of the (a) Sr 3*d* and (b) Ti 2*p* after deposition of a 24-nm thick STO film (22.5 nm ALD plus 1.5 nm MBE) at 250 °C.

To examine the growth rate of ALD-grown STO on the STO/Si(001) template, films were grown under identical dosing conditions for a varying number of supercycles with a 1:1 (Sr:Ti) cycle ratio. The thickness of the ALD-grown film was directly proportional to the number of supercycles (Figure 5.2). However, the composition of the films in the center of the sample varied with a Sr/(Sr+Ti) ratio between 0.48 to 0.56. Further studies (described below) suggest that variance in the degree of crystallinity and stoichiometry of the as-deposited films is a result of thermal decomposition of the Sr precursor, leading to spatial variation of the cation ratio.

As shown in Figure 5.2, crystalline STO films grew at a higher rate than amorphous STO films under the same deposition conditions. For films that were crystalline as-deposited, the average growth rate was found to be 0.11 nm/unit-cycle (0.22 nm/supercycle) using a 1:1 (Sr:Ti) cycle ratio. For comparison, STO films were

grown on SiO_2/Si(001) native oxide substrates with a 1:1 (Sr:Ti) cycle ratio. The films were amorphous as-deposited and nearly stoichiometric, Sr/(Sr+Ti) = 0.52. The average growth rate of the amorphous STO films was 0.076 nm/unit-cycle (0.15 nm/supercycle); therefore, under the same deposition conditions, stoichiometric, crystalline STO grows approximately 1.5 times faster than amorphous STO.

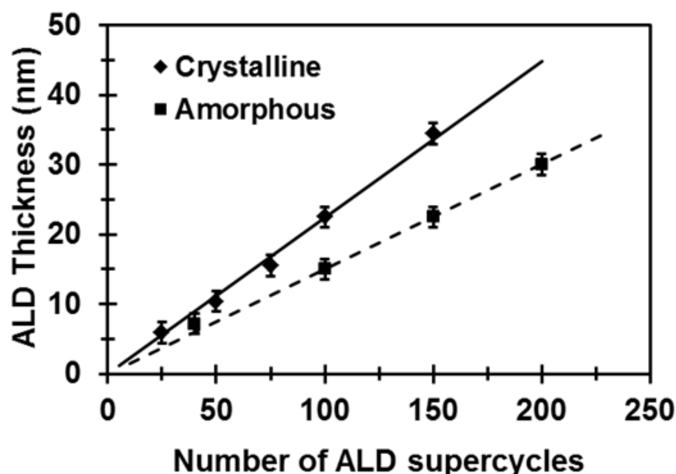

Figure 5.2. Linear growth behavior of $SrTiO_3$ films grown by ALD using HyperSr, TTIP, and H_2O precursors at 250 °C. Higher growth rates were observed for crystalline STO (solid line) as compared with amorphous STO (dashed line) under the same deposition conditions at 250 °C.

The observed crystalline growth rate (0.11 nm/unit-cycle) is higher than previous reports of ALD-grown STO films at 250 °C.[42-45,49-51] However, a highly enhanced growth rate of STO (0.107 nm/unit-cycle) was recently reported at a deposition temperature of 370 °C using Ti(O-^{i}Pr)$_2$-(tmhd)$_2$ and HyperSr as the precursors.[60] Under our experimental conditions, the relatively high growth rate observed at 250 °C is likely due to the crystalline nature of the as-grown films. This phenomenon has already been examined for TiO_2 films, where under the same deposition conditions polycrystalline anatase grows faster than amorphous TiO_2.[56,61] A recent study, using *in situ*

spectroscopic ellipsometry, has revealed that there may be more than one operation regime for the ALD process of HyperSr and water due to the large change in saturated growth rate (0.05 up to 0.33 nm/cycle) between substrate temperatures of 150 to 350 °C.[62] Similar to the effects of deposition temperature, the crystalline surface may promote the partial decomposition of the Sr and/or Ti precursors, leading to an enhanced rate of film growth.

5.3.2. Composition variation and effects on crystallinity

Compositional variation was monitored for several samples across the 20×20 mm^2 Si wafer after STO deposition. The cation ratio is particularly important when crystalline films are desired. Variance in the cation ratio can cause amorphous regions in the as-deposited films. Based on qualitative analysis using RHEED, Sr-rich films with Sr/(Sr+Ti) ≈ 0.60 remain crystalline as-deposited, while Ti-rich films with Sr/(Sr+Ti) ≈ 0.40 are amorphous. Therefore, stoichiometric to slightly Sr-rich films are preferred to ensure crystalline film growth.

The cation ratio, Sr/(Sr+Ti), was measured over a roughly 15×15 mm^2 area at nine different points roughly 5 mm apart, which are labeled in Figure 5.3 along with the gas flow direction. The XPS analyzer has an incident spot size of 1×3 mm^2 on the sample surface, with the long dimension parallel to the gas flow (see Fig. 5.3). Using this data collection method, several parameters in the deposition process were varied to minimize the compositional variation across the wafer. Deposition temperature, cycle ratio (Sr:Ti), and purge time were among the ALD parameters varied. In addition, slight modifications to the sample holder were also evaluated to determine its impact. As described in detail below, appropriate deposition conditions can minimize the

compositional variation across the wafer, allowing for the growth of crystalline STO films by ALD.

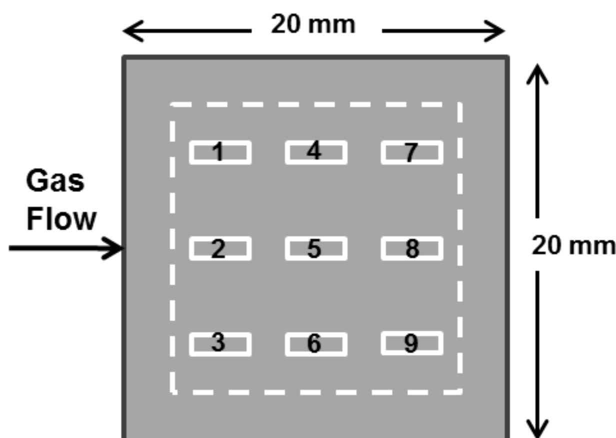

Figure 5.3. Schematic of a typical 20×20 mm^2 sample, indicating direction of gas flow with relation to the designated points for compositional analysis by XPS.

In all cases, the hot wall, crossflow-type ALD reactor yielded an increase in Sr deposition at the leading edge of the wafer. In other words, the Sr/(Sr+Ti) ratio decreased from the leading edge (Position 1-3) to the back of the wafer (Position 7-9). Compositional variation in the direction perpendicular to the flow was significantly less than it was parallel to the flow, often yielding no measurable variation (within experimental error). Small variations in temperature across the wafer are suspected of being a contributor to the observed compositional variation by XPS. Our reactor design may be especially susceptible to temperature variation in the flow direction due to the inability to heat the gate valve connecting the ALD reactor and main transfer line to the same temperature as the side walls. Ideal ALD conditions are insensitive to thermal variations, indicating that the Sr precursor, HyperSr, has chemical vapor deposition (CVD)-like properties. Thermal decomposition of this Sr precursor has been noted as a 'major concern' for spatial variation in previous work.[42]

A summary of the composition variation under varying deposition conditions is given in Table I. For the five samples presented, STO deposition occurred through 200 unit-cycles, corresponding to film thicknesses of approximately 22-25 nm. In our system, the two primary causes of compositional variation were determined to be insufficient purging times and temperature variation. One approach to minimize temperature variation was to reduce the overall deposition temperature to 200°C. However, as shown in Table I, reducing the deposition temperature and using the same Sr:Ti cycle ratio caused a significant decrease in overall Sr content. The STO film (noted as Sample 2) was mostly amorphous, with only the leading edge crystallized, as observed by RHEED. To accommodate for the decrease in Sr content at the lower deposition temperature, a cycle ratio (Sr:Ti) of 3:2 was used. This sample (Sample 3) appeared fully crystalline by RHEED, even at the reduced substrate temperature (200 °C).

Table 5.1. Observed Sr/(Sr+Ti) ratio for ALD-grown STO films.

Sample	**Deposition temp. (°C)**	**Sr:Ti cycle ratio**	**Ar purge (sec)**	**RHEED image**	**Sr/(Sr+Ti) Average (± 0.01)**	**Sr/(Sr+Ti) Range (± 0.01)**
1	**250**	**1:1**	**10**	**Partly Crystalline**	**0.48**	**0.40 – 0.54**
2	**200**	**1:1**	**10**	**Mostly Amorphous**	**0.37**	**0.33 – 0.43**
3	**200**	**3:2**	**10**	**Crystalline**	**0.55**	**0.51 – 0.57**
4	**250**	**1:1**	**15**	**Crystalline**	**0.55**	**0.53 – 0.56**
5	**250**	**4:3**	**15**	**Crystalline**	**0.57**	**0.55 – 0.59**

For our reactor design, thermal variation in the flow direction could also be minimized by providing a thermal 'break' between the sample and the molybdenum sample holder. This was accomplished by cutting the wafer to approximately 16×20 mm^2, where the shorter dimension was placed in the direction of the flow. Therefore, the edges of the wafer were not in direct contact with the sample puck at the leading edge and back of the wafer. This was found to be an effective method to minimize edge variation with our crossflow-type reactor, particularly with thicker films. For example, without using a thermal break between the sample and the puck, the Sr/(Sr+Ti) ratio of a 46-nm thick STO film varied from 0.53 to 0.43, with the leading edge being Sr-rich. However, under the same deposition conditions and using a thermal break, a similar 46-nm thick STO film showed small variance in the Sr/(Sr+Ti) ratio across the wafer (0.53 to 0.51), which is less than 5 percent.

Purging times less than 15 sec yielded increased variation in the Sr/(Sr+Ti) ratio. At 10 sec purging and no thermal break, one sample was observed to be crystalline (at the leading edge) to amorphous (at the back of the wafer), where the Sr/(Sr+Ti) ratio varied from 0.54 to 0.40, respectively. This indicates that shorter purge times cause chemical vapor deposition (CVD)-like deposition rather than true ALD. Interestingly, our earlier studies of the binary oxides TiO_2[56] and SrO (not presented), showed controlled ALD-like growth with only 10 sec purging. Therefore, the growth of the ternary oxide, STO, appears to require longer purging times than expected.

In summary, compositional variation was minimized by lowering the deposition temperature (Sample 3) or increasing the Ar purging time (Sample 4/5). The reduced deposition temperature may reduce crystallinity of the as-deposited film, and appears to be outside the optimal ALD temperature window for both the Sr and Ti precursors.[42] Therefore, deposition at a substrate temperature of 250 °C with increased purging times

is preferred for growing crystalline STO films by ALD. Under these conditions, using a Sr:Ti cycle ratio of 1:1 up to 4:3 appear to provide similar cation compositions. In addition to the increased purging time, a method to minimize thermal variation in the ALD reactor must be considered to compensate for the CVD-like behavior of the Sr precursor, HyperSr.

5.3.3. Film impurities and effect of post-deposition annealing

Small carbon impurities in SrO and STO films have been previously reported when using HyperSr and water reagents.[42,47] This is often observed due to the formation of $SrCO_3$, either during film growth or upon exposure to ambient. Using *in situ* XPS analysis after ALD growth, carbon impurities were observed sporadically after film growth. To examine this in more detail, a standard four-unit cell STO template was grown by MBE and transferred to the ALD chamber for deposition of 15 STO supercycles using a 1:1 (Sr:Ti) cycle ratio. The resulting STO film was approximately 5 nm thick (ALD plus MBE). After ALD deposition, the sample was transferred *in vacuo* for collection of XP spectra. The C 1*s*, O 1*s*, Si 2*p*, and Ti 2*p* spectra are shown in Figures 5.4(a)-(d), respectively. For this sample, two different carbon species appear in the C 1*s* XP spectra, as shown in Figure 5.4(a). The binding energy (BE) peak positions are consistent with carbonate (BE ≈ 290 eV) and single C-O bonding (BE ≈ 286 eV) species.[59] In addition, a secondary shoulder peak (BE ≈ 532.5 eV) is observed in the O 1*s* XP spectra (Fig. 5.4(b)). The shoulder peak is also consistent with the presence of C-O bonding.[59]

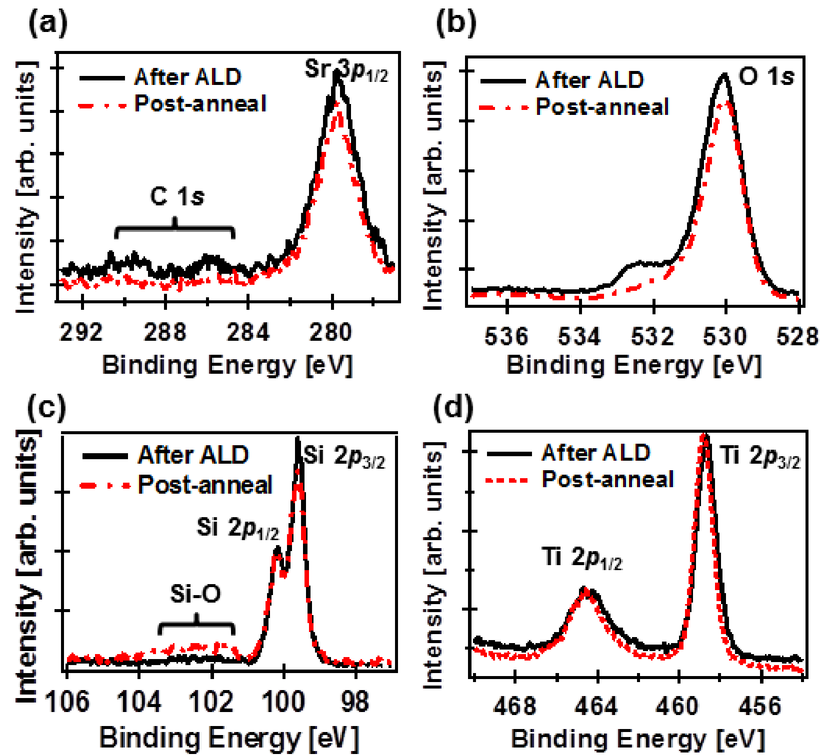

Figure 5.4. X-ray photoelectron spectra of (a) C 1*s* and Sr $3p_{1/2}$, (b) O 1*s*, (c) Si 2*p*, and (d) Ti 2*p* after 15 ALD supercycles (solid black line) with subsequent post-deposition annealing at 350 °C for 15 min (dashed red line).

Some samples appeared to be free of carbon contamination under identical deposition conditions. Therefore, some steps in our post-deposition processing may have impact on the carbon impurities present. Post-deposition vacuum annealing (10^{-9} torr) of the STO film at 350 °C for 15 min eliminated nearly all carbon species and reduced the O 1*s* shoulder peak observed in Figure 5.4(b). However, examination of the Si 2*p* XP spectra showed a slight increase in Si-O bonding due to the post-deposition annealing. Interestingly, no reduced Ti species (Ti^{3+}) was observed (Fig. 5.4(d)), contrary to the post-deposition annealing of TiO_2 films in the same system.[40]

To minimize the formation of Si-O bonding, a light post-deposition annealing (250 °C for 30 min) was used directly after ALD. Once again, a standard four-unit cell

STO/Si(001) template was grown by MBE and XP spectra were collected. The sample was then moved to the ALD chamber and exposed to 15 STO supercycles using a 1:1 (Sr:Ti) cycle ratio. The sample was then post-deposition annealed in the ALD chamber at low pressure (10^{-6} torr), and finally transferred *in vacuo* for collection of XP spectra. Figures 5.5(a)-(c) show the XP spectra for C 1*s*, O 1*s*, and Si 2*p*, respectively. As can be seen in Figure 5.5(a), negligible carbon impurities (below XPS detection limit) are present after MBE growth, before ALD, and after the ALD and light annealing process. The sharpness of the O 1*s* spectra (Fig. 5.5(b)) also indicates that there is negligible presence of carbonate species in the STO film.

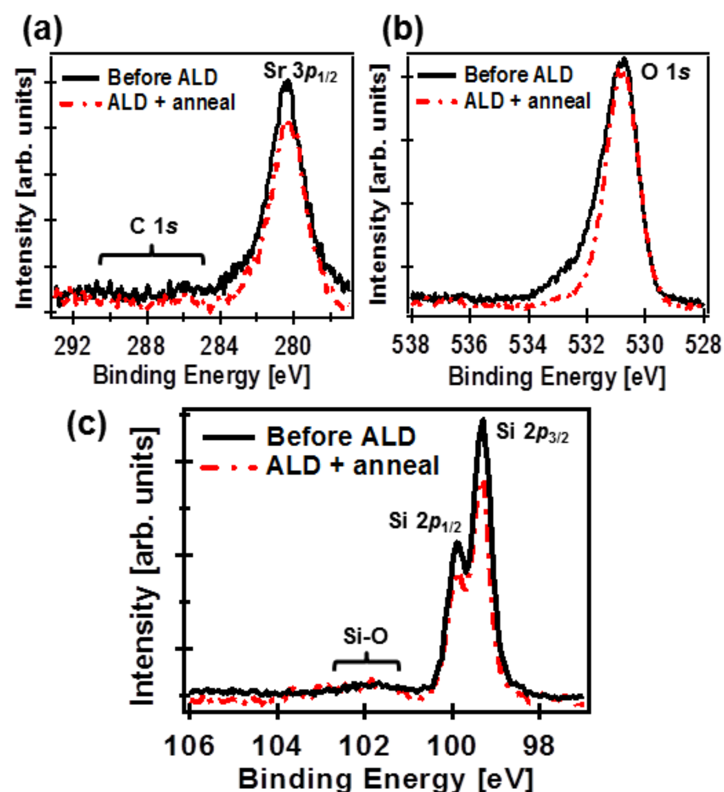

Figure 5.5. X-ray photoelectron spectra of (a) C 1*s* and Sr $3p_{1/2}$, (b) O 1*s*, and (c) Si 2*p* before ALD (solid black line) and after ALD with post-deposition annealing at 250 °C for 30 min (dashed red line).

When annealed under these conditions, there was not a noticeable enhancement of the crystallinity (based on RHEED and XRD) compared with the as-deposited film. The primary change appeared to be in the carbon and oxygen XP spectra. In addition, minimal increase in Si-O bonding is observed after the ALD growth and light annealing conditions (Fig. 5.5(c)). Thus, the relatively low ALD and annealing temperature (250 °C) minimized the oxidation of Si at the STO-Si(001) interface. Integration of epitaxial oxides on silicon using ALD may therefore be advantageous by eliminating concern for formation of a substantial interfacial amorphous layer during film growth. Currently, up to 50-nm thick crystalline STO films have been grown by ALD on Si(001) using the STO buffer layer grown by MBE, with minimal carbon impurities (< 1%).

5.3.4. Crystalline quality of ALD-grown STO films

High-quality epitaxial STO films have been grown directly on Si(001) by MBE with no interfacial amorphous layer.[14-16] However, thicker crystalline films (> 10 nm) can be difficult to grow by MBE. Lower temperature co-deposition of Sr and Ti is often used to avoid SiO_x formation at the interface, and the MBE-grown STO films are subsequently crystallized at higher temperatures (> 400 °C). Alternatively, layer-by-layer growth by MBE is possible, but small deviations in the flux rate can amount to large variations in composition for thicker films. Despite the thermal decomposition observed with the HyperSr precursor, the ALD method is able to provide controlled pulsed delivery and the growth rate is independent of the film thickness. This may provide an advantage to ALD growth when thicker epitaxial STO films are desired.

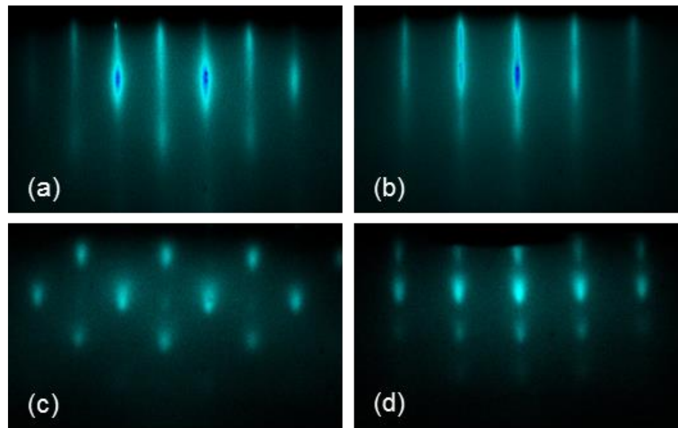

Figure 5.6. RHEED images obtained before [(a), (b)] and after [(c), (d)] ALD growth of a 24-nm thick STO film on four-unit cell STO-buffered Si(001) at 250 °C. The beam is aligned along the [100] for (a) and (c), and [110] azimuth for (b) and (d).

The layer-by-layer growth of ALD at relatively lower temperature has been shown to allow for direct crystallization of TiO_2 on STO-buffered Si(001) without forming an interfacial amorphous layer.[40] Therefore, direct crystallization of STO grown by ALD on the STO/Si(001) template is expected. Figures 5.6(a) and 5.6(b) show the RHEED patterns of a typical STO/Si(001) template, where four unit cells of STO is grown directly on Si(001); as taken along the [100] and [110] directions, respectively. The streaks appear sharp and elongated, indicative of a highly crystalline and atomically smooth STO film. The STO/Si(001) template is then transferred *in situ* to the ALD chamber to continue STO growth. Figures 5.6(c) and 5.6(d) show RHEED patterns of a typical STO film after ALD, taken along the [100] and [110] directions, respectively. The increase in intensity modulation along the streak direction indicates an increase in surface roughness due to the ALD growth compared with the MBE-grown STO/Si(001) template. AFM measurements indicate that this difference in roughness has approximately doubled after ALD growth, as shown in Figures 5.7(a) and 5.7(b). The

root-mean-square (RMS) roughness was found to be 0.21 ± 0.06 nm for the STO/Si(001) template and 0.38 ± 0.14 nm after ALD growth. In addition, there was no significant increase in RMS roughness for STO film thicknesses between 5 and 50 nm. For example, a 46-nm thick STO film yielded a RMS roughness ranging from 0.34 to 0.43 nm (less than 1% of the total film thickness) over a 20×20 μm^2 area.

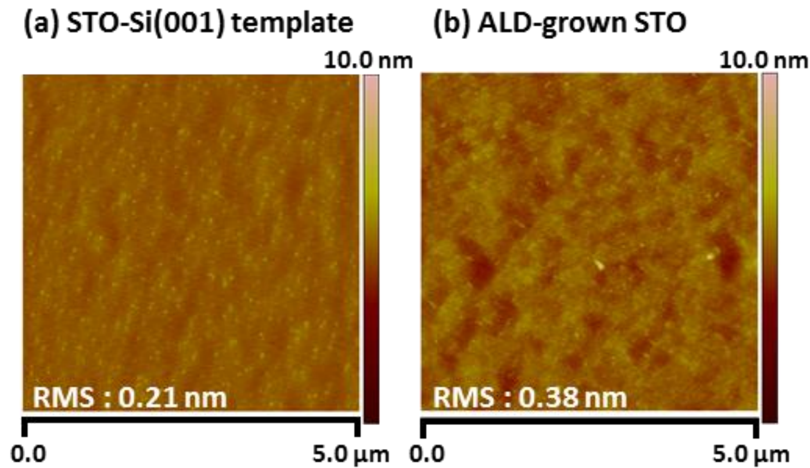

Figure 5.7. AFM images before (a) and after (b) ALD growth of an 8-nm thick STO film grown on the STO-Si(001) template. The substrate temperature was 250 °C.

XRD of the as-deposited STO films is consistent with the perovskite structure (Fig. 5.8). The sole presence of the {001} reflections indicate the preferred orientation of the ALD-grown films. For thin STO films (< 5 nm), the STO(002) reflection is shifted from the nominal powder value ($2\theta \approx 46.4°$) to a slightly lower value ($2\theta \approx 45.9°$), indicating that the *c* lattice constant is 3.95 Å. An increased *c* lattice constant is consistent with reduced *a*-*b* lattice constants relative to that of bulk STO. This reduces the in-plane lattice mismatch of STO to Si(001), where the STO is compressively strained to Si. Theoretical prediction of the STO(002) reflection for thin films can be made assuming that the film is perfectly strained to Si (a = 3.84 Å), with a Poisson ratio equal

to 0.232.[63] Under these assumptions the STO(002) reflection should be shifted to a value of 2θ = 46.0°, which is consistent with our experimental data. However, thicker films of STO showed higher 2θ-values for the STO(002) reflection (up to 2θ = 46.6° for a 36-nm thick film). Figure 5.9 gives a graphical representation of the relative positioning of the STO(002) peak for varying film thickness. This suggests that STO films grown by ALD on the STO/Si(001) template are initially strained to Si, relax with increasing thickness, and appear fully relaxed at thicknesses greater than 15-nm.

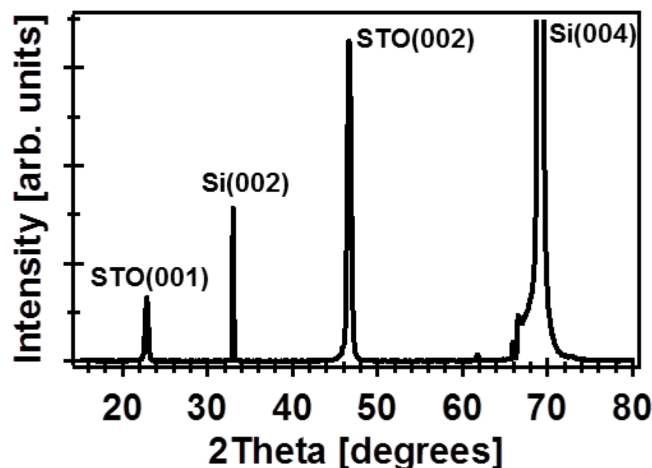

Figure 5.8. X-ray diffraction pattern of a 24-nm thick STO film grown by ALD on four-unit cell STO-buffered Si(001) at 250 °C.

To determine the degree of out-of-plane orientation, a rocking curve analysis was performed around the STO(002) reflection, giving a full-width half maximum (FWHM) of 0.34° for a 24-nm thick film (Fig. 5.10). The epitaxial relationships between the STO film and the Si(001) substrate were determined by a φ-scan around the {105} reflections of STO and the {115} reflections of silicon. The STO film was aligned such that $(001)_{STO} \| (001)_{Si}$ and $(100)_{STO} \| (110)_{Si}$, confirming the 45° in-plane rotation that is expected for lattice matching between the STO and Si(001) substrate.

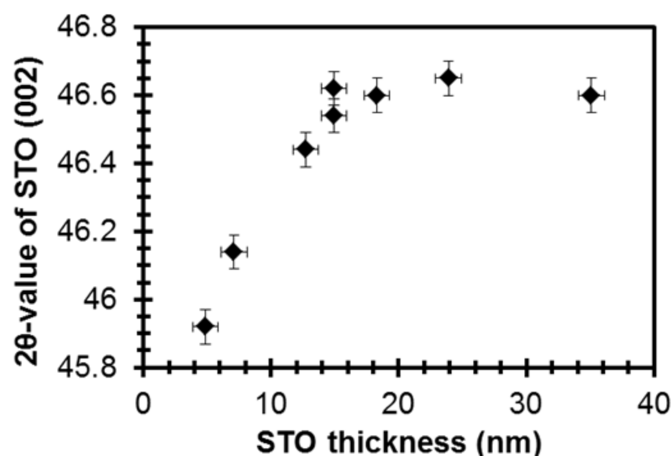

Figure 5.9. Plot of 2θ-value for the STO(002) reflection versus thickness of the STO film. Samples were grown using ALD with a 1:1 (Sr:Ti) cycle ratio at 250 °C on the STO-Si(001) template.

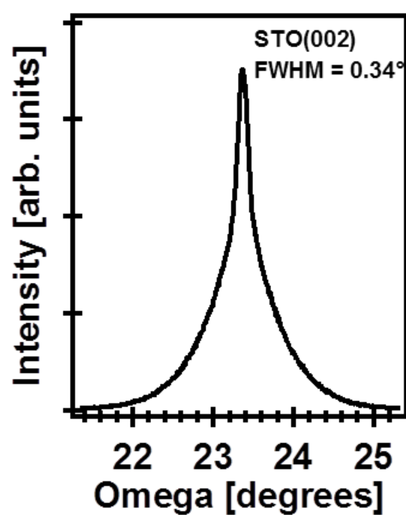

Figure 5.10. Rocking curve of the STO(002) reflection at a fixed 2θ = 46.6° for a 24-nm thick STO film grown by ALD on four-unit cell STO-buffered Si(001) at 250 °C.

In addition, the epitaxial relation and crystallinity of the STO films on Si(001) substrates were observed by cross-sectional TEM. Figure 5.11 shows a transmission electron micrograph of a 24-nm thick STO film (22.5-nm from ALD plus 1.5-nm from

MBE). The ALD film as-deposited at 250 °C appears fully crystalline. No clear interface is visible between the ALD-grown STO film and the four-unit-cell STO template grown by MBE, although well-separated grain boundaries are observed. In addition, a partially amorphized layer (≈ 0.5-nm thick) is sometimes observed at the STO-Si(001) interface (see top left inset of Fig. 5.11). This is believed to occur during TEM sample preparation, since the region at the Si-STO interface has the weakest bonds and tends to amorphize during ion-milling to final transparency. Nevertheless, the TEM results confirm that the four-unit-cell STO buffer layer on Si(001) provides an adequate template for growth of crystalline STO by ALD.

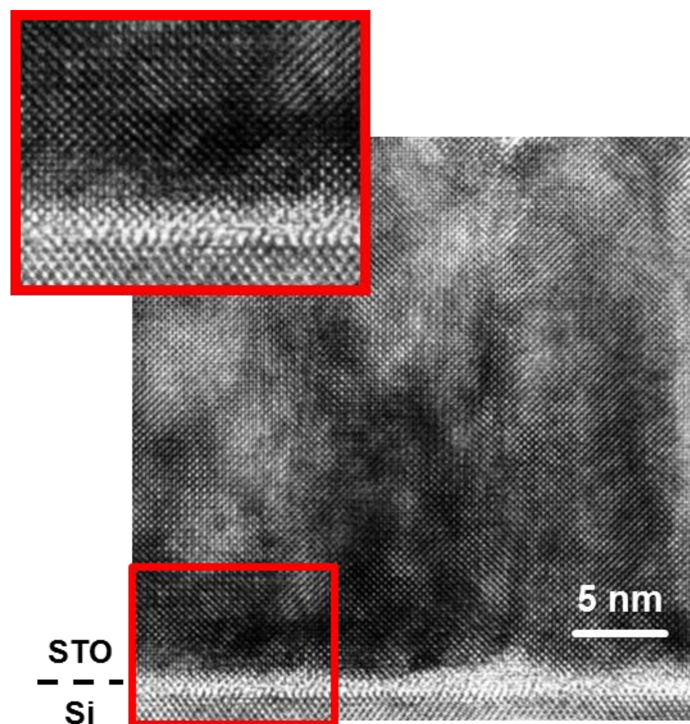

Figure 5.11. High-resolution transmission electron micrograph showing cross section of 24-nm thick STO film (22.5 nm from ALD plus 1.5 nm from MBE) on Si(001) substrate. (top left inset) Magnification of the highlighted region showing the STO-Si(001) interface, as well as the ALD-MBE interface.

5.4. Application of Strontium Titanate Thin Films on Si (001) for Photoelectrochemical Water Splitting

5.4.1. Silicon-based photocathode for water reduction with an epitaxial $SrTiO_3$ protection layer and a nanostructured catalyst

Details of this section are published in Nature Nanotech. ***10****, 84-90 (2015) in collaboration with Li Ji from Prof. Edward Yu's group at the University of Texas at Austin.*

The fast growing global energy demand and environmental impact of fossil fuels have spurred the search for alternative clean energy. Converting solar energy into hydrogen fuel is a promising way. Here, efficient and stable hydrogen production from water is demonstrated using a Si-based photocathode with an epitaxial oxide capping layer. A thin epitaxial strontium titanate, $SrTiO_3$, protection layer is grown directly on Si (001) by molecular beam epitaxy. By taking advantage of the conduction band alignment and lattice match between single crystalline $SrTiO_3$ and Si, the photogenerated electrons easily transport through the $SrTiO_3$ layer with minimized interface trap states and reduced recombination rate. Metal-insulator-semiconductor (MIS) photocathodes under broad-spectrum illumination at 100 mW/cm^2 exhibited a photocurrent density and photovoltage of 35 mA/cm^2 and 450 mV, respectively. There was no observable decrease in performance after 10 hr operation in 0.5M H_2SO_4. The efficiency and performance were highly dependent on the size and spacing of the structured metal catalyst. Using a nanosphere lithography lift-off process, 50 nm mesh-like Ti/Pt structures were created for the MIS photocathode and achieved an applied-bias-photon-to-current efficiency of 4.9%.

Key Results of $SrTiO_3$-protected Si (001) for water reduction

Single-crystal $SrTiO_3$ (STO) is grown on Si (001) by molecular beam epitaxy. The crystalline structure of the STO protective layer grown on Si (001) was confirmed by reflection high-energy electron diffraction (RHEED). RHEED images for a 4-unit-cell (~1.6 nm) thick STO film grown by MBE are shown in Fig. 5.12(a) and 5.12(b). The RHEED images are taken along the [110] and [210] azimuth of the cubic perovskite. The elongated streak patterns indicate a well-crystallized and atomically smooth film. Rotation of the sample under electron illumination confirmed the four-fold symmetry and registry with the underlying Si substrate.

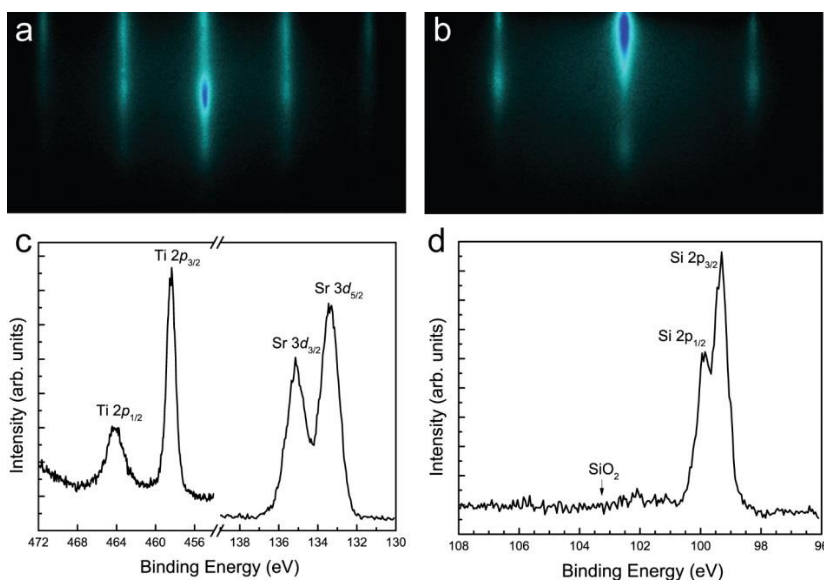

Figure 5.12. RHEED images of a 4-unit-cell (1.6 nm) STO film grown by MBE on p- Si (001). The beam is aligned along the [110] and [210] azimuth for (a) and (b), respectively. High-resolution X-ray photoelectron spectra of an 8-unit-cell (3.1 nm) thick STO film showing (c) the Sr 3*d* and Ti 2*p* core levels, and (d) the Si 2*p* core level confirming that negligible SiO_2 present.

Film composition and quality of the STO-Si interface were analyzed using *in situ* XPS. The STO film composition was shown to be stoichiometric (50%) to slightly Sr-

rich (52%) for thicknesses between 4-10 unit cells (1.6-4 nm). Figure 5.12(c) shows high resolution XPS spectra of the Sr 3*d* and Ti 2*p* core levels. The binding energy peak positions of the Sr $3d_{5/2}$ (133.5 eV) and Ti $2p_{3/2}$ (458.4 eV) are consistent with fully oxidized species (Sr^{2+} and Ti^{4+}) as found in bulk, single crystal STO. Figure 5.12(d) shows the Si 2*p* core level after deposition of an 8-unit-cell thick (3.1 nm) STO film. The absence of a peak at ~103.3 eV suggests that the interface is nearly free of amorphous SiO_2; however, a small presence of suboxide (SiO_x) or silicate is observed at a slightly lower binding energy (~102 eV). Nevertheless, the STO film is of high crystalline quality with a reasonably abrupt STO-Si interface. This provides an ideal material system for electron transport from the Si substrate to the STO surface.

Figure 5.13(a) shows a schematic diagram of the STO/p-Si photocathode. Incident light will travel through the ultra-thin STO layer and be absorbed predominantly by the silicon substrate. Photogenerated electrons will then travel across the STO layer to the Ti/Pt metallic catalyst, where hydrogen is produced. As indicated in Fig. 5.13(b), electron transport across the STO is facilitated by the small conduction band offset. Prior studies have shown that work function engineering using a Ti/Pt bilayer could further improve catalyst performance. The Ti/Pt bilayer structure was used for the following two reasons. First, the adhesion of Pt directly to the STO surface was weak. After several minutes of PEC operation, Pt came off the STO surface and the performance degraded significantly. Inserting a Ti layer improves the adhesion and solves this problem. Second, in metal-insulator-semiconductor (MIS) PEC cells, the metal is serving as the catalyst while simultaneously forming a Schottky junction. The open circuit voltage (V_{oc}) obtained in MIS junctions depends on the work function difference between the metal and semiconductor. Though Pt is a good catalyst, its work function is large and comparable to p-Si, resulting in small V_{oc}. By inserting a Ti layer underneath Pt, the roles of the metal in

determining V_{oc} and as a catalyst are decoupled, with Pt serving as the catalyst and Ti forming the MIS junction.

To confirm the design principle that the solid-state properties of the oxide and its interface affect the PEC performance, linear sweep voltammetry (LSV) measurements were conducted in 0.5 M H_2SO_4 deaerated by Ar gas without any sacrificial reagent. A xenon arc lamp was used as the light source and the light intensity was calibrated to 100 mW/cm^2 by a silicon photodiode. Pt wire and Ag/AgCl were used as the counter electrode and reference electrode, respectively. Before testing MIS photocathodes, a Pt wire was used as the working electrode and LSV was performed to calibrate the normal hydrogen electrode (NHE), illustrated as the grey line in Fig. 5.13(c). LSV provides information on both the metal-electrolyte interface and MIS junction. For the metal-electrolyte interface, fast charge transfer is required.

For a MIS junction, the quality of the oxide layer impacts the photocurrent density, onset potential, and transient behavior. Tunneling is the most common conduction mechanism through insulators under high fields. For tunneling transport, the current density is given by:

$$J \propto \left(\frac{V}{d}\right)^2 \exp\left[-\frac{4\sqrt{2m^*}(q\phi_B)^{\frac{3}{2}}}{3q\hbar\left(\frac{V}{d}\right)}\right] \quad (1)$$

where J = tunneling current density, V = applied bias, d = oxide thickness, m^* = effective mass, q = electron charge, ϕ_B = barrier height and $\hbar$ = reduced Planck's constant. From Equation (1), we know that the tunneling current density will decrease exponentially with increasing oxide thickness and barrier height. According to Eq. (1), the tunneling current should show an approximately inverse square relationship with thickness as $\phi_B \rightarrow 0$, since the exponential factor approaches unity. In addition, the overall current density will be dramatically higher than for a structure with a more typical oxide barrier height. Thus, a

key advantage of utilizing STO as the protection layer is the minimal conduction band offset with silicon, as shown in Fig. 5.13(b). This can be demonstrated by comparing the limiting photocurrent density for samples with different STO thickness with thin film metal coating.

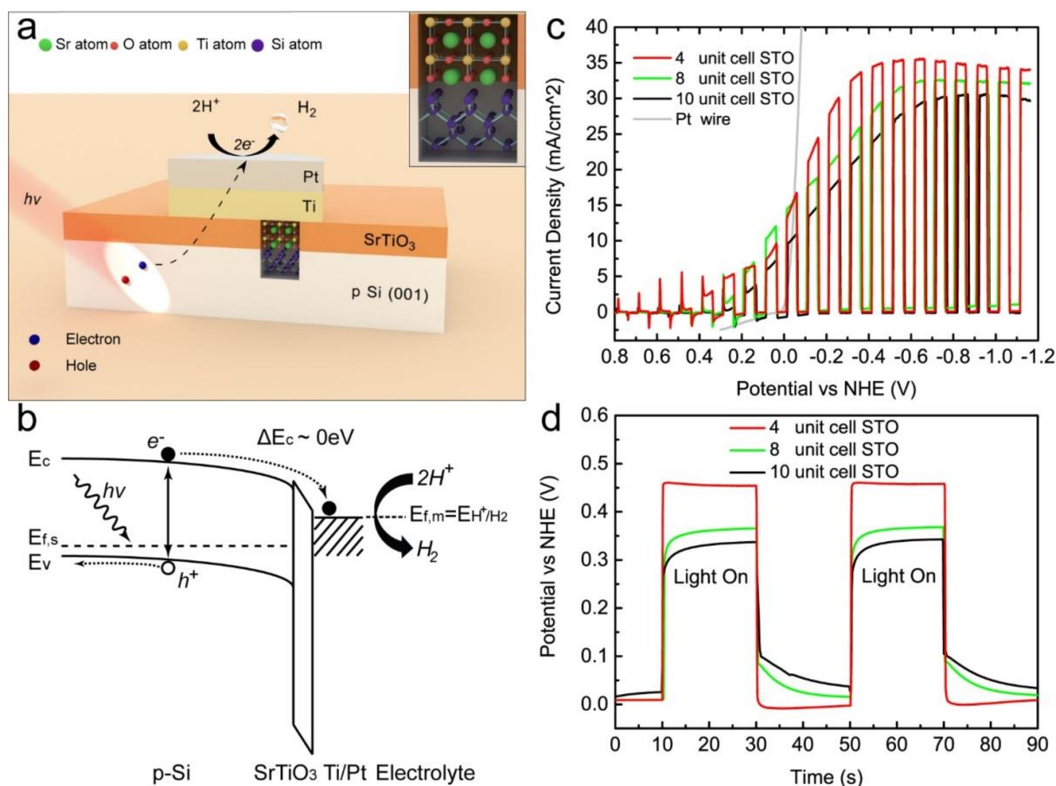

Figure 5.13. (a) Schematic of the STO-protected Si photocathode shows light is absorbed by the p-Si substrate and the photogenerated electrons will tunnel to the surface metallic dots, where hydrogen is produced. Inset plot represents the interface between STO and Si (001), with good lattice match. (b) Energy band diagram shows carrier generation and transport, with negligible conduction band offset between STO and Si, facilitating electron transport. (c) Linear sweep voltammetry (LSV) and (d) open-circuit potential measurements with illumination chopped for 20 nm Pt/30 nm Ti/STO/p-Si (001) for various STO thicknesses from 4 to 10 unit cells. The sweep rate for LSV was 50 mV/sec. The catalyst structures consisted of Pt/Ti dots that are 60 μm in diameter and in a square array with 75 μm period. The light source was chopped during the PEC measurements.

Figure 5.13(c) shows the LSV results of 4, 8 and 10 unit-cell STO/p-Si samples with 60 µm diameter metal catalysts. The limiting photocurrent density for these samples only decreases slightly with increasing STO thickness, consistent with the negligible conduction band offset. The photocurrent density of the 4-unit-cell STO sample reaches as high as 35 mA/cm^2, which is the highest limiting photocurrent reported for single-junction Si-based photoelectrodes. This is attributed to the small ΔE_c and single crystalline nature and epitaxial interface of MBE-grown STO on Si which reduces recombination at the Si/STO interface. Recombination peaks are often observed during transient state when switching the light on/off. However, as illustrated in Fig. 5.13(c), all the single crystalline STO samples exhibit no recombination peaks, indicating excellent metal-oxide interface quality and low concentration of interface traps and defects which can serve as recombination centers for photogenerated electron-hole pairs.

The onset potential shift for the 4 unit-cell STO sample obtained from the LSV results in Fig. 5.13(c) is 460 mV. To confirm this, the open-circuit-potential versus time was measured. The onset potential shifts for 4, 8 and 10 unit-cell samples are 450 mV, 350 mV and 300 mV, respectively, as shown in Fig. 5.13(d). The decreasing onset potential shift with increasing STO thickness can be explained by the voltage drop across the oxide layer increasing due to the high dielectric constant of STO (*k*~300 for bulk).

Devices with 4 unit-cells of STO on p-Si and 1 µm diameter Ti/Pt metal catalyst were utilized to examine the PEC performance in more detail. Figure 5.14(a) shows the LSV results and applied-bias-photon-to-current efficiency (ABPE). External bias (V_b) must be applied between the photoelectrode and counterelectrode for small bandgap materials, such as Si, with the resulting ABPE being given by:

$$\text{ABPE} = \left[\frac{|j(mA\ cm^{-2})| \times (1.23 - |V_b|)(V)}{I\ (mW\ cm^{-2})}\right] \times 100\% \qquad (2)$$

where j = photocurrent density, I = 100 mW/cm^2 in this work, V_b = potential versus ideal counterelectrode. The calculated ABPE for the 4-unit-cell STO on p-Si with 1 μm diameter Ti/Pt catalyst is 2.9%. Stability measurements were conducted using chronoamperometry at a fixed potential of 0 V versus Ag/AgCl. As shown in Fig. 5.14(b), no degradation was observed after 10 hr operation, suggesting stable photocathode performance. The small fluctuation of photocurrent was due to the produced hydrogen bubbles coming off the photocathode surface. The inset figure shows a gas chromatography response of the gaseous product collected at the photocathode, confirming hydrogen production.

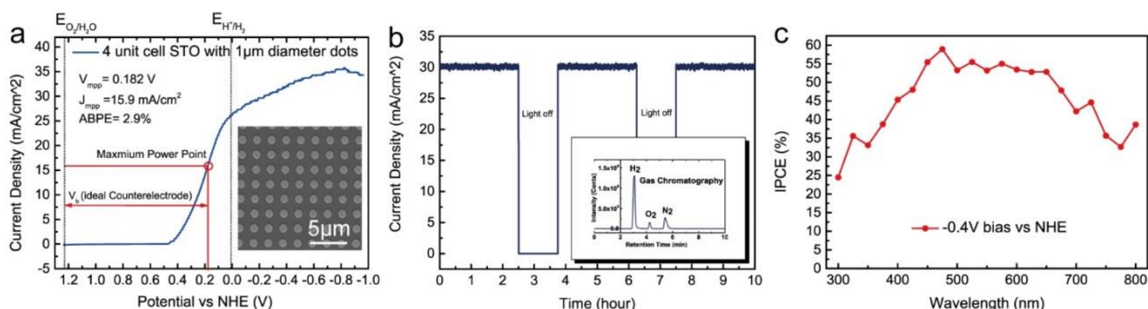

Figure 5.14. (a) Linear sweep voltammetry of 4 unit-cell 20 nm Pt/30 nm Ti/STO/p-Si (001) sample. The diameter and spacing of Pt/Ti dots are 1 μm and 2 μm, respectively, as shown in the inset top view SEM image. (b) Stability, as indicated by steady-state photocurrent characterization with device held at 0 V versus Ag/AgCl under 100 mW/cm^2 illumination in 0.5M H_2SO_4. Inset figure is gas chromatography of produced gas. (c) Incident photon-to-photocurrent efficiency (IPCE) was measured at applied potentials using xenon arc lamp equipped with a monochromator.

Incident-photon-to-current conversion efficiency (IPCE), was also determined for this device and is given by:

$$\mathrm{IPCE} = \frac{1239.8\ (V\ nm)\times|j\ (mA\ cm^{-2})|}{P_{mono}\ (mW\ cm^{-2})\times\lambda(nm)} \qquad (3)$$

where j = photocurrent density, P_{mono} = monochromated illumination power intensity and λ = wavelength. As illustrated in Fig. 5.14(c), the shape of the IPCE curve accords well with traditional silicon-based solar cells with effective current response from 475 - 725 nm.

Comparing LSV results for the 4-unit-cell samples in Fig. 5.13(c) and Fig. 5.14(a), we found the performance was improved by decreasing the size of metal catalyst. Since the total thickness of the bilayer metal catalyst is 50 nm, light can only be absorbed by uncovered regions. A potential inversion channel is formed underneath the oxide layer along which electrons can travel to adjacent metal catalyst, as shown in Fig. 5.15(a). However, during long distance travel in an inversion layer, electrons will suffer from electron-phonon scattering and electron-hole recombination. In addition, decreasing the ratio of covered region to exposed surface area will enhance light absorption and performance. For these reasons, we explored nanosize metal catalysts to increase PEC performance.

Metal nanostructures can be fabricated in many ways. Electron-beam lithography could define nanostructures precisely but suffers from limited throughput and high cost. In nanocrystal-nonvolatile-memory devices, nanocrystals are obtained by annealing of a thin-film meta. However, as discussed earlier, a 30 nm Ti layer with 20 nm Pt is utilized for improved work function and performance of the MIS structure. It is difficult to create nanocrystals by annealing with a bilayer metal. As an alternative method for metal catalyst nanostructuring, we employ nanosphere lithography. It is an inexpensive, maskless process for submicron scale structure fabrication and is compatible with bilayer metal deposition. The nanosphere lithography process flow for producing the Ti/Pt nanostructures is shown schematically in Fig. 5.15(b). From left to right are nanosphere deposition (Langmuir-Blodgett method), metal deposition, and nanosphere lift-off. A

scanning electron microscopy (SEM) image of the Ti/Pt nanostructured surface is shown in Fig. 5.15(b).

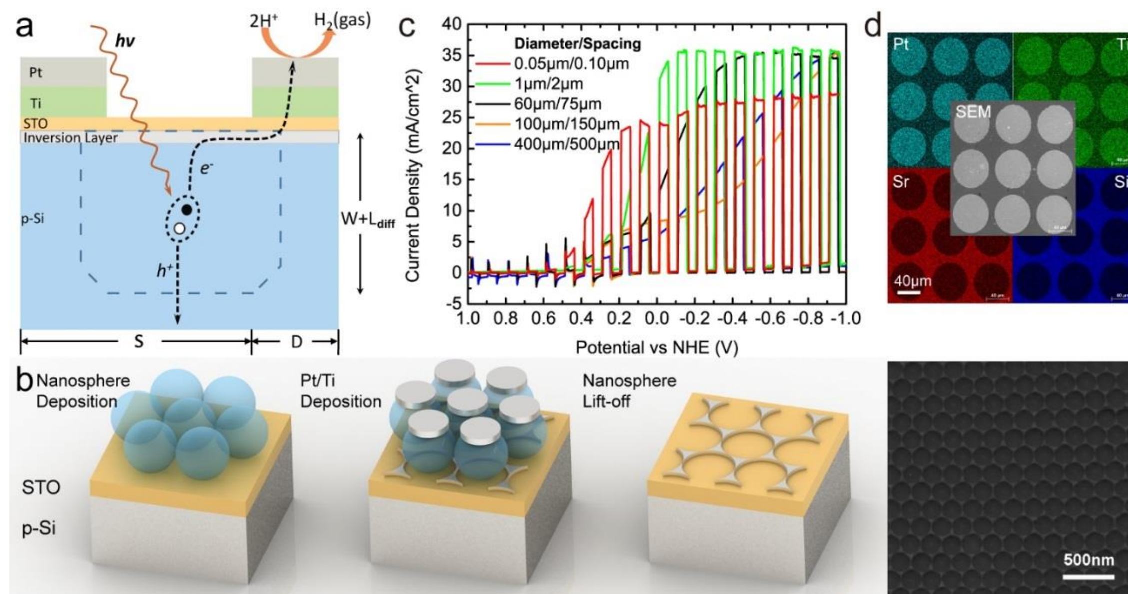

Figure 5.15. (a) Schematic plot of minority carrier transport. W = depletion width, L = electron diffusion length, D = metal dots diameter, S = spacing of adjacent metal dots. (b) Schematic nanosphere lithography process. From left to right are nanosphere deposition, metal deposition and nanosphere lift-off. The final structure was characterized by SEM. (c) Linear sweep voltammetry of 4 unit-cell 20 nm Pt/30 nm Ti/STO/p-Si (001) sample with various metal catalyst feature size. (d) Energy Dispersive X-ray (EDX) image of 4 unit-cell sample with 60 μm catalyst metal feature size is shown. 60 μm feature size sample was chosen due to the resolution limit of EDX.

LSV results and a summary of the measurements for samples with different metal catalyst size are presented in Fig. 5.15(c) and Table 1. W_{dep} is the depletion width and L_{diff} is the diffusion length of electrons. In the p-Si substrate, we estimate $W_{dep} \sim 2$ μm and $L_{diff} \sim 60$ μm for the wafer doping concentration we used. D and S represents the diameter and spacing of the metal catalyst, respectively, and L_t is the maximum distance an electron needs to travel to the nearest metal catalyst. For $L_t > L_{diff}$ (D/S of 100 μm/200

μm and 400 μm/500 μm), efficiency is enhanced with decreasing surface coverage ratio due to increased light absorption, as seen in Fig. 5.15(c) and Table 1. However, for feature size larger than 100 μm, the fill factor in the LSV measurements shown in Fig. 5.15(c) is very low for two reasons. First, for electrons traveling in the inversion layer, the large channel length will introduce more electron-phonon scattering and recombination, which decreases the current density. Second, only some of the photogenerated electrons can be injected into the inversion layer. The rest of the electrons will transport by diffusion into the bulk. This can be seen in samples with D/S of 60 μm/75 μm. Though having the same surface coverage ratio as the 400 μm /500 μm structure, the 60 μm/75 μm sample has much higher fill factor compared to the 400 μm/500 μm sample since $L_t < L_{diff}$ for the 60 μm/75 μm sample. For $L_t < L_{diff}$, a smaller coverage ratio also yields higher efficiency as seen from comparing the 60 μm/75 μm with the 1 μm/2 μm sample. However, by observing LSV for the 60 μm/75 μm, 100 μm/200 μm and 400 μm/500 μm samples, we found they all present a kink around 0 V versus NHE, in which region the photocurrent density remains at a low level. This suggests that there must be another limiting factor. By comparing 0.05 μm/0.1 μm and 1 μm/2 μm samples, it can be found that the ABPE is doubled if $L_t \ll W_{dep}$. The origin for this phenomenon is currently unclear and further study is in progress. The 0.05 μm/0.1 μm sample created by nanosphere lithography achieves a record-high 4.9% ABPE for water reduction in a single junction Si-photocathode, where the photogenerated electrons only need to travel very short distances to the nearest metal catalyst.

Table 5.2. Relationship between D/S, coverage factor, and ABPE.

D/S (μm/μm)	Coverage Ratio ($\pi D^2/4S^2$)	Maximum Distance to Metal Catalyst (μm)	ABPE (%)
0.05/0.1	~0.196	0.1	4.9%
1/2	0.196	1.8	2.9%
60/75	0.5	46	1.25%
100/200	0.196	183	1.23%
400/500	0.5	307	0.78%

D = Diameter of metal catalyst, S = Spacing between metal catalyst structures

5.6. SUMMARY

Crystalline STO films have been grown by ALD on Si(001) substrates using a four-unit-cell STO template layer grown by MBE. Stoichiometric, crystalline films were obtained using a 1:1 (Sr:Ti) cycle ratio at a deposition temperature of 250 °C. XRD and cross-sectional TEM analysis verified the high degree of crystallinity in the as-deposited STO films. *In situ* XPS analysis revealed minimal, if any, interfacial amorphous layer at the STO-Si interface. The successful integration of epitaxial oxide films on Si(001) substrates by ALD, using a thin STO buffer layer grown by MBE, is a promising method for large-scale fabrication of multifunctional perovskites integrated with semiconductor technology.

We also demonstrated that the epitaxial STO/Si heterojunction is an efficient and stable photocathode for water splitting. High photocurrent density (35 mA/cm^2), onset potential shift (450mV), and long-time stability were achieved due to the single crystalline nature of STO, lattice matching, crystalline interface quality and negligible

conduction band offset between STO and Si. In addition, we extended work on the relation between size of surface metal catalyst and efficiency. Results indicate that utilizing characteristic sizes smaller than the limiting factors -- diffusion length and depletion width -- would greatly increase the efficiency. Hence sub-100 nm nanostructures made by nanosphere lithography yielded the highest reported ABPE efficiency of 4.9%. This finding is not limited to STO/Si platform but should provide a general way for catalyst engineering.

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Chapter 6: Incorporation of La in epitaxial $SrTiO_3$ thin films grown by atomic layer deposition on $SrTiO_3$-buffered Si (001) substrates

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6.1. INTRODUCTION

The monolithic integration of crystalline oxides on Si (001) has presented opportunities to extend and enhance silicon technology.[1-3] Since the early 2000s, several groups have reported on the direct deposition of epitaxial strontium titanate, $SrTiO_3$ (STO), on Si (001) substrates.[4-12] Furthermore, creation of STO pseudo-substrates has opened up a route to the integration of functional oxides and heterostructures onto a silicon platform. The use of a ferroelectric gate dielectric in a field-effect transistor (the so-called FeFET) has been proposed as a means to reduce the sub-threshold slope of the field-effect transistor below the thermodynamic limit of 60 mV/decade,[13] which is desired for low voltage, low power applications. Integration of the ferroelectric perovskite $BaTiO_3$ (BTO) with Si (001) is considered a prime material candidate for the aforementioned FeFETs.[14] However, the direct integration of BTO on Si (001) is challenging due to the large lattice mismatch (~4.4% at 25 °C) and the reaction of Si with oxygen to form amorphous SiO_2. To resolve this issue, several groups have utilized a STO buffer layer to facilitate growth of BTO on Si (001),[14-19] demonstrating the potential for an epitaxial oxide FeFET gate stack.

Recent theoretical work has suggested that a thin conductive layer coupled between the semiconductor channel and ferroelectric layer can help modulate current

[IV] M. D. McDaniel, A. Posadas, T. Q. Ngo, C. Karako, J. Bruley, V. Narayanan, A. A. Demkov, and J. G. Ekerdt, "Incorporation of La in epitaxial $SrTiO_3$ thin films grown by atomic layer deposition on $SrTiO_3$-buffered Si (001) substrates," J. Appl. Phys. **115**, 224108-(1-8) (2014). MDM designed and performed experiments. MDM, AP, TQN, CK, JB, VN, AAD, and JGE contributed to the conception and analysis of data. JB acquired transmission electron microscopy data.

flow through the semiconductor to achieve steep sub-threshold swing (< 60 mV/decade).[20,21] A material candidate for this conductive layer is $La_xSr_{1-x}TiO_3$ (La:STO), which is stable in contact with silicon under appropriate growth conditions and can be paired with a crystalline ferroelectric. An epitaxial oxide heterostructure based on conductive La:STO and ferroelectric BTO, integrated with Si for use as a FeFET gate stack, is motivation for the current work.

The electrical properties of La:STO single crystals have been studied previously, showing resistivity values in the range of 10^{-4}-10^{-3} Ω-cm at room temperature.[22] The mobility of bulk La:STO single crystal is reported to be around 5-7 cm^2/V-s at room temperature.[23] Polycrystalline La:STO ceramics and powders, however, have shown significantly higher resistivity values (10^{-2}-1000 Ω-cm) at room temperature compared with the single crystal values. Resistivity measurements of La:STO (x~0.10) powders exhibited semiconducting behavior in stark contrast to the metallic single crystal data.[24] Further studies have directly compared the electronic transport in La:STO single crystals versus polycrystalline ceramics,[25] where the electrical behavior of the ceramics was governed by grain boundaries. The resistivity reported for La:STO (x~0.10) ceramics was ~ 1×10^{-2} Ω-cm at room temperature, over two orders of magnitude higher than the single crystal value. In separate work, the resistivity of La:STO powders changed by four orders of magnitude depending on the atmosphere during sintering.[26] Lower resistivity values (~1×10^{-2} Ω-cm) were reported for powders sintered in reducing environments as compared to powders sintered in air with much higher resistivities (~100 Ω-cm). More recently, Buscaglia *et al.* reported on thermal and electrical conductivity of La:STO (x~0.10) ceramics of varying grain size and different annealing temperatures for 24 h in Ar-5% H_2 atmosphere.[27] Samples annealed at 800 °C with small grain sizes of ~28 nm

exhibited high resistivities (~1000 Ω-cm) as compared with samples annealed at 1400 °C with larger grain sizes of ~6.2 μm and much lower resistivities (~2 × 10^{-3} Ω-cm).

Electrical measurements have been reported previously for epitaxial La:STO thin films grown on different single-crystal substrates $LaAlO_3$ (LAO), STO, and $(LaAlO_3)_{0.3}(Sr_2AlTaO_6)_{0.7}$ (LSAT).[28-30] Olaya *et al.* reported resistivities on the order of ~1 × 10^{-1} to 2 × 10^{-2} Ω-cm for 150-nm-thick epitaxial La:STO (x~0.01) films on LAO and STO single-crystal substrates grown using laser ablation, with low-temperature (4 K) mobilities between 8-131 cm^2/V-s and room temperature mobilities between ~1-10 cm^2/V-s.[28] In contrast, extremely high mobilities (30,000 to 120,000 cm^2/V-s) were reported at low temperatures (~2 K) for ~ 800-nm-thick epitaxial La:STO films with very low La concentrations (x~10^{-4}) grown using metal-organic molecular beam epitaxy on STO single-crystal substrates.[29,30] The wide range of resistivity values and mobilities reported for La:STO may be attributed to the differences in film thickness, La concentration, and crystal quality. Recent work within our group has examined thinner films (~20-nm-thick) of La:STO (x~0.05-0.25) grown on insulating oxide substrates STO, LAO, LSAT, and $DyScO_3$.[31] At room temperature, the thin film resistivities ranged from ~1 × 10^{-5} (x~0.25) to 1 × 10^{-2} Ω-cm (x~0.05) with mobilities ~1-9 cm^2/V-s. High-temperature annealing (~750 °C) was required after film deposition to obtain complete electrical activation of the incorporated La species. The necessity for high-temperature annealing may be problematic when integrating La:STO with Si (001), due to the reaction of STO and Si at temperatures above ~650 °C,[32] especially when an abrupt interface is desired for a FeFET.

The growth of epitaxial La:STO thin films directly on Si (001) has already been demonstrated by molecular beam epitaxy (MBE).[33] Subsequent growth of BTO by MBE is then possible; however, the elevated growth temperatures in the presence of oxygen

often lead to formation of a significant (> 2 nm) SiO_2 amorphous layer at the STO-Si interface.[14,18,19] The formation of a low-k amorphous SiO_2 in series with the ferroelectric is undesirable for the ferroelectric field effect. In addition, the formation of amorphous SiO_2, and subsequent strain relaxation of STO,[34] tends to favor a polar axis lying in-plane rather than out-of-plane as the stacks are cooled down to room temperature.[15,19] Lower temperature growth methods, such as atomic layer deposition (ALD), provide an alternative route for integrating epitaxial oxides onto Si.

In previous work, we demonstrated a combined MBE-ALD growth technique for integrating epitaxial oxides onto Si, which minimized formation of an amorphous layer at the STO-Si interface.[35,36] A four-unit-cell STO buffer layer grown on Si (001) by MBE provided a stable template for the growth of several crystalline oxides, including anatase TiO_2, STO, BTO, and LAO.[35-38] Crystalline BTO grown by this method was c-axis oriented, indicating an out-of-plane polarization, with negligible amorphous layer and a sharp STO-Si interface.[38]

In this work, we validate the growth of crystalline La:STO films on Si (001) substrates using a combined MBE-ALD growth method. By modifying the cycling conditions of a layered oxide heterostructure, we demonstrate the selective incorporation of lanthanum into the STO lattice at the nanometer scale. This highlights the potential for this technique to be used for fabrication of an epitaxial oxide-based FeFET gate stack on Si. Detailed structural and initial electrical characterization of epitaxial La:STO films are reported.

6.2. EXPERIMENTAL DETAILS

STO thin films, ranging in thicknesses from 5-25 nm, were grown on silicon substrates with varying lanthanum concentrations. Thin film growth was done using a combined MBE and ALD technique. As originally reported, this combined MBE-ALD growth technique allows for crystalline film growth by ALD while minimizing interfacial reactions at the STO-Si interface.[35] Direct crystallization by a chemical-only method on Si has not been proven due to interfacial reactions and/or the formation of amorphous SiO_2. To circumvent this issue, the growth of a thin STO layer by MBE creates a stable template on Si (001), allowing for crystalline oxide growth by ALD.

After removal of the native silicon dioxide via a Sr-assisted deoxidation process, MBE was used to grow a template layer of 4 unit-cells (~1.6 nm) of STO using a variant of the Motorola-developed process.[39] The MBE system is a commercial DCA 600 equipped with reflection high-energy electron diffraction (RHEED) and a silicon carbide heater. In order to ensure a good crystalline template for ALD growth, the 4 unit-cell STO layer grown by MBE was crystallized by vacuum annealing at 550 °C. RHEED imaging was used to view the formation of the crystalline structure during annealing. Upon cooling, the STO-buffered Si (001) substrate was transported *in vacuo* to the ALD chamber to grow La:STO.

The growth of La:STO films is similar to undoped STO, where some of the Sr subcycles are replaced with La subcycles. The supercycle is described as x La subcycles: y Sr subcycles: z Ti subcycles, where generally $(x + y) = z$ for stoichiometric films under the reported conditions. La:STO thin films were grown by ALD at 225 °C using strontium bis(triisopropylcyclopentadienyl) [$Sr(^iPr_3Cp)_2$] (HyperSr),[40] lanthanum tris(N,N'-diisopropylformamidinato) [$La(^iPr_2\text{-fmd})_3$] (La-FAMD),[41] titanium tetraisopropoxide [$Ti(O\text{-}^iPr)_4$] (TTIP),[42] and purified water as co-reactants. The

precursor dosing times were each 2 sec followed by a 15 sec purge. HyperSr, La-FAMD, and TTIP were vaporized at 135 °C, 110 °C, and 40 °C, respectively, and water was held at room temperature (26 °C). The water dosing was regulated using an in-line needle valve. The ALD chamber is a cross-flow type reactor that is maintained at ~1 torr during deposition. The carrier/purge gas (ultrahigh purity argon) and precursors were introduced through a common manifold at the front of the chamber. Following ALD growth, the samples were post-deposition annealed in vacuum between 550-650 °C for 5 min.

After finishing the film growth and annealing, the sample was again transported *in vacuo* to the x-ray photoelectron spectroscopy (XPS) chamber for analysis. XPS was performed *in situ* with a monochromatic Al Kα source at 1486.6 eV using a VG Scienta R3000 XPS system to determine the film composition and to verify the absence or presence of SiO_x at the STO-Si interface. Analysis of the XPS data also revealed the percentage of lanthanum incorporation, x = La/(Sr+La), where the atomic values were quantified using CasaXPS. The analyzer is calibrated using a silver foil, where the Ag $3d_{5/2}$ core level is defined to be at 368.28 eV and the Fermi level of Ag at 0.00 eV. High-resolution spectra of the Sr 3*d*, La 3*d*, Ti 2*p*, O 1*s*, C 1*s*, and Si *2p* core levels are measured using a pass energy of 100 eV with an analyzer slit width of 0.4 mm. Each high-resolution scan is measured four times and summed, using 50 meV steps with a dwell time of 157 ms per step. Film composition was estimated using CasaXPS (ver. 2.3.16) peak fitting, where the integrated intensities are divided by the Wagner relative sensitivity factors after a Shirley background subtraction.[43] Additionally, a thickness dependent energy exponent between 0 and 0.78 is used to account for the variation of electron escape depth with kinetic energy.[44] The maximum exponent value (0.78) was calibrated using an STO single crystal substrate (MTI Corp.) where the Sr:Ti ratio was assumed to be 1:1.

X-ray reflectivity (XRR), X-ray diffraction (XRD), and rocking curve analysis, were performed to analyze the thickness, structure, and crystalline quality of the La:STO films, respectively. X-ray analysis was conducted using an X'PERT Powder Diffractometer using a sealed tube Cu Kα radiation (λ ~ 1.5406 Å). Additionally, the crystalline structure and interface quality of a La:STO/STO heterostructure grown on Si (001) was verified by transmission electron microscopy (TEM). The TEM samples were prepared using the focused ion beam (FIB). Observations were made in dark field scanning TEM mode using an FEI TITAN microscope fitted with a probe aberration corrector and a Gatan Quantum energy-loss imaging filter. Elemental maps were acquired by electron energy-loss spectrometry with an acquisition time of 0.05 s per pixel. The maps represent the net counts under the respective Si-K, La-M, O-K, Ti-L, and Sr-M ionization edges after power law background removal.

Resistivities of the La:STO films were measured using the van der Pauw method. Electrical contacts were created on the La:STO surface via gold sputter deposition with a gallium-indium eutectic alloy above. The sputtered gold provided a wetting layer between the gallium-indium liquid metal contacts and the La:STO film. The gallium-indium droplets were micropipetted onto the gold contacts. Electrical testing was performed using a four-point probe station with a Keithley 4200 semiconductor characterization system. The cat whisker probe tips were carefully brought into contact with the gallium-indium to avoid penetrating the thin film surface. Intrinsic silicon substrates (ρ > 10 kΩ-cm) were used for all the electrical measurements. By initially measuring the bare Si substrate, the sheet resistance of the La:STO/Si heterostructure was used to estimate the resistivity of the La:STO epitaxial film.

6.3. RESULTS AND DISCUSSION

6.3.1. Deposition and Crystallization of $La_xSr_{1-x}TiO_3$

Incorporation of lanthanum at varying concentrations (x~0.02-0.20) into STO thin films was accomplished by adjusting the ALD cycling conditions. The A:B cycle ratio, where A and B are the (Sr+La) and Ti cations, respectively, was set between 1:1 to 4:3 to achieve stoichiometric to slightly A-rich films (up to 60%). The average growth rate was estimated from the total number of subcycles (Sr, La, and Ti). Based on XRR thickness estimates, the growth rate was found to vary between 0.05 – 0.07 nm / subcycle in the range of La concentrations studied. Correct stoichiometry ensured crystallization of the La:STO film upon post-deposition vacuum annealing between 550-650 °C. In general, higher La content required slightly higher temperatures for crystallization. Compositional analysis of the La:STO films was performed via *in situ* XPS analysis before and after the vacuum annealing.

Representative XPS core level spectra are shown in Figure 6.1 for the Sr 3*d*, La 3*d*, Ti 2*p*, and C 1*s* / Sr $3p_{1/2}$ after growth and annealing of a 7.5-nm-thick La:STO thin film (x~0.15). The sample was post-deposition annealed in vacuum at 550 °C for 5 min. Compositional analysis shows the film is nearly stoichiometric with an overall A:B ratio of 50.3 to 49.7. The Sr and La features (Fig. 6.1(a) and 6.1(b)) are consistent with fully oxidized species, Sr^{2+} and La^{3+}. The Ti spectrum (Fig. 6.1(c)) shows a majority of the Ti signal is consistent with Ti^{4+}, with the addition of a small Ti^{3+} feature at slightly lower binding energy. We attribute the Ti^{3+} to the incorporation of La into the STO lattice, which is expected to donate one electron per La atom. Under similar growth and annealing conditions, undoped STO films do not show any Ti^{3+} feature. Therefore, we expect the ratio of Ti^{3+} to total Ti to correlate with the amount of electrically active (electron-donating) La species. For this sample, vacuum annealing at 550 °C appeared to

crystallize the La:STO film completely; however, only a small portion of the La appeared electrically active (~13% of the total La) based on the Ti^{3+} signal. This result was somewhat unexpected since the crystallization is often associated with the activation of dopants with semiconductors. The correlation between La activation and annealing temperature is discussed further in Section 3.2.

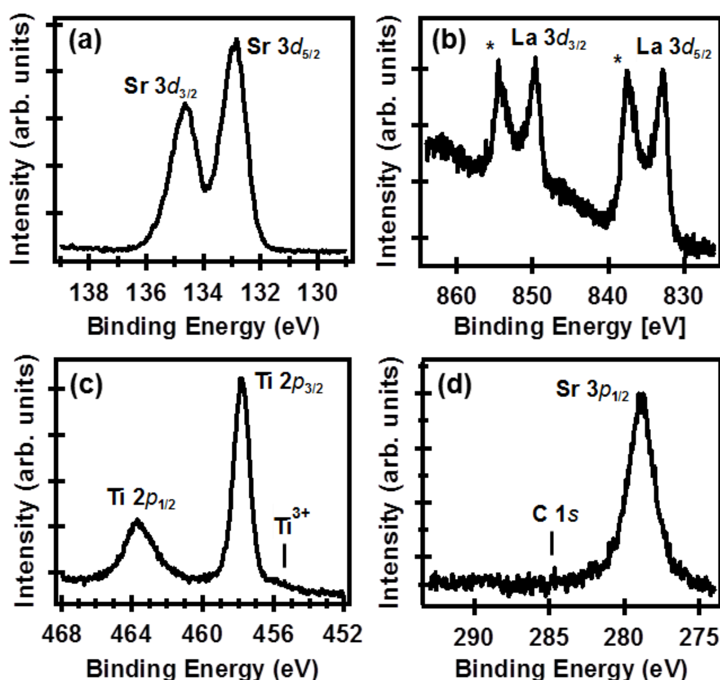


Figure 6.1. X-ray photoelectron spectra of a 7.5-nm-thick La:STO (x~0.15) film grown on STO-buffered Si (001) by ALD with post-deposition annealing at 550 °C for 5 min. High-resolution scans of the relevant core levels are shown for (a) Sr 3*d*, (b) La 3*d*, (c) Ti 2*p*, and (d) C 1*s* / Sr 3$p_{1/2}$. For the La 3*d* spectrum in (b), the * denotes the shake-up satellite peaks.

La:STO films of good crystalline quality were grown for several different La concentrations up to ~20%. Representative RHEED images are shown in Figure 6.2 for La concentrations of 10%, 15%, and 20%. Higher La concentration (above ~25%) did not maintain good epitaxial relation with the Si substrate, resulting in polycrystalline

films that had (001) preferred orientation. This is likely associated with the phase transition from cubic (*Pm3m* space group) to orthorhombic (*Ibmm* space group) for La concentrations above ~20%.[24] Nevertheless, STO thin films grown by ALD with up to 20% La concentration can be crystallized in the cubic perovskite structure with epitaxial registry to the underlying Si substrate.

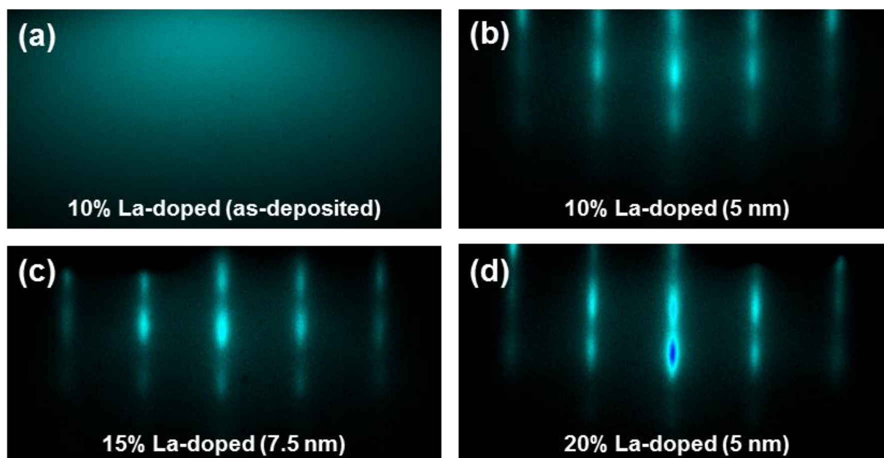


Figure 6.2. Reflection high-energy electron diffraction images captured (a) before and (b) after post-deposition annealing of a 5-nm-thick La:STO film (*x*~0.10) grown by ALD, and images after post-deposition annealing of (c) a 7.5-nm-thick La:STO film (*x*~0.15) and (d) a 5-nm-thick La:STO film (*x*~0.20). All three samples were post-deposition annealed in vacuum at 550 °C for 5 min. Images are taken along the [110] azimuth.

X-ray analysis of a 15-nm thick La:STO film (*x*~0.18) is shown in Figure 6.3. The thickness can be estimated from XRR (Fig. 6.3(a)) where the period of the oscillations is related to the thickness of the film via Bragg's Law. The θ-2θ scan shown in Fig. 6.3(c) is consistent with the cubic perovskite structure of STO. Only the (00n) reflections are present due to the *c*-axis orientation. The STO (002) peak position is found to be 46.5 ± 0.1°, indicating that the La:STO film is relaxed to the nominal bulk value (~3.91 Å). Previous work has shown that there is only a slight increase in the

lattice parameter of STO with La incorporation, where the lattice parameter increased from 3.905 Å (bulk STO) to 3.909 Å for La:STO (*x*~0.10).[45] When considering ionic radii, the increase in lattice parameter is consistent with the increased size of Ti^{3+} (0.76 Å) versus Ti^{4+} (0.68 Å) for 6-fold coordination.[22] The rocking curve shown in Fig. 6.3(b) is taken at a fixed 2θ-angle of 46.5°. The full-width at half-maximum (FWHM) was found to be 0.50°, indicating a reasonable degree of out-of-plane orientation for the 15-nm-thick La:STO film.

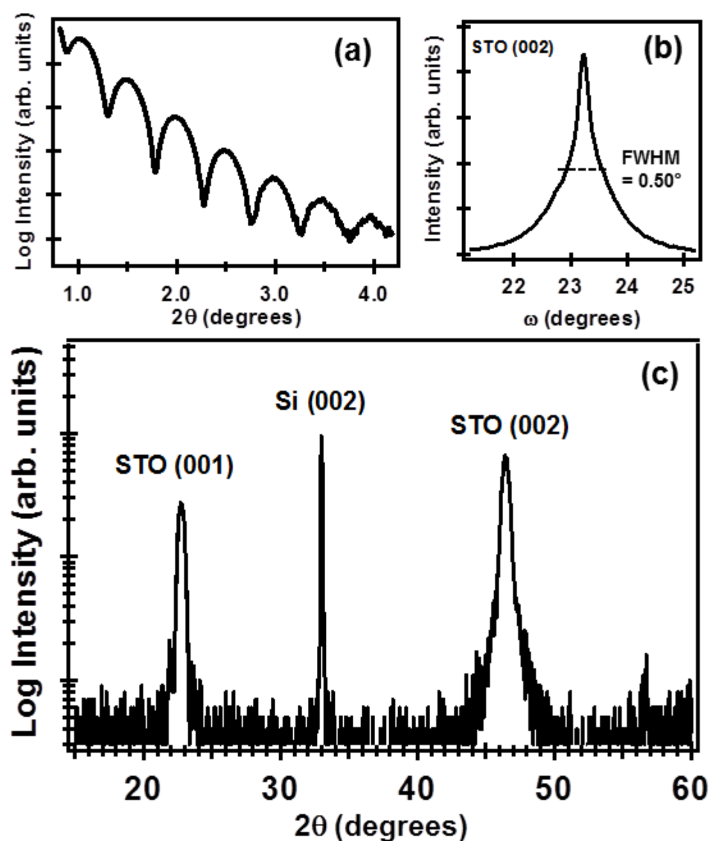


Figure 6.3. X-ray analysis of a 15-nm thick La:STO film (x~0.18) grown by ALD: (a) X-ray reflectivity curve, (b) rocking curve of the STO (002) reflection taken at a fixed 2θ-angle of 46.5° showing a full-width half-maximum of 0.50°, and (c) the θ-2θ diffraction scan. The sample was post-deposition annealed in vacuum at 550 °C for 5 min.

6.3.2. La activation and the STO-Si interface quality

When considering post-deposition annealing of the La:STO films, there is a delicate balance between electrical activation of the La species and the quality of the STO-Si interface. Electrical activation of the La atoms (*i.e.*, transfer of a La electron to the conduction band) in STO requires increased annealing temperatures, which is problematic when trying to avoid interfacial reaction between STO and Si. As mentioned previously, the amount of Ti^{3+} is expected to correlate with the amount of electrically active La species, where one electron is donated per La atom. Therefore, the total number of La atoms incorporated in the STO lattice should be equal to the amount of Ti^{3+} (*i.e.*, La:Ti^{3+}~1:1) for complete La activation. Interestingly, after ALD growth and post-deposition annealing at 550 °C, the La:STO film appeared fully crystallized by RHEED, XRD, and TEM, suggesting that the La is substituted on the A-site; however, the La:Ti^{3+} ratio differs significantly (La:Ti^{3+}~1:0.1). This could be associated with incomplete La activation due to the incorporation of a charged anion or cation vacancies in the film. The incorporation of excess oxygen and/or presence of Sr vacancies as acceptor defects in La:STO films has been investigated previously.[26,46-49] La:STO with La concentration as high as 20% is reported to be completely self-compensating by the incorporation of excess oxygen.[46]

To study the effect of post-deposition annealing on La activation, several La:STO films were subjected to increasing post-deposition annealing temperatures from 550 °C to 650 °C. Higher annealing temperatures of La:STO films with the same La concentration resulted in an increase of Ti^{3+} due to increased electrically active La species or thermal/chemical reduction of Ti^{4+} through annealing. Undoped STO films annealed under similar conditions do not show the presence of any Ti^{3+} species, suggesting that the increase of Ti^{3+} observed here is due to the increased La activation. Shown in Figure 6.4

is a comparison of Ti 2*p* core level spectrum between a 20-nm-thick La:STO film (x~0.15) with post-deposition annealing at 550 °C and 650 °C. Since the 20-nm thickness of the film is greater than the electron escape depth, the Ti^{3+} is attributed to the activated La species in the La:STO film rather than reduced Ti at the STO-Si interface. The higher annealing temperature results in the percentage of Ti^{3+} increasing from ~2.7% to about 13.8%. For complete La activation, ~15% Ti^{3+} is expected for La:STO when x~0.15.

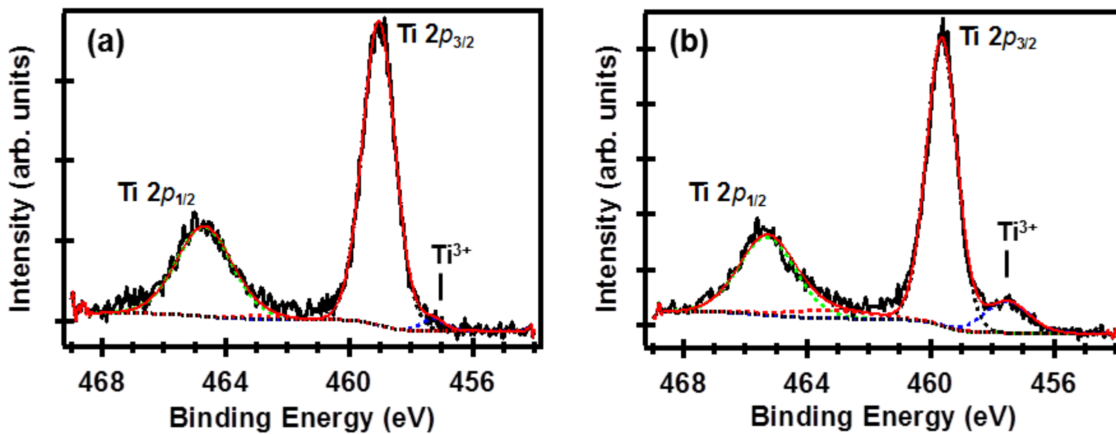


Figure 6.4. X-ray photoelectron spectrum of the Ti 2*p* core level for a 20-nm-thick La:STO film (x~0.15) with post-deposition vacuum annealing at (a) 550 °C and (b) 650 °C. Deconvolution of the spectrum was done in CasaXPS to show the relative contribution of Ti^{4+} and Ti^{3+} species.

Despite the improvement in La activation with higher annealing temperature, there is concern of the interface stability between STO and Si at these elevated temperatures. The interface quality between STO and Si was investigated through cross-sectional TEM and *in situ* XPS. Figure 6.5 shows a cross-sectional TEM image of a La:STO film (x~0.20) grown on STO-buffered Si (001), confirming the high crystalline quality of the La:STO film and epitaxial registry to the Si substrate. The low temperature

ALD process and post-deposition vacuum annealing at temperature at 550 °C for 5 min results in only a small amorphous interfacial layer (~0.5 nm). In addition, there is an abrupt transition between the ALD-grown La:STO and MBE-grown STO template layer. However, higher vacuum annealing (required for full La activation) resulted in increased interfacial reaction between STO and Si.

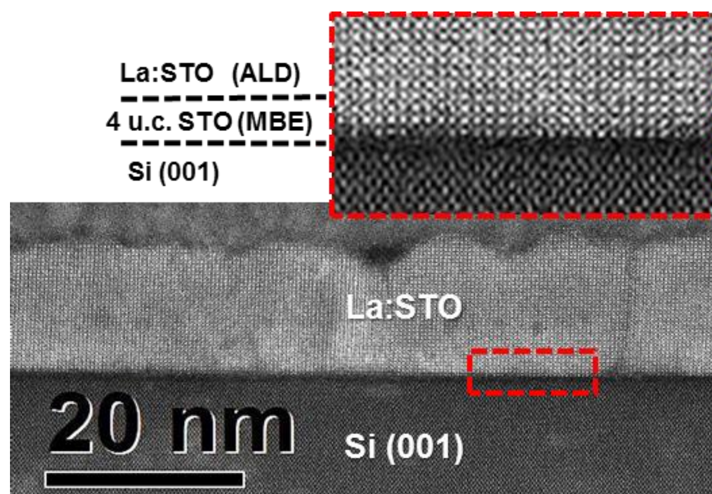


Figure 6.5. Cross-sectional transmission electron micrograph of a 15-nm-thick La:STO film (x~0.20) grown on STO-buffered Si (001). The post-deposition annealing at 550 °C for 5 min still maintains a relatively clean STO-Si interface.

The effect of higher annealing temperatures was observed using *in situ* XPS by growing a thin (~3 nm) La:STO film by ALD and observing the change in the Si 2*p* and Ti 2*p* core level before and after post-deposition annealing. The change in the Si 2*p* core level could not practically be quantified due to the overlapping of the La 4*d* core level. Alternatively, the Si 2*s* core level could be used, but the signal is not as well-defined. Regardless, the observation of the Ti 2*p* core level with increasing annealing temperature from 600 °C to 650 °C is shown in Figure 6.6. Comparison of the two spectra clearly shows that there is significantly more interfacial reaction as a result of increased

annealing temperature. Both La:STO films had ~15% La incorporation, allowing for some Ti^{3+} formation to be attributed to the La activation. However, with annealing at 650 °C, there is a significant portion (>60%) of the Ti signal that is reduced to Ti^{3+} and even Ti^{2+}. This is a result of the interfacial reaction between STO and Si at temperatures of ~650 °C.[32] Therefore, despite increasing the La activation (as observed with the 20-nm-thick La:STO film), the increased annealing temperature causes interfacial reaction at the STO-Si interface. For some applications, including the FeFET epitaxial oxide stack, this amorphous interfacial layer would be highly undesirable.

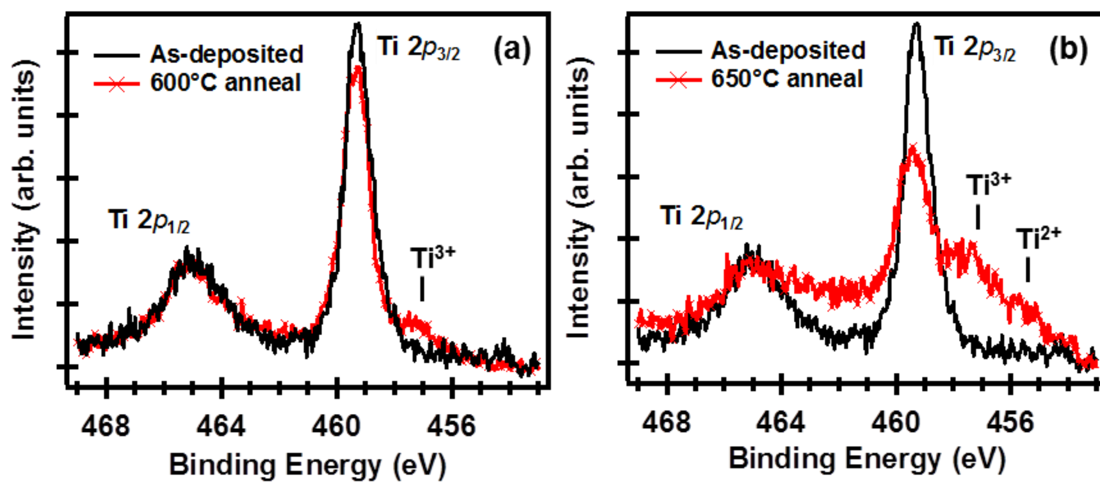
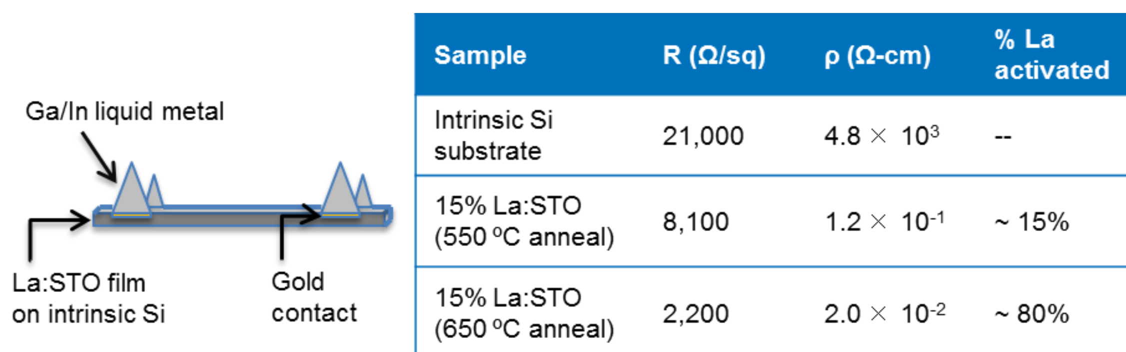


Figure 6.6. X-ray photoelectron spectrum of the Ti 2*p* core level for 3-nm-thick La:STO films (x~0.15) taken before (black line) and after (red line) post-deposition vacuum annealing at (a) 600 °C and (b) 650 °C. Significant interfacial reaction is observed due to the increased annealing temperature.

6.3.3. Electrical measurements

To characterize the electrical resistivity of the La:STO thin films grown on the STO-buffered Si (001) substrate, intrinsic Si substrates (ρ ~ 10 kΩ-cm) were used to minimize parasitic conduction through the Si layer. A 20-nm-thick La:STO film (x~0.15)

was tested after post-deposition annealing at 550 °C and 650 °C. The sheet resistance was measured at room temperature for both the La:STO film on Si and the bare intrinsic Si substrate, as shown in Figure 6.7. At lower annealing temperature (550 °C), only a small fraction (~15%) of the incorporated La appeared electrically active. The measured sheet resistance was 8,100 Ω/sq versus 21,000 Ω/sq for the bare Si substrate. With a higher post-deposition annealing (650 °C), there was significantly more Ti^{3+} observed by XPS (Fig. 6.4). This should correlate to more activated La species in the bulk of the film (interfacial contributions are negligible since the film is 20-nm thick). Under the same measurement conditions, the increased annealing temperature indeed led to a lower sheet resistance of 2,200 Ω/sq.



Sample	R (Ω/sq)	ρ (Ω-cm)	% La activated
Intrinsic Si substrate	21,000	4.8×10^{3}	--
15% La:STO (550 °C anneal)	8,100	1.2×10^{-1}	~ 15%
15% La:STO (650 °C anneal)	2,200	2.0×10^{-2}	~ 80%

Figure 6.7. (left) Schematic of the electrical contacts used for estimating the resistivity of the epitaxial La:STO film grown on intrinsic Si (001), and (right) measured values for the sheet resistance (R), the calculated resistivity of the La:STO film (ρ), and the estimated percent of La activation in the La:STO film after post-deposition annealing.

To estimate the resistivity of the La:STO thin film, the substrate and film were modeled as simple resistors in parallel, recognizing that there is still some conduction through the Si substrate. Using the sheet resistance measured for the bare Si substrate and measuring the sheet resistance with the La:STO film, the resistance due to the film

could be calculated. For a 20-nm-thick film, the resistivity of the La:STO film was found to be 1.2×10^{-1} and 2.0×10^{-2} Ω-cm for post-deposition annealing at 550 °C and 650 °C, respectively. Based on the amount of Ti^{3+} (*i.e.*, activated La concentration) being equal to the carrier concentration, the mobility at room temperature is estimated to be 0.14 and 0.15 cm^2/V-s for the La:STO film annealed at 550 °C and 650 °C, respectively. For the sample annealed at 650 °C, there may be some error introduced in estimating the mobility depending on the extent of the interfacial reaction. At the lower annealing temperature (550 °C), with negligible interfacial reaction, the estimated carrier concentration and mobility should be valid for the entirety of the doped film. Both the resistivity and mobility estimated here are 1-2 orders of magnitude lower than bulk La:STO single crystal, reported to have a resistivity of 10^{-3}-10^{-4} Ω-cm and a mobility around 5-7 cm^2/V-s at room temperature.[22,23]

There have been several discrepancies between the observed resistivity and mobility values of La:STO reported in the literature. The crystalline quality of the La:STO (polycrystalline vs. single crystals) appears to have a significant influence on the resistivity of La:STO. Resistivity measurements of La:STO (x~0.10) powders and ceramics have shown semiconducting behavior and higher resistivity (~1×10^{-2} Ω-cm) compared with the metallic single crystal data.[24,25] The source of the discrepancy is attributed to differences in Ti^{3+} concentration (activated La species) and the presence of grain boundaries. Most recently, Buscaglia *et al.* have reported on the observed thermal and electrical conductivity of 10% La:STO ceramics with different grain size.[27] Small grain sizes of ~28 nm had high resistivities (~1000 Ω-cm) as compared with larger grain sizes of ~6.2 μm with much lower resistivities (~7×10^{-2} Ω-cm), much closer to that of the bulk single-crystal La:STO value. For our epitaxial La:STO thin films, we do not expect a significant fraction of grain boundaries; however, deviations from ideal

crystalline order are observed in the rocking curve scans (FWHM~0.5°) and the presence of vertical domains and grain boundaries are observed in the cross-sectional TEM image of Figure 6.5. In addition, thin films will be significantly more affected by interface scattering as compared to bulk single crystals.

The electrical properties of epitaxial La:STO films have been reported previously.[28-30] Unfortunately, direct comparison with our current work is complicated because the films were grown on different single-crystal substrates (LAO, STO, and LSAT) and thicknesses of 1-2 orders of magnitude greater (150-nm-thick to 800-nm-thick). Resistivities were reported on the order of ~1×10^{-1} to 2×10^{-2} Ω-cm for 150-nm-thick epitaxial La:STO films on LAO and STO single-crystal substrates, with low temperature mobilities between 8-131 cm^2/V-s.[28] In other work, extremely high mobilities at low temperature (30,000 to 120,000 cm^2/V-s) were reported for ~ 800-nm-thick epitaxial La:STO films with extremely low La concentrations (x~10^{-4}) grown on STO single-crystal substrates.[29,30] Based on this wide disparity of reported data, we conclude that the electrical conductivity observed in La:STO thin films is highly dependent on the quality of the crystal, grain boundaries, interface scattering, and stoichiometric deviations. This makes accurate prediction of the electrical properties of thin epitaxial La:STO (< 20 nm) highly dependent upon the substrate (amount of strain) and growth conditions, such as temperature.

6.3.4. Selective La incorporation

The nanoscale control of ALD is highly desired for many applications, including modern electronics. In a recent report, it has been postulated that within the FeFET device structure, a thin conductive layer coupled between the semiconductor channel and ferroelectric layer is desired.[20,21] With an epitaxial oxide stack, La:STO would be a

convenient material system as the thin conductive layer between the semiconductor and ferroelectric (BTO) as well as the gate metal. To demonstrate the potential for this type of epitaxial oxide stack, an undoped STO layer was sandwiched between two La:STO layers epitaxially grown on Si (001) buffered with 4-unit-cell thick STO. The resulting heterostructure was La:STO (*x*~0.20) / undoped STO / La:STO (*x*~0.05) / STO-buffered Si (001). After each ALD-grown layer, the sample was post-deposition annealed at 550 °C for 5 min in vacuum to promote crystallization of the oxide film while minimizing reaction at the STO-Si interface.

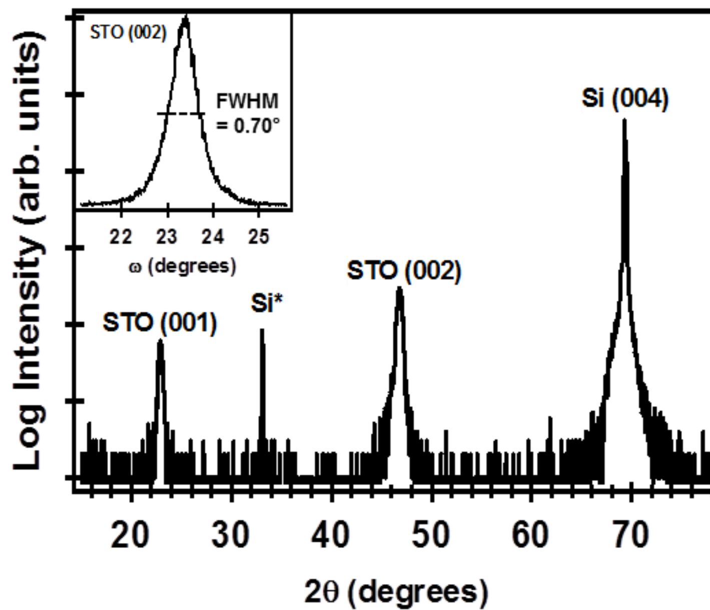


Figure 6.8. X-ray diffraction θ-2θ scan of a 20-nm thick La:STO (*x*~0.20) / STO / La:STO (*x*~0.05) / STO-Si (001) heterostructure. (inset) Rocking curve of the STO (002) reflection taken at a fixed 2θ-angle of 46.5° with a full-width half-maximum of 0.70°.

As shown in Figure 6.8, a θ-2θ XRD scan shows that the oxide stack is *c*-axis oriented with only the (00n) STO reflections present. The inset of Fig. 6.8 also shows that the heterostructure maintains reasonable out-of-plane orientation with a FWHM =

0.70°. The compositional variation observed by analytical electron microscopy highlights the control and selective incorporation of lanthanum in the crystalline STO heterostructure. As can be seen in Figure 6.9, the electron energy loss spectroscopy (EELS) compositional mapping shows the distribution of Si, Sr, Ti, O, and La throughout the oxide-silicon heterostructure. In particular, the distribution of La is confined to two areas: (1) a small region between the undoped STO and the Si substrate, which corresponds to the La:STO (x~0.05) layer and (2) the top region of the gate stack, which corresponds to the La:STO (x~0.20) layer. The high-resolution cross-sectional scanning TEM (right side of Fig. 6.8) shows well-defined and sharp interfaces between the STO and La:STO layers, as well as minimal SiO_x formation at the STO-Si interface (<0.5 nm). This demonstrates the potential for the combined ALD-MBE growth technique to be used in making a FeFET structure based on epitaxial oxides.

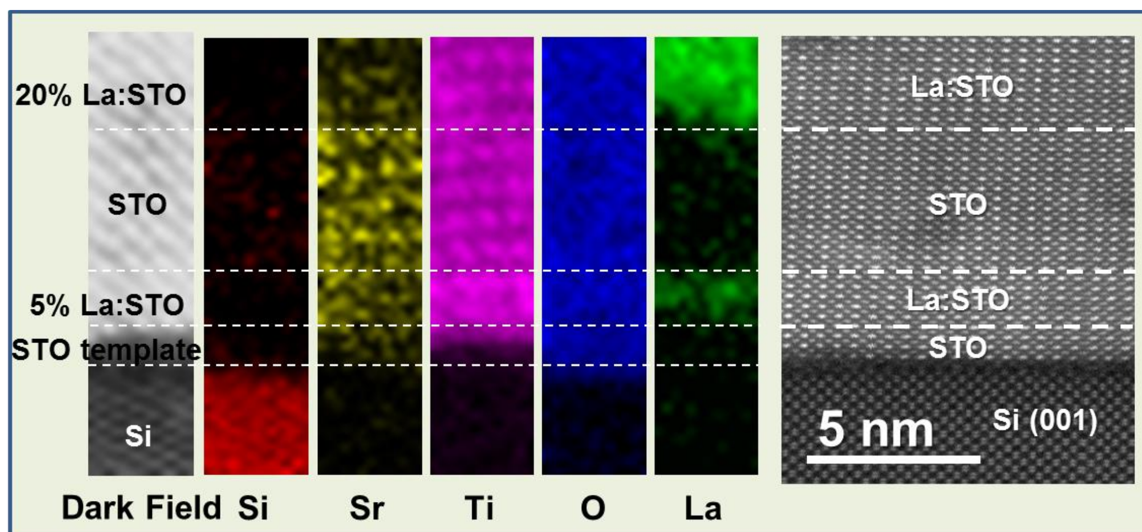


Figure 6.9. (left) EELS composition mapping highlighting the control of La distribution in select layers, and (right) high-resolution cross-sectional scanning TEM image showing the sharp interface between Si-STO as well as STO and the La:STO layers. After each ALD-grown layer, the sample was post-deposition annealed at 550 °C for 5 min in vacuum.

6.4. SUMMARY

We have demonstrated the growth of epitaxial strontium titanate thin films incorporated with up to 20% lanthanum on Si substrates. The $La_xSr_{1-x}TiO_3$ films were grown by ALD on Si (001) buffered with four-unit-cells of STO grown by MBE. The La:STO films crystallized in the cubic perovskite structure upon post-deposition annealing at 550-650 °C. Lower annealing temperatures (~550 °C) crystallize the La:STO film with epitaxial registry to the Si substrate, while maintaining an abrupt STO-Si interface. However, complete electrical activation of the La atoms requires higher temperature annealing. This creates an undesirable trade-off between La activation and the quality of the STO-Si interface. The ALD growth method can selectively incorporate La into the STO lattice at the nanometer scale. This work demonstrates potential for the combined MBE-ALD growth method for integrating epitaxial oxides for use as a FeFET gate stack.

6.5. REFERENCES

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Chapter 7: A Chemical Route to Monolithic Integration of Crystalline Oxides on Semiconductors

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7.1. INTRODUCTION

The monolithic integration of crystalline oxides on silicon was first reported by McKee and co-workers in 1998.[1] Since that initial work, several research groups have been extensively involved in studying the growth of crystalline oxides integrated on semiconductors.[2–10] Recently, epitaxial oxide heterostructures have been studied to explore interface phenomena, such as superconductivity, magneto-electric coupling, and quantum Hall effect.[11-17] A wide-array of properties, in combination with monolithic integration on semiconductors, make crystalline oxides attractive candidates for next-generation electronic devices. Molecular beam epitaxy (MBE) has been the dominant method for growth on silicon due to the layer-by-layer growth mode and precise oxygen control, which prevents formation of an amorphous interfacial layer (*e.g.*, SiO_2) under appropriate conditions.[6-8] However, for industrial applications, atomic layer deposition (ALD) has advantages over MBE primarily due to its conformal coverage, low thermal budget, scalability, and cost.[18,19]

Over the last several decades, silicon has been the workhorse for the semiconductor industry, because of its high-quality oxide SiO_2. More recently, device scaling to smaller feature sizes in complementary metal-oxide-semiconductor (CMOS) technology has led to the development of high-*k* dielectrics to replace the traditional SiO_2

[V] M. D. McDaniel, T. Q. Ngo, A. Posadas, C. Hu, S. Lu, D. J. Smith, E. T. Yu, A. A. Demkov, and J. G. Ekerdt, "A chemical route to monolithic integration of crystalline oxides on semiconductors," Adv. Mater. Interfaces **1**, 1400081 (2014). MDM designed and performed experiments. MDM, TQN, AP, AAD, and JGE contributed to the conception and analysis of data. CH and ETY performed electrical measurements. SL and DJS acquired transmission electron microscopy data.

gate oxide due to unacceptably high leakage current in ultrathin (< 1 nm) SiO_2.[20,21] High-k dielectrics (*e.g.*, HfO_2) allow for thicker gate oxides to be used by a factor of $k/3.9$, and can therefore be used to reduce the leakage current. When using alternative high-k dielectric layers, the presence of any SiO_2 at the oxide-semiconductor interface lowers the effective gate capacitance, reducing the benefits of the high-k material.

Germanium exhibits higher hole and electron mobilities than silicon,[22] potentially enabling device operation at higher speed. The 2012 international technology roadmap for semiconductors (ITRS) expects the introduction of high-mobility channels by 2018.[23] When high-k dielectrics are desired, the chemical instability of GeO_2 versus SiO_2 may actually be an advantage. Integration of high-k dielectrics on germanium has been studied by several groups,[24-29] but the electrical performance of Ge-based devices has been less than optimal. Several methods have been employed to control the interface state density (D_{it}) in order to achieve high performance.[27-29] Typical values reported for high-k/Ge gate stacks show $D_{it} \sim 10^{11}$-10^{12} cm^{-2} eV^{-1}. For practical realization of high-mobility channels in CMOS technology, surface passivation of the semiconductor substrate and a high-quality oxide-semiconductor interface must be realized. Previous work has shown that crystalline oxides on semiconductors have the potential to create a nearly perfect electrical interface by drastically reducing the interface trap density ($D_{it} < 10^{10}$ cm^{-2} eV^{-1}).[30]

To date, the majority of research on crystalline oxides integrated with semiconductors has been based on strontium titanate, $SrTiO_3$ (STO), epitaxially grown on Si (001) by MBE. Furthermore, many of the functional crystalline oxides and heterostructures integrated with Si have utilized an STO buffer layer.[31-38] Despite the promise of crystalline oxides on semiconductors, the lack of alternative growth methods has limited their study. Previous attempts to grow crystalline oxides directly on Si by

chemical routes, including ALD, have been unsuccessful. In earlier work, we demonstrated a combined MBE-ALD growth technique, where a four-unit-cell STO buffer layer grown by MBE was required to provide a stable template for the growth of crystalline oxides by ALD on Si (001), including anatase TiO_2, $SrTiO_3$, $BaTiO_3$, and $LaAlO_3$.[39-42] Despite this success, a purely chemical route to integrating crystalline oxides on semiconductors is still lacking.

In this current work, we demonstrate the ability to grow a crystalline oxide, STO, directly on Ge (001) by ALD. After removing the native oxide of Ge under ultra-high vacuum conditions, the substrate is transferred *in vacuo* to the ALD chamber. Post-deposition annealing at 650°C is required after the deposition, resulting in a crystalline STO film in epitaxial registry with the underlying Ge (001) substrate. Detailed structural and initial electrical characterization of epitaxial STO and Al-doped STO on Ge (001) is described.

7.2. Experimental Details

The as-received Ge wafer (provided by MTI Corp.) is diced into approximately 18×20 mm^2 sample sizes. Before loading into the UHV system, the sample is degreased by placing the wafer in ultrasonic baths of acetone, isopropyl alcohol, and water for 10 min each. The sample is then dried with nitrogen and exposed to ultraviolet/ozone for 15 min to remove residual carbon contamination. The sample is immediately loaded into the load lock chamber and pumped by a turbomolecular pump to a vacuum below 5×10^{-7} torr before transferring into the annealing chamber. The sample is annealed at 700 °C in vacuum for 1 hr, and then lowered to 200 °C before transfer to the ALD system. The heating and cooling rates were fixed at 20 °C min^{-1}.

The ALD system consists of a custom-built, hot-wall stainless steel rectangular chamber that is approximately 20-cm long, with a reactor volume of 460 cm^3, as described in more detail elsewhere.[60] After loading the substrate into the ALD chamber, the reactor temperature is allowed to equilibrate for at least 30 min. Ultra-high purity argon is used as both the carrier and purge gas. Under deposition conditions, the argon is flowed into the ALD chamber, which is continuously pumped by a dual-stage rotary vane pump with a peak pumping speed of 6 ft^3 min^{-1}. This maintains the ALD operating pressure at ~ 1 torr. HyperSr and TTIP were vaporized at 130 °C and 40 °C, respectively, and water was held at room temperature (26 °C). The water dosing was regulated using an in-line needle valve.

XPS was performed using a VG Scienta R3000 analyzer and a monochromated Al Kα source at 1486.6 eV. The analyzer is calibrated using a silver foil, where the Ag 3$d_{5/2}$ core level is defined to be 368.28 eV and the Fermi level of Ag at 0.00 eV. High-resolution spectra of the Sr 3*d*, Ti 2*p*, O 1*s*, C 1*s*, and Ge 3*d* core levels are measured using a pass energy of 100 eV with an analyzer slit width of 0.4 mm. Each high-resolution scan is measured four times and summed, using 50 meV steps with a dwell time of 157 ms per step. Film composition was estimated using CasaXPS (ver. 2.3.16) peak fitting, where the integrated intensities are divided by the Wagner relative sensitivity factors after a Shirley background subtraction.[61] Additionally, a thickness dependent energy exponent between 0 and 0.78 is used to account for kinetic energy variation with sampling depth.[62] The maximum exponent value (0.78) was calibrated using an STO single crystal substrate (MTI Corp.) where the Sr:Ti ratio was assumed to be 1:1.

RHEED patterns were obtained with an electron energy of 21 keV at a glancing angle of ~3°. X-ray diffraction (XRD), x-ray reflectivity (XRR), rocking curve analysis,

and off-axis phi scans were all conducted using a Bruker-AXS D8 Advance Powder Diffractometer using a sealed tube Cu Kα radiation. Cross-sectional transmission electron microscopy (TEM) was performed with a 400-keV high-resolution electron microscope (JEM-4000EX) equipped with a double-tilt specimen holder. The sample was prepared using standard mechanical polishing followed by argon-ion-milling to perforation.

Capacitance-voltage (CV) and current-voltage (IV) measurements were performed on several undoped and Al-doped STO films grown by ALD on heavily doped n-type Ge (ρ ~ 0.04 Ω-cm). The STO films were annealed in air at 300 °C for 30 min prior to electrode deposition. The top electrode (50 μm radius) on the STO surface was formed by photolithography, e-beam evaporation of 20-nm Ti followed by 160-nm Au, and lift-off. The Ge substrate was coated with Ti/Au as a bottom electrode. Both CV and IV were measured in air at room temperature by an Agilent 4156A precision semiconductor parameter analyzer. The sweeping voltage was applied to the top electrode with the bottom electrode grounded.

7.3. RESULTS AND DISCUSSION

7.3.1. Growth of Crystalline $SrTiO_3$ on Ge (001)

Preparation of the Ge (001) surface

Before deposition of the STO film, a nearly oxygen-free Ge (001) surface is prepared in an ultra-high vacuum (UHV) system with a base pressure below 3×10^{-9} torr. After solvent degreasing, the sample is dried and exposed to an ultraviolet/ozone unit to remove residual carbon contamination. The sample is moved directly into the UHV annealing chamber, equipped with a silicon carbide heater and reflection high-energy

electron diffraction (RHEED). Thermal deoxidation of the Ge wafer is achieved by annealing the sample at a temperature 700 °C for 1 hr. A representative x-ray photoelectron spectrum of the Ge 3*d* feature illustrates the possible presence of Ge_2O, accounting for 0.8% of the total Ge signal after annealing and transferring the sample into the analytical chamber. When the sample is cooled below 200 °C, the 2×1 reconstructed Ge (001) surface is observed by RHEED (not shown). The 2×1 reconstruction was also observed along the perpendicular surface direction by rotating the sample 90° under electron illumination. The intensity of the ½-order spots in the 2×1 surface reconstruction is a strong indicator of the quality of the cleaned Ge surface. In our previous work, thermal deoxidation of the Ge surface was acheived by using *in situ* oxygen plasma treatment followed by annealing at 650 °C or higher for 30 min, where the root-mean-square roughness over a 5×5 μm^2 area decreased from 0.9 ± 0.2 nm when using a similar protocol to that employed for the study herein to 0.3 ± 0.1 nm, respectively.[43] However, in this work, only the thermal deoxidation described above is used to prepare the Ge surface for ALD growth. We found that provided a reasonable 2×1 reconstruction was observed, crystalline STO film growth could be achieved.

Atomic Layer Deposition of Crystalline $SrTiO_3$

After preparing the 2× reconstructed Ge (001) surface, the sample is transferred *in vacuo* from the annealing chamber to the ALD system. Thin film growth of STO on the thermally deoxidized Ge (001) substrate is achieved by ALD at a substrate temperature of 225°C using strontium bis(triisopropylcyclopentadienyl) [$Sr(^iPr_3Cp)_2$] (HyperSr),[44] titanium tetraisopropoxide [$Ti(O\text{-}^iPr)_4$] (TTIP),[45] and purified water as co-reactants. Both the Sr and Ti metalorganic precursors were chosen for this study due to their commercial availability and common use in ALD.[46-55]

As with the deposition of any ternary oxide by ALD, the "supercycle" consists of a combination of subcycles for the binary oxides. Each subcycle of Sr and Ti consists of a 2-sec dose of the metalorganic precursor, a 15-sec purge with Ar, a 1-sec pulse of H_2O, and a final 15-sec purge with Ar. From our previous experience of growing STO on STO-buffered Si (001), Sr:Ti cycle ratios of 1:1 to 4:3 were needed to achieve nearly stoichiometric films.[40] However, the initial STO growth on Ge behaves differently. The STO nucleation on Ge uses a Sr-heavy supercycle (a ratio of 2 Sr subcycles to 1 Ti subcycle) to achieve stoichiometric to slightly Sr-rich STO films, which is critical to achieving an epitaxial crystalline film. Under these conditions, a thin amorphous STO film (~2 nm) is first deposited with 12 supercycles, equivalent to 36 subcycles.

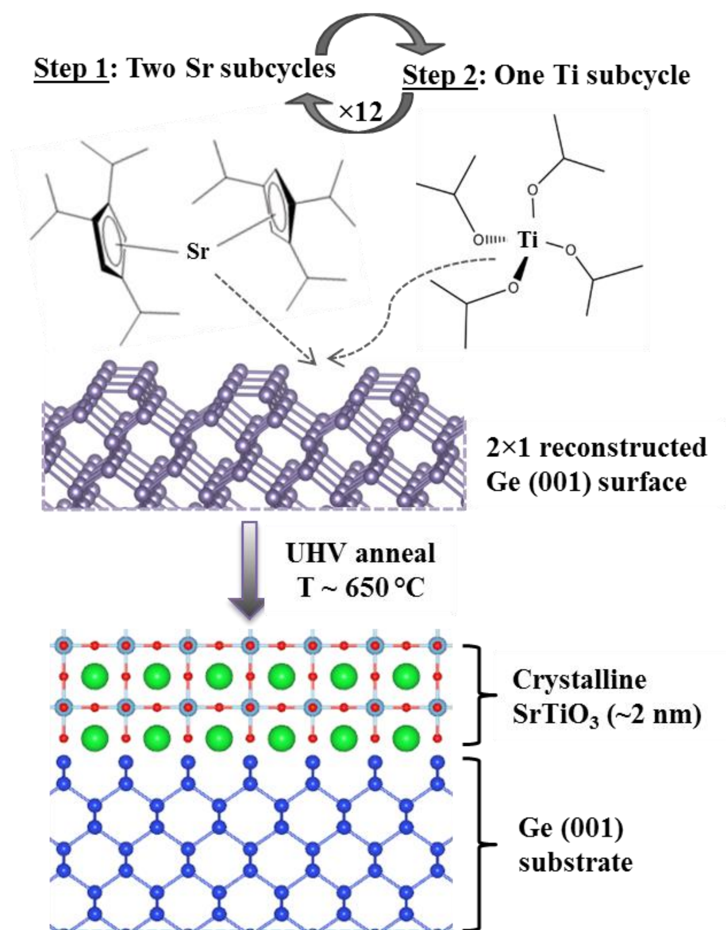

Figure 7.1. Schematic of the nucleation process for STO on Ge (001) by ALD. The deposition subcycle includes the H_2O exposure and argon purge steps.

The thin STO film on Ge is then transferred *in vacuo* back to the annealing chamber. The film is heated to a substrate temperature of 650°C at a rate of 20 °C min^{-1} for crystallization. The process flow for growth and crystallization of the STO layer on Ge (001) is shown schematically in Figure 7.1. The atomic model of the STO-Ge interface illustrated in Figure 1 is only an elementary schematic, as the exact interface structure and bonding across the interface is not known at this time. Upon post-deposition annealing, the transition of the film from amorphous to crystalline is directly observed by the RHEED imaging system, as shown in Figure 7.2. After annealing, the

sample is cooled to below 200 °C. Further growth on the crystalline STO-Ge heterostructure is then possible.

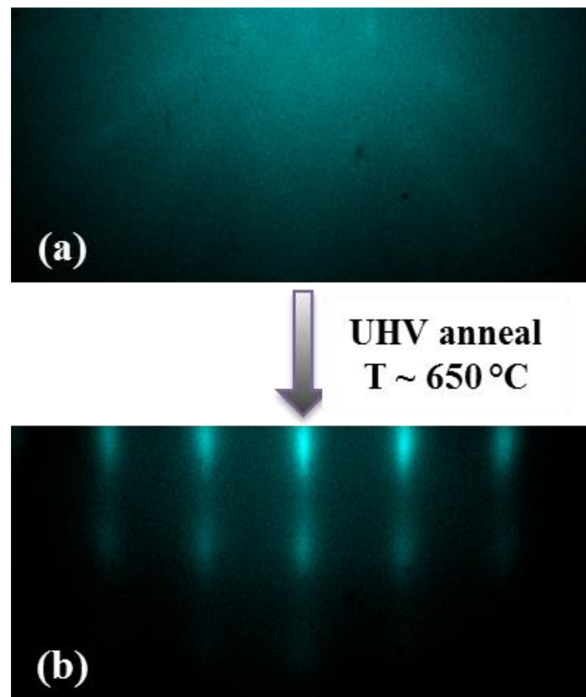

Figure 7.2. RHEED images (a) after ~2 nm STO film growth by ALD (36 subcycles) and (b) after vacuum annealing at 650 °C, where the beam is aligned along the [110] azimuth.

The detailed mechanism of the initial nucleation of STO on the Ge (001) surface is not yet completely understood. The clean Ge (001) surface that is transferred into the ALD system is without surface hydroxyl groups, which are the presumed reaction sites for these ALD precursors. Interestingly, initial growth analysis of the two binary oxides, SrO and TiO_2, suggests that the Sr precursor (HyperSr) reacts with the Ge (001) surface to initiate film nucleation. Using only the Ti precursor (TTIP), no film deposition was observed even after 100 ALD subcycles. Considering the structure of the cyclopentadienyl-based precursor compared with the alkoxide, the nucleation process

may result more from direct chemical bonding between the electropositive Sr and the empty dangling bond states on the Ge (001) surface. A more detailed study of the cyclopentadienyl-based precursor interaction with the Ge surface is beyond the scope of this current work.

Thicker Oxide Film Growth

For thicker STO films, the crystallized STO on Ge was transferred back into the ALD chamber, following the same general procedure outlined above. However, continued STO growth did not require Sr-heavy cycling. A supercycle consistent with four Sr to three Ti subcycles (Sr:Ti cycle ~ 4:3) at 225 °C yielded nearly stoichiometric film growth, consistent with our previous study.[40] Following the second growth step, the as-deposited STO films are amorphous to weakly crystalline. After completion of ALD growth, the STO films were annealed at 650 °C for 5 min to crystallize the deposited film fully on the STO seed layer.

Stoichiometric, crystalline STO films of up to 15-nm thick were produced using this two-step growth process. Thicker films may require more growth and anneal steps, or higher temperature growth to promote *in situ* crystallization. However, this method produces crystalline STO films in the appropriate thickness range (< 10 nm) for potential electronic applications, including high-mobility Ge-based transistors. Our expectation is that other crystalline oxides previously grown by ALD on single-crystal STO or STO-buffered Si (001) substrates can be monolithically integrated with Ge (001) by this growth technique.

7.3.2. Chemical and Structural Characterization

In situ X-ray Photoelectron Spectroscopy

The STO film and Ge-STO interface were analyzed using *in situ* x-ray photoelectron spectroscopy (XPS). After crystallization, the sample was transferred into the XPS analysis chamber. One of the keys to successful crystallization of the initial STO layer on Ge is ensuring that the film is stoichiometric to slightly Sr-rich. In addition, the presence of any amorphous layer (*e.g.*, GeO_2) prevents crystalline STO formation. Using *in situ* XPS, an optimized cycling ratio of two Sr cycles to one Ti cycle was found to produce stoichiometric to slightly Sr-rich (~54%) films.

XPS analysis also verified that minimal, if any, GeO_x formation is caused by the deposition of STO by ALD or the post-deposition annealing process. The presence of GeO_x is generally identified by the chemical shifts ($\Delta\varepsilon$) of the Ge^{1+} ($\Delta\varepsilon = 0.70 \pm 0.05$ eV), Ge^{2+} ($\Delta\varepsilon = 1.70 \pm 0.10$ eV), Ge^{3+} ($\Delta\varepsilon = 2.81 \pm 0.06$ eV), and Ge^{4+} ($\Delta\varepsilon = 3.5 \pm 0.1$ eV) oxidation state components.[56] Deconvolution of the Ge 3*d* high-resolution spectrum was performed using CasaXPS as described in the Experimental Details to identify contributions of different Ge species after STO deposition and annealing, as shown in Figure 7.3. The spectrum is found to have contributions from bulk Ge ($3d_{5/2}$ and $3d_{3/2}$ at 29.62 and 30.12 eV, respectively), an interfacial Ge species at lower binding energy ($3d_{5/2}$ and $3d_{3/2}$ at 29.08 and 29.67 eV, respectively), and Ge_2O (Ge^{+1}) with $3d_{5/2}$ and $3d_{3/2}$ components at 30.28 and 30.91 eV, respectively. The exact bonding of the interfacial Ge species is not fully known, but appears similar to the shift that is observed for the Ge (001) surface dimerization.[57] It can be reasonably concluded that the interface is free of any further suboxides, namely, GeO (Ge^{2+}), Ge_2O_3 (Ge^{3+}), or GeO_2 (Ge^{4+}) species. As a comparison, deconvolution of the Ge 3*d* high-resolution spectrum for the clean Ge (001) surface is compared. The Ge_2O (Ge^{+1}) component is estimated at 1.3% of the total Ge

signal (Figure 7.3), which is comparable to the 0.8% contribution Ge_2O makes to cleaned Ge. Since the samples must be transferred from the annealing chamber into either the analytical or the ALD chambers it is not possible to establish if any, or additional, Ge_2O forms during ALD and subsequent annealing of the STO layer.

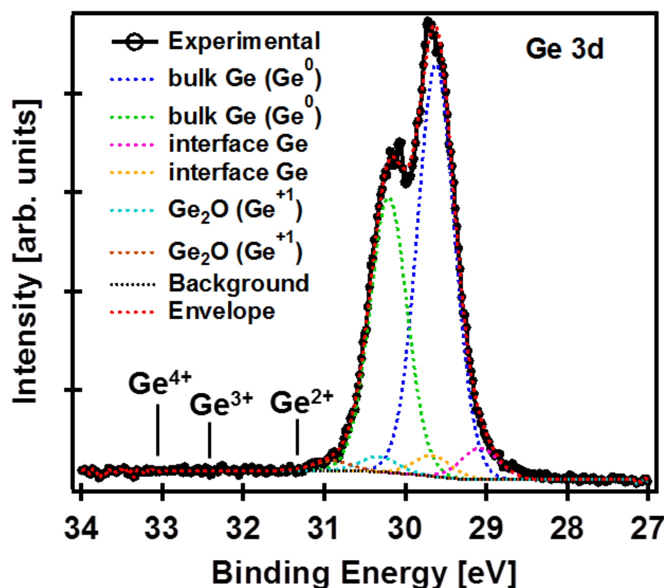

Figure 7.3. Spectral fitting of the high-resolution Ge 3*d* core-level spectrum after deposition of ~2 nm STO and post-deposition annealing at 650 °C. The approximate positions of the Ge^{2+}, Ge^{3+}, and Ge^{4+} oxidation state components are indicated.

Figure 7.4 shows XP spectra of an 8-nm thick STO sample grown on germanium. The XPS scans were taken before ALD growth, after 36 subcycles (~2 nm), and after 155 subcycles (~8 nm). The STO layer was crystallized each time by post-deposition vacuum annealing at 650 °C for 5 min. After cooling, the sample was moved to the XPS analysis chamber. Core levels of Ge 3*d* and O 1*s* are shown in Figure 7.4(a) and 7.4(b), respectively. The Ge 3*d* signal intensity decreases with the number of ALD cycles (thickness of STO film) and consistent with Figure 7.4, no GeO_x ($x \geq 1$) formation is

observed. The Sr 3*d* and Ti 2*p* core levels shown in Figure 7.4(c) and 7.4(d) are consistent with fully oxidized species (Sr^{2+} and Ti^{4+}).

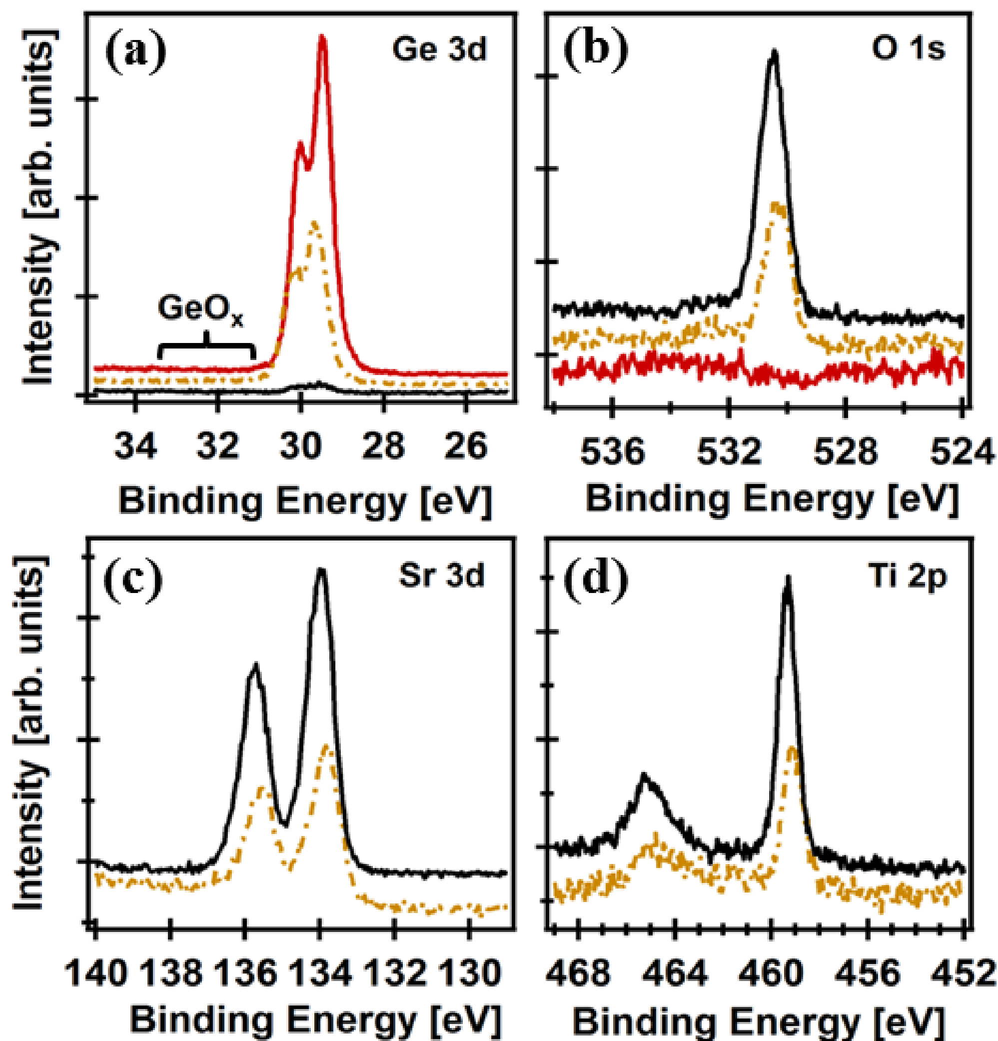

Figure 7.4. X-ray photoelectron spectra of the (a) Ge 3*d*, (b) O 1*s*, (c) Sr 3*d*, and (d) Ti 2*p* before ALD growth (solid red line), after 36 subcycles (~2 nm STO) (dashed brown line), and after 155 subcycles (~8 nm STO) (solid black line). The deposition temperature was 225 °C with a Sr:Ti subcycle ratio of 2:1 for the crystalline seed layer and 4:3 for the thicker STO film.

X-ray and Electron Diffraction

X-ray and electron diffraction techniques were used to confirm the crystalline structure, epitaxial relation, and thickness of the STO films. Evolution of the RHEED patterns from the Ge substrate to an 8-nm thick crystalline STO film is shown in Figure 7.5. The 2×1 surface reconstruction of the clean Ge surface after thermal deoxidation is shown in Figure 7.5(a). The intensity of the ½-order spots are a strong indicator of the quality of the Ge (001) surface. After thermal deoxidation at 700 °C for 1 hr, a high-quality Ge (001) surface is achieved, provided that there is minimal residual carbon in the annealing chamber. The sample can then be transferred *in vacuo* to the ALD chamber. Deposition of the STO film occurs at a relatively low substrate temperature (225 °C), which results in the as-deposited film being amorphous to weakly crystalline. An example RHEED pattern of an 8-nm thick film, prior to crystallization, is shown in Figure 7.5(b).

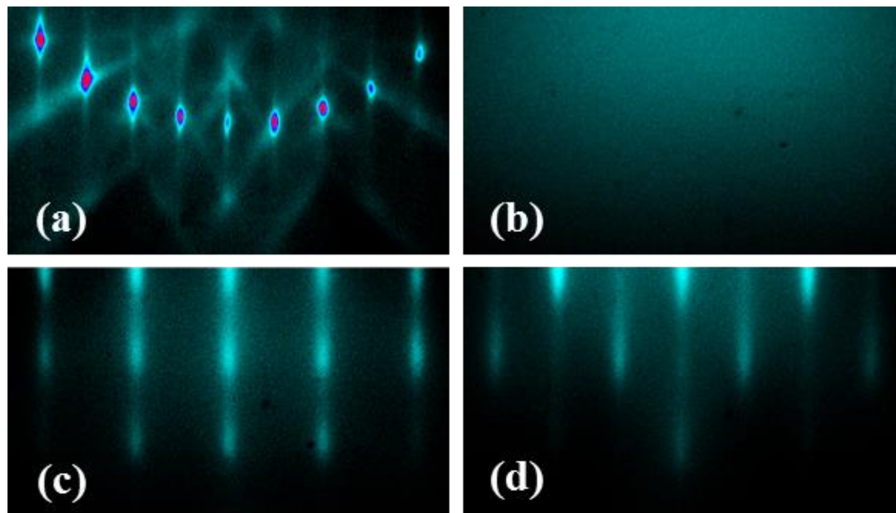

Figure 7.5. RHEED images of (a) clean Ge surface (before ALD growth), (b) after the second STO deposition (155 total subcycles), and [(c), (d)] after growth and annealing at 650 °C of an 8-nm thick STO film. The beam is aligned along the [110] and [100] azimuth for (c) and (d), respectively.

Provided that the film is stoichiometric to slightly Sr-rich, post-deposition annealing at 650 °C for 5 min results in a crystalline film with epitaxial registry to the underlying Ge (001) substrate. The RHEED patterns for an 8-nm thick STO film grown on Ge (001) are shown in Figure 7.5(c) and 7.5(d). The images are taken along the [110] and [100] azimuth of STO, respectively. The streak patterns are comparable to that of STO films grown by molecular beam epitaxy, confirming the high degree of crystallinity for the ALD-grown film.

The structure of the STO film was confirmed by XRD to be consistent with the cubic perovskite, as shown in Figure 7.6. A rocking curve around the STO (002) peak gave a full-width half-maximum of ~0.8° (Figure 7.6 inset), indicating a reasonable degree of out-of-plane orientation. The STO and Ge (001) substrate are epitaxially aligned such that $(001)_{STO} \| (001)_{Ge}$ and $(100)_{STO} \| (110)_{Ge}$, leading to a 45° in-plane rotation that is expected for lattice-matching between the STO and Ge (001) substrate. From the bulk lattice constant for STO (a = 3.905 Å) and the Ge (001) surface spacing along the [110] direction (3.992 Å), the STO film is 2.1% tensile-strained when grown on Ge (001). Assuming STO is perfectly strained to Ge with a Poisson ratio of 0.232,[58] the STO (002) peak should be at 46.73°. Experimentally, XRD of an 8-nm thick STO film gave a peak position of 46.75 ± 0.05°. However, thicker films relaxed to the nominal powder value (2θ ~ 46.47°). Films greater than about 15 nm appear fully relaxed, with the STO (002) peak position at 46.45 ± 0.05°.

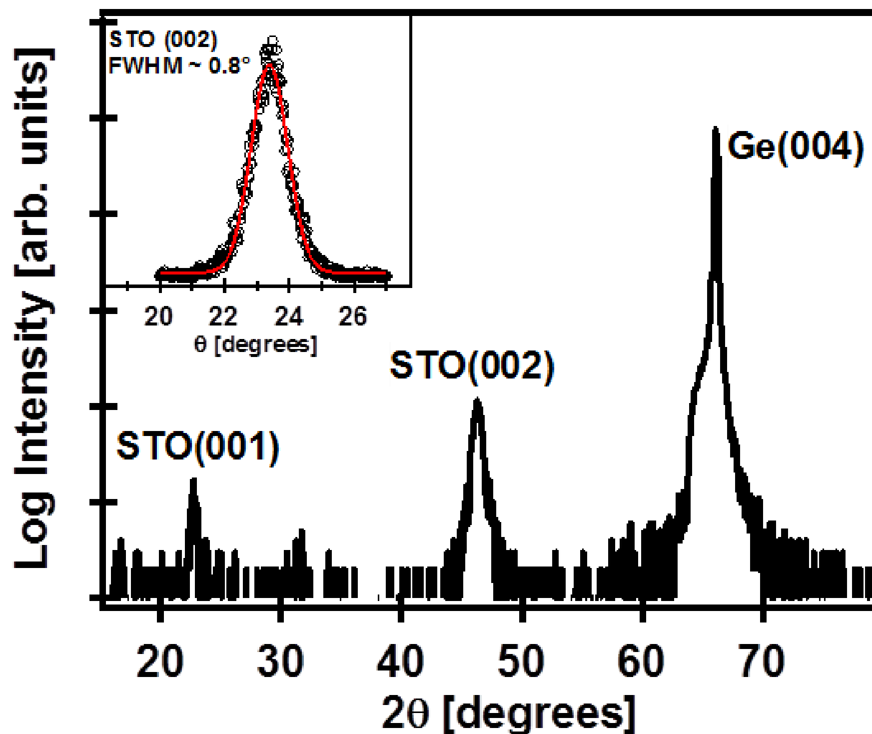

Figure 7.6. X-ray diffraction pattern for a 15-nm thick STO film grown by ALD on Ge (001) at 225 °C. (top left inset) Rocking curve around the STO (002) peak showing a FWHM of ~0.8°. The sample was post-deposition annealed in vacuum at 600 °C for 5 min.

High-resolution electron microscopy was used to examine cross-sections of the ALD-grown STO films. The cross-sectional TEM image (Figure 7.7) confirms the exceptional crystallinity of the STO film. There is an abrupt STO/Ge interface with no indication of an amorphous transition layer, in agreement with the XPS results. The selected-area electron diffraction pattern (Figure 7.7 inset) also confirms the excellent epitaxial registry between the two materials.

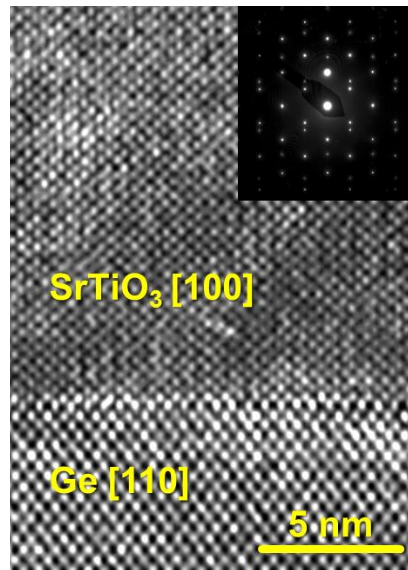

Figure 7.7. High-resolution transmission electron micrograph showing cross-section of a 15-nm thick STO film grown on Ge (001) by ALD. (top right inset) Selected-area electron diffraction pattern showing epitaxial registry between the substrate and film.

7.3.3. Electrical Characterization of $SrTiO_3$ and Al-doped $SrTiO_3$ films

Dielectric Performance of Crystalline $SrTiO_3$ on Ge (001)

Electrical characterization of a 15-nm thick STO film was carried out by creating capacitor (metal-insulator-semiconductor) structures, as shown in Figure 7.8. Capacitance-voltage (CV) and current-voltage (IV) measurements were performed on a 50-µm radius top electrode. Both CV and IV curves are shown in Figure 7.9, where the capacitance and current are normalized by the area of the contact pad. From the CV measurement shown in Figure 7.9(a), the capacitance of the structure is estimated to be 5.3 $\mu F/cm^2$. This corresponds to a relatively high dielectric constant ($k \sim 90$) for the STO thin film, with an equivalent oxide thickness less than 0.7 nm.

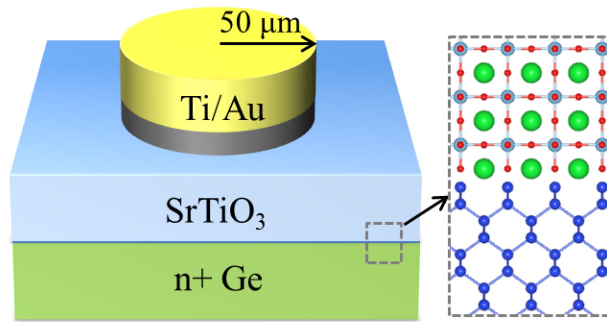

Figure 7.8. Schematic of the metal-insulator-semiconductor capacitor structure for crystalline STO grown on Ge (001) by ALD.

As shown in Figure 7.9(b), the leakage current density is relatively high ~10 A/cm^2 at +1 V (0.7 MV/cm) bias. The high leakage current is attributed to the small conduction band offset between STO and Ge, which we found experimetally to be 0.12 ± 0.1 eV based on XPS measurements of shallow core-level and valence band spectra. The relatively small conduction band offset (~0.12 eV) of the STO/Ge heterojunction makes undoped STO unsuitable as a high-*k* dielectric for Ge-based transistors.

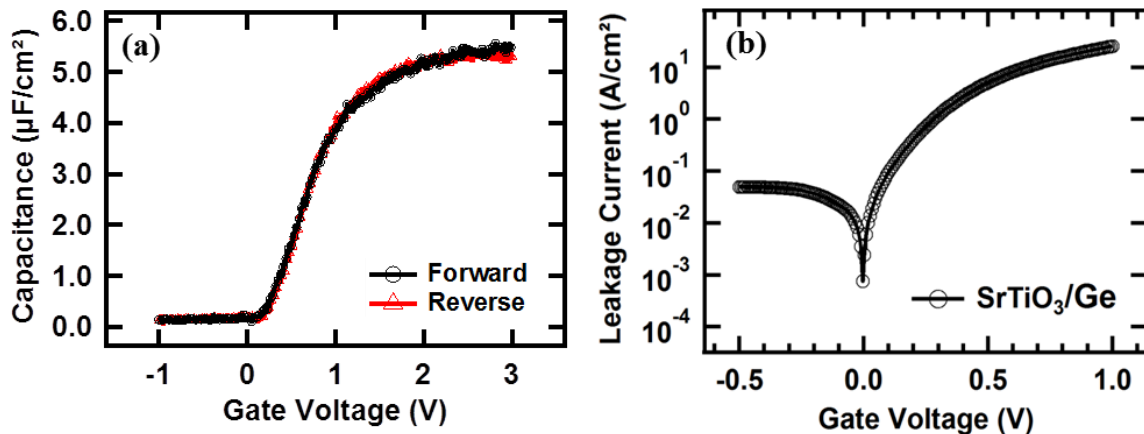

Figure 7.9. (a) Specific capacitance as a function of voltage bias for a 15-nm thick STO film grown on n+ Ge (001) by ALD, and (b) the leakage current density as a function of voltage bias measured from a typical Au(Ti)/STO/Ge structure.

Improved leakage current of Al-doped $SrTiO_3$ films

Different methods to reduce the leakage current of STO, such as inclusion of extra SrO layers and Al-doping of STO films, have been demonstrated previously.[30,59] By modifying our ALD cycle conditions to include an aluminum precursor, Al-doped STO films ($SrTi_{1-x}Al_xO_{3-\delta}$) were grown on the crystalline STO seed layer. The growth of the Al-doped STO films was similar to the growth of undoped STO, where some of the Ti subcycles were replaced with Al subcycles. Trimethyl aluminum (TMA) was used as the aluminum source. Several Al-doped STO films were grown with Al content varying between 8-13%. The films exhibited crystalline structure and quality similar to the undoped STO films using RHEED and XRD (not shown). The thicknesses of the Al-doped films were ~8 nm, which includes the STO seed layer.

Electrical characterization of the Al-doped STO capacitor structures was carried out using a 50-μm radius top electrode. The leakage current density as a function of gate voltage is shown in Figure 7.10. Al-doped STO films of 8% and 13% show a leakage current density of ~0.5 A/cm^2 and ~0.1 A/cm^2, respectively, for an applied field of 0.7 MV/cm. When compared to a 15-nm thick STO film, the leakage current density of an 8-nm thick Al-doped STO film with sufficient Al doping (~13%) was two orders of magnitude lower. Considering the difference in thickness of the undoped and Al-doped films, the leakage current reduction is significant. The decrease in leakage current is expected as a result of the band gap increase of ~0.3 eV due to Al doping.[59] Similar band gap engineering concepts may be employed to further reduce the leakage current of high-*k* crystalline oxides grown by ALD on Ge.

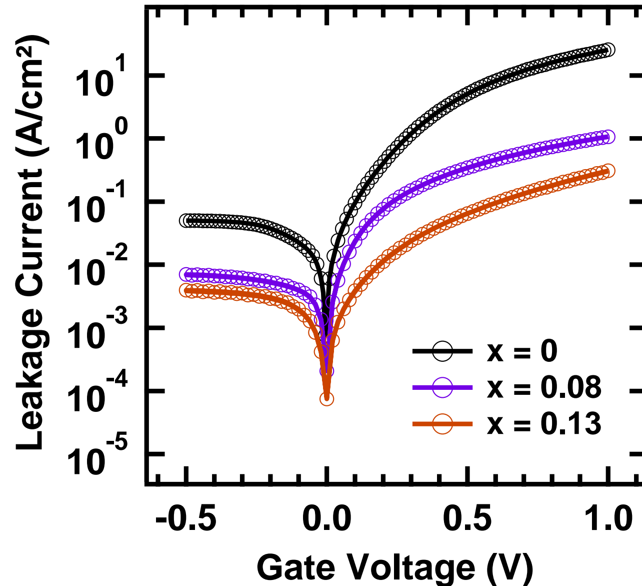

Figure 7.10. Gate leakage density as a function of voltage bias measured for Al-doped STO capacitor structures, Au(Ti)/$SrTi_{1-x}Al_xO_{3-\delta}$ /Ge. The leakage current decreases with increasing aluminum content.

7.4. SUMMARY

We have grown crystalline $SrTiO_3$ (STO) directly on germanium via a purely chemical method, atomic layer deposition (ALD). *In situ* x-ray photoelectron spectroscopy confirms the presence of stoichiometric STO with no GeO_x ($x \geq 1$) formation or carbon impurities observed. Epitaxial STO films up to 15-nm thick with a high-degree of crystallinity were grown on the Ge (001) substrate. The crystalline structure and orientation are confirmed via electron and x-ray diffraction. Capacitance-voltage and current-voltage measurements were performed on a 15-nm thick undoped STO film. The undoped STO showed a large dielectric constant of ~90; however, the leakage current was unacceptably high (~10 A/cm^2 at 0.7 MV/cm). To lower the leakage current, the STO films were doped with aluminum. An 8-nm thick Al-doped STO film

showed a leakage current density ~0.1 A/cm^2 at 0.7 MV/cm, roughly two orders of magnitude lower than the undoped STO.

Considering the wide-array of properties and lattice matching for perovskite oxides, this chemical growth technique has wide reaching potential for the monolithic integration of many functional oxides and heterostructures with semiconductor devices. The current work demonstrates the promise for ALD-grown crystalline oxides for advanced electronic applications in the near future, especially for high-mobility Ge-based transistors.

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Chapter 8: Atomic layer deposition of crystalline $SrHfO_3$ directly on Ge (001) for high-*k* dielectric applications

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8.1. INTRODUCTION

In the last decade, significant material changes to complementary metal oxide semiconductor (CMOS) devices have included the introduction of strained Si channels to improve performance and efficiency and metal gate/high-*k* dielectric stacks to address leakage current issues.[1-3] More recently, there has been renewed interest in using Ge as a channel material due to its higher hole (1900 vs. 500 cm^2/V-s) and electron (3900 vs. 1400 cm^2/V-s) mobility compared to Si.[4-7] Crystalline oxides are also being considered by the semiconductor industry as next-generation high-*k* dielectrics.[8] For example, there is tremendous interest in epitaxial integration of perovskite oxides, such as $SrTiO_3$ (STO) or $BaTiO_3$ (BTO), on semiconductors due to their functional properties and very high permittivities.[9-12] One primary advantage of crystalline, epitaxial dielectrics is the possibility of having virtually no defects in the bulk of the dielectric or at the interface with the semiconductor in an ideal heteroepitaxial system. For practical realization of high-mobility channels in CMOS technology, surface passivation of the semiconductor substrate and a high-quality oxide-semiconductor interface must be realized.

Integration of high-*k* dielectrics on germanium has been studied by many groups,[13-19] but the electrical performance of Ge-based devices has been less than optimal. Several methods have been employed to control the interface trap density (D_{it})

[VI] M. D. McDaniel, C. Hu, S. Lu, T. Q. Ngo, A. Posadas, A. Jiang, D. J. Smith, E. T. Yu, A. A. Demkov, and J. G. Ekerdt, "Atomic layer deposition of crystalline $SrHfO_3$ directly on Ge (001) for high-k dielectric applications," J. Appl. Phys. **117**, 054101-(1-9) (2015). MDM designed and performed experiments. MDM, CH, TQN, AP, ETY, AAD, and JGE contributed to the conception and analysis of data. CH, AJ, and ETY performed electrical measurements. SL and DJS acquired transmission electron microscopy data.

in order to achieve high performance.[15,16,18] Typical values reported for high-k/Ge gate stacks show D_{it} ~ 10^{11}-10^{12} cm^{-2} eV^{-1}. However, crystalline oxides have the potential to create a nearly perfect electrical interface by drastically reducing the interface trap density ($D_{it} < 10^{10}$ cm^{-2} eV^{-1}).[19,20] For a material to be suitable as a gate dielectric replacement, it needs to satisfy several requirements, including high permittivity, sufficiently large band gap and proper band alignment (with 1 eV offset to both bands) to the semiconductor, thermodynamic stability, good film morphology, and high interface quality. Materials related to TiO_2, including STO and BTO, have high permittivities, but the conduction band offsets with Si and Ge are very small to negligible.[21-23] Alternatively, crystalline strontium hafnate, $SrHfO_3$ (SHO), meets many of the high-k requirements and has a reasonable lattice match to Ge (~1.9% mismatch), making it an ideal material candidate for Ge-based transistors.

There are relatively few reports on thin film deposition of SHO to date.[24-32] In some early work, crystalline SHO was investigated as a future gate dielectric material for Si-based devices.[25,27] The SHO films were grown by molecular beam epitaxy (MBE) on Si (001) despite the 6% lattice mismatch. The electrical performance of epitaxial SHO on Si showed low equivalent oxide thickness (EOT) of 0.7 nm and low leakage current (10^{-6} A/cm^2) at -1 V.[25] However, the relatively high D_{it} (~10^{13} $eV^{-1}cm^{-2}$) likely contributed to the poor mobility of the SHO/Si field-effect transistors (FETs), where both n-FETs and p-FETs exhibited carrier mobilities of ~25 cm^2/V-s at 1 MV/cm.[25] Later work showed that the SHO films on Si lacked significant strain and confirmed the in-plane misalignment of grains, which can degrade mobility.[30] The large lattice mismatch between SHO and Si, and subsequent relaxation of the film, likely contributed to the formation of these undesirable defects.

For epitaxial $SrHfO_3$ thin films, Ge is a more suitable substrate than Si in terms of the lattice match. Cubic SHO has a lattice constant of 4.069 Å.[33] The Ge (001) surface has an in-plane atomic spacing of 3.992 Å, which would lead to compressive lattice strain in commensurate, epitaxial SHO films of 1.9%. In addition to the closer lattice match, other physical properties make crystalline SHO a good candidate dielectric for Ge-based devices. Polycrystalline SHO films are reported to have a dielectric constant up to k ~35,[24,28] leading to an EOT of less than 0.6 nm with a 5 nm film using the ratio of k/3.9. However, other studies have reported lower dielectric constants (k~20) for SHO,[26,32] similar to the binary oxide HfO_2. Finally, SHO has a large band gap of 6.1 eV with favorable conduction band offset (~2.2 eV) and valence band offset (~3.2 eV) with Ge.[26,34] This is in contrast with Ti-based perovskites, where the Ti 3d states yield negligible conduction band offsets with Si and Ge (~0.1-0.5 eV).[21,22,35] A direct comparison between SHO and STO films on Si (001) has shown a reduction in gate leakage by 4 orders of magnitude for SHO versus STO.[26]

Recently, we reported the growth of single crystal STO (a = 3.905 Å) on Ge (001) by atomic layer deposition (ALD) followed by post-deposition annealing in vacuum.[23] Capacitor structures revealed a large dielectric constant (k~90) for the STO films, but a high leakage current of ~10 A/cm^2 for an applied field of 0.7 MV/cm. To circumvent this leakage issue, we explore the Hf-based perovskite, SHO, with optimal band alignments to Ge and associated reduction in leakage current. As detailed in our previous report,[23] the controlled growth by ALD on a clean Ge (001) surface enables a chemical route to epitaxial oxide integration with semiconductors. Here we confirm this growth and annealing protocol to realize crystalline SHO films, and evaluate the potential for epitaxial SHO films as a future gate dielectric for Ge-based transistors.

8.2. EXPERIMENTAL DETAILS

Strontium hafnate, $SrHfO_3$ (SHO), thin films are deposited by ALD at a substrate temperature of 225 °C using strontium bis(triisopropylcyclopentadienyl) $[Sr(^iPr_3Cp)_2]$ (HyperSr),[36] hafnium formamidinate (Hf-FAMD),[37] and purified water as co-reactants. Both the Sr and Hf metalorganic precursors are commercially available, reactive with water, and have been previously used for ALD. [38-48] Alternating subcycles of Sr and Hf are used to deposit stoichiometric to slightly Sr-rich (56%) films. During each subcycle the metalorganic is dosed for 2 sec to ensure complete saturation of the surface, and subsequently purged for 15 sec with ultrahigh purity Ar. The water co-reactant is dosed for 1 sec followed by a 15 sec Ar purge.

The Ge (001) substrate is prepared from a 4-inch Ge wafer (Sb-doped, ρ~0.04 Ω-cm) from MTI Corp. The as-received Ge wafer is diced into approximately 18×20 mm^2 sample pieces. The sample is degreased by placing the wafer in ultrasonic baths of acetone, isopropyl alcohol, and water for 10 min each. The sample is then dried with nitrogen and exposed to ultraviolet/ozone for 30 min to remove residual carbon contamination. The sample is then immediately loaded into the load lock chamber and pumped by a turbomolecular pump to a vacuum below 5×10^{-7} torr before transferring into the annealing chamber. The surface GeO_2 is removed by annealing the sample at 700 °C in vacuum (< 2×10^{-9} torr) for 1 hr. After thermal deoxidation, the Ge substrate is brought to below 200 °C before transfer into the ALD system. The heating and cooling rates are fixed at 20 °C min^{-1}. The low base pressure of the annealing chamber minimizes potential contamination of the Ge surface during thermal deoxidation. The clean Ge (001) surface then shows a sharp, intense 2×1 reconstruction that is observed by *in situ* reflection high-energy electron diffraction (RHEED).

After achieving the 2×1 reconstructed Ge surface, the sample is transferred into the ALD chamber, with a base pressure of 5×10^{-7} torr, and allowed at least 30 min to reach thermal equilibrium. Ultrahigh purity argon is used as the carrier/purge gas and maintains the deposition pressure at 1.0 torr. To deposit stoichiometric to Sr-rich (~56%) films of SHO, a subcycle ratio of 1:1 (Sr:Hf) is used. This is in contrast to STO films, where the initial deposition on Ge required a Sr-heavy subcycle ratio of 2:1 (Sr:Ti).[23] Upon deposition of the SHO film, the sample is transferred back into the annealing chamber for crystallization. Post-deposition annealing is carried in vacuum ($< 2 \times 10^{-9}$ torr) with a temperature ramp rate of 20 °C/min.

The SHO films were post-deposition annealed at a substrate temperature of 650-850 °C. The transition of the films from amorphous to crystalline is observed in real time by *in situ* RHEED. After crystallization, *in situ* x-ray photoelectron spectroscopy (XPS) is used to check the chemical composition and oxidation states, as well as to measure the valance band offset of the SHO-Ge heterostructure. XPS is performed using a VG Scienta R3000 analyzer and a monochromated Al Kα source at 1486.6 eV. The analyzer is calibrated using a silver foil, where the Ag $3d_{5/2}$ core level is defined to be 368.28 eV and the Fermi level of Ag at 0.00 eV. High-resolution spectra of Sr ($3d$, $3p$), Hf ($4f$, $4d_{5/2}$), O $1s$, C $1s$, and Ge ($3d$, $2p_{3/2}$) core levels are measured using a pass energy of 100 eV with an analyzer slit width of 0.4 mm, resulting in an effective resolution of 350 meV. Each high-resolution scan is measured four times and summed, using 50 meV steps with a dwell time of 157 ms per step. Film composition is estimated using CasaXPS (ver. 2.3.16) peak fitting with a Shirley background subtraction and relevant sensitivity factors.[49]

The epitaxial SHO films are characterized *ex situ* by x-ray reflectivity (XRR), x-ray diffraction (XRD), and cross-section transmission electron microscopy (TEM). XRR

is performed using a Rigaku Ultima IV equipped for thin-films with automated alignment. XRD is performed using an X'PERT Powder Diffractometer with a sealed tube Cu Kα radiation (λ~1.5406 Å). Cross-sectional TEM is performed with a 400-keV high-resolution electron microscope (JEM-4000EX) equipped with a double-tilt specimen holder. The samples are prepared using standard mechanical polishing followed by argon-ion-milling to perforation.

Standard metal-oxide-semiconductor capacitor (MOSCAP) structures are created for capacitance-voltage (C-V) and current-voltage (I-V) measurements. The top electrode on the oxide surface is formed using sputtering of TaN, photolithography, and SF_6-based plasma etching. The bottom electrode is formed by using silver paste on the scratched backside of the Ge substrate. Both C-V and I-V were measured in air at room temperature under dark conditions using an Agilent B1500A semiconductor device parameter analyzer with a Cascade Microtech probe station. The sweeping voltage was applied to the top electrode with the bottom electrode grounded. The density of interface traps (D_{it}) was estimated using the conductance method with a range of frequencies extending from 1 kHz to 1.2 MHz.[50]

8.3. Results and Discussion

8.3.1. Deposition and crystallization of $SrHfO_3$ on Ge

Strontium hafnate films were deposited by ALD on the reconstructed Ge (001) at 225 °C. Film thicknesses between 1 to 20 nm were deposited, and the films were subsequently crystallized in vacuum at temperatures greater than 650 °C (typically 700 °C). Some thicker SHO films (> 5 nm) were grown in a two-step growth and anneal process for comparison. Figure 8.1 shows a series of RHEED images for a 2-nm-thick

SHO deposition: (a) after thermal deoxidation of the Ge (001) substrate showing a clear 2×1 reconstructed surface; and (b) the amorphous SHO film after ALD, and the crystalline SHO film after post-deposition vacuum annealing at 700 °C for 5 min, where the beam is aligned along the (c) <100> and (d) <110> directions of the perovskite oxide. Four-fold symmetry of the crystalline SHO film was observed by rotating the sample under electron illumination.

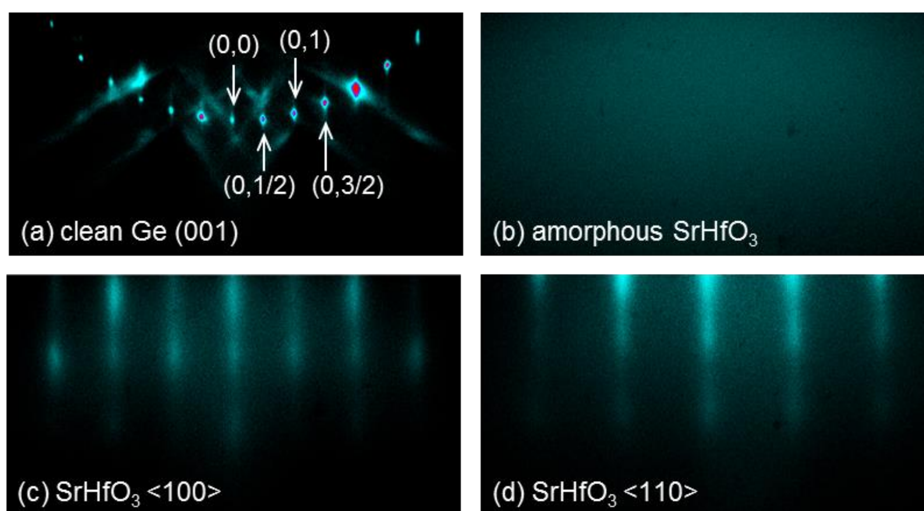

Figure 8.1. RHEED patterns for a 2-nm-thick $SrHfO_3$ deposition (a) after thermal deoxidation of the Ge (001) substrate showing a visible 2×1 reconstructed surface, (b) the amorphous $SrHfO_3$ film after ALD, and the crystalline SHO film after post-deposition vacuum annealing at 700 °C for 5 min where the beam is aligned along the (c) <100> and (d) <110> directions of $SrHfO_3$.

In situ XPS analysis was used to check the SHO film stoichiometry. High-resolution scans of the most prominent core-levels, Sr 3*d* and Hf 4*f*, were used for compositional analysis. Representative core-level spectra for a 2-nm-thick SHO film are shown in Figure 8.2. Both the Sr 3*d* and Hf 4*f* chemical shifts shown in Fig. 8.2(a) and 8.2(b), respectively, are consistent with the fully oxidized species ($SrHfO_3$). The fitted peak positions are located at binding energies of 134.0 eV and 135.7 eV for Sr $3d_{5/2}$ and

Sr $3d_{3/2}$, respectively, and 16.9 eV and 18.5 eV for Hf $4f_{7/2}$ and Hf $4f_{5/2}$, respectively. The asymmetry observed on the high binding energy side of the Hf $4f$ high-resolution scan is due to overlap of the Sr $4p$ peak, at approximately 19.8 eV. Deconvolution of the spectra allows for subtraction of the Sr $4p$ component and appropriate estimation of the film stoichiometry. For the sample shown in Fig. 8.2, the Sr:Hf ratio is 56:44. For the growth of crystalline perovskite oxides, stoichiometric to slightly Sr-rich is preferred due to the relative ease with which additional SrO layers can be incorporated while maintaining the film crystallinity. Previous work from our group has shown that Sr-rich STO films maintain the perovskite structure, while Ti-rich STO films are more likely to be amorphous.[46] The samples grown for this study varied slightly in cation stoichiometry from 52% to 56% Sr.

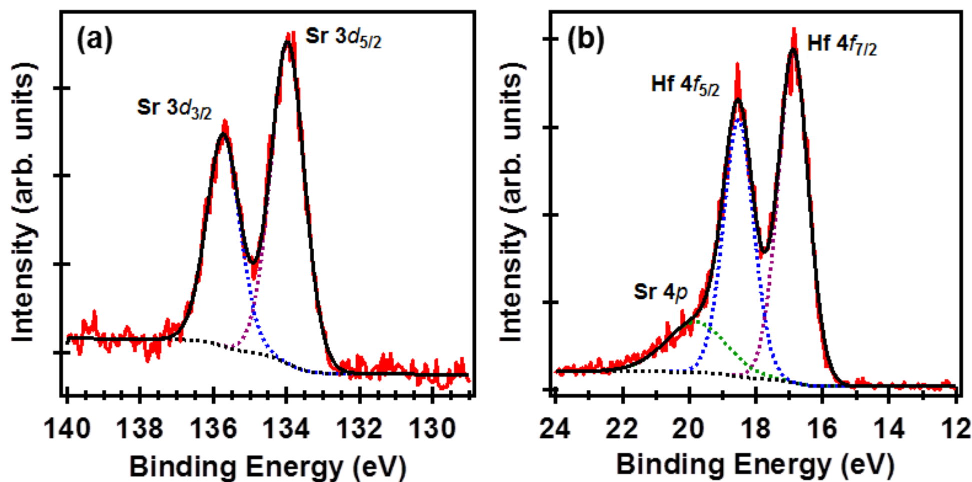

Figure 8.2. X-ray photoelectron spectra of a 2-nm-thick $SrHfO_3$ film showing the most prominent core-levels: (a) Sr $3d$ and (b) Hf $4f$. Deconvolution of the spectra (dashed lines) highlights the individual contributions of the Sr and Hf core-levels to the overall intensity.

XRD and rocking curve analyses were performed *ex situ* to verify the crystalline structure and out-of-plane alignment, as shown in Figure 8.3. Fig. 8.3(a) shows a rocking

curve around the SHO (002) peak for a 4.6-nm-thick SHO film, with a full-width half-maximum of 1.2°. The SHO film was post-deposition annealed in vacuum at a substrate temperature of 725 °C for 5 min. Fig. 8.3(b) shows a schematic model of the cubic perovskite $SrHfO_3$, where the bulk lattice constant is 4.069 Å. Fig. 8.3(c) shows a θ-2θ scan of the 4.6 nm SHO film on Ge, where only the (001)-oriented peaks are present. The SHO (002) peak position, 44.35 ± 0.05°, corresponds to an experimental *c*-axis lattice spacing of 4.082 ± 0.005 Å for the epitaxial film. This suggests that the *c*-axis is slightly expanded from the bulk, consistent with compressive in-plane strain. Assuming SHO (*a* ~ 4.069 Å) is perfectly strained to the Ge surface (3.992 Å), and a Poisson ratio of 0.25,[51] the expected out-of-plane lattice spacing would be 4.088 Å. This suggests that the 4.6 nm SHO film is at least partially strained to the underlying Ge substrate for the growth and annealing conditions.

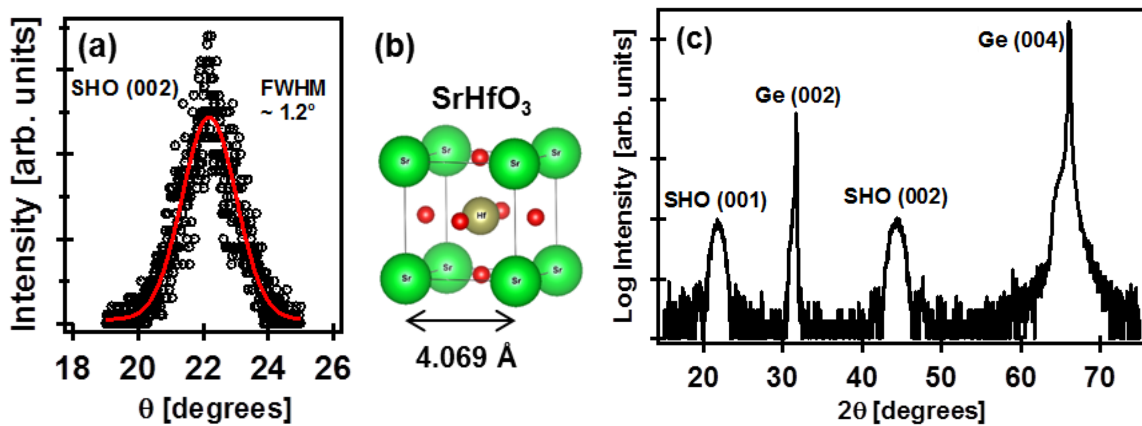

Figure 8.3. X-ray diffraction and rocking curve analysis of a 4.6-nm $SrHfO_3$ film on Ge: (a) rocking curve around the SHO (002) peak, with a full-width half-maximum of 1.2°, (b) schematic model of the cubic perovskite $SrHfO_3$ (a~4.069 Å), and (c) θ-2θ scan of the 4.6-nm SHO film on Ge, where only (001)-oriented peaks are present.

8.3.2. Band offset of the $SrHfO_3$-Ge heterojunction

In situ XPS analysis was used to estimate the band offset of the SHO-Ge heterojunction. Shallow core-level and valence band spectra were collected for bulk Ge (001), 11.2-nm-thick SHO (001) film grown by ALD, and the SHO-Ge (001) heterojunction. The thick SHO film was grown in a two-step growth and anneal process, with a measured stoichiometric ratio of 54:46 (Sr:Hf). The Ge substrate was prepared by solvent degreasing, UV/ozone exposure, and UHV annealing (700 °C for 1 hr) as described in the Experimental Section. Both core-level and valence band spectra were collected using a monochromated Al Kα source at 1486.6 eV. The valence band spectra for both the clean Ge (001) substrate and the 11.2-nm-thick SHO film are shown in Figure 8.4.

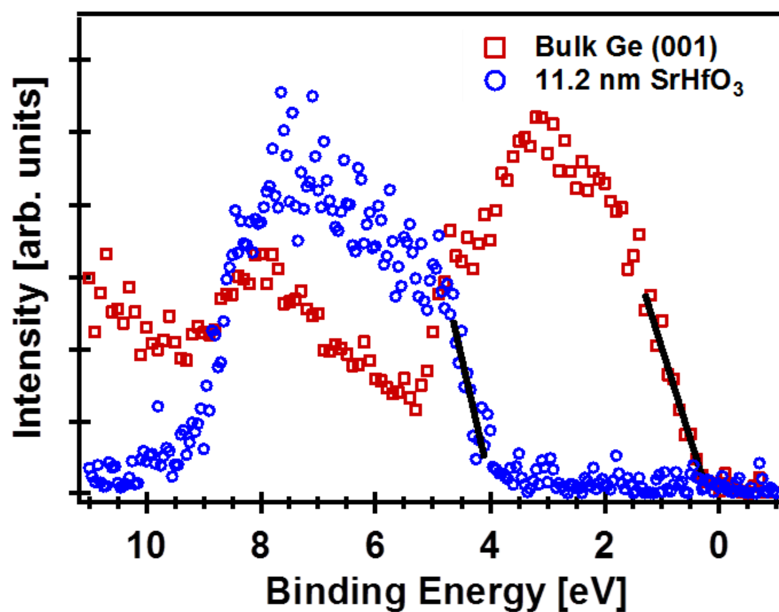

Figure 8.4. Valence band spectra for both clean Ge (001) substrate (red squares) and 11.2-nm-thick $SrHfO_3$ film (blue circles).

For the Ge (001) substrate, the energy difference between the valence band edge and Ge $3d_{5/2}$ centroid was 29.30 ± 0.05 eV. For the 11.2-nm-thick SHO film, the energy difference between the valence band edge and the Hf $4f_{7/2}$ centroid was 13.26 ± 0.05 eV. To probe the SHO-Ge heterojunction, a thin (~2 nm) epitaxial SHO film was grown on Ge. Both the Ge 3*d* and Hf 4*f* core-levels were measured, where the energy difference between the Ge $3d_{5/2}$ and Hf $4f_{7/2}$ centroids was 12.77 ± 0.05 eV. Using the measured energy differences, the valence band offset (VBO) between SHO and Ge was estimated to be -3.27 ± 0.10 eV.

To calculate the conduction band offset (CBO), we assume the bulk band gap values of SHO and Ge to be 6.1 eV and 0.66 eV, respectively.[26,52] The resulting CBO is 2.17 ± 0.10 eV, as shown schematically in Figure 8.5. The positive band offset value means the band energy is higher in the epitaxial SHO film. It should be noted, however, that the CBO may be overestimated due to the uncertainty in the bulk SHO band gap value. In other work, the electronic band gap for SHO has been reported to be 5.8 eV based on photoemission spectra and x-ray absorption data.[31] Regardless, the band alignment between crystalline SHO and Ge (001) is well above the minimum ~1 eV band offset required for suitable gate dielectrics.[53]

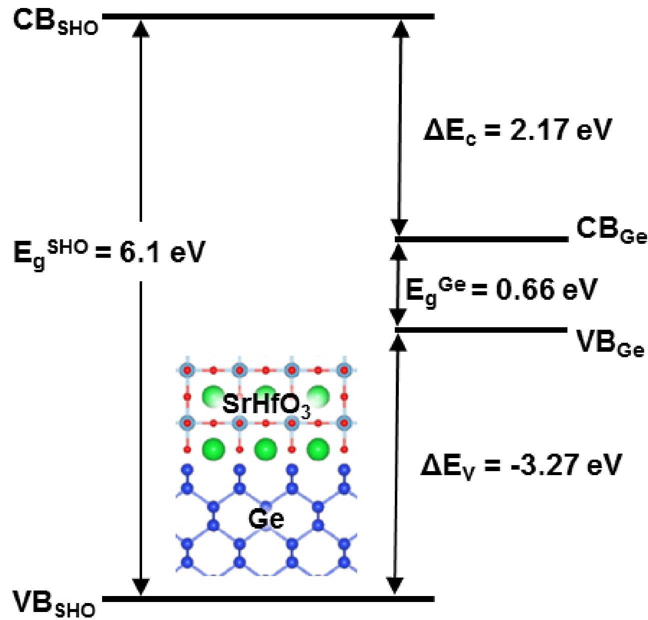

Figure 8.5. Band alignment of the SHO-Ge heterojunction estimated using shallow core-level and valence band spectra. The bulk band gap values of SHO and Ge were taken to be 6.1 eV and 0.66 eV, resulting in a CBO of 2.17 eV and VBO of -3.27 eV.

8.3.3. MOSCAP performance

Capacitor structures were made on five samples of varying SHO thickness to measure the capacitance of the oxide layer (C_{ox}) and extract the dielectric constant. These data are summarized in Figure 8.6 as a plot of capacitance equivalent thickness (CET) versus physical thickness of the epitaxial SHO layer. The dielectric constant is estimated to be k~18 for crystalline SHO. This value is much lower than the k~35 that was reported previously for polycrystalline SHO grown on TiN/Si substrates by MBE;[24,28] however, it is consistent with lower values reported for epitaxial SHO on Si (k~20) and polycrystalline SHO grown by plasma-assisted ALD (k~21).[26,32] The high dielectric constant (k~35) for polycrystalline SHO was only achieved after post-deposition annealing at 800 °C or higher on TiN/Si substrates,[28] possibly resulting in Ti

diffusion into the SHO layer. It is therefore reasonable to conclude that the dielectric constant of SHO is similar to that of the binary oxide HfO_2 (k~20).

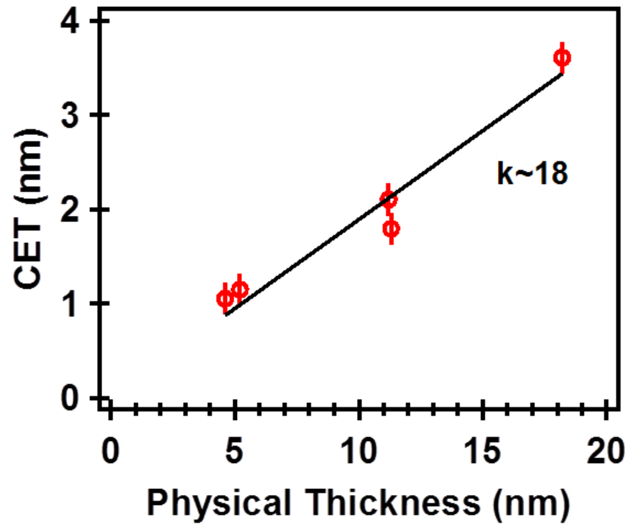

Figure 8.6. Plot of capacitance equivalent thickness (CET) versus physical thickness for extraction of the dielectric constant for epitaxial $SrHfO_3$ layers grown directly on Ge by atomic layer deposition. The films were crystallized by post-deposition vacuum anneal at 700 °C for 5 min.

To understand the effect of crystallization on the electrical performance, a comparison was made between crystalline and amorphous SHO films. Both SHO films were grown directly on the 2×1 reconstructed Ge surface with a nominal thickness of 20 nm. The amorphous SHO film was not post-deposition annealed, whereas the crystalline SHO film was post-deposition annealed at 700 °C for 5 min in vacuum. Metal-oxide-semiconductor capacitor (MOSCAP) structures were formed for both the crystalline and amorphous SHO samples. The amorphous SHO film showed a much lower saturation capacitance (C_{ox}) than the crystalline SHO film. This results in an effective dielectric constant of k~12 for the amorphous SHO and k~20 for the crystalline SHO film. However, despite an increase in dielectric constant, the observed D_{it} was significantly

higher for the crystalline film. Using the conductance method, the D_{it} was estimated to be 2×10^{12} cm^{-2} eV^{-1} and 4×10^{13} cm^{-2} eV^{-1} for the amorphous and crystalline SHO films, respectively. The increase of interface traps for the crystalline film is cause for concern since one of the expected benefits of epitaxial oxide dielectrics is the potential for drastically reduced interface traps. Additional studies are needed to understand the origin of these interface trap states in ALD-grown epitaxial dielectrics on Ge.

MOSCAP structures were used to evaluate the electrical performance of a 4.6-nm-thick SHO film grown on Ge by ALD, where the SHO film is still partially strained to the Ge substrate. The SHO was crystallized with a post-deposition anneal at 725 °C in vacuum for 5 min. Both C-V and I-V measurements were performed on a 15-µm radius top electrode. The C-V and I-V curves for the 4.6-nm SHO on Ge are shown in Figure 8.7, where the capacitance and current are normalized by the area of the top electrode. Fig. 8.7(a) shows the C-V and I-V response of the 4.6-nm-thick SHO film after removal from the UHV system, where the C-V is taken at a frequency of 1 MHz. C_{ox} saturates at ~3.3 µF/cm^2 under accumulation, yielding a dielectric constant of $k \sim 17$ for the SHO film. The 4.6-nm-thick SHO film shows a low leakage current of 6.3×10^{-6} A/cm^2 for an applied electric field of 1 MV/cm with an EOT of ~1.0 nm. This corresponds to a reduction of over seven orders of magnitude in leakage current when compared with a 15-nm-thick STO film on Ge.[23] The massive reduction in leakage current is attributed to the favorable conduction band offset (2.2 eV) for SHO on Ge; whereas, STO shows negligible conduction band offset (0.1 eV) under similar measurement conditions.[23]

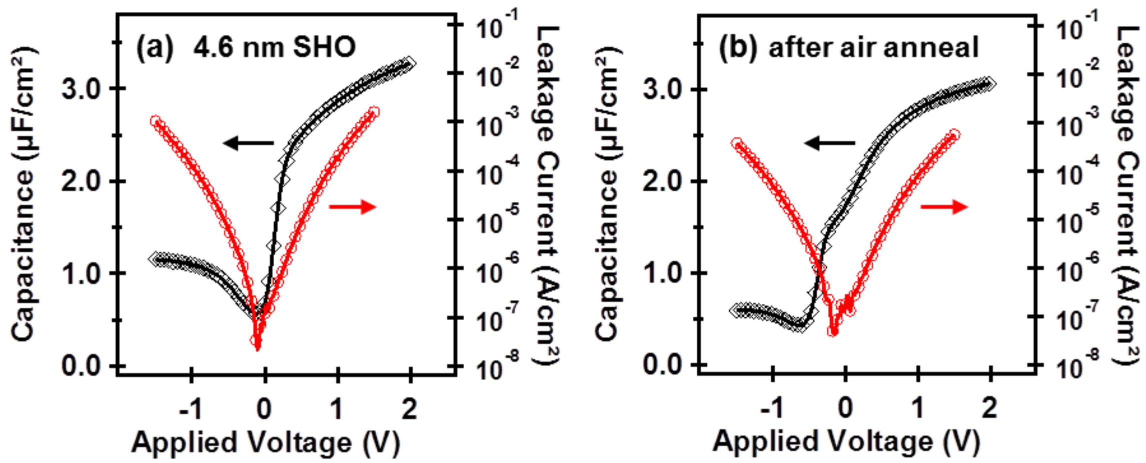

Figure 8.7. Capacitance-voltage (black curves) and current-voltage (red curves) measurements for a 4.6-nm-thick SHO film grown by ALD on Ge. The SHO film was crystallized by a post-deposition vacuum anneal at 725 °C for 5 min. Electrical measurements were taken: (a) before, and (b) after, *ex situ* air anneal at 300 °C for 30 min.

Using the conductance method, D_{it} was estimated to be 1×10^{13} cm^{-2} eV^{-1}. This relatively high D_{it} may result from an interfacial reaction that occurs during the vacuum anneal for crystallization of the SHO layer. This reaction is studied in detail in the next section. In efforts to reduce D_{it}, the 4.6-nm-thick SHO was post-deposition air annealed at 300 °C for 30 min after removal from the UHV system. Fig. 8.7(b) shows the C-V and I-V response of the SHO film after air anneal. The C-V response at a frequency of 1 MHz shows the emergence of a bump in the weak inversion region (~ -0.2 V) after air anneal that was not observed in the as-deposited sample. The exact origin of this defect state is not yet known. C_{ox} saturates at ~3.1 μF/cm^2 under accumulation, indicating minimal change in the dielectric constant (k~16). The leakage current is slightly improved to 4.0×10^{-6} A/cm^2 for an applied electric field of 1 MV/cm with an EOT of ~1.1 nm. The D_{it} for the air annealed sample was reduced to 6×10^{12} cm^{-2} eV^{-1}.

For comparison, the electrical performance of 2-nm-thick crystalline SHO with a 2-nm-thick Al_2O_3 capping layer was evaluated. The 2-nm-thick SHO film was crystallized at a relatively lower temperature of 650 °C, leading to a more abrupt interface, as discussed in the next section. The Al_2O_3 capping layer was needed to prevent excess leakage current through the thin SHO layer. With this dielectric stack, the crystalline SHO layer is used to minimize D_{it} at the oxide-Ge interface and the amorphous Al_2O_3 is an excellent leakage barrier. Figure 8.8 shows the C-V and I-V response of the SHO/Al_2O_3 dielectric stack on Ge after air annealing at 300 °C for 30 min. The SHO/Al_2O_3 stack has a very low leakage current of 1.9×10^{-7} A/cm^2 for an applied electric field of 1 MV/cm with an EOT of ~1.5 nm. As expected, the overall C_{ox} saturates at a lower value (~2.3 μF/cm^2) than the 4.6-nm-thick SHO film. Once again, a small bump is observed in the weak inversion region of the C-V response after air anneal. Assuming a dielectric constant of k~18 for the SHO film, the dielectric constant of the Al_2O_3 capping layer is k~8. This value is consistent with other reports of Al_2O_3 deposited by ALD with the same co-reactants under similar conditions.[54,55] The D_{it} for the SHO/Al_2O_3 dielectric stack is estimated to be 2×10^{12} cm^{-2} eV^{-1}. We attribute this lower D_{it} value to the lower annealing temperature (650 °C) required to crystallize the SHO film. More detailed analysis of the electrical performance and origin of defect states in crystalline SHO on Ge is the subject of another work.[56]

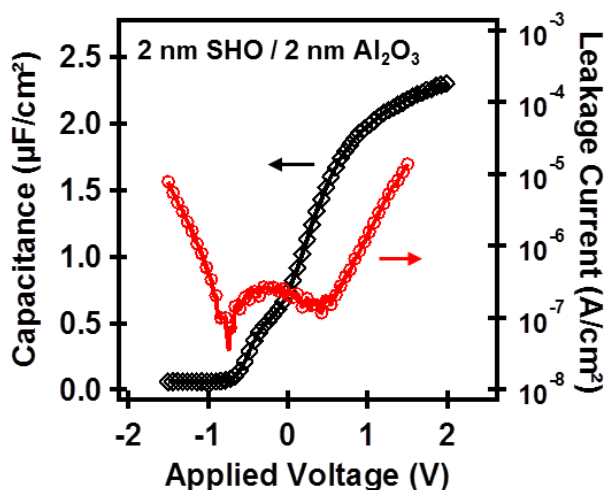

Figure 8.8. Capacitance-voltage (black curve) and current-voltage (red curve) measurements for 2-nm-thick SHO film on Ge with a 2-nm-thick Al_2O_3 capping layer. The SHO film was crystallized by a post-deposition vacuum anneal at 650 °C for 5 min before depositing the amorphous Al_2O_3 capping layer.

8.3.4. Crystallization temperature and the $SrHfO_3$-Ge interface

In all cases, strontium hafnate films deposited by ALD required post-deposition annealing for crystallization; however, the onset of crystallization varied between 650-750 °C depending on the thickness of the SHO film. The lowest crystallization temperature observed was at a substrate temperature of 650 °C for a 2-nm-thick SHO film. For very thin (~1 nm) SHO films, the temperature required for crystallization increased to 750 °C due to the substrate retarding crystallization. In all cases, SHO films between 2 and 20-nm-thick appeared fully crystallized when vacuum annealed at a substrate temperature of 700 °C for 5 min. At 700 °C, the temperature is approximately 80% of the Ge melting point (~940 °C), which could lead to interfacial instabilities due to Ge diffusion. In previous work, interfacial reaction between Ge and Hf metal has been reported to cause formation of a hafnium germanide ($HfGe_2$) at temperatures above ~600 °C.[57]

The effects of annealing temperature on the SHO-Ge heterostructure were examined by *in situ* RHEED and XPS. A very thin (~1 nm) SHO film was used so that the subtle changes in the Ge 3*d* core-level with increasing anneal temperature could be observed. A series of RHEED patterns are shown in **Figure 8.9** (a-c). The crystallization of the film can be observed at increasing temperatures of 650, 750, and 850 °C. At the lowest temperature of 650 °C (Fig. 8.9(a)), the SHO film appears amorphous. The film is thin enough that some electron diffraction is observed from the underlying Ge substrate. After annealing to 750 °C (Fig. 8.9(b)), the SHO film appears crystalline as shown by the appearance of an ordered streak pattern. The beam is aligned along the <100> direction of the film. When annealed at 850 °C (Fig. 8.9(c)), the diffraction patterns are more prominent. However, there are additional ½-order streaks present that may be due to a secondary phase formation at the interface.

The corresponding series of Ge 3*d* spectra collected by *in situ* XPS shown in Fig. 8.9 (d-f) provide insight into the interfacial reaction that occurs between SHO and Ge. The overall Ge 3*d* signal becomes less defined (broader) with increasing anneal temperature. Deconvolution of the Ge 3*d* core-level in CasaXPS also reveals that spectral components of both lower and higher binding energy than the bulk peak increase with higher temperature annealing. The lower binding energy component is attributed to a combination of "interfacial Ge" and Ge-Hf bonding. The chemical shift ($\Delta\varepsilon$ = -0.5 eV) observed for the interfacial Ge component appears similar to Ge (001) surface dimerization.[58] A similar chemical shift (-0.46 eV) is expected for Ge-Hf bonding from first-principles calculations.[59]

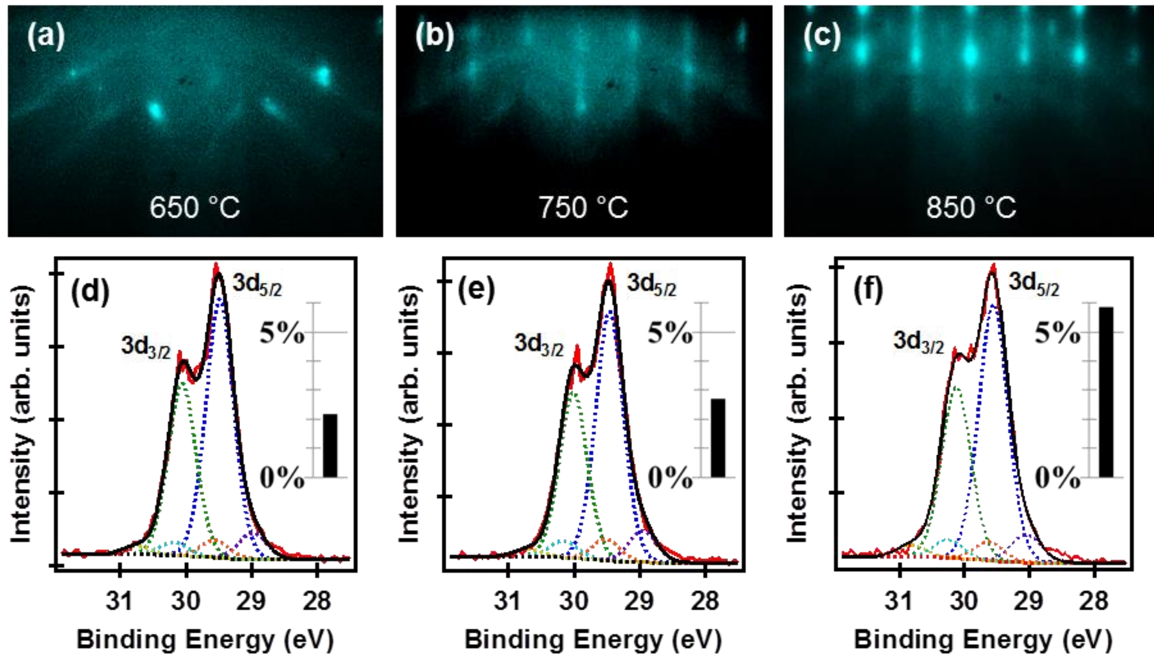

Figure 8.9. Effects of annealing temperature on the SHO-Ge heterostructure examined by *in situ* RHEED and XPS. RHEED patterns are shown at increasing anneal temperatures of (a) 650 °C, (b) 750 °C, and (c) 850 °C. The corresponding Ge 3*d* core-level spectra is shown in (d)-(f) for the 650-850 °C anneal temperature, respectively. The extent of interfacial reaction is quantified by the percent of Ge $3d_{5/2}$ for the lower binding energy component relative to the total Ge signal, as shown graphically on the right side of the high-resolution scan.

The percentage of the Ge $3d_{5/2}$ component associated with the lower binding energy relative to the entire Ge signal is shown to increase with temperature. The relative area of this component is 2.2%, 2.7%, and 5.6% for the film annealed at 650 °C, 750 °C, and 850 °C, respectively. We associate the increase in this component with an interfacial reaction between SHO and Ge with increasing temperature, although the small difference in relative area between 650 °C to 750 °C may not be significant. The more substantial change in the relative area of the lower binding energy component at 850 °C is attributed to an increase in Ge-Hf bonding. There is also an increase in the higher binding energy component, which is attributed to Ge^{1+} formation ($\Delta\varepsilon$ = 0.70 eV).[60] At higher annealing

temeperatures, desorption of the SHO film may occur; however, no noticeable changes in the Sr 3*d* or O 1*s* core-levels were observed after annealing at 850 °C (not shown). Only a slight shift (~0.2 eV) to lower binding energy was observed in the Hf 4*f* core-level with increased annealing temperature (not shown), which is also attributed to an increase in Ge-Hf bonding.

As further confirmation of an interfacial reaction, the SHO-Ge heterostructure was explored by cross-sectional TEM observations. SHO films were vacuum annealed at 650 °C and 700 °C to compare the abruptness of the SHO-Ge interface. The 2-nm-thick SHO film was post-deposition annealed at 650 °C for 5 min and then capped with 2 nm of amorphous Al_2O_3 before removal from the UHV system. The thicker SHO film (5.2-nm-thick) was annealed at 700 °C and was removed from the system without a capping layer. The 5.2-nm-thick SHO film was grown in a two-step growth and anneal process (2 nm plus 3.2 nm) with post-deposition annealing at 700 °C for 5 min following each growth. Electron micrographs of the two films are compared in Figure 8.10. At a substrate temperature of 650 °C (Fig. 8.9(a)), the SHO-Ge interface appears abrupt with a negligible interfacial layer (IL). However, for the higher substrate temperature of 700 °C (Fig. 8.10(b)), there is a clear presence of an IL at the SHO-Ge interface. The thickness of this IL appears to be ~0.5 nm, indicating that the interfacial reaction here is limited to 1-2 atomic layers. Regardless, this IL formation appears correlated to higher D_{it} values as discussed in the previous section. The electron micrographs, along with the XPS analysis, indicate that a low crystallization temperature (< 650 °C) is necessary to maintain an abrupt interface for the SHO-Ge heterojunction. An abrupt interface may be necessary to reduce D_{it} for the desired electrical performance of the crystalline oxide on Ge.

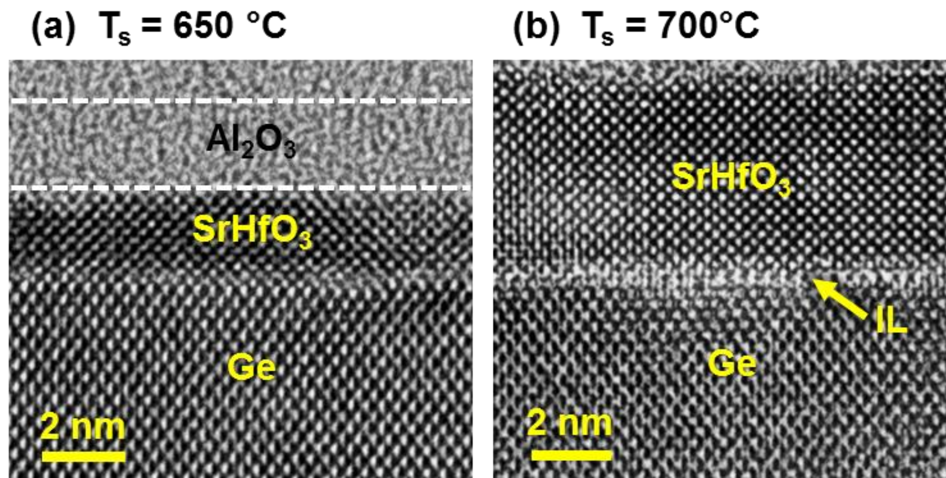

Figure 8.10. Transmission electron micrographs of: (a) 2-nm-thick SHO post-deposition annealed at 650 °C for 5 min and then capped with 2 nm of amorphous Al_2O_3; and (b) 5.2-nm-thick SHO film grown in a two-step growth and anneal process (2 nm plus 3.2 nm) with post-deposition annealing at 700 °C for 5 min. A higher anneal temperature of 700 °C, results in the formation of a very thin IL at the SHO-Ge interface.

With this material system, there is a tradeoff between sufficient thermal energy for crystallization to achieve a higher dielectric constant, while also maintaining a lower temperature to minimize interfacial reactions and D_{it}. As mentioned above, the 2-nm-thick SHO film began crystallizing at the lowest temperature of 650 °C. However, typical SHO films grown by this method crystallized somewhere between 650-700 °C, appearing fully crystalline by RHEED at 700 °C. The obvious concern is that at temperatures below 700 °C, films will not be fully crystallized and suffer from a lower dielectric constant. As a complicating factor, higher anneal temperatures are also correlated with increasing D_{it} values. The lowest D_{it} values for SHO on Ge were measured for films with no post-deposition anneal (amorphous films) or where the post-deposition anneal was kept at or below 650 °C. Low magnification electron micrographs of the two films discussed above are shown in Figure 8.11. The top image (Fig. 8.11(a))

reveals that the SHO film annealed at 650 °C has some tiny isolated amorphous regions, as denoted by the arrows. The thicker SHO film annealed at 700 °C, shown in Fig. 8.11(b), does not show any sign of amorphous regions. In both cases, the SHO films show excellent epitaxial alignment with the Ge substrate, and the deposited films are uniform in thickness. Further study is clearly required to optimize the annealing conditions to achieve high crystallinity to increase the dielectric constant, while maintaining an abrupt interface to minimize interface traps.

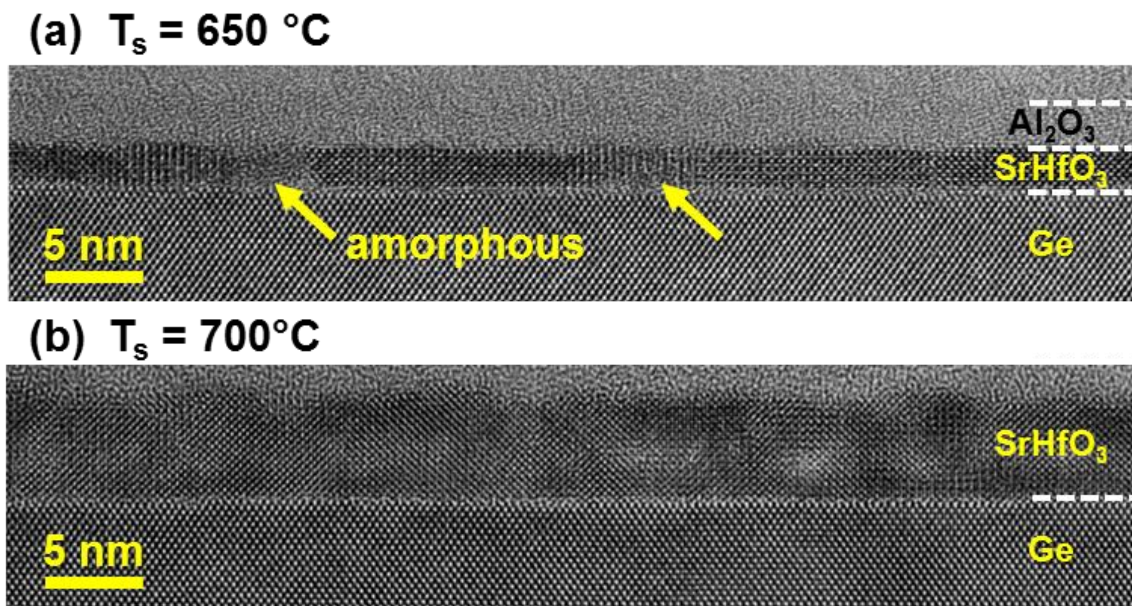

Figure 8.11. Low magnification electron micrographs of: (a) 2-nm-thick SHO film post-deposition annealed at 650 °C for 5 min and then capped with 2 nm of amorphous Al_2O_3; and (b) 5.2-nm-thick SHO film grown in a two-step growth and anneal process (2 nm plus 3.2 nm) with post-deposition annealing at 700 °C for 5 min. Tiny amorphous regions are visible in (a), attributed to the reduced post-deposition anneal temperature.

8.4. Detailed MOSCAP Performance of Strontium Hafnate on Germanium

8.4.1. A low-leakage epitaxial high-*k* gate oxide for germanium metal-oxide-semiconductor devices

Details of this section have been submitted to Appl. Phys. Lett. (2015) in collaboration with Chengqing Hu from Prof. Edward Yu's group at the University of Texas at Austin.

Germanium-based metal-oxide-semiconductor field-effect transistors are a promising candidate for high performance, low power electronics at the 7 nm technology node and beyond. However, the availability of high quality gate oxide/Ge interfaces that provide low leakage current density and effective oxide thickness, robust scalability, and acceptable interface state density (D_{it}) has emerged as one of the most challenging hurdles in the development of such devices. Here we demonstrate and present detailed electrical characterization of a high-*k* epitaxial oxide gate stack based on crystalline $SrHfO_3$ grown on Ge (001) by atomic layer deposition. Metal-oxide-Ge capacitor structures show extremely low gate leakage, small and scalable equivalent oxide thickness, and good and reducible D_{it}. Detailed growth strategies and post-growth annealing schemes are employed to reduce D_{it}. The physical mechanisms behind these phenomena are studied, and suggest approaches for further reduction of D_{it}.

Key Results

Capacitor structures were created for three high-*k* gate stack structures composed of epitaxial $SrHfO_3$ grown directly on Ge by ALD. For each stack, amorphous $SrHfO_3$ films were deposited on the clean, 2×1 reconstructed Ge (001) surface at a substrate temperature of 225 °C using strontium bis(triisopropylcyclopentadienyl) $[Sr(^iPr_3Cp)_2]$ (Absolut-Sr), hafnium formamidinate (Hf-FAMD), and purified water as co-reactants. The films were subsequently crystallized at temperatures between 650–725 °C in vacuum

($<2\times10^{-9}$ Torr) with a temperature ramp rate of 20 °C/min. The first gate stack consisted of a 4 nm $SrHfO_3$ film (4nm) that was crystallized by post-deposition vacuum annealing at 725 °C for 5 min. The second gate stack consisted of a 4 nm $SrHfO_3$ film capped with 2 nm of amorphous Al_2O_3 (4nm/2nm). In this case, the 4 nm $SrHfO_3$ film was grown in a two-step growth and anneal process, where 2 nm of $SrHfO_3$ were deposited each time and subsequently crystallized in vacuum at 700 °C for 5 min. In general, thinner $SrHfO_3$ films allowed for reduced annealing temperature for crystallization. For the third gate stack, 2 nm of $SrHfO_3$ was capped with 2 nm of amorphous Al_2O_3 (2nm/2nm). For this sample, the $SrHfO_3$ film was crystallized at 650 °C for 5 min, which was the lowest anneal temperature for which crystallization of the ALD-deposited $SrHfO_3$ layer was observed.

Fig. 8.12(a) shows a schematic of the different gate stack structures for the 4nm sample, the 2nm/2nm sample, and the 4nm/2nm sample, respectively. Fig. 8.12(b), (c) and (d) show reflection high-energy electron diffraction (RHEED) images of the 4nm sample, the 2nm/2nm sample, and the 4nm/2nm sample, respectively, before deposition of the top amorphous Al_2O_3 layer (if any). For the 4nm/2nm sample, RHEED images taken after crystallization of the initially deposited 2 nm $SrHfO_3$ (upper two images) and after crystallization of the latter 2 nm $SrHfO_3$ (lower two images) are both shown in Fig. 8.12(d). Streak patterns can be seen for all the three samples, indicative of the high crystalline quality of the $SrHfO_3$ film upon post-deposition annealing. Circular top electrode contacts with 15 μm radius were formed by sputtering of 200 nm TaN, photolithography, and SF_6-based inductive coupled plasma etching. The scratched backside of the n-type Ge substrate (ρ ~ 0.029–0.054 Ω-cm) was coated with silver paste and then attached to a metal specimen disc. Electrical measurements were performed on a Cascade Microtech probe station in ambient conditions by applying voltage to the top

electrode with the sample bottom grounded using an Agilent B1500A semiconductor device parameter analyzer.

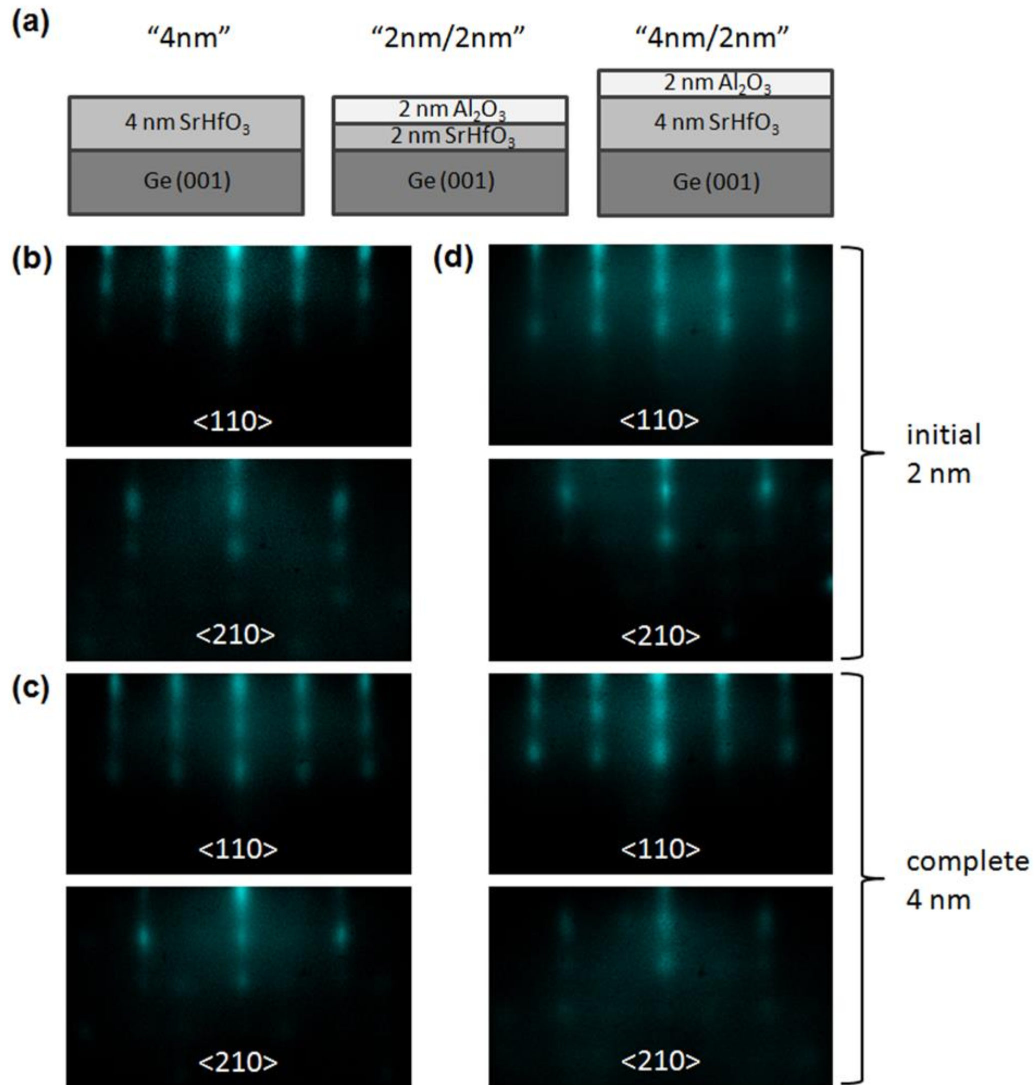

Figure 8.12. (a) Schematic diagrams of the 4nm, the 2nm/2nm, and the 4nm/2nm samples. Reflection high-energy electron diffraction images obtained from as-crystallized (b) 4 nm $SrHfO_3$ film for the 4nm sample, (c) 2 nm $SrHfO_3$ film for the 2nm/2nm sample, and (d) the initial 2 nm $SrHfO_3$ film (upper two images) and the complete 4 nm $SrHfO_3$ film (lower two images) for the 4nm/2nm sample. For each set of images taken, the beam is aligned along the [110] (top image) and the [210] (bottom image) azimuth.

Fig. 8.13(a) and (b) show the capacitance–voltage (C–V) and conductance–voltage (G–V) characteristics of the 4nm sample measured at frequencies ranging from 1 kHz to 1 MHz. The frequency dispersion of the C–V curves shows a clear signature of high-rate generation-recombination of minority carriers via midgap bulk traps in the Ge depletion layer (in the strong inversion regime) and via interface states (in the depletion and weak inversion regime), as well as a very short minority carrier response time, both due to the smaller band gap of Ge ($E_{g,Ge}$ = 0.67 eV) as compared to Si ($E_{g,Si}$ = 1.12 eV).[61,62] This behavior is also indicated in the G–V curves shown in Fig. 8.13(b), from which conductance plateaus in strong inversion and outstanding conductance peaks in depletion and weak inversion are observed. C increases as V becomes more negative in the strong inversion regime even at 1 MHz, suggesting impurity (e.g., hafnium atom) diffusion into the Ge substrate near the Ge/$SrHfO_3$ interface, which act as bulk traps assisting generation/recombination of minority carriers within the depletion layer in the strong inversion regime.[61] Such behavior together with the large conductance plateaus in strong inversion was not seen for the 2nm/2nm sample and the 4nm/2nm sample, which were crystallized at lower temperatures. This indicates that crystallization temperature plays a significant role in the occurrence and degree of impurity diffusion from the gate dielectric to the Ge substrate, as also reflected in a comparison of the transmission electron microscopy images.[63] Fig. 8.13(c) shows that the dielectric leakage current of the 4nm sample scales almost linearly with the device area, indicating an area-distributed leakage current through the 4 nm $SrHfO_3$ layer rather than a localized one. Fig. 8.13(d) shows the capacitance per unit area measured in the accumulation regime for different thicknesses (4.6 nm, 5.2 nm, 11.2 nm, and 18.2 nm) of the crystallized $SrHfO_3$ film, from which a dielectric constant of k=16 can be extracted.

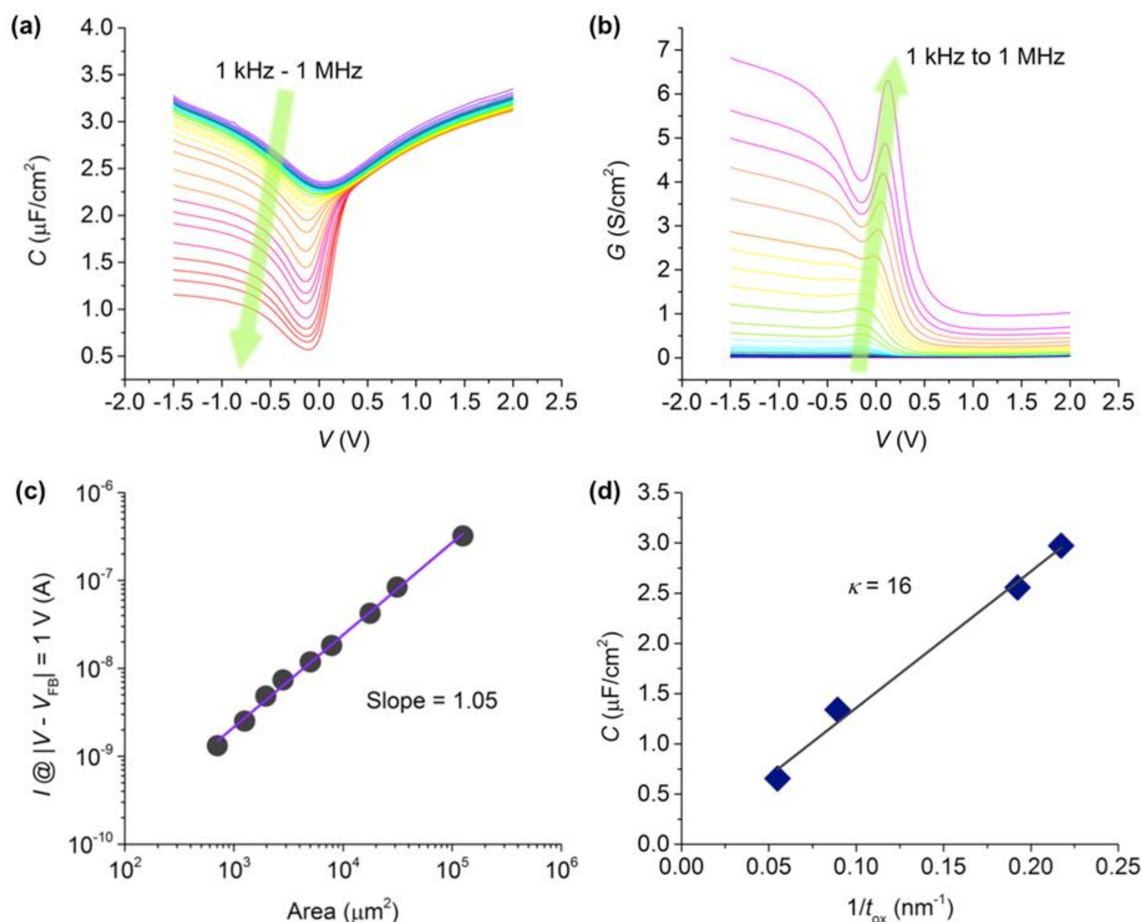

Figure 8.13. (a) Capacitance–voltage and (b) conductance–voltage characteristics of the 4nm sample for frequencies from 1 kHz to 1 MHz; (c) leakage current as a function of device area for the 4nm sample; (d) capacitance measured at 1 MHz in the accumulation regime for the $SrHfO_3$ films of different thickness for extraction of the dielectric constant of $SrHfO_3$.

Fig. 8.14(a), (b) and (c) show the current density–voltage (*J*–*V*) characteristics for the 4nm, 2nm/2nm, and 4nm/2nm samples, respectively, all measured from the same 15 μm-radius devices used for *C*–*V* and *G*–*V* measurements, with their corresponding *C*–*V* curves obtained at 1 MHz shown in Fig. 8.14(d), (e) and (f). The 2nm/2nm sample is more insulating than the 4nm sample, which can be understood by the fact that Al_2O_3 has a large band gap of 8.8 eV and a conduction band offset (CBO) of at least 2.6 eV with

Ge,[64] whereas the $SrHfO_3$ has a band gap of 6.1 eV and a CBO of 2.17 eV with Ge.[63] As shown in Fig. 8.14(c), the 4nm/2nm sample is the most insulating among the three samples, further verifying the high quality of the as-grown $SrHfO_3$ film. Note that the flattened *J–V* curves around 0 V shown in Fig. 8.14(b) and (c) are due to the minimum current level detectable by the testing equipment. Nevertheless, the current densities are well below the level required for these oxide stacks to be used as a gate dielectric.

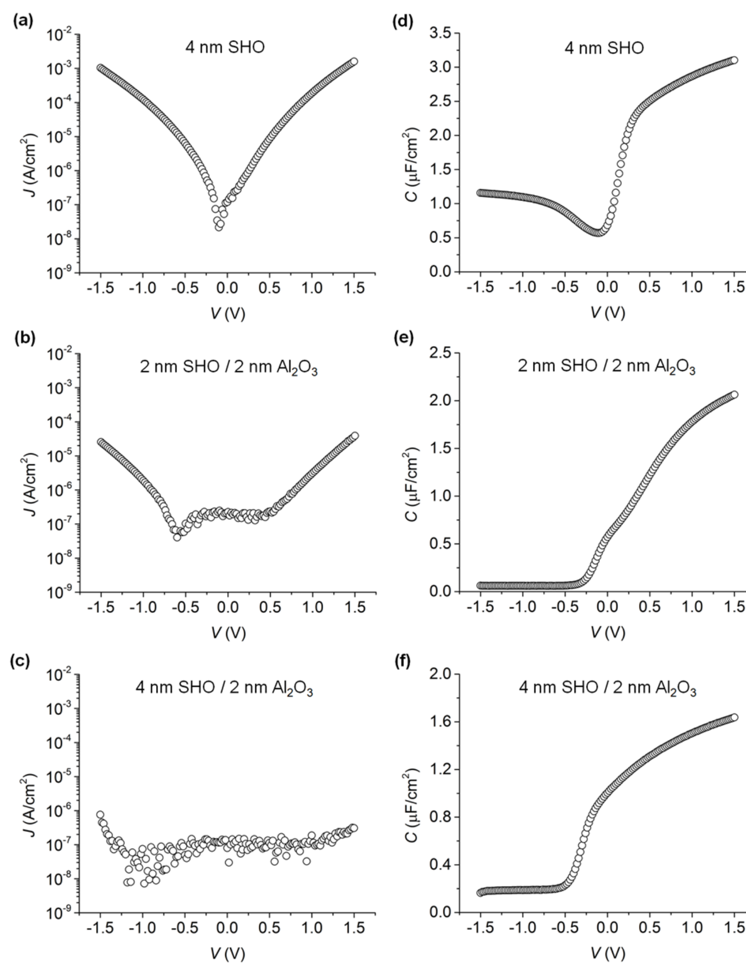

Figure 8.14. Leakage current density as a function of voltage for (a) the 4nm, (b) the 2nm/2nm, and (c) the 4nm/2nm samples, with their corresponding capacitance-voltage characteristics measured at 1 MHz shown in (d), (e), and (f), respectively.

The interface trap density D_{it} has also been extracted for all the samples under study using the conductance method. Shown in Fig. 8.15(a) are the parallel conductance loss peaks (G_p) in the frequency domain for the un-annealed 4nm/2nm sample as an example. Fig. 8.15(b) shows the energy profile of D_{it} for the un-annealed 4nm, un-annealed and annealed 4nm/2nm, and un-annealed and annealed 2nm/2nm samples, respectively. For the samples with an Al_2O_3 capping layer, it is expected that the Al_2O_3 layer would not affect D_{it} due to the underlying $SrHfO_3$ layer, which is at least 2 nm thick. The un-annealed 4nm/2nm sample shows a midgap (minimum) D_{it} of 1.4×10^{13} cm^{-2} eV^{-1}, much lower than that of the un-annealed 4nm sample (5.1×10^{13} cm^{-2} eV^{-1}). It is noteworthy that the crystallization temperature for the 4nm/2nm sample is 25 °C lower than the 4nm sample, reducing the possibility of intermixing at the $SrHfO_3$/Ge interface,[63] which is known to cause high D_{it}.

The improvement in D_{it} from the 4nm sample to the 4nm/2nm sample is believed to be related to the two-step growth technique, allowing for lower crystallization temperature to be adopted after $SrHfO_3$ growth of the 4nm/2nm stack. As shown in Fig. 8.12, the RHEED images for the as-crystallized initial 2 nm $SrHfO_3$ (Fig. 8.12(d)) show sharper lines than that of the one-step grown and as-crystallized 4 nm $SrHfO_3$ (Fig. 8.12(b)), indicating that higher crystallinity (less disorder) can be achieved by annealing a thinner 2 nm $SrHfO_3$ film. The improvement in D_{it} with lower crystallization temperature can be further justified through the comparison between the un-annealed 4nm/2nm sample and the un-annealed 2nm/2nm sample, for which the midgap D_{it} is 5.4×10^{12} cm^{-2} eV^{-1}, and for which the crystallization temperature is 50 °C lower than the former. Lower annealing temperature may result in small, isolated amorphous regions in the $SrHfO_3$ film.[63] However, our measurements of the $SrHfO_3$ dielectric constant, shown in Fig. 8.13(d), indicate that any formation of such small and isolated amorphous regions

that occurs here does not increase EOT, despite the fact that the dielectric constant of as-deposited amorphous $SrHfO_3$ is determined to be ~7 based on the *C*–*V* measurements (not shown).

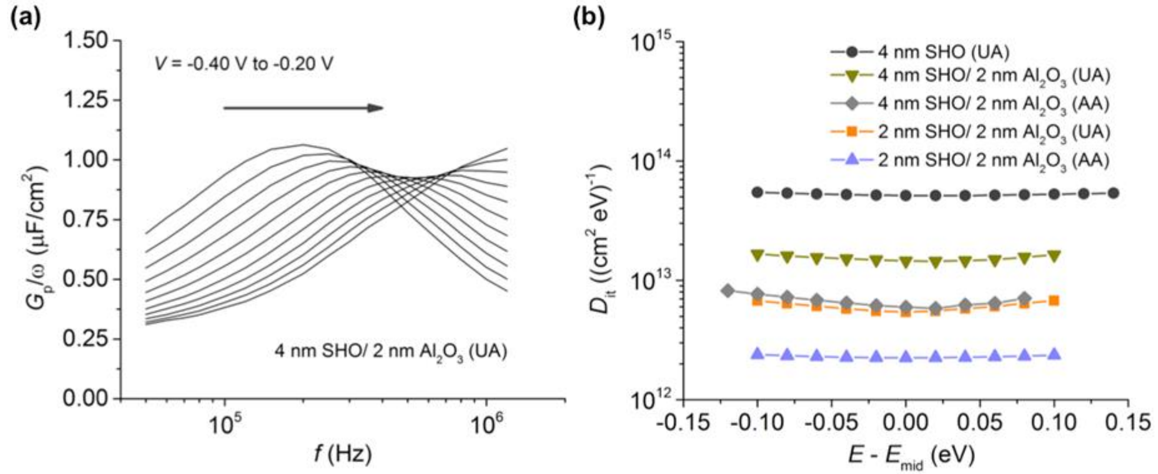

Figure 8.15. (a) Parallel conductance loss peaks in the frequency domain for the 4nm/2nm sample; (b) Energy profile of interface trap density extracted for the un-annealed 4nm, un-annealed and air-annealed 4nm/2nm, and un-annealed and air-annealed 2nm/2nm samples, respectively. "UA" and "AA" denote "un-annealed" and "air-annealed", respectively.

The influence of additional annealing procedures on D_{it} has also been investigated. As indicated in Fig. 8.15(b), 30 min annealing in air at 300 °C after the sample growth and before the device fabrication lowers D_{it} minimum for the 4nm/2nm sample and the 2nm/2nm sample to 5.8×10^{12} cm^{-2} eV^{-1} and 2.2×10^{12} cm^{-2} eV^{-1}, respectively, both by ~60%. While the air anneal is clearly very effective in reducing D_{it}, it was experimentally verified that other annealing schemes such as wet oxidation anneal or forming gas anneal at temperatures similar to 300 °C did not reduce D_{it} (not shown). It should also be noted that the air anneal performed in this work did not cause any significant degradation of EOT. Specifically, EOTs for the un-annealed 4nm, 2nm/2nm,

and 4nm/2nm are 1 nm, 1.7 nm, and 2.1 nm, respectively, whereas EOTs for the air-annealed 4nm, 2nm/2nm, and 4nm/2nm are 1.1 nm, 1.6 nm, and 2.2 nm, respectively. To further reduce D_{it}, the influence of chemical composition of the annealing atmosphere on D_{it} reduction and the physical mechanism of how the $SrHfO_3$/Ge interface is affected by air annealing need to be clarified. It is believed that D_{it} can be improved with further optimization of the annealing atmosphere and temperature.

Our results yield combinations of leakage current suppression and EOT that compare very favorably with the current state of the art. Fig. 8.16 shows J vs. EOT found in recent reports that represent the state of the art of gate stack development for Ge-based MOSFETs,[65-73] along with our results in this work (indicated by stars). Specifically, leakage currents measured for both the un-annealed and the air-annealed $SrHfO_3$ films or $SrHfO_3/Al_2O_3$ stacks in this work define the lower bound of J for their corresponding ranges of EOT in Fig. 8.16, respectively. Moreover, with further scaling of the gate dielectric stacks, it is expected that the advantage of using the gate stacks developed in this work regarding the combination of J and EOT would be even more pronounced. It should also be noted that for the previous publications shown in Fig. 8.16 that reported a D_{it} minimum,[65,66,68,71-73] the D_{it}'s are mainly on the order of lower 10^{11} cm^{-2} eV^{-1}, which is about 10 times lower than the best D_{it} achieved in this work. Therefore, for our $SrHfO_3$-based gate stacks, a D_{it} comparable to the current state of the art remains to be achieved.

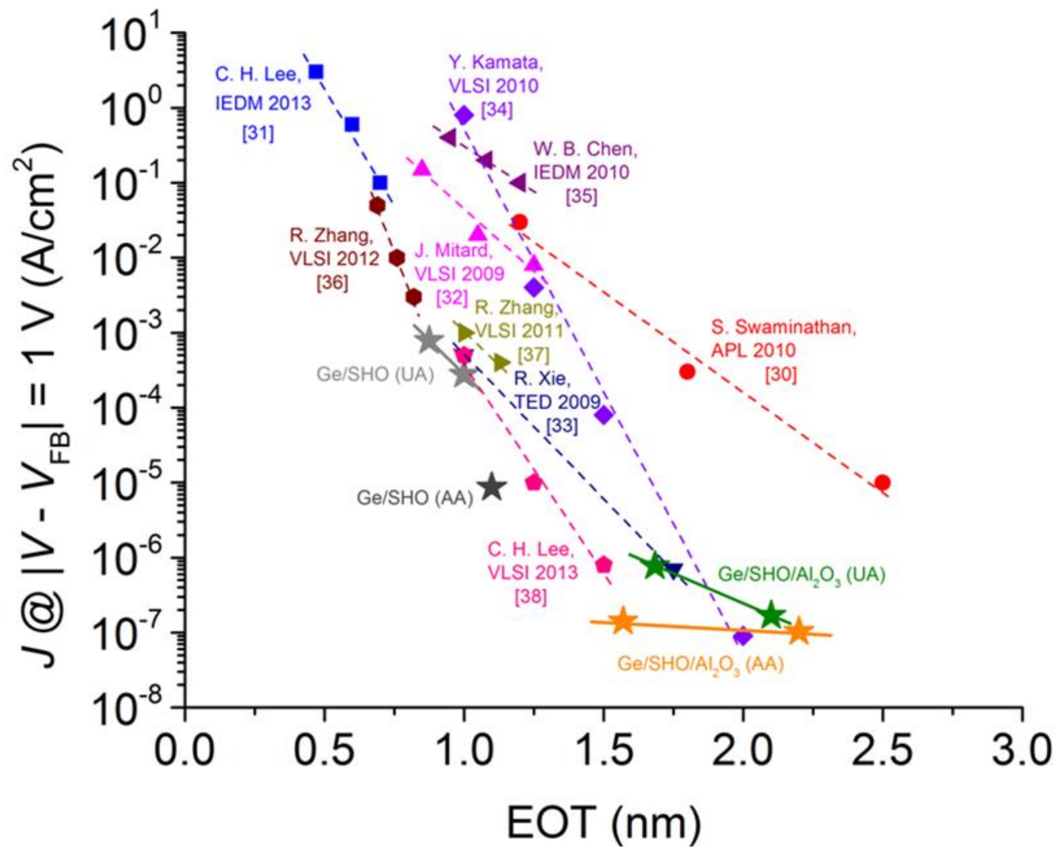

Figure 8.16. Leakage current versus EOT reported as the state of the art in recently published work together with our results in this work (star symbols). "UA" and "AA" denote "un-annealed" and "air-annealed", respectively.

8.5. SUMMARY

Crystalline strontium hafnate, $SrHfO_3$ (SHO), films have been grown by atomic layer deposition directly on Ge (001) substrates. The 2×1 reconstructed Ge (001) surface was prepared by thermal annealing in vacuum and transferred *in situ* to the ALD system. After deposition of an amorphous SHO layer (~2-20 nm), the film was crystallized by post-deposition anneal (~700 °C) in vacuum. The crystalline SHO films were confirmed to be (001)-oriented with epitaxial registry to the Ge (001) surface. Band offset

measurements indicate that the SHO has favorable band offsets with Ge for gate dielectric applications, with a VBO of -3.27 eV and CBO of 2.17 eV. Electrical measurements of MOSCAP structures estimate the dielectric constant of crystalline SHO to be k~18. The leakage current of a 4.6-nm-thick SHO film was 6.3×10^{-6} A/cm^2 for an applied electric field of 1 MV/cm, which indicates a significant advantage of Hf-based perovskites over Ti-based perovskites, such as STO. The lowest D_{it} value for the SHO-Ge heterojunction was estimated to be 2×10^{12} cm^{-2} eV^{-1}. Interestingly, D_{it} is not improved by crystallization of the SHO layer and is negatively impacted by higher post-deposition annealing temperature and corresponding abruptness of the SHO-Ge interface. The current work shows extremely promising potential for the integration of crystalline oxides on Ge by atomic layer deposition for advanced electronic applications.

The use of gate dielectric stacks based on ALD-grown epitaxial $SrHfO_3$ for Ge-based MOS applications was demonstrated. The gate stacks developed yield combinations of ultralow leakage current and a small EOT which are comparable or superior to the state of the art published so far in the gate stack development for Ge-based MOSFETs. In addition, D_{it} has shown to be lowered by using (i) a two-step technique for the epitaxial growth; (ii) a lower crystallization temperature for minimized intermixing at the $SrHfO_3$/Ge interface; and (iii) post-growth air annealing. Findings of this work hold a great promise of using epitaxial gate dielectrics for Ge MOSFETs and suggest possible routes to further optimizing the electrical properties of these gate stacks.

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Chapter 9: Research Summary

9.1. Conclusions

Epitaxial anatase titanium dioxide (TiO_2) films have been grown by atomic layer deposition (ALD) on Si(001) substrates using a strontium titanate (STO) buffer layer without any amorphous SiO_x layer at the STO-Si interface. Four unit cells of STO grown by molecular beam epitaxy (MBE) serve as the surface template for ALD growth. The growth of TiO_2 was achieved using titanium isopropoxide and water as the co-reactants at a substrate temperature of 225-250 °C. To preserve the quality of the MBE-grown STO, the samples were transferred *in-situ* from the MBE chamber to the ALD chamber. After ALD growth, the samples were annealed *in-situ* at 600 °C in vacuum (10^{-7} Pa) for 1-2 hr. Reflection high-energy electron diffraction was performed during the MBE growth of STO on Si(001), as well as after deposition of TiO_2 by ALD. The ALD films were shown to be highly ordered with the substrate. X-ray diffraction revealed the TiO_2 films were anatase with only the (004) reflection present at $2\theta \sim 38.2°$, indicating that the *c*-axis is slightly reduced from that of anatase powder ($2\theta \sim 37.9°$).

Anatase TiO_2 films up to 100 nm thick have been grown that remain highly ordered in the (001) direction on STO-buffered Si(001) substrates. *In situ* X-ray photoelectron spectroscopy analysis revealed that the ALD process did not induce Si-O bonding at the STO-Si interface. Slight improvement in crystallinity of the TiO_2 film was achieved through *in situ* annealing under vacuum (10^{-9} Torr) at 450-600 °C. However, the amount of Si-O bonding increased following annealing at temperatures greater than 250 °C. X-ray diffraction revealed that TiO_2 films annealed at a temperature of 250 °C in vacuum (10^{-9} Torr) for 1 hr were the anatase phase and well crystallized.

The results indicate that careful consideration of growth temperature and annealing conditions may allow epitaxial oxide films to be grown by ALD on STO-buffered Si(001) substrates without formation of an amorphous SiO_x layer.

Epitaxial strontium titanate (STO) films have been grown by atomic layer deposition (ALD) on Si(001) substrates with a thin STO buffer layer grown by molecular beam epitaxy (MBE). Four unit cells of STO grown by MBE serve as the surface template for ALD growth. The STO films grown by ALD are crystalline as-deposited with minimal, if any, amorphous SiO_x layer at the STO-Si interface. The growth of STO was achieved using bis(triisopropylcyclopentadienyl)-strontium, titanium tetraisopropoxide, and water as the co-reactants at a substrate temperature of 250 °C. *In situ* X-ray photoelectron spectroscopy (XPS) analysis revealed that the ALD process did not induce additional Si-O bonding at the STO-Si interface. Post-deposition XPS analysis also revealed sporadic carbon incorporation in the as-deposited films. However, annealing at a temperature of 250 °C for 30 min in moderate to high vacuum (10^{-6} to 10^{-9} torr) removed the carbon species. Higher annealing temperatures (> 275 °C) gave rise to a small increase in Si-O bonding, as indicated by XPS, but no reduced Ti species were observed. X-ray diffraction revealed that the as-deposited STO films were *c*-axis oriented and fully crystalline. A rocking curve around the STO(002) reflection gave a full-width half-maximum of 0.30 ± 0.06 degrees for film thicknesses ranging from 5 to 25 nm. Cross-sectional transmission electron microscopy revealed that the STO films were continuous with conformal growth to the substrate and smooth interfaces between the ALD- and MBE-grown STO. Overall, the results indicate that thick, crystalline STO can be grown on Si(001) substrates by ALD with minimal formation of an amorphous SiO_x layer using a four-unit-cell STO buffer layer grown by MBE to serve as the surface template.

Strontium titanate, $SrTiO_3$ (STO), thin films incorporated with lanthanum were grown on Si (001) substrates at a thickness range of 5-25 nm. Atomic layer deposition (ALD) was used to grow the $La_xSr_{1-x}TiO_3$ (La:STO) films after buffering the Si (001) substrate with four-unit-cells of STO deposited by molecular beam epitaxy. The crystalline structure and orientation of the La:STO films were confirmed via reflection high-energy electron diffraction, X-ray diffraction, and cross-sectional transmission electron microscopy. The low temperature ALD growth (~225 °C) and post-deposition annealing at 550 °C for 5 min maintains an abrupt interface between Si (001) and the crystalline oxide. Higher annealing temperatures (650 °C) showed more complete La activation with film resistivities of $\sim 2.2 \times 10^{-2}$ Ω-cm for 20-nm-thick La:STO (x~0.15); however, the STO-Si interface is slightly degraded due to the increased annealing temperature. To demonstrate the selective incorporation of lanthanum by ALD, a layered heterostructure was grown with an undoped STO layer sandwiched between two conductive La:STO layers. Based on this work, an epitaxial oxide stack centered on La:STO and $BaTiO_3$ integrated with Si is envisioned as a material candidate for a ferroelectric field-effect transistor.

The growth of crystalline $SrTiO_3$ (STO) directly on germanium via a chemical method was demonstrated. After thermal deoxidation, the Ge substrate is transferred *in vacuo* to the deposition chamber where a thin film of STO (~ 2 nm) was deposited by atomic layer deposition (ALD) at 225 °C. Following post-deposition annealing at 650 °C for 5 min, the STO film became crystalline with epitaxial registry to the underlying Ge (001) substrate. Thicker STO films (up to 15 nm) were then grown on the crystalline STO seed layer. The crystalline structure and orientation are confirmed via reflection high-energy electron diffraction, X-ray diffraction, and transmission electron microscopy. Electrical measurements of a 15-nm thick epitaxial STO film on Ge showed a large

dielectric constant (k ~ 90), but relatively high leakage current of ~10 A/cm^2 for an applied field of 0.7 MV/cm. To suppress the leakage current, an aluminum precursor was cycled during ALD growth to grow crystalline Al-doped STO ($SrTi_{1-x}Al_xO_{3-\delta}$) films. With sufficient Al doping (~13%), the leakage current decreased by two orders of magnitude for an 8-nm thick film. The current work demonstrates the potential of ALD-grown crystalline oxides to be explored for advanced electronic applications, including high-mobility Ge-based transistors.

The crystalline perovskite oxide, strontium hafnate, was explored as a potential high-k gate dielectric for Ge-based transistors. $SrHfO_3$ (SHO) was grown directly on Ge by atomic layer deposition and became crystalline with epitaxial registry after post-deposition vacuum annealing at ~700 °C for 5 min. The 2×1 reconstructed, clean Ge (001) surface was a necessary template to achieve crystalline films upon annealing. The SHO films exhibited excellent crystallinity, as shown by x-ray diffraction and transmission electron microscopy. The SHO films have favorable electronic properties for consideration as a high-k gate dielectric on Ge, with satisfactory band offsets (> 2 eV), low leakage current (< 10^{-5} A/cm^2 at an applied field of 1 MV/cm) at an equivalent oxide thickness of 1 nm, and a reasonable dielectric constant (k~18). The interface trap density (D_{it}) was estimated to be as low as ~2×10^{12} cm^{-2} eV^{-1} under the current growth and anneal conditions. Some interfacial reaction was observed between SHO and Ge at temperatures above ~650 °C, which may contribute to increased D_{it} value. This study confirms the potential for crystalline oxides grown directly on Ge by atomic layer deposition for advanced electronic applications.

9.2. Recommendations for Future Work

The overarching goal of my research was to develop methods for depositing crystalline oxides on Si and Ge via atomic layer deposition (ALD). Successful deposition on Si required a $SrTiO_3$ buffer layer to serve as a robust template to seed crystallization. However, other surface templating on Si should be explored in more detail. For example, the half-monolayer Sr on Si has shown to be a viable template for crystalline $SrTiO_3$ growth by molecular beam epitaxy (MBE). I have attempted to use this template for ALD-grown $SrTiO_3$ as well. Interestingly, no Si-O bonding was observed after ALD; however, subsequent vacuum annealing did not form an epitaxial film and induced some interfacial reaction. It may be possible to suppress this interfacial reaction by altering the anneal conditions, such as rapid thermal annealing. This may provide a route to eliminate the need for the MBE-grown template layer for crystalline oxide growth on Si.

One of the key successes of my research was the formation of crystalline oxide directly on Ge via ALD. At the present, only a few crystalline oxides have been studied that include $SrTiO_3$, $SrHfO_3$, and $BaTiO_3$. $SrTiO_3$ was found to crystallize at a lower temperature than $SrHfO_3$. However, $SrTiO_3$ films were very leaky under applied bias voltage. $SrHfO_3$ films showed reduced leakage current, but a much lower permittivity. We recently began to explore the deposition of $Sr(Hf,Ti)O_3$ to maintain a low leakage current, increase permittivity, and provide improved lattice-matching to the Ge (001) surface. In consideration of lattice-matching, $CaHfO_3$ is also an interesting material due to its nearly perfect lattice match with the Ge (001) surface. Crystallization of the $CaHfO_3$ perovskite phase should stabilize the pseudocubic material. This will provide insight into whether or not the lattice mismatch of $SrHfO_3$ plays a significant role in the observed D_{it}.

Beyond the intrinsic properties of the crystalline oxide, a detailed study of the annealing conditions that impact interface trap density (D_{it}) is necessary. Despite the appearance of an abrupt interface between $SrTiO_3$ and Ge, the observed D_{it} is greater than 10^{13} cm^{-2} eV^{-1}. Improvement of the D_{it} (~10^{12} cm^{-2} eV^{-1}) was observed for $SrHfO_3$ by maintaining a lower vacuum anneal temperature for crystallization and subsequent air annealing. The origin of D_{it} must be different between $SrTiO_3$ and $SrHfO_3$. Regardless, significant improvement in the oxide-Ge interface is required to drive D_{it} below 10^{11} cm^{-2} eV^{-1}. Experiments with different post-deposition anneal treatments are needed to understand the origin of D_{it} and possible ways to reduce it.

Moving beyond Si and Ge, there is also the opportunity to explore the deposition of crystalline oxides on III-V semiconductors, such as GaAs or GaN, using ALD growth. Epitaxial $LaLuO_3$ films grown on GaAs by ALD were already demonstrated by the Gordon group at Harvard University. There is the potential to capitalize on applications for functional perovskite oxides integrated with III-V semiconductors. For example, high-mobility NMOS transistors would benefit from the significantly higher electron mobility for GaAs over Si. Again, one of the major tasks is to understand the interface structure between the crystalline oxide and semiconductor, and find methods to reduce the interface trap states.

Appendix

FIRST-AUTHOR PUBLICATIONS

(1) M. D. McDaniel, C. Hu, S. Lu, T. Q. Ngo, A. Posadas, A. Jiang, D. J. Smith, E. T. Yu, A. A. Demkov, and J. G. Ekerdt, “Atomic layer deposition of crystalline $SrHfO_3$ directly on Ge (001) for high-k dielectric applications,” J. Appl. Phys. **117**, 054101-(1-9) (2015).

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TECHNICAL PRESENTATIONS

(1) (Presentation/Poster) *Atomic layer deposition of crystalline* $SrHf_xTi_{1-x}O_3$ *directly on Ge (001) for high-k dielectric applications*, 42nd Conference on the Physics and Chemistry of Surfaces and Interfaces (PCSI-42); Salt Lake City (Snowbird), Utah; January 19, 2015.

(2) (Presentation) *Crystalline SrHfO3 grown directly on Ge (001) by atomic layer deposition as a gate oxide for high-mobility Ge-based transistors*, American Vacuum Society (AVS) Fall 2014 meeting; Baltimore, Maryland; November 14, 2014.

(3) (Presentation) *A chemical route to epitaxial oxides on semiconductors: Crystalline* $SrTiO_3$ *and* $SrHfO_3$ *grown directly on Ge (001) by ALD*, 14th International Conference on Atomic Layer Deposition (ALD 2014); Kyoto, Japan; June 18, 2014.

(4) (Poster) *Integration of a Conductive Perovskite [La-doped* $SrTiO_3$*] on Si (001) by ALD Using a Thin* $SrTiO_3$ *Buffer Layer*; Materials Research Society (MRS) Fall 2013 Meeting & Exhibit; Boston, Massachusetts; December 5, 2013.

(5) (Presentation) *Growth of epitaxial oxide films on silicon substrates using ALD: Case study of* TiO_2*,* $SrTiO_3$*, and* $LaAlO_3$ *on* $SrTiO_3$*-buffered Si(001)*; 12th International Conference on Atomic Layer Deposition (ALD 2012); Dresden, Germany; June 20, 2012.

(6) (Presentation) *Growth and Characterization of Epitaxial Anatase (001) on* $SrTiO_3$*-buffered Si (001) Using Atomic Layer Deposition*; 2012 MRS Spring Meeting & Exhibit - Symposium Q: Titanium Dioxide Nanomaterials; San Francisco, California; April 13, 2012.

(7) (Presentation/Poster) *Growth and Characterization of Epitaxial Oxide Films on Silicon Substrates using Atomic Layer Deposition: A Case Study of anatase (001) on* $SrTiO_3$*-buffered Si(001)*; 39th Conference on the Physics and Chemistry of Surfaces and Interfaces (PCSI-39); Santa Fe, New Mexico; January 24, 2012.

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Vita

Martin Douglas McDaniel was born and raised in Bloomington, Indiana. He is an honors graduate of Bloomington High School South class of 2002. Martin completed his undergraduate degree in chemical engineering at Rose-Hulman Institute of Technology (Terre Haute, Indiana) in May 2006. In his senior year at Rose-Hulman, he received the Sam C. Hite award given to the most outstanding chemical engineering senior, as well as the Captain "Sarge" Kearns award given to the Wabash Battalion distinguished Army ROTC graduate. In May 2006, he was also commissioned as a Second Lieutenant in the United States Army. Martin met his beloved wife, Jennifer, in March 2007 and they were married in June 2012.

Before returning to graduate school, Martin served dual functions as an Army reserve officer and chemical process engineer at Naval Surface Warfare Center, Crane Division (NSWC Crane) for over five years. As an Army officer, Martin was deployed in support of Operation Iraqi Freedom from December 2007 to December 2008. He served as the Executive Officer for a convoy security company stationed in northern Iraq. Upon returning from deployment, Martin continued to work in a small manufacturing shop for printed circuit boards at NSWC Crane. His work included research and development of new materials and process optimization for printed circuits.

In January 2011, Martin began his graduate studies researching advanced semiconductor materials under the advisement of Prof. John Ekerdt at the University of Texas at Austin. His graduate research developed chemical routes to the growth of many crystalline perovskite oxides on both silicon and germanium, including photocatalytic anatase TiO_2, $SrTiO_3$, ferroelectric $BaTiO_3$, high-k dielectrics ($LaAlO_3$ and $SrHfO_3$), and

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