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Grain Size And Cap Layer Effects On Electromigration Reliability Of Cu Interconnects: Experiments And Simulation

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Abstract. This paper combined experiments and simulation to investigate the grain size and cap layer effects on electromigration (EM) reliability of Cu interconnects. First the statistical distribution of EM lifetime and failure modes were examined for in laid Cu interconnects of large and small grain structures with two different cap layers of SiCN vs. CoWP. The CoWP cap was found to significantly improve the EM lifetime due to the suppression of the interfacial mass transport as a result of strengthening of the Cu/cap interface bonding. In addition, the grain size was observed to affect the EM reliability significantly, particularly for the CoWP capped structures. Resistance traces and failure analysis revealed two distinct failure modes: mode I with voids formed near the cathode via corner and mode II with voids formed in the trench several microns away from the cathode via. It was found that large grain size and strong cap interface reduced the mass transport rate and the void diffusion in the Cu line, leading to a longer EM lifetime and a higher proportion of mode II failures. A statistical simulation of EM lifetimes was also applied to Cu interconnects with grain structures generated by the Monte Carlo method. The simulation results for different grain sizes and cap interfaces are in good agreement with the experimental observations.

Keywords: Electromigration, Cu Interconnect, grain size, cap layer, failure mode
PACS: 66.30.Qa, 85.40.Ls, 85.40.Qx

INTRODUCTION

Electromigration (EM) of Cu interconnects remains a major reliability concern as aggressive physical dimension and current density scaling continues. During EM, Cu atoms migrate along the electron flow direction and leave a void at the cathode end of the line to cause an open circuit failure. EM in Cu interconnects differs significantly from that in Al interconnects, in which a stable Al oxide layer passivates the top interface and grain boundaries are the fastest pathways[1-2]. However, for Cu interconnects, mass transport along the Cu/SiNx interface is faster than at grain boundaries due to the defects on that interface created by the CMP process before cap layer deposition[3-6]. Prior to the 65 nm node with line width exceeding 100 nm, the Cu damascene lines were commonly observed to have a bamboo-like grain structure and the Cu/SiNx interface diffusion dominated the mass transport. In this case, the EM

lifetime degraded by half for each new generation due to the geometrical scaling of the critical void size[5]. The continuous degradation of EM reliability has stimulated extensive studies in strengthening the cap interface by various methods, including the use of a metal cap (CoWP, CoSnP, Ta)[7-9] or a surface alloy (Al) layer[9] before the SiNx cap deposition. Two orders of magnitude of improvement in EM lifetime have been demonstrated by using the CoWP cap[7-9]. However, a recent study showed that the Cu grain structures were no longer bamboo-like when the Cu line width scaled down to 90 nm[10]. Line sections of polycrystalline structures were observed, especially at the trench bottom. As scaling continues, the Cu trench aspect ratio and the surface to volume ratio continue to increase, thus it becomes increasingly difficult to completely fill the Cu trench and to obtain bamboo-like structures. This raises an interesting and important question regarding the effect of grain structure on EM reliability for future technology even with the implementation of metal cap layer.

In this paper, we first investigated the effects of grain size on EM lifetime and failure modes for both standard SiCN cap and strengthened metal cap (CoWP) by performing package-level accelerated tests. Then, a statistical simulation of EM lifetimes was performed to study the grain size effects for various interface strengths. The grain structures used in this model were generated by a Monte Carlo simulation on grain growth.

EXPERIMENTS: GRAIN SIZE AND CAP LAYER EFFECTS ON EM LIFETIME AND FAILURE MODES

Experimental Details

The test structure used for this study was a single-linked EM structure consisting of three-level interconnects as shown in Fig. 1. The dimensions of the M2 test line were 72 nm wide, 144 nm thick and 200 um long. The M1 and M3 feeder lines were made wider to minimize the EM failure probability in these lines. The test structures were fabricated using the standard damascene process. The Cu lines and vias were surrounded by Ta-based liners at the bottom and the sidewalls, and were coated with low dielectric SiCN cap on the top. For the M2 test line, two different grain sizes, large grain (LG) and small grain (SG), were obtained by changing the process parameters during electroplating. Two types of cap layers, SiCN with and without a CoWP layer, were applied to the M2 Cu line. Later in this paper, we quoted it as SiCN cap and CoWP cap, respectively. In this way, four sets of test structures were obtained and compared: Cu lines of LG/SG structures with SiCN/CoWP caps.

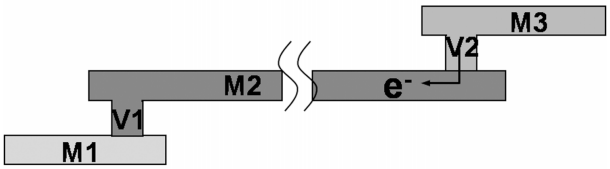

FIGURE 1. Schematic diagram of three-level interconnect EM test structure. M2 line is the test line.

Package level EM tests were performed in a vacuum chamber with a current density of 1.03 MA/cm^2 and test temperature of 330 ^{o}C. The DC current flew downward from the M3 level to the M2 level. EM lifetimes were determined at a fixed proportion of resistance increase (10%). Failure analysis was performed afterwards by using dual-beam focused ion beam/scanning electron microscopy (FIB/SEM) and transmission electron microscopy (TEM).

Microstructure Characterization

Figure 2 shows the longitudinal TEM images of the M2 line with LG and SG structures, and the results of grain size analysis were summarized in Table 1. The results clearly showed the difference in these two types of grain structures. The LG structure revealed a larger average grain size at the trench top (~215 nm) than at the trench bottom (~181 nm), which was consistent with the previous results reporting more small grain agglomerations at the trench bottom in dual damascene Cu lines narrower than 90 nm[10]. However, for the SG structure, the average grain sizes at the trench top (~123 nm) and bottom (~126 nm) were comparable, and both were significantly smaller than those of the LG structure.

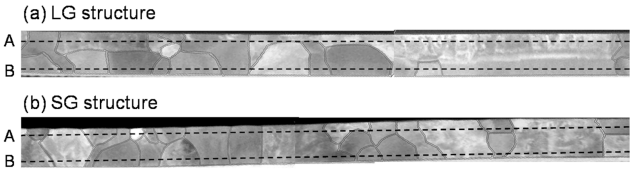

FIGURE 2. Longitudinal TEM images of Cu interconnects with two different grain sizes: a) LG structure, b) SG structure.

TABLE 1. Average grain size for large and small grain structures along the lines A and B in Fig. 2. The grain size was calculated by averaging along the dashed line.

Grain Structure	Average Grain Size Along Line A (nm)	Average Grain Size Along Line B (nm)
Large Grain	215	181
Small Grain	123	126

Electromigration Lifetime and Failure Analysis

Figure 3 plots the EM test results for the four sets of test structures described above. The cap layer and grain size effects can be clearly observed from the EM lifetime distribution. First, compared with the SiCN cap, the CoWP capped structures show a significantly improved EM lifetime. For the LG and SG structures, the improvement is over 100x and ~24x, respectively. This improvement in EM lifetime for the CoWP cap can be attributed to the reduction in Cu/cap interface diffusion, which could result from the highly ordered crystalline interface between Cu and CoWP[9], as well as the much higher bonding strength between Cu to Co compared

with Cu to amorphous SiCN[11]. The difference in the interface crystalline quality was demonstrated in Fig. 4 by performing high resolution TEM (HR-TEM) analysis along the Cu/SiCN and Cu/CoWP interfaces. It can be seen that the Cu line has a sharp interface with the SiCN cap, which has no distinct crystalline features. In contrast, for the Cu/CoWP interface, almost perfect crystalline planes of Cu extend all the way through the CoWP metal cap with no distinguishable interface in between. Thus the Cu/CoWP interface is characterized by highly ordered crystalline structures with good bonding strength to suppress the interface diffusion. This result supports the observation of highly disordered Cu/SiN_x interfaces and highly ordered, dominantly metallic bonding Cu/Co interfaces[12]. The EM lifetime improvement by using the CoWP cap observed in this study is consistent with the results reported previously[7, 8, 13].

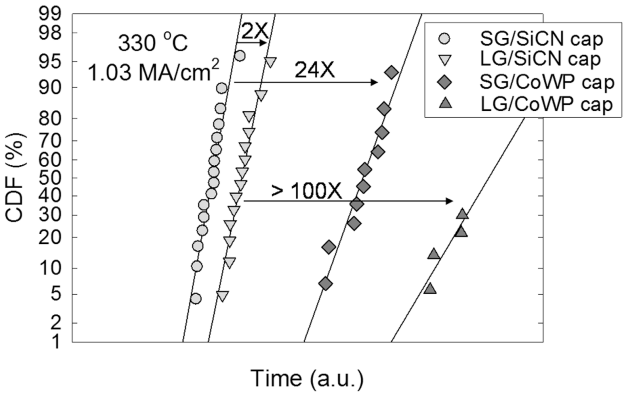

FIGURE 3. Cumulative distribution function (CDF) plots of four sets of Cu interconnects: LG/SG structures with SiCN/CoWP caps. EM tests were performed at 330 °C and 1.03 MA/cm^2.

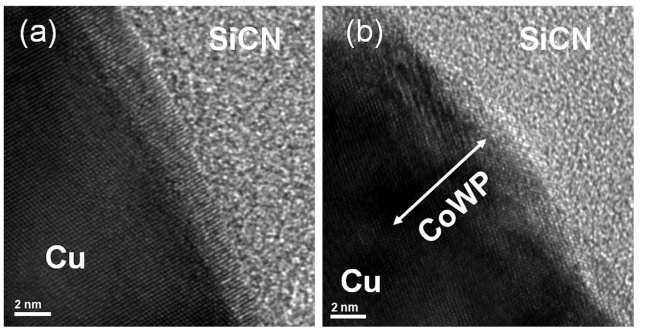

FIGURE 4. HR-TEM images of different Cu/cap interfaces: (a) SiCN cap and (b) CoWP cap.

In addition, the results showed a clear grain size effect on EM lifetime for both cap layers. For the SiCN cap, the EM lifetime degraded by half when changing from LG to SG structure. This effect became more significant for the CoWP cap, for which, the EM lifetime degraded to about one fifth of the LG structure. The degradation in EM

lifetime of the SG structure is due to the additional grain boundary diffusion contribution to the mass transport. Previous studies showed that for very weak interfaces, the interface diffusivity is much larger than that of the grain boundary diffusion. In this case, the grain size effect on EM lifetime can be neglected even for the polycrystalline structure[3, 4]. However, when the Cu/cap interface strength is improved, the grain size effect becomes more evident. Furthermore, when the cap interface is further strengthened by the metal cap, the interface diffusion is markedly suppressed so that it contributes little to the atomic transport. The grain structure then plays a dominant role in controlling the mass transport and in turn the EM reliability.

Postmortem failure analysis was performed on FIB cross-sectioned failure samples by SEM and TEM observations. For SiCN capped samples, two failure modes were observed as manifested by different initial resistance steps as shown in Fig. 5. Mode I failure showed a small initial resistance increase followed by a gradual resistance increase.

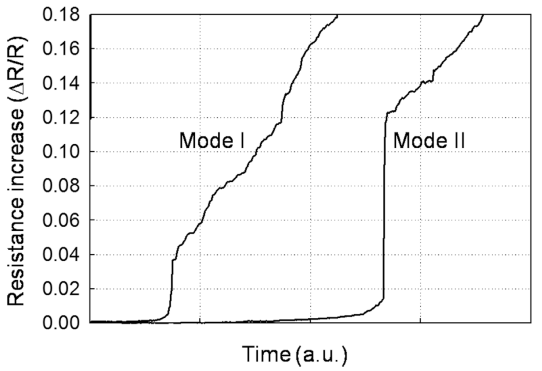

FIGURE 5. Typical resistance traces of mode I and mode II failures in SiCN capped samples: mode I with a small initial resistance step and mode II with a large initial resistance jump.

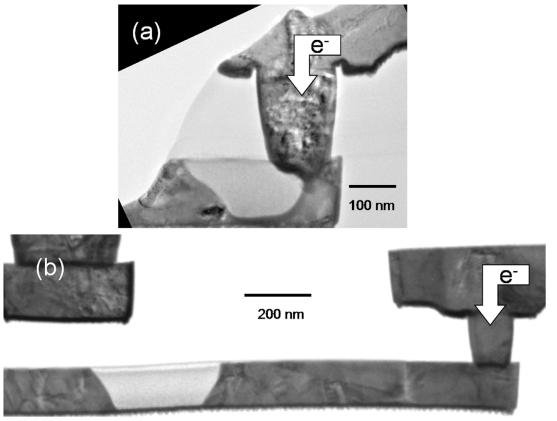

FIGURE 6. Cross-sectional TEM images of EM failed samples showing different voiding locations: (a) at the cathode via corner, (b) in the trench away from the cathode via, representing mode I and mode II failures in Fig. 5, respectively.

TEM images in Fig. 6(a) showed that mode I failure was due to void formation located at the cathode via corner. This often resulted from a small critical void size during EM failure, leading to a small initial resistance step. In comparison, the mode II failure showed a larger initial resistance jump, reflecting a larger critical void size to induce the EM failure. This mode was mostly due to void formation by mass depletion of individual grains in the M2 trench line located several microns away from the cathode via, as shown in Fig. 6(b). Overall, mode II failures demonstrated a longer EM lifetime as compared with mode I failures.

The different void locations for these two failure modes are attributed to two factors: one is the flux divergence sites where vacancy can agglomerate, the other is the effective diffusivity controlling void diffusion in Cu interconnects. During EM, Cu atoms diffuse along the electron flow direction driven by the momentum transfer due to scattering by the electrons. Voids form at flux divergence sites where there exist an unbalanced Cu flow rate, i.e., Cu atoms that come from the cathode end of the sites are less than those that diffuse away from the sites. For downstream EM, flux divergence sites can reside at the cathode via corner where the Ta barrier at the via bottom blocks the Cu atoms in the via from diffusing down to the trench line. Flux divergence sites can also occur at interface/grain boundary intersections due to either process defects or the grain texture induced interface diffusivity variations[14]. After voids nucleate at these flux divergence sites, they will evolve as current stressing continues in different ways. In some cases they can diffuse along the Cu line opposite to the electron current flow direction. Voids can change their shape and size during evolution. In other cases, voids will get trapped at these locations and then grow larger until failure occurs. This process of void evolution and growth is significantly affected by cap interface adhesion strength and Cu grain structures[14].

The failure modes of the four sets of structures were summarized in Fig. 7 together with their EM lifetimes. The EM lifetime increases from SiCN/SG, SiCN/LG to CoWP/SG, and CoWP/LG structures, corresponding to a combination of cap layer and grain structure changing from the weakest case to the strongest case. This is accompanied with a decrease in the proportion of mode I failures and an increase of mode II failures. The latter trend can be understood by considering the effective diffusivity difference in Cu interconnects considering contributions from both cap interface and grain boundary diffusions. For the SiCN cap, the cap interface diffusivity is large. Voids can readily move along the interface and eventually accumulate at the cathode via corner to fail the line. For the CoWP cap with significantly suppressed interface diffusion, voids can easily get trapped at locations with either an interface defect or a large grain triple junction, where the voids will grow further, leading to mode II failures. Similarly, compared with the SG structure, the LG structure reduces the grain boundary mass transport and the effective diffusivity for void diffusion. This will lead to void formation due to mass depletion at local grains and consequently making the Cu line more prone to mode II failures. The combination of these two factors, cap material and Cu grain size, shift the failure mode from mode I to mode II, yielding a superior EM performance for the CoWP capped LG structure.

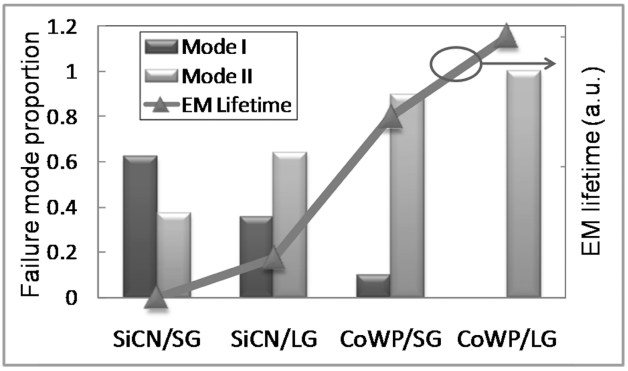

FIGURE 7. Comparison of failure mode proportions and relative EM lifetimes for M2 Cu interconnects with different cap layers and grain sizes.

SIMULATION: GRAIN SIZE AND CAP LAYER EFFECTS

The results so far showed a clear beneficial effect of using CoWP cap layer and large grains to improve the EM lifetime. The different failure modes observed revealed a complex process of void nucleation, diffusion and growth during EM failure. A simulation based on Cu grain structures generated by the Monte Carlo method was used to investigate the grain size and cap layer effects on EM reliability. In this model, the grain structures of the Cu lines were first generated by a Monte Carlo method. Then, the mass transport rates under EM along the interface and grain boundaries were modeled and the void growth was calculated at various sites of flux divergence. For each grain, the interface and grain boundary diffusivities were randomly selected within a specific range to model the statistical nature of grain and interfacial mass transport. Finally, the electrical resistance of the interconnect line during void growth was monitored and the EM lifetime was determined by a resistance increase criterion. The simulation was repeated for 100 Cu lines and the results were accumulated to yield EM statistics. Six cases were studied: Cu lines of small/large grains with strong, weak and weakest interfaces. For computational efficiency, small grains were selected with an average grain size of 35 units and large grains with a size of 45 units. These sizes were chosen so that a sufficient number of grains can be presented in the Cu line of 300 units in length and 100 units in thickness. The results presented here were obtained using a 2D model where more detailed description can be found elsewhere[15].

Figure 8 summarizes the simulation results of the six cases. Overall, a trend of increasing EM lifetime with decreasing interfacial diffusivity is clearly observed, which is consistent with the experimental observations. The effect of a strong cap interface for small grains with interfacial diffusivity suppressed from 400-500 to 1-10 yields an improvement of only ~4x in EM lifetime, considerably less than the ~24x improvement observed. Therefore, this simulation is best used for qualitatively interpretation of the cap layer effect on EM lifetime. The smaller EM lifetime improvement obtained in simulation is likely due to the fact that the Cu grain size used in the simulation is smaller than that in the real structure in order to save the

computation time. This will increase the contribution of grain boundary diffusion to the overall mass transport than in the actual experiments, thus diminish the benefit of interface strengthening of the CoWP cap. Interestingly, the overall grain size effect on EM lifetime becomes more evident for the stronger interface. This is consistent with our experimental results showing that when the Cu/cap interface diffusion is suppressed by the CoWP layer, it contributes little to the mass transport; consequently the change in the grain sizes can have a more significant effect on the overall EM reliability as compared with the standard SiCN cap.

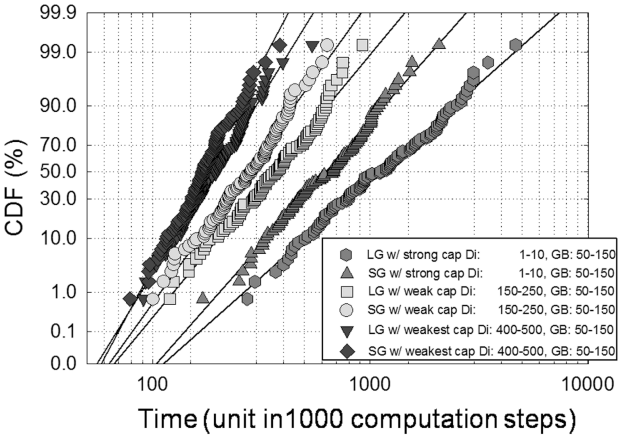

FIGURE 8. Simulated CDF plots of six cases for large and small grain interconnects with different cap layers.

CONCLUSION

The effects of grain size and cap layer on EM reliability were investigated by combining both statistical experimental study and Monte Carlo simulation. Downstream EM tests were performed on four sets of Cu interconnects: large/small grain structures with SiCN/CoWP caps. The CoWP cap was found to significantly improve the EM performance compared with the SiCN cap. In addition, LG structure showed a longer EM lifetime than the SG structure, particularly for the CoWP capped structures. Two failure modes were identified by distinct resistance traces and void locations. Mode I failures corresponded to a small initial resistance increase with void formed at the cathode via corner, while mode II failures corresponded to a large initial resistance increase with void formed several microns away from the cathode via. Overall, mode II failures corresponded to a longer EM lifetime. The proportion of mode II failures increased from SG to LG structure, from SiCN cap to CoWP cap. This can be understood by considering void nucleation and growth process and the effective diffusivity under EM. For SiCN interface, voids move readily along the cap interface and accumulate at the cathode via corner to cause the failure. In general, the SG structure provides more grain boundary diffusion paths to facilitate the void formation and agglomeration at the cathode via. On the contrary, for the metal cap

strengthened interface, the atomic diffusion along that interface is significantly suppressed. Consequently, voids can not move freely along the Cu line and become trapped at interface/grain boundary intersections.

The statistical simulation results of EM lifetimes are in good agreement with the experimental observations, which confirms the role of grain size and Cu/cap interface in controlling the EM performance. For the current technology node, the application of the CoWP metal cap seems to be able to meet the EM reliability requirements. With further scaling, however, the grain structure will degrade from bamboo-like to polycrystalline grain structures, it will be critical to control the Cu grain size and microstructure to ensure the EM performance for future technology node.

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