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Pseudo Pipelined SAR ADC with Regenerative Amplifier

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Pseudo Pipelined SAR ADC with Regenerative Amplifier

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Report

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Dedication

This work is dedicated to

my God, Jesus Christ, who gave me the gift of life and sustains me each day

my wife, Preethi Hannah, without whom I am incomplete

my parents, Mr. Prakasam and Mrs. Selvi, who have given up everything for me

my brother, Rufus Michael Gnana, without whom I would not have taken up this journey

my nephew/niece, who is on his/her journey into this world at the moment

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Thank you everyone for playing a part in my life. I hope to run a successful race with your help.

Abstract

Pseudo Pipelined SAR ADC with Regenerative Amplifier

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The power consumption of Analog to digital converters (ADCs) is an important design criterion in today's market of wireless and battery operated stand alone systems. Successive approximation register (SAR) ADCs do very well in this regard and have been designed with excellent figures of merit with respect to power. However, their speeds of operation are low. Pipelined ADCs have been known to do very well where speed and performance are important criteria. There have been multiple works where combinations of the two have been used in order to leverage on the benefits of each. This work explores the different options we have in implementing the residue amplifier in a two stage pipelined ADC. A linear op-amp is traditionally used to implement the residue amplifier. Integrators have been used for this purpose as well. This design takes it one step further and explores the feasibility of using positive feedback amplification in order to achieve the function of the residue amplifier. The challenges and concepts of this new design architecture are explored. A test chip will be fabricated with this design as well and its performance in silicon will be published at a later time.

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Chapter 1: Introduction

With power being an important concern in Analog To Digital Converters being designed today, we are driven towards discovering innovative methods to reduce power consumption in systems, while retaining their performance. SAR ADCs in particular have very good power efficiency. They are digital friendly and scaling down to lower technology node helps greatly in reducing their power consumption. The number of analog components in a SAR ADC is few, leading to an easier design process. SAR ADCs are especially power efficient for large input signals. Pipelined ADCs have good noise performance.

Adding pipelining to a SAR topology has a number of benefits. The conversion speed is increased due to the reduction in the size of the MSB capacitor. This reduces the DAC settling time. The total area comes down due to reduced total capacitance. The power consumption too goes down.

A paper has been published recently, which showcased a design with a good combination of the two ADCs and tries to attain an optimal noise and power performance [1]. This work inspired us to take the design a step further and replace the amplifier with a positive feedback regenerative amplifier. Our work in ADC design is the first of its kind where positive feedback amplification is used to achieve a fixed inter stage gain.

The innovation in this work lies in the use of a regenerative positive feedback, cross-coupled inverter, as an amplifier. In a typical pipelined ADC, we have a first stage ADC, followed by a residue gain amplifier and a second stage sub ADC. Traditionally, an amplifier in negative feedback is used to achieve the required gain. A novel idea is to replace this amplifier with a cross-coupled inverter latch and time the positive feedback

with a programmable pulse to achieve the same gain. We also know that a positive feedback system has an exponential output response and is the quickest way to amplify the input. Therefore, we might experience speed benefits during the amplification stage.

We will first study the latch in detail and try to see if there are any major concerns in using it as an amplifier. Linearity would be an important concern that we would spend a lot of time on. Once this is done, we will use the knowledge we obtain to design an ADC, which uses this latch as a residue amplifier.

Chapter 2: Latch

This chapter focuses on the study of the characteristics of the latch amplifier, that is a central part of this design. We will first look at different architectures of the latch in brief. Once we decide on a particular architecture for the latch, we will go ahead and analyze it more detail and how it fits into our ADC from a system perspective.

2.1 LATCH ARCHITECTURE

There are a couple of architectures that were considered for implementing the positive feedback amplifier.

- Cross coupled inverter latch
- Strong arm latch

Both these architecture have their own features that are explored in the following sections.

2.1.1 Strong Arm Latch

A strong-arm latch works in two stages. The first stage is an integration step where the output falls till the pmos transistors switch ON. The second stage is the positive feedback amplification stage where the differential signal is amplified exponentially. Therefore, the overall response time is slower as compared to a purely exponential response.

The strong-arm latch has different set of nodes for the input and output. The two stages would thus be decoupled from each other and we would obtain the benefits of

pipelining. The two stages can function in parallel and this helps in boosting up the speed of the conversion.

There happens to be a critical tradeoff between linearity and gain of the amplifier. In order to improve the linearity of the amplifier, the input supplied to it needs to be small so as to satisfy the small signal approximation. In order to have a small residue, we would have to increase the resolution of the first stage. However, the gain required of the residue amplifier depends on the resolution of the first stage. The higher the resolution of the first stage, the more amount of gain you would need.

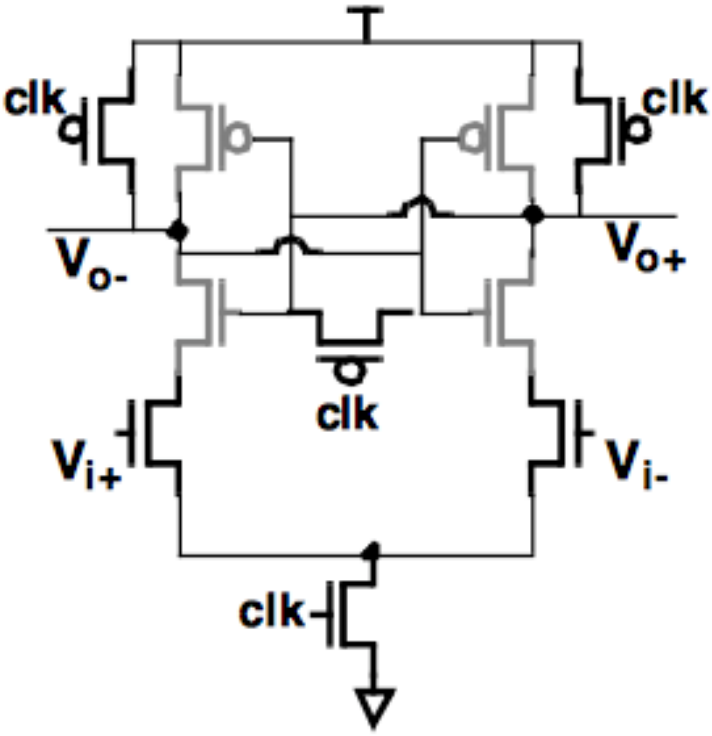

Figure 1: Strong Arm Latch Circuit

2.1.2 Cross coupled Inverter Latch

The cross-coupled inverter latch is a novel method of implementing the inter stage gain. One of the main differences is that output starts exponentially gaining up the input right from the beginning of amplification. Hence, for the same size, the response time is faster as compared to the strong-arm latch.

One of the unique features of the cross-coupled inverter latch is that it shares the same input and output nodes and hence, the two stages are coupled to each other. We lose the advantage of pipelining, as both the stages have to function in sequential fashion. Even if the latch works faster due to its exponential response time, the speed advantage we get, is probably counter productive due to the loss of the pipelining advantage.

However, the pipelining does help in reducing the MSB capacitor size and the total size of the capacitive DAC as compared to its single stage SAR ADC counterpart. Hence, pipelining with a cross coupled inverter latch as the gain amplifier is not without its advantages.

Also, as it will be shown in this work, the gain requirement on the amplifier is much lesser because of this coupling. Some interesting properties of this system helps us to develop certain architectures that help in amplifier gain reduction.

Moreover, using the cross coupled inverter as an amplifier is a novel approach and has not been explored to the best of our knowledge. For all these reasons, we will therefore be using the cross-coupled inverter latch as a residue amplifier in this design.

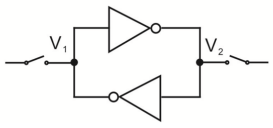

Figure 2: Cross coupled inverter latch

2.2 LATCH LINEARITY

The linearity of the latch is an important factor that influences the budgeting and partitioning of our design. The residue at the end of the first stage needs to be amplified and then converted by the second stage. This amplification needs to conserve the linearity of the input. The non-linearity of this operation imposes a limitation on how many effective bits we will be able to resolve in the second stage. The linearity can be measured by studying the variation of gain for a wide range of input voltages.

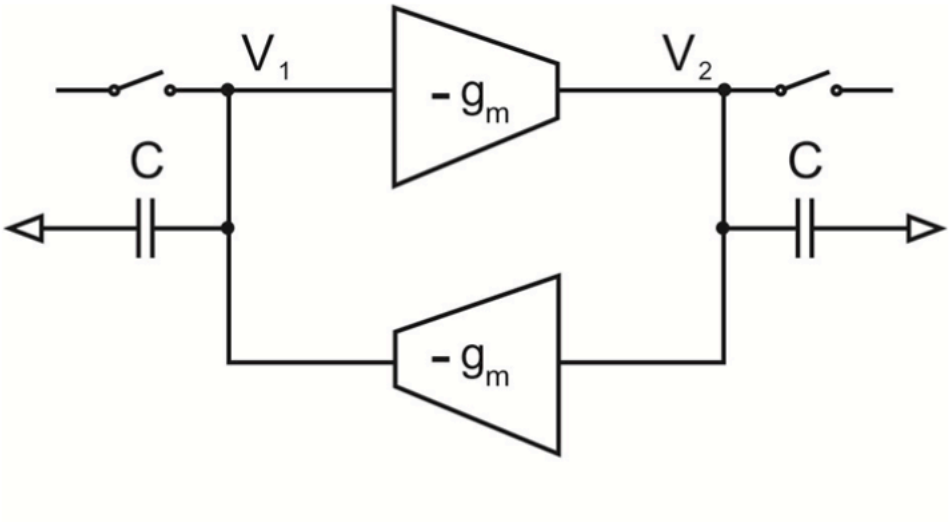

Figure 3: Small signal model of the cross coupled inverter latch

The exponential response of the latch is given by the following equation

$$V_{FINAL} = V_{INITIAL} * e^{\frac{T}{\tau}}$$

where,

$V_{INITIAL}$ = Initial voltage on the residue node

V_{FINAL} = Final voltage on the residue node

T = Time for which amplification takes place

$\tau = 1 / (G_M / C)$

G_M = Effective G_M of the latch

As seen from the equation, the voltage is being amplified exponentially and the rate of amplification depends on the time constant of the latch. The effective transconductance of the cross-coupled inverter latch is the product of the transconductances of the individual inverters.

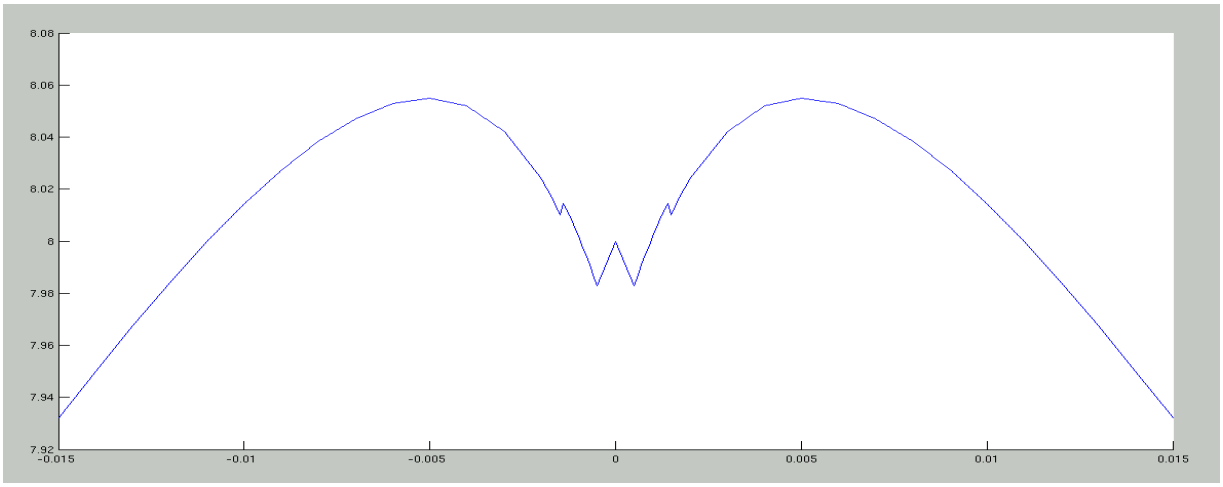

Figure 4: Variation of gain for different input voltages.

On analyzing Figure 1 closely, we see that the variation of the gain of the latch varies around 8. The variation of the gain is within 1.25%. The gain is lower when the input is lower and it reaches a peak around 5mV. And for inputs higher than that, the gain again begins to fall down. This graph can be explained by taking a look at the variation of transconductance of the two inverters.

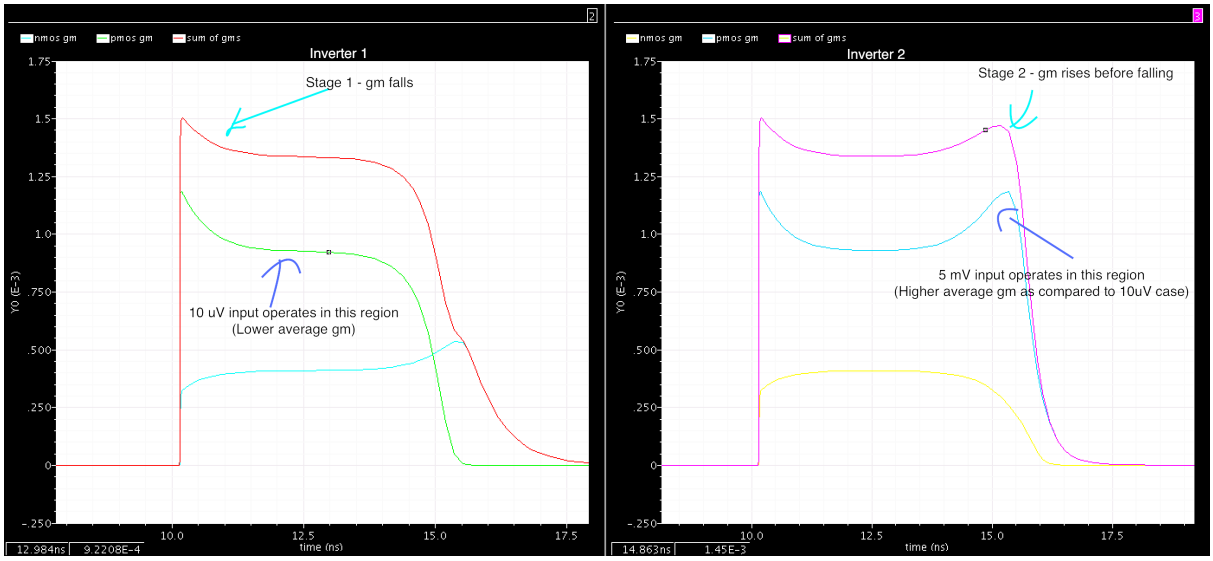

Figure 5: Variation of transconductance of the two inverters of the inverter pair

When the latch is operational, one of the outputs tends to go down and the other tends to go up immediately. This is under the assumption that the nmos and pmos transistors are perfectly balanced and therefore the integration step is negligible. During the variation of these voltages, the transconductance of the transistors varies too. Consider the nmos transistor whose gate voltage is growing and drain voltage is dropping. The increase in gate voltage tends to increase the transconductance of the device, while the fall in drain voltage tends to push the transistor from saturation region to linear region and hence, effectively reduce the transconductance. These two opposing

forces act at the same time. The second effect eventually wins and the transconductance falls. However, the transistor goes through an intermediate stage where the first effect is dominant. This reflects in the transconductance going through a peak before falling down to 0. It is this peak that results in an increase in the effective transconductance of the amplifier for certain values of the input and hence, a reduction in time constant of amplification. This results in an increase in gain for a given time period of amplification and leads to a peak in the gain curve for different input voltages.

This graph on linearity can be used to predict the effective resolution of the second stage. The following tables shows the linearity required for different resolutions of the second stage.

Second Stage Resolution	Linearity
1	50.00 %
2	25.00 %
3	12.50 %
4	6.25 %
5	3.12 %
6	1.56 %
7	0.78 %
8	0.39 %
9	0.20 %

Table 1: Linearity requirement of amplifier based on second stage resolution

The linearity of the amplifier varies based on a number of factors –

- The size of the transistors
- The scaling factor between nmos and pmos transistor
- The output load
- The common mode voltage

A decision needs to be taken on the sizing of the latch based on design requirements and simulation results.

2.3 LATCH NOISE

It would be helpful to measure the input referred noise for varying parameters

- Size of the latch
- Gain

Here are the results obtained from a transient noise analysis. The numbers indicate the input referred noise of the latch.

Transistor Size	Sampling Noise	Gain = 4	Gain = 8	Gain = 16	Gain = 32	500 SAMPLES
N = 5	115.77uV	181.10uV	178.90uV	169.82uV	162.22uV	
N = 25	122.75uV	193.63uV	191.03uV	183.51uV	173.56uV	Switch Noise Enabled
Transistor Size	Sampling Noise	Gain = 4	Gain = 8	Gain = 16	Gain = 32	500 SAMPLES
N=5	0	134.93uV	135.67uV	129.37uV	123.59uV	
N=25	0	147.48uV	146.80uV	141.70uV	134.19uV	Switch Noise Disabled

Table 2: Noise analysis of the latch

We see that the noise is fairly invariant with the gain and the size of the transistor. However, it would be helpful to explain the minor variations.

2.3.1 Variation with Size

We see that for a larger transistor size, the effective noise is higher for the same gain. This is expected because a larger transistor contributes more noise power. Since the signal gain is essentially the same, the effective noise power is bound to go up.

An alternative way of looking at this is to look at it from the noise bandwidth perspective. As we size up the latch, the amplification becomes faster due to the increased transconductance. Therefore, a constant gain can be achieved in a shorter time. Therefore, a larger transistor latch integrates noise over a larger frequency range, hence resulting in more noise power.

2.3.2 Variation with Gain

With the increase in the gain of the latch, the noise power reduces. This can again be explained in terms of the noise bandwidth. In order to achieve a higher gain, we need to amplify for a longer time. This gives the noise a longer time to average out. Or in other words, the noise bandwidth becomes smaller. This results in the reduction of the effective noise at the output.

2.4 LATCH GAIN

Choosing a cross-coupled inverter latch for the residue amplifier has significant impact on the gain requirement. Traditionally, a pipelined ADC with N1 bits in the first stage and N2 bits in the second stage, would need a gain of 2^{N1} to bring up the residue voltage back to full scale. Having a large number of bits in the first stage would mean that the amplifier would have to provide for a lot of gain.

In the case of a cross-coupled inverter latch, on writing out the charge conservation equations, it can be shown that the gain of the amplifier is decided solely by the resolution of the second stage and is independent of the resolution of the first stage. Also, since the two stages are coupled together, one can play with the unit capacitances of the two stages to change the gain requirement. The gain requirement is given by the following equation.

$$G = 2^{N2} * \frac{C_{U2}}{C_{U1}}$$

where,

N2 = Resolution of the second stage

C_{U2} = Effective Unit capacitance of the second stage

C_{U1} = Effective Unit capacitance of the first stage

Effective unit capacitance for a stage is defined in the following manner.

$$C_U = \frac{C_{TOT}}{2^K}$$

where,

C_{TOT} = Total capacitance of the stage

K = Resolution of the stage in bits

It is useful to define an effective unit capacitance because the equation of the gain doesn't depend on the actual physical unit capacitance used in the stage. It also depends on the total capacitance of the stage. There are a number of switching schemes available that use different number of unit capacitances for the same resolution. This means that the choice of the switching scheme used also determines the gain requirement of the

amplifier. This is a critical difference as compared to the traditional pipelined scheme where the two stages are completely decoupled from each other.

We can make some basic inferences from this equation. For example, using a switching scheme with lower effective unit capacitance in the second stage and a higher effective unit capacitance in the first stage is going to reduce the gain requirements and hence relax the linearity requirements on the amplifier.

Finally, the gain requirement can be further reduced by a factor of 2 by adding gain redundancy between the stages. This also helps in adding offset correction to the design.

2.5 LATCH OFFSET

The latch is bound to be sensitive to offset as well. The offset causes a common mode shift and this shift is bound to affect the performance of the latch.

	N2 (Second Stage) Achievable resolution			
Common mode shift	Gain = 4	Gain = 8	Gain = 16	Gain = 32
0 mV	12	9	7	5
3.5 mV	7	7	7	6
7 mV	6	6	6	9
14 mV	5	5	5	5
28 mV	4	4	3	4

*Data generated for N1 = 10 Bits

Table 3: Variation of the linearity of the latch with a common mode shift

Based on the partitioning of the design we choose, there would be a limit on the variation in common mode shift of the residue node, in order to preserve the linearity of the latch. This table would help us in determining that limit and designing our circuit appropriately.

2.6 LATCH TIMING

There are a number of ways to time the latch for a certain duration of time to achieve the necessary gain. The simplest way to do this is to add header and footer switches to the latch and time those switches to switch on the latch when needed. Care must be taken to ensure that such a scheme does not degrade the linearity of the design.

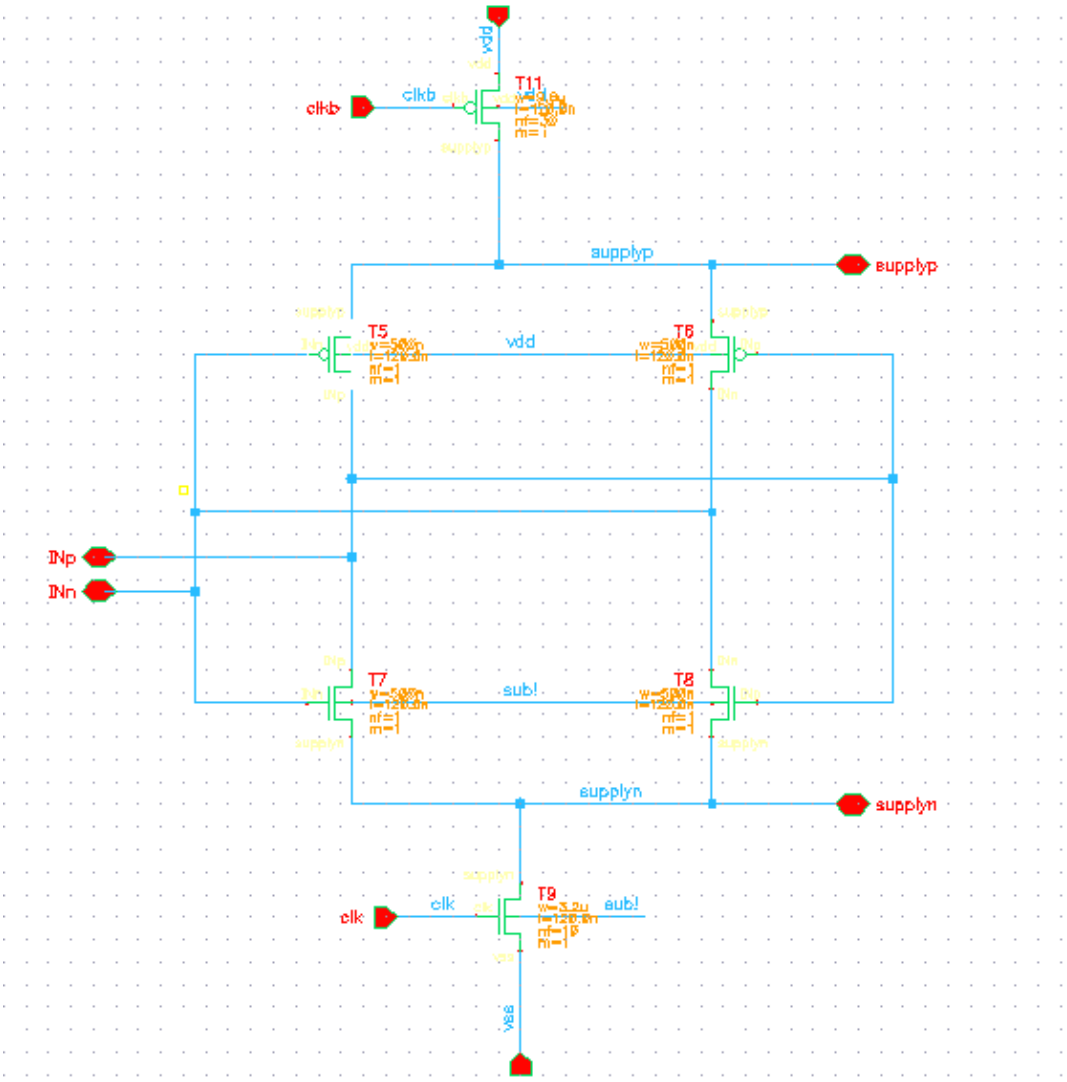

Figure 6: Timing the cross coupled inverter latch

Power switches are added to the cross-coupled inverter and are used to control the amplification time of the latch, we need to be aware that a lot of non-linearity is involved. Initially, the inverter pair is not charged and is left floating. The transistors are operating in the cutoff region. When you abruptly switch on the power gating switches, the source nodes of the transistors need to immediately charge up to the power rails. During this

time the transistors move from cut-off to saturation region. This is a non-linear operation. The amount of current taken to charge up all the parasitic capacitances and bring the transistors to saturation is an indication of how non-linear this operation is going to be.

Experimenting with various latch sizes, it was observed that larger latches tend to have lower linearity, provided the input voltage and the gain is kept constant. This was in line with our expectations. Larger latches have more parasitic capacitance and hence the non-linearity of the initial switching operation tends to be higher. We are therefore limited to using smaller latches in order to preserve the linearity constraints required by the second stage.

Another non-linearity to note is the input gate capacitance of the latch. Based on the switching scheme used in the DAC, the common mode voltage of the residue node could vary widely. If the latch nodes were directly connected to the residue nodes, the common mode variation would be experienced at the latch as well. The gate capacitance could vary significantly on both the nodes. This non-linearity will directly affect the residue node voltage and could skew decisions in the wrong direction.

In order to correct this effect, the latch is disconnected from the residue node when the common mode change is high and it is connected only when the common mode stabilizes. A switching scheme needs to be chosen such that the common mode stabilizes to V_{CM}, which would be the operational starting point of the cross-coupled inverter latch.

Chapter 3: Architecture

This work focuses on a two-stage implementation of a SAR ADC. The first stage resolves the MSB bits and leaves behind a residue that is amplified before being fed into the second stage. The second stage is a sub-ADC that resolves the LSB bits.

Important architectural decisions need to be taken before proceeding with the design of the ADC. The linearity of the positive feedback amplifier would be an important factor in determining the partitioning of the design. Other considerations include thermal noise.

Budgeting needs to be done for latch non-idealities, comparator non-idealities, quantization noise and thermal noise. Having a reasonable idea of numbers for each of them would help us in determining our target ENOB.

3.1 SWITCHING SCHEME

We have a number of switching schemes available. Conventional switching scheme is the basic scheme. It's advantages include a constant common mode voltage. However, it consumes a lot of power. The split capacitor scheme achieves savings in switching energy as compared to the conventional scheme. V_{CM} based switching methods are also available. Monotonic switching schemes help in saving power with the cost of changing common mode. Finally, bidirectional single sided switching technique saves power and at the same time reduces the common mode variation seen in the monotonic switching scheme. It also ensures zero switching energy in the first two cycles.

Choosing the right switching scheme is going to affect the gain requirements on the latch and is hence a critical decision to be made. We are going to consider four schemes here. They are as follows –

- Conventional
- Monotonic [7]
- Bidirectional Single Sided Switching Technique (BSSST) [2]-[5]
- Bidirectional Single Sided Switching Technique without V_{CM} application ($BSSST^{M}$)

$BSSST^{M}$ is a technique where the final bit is not applied through a V_{CM} reference voltage, as is typical with BSSST.

Let us calculate the effective unit capacitance for each of these schemes based on the equation given in the Section 2.4. We need to remember that the unit capacitances will vary based on whether the switching scheme is being used for the first stage or the second stage. The reason is because, in the first stage, it is not enough to make N decision bits, but all the decisions need to be fed back through the DAC in order to create the right residue voltage that can be used by the second stage. On the other hand, in the second stage, the last bit decision need not be fed back through the DAC since we need not make another decision. The following table shows the effective unit capacitance in both the schemes based on the stage they are used in.

Switching Scheme	Effective Unit Capacitance	
	First Stage	Second Stage
Conventional	$2*C_U$	C_U
Monotonic	C_U	$C_U/2$
BSSST	$C_U/2$	$C_U/4$
$BSSST^M$	C_U	$C_U/2$

Table 4: Effective unit capacitance of different switching schemes

Note that C_U is the physical unit capacitance used in a scheme.

We can see that the first stage tends to have a higher unit capacitance by a factor of 2, as compared to the second stage due to the additional bit that needs to be fed back in through the DAC. In order to reduce the gain requirements on the latch, we know that we need to choose a switching scheme with a high effective unit capacitance in the first stage and a low effective unit capacitance in the second stage. From this table, we can see that the best possible way to do this is to use the following combinations

- Monotonic (Stage 1) + BSSST (Stage 2)
- $BSSST^M$ (Stage 1) + BSSST (Stage 2)

Both these choices of switching schemes help in reducing the overall gain requirement on the latch by a factor of 4. This is significant savings and eases the burden on the design of the amplifier. $BSSST^M$ is a better scheme than monotonic because of its low switching power and smaller change in common mode voltage. The common mode voltage in $BSSST^M$ starts at V_{CM} and ends at V_{CM}. However, in the monotonic switching scheme, the common mode varies a lot. $BSSST^M$ has lesser dynamic offset as compared to monotonic. We therefore choose $BSSST^M$ over monotonic in this design. Having one

bit of gain redundancy between the stages is going to reduce the gain requirement even further. Therefore maximum gain reduction of 8X has been achieved in this design.

The final choice is to use BSSST^{M} for the first stage and BSSST for the second stage.

3.2 PARTITIONING

The number of bits for each stage needs to be allocated. Linearity of the amplifier and thermal noise are important considerations that help you partition the design appropriately.

3.2.1 Latch Linearity

The linearity of the latch for various input voltages was plotted in Section 2.2. The resolution of the first stage determines the size of the residue for amplification. The linearity of the latch for that residue then helps in determining the maximum resolution of the second stage. Here are some possible partitioning schemes that can be used for a given size of the latch.

	Resolution Configurations				
Size	N1 (First Stage)	N2 (Second Stage) Achievable Resolution			
		Gain = 4	Gain = 8	Gain = 16	Gain = 32
N = 1	10	12	10	7	5
	9	11	8	5	4
	8	9	6	4	2
	7	7	4	2	1

Table 5: Achievable second stage resolution for varying configurations

It is evident from the table that the achievable resolution in the second stage reduces as the resolution of the first stage increases. This is because the residue increases. With a large first stage residue, the latch deviates further away from the small signal approximation and linearity takes a dip. In order to maximize the linearity of the latch, we need to increase the resolution of the first stage. However, increasing the resolution also increases the MSB capacitor and hence the speed reduces.

Also, it can be seen that with the increase in gain of the latch, the linearity obtained from the amplifier reduces. This is expected as well. With larger gain, the signal tends to towards large signal characteristics and linearity takes a hit. It is advantageous to reduce the gain in order to improve the performance of the latch. This is why it is essential that we try to reduce the gain requirement. As discussed in a Section 3.1, we can achieve up to 8X reduction in gain requirement by adding redundancy between the stages and choosing the right switching scheme for both stages.

3.2.2 Noise

Thermal noise is an important consideration when we try to partition the design. The noise power is inversely proportional to the capacitance (kT/C). The first stage capacitance onto which the input is sampled solely contributes to the thermal noise of the design. The additional parasitics and the second stage capacitance, even though is connected to the same residue nodes, do not contribute to the reduction in kT/C noise. Therefore, the amount of sampling capacitance you dedicate to the first stage is a very critical factor in determining thermal noise. The following table gives an indication of how much thermal noise is expected in the design for various partitions. The unit

capacitance assumed for implementation is 3.3fF. The overall resolution is assumed to be 13 bits.

ADC Resolution	First Stage Resolution	Second Stage Resolution	Total Sampling Capacitance (pF)	Noise Power (uVrms)
13	12	1	13.5	17.40
13	11	2	6.8	24.61
13	10	3	3.4	34.81
13	9	4	1.7	49.23
13	8	5	0.8	69.63
13	7	6	0.4	98.47
13	6	7	0.2	139.26
13	5	8	0.1	196.94
13	4	9	0.05	278.52
13	3	10	0.025	393.89

Table 6: Noise Power of ADC for different partitioning choices

On observing the table closely we see that partitioning more number of bits to the first stage can reduce the noise power. However, partitioning too many bits to the first stage would increase the MSB capacitance and thus, increase the DAC settling time. The conversion speed of the ADC would reduce.

Partitioning too few bits to the first stage could lead to excessive noise that is going to dominate over quantization noise and other non-idealities. That would also reduce the effective ENOB of our ADC.

The optimal partitioning choice needs to be reached at considering all parameters in the design.

3.3 BUDGETS

Our target for this design is going to be a 12-bit ADC. In order to achieve a final noise performance of 12 bits, we need to design a 13-bit ADC. The supply and reference voltage used is going to be 1.2V. The technology used has 130nm minimum channel length.

Our total noise power budget can be calculated to be 169 uVrms. This corresponds to the final ENOB of 12 bits.

Quantization noise can be calculated corresponding to the 13-bit resolution. This is 84.57 uVrms.

The remaining noise power needs to be allocated to the comparator noise, latch noise and thermal noise. Amount of budget available for all these noise sources can be calculated from the total noise budget and the quantization noise power, assuming them to be independent. The budget for these noise sources is 146.3 uV. This means that the first stage resolution needs to be greater than or equal to 7 bits (refer table).

Let us start off by assuming a 7 + 6 bit split up between the two stages. This kind of partitioning should help us meet the thermal noise requirements for a 13-bit ADC. Let us now look at the linearity of the latch amplifier for the residue of a 7 bit first stage ADC. Referring to table, we can see that this is kind of linearity can only be achieved for a gain of 4. For higher gains, the linearity is low and the error is going to be too high for a 6 bit second stage. Therefore, this configuration is not possible.

Our next step is to assume an 8 + 5 bit split up between the two stages. Again, this kind of partitioning should help us in meeting the thermal noise requirement. Using table to check the linearity of the amplifier at this residue, we see that we can achieve upto 6 bits of resolution in the second stage with a gain of 8.

This seems to be a more reasonable configuration. Taking into account our discussion in Section 2.4, the interstage gain depends solely on the second stage. In order to achieve 6 bits in the second stage we would require a gain of 2^6 or 64. Recalling Section 3.1, we see that we can reduce the gain by a factor of 8. Therefore, our final gain requirement is only 8. This matches well with the linearity of the amplifier.

Therefore, it seems reasonable to choose an 8 + 5 (or 6) split up between the two stages. This configuration satisfies thermal noise and linearity limitations. The extra bit in the second stage can be used for gain redundancy.

3.4 REDUNDANCY

There are two types of redundancy that can be exploited. The first is capacitance redundancy. This can be added in the first stage in order to restore the residue back to the correct limits, in case a wrong decision was made somewhere along the line. A decision needs to be taken as to where this redundancy needs to be added. Adding it closer to the MSB bit will help you correct a greater error. However, it will only be able to correct errors in the MSB bits that come before it. Adding it later in the flow helps you correct for errors that could have happened over a wide range of bits. In this design, capacitance redundancy was added in the third LSB bit of the first stage. Therefore, the first stage has 9 bits of resolution with an effective resolution of 8 bits.

The second type of redundancy that is exploited in this design is gain redundancy between the two stages. This redundancy helps in correcting for offset errors in the comparator and latch.

Chapter 4: Implementation

This chapter will show all the efforts taken to implement the idea showcased so far. At first, the proof of concept was obtained by using ideal blocks and ensuring that the ADC was working and its performance was up to mark. The only non-ideal component at this stage was the latch. The second stage involved a transistor level design and all the ideal blocks were replaced by transistors level implementation. The third and final stage involved designing the layouts for each of the blocks and putting them all together and getting it ready for tapeout. Calibration will be added at this stage as well to correct for offset errors [6].

Here is a brief description of the different blocks used in the design.

4.1 BLOCKS

4.1.1 Capacitive DAC

This block consists of a series of scaled capacitances that feed back each of the ADC decisions back to the residue node so that the next decision can be made. The switches feeding the reference voltages to the capacitances need to be appropriately sized based on the size of the capacitance. This ensures that the DAC settling time is well within our design limits.

The layout of the DAC is an important aspect of the design. Access needed to be provided to the capacitances from all four directions and it was pretty challenging to reduce the cross coupling capacitance and improve the matching between different bits.

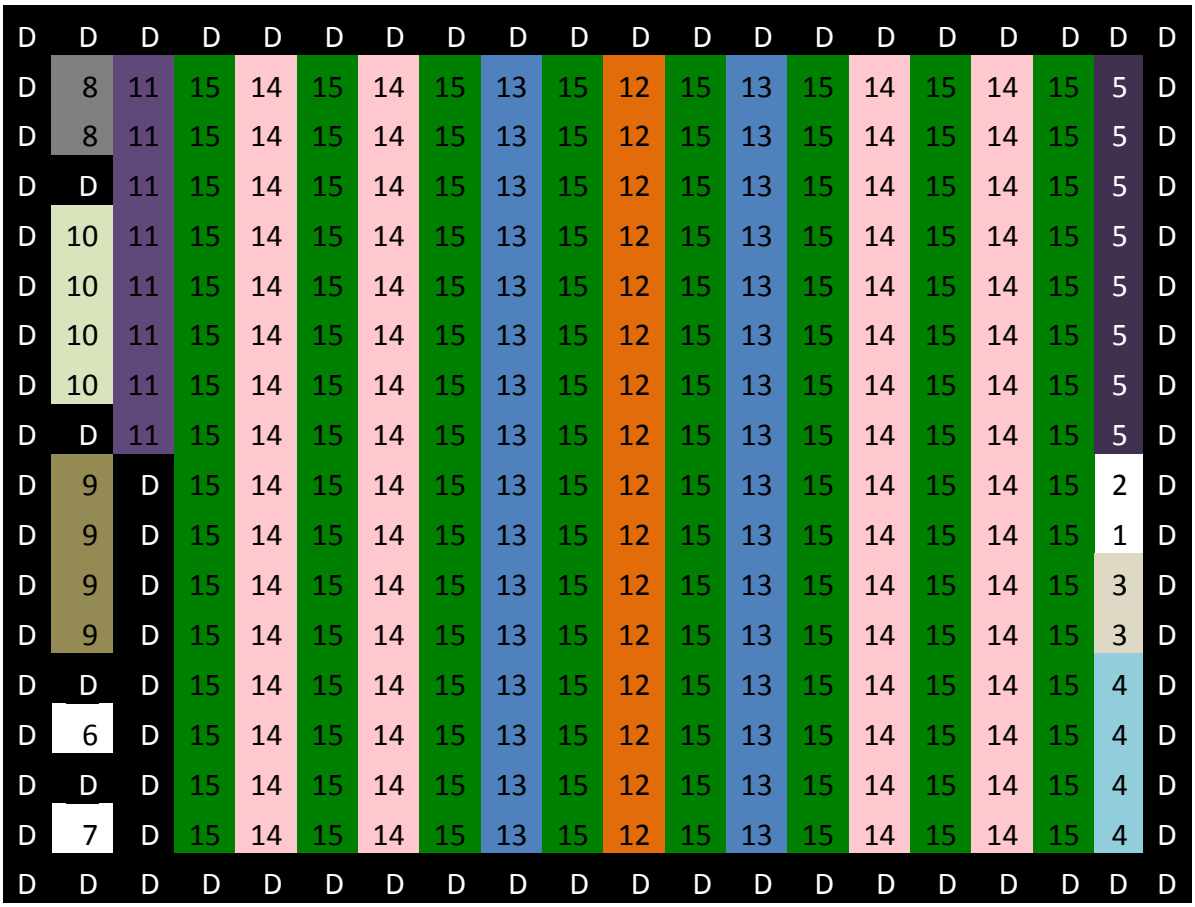

Figure 7: Placement of unit capacitors of capacitive DAC

Legend	Identifier	Number of Occurences
Stage 1		
BIT 9	15	128
BIT 8	14	64
BIT 7	13	32
BIT 6	12	16
BIT 5	11	8
BIT 4	10	4
BIT 3	9	4
BIT 2	8	2
BIT1	7	1
LSB	6	1
Stage 2		
BIT 6	5	8
BIT 5	4	4
BIT 4	3	2
BIT 3	2	1
BIT 2	1	1
DUMMY	D	84

Table 7: Legend for placement of unit capacitors of capacitive DAC

The switching scheme used for the first stage was Bi Directional Single Sided Switching without V_{CM} application and the scheme used for the second stage was Bi Directional Single Sided Switching with V_{CM} application. Therefore, the common mode voltage starts off at V_{CM} at the beginning of conversion and ends up at V_{CM} at the end of conversion as well. The MSB bits were set to 0 and all the other bits were set to 1. This means that in the first conversion cycle, the common mode would go up from V_{CM} to 1.5* V_{CM} and then gradually decrease to V_{CM} in the subsequent steps.

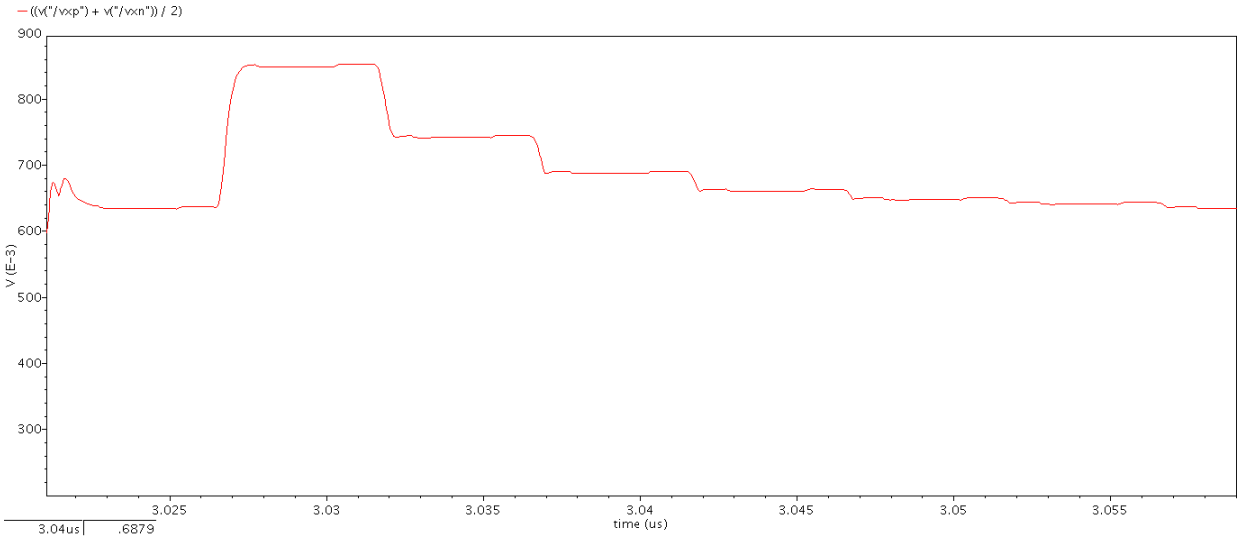

Figure 8: Variation of common mode voltage with each conversion step

4.1.2 Comparator

A strong-arm latch was used as a comparator. NMOS transistors are used for the input pair because the common mode voltage varies between V_{CM} and 1.5 V_{CM}.

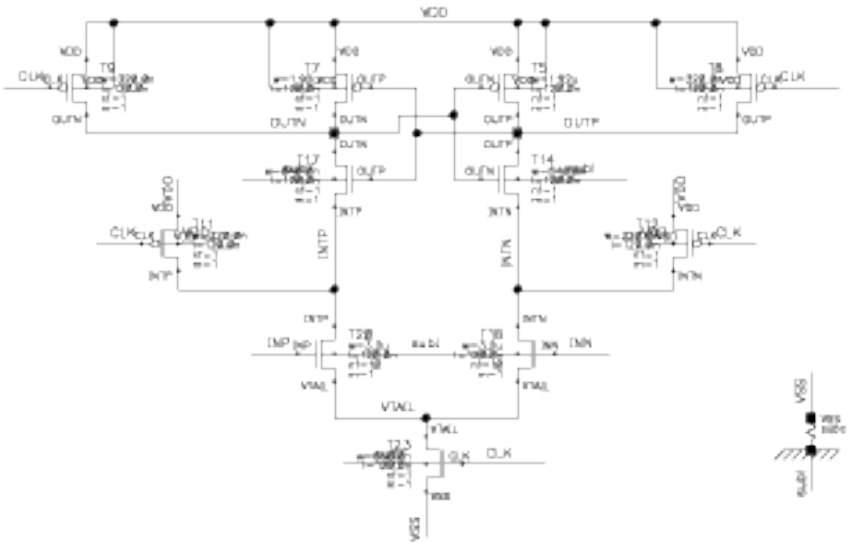

Figure 9: Comparator schematic

4.1.3 Latch

The design of the latch was discussed in detail in the Chapter 2. The main design consideration for the latch is the linearity.

In order to shield the varying gate capacitance of the latch from the residue node, switches are added to time the connection of the latch when the common mode has more or less settled. An interesting phenomenon was observed when designing these switches. It was observed that the amplification at the residue node due to the latch was slower when you use bigger switches.

Intuitively, you would expect the response time to be better when you use bigger switches. The reason for this is that bigger switches have lower resistance and the DAC capacitance is better connected to the nodes being amplified. Using a smaller switch would increase the resistance and make it harder for the latch to amplify the residue node.

The observed effect can be explained through the means of resistive shielding. When the switch is bigger, the resistance is smaller. This means that most of the DAC capacitance is seen at the latch output nodes. The DAC capacitance is huge compared to the parasitic capacitance of the latch. Therefore, the time constant of amplification for the positive feedback system increases and the amplification becomes slower. On using smaller switches, the entire DAC capacitance is resistively shielded from the latch amplification nodes. This drastically improves the speed.

We see that there are two opposite effects at work here. High resistance of the switches could either speed up or slow down the amplification depending on which effect is dominant. It was observed through simulations that the resistive shielding effect was in fact more dominant. This meant that using a smaller switch improved the response time.

However, it is not a very good idea to use smaller switches. The reason for this is that the parasitic capacitance at the latch output nodes would dominate the load seen by the latch. This would make the response of the latch unpredictable after fabrication.

Another point to note is that using a large transmission gate as a switch is going to add additional capacitance on the latch output nodes. As was discussed in Section 2.5, we are restricted to use small latches to preserve the linearity. Therefore, any additional parasitic load at the latch node is going to be detrimental to the speed. A transmission gate has a NMOS and PMOS transistor connected in parallel. The PMOS transistor is scaled up compared to the NMOS and is the main contributor to the parasitic capacitance. A way to fix this issue is to use just a NMOS transistor as a switch and provide more time for the charging up of the latch nodes. Experiments showed that using a NMOS transistor was actually more beneficial from a speed perspective as compared to using a transmission gate.

4.1.4 Digital Logic

The digital logic used in this design is pretty straightforward and is commonly used in a SAR ADC. It consists of a shift register that is used to generate the clock for capturing different bits. The shift register feeds to an array of NMOS latches whose structure is very similar to the comparator used in this design. The property of the latch of having both outputs high when reset and having a high and low output when clocked with an input, is ideal for our switching scheme. In the bidirectional single sided switching scheme, both the sides of DAC are driven to the same voltage. When each decision is made, one side of the DAC output switches. Therefore, the DAC works well with the latch control bits.

4.1.5 Clock Generator

There are four important clocks that need to be generated for this design. They are listed as follows.

- clkC – Master Clock
- clkS1 – Sampling clock
- clkAMP – Amplification clock
- clkConnect – Clock that connects the residue node to the latch nodes

The master clock is used to generate all the other clocks in the design. It is the highest frequency clock.

The sampling clock spans about 2.5 cycles of the master clock. This is the clock cycle where the input is sampled onto the DAC capacitance that also acts as an inherent sample and hold.

The amplification clock is timed once the first stage conversion is completed. This clock controls the header and footer power switches of the cross-coupled inverter

latch. Current starved inverters are used to control the duration of the pulse. The amplification clock consists of a fixed delay equal to one clock cycle of the master clock and a variable delay that can be controlled by a differential voltage given by the user from the external world. This variability is needed because the amplification time will depend on the fabricated parameters. The maximum budget for the amplification clock is two and a half clock cycles.

The connect clock is used to connect the latch nodes to the residue nodes to shield it from the non-linear gate capacitance. It is switched ON a cycle before the amplification clock and is switched OFF a cycle after the amplification clock dies down.

4.2 SIMULATION RESULTS

The design is completed with complete schematics and we have achieved upto 13 bits of ENOB on the design. Setting out the layout of the design is in progress and is in schedule for the tapeout. The following results are from the complete schematic version of the circuit and there are no ideal circuit components.

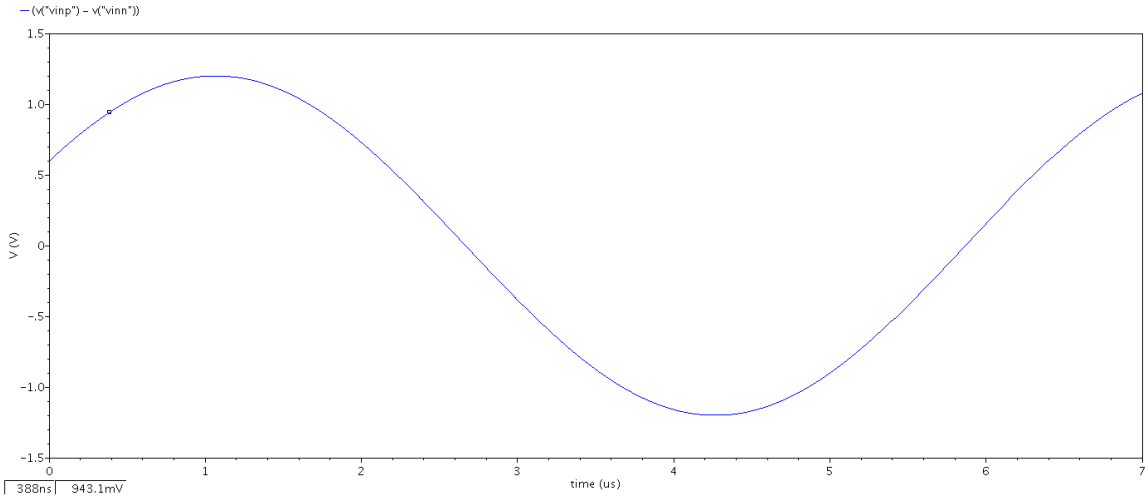

Figure 10: Input voltage applied to the ADC

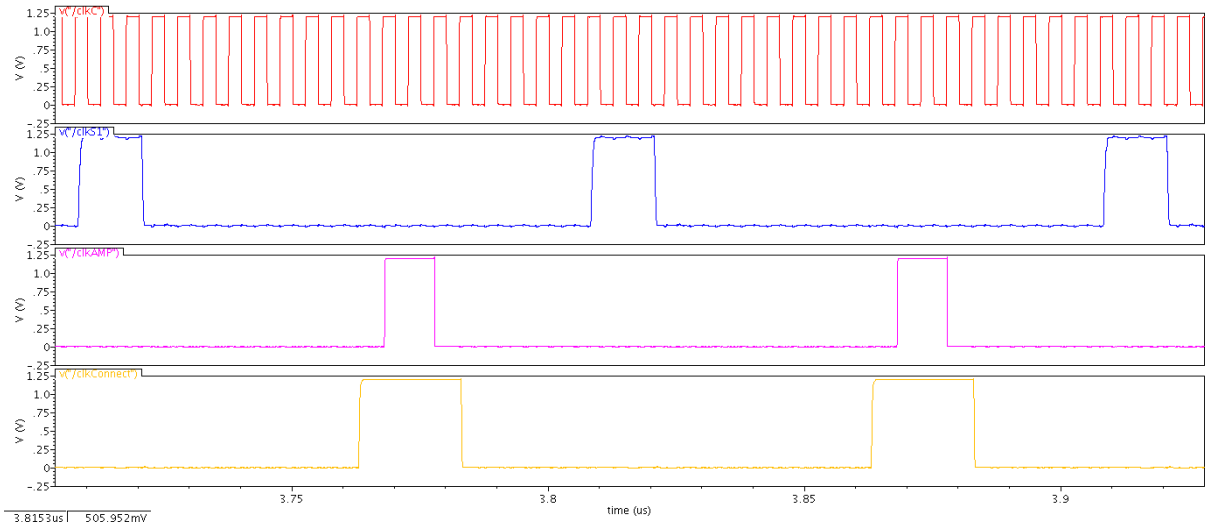

Figure 11: The four main clocks

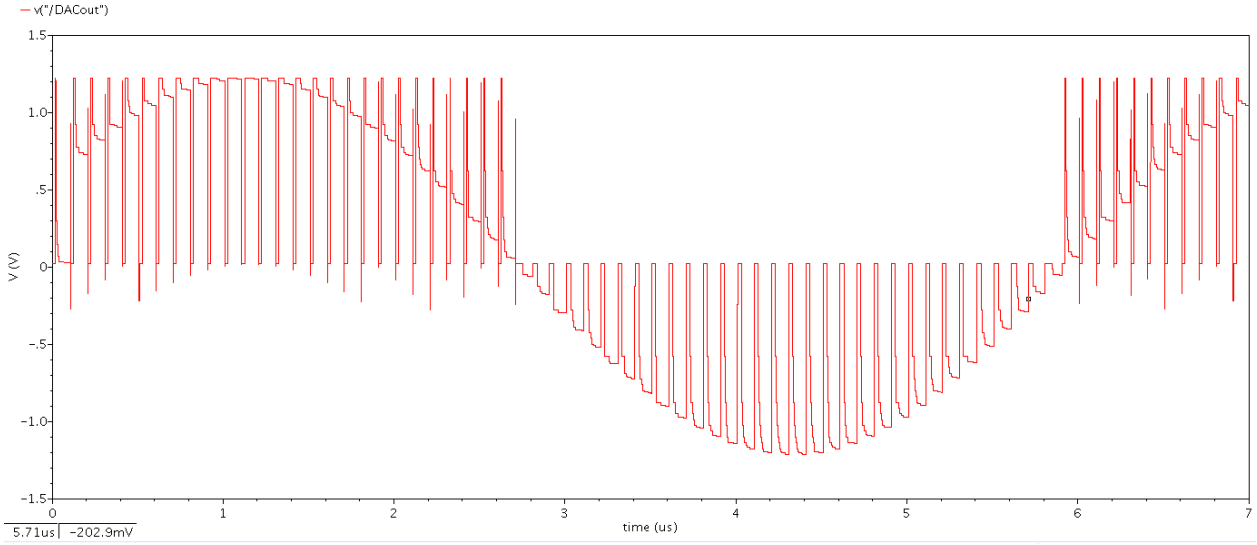

Figure 12: Variation of ADC output voltage with each conversion step

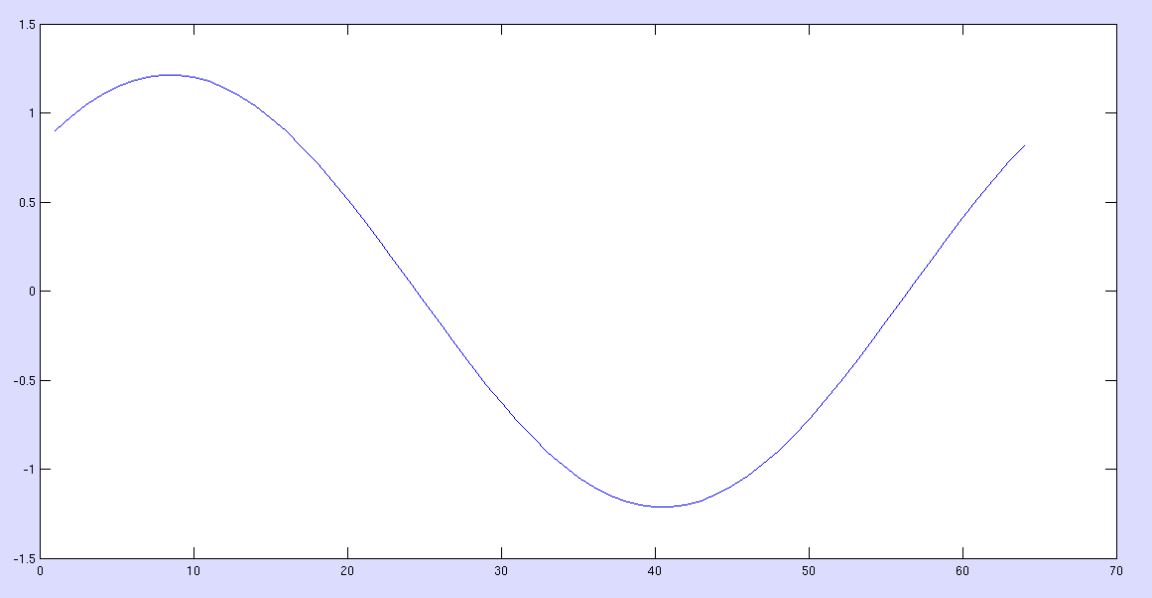

Figure 13: Sampled ADC output voltage

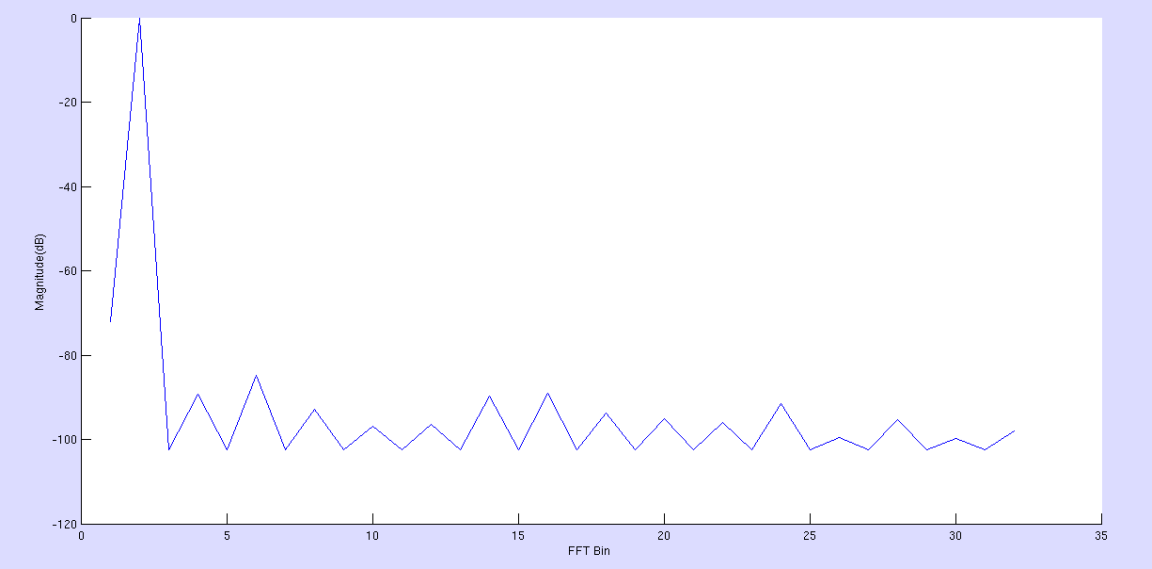

Figure 14: FFT plot of ADC output

SNR achieved = 79.58 dB (@fs/64) & 79.26 dB (@ fs*2/5)

4.3 CONCLUSION AND FURTHER WORK

Hence, we have accomplished proof of this concept. We are able to achieve 13 bits of resolution by using a latch as a residue amplifier. Next step is to complete the layout of each of the blocks and tapeout the chip. Once the chip gets back from the foundry, we will test out its performance and draw final conclusions.

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