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# Analog-to-Digital Converter Circuit and System Design to Improve with CMOS Scaling

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# Analog-to-Digital Converter Circuit and System Design to Improve with CMOS Scaling

**by**

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**DISSERTATION**

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

**DOCTOR OF PHILOSOPHY**

THE UNIVERSITY OF TEXAS AT AUSTIN

May 2015

Dedicated to my mother, my father, and my wife

# Acknowledgments

I wish to thank many people who have been a source of knowledge and inspiration to me through the years.

First and foremost, I would like to express my deepest gratitude to my advisor Prof. Brian L. Evans, who encouraged me to pursue post-graduate studies under his supervision, and guided and mentored me for my entire time at The University of Texas at Austin. Without his kindness and patience, I would not have been able to succeed.

Second, I would like to sincerely thank Dr. Arjang Hassibi, who gave me a chance to collaborate with him and his former student Dr. Woo Young Jung, and inspired us both to achieve something new, by thinking outside the box, across analog/digital boundaries.

I am also grateful to my committee members and professors: Prof. Todd E. Humphreys, Prof. Earl E. Swartzlander, and Prof. Ahmed H. Tewfik. In their classes, they have all taught me advanced topics and concepts that have directly or indirectly guided me throughout this dissertation. Their guidance and role on my doctoral committee is deeply appreciated.

As the person who first taught me about $\Delta\Sigma$ ADCs, I am deeply indebted to Eric J. Swanson, who caught my interest in the field of $\Delta\Sigma$ ADCs, gave me a deep understanding of such ADCs, and even mentored and sup-

ported me while he was at Cirrus Logic, Inc.. May he rest in peace.

I wish to express my gratitude to both my loving parents, who always supported and motivated me, as well as pushed me to limits I didn't know I could achieve. And finally, many thanks and appreciation to my wife Sebar, who has been very patient, loving, and understanding throughout the final years of my studies.

# Analog-to-Digital Converter Circuit and System Design to Improve with CMOS Scaling

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There is a need to rethink the design of analog/mixed-signal circuits to be viable in state-of-the-art nanometer-scale CMOS processes due to the hostile environment they create for analog circuits. Reduced supply voltages and smaller capacitances are beneficial to circuit speed and digital circuit power efficiency; however, these changes along with smaller dimensions and close coupling of fast-switching digital circuits have made high-accuracy voltage-domain analog processing increasingly difficult. In this work, techniques to improve analog-to-digital converters (ADC) for nanometer-scale processes are explored.

First, I propose a mostly-digital time-based oversampling delta-sigma ($\Delta\Sigma$) ADC architecture. This system uses time, rather than voltage, as the analog variable for its quantizer, where the noise shaping process is realized by modulating the width of a variable-width digital "pulse." The merits of

this architecture render it not only viable to scaling, but also enable improved circuit performance with ever-increasing time resolution of scaled CMOS processes. This is in contrast to traditional voltage-based analog circuit design, whose performance generally decreases with scaling due to increasingly higher voltage uncertainty due to supply voltage reduction and short-channel effects.

In conjunction with Dr. Woo Young Jung while he was a Ph.D. student at The University of Texas at Austin, two prototype implementations of the proposed architecture were designed and fabricated in TSMC 180 nm CMOS and IBM 45 nm Silicon-On-Insulator (SOI) processes. The prototype ADCs demonstrate that the architecture can achieve bandwidths of 5-20 MHz and $\sim$50 dB SNR with very small area. The first generation ADC core occupies an area of only 0.0275 $mm^2$, while the second generation ADC core occupies 0.0192 $mm^2$. The two prototypes can be categorized as some of the smallest-area modulators in the literature.

Second, I analyze the measured results of the prototype ADC chips, and determine the source for the harmonic distortion. I then demonstrate a digital calibration algorithm that sufficiently mitigates the distortion. This calibration approach falls in the general philosophy of digitally-assisted analog systems. In this philosophy, digital calibration and post-correction are favored over traditional analog solutions, in which there is a high cost to the analog solution either in complexity, power, or area.

# Table of Contents

# List of Figures

# Chapter 1

# Introduction

Moore's Law [2], or the doubling of transistors on an integrated circuit (IC) every 18–24 months, has been the driving force behind the exponential growth in the consumer electronics industry over the past few decades. State-of-the-art CMOS fabrication processes continually offer smaller transistors, which are faster and consume less active power due to lower capacitive loading and lower supply voltage. Nowadays, commercial technology nodes offer minimum transistor gate lengths of 65 nm, 45 nm, 22 nm, ... rendering multibillion-transistor ICs not only feasible, but also cost effective.

The demand for reducing costs and building more compact electronic devices has provided incentives to integrate more functionality on a single application-specific IC (ASIC). Multi-chip solutions are less attractive in today's battery-powered handheld devices in which low-power operation is key. This is in part due to the need to reduce printed circuit board (PCB) size, as well as to reduce power lost in package pins, bond wires, and matched 50 $\Omega$ transmission-lines. Given these constraints, single-chip ASICs that integrate not only digital but also analog functions have become a necessity for many years. These so-called "mixed-signal" ICs present a plethora of new challenges

that have been partially addressed.

Consider a wireless radio receiver as an example application that requires both analog and digital processing. Examples of analog circuits used in this application include: low-noise amplification of low-level signals received by the antenna, bandpass filtering to remove a large portion of out-of-band noise and interference, and mixing the radio frequency (RF) signal down to an intermediate frequency (IF). At the boundary between analog and digital, an analog-to-digital converter (ADC) samples the analog signal into quantized (digital) discrete-time samples that are streamed to the baseband processor. The role of the digital baseband processor is to efficiently decode the transmitted message using digital signal processing algorithms.

Availability of increasingly smaller transistors in state-of-the-art CMOS processes translates into faster digital as well as analog circuits; however, analog circuit accuracy generally degrades with reduced dimensions and supply voltages. These mixed-signal integrated circuits are a hostile environment for analog circuit design for several reasons, such as:

- Due to the market dominance of digital circuits, the latest CMOS processes are generally optimized for digital circuits while quantities of interest to analog circuit design, such as intrinsic transistor gain, are sacrificed.

- Coexistence of a larger number of analog and digital circuits in closer proximity increases the noise coupled onto analog circuits from fast-

switching digital circuits.

- Reduced supply voltages to avoid breakdown of thin gate oxides reduces voltage headroom of analog circuits, thereby resulting in smaller linear operating regions and lower dynamic range.

- Reduced transistor dimensions reduces analog matching accuracy due to process variations [3], and reduced area lowers capacitance, which in turn increases thermal noise ($kT/C$ noise).

Thus, there is both a need and a trend to rethink the design of analog circuits to be viable in advanced "digital-friendly, but analog-hostile" processes. The focus of this work is an important mixed-signal circuit that interfaces between analog and digital circuits, the Analog-to-Digital Converter (ADC). For the rest of this work, I restrict my focus to ADC circuits but many of the techniques could be used for other mixed-signal circuits with a similar approach. The rest of this chapter serves as an introduction to current approaches to improving ADCs in nanometer-scale CMOS processes.

Murmann [4] plots the trends in ADC performance from a power-efficiency viewpoint and observes an average reduction in energy by a factor of two approximately every 1.9 years. However, from a speed-resolution viewpoint, a weak doubling every 3.6 years is observed, although top performance has not increased much since the early 2000s. Additionally, he studies impact of scaling in ADC design and references improved architectural schemes.

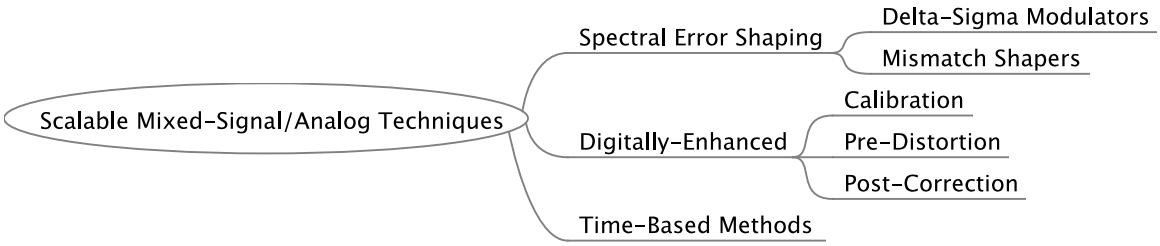


Figure 1.1: A classification of techniques to improve scaling of analog integrated circuits in nanometer-scale CMOS processes.

## 1.1 ADC Circuits Suited for Scaling

Several techniques can make ADC circuits more suitable for CMOS scaling. These techniques either relax accuracy requirements of analog circuits for improved area/power efficiency, or provide a means to mitigate the impairments associated with scaling. Here, I classify the techniques into three main categories: spectral error shaping, digitally-enhanced analog, and time-based processing. This classification is illustrated in Fig. 1.1 and the approaches are briefly explained below. For another classification and additional insight, please refer to [5].

### 1.1.1 Spectral Error Shaping

A widely used technique that allows one to build accurate mixed-signal/analog circuits is used in delta-sigma ($\Delta\Sigma$) modulators (DSM). Simply stated, DSMs create a feedback loop to perform noise-shaping by pushing most of the energy of quantization noise into the high end of the spectrum. Combined with oversampling and low-pass filtering, DSMs enable overall higher

resolution conversion with components as inaccurate as 1-bit ADCs. DSMs are also used in DACs. Another widely used technique to push error signal due to mismatch into the high end of the spectrum is mismatch shaping [6]. The $\Delta\Sigma$ ADC is introduced in more detail in Section 2.2.

### 1.1.2 Digitally-Enhanced Analog

The term "Digitally-Enhanced Analog" or "Digitally-Assisited Analog" refers to a collection of techniques that utilize digital signal processing (DSP) algorithms to improve the overall performance of a mixed-signal/analog circuit by relaxing the analog component requirements and letting DSP algorithms correct for the losses. The DSP overhead must be such that the area/energy efficiency of the overall system be better than the case where a more accurate analog component is used.

As processes scale and analog accuracy becomes harder to achieve, the reduced cost of digital gates makes this approach increasingly effective. Examples of digitally-assisted circuits will be given in Chapter 7.

### 1.1.3 Time-Based Methods

As voltages and currents scale down, voltage and current accuracies are reduced. Analog circuit linearity decreases when supply voltages are reduced. Also, thermal noise ($kT/C$) increases when capacitance decreases. The idea to move analog quantities from the (voltage or current) amplitude axis to the time axis becomes attractive. Scaled processes offer higher time resolution,

and continue to do so. If analog quantities are represented on the time axis, an opportunity exists for circuits designed with this paradigm to not only be viable to scaling, but also improve with process generation. In Section 2.3, I discuss time-based signal processing in more detail.

## 1.2 Proposed Contributions

I propose to improve performance of mixed-signal/analog circuits, in particular Analog-to-Digital Converters (ADCs), in nanometer-scale CMOS using novel architectures and techniques. In particular, I will be defending the following thesis statement:

> *Architecting low-area delta-sigma data converters that scale with CMOS technology requires replacing voltage-domain with time-domain processing.*

I will give evidence to support this claim through the following contributions:

1. Design and modeling of a novel noise-shaping $\Delta\Sigma$ ADC architecture that features the following:
   (a) mostly-digital time-based processing, which
      i. accepts a voltage signal at the input, but internally converts it to a pseudo-differential pulse, and
      ii. all subsequent processing is performed on pulses whose widths encode the signal information.

(b) asynchronous modulator with loop delay calibration unit, which

i. provides a known time base using an external reference clock,

ii. removes harmonic distortion due to non-uniform sampling, which arises from input-dependent time drift in the asynchronous loop, and

iii. reduces the need for an accurate clock network.

(c) a novel multi-bit invertible TDC/DTC (ADC/DAC), wherein

i. the width of the pulse is quantized by a delta-sigma modulator with a flash time-to-digital converter (TDC) as the internal ADC,

ii. reduces area through sharing the unit delay elements,

(d) removes the sample-and-hold amplifier and replaces it with a continuous-time comparator which simplifies the circuit even further.

2. Design, fabrication, and testing two prototype ADC chips using the proposed architecture (in collaboration with Dr. Woo Young Jung), using

(a) TSMC 180nm CMOS process, and

(b) IBM 45nm SOI process.

3. Nonlinear circuit linearization of the ADC

(a) using digital post-correction to estimate and correct for nonlinearity due to DTC mismatch

(b) without the need of a calibrating DAC

## 1.3 Organization

Background information about ADCs, $\Delta\Sigma$ modulation, and time-based approaches are presented in Chapter 2. The proposed time-based delta-sigma ADC is discussed in Chapter 3. Behavioral modeling of the proposed time-based delta-sigma ADC is presented in Chapter 4. First and second generation chip prototypes are presented in Chapters 5 and 6, respectively. Chapter 7 discusses the sources of nonlinearity in the two prototype chips and shows a method of calibrating the nonlinearity. Finally, conclusions are drawn in Chapter 8.

## 1.4 Abbreviations

| | |
|---|---|
| ADC | Analog-to-Digital Converter |
| ADPLL | All Digital Phase Lock Loop |
| ASIC | Application-Specific Integrated Circuit |
| CMOS | Complementary Metal Oxide Semiconductor |
| DAC | Digital-to-Analog Converter |
| DPLL | Digital Phase Locked Loop |
| DSP | Digital Signal Processing |
| DSM | Delta-Sigma Modulator |
| DTC | Digital-to-Time Converter |
| FFT | Fast Fourier Transform |
| FPGA | Field Programmable Gate Array |
| IC | Integrated Circuit |
| LSB | Least Significant Bit |
| LVCMOS | Low Voltage CMOS |
| LVDS | Low Voltage Differential Signaling |
| LVTTL | Low Voltage Transistor-to-Transistor Logic |
| OFDM | Orthogonal Frequency Division Multiplexing |
| OSR | OverSampling Ratio |
| RMS | Root Mean Squared |
| SFDR | Spurious-Free Dynamic Range |
| SOI | Silicon-on-Insulator |
| TDC | Time-to-Digital Converter |
| VCO | Voltage Controlled Oscillator |
| VTC | Voltage-to-Time Converter |

# Chapter 2

# Background and Prior Work

This chapter introduces important concepts which will be used in subsequent chapters. Toward this goal, an overview of ADC architectures is presented. Then, the concept of delta-sigma modulation as applicable to ADCs is presented. Next, the time-based approach in analog signal processing is described. Finally, different methods of combining time-based techniques with delta-sigma modulation are reviewed.

## 2.1 Analog-to-Digital Conversion

Analog-to-Digital Conversion is the process of converting a real-valued continuous-time waveform $x_c(t)$ to a discrete-amplitude discrete-time sequence $x[k]$, suitable for digital signal processing. Typical ADCs consist of: 1) low-pass filtering (anti-aliasing filter), 2) sampling, 3) quantization, and 4) digital encoding and filtering (see Fig. 2.1). First I review the Nyquist sampling theorem to explain the first two operations, then I introduce concepts in quantization and coding.

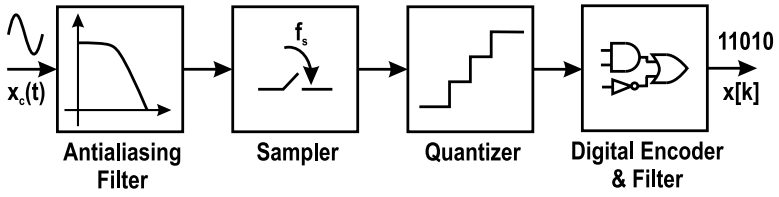


Figure 2.1: Block diagram of a typical analog-to-digital converter.

### 2.1.1 Sampling Theory

The Nyquist Sampling Theorem (see [7]) states that a band-limited signal $x_c(t)$ with

$$X_c(f) = 0 \quad \text{for } |f| \geq f_N, \tag{2.1}$$

is uniquely determined by its samples $x[n] = x_c(nT), n = 0, \pm 1, \pm 2, \ldots$ if

$$f_s = \frac{1}{T} \geq 2f_N. \tag{2.2}$$

where $f_N$ is called the *Nyquist frequency* and $2f_N$ is the *Nyquist rate*. In practice, bandlimited signals are rare (or impossible for finite-duration signals) and there exists additive noise that may fill the higher frequency range. Thus to avoid aliasing into the lower frequency range, an analog prefilter (called an antialiasing filter) must enforce bandlimitedness. Without, oversampling, i.e., when $f_s = 2f_N$, an ideal "brick wall" low-pass filter is required. In the frequency domain, this ideal filter is defined as:

$$H_{AA}(f) = \begin{cases} 1, & |f| < f_s/2 \\ 0, & |f| > f_s/2 \end{cases}, \tag{2.3}$$

but since such a filter would be noncausal and have infinite delay, it must be approximated by a physically-realizable analog filter. Limitations of the

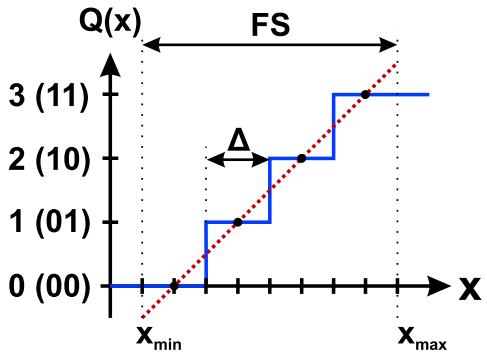


Figure 2.2: $N = 2$-bit uniform quantizer function.

analog filter include finite stop-band attenuation, finite transition-band slope, and non-zero pass-band ripple. To obtain a better approximation to the ideal brick wall filter, the implementation cost of the antialiasing filter increases.

With oversampling (sampling above the Nyquist rate), the requirements of the analog filter can be relaxed at the expense of increasing the rate of the Digital Signal Processing (DSP) downstream. If the DSP algorithm desires the rate to be reduced to the Nyquist rate, a (digital) decimation filter is required. Thus oversampling can be viewed as a technique to trade analog filter complexity with digital decimation filter complexity.

### 2.1.2 Quantization

In contrast to ideal sampling at the Nyquist rate or greater, which preserves information in the signal, quantization is an irreversible (lossy) operation that is inherently non-linear. A typical $N$-bit uniform quantizer, such as the one shown in Fig. 2.2, rounds the real-valued (analog) sample to the near-

est one of $2^N$ discrete levels. Such a quantizer $y = Q(x)$, divides the interval $[x_{min}, x_{max}]$ with full-scale range $FS = x_{max} - x_{min}$ into $2^N$ uniform intervals with width $\Delta = \frac{FS}{2^N}$, also called the LSB. Within the full-scale range, i.e., no saturation, the uniform quantizer function may be described mathematically as:

$$Q(x) = \left\lfloor \frac{x - x_{min}}{\Delta} \right\rfloor, \qquad x_{min} \leq x < x_{max} \tag{2.4}$$

where $\lfloor u \rfloor$ denotes the flooring operation, i.e., the largest integer $\leq u$. Thus $Q(x)$ is a number from 0 to $2^N - 1$, and the analog equivalent of $Q(x)$ is:

$$\tilde{Q}(x) = \Delta \left\lfloor \frac{x - x_{min}}{\Delta} \right\rfloor + x_{min}, \qquad x_{min} \leq x < x_{max} \tag{2.5}$$

The difference between the quantized version of a sample and the true analog value is called quantization error or quantization noise:

$$e = x - \tilde{Q}(x), \tag{2.6}$$

which ranges from $-\frac{\Delta}{2}$ to $\frac{\Delta}{2}$. For large inputs within the quantization range (i.e., no saturation), the error can be assumed to be a uniformly-distributed random variable uncorrelated with the input, thus the quantization noise power (variance) is:

$$\sigma_e^2 = \int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} \frac{1}{\Delta} e^2 \, de = \frac{\Delta^2}{12} = \frac{FS^2}{12\,(2^N)^2} \tag{2.7}$$

A linear model for quantization therefore becomes:

$$y = G\,(x - x_{min}) + e \tag{2.8}$$

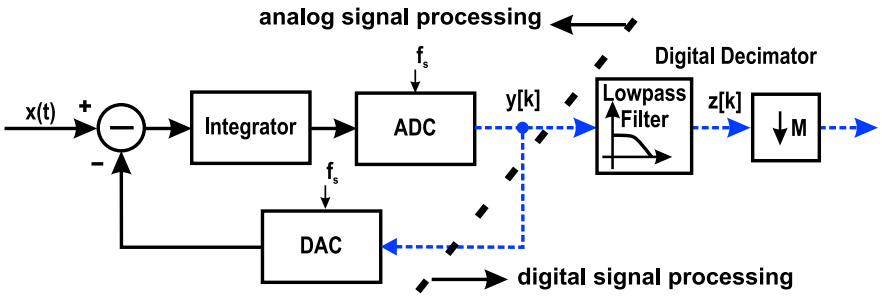


Figure 2.3: First-order delta-sigma analog-to-digital converter.

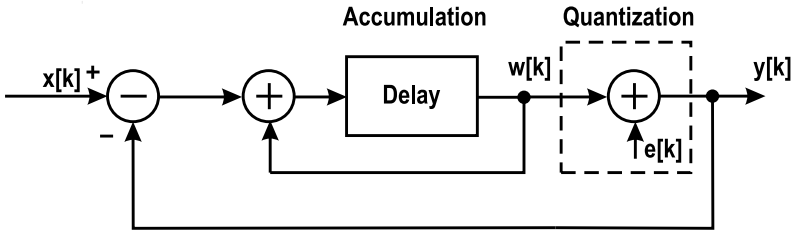


Figure 2.4: Sampled-data linear model of the analog portion of the first-order delta-sigma analog-to-digital converter shown in Fig. 2.3.

where $G$ is the gain (or the slope of the dotted line connecting $x_{min}$ and $x_{max}$ in Fig. 2.2), which may be assumed to be 1, without loss of generality.

The larger the number of quantization bits $N$, the smaller the LSB ($\Delta$), and hence the smaller the quantization noise. Every application usually has its own requirement for $N$, but it may range from a few bits (control applications) up to 24 bits (hi-fidelity audio). The output of the quantizer is subsequently encoded; i.e., each quantization level is assigned a binary digital code, e.g., a 2's complement signed $N$-bit number.

## 2.2 Delta-Sigma Modulation

In the 1950s and 1960s, it was shown that the effective resolution of a coarse quantizer may be increased by using feedback and oversampling. The so-called delta modulator [8], [9] and its successor the delta-sigma ($\Delta\Sigma$) modulator [10] have since then evolved considerably both in theory and practice. To understand its operation [11–13], consider the first-order $\Delta\Sigma$ ADC and its equivalent sampled-data model shown in Fig. 2.3 and Fig. 2.4, respectively. The output of the accumulator is

$$w[k] = x[k-1] - e[k-1] \tag{2.9}$$

and the output of the ADC is

$$y[k] = w[k] + e[k] = x[k-1] + (e[k] - e[k-1]) \tag{2.10}$$

Therefore, the output $y[k]$ contains a delayed version of the input $x[k-1]$ plus a differentiated version of the quantization error. In other words, the first difference of the noise appears at the output while the signal is unchanged. The spectral density of the noise is given by [11]:

$$N(f) = E(f)\,|1 - e^{-j2\pi fT}| = 2\,e_{\text{rms}}\sqrt{2T}\sin\left(\frac{2\pi fT}{2}\right) \tag{2.11}$$

As shown in Fig. 2.5, the $\Delta\Sigma$ modulator reduces the noise in low frequencies at the expense of increasing noise at high frequencies. The high frequency noise is removed by the digital low-pass filter that is part of the decimator used to reduce the sampling rate. When the oversampling ratio (OSR) defined as

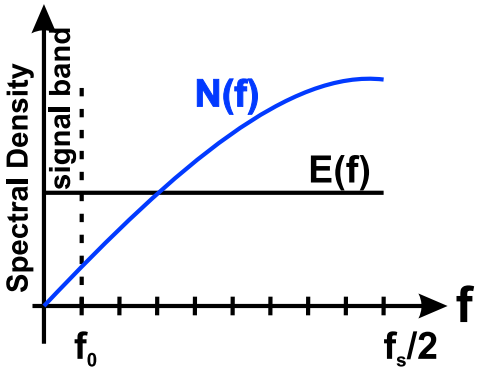


Figure 2.5: Spectral density of noise from delta-sigma quantization $N(f)$ compared to ordinary quantization $E(f)$.

$M = \frac{f_s/2}{f_0}$ is high, the modulation noise in the signal band is much less than the ordinary quantization error. The total noise in the signal band is:

$$n_0^2 = \int_0^{f_0} |N(f)|^2 df \approx e_{\text{rms}}^2 \frac{\pi^2}{3} (2 f_0 T)^3 \qquad f_s \gg f_0 \tag{2.12}$$

In other words, the RMS value is:

$$n_0 \approx e_{\text{rms}} \frac{\pi}{\sqrt{3}} (OSR)^{-3/2} \tag{2.13}$$

Therefore, with a highly selective digital low-pass filter, every doubling of OSR reduces the noise by 9 dB (1.5 bits), but in practice for the sake of relaxing the requirements of the digital filter, some of the high frequency noise is allowed to alias into the signal band. With higher orders of integration, the slope of $N(f)$ at low frequency increases and thus reduces in-band noise even lower. Reference [14] provides a more detailed analysis that is not included here for brevity.

Another topology for first-order noise shaping is that of the error feedback topology, shown in Fig. 2.6. While it is used less often in traditional

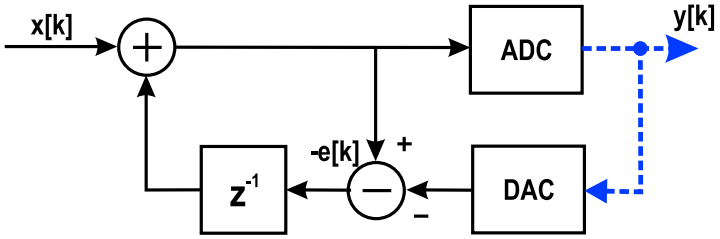


Figure 2.6: Error feedback only delta-sigma modulator.

voltage-based ADCs, it has advantages which will become clear in Chapter 3. To conclude this section, note the benefits of using $\Delta\Sigma$ modulation from a scaling perspective [15]:

1. Reduced analog accuracy requirements, e.g., a coarse internal quantizer, as low a single-bit may be used for an overall higher resolution converter.

2. A large component, namely the digital decimation filter improves with scaling (implemented by digital gates)

3. Analog antialiasing filter prior to sampling has more relaxed specifications

## 2.3 Time-Based Signal Processing

Traditionally, analog circuits represent and manipulate information in the (voltage) amplitude domain, which becomes increasingly unreliable in nanometer-scale mixed-signal integrated circuits. This is due to reduced supply voltages, reduced linearity, short-channel effects, and coupled noise from

digital circuits on the same chip. Thus, one needs to rethink analog processing to find techniques that are more viable to CMOS scaling. One method of solving this problem in state-of-the-art CMOS processes is to exchange the amplitude axis for the time axis [16]. Thus, an analog voltage quantity is converted to time and is subsequently processed. This approach not only alleviates the problem of reduced voltage, but it also takes advantage of the increased time-resolution due to higher intrinsic transistor speeds. The voltage-to-time conversion (VTC) may take many forms, such as pulse frequency modulation, pulse duration modulation and duty-cycle modulation [16].

In ADC applications, a time-based signal represented by a pulse duration, may be quantized using a time-to-digital converter (TDC) circuit which measures the time between two pulses. TDCs have been traditionally been used in applications such as time-of-flight measurement in physics experiments, and digital phase lock loops (DPLL). It is one of the fundamental components in time-based signal processing. Another block is the digital-to-time converter (DTC), which is the reverse operation of the TDC. In [17], an overview of TDC and DTC circuits is given, and TDCs are classified into four categories:

1. Single counter
2. Flash TDC
3. Vernier oscillator, e.g., [18, 19]
4. Cyclic pulse-shrinking TDC, e.g., [20]

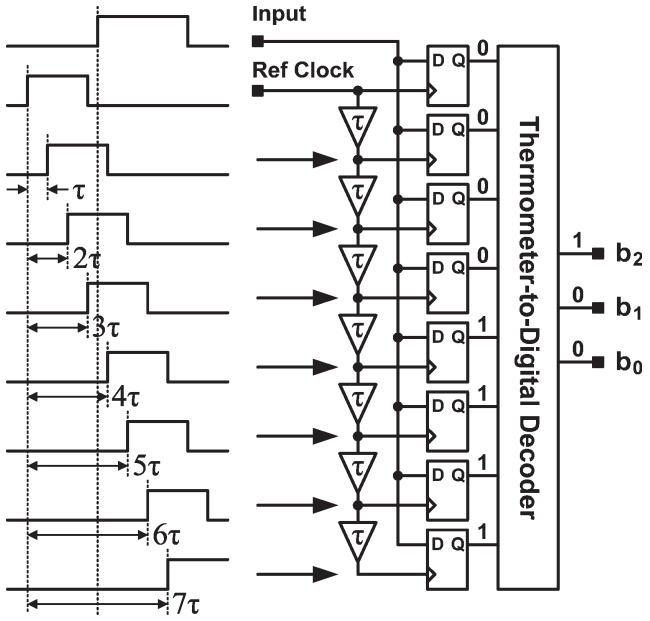


Figure 2.7: A 3-bit flash time-to-digital converter [17].

As an example, consider the flash TDC illustrated in Fig. 2.7. Such a circuit is implemented using digital circuits: buffers for unit delay by $\tau$, latches for strobing the value of the input pulse at equally spaced time-intervals, and digital logic to convert a thermometer code to a binary word. The benefits of time-based processing are clear by examining this circuit:

1. Improved timing accuracy with transistor scaling

2. Time-based operations have "digital" implementation that scale well (even if treated as analog with custom layout)

3. Not thermal noise limited, therefore no need for large capacitances

Examples of circuits and systems using the time-based processing approach include: an all-digital PLL (ADPLL)-based Bluetooth radio frequency synthesizer [21], or recent voltage-controlled oscillator (VCO)-based ADCs in which the information in the phase-domain is quantized.

## 2.4 Time-Based Delta Sigma ADCs

Analog-to-digital converter systems that combine $\Delta\Sigma$ modulation and time-based processing include the following:

1. Voltage-Controlled Oscillator (VCO)-based ADCs,

2. Time-Based Delta-Sigma ADCs.

The concept of using VCOs as multi-bit quantizers in $\Delta\Sigma$ ADCs was introduced in 1999 [22]. Since its inception, many prototypes have utilized this scheme for a variety of applications, primarily in the design of high-speed data converters for wireless systems. The key advantage of using a VCO in an oversampling converter is that the conversion from voltage to time using a VCO that generates binary pulses whose frequency is proportional to the input voltage, and whose phase is the integral of the frequency. Thus by sampling the phase of the VCO, quantization of the integral of input voltage is achieved. This architecture provides inherent noise-shaping properties and can operate at low supply voltages and high sampling rates. While the natural integration and quantization using a VCO quantizer achieves first-order noise shaping,

it may be used as the quantizer in a multi-order $\Delta\Sigma$ ADC with additional OpAmp-based integration stages [23–25].

It is widely known that the linearity of a VCO's voltage-to-frequency relationship is limited [26]. Thus, a lot of the focus in VCO-based ADC implementations is on the linearity improvement. Taylor and Galton use pseudo-random binary sequences and an auxiliary DAC to measure nonlinearity using an LMS algorithm and cancel it at the output of the modulator using a lookup table [27–29]. On the other hand, Rao, *et al* proposed the use of a two-level pulse-width modulator (PWM) in front of the VCO-based $\Delta\Sigma$ ADC [30]. By restricting VCO input to only two levels, the architecture becomes insensitive to VCO voltage-to-frequency nonlinearity. However the PWM modulator is built using OpAmps which do not scale well.

Despite drawbacks to the VCO-based $\Delta\Sigma$ ADC, many solutions to these drawbacks have been proposed and the momentum is moving towards commercially viable data converters. This architecture is particularly attractive at bulk CMOS process nodes at or below 65nm. There is evidence of commercial VCO-based ADC designs under development.

Alternative time-based ADCs are proposed [31], [32], and [33]. A time-domain ADC architecture that implements a PWM and time-to-digital converter (TDC) in the feedback loop is presented [34]. This architecture improves the linearity of PWM. However, major analog blocks (integrator and filter) are required for the noise shaping. Another innovative architecture [35] replaces the quantizer and DAC in a $\Delta\Sigma$ ADC with a time-encoding quantizer

(TEQ).

## 2.5 Summary

In summary, I introduced analog-to-digital conversion, and described $\Delta\Sigma$ modulation as a leading approach that benefits from CMOS process scaling due to oversampling and noise shaping. I reviewed time-based concepts for signal processing. Then, I mentioned advantages of combining the two approaches as an attractive method of reducing ADC circuit area in scaled process nodes.

In the next chapter, I discuss the design of an ADC circuit that uses both the time-based processing scheme and $\Delta\Sigma$ modulation, therefore combining the benefits of the two approaches for improved performance with scaling.

# Chapter 3

# Time-Based $\Delta\Sigma$ ADC

## 3.1 Introduction

In Chapter 2, I discussed the benefits of delta-sigma modulation (DSM) and time-based processing from a scaling point-of-view. In this chapter, I propose a time-based $\Delta\Sigma$ ADC that aims to benefit from the merits of both techniques in order to improve the viability of ADCs under transistor scaling. The proposed mostly-digital asynchronous time-based $\Delta\Sigma$ ADC features the following:

1. At the input, the ADC accepts a voltage signal, which is internally converted to a pseudo-differential pulse. All subsequent processing is performed on pulses whose widths encode the signal information.

2. The asynchronous modulator can be synchronized to an external clock through a loop delay calibration unit. This scheme provides a known

This chapter is based in part on W. Jung, Y. Mortazavi, B. L. Evans, and A. Hassibi, "An all-digital PWM-based ADC with an inherently matched multi-bit quantizer," in *Proc. 2014 IEEE Custom Integrated Circuits Conference (CICC)*. IEEE, 2014, pp. 1-4. Authors Jung and Mortazavi are equal contributors. Authors Evans and Hassibi are supervisors and primary investigators of the work.

time base, and removes harmonics due to non-uniform sampling which arises from input-dependent time drift in the asynchronous loop.

3. The width of the pulse is quantized by a delta-sigma modulator with a flash time-to-digital converter (TDC) as the internal ADC.

4. A novel multi-bit invertible TDC/DTC (ADC/DAC) is possible thanks to time-domain processing. This approach reduces area.

5. The proposed structure presents an opportunity to use the "minimalistic design" scheme [4] to further reduce power through reliance on digital calibration rather than precision analog circuitry.

6. It also removes the sample-and-hold amplifier and replaces it with a continuous-time comparator which simplifies the circuit even further.

In the following section, I review analog-to-digital converter systems that combine $\Delta\Sigma$ modulation and time-based processing.

## 3.2 Time-Based $\Delta\Sigma$ Modulator Architecture

This section describes the operation principle of the proposed time-based $\Delta\Sigma$ ADC, whose model is shown in Fig. 3.1. First, the concept of information encoding using pseudo-differential pulses is described. Then pulse width addition and subtraction in the time domain is introduced. Finally, the modulator topology of the proposed ADC is presented.

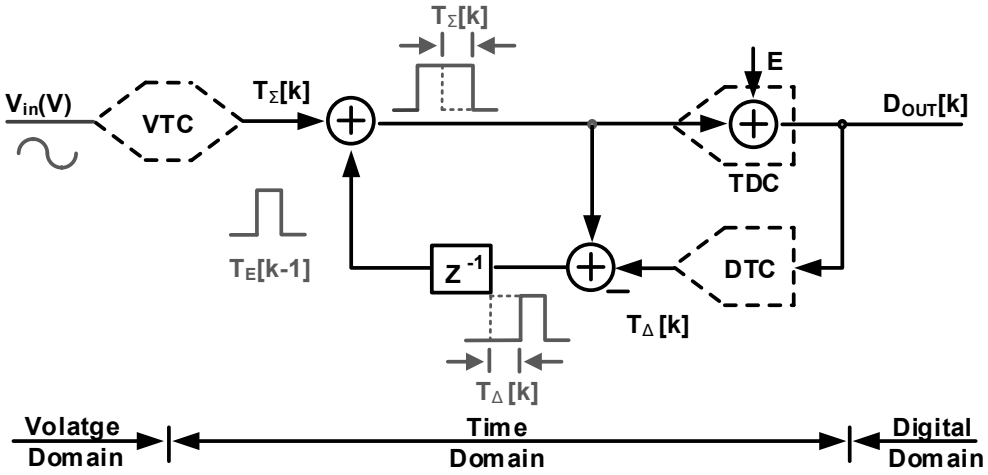


Figure 3.1: $\Delta\Sigma$ modulator model showing boundaries of voltage/time/digital domain processing. VTC = voltage-to-time converter, TDC = time-to-digital converter, DTC = digital-to-time converter.

### 3.2.1 Pulse Width Information Encoding

In the proposed ADC, analog information is encoded in the form of "pulse width." A conventional digital pulse $T_a$, shown in Fig. 3.2, consists of a signal that is either low (0 V) or high ($V_{DD}$). The *pulse width* is defined as the duration of time in which the pulse is high. Conceptually, this definition is simple to understand; however, for both accuracy and robustness, pseudo-differential pulses are often preferred. A pseudo-differential pair of pulses $(T_{b,rise}, T_{b,fall})$ as shown in Fig. 3.2, encode pulse width in the time duration between the rise transition of $T_{b,rise}$ and that of $T_{b,fall}$.

The advantages of pseudo-differential pulses for encoding analog quantities are twofold: (1) By encoding information in the rise-to-rise delay rather than rise-to-fall delay, errors due to skewed low-to-high vs. high-to-low propagation delays are eliminated, and (2) this encoding removes the restriction on minimum pulse widths due to vanishing pulses. Every circuit in the proposed ADC operates using pseudo-differential pulses, even though some of the timing diagrams in this chapter illustrate the conventional pulse (for simplicity).

In reference to the pulses illustrated in Fig. 3.2, the following notation is used for the remainder of this chapter:

- A pulse represented by a pair of numbers $T_a = (t_{rise} \rightarrow t_{fall})$ indicates a transition from zero to $V_{DD}$ at time $t_{rise}$ and back to zero at time $t_{fall}$. The pulse width represented by $\Delta T_a = t_{fall} - t_{rise}$ is the analog quantity encoded by the pulse.

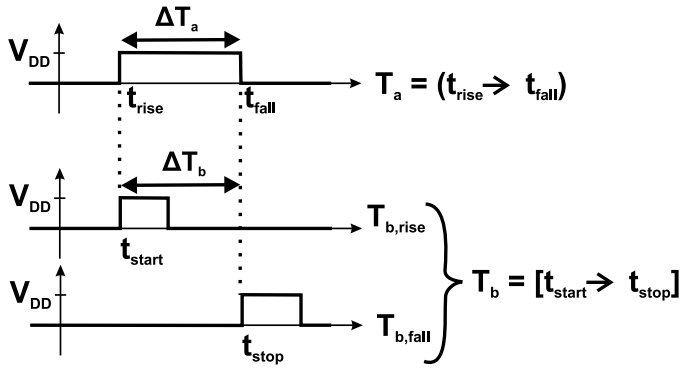


Figure 3.2: Definition of pulse and pseudo-differential (conceptual) pulse.

- A pseudo-differential pulse (or **conceptual pulse**) is represented as a pair of numbers $T_b = [t_{start} \rightarrow t_{stop}]$ and is defined as two pulses, the "rise pulse" $T_{b,rise} = (t_{start} \rightarrow t_{start}+\Delta t_r)$ and the "fall pulse" $T_{b,fall} = (t_{stop} \rightarrow t_{stop} + \Delta t_f)$. Square brackets denote pseudo-differential pulses. The information contained in the pseudo-differential pulse is $\Delta T_b = t_{stop} - t_{start}$ which is the rise-to-rise delay between the two pulses, which is called **pulse width**. Note that $\Delta t_r$ and $\Delta t_f$ have no significance in the signal information; however, they are required to be a fraction of a sampling period.

- The **rise pulse** of $T_b$ is denoted by $\text{rise}(T_b) = t_{start}$

- The **fall pulse** of $T_b$ is denoted by $\text{fall}(T_b) = t_{stop}$

The remainder of this chapter uses pseudo-differential pulses for all circuits, even if conventional pulses are shown in the timing diagrams (for simplicity).

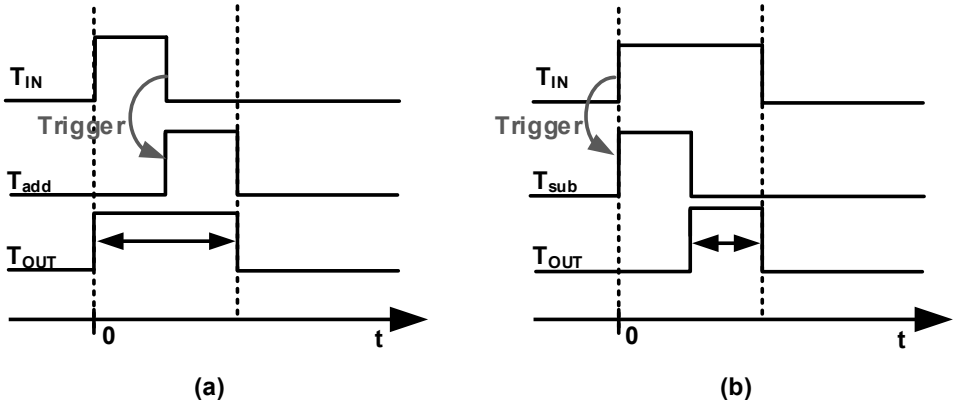


Figure 3.3: (a) Addition and (b) subtraction in time-domain using pulse widths.

### 3.2.2 Time-Domain Addition and Subtraction

Analog time-domain processing using pulse width as the analog quantity is shown in Fig. 3.3. To add two pulses, say $T_{in}$ and $T_{add}$, as depicted in Fig. 3.3(a), we align the start of $T_{add}$ to the end of $T_{in}$. Then the sum of the pulse widths is simply the pulse $T_{out}$ that begins with $T_{in}$ and ends with $T_{add}$. Subtraction, depicted in Fig. 3.3(b), requires aligning the start of $T_{sub}$ with that of $T_{in}$. The result of subtraction is the pulse $T_{out}$ which begins when $T_{sub}$ ends, and ends when $T_{in}$ ends. Aligning pulses in the manner described requires a triggering mechanism (and asynchronous digital circuits), which is described later.

With respect to pseudo-differential pulses, it is clear how pulse widths can be added and subtracted. If two pulses are appropriately aligned, adding a pulse to another is achieved by simply delaying the $f$ pulse of the output.

Similarly, to subtract two pulses aligned with their $r$ pulses, only the output $r$ pulse needs to be delayed. This method of pulse arithmetic has the advantage of simple implementation using digital logic gates. It also has the complexity of dealing with the alignment of pulses. In the next section, it shall become clear that using an error feedback structure, where the order of addition and subtraction is reversed (relative to conventional first-order $\Delta\Sigma$ modulators) resolves the pulse alignment problem.

### 3.2.3 Modulator Topology and System Modeling

The proposed time-based $\Delta\Sigma$ ADC architecture is shown in Fig. 3.4(a). It comprises three major blocks:

1. VTC/Adder,
2. Delay Control Unit (DCU), and
3. Time-to-Digital Converter/Digital-to-Time Converter (TDC/DTC).

The conceptual timing digram depicted in Fig. 3.4(b) shows conventional pulses for brevity; however, pseudo-differential pulses are used throughout this chapter. The topology of the modulator is first order error feedback (introduced in Fig. 2.6). The system equations are the following:

$$\begin{aligned} V(z) &= Y(z) + E(z) && (3.1)\\ &= \big(U(z) + z^{-1}Y(z) - z^{-1}V(z)\big) + E(z) && (3.2)\\ &= U(z) + E(z) - z^{-1}\left(V(z) - Y(z)\right) && (3.3) \end{aligned}$$

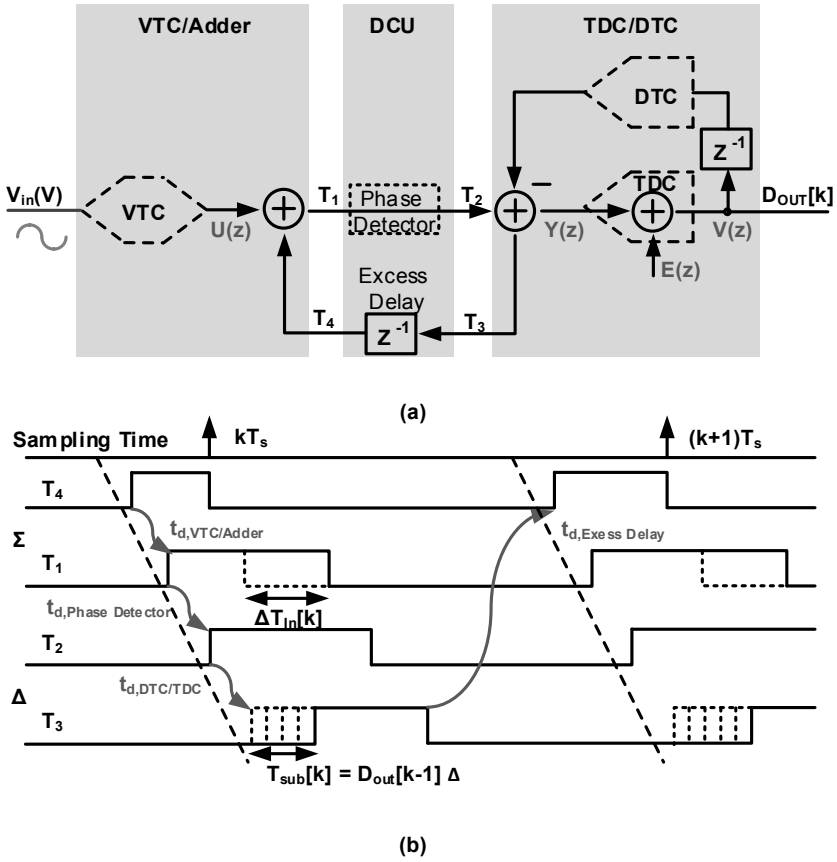


Figure 3.4: (a) Architecture and (b) timing diagram of the time-based $\Delta\Sigma$ ADC. VTC = voltage-to-time converter, DCU = delay control unit, TDC = time-to-digital converter, DTC = digital-to-time converter.

$$V(z) \;=\; U(z) + (1 - z^{-1})E(z) \tag{3.4}$$

This shows that the signal transfer function (STF) is unity

$$STF = \frac{V(z)}{U(z)} = 1, \tag{3.5}$$

and the noise transfer function (NTF) is that of a first order $\Delta\Sigma$ modulator:

$$NTF = \frac{V(z)}{E(z)} = 1 - z^{-1} \tag{3.6}$$

The input to the ADC is an analog voltage-domain waveform $V_{in}(t)$, which after sampling at $t = kT_s$ is converted to a time-domain quantity by the V*oltage to* T*ime* C*onverter (VTC)*. The analog sample $V_{in}(kT_s)$ is converted to a conceptual pulse (pseudo-differential pulse) [see definition in Section 3.2.1] after a transformation such as a linear transformation (for simplicity):

$$\Delta T_{in}[k] = a + b\, V_{in}(kT_s). \tag{3.7}$$

The *VTC/Adder* block adds the pulse widths of the feedback pulse and the input sample, $\Delta T_4$ and $\Delta T_{in}$, respectively.

$$\Delta T_1[k] = \Delta T_4[k] + \Delta T_{in}[k]. \tag{3.8}$$

The *Delay Control Unit (DCU)* block has two functions:

1. to control the startup conditions, and

2. to take measurements that facilitate loop delay calibration and tracking.

The output of this block, $T_2$, under normal closed-loop operation of the ADC, is simply a delayed version of $T_1$. Therefore, the duration of the pulse is unchanged, and

$$\Delta T_2[k] = \Delta T_1[k] \tag{3.9}$$

The *TDC/DTC* block implements both subtraction and quantization operations in the time domain. Quantization in the time domain is achieved using a multi-bit (e.g., 3-4 bit) Flash Time-to-Digital Converter (TDC) with quantization step $\Delta$. Subtraction is achieved by delaying the pulse rise by the appropriate number of quantization steps, as determined by $D_{out}$ from the previous cycle (i.e., $D_{out}[k-1]$). Subtraction precedes quantization, and the delay stages used in the DTC are reused in the TDC sequentially.

$$\Delta T_3[k] = \Delta T_2[k] - D_{out}[k-1]\Delta \tag{3.10}$$

$$D_{out}[k] = \left\lfloor \frac{T_3[k]}{\Delta} \right\rfloor \tag{3.11}$$

The *Excess Delay* block outputs $T_4$, which is a delayed version of $T_3$, without changing its width.

$$\Delta T_4[k] = \Delta T_3[k-1] \tag{3.12}$$

The combination of the delays due to the *Excess Delay* block and all other blocks in one cycle should ensure that the sampling interval is approximately uniform. The required amount of delay is calculated in Section 3.2.6.

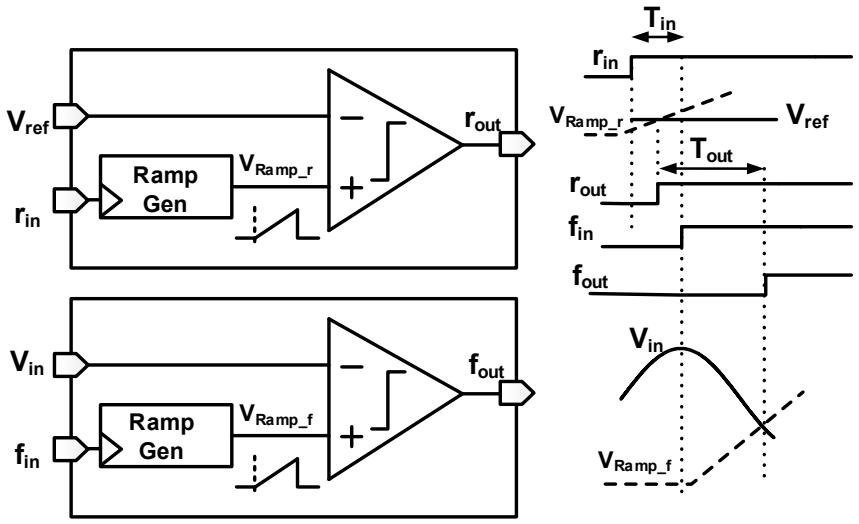


Figure 3.5: Functional block diagram and timing diagram of the VTC/Adder.

### 3.2.4 Voltage-to-Time Converter/Adder

The addition as well as the preceding voltage-to-time conversion operation shown in Fig. 3.4 is performed by the VTC/Adder block. At every cycle, the VTC/Adder conceptually adds to its input pulse $T_4$, a pulse width proportional to $V_{in} - V_{ref}$, and $T_1$ results. Both the input and output pulses are pseudo-differential pulses $(r_{in}, f_{in})$ and $(r_{out}, f_{out})$. To implement the voltage-to-time conversion and addition, two identical half-circuits are used, as shown in Fig. 3.5. The identical circuits have a ramp generator and a continuous-time comparator.

As shown in the bottom half of Fig. 3.5, the analog input $V_{in}(t)$ is

connected to a continuous-time comparator. The fall edge of the feedback pulse $f_{in} = T_{4,fall}$ triggers a ramp generator to produce a linear ramp from 0 to 1.8V. Once the ramp generator output ($V_{Ramp,r}$) crosses $V_{in}$, the output $f_{out}$ propagates. The larger the value of $V_{in}$, the longer it takes for the ramp voltage to reach $V_{in}$. Therefore, the information about the voltage amplitude of $V_{in}$ is stored in time. The proportionality is linear, when the ramp is linear, and therefore

$$f_{out} = \text{fall}(T_1[k]) \quad = \quad \text{fall}(T_4[k]) + t_d + k\, V_{in}(kT_s) \tag{3.13}$$

where

$$t_d \quad = \quad t_{\text{ramp gen}} + t_{\text{comparator}}, \quad \text{and} \tag{3.14}$$

$$k \quad = \quad (\text{ramp slope})^{-1}[\text{s/V}] \tag{3.15}$$

The simplest way to remove the fixed offset $t_d$ due to the delays of the ramp generator and comparator in the VTC/Adder is to replicate the same circuit for the rise signal (top half of Fig. 3.5). $V_{ref}$ represents the minimum usable input voltage (which may be different from zero if the input voltage range is other than 0 to 1.8V) due to linearity concerns. This replica circuit for removing offset is not optimal in terms of power, but it follows the pseudo-differential principle where the paths between both the rise and fall pulses of the pseudo-differential pulse are equalized as much as possible.

$$\text{rise}(T_1[k]) \quad = \quad \text{rise}(T_4[k]) + t_d + k\, V_{ref} \tag{3.16}$$

Combining (3.13) and (3.16) results in:

$$\begin{aligned} \Delta T_1[k] &= \text{fall}(T_1[k]) - \text{rise}(T_1[k]) && (3.17) \\ &= \Delta T_4[k] + k(V_{in}(kT_s) - V_{ref}) && (3.18) \\ &= \Delta T_4[k] + \Delta T_{in}[k] && (3.19) \end{aligned}$$

which means the transformation from voltage to time is linear as stated in (3.7) and the VTC/Adder implements addition according to (3.8).

The output of the VTC/Adder ($T_1$) passes through the phase detector block of the Delay Control Unit ($T_2$) without modification, except for delay $t_{d,\text{Phase Detector}}$ applied to both rise and fall pulses. It is then processed by the TDC/DTC block described next.

### 3.2.5 Time-to-Digital Converter/Digital-to-Time Converter

The TDC/DTC block performs the functions of both the ADC and the DAC in the first-order delta-sigma error feedback only structure shown in Fig. 2.6. In an effort to save area, a reusable structure for both subtraction and multi-bit quantization is devised. This novel invertible ADC/DAC is possible thanks to time-domain processing and is not possible in voltage-domain processing.

Figure 3.6 shows the block diagram of the TDC/DTC. It consists of tapped inverter stages with delay of $\Delta$ per stage. 16 stages are required for 4-bit quantization; however, to reduce variation in the boundary stages and add extra timing margin, additional "dummy stages" are inserted before and

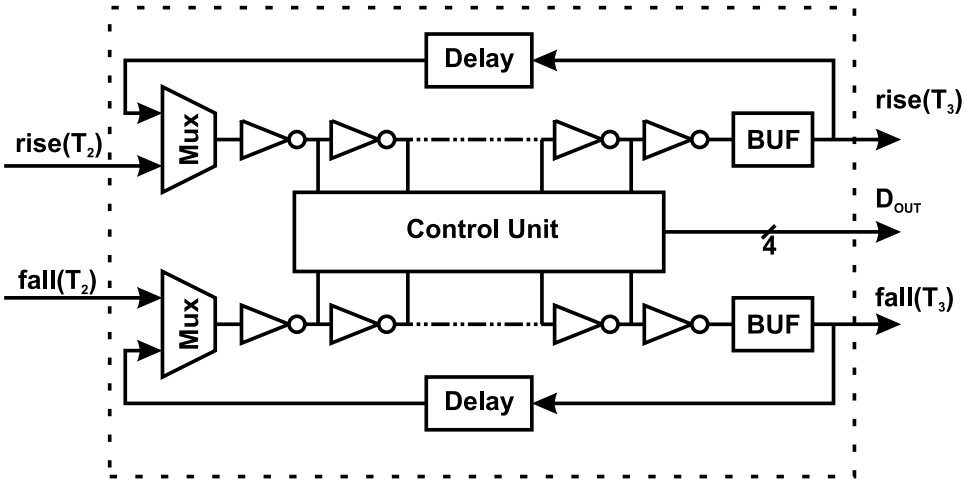


Figure 3.6: Functional block diagram of the TDC/DTC.

after the main stages.

When a pseudo-differential pulse is received, the fall pulse passes through the dummy stages, but the rise pulse passes through the dummy stages and $D_{out}[k-1]$ out of 16 stages, where $D_{out}[k]$ is defined in Fig. 3.4. Therefore:

$$\text{rise}(T_3[k]) = \text{rise}(T_2[k]) + t_{\text{dummy stages}} + D_{out}[k-1]\Delta \quad (3.20)$$

$$\text{fall}(T_3[k]) = \text{fall}(T_2[k]) + t_{\text{dummy stages}} \quad (3.21)$$

Thus, the subtraction operation is implemented as

$$\Delta T_3[k] = \Delta T_2[k] - D_{out}[k-1]\Delta \quad (3.22)$$

After the first time through the inverter stages, and after a small delay, the result of the subtraction is fed back through the same inverter stages to quantize the time between the two pulses (i.e., the width of the pseudo-differential

pulse) in terms of the number of inverter stages:

$$D_{out}[k] = \left\lfloor \frac{\Delta T_3[k]}{\Delta} \right\rfloor \tag{3.23}$$

### 3.2.6 Delay Control Unit

The main responsibilities of the DCU are to properly startup the loop after global reset and also prevent unwanted pulse drifts through dynamically adjusting the excess loop delay. The two components of the DCU are

1. Phase Detector
2. Excess Delay

The role of the Excess Delay block is to calibrate and "equalize" the loop delay to maintain constant sampling interval that matches the external reference clock over process, temperature, and supply variation as well as modulation by the input itself. Because sampling occurs effectively at the fall edge of $T_4$ (as shown in Fig. 3.4) and fall($T_3[k]$) is a function of the $k$th sample ($\Delta T_{in}[k]$), as the input grows larger, fall($T_3$) arrives later in time, and therefore the Excess Delay block must add a smaller delay to $T_3$ (to get $T_4$) to counteract the change. This will ensure that sampling instances, i.e., fall($T_4$) are approximately uniformly-spaced. Equivalently:

$$T_s \approx \text{fall}(T_4[k+1]) - \text{fall}(T_4[k]) \tag{3.24}$$

$$= t_d + \Delta T_{in}[k] + t_{d,Excess\ Delay}, \quad \text{where} \tag{3.25}$$

$$t_d = t_{d,VTC/Adder} + t_{d,Phase\ Detector} + t_{d,DTC} \tag{3.26}$$

$$\tag{3.27}$$

Where $t_{d,block}$ is the propagation delay through the named *block* (delay experienced by both rise and fall pulses). Therefore, the Excess Delay block must add an additional propagation delay according to the following formula:

$$t_{d,Excess\ Delay} \approx T_s - (t_d + \Delta T_{in}[k]) > 0. \tag{3.28}$$

Since a high amount of oversampling is used and drift is assumed to be slow, a slow tracking loop may be used to follow the changes, by using the bang-bang control signals provided by the Phase Detector block (*lead* and *lag* outputs).

The Phase Detector block compares the $f$ pulses at each cycle with the rising edge of a clock with frequency $f_s = 1/T_s$. This activates either a *lead* or *lag* signal that is then applied to the excess delay block of the modulator to increase or decrease the loop delay of both $r$ and $f$ pulses through the excess delay block. The excess delay block overcompensates every time a *lead* or *lag* signal is present. Mathematically,

$$lead = \mathcal{I}\left(\text{fall}(T_4(k)) < kT_s - T_{d,hyst}\right) \tag{3.29}$$

$$lag = \mathcal{I}\left(\text{fall}(T_4(k)) > kT_s + T_{d,hyst}\right) \tag{3.30}$$

where $\mathcal{I}(\cdot)$ is the indicator function.

With these two bits (*lead*, and *lag*) the Excess Delay block adjusts the excess loop delay by 0 (no adjustment) or $\pm T_{d,hyst2}$ in each cycle. Note $T_{d,hyst2} > T_{d,hyst}$. This is in addition to a programmable fixed delay for a wide tuning range of $f_s$. By using this approach, one can ensure that the average oversampling frequency is always locked to an external $f_s$ clock. It is important to recognize that the fluctuation in the sampling time of this time-based ADC does create errors that are similar in nature to noise artifacts generated by noisy clocks.

After releasing the global reset signal, the Phase Detector provides an initial zero-width pseudo-differential pulse to startup the circuit. In normal mode, the Phase Detector passes through the input pulse to the output with a constant amount of delay ($t_{d,\text{Phase Detector}}$) in Fig. 3.4.

## 3.3 Summary

In this chapter, I propose a novel time-based delta-sigma ADC quantizing pseudo-differential pulse width. I explain the system model and mathematically model the system. The advantages of the structure are the following:

1. Utilization of time-based processing in the pulse domain enables mostly-digital (two-level) circuits for processing the analog quantity, with the benefit of improved resolution with CMOS scaling.

2. At the input, the ADC accepts a voltage signal, which is internally converted to a pseudo-differential pulse. All subsequent processing is per-

formed on pulses whose widths encode the signal information.

3. The asynchronous (and self-oscillating) modulator can be synchronized to an external clock through a loop delay calibration unit. This scheme provides a known time base, and removes harmonics due to non-uniform sampling which arises from input-dependent time drift in the asynchronous loop. It also reduces the need for an accurate clock network.

4. The width of the pulse is quantized by a delta-sigma modulator with a flash time-to-digital converter (TDC) as the internal ADC.

5. A novel multi-bit invertible TDC/DTC (ADC/DAC) is possible thanks to time-domain processing. This approach reduces area.

6. It also removes the sample-and-hold amplifier and replaces it with a continuous-time comparator which simplifies the circuit even further.

In the next chapter, I present the behavioral model of the proposed modulator in MATLAB/Simulink along with plots showing the operation of the modulator. I also investigate and model non-idealities associated with different sub-blocks.

# Chapter 4

# Behavioral Modeling of Time-Based $\Delta\Sigma$ ADC

To study the operation of the proposed time-based $\Delta\Sigma$ ADC, a behavioral model is created in MATLAB/Simulink. Every block in the model calculates and propagates the rise and fall times of the pseudo-differential pulse in each cycle. Every block is modeled according to the equations described in Chapter 3. With this model, quick exploration of different parameters in the system is possible, thereby allowing a designer to understand the system from a high-level before making decisions about circuit implementation of the individual blocks.

## 4.1 Functional Model

A top-level Simulink block diagram of the proposed time-based $\Delta\Sigma$ ADC is shown in Fig. 4.1. Individual sub-blocks of the model are shown in Figs. 4.2, 4.3, 4.4, and 4.5. The model uses a fixed time-step solver.

### 4.1.1 VTC/Adder Model

To model the time-varying sampling operation, the VTC/Adder block (Fig. 4.2) converts from continuous-time to discrete-time by evaluating a math-

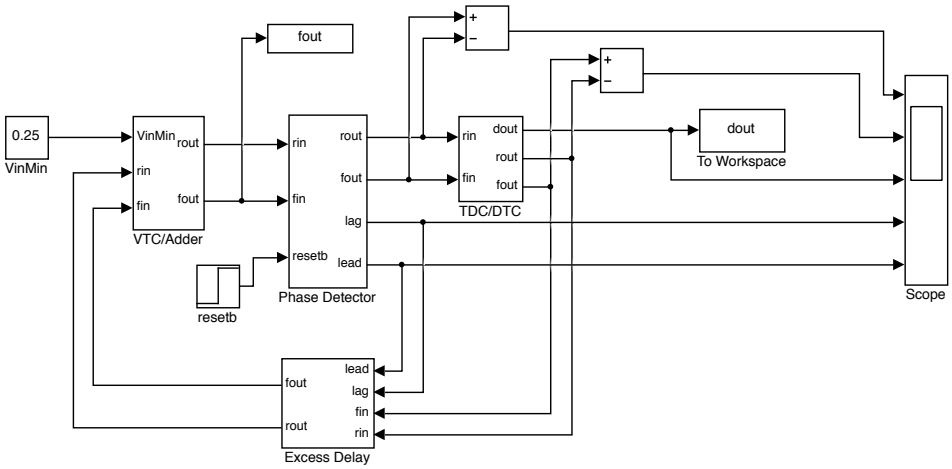


Figure 4.1: Top-Level Simulink Model of the proposed time-based $\Delta\Sigma$ ADC.

ematical sine function at the true sampling instance in each cycle ($t = f_{in}(k)$). This is the reason for the absence of an input sine wave in the model of the proposed ADC. Instead, the sine function is evaluated internally in the VTC/Adder block.

### 4.1.2 Phase Detector Model

The model for the phase detector (Fig. 4.3), keeps track of an ideal external reference clock with period $T_s$. In each cycle, the reference is incremented by $T_s$ and compared to the edge of $f_{in}$ input to the Phase Detector block. Recall, this is the edge that corresponds to sampling and needs to be uniformly spaced from one cycle to the next. If $f_{in}$ is within $\pm T_{d,hyst}$ of the ideal edge, then *lead* and *lag* are both 0. Otherwise, one of *lead* or *lag* is asserted and the Excess Delay block compensates by adding more or less delay,

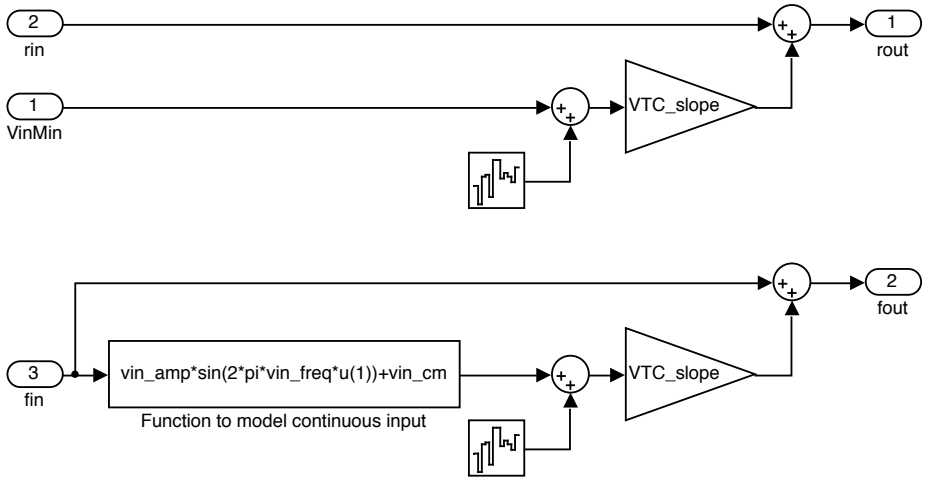


Figure 4.2: Simulink model for the VTC/Adder block of the proposed time-based $\Delta\Sigma$ ADC.

respectively. Besides generating *lead* and *lag* signals, the Phase Detector block is responsible for startup with a zero width pulse, i.e., same edges for $r_{out}$ and $f_{out}$ (in this case ideal clock). Under normal operation, this block only adds a fixed delay to both rise and fall pulses, as evident in the model of Fig. 4.3.

### 4.1.3 TDC/DTC Model

The TDC/DTC block is modeled as shown in Fig. 4.4. In the DTC phase, in addition to adding fixed delay ($t_{d,DTC}$) to both edges, this block delays the $r_{in}$ edge by $T_{LSB} \cdot D_{out}[k-1]$, effectively shortening the resulting pseudo-differential pulse by the same amount. In the TDC phase, the output of the pseudo-differential pulse from the DTC phase is quantized. This requires taking the time difference between, $f_{out}$ and $r_{out}$, the fall and rise pulses from

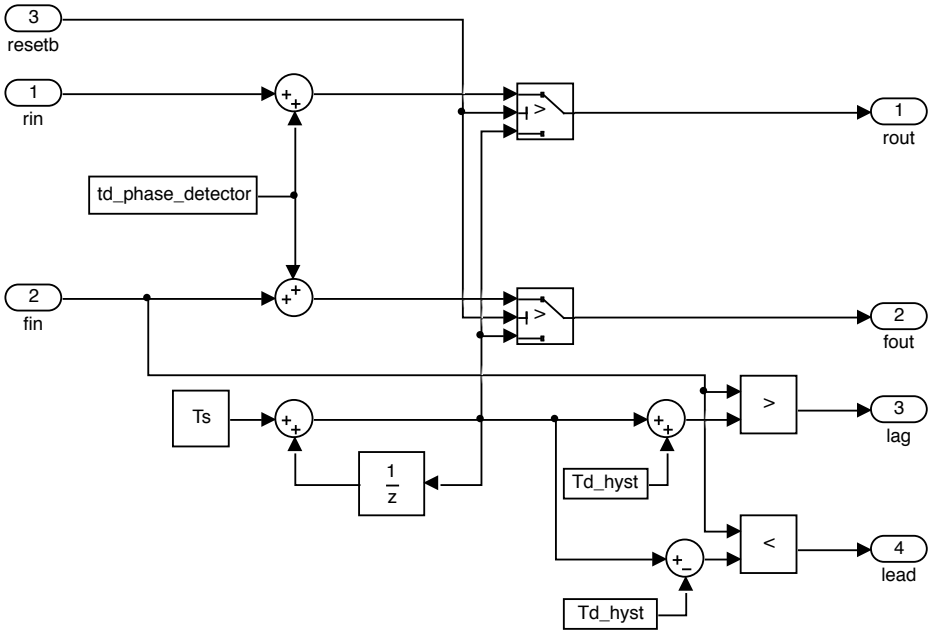


Figure 4.3: Simulink model for the Phase Detector block of the proposed time-based $\Delta\Sigma$ ADC.

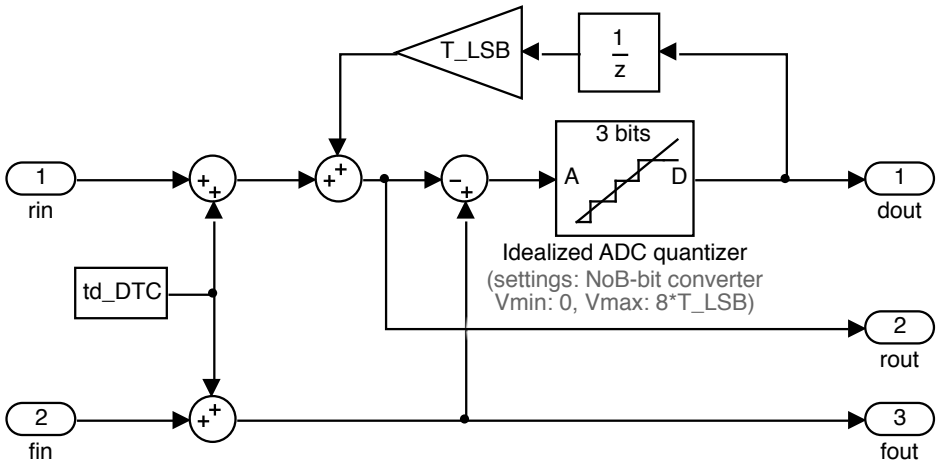


Figure 4.4: Simulink model for the TDC/DTC block of the proposed time-based $\Delta\Sigma$ ADC.

the DTC phase.

### 4.1.4 Excess Delay Model

The Excess Delay block is modeled according to the block diagram shown in Fig. 4.5. As described in the description of the Phase Detector block, this block compensates for pulse drift due to various delays and the delay modulation due to the input itself. In response to *lead* and *lag* signals generated in the Phase Detector block, the Excess Delay block adds or subtracts delay to both edges such that $f_{out}$ becomes approximately uniformly spaced from cycle to cycle. This effect is seen in the simulation results in Section 4.1.5 below.

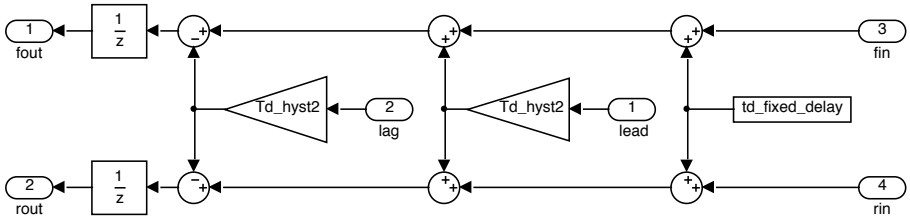


Figure 4.5: Simulink model for the Excess Delay block of the proposed time-based $\Delta\Sigma$ ADC.

Table 4.1: Parameters used in the behavioral simulation.

| Parameter | Value | Units |
|---|---|---|
| Ts | 6.94 | ns |
| vin_freq | 200 | kHz |
| vin_amp | 0.18 | V |
| vin_cm | 0.482 | V |
| VTC_slope | 1.5 | nV / s |
| td_phase_detector | 0.5 | ns |
| td_DTC | 2.7 | ns |
| td_fixed_delay | 3.025 | ns |
| T_LSB | 100 | ps |
| NoB | 3 | - |
| trip_en | 0/1 | - |
| Td_hyst | trip_en & 0.3 | ns |
| Td_hyst2 | trip_en & 0.4 | ns |

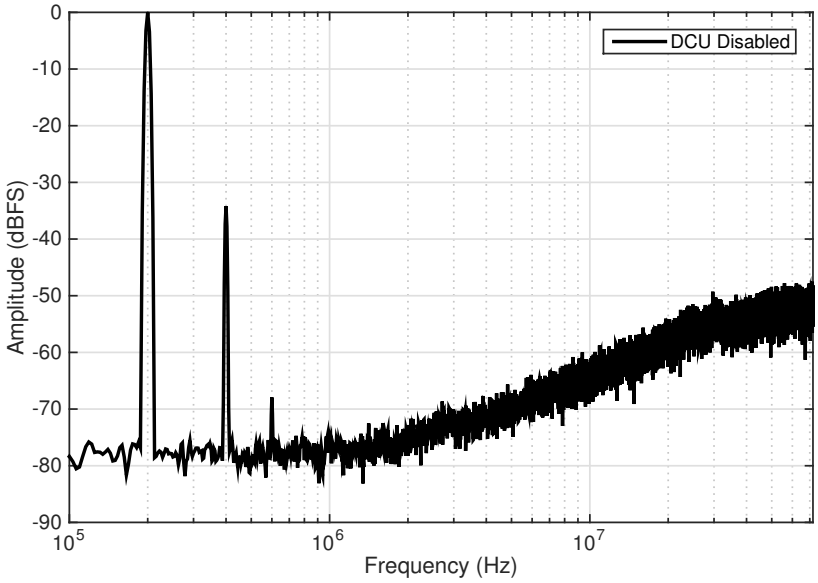


Figure 4.6: Averaged FFT Spectrum of the behavioral model with DCU disabled. Odd harmonics are due to input-dependent modulation of sampling interval when the DCU is disabled.

### 4.1.5 Simulation Results

In this section, simulation results showing the operation of the proposed time-based $\Delta\Sigma$ ADC is presented. The parameters used in the simulation are listed in Table 4.1. To understand the effectiveness and need for the DCU and loop delay compensation, Td_hyst and Td_hyst2 are set to zero first. The resulting spectrum is shown in Fig. 4.6, in which dominant third harmonic of the input sine wave is observed. This is caused by the input-dependent modulation of sampling interval, and results in a total harmonic distortion (THD) of -34 dB. Therefore, the non-uniform sampling needs to be made uniform.

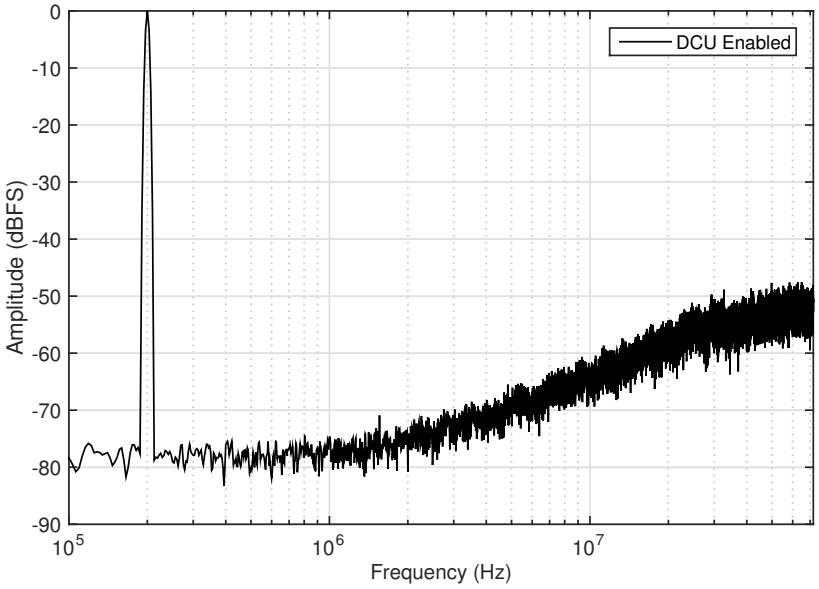


Figure 4.7: Averaged FFT Spectrum of behavioral model with DCU enabled.

If the DCU is enabled by setting Td_hyst and Td_hyst2 to nonzero values with Td_hyst2 > Td_hyst, the spectrum of Fig. 4.7 is obtained. Note: the odd harmonics are removed. With the DCU enabled, the sampling interval becomes approximately uniform. A typical waveform showing the operation of the time-based $\Delta\Sigma$ ADC is shown in Fig. 4.8. As illustrated, when the input is at its highest, the pulse widths at the phase detector output and the DTC output are their highest values. Higher pulse widths create extra delay: therefore, there will be a larger density of *lag* signals. On the contrary, when the input is at its lowest, the density of *lead* is highest.

One measurable quantity to better understand the effect of the DCU

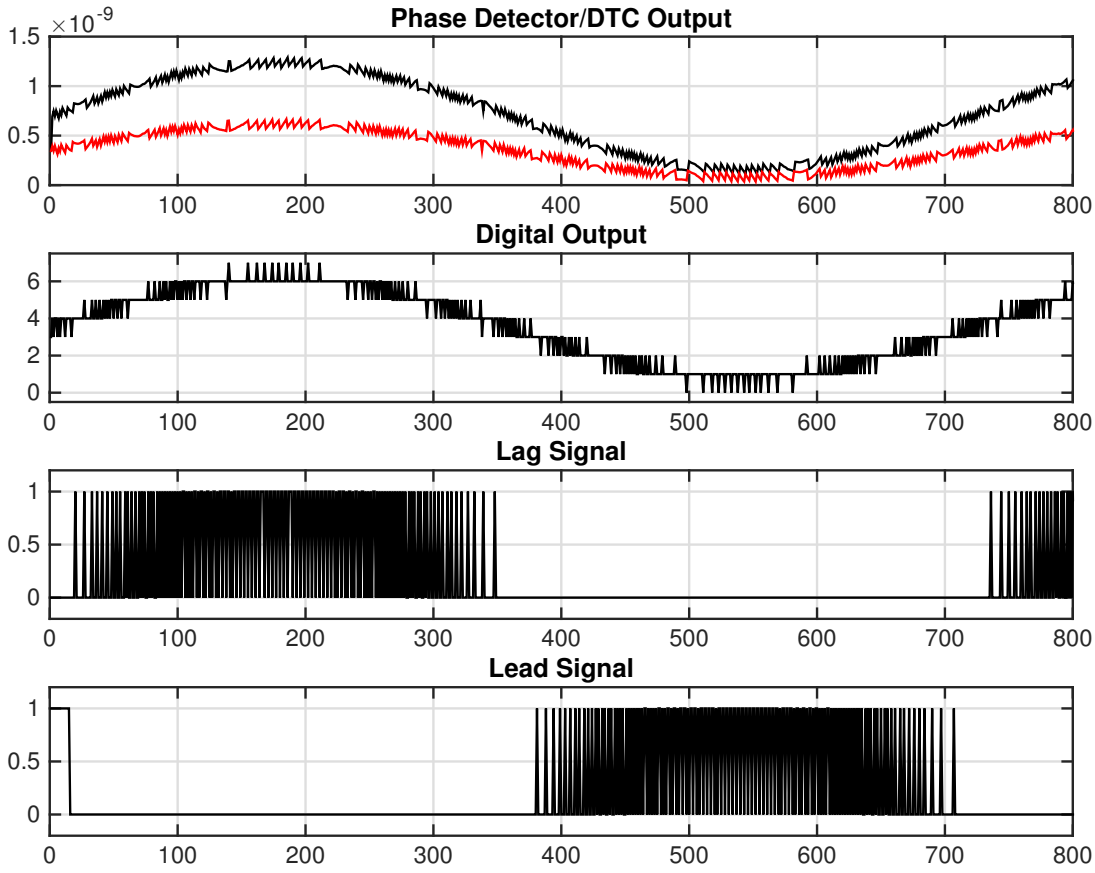


Figure 4.8: Waveforms for different signals in the behavioral model of the proposed time-based $\Delta\Sigma$ ADC.

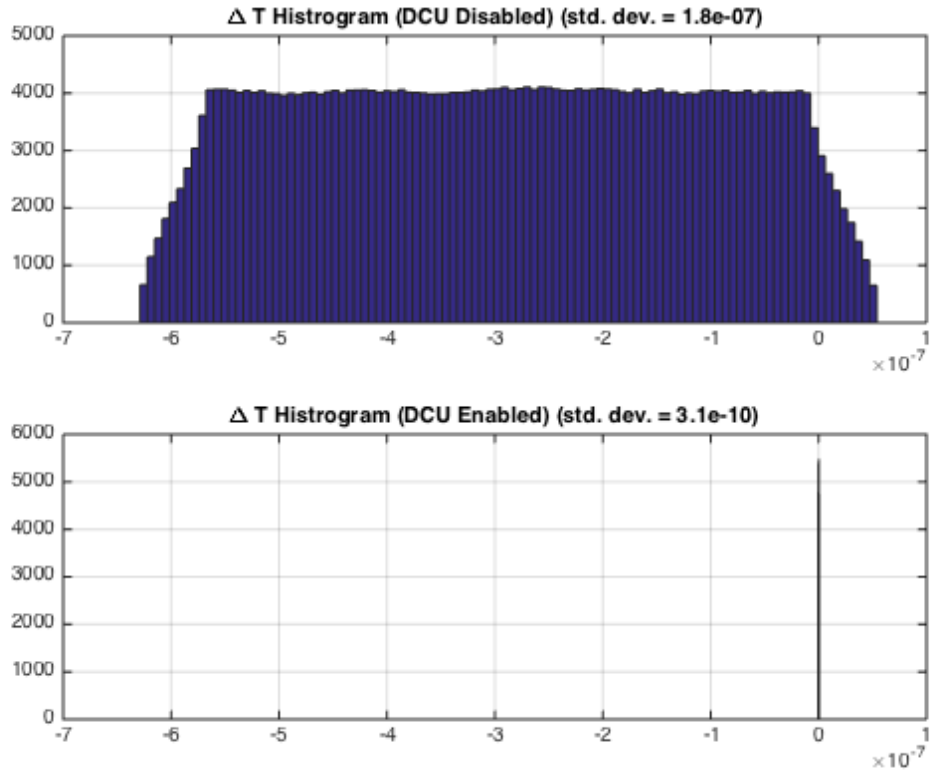


Figure 4.9: Histograms for $\Delta T = t(f_{\text{out, phase detector}}) - k \cdot T_s$ showing the deviation from ideal sampling times $k \cdot T_s$ when the DCU is disabled/enabled.

in creating conditions for uniform sampling is the standard deviation of

$$\Delta T = t(f_{\text{out, phase detector}}) - k \cdot T_s$$

Observe the histogram in Fig. 4.9, shows a standard deviation that is more than two orders of magnitude smaller when the DCU is enabled, as compared to the DCU disabled case. It is now clear how the DCU drastically reduces variations from ideal/uniform sampling times ($k \cdot T_s$). The histogram of the DCU enabled case is shown independently in Fig. 4.10.

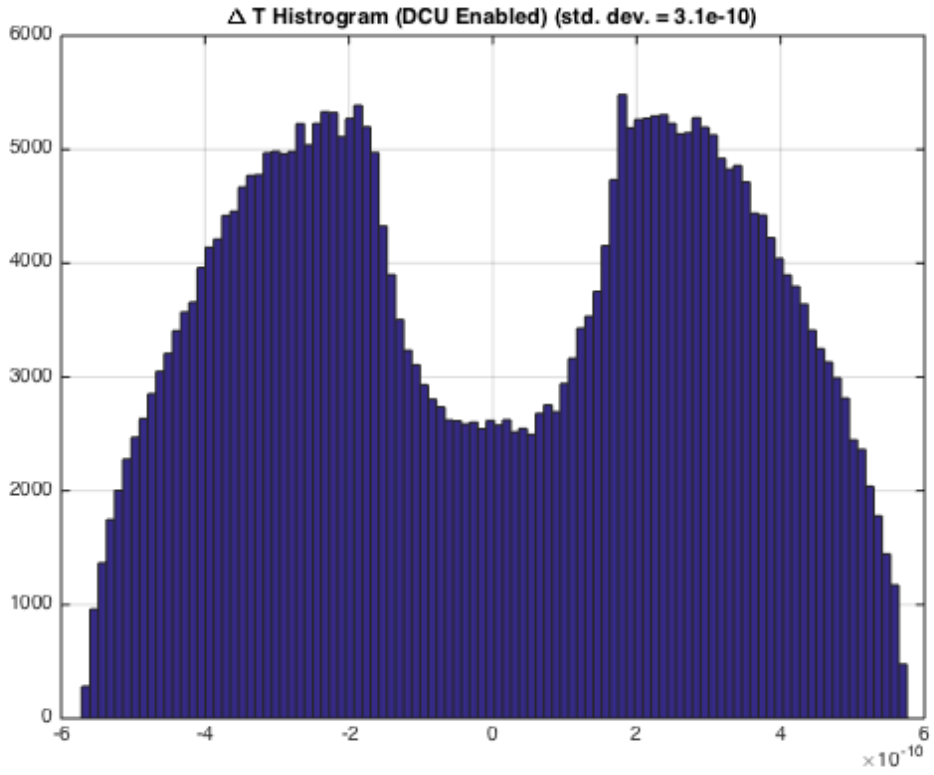


Figure 4.10: Histogram for $\Delta T = t(f_{\text{out, phase detector}}) - k \cdot T_s$ showing the deviation from ideal sampling times $k \cdot T_s$ when the DCU is enabled.

## 4.2 Modeling Sources of Nonlinearity

Prior analysis and simulations assumed all circuits/sub-blocks in the proposed time-based $\Delta\Sigma$ ADC are linear. In this section, the effect of nonlinearity in different circuit blocks is studied.

Conventional multi-bit $\Delta\Sigma$ modulators are widely known to exhibit nonlinearity primarily in the presence of DAC nonlinearity, and secondarily in the presence of ADC nonlinearity. These nonlinearities arise from the mismatch between unit elements in the multi-bit DAC or multi-bit ADC. Single-bit DACs and ADCs are linear by definition. While the nonlinearity due to the ADC is attenuated according to the noise transfer function (NTF), the nonlinearity due to the DAC passes through, i.e., according to the signal transfer function (STF). Therefore, among the two contributors of modulator nonlinearity (ADC and DAC), the DAC nonlinearity is the larger contributor. Therefore, the mismatch in DTC (i.e., DAC) and TDC (i.e., ADC) are analyzed in Sections 4.2.1 and 4.2.2.

Any nonlinearity outside of the modulator loop, appears at the ADC's output without shaping, or more precisely according to the signal transfer function (STF). Thus, VTC/Adder nonlinearity can be an important source of nonlinearity, and is therefore analyzed in section 4.2.3.

### 4.2.1 Modeling DTC Element Mismatch

To understand the effect of DTC element mismatch, the Simulink model for the TDC/DTC is modified (see Fig. 4.11). A lookup table is added in the

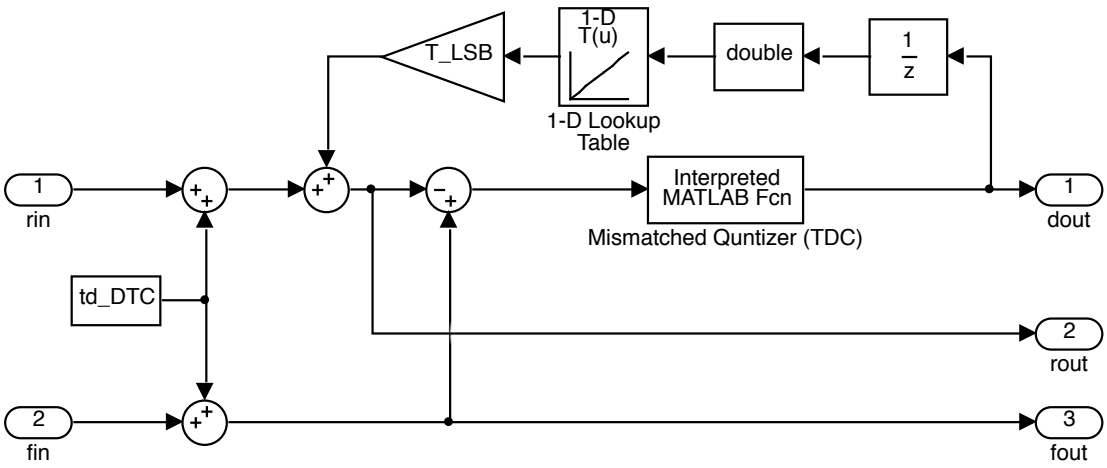


Figure 4.11: Simulink model for TDC/DTC including the element mismatch for DTC/TDC phases.

feedback path that models the DTC operation. The $2^{NoB}$ entry lookup table, maps each output code (0 to $2^{NoB} - 1$) to a slightly perturbed value of

$$T[u] = u + \epsilon[u], \qquad u = 0, 1, \ldots, 2^{NoB} - 1$$

where $\epsilon[u]$ is the normalized mismatch for code $u$ given by

$$\epsilon[u] \sim \mathcal{N}(0, \sigma_{mismatch}).$$

Generating three random vectors $\bar{\epsilon}$ with an element mismatch of $\sigma = 10\%$ of the unit delay, and simulating the modulator, the three spectra shown in Fig. 4.12 are obtained. Note the variation of harmonic content in the different realizations of mismatch. Based on these results, it is clear that DTC nonlinearity is a dominant source of overall modulator nonlinearity.

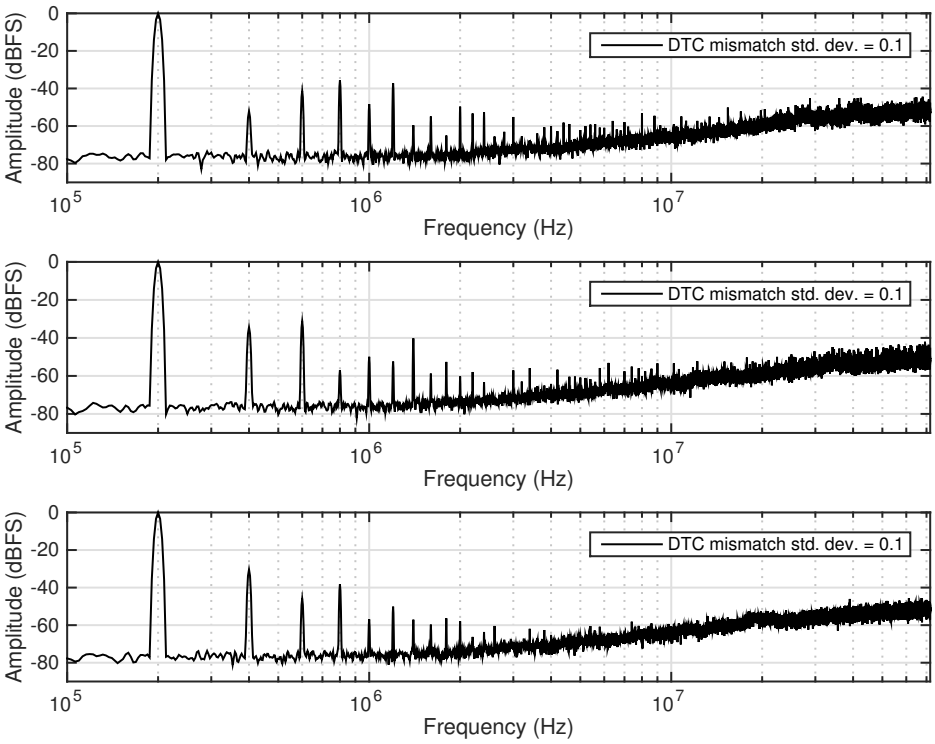


Figure 4.12: Output spectrum showing the effect of DTC element mismatch with $\sigma = 10\%$ for 3 different random mismatch vectors.

### 4.2.2 Modeling TDC Element Mismatch

Another modification to the ideal DTC/TDC model that was shown in Fig. 4.11), was to replace the ideal ADC with one that takes arbitrary boundaries for the flash-ADC. The ADC is modeled as an interpreted MATLAB function, that evaluates the following expression:

```
sum(u(1) > tdc_boundaries(:))-1
```

where `tdc_boundaries(:)` contains the vector of ADC decision boundaries. Thus, it is possible to create boundaries that are not perfectly linear and are perturbed from their ideal (linear) boundaries.

Figure 4.13 shows the effect of 10% mismatch between delay elements in the TDC. Note how the nonlinearity of the overall modulator is more than 20 dB (10 times) better than the same level of mismatch in the DTC. This is expected, since the ADC (in this case TDC) nonlinearity is shaped by the noise transfer function (NTF), whereas the DAC (in this case DTC) nonlinearity is shaped by the signal transfer function (STF). Recall that at low frequency, STF is approximately unity and NTF is $\ll 1$.

The plot shown in Fig. 4.14 shows the trend for total harmonic distortion (THD) vs. TDC and DTC mismatch. This is further verification that DTC nonlinearity is more important than TDC nonlinearity.

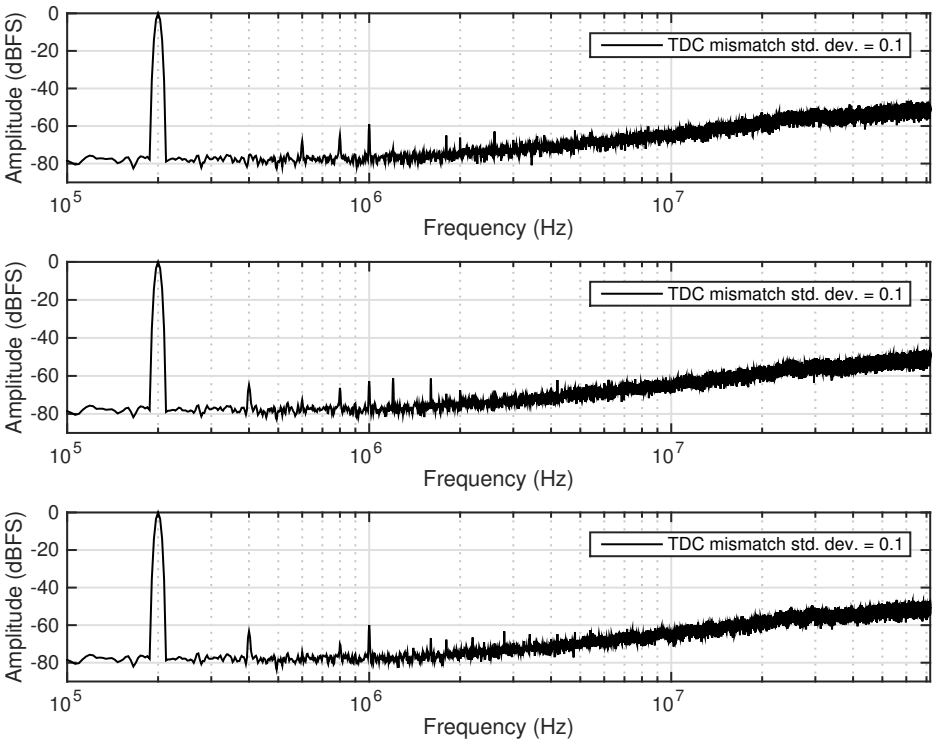


Figure 4.13: Output spectrum showing the effect of TDC element mismatch with $\sigma = 10\%$ for 3 different random mismatch vectors.

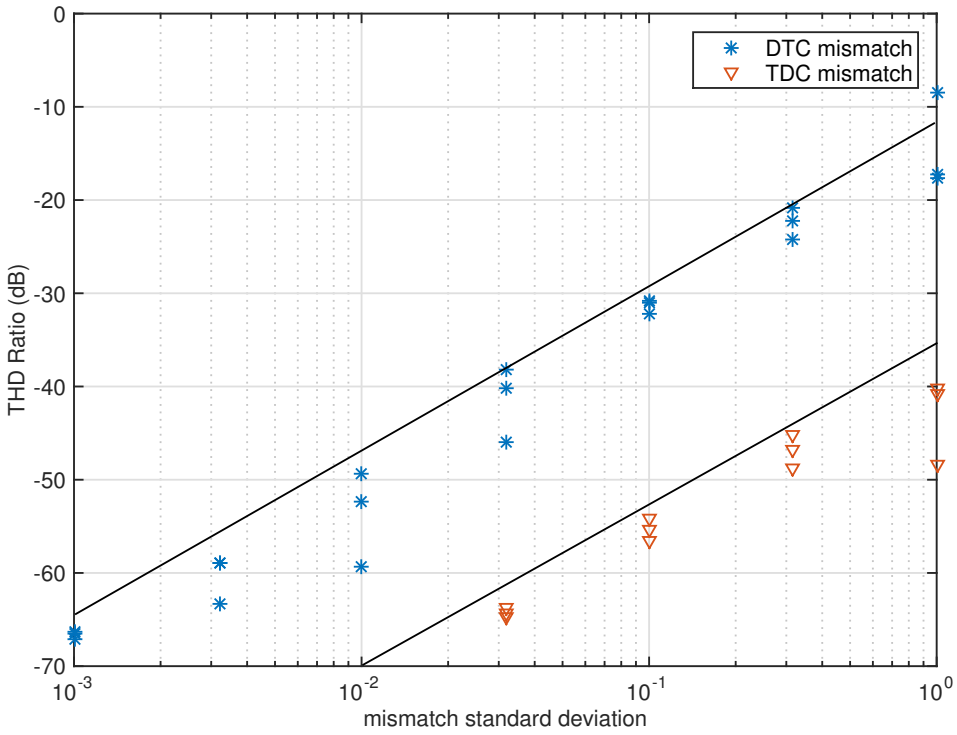


Figure 4.14: Total Harmonic Distortion vs. $\sigma$ of DTC and TDC element mismatch. Note DTC mismatch results in more than 20 dB higher THD relative to TDC mismatch with comparable standard deviation.

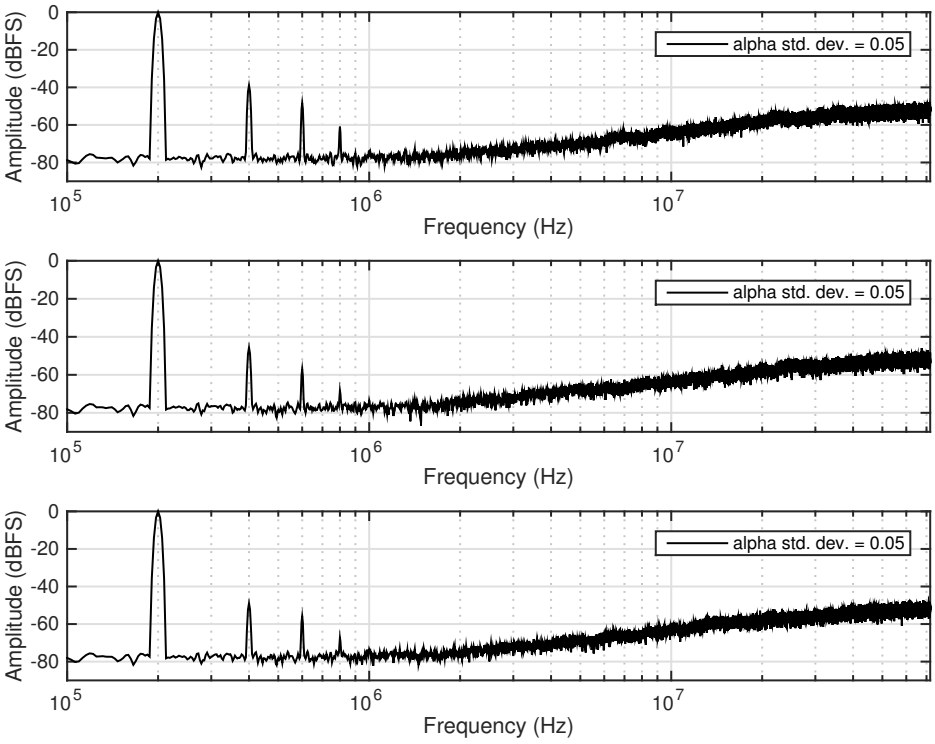


Figure 4.15: Output spectrum showing the effect of VTC/Adder nonlinearity for 3 different random nonlinearity coefficient ($\alpha$) vectors.

### 4.2.3 Modeling VTC/Adder Nonlinearity

The final source of nonlinearity that is considered in this analysis is VTC/Adder nonlinearity. Assume that the VTC/Adder comparators have not only a fixed delay $\alpha_0$, but also, input-dependent delay terms $f(V_{in})$:

$$t_{d,VTC/Adder} = \alpha_0 + f(V_{in}) \quad (4.1)$$

$$= \alpha_0 + \alpha_1 V_{in} + \alpha_2 V_{in}^2 + \ldots + \alpha_N V_{in}^N \quad (4.2)$$

Then the nonlinearity will be directly transferred to the output. This is seen in Fig. 4.15.

## 4.3 Summary

I conclude that while TDC nonlinearity is not dominant, DTC nonlinearity poses a large bottleneck to overall modulator linearity. This is similar to conventional $\Delta\Sigma$ modulators, which may be mitigated using several techniques:

1. Dynamic Element Matching
2. Calibration of DAC elements
3. Digital Post-Correction

In Chapter 7, I show how to use digital post-processing to calibrate the mismatch of the DAC elements. The next chapter presents the design and characterization of the first prototype chip using the proposed time-based $\Delta\Sigma$ ADC architecture.

# Chapter 5

# First Generation Chip

## 5.1 Introduction

In Chapter 3, I presented the proposed time-based $\Delta\Sigma$ ADC architecture. Then in Chapter 4, I presented the system model in MATLAB/Simulink. In this chapter, I discuss the design of the first-generation chip that was designed, fabricated, and tested in collaboration with Dr. Woo Young Jung while he was a Ph.D. student at The University of Texas at Austin. The first-generation ADC chip was fabricated in TSMC's 180 nm digital CMOS process.

In this chapter, I present the modulator design, test methodology and experimental results for the 180 nm chip. I analyze the results and discuss sources of impairment in detail.

---

This chapter is based in part on W. Jung, Y. Mortazavi, B. L. Evans, and A. Hassibi, "An all-digital PWM-based ADC with an inherently matched multi-bit quantizer," in *Proc. 2014 IEEE Custom Integrated Circuits Conference (CICC)*. IEEE, 2014, pp. 1-4. Authors Jung and Mortazavi are equal contributors. Authors Evans and Hassibi are supervisors and primary investigators of the work.

Table 5.1: First-Generation Chip Parameters.

| Parameter | Value | Units |
|---|---|---|
| Process | TSMC 180nm 6M 1P | - |
| Supply Voltage ($V_{DD}$) | 1.8 | V |
| Oversample Frequency ($f_s$) | 144 | MHz |
| Quantizer (TDC) Number of Bits | 3 | bits |
| DAC (DTC) Number of Bits | 3 | bits |
| TDC LSB ($\Delta$) | 80 | ps |
| $t_{\text{d,VTC/Adder}}$ | 2.1 | ns |
| $t_{\text{d,PhaseDetector}}$ | 0.57 | ns |
| $t_{\text{d,DTC}}$ | 1.24 | ns |
| $t_{\text{d,ExcessDelay}}$ (Average) | 2.8 | ps |
| Area | 0.0275 | $\text{mm}^2$ |

## 5.2 Circuit Implementation

The modulator for the first-generation chip has the parameters listed in Table 5.1. In the following sections, circuit implementations of the proposed architecture are described.

### 5.2.1 VTC/Adder

Recall from Chapter 3 that the VTC/Adder consists of two identical half circuits, each of which have a ramp generator and a continuous-time comparator. The circuit topology of the VTC/Adder is shown in Fig. 5.1.

The ramp generator consists of a wide-swing current source ($I_B$ = 200 $\mu$A), an integrating capacitor ($C_I$ = 110 fF), and digital switches to create a 0 to 640ps full scale $T_\Sigma[k]$ corresponding to a (0.28 V-0.68 V) linear range of $V_{in}$ with $V_{ref}$ = 0.28 V.

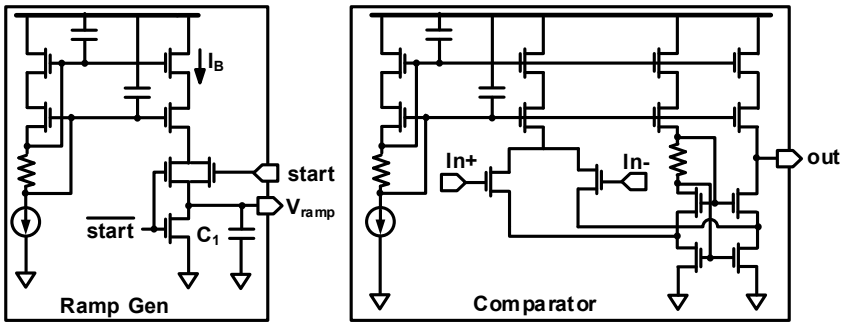


Figure 5.1: VTC/Adder circuit showing ramp generator and comparator.

The continuous-time comparator is a PMOS-input folded-cascode differential amplifier with a buffered output stage. The fixed overall latency is 2.10 ns ($t_{d,\mathrm{VTC/Adder}}$).

### 5.2.2 TDC/DTC

The TDC/DTC block performs the functions of both the ADC and the DAC in the first-order $\Delta\Sigma$ error feedback only structure. The unit delay array (with fixed time interval $\Delta = 80$ ps) is the common block to both the ADC and the DAC in time-domain. If the operation of these functions can be performed sequentially, then those blocks may be shared. Thus, a reusable structure of multi-bit subtraction and quantization can save area. This novel merged ADC/DAC is possible thanks to time-domain processing, which is not possible in voltage-domain processing.

The TDC/DTC operates in two phases. In phase 0 (DTC), the block

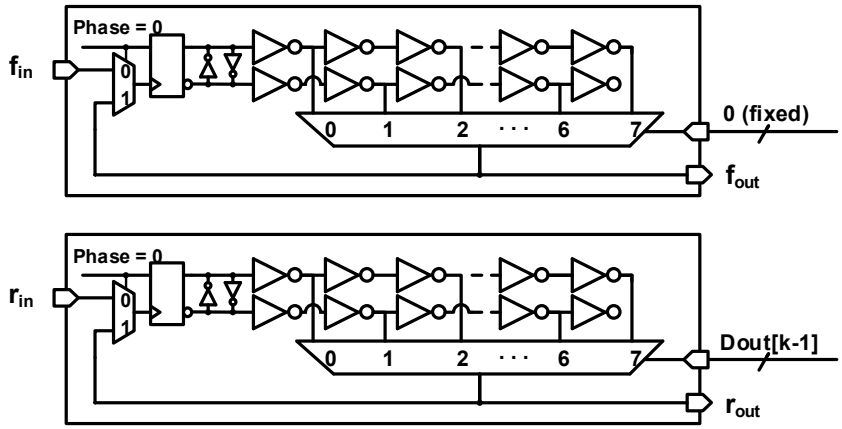


Figure 5.2: Digital-to-time converter (DTC) phase (phase 0) of the DTC/TDC circuit. Output pulse is recirculated through the block a second time for the TDC operation (phase 1).

shown in Fig. 5.2 performs time-based subtraction by delaying the $r$ pulse by a number of LSB time-units ($D_{out}[k-1]$ from the phase 1 output of the previous cycle). The $f$ pulse is passed through a replica structure that has fixed delay. The resulting pseudo-differential pulse ($T_3$) is output to the excess delay block and also recirculates through the TDC/DTC for phase 1 (TDC phase). The same unit delay elements are used in conjunction with flip-flops and thermometer-to-binary logic that implement the time-based quantizer shown in Fig. 5.3. This structure resembles a flash TDC which uses (inverting) delay lines and flip-flops to quantize a pulse to a number of unit delays (LSB). The use of inverting delay lines allows the LSB to be half as small, as compared to using non-inverting buffers (two inverters).

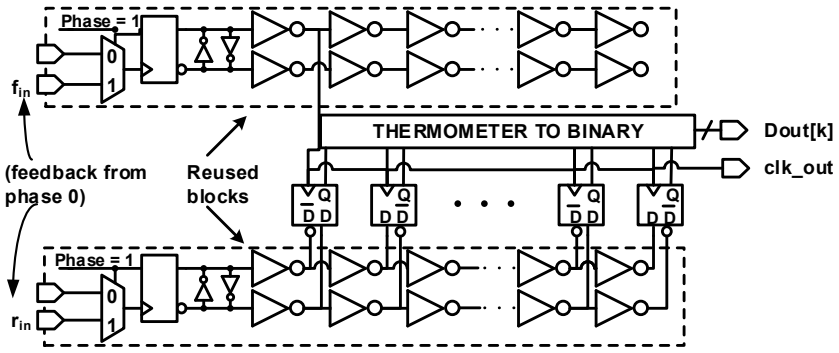


Figure 5.3: Time-to-digital converter (TDC) phase (phase 1) of the DTC/TDC circuit. Note the reuse of the unit delay elements from the previous phase (DTC).

Both the DTC and the TDC are 3-bits in this implementation, with a unit delay (LSB) of 80 ps.

### 5.2.3 Delay Control Unit (DCU)

As introduced in Chapter 3, the DCU consists of the Phase Detector that generates *lead* and *lag* signals which are used by the Excess Delay to adjust the loop delay to ensure uniform sampling interval is maintained each cycle.

The circuit for the Phase Detector is shown in Fig. 5.4. Initially, after reset, the external clock ($f_s$) is fed in the loop (as $r_2$ and $f_2$) as a zero width pulse. The phase detector signals a *lag* event if $f_1$ transitions high later than $Lag\_WD$ after the rising edge of $f_s$. Similarly, *lead* is signal if $f_1$ is more than

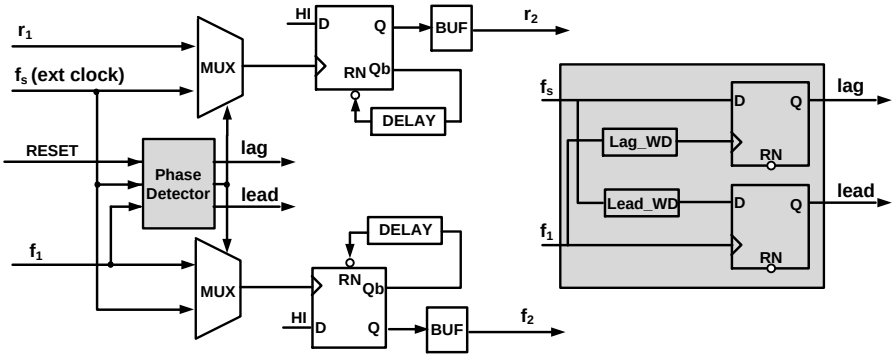


Figure 5.4: Delay Control Unit, including phase detector.

*Lead _WD* earlier than the rise of $f_s$.

### 5.2.4 Complete ADC System

The complete ADC system for the first-generation chip is shown in Fig. 5.5. To facilitate testing of the prototype and to enable fine control over the loop delay, a control voltage ($V_{ctrl}$) was added to the Excess Delay block. By varying the voltage on $V_{ctrl}$, additional delay may be obtained in the loop to account for process variation. In practice, calibration logic with a DAC would be required.

## 5.3 Test and Measurement

### 5.3.1 Test Methodology

To test the prototype ADC after fabrication, the following steps were followed:

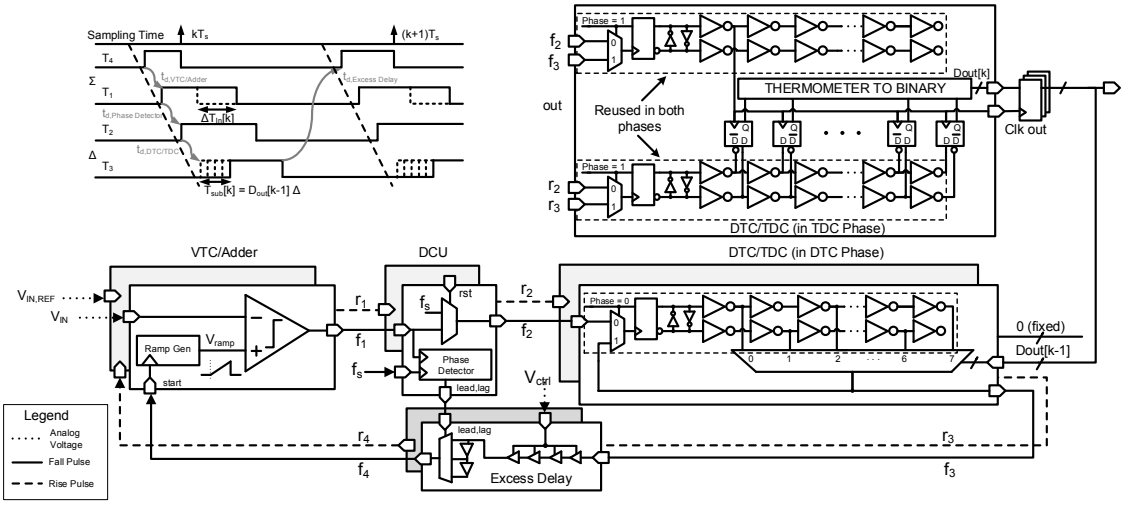


Figure 5.5: Complete PWM-based $\Delta\Sigma$ ADC System.

1. Package Selection: Choosing a package whose parasitics were not limiting to the intended operation frequency. In this case, the 64-Pin QFN package with 0.5mm pitch was selected.

2. Printed Circuit Board Design: Using the selected package several PCBs were designed to be able to provide all required supplies and signals without coupling excess noise from digital to analog.

3. Capture PCB Interface Design: The high-speed digital output data needed to be captured in memory with adequate signal integrity. A commercial FPGA board from Xilinx was chosen, and an adapter PCB was designed to interface with the FPGA board's high-speed connector (FMC-LPC).

4. Dicing: Separating the fabricated chips from the same shuttle submission

into individual chips. (This was done by VLSIP Technologies, Inc..)

5. Package Assembly and Wire Bonding: Mounting the chip to the QFN-64 package using conductive epoxy in the optimal location for wire bonding (in this case, off-center for optimizing inductance). A map of how to bond the chip pads to the package pins was designed, minimizing inductance and/or coupling capacitance on sensitive signals. PCB design and wire bonding diagram were co-designed and iteratively optimized. The gold wire diameter was chosen appropriately for the pads. Wire bonding was performed by VLSIP Technologies, Inc..

6. Soldering: Once the dicing, package assembly and wire bonding was done and the QFN unit were received, we soldered the QFNs onto the PCBs ourselves using a solder-stencil, solder paste, and a reflow oven with a controlled temperature profile. An open-source Reflow Oven Controller was built, which consisted of solid-state relays and a PIC microcontroller running a PID control loop.

7. FPGA Program Development: Developing a platform to capture the digital output from the ADC in real-time, and store it in block RAM in the FPGA. Then using a slower read-back loop, send the data to the PC using a USB UART transceiver.

8. Analyze the captured data in MATLAB.

A photo of the complete test setup is shown in Fig. 5.6.

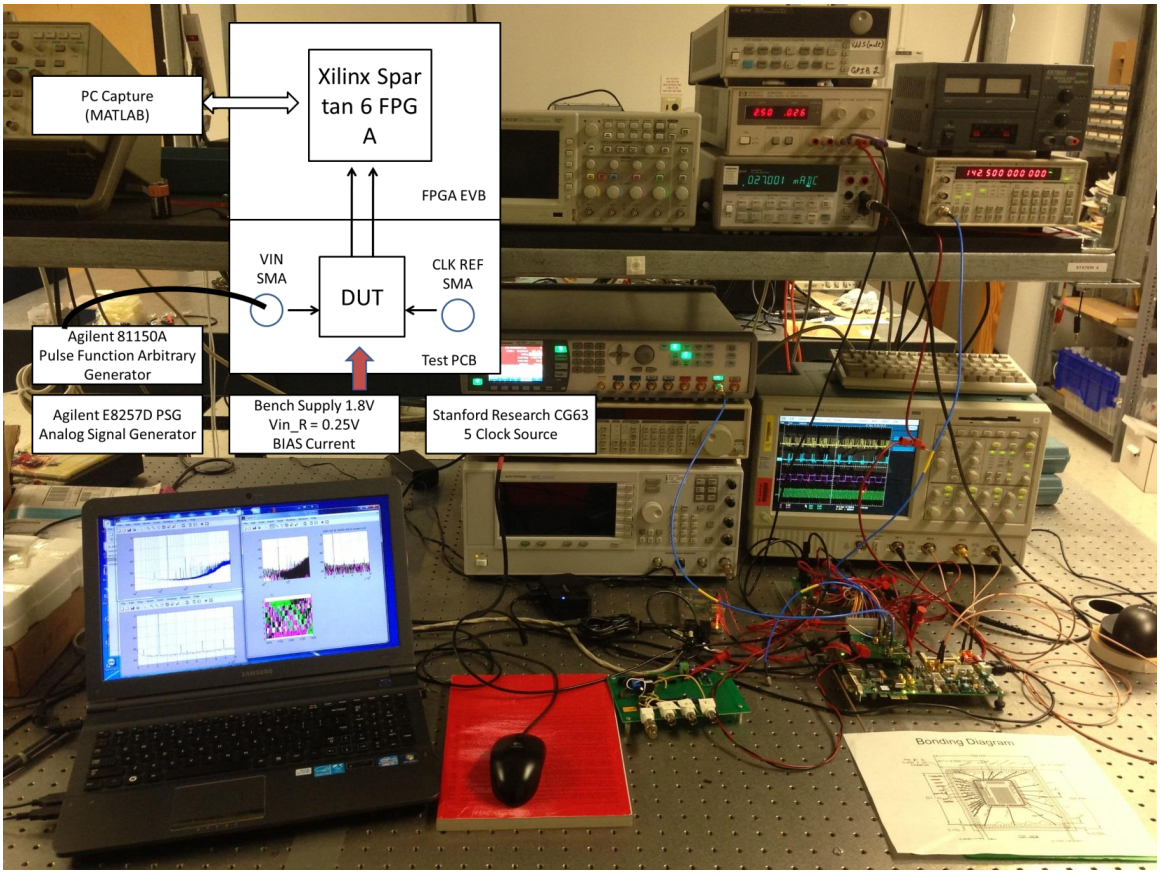


Figure 5.6: Photo of the test setup.

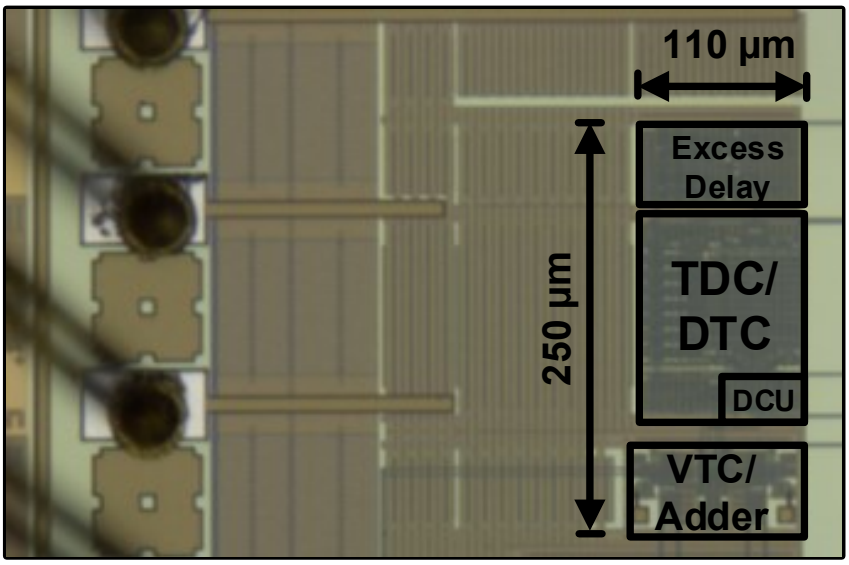


Figure 5.7: Die photo of the first-generation prototype ADC.

### 5.3.2 Die Photo

The die photo of the first-generation chip in TSMC 180nm 6M 1P digital CMOS process is shown in Fig. 5.7. The total core area is 250 $\mu$m $\times$ 110 $\mu$m = 0.0275 mm$^2$. The wirebonding diagram is shown in Fig. 5.8.

### 5.3.3 Experimental Results

The experiment results obtained on the first generation chip consist of power measurement and FFT magnitude spectra obtained on a sinusoidal input.

The total power consumption is 2.7 mW using a 1.8V supply, where

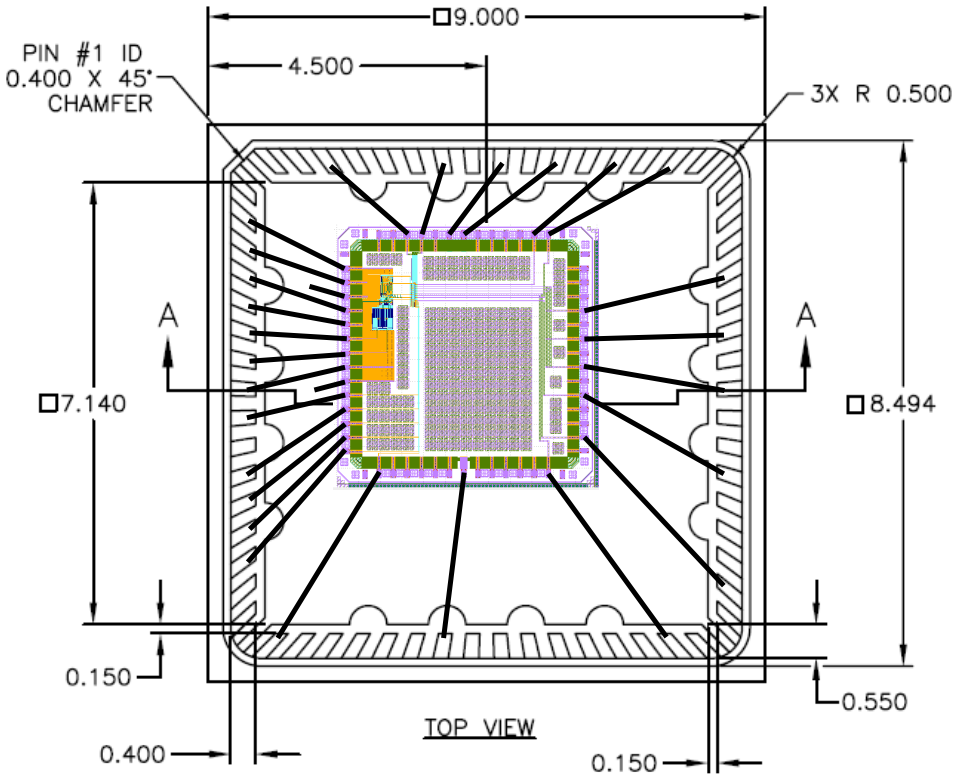


Figure 5.8: Wirebonding diagram for the first-generation prototype ADC. Die is shown larger than the scale suggests. Die is 2 mm×2 mm, QFN-64 package is 9 mm×9 mm.

Table 5.2: Summary of Measurement Results of First-Generation Chip

| Quantity | Value | Units |
|---|---|---|
| $f_s$ | 144 | MHz |
| OSR | 36 | - |
| BW | 2.0 | MHz |
| $f_{in}$ | 146.1 | kHz |
| $V_{in,pk-pk}$ | 400 | mV |
| SNR | 44.6 | dB |
| SNDR | 34.6 | dB |
| THD | -35.0 | dB |
| ENoB | 5.5 | bits |
| Power | 2.7 | mW |

2.52 mW is consumed by the VTC/Adder and the rest of the digital core consumes merely 180 $\mu$W.

Fig. 5.9 shows the time-domain waveform and the decimated output of the ADC for a 400 mV pk-pk (0 dBFS) and 146.1 kHz sinusoidal input converted with an oversampling frequency of $f_s = 144$ MHz. Fig. 5.10 shows the measured output spectrum. FFT length of 128K is used to generate the plot with a 7-term Blackman-Harris window. Fig. 5.11 shows the averaged FFT spectrum with 30 averages, and Fig. 5.12 shows the same but only from DC to $f_s/(2OSR)$. With OSR = 36, and BW = 2 MHz, SNR and SNDR were measured to be 44.6 dB and 34.6 dB, respectively. THD was measured to be -35.0 dB. These measurements results are also summarized in Table 5.2.

The spectrum shown in Fig. 5.10 shows an unusually high number of harmonic tones that are about -40 dB below the signal. These tones increase the total harmonic distortion (THD), and also limit the signal-to-noise-and-

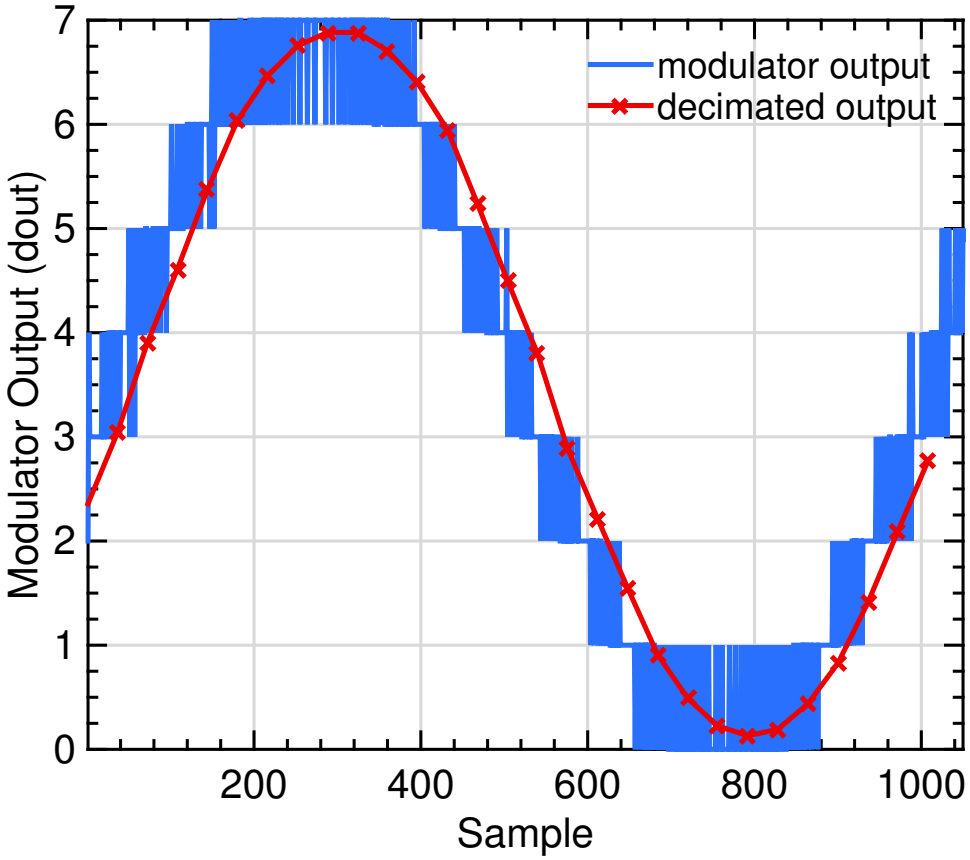


Figure 5.9: Time-domain waveform showing 1 cycle of a 146.1 kHz sine wave

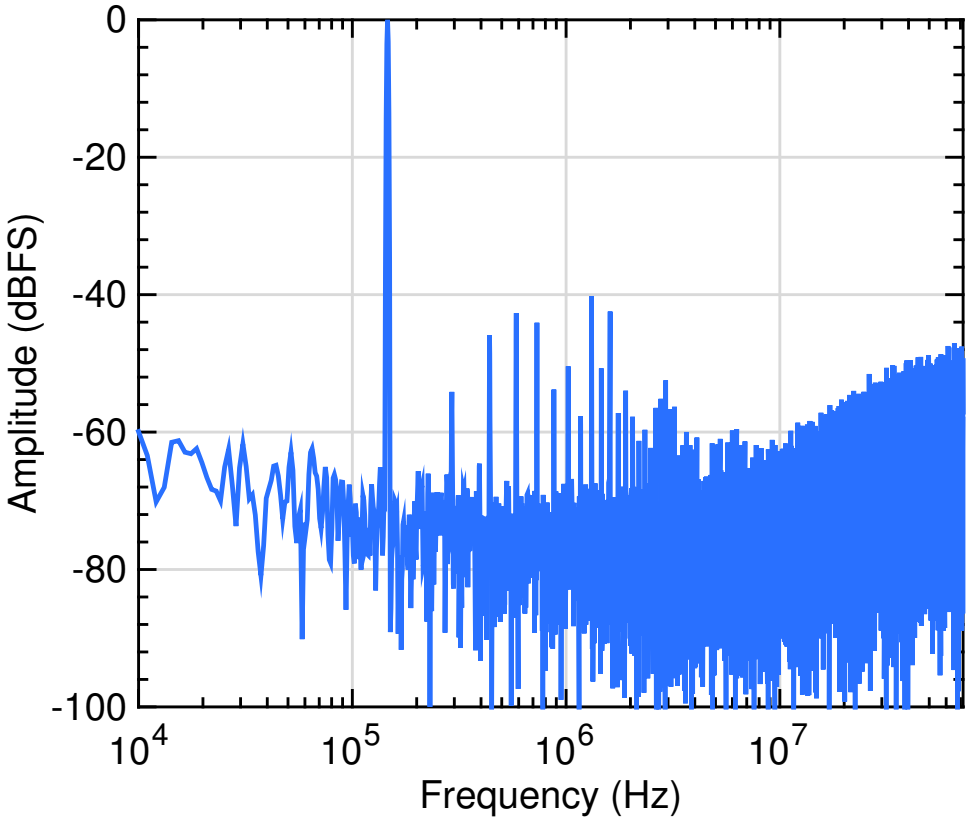


Figure 5.10: Magnitude FFT spectrum of a 146.1 kHz sinusoid sampled with $f_s = 144$ MHz

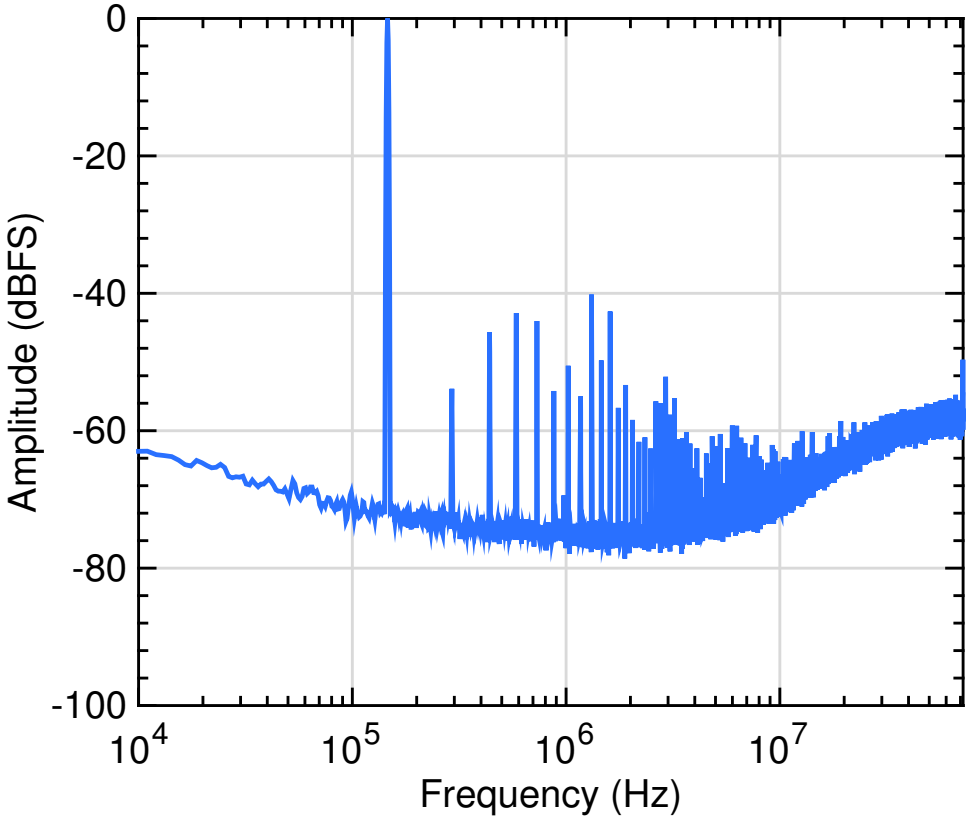


Figure 5.11: Averaged magnitude FFT spectrum of a 146.1 kHz sinusoid sampled with $f_s = 144$ MHz,$N_{avg} = 30$

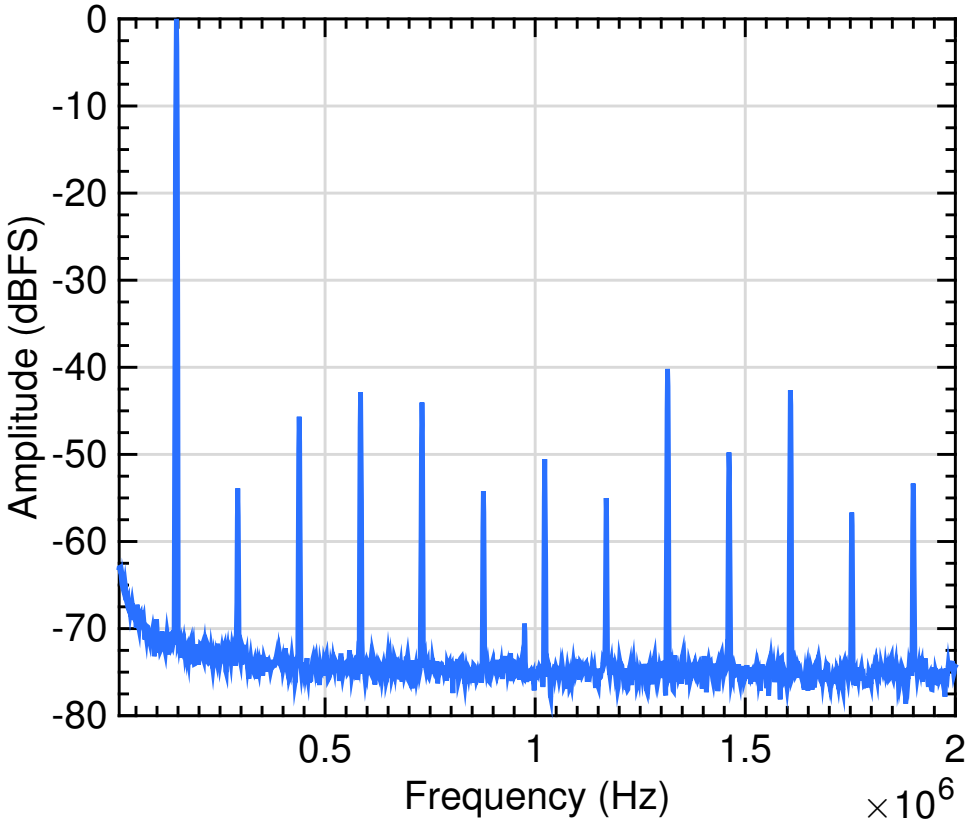


Figure 5.12: Averaged magnitude FFT spectrum of a 146.1 kHz sinusoid sampled with $f_s = 144$ MHz, OSR = 36, Showing DC to $\frac{f_s}{2 \cdot OSR}$

distortion ratio (SNDR). In Section 4.2, where I modeled different sources of nonlinearity, I discussed how DTC element mismatch could be a major source of nonlinearity in the overall modulator. Here, the observation seems to agree with that finding. In Chapter 7, I will analyze this effect in more detail and offer some insight for the exact source of this effect in the time-based $\Delta\Sigma$ ADC and propose an improved circuit that reduces this effect.

## 5.4 Summary

In summary, the first generation ADC prototype [36,37] of the proposed time-based $\Delta\Sigma$ ADC demonstrates the feasibility of the architecture. Given the high harmonic distortion in the measured data, which limits SNDR and ENoB, the source of the nonlinearity is a topic to be analyzed and mitigated in Chapter 7.

The next chapter describes the second generation prototype chip, which uses a more advanced process node, operates at a higher frequency and has a higher number of quantizer bits.

# Chapter 6

# Second Generation Chip

## 6.1 Introduction

After describing the first prototype ADC using TSMC 180 nm CMOS process in Chapter 5, I present the second prototype ADC in IBM 45 nm SOI process. Due to the smaller geometries of the 45 nm process, faster circuits are possible, which allow higher bandwidths for the proposed modulator. At the same time, higher number of internal bits with a smaller LSB in TDC and DTC is possible. The second prototype was also designed, fabricated, and tested in collaboration with Dr. Woo Young Jung while he was a Ph.D. student at The University of Texas at Austin.

Similar to Chapter 5, this chapter presents the modulator design, test methodology and experimental results for the 45 nm chip. I analyze the results and discuss the sources of impairment in detail.

## 6.2 Circuit Implementation

The modulator for the 45 nm chip has the parameters listed in Table 6.1. In the following sections, circuit implementations of the proposed architecture are described.

Table 6.1: Second-Generation Chip Parameters.

| Parameter | Value | Units |
|---|---|---|
| Process | IBM 45 nm SOI 10M 1P | - |
| Supply Voltage ($V_{DD}$) | 1.8/1.0 | V |
| Oversample Frequency ($f_s$) | 640 | MHz |
| Quantizer (TDC) Number of Bits | 4 | bits |
| DAC (DTC) Number of Bits | 4 | bits |
| TDC LSB ($\Delta$) | 15.8 | ps |
| $t_{\text{d,VTC/Adder}}$ | 714 | ps |
| $t_{\text{d,PhaseDetector}}$ | 116 | ps |
| $t_{\text{d,DTC}}$ | 302 | ps |
| $t_{\text{d,ExcessDelay}}$ (Average) | 400 | ps |
| Area | 0.0192 | $\text{mm}^2$ |

### 6.2.1 VTC/Adder

Similar to the VTC/Adder of the first-generation chip, the VTC/Adder of the second-generation chip consists of two identical half circuits, each of which have a ramp generator and a continuous-time comparator. As shown in Fig. 6.1, the VTC/Adder of the second-generation chip also includes level-shifters that translate the logic levels from the core supply voltage (1.0 V) to the I/O supply voltage (1.8 V) and back. The reason for adding level-shifters is that the comparators and ramp generators operate with the 1.8 V supply and are designed using I/O (thick-gate) devices for improved headroom and linearity. The rest of the ADC operates with 1.0 V supply and core (thin-gate) devices.

The ramp generator consists of a wide-swing current source ($I_B$ = 500 $\mu$A), an integrating capacitance ($C_I$ = 92.5 fF), and digital switches to

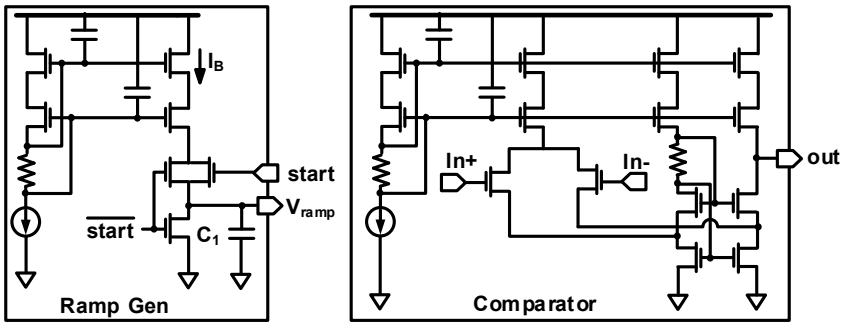


Figure 6.1: VTC/Adder circuit showing ramp generator and comparator.

create a 0 to 238 ps full scale $T_\Sigma[k]$ corresponding to a (0.23 V-0.83 V) linear range of $V_{in}$ with $V_{ref} = 0.23$ V.

The continuous-time comparator is a PMOS-input folded-cascode differential amplifier with a buffered output stage. The fixed overall latency is 740 ps ($t_{d,\mathrm{VTC/Adder}}$).

### 6.2.2 TDC/DTC

The TDC/DTC block performs the functions of both the ADC and the DAC in the first-order $\Delta\Sigma$ error feedback only structure The unit delay array (with fixed time interval $\Delta = 15.8$ ps) is the common block to both the ADC and the DAC in time-domain. If the operation of these functions can be performed sequentially, then those blocks may be shared. Thus, a reusable structure of multi-bit subtraction and quantization can save area. This novel merged ADC/DAC is possible thanks to time-domain processing, not possible

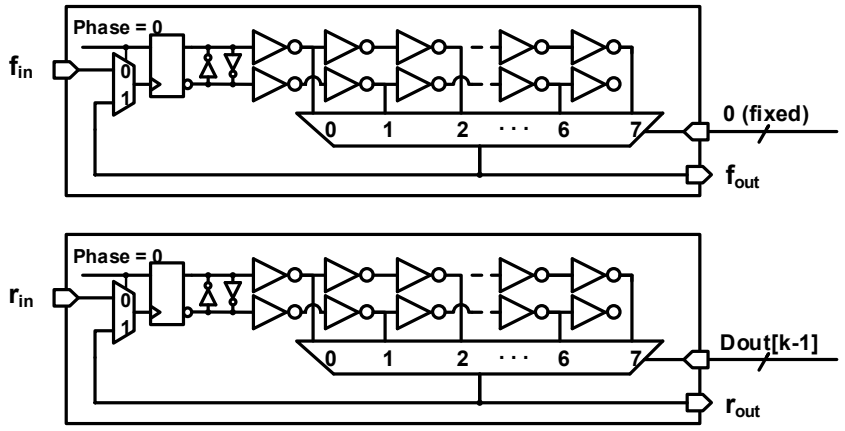


Figure 6.2: Digital-to-time converter (DTC) phase (phase 0) of the DTC/TDC circuit. Output pulse is recirculated through the block a second time for the TDC operation (phase 1).

in voltage-domain processing.

The TDC/DTC operates in two phases. In phase 0 (DTC), the block shown in Fig. 6.2 performs time-based subtraction by delaying the $r$ pulse by a number of LSB time-units ($D_{out}[k-1]$ from the phase 1 output of the previous cycle). The $f$ pulse is passed through a replica structure that has fixed delay. The resulting pseudo-differential pulse ($T_3$) is output to the excess delay block and also recirculates through the TDC/DTC for phase 1 (TDC phase). The same unit delay elements are used in conjunction with flip-flops and thermometer-to-binary logic that implement the time-based quantizer shown in Fig. 6.3. This structure resembles a flash TDC which uses (inverting) delay lines and flip-flops to quantize a pulse to a number of unit

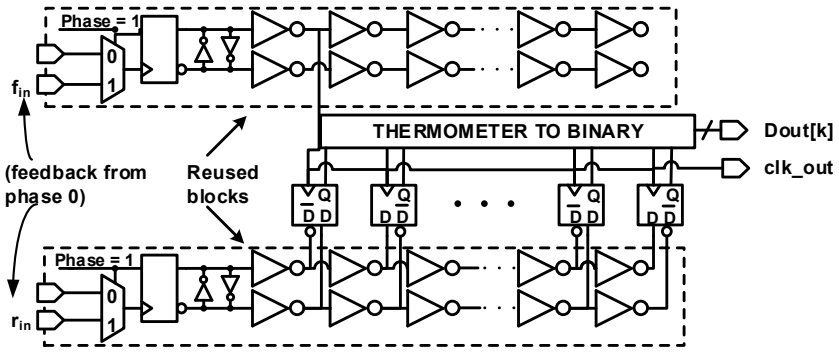


Figure 6.3: Time-to-digital converter (TDC) phase (phase 1) of the DTC/TDC circuit. Note the reuse of the unit delay elements from the previous phase (DTC).

delays (LSB). The use of inverting delay lines allows the LSB to be half as small, as compared to using non-inverting buffers (two inverters).

Both the DTC and the TDC are 4-bits in this implementation, with a unit delay (LSB) of 15.8 ps.

### 6.2.3 Delay Control Unit (DCU)

As introduced in Chapter 3, the DCU consists of the Phase Detector that generates *lead* and *lag* signals which are used by the Excess Delay to adjust the loop delay to ensure uniform sampling interval is maintained each cycle.

The circuit for the Phase Detector is shown in Fig. 6.4. Initially, after reset, the external clock ($f_s$) is fed in the loop (as $r_2$ and $f_2$) as a zero width

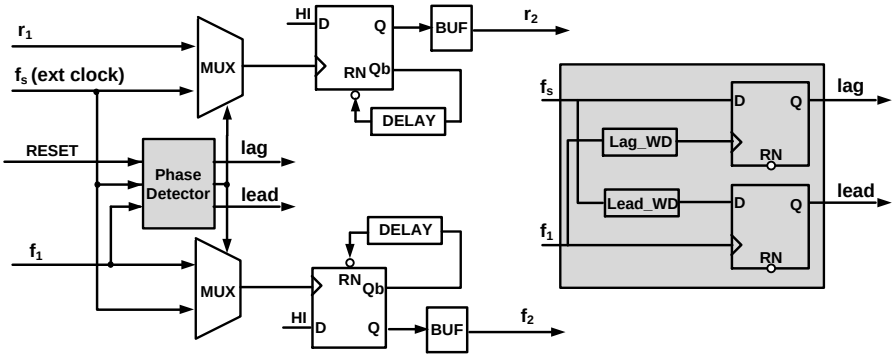


Figure 6.4: Delay Control Unit, including phase detector.

pulse. The phase detector signals a *lag* event if $f_1$ transitions high later than $Lag\_WD$ after the rising edge of $f_s$. Similarly, *lead* is signal if $f_1$ is more than $Lead\_WD$ earlier than the rise of $f_s$.

### 6.2.4 Complete ADC System

The complete ADC system for the second-generation chip is shown in Fig. 6.5.

### 6.2.5 Chip Layout

The layout of the core as a full-custom ASIC using IBM's 45 nm SOI process in shown in Fig. 6.6. The core occupies an area of 160 $\mu$m $\times$ 120 $\mu$m = 0.019 mm$^2$. The area could be reduced by an estimated 66% using a bulk CMOS process, since only (area-inefficient) SOI body-connected transistors were used to mimic the behavior of bulk CMOS.

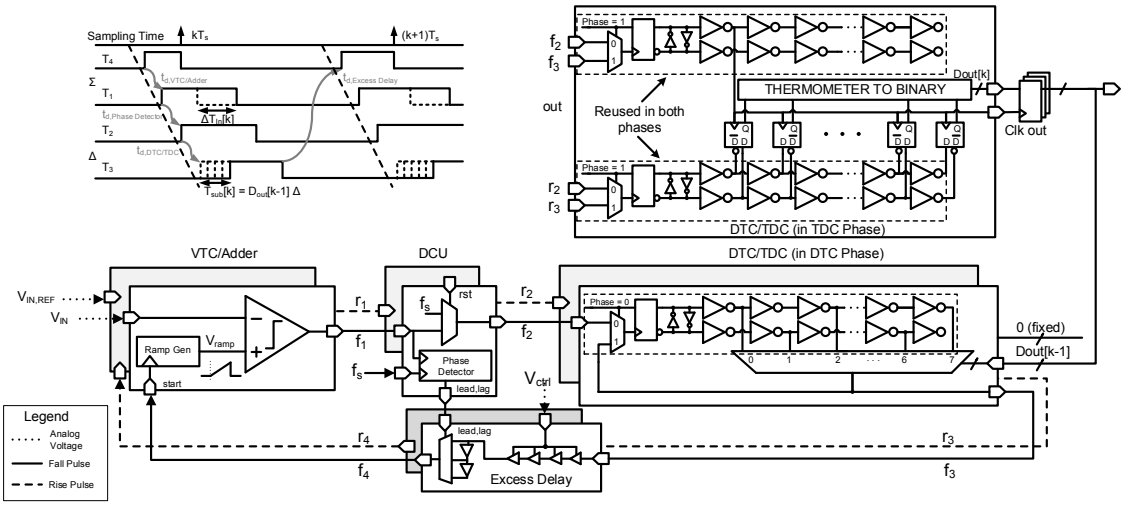


Figure 6.5: Complete PWM-based $\Delta\Sigma$ ADC System.

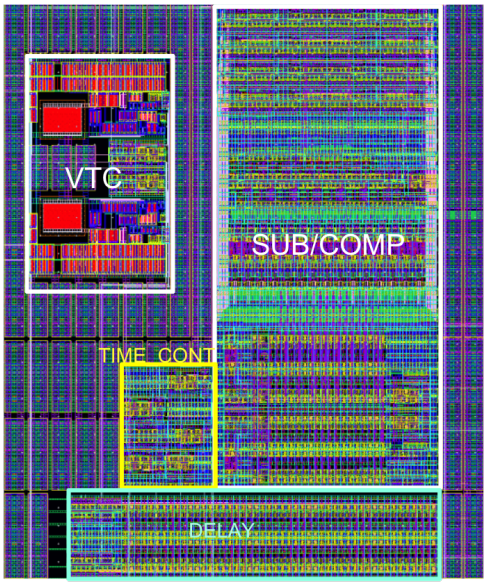


Figure 6.6: Core Layout. Dimensions are 160 $\mu$m $\times$ 120 $\mu$m.

## 6.3 Test and Measurement

This section outlines the experimental procedure to test and characterize the fabricated ADC integrated circuit. The test methodology, while often considered trivial and/or neglected during the design phase, can create external performance bottlenecks that limit the measured performance of the chip. Therefore, considerable amount of care and planning must be taken to obtain experimental results that are mainly limited by the ADC itself, and not the test enviroment.

### 6.3.1 Package Assembly and Wire Bonding

After the chip is fabricated, the first step is assembling the package. First the diced chip is mounted inside a selected package using a conductive epoxy. Then the I/O pads of the chip are connected the pins/leads of the package using gold wire bonds. Of foremost importance in test procedure, is planning the I/O pads and wire bonding diagram. On a mixed signal chip, such as an ADC, analog I/O signals and supplies need to be protected from digital switching inteference by digital I/O pads.

Digital I/O pads need to ensure signal integrity for the operating frequency. Seperate analog and digital supply/ground is common practice. Furthermore, the length of the wire bond and the adjacency of different I/O pads is important.

The inductance of the wirebond on power supply pins can reduce the effectiveness of external off-chip decoupling capacitors that provide instanta-

neous current during switching. Thus supply pins need to have low series inductance. Analog inputs/outputs have a similar requirement but due to coupling and frequency response considerations.

To minimize wire bond length, a 9 × 9 mm 64 pin QFN (Quad Flat No-leads) package was selected for its small cavity for a given I/O pin count. Many other package types, such as the more common ceramic LCC (Lead-less Chip Carrier), CFP (Ceramic Flat Pack), and PGA (Pin Grid Array) all had a larger cavity for a given pin count.

A technique to reduce wire bond length for critical I/O pads was to place the analog/supply pads closer to the edge of the package. Therefore, by placing the die off-center, the wire length for critical pads are reduced even further.

Given the small size of the die (2 mm × 2 mm) and the many I/O pins needed, a staggered bond pad was used. Staggered bonds pads have two rows of bond pads along each edge of the die. The example scanning electron microscope (SEM) image in Fig. 6.7 shows how the staggered bonding works. Different heights are needed; the wires coming from the inner bond pads require higher elevation from the die before bending down towards package pins. The wirebonding diagram for the second-generation chip is shown in Fig. 6.8. Different color wires represent the different elevation from the die before bending.

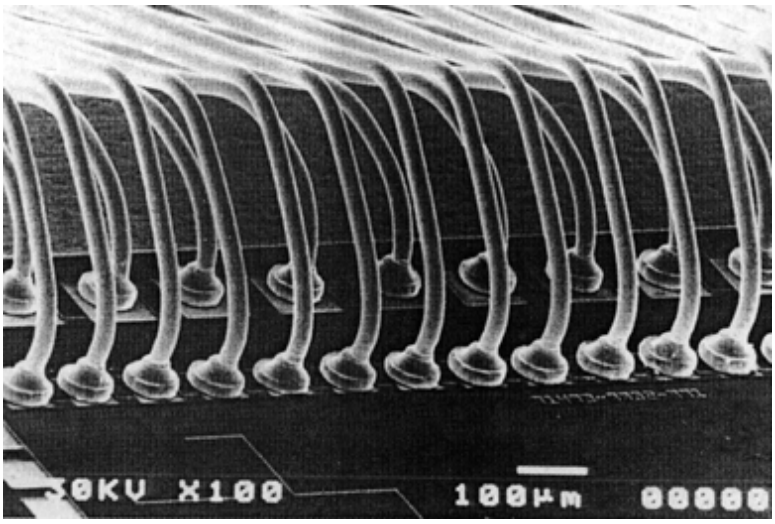


Figure 6.7: Example of a staggered wire bond [1]. Note the different heights and angles used to avoid other wires.

### 6.3.2 Capture Printed Circuit Board Design

The high-speed digital output (700+ MHz) data needed to be captured for processing in MATLAB. This posed a challenge, in particular, given the asynchronous nature of the modulator. To reliably capture the data on the asynchronous clock domain, a PCB was designed to interface the prototype chip with a Xilinx Spartan 6 Evaluation Board using the FMC-LPC high speed connector.

Matched differential 100 Ω transmission lines were drawn to route clock and high speed data from the prototype ADC to the Spartan 6 FPGA. Once in the FPGA high-speed SerDes (serializer/deserializer) blocks were needed to convert from high-speed serial to moderate speed parallel data.

Xilinx FPGAs allow fine delay adjustment to individual data lines, to

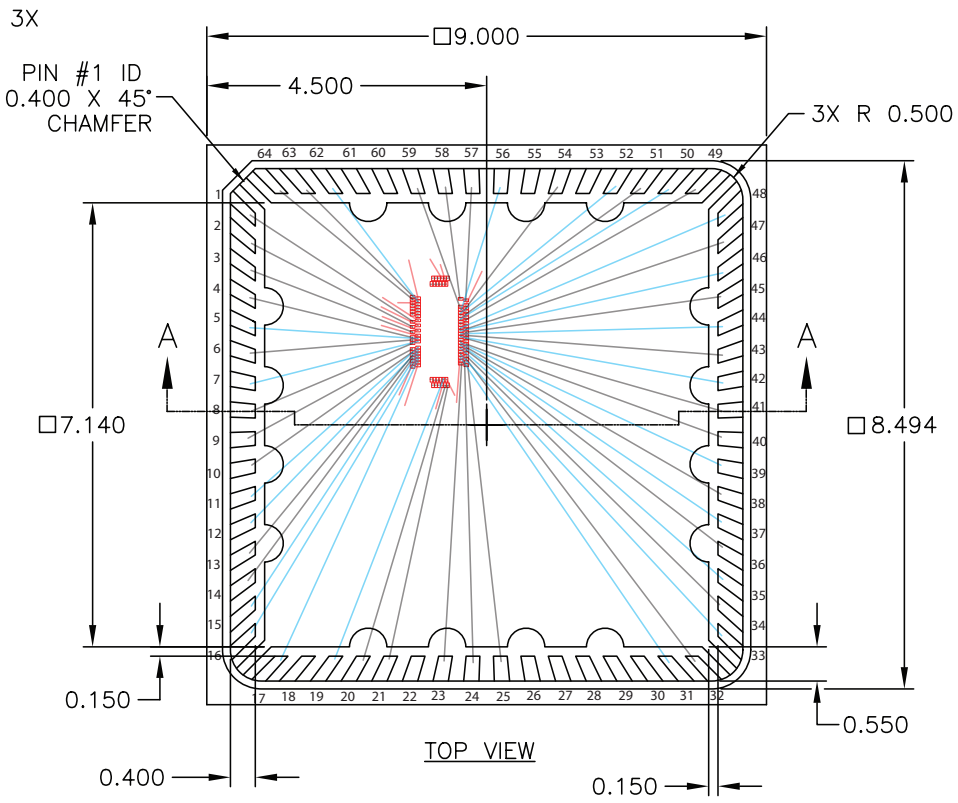


Figure 6.8: Wirebonding diagram for the second-generation prototype ADC. Die is 2 mm×1 mm, QFN-64 package is 9 mm×9 mm.

minimize skew and enable reliable data transmission, given the relative lengths of the traces. Another requirement for reliable capture is to use the same I/O half-bank on all the data that originates from the same clock.

### 6.3.3 Experimental Results

The experiment results obtained on the second generation chip consist of power measurement and FFT magnitude spectra obtained on a sinusoidal input. The total power consumption is 8 mW using 1.8 V/1.0 V supplies.

Fig. 6.9 shows the time-domain waveform and the decimated output of the ADC for a 600 mV pk-pk (0 dBFS) and 500 kHz sinusoidal input converted with an oversampling frequency of $f_s$ = 705 MHz. Fig. 6.10 shows the measured output spectrum. FFT length of 64K is used to generate the plot with a 7-term Blackman-Harris window. Fig. 6.11 shows the averaged FFT spectrum with 30 averages, and Fig. 6.12 shows the same but only from DC to $f_s/(2OSR)$. With OSR = 36, and BW = 9.8 MHz, SNR and SNDR were measured to be 41.2 dB and 37.5 dB, respectively. THD was measured to be -39.6 dB. These measurements results are also summarized in Table 6.2.

The spectrum shown in Fig. 6.10 shows an unusually high number of harmonic tones that are about -45 dB below the signal. These tones increase the total harmonic distortion (THD), and also limit the signal-to-noise-and-distortion ratio (SNDR). In section 4.2, where I modeled different sources of nonlinearity, I discussed how DTC element mismatch could be a major source of nonlinearity in the overall modulator. Here, the observation seems to agree

Table 6.2: Summary of Measurement Results of Second-Generation Chip.

| Quantity | Value | Units |
|---|---|---|
| $f_s$ | 705 | MHz |
| OSR | 36 | - |
| BW | 9.8 | MHz |
| $f_{in}$ | 500 | kHz |
| $V_{in,pk-pk}$ | 600 | mV |
| SNR | 41.2 | dB |
| SNDR | 37.5 | dB |
| ENoB | 6 | bits |
| THD | -39.6 | dB |
| Power | 8.0 | mW |

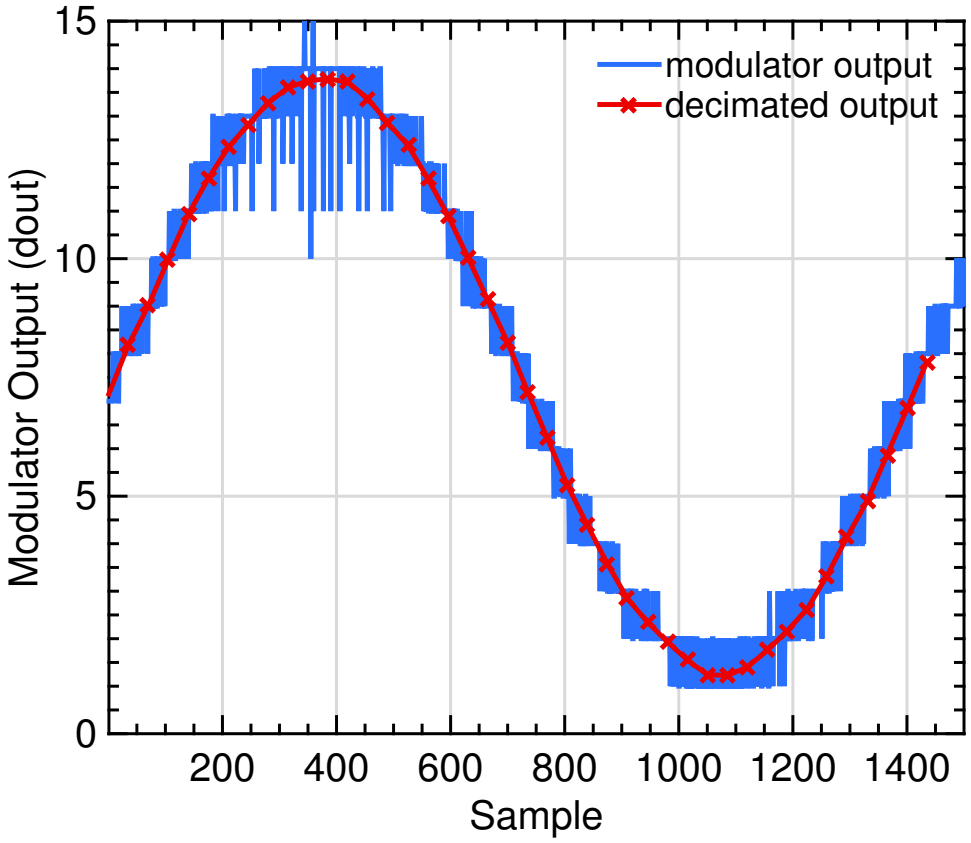


Figure 6.9: Time-domain waveform showing 1 cycle of a 0.5 MHz sine wave.

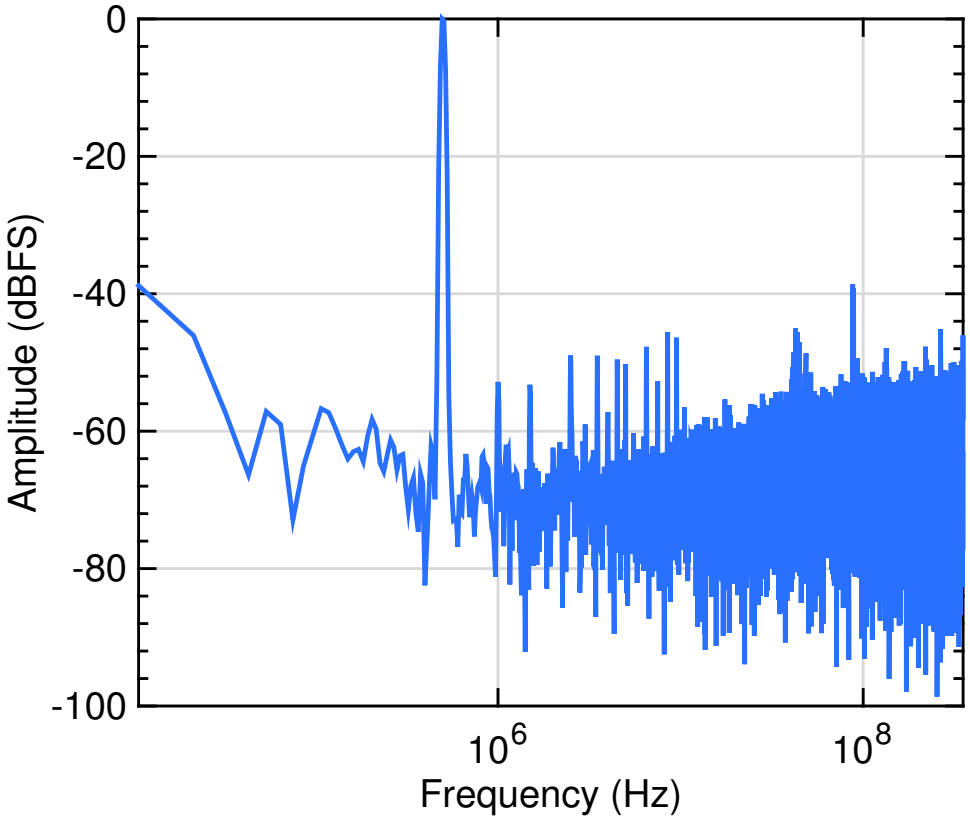


Figure 6.10: Magnitude FFT spectrum of a 500 kHz sinusoid sampled with $f_s$ = 705 MHz.

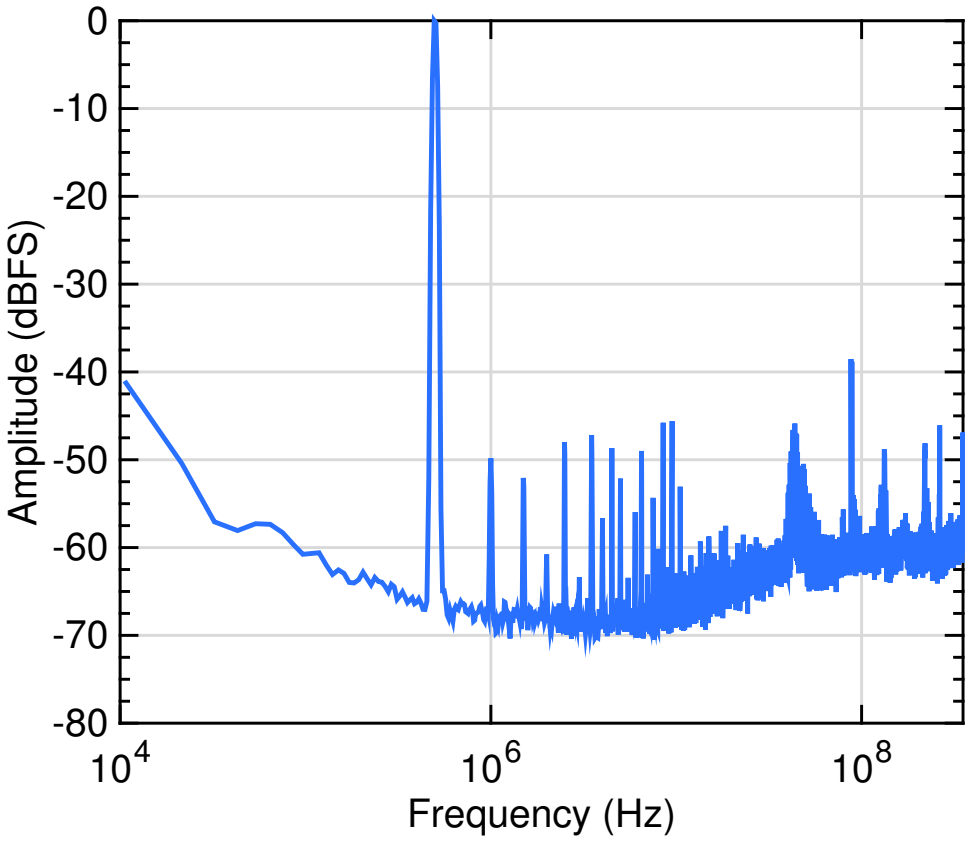


Figure 6.11: Averaged Magnitude FFT spectrum of a 500 kHz sinusoid sampled with $f_s = 705$ MHz, $N_{FFT} = 64$K, $N_{avg} = 30$.

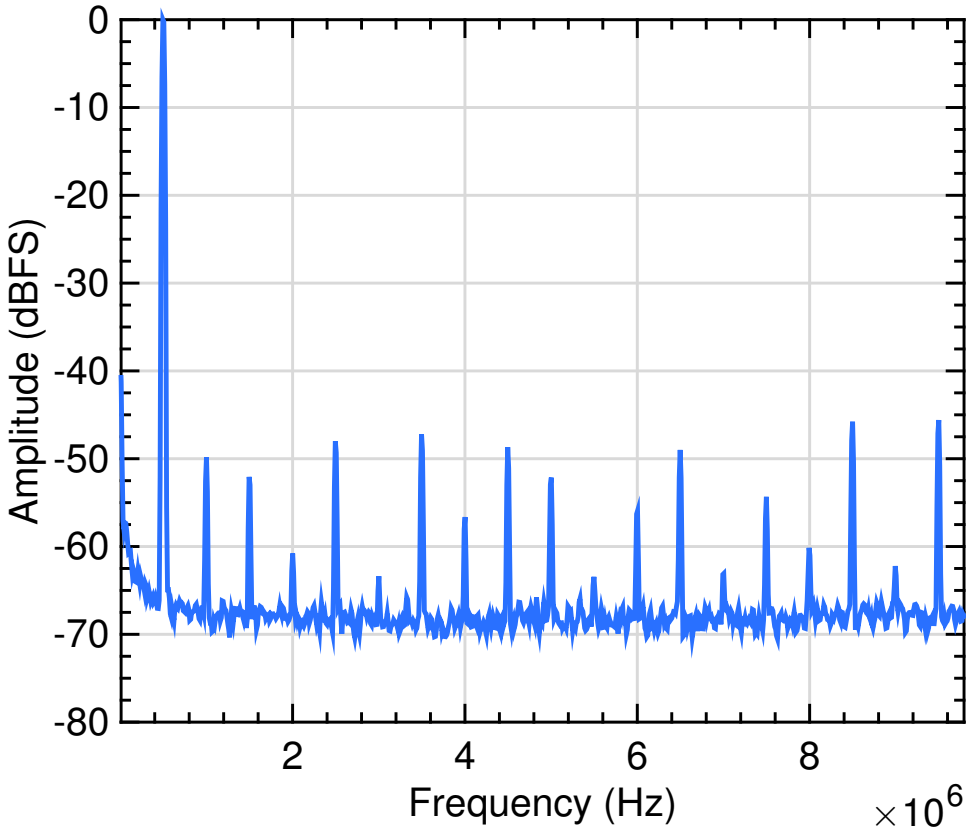


Figure 6.12: Magnitude FFT spectrum of a 500 kHz sinusoid sampled with $f_s$ = 705 MHz, OSR = 36, showing DC to $\frac{f_s}{2 \cdot OSR}$.

with that finding. In Chapter 7, I will analyze this effect in more detail and offer some insight for the exact source of this effect in the time-based $\Delta\Sigma$ ADC and propose an improved circuit that reduces this effect.

## 6.4 Summary

In summary, I presented the second-generation prototype ADC in this chapter. Similar to the first-generation prototype, limited THD was observed, which becomes a bottleneck for SNDR and ENoB. In the following chapter, I analyze the source of the nonlinearity in the two ADC prototypes, and offer two solutions for improving the proposed modulator.

# Chapter 7

# Nonlinear Circuit Linearization

## 7.1 Introduction

In Chapters 5 and 6, I discussed how the performance of the two fabricated prototype chips were limited by distortion. In this chapter, the source of the distortion in both chips is analyzed and digitally-corrected.

In Chapter 4, I showed through simulation using the behavioral model that DTC element mismatch is the largest contributor to the overall modulator nonlinearity. Assuming DTC mismatch is the dominant source of nonlinearity in the two prototype ADCs, I show and implement a method of estimating and correcting for the DTC mismatch in Section 7.2. Based on the findings from the analysis of DTC mismatch and its systematic pattern, I suggest an improved method of implementing the DTC/TDC block in Section 7.3.

Early work in ADC calibration (in 1984) performed *foreground* calibration by interrupting the operation of the ADC and injecting a known signal by using a precise calibrating DAC [38]. More recently, *background* calibration as a transparent alternative that works during normal ADC operation has attracted attention (see references in [39]). This approach calibrates the ADC without test signal injection or at least without explicit injection. The input

signal itself is thus used with one of 1) statistics-based code-domain equalization, 2) split ADC technique, or 3) pseudo-random noise injection. Finally, a hybrid approach called the *skip and fill* technique removes input samples and injects known samples, and fills the missing samples later using polynomial interpolation [40].

## 7.2 DTC Mismatch Calibration

In this section, I present the calibration of DAC element mismatch. Although this method can be equally applied to conventional multi-bit $\Delta\Sigma$ ADCs, the analysis and description of the method is described in the context of the proposed time-based $\Delta\Sigma$ ADC.

In Section 4.2.1, I showed how DTC element mismatch can be modeled. To recap, I used a $2^{NoB}$ element lookup table with perturbed values from the ideal values. In the presence of error in the DTC units, each code will have a fixed but non-ideal value. Let the distance from the ideal code $u$ be $\epsilon[u]$, where $u \in \{0, 1, \ldots, 2^{NoB} - 1\}$.

In the presence of DTC mismatch, as illustrated in Fig. 4.12, harmonic distortion results. If somehow $\epsilon[u]$ was known, a similar lookup table as that used in the behavioral model placed at the output of the modulator would cancel the nonlinearity due to the DTC. This is shown in Fig. 7.1, where the spectrum after calibration with a lookup table is similar to that of the ideal (no mismatch) spectrum.

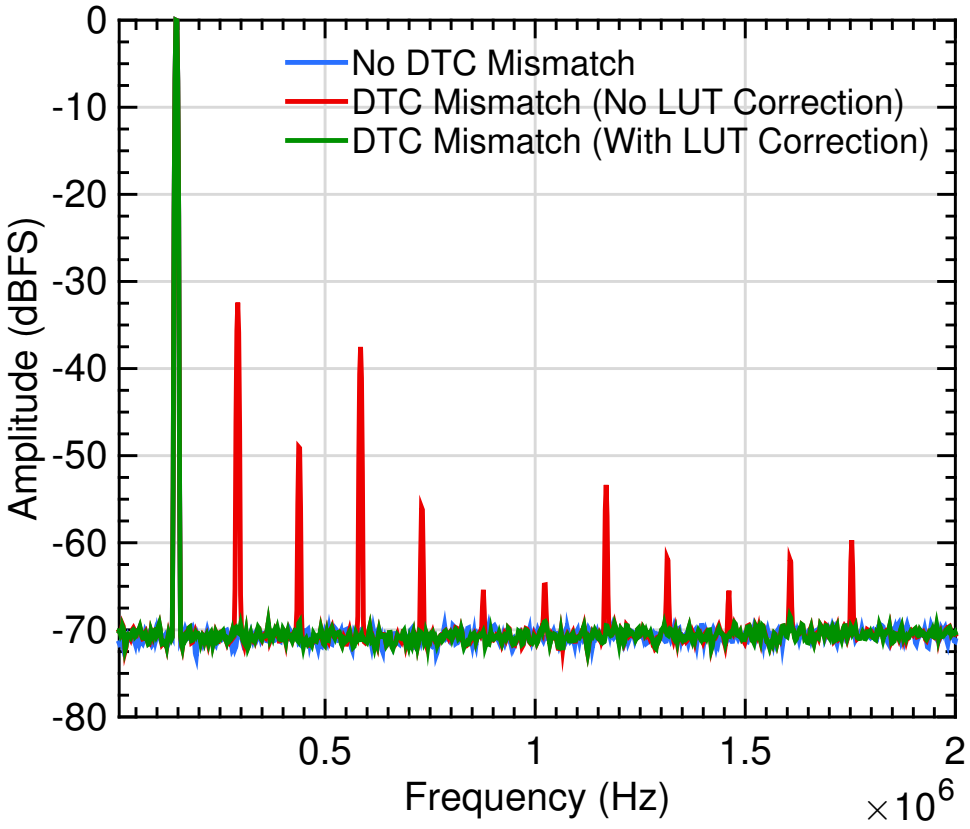


Figure 7.1: Simulated magnitude spectrum showing (a) no DTC mismatch, (b) DTC mismatch, and (c) DTC mismatch with LUT correction with perfect knowledge of $\epsilon[u]$.

To understand why adding a lookup table at the output of the modulator cancels or calibrates the nonlinearity due to the DTC, consider that the DTC plays the role of the DAC in a first-order $\Delta\Sigma$ modulator. Assume for simplicity, one code, e.g., the mid-code has an error, such that the mid-code is higher than the ideal value. Every time the quantizer (TDC) selects the mid-code, the feedback will contain an error, which will be corrected by the loop. If the feedback signal is higher than the ideal mid-code, then the modulator will reduce the density of the mid-code to compensate. For this reason, a lookup table that mimics the error in the DAC is needed, so that the output stream accurately represents the input. In other words, due to the error feedback, what appears at the output of the DAC and the output of the modulator need to be the same so as to minimize the error. When the error is minimized, the output represents the input.

Given, that the nonlinearity due to the DTC mismatch, may be cancelled if the mismatch in the DTC is known, I demonstrate an estimation algorithm is to find $\epsilon[u]$. Following, the estimation of $\epsilon[u]$, the lookup Table $T(u) = u + \epsilon[u]$ is populated and the nonlinearity due to DTC mismatch is cancelled.

The method used to estimate the DTC mismatch is loosely based on [41]. Given the modulator has an input large enough to hit all of the $2^{NoB}$ codes, the estimation algorithm is the following:

1. Calculate $X[k]$, the windowed-FFT of the modulator output ($x[n]$).

2. Repeat the following for $u \in \left\{1, 2, \ldots, 2^{NoB} - 2\right\}$

   (a) Calculate $I_u[k]$, the windowed-FFT of the event that the modulator code equals $u$, i.e., $\mathbf{1}(x[n] = u)$.

   (b) Correlate a predetermined set of bins $(k_1, \ldots, k_j)$ from $X[k]$ with the same bins from $I_u[k]$. Call the result $\epsilon[u]$.

   (c) Where $x(n) = u$, replace $x(n)$ with $T(u) = u + \epsilon[u]$.

Mathematically,

$$\epsilon[u] = \frac{\sum_{k=k_1}^{k_j} \{\Re(X[k]I_u[k]) + \Im(X[k]I_u[k])\}}{\sum_{k=k_1}^{k_j} \{\Re(I_u[k]I_u[k]) + \Im(I_u[k]I_u[k])\}} \tag{7.1}$$

where $\Re(\cdot)$ and $\Im(\cdot)$ denote the real and imaginary parts of the argument, respectively.

In the case of a sinusoidal input, the predetermined set of bins $(k_1, \ldots, k_j)$ can simply be chosen in a manner to remove the bins nears the input frequency. In my analysis, I use bins that include the frequency range from $1.5f_{in}$ till $f_s/2/OSR$.

### 7.2.1 Calibration of the First Generation ADC

Using the measured data of the first generation chip, the calibration algorithm described above is performed to estimate and correct for the DTC (DAC) element mismatch. The ADC performance with and without calibration is compared. The uncalibrated and calibrated spectra are shown in

Table 7.1: Measured first generation ADC performance with/without calibration for OSR = 14, BW = 5.14 MHz.

| | Uncalibrated | Calibrated | Improvement | Units |
|---|---|---|---|---|
| SNR | 41.1 | 41.3 | 0.2 | dB |
| SNDR | 33.7 | 40.0 | 6.3 | dB |
| THD | -34.5 | -45.7 | 11.2 | dB |
| ENoB | 5.3 | 6.3 | 1 | bit |

Table 7.2: First generation ADC performance with/without calibration for OSR = 36, BW = 2.0 MHz.

| | Uncalibrated | Calibrated | Improvement | Units |
|---|---|---|---|---|
| SNR | 44.6 | 44.8 | 0.2 | dB |
| SNDR | 34.6 | 44.0 | 9.4 | dB |
| THD | -35.0 | -51.0 | 16.0 | dB |
| ENoB | 5.5 | 7.0 | 1.5 | bit |

Fig. 7.2 and 7.3. These figures show a drastic reduction in the harmonic content through digital post-correction of DTC (DAC) element mismatch. ADC perfomance is summarized in Tables 7.1 and 7.2.

The values of the mismatch found by the calibration algorithm for the first generation chip are plotted in Fig. 7.4. Note there is a trend of alternating sign in mismatch coefficients. This can be explained by the TDC/DTC structure which incorporates inverters, rather than buffers as the unit delay element. This approach, while having the advantage of creating smaller unit delays and ultimately faster conversion rates, however, it is responsible for the majority of the measured nonlinearity. Since PMOS and NMOS transistors in the inverters cannot match under normal process variations, it is much more advantageous to use buffers as unit delay elements.

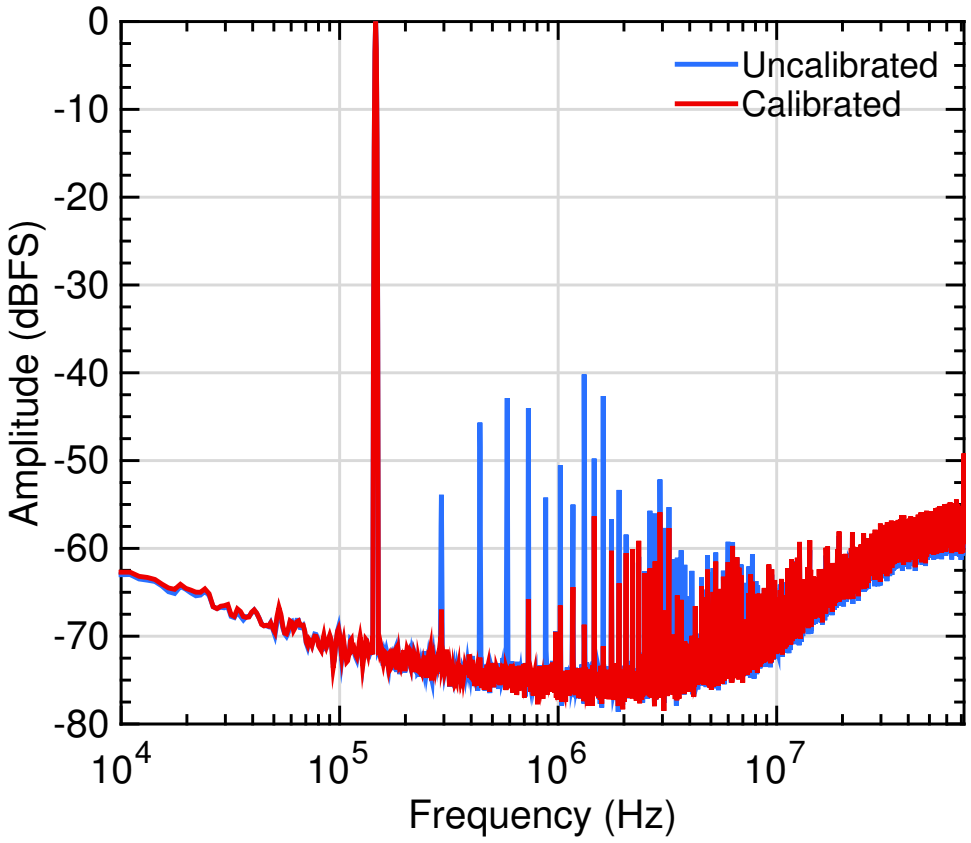


Figure 7.2: Spectrum showing linearity improvement using the calibration algorithm for first generation chip measured data. Uncalibrated THD = −34.5 dB, calibrated THD = −45.7 dB. THD is improved by 11.2 dB for OSR = 14, BW = 5.14 MHz.

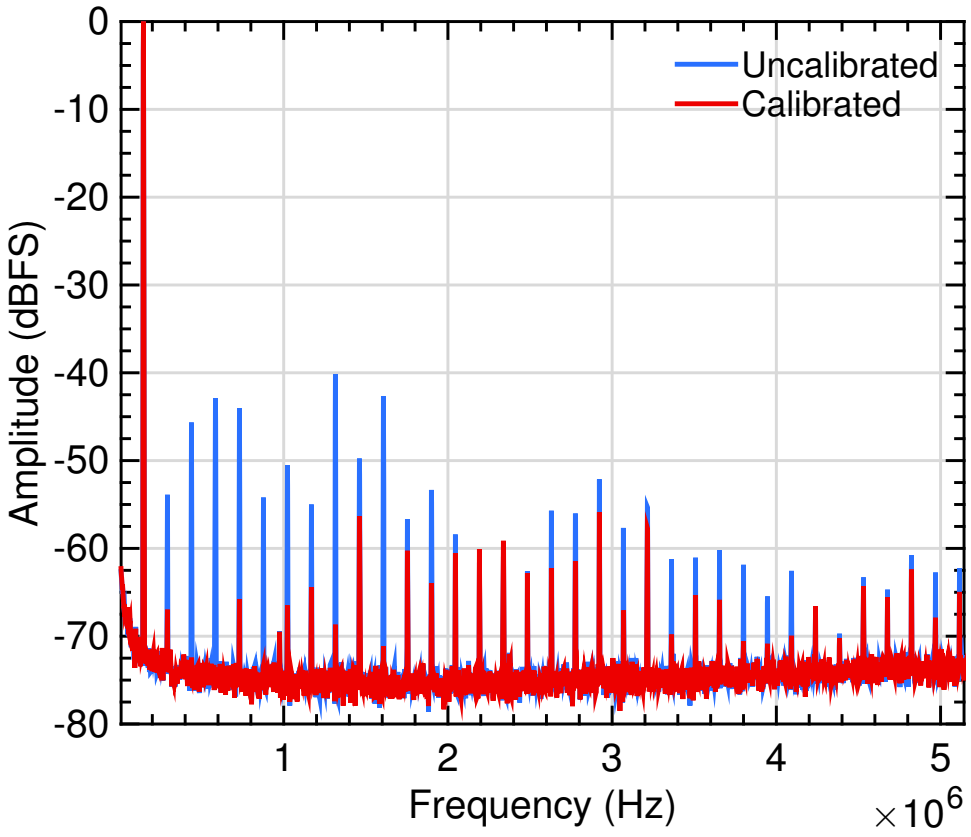


Figure 7.3: Spectrum showing linearity improvement using the calibration algorithm for first generation chip measured data. Uncalibrated THD = −34.5 dB, calibrated THD = −45.7 dB. THD is improved by 11.2 dB for OSR = 14, BW = 5.14 MHz.

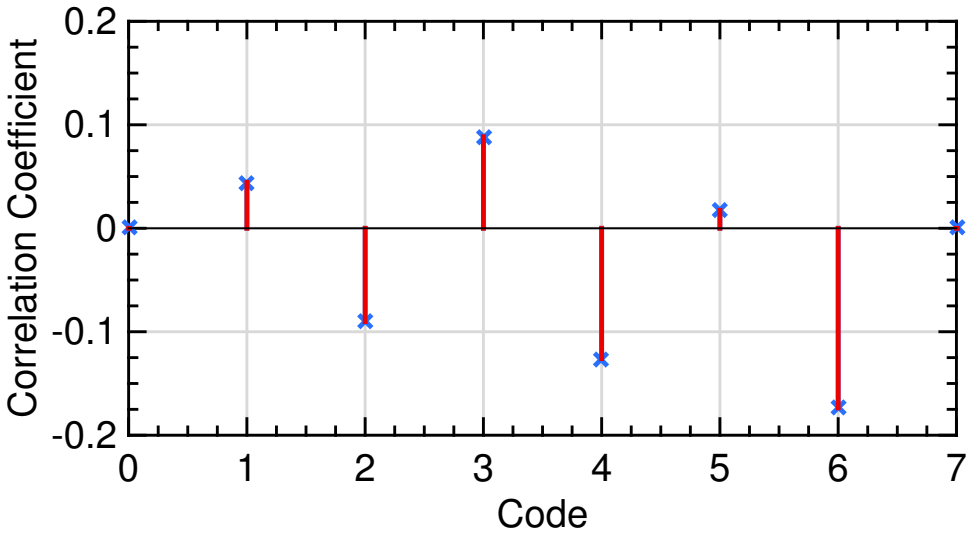


Figure 7.4: Estimated mismatch coefficients for each code on measured first chip data.

To benchmark the accuracy of the calibration algorithm, known/random mismatch coefficients are used in the simulator. The goal of the calibration algorithm is to accurately estimate the mismatch coefficients so that the nonlinearity introduced by the DAC may be cancelled, using a $2^{NoB}$ element lookup table, prior to decimation filtering.

If the same mismatch coefficients as those obtained from measured data are used in the simulator, the expected degradation in linearity may be studied and compared to measured data. Also, the theoretical best case cancellation limit and the achievable cancellation from the calibration algorithm may be compared. Fig. 7.5 shows the simulated mismatch vs. the estimated mismatch from the calibration algorithm. Note: the calibration algorithm tracks the actual mismatch very closely. The mean squared error is $\approx 10^{-7}$.

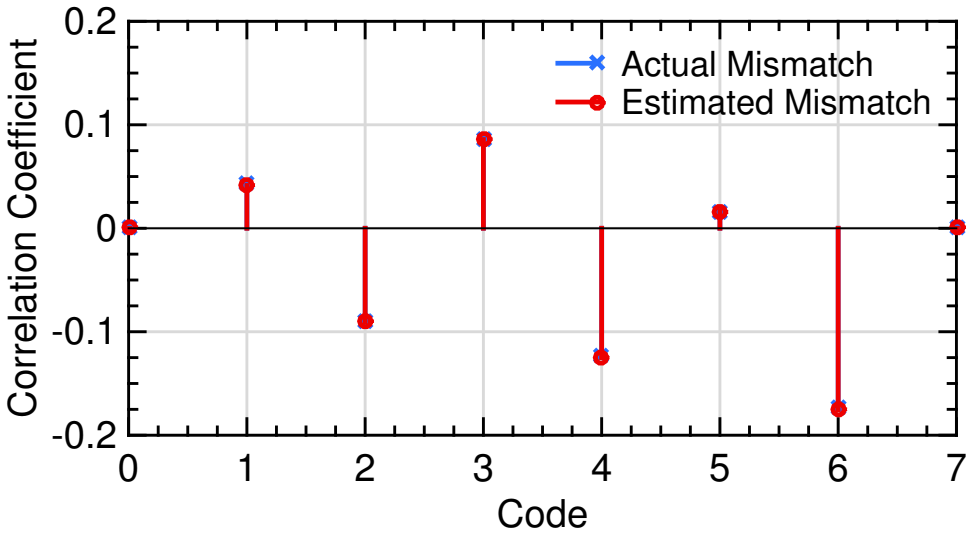


Figure 7.5: Actual and estimated mismatch coefficients for each code on simulated data. Mean squared error is $\approx 10^{-7}$.

Table 7.3: Simulated first generation ADC performance with/without calibration for OSR = 14, BW = 5.14 MHz.

| | Uncalibrated | Calibrated | Improvement | Perfect Cal. | Units |
|---|---|---|---|---|---|
| SNR | 41.7 | 44.2 | 2.5 | 44.2 | dB |
| SNDR | 34.5 | 43.1 | 8.6 | 43.1 | dB |
| THD | -35.4 | -49.1 | 13.7 | -49.6 | dB |
| ENoB | 5.4 | 6.9 | 1.5 | 6.9 | bit |

ADC performance from simulated results before and after calibration (algorithm vs. perfect cancellation) are summarized in Tables 7.3 and 7.4. The spectra obtained from the simulated ADC outputs before and after calibration are plotted in Fig. 7.6.

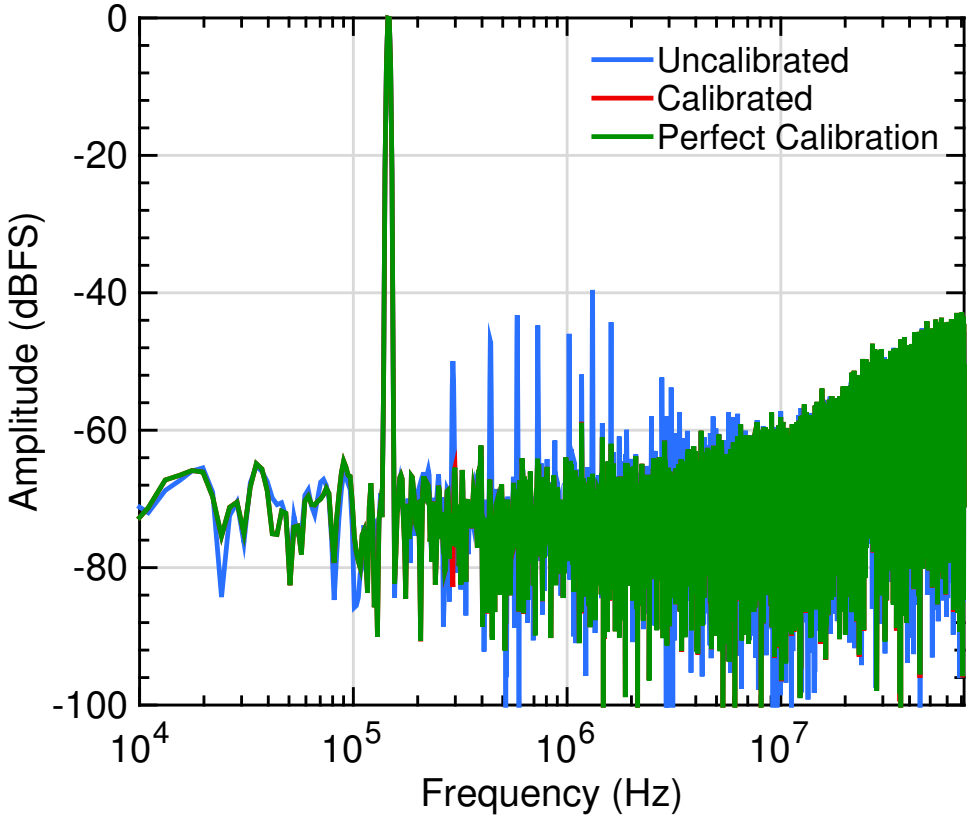


Figure 7.6: Spectrum showing linearity improvement using the calibration algorithm for simulated data that matches the estimated mismatch of the first generation chip. Uncalibrated THD = −35.4 dB, calibrated THD = −49.1 dB. THD is improved by 13.7 dB for OSR = 14, BW = 5.14 MHz.

Table 7.4: Simulated first generation ADC performance with/without calibration for OSR = 36, BW = 2.0 MHz.

| | Uncalibrated | Calibrated | Improvement | Perfect Cal. | Units |
|---|---|---|---|---|---|
| SNR | 45.5 | 46.0 | 0.5 | 46.0 | dB |
| SNDR | 35.1 | 44.8 | 9.9 | 44.8 | dB |
| THD | -35.5 | -50.7 | 15.0 | -50.7 | dB |
| ENoB | 5.5 | 7.2 | 1.7 | 7.2 | bit |

Table 7.5: Measured second generation ADC performance with/without calibration for OSR = 36, BW = 9.8 MHz.

| | Uncalibrated | Calibrated | Improvement | Units |
|---|---|---|---|---|
| SNR | 44.6 | 44.8 | 0.2 | dB |
| SNDR | 34.6 | 44.0 | 9.4 | dB |
| THD | -35.0 | -51.0 | 16.0 | dB |
| EnoB | 5.5 | 7.0 | 1.5 | bit |

### 7.2.2 Calibration of the Second Generation ADC

Using the measured data of the second generation chip, the calibration algorithm is used to estimate and correct for the DTC element mismatch. The ADC performance with and without calibration is compared in Table 7.5. The uncalibrated and calibrated spectra are shown in Fig. 7.7 and 7.8. These figures show a drastic reduction in the harmonic content through digital post-correction of DTC (DAC) element mismatch.

The values of the mismatch found by the calibration algorithm for the second generation chip are plotted in Fig. 7.9. Note that similar to the first generation chip, there is a trend of alternating sign in mismatch coefficients. This can be explained by the TDC/DTC structure which incorporates inverters, rather than buffers as the unit delay element.

## 7.3 Improved Design For TDC/DTC

From the calibration of the DTC in the first and second generation chips, I determined the root cause of the modulator distortion to be predominantly the mismatch in the DTC. I also found a systematic pattern to the

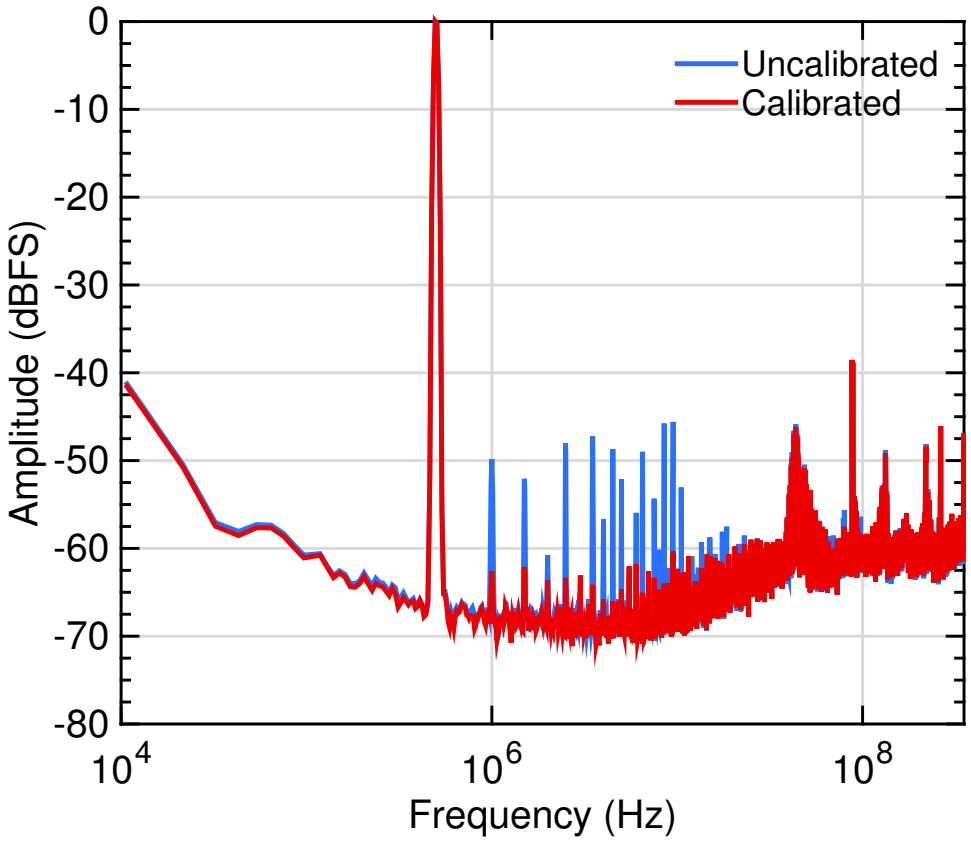


Figure 7.7: Spectrum showing linearity improvement using the calibration algorithm for second generation chip measured data. Uncalibrated THD = −35.0 dB, calibrated THD = −51.0 dB. THD is improved by 16.0 dB for OSR = 36, BW = 9.8 MHz.

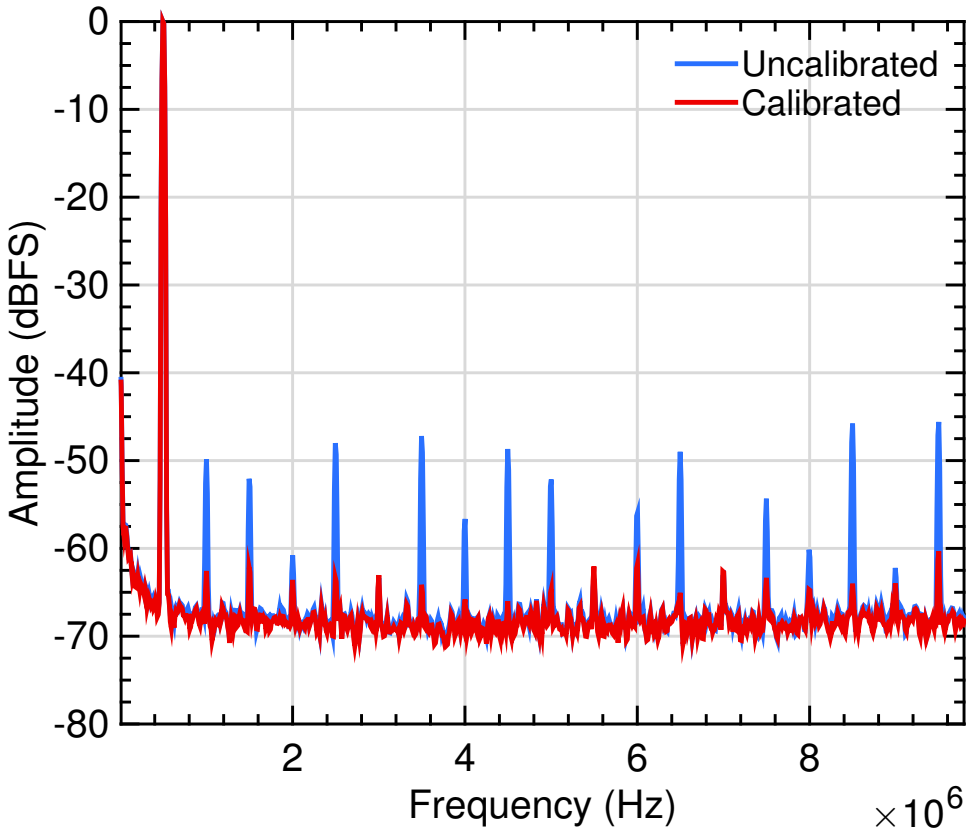


Figure 7.8: Spectrum showing linearity improvement using the calibration algorithm for second generation chip measured data. Uncalibrated THD = −35.0 dB, calibrated THD = −51.0 dB. THD is improved by 16.0 dB for OSR = 36, BW = 9.8 MHz.

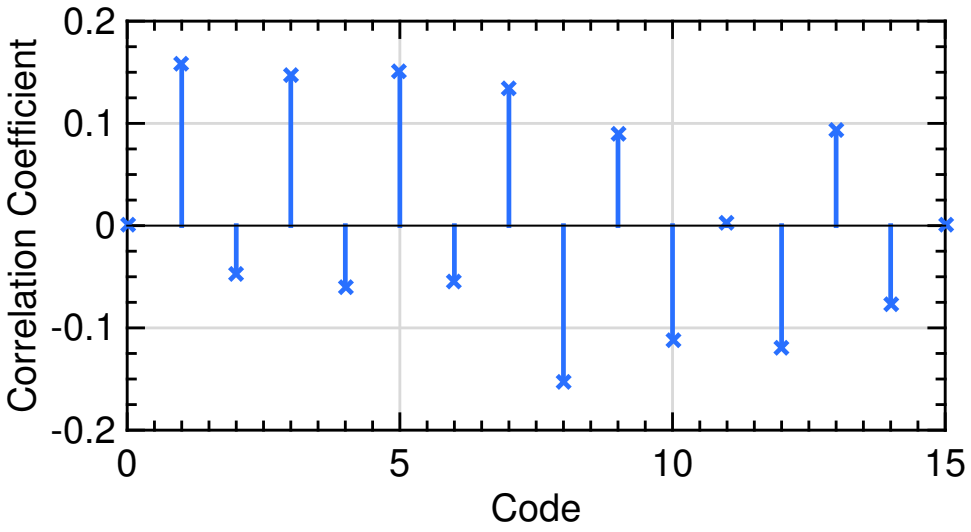


Figure 7.9: Estimated mismatch coefficients for each code on measured second chip data.

mismatch, where alternating codes were mismatched somewhat similarly. This was attributed to the use of inverters rather than buffers, in the DTC/TDC block, for improved resolution.

An improved implementation of the proposed time-based $\Delta\Sigma$ ADC, would consider one of the following:

1. Utilize buffers, rather than inverters as the unit elements in the DTC/TDC.
2. Use the same structure of DTC/TDC, however, truncate the LSB from the TDC result, such that the DTC code is always an even number of stages.
3. Use extra inverter stages and implement a first-order DWA, or similar low-complexity DEM.

## 7.4 Summary

To summarize this chapter, I presented a frequency-domain algorithm for estimating DTC element mismatch. I applied the algorithm to simulated data from a modulator that exhibits DTC element mismatch and its associated harmonic distortion, and showed that with a lookup table following the modulator, the distortion is removed to the level of the ideal modulator without mismatch.

Applying the same algorithm to measured data on the first and second generation chips resulted in both improved THD by up to 16 dB and improved SNDR by up to 1.5 bits.

An important insight offered by the analysis was to identify the systematic pattern of mismatch, where even and odd codes were correlated with each other. This lead to the explanation that inverter stages used as unit delay elements suffer from systematic mismatch, due to the difference in drive strength of NMOS and PMOS transistors. Alternative circuit implementation were suggested to overcome this limitation.

# Chapter 8

# Conclusions and Future Work

## 8.1 Summary

While the benefits of transistor scaling for digital circuits drive the development of the latest CMOS processes, state-of-the-art nanometer-scale processes present a new challenge for mixed-signal circuits. In the case of analog-to-digital converters, increased uncertainty in analog quantities represented by voltage calls for rethinking the traditional approaches to analog signal processing. The time-based processing approach with delta-sigma modulation offers a promising combination that not only mitigates the problem of increased voltage-domain inaccuracy, but also benefits from the enhanced time-resolution of nanometer scale processes. Digital enhancement and system-level coordination between analog and digital subcircuits in a mixed-signal integrated circuit offers potential to improve traditional standalone circuits like ADCs.

## 8.2 Contributions

In summary, I propose improving performance of mixed-signal/analog circuits, in particular Analog-to-Digital Converters (ADCs), in nanometer-

scale CMOS using novel architectures and techniques. The contributions of my dissertation research follow:

1. Design and modeling of a novel noise-shaping $\Delta\Sigma$ ADC architecture that features the following:
   (a) mostly-digital time-based processing, which
      i. accepts a voltage signal at the input, but internally converts it to a pseudo-differential pulse, and
      ii. all subsequent processing is performed on pulses whose widths encode the signal information.
   (b) asynchronous modulator with loop delay calibration unit, which
      i. provides a known time base using an external reference clock,
      ii. removes harmonic distortion due to non-uniform sampling, which arises from input-dependent time drift in the asynchronous loop, and
      iii. reduces the need for an accurate clock network.
   (c) a novel multi-bit invertible TDC/DTC (ADC/DAC), wherein
      i. the width of the pulse is quantized by a delta-sigma modulator with a flash time-to-digital converter (TDC) as the internal ADC,
      ii. reduces area through sharing the unit delay elements,

(d) removes the sample-and-hold amplifier and replaces it with a continuous-time comparator which simplifies the circuit even further.

2. Design, fabrication, and testing two prototype ADC chips using the proposed architecture (in collaboration with Dr. Woo Young Jung), using

   (a) TSMC 180nm CMOS process, and

   (b) IBM 45nm SOI process.

3. Nonlinear circuit linearization of the ADC

   (a) using digital post-correction to estimate and correct for nonlinearity due to DTC mismatch

   (b) without the need of a calibrating DAC

## 8.3 Future Work

To improve upon the architecture and prototype circuits proposed in this dissertation, the following work is envisioned:

1. improving the mismatch between unit delay elements in the DTC, by

   (a) utilizing buffers, rather than inverters as the unit elements in the DTC/TDC.

   (b) using the same structure of DTC/TDC, however, truncating the LSB from the TDC result, such that the DTC code is always an even number of stages.

(c) using extra inverter stages and implementing a first-order DWA, or similar low-complexity DEM.

2. improve circuit-level performance parameters, such as

   (a) investigate reducing the thermal, and flicker noise from the front-end circuits, mainly the comparator, e.g., by chopping

   (b) reduce the power of front-end circuit and removing the replica ramp generator and comparator in the VTC/Adder, and replacing it with a calibrated delay cell.

3. add calibration circuits to enable the system to work better under different process corners, without the need for tuning delay in the excess loop delay circuit by a control voltage.

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# Vita

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From 2005 to 2006, he was employed as an embedded software designer at Niktek, Inc. in Tehran. From 2006–2012, he was a Research Assistant at the Embedded Signal Processing Laboratory at The University of Texas at Austin. His research interests include digitally-enhanced analog/mixed-signal system design.

He has been fortunate to work with outstanding engineers in three internship positions at Intrinsity, Inc. (later acquired by Apple, Inc.) in 2008 and 2009, and at Cirrus Logic, Inc. in 2011. Since Oct. 2012, he has been working full time at Cirrus Logic, where he designed integrated circuits for mixed-signal audio, including an open-loop digital class-D amplifier, and an ultra-low power continuous time $\Delta\Sigma$ ADC in 55nm CMOS.

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