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Effects of Scaling on Microstructure Evolution of Cu Nanolines and Impact on Electromigration Reliability

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Effects of Scaling on Microstructure Evolution of Cu Nanolines and Impact on Electromigration Reliability

by

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Dedication

To my parents and friends

Effects of Scaling on Microstructure Evolution of Cu Nanolines and Impact on Electromigration Reliability

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The University of Texas at Austin, 2014

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Scaling can significantly degrade the electromigration (EM) lifetime for Cu interconnects, raising serious reliability concerns. Different methods have emerged to enhance the EM resistance of Cu by suppressing the interface diffusion (the historically fastest diffusion path), notably using CoWP metal cap and Mn alloying. With further scaling of Cu interconnects, EM reliability becomes increasingly complex due to changes in Cu microstructure. In ultra-fine Cu lines a large population of small grains mix with bamboo-type grains, resulting in an additional contribution of grain boundary diffusion to EM degradation. With the interface diffusion suppressed by CoWP or Mn alloying, the grain structure effect becomes even more important.

The objective of this study is to investigate the EM reliability of ultra-fine Cu interconnects, focusing on the scaling effect on grain structure and mass transport. First, the detailed microstructure information of Cu interconnects down to the 22 nm node was analyzed using a transmission electron microscope (TEM)-based high resolution diffraction technique. A dominant sidewall growth of {111} grains was observed for 70 nm Cu lines (45 nm node), reflecting the importance of interfacial energy in controlling grain growth. The strength of the {111} texture was found to significantly increase as line width was reduced to 40 nm (22 nm node), while the length fraction of coherent twin

boundaries was reduced to ~1%. Secondly, the results from microstructure together with the deduced interfacial and grain boundary diffusivities were used to identify flux divergent sites for void formation and to analyze the grain structure effect on EM statistics using a microstructure-based kinetic model. Finally, based on the analysis of Cu grain structure evolution with downscaling, the scaling behavior of EM drift velocity was investigated for Cu interconnects with CoWP capping and Mn alloying. This enables us to project the EM lifetime and statistics for future technology nodes. The Mn alloying effect on mass transport in combination of grain structure control was found to provide an effective means to improve EM reliability especially with further scaling. In summary, this study establishes a correlation between the microstructure of Cu nanolines, void formation kinetics, and EM statistics.

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Chapter 1: Introduction

In advanced integrated circuits (ICs), the ever-growing demands of high device density and high circuit performance have driven the minimum feature size of transistors to shrink approximately 30% for each generation of CMOS technology in accordance with Moore's Law (Figures 1.1) [1]. This downscaling trend of transistors is accompanied by the increasing complexity of the wiring structure for on-chip interconnects. Intel recently announced their 14 nm technology in volume production featuring the 2nd-generation tri-gate technology (Figure 1.2) [2]. With the aggressive scaling of advanced ICs to the sub-100 nm regime, the RC signal delay caused by interconnects becomes increasingly significant compared to the gate delay (Figure 1.3). To address the RC delay issue and to continue the expected performance improvement, copper (Cu)/low-*k* interconnect structures have been developed to replace the aluminum (Al)/SiO_2 structures since 1997 [3]. The implementation of Cu/low-*k* structures requires the development of a new integration scheme with distinct microstructures and interfaces, all of which can impact the reliability of Cu/low-*k* interconnects.

Electromigration (EM) is one of the most important reliability problems for Cu interconnects. While the EM phenomenon is well-established, the scaling effects on EM reliability need further understanding [4]. As the interconnect dimensions continue to decrease, EM reliability becomes increasingly complex due to changes in Cu microstructure and failure mechanisms that control the EM lifetime and early failure statistics. Continuous downscaling together with the increase in the current density [5] can significantly degrade the EM lifetime for Cu interconnects, raising new reliability challenges for advanced chips of future technology nodes. Potential solutions have been developed by suppressing the interfacial mass transport (the fastest diffusion path [6]),

notably using CoWP metal cap [7, 8] and Mn-alloyed seed layer [9-15]. The use of a thin interface layer of CoWP has shown to be the most direct and efficient approach to reduce the interface diffusion and thus improve EM performance. However, the effectiveness of the CoWP cap layer has been found to be strongly dependent on the Cu microstructure [16-19]. Once the interface diffusion is suppressed by the CoWP cap layer, the grain boundary (GB) diffusion becomes dominant, reducing the lifetime for Cu lines with small grain structure. This suggests that Cu interface engineering in combination with Cu GB engineering would provide an optimum approach for improving EM reliability for future technology nodes.

In addition to EM lifetime, the effects of scaling and grain structure on EM lifetime statistics is also of serious concern. All of the parameters that control void formation are statistically distributed, such as the variations in grain size and grain orientation [20-22]. A recent study showed that Mn alloying was particularly effective in sustaining a small statistical deviation σ although the improvement of EM lifetime was less than the CoWP cap [15, 16]. During subsequent annealing, Mn from an alloy seed layer was found to segregate at grain boundaries and Cu/cap layer interfaces, reducing Cu diffusion at active diffusion paths. It is not clear, however, how effective Mn alloying would be as scaling continues. With the interface diffusion suppressed by Mn addition, the effect of grain structure on the overall EM mass transport becomes as important as observed for the case of CoWP capping. The scaling effect of Mn alloying on EM reliability and the microstructure evolution of ultrafine Cu lines has to be better understood in order to implement this process for the future technology.

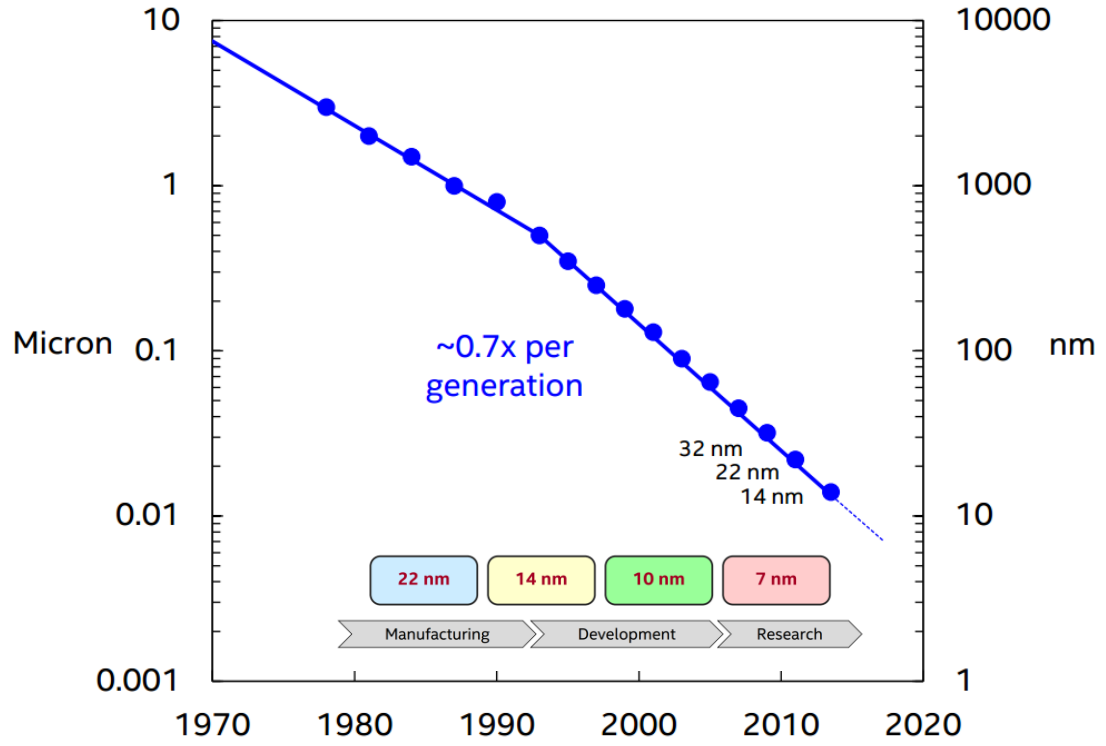
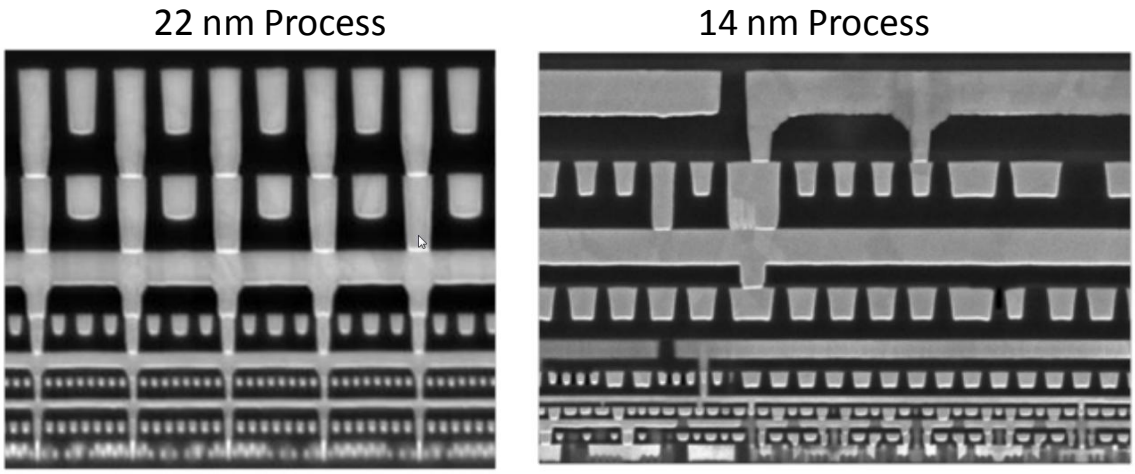


Figure 1.1 Intel's scaling trend and technology roadmap [2] .



	22 nm	14 nm	Scale
Transistor Fin Pitch	60	42	.70x
Transistor Gate Pitch	90	70	.78x
Interconnect Pitch	80	52	.65x

Figure 1.2 Cross-sectional images of Intel's most advanced 22 and 14 nm technologies and their minimum feature sizes [2].

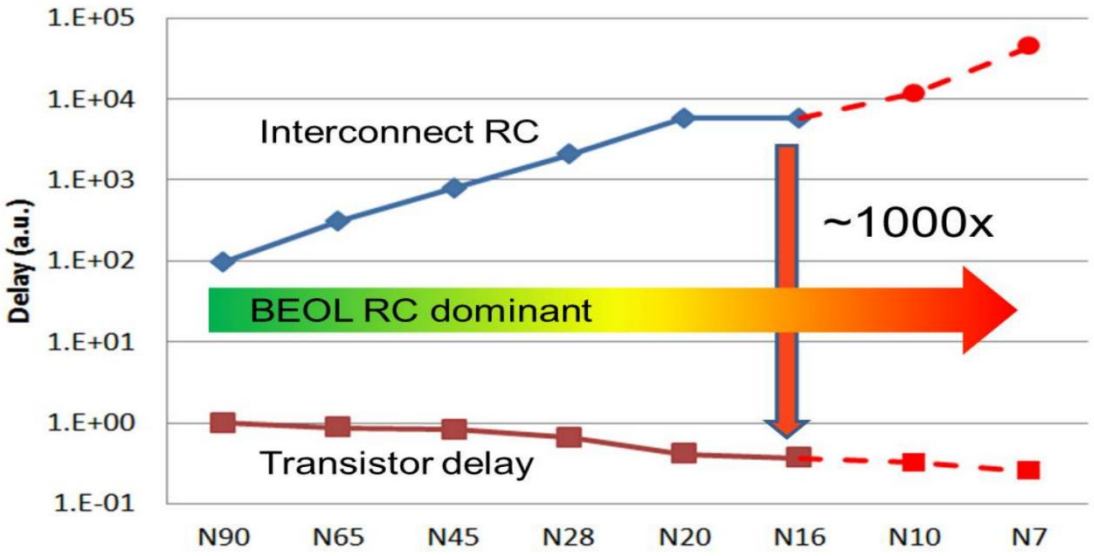


Figure 1.3 Comparison of RC delays between transistors and interconnects [23].

1.1 Cu Metallization in Integrated Circuits

The differences in material properties make the integration of Cu/low-*k* interconnect structures very different from Al/SiO_2 (Figure 1.4). Due to the lack of the

proper dry etch plasma chemistry, Cu lines cannot be patterned using the conventional subtractive etching approach. Also, unlike Al, Cu doesn't possess the self-passivation characteristics by forming a stable oxide layer. To overcome these integration challenges, a "dual damascene" process was introduced for Cu/ low-k interconnects [3]. Both trenches and via structures are patterned simultaneously by selectively etching the dielectric layer. The "via-first" approach is particularly useful when etching high aspect-ratio structures [24]. As illustrated in Figure 1.5, the via-first process starts with the patterning of the via throughout the 2 layers of the interlayer dielectrics (ILD), followed by a trench etch into the 1st ILD layer until reaching the etch stop layer. A barrier layer is applied to promote adhesion of the subsequent Cu seed layer to the underlying ILD material. Cu then fills up both via/trench structures by the electro-chemical plating (ECP) technique. After annealing, the Cu overburden is removed using chemical mechanical polishing (CMP). Finally the top Cu surface is capped with a dielectric layer such as SiC_xN_y.

Cu vias are considered as the weakest link and thus a serious reliability concern in the interconnect structure. As shown in Figure 1.4, there exists a misalignment between the via and liners below due to the cap layer on top of the Cu surface. Therefore, if a void forms underneath the via in the Cu below, there is no redundant layer for current shunting, resulting in early failures in Cu interconnects.

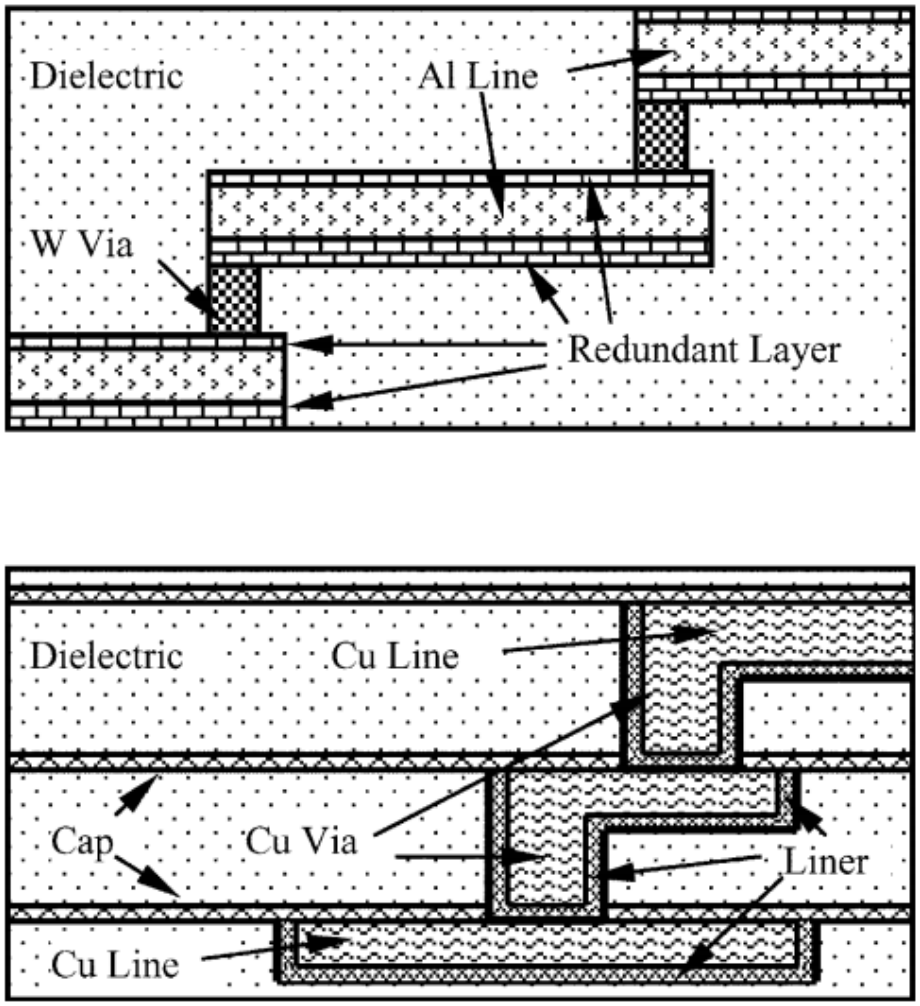


Figure 1.4 Schematics of layout structures and materials for Al (top) and Cu (bottom) interconnects [25].

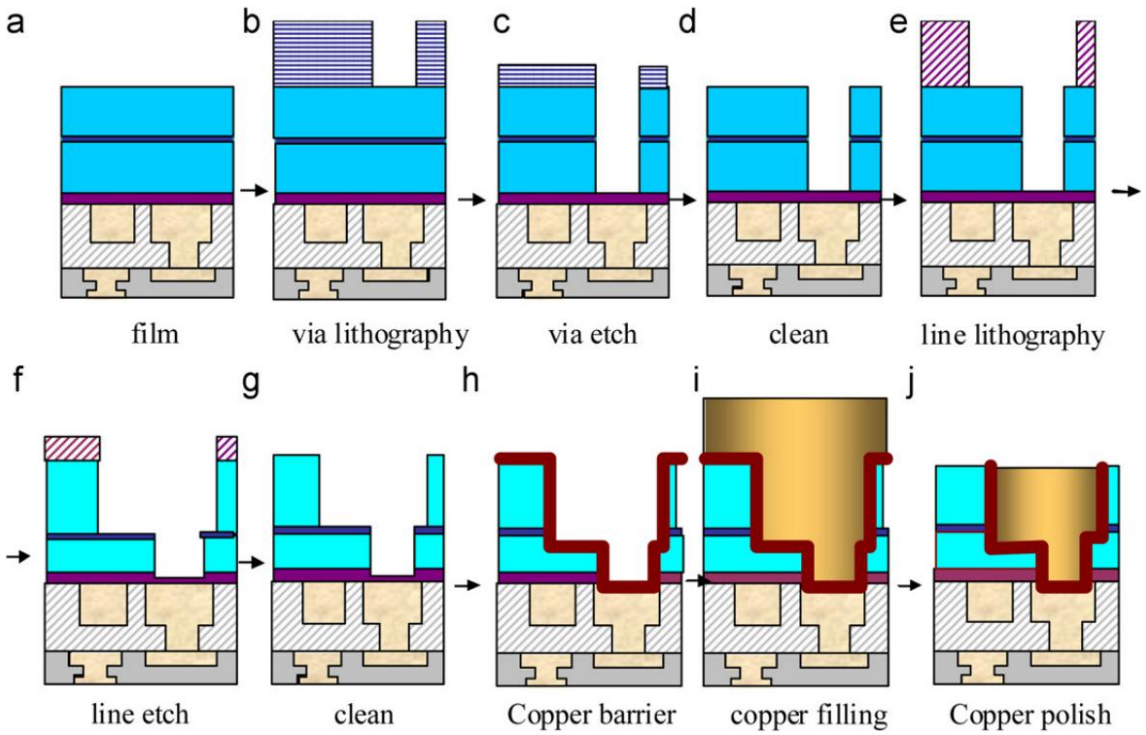


Figure 1.5 Schematic of Cu interconnect dual-damascene process (via-first) [24].

1.2 ELECTROMIGRATION PHENOMENON

1.2.1 EM-induced Diffusion Mechanisms

Electromigration is a diffusion-controlled mass transport phenomenon driven by the momentum transfer between the moving electrons and the metal ions [26, 27]. The EM-induced atomic flux can lead to void formation and extrusion shorts to fail the interconnect structure. The atomic flux driven by the "electron wind force" F_e can be written as $J = nv_d$, where n is the atomic density and v_d is the drift velocity of moving metal ions. The drift velocity is given by:

$$v_d = (D_{eff}/kT)F_e = (D_{eff}Z^*_{eff}/kT)e\rho j \quad (1.1)$$

where D_{eff} is the effective diffusivity of the metal ions, Z_{eff}^* is the effective charge, e is the electron charge, k is the Boltzmann constant, T is the absolute temperature, ρ is the metal resistivity, and j is the current density. In Cu damascene structure, EM mass transport mainly occurs via two fast diffusion paths, the Cu/SiCN cap layer interface and the grain boundary, with their activation energies the lowest among all available diffusion pathways. Diffusion activation energies for Cu interconnects have been measured to be 0.8–1 eV for the grain boundary and 0.8–1.1 eV for the Cu/SiCN interface, significantly lower than 2.2 eV for the bulk diffusion [25, 28]. Accordingly, the parameter $D_{eff}Z_{eff}^*$ can be expressed as:

$$D_{eff} Z_{eff}^* = (1 - f_c) \frac{\delta_i}{h} D_i Z_i^* + f_c \frac{\delta_{gb} f}{d} D_{gb} Z_{gb}^* \tag{1.2}$$

where the subscripts i and gb identify the diffusion pathways as the Cu/SiCN interface and the grain boundary, respectively. δ is the width of the interface or the grain boundary (typically 0.5 nm), d is the mean grain size, and h is the line thickness. The parameter f_c is the average length fraction of the cluster segment (the section composed of poly-crystalline grains), which represents the relative contribution of GB and interface diffusion to overall drift velocity for a Cu interconnect line. The interfacial and GB diffusivities can be experimentally deduced from the resistance evolution traces observed in EM testing, which will be covered in detail in Chapter 5. The interface diffusion D_i is strongly dependent on the orientation of the individual grain normal to the Cu/capping interface, with {111} being the fastest and {100} the lowest for FCC metals [21, 22]. The GB diffusion D_{gb} is also strongly microstructure dependent, with coherent twin

boundaries being the lowest diffusion path compared with other high-angle boundaries. It is worth noting that only those grain boundaries which have components aligned in the direction of current flow contribute to the EM mass transport. For instance, bamboo grains with grain boundaries aligned nearly perpendicular to the current flow direction essentially has zero GB contribution. Therefore, a geometrical factor *f* is defined as the average orientation of the grain boundaries relative to the current flow [29].

In order for EM-induced atomic flux to cause void formation, it is necessary to have flux divergence from unbalanced mass flow. Mathematically, it can be expressed by the continuity equation [28] as:

$$\frac{dn}{dt} = -\nabla J = -\frac{J_{out} - J_{in}}{\Delta x} \tag{1.3}$$

where n is the atomic density of the metal and J_{in} and J_{out} represent the Cu atomic flux entering and leaving at a certain location. The net mass flow determines the local flux divergence, where void formation occurs at positive flux divergence sites. In Cu interconnects, the metal adhesion/diffusion barrier liner creates material dissimilarity at the Cu line/via interface (blocking boundary) and causes the imbalance of the diffusion flux. In addition, variations of the local microstructure can change diffusivity of Cu and induce EM flux divergence at places without material discontinuity. For instance, void formation commonly occurs at grain boundary/interface triple junctions bounded by neighboring Cu grains with different sizes and crystallographic orientations. To evaluate the flux divergence, it is necessary to determine the local grain structure in the line and the corresponding diffusivities for adjacent grains.

1.2.2 EM-induced Backflow Stress (Short Length Effect)

Under EM, Cu atoms are transported from the cathode end to the anode end following the direction of the electron flow. As a result, the depletion of atoms at the cathode end induces local tensile stress and the accumulation of atoms at the anode end induces a local compressive stress (Figure 1.6). The resultant stress gradient gives rise to a backflow of atoms towards the cathode, counteracting the role of electron wind force. The net drift velocity combining these two opposing transport mechanisms can be expressed as:

$$v_d = \frac{D_{eff}}{kT}\left(Z^*_{eff} e\rho j - \Omega \frac{d\sigma}{dx}\right) \tag{1.4}$$

where Ω is the atomic volume and $d\sigma/dx$ is the back-stress gradient within the conductor. An important implication of this back-stress effect is that for sufficiently short lines or low current densities, the stress gradients can completely suppress mass transport. At the steady state, a linear stress profile is attained along the conductor. The balance of EM and stress-induced backflow (v_d = 0) defines a threshold $(jL)_c$ product as:

$$(jL)_c = \frac{\Omega \Delta\sigma}{eZ^*_{eff}\rho} = \frac{2\Omega\sigma_c}{eZ^*_{eff}\rho} \tag{1.5}$$

where L is the conductor length and $\Delta\sigma$ is the stress difference cross the conductor. For a Cu damascene structure, the value of $\Delta\sigma$ that can be sustained depends on the mechanical confinement on the Cu structure imposed by ILD and the surrounding barrier and cap layers. In addition to the mechanical strength of the surrounding materials, the anode end of the line has to be connected to a complete blocking boundary to generate the short-

length effect. Once the stress at the cathode reaches a critical value (σ_c), a void will be nucleated. Different from Al interconnects, void can nucleate more readily at the Cu interface near the cathode end under a moderate tensile stress of about 100 MPa [30, 31]. Equation (1.5) describes the (jL) condition below which EM damage is completely eliminated.

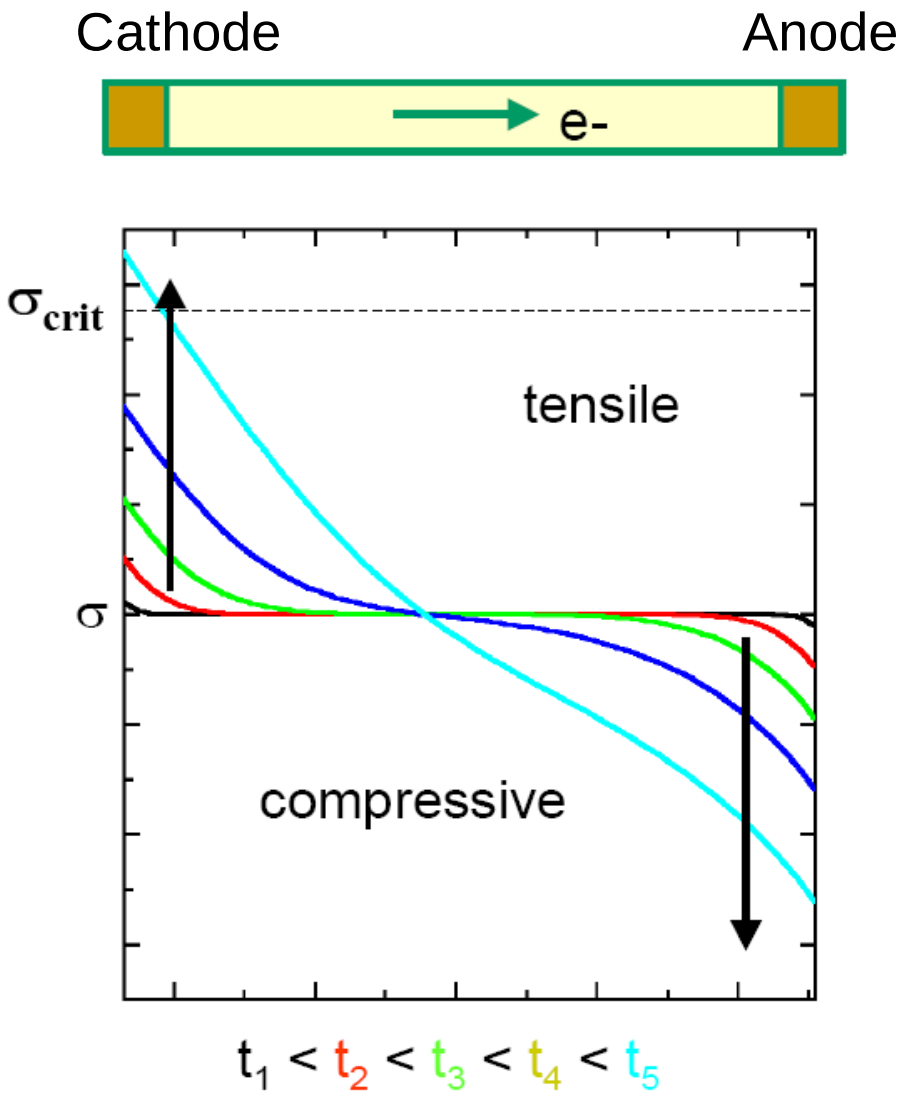


Figure 1.6 Schematic of stress evolution during EM [30].

Once the void is nucleated the stress in the vicinity of the void is reduced to zero and the stress distribution along the conductor changes. The void continues to grow through mass transport from the void to the anode and eventually a new steady state will be established (Figure 1.7). A new threshold product where void growth saturates at a critical size ΔL_{cr} is defined as:

$$j_c L^2 = \frac{2\Omega B \Delta L_{cr}}{eZ^* \rho} \tag{1.6}$$

where B is the effective bulk modulus of the conductor and the surrounding dielectric structure. Suo [32] has shown for equally spaced interconnects B may be approximated by:

$$B \approx G_{ILD} + G_L \frac{t_b}{w} \tag{1.7}$$

where G_{ILD} and G_L are the shear modulus for the dielectric and trench barrier liner, respectively, t_b is the thickness of the liner and w is the conductor width. Equation (1.6) describes the $j_c L^2$ condition where EM damage is limited by the critical void size.

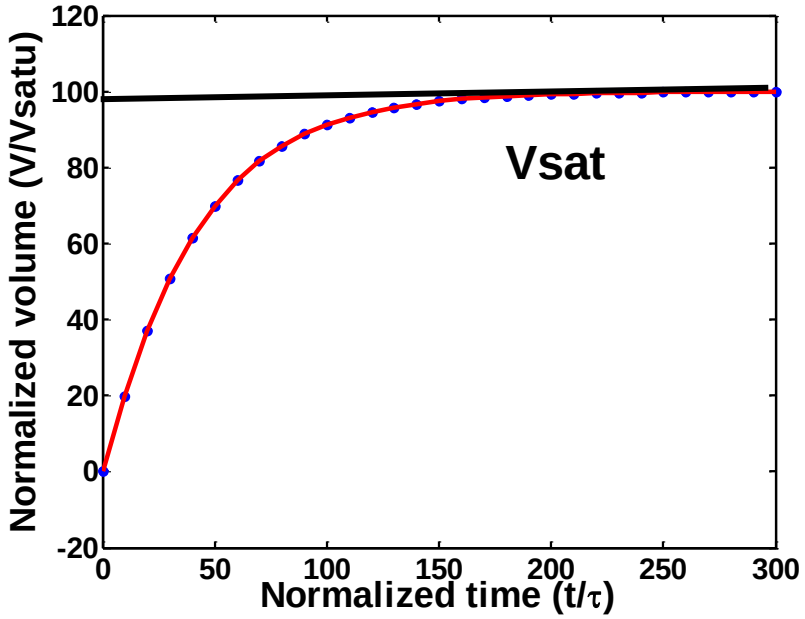


Figure 1.7 Illustration of void size as a function of time during EM calculated using Korhonen's model [33, 34].

The short length effect has been effectively used to extend the current carrying capability of conductor lines and has dominated the current density design rule for interconnects. It has been shown that immortality is reached for a given current density or wire length below the limit of the critical product $(jL)_c$. However, since EM is statistical in nature failures still occur for a large population of nominally identical conductors (typical of ICs) when the sample average is below j_c [35]. Moreover, ultrathin barrier layers (t_b < 30Å) that are required for RC reduction may be permeable to Cu. This partial blocking boundary would lead to a reduction in the compressive stress in the anode region and consequently a reduction in the stress gradient associated with the EM flux. Therefore, the actual $(jL)_c$ value would be lower than theoretically predicted.

1.3 EM CHALLENGES AND ENHANCEMENT SOLUTIONS

1.3.1 EM Lifetime Scaling

Hu *et al.* [28, 29] have proposed a simple model to predict the EM lifetime degradation based on the growth rate to reach the critical-size void as:

$$\tau = \frac{\Delta L_{cr}}{v_d} = \frac{(\Delta L_{cr} h) kT}{D_i \delta_i Z_i^* e \rho j} \tag{1.8}$$

where τ is the EM lifetime, ΔL_{cr} is the critical void length to fail the line under EM, and v_d is the drift velocity. This is essentially a geometrical model assuming that the void is located at the cathode end of the interconnect wire containing a single via and the EM drift velocity is dominated by interfacial diffusion. Assuming constant current density, the model predicts τ scales with the product $\Delta L_{cr} h$. If the critical void size is about the same as the line width w, τ would be scaled with wh, the cross-sectional area of the line, or $1/s^2$ with s being the scaling factor. For each technology generation, the line dimensions are scaled by a factor of ~0.7, which yields a reduction of ~50% in EM lifetime. This trend has been confirmed by Hu *et al.* for Cu interconnects with the SiCN cap (Figure 1.8).

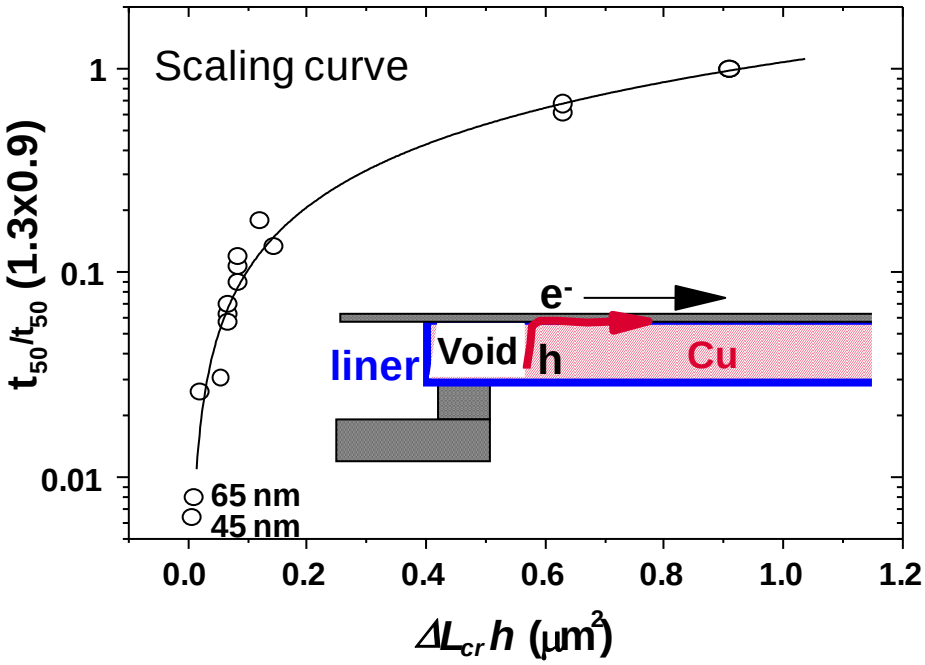


Figure 1.8 Evolution of EM lifetime with interconnect scaling. Circles represent experimental data in [28].

At the 65 nm node and beyond, τ was found to degrade due to the emergence of small grains which contributed to the mass transport via grain boundary diffusion. Combining the contribution of the Cu/SiCN interface and the grain boundary on EM mass transport, EM lifetime can be expressed as [29]:

$$\tau = \frac{\Delta L_{cr} hkT}{Z_i^* D_i \delta_i e\rho j(1+ fgh/d)} \tag{1.9}$$

where $g = Z_{gb}^* D_{gb} \delta_{gb} / Z_i^* D_i \delta_i$, which is the ratio of the mass transport via grain boundaries vs. the cap interface. The grain structure effect on EM lifetime can be estimated by considering the term (1 + *fgh/d*). For sub-100 nm lines, the emergence of the small grains can significantly enhance the grain structure effect. In this case, the size of the small grain can be considerably less than the line height and with most of the

boundaries inclined to the current flow and thus subject to EM driving force. Therefore, the grain boundary contribution to mass transport can be substantial.

The EM lifetime is inherently statistical in nature as it is related to the rate of damage formation at various flux divergence sites. In addition to EM lifetime as described in the scaling model, it is important to take into account the EM lifetime statistics, particularly when extrapolating the EM lifetime to the operating condition for a large ensemble of interconnects. A microstructure-based EM kinetic model will be discussed in Chapter 5 to evaluate EM lifetime and its statistics for nanoscale Cu interconnects.

1.3.2 EM Enhancement: Metal Capping and Alloying

1.3.2.1 Selective Metal Capping

Different methods have emerged to enhance the EM resistance of Cu by suppressing the fastest diffusion path at the Cu/cap layer interface. The most efficient one is to add a thin metal layer, such as selective CoWP plating [7, 8] or selective chemical-vapor deposition (CVD) of Co or Ru [36-38], between the Cu trench and the dielectric SiCN cap. The CoWP is formed selectively on Cu using electroless plating with either Pd activation or self-activation (Figure 1.9). Compared to the interfacial bonding between Cu and SiCN dielectric cap (metal-dielectric bond, adhesion energy: 10-20 J/m^2 [39]), an additional layer of CoWP in between enables a stronger interface adhesion with Cu (metal-metal bond, >40 J/m^2 [39]) and thus substantially slows down the migration at the interface (Figure 1.10). This corresponds to an increase in EM activation energy from 0.9 eV to 1.2 eV [39].

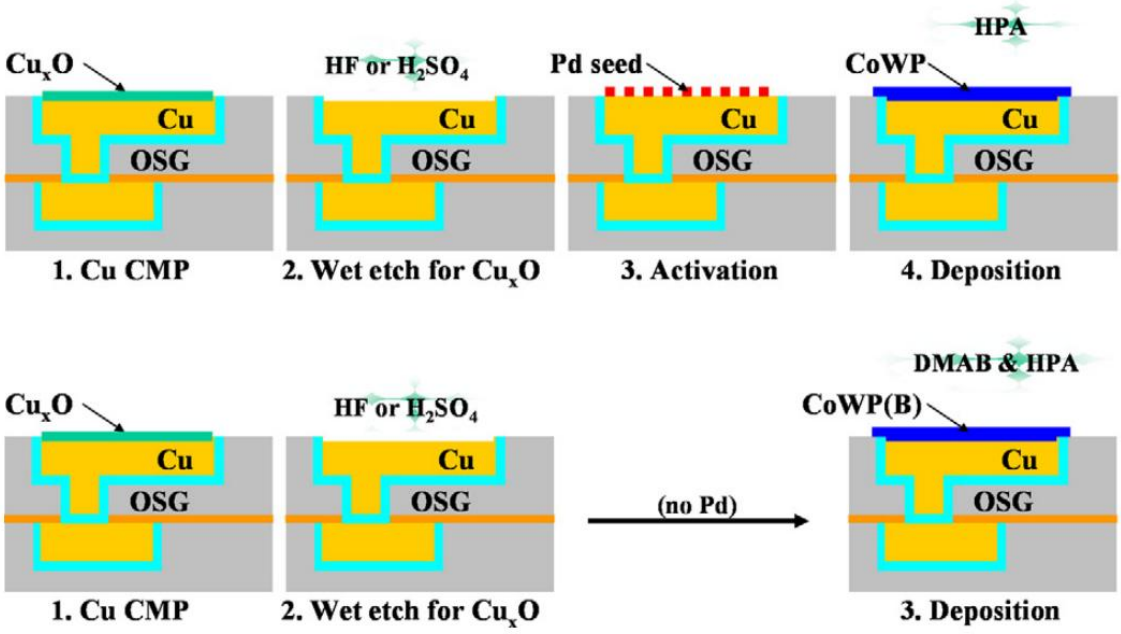


Figure 1.9 Process flows of electroless deposition of CoWP on Cu with Pd activation (top) or with self-activation (bottom) [7].

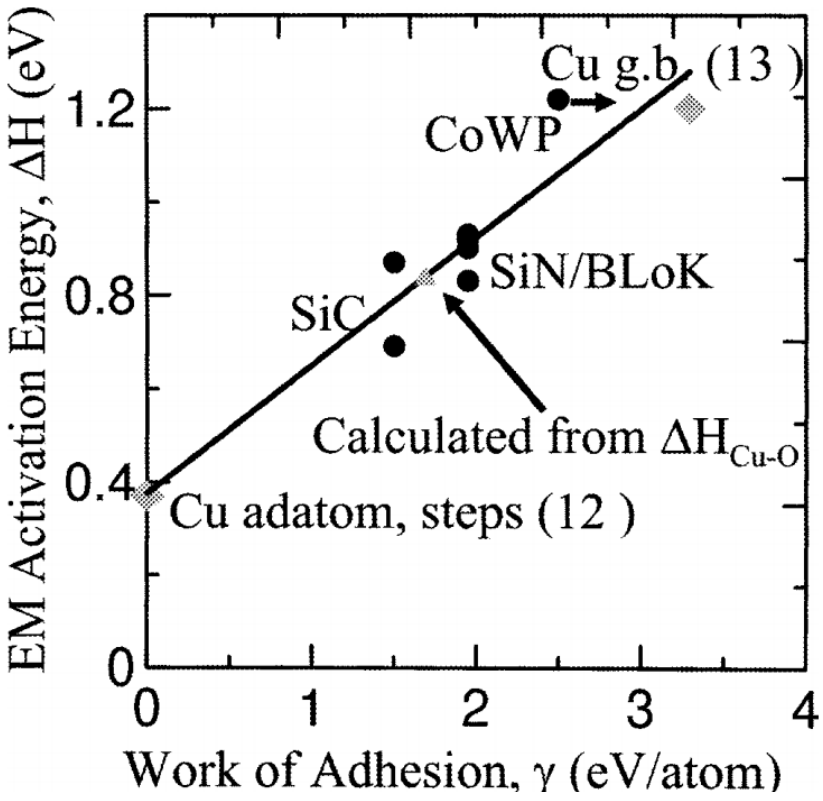


Figure 1.10 EM activation energy as a function of the work of adhesion for Cu/dielectric and Cu/CoWP interfaces along with literature data for diffusion along a Cu surface and in a Cu grain boundary. Note the work of adhesion for Cu/CoWP is a lower bound [39].

CoWP + dielectric cap was found to improve EM lifetime of Cu interconnects over 100x [7]. However, the spread in EM lifetime distribution is greater compared to those with a stand-alone SiN cap. The larger sigma could be attributed to the non-uniformity in the CoWP thickness and the sensitivity of CoWP metal capping to processing defects. It is very challenging to grow a sufficiently thick CoWP which can enhance EM and meanwhile have a high selectivity relative to the surrounding dielectrics to avoid shorting and leakage.

1.3.2.2 Cu Alloying

An alternative approach of improving cap layer adhesion is to introduce minor dopants (<1.0% in the concentration) into Cu trench, such as Mn, Al, Ti. There are 3 basic options for making Cu alloy interconnects (Figure 1.11). Dopants can be introduced into plated Cu from alloyed seed layers (Figures 1.12a-f), from the Cu top surface (Figures 1.12g-i), or by the direct plating of Cu alloy (Figures 1.12j-l). Among these options, alloy seed layer is the most popular approach to improve interconnect reliability. During subsequent high temperature processes (*e.g.* cap layer deposition), dopants will redistribute in the Cu, segregate to the top interface and bond chemically to the capping layer.

Mn has been reported as the best candidate for the alloy seed layer approach. The main challenge with alloy seed layers is the increase in resistivity caused by the incomplete segregation of dopant atoms from the solid solution. Mn forms a solid solution with Cu without intermetallic compound formation. And Mn can easily escape from the solid solution, resulting in a low final resistivity. Furthermore, Mn reacts more actively with oxygen compared to Cu, which provides a driving force for the dopant segregation.

The cap/Cu interfacial adhesion has been reported to increase significantly with Mn doping. A double layered MnO/Mn segregation structure was proposed by Nogami *et al.* [11]. In addition to Mn-O formation which is self-limited due to the limited supply of O atoms, the excess of Mn can diffuse through Cu grain boundaries and form a metallic state of Mn at Cu/SiCN interface to improve EM performance. Mn can also help patch some local liner defects (Figure 1.12) or can even be used as a "self-forming" barrier to replace Ta/TaN by forming Mn oxide or silicate.

Mn alloyed seed layer was developed for the 32 nm node and has been shown to enhance EM lifetime up to 10x depending on the doping concentration [11]. Even though Cu(Mn) may not be as effective as CoWP in slowing down the interfacial diffusion, it can reduce the GB diffusion and repair local defects in the ultra-thin barrier, resulting in a tighter lifetime distribution (σ: 0.3-0.5). In ultra-fine Cu lines where a large population of small grains mixing with bamboo-type grains, grain boundary diffusion makes a large contribution to EM-induced mass transport. With the interface diffusion suppressed by CoWP or Mn alloying, the grain structure effect becomes even more important. Therefore, a good control of Cu microstructure is essential to maximize their effectiveness.

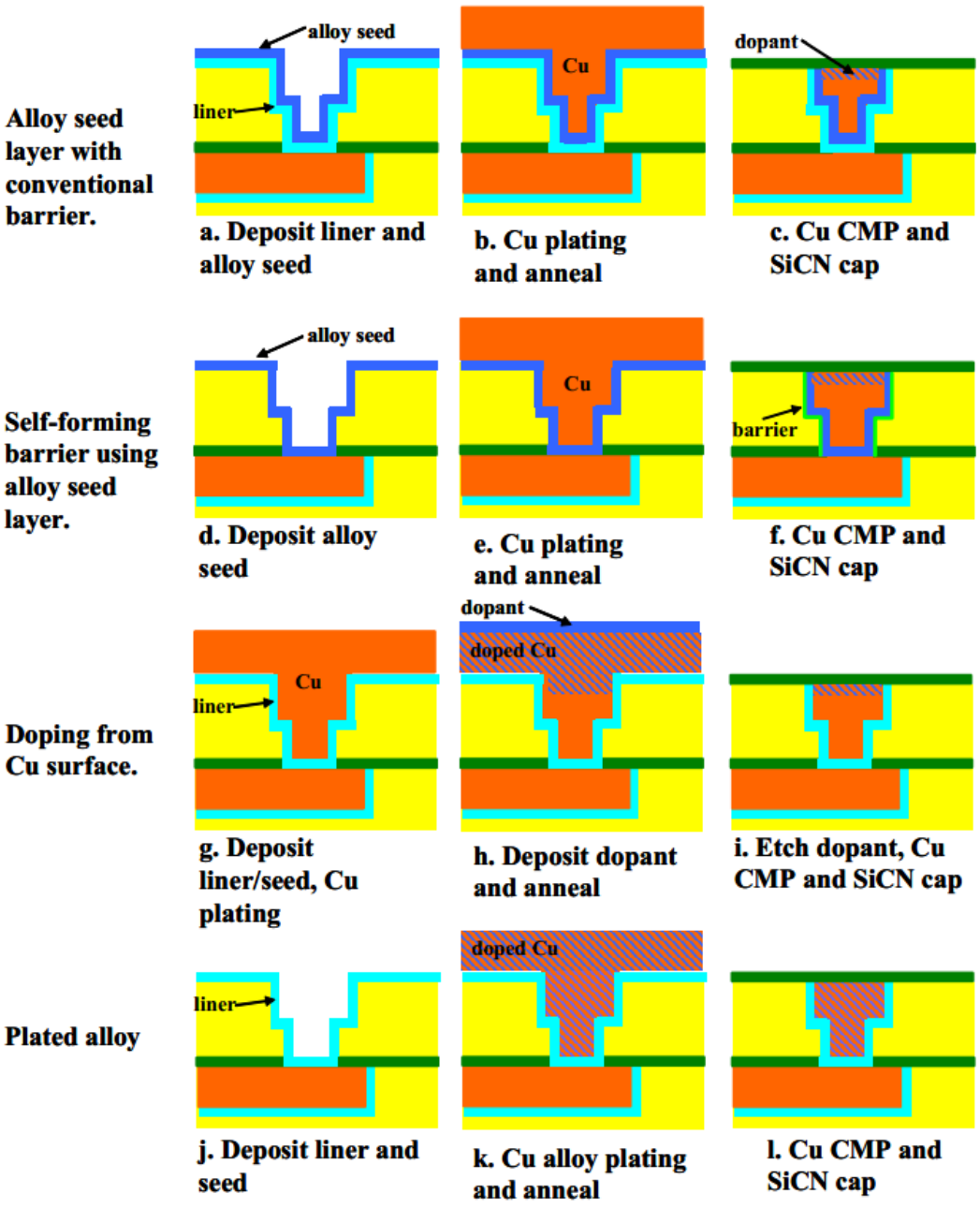


Figure 1.11 Schematics of Cu alloying processes [12].

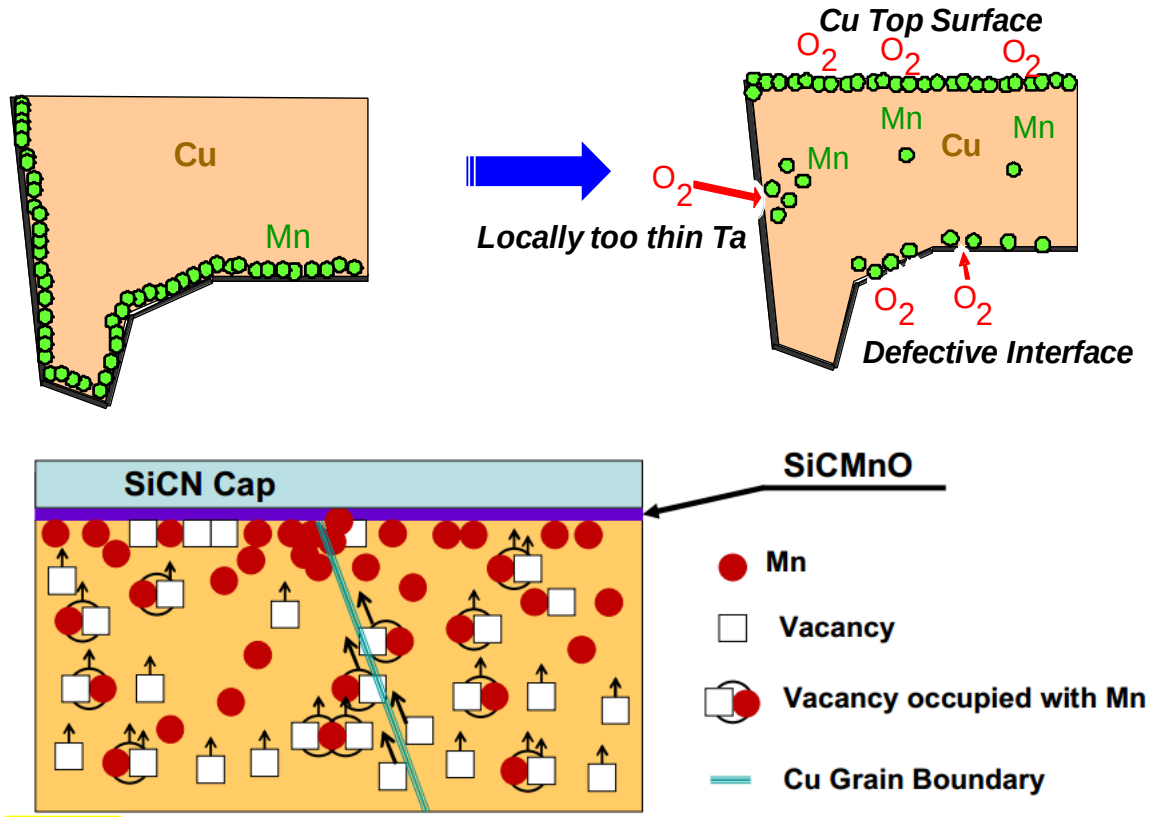


Figure 1.12 Schematic of the mechanism of Mn alloying in Cu seed layer as an effective EM resistance booster [11].

1.3.3 Effects of Cu Microstructure on EM Reliability

EM mass transport along active diffusion paths is strongly microstructure dependent and the microstructure effect on EM reliability has been studied extensively [40-42]. For dual-damascene Cu interconnects, with interfacial diffusion dominating EM mass transport, the impact of microstructure on EM was expected to be less influential. However, a recent study by Hu *et al.* [43] showed that the emergence of polycrystalline Cu grain structure in fine lines for the 65 nm node technology and beyond markedly reduced the Cu EM reliability due to the grain boundary contribution to the overall mass

transport. With continued scaling, it is important to study how Cu grain structure will evolve and its impact on EM reliability [17, 29, 44]. Moreover, when the Cu/cap interface is improved by process optimization, the effect of Cu microstructure on the EM lifetime is more pronounced. This raises an interesting question regarding the microstructure effect on EM performance when the Cu cap interface is further improved by a metal capping.

Specifically, the diffusivity of Cu atoms across free Cu surfaces has been reported to depend strongly on the grain orientation. The activation energy for surface diffusion on Cu {111} surfaces is significantly lower than on {100} or {110} surfaces [45, 46]. In Cu interconnects, the surface is usually covered with a dielectric capping layer. Hence, the activation energy for interface diffusion will depend on the atomic structure and the chemical bonding of the interface, relating to the adhesion between Cu and the capping layer [39]. However, since the effect of grain orientation on diffusivity is not well known for Cu, it is assumed that it follows the same trend as the variation of surface diffusivity. Another effect of the microstructure on the EM behavior in Cu interconnects is the effect of grain orientation on void formation, such as high energy versus low energy boundary and their inclination angles towards the line. Variations of the local microstructure can change diffusivity of Cu and cause an electromigration flux divergence, particularly at the grain boundary/interface triple junctions [46].The influence of microstructure on mass transport and EM reliability has been examined by Meyer *et al*. [47]. In-situ scanning electron microscope (SEM) studies combined with electron back-scattering diffraction (EBSD) analysis showed that void formation and growth under EM occurred mainly at local interface junctions of small grains, depending on grain orientation. Due to the elastic anisotropy of copper, the grain orientation can also affect the local stress evolution

during void formation. Since the microstructure is statistical, the EM lifetime will also be statistical in nature, which has been observed to follow lognormal statistics [48].

Beyond the 32 nm node, Cu resistivity has been found to increase above the bulk value (1.75 μΩ cm) with decreasing Cu line width [49, 50]. For ultra-fine Cu interconnects, the resistivity of Cu is expected to approach that of Al, diminishing the benefits of Cu in reducing RC delay. This size effect was traced to the increase in electron scattering at grain boundaries and surfaces as the Cu line width approaches the electron mean free path (39 nm at room temperature for Cu). Grain structure evolution of ultrafine Cu interconnects has to be better understood and optimized for both reliability and resistivity improvement.

1.4 ORGANIZATION OF THE DISSERTATION

The objectives of this work are summarized as follows:

1) To investigate the effects of scaling and grain structure on EM lifetime, statistics, failure mechanisms, and void formation kinetics of Cu interconnects with metal capping and alloying down to the 22 nm technology node.

2) To investigate the effect of geometrical scaling on microstructure evolution of Cu interconnects down to the 22 nm technology node, using a novel high-resolution orientation mapping technique. Here the aims are: a) To establish a database on grain orientation, texture, grain size and grain boundary characteristics for electroplated Cu interconnects, and b) To analyze the mechanisms of abnormal grain growth (energetics vs. kinetics) for Cu lines of current nodes and beyond.

3) To develop a microstructure-based kinetic model to analyze the grain structure and cap layer effects on EM lifetime and statistics taking into account the statistical

distribution of the grain structure and mass transport at interfaces and grain boundaries; To project the scaling effect on EM lifetime and Cu line resistivity beyond the 22 nm node.

This dissertation is organized as follows:

Chapter 2 gives a brief description of the EM testing system, the statistical analysis of the EM failure distribution, failure analysis and the precession electron diffraction (PED) in transmission electron microscopy (TEM) for microstructure analysis.

Chapter 3 describes experimental studies of EM reliability for Cu interconnects with standard SiCN capping, CoWP metal capping and Mn alloying. The effect of grain structure on EM behaviors of Cu interconnects with CoWP capping is also discussed. The EM enhancement from CoWP and Mn alloying will be compared in terms of EM statistics, failure modes and the overall diffusivity.

In Chapter 4, the effects of scaling on the microstructure evolution of Cu interconnects are investigated. Here the grain growth mechanisms in Cu thin film structures is first reviewed along with the microstructure studies on Cu wide lines. Then, the results of the microstructure characteristics of nanoscale Cu interconnects from the 45 to 22 nm node are discussed in terms of grain orientation, grain size and grain boundary distributions. Finally, the roles of the surface/interface energy and elastic strain energy associated with the abnormal grain growth are examined in order to understand the variations of Cu texture, grain size and coherent twin boundary population with interconnect scaling.

In Chapter 5, a microstructure-based kinetic model is developed to evaluate the effects of capping layer and grain structure on EM lifetime and statistics of Cu interconnects. The model is extended from Korhonen's classic theory of stress evolution during EM. The microstructure of the Cu line is simplified into a series of bamboo and

cluster segments. The statistics of cluster length distributions as obtained from the PED analysis is shown to correlate with the EM failure statistics using the weakest link approximation.

This dissertation concludes with a summary of main contributions and future work.

Chapter 2: Experimental Methodology

2.1 Accelerated Lifetime Testing

EM tests are typically conducted with constant DC current at elevated temperatures and current densities compared to use conditions to obtain lifetime distributions in a reasonable time. Test data under accelerated EM testing is extrapolated to use conditions using industry-standard Black's Equation [51]. It is an empirical relationship showing mean time to failure (*MTTF*) as a function of temperature and current density:

$$MTTF = Aj^{-n} \exp(E_a/kT) \tag{2.1}$$

where A is a constant, j the current density, n the current density exponent, E_a the activation energy, k Boltzmann's constant, and T the device temperature. In addition, only a limited number of lines are being tested, whereas hundreds of millions of interconnects exist on each chip. Hence, the extrapolation needs to take into account how to assess on-chip interconnect reliability from the EM-tested sample population. Time to failure under use conditions and required cumulative failure percentile target (*e.g.* 10^{-4}%, the so-called -6σ), TTF_{oper}, can be described as [52]:

$$TTF_{oper} = MTTF_{stress}\left(j_{stress} / j_{oper} \right)^{n} \exp\left[\frac{E_a}{k}\left(\frac{1}{T_{oper}} - \frac{1}{T_{stress}} \right) + NSD \cdot \sigma \right] \tag{2.2}$$

where the subscripts 'stress' and 'oper' refer to EM testing and actual operating conditions, respectively. σ is the lognormal standard deviation and *NSD* is the number of standard deviations. The variable *NSD* represents the target cumulative failure percentile,

which is used to extrapolate the time to, for example, 10^{-4}% failure value under use conditions from the experimentally obtained 50% time-to-failure. When extrapolating to use conditions for a very low failure percentile, the distribution with a smaller σ can be more advantageous although the median time-to-failure is shorter. This is where Mn alloying is superior to CoWP metal capping. For pure Cu, E_a has been found to be ~0.9 eV with the EM mass transport primarily along the Cu/dielectric cap interface. The reported n values vary significantly between 1 and 2, depending on the relative contribution of void nucleation and void growth. For the extrapolation purpose, conservative values of $E_a \sim 0.9$ eV and $n \sim 1$ are usually being used.

2.2 EM TESTING STRUCTURE

Standard EM testing is performed in Cu line structures containing multiple wiring levels fabricated by the damascene technique. The EM test structure for the technology node of interest is composed of either a single line (single-link) or multiple lines arranged in series (multi-link) terminated by vias at both ends to a lower or upper feeder line. These feeder lines are made wide and short in order to minimize the EM failure probability in them. EM test line is typically designed to be long enough to minimize the short length effect and to fail the test line within a reasonable amount of time. If the electron current flows from a upper metal level through the via into the test line, the test is called “downstream”, whereas it is called “upstream” for test lines located at the upper metal level. To achieve the testing flexibility for both downstream and downstream, it is desirable to design a three-level EM test structure. The single-link test structure is studied in this work (Chapter 3).

2.3 EM TESTING SYSTEM AND TESTING PROCEDURE

Typical procedure of an EM reliability testing is outlined in Figure 2.1. All test structures used in this work are fabricated by GLOBALFOUNDRIES Inc. EM tests are performed at the package level (Figure 2.2) in a high-vacuum testing system at UT Austin (Figure 2.3).

An accurate control of constant current density in devices under test (DUTs) is assured by an array of customized constant current boards. In each channel of the board, a dummy resistor of 1095 Ω is connected in series with a DUT. The potentiometer associated with each resistor is adjusted before testing to obtain the desired current level through each channel. A Keithley 196 digital multimeter is used to measure the voltage drop across each DUT. The cyclic monitoring of the real-time resistance data for each DUT is achieved by a Keithley 7002 switch system and a LabVIEW program developed in this lab.

The testing temperature is maintained by two heating plates at the top and the bottom of the chamber. They are controlled separately by two temperature controllers. The uniformity and stability of the chamber temperature is improved with additional heating coils at the peripheral of the chamber and a back filling of pure N_2 to about 20 Torr.

Once the resistance of some DUT reaches a certain failure criterion (*e.g.* 10% resistance increase in this work), the current of that channel is switched off manually to stop further EM damage. After most of samples fail or a reasonable amount of time is reached, the EM test is terminated. Resistance evolution as a function of time for individual samples and their failure distribution is then analyzed. Failure analysis for some selected samples is performed to examine their void formation and related failure mechanisms.

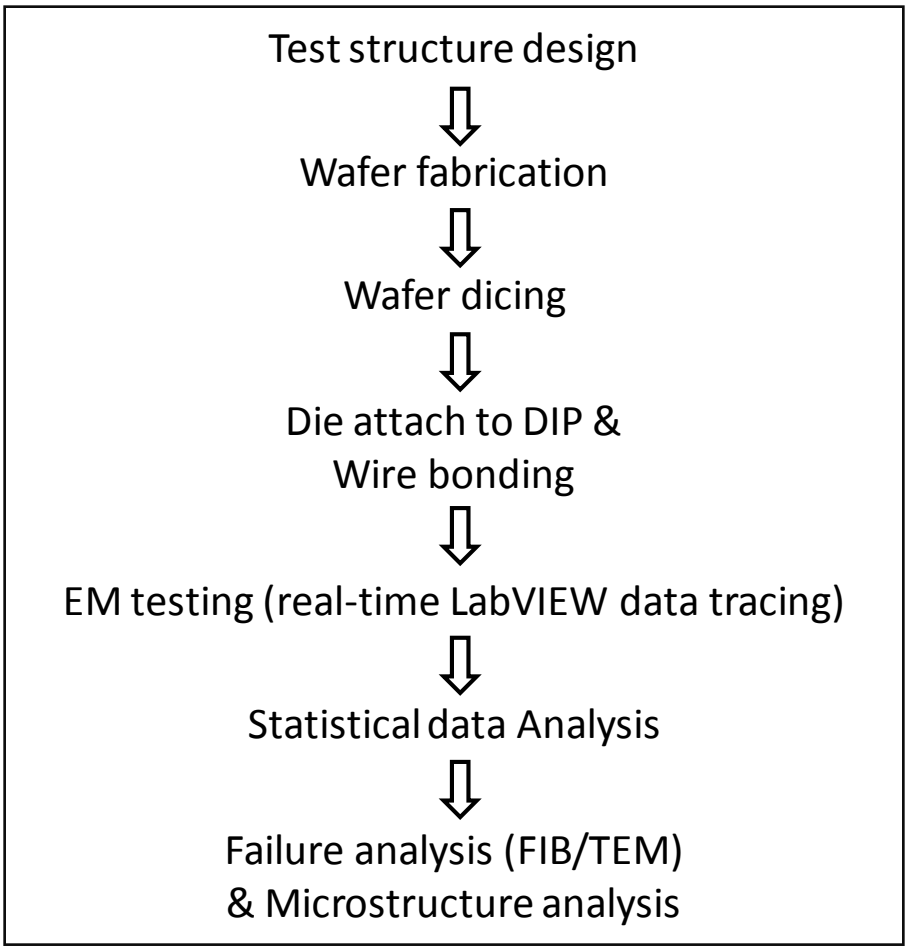


Figure 2.1 Typical procedure of an EM experiment.

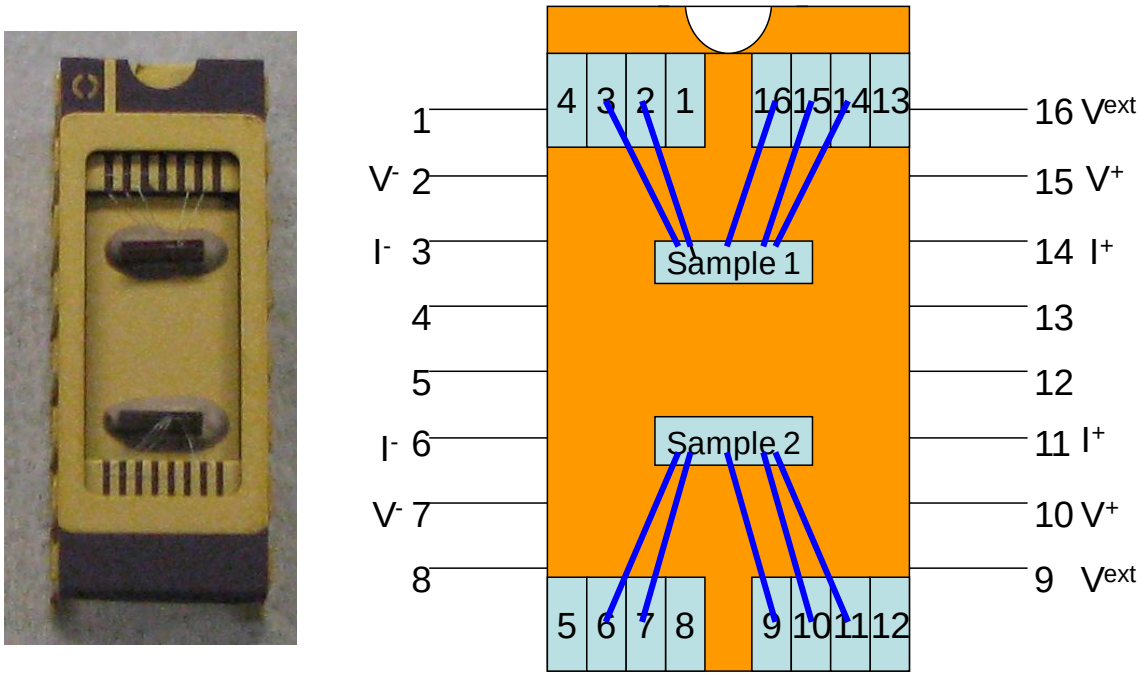


Figure 2.2 Left: 16-pin dual-in-line package with 2 DUTs attached and wire-bonded. Right: the wiring configuration of the customized EM testing system in this work.

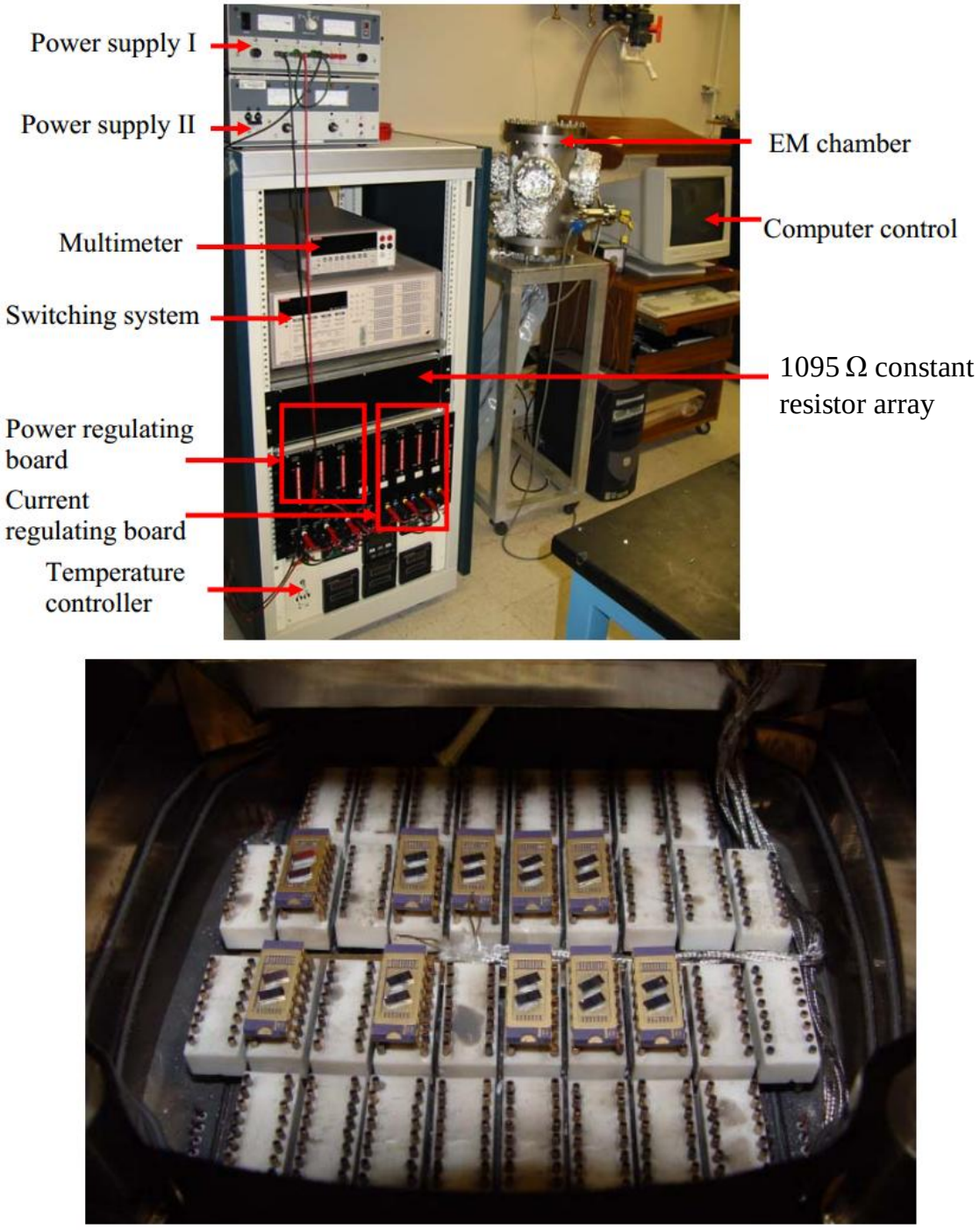


Figure 2.3 In-house package-level EM testing system with a close-up of the interior of the chamber.

2.4 RESISTANCE TRACES

The resistance change of the test structure as a function of time was monitored during the EM test to help determine the EM lifetime and the failure mechanism. The resistance trace is well known to reflect void growth kinetics and void morphologies.

A small initial resistance increase followed by a gradual resistance climb, as shown in Figure 2.4, is a typical resistance change for a Cu interconnect with voiding in the trench line away from the via. The resistance trace in this case is composed of three stages. At Stage I, the resistance remains almost constant with a slight increase. The EM-induced void nucleates at the Cu/cap layer interface (*e.g.* Figure 2.5) and continues to grow downwards towards the bottom of the trench. Until Cu is completely depleted of the whole cross section area, current can still pass through the remaining Cu region, making the resistance increase electrically undetectable. Once the void grows to span the whole line thickness, the current has to go through the highly resistive Ta/TaN barrier layer (150-220 μΩ cm for β-Ta), causing a sudden step-like resistance increase (R_{step}) at Stage II. With the Ta/TaN barrier layer as a current shunting path, the void further grows by edge displacement [28] in the direction of the electron flow, causing a progressive resistance increase at a constant rate (R_{slope}). For this type of resistance trace, the EM lifetime is determined as the time when the first resistance jump occurs or a fixed proportion of resistance increase is reached (typically 10% as the failure criterion).

In addition, an abrupt resistance jump to infinity at Stage II could occur when a slit-like void forms underneath the via for the downstream EM test and extends to cause open failure. It could also be a premature extrinsic failure caused by process-induced defects in the line or an ultrathin barrier layer (for the upstream stressing). In this case, the EM lifetime is determined as the onset of the resistance pop-up.

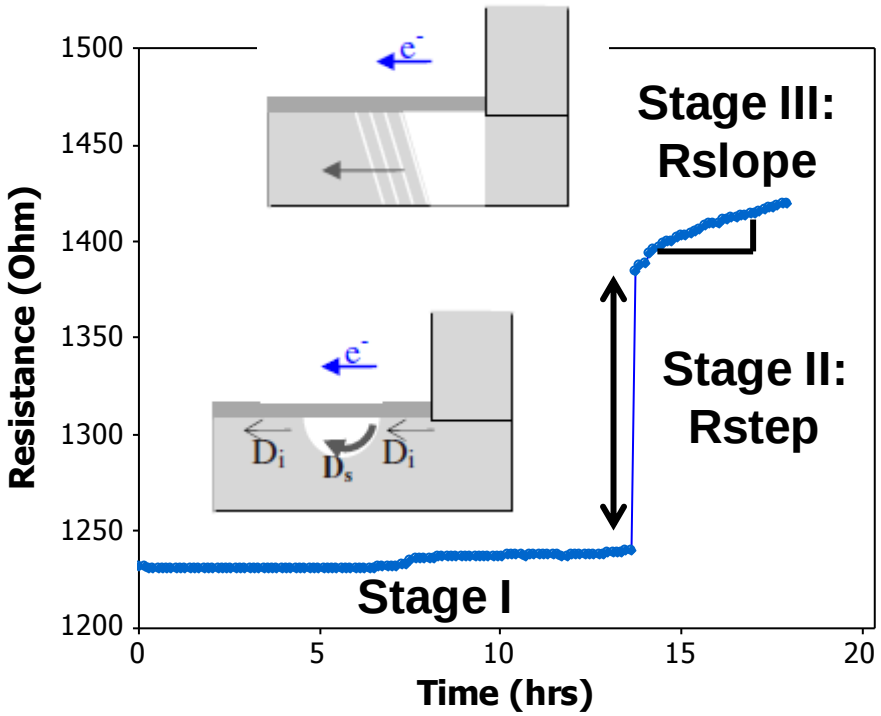


Figure 2.4 Typical resistance trace observed during EM testing with 3 distinct stages. The corresponding void morphology is also included.

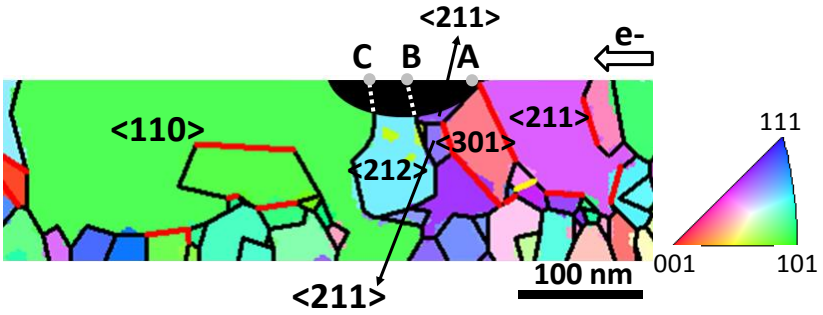


Figure 2.5 Color-coded grain orientation mapping for a Cu line with a slit-shape void formed at the top interface. Points A, B, and C are assumed to be potential flux divergence sites prior to the void formation. The void was probably first nucleated at C (the largest flux divergence site), and then grew further to B and A driven by the inner void surface diffusion in the direction opposite to electron flow [46].

Parameters inherent to EM degradation kinetics can be extracted from detailed analysis of resistance traces, which provides valuable information about physical mechanisms involved in EM-induced void nucleation and growth. R_{step} [53] is found linearly proportional to the critical void length l_c (the one associated with the resistance jump failure)

$$R_{step} = \frac{\rho_b}{A_b} l_c \tag{2.3}$$

where ρ_b is the resistivity of the barrier layer and A_b is the barrier cross section. R_{slope} can be correlated to the EM-induced mass transport as

$$R_{slope} = dR/dt = \frac{\rho_b}{A_b} v_d \tag{2.4}$$

where v_d is the Cu drift velocity. The effective diffusivity of Cu atoms under EM can be then extracted from R_{slope} based on its relationship with v_d

$$D_{eff} = \frac{kT}{Z^*_{eff} e \rho j} \cdot v_d \tag{2.5}$$

More discussion about resistance trace analysis will be given in Chapter 3.

2.5 EM LIFETIME STATISTICS - LOGNORMAL DISTRIBUTION

From resistance traces, the failure time of each sample can be acquired as t_i (i = *1,…,N*). N is the sample size (typically <30 for the single-link structure). Lognormal

distribution has been traditionally used to describe the EM failure characteristics. The lognormal probability density function of failure (PDF) in time t is given by

$$f(t) = \frac{1}{\sigma t\sqrt{2\pi}} \exp\left(-\frac{(\ln t - \ln t_{50})^2}{2\sigma^2}\right) \tag{2.6}$$

where t_{50} is the median time to failure and σ the lognormal standard deviation. The cumulative distribution function (CDF), which describes the probability that an interconnect fails within the time interval [0, t], can be expressed as

$$F(t) = \int_0^t f(u)du = \frac{1}{2\pi^2}\int_{-\infty}^{z} e^{-\frac{v^2}{2}}dv = \frac{1}{2}erfc\left(-\frac{z}{\sqrt{2}}\right) \tag{2.7}$$

where $z = [ln(t) - ln(t_{50})]/\sigma$. The CDF value of a interconnect line failure within time t_i can be estimated based on the median rank theory

$$F(t_i) = \frac{i - 0.3}{N + 0.4} \tag{2.8}$$

where i is the index of the sample after all the samples are sorted by time to failure as $t_{min}, \ldots, t_i, \ldots, t_{max}$.

2.6 FAILURE ANALYSIS

Selected samples with distinct resistance traces and (or) failure times are cross sectioned using a focused ion beam (FIB) system to expose the void morphology and its location (Figure 2.6). A FEI Strata™ Dual Beam system is used in this study. The dual

beam system incorporates both a FIB and a scanning electron microscope (SEM) in a single system. This combination offers several advantages over a single-beam FIB system, especially for precision sample preparation [54]. The ion-beam can be used for site-specific material removal and the SEM for nondestructive imaging and analysis. FIB can be also used to prepare the cross-sectional Cu lines for transmission electron microscopy (TEM) analysis as shown in Figure 2.7. A JEOL 2010F TEM (200 kV) was used in this work for both failure analysis and Cu microstructure characterization (see Section 2.7).

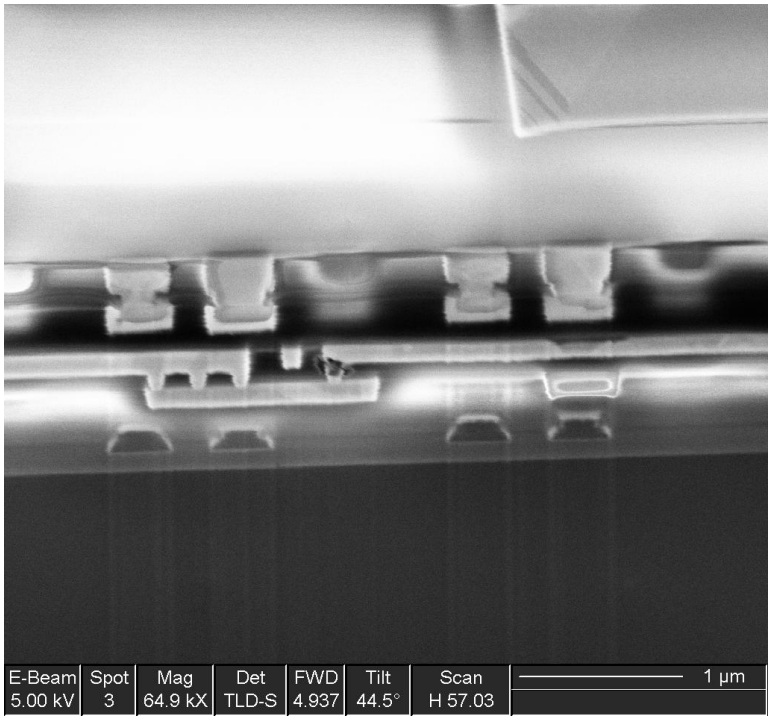


Figure 2.6 An example of FIB/SEM image showing void formation inside the via and in the trench away from the via for the upstream EM stressing.

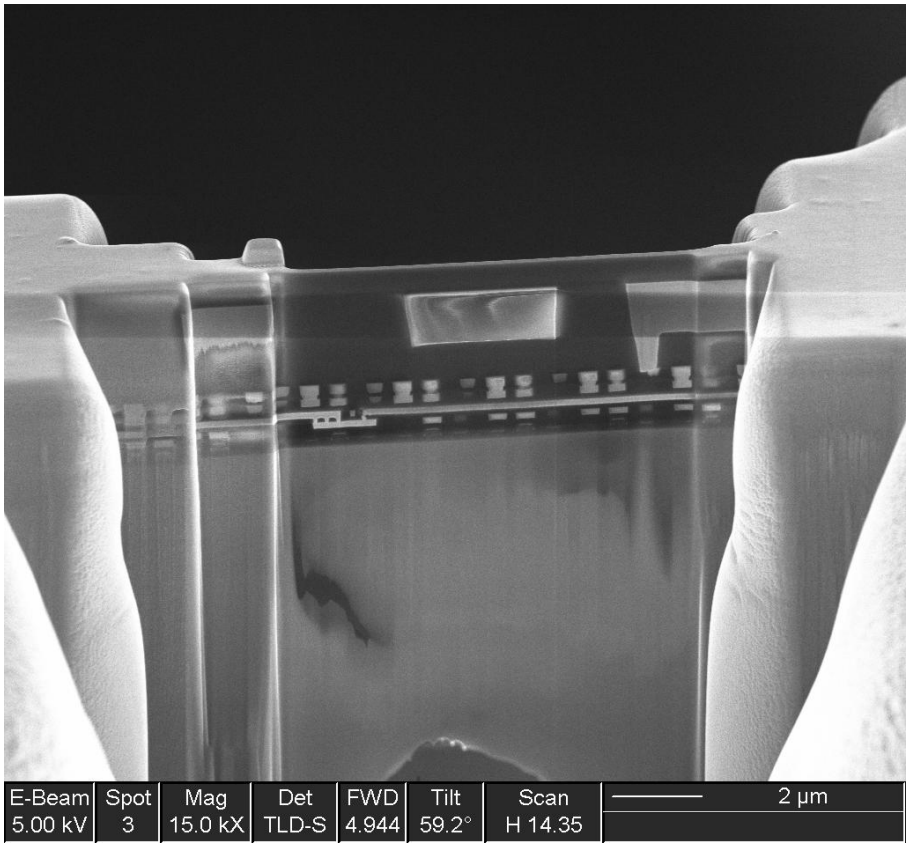


Figure 2.7 Illustration of the cross-section TEM sample preparation using FIB.

2.7 MICROSTRUCTURE CHARACTERIZATION TECHNIQUE

To study the microstructure effect on EM, detailed information on the grain structure with statistical significance and its contribution to mass transport is required. The SEM based electron backscatter diffraction (EBSD) is commonly employed as a characterization technique for automatic determination of individual grain orientations, local texture, and grain size distribution on surfaces of blanket Cu films and wide interconnect lines [55]. The SEM-EBSD technique is based on precise measurements of Kikuchi lines acquired point by point within the scanning area. The presence and quality

of these lines are strongly affected by the specimen surface conditions. Also, the lateral spatial resolution of EBSD at its best when used with a field emission gun (FEG) SEM is only ~25 nm for Cu. For the 45 nm technology node and beyond, Cu interconnects have been observed to possess a mixture of large grains and small grains with grain diameters significantly smaller than the line width, especially at the trench bottom. Therefore, EBSD is no longer suitable for comprehensive Cu microstructure analysis due to it spatial resolution limit.

Comparable techniques on transmission electron microscopy (TEM) appear to be an interesting alternative for microstructure analysis of small Cu grains. Different from Kikuchi bands used for orientation determination in EBSD technique, spot diffraction patterns work the best with TEM for the purpose of automated grain orientation analysis of nanocrystalline materials. However, for grains oriented off-axis with respect to the beam direction and regions with a high density of defects, the orientation analysis is affected and manual tuning may be required. So far, detailed information on grain structure has been rarely reported for Cu nanolines, primarily due to the limited spatial resolution and the difficulties in obtaining the statistical distribution of grain orientations for a large population of nanoscale grains in an automatic fashion.

To address these issues, a high-resolution automatic orientation mapping technique developed by Rauch *et al.* [56] was employed in this work to characterize the grain structure of Cu nanolines in detail. It is based on a TEM technique termed precession electron diffraction (PED) introduced by Vincent and Midgley in 1994 [57]. Prior to the interaction with specimen, the incident beam is tilted off the optic axis by a precession angle (0.4° in this work) and simultaneously rotated around the optic axis on the surface of a cone. The observed diffraction pattern is an integration of all the diffraction patterns within the precession cone and directly interpretable. Also, with the

use of beam precession many more reflections are visible in the spot patterns, which helps eliminate the indexing ambiguity for highly symmetric cubic crystals. As a result, PED is recognized as a promising technique for highly reliable diffraction pattern collection under quasi-kinematical conditions, even if the grain is not perfectly aligned with a particular zone axis.

This TEM-based PED technique was successfully applied to the area of automatic grain orientation mapping and implemented by a commercial precession system called DigiSTAR^{TM} from NanoMEGAS Inc. This system is interfaced with JEOL 2010F TEM at UT Austin and can provide information at a spatial resolution of 1-2 nm on grain orientation distributions (crystallographic texture), grain size distributions and grain boundary characteristics. A series of beam alignments are carefully performed before acquisition to ensure a high quality of diffraction patterns. Spot patterns are collected with an external charge-coupled device (CCD) camera while the specimen area of interest is scanned by the precessed electron beam. The acquired spot patterns are then indexed in an automated manner using a template matching algorithm, which compares the recorded patterns with pre-calculated templates for all possible orientations. With beam precession properly set up, pattern identification through template matching can be significantly improved.

The PED-assisted orientation mapping technique allows the determination of the complete three-dimensional orientation of individual grains, which can be projected onto three orthogonal directions to form the orientation pole plots. The quantitative texture plots [55] obtained using the EDAX-TSL OIM^{TM} Data Analysis software are expressed as “multiples of random distribution” (MRD) [55] such that an MRD value of 1 represents a completely random distribution of grain orientations. The orientation maps

are used to yield grain size and grain boundary statistics. The microstructure information of Cu interconnects down to 40 nm will be presented in Chapter 4.

Chapter 3: Effects of Mn Alloying and Metal Capping on Electromigration Reliability of Cu Interconnects

3.1 INTRODUCTION

Scaling can significantly degrade the electromigration (EM) lifetime for Cu interconnects, raising serious reliability concern for advanced chips of future technology nodes. A scaling rule has been proposed based on the growth rate to reach the critical-size void as $\tau = \Delta L_{cr}/v_d$ where τ is the EM lifetime, ΔL_{cr} the critical void length and v_d the drift velocity. Assuming constant current density and interfacial diffusivity, τ will degrade by half for each new generation [58]. At the 65 nm node and beyond, τ was found to further degrade due to the emergence of small grains which contributed to the mass transport via grain boundary (GB) diffusion. These studies have generated great interest in the development of metallizations to improve EM reliability by suppressing interface diffusion, notably using CoWP metal cap [8] and Mn alloying [11]. Mn alloying was particularly effective in sustaining a small statistical deviation σ although the improvement of EM lifetime was less than the CoWP cap. During subsequent annealing, Mn from an alloy seed layer was found to segregate at grain boundaries and Cu/cap layer interfaces, reducing Cu diffusion at active diffusion paths. It is not clear, however, how effective Mn alloying would be as scaling continues. With the interface diffusion suppressed by Mn addition, the effect of grain structure on the overall EM mass transport becomes important. The scaling effect of Mn alloying on EM reliability and the microstructure evolution of ultrafine Cu lines has to be better understood in order to implement this process for the future technology.

In this chapter, EM reliability of Cu interconnects with Mn doping were studied by measuring the effects of line width and length on void formation kinetics, EM lifetime and statistics up to the 28 nm node. Both upstream and downstream EM tests were

performed. Failure modes and mass transport mechanisms responsible for EM degradation were examined using the resistance traces recorded during EM testing. The effect of Mn alloying on EM reliability was further investigated by comparing the lifetime statistics to Cu interconnects with standard SiCN and CoWP caps.

3.2 EXPERIMENTAL DETAILS

The EM test structures for this study are single-linked, three-level structures with M2 as the EM stressing line (Figure 3.1). The M1 and M3 feeder lines were made wider in order to minimize the EM failure probability in the feeder lines. Under this configuration both downstream (referred as V2M2) and upstream (V1M2) EM tests could be performed. The pure Cu lines and Cu lines with minor Mn doping in the seed layer (Table 3.1) were fabricated by GLOBALFOUNDRIES Inc. using a standard damascene process. For the pure Cu structure of the 45 nm node, the M2 line is 70 nm wide, 144 nm thick and 200 μm long. They are capped with either standard SiCN dielectric or with an additional layer of CoWP in between Cu and SiCN. The grain structure of Cu lines was adjusted to study the microstructure effect on the EM reliability using both small grain (SG) and large grain (LG) structures. EM tests were conducted with down-flow electron current along M3-V2-M2 direction with current density of 10-20 $mA/\mu m^2$ at temperatures ranging from 260 ºC to 380 ºC.

For the Cu(Mn) seed-layered structure, the M2 baseline structure (W_{min}) is 45 nm wide, 115 nm thick and 180 μm long, capped with the standard SiCN layer. In addition, 45 nm lines with line lengths ranging from 4.5 to 180 μm were studied for the short length effect. Wide lines with line width of 0.162 μm ($3.5W_{min}$) were also tested to investigate the width effect and compare with baseline structure. Via diameters were 45

nm for both baseline and wide line structures. EM stressing was performed with nominal current densities of 5-64 mA/μm^2 at temperatures ranging from 275 to 325 ºC. Both electron current flow passing downward along M3-V2-M2 direction (V2M2) and upward along M1-V1-M2 (V1M2) were studied. A resistance increase of 10% was used as the failure criterion in this study.

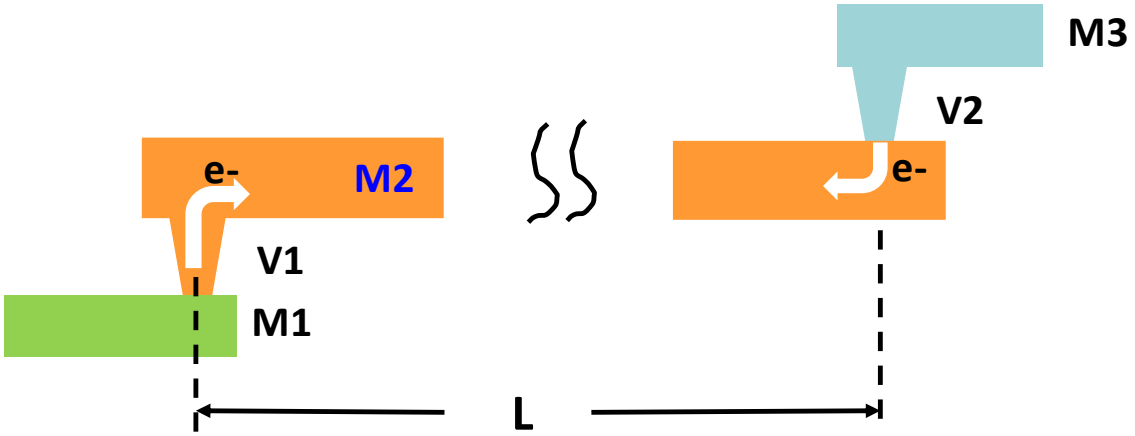


Figure 3.1 Schematic of 3-level EM test structure (M2 as the EM stressing line) illustrating both downstream (V2M2) and upstream (V1M2) configurations.

Table 3.1 Summary of the details of EM test chips for both 45 nm and 28 nm nodes.

	45 nm node		28 nm node
Alloying	**Pure Cu**		**Cu(Mn)**
Grain structure/ Geometry variation	**LG or SG**		**W_{min} or 3.5 W_{min}**
Capping	**SiCN**	**CoWP**	**SiCN**

3.3 Effects of Mn Alloying on EM Reliability

3.3.1 EM Behaviors of Cu(Mn) Baseline Structures (W_{min})

The EM lifetime distributions of the baseline structure tested at 325 °C and 5mA/μm^2 for upstream (V1M2) and downstream (V2M2) electron flows are shown in Figure 3.2. The median EM lifetime of baseline samples stressed under downstream (V2M2) condition is about 2 times longer compared with those stressed under upstream (V1M2), while the sigma value is higher for V2M2 (0.41) than for V1M2 (0.3).

The behavior of EM degradation was examined using the resistance traces and analyzed to investigate the EM failure mechanism. An examination of the resistance degradation revealed two distinct failure modes for the downstream V2M2 test (Figure 3.3). The Mode I failure is represented by an abrupt resistance jump while the Mode II failure shows a small initial resistance increase followed by a gradual resistance increase. In a previous study [35], such failure modes were found to be closely related to EM-induced void morphology. Mode I failure is typically associated with voids formed underneath the via and to extend along the interface to induce open failure, as evidenced by a resistance pop-up. In contrast, Mode II failure arises from voiding in the M2 trench line away from the via. When the void grows to span the whole line thickness, the barrier layer serves as a current shunting path resulting in a step-like resistance increase. Further void growth along the current flow direction induces resistance increase with a constant slope which is related to the Cu drift velocity. In this way, the Mode II failure has a longer EM lifetime compared with Mode I. The population of Mode II failures in V2M2 test is considerably larger as compared to V1M2 test, resulting in a longer EM lifetime. In general, the mixture of Mode I and II in V2M2 test leads to a larger lifetime deviation as observed in Figure 3.2 while V1M2 mostly fails by Mode I.

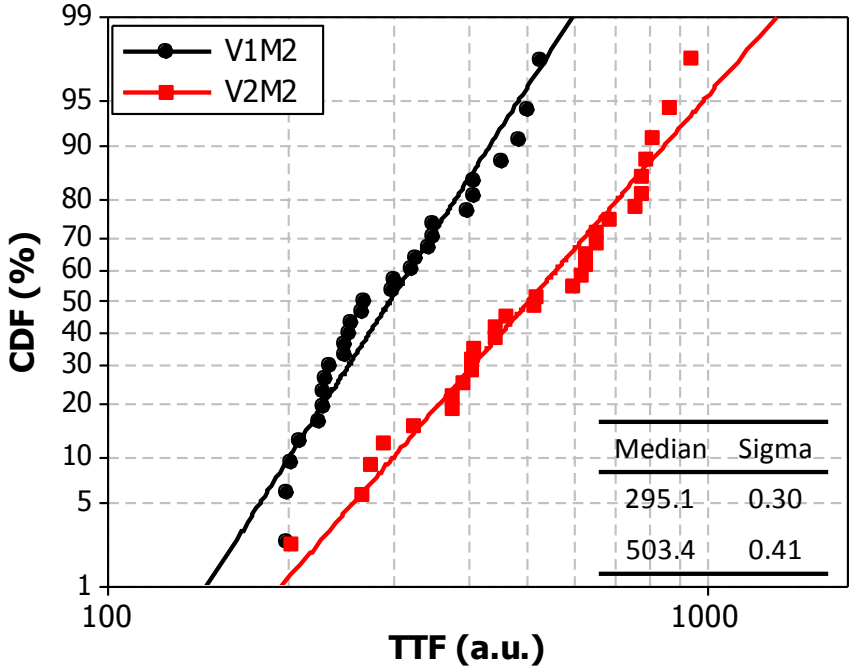
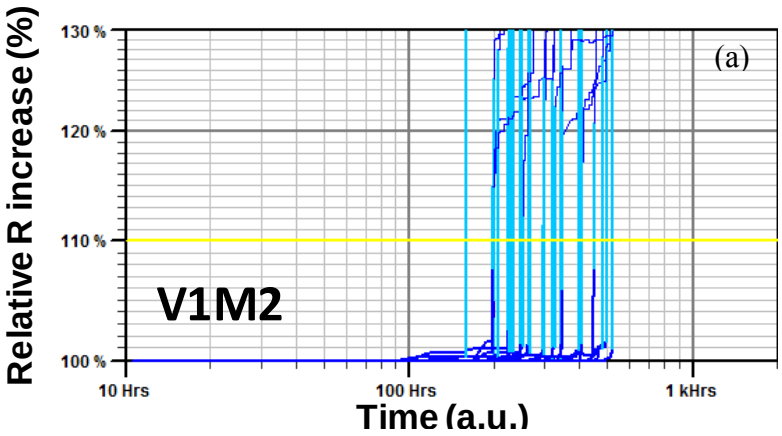


Figure 3.2 EM lifetime distributions of baseline structures stressed under downstream (**V2M2**) and upstream (**V1M2**) electron flow directions. Median EM lifetime and sigma are summarized in the inset.



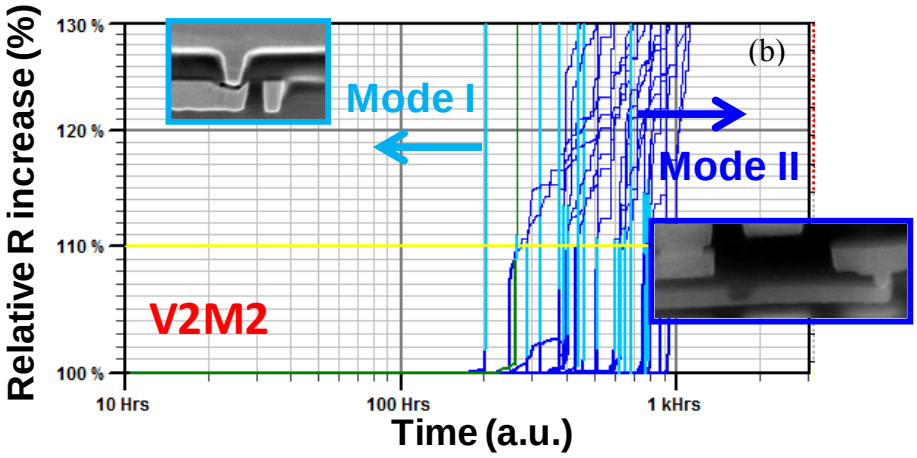
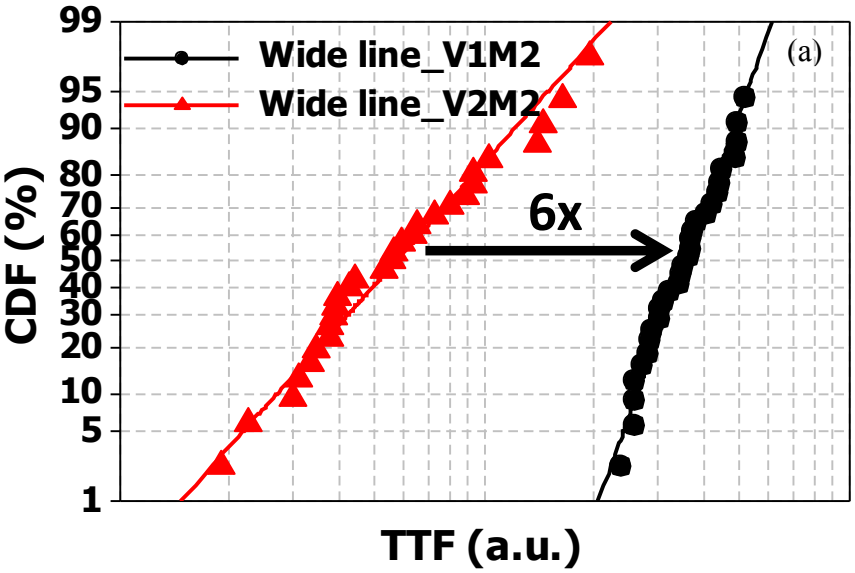
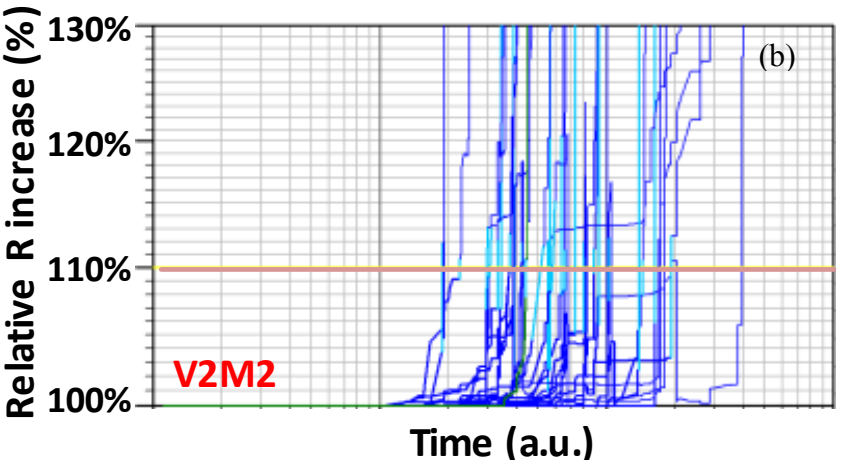


Figure 3.3 Resistance traces of baseline samples for V1M2 (a) and V2M2 (b). Two failure modes (Mode I and Mode II) are illustrated together with their representative void morphology.

3.3.2 EM Behavior of Cu(Mn) Wide Lines ($3.5W_{min}$)

The wide line structure, about 3.5 times wider than the baseline structure, was studied to investigate the width effect. Different from the baseline structures, the V1M2 wide lines showed a 6x lifetime improvement over the V2M2 lines (Figure 3.4a). The lifetime statistics for V1M2 was also improved with a sigma value as small as 0.24. These results suggest that Mn is more effective for improving the EM lifetime and statistics for V1M2 lines, where voids formed closely to the via. This is reflected in the characteristics of the resistance traces. As shown in Figures 3.4b and 3.4c, V1M2 tests showed mostly Mode II failures, leading to a longer EM lifetime and a tighter lifetime distribution as compared with V2M2. Only few pop-up failures were observed in V1M2 tests, indicating the improved liner quality in the via for wide lines.


99
95
90
80
70
60
50
40
30
20
10
5
1
CDF (%)
Wide line_V1M2
Wide line_V2M2
6x
(a)
TTF (a.u.)


130%
120%
110%
100%
Relative R increase (%)
V2M2
(b)
Time (a.u.)

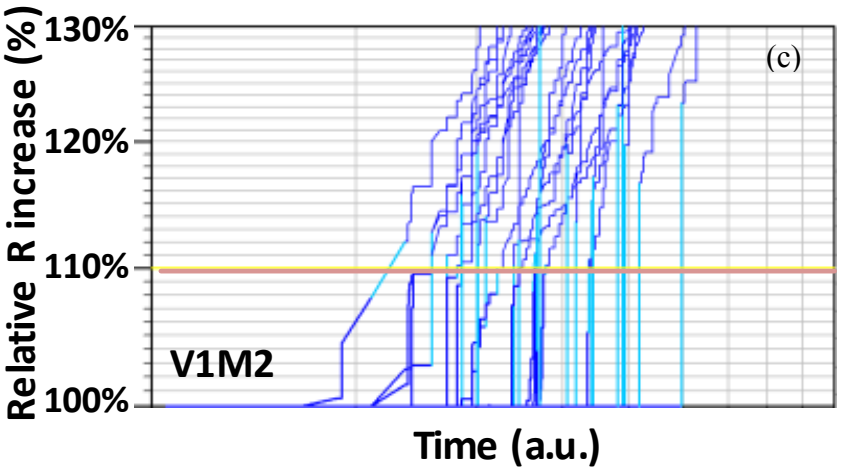

130%
120%
110%
100%
Relative R increase (%)
V1M2
(c)
Time (a.u.)

Figure 3.4 (a) EM lifetime distributions of wide lines stressed under V1M2 and V2M2 and their resistance traces for (b) V2M2 and (c) V1M2, respectively.

The EM lifetime of narrow lines and wide lines stressed at 325°C, 21 mA/μm^2 are summarized in Figure 3.5. For upstream V1M2 tests, wide lines showed a 9x lifetime improvement over narrow lines. The large improvement was consistent with their resistance traces. The number of Mode II failures increased from 3 for the narrow lines (sample size: 29) to 26 for the wide lines (sample size: 30). The rate of resistance increase R_{slope} from V1M2 tests was evaluated to compare the EM drift velocity v_d and effective diffusivity D_{eff} for wide and narrow lines (Figure 3.6). D_{eff} for narrow lines at 325 °C was found to be about 5x larger than that of wide lines. This large EM lifetime improvement for wide lines in V1M2 is accompanied by a reduction in sigma to 0.24. In comparison, the lifetime improvement in V2M2 for wide lines is limited and is traded off by an increase in sigma to about 0.6. These results indicate Mn works better for wide lines for upstream stressing. Vias are more prone to process defects (*e.g.* poor liner coverage or preexisting voids) and they are closely related to early EM failures in the upstream electron flow configuration. Narrow lines are more likely to have local defects in via regions and they have more small grains. Thus the role of Mn in suppressing diffusion at the top interface is considerably reduced. As the lines become wider, vias become more robust and the grain structure is more bamboo-type. Mn alloying elements tend to segregate to the top Cu surface to suppress interfacial diffusion rather than accumulate at grain boundaries and defective spots. As a result, the effectiveness of Mn doping to improve EM reliability for V1M2 is enhanced for wide lines. For V2M2, EM failures occur either underneath the via or away from the via in the trench, which are less

sensitive to via defects. Therefore, the difference in EM lifetime between narrow and wide lines is not significant (Figure 3.5b).

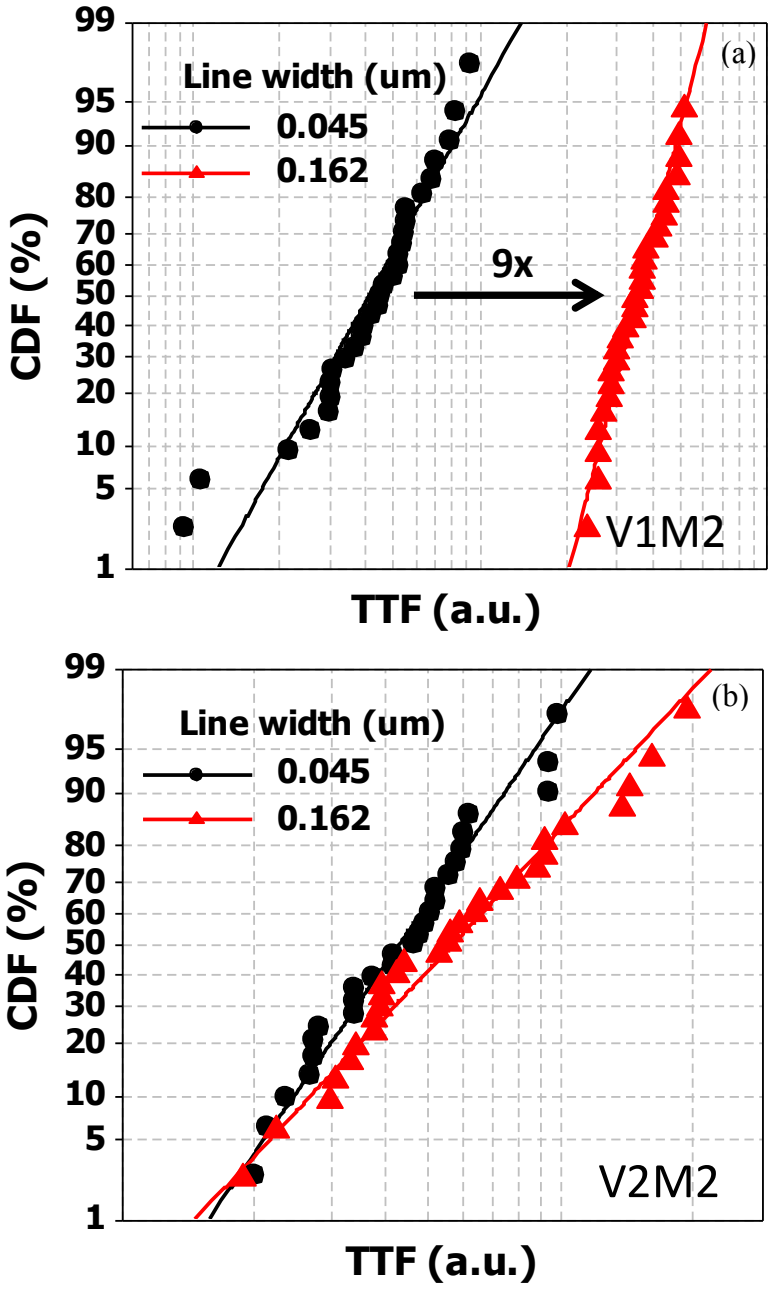


Figure 3.5 Comparison of EM lifetime distributions between narrow lines ● and wide lines ▲ stressed at 325 °C and 21 mA/μm^2: (a) V1M2, (b) V2M2.

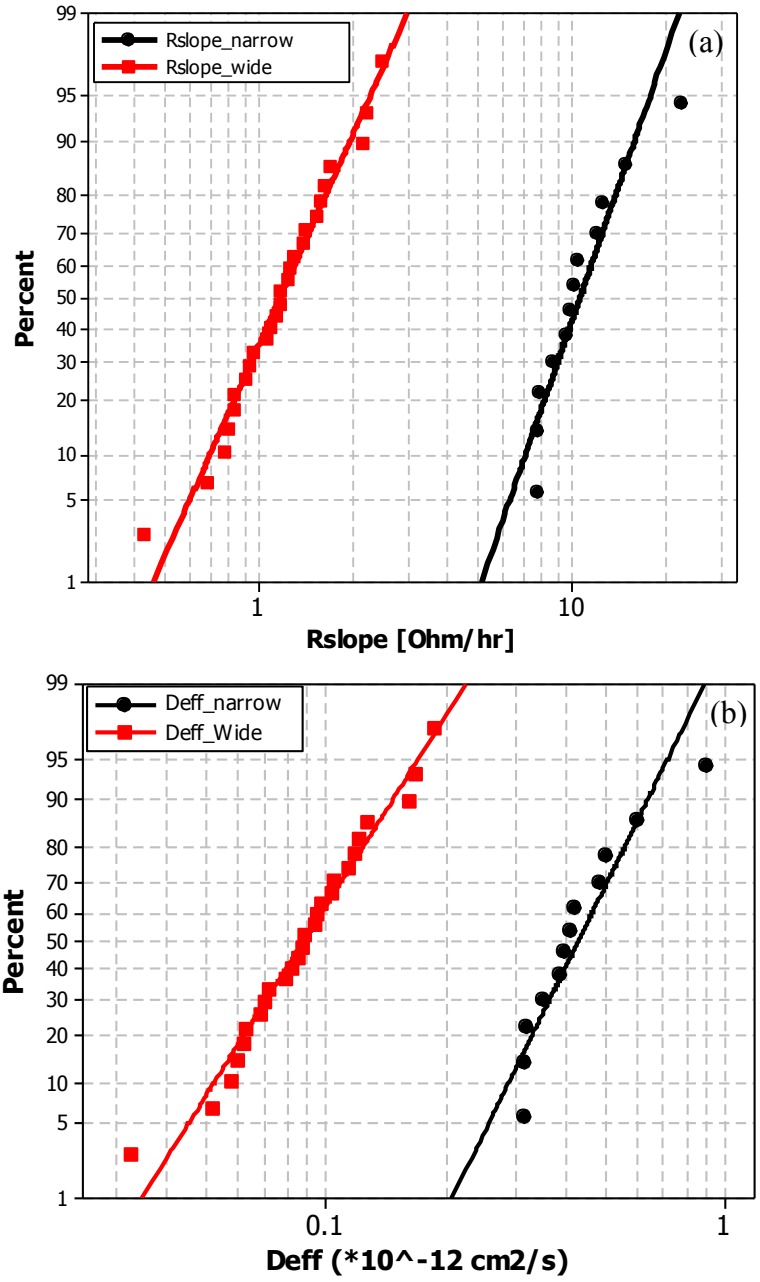


Figure 3.6 Statistical distributions of R_{slope} (a) and D_{eff} (b) for narrow lines and wide lines extracted from EM testing at 325 °C, 21 mA/μm^2.

3.3.3 EM Intrinsic Parameters: Current Density Exponent and Activation Energy

To study the effect of Mn doping on mass transport, the activation energy of baseline structures was measured by performing EM tests at 3 different temperatures (275, 300 and 325 ^{o}C) with a constant current density of 21 mA/μm^2 (Figure 3.7). Based on Black's equation, the activation energies were found to be 1.10±0.02 eV and 1.07±0.07 eV for V1M2 and V2M2 electron flow, respectively, which are higher than 0.8-0.9 eV typically for Cu interconnects with SiCN cap. The higher values suggest that Mn is bonded to both Cu/cap layer interface and Cu grain boundary to reduce mass transport.

To study voiding kinetics for Mn-doped Cu interconnects, EM tests at 3 different current densities (5, 11 and 21 mA/μm^2) and a constant temperature (325 ^{o}C) were performed to extract current density exponent *n* in Black's equation. The current density exponent *n* was found to be 1.43±0.13 and 1.80±0.10 for V1M2 and V2M2, respectively (Figure 3.8). These values are in the range of 1-2, indicating both void-nucleation and void-growth processes contribute to EM failures [59]. The *MTTF* value can be expressed as the sum of void nucleation time t_n and void growth time t_{growth}:

$$t_{50} = t_n + t_{growth} = \left(\frac{AkT}{j} + \frac{B(T)}{j^2}\right)\exp\left(\frac{E_a}{kT}\right) \tag{3.1}$$

where A is a constant and B(T) is temperature dependent. All other parameters have the same meanings as described in Chapter 2. Upon examination, Mode I failure was found to associate with via where a small critical void size is sufficient to fail the line. Thus this type of failure is mostly nucleation-limited (n = 2). In contrast, for Mode II a fully grown void was required in order to reach a critical void size to fail the line, and thus it is growth-limited (n =1).

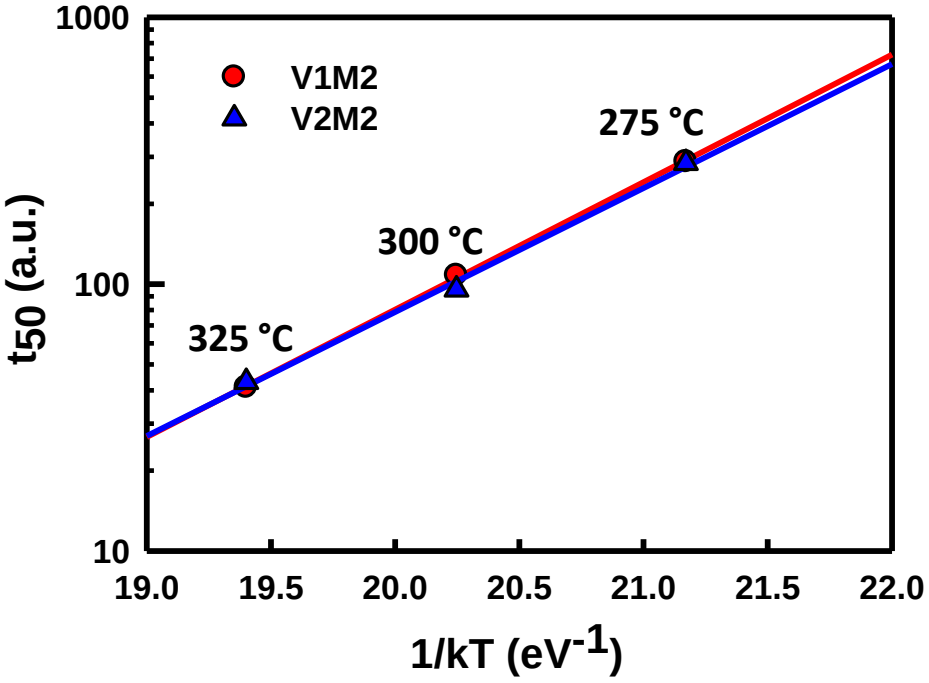


Figure 3.7 Median EM lifetime as a function of temperature for upstream (V1M2) and downstream (V2M2) stressing.

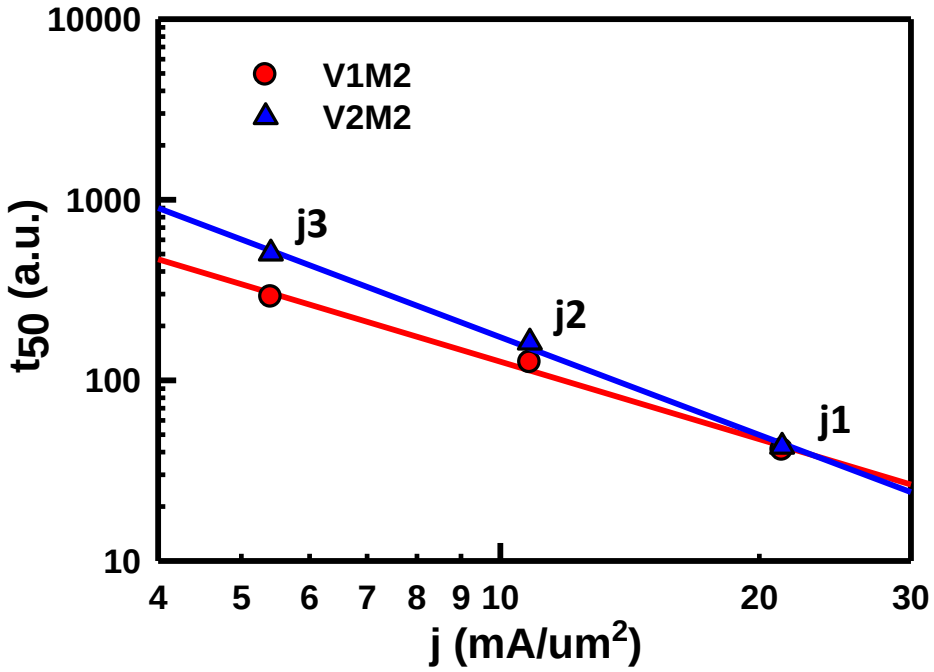


Figure 3.8 Median EM lifetime as a function of current density for upstream (V1M2) and downstream (V2M2) stressing.

3.3.4 Short Length Effect

An important factor in EM reliability is the critical current density j_c, below which no EM failure occurs. The critical Blech product $(jL)_c$ was measured for 45 nm wide Mn-doped Cu interconnects with line lengths of 4.5, 15, 22.5, and 180 µm. The tests were performed at 325°C with current densities ranging from 5 to 64 mA/µm^2 for both upstream (V1M2) and downstream (V2M2) electron flows (Table 3.2). The $(jL)_c$ was determined from the linear fit to the L/t_{50} vs. (jL) plot (Figure 3.9) and found to be 290 mA/µm for V1M2 stressing and 432 mA/µm for V2M2 stressing, which are similar to $(jL)_c$ reported for pure Cu and Cu with Mn doping [60]. This suggests that the difference in the critical Blech product for V1M2 and V2M2 is due to the different failure modes.

As discussed earlier (Figure 3.3), V2M2 is mostly comprised of Mode II failures (trench void) while V1M2 is dominated by Mode I failures. This is consistent with the study of Oates *et al*. [61]. They observed that the $(jL)_c$ associated with slit void is smaller than with the trench void. The downstream EM failure is more affected by the stress gradient in the trench, where the shorter the line, the larger the back stress gradient $\Delta\sigma/L$. In comparison, the upstream EM degradation seems to be less affected by the trench stress gradient since most of the void formation is confined within the via. This yields a smaller $(jL)_c$ for V1M2 and explains why the 4.5 μm-long line failed faster under upstream V1M2 stressing than downstream V2M2 stressing.

Table 3.2 EM testing matrix and results for V1M2 and V2M2 to determine the critical Blech product $(jL)_c$ at 325 ^{o}C.

325 ^{0}C				
			TTF (a.u.)	
L (um)	*j* (mA/um^2)	*jL* (mA/um)	V1M2	V2M2
180	21	3780	41	43
180	11	1944	125	162
180	5	900	295	503
22.5	35	788	26	23
15	27	405	174	170
4.5	64	288	464	x
4.5	32	144	1272	x

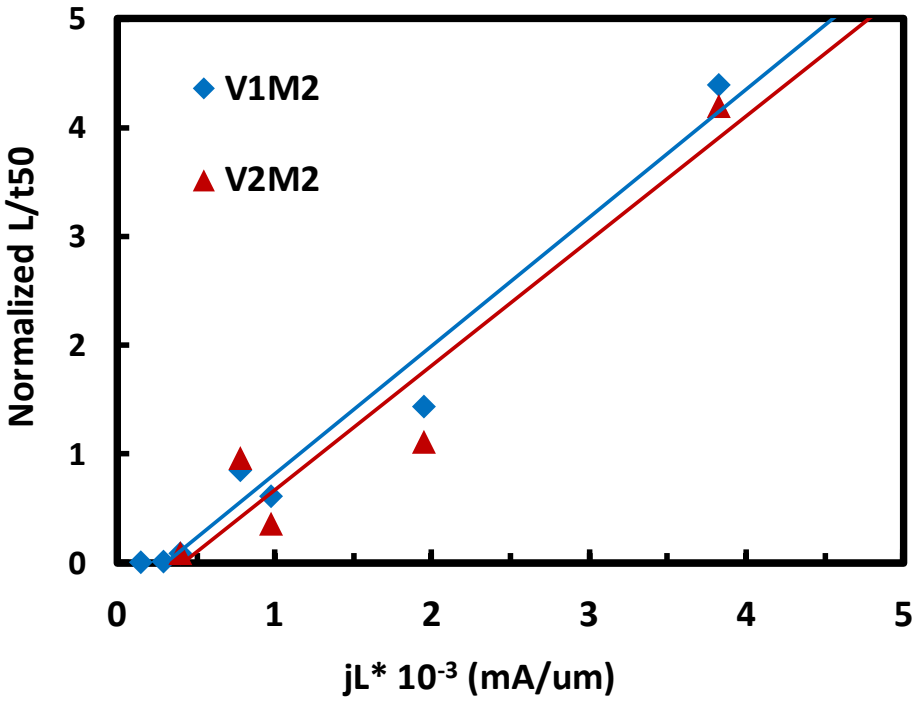


Figure 3.9 L/t_{50} vs. (jL) plot with linear fitting to extract the critical Blech product $(jL)_c$ for V1M2 and V2M2 stressing.

EM failure distributions of Cu(Mn) lines stressed at the same temperature and current density for V1M2 electron flow as a function of line length are plotted in Figure 3.10 to illustrate the short length effect. As the line length was reduced from 180 to 22.5 μm, the overall lifetime distributions stayed about the same. Since jL products for both lines were well above $(jL)_c$, the short length effect were not significant. With the line length reduced to 4.5 μm at $jL = 0.5(jL)_c$, a large lifetime improvement up to 48x was observed together with a small deviation in the lifetime distribution (σ = 0.4). This indicates that Mn is effective in repairing process defects in the via for upstream V1M2 testing, making the lifetime less sensitive to process variations. Both improvements of EM lifetime and lifetime variation would be particularly beneficial when extrapolating the EM lifetime to the operating condition for a large ensemble of interconnects.

Interestingly, no immortal behavior with a large broadening of EM failure distribution was found for Cu lines as short as 4.5 μm. Nevertheless, a resistance saturation phenomenon was observed in the resistance traces, exhibiting the presence of back stress to suppress the Cu atomic flux (Figure 3.11a). The magnitude of the back stress was not large to start with, as it became effective only after EM-induced voids were fully grown. This saturation behavior was not observed in the 22.5 and 180 μm lines stressed at the same current density (Figure 3.11b and c).

The sub-critical EM failure associated with 4.5 μm Cu(Mn) lines for V1M2 stressing could be attributed to the critical stress σ_c required to nucleate a void at a blocking boundary (*e.g.* the cathode end of the line). In Korhonen's model [33], stress evolution at the blocking boundary prior to voiding can be expressed as:

$$\sigma(t) = \sqrt{\frac{4t}{\pi}\frac{\Omega D}{kT}}\frac{eZ^*\rho j}{\Omega} \times \sqrt{B} \tag{3.2}$$

where B is the effective bulk modulus and t is the time required to build up the stress. All other parameters have the same meanings as explained in Chapter 1. B can be approximately expressed as

$$B = G_{ILD} + G_b\frac{t_b}{w} \tag{3.3}$$

where G_{ILD} and G_b are shear moduli of the surrounding dielectrics and trench barrier layers, respectively, t_b is the barrier thickness and w is the trench width. Based on Equations (3.2) and (3.3), the effects of barrier thickness on $(jL)_c$ can be deduced as shown in Figure 3.12. Both $(jL)_c$ and B decrease with decreasing barrier thickness

because of less confinement of the interconnect structures. For the 28 nm node Cu(Mn) structures with V1M2 stressing, $(jL)_c$ decreased more than expected based on the effective modulus B. It is likely that the reduced $(jL)_c$ is related to the permeability of the barrier to Cu in the via region during V1M2 stressing, which would lead to a reduction in the stress gradient associated with the EM flux. Ultra-thin barrier layers required for RC reduction only contain a few atomic layers (in this study, t_b < 30Å on the trench sidewall) and may be leaky because of defects. As a result, lines may fail sub-critically especially under V1M2 stressing which is more sensitive to liner defects around the via.

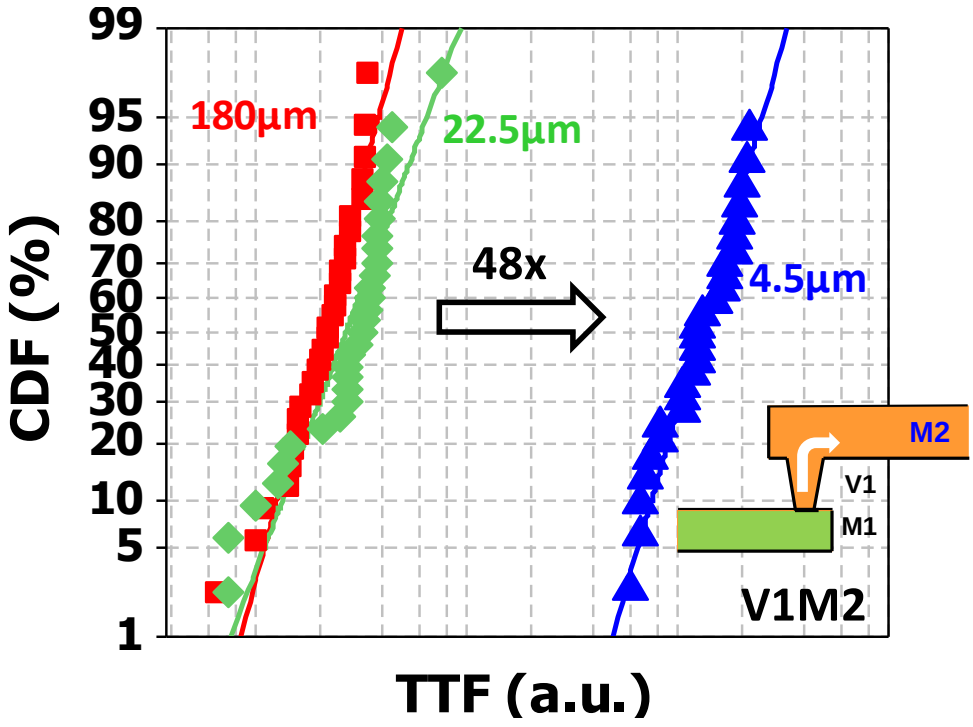


Figure 3.10 V1M2 EM behaviors for different line lengths at 325 °C and the same current density.

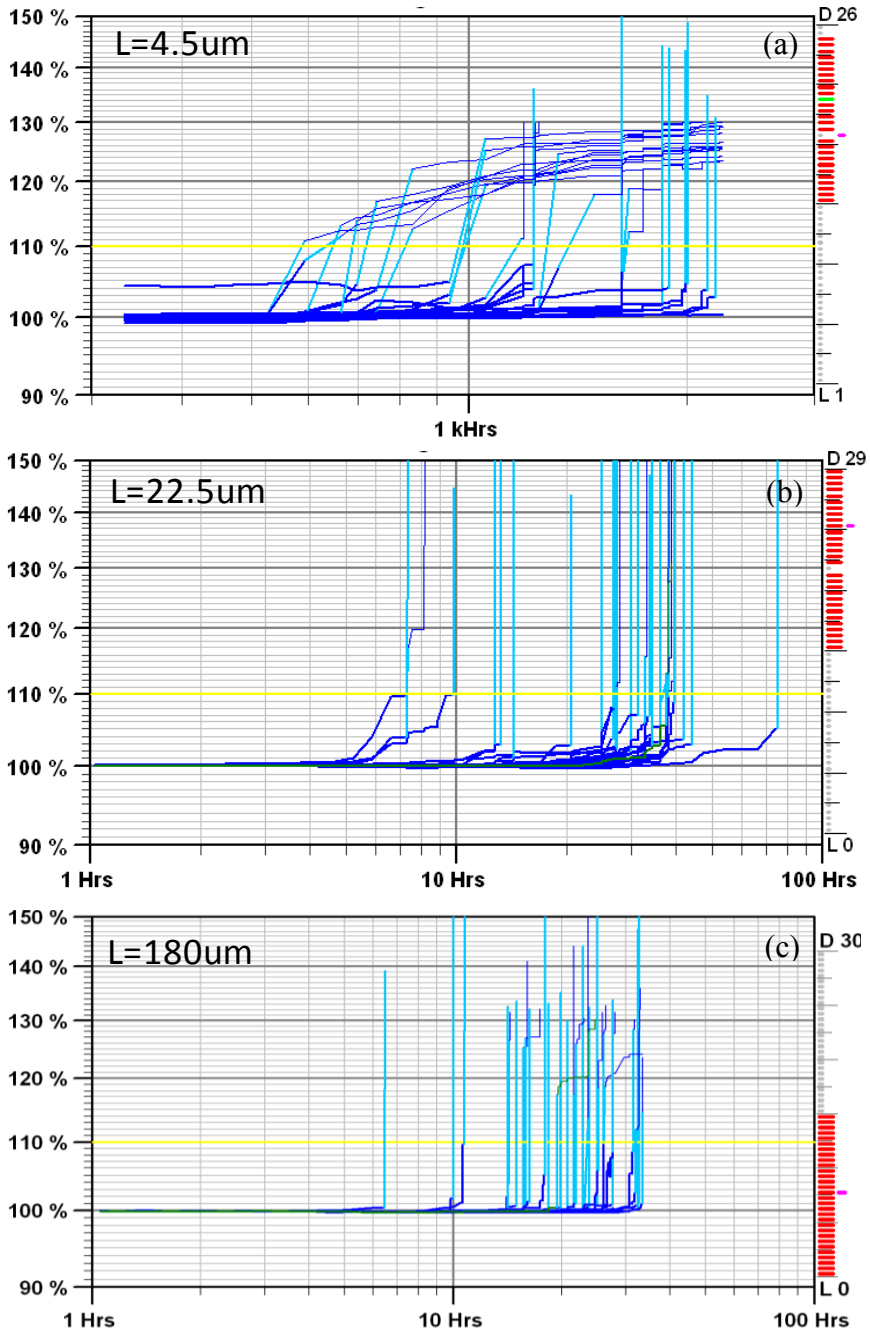


Figure 3.11 Resistance traces of Cu(Mn) interconnects (Wmin) with different line lengths: (a) L = 4.5 µm (showing resistance saturation), (b) L = 22.5 µm, (c) L = 180 µm.

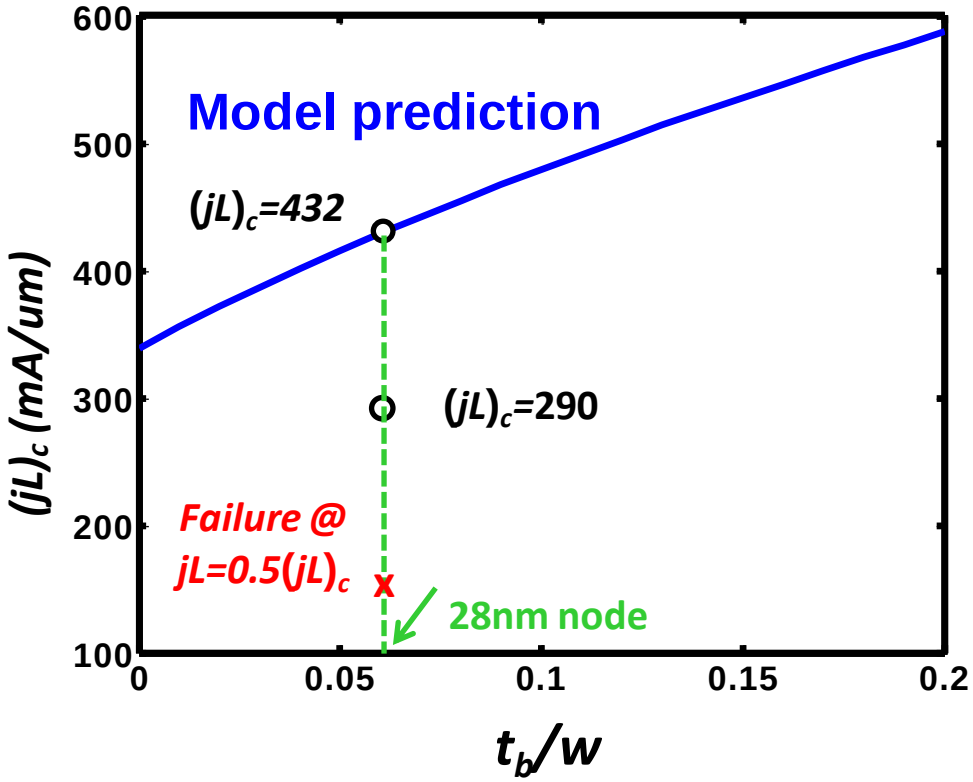


Figure 3.12 The effect of barrier thickness on the critical Blech product $(jL)_c$ predicted by Korhonen's model [33]. Circles represent experimental data in this study for the 28 nm node Cu(Mn) lines.

In summary, EM reliability of Mn-doped Cu interconnects for the 28 nm node was investigated. Mn was found to improve the EM performance by reducing both interfacial and grain boundary diffusion and repairing local process defects. Although immortality was not observed, EM lifetime of short lines was significantly improved together with a reduction in lifetime deviation. This is attributed to the effectiveness of Mn in repairing process defects, particularly for via-related void formation in V1M2 electron flow direction.

3.4 Effects of Metal Capping and Grain Structure on EM Reliability

3.4.1 SiCN vs. CoWP and LG vs. SG

The downstream (V2M2) EM lifetime statistics of 45 nm node pure Cu interconnects tested at 330 ºC and 10 mA/μm^2 are shown in Figure 3.13. Compared with the standard SiCN cap, Cu interconnects with CoWP metal cap were found to greatly improve EM lifetime by 24x or 156x, depending on the grain structure. With the CoWP cap, EM lifetime for SG and LG structures differed by 12x. It is important to note that the lifetime improvement was accompanied by an increase in the statistical deviation σ from 0.25-0.29 for SiCN to 0.50-0.73 for CoWP. The increase in σ would greatly reduce the usefulness of the CoWP cap when extrapolating the EM lifetime to the operating condition. Since the role of CoWP is very sensitive to Cu grain structure, it is important to control Cu grain size to maximize the effectiveness of CoWP.

To analyze the effects of metal capping and grain structure on EM reliability of Cu interconnects, R_{slope} and R_{step} were extracted from resistance traces recorded during EM testing for both SiCN and CoWP caps with SG or LG structure (Figure 3.14). R_{slope} was found to vary greatly with interfacial capping materials and Cu grain structure, with SiCN/SG group being the largest and CoWP/LG the smallest. As discussed earlier, R_{slope} is known to reflect the EM-induced mass transport process. Based on R_{slope}, the effective diffusivity D_{eff} at 330 ºC was determined as shown in Figure 3.15. LG with CoWP metal capping has the lowest D_{eff} of $2\text{x}10^{-14}$ cm^2/s, which is more than 2 orders of magnitude lower compared to LG with standard SiCN dielectric capping ($2.86\text{x}10^{-12}$ cm^2/s). This demonstrates the effectiveness of CoWP in slowing down the Cu interface diffusion. The role of CoWP is weakened when the Cu grain structure reduces from LG to SG. This indicates that grain boundary diffusion becomes more significant once the top interface diffusion is suppressed by CoWP. The R_{step} values are less different among 4 groups as

compared to R_{slope}. In general, they are similar although that for CoWP/LG, R_{step} is about 2x smaller. As discussed in Chapter 2, R_{step} is proportional to the critical void size, so CoWP/LG has the smallest overall diffusivity. Once the void is nucleated at the interface it tends to stay and grow downward till reaching the trench bottom. Since the extent of CoWP to improve EM performance is strongly affected by Cu microstructure, it is important to investigate Cu grain structure and to understand how CoWP could be implemented for the future technology node. These will be covered in Chapter 5.

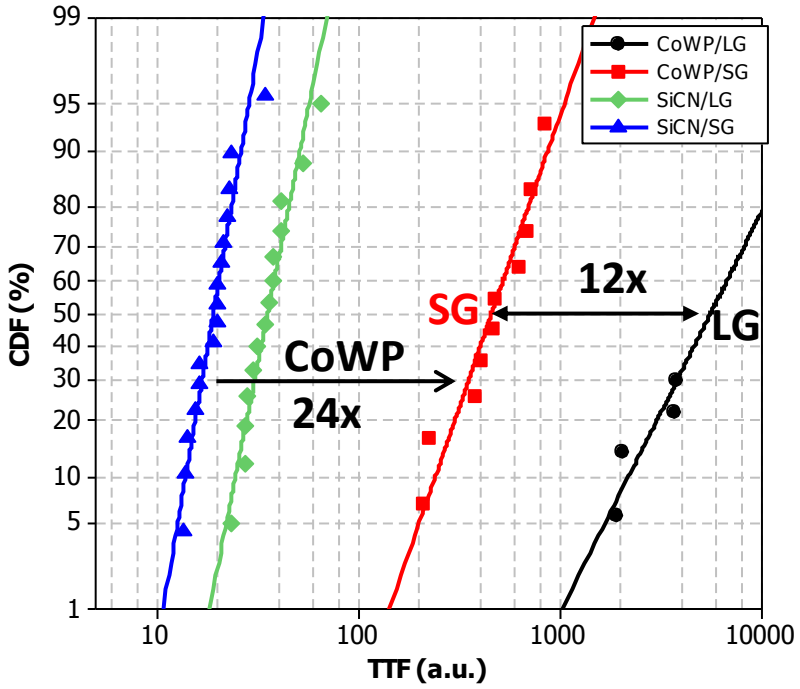


Figure 3.13 Statistical distributions of EM lifetime for 45 nm node Cu interconnects with 2 different capping materials (SiCN or CoWP) and 2 different grain structures (SG or LG).

Table 3.3 Summary of statistics of EM failure distributions in Figure 3.9.

	Median	Sigma
SiCN/SG	19.1	0.25
SiCN/LG	35.6	0.29
CoWP/SG	458	0.50
CoWP/LG	5570	0.73

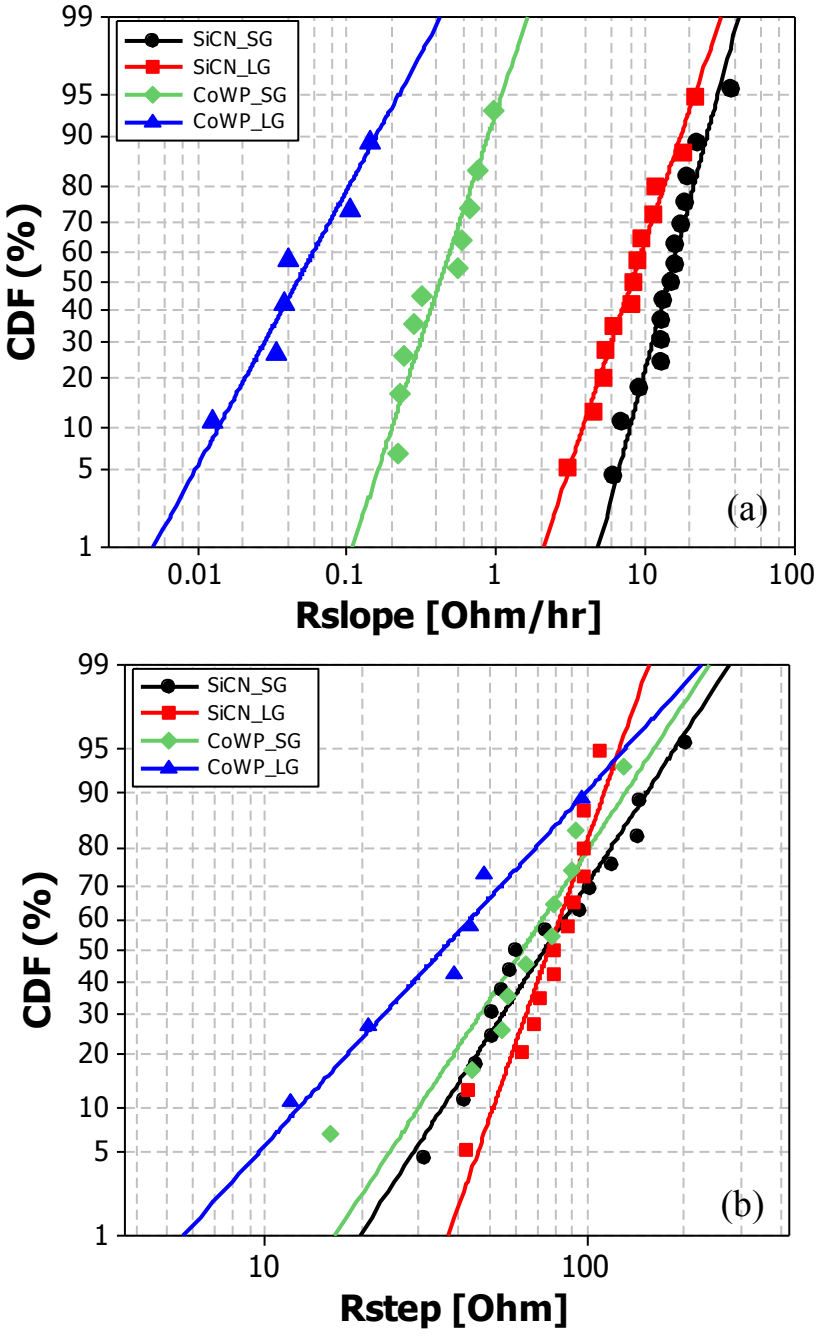


Figure 3.14 Statistical distributions of R_{slope} (a) and R_{step} (b) extracted from resistance traces during EM testing for 45nm node Cu interconnects with different capping layers and grain structures.

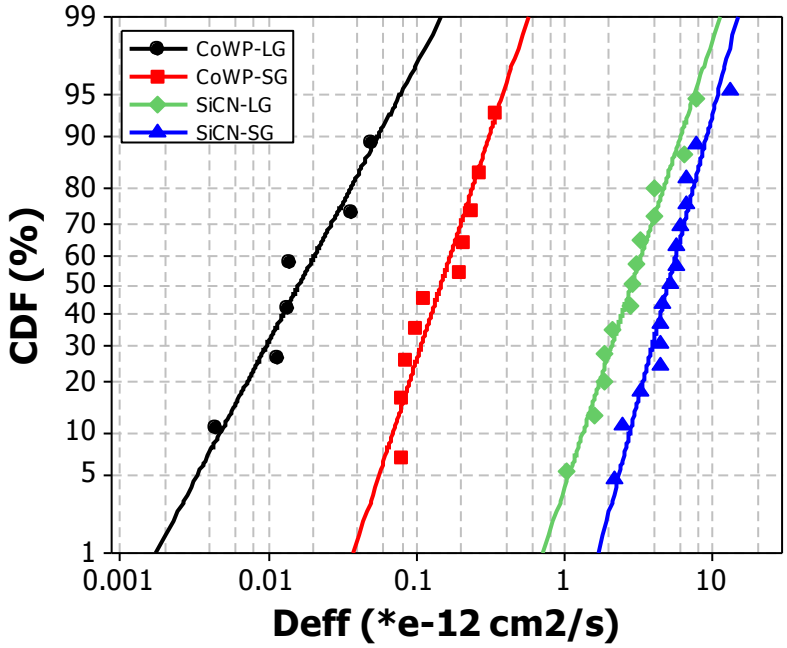


Figure 3.15 Statistical distributions of D_{eff} (at 330 ºC) calculated from R_{slope} for 45nm node Cu interconnects with different capping layers and grain structures.

3.4.2 Comparison of Mn Alloying vs. CoWP

EM failure distributions of Mn-alloyed Cu interconnects for the 28 nm node stressed at 330 ºC and 10 mA/μm^2 are plotted together with pure Cu interconnects for the 45 nm node to compare the effect of Mn doping vs CoWP metal capping for EM imporvement. As shown in Figure 3.16, the Mn-doped Cu interconnects for the 28 nm node achieved an EM lifetime improvement of ~8x comparing to pure Cu interconnects with SiCN cap for the 45 nm node. Even though the improvement is less as compared with CoWP (24x), a better sigma (0.37) was obtained with Cu(Mn). This is important for the extrapolation of EM time to failure to a very low percentile (*e.g.* 1 ppm). The result is consistent with that reported by Christiansen *et al.* who found that the spread in the failure distributions was much smaller for CuMn (0.3-0.5) than CoWP (0.6-0.9). An

analysis of resistance traces revealed that Mn doping effectively suppressed EM mass transport, reducing the effective diffusivity by about one order of magnitude as compared with pure Cu interconnects with SiCN cap (Figure 3.17).

It is not clear, however, how effective Mn alloying would be as scaling continues. With the interface diffusion suppressed by Mn addition, the effect of grain structure on the overall EM mass transport would be expected to be as important as observed for the case of CoWP capping. The scaling effect of Mn alloying on EM reliability and the microstructure evolution of ultrafine Cu lines has to be better understood in order to implement this process for the future technology.

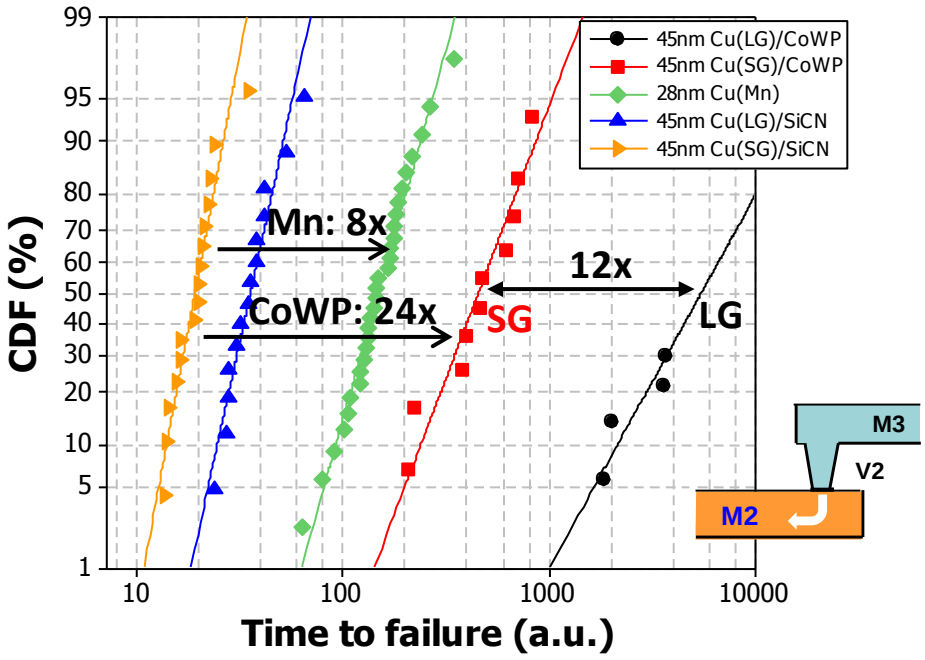


Figure 3.16 Comparison of downstream (V2M2) EM lifetime distributions between pure Cu with standard SiCN cap and CoWP metal cap and Cu(Mn) stressed under 330 ºC and 10 mA/μm^2.

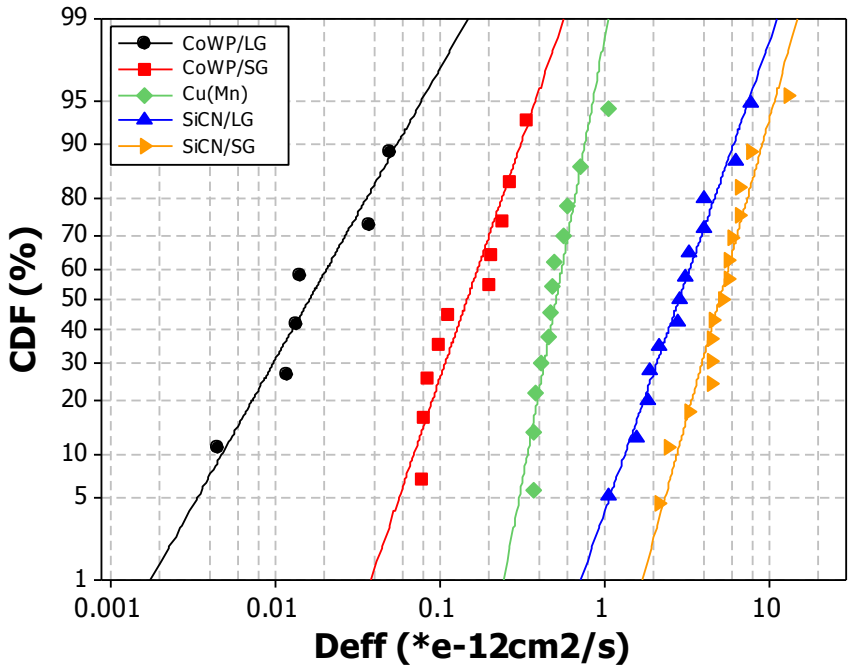


Figure 3.17 Statistical distributions of D_{eff} (at 330 ºC) calculated from R_{slope} for 28 nm Cu(Mn) interconnects and 45 nm node Cu interconnects with different capping layers and grain structures.

Chapter 4: Effects of Scaling on Microstructure Evolution of Cu Interconnects

4.1 INTRODUCTION

The microstructure of Cu interconnects is more complex than Al interconnects because of the different fabrication process used. The texture and grain structure of Al interconnects are easy to evaluate because they have a columnar grain structure, similar to those of films. The Cu interconnects are fabricated using a damascene process where Cu is electroplated onto a seed layer covering the damascene line/via structure. Chemical additives are required for Cu superfilling of the line/via structure that has a high aspect ratio and a narrow line width. The additives and the damascene geometry play an important role in controlling the evolution and structural characteristics of Cu grains [62].

One unique characteristic of electrochemically deposited (ECD) Cu lines is the room-temperature recrystallization or self-annealing phenomenon where Cu grains grow at room temperature accompanied by an increase in Cu {111} texture and a 20~25% decrease in resistivity [63, 64]. A moderately high temperature annealing is used to expedite the grain growth in small interconnect structures, resulting in "bamboo-like" grain structures to reduce the electrical resistivity and improve electromigration resistance. However, as the structures continue to scale, it becomes increasingly difficult for the grain growth to extend into the fine structures.

The grain growth of ECD Cu lines is sensitive to several parameters, such as the properties of the Cu plating seed layer and the barrier layer, the electroplating conditions (current density and bath chemistry), initial grain size, as well as the impurity incorporation. The microstructure characteristics of Cu lines can significantly affect the thermo-mechanical properties and reliability performance. This has generated extensive interest in studying the kinetics and mechanisms of grain growth and texture evolution of

Cu. In this chapter, detailed characteristics of microstructure evolution with interconnect scaling from 45 nm to 22 nm nodes are analyzed and compared with wider Cu lines. The mechanisms driving the grain structure evolution in confined Cu lines are investigated from the perspectives of energetics and kinetics.

4.2 Mechanisms of Grain Structure Evolution in electroplated Cu

4.2.1 Driving Forces for Grain Growth

Grain structure evolution in polycrystalline thin films have been extensively studied [65, 66]. Grain growth is known to occur through motion of grain boundaries reducing sizes of small grains and increasing the average size of the remaining grains. Grain growth in thin films is usually classified into two regimes: normal grain growth, in which grain growth is characterized by a "steady state" behavior with a monomodal grain size distribution; and abnormal (or secondary) grain growth, in which the grain size distribution is bimodal with some very big grains in a matrix of small grains.

Grain growth processes, which can occur during film formation as well as during post-deposition annealing, are driven by a reduction of the overall energy in the system, which comes from a number of sources including grain boundaries, surfaces, interfaces, stresses and impurities. In the following, how the reduction of these energies can drive grain growth and texture development will be examined.

4.2.1.1 Grain Boundary Energy

As-deposited films typically possess small grains and a high amount of energy is stored in grain boundaries. As a result, grain growth is driven by the reduction in the total grain boundary area and thus in the total grain boundary energy. At a more microscopic

scale, this is accomplished when individual boundaries move toward their centers of curvature in order to reduce boundary curvature and therefore boundary energy. If a film with an average grain size r_0 grows to an average grain size r, the reduction in grain boundary energy can be described as

$$\Delta F_{gb} = \gamma_{gb}(\frac{1}{r_0} - \frac{1}{r}) \tag{4.1}$$

where γ_{gb} represents the average grain boundary energy per unit boundary area. The rate of this growth process v is defined by the mobility of the grain boundaries m and the driving force ΔF_{gb}:

$$v = \frac{dr}{dt} = m\Delta F_{gb} = m\gamma_{gb}\kappa \tag{4.2}$$

where κ is the average grain boundary curvature. Since this process is diffusion-controlled, the grain boundary mobility has a strong temperature dependence given by the Arrhenius relationship. Thus, when the temperature or the average grain boundary energy is higher, the grain growth is faster. From Equations (4.1) and (4.2) it is expected that the average grain radius will increase with $t^{1/2}$. It is also expected that the shape of the grain size distribution will be time-invariant. Grain growth with these characteristics is referred as normal grain growth. The normal grain growth process, which is not orientation selective, leads to a monomodal grain size distribution.

In contrast, abnormal grain growth describes a different process, in which large grains grow rapidly within a background of small grains. The grain growth does not occur uniformly; instead subpopulations of grains will occur until all favored grains are

eliminated, resulting in a bimodal grain size distribution with some very big grains in a matrix of small grains. The driving forces for abnormal grain growth are local surface/interface and strain energies, both of which depend on the crystallographic orientations of the grains. This will induce preferred growth of grains with low surface, interface or strain energies to reduce the total energy of the film. Since grains in the favored subpopulation have specific crystallographic orientations, abnormal grain growth in thin films necessarily leads to a microstructure evolution towards a uniform or restricted texture.

4.2.1.2 Surface/Interface Energy

The minimization of surface and interface energy can lead to abnormal grain growth with a kinetic rate of

$$v = m\frac{2\Delta\gamma_{s/i}}{h} \tag{4.3}$$

where $\Delta\gamma_{s/i}$ is the differences of the surface and interface energies for grains on either side of the boundary (a factor of 2 is used if both film top surface and bottom interface are included in the calculation) and h is the film thickness. The effects of surface and interface energy minimization on grain growth and texture evolution is strongly dependent on the thickness of the film. In an ultra-thin film, the overall ratio of surface and interface area to volume is large. Thus the driving force for development of textures with minimum surface/interface energy becomes the strongest. It should be noted that the surface and interface energies are not necessarily favoring the same grain orientation.

There are few experimental data on the variation of surface energy with orientation for Cu. For low Miller index planes, the ordering of surface energies generally follows: $\gamma_{110} > \gamma_{100} > \gamma_{111}$. The values reported by McLean and Gale [67] are extrapolated to 200 °C and summarized in Table 4.1. The close-packed {111} planes have the lowest surface energy for the Cu fcc crystal structure. This leads to a primarily {111} fiber textured films where the {111} plane normal is closely aligned with the film normal.

Table 4.1 The anisotropy of the surface energy of Cu at 200 °C for {111}, {100} and {110} planes [67].

	{111}	{100}	{110}
Surface energy (J/m^2)	2.534	2.610	2.734
$\gamma_{hkl}/\gamma_{111}$	1.000	1.030	1.079

Different from thin films, Cu damascene line structure is a more complex system encapsulated with metal or dielectric barriers to prevent Cu diffusion into the silicon. Trench sidewalls provide additional interfaces which can contribute to the overall interfacial energy and affect the grain orientation in the line structure. Therefore, the contribution of trench sidewall interfaces to the driving force from the surface/interface

energy has to be considered. Accordingly, the reduction of the surface and interface energy density (energy/volume) is given by

$$\Delta F_{s/i} = \frac{2\Delta\gamma_{s/i}}{h} + \frac{2\Delta\gamma_i^{SW}}{w} \tag{4.4}$$

where γ_i^{SW} is the interface energy at the trench sidewalls, w the trench width and h the trench height. This effect is expected to be more pronounced for ultra-fine Cu interconnects in advanced ICs with increased aspect ratio (the ratio of trench thickness to trench width). As the downscaling of Cu interconnects continues, the surface/interface-to-volume ratio increases. Therefore, the contribution of surface/interface energy to microstructure evolution becomes increasingly important in ultrafine Cu interconnect structures. In particular, as the trench aspect ratio increases with interconnect scaling, the sidewall interfaces exert more influence on Cu grain growth during post-electroplating annealing process than the bottom interface. This leads to the preferential growth of a sub-population of grains with crystallographically favorable orientations to minimize the sidewall interfacial energy.

To understand the effect of trench sidewall interfacial energy on the texture of ECP Cu, it is important to recognize the structures of various thin layers surrounding a Cu line. In the damascene process, a Cu (seed layer)/Ta (adhesion layer)/TaN (barrier layer) stack was commonly deposited by physical vapor deposition (PVD) prior to Cu trench electroplating. Ta can exist in two different crystal structures, which depends on the processing conditions. The metastable phase β-Ta is typically formed when PVD Ta is directly deposited on top of a dielectric material (*e.g.* SiO_2). β-Ta phase has tetragonal

crystal structure and a high room-temperature resistivity of ~ 150-220 μΩ cm. In comparison, a TaN underlayer is commonly used to produce the α-Ta phase, which is in the form of body-center cubic (BCC) with a low resistivity of approximately 15 to 30 μΩ cm. TaN formed by PVD under specific conditions can lead to a HCP-TaN with a lower resistivity compared to BCC-TaN. To reduce the RC delay, a bilayer barrier of *α*-Ta/HCP-TaN is preferred. Subsequently, a continuous seed layer of Cu prior to plating is required to ensure a void-free Cu plating in high aspect ratio features.

The surface conditions and microstructure of the PVD seed layer and barrier layer can strongly affect the texture and grain size of the overlying electroplated Cu, which are critical factors that determine the EM reliability of Cu interconnects. The texture of the thin PVD Cu seed layer is influenced by different diffusion barrier systems underneath, which in turn affects the texture of the subsequently electroplated Cu. The effect of Ta-based barrier layers on the microstructure of PVD Cu seed layer has been studied by Stangl *et al.* [68] and similar PVD Cu microstructures were found for both *α*-Ta and *β*-Ta underlayers with a very strong {111} fiber texture, while the {111} volume fraction is very low if PVD Cu is directly formed on TaN. Stronger {111} texture is commonly developed in the Cu seed layer on Ta than TaN, which can be attributed to the heteroepitaxial growth of Cu on Ta [69]. However, such a relationship has not been reported between Cu and TaN. Lee *et al.* [70] revealed that Cu texture does not always grow under the influence of epitaxial relationship with the underlying barrier. The strongest {111} texture was found to develop in the PVD Cu seed layer deposited on amorphous TaSiN. This suggests that the dramatic difference of Cu {111} texture introduced by different barrier systems arise from the difference in the interface bonding strength between Cu and the underlying barrier. The interface quality, quantified by roughness of the Cu surface, is assessed by the degree of agglomeration of Cu on a

barrier layer driven by minimization of surface energy. Higher {111} texture of Cu is developed on better wetting interface of Cu/barrier. The lower degree of agglomeration of Cu on Ta compared to TaN is believed to be due to better adhesion at the epitaxial Cu/Ta interface.

The barrier materials not only affect the texture of freshly deposited Cu but also the kinetics of Cu annealing. In general, the higher the volume fraction of {111} oriented crystals, the slower the kinetics of self-annealing proceeds [62]. This is attributed to a reduction in driving forces for grain growth. In more strongly textured features, the grain boundaries are primarily tilt boundaries, with their grain-to-grain misorientation angles grouped around certain angles that correspond to low angle grain boundaries exhibiting low energy and mobility and the elastic modulus is very similar for those grains that are closely oriented.

For the damascene Cu lines, the strength of the {111} fiber texture weakens as the line widths decrease. This is likely due to the increasing effect of nucleation and growth from the side walls of the trenches with decreasing width. The surface energies of {110} and {112} planes are similarly low in FCC metals and they are at 90° from each other in the {111} planes. It is reasonable to conclude that the arrangement of these 3 orientations along the 3 orthogonal directions in the Cu trench will provide an ideal configuration for the surface/interface energy minimization.

4.2.1.3 Elastic Strain Energy

Another important driving force for abnormal grain growth is the strain energy in thin films. The Cu film and the Si substrate have different elastic and thermal properties. For instance, Si has a coefficient of thermal expansion (CTE) of 4.6×10^{-6} /K, whereas

CTEs of Al and Cu are 23.1×10^{-6} /K and 16.5×10^{-6} /K, respectively. Upon a temperature change, the CTE mismatch can lead to a significant strain since the film and the substrate are rigidly attached to each other. Under plane stress conditions, a strain energy density for each grain can be expressed as:

$$E_\varepsilon = \varepsilon^2 M_{hkl} \tag{4.5}$$

where ε is the biaxial strain between the film and the substrate and M_{hkl} represents the effective biaxial modulus for the grain with crystallographic direction <hkl> with respect to the plane of the strain. Following Murakami's work [71], M_{hkl} can be calculated as

$$M_{hkl} = C_{11} + C_{12} + K - \frac{2(C_{12} - K)^2}{C_{11} + 2K}$$

$$K = (2C_{44} - C_{11} + C_{12})(h^2k^2 + k^2l^2 + l^2h^2)$$
$$h^2 + k^2 + l^2 = 1 \tag{4.6}$$

where C_{11}, C_{12} and C_{44} are the stiffness constants. For Cu, C_{11}=168.3 GPa, C_{12}=122.1 GPa, C_{44}=75.7 GPa. Cu is a highly elastically anisotropic material with M_{hkl} at the maximum for {111}-textured grains and the minimum for {100} grains. Thus in biaxially strained films, grains with different orientations have different strain energy densities and these energy differences can contribute to the driving force for grain growth, favoring grains with strain energy density minimizing orientations. The effects of strain energy minimization to abnormal grain growth can be expressed as:

$$v = m\Delta W_\varepsilon = m\varepsilon^2 \Delta M \tag{4.7}$$

where ΔM is the difference in the biaxial moduli of the two grains meeting at the boundary under consideration.

The Cu interconnect structure is a dimensionally confined system with multiple interfaces and materials fabricated using a complex dual damascene process. The thermal expansion mismatch between the metal and surrounding dielectric generates thermal stresses, which can induce void formation and degrade interconnect reliability. Unlike the biaxial stress state of a uniform thin film, a patterned line structure has a triaxial stress state with an effective modulus depending on the grain orientation, which should be used in calculating the strain energy for grain growth. Wilson *et al.* [72] studied the scaling effect on stresses in advanced Cu/low-k interconnects using synchrotron measurement and found that all three normal stresses increase with decreasing line width. Interestingly, beyond the 100 nm, the trend is reversed. They attributed this to the grain structure effect on stress evolution in that the stress in the polycrystalline wide lines continues to relax, while the grains in the bamboo-like narrower lines become pinned in the line width, limiting further grain growth and leading to an increase in stress. Beyond the 100 nm, Cu lines become polycrystalline again, where grains can reorder during grain growth to relieve the thermal stress.

Among the three normal stresses, the one along the line length direction was usually found to be the highest. Therefore, to minimize the elastic strain energy, Cu grains would orient themselves in such a way that the lowest elastic modulus direction is aligned with the maximum stress direction. Cu is strongly elastically anisotropic (Figure

4.1), with its elastic modulus along the <111> direction about 3 times higher than the <100> direction.

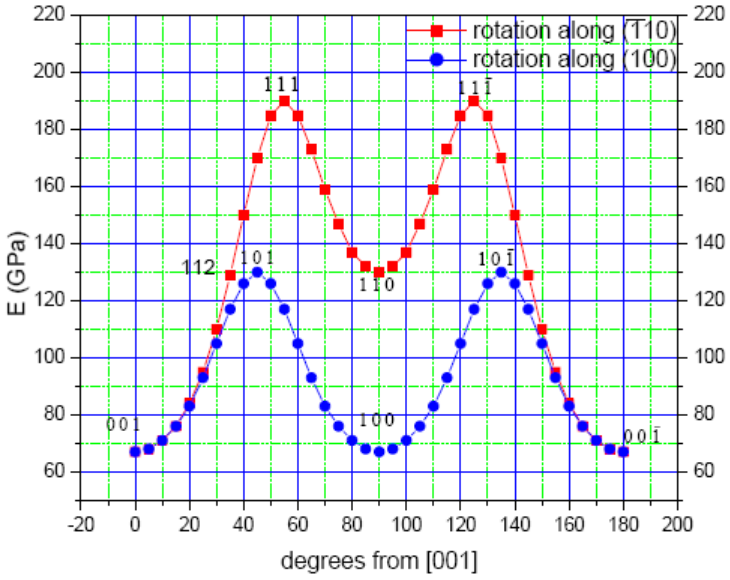


Figure 4.1 Elastic modulus of Cu along different crystal directions.

It is important to note the orientation of minimum strain energy is generally not the same as the orientation of minimum surface/interface energy. For Cu lines, the surface and interface energies are lowest for grains with a {111} texture, whereas the strain energy favors a {100} texture. Since it is impossible to have {111} and {100} planes perpendicular to each other and coexist in a grain, a competition between {111} and {100} oriented grains exists in Cu lines. For instance, abnormal grain growth of {111} oriented grains would occur if the surface/interface energies are higher than the strain energy. On the other hand, if the minimization of strain energy dominates the abnormal grain growth process, a {100} texture would develop. Furthermore, the geometric constraints imposed by the dual-damascene process influence the texture

evolution during grain growth. It is worth noting that in narrow Cu lines grain growth could be constrained by kinetics involving growth of sidewall, bottom-up and overburden grains.

4.2.2 Overburden effect

Electroplated Cu for silicon chip interconnections are deposited first at room temperature by an energetically gentle process, and may be considered metastable immediately after deposition. This process leads to Cu with a small as-deposited grain size. Harper *et al.* [64] proposed that the fine as-deposited grain structure is a result of grain boundary pinning by additives introduced into Cu from the electroplating bath. Additives in the plating baths are introduced to improve the trench fill, or the "superfill" capability. After electroplating, an annealing step is carried out to promote grain growth before Cu in the overburden layer is removed using chemical-mechanical polishing (CMP). The additives are particularly important in controlling the kinetics of grain growth during post-plating annealing, which is attributed to the additive desorption from the pinning sites at grain boundaries. Studies have shown that the grain growth in Cu lines starts from the overburden layer and propagates into the trenches below since the impurity level at the top of the overburden layer is the highest at the end of the superfilling process. As a result, the overburden layer is characterized by a columnar grain structure, consistent with the high degree of grain growth expected for Cu thin films.

For wide lines with line widths larger than 300 nm, the microstructure in the trench and the overburden layer are comparable [73, 74]. Almost complete invasion of the trench from the overburden layer has been observed where grains extend all the way

from the overburden surface down to the trench bottom, leading to the formation of near-bamboo grains in the line. Narrow lines, however, are not fully invaded even under annealing at elevated temperatures. These studies suggest grain growth inside the Cu trench is strongly dependent on geometrical constraints due to the narrow line width and high trench aspect ratio [75]. Abnormal grain growth in narrow lines can progress very fast before grains from the overburden reach the trench. Interfaces can also limit the impact of the overburden layer on the in-line grain growth particularly for Cu lines with higher aspect ratios. The extension of the overburden layer into the trench may be restricted by the growth of sidewall {111} grains, resulting in a polycrystalline grain structure with clusters of small grains mixed with some large grains. Thus, in narrow Cu interconnects, the thermodynamically driven grain growth phenomenon can be constrained by kinetics involving a balance between growth of trench grains (*e.g.* sidewall components) and overburden grains.

4.3 Scaling Effects on Cu Microstructure

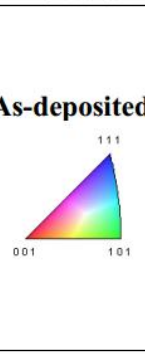
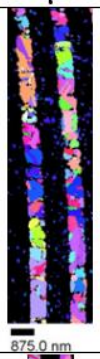
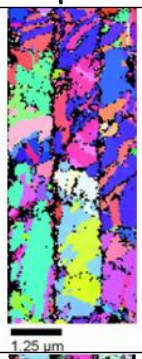
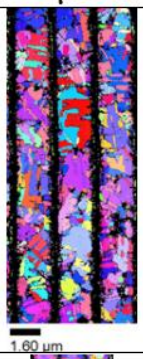
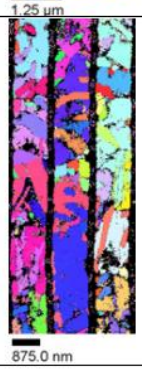
4.3.1 Cu Thin Films and Wide Lines

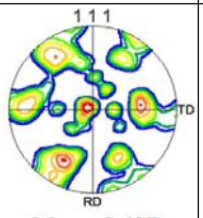
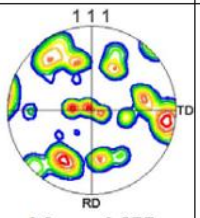
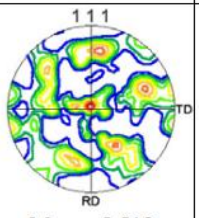
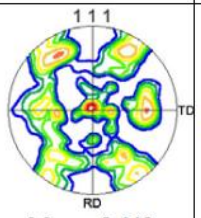
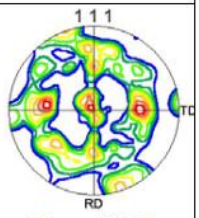
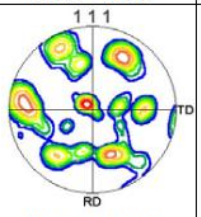
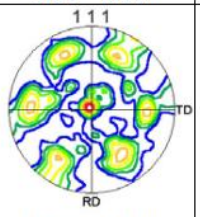
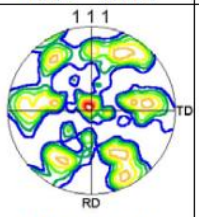
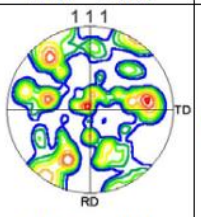
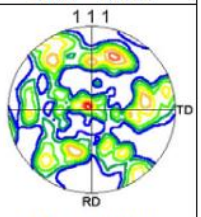
The microstructure of an Al line is essentially identical to those of Al thin films because patterned lines are fabricated simply by etching the films. Thus, a bamboo structure can be readily achieved for Al interconnects. The microstructure of Cu damascene lines, however, is very different from that of Cu thin films. The electroplated Cu grows from three directions simultaneously, from both the sidewalls and the bottom of the trenches. As a result, a bamboo structure can be difficult to attain for narrow Cu lines. Grain size in the line and the degree of growth twinning will be reduced. These

properties will affect the mechanical and diffusional behavior of Cu with possible impact on reliability performance of Cu interconnects, particularly for ultra-fine lines.

Microstructure evolution with line scaling has been extensively studied, mostly for wide lines using x-ray diffraction (XRD) and EBSD technique. XRD pole figure analysis is usually used for texture characterization of Cu thin films. The low spatial resolution of X-ray analysis, however, limits the determination of the local Cu microstructure. Besser *et al.* [76] investigated the microstructure of inlaid Cu lines with trench width ranging from 0.35 to 1.06 μm using XRD. They found that the grain texture of these lines is predominantly {111} out-of-plane with preferred [110] in-plane orientation parallel to the trench sidewall and independent of the annealing temperature.

In addition to XRD which is mostly used to obtain average information about texture, EBSD equipped with SEM has been used to obtain detailed local microstructure characteristics for Cu lines. Cho *et al.* [77, 78] studied the annealing effect on the microstructure evolution of Cu interconnects for line widths from 0.14 to 2 μm (Figure 4.2). They found out as the line width increases the texture becomes more fiber-like with preferred {111} orientation along the trench normal, which is consistent with the results from Besser *et al*. [76]. The maximum intensity of the texture, as shown in {111} pole figures, was found to increase with decreasing line width after annealing. They also studied the grain boundary characteristics and found more twin boundaries with less Σ3 boundary characteristics when the line width was reduced from 0.5 μm to 0.14 μm. It is worth noting after annealing the twin population is reduced especially for 0.14 μm Cu lines. In their study, the twin boundaries were distinguished by a misorientation criterion alone so both coherent and incoherent twins were counted together.

Line Width	0.14µm	0.24µm	0.5µm	1µm	2µm
As-deposited					
Annealed (a)					

Line Width	0.14 µm	0.24 µm	0.5 µm	1 µm	2 µm
As-deposited	 Max = 8.697	 Max = 6.577	 Max = 5.512	 Max = 5.648	 Max = 3.915
Annealed (b)	 Max = 14.054	 Max = 8.878	 Max = 6.043	 Max = 6.094	 Max = 4.056

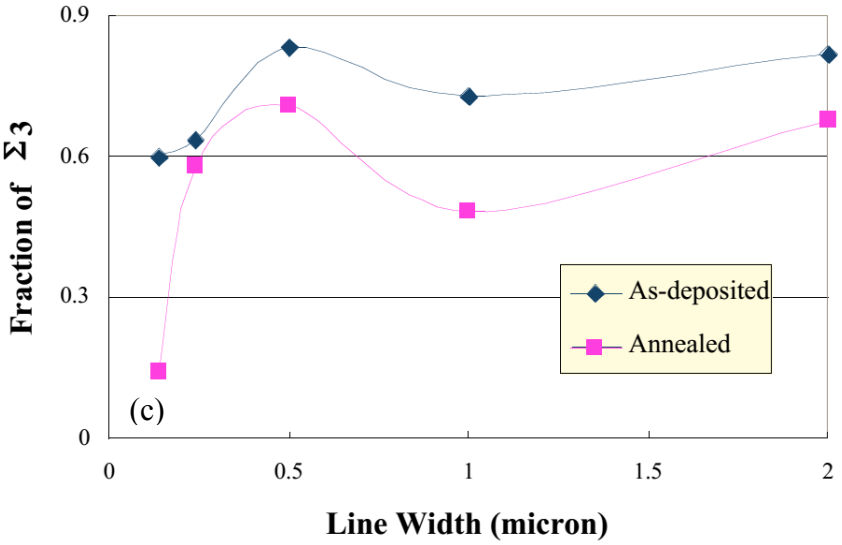


Figure 4.2 Cu interconnects with line widths from 0.14 μm to 2 μm: (a) Inverse pole colored orientation maps for as-deposited and annealed (200 °C) samples. (b) {111} pole figures. (c) Fraction of Σ3 boundaries in Cu interconnects [77, 78].

Muppidi and Field *et al.* [79, 80] studied the effects of barrier layer, line geometry and alloying on the microstructure of electroplated Cu films and lines. Compared to thinner films (480 nm), a slightly weaker {111} texture, a higher fraction of twin boundaries, and larger grains were found with increasing film thickness, *e.g.* at 850 nm. They observed that the microstructure of the damascene Cu lines is a strong function of line geometry (0.2-5 μm in line width). Interestingly, a decrease in texture intensity was observed to associate with an increase in the twin population (Figure 4.3), indicating twinning in grains randomizes the texture. They further concluded that twin formation dominated microstructure evolution particularly in the damascene structures. This was attributed to the transition of the stress state in the confined geometry from primarily biaxial in wide lines to triaxial in narrow lines [81].

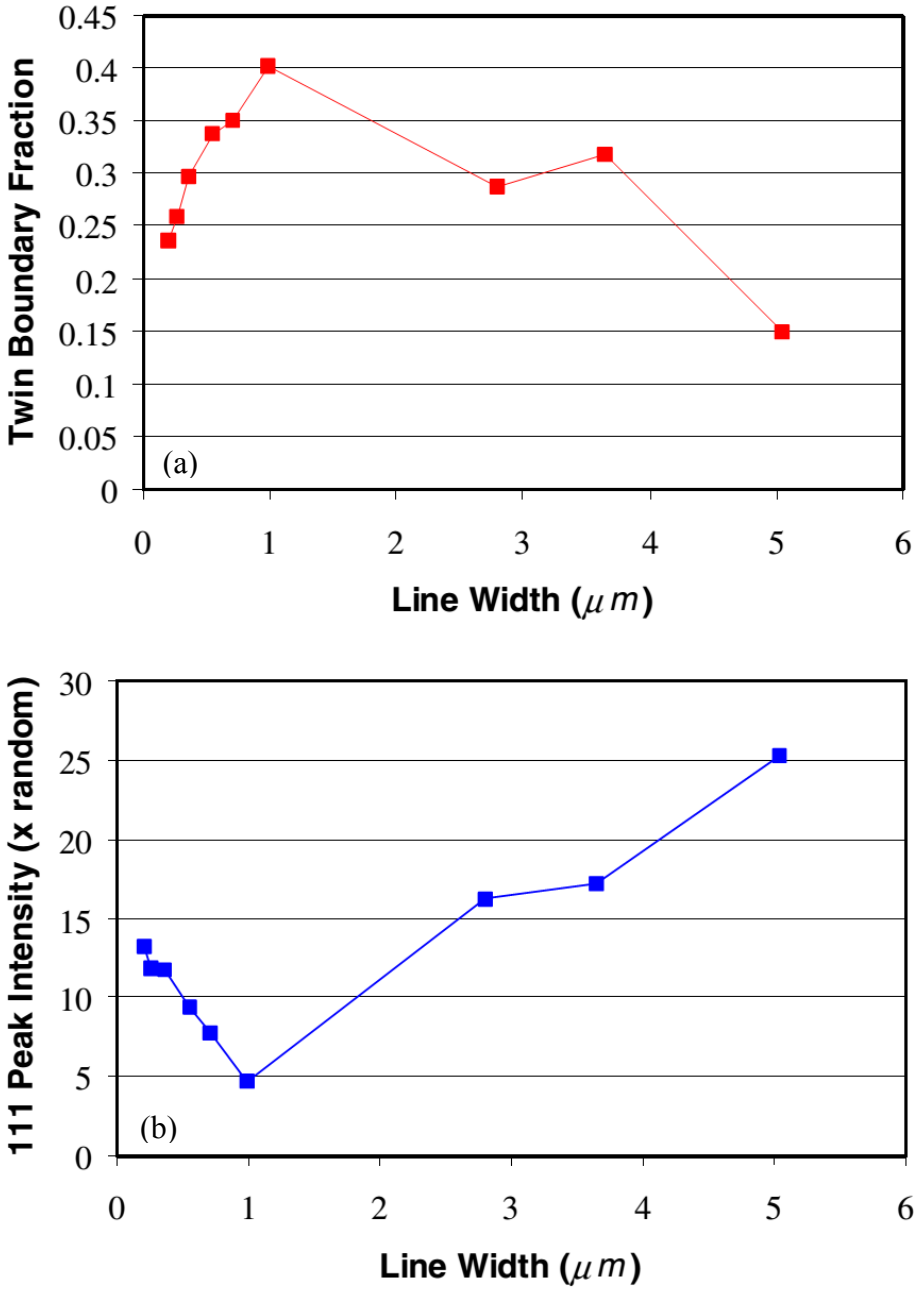


Figure 4.3 (a) The fraction of twin boundaries as a function of line width. (b) The change in the {111} peak intensity with varying line widths [79].

A high degree of twinning along with a bimodal grain size and random texture components are commonly found in plated Cu thin films. In general, annealing twins are formed during grain growth and become most prevalent in large Cu grains, as evidenced by many individual grains show multiple twin sites. As strain energy increases during grain growth, twins are formed with the motion of coherent twin boundaries.

4.3.2 Nanoscale Cu Lines

Detailed information on grain structure has been rarely reported for sub-100 nm Cu lines, primarily due to the limited spatial resolution and the lack of automation in obtaining the statistical distribution of microstructure for nanoscale grains. Using the aforementioned precession electron diffraction technique, the microstructure details of Cu grains less than 5 nm can be clearly detected.

4.3.2.1 70 nm Cu Lines (45 nm node)

Grain orientation and texture observed in typical segments of the 70 nm wide Cu lines using the high-resolution PED technique are shown in Figures 4.5 and 4.6 for SiCN capped structures with small grains and large grains, respectively. For comparison, the grain structure observed in a standard cross-sectional TEM image is shown in Figure 4.4, which does not produce sufficient contrast to analyze the grain structure characteristics. In contrast, the grain structure could be clearly observed using the PED technique. The inverse pole figure (IPF) [82] texture plots of the SG structure exhibited a strong {111} and {110} texture along the trench width and trench normal, respectively, indicating a dominant growth of {111} grains from the sidewall in Cu nanolines. The large grain (LG) line showed a similar but weaker bi-axial texture (Figure 4.6). For the 70 nm lines, the

sidewall growth of {111} grains became dominant, reflecting the increasing importance of the interface energy in controlling grain growth with further scaling of Cu interconnects.

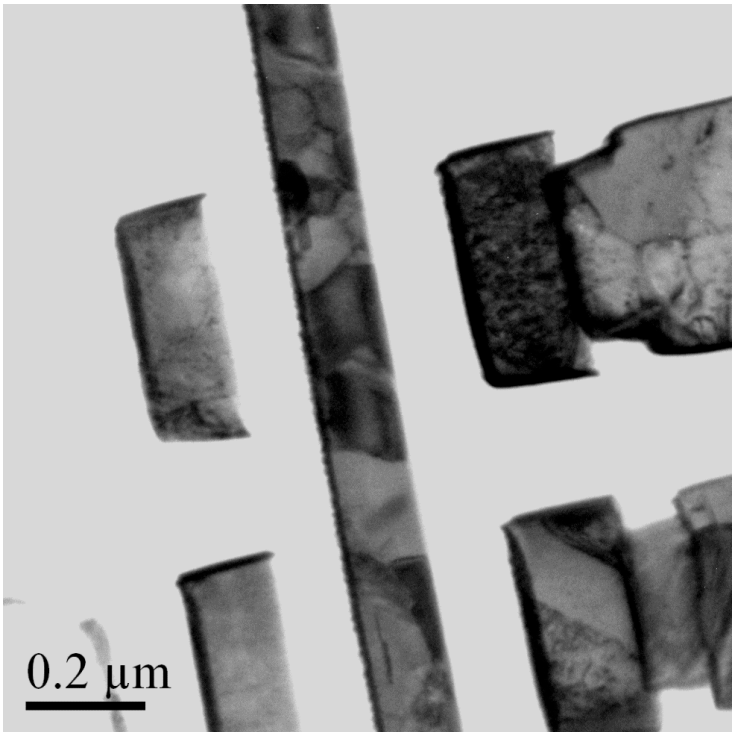


Figure 4.4 Representative TEM image of the 45 nm node Cu interconnect line.

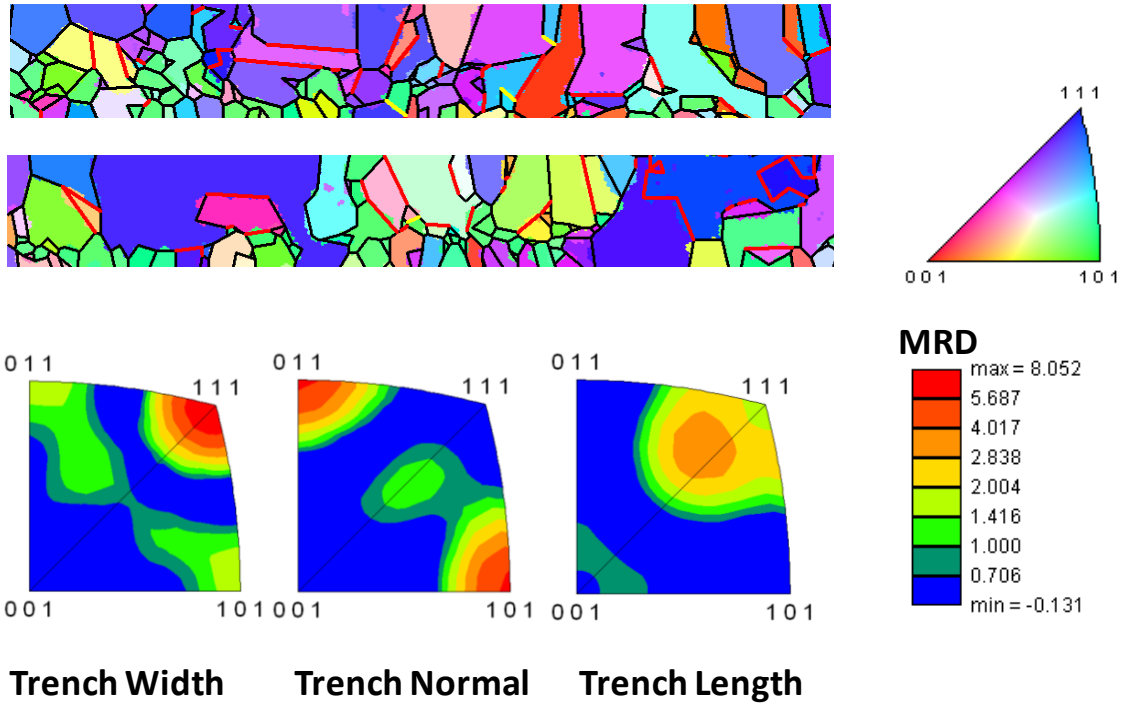


Figure 4.5 45 nm node SG structure: (top) Representative color-coded IPF orientation maps (along trench width) overlaid with the reconstructed grain boundaries. Color codes for orientations are represented in the standard stereographic triangle. (bottom) Texture plots along the trench width, trench normal, and trench length.

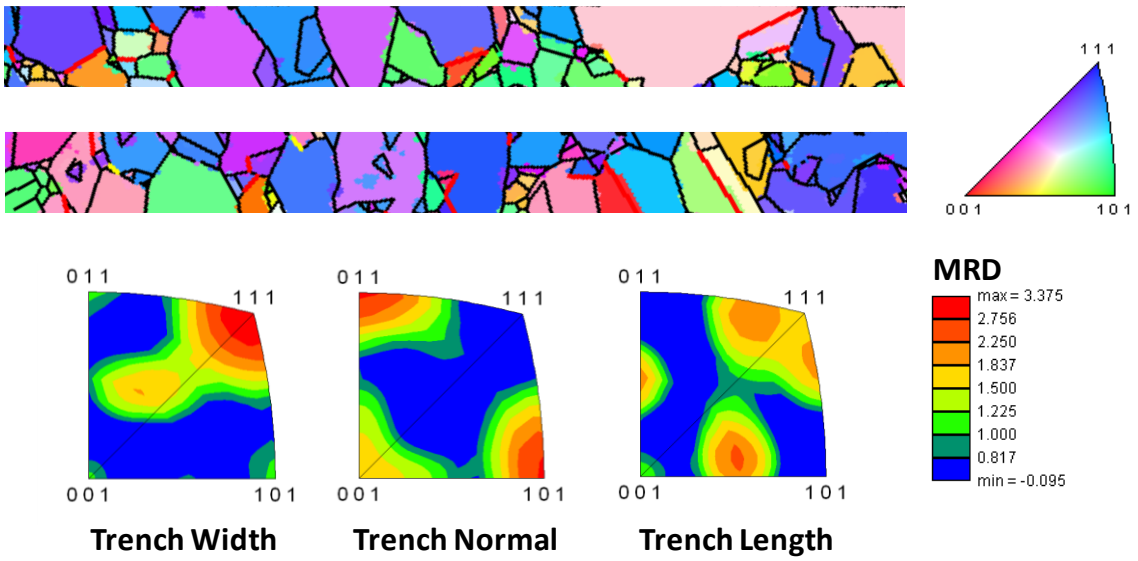


Figure 4.6 45 nm node LG structure: (top) Representative color-coded IPF orientation maps (along trench width) overlaid with the reconstructed grain boundaries. (bottom) Texture plots along the trench width, trench normal, and trench length.

Grain boundary trace analysis was used to characterize the coherent Σ3 type boundaries, marked by red lines in Figures 4.5 and 4.6. The length fraction of these boundaries was found to be about 16% and 12% for the SG and LG structures, respectively. Typically, such coherent twin boundaries are low energy boundaries and do not constitute fast diffusion paths for EM mass transport [28]. Other boundaries marked by dark lines are high-angle boundaries with misorientation angles larger than 10°. The overall distributions of misorientation angles were similar for both SG and LG structures (Figure 4.7). The grain size followed a lognormal distribution for both structures with a larger σ for SG as shown in Figure 4.8, where the average grain sizes for the SG and LG lines were found to be 42 nm and 58 nm in diameter, respectively. Many small grains of less than 5 nm were observed at the bottom of the SG lines and most of them were

separated by high-angle boundaries (Figure 4.5). This can be attributed to the fact that as a result of the preferential sidewall growth of {111} type grains, small bottom-up growing grains filled in the remaining space in the line and formed connecting high-angle boundaries. The presence of the small grains seems to be caused by interconnect downscaling, which increases the grain boundary contribution to mass transport and further degrades EM lifetime.

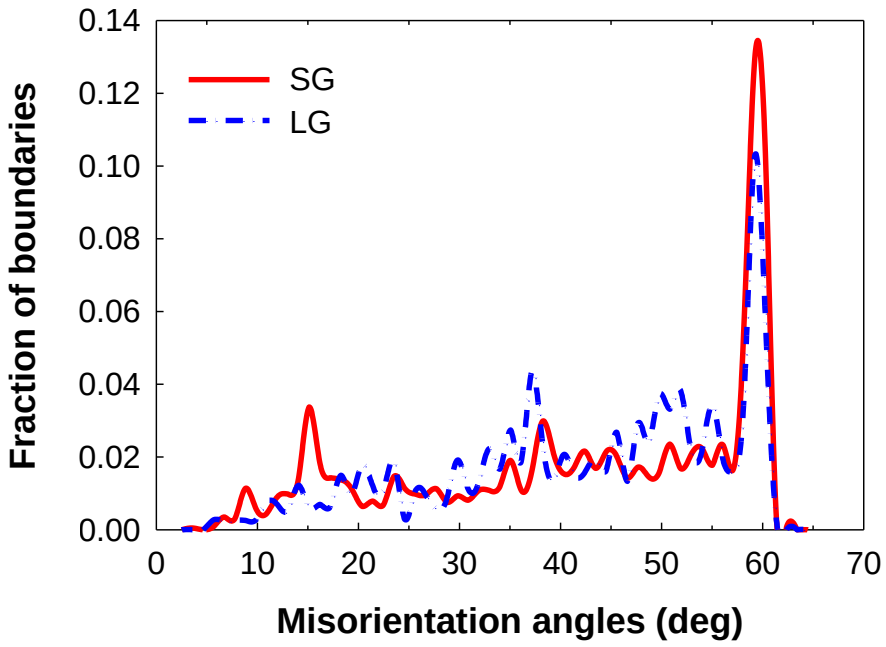


Figure 4.7 Grain boundary characteristics of 45 nm node SG and LG structures.

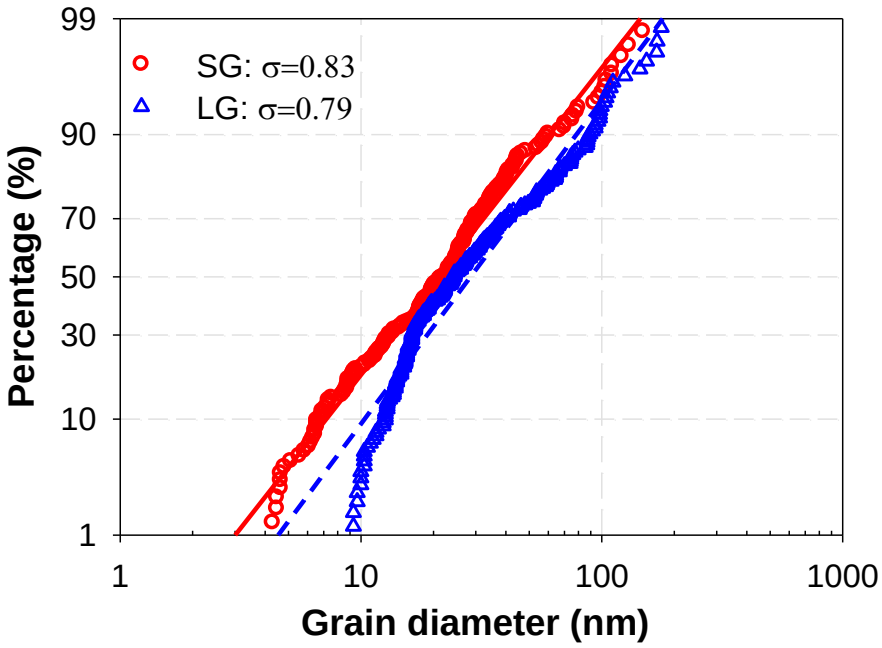


Figure 4.8 Grain size distribution of 45 nm node SG and LG structures.

The microstructure analysis was further applied to the via/line region since a better understanding of the local microstructure details close to the via/line interface is particularly important to study downstream EM void formation. An example is shown in Figure 4.9 where the grain structure observed for a downstream via/line structure (SG) revealed that several small grains with high angle boundaries aggregated right underneath the V2 via and adjacent to 2 large grains separated by a coherent Σ3 boundary. This yielded a configuration well-suited for formation of "slit" voids at the interface to induce early failure when the downstream current flow from the via (coarse-grained region) to a lower level line (fine-grained region). This would provide a mechanism responsible for EM failures observed with tests performed under the Blech short length limit of jL_c [35].

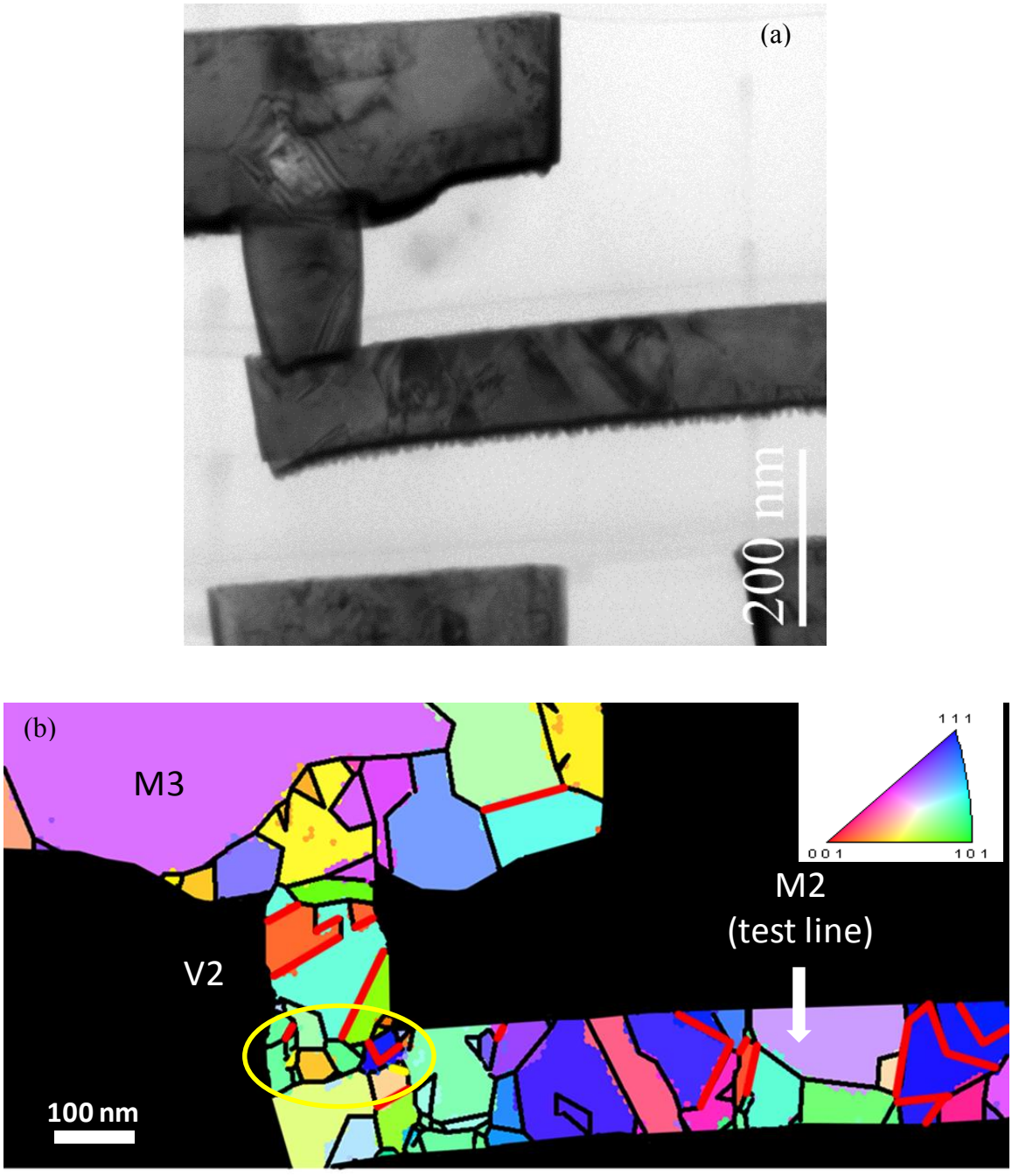


Figure 4.9 (a) BF TEM image of Cu trench (M2) and via (V2) for the 45 nm node SG structure. (b) The color coded IPF orientation map for the same via/line region.

4.3.2.2 45 nm Cu Lines (28 nm node)

Grain orientation mapping along the 45 nm trench width for the 28 nm node Cu interconnects is shown in Figure 4.11. The orientations and boundaries of grains less than 5 nm are clearly detected, demonstrating the capability of the PED technique. Such microstructure details would be difficult to extract from the BF TEM images because of the presence of local defects and off-zone grains (Figure 4.10). Statistical distributions of grain orientations (texture) are plotted in Figure 4.11 along 3 orthogonal directions (trench width, trench normal and trench length). The IPF plots reveal a very strong {111} texture (max. MRD=14), reflecting the increasing importance of Cu/Ta interfacial energy in controlling grain growth as line width is reduced to 45 nm. It is worth noting that as line width decreases from 70 nm to 45 nm, the {111} texture begins to shift its preferred orientation from along the trench width to the trench length.

Grain boundary trace analysis was performed to characterize coherent Σ3 type boundaries, as marked by red lines in Figure 4.11. The length fraction of these boundaries was found to be only 2%, significantly reduced from the 12% observed for 70 nm Cu lines as discussed in the previous section. Coherent twin boundaries are of particular interest because they are low-energy boundaries and not fast diffusion paths for EM mass transport. Also, the resistivity of twin boundary is about one order of magnitude smaller than other grain boundaries [83]. The effect of grain boundary scattering on Cu resistivity will become important as line dimensions approach the mean free path for electron scattering (39 nm @ room temperature). Other boundaries marked by dark lines are high-angle boundaries with misorientation angles larger than 10°. The overall grain structure is of polycrystalline type with very short bamboo segments. The average grain size is about 26 nm in diameter following a lognormal distribution with smaller grains aggregating at lower surfaces.

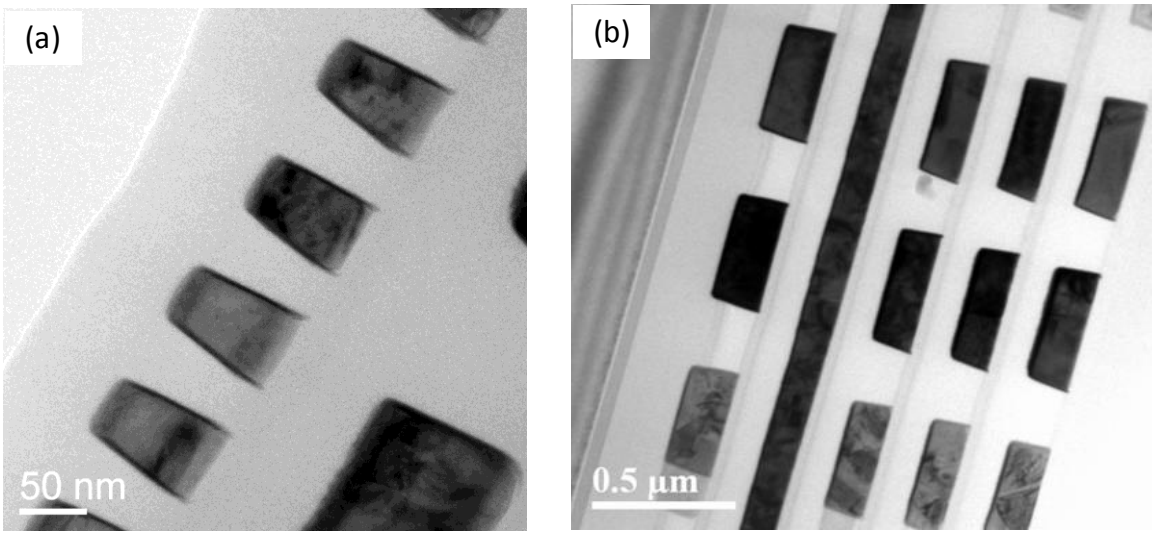


Figure 4.10 (a) BF TEM image of periodic M2 Cu lines for the 28 nm node. (b) BF TEM image of a single M2 line along the line length direction.

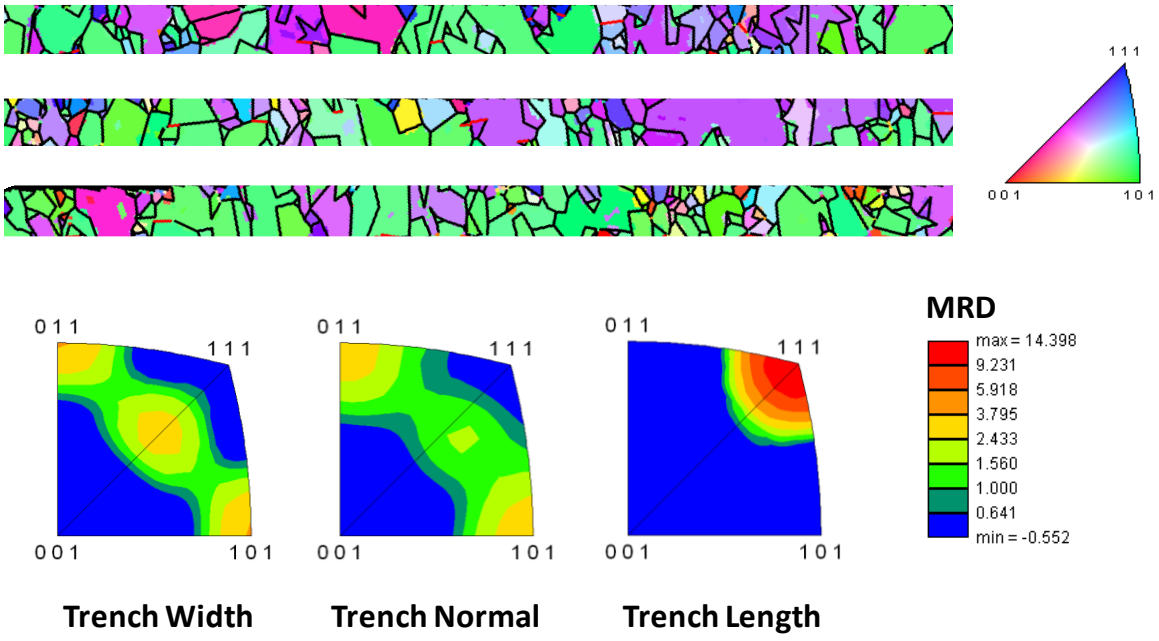


Figure 4.11 28 nm node Cu lines: (top) Representative color-coded IPF orientation maps (along trench width) overlaid with the reconstructed grain boundaries. (bottom) Texture plots along the trench width, trench normal, and trench length.

4.3.2.3 40 nm Cu Lines (22 nm node)

The grain structure analysis using the PED technique was further extended to Cu lines of the 22 nm node (40 nm in line width). With the small precession angle of 0.4°, the detailed microstructure information from hundreds of Cu grains (as small as a few nanometers) within a single Cu line (Figure 4.12) can be accurately measured in an automatic fashion. Similar to Cu lines of the 28 nm node, the texture of the 22 nm Cu lines is dominated by {111} along the line length direction, while the intensity of {111} texture is higher (max. MRD=17). The coherent twin boundaries almost completely disappear in the 40 nm Cu lines with a length fraction of only 0.5% among all the grain boundaries. Also, bamboo segments are barely observable in the 40 nm Cu lines with an

average grain size of about 20 nm. With smaller grains and less twin population for ultra-fine Cu interconnects, there will be more GB scattering contributing to Cu resistivity and more GB diffusion further degrading EM performance.

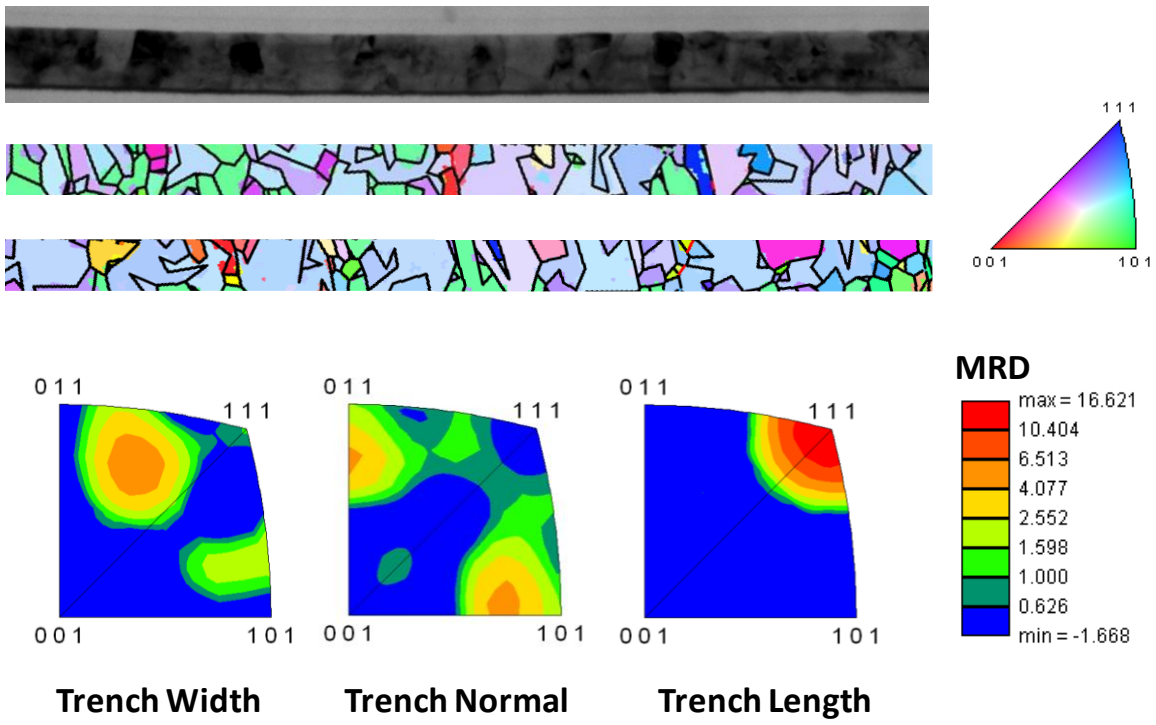


Figure 4.12 22 nm node Cu lines: (top) Representative BF TEM image. (middle) Representative color-coded IPF orientation maps (along trench width) overlaid with the reconstructed grain boundaries. (bottom) Texture plots along the trench width, trench normal, and trench length.

4.3.3 Microstructure Scaling at the Nanoscale

The microstructure characteristics of Cu lines observed so far differ significantly from that of wider Cu lines and Cu thin films. In comparison, microstructure studies of 1.8 μm and 180 nm wide lines show a strong {111} fiber texture along the trench normal,

demonstrating a dominant Cu grain growth from the trench bottom for wide Cu lines. As the line width is reduced to 120 nm, the {111} fiber texture is weakened and a slight preference for {111} orientations emerges along the trench width (max. MRD=4). With further scaling to 70 nm line width, the sidewall growth of {111} grains becomes dominant as discussed earlier in this study. In addition to the texture change with increasing line widths, downscaling of Cu interconnects also leads to changes of grain boundary characteristics. In 1.8 μm lines, 42% of the grain boundaries are of the coherent Σ3 type. For 180 nm and 120 nm lines, the length fraction of coherent twin boundaries is reduced to about 25% and 18%, respectively. The decrease in coherent twin percentage with scaling continues towards 40 nm lines where coherent twins become barely observable.

4.3.3.1 Scaling Effect on Crystallographic Texture

Grain orientation mapping along the trench width for Cu interconnects is plotted in Figure 4.13 for three technology nodes (45 nm, 28 nm and 22 nm). Statistical distributions of grain orientations (texture) are plotted in Table 4.2 along 3 orthogonal directions (trench width, trench normal and trench length). For the 70 nm wide Cu lines (45 nm node), the IPF texture plots exhibited a strong bi-axial texture with {111} along the trench width and {110} along the trench normal, indicating a dominant growth of {111} grains from the trench sidewall in Cu nanolines. A careful examination of 45 nm and 40 nm Cu lines revealed an increase in the maximum intensity of {111} texture (Figure 4.14) from MRD of 10 for the 70 nm lines to 22 for 45 nm and further to 25 for the 40 nm Cu lines, reflecting the increasing importance of Cu/Ta interfacial energy in controlling grain growth as a result of decreasing line width and increasing trench aspect

ratio. Interestingly, different from the 70 nm lines, the prominent {111} texture for 45 nm and 40 nm lines showed a transition from along the trench width to along the trench length. It could be attributed to the effect of the geometrical confinement on the ultrafine interconnect structures. In a Cu line with width less than 45 nm, {111} grains growing from the sidewall along the trench width tend to impinge onto each other impeding further grain evolution except along the trench length. This was observed as shown in Figure 4.12.

So far, the results for sub-100 nm nanolines and wider lines up to 1.8 μm width reveal a systematic change in electroplated Cu grain structure for Cu interconnects as a function of line width. Starting from the 1.8 μm wide Cu lines [84], a strong fiber texture with {111} along the trench normal (the so-called "bottom growth component", Figure 4.15) was observed, where the strength of the fiber texture continued to increase for 0.18 μm Cu lines. As the line width further reduced to 120 nm, a weak {111} texture along the trench width (the so-called "sidewall growth component", Figure 4.15) started to emerge, marking a transition of the {111} texture from along the trench normal for wider lines to along the trench width for narrower lines. The intensity of the sidewall {111} texture became stronger for Cu lines of 70 nm and narrower width.

Such microstructure features differentiating narrow Cu lines from wide lines can be understood in terms of minimization of the overall energy driving the microstructure evolution. The problem is complex since the Cu line is constrained in nanoscale by multiple interfaces. With continued downscaling, the ratio of the surface and interface area to volume ratio increases. Therefore, the contribution from the trench sidewall interface to Cu grain growth becomes increasingly important with respect to the trench bottom surface. This leads to the preferential sidewall growth of Cu {111} grains to minimize the Cu/Ta interfacial energy. To further minimize the trench bottom surface

energy, the {111} grains growing sidewall-like would tend to align with the {110} planes along the trench normal, as shown in the case of 70 nm Cu lines. Finally, grains with {111} texture along the trench width and {110} along the trench normal converge to a {112} texture along the length of the Cu line. This orientation minimizes the elastic strain energy.

Technology	Line Width (nm)	Representative Grain Orientation Mapping
45 nm	70	
28 nm	45	
22 nm	40	

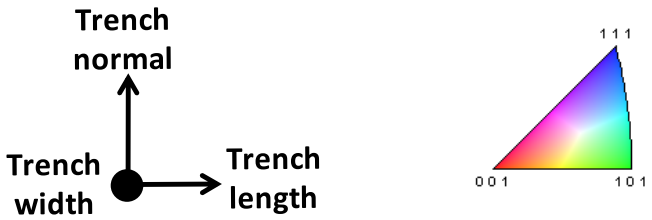
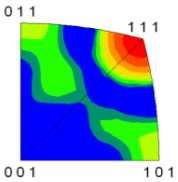
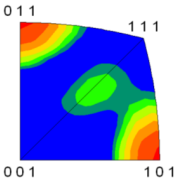
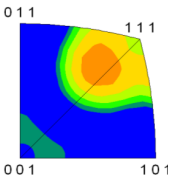
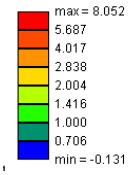
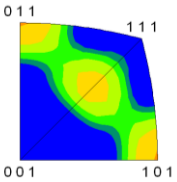
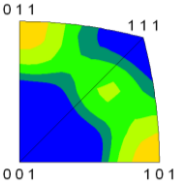
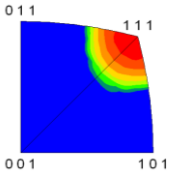
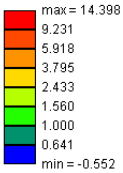
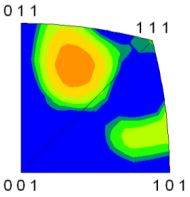
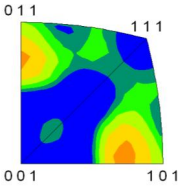
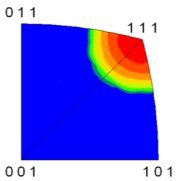
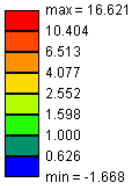


Figure 4.13 Representative color-coded IPF grain orientation maps (along the trench width direction) for Cu lines of the 45 nm, 28 nm and 22 nm technology nodes. Color keys for orientations are represented in the standard stereographic triangle.

Table 4.2 Color-coded IPF maps for grain orientation distribution (texture) for Cu lines of the 45 nm, 28 nm and 22 nm technology nodes.

Technology	Line Width (nm)	Trench Width	Trench Normal	Trench Length	Texture Strength (MRD)
45nm	70				
28nm	45				
22nm	40				

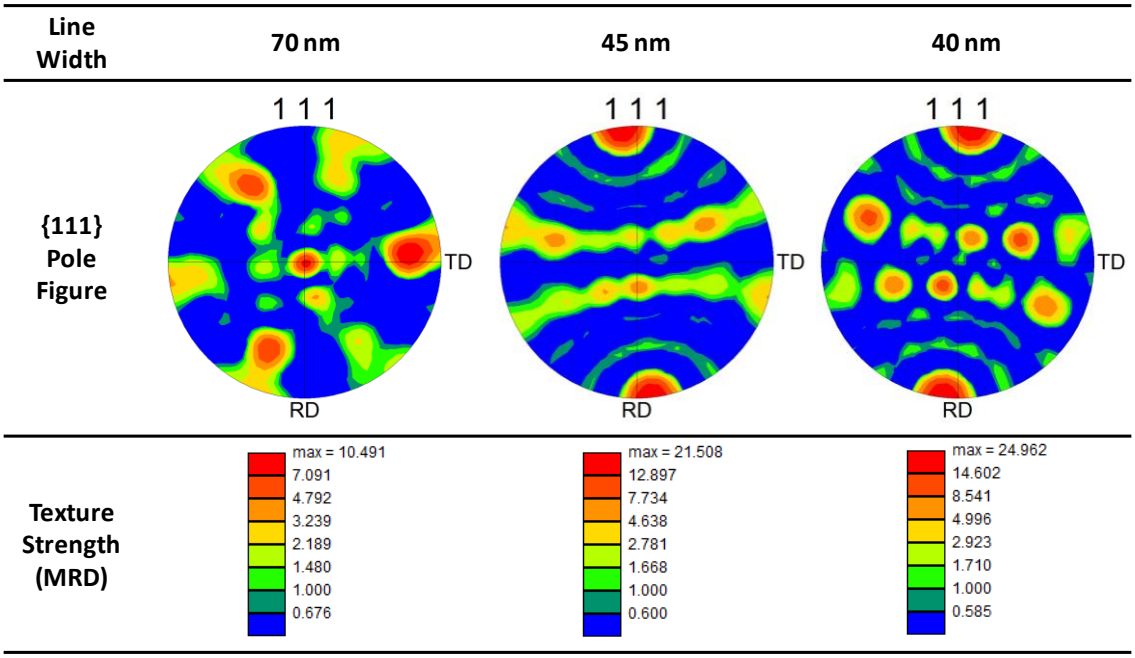
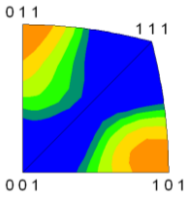
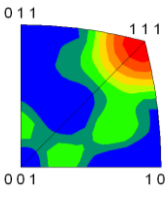
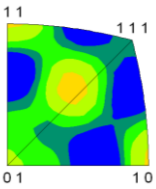
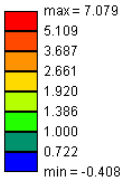
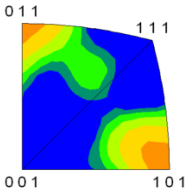
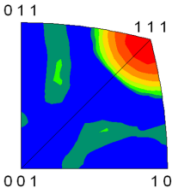
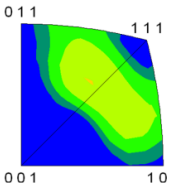
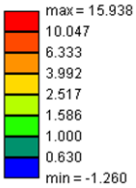
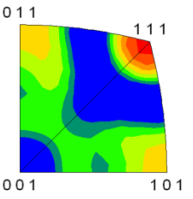
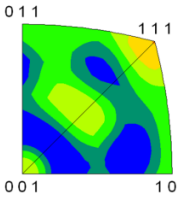
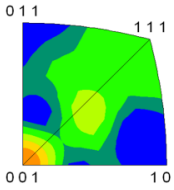
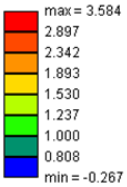


Figure 4.14 {111} pole figures of Cu lines for the 45 nm, 28 nm and 22 nm technology nodes.

Table 4.3 Color-coded IPF maps for grain orientation distribution (texture) for wider Cu lines with line widths ranging from 0.12 μm to 1.8 μm [84].

Technology	Line Width (nm)	Trench Width	Trench Normal	Trench Length	Texture Strength (MRD)
	1800				
130 nm	180				
90 nm	120				

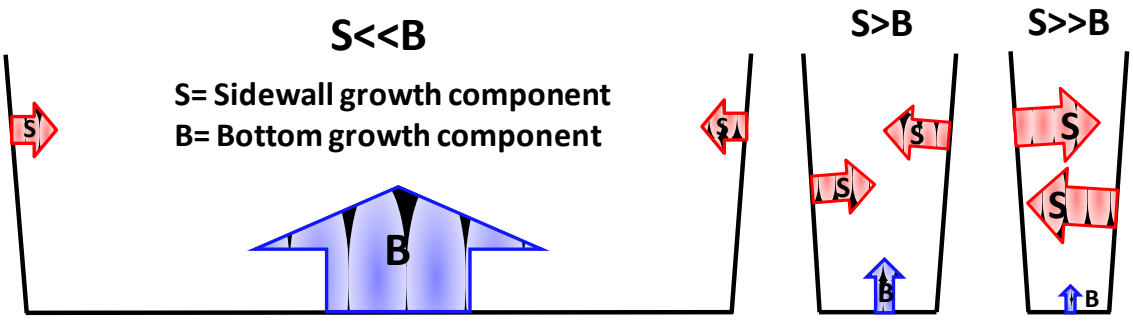


Figure 4.15 Schematic illustration of the relative contribution of "bottom growth component" versus "sidewall growth component" to the microstructure evolution of Cu interconnects with geometrical downscaling.

4.3.3.2 Scaling Effect on Coherent Twin Boundaries

Grain boundary trace analysis was performed on Cu interconnects for the 45 nm, 28 nm and 22 nm nodes. Coherent Σ3 type boundaries are marked by red lines in Figure 4.13 where grain boundaries outlined by dark lines are high angle boundaries with misorientation larger than 10°. In Table 4.4, different types of grain boundaries observed in electroplated Cu lines are summarized together with their respective energies [85].

Here a "twin" refers to a grain that has one or two twin boundaries embedded in a larger grain. Twin boundary is a common planar defect in crystalline Cu with low stacking fault energy, which usually results from mechanical deformation or thermal annealing. For the FCC crystal structure, the twin boundary (TB) misorientation can be obtained by rotating the orientation of the parent grain 60° about the <111> axis. For a coherent twin boundary (CTB) [86], the boundary plane is parallel to the {111} plane while an incoherent twin boundary has a boundary plane different from the {111} plane. The energy of CTBs is about one order of magnitude lower than that of other boundaries including incoherent TBs. CTBs can be also referred as coincident Σ3 boundaries, meaning the reciprocal density of common lattice points in the two grains (Σ) is 3.

Coherent twin boundaries are of particular interest because they are low energy boundaries and do not constitute fast diffusion paths for electromigration (EM) mass transport. Also, the electrical resistivity of CTBs is negligibly small, about one order of magnitude smaller than other grain boundaries. The effect of grain boundary scattering on Cu resistivity is becoming important as line dimensions approach the mean free path for electron scattering (39 nm @ room temperature). The length fraction of CTBs was found to be only 0.5% (Figure 4.16) for 40 nm wide Cu lines, significantly reduced from 13% observed for 70 nm Cu lines. The population of CTBs was further increased to about

42% for 1.8 μm lines [84]. It is expected both the reliability and the RC delay of Cu nanolines will become worse with the interconnect scaling.

Interestingly, the decrease in the twin percentage with scaling was found to correlate with an increase in the strength of the {111} texture as illustrated in Figure 4.17. It has been reported annealing twins including {511}, {522}, {211}, and {322} textures form during thermal processing in Cu films [79]. As the twins develop, the texture strength necessarily weakens due to the presence of new orientations.

In this study, the concentration of twin-oriented grains was found to be a function of line geometry, tending to decrease as the line width decreases. In general, annealing twins develop during grain growth and are most prevalent in plated Cu grains where many individual grains show multiple twin sites [87]. Grain growth favors the reduction of general and low-angle boundaries to the benefit of twin boundaries, which confirms that the mobility of twin boundaries is relatively small. Furthermore, as strain energy increases in a growing grain, twins may be formed to relieve the pressure. It is likely that the stress/strain energy in the line drives the formation of coherent twin boundaries.

In wider Cu lines, the contribution of the strain energy to the total energy of the system overweighs that of the surface/interface energy. Therefore, ideally Cu {100} grains with the minimum stain energy will grow at the expense of {111} grains. This is confirmed by a recent x-ray micro-diffraction study on the change of the strain energy during recrystallization of electroplated Cu films [88]. It was found that in thick films {100}-oriented grains tend to grow preferentially, leading to more reduction in elastic strain energy in comparison to the decrease in surface energy produced by growth of the {111} grains. The elastic energy density deduced in this study is plotted in Figure 4.18. The difference of the elastic strain energy between {111} and {100} grains are quite high reaching about 302 GJ/m^3, which renders a direct transformation from {111} to {100}

grains difficult. As a result, twins are introduced to facilitate the reduction of {111} elastic strain energy. For example, the transition from {111} grains to {511} twins is about 79% of the energy relaxation for a direct conversion to the {100} grains. In addition, the formation of coherent twin boundaries can further reduce the grain boundary energy to ~0.03 J/m^3. In combination, the twinning process reduces the {111} texture strength as an efficient step to reduce of the overall strain energy density in the confined Cu line system [89]. This results in a large number of CTBs in wide Cu lines as shown in Figure 4.16.

For narrow Cu lines with a high surface/interface-to-volume ratio, the surface energy dominates in favor of growth of {111} grains. As discussed in the previous section, the intensity of the {111} texture greatly increases with downscaling where the sidewall growth of {111} grains become more dominant with increasing trench aspect ratio. Murray *et al.* [88] calculated the difference of elastic strain energy between {111} and {100} grains for Cu films as a function of line width with results plotted in Figure 4.19. They observed a crossover at the film thickness of 0.65 μm below which {111} grains will growth preferentially since the driving force from the surface/interface energy exceeds that from strain energy. In addition to the energetics, kinetics are important, particularly for ultra-fine Cu interconnects. The geometrical confinement in the Cu nanolines can further limit grain growth and thus the twin formation. Here grain boundary twinning is mainly induced by single-grain deformation during grain growth. Plastic deformation of Cu can become more difficult with decreasing grain size due to the Hall-Petch relationship. This further limits twin formation with interconnect scaling.

Table 4.4 Characteristics of grain boundaries (GB) and their associated energies [85, 86].

	Coherent ∑3 boundary	Incoherent ∑3 boundary	High angle boundary
Misorientation	60° <111> GB plane: {111}	60° <111>	> 10°
GB energy (mJ/m^2)	24	498	625

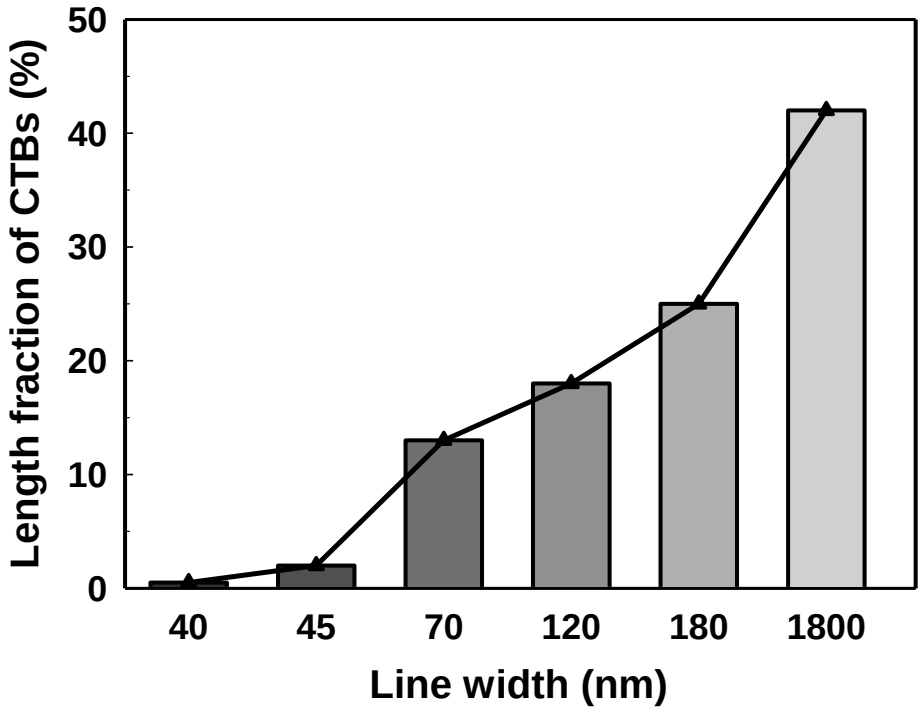


Figure 4.16 Scaling of the length fraction of coherent twin boundaries with Cu interconnects downscaling from 1.8 μm to 40 nm.

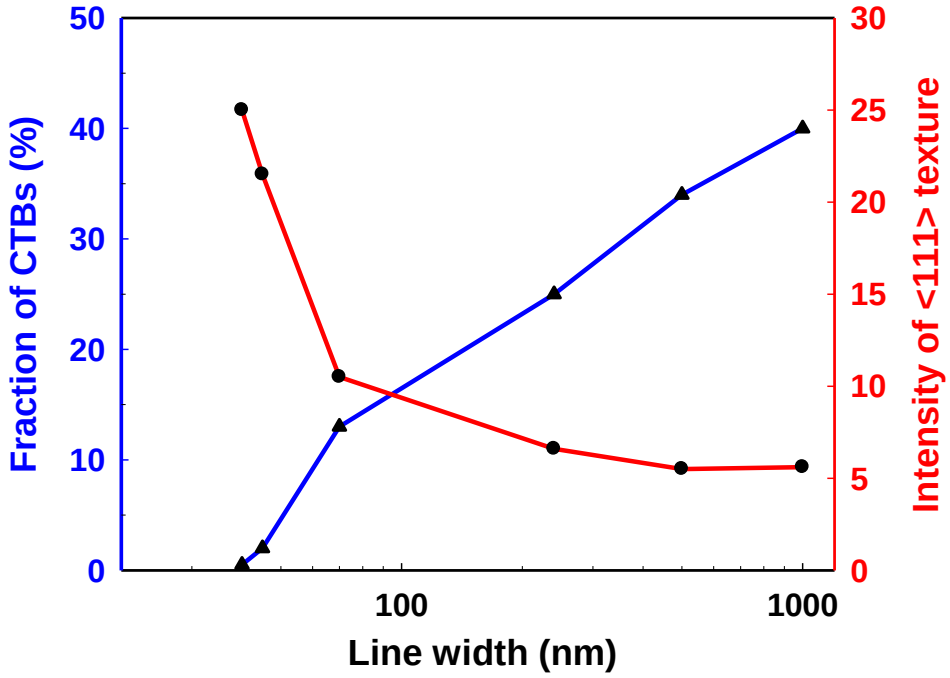


Figure 4.17 Scaling of the length fraction of coherent twin boundaries (CTBs) and the strength of {111} texture as a function of Cu line width.

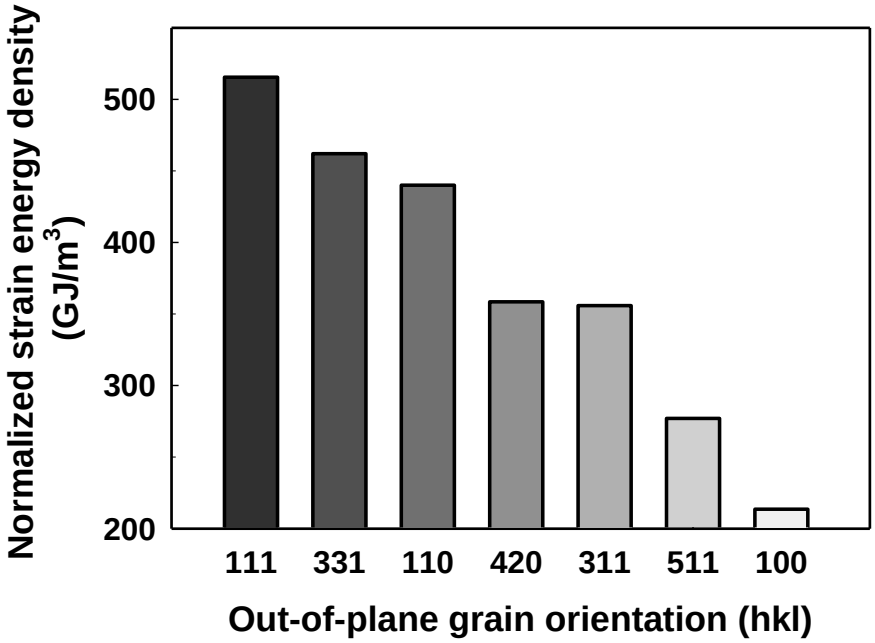


Figure 4.18 Normalized elastic strain energy calculated for grains with specific out-of-plane orientations [88].

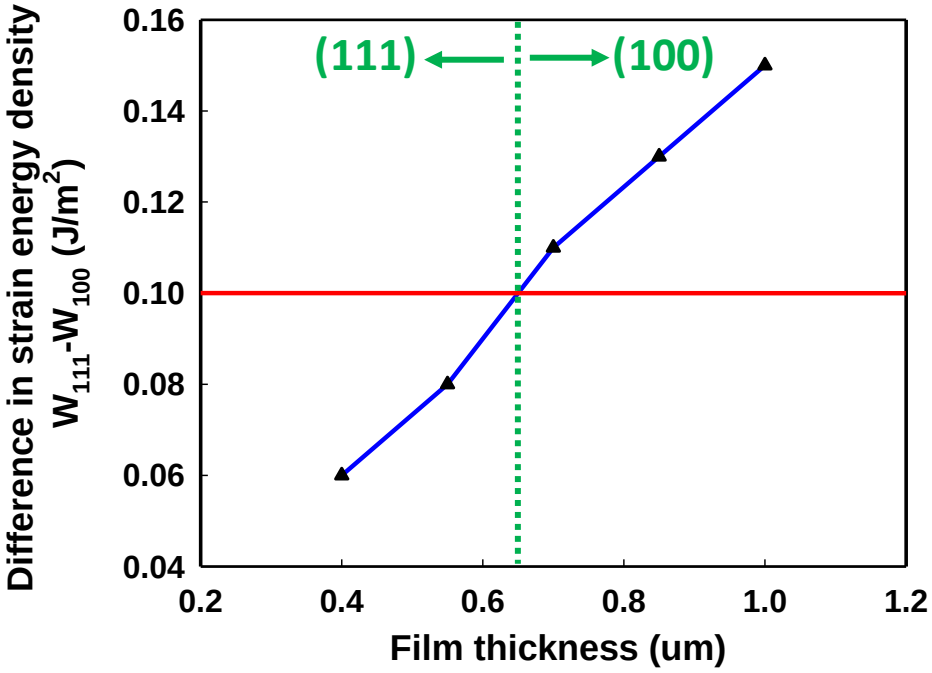


Figure 4.19 Calculated elastic strain energy difference between {111} and {100} grains for Cu films as a function of film thickness [88]. Surface energy difference between {100} and {111} grains at 300 K is plotted as the red line (including both top surface and bottom interface).

4.3.3.3 Scaling Effect on Grain Size

In addition to the texture and grain boundary data extracted from the PED analysis, detailed grain size data can be obtained using the image processing software, *e.g.* Image Pro. The results are reported in this section where the grain size is expressed as an equivalent grain diameter assuming a circular grain.

With scaling to sub-100 nm line width, the grain structure becomes polycrystalline with the emergence of small grains. In general, small grains are agglomerated to the lower half of the line mixing with near-bamboo grain sections in the line. To deduce reliable statistics, thousands of grains are required. The grain size

distributions of Cu lines with line widths of 40 nm, 45 nm and 70 nm are summarized in Figure 4.20 in a cumulative statistical plot, where the x-axis represents grain diameter in log-scale and the y-axis the cumulative probability scale. For example, about 70% of grains are smaller than 40 nm in diameter. The grain size distribution for the three line widths seems to follow a log-normal statistics but with a bi-modal grain size distribution at the lower bound starting at 40 %. This confirms an abnormal grain growth in Cu damascene lines during annealing. This correlates well with the evolution of the grain structures discussed earlier tracing to the minimization of the surface/interface energy vs. the strain energy. In the bimodal distribution of the small grains at < 40%, the grain size is generally smaller with decreasing line width. This indicates that with further downscaling, more small grains are pinned at the sidewalls and trench/via bottoms, as shown in Figure 4.13. Interestingly, Most of the small grains are separated by high-angle boundaries, which will increase the grain boundary contributions to electron scattering as well as mass transport under EM. This will increase the electrical resistivity and degrade EM reliability. For EM, these small grains can be detrimental if they are located at critical locations to induce flux divergence, particularly in a downstream EM configuration as shown in Figure 4.9. Also, with an increase in the population of small grains the average length of bamboo segments will shrink as observed in 40 nm and 45 nm lines where bamboo segments are barely observable. This will diminish their role as blocking boundaries and significantly weaken the short length effects and degrade EM reliability.

Finally, since about 70% of grains are smaller than 40 nm (the mean free path of copper at room temperature), the resistivity of Cu nanolines will increase dramatically beyond 22 nm node due to the additional contributions of surface and grain boundary scattering.

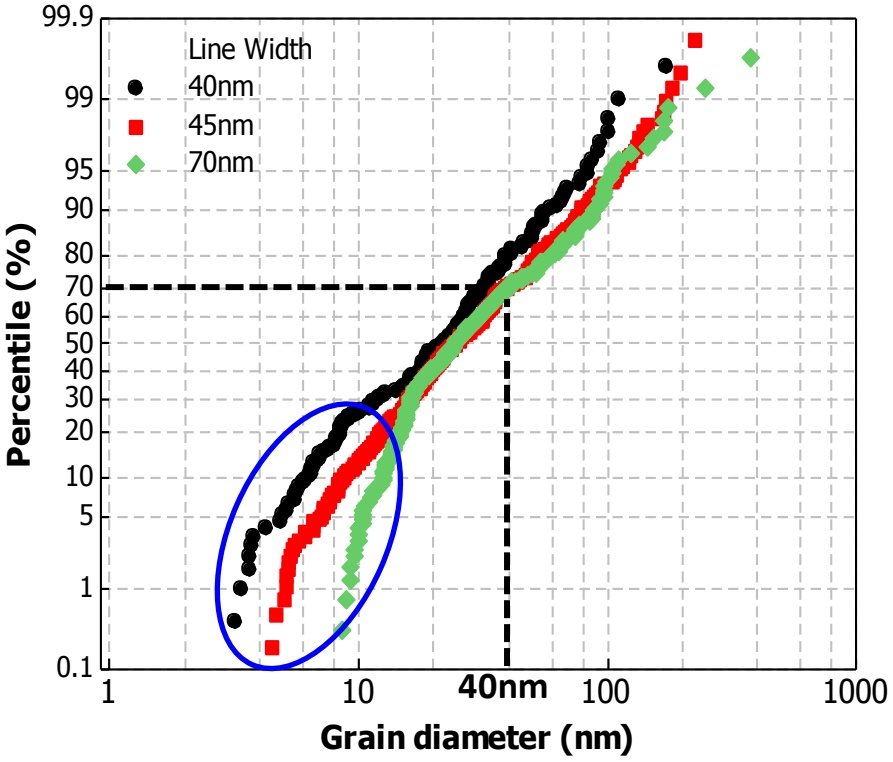


Figure 4.20 Grain size distributions of Cu lines with line widths ranging from 40 nm to 70 nm.

Chapter 5: Microstructure-based Statistical Modeling of Electromigration-induced Void Formation in Cu Interconnects

5.1 INTRODUCTION

The microstructure results obtained using the PED technique were used in a microstructure-based statistical model to analyze the grain structure effect on EM lifetime and statistics for Cu lines with CoWP capping. The purpose of this simulation is to establish a direct correlation between the microstructure of Cu nanolines, void formation kinetics, and EM statistics. The physical model was originally proposed by Korhonen *et al.* for Al interconnects [33, 90]. As discussed in Chapter 1, EM mass transport in Al interconnects is dominated by grain boundary diffusion since the top interface diffusion is strongly suppressed by Ti/TiN capping. This is very similar to the case of Cu interconnects with CoWP capping, except that Cu microstructure from electroplating is very different from Al interconnects.

The model is essentially formulated in three steps. First, the grain structure in the Cu interconnect is analyzed as a statistical series of N poly-grain clusters of length L. In each segment, voids can nucleate and grow under EM depending on the distribution of the flux divergent sites and the local mass transport. The second step is to evaluate the flux divergence in order to deduce the kinetic rate for void formation under EM in individual line segments. The flux divergence depends on the grain structure and thus the imbalance of the diffusion flux from grain boundary and interface in each cluster segment. Finally, the EM lifetime statistics for a Cu line with N segments connected in series is evaluated based on the weakest link approximation (WLA).

5.2 STRESS EVOLUTION IN CU INTERCONNECTS DURING EM

The grain structure in a Cu interconnect line is analyzed as a statistical series of poly-grain cluster and single-grain bamboo segments (Figure 5.1). Under EM stressing flux divergences arise due to the different diffusivities in cluster and bamboo regions (Figure 5.2). In a cluster segment the EM mass transport is mainly through grain boundaries (D_{gb}) while in a bamboo segment, the atomic flux is dominated by diffusion along the Cu/cap layer interface (D_i). For CoWP-capped Cu interconnects, D_{gb} is much larger than D_i due to the suppression of the interfacial mass transport. As a result, EM flux depletes Cu atoms via grain boundaries from the cathode end of a cluster and accumulates them at the anode end. Correspondingly, a back-stress gradient builds up locally within the cluster section.

As discussed in Chapter 1, the net atomic flux due to EM driving force and the stress-induced backflow can be described as

$$J = \frac{nD_{eff}}{kT}\left(Z^*_{eff} e\rho j - \Omega \frac{d\sigma}{dx}\right) \tag{5.1}$$

where $n = /\Omega$ represents the atomic concentration. In confined metal lines, the requirement of mass balance yields the governing equation for the stress evolution along the interconnect line during EM

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}[\kappa(\frac{\partial \sigma}{\partial x} + \gamma)] \tag{5.2}$$

where σ is the stress at time t and x is the distance along the line length. $\kappa = DB\Omega/kT$ is defined as the effective diffusivity and B is the effective bulk modulus. $\gamma = eZ^*\rho j/\Omega$

denotes the EM driving force. Equation (5.2) is very similar in form to the partial differential equation for diffusion. Accordingly, the solutions for Equation (5.2) can be deduced by replacing the conventional diffusion coefficient D with κ.

The stress distributions solved from Equation (5.2) are plotted in Figure 5.3 as a function of time. There exist 3 distinct stages during which EM-induced stress evolution occurs. At an early stage, a tensile stress begins to build up at the cathode end of a cluster and a compressive stress at the anode end. The variations of the tensile and compressive stresses are mostly constrained within the polygranular clusters. Stresses continue to rise within the clusters until a quasi-steady state is reached as represented by the solid lines in the cluster sections in Figure 5.3a. At that point, the stress-gradient-induced backflow exactly balances the EM mass transport. At intermediate times, significant diffusion into the bamboo segments takes place, without appreciable changes of the stress profiles in the clusters. Different from in the cluster segment, the stress gradient in the bamboo segment enhances EM atomic flux. As a result, the mass transport between clusters is activated by the build-up of the stress gradient in the bamboo section. At very long times, the stress coupling between clusters leads to substantially higher stresses than without cluster interaction until a linear steady state stress distribution is achieved throughout the entire line. In this simulation, clusters are assumed to act independently, which is close to the case for CoWP-capped Cu interconnects. If voids form at the cathode end of clusters (Figure 5.3b), stresses become essentially zero at the failure locations and a new equilibrium state will establish with compressive stresses distributed along the entire line. Additionally, process-induced thermal stresses can enhance void growth by stress-induced atomic flux. However, for simulation of EM behaviors under highly stressed conditions (*e.g.* 330 ^{o}C and 10 mA/cm^{2}), the effect of process-induced stresses can be neglected.

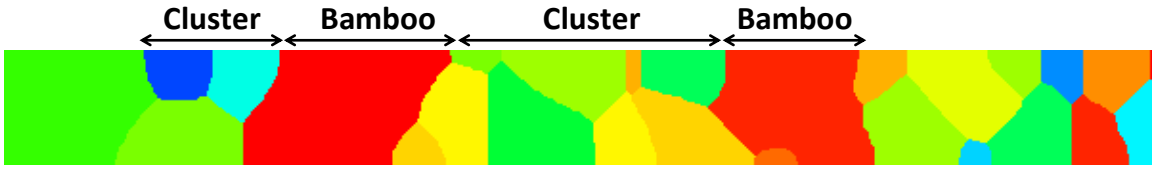


Figure 5.1 Color-coded grain orientation map of a Cu interconnect line composed of segments of clusters and bamboos connected in series.

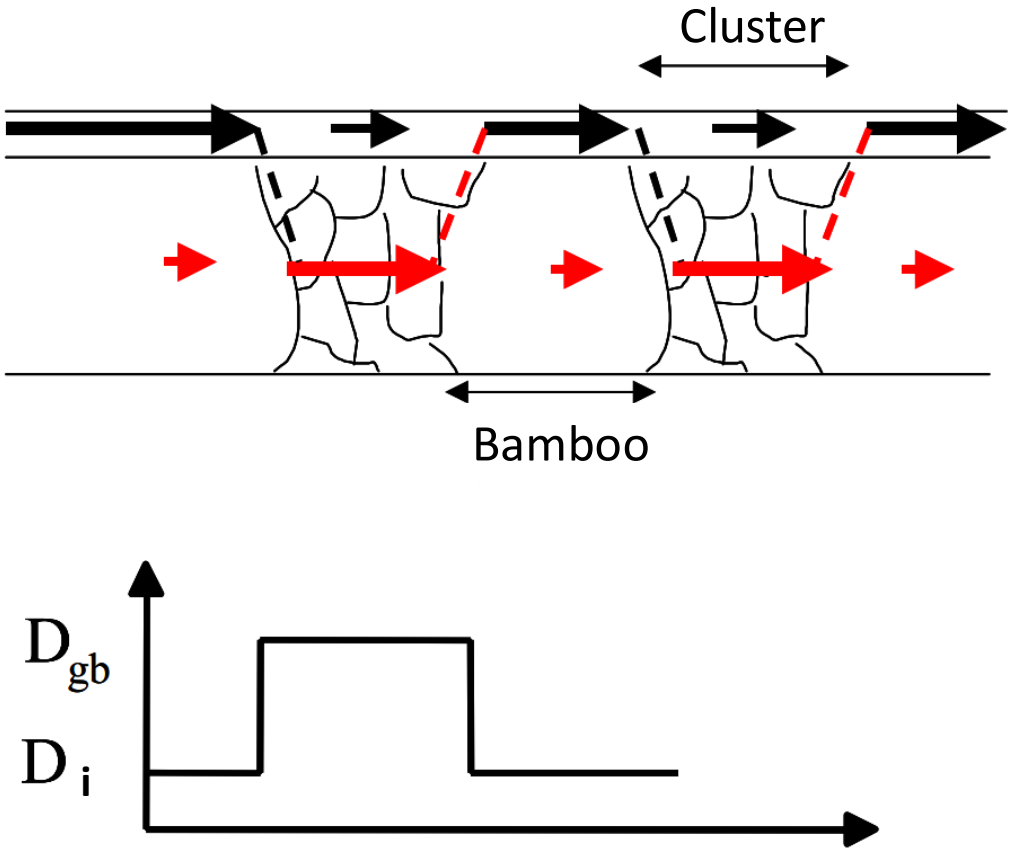
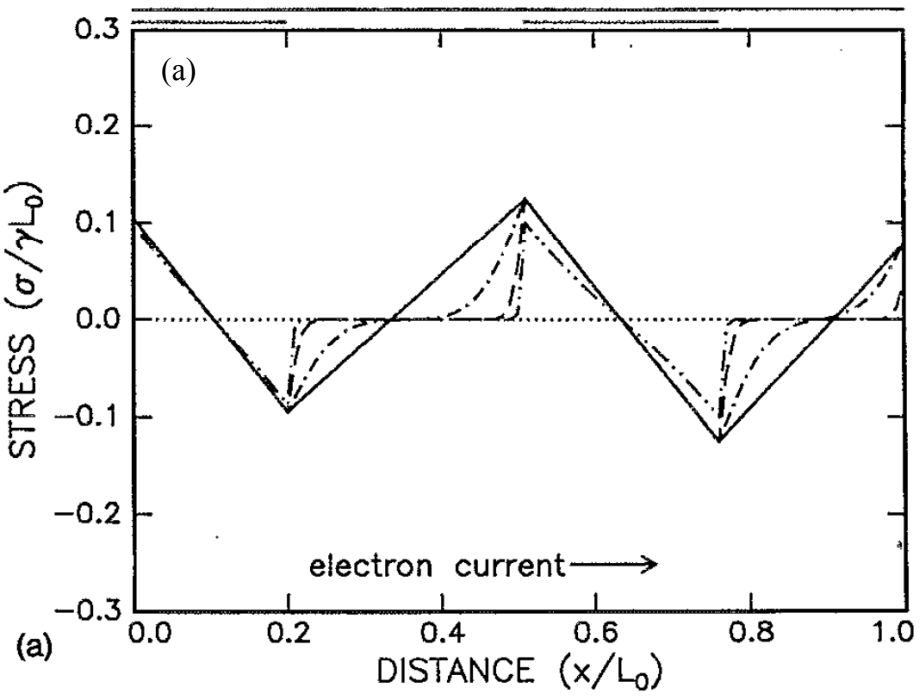


Figure 5.2 Schematic showing the dominant diffusion paths in cluster and bamboo segments.


(a)
0.3
0.2
0.1
0.0
−0.1
−0.2
−0.3
STRESS (σ/γL0)
electron current
0.0
0.2
0.4
0.6
0.8
1.0
DISTANCE (x/L0)
(a)

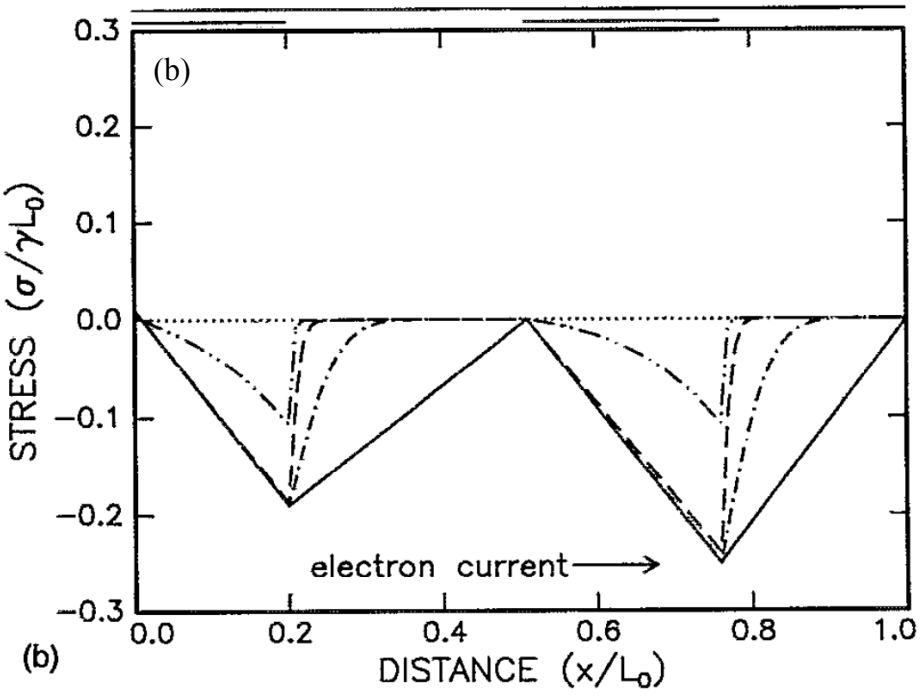

(b)
0.3
0.2
0.1
0.0
−0.1
−0.2
−0.3
STRESS (σ/γL0)
electron current
0.0
0.2
0.4
0.6
0.8
1.0
DISTANCE (x/L0)
(b)

Figure 5.3 Stress profiles of a Cu line consisting of cluster and bamboo segments at different stages of EM degradation: (a) before voids form, (b) after voids form at the cathode end of the cluster segment. Solid lines represent the final stress distributions after reaching the quasi-steady state [90].

5.3 CORRELATION OF EM LIFETIME STATISTICS WITH CLUSTER LENGTH DISTRIBUTION

In the microstructure-based EM model, the failure mechanism is strongly dependent on the matching of the cluster length L to the critical cluster length L_c. If the poly-grain cluster is longer than the critical length L_c, grain boundary diffusion in the cluster can induce rapid void formation to reach a critical size V_c for the metal line to fail. In this case, the cluster segment becomes the weakest link, inducing an early failure. However, if the cluster length is shorter than the critical length L_c, void growth in the cluster alone is not sufficient to cause the interconnect failure. In this case, additional flux divergence from the neighboring bamboo segment is required to induce line failure. The involvement of the slow interfacial diffusion in the bamboo segment will result in a longer EM lifetime.

In long enough cluster segments, critical size voids can grow by GB diffusion alone ("GB controlled failure") [90]. Assuming a void is already nucleated at the cathode end of the cluster at zero initial thermal stress ($\sigma = 0$ at $x = 0$), the stress evolution along the cluster length L can be described as

$$\sigma(x,t) = -\gamma[x - 2L\sum_{n=0}^{\infty}(-1)^n \exp(-m^2\kappa_c t / L^2)\sin(mx/L)/m^2] \tag{5.3}$$

where κ_c is the effective diffusivity in the cluster segment and $m = (n+1/2)\pi$. Figure 5.4 illustrates how the normalized stress ($\sigma/\gamma L$) develops within the cluster towards the steady state. Eventually the maximum compressive stress $-\gamma L$ is attained at the cluster/bamboo boundary ($x/L = 1$).

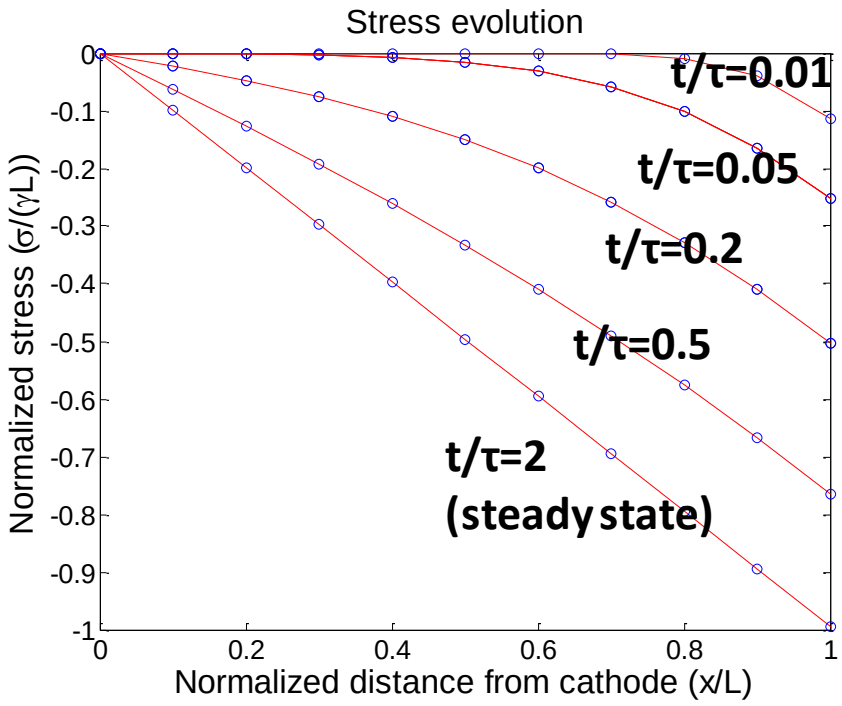


Figure 5.4 Evolution of the EM-induced back-stress in the cluster segment. τ is defined as $\tau = L^2/\kappa_c$.

The EM-induced void volume as a function of time can now be calculated by integrating the volumetric strain associated with the atomic redistribution during EM:

$$V(t) = (1/B)\int_0^L \sigma(x,t)dx \tag{5.4}$$

where *V(t)* is the void volume normalized by the line cross section for this one dimension model. For simplicity the stress σ is assumed to be hydrostatic and related to the volumetric strain through an effective bulk modulus *B*. *B* can be calculated based on the Eshelby theory of inclusions or by finite element analysis [91]. Substituting Equation (5.3) into Equation (5.4) gives

$$V(t) = \gamma L^2 / 2B[1 - 4\sum_{n=0}^{\infty}(-1)^n \exp(-m^2 \kappa_c t / L^2) / m^3] \tag{5.5}$$

Figure 5.5 illustrates how stress driven void growth proceeds during EM for cluster segments with different lengths. At initial stages void growth rates are very fast. For short clusters (*e.g.* L = 4.5 μm), further void growth becomes limited by the finite cluster length which cannot accommodate enough Cu atoms for the void to reach the critical size V_c. This can be calculated from the characteristic time to reach the saturated void volume $\gamma L^2/2B$ given by

$$t_L = L^2/\kappa_c \tag{5.6}$$

Accordingly, cluster segments as short as 4.5 μm will never fail when GB diffusion alone is involved. However, for long cluster segments, *e.g.* L = 180 μm, the void can reach the critical size V_c to induce line failure before the EM flux is totally balanced by the back stress gradient. In this case, the EM time to failure can be determined by substituting $V = V_c$ into Equation (5.5).

The critical cluster size L_c is a key parameter in this model and can be defined based on the critical void volume as $L_c = (2BV_c/\gamma)^{1/2}$. To develop a void on the order of 100 nm as observed in this study solely by GB diffusion in cluster segments, the segment

length must be longer than 12 μm which is not the case in this study as measured from the microstructure analysis. The values of the simulation parameters used in this calculation will be discussed later. Therefore, only the stress solution for clusters with lengths smaller than the critical length needs to be investigated for this study.

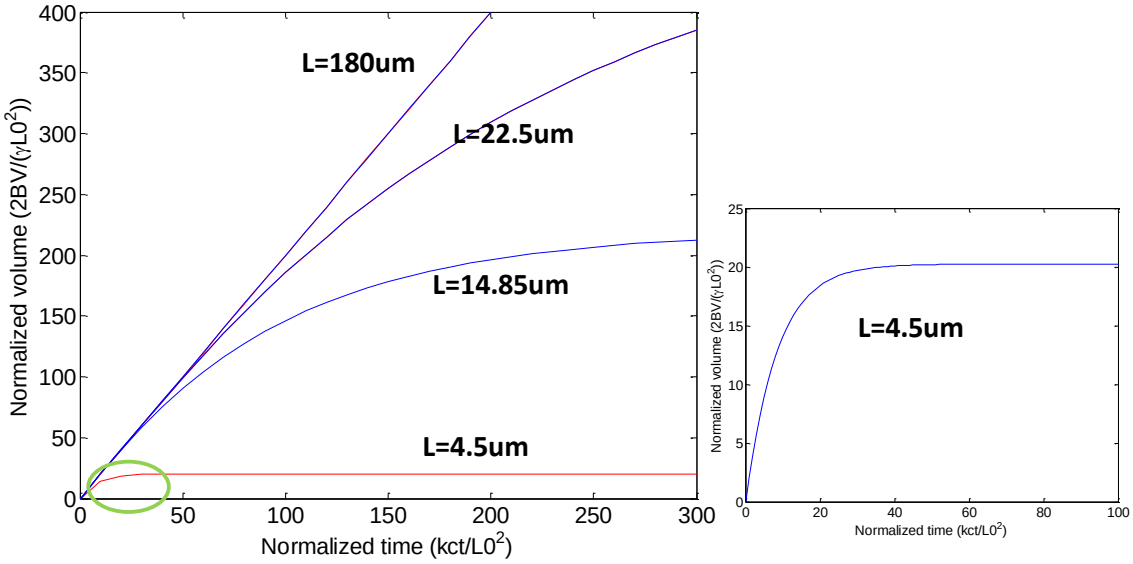


Figure 5.5 Void growth for clusters with different lengths. Normalized void volume ($2BV/\gamma L_0^2$) and normalized time ($\kappa_c t/L_0^2$) are used for simplicity. Length unit $L_0 = 1$ μm.

In the case of $L < L_c$, the bamboo section adjoining to the cluster segment has to be considered to account for the EM mass transport. The void growth rate is dominated by the leakage of atoms into the bamboo segment through interface diffusion, resulting in an "interface diffusion controlled failure" [90]. Since the diffusivity in the cluster segment κ_c is much faster than κ_b (*e.g.* $\kappa_b = 0.01\ \kappa_c$), stress distribution in the cluster reaches a linear steady state before any significant diffusion into the bamboo segments occurs (Figure 5.3b). The stress at the cluster/bamboo boundary ($x = L$) will essentially

remain at $-\gamma L$. Based on the analogy to heat conduction, the stress evolution in the bamboo sections can be deduced as

$$\sigma(x', t') = \gamma L \cdot erfc\left(x'/2\sqrt{\kappa_b t'}\right) \tag{5.7}$$

where κ_b is the effective diffusivity in the bamboo segments and x' represents the distance from the boundary of the cluster and bamboo segments with $x' = x - L$. $t' = t - t_L$ to count from the onset of the diffusion into the bamboo segment. Substituting Equation (5.7) into Equation (5.4) with the integration limit set from 0 to $L_b \approx \infty$ (cluster segments are treated as independent units separated by long bamboo segments as blocking boundaries), the additional contribution of the bamboo section to the void growth can be calculated as

$$V\left(t'\right) = \frac{\gamma L}{B}\sqrt{\kappa_b t'} \tag{5.8}$$

The total void volume due to the atomic diffusion in a cluster and its connecting bamboo can now be expressed as

$$V = V_L + V\left(t'\right) = \gamma L^2/2B + \gamma L/B\sqrt{\kappa_b t'} \tag{5.9}$$

EM failure will occur once the total void volume reaches the critical size V_c. Accordingly, the total EM time to failure for cluster segments with length $L < L_c$ is described as

$$t = t_L + t' = L^2/\kappa_c + \left(\frac{BV_c - \gamma L^2/2}{\gamma L}\right)^2 \Big/ \kappa_b$$

(5.10)

This formula establishes the relationship between the subcritical cluster length L, i.e. $L < L_c$ and EM failure time t. In this microstructure-based EM model, the lifetime t is strongly dependent on the two effective diffusivities κ_c and κ_b.

In this simulation, a cluster segment and its neighboring bamboo segment constitute a "failure unit". A Cu line can be viewed as independent failure units being connected in series. Based on the "weakest link rule" of statistics, it is the first EM failure from the weakest link that determines the lifetime of an entire line. If the probability that a single unit fails within t is denoted as $F(t)$, then the probability that an entire line composing of N units fails can be given by

$$F_N(t) = 1 - [1 - F(t)]^N$$

(5.11)

The weakest link approximation (WLA) predicts that the EM time to failure and its deviation decrease with increasing N.

In this study it is assumed that cluster segments are separated from each other by relatively long bamboo segments. Therefore the lifetime of a failure unit is predominantly determined by the cluster length alone. As shown in Equation (5.10), there exists a monotonic relationship between the lifetime t and the cluster length L. If $G(L)$ is defined as the cluster length distribution in the Cu line with a probability that a cluster length is smaller than L in the interconnect, then $F(t) = 1\text{-}G(L)$. The lifetime distribution of the line can then be expressed as:

$$F_N(t) = 1 - [G(L)]^N \tag{5.12}$$

Here Equation (5.12) provides the correlation between the lifetime statistics and the grain size distribution based on the WLA. Equations (5.10) and (5.12) provide the basic findings from the microstructure-based EM statistical model.

5.4 SIMULATION RESULTS

5.4.1 Cluster Length Distribution

The EM lifetime and its statistics of 45 nm node Cu interconnects with CoWP capping were evaluated using the microstructure-based statistical model. To illustrate the model, first the cluster length distribution was determined from the grain orientation mapping of Cu interconnects as discussed in Chapter 4. The poly-grain cluster length distributions extracted from the SG and LG structures are plotted in Figure 5.6. In general, they follow a lognormal distribution function $G(L;\mu,\sigma) = \frac{1}{2} erfc(-\frac{\ln L - \mu}{\sigma\sqrt{2}})$ with median lengths of 0.45 μm and 0.21 μm and σ values of 0.42 and 0.50, respectively. The SG structure has longer cluster segments compared to the LG structure due to the larger population of small grains. Since the cluster lengths for both structures are less than 1 μm ($< L_c$ = 12 μm), bamboo segments have to be included in the EM damage process.

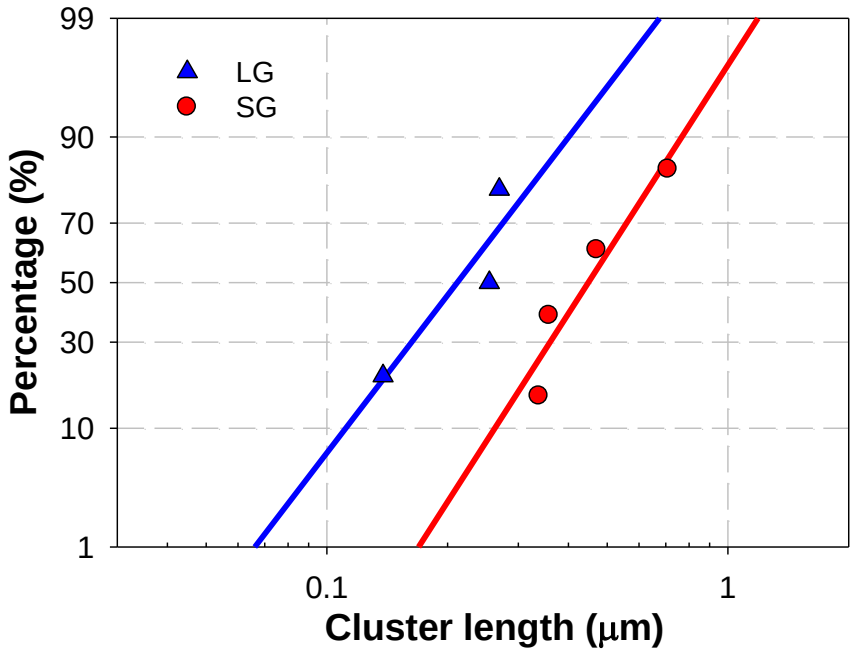


Figure 5.6 Cluster length distributions for the SG and LG structures with the lognormal fitting.

5.4.2 Interfacial Diffusivity κ_b and Grain Boundary Diffusivity κ_c

In this statistical study, the second step is to evaluate the void formation under EM in individual failure units. Effective diffusivities in cluster segments κ_c and in bamboos κ_b are two key parameters required to estimate the EM lifetime. Gupta *et al.* [92] have measured GB diffusivity in Cu poly-crystals as

$$D_{gb} = D_{gb0} \exp\left(-\frac{Q_{gb}}{kT}\right) = 0.058exp\left(-\frac{0.95}{kT}\right) \tag{5.13}$$

where D_{gb0} is the GB diffusivity pre-exponential factor (unit: cm^2/s) and Q_{gb} is the GB activation energy (unit: eV). For Cu interconnects stressed at 330 ^oC, D_{gb} is estimated to be $6.7x10^{-10}$ cm^2/s. This value agrees reasonably well with others [93, 94]. However, the

interfacial diffusivity in Cu has not been measured [95]. Based on the statistical model, the ratio of the interface and grain boundary diffusivities for Cu interconnects with the CoWP cap can be deduced. The procedure is first to calculate the EM lifetime predicted by the model as a function of the ratio of the interface and grain boundary diffusivities at the test temperature, and then determine the diffusivity ratio according to the measured EM lifetime. Diffusivity parameters determined in this way are summarized in Table 5.1. The critical void volumes V_c in the model were measured from TEM images of Cu lines after EM stressing, which are around 170 nm for SG structures and 110 nm for LG structures.

Table 5.1 Summary of parameters used in the simulation.

Parameter	Value
EM stressing temperature T (K)	603.15
EM stressing current density j (mA/um^2)	10
Effective bulk modulus B (GPa)	20
Atomic volume Ω (cm^3)	1.179e-23
Cu resistivity ρ (μOhm·cm)	3.94
Effective charge Z*	5

The results are shown in Figure 5.7a for the large grain structures using $N = 1$ in the model. This yields a ratio of 216, corresponding to κ_b of 1.8×10^{-12} cm^2/s. A similar calculation was carried out for the small grains structure which has a shorter EM lifetime.

The results are shown in Figure 5.7b yielding a κ_b of 2.3×10^{-12} cm^2/s. This value is in reasonable agreement with the large grain structures. Considering the experimental and modeling uncertainty, an effective diffusivity κ_b of 2.1×10^{-12} cm^2/s is obtained for the Cu/CoWP interface. This value is more than two orders of magnitude less than the grain boundary diffusivity, indicating that the CoWP cap is very effective in suppressing the interfacial mass transport.

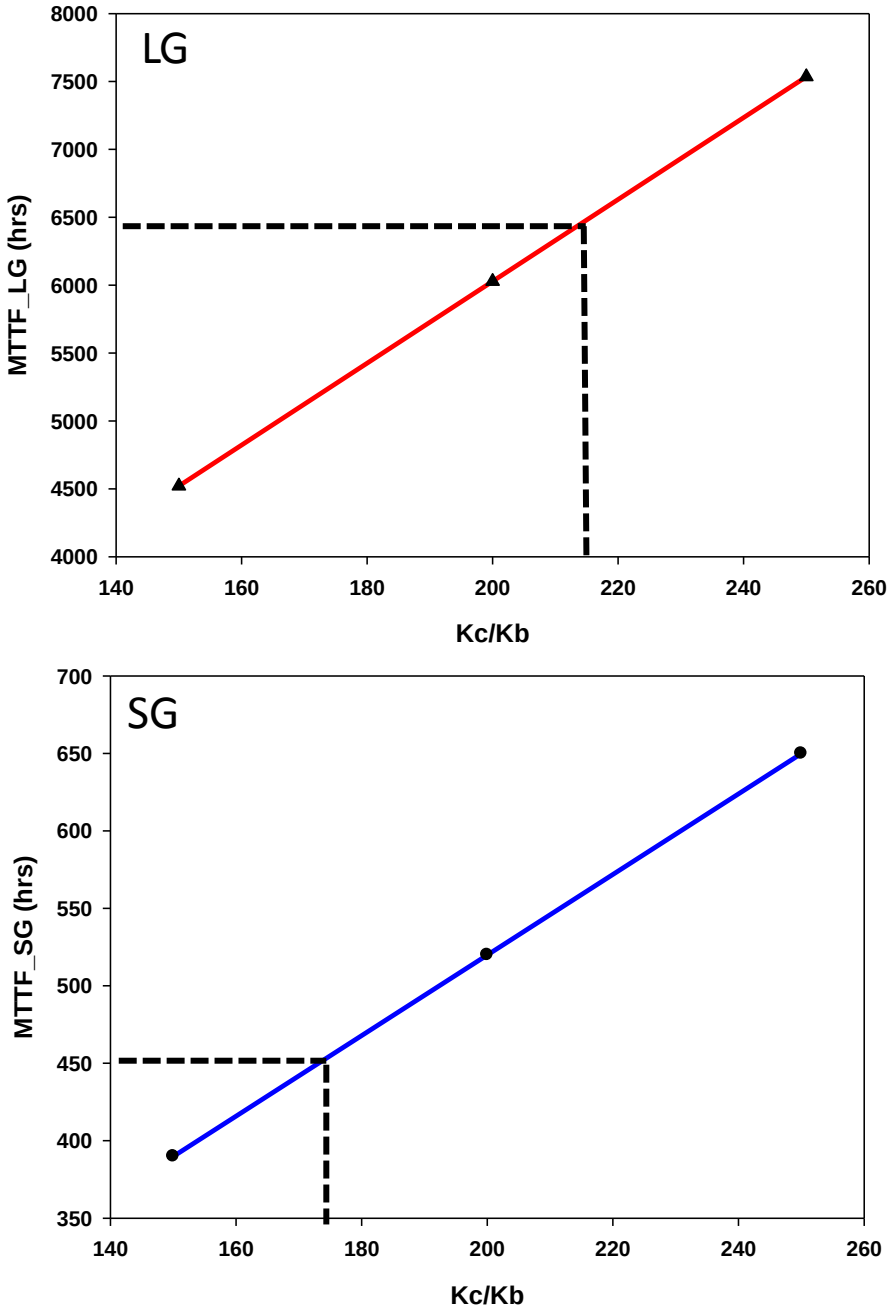


Figure 5.7 Simulated MTTFs of LG and SG structures as a function of κ_c/κ_b. Dash lines represent the κ_c/κ_b values determined from the experimentally measured MTTF values.

5.4.3 Statistical Simulation of EM Lifetime

Finally, the results obtained from PED analysis on cluster length distributions along with the deduced interface and grain boundary diffusivities were put into the statistical model to calculate the EM lifetime and statistics for SG and LG lines with CoWP capping. The cumulative distribution function (CDF) plots of the EM lifetime in Figure 5.8b from simulation agree well with the experiments shown in Figure 5.8a, especially for a small *N*. This suggests that only the few cluster segments adjacent to the cathode end of the line contribute to the void growth and the final EM failure. This prediction is confirmed by the experiments where voids are usually observed within a few grains adjacent to the cathode via to induce EM failure in CoWP capped samples. For the same grain structure, an increase in *N* decreases the lifetime but improves the statistical deviation, which is consistent with the prediction of the weakest-link statistics. The ratio of the extracted lifetimes for large and small grain structures and their respective sigma values are summarized in Table 5.2 and compared with the experimental results. Overall, the simulation results are in good agreement with experimental results, revealing that once the interface diffusion is suppressed by the CoWP cap, the effect of grain structure becomes significant. The longer EM lifetime and the larger statistical deviation for samples with the large grain structure can be attributed to the shorter average cluster length and a wider cluster length distribution. It is important to point out that the simultaneous increase in the EM lifetime and the statistical deviation for the LG structure may not lead to an improvement in EM reliability when extrapolated to the operating condition. In this case, a better control of Cu microstructure would be particularly important for improving EM reliability especially with further scaling of Cu interconnects.

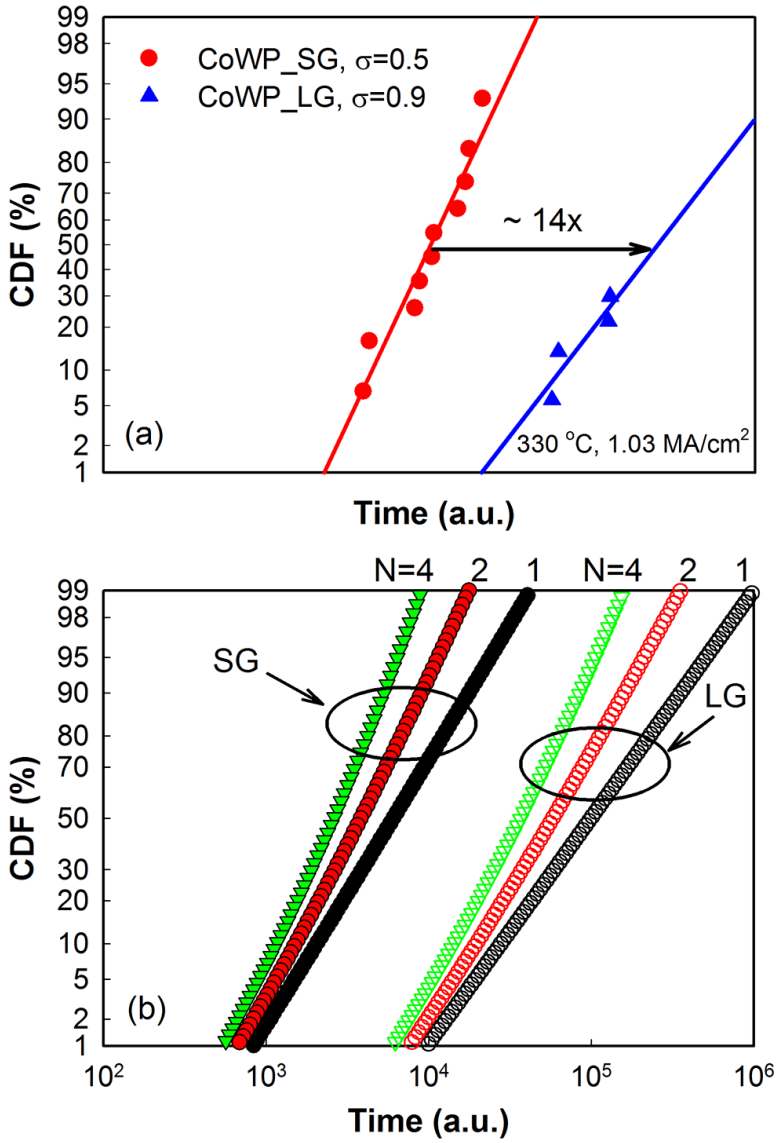


Figure 5.8 (a) Experimental results of EM lifetime distributions for CoWP capped Cu interconnects with LG and SG structures. (b) Simulation results of the same structures with varying *N*.

Table 5.2 Summary of simulation and experimental results of EM lifetime and statistics for LG and SG structures.

	Simulation		Experiment	
	LG (N=2)	SG (N=4)	LG	SG
Sigma	0.8	0.5	0.9	0.5
t_{50} Ratio (LG/SG)	16		14	

In summary, the grain structure statistics were taken into account in a microstructure-based model to identify the local critical flux divergent sites for void formation and to analyze the EM lifetime statistics. The analysis developed can be used to project the microstructure effect on EM reliability and provide a guideline for improving EM reliability as Cu interconnects continue to scale down in dimensions.

Chapter 6: Summary and Future Work

In this work, the evolution of Cu grain structure down to 40 nm was systematically studied using a high-resolution TEM-based orientation mapping technique. The effects of surface/interface energy over strain energy in controlling Cu grain growth were found to significantly increase with downscaling. Ultrafine Cu lines have a very strong {111} texture along the line length direction, accompanied by a very small percentage of coherent twin boundaries. Also the grain size is getting smaller and smaller with scaling, raising serious concerns about EM reliability and Cu resistivity. Short bamboos associated with small grain size for the 22 nm node and beyond are very detrimental and they will weaken the benefits of the short length effect.

With the establishment of a microstructure database for the electroplated Cu, the effects of Cu microstructure on EM reliability can be properly investigated. In this work, the EM reliability of Cu interconnects with metal capping and Mn alloying was studied by comparing their roles in EM lifetime improvement and their extendibility to future technology. CoWP was observed to improve EM performance up to 100x dependent on the grain structure while Mn is less sensitive to the variation in Cu microstructure and local defects. Therefore Mn alloyed seed layers provide a better solution for the ultrafine Cu interconnects. A good control of Cu microstructure is also necessary for maximizing its advantages.

A more direct correlation between microstructure and EM reliability was established in a microstructure-based physical model. EM lifetime statistics was found closely related to the distributions of poly-grain clusters. Cu lines with longer clusters tend to fail faster due to the predominant contribution of GB diffusion to the void growth. With further scaling, bamboo segments in between clusters are getting shorter. As a

result, the effects of cluster interaction become significant, which will accelerate the EM damage. The stress evolution with cluster interaction is an interesting topic for future study.

It is also important to understand the effect of scaling on Cu resistivity increase, particularly taking into account the grain boundary scattering. The microstructure information (including grain size and grain boundary properties) obtained in this work is very useful for establishing a microstructure-based grain boundary scattering model.

Furthermore, CVD Co [36] has been studied to replace traditional Ta/TaN liner for the ultrafine Cu interconnects. However, how the integration of Co in the barrier affects the Cu microstructure deposited on top and thus the resistivity of the Cu line remains unclear. The comparison of Cu grain structure with different barrier materials (*e.g.* Co vs. Ta) would be very helpful for the future development of Cu/low-*k* interconnects.

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