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Study of Initial Void Formation and Electron Wind Force for Scaling Effects on Electromigration in Cu Interconnects

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Study of Initial Void Formation and Electron Wind Force for Scaling Effects on Electromigration in Cu Interconnects

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Dissertation

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

Doctor of Philosophy

The University of Texas at Austin

May 2013

Dedication

To my family

Acknowledgements

It is a great pleasure for me to express my gratitude to many people for their support to this dissertation.

First of all, I would like to express my very great appreciation to Professor Paul S. Ho for his guidence and support throughout my doctoral work. I am deeply indebted to him and truly appreciate his constant encouragement and advising to my research.

I would like to thank other members of my committee, Professor Maxim Tsoi, Professor Chih-Kang Shih, Professor Rui Huang and Professor Zhen Yao, for their support and advice. I am particularly grateful to Professor Rui Huang for the helpful discussions in developing the stress model in Cu electromigration.

I would also like to thank Dr. Ki-Don Lee from Texas Instruments for providing test samples as well as patient discussions.

I would like to offer my special thanks to Dr. Junjun Liu for many patient discussions on the work of elctreon wind force. I also truly appreciate him for his valuable suggestions in general.

I would like to thank Xi Chen for his help in fluorescence microscopy of nanochannels.

I’m grateful to Dr. Jang-Hi Im for his help in my research and proofreading my dissertation. Special thanks to Ms. Jo Ann Smith for her administratvie support and help in the past few years.

My thanks are extended to my colleagues and friends in the Laboratory of Interconnect and Packaging including former members, Scott Smith, Bin Li, Zhiquan Luo, Junjing Bao, Huangliang Shi, Gary Lu, Xuefeng Zhang, Lijuan Zhang, Brook Chao, Soo Young Choi, Seung-Hyun Chae, Matthias Kraatz, Huai Huang, and current members, Qiu Zhao, Yiwei Wang, Linjun Cao, Tengfei Jiang and Laura Spinella for their help, collaboration, advices and discussions of my doctoral work. Special thanks to Zhiquan Luo for training me on semiconductor processes.

Finally, my great thanks go to my parents, my sister and my wife for their endless and unconditional love, trust, caring, understanding and patience.

Study of Initial Void Formation and Electron Wind Force for Scaling Effects on Electromigration in Cu Interconnects

Publication No._____________

Zhuojie Wu, Ph.D.
The University of Texas at Austin, 2013

Supervisor: Paul S. Ho

The continuing scaling of integrated circuits beyond 22nm technology node poses increasing challenges to Electromigration (EM) reliability for Cu on-chip interconnects. First, the width of Cu lines in advanced technology nodes is less than the electron mean free path which is 39nm in Cu at room temperature. This is a new size regime where any new scaling effect on EM is of basic interest. And second, the reduced line width necessitates the development of new methods to analyze the EM characteristics. Such studies will require the development of well controlled processes to fabricate suitable test structures for EM study and model verification. This dissertation is to address these critical issues for EM in Cu interconnects.

The dissertation first studies the initial void growth under EM, which is critical for measurement of the EM lifetime and statistics. A method based on analyzing the resistance traces obtained from EM tests of multi-link structures has been developed. The results indicated that there are three stages in the resistance traces where the rate of the initial void growth in Stage I is lower than that in Stage III after interconnect failure and they are linearly correlated. An analysis extending the Korhonen model has been formulated to account for the initial void formation. In this analysis, the stress evolution in the line during void growth under EM was analyzed in two regions and an analytic solution was deduced for the void growth rate. A Monte Carlo grain growth simulation based on the Potts model was performed to obtain grain structures for void growth analysis. The results from this analysis agreed reasonably well with the EM experiments.

The next part of the dissertation is to study the size effect on the electron wind force for a thin film and for a line with a rectangular cross section. The electron wind force was modeled by considering the momentum transfer during collision between electrons and an atom. The scaling effect on the electron wind force was found to be represented by a size factor depending on the film/line dimensions. In general, the electron wind force is enhanced with increasing dimensional confinement.

Finally, a process for fabrication of Si nanotrenches was developed for deposition of Cu nanolines with well-defined profiles. A self-aligned sub-lithographic mask technique was developed using polymer residues formed on Si surfaces during reactive ion etching of Si dioxide in a fluorocarbon plasma. This method was capable to fabricate ultra-narrow Si nanotrenches down to 20nm range with rectangular profiles and smooth sidewalls, which are ideal for studying EM damage mechanisms and model verification for future technology nodes.

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Chapter 1: Introduction

This chapter introduces the general background for the development of Cu interconnects. The increased complexity of the interconnect structures necessitates the studies of long term reliability such as electromigration (EM). Cu interconnects have unique EM characteristics originated from the damascene structure and its fabrication process. This chapter also provides a brief introduction of the EM phenomenon and the challenges to Cu EM reliability raised by interconnect scaling. This motivates the research work in this dissertation. The scope of the dissertation is outlined at the end of this chapter.

1.1 GENERAL BACKGROUND

For several decades, integrated circuit (IC) has distinguished itself by the rapid pace in scaling. Following Moore's law, the density of transistors on ICs doubles every 18 to 24 months. To meet this requirement, dimensional scaling occurs both in front-end-of-line (FEOL), where transistors locate, and back-end-of-line (BEOL), where metal interconnects are made to connect transistors. BEOL interconnects perform essential functions in an IC-system by providing clock signals, electrical signals, power distribution and ground distribution.

The scaling of ICs always comes with innovation of materials. The interconnect is no exception. When ICs were first produced, Al was used as interconnecting metallization due to its ease of deposition and etching. The resistivity of Al is 2.8 μΩ-cm, lower than that of most metals. The interconnect wires at that time were wide and thick and thus had low resistance. The resistance-capacitance (RC) delay of the Al interconnects was negligible compared to the switching delay of the transistors, also known as gate delay. As the device channel length shrinks during scaling, the transistors switch faster and faster. However, the interconnect wires become narrower, driving up the resistance so that interconnect RC delay becomes the bottleneck for the chip performance. For that reason, Cu was introduced to replace Al interconnects by IBM in 1997 [Edelstein *et al.*, 1997, Rosenberg *et al.*, 2000]. Cu has a lower resistivity of 1.7 μΩ-cm, considerably lower than that of Al.

The Cu interconnects in the advanced ICs have highly complex hierarchical structures. As an example, Figure 1.1 shows scanning electron microscopy (SEM) images of the interconnects of an Intel's 32nm high performance logic chip, where the whole structure contains 9 metal levels. The overall metal wiring structure follows the reverse scaling rule, where the lower-levels of the local interconnects employ thin Cu wires to match the size and pitch of the transistors in Si while wires with increasing dimensions are used in the upper-levels of global interconnects. Metallization following the reverse scaling rule is adopted to reduce the RC delay and power consumption.

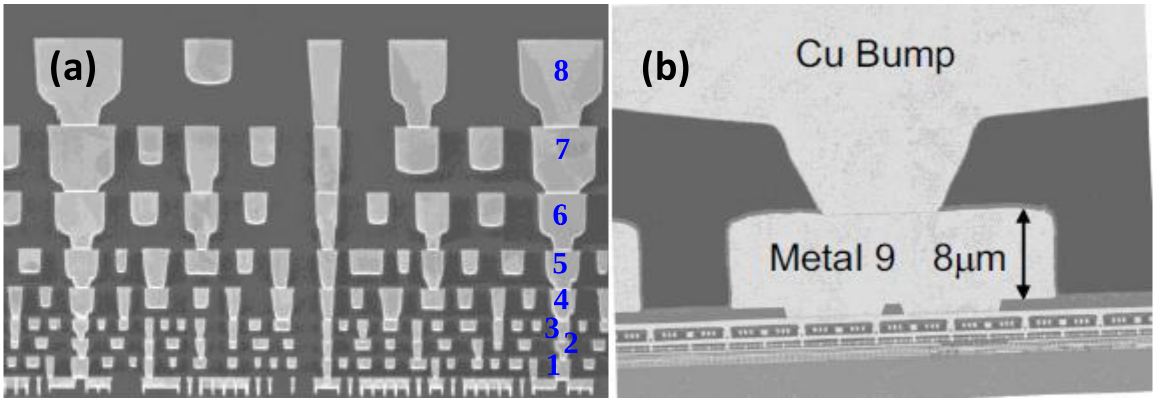


Figure1.1 SEM image of Intel 32nm interconnects (a) from metal-1 to metal-8 and (b) metal-9 to Cu bump. [Brain *et al.*, 2009]

As a result of the progressive scaling, billions of transistors and interconnects can now be packed into an advanced micro-chip. This poses increasing concern in the reliability of ICs. The failure of one out of billions of units in a micro-chip may cause the failure of the entire chip. The BEOL reliability is generally assessed by studying electromigration (EM), stress induced voiding (SIV) and time dependent dielectric breakdown (TDDB). With the aggressive scaling of metal line dimensions and density, EM and TDDB are becoming increasingly important reliability concerns. Chip package interaction (CPI) is also an important reliability problem if the full IC-system is considered. This dissertation studies the EM of Cu interconnects. The local interconnects in metal-1 (M1) and metal-2 (M2) levels are more subjected to EM damage due to much smaller dimensions and higher current density.

Compared to Al interconnects, Cu interconnects have the advantage of a higher resistance to EM. EM is a diffusion process, the activation energy of which scales with the melting temperature of the material. Cu has a higher melting point of 1083°C compared with Al of 660°C. At a given temperature, the diffusion in Cu is thus reduced compared with Al.

1.2 THE DAMASCENE PROCESS

Besides the improved performance of RC delay and EM, Cu has other properties very different from Al, which requires a different process to fabricate and to implement the interconnects. The processes and integration scheme in turn greatly affect the EM characteristics of Cu interconnects.

First of all, there is no good dry etch process for Cu due to the lack of volatile Cu compound at low temperature. A prerequisite requirement for the dry etch process is that the main etching byproducts should be volatile at low temperatures. For example, the chlorine plasma reacts with Al, forming $AlCl_3$. $AlCl_3$ sublimates at 178°C [Plummer *et al.*, 2000], i.e., volatile at a low temperature. Ion bombardment can then easily remove $AlCl_3$ from the surface and pump it out of the system. Therefore, a subtractive reactive ion etching (RIE) process can be employed to fabricate the Al interconnects, as shown in Figure 1.2(a). In the fabrication process, the patterning by photolithography is first performed on an Al film. Then the RIE process is used to form Al wiring structure which is followed by a subsequent dielectric deposition process to insulate the Al wires. Finally, a chemical mechanical polishing (CMP) process is used to planarize the dielectric layer to complete one level of Al interconnect.

In comparison, the sublimation temperature for CuCl is 1490°C [Plummer *et al.*, 2000], due to a tight binding of CuCl with the surface. It is difficult to remove CuCl from the surface even with ion bombardment and thus no good dry etching process is available for Cu. Instead, a different "damascene" process is used to fabricate Cu interconnects, as shown in Figure 1.2(b). First, the photolithography and RIE process are performed on the dielectric layer. The alignment of photolithography on the transparent dielectric film is easier than on the opaque and shiny metal film. However, the RIE of low-k dielectrics turns out to be difficult since it is prone to plasma damage in the RIE process. The low-k dielectrics were introduced to replace SiO_2 to further reduce the RC delay, crosstalk noise and power consumption of the interconnects but can be easily damaged by plasma processing [Baklanov *et al.*, 2012, Shi *et al.*, 2008]. After the patterning of the dielectric layer, Cu is electroplated into the via and trench openings on the dielectric layer. In a single damascene process, the vias and trenches are patterned and electroplated in separate steps. In a dual damascene process, the electroplating of Cu into the vias and the trenches are performed simultaneously. The dual damascene process not only simplifies process steps, but also decreases the via resistance and improves the EM reliability. Therefore, it is widely used in most of the advanced ICs.

Another undesired property of Cu is its high diffusivity in Si and silicate dielectrics, which can cause electrical leakage between adjacent Cu lines or TDDB of the dielectric. The Cu in the active Si can create deep trap states thus degrades the device performance. To prevent the potential out-diffusion of Cu, a barrier, also called a liner, has to be formed before the Cu seed layer deposition and electroplating, as demonstrated in Figure 1.2(b). Besides the capability of blocking Cu diffusion, the candidate material for the barrier must have low diffusivity itself and adhere well to the low k dielectric material. Low resistivity is also required to reduce RC delay. Tantalum (Ta) with melting temperature of 3020°C fulfills these requirements. The body-centered cubic (BCC) α-Ta has a resistivity of 15-50 μΩ-cm [Baklanov *et al.*, 2012]. Cu also has a fairly low surface diffusivity on α-Ta, 2.0×10^{-12} cm^2/s at 550°C [Fillot *et al.*, 2007]. To improve the adhesion between the Ta barrier and the low-k dielectric, a TaN layer is usually buffered in between. The Ta/TaN bilayered diffusion barrier is deposited using a physical vapor deposition (PVD) process.

The electroplating of Cu starts from the trenches and the surface of the dielectric layer simultaneously. An overhang of Cu, also called overburden, forms after the trenches are filled. Then a low temperature annealing (150-250°C) is performed to promote the Cu grain growth to stabilize the Cu microstructure. By comparison, the annealing of Al interconnects is performed on the Al thin film. This leads to different microstructures for Cu and Al interconnects.

While Al has a stable native oxide Al_2O_3 as a good passivation layer, the easily oxidized Cu surface is not passivated well by the unstable oxide layer. Therefore, a capping layer, such as SiN_x is applied, by plasma-enhanced chemical vapor deposition (PECVD), to the Cu surface after it is planarized by CMP. This capping layer also functions as an etch stop for the patterning on the dielectric layer. Carbon can be added to form SiC_xN_y to reduce the dielectric constant of this layer [Prasad *et al.*, 2002], but with the risk of decreasing the adhesion with Cu [Wang *et al.*, 2006]. As a result, the Cu/cap interface becomes a major diffusion path in Cu interconnects [Vairagar *et al.*, 2005].

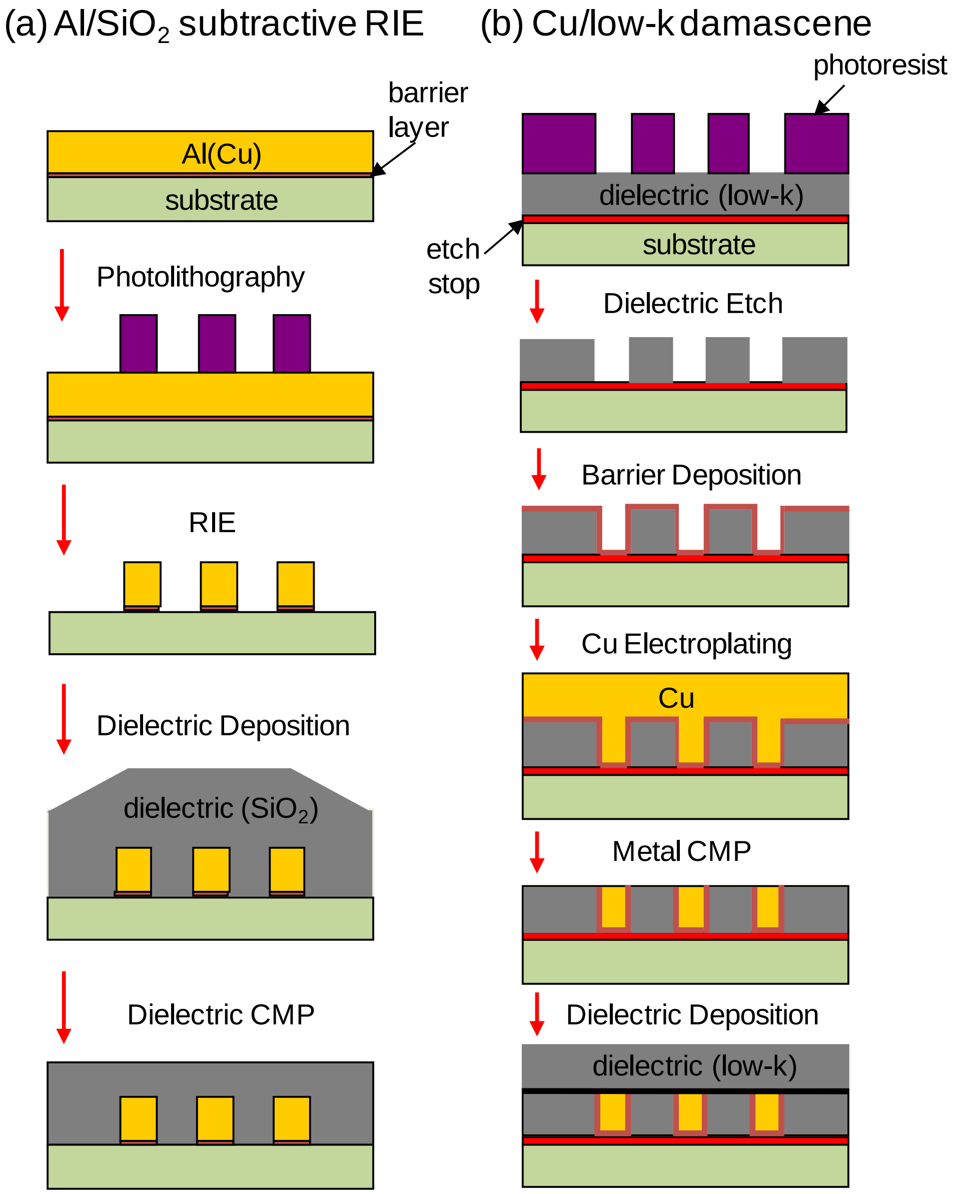

(a) Al/SiO_2 subtractive RIE
(b) Cu/low-k damascene
barrier layer
Al(Cu)
substrate
Photolithography
RIE
Dielectric Deposition
dielectric (SiO_2)
Dielectric CMP
photoresist
dielectric (low-k)
etch stop
substrate
Dielectric Etch
Barrier Deposition
Cu Electroplating
Cu
Metal CMP
Dielectric Deposition
dielectric (low-k)

Figure1.2 Schematic diagrams of (a) conventional RIE process for Al interconnects and (b) damascene process for Cu interconnects.

1.3 EM IN CU INTERCONNECTS

EM describes a mass transport process where metallic ions are driven by an electron current. Accelerated by the electric field, the electrons collide with an ion near a lattice vacancy as illustrated in Figure 1.3. The momentum transfer in the collision gives rise to an "electron wind" force, driving the atom to diffuse along a diffusion path, resulting in EM. The EM driving force F_{EM} excreted on the ion is composed of two parts: the electron wind force F_{wind} and the direct force F_{direct} from the applied electric field. F_{wind} and F_{direct} have opposite directions. In materials such as Cu, the wind force dominates and the F_{EM} can be expressed as:

$$F_{EM} = F_{wind} + F_{direct} \approx F_{wind} = Z^{*} e \rho j \,, \tag{1.1}$$

where Z^{*} is the effective charge number, e the electron charge, ρ the resistivity of the conductor and j the electric current density.

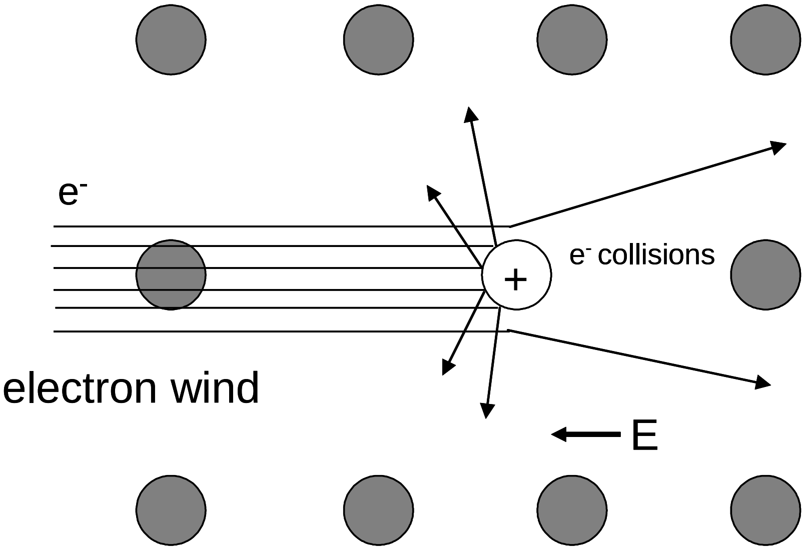


Figure 1.3 Schematic of the collisions between the electron wind and an metal ion. With the electric field E, electrons collide with metal atoms in the electron flow direction resulting in EM phenomenon.

The first report of EM can be traced back to 1861, when Gerardin observed it in molten lead-tin and mercury-sodium alloy [Ho *et al.*, 1989]. EM received much attention only after the major semiconductor companies observed it as a failure mechanism for Al interconnects in the late 1960s [Lloyd, 1999, Ceric *et al.*, 2010]. For a short period of time, the existence of ICs was threatened by EM [Sello *et al.*, 1966, Tan *et al.*, 2007].

EM is a diffusion-controlled mass transport process, which is directly proportional to the atomic drift velocity v_d given by

$$v_d = \mu F \,, \tag{1.2}$$

where μ is the mobility of the ion and F is the driving force including F_{EM} and stress induced back flow force if any. The mobility is directly related to the diffusivity D of the metal ion through the Einstein relationship: $\mu = D/k_BT$. k_B is the Boltzmann constant and T the absolute temperature.

Atoms can diffuse along two major diffusion pathways in Cu interconnects: Cu/cap interfaces and grain boundaries, as demonstrated in Figure 1.4. In general, the diffusion along Cu/barrier interfaces is relatively slow and can be ignored. The effective diffusivity of a Cu line can be expressed as:

$$D_{eff} = \frac{\delta_N}{h} D_N + \frac{\delta_{GB}}{d} D_{GB} \,, \tag{1.3}$$

where the subscripts N and GB denote Cu/cap interface and grain boundary, respectively. δ is the effective width for corresponding diffusion pathways. h is the line thickness and d is the average grain size. For a line mostly composed of bamboo type grains, the diffusion along grain boundaries can be ignored as well.

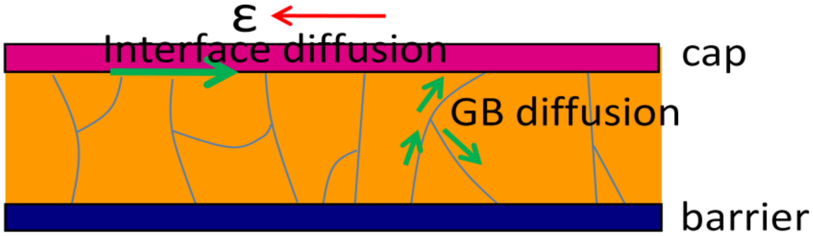


Figure 1.4 Schematic of major diffusion pathways in Cu interconnects.

The atomic diffusion itself does not necessarily lead to void formation. Voids only occur at flux divergence sites, where more atoms flow out and less atoms flow in. Such flux divergence sites are commonly located at geometric discontinuity points and grain boundary triple points. Figure 1.5 shows three possible flux divergence sites for Cu interconnects fabricated by dual damascene process. In this example, electrons flow from metal-1 (M1) through via-1 (V1) to metal-2 (M2). Voids are commonly observed at the cathode end of M2 line, where the supply of atoms is blocked by the Cu/barrier interface although the atoms can diffuse out freely through the Cu/cap interface. Process defects generated on the upper surface of the Cu line by CMP process also makes this site more prone to void formation. Voids within the vias are more often observed in the initial process development stage, when the via fabrication process has not been optimized.

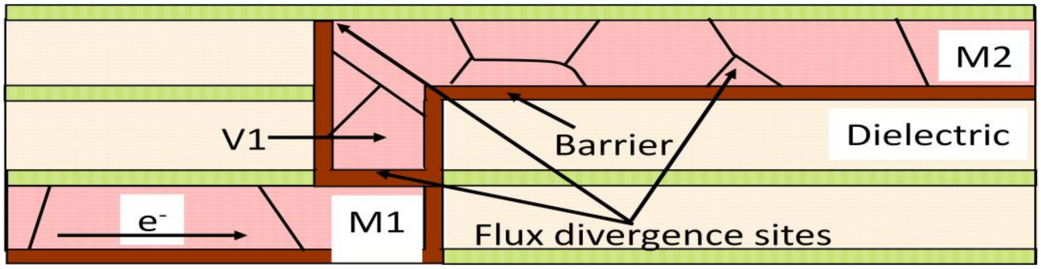


Figure 1.5 Schematic showing flux divergence sites in a Cu interconnect [Ogawa *et al.*, 2002].

The initial void formation at the Cu/cap interface can also be observed in the resistance versus time trace recorded during EM tests, as shown schematically in Figure 1.6. The trace first appears as a flat region when an initial void forms at the Cu/cap interface with a very small increase in the line resistance. An abrupt jump in the line resistance is usually observed when the void is large enough to fail the line. This is followed by a region with gradual resistance increase when the void continues to grow after the line fails.

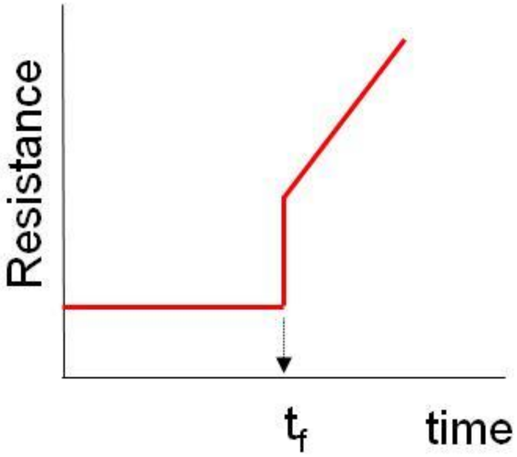


Figure 1.6 Resistance trace for EM of Cu interconnects including a flat region, an abrupt jump and a gradual increase region.

1.4 SCALING CHALLENGES TO CU EM

The scaling of transistor and interconnects continues to further improve the chip performance and reduce the cost per function. However, beyond the 22nm technology node, the scaling of interconnects becomes extremely difficult. One of the problems comes from the resistivity increase of Cu due to increasing sidewall scattering of the conducting electrons as the line width continues to be reduced. So far, the solution to mitigate the impact of this size effect has yet to be discovered. Together with the scaling of Cu line width, the barrier thickness also scales down accordingly to reduce the resistance. It is very challenging to form a barrier of only several monolayer thick, but maintaining the barrier function to block the out-diffusion of Cu. Reliability challenges are becoming an important limiting factor as well. Aware of the difficulty, some semiconductor companies are actually planning to use 14nm node FEOL mixed with 22nm node BEOL to meet the time-to-market requirement.

The most severe scaling challenge to Cu EM is that the EM lifetime is reduced approximately by half for each new technology node even with a fixed current density. This is demonstrated in Figure 1.7. The void at the cathode end of a line will cause line failure when its length ΔL_{cr} is longer than the via diameter which is about the line width w. The EM lifetime is proportional to $\Delta L_{cr}/v_d$. When the interface diffusion through Cu/cap interface dominates, the drift velocity scales with $1/h$ as indicated in Equation (1.3). Therefore the EM lifetime scales with $w*h$ if the current density j is constant. Since both line width and thickness are reduced by 0.7x drop each generation, the EM lifetime decreases by half for each technology node. The experimental data points for various nodes, represented by the open circles in Figure 1.7, agree well with the prediction by this simple scaling model.

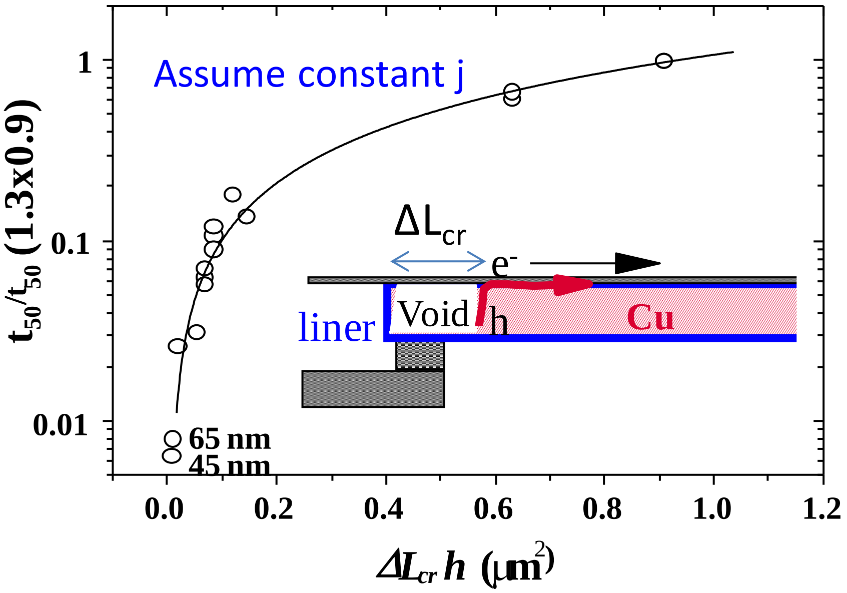


Figure 1.7 Normalized EM lifetime as function of critical void dimensions for various technology generations. [Hu *et al.*, 2006]

The situation is even more severe if one takes the scaling of current density into account. Figure 1.8 shows the evolution of J_{max} and J_{EM} in conventional Cu interconnects. J_{EM} is the maximum current density which meets the targeted EM lifetime requirement. It scales down with $w*h$. J_{max} is defined by the maximum equivalent DC current expected in a digit circuit divided by the cross-sectional area of an intermediate interconnect line. It keeps increasing not only because the cross-section of the line is decreasing, but also because the high performance device requires a larger drive current. FEOL devices are now in transition from planar transistors to FinFETs which can carry much larger current. This poses even more difficult scaling challenge to EM reliability.

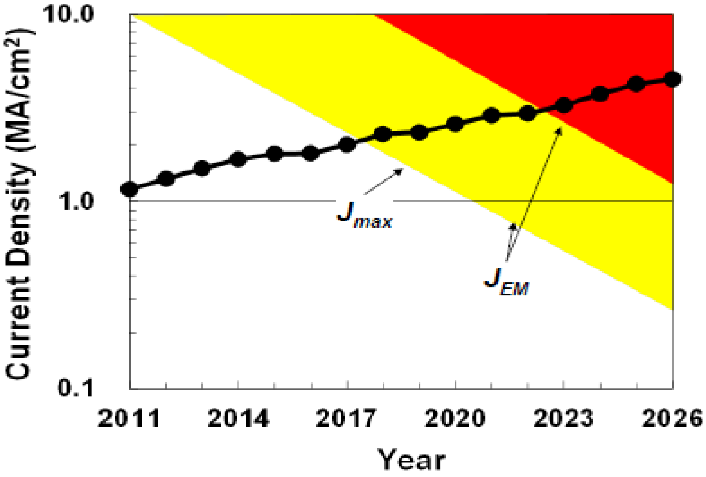


Figure 1.8 Evolution of J_{max} (from device requirement) and J_{EM} (from targeted EM lifetime). [ITRS, 2011]

Bamboo type grains are commonly observed in Cu interconnects prior to 65nm node. However, at 65nm node and beyond, the Cu lines in interconnects are usually composed of a mixture of bamboo and polycrystalline grains [Zhang *et al.*, 2007, Steinhogl *et al.*, 2005, Hu *et al.*, 2007a]. The grain boundaries associated with such grain structures provide additional diffusion pathways, and thus reduce the resistance to EM [Hu *et al.*, 2007a]. Further scaling of line width introduces more small grains in the trench bottom [Kameswaran, 2011], which further degrades the EM performance.

Significant efforts have been taken in introducing new materials to Cu interconnects to improve the EM reliability. Approaches can be categorized into two directions: improving the Cu/cap interface and/or engineering the Cu seed layer. For the first approach, methods include inserting a metal capping layer, alloying Cu surface with Al and forming Cu silicides at the top surface. Among these, a CoWP metal cap deposited by electroless plating was found to be particularly effective in suppressing the diffusion at the Cu/cap interface [Christiansen *et al.*, 2011, Gambino *et al.*, 2006, Zhang, 2010, Hu *et al.*, 2004a]. This is due to the fact that Co can form a strong adhesive interface with Cu. However, this process is difficult to implement and it also degrades the TDDB performance of low-k dielectrics [Tan *et al.*, 2008, Chen *et al.*, 2010]. This prevents it from being adopted in advanced interconnects. For the approach of using a Cu seed layer, elements such as Ti, Al, Mn, Ge, Co have been added as dopants [Hu *et al.*, 2012, Nogami *et al.*, 2010, Christiansen *et al.*, 2011, ITRS, 2011]. Upon annealing, the dopants at the sidewalls can diffuse to the Cu/cap interface and segregate there to strengthen the interface. The dopants can also segregate at the grain boundaries, blocking the grain boundary diffusion. This approach is limited, however, by the electrical resistance increase induced by the Cu alloying process [ITRS, 2011].

1.5 MOTIVATION

The research performed in this dissertation is motivated by the challenges for the future scaling of the Cu interconnects beyond 22nm technology node. First, the ever decreasing line width and increasing number of new materials introduced require new methodology to be developed for Cu EM study. For example, EM-induced void formation is a problem of paramount importance and fundamental interest. Due to resolution limitation, it becomes more and more difficult to directly use SEM to investigate the void formation beyond 22nm node. In addition, EM and void formation are subjected to statistical variation and its investigation requires a large number of samples. It is also impractical to use transmission electron microscopy (TEM) to study the void formation, considering the effort required to prepare even a single sample for TEM observation. Therefore, it is highly desirable to develop a method to extract the void growth information based on analysis of EM data. Recently, it has been found that useful information for EM can be extracted from the resistance traces [Arnaud *et al.*, 2011, Doyen *et al.*, 2008, Federspiel *et al.*, 2007, Lamontagne *et al.*, 2010, Doyen *et al.*, 2007, Arnaud *et al.*, 2010]. However, the void growth rate deduced in these works seemed to have referred to that after EM failure, i.e., the gradual increase region in Figure 1.6. Clearly, the void growth at the flat region actually determines how fast a line fails, so extracting information from this initial void growth stage is more critical. To develop such an approach for studying EM will be the research focus of this dissertation.

Second, the dimensions of interconnect lines are now in a new size regime. The line width for M1 interconnects at 22nm node is 32nm. It is comparable to the electron mean free path which is 39nm for Cu at room temperature. It is well known that, in this so called classical size regime, the electrical resistivity increases significantly due to increased interface scattering and grain boundary scattering. The electrical resistance in a metal is caused by the scattering between electrons and atoms. As shown in Figure 1.3, the same scattering events also deliver momentum to the atom and cause it to migrate along the diffusion path. In this sense, EM closely correlates with electrical resistance. This raises an important question: Does a similar significant size effect exist on EM? It will be addressed in this dissertation as well.

Third, as scaling continues, the EM of Cu interconnects is more sensitive to small process variations. This is schematically illustrated in Figure 1.9. While a 10nm square notch causes 10% width variation in a 100nm wide line as shown in Figure 1.9(a), the notch with the same size accounts for 30% width reduction in a 30nm wide line as shown in Figure 1.9(b). A 30% reduction of line width may easily induce a different EM failure mode and early failures [ITRS, 2011]. Due to the random nature of process variations, the lifetime could yield different distributions for different sets of samples. This poses critical challenges for EM mechanism study. Such line edge roughness (LER) problem is expected to have more effect on EM reliability beyond the 22nm node, mainly because of lithography limitation. The current generation of optical lithography system with a 193nm wavelength source, combined with the optimization of computational lithography, reaches a resolution limit at 22nm node [ITRS, 2011]. The next generation lithography system using extreme ultraviolet (EUV) source with 13.5nm wavelength will not be ready for at least another two technology nodes. Therefore, it is of great importance to develop alternative processes to fabricate well-controlled Cu nanolines for investigation of EM mechanisms. Furthermore, due to the increasing difficulty in experimental study, modeling work is becoming more useful and important for Cu EM in advanced nodes. For simplicity in modeling, Cu line is commonly assumed to have a rectangular cross-section. However, an actual Cu interconnect line usually has a taped profile. It would be greatly valuable to have Cu lines with ideal profiles for model verification. Developing processes to fabricate such ideal test structures is also one of the objectives of this dissertation.

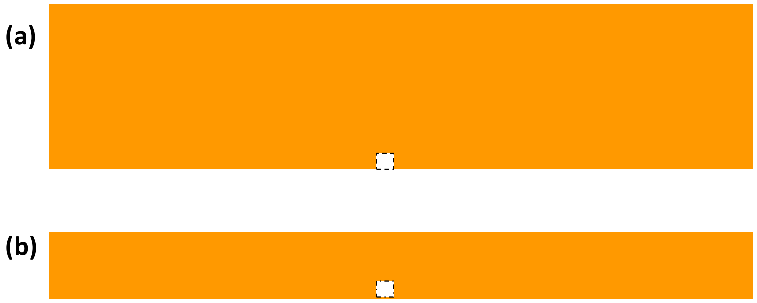


Figure 1.9 Schematic showing that narrower lines are more sensitive to process variations. (a) 100nm wide line with a 10nm square notch; (b) 30nm line with a 10nm square notch.

1.6 SCOPE OF THIS WORK

The work contained in this dissertation is organized into 6 chapters as follows:

Chapter 1 provides an introduction of Cu interconnects and challenges of Cu EM caused by interconnect scaling.

Chapter 2 investigates the EM induced initial void formation in Cu interconnects by analyzing the EM resistance traces. A method of resistance trace analysis is developed for this purpose. EM tests are performed with multi-link structures to extract the statistics of resistance parameters and the initial void growth rate.

Chapter 3 develops a void growth model based on the stress evolution in a Cu line under EM. The model is compared with the EM data presented in Chapter 2. Monte Carlo grain growth simulations based on the Potts model are performed to investigate the microstructure characteristics of a Cu line.

Chapter 4 studies the size effect of electron wind force for a Cu thin film and a Cu line. The dimensions under discussion are close to the electron mean free path of Cu.

Chapter 5 describes a process development for fabrication of Si nanotrenches for deposition of Cu nanolines with well-defined profiles. A method to use the polymer residues formed in fluorocarbon plasma as self-aligned sub-lithographic mask is developed.

Chapter 6 summarizes the research results obtained in this dissertation and suggests future studies.

Chapter 2: Electromigration Induced Void Formation in Cu Interconnects

This chapter studies electromigration (EM) induced void formation mechanism in Cu interconnects. A method was developed to investigate the kinetics of the initial void formation based on the analysis of resistance traces recorded during EM tests. EM tests were performed using multi-link structures to measure the EM failure time and their statistical distributions together with the resistance traces. The method of resistance trace analysis was applied to deduce the correlation of the void growth rates before and after line failure.

2.1 INTRODUCTION

Electromigration (EM) describes the diffusion of metal atoms in a metallic conductor driven by an electron current. For Al or Cu interconnects, the EM induced mass transport occurs along surfaces, interfaces and grain boundaries, moving in a direction from the cathode towards the anode. The local imbalance of the mass transport gives rise to flux divergence which can lead to void formation at the cathode or hillock growth at the anode of the interconnect structure [Bauguess *et al.*, 1996]. The formation of void or hillocks can result in circuit open and short failure at a rate depending on the interconnect dimensions, fabrication process and temperature. As device scaling continues to reduce the interconnect dimensions, the increase in the current density will accelerate the EM induced void formation rate, raising a major reliability concern for on-chip interconnects. For Cu interconnects, the mass transport is dominated by diffusion at the interface between the Cu line and the SiCN capping layer due to the relatively weak bonding in this interface. Defects generated on the upper surface of a Cu line by the chemical-mechanical polishing (CMP) process, also makes the Cu/cap interface most prone to void formation. This is schematically shown in Figure 2.1 (a) where void formation takes place at the interface. Figure 2.1 (b) shows that such a void was indeed observed by TEM at its initial stage and close to the interface. Such a void will continue to grow until it spans the whole cross-section of the Cu line and fails the interconnect line. This void formation mechanism as illustrated is different from that observed in Al interconnects where the Al interface is relatively defect free due to the presence of the natural aluminum oxide which is a good passivation layer. Instead, the voids usually form at grain boundary triple points in Al interconnects.

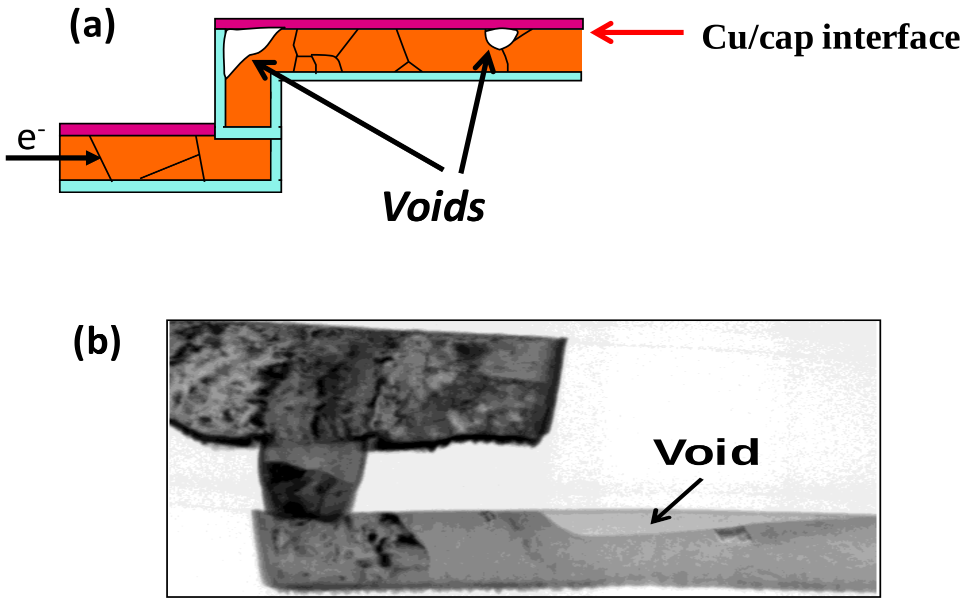


Figure 2.1 (a) Schematic showing voids formed at weak Cu/cap interface. (b) TEM image showing an initial void formed close to the interface [Zhang, 2010].

This unique feature of EM void formation for Cu interconnects is reflected in the resistance trace recorded during EM tests as a function of time. As shown in Figure 2.2, three stages are commonly observed in a resistance trace. Stage I is a relatively flat region when the voids are initially formed. The dominance of the interfacial mass transport renders the downward outgrowth of the void from the interface. During this stage, the resistance increase is usually quite small and barely detectable in the resistance trace. Once a void spans the whole cross-section of the Cu line, the electric current is forced to shunt through the resistive barrier layer. This causes line failure at Stage II and a steep resistance jump is observed in the trace. This is followed by a gradual resistance increase region at Stage III when the void further grows along the direction of line length. Clearly the first stage determines how fast the line fails. However, this most critical stage is least studied, perhaps because the resistance trace at Stage I remains nearly flat with no significant increase in resistance. It may also be due to the fact that there is no good model so far to analyze the initial void formation stage in Cu lines.

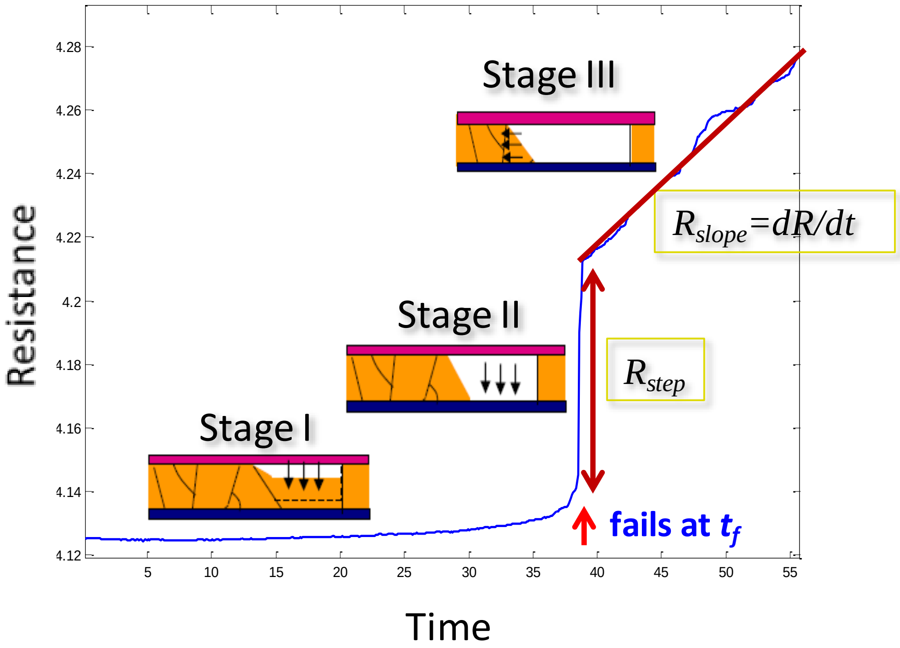


Figure 2.2 Typical EM resistance traces with definition of three Stages and the parameters R_{step} and R_{slope}.

One way to study the initial void formation at Stage I is to use in-situ SEM to observe the void during EM stressing [Liniger *et al.*, 2002, Vairagar *et al.*, 2005, Liniger *et al.*, 2003]. However, the continuing scaling in microelectronic devices makes such direct SEM observation impractical when the line dimension is close the spatial resolution limit of SEM.

Recently, a technique using a local sense structure close to the void is developed to detect the initial void growth rate at Stage I [Croes *et al.*, 2011, Kirimura *et al.*, 2012]. For a standard EM test structure, the voltage sense terminals are placed very close to the current injector so that the resistance of a long entire line is measured, as shown in Figure 2.3(a). Any resistance change caused by void formation in the line is relatively small compared to the line resistance. So the resistance trace does not provide enough sensitivity for observing void formation. In the newly proposed local sense structure, the voltage sense terminals are placed very close (only 10 μm away) to the via where void usually forms, as shown in Figure 2.3(b). In this way, the resistance change caused by void formation can be readily detected as a considerable portion of the resistance measured by the sensor. Figure 2.3(c) shows the increased sensitivity of such a local sensing structure. The drift velocity obtained by this technique at Stage I was found to be between 0.1 and 2 nm/h [Croes *et al.*, 2011]. In comparison, the drift velocity at Stage III has been reported to be larger from 0.1 up to 25 nm/h at 330°C. [Yokogawa, 2004, Doyen *et al.*, 2008, Lin *et al.*, 2010, Hu *et al.*, 2007].

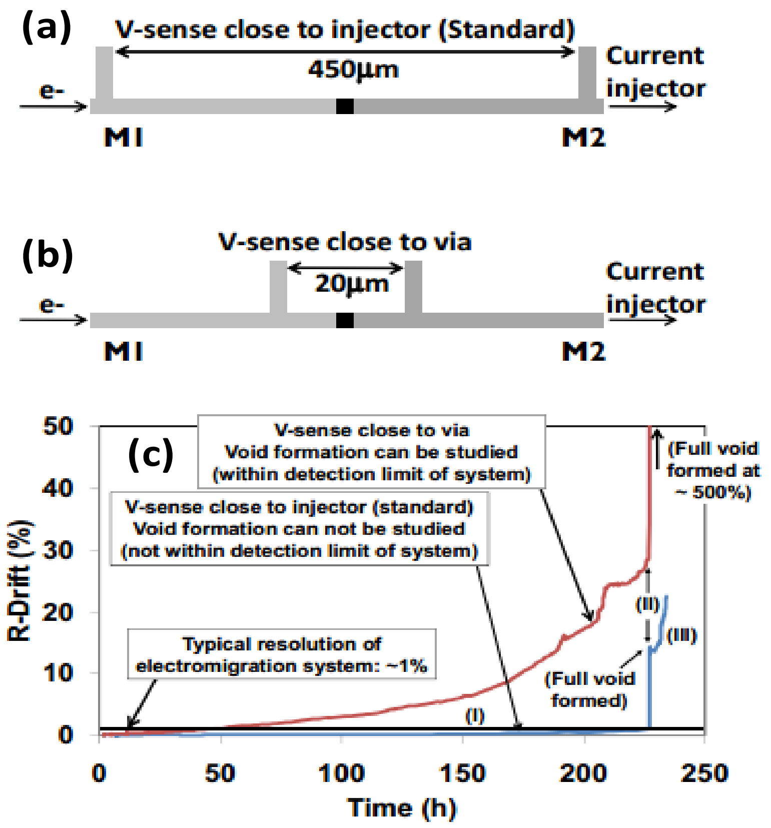


Figure 2.3 (a) Standard EM test structure with the voltage-senses close to the current injector; (b) New local sense test structure with voltage-sensors close to via; (c) Typical EM resistance traces when sensing at the injector/local senses. [Croes *et al.*, 2011]

However, such dedicated local structure requires extra fabrication efforts. In addition, being adjacent to the void, the presence of the local sensing structure may affect the void formation kinetics. Considering the fact that extensive experiments have been performed on EM with standard test structures, there is a need to develop a method to analyze the initial void growth behavior at Stage I with standard EM test structures. This is the goal of this chapter.

2.2 ANALYSIS OF RESISTANCE CHANGE INDUCED BY VOID FORMATION

For simplicity, a rectangular void is assumed. The void starts from the weak Cu/cap interface with an initial long slit shape growing downwards. After it reaches the bottom, the void further grows in the horizontal direction. Although the actual voiding behavior is more complex, this model catches the essential feature of EM voiding in Cu lines. Therefore it has also been used by other authors [Arnaud *et al.*, 2011, Lamontagne *et al.*, 2010]. Figure 2.4 shows the schematics for this voiding process.

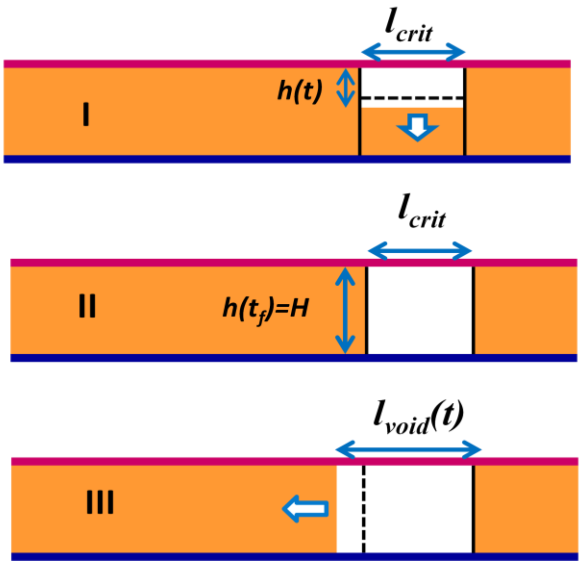


Figure 2.4 Schematics for the growth process of a rectangular void.

It is further assumed that the line failure time is dominated by void growth instead of void nucleation. This seems to be a reasonable assumption, since the CMP process, a unit process used to fabricate the damascene Cu interconnects, commonly induces significant amount of process defects on the upper surface of Cu lines. It is reasonable to believe that enough number of small voids have already been nucleated during subsequent annealing and room temperature storage. In this void growth dominated case, the failure time t_f can be calculated from the amount of material needs to be removed and how fast the material is removed.

$$t_f = V_{crit} / A * v_{d,I} = l_{crit} / v_{d,I} . \tag{2.1}$$

The time t_f is the measured failure time which is defined as the time corresponding to the first abrupt resistance jump in the resistance trace, as shown in Figure 2.2. In Equation (2.1), V_{crit} is the critical void volume causing line failure. l_{crit} is the critical void length. A is the line cross-sectional area. $v_{d,I}$ is the drift velocity at Stage I. Rigorously speaking, the drift velocity can only be applied to void growth by edge displacement mechanism, where the drift velocity is the velocity of the void front, which is also identical to the velocity of atom motion. As indicated in the schematic in Figure 2.2, the void growth at Stage I follows a grain thinning mechanism instead of an edge displacement mechanism as at Stage III. However, one can mathematically define an effective drift velocity based on the void growth rate. $v_{d,I}$ can be interpreted as the void growth rate at Stage I normalized by A.

Once the void spans the line cross-section, the electric currentis forced to shunt through the resistive TaN/Ta barrier layer. The resistance trace shows a steep jump with resistance increase R_{step}, as shown in Figure 2.2. The resistance of the failed line is equivalent to the resistance of two resistors in series: the remaining Cu line and the barrier in the void segment.

$$R = R_{Cu} + R_b = \frac{\rho_{Cu}}{A}(L - l_{void}) + \frac{\rho_b}{A_b} l_{void} , \tag{2.2}$$

where ρ_{Cu} and ρ_b are the resistivity of Cu and TaN/Ta barrier, respectively, L the total line length, A_b the cross-sectional area of the barrier, l_{void} the length of void. The critical void length upon failure is typically on the order of 100nm. The Cu line length L under EM test is typically on the order of 10-100μm. So the first term in Equation (2.2) is rather independent of the void length and the increase of the resistance comes essentially only from the second term in Equation (2.2) which is the barrier resistance at the void segment. Upon failure, l_{void} is identical to l_{crit}. Therefore the resistance jump at Stage II is

$$R_{step} = \frac{\rho_b}{A_b} l_{crit} \,. \tag{2.3}$$

This suggests that the critical void length is proportional to the resistance jump upon failure. For example, assume the effective resistivity of barrier as 2 μΩ-m [Doyen *et al.*, 2008]. When a void with length of 100nm fails a line with cross-section area of 50nm*100nm and barrier thickness of 10nm, the resistance jump can be calculated from Equation (2.3) as 87 Ω. As one will find in Section 2.4, this is a typical resistance jump value commonly observed in the EM tests for this study. By knowing the effective barrier resistivity and barrier cross-section, one can also calculate the void length from the resistance increase. In Figure 2.5, the void length calculated by this method is compared to the actual void length measured by SEM to verify this linear relationship [Doyen *et al.*, 2008].

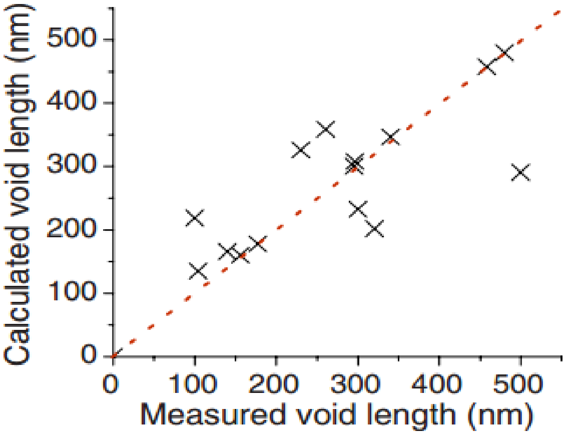


Figure 2.5 Comparison of the calculated and physically measured void length.[Doyen *et al.*, 2008]

At Stage III, the slope of the region with gradual resistance increase is

$$R_{slope} = \frac{\rho_b}{A_b}\frac{dl_{void}}{dt} = \frac{\rho_b}{A_b} v_{d,III}, \tag{2.4}$$

where $v_{d,III}$ is the drift velocity at Stage III. Here the drift velocity and the void growth rate are defined for two different Stages (I and III) of void growth. In previous EM studies, R_{slope} as defined in Equation (2.4) is commonly used to extract the drift velocity or the void growth rate that determines the EM lifetime [Doyen *et al.*, 2008, Arnaud *et al.*, 2011, Yokogawa, 2004, Lin *et al.*, 2010, Hu *et al.*, 2007b]. However, most of these studies did not differentiate the void growth rates between Stage I and III. But there is no evidence to show that the void growth rate at Stage I is identical to that at Stage III.

Nonetheless, a failure time can be defined based on the drift velocity at Stage III:

$$t_{f\_calc} = \frac{l_{crit}}{v_{d,III}} = \frac{R_{step}}{R_{slope}}. \tag{2.5}$$

Defined in this way, the parameter t_{f_calc} can be determined by measuring both R_{step} and R_{slope} from the resistance trace. This calculated failure time (t_{f_calc}) is based on the assumption (or model) that $v_{d,I}$ equals to $v_{d,III}$. In the following sections, the calculated failure time (t_{f_calc}) and the measured failure time (t_f) will be compared. If the calculated failure time (t_{f_calc}) and the measured failure time (t_f) are identical, then the plot of t_{f_calc} and t_f will yield a linear curve with slope of 1 and passing the origin of the coordinates. Otherwise, the plot would provide an indication about how much difference exists between $v_{d,I}$ and $v_{d,III}$ [Wu *et al.*, 2013].

Since R_{step}, R_{slope} and t_f are all statistically distributed, one has to control these parameters to obtain several sets of t_{f_calc} and t_f. There are several possible ways to achieve this. R_{slope} is proportional to the drift velocity. And in general, the drift velocity is proportional to diffusivity following the Einstein relation:

$$v_d = \mu F = \frac{D}{k_B T} F , \tag{2.6}$$

where μ is mobility, F the driving force, D the diffusivity, k_B the Boltzmann constant, and T the absolute temperature. So by varying the diffusivity one can change R_{slope}. There are two major diffusion paths in Cu interconnects: Cu/cap interface diffusion and grain boundary diffusion. Selective metal capping based on Co alloys, such as CoWP [Zhang, 2010, Christiansen *et al.*, 2011, Hu *et al.*, 2004a, Gambino *et al.*, 2006], has been demonstrated as an effective way to suppress the interface diffusion, although this process may potentially reduce the time dependent dielectric breakdown (TDDB) [Chen *et al.*, 2010, Tan *et al.*, 2008] performance of low-k dielectrics— another major reliability concern for interconnects. Another way to suppress the diffusion, especially grain boundary diffusion, is to add dopants, such as Ti, Al, Ge, Mn to the Cu seed layer [Christiansen *et al.*, 2011, Hu *et al.*, 2012, Nogami *et al.*, 2010, ITRS, 2011]. Those dopants will diffuse to grain boundaries and interfaces during the subsequent annealing process and slow down the Cu atom diffusion along these paths. The other parameter R_{step} is proportional to the critical void volume. In principle, this can be varied by tuning the grain size. Smaller grain size in a line may results in a smaller critical void volume. On the other hand, more grain boundaries in small-grain structures also provide more diffusion paths and larger diffusivity. The degradation of EM lifetime in lines with small grains has also been reported [Zhang *et al.*, 2011].

All these approaches mentioned necessitates a change of the processing conditions for Cu lines, which potentially changes the resistivity of the line, stress conditions etc.. Furthermore, the change of processes also requires samples to be fabricated in different wafers, which would cause more uncontrollable variations. To overcome these issues, multi-link structures from the same wafer are used in this study.

Figure 2.6 shows a schematic of multi-link test structure, where M1 is the structure subject to EM test. The electric currentflows through multiple M1 lines serially linked by via and M2 lines. The structure fails when one of the links fails. Such structures have been used to study the early failure problem and to detect the failure mode that can be difficult to be observed in single-link structures [Gall *et al.*, 1999, Ogawa *et al.*, 2001, Hauschildt *et al.*, 2007, Hau-Riege *et al.*, 2007, Ogawa *et al.*, 2002]. The purpose to use multi-link structure in this work is different from conventional studies. Multi-link structures are used to statistically tune the R_{step} and R_{slope} in the earliest failed line. Presumably, in a structure with more links, one would have a higher chance to find a link with smaller critical void volume and larger diffusivity, in other words, smaller R_{step} and larger R_{slope}. Meanwhile, all lines experience the same processing condition, which makes the comparison between lines more meaningful.

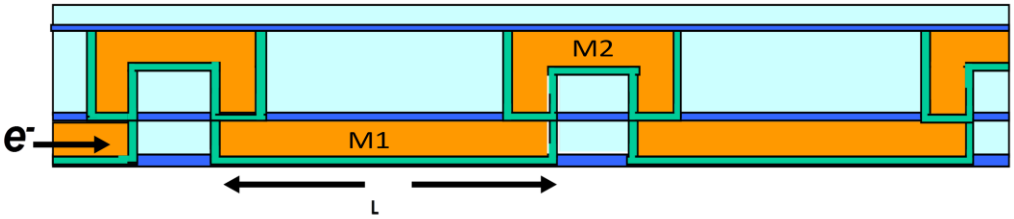


Figure 2.6 Schematic of the cross-section of a multi-link EM test structure.

2.3 SAMPLE INFORMATION AND EM EXPERIMENTAL PROCEDURE

The EM test structures were 45nm node two-level Cu/low-k structures from Texas Instruments. The link number varies from 2, 10, 50 and 100 with the M1 EM line length fixed at 100µm. The line width is 70nm except at line ends which are designed to be wider for contacting the 70nm*70nm vias. Figure 2.7(a) shows a layout of the 2-link structure, where two pink M1 lines linked by black square vias and one horizontal green M2 line. The M2 line is designed to be wide and short so that the EM in this layer is suppressed. Extrusion monitor lines surrounding the M1 lines are also fabricated to monitor potential anode extrusion. Both inter-layer dielectric (ILD) and inter-metal dielectric (IMD) used are organosilicate glass (OSG) with effective permittivity *k* of about 2.7. The thickness for the low-k dielectric stack is: 95nm for M1 IMD, 110nm for V1 ILD, 135nm for M2 IMD. A standard SiCN cap layer is performed for both M1 and M2 lines. And a 400nm SiON protective coating is deposited over the M2 layer. All samples studied are from a single 300mm wafer.

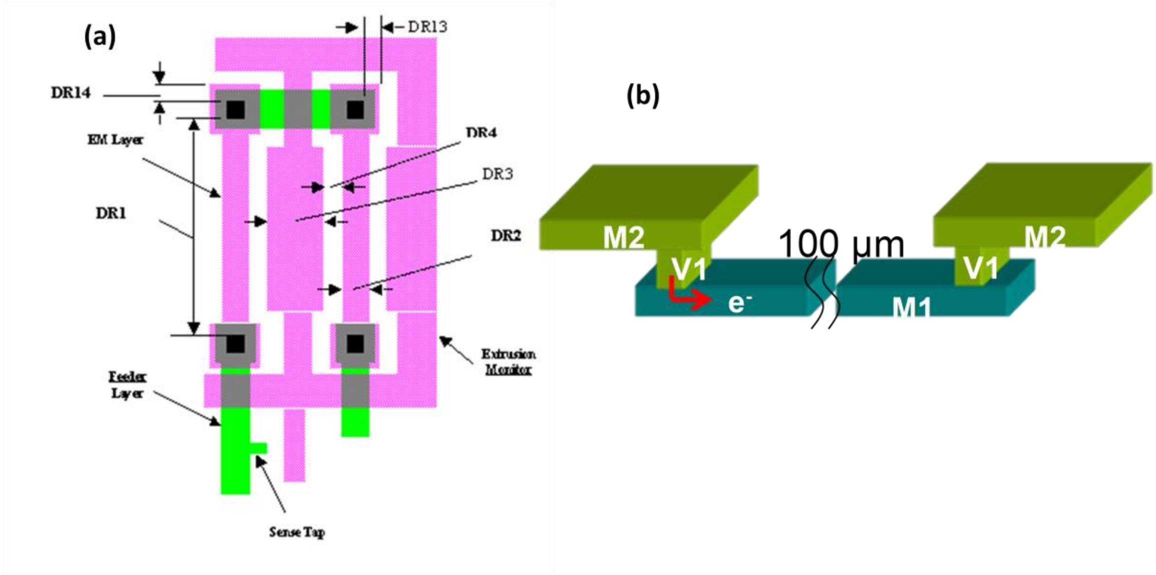


Figure 2.7 (a) Layout of the 2-link EM structure tested. (b) 3D schematic of M2V1M1 downstream test configuration.

All EM tests performed are package-level tests with a system shown in Figure 2.8. Tests were performed with a current density of 1.0MA/cm^2 in a downstream configuration. Figure 2.7(b) shows the schematic of such a downstream configuration. This current density corresponds to a 0.0665mA current through 70nm*95nm cross-section and 72.8mV over the 1095Ω resistor in the constant current source. The experiments were carried out in a test chamber vacuumed by a mechanical pump and backfilled with nitrogen to 20Torr to improve the temperature uniformity within the chamber. The heating of the chamber is realized by two sets of heating coils: the primarily heating coils located at the top and bottom plates to control the test temperature and the secondary heating coils mounted at the chamber sidewall to reduce the temperature gradient from the center to the edge of the chamber. The targeting test temperature is set at 330°C by ramping up at the rate of about 3°C/min. Each heating coil has a separate temperature controller.

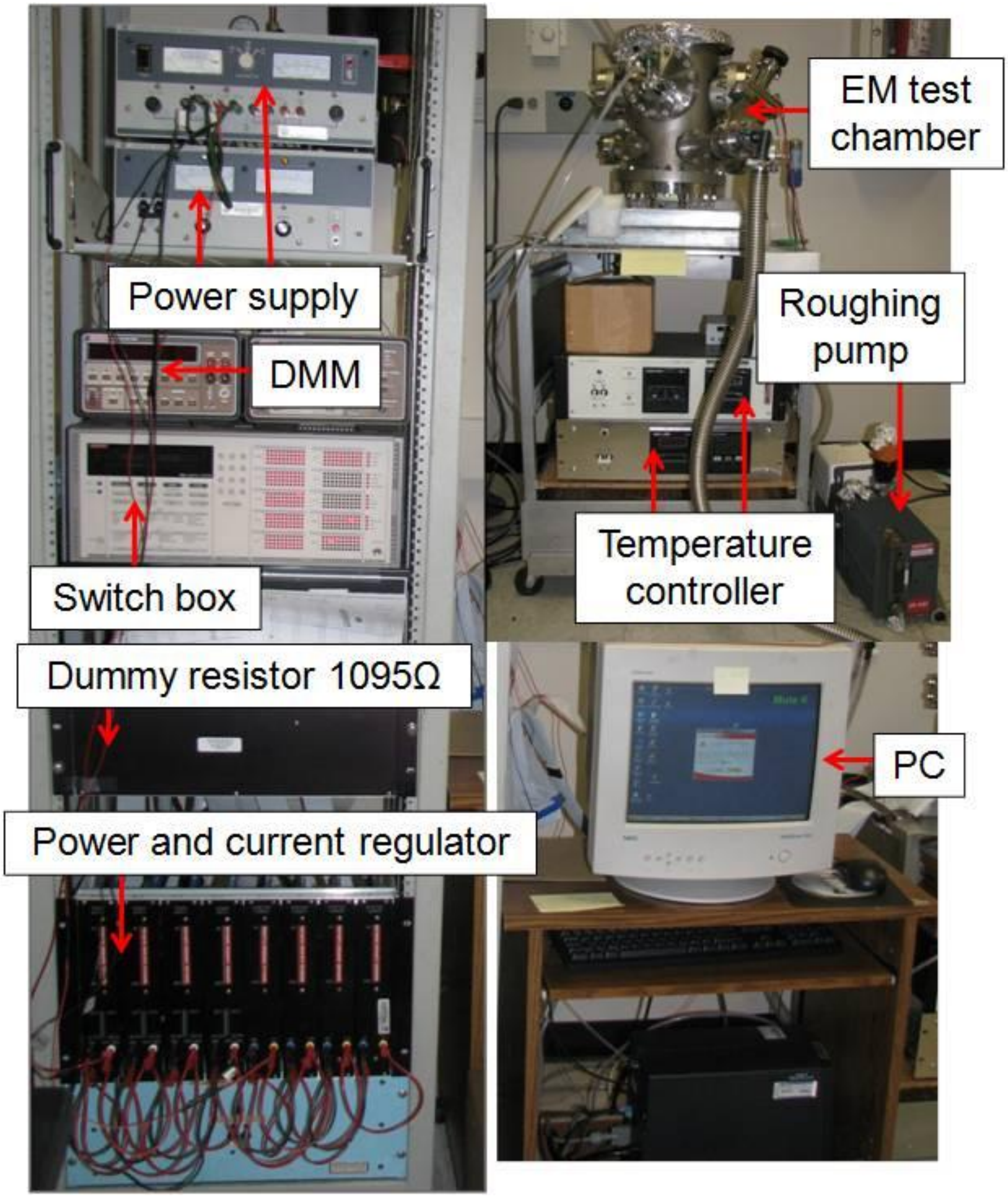

EM test chamber
Power supply
Roughing pump
DMM
Temperature controller
Switch box
Dummy resistor 1095Ω
PC
Power and current regulator

Figure 2.8 Package-level EM test system.

A current regulator is employed to maintain the constant current density during tests. The power supply can support output up to 80V and 10mA. A Keithley 7002 switching box is used to select the channel of the sample under test in sequence. A Keithley 196 digital multimeter (DMM) is used to measure the voltage drop thus the resistance across the testing samples. The data acquisition is controlled by a National Instruments LabView program.

After receiving the wafer with desired EM structures, wafer dicing, die attach, and wire bonding must be performed before the package level EM test. Some information for each step is listed below.

The wafer is diced into 2mm*3.6mm pieces with the test module of interest in the die. An ADT 7100 dicing saw with a Ni blade (Q1235-Q5SH-000) from Kulicke&Soffa (K&S) are used for dicing.

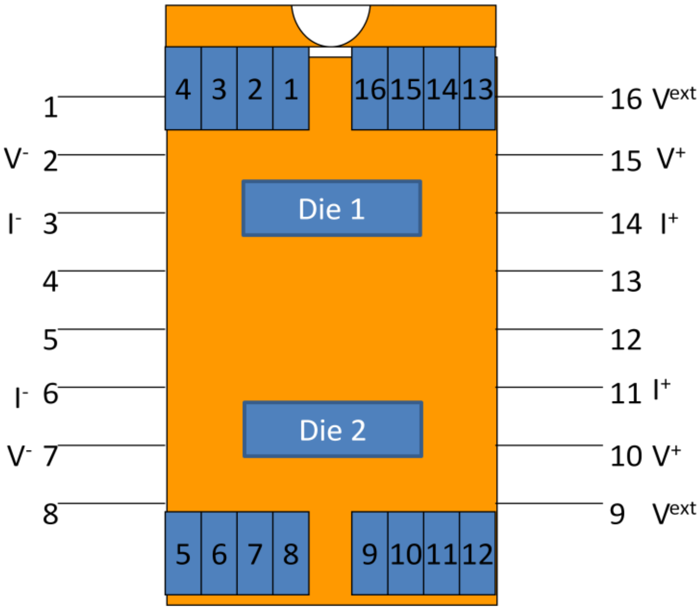


Figure 2.9 16-pin DIP package with two dies attached.

The dies are attached to 16-pin ceramic dual-in-line (DIP) packages, as schematically shown in Figure 2.9. Each package contains two dies. The die attach paste used is a conductive silver paint from SPI. Curing of package is realized with 24-hour room temperature storage.

A West Bond Model 7400A Ultrasonic Wire Bonder is then used to electrically connect the EM module with the DIP package. The bonding wire used is 1% Si-Al alloy wire with 1.5 mil diameter. The pin to pin resistance is measured by a multimeter after wire bonding to ensure proper bonding.

The packages are then carefully loaded into the EM chamber to ensure good DIP pin to socket electrical contact, which is verified by multimeter measurements. An electrostatic discharge (ESD) strap is worn during all pre-EM-test procedures to protect the EM structure from electrostatic discharge damage.

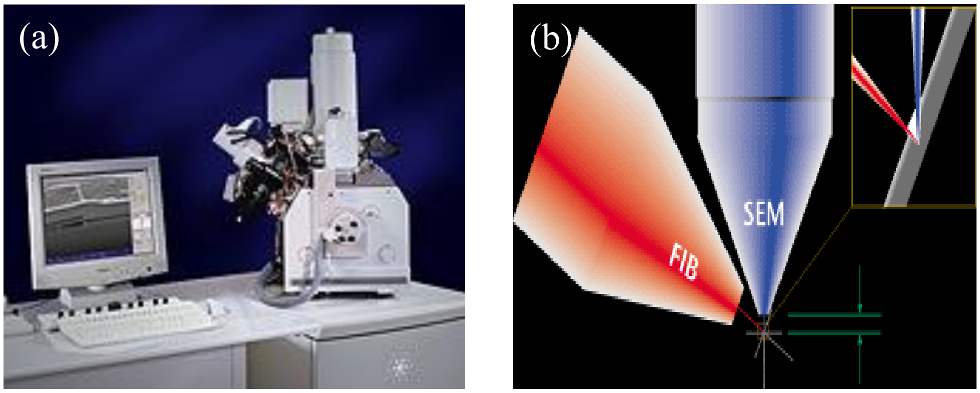


Figure 2.10 (a) FEI Strata^{TM} DB235 dual beam FIB/SEM system and (b) schematic illustration of the configuration of the two beams (52° in between).

After EM tests, certain failed samples are selected for failure analysis. The sample is cut by a Focused Ion Beam (FIB) to check the cross-section of the line and location of the void. This is conducted by a FEI Strata^{TM} DB235 dual beam FIB/SEM system which is shown in Figure 2.10. The sample is tilted to be perpendicular to the focused Ga ion beam during cutting. Meanwhile the electron beam, which has a 52° angle with the ion beam, is used to take SEM images to monitor the cutting position.

2.4 RESULTS AND DISCUSSION

2.4.1 Resistance Traces and Failure Mode

Figure 2.11 shows a typical EM resistance trace for a 2-link structure. Two clear resistance jumps are observed, which corresponds to 2 voids spanning the line cross-section. In a relatively long period of EM stressing, only two voids are observed for 2-link structure. This suggests that each line probably contains one void, although multiple voids formed in a single line has been reported before [Zhang, 2010]. The 1st jump determines the failure time t_f. The statistics of R_{step} and R_{slope} in the following sections is based on the 1st jump and its subsequent gradual increase region. For higher number of links, more resistance jumps are observed. Figure 2.12 shows a typical resistance traces for 10-link structures with multiple resistance jumps.

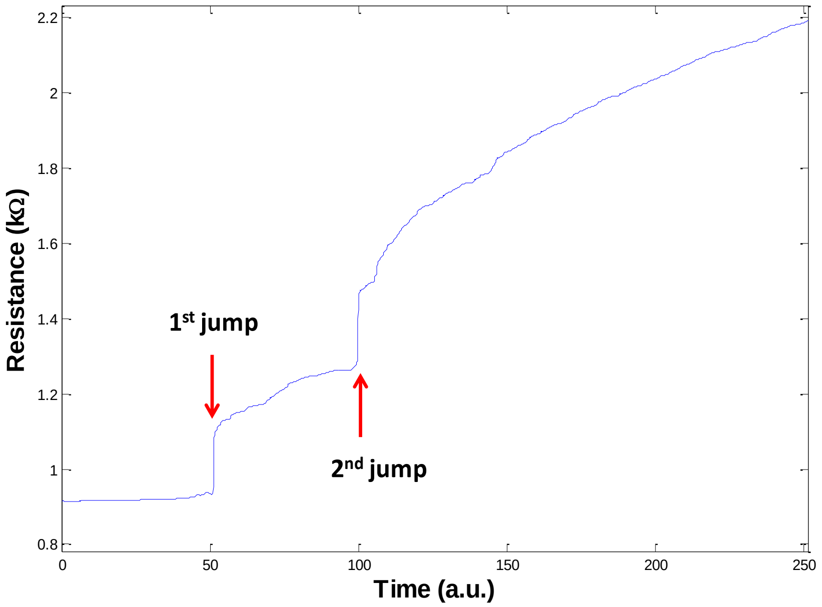


Figure 2.11 Typical resistance trace for 2-link structure showing two resistance jumps.

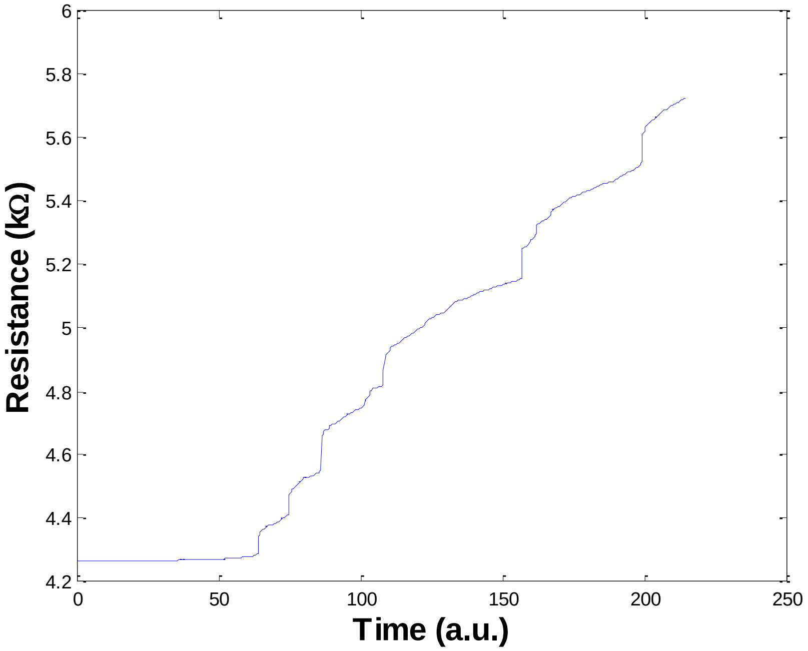


Figure 2.12 Typical resistance trace for 10-link structure.

The typical resistance increase for these jumps is about 100Ω, which corresponds to a trench type void. The post-mortem failure analysis also confirms the void type. Figure 2.13 (a) shows a post-test sample cut by FIB. The void is a trench type with an average length of about 100nm. By assuming TaN/Ta barrier thickness as 10nm [Zhang, 2010], the effective barrier resistivity is found to be 2.3 μΩ-m in agreement with the reported value (2-3 μΩ-m) [Doyen *et al.*, 2008]. Figure 2.13 (b) shows an initial void formed at the interface between Cu and cap layer which agrees with the model analysis shown in Figure 2.2 and Figure 2.4.

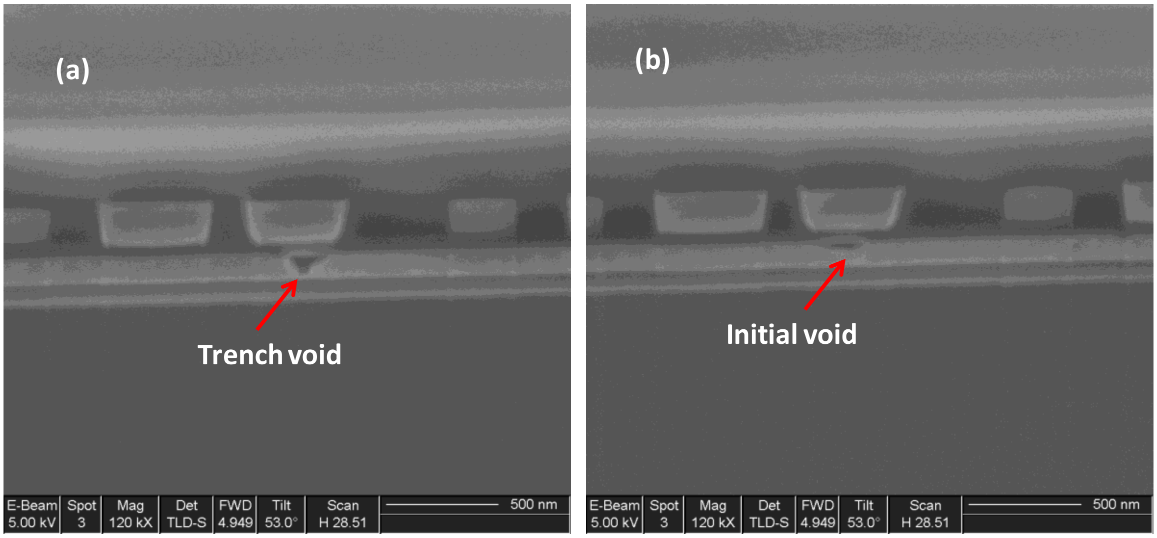

(a)
Trench void
E-Beam 5.00 kV
Spot 3
Mag 120 kX
Det TLD-S
FWD 4.949
Tilt 53.0°
Scan H 28.51
500 nm
(b)
Initial void
E-Beam 5.00 kV
Spot 3
Mag 120 kX
Det TLD-S
FWD 4.949
Tilt 53.0°
Scan H 28.51
500 nm

Figure 2.13 SEM images of void formed. (a) trench type void fails the line; (b) initial long slit type void formed at the Cu/cap interface.

Some resistance traces have a relative short plateau right after the jump, which is followed by a gradual increase region. Figure 2.14 shows such an example. In this case, the calculation of R_{slope} is based on the gradual increase region only.

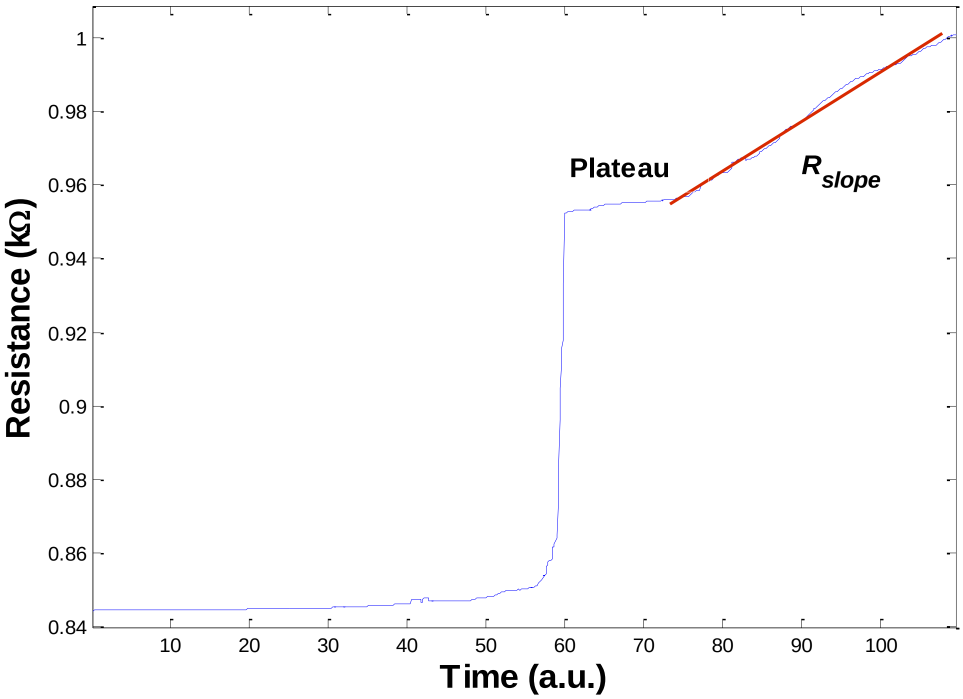


Figure 2.14 A plateau followed by a gradual increase region in a trace.

Some resistance traces are noisy or have small resistance increases before the jump. Sometimes it may not be easy to tell which increase relates to a line failure. To better discern the resistance jump and slope, the time differentiation of the resistance was also plotted together with the trace. As shown in Figure 2.15, a sharp δ-function like signal appeared to signify a real resistance jump caused by line failure. This is distinguished from bumps caused by resistance noise in the trace.

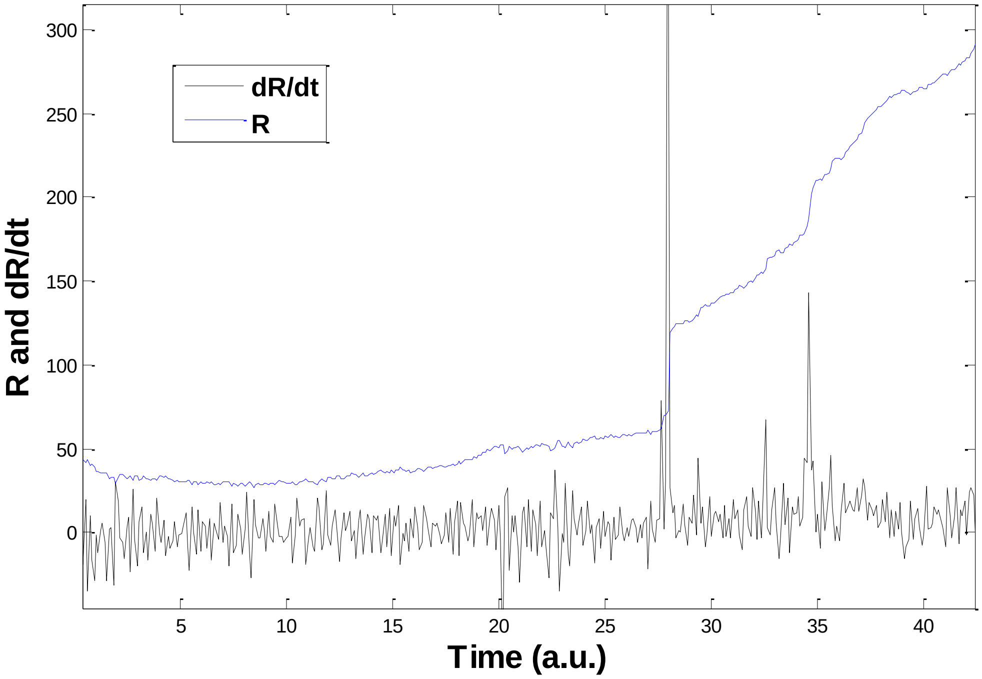


Figure 2.15 Noisy resistance trace with its time differentiation.

A linear curve best fitting the gradual increase region is used to derive R_{slope}. For those structures with many links, small voids were formed in each link before one of them grew big enough to fail the structure. Although one small void causes negligible resistance change, the resistance increase resulted from a large amount of small voids in many links is considerable. This can be easily observed in Figure 2.16 for a 100-link structure, where the resistance starts the gradual increase before the abrupt jump. R_{slope} should be the rate of resistance increase from the critical void failed the structure only. In this case, R_{slope} is calculated as the difference between the slope after and before the jump, as demonstrated in Figure 2.16.

$$R_{slope} = slope1 - slope2\,. \tag{2.7}$$

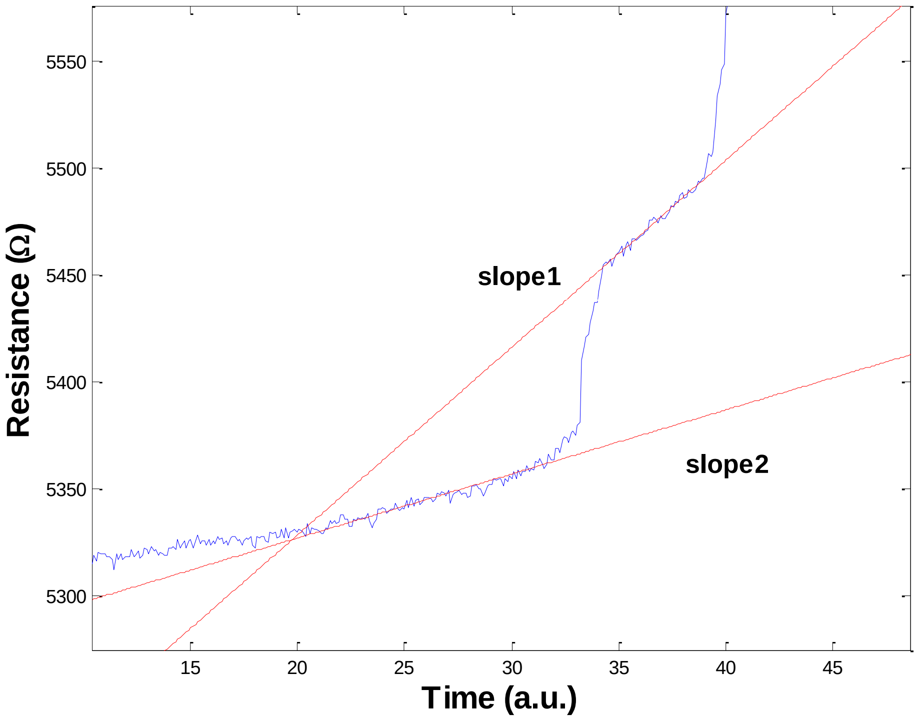


Figure 2.16 The large amount of small voids formation cause resistance increase before line failure. The R_{slope} is the difference between slope1 and slope2.

Resistance jump R_{step} much bigger than the typical value 100Ω is occasionally observed. Figure 2.17 and 2.18 show two examples of such big jump observed from 10-link and 100-link structures. The R_{step} for these two cases are about 1.5 kΩ and 8 kΩ respectively. If such failures are also caused by the trench type void, the critical void length would be as long as several microns, which is an unrealistic occurrence. So this should correspond to a different failure mode. Resistance jumps bigger than 1 kΩ have been reported by other authors before and they were identified as slit-type void formed under vias [Oates *et al.*, 2006, Lee *et al.*, 2006, Oates *et al.*, 2009b, Oates *et al.*, 2012], as shown in Figure 2.19.

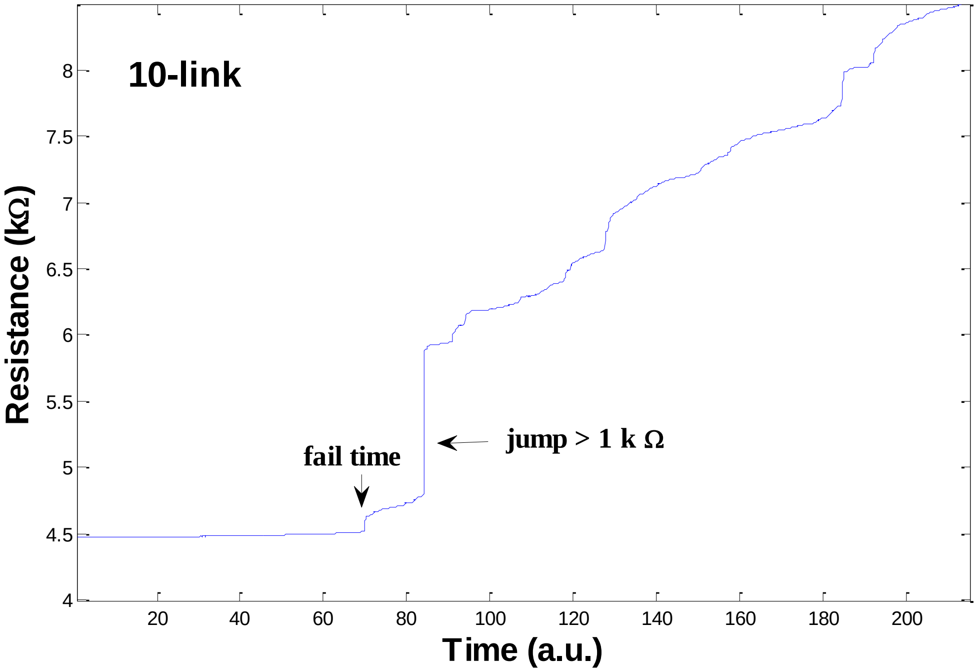


Figure 2.17 Big resistance jump observed in a 10-link structure.

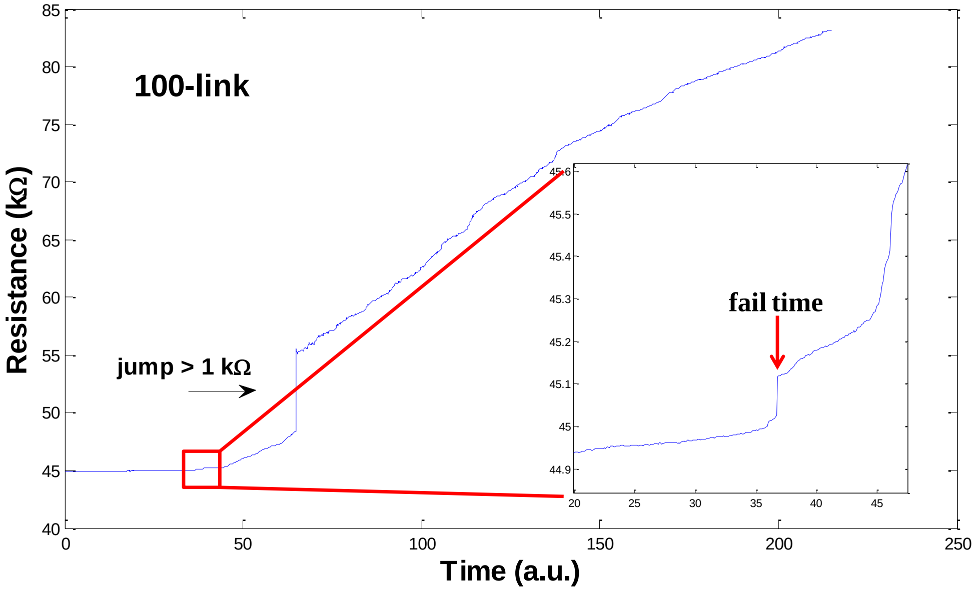


Figure 2.18 Big resistance jump observed in a 100-link structure.

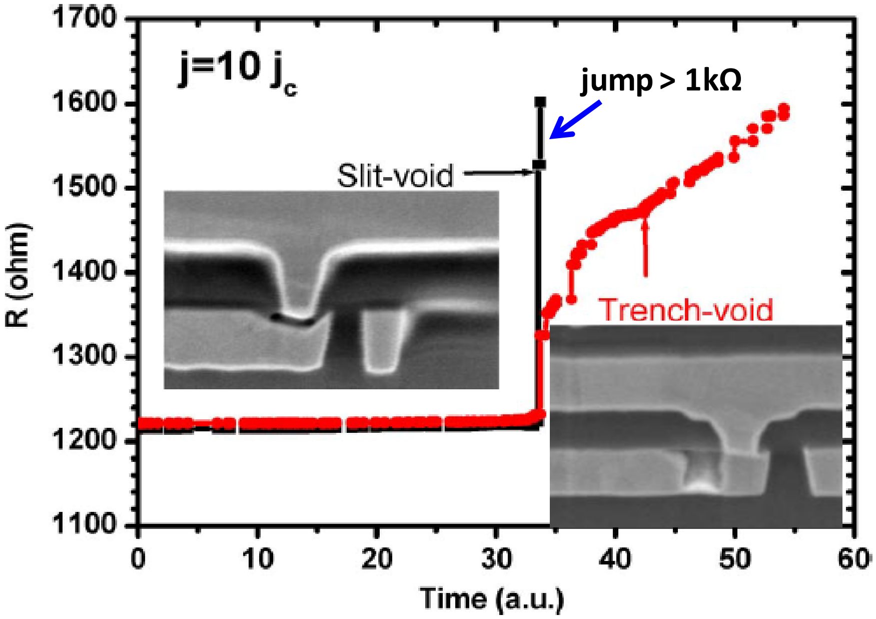


Figure 2.19 Big resistance jump (> 1 kΩ) corresponds to a slit-void. [Oates *et al.*, 2009b]

The samples under this study have M1 line ends wider than the vias as described in Figure 2.6(a). Once a slit-void is formed under the via, there is no electrical redundancy between M1 and V1 to bypass the electrical current. This results in a huge resistance jump as observed. Such slit-voids are more frequently observed in multi-link structures [Lee *et al.*, 2006]. The results in Table 2.1 show that the chance to find them in 100-link structures is higher than in 10-link structures. No such big resistance jump is observed in the 2-link structures. This also supports that the big resistance jumps correspond to slit-void. The slit-voids only require very limited amount of mass transport of Cu atom to open the connection between the line and the via. The failure time caused by such voids can be much shorter than the regular trench type void, which is of great interest in EM reliability study [Li *et al.*, 2004, Lee *et al.*, 2006]. However, all the big jumps observed in samples of this study are not the first jump. This indicates that the V1M1 interfaces in this particular batch of samples are good in suppressing the mass transport. Since this study is only interested in the line failure caused by the first jump, the slit-void failure mode will not be further studied in this dissertation.

Table 2.1 Number of big resistance jump observed in different links.

	# of big resistance jumps	# of samples tested
2-link	0	20
10-link	3	22
100-link	5	23

2.4.2 Joule Heating and TCR

When electric currentflows through an EM structure, the Joule heating may cause temperature increase. The power of Joule heating is proportional to the resistance of the test structure. The resistance of a multi-link EM structure is proportional to its link number. This may result in a temperature difference between different links, which would greatly affect the EM performance. It is well know that the EM lifetime has an exponential dependence on temperature. So it is of importance to estimate the potential temperature increase due to Joule heating for different links to achieve a fair comparison between them.

The follow procedure is used to evaluate the Joule heating in the test structure [Lee, 2003]:

1) Under a relatively small current applied to the EM samples, slowly increase the temperature of the EM chamber. The resistances of the samples with respect to temperature is recorded and used to calculate the temperature coefficient of resistivity (TCR).
2) Slowly increase the current density until the target current is reached. The resistance increase of the samples due to temperature increase caused by Joule heating is determined.
3) Use the TCR measured in step 1 and resistance increase in step 2 to calculate the temperature increase due to Joule heating.

The TCR (α) is defined as the fractional change in resistance per unit change in temperature:

$$\alpha = \frac{\Delta R}{\Delta T} / R_0, \tag{2.8}$$

where R_0 is the resistance at room temperature or reference temperature, ΔR and ΔT are the resistance change and temperature change, respectively. The resistance increase in high temperature for Cu is due to increased carrier scattering mostly with phonons. TCR can also be defined based on resistivity

$$\alpha = \frac{\Delta\rho}{\Delta T} / \rho_0 . \tag{2.9}$$

The resistance at room temperature (25°C) and EM temperature (330°C) for 21 samples with different links is recorded. The TCR measured was 0.002326 ± 0.000022 $(°C)^{-1}$. No dependence on link number of TCRs was observed. This value is smaller than the TCR for bulk Cu 0.0039 $(°C)^{-1}$ and the TCR for 0.5μm wide Cu line 0.0033 $(°C)^{-1}$ reported in [Lee, 2003]. This can be understood as the size effect of the resistance or resistivity for the metal line. In the expression of TCR, $\Delta\rho / \Delta T$ is relatively constant independent of line width, since it is from the contribution of phonon scattering. However, it is well known that resistivity has a significant size effect when the line width approaches the electron mean free path (39nm for Cu at room temperature). This size effect will be discussed more in detail in Chapter 4. The increase of ρ_0 in smaller line width (70nm for this set of samples) decreases the TCR. Other authors also reported reduced TCRs for Cu lines with smaller width [Schindler *et al.*, 2003, Huang *et al.*, 2008]. Since the Cu lines are constrained within TaN/Ta barrier and low-k dielectric which have different thermal expansion, the thermal strain may also have an effect on TCR [Warkusz, 2001].

Apparently, the 100-link structures would have the most significant potential Joule heating induced temperature increase compared to other links. So 10 samples of 100-link structure at the targeted EM temperature 330°C were first tested. A relatively small current density (0.25 MA/cm^2) was employed to first measure the resistances, which yields a result of 43.94 ± 1.69 kΩ. Then the current density was increased to the targeted density (1 MA/cm^2). This current difference is equivalent to 16 times of Joule heating power. The resistance measured at the target current density was 43.63 ± 1.67 kΩ. The resistance actually decreased by 0.31 kΩ (0.7%), instead of being increased through Joule heating as normally expected. A possible explanation is given below. The power of Joule heating is

$$P = I^2 R = (jA)^2 \rho \frac{L}{A} = j^2 \rho L A\,. \tag{2.10}$$

It is proportional to line cross-section A, when current density j and line length L is set. The heat generated in a 70nm wide line is probably insignificant and dissipated away quickly without causing considerable temperature increase. The decrease of the resistance may arise from the grain growth at 330°C. It took about 2 hours to manually tune the current to 1MA/cm^2 for all the channels and started the measurement at the targeted current. During this time period, the grain growth might have taken place causing the resistance to decrease. Such resistance decrease is also observed in the initial stage of the EM resistance traces. Figure 2.20 shows an example.

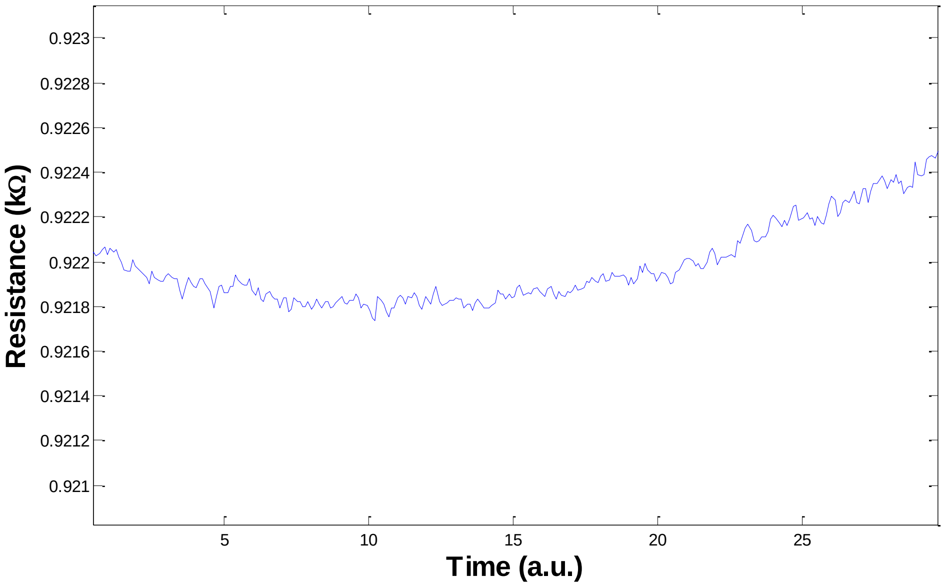


Figure 2.20 Initial resistance decrease in an EM resistance versus time trace.

Overall, no measurable Joule heating induced temperature increase was observed in the samples. EM structures with different link numbers can be considered at the same temperature within experimental errors.

2.4.3 Failure Time Statistics

A total of 127 devices were prepared for this study. Many of them lost electrical contact with the sockets of the chamber during loading or testing. Some tests, although successful, had two resistance jumps too close to each other to extrapolate the R_{slope}. Some, especially those with more links, had relatively steep gradual increase region before failure so that it was difficult to resolve the R_{step}. In the end, enough data were produced to generate statistics for 2, 10, and 100 links. So only 2, 10 and 100 links are used to for the following study. A brief introduction of the fundamentals of EM failure time statistics is presented below.

EM failure time has traditionally been assumed to follow lognormal distribution. The lognormal failure distribution can be conceptually understood as that the logarithms of the failure times follow a normal distribution. The probability density function (PDF) of a lognormal distribution is

$$f(t) = \frac{1}{t\sigma\sqrt{2\pi}} \exp\left(-\frac{(\ln t - \ln t_{50})^2}{2\sigma^2} \right), \tag{2.11}$$

where t_{50} is the median failure time and σ is the standard deviation in lognormal distribution or the standard deviation of the log value of failure time. The cumulative distribution function (CDF), which describes the probability of a line failing within time interval [0, t], can be expressed as a complimentary error function:

$$F(t) = \int_0^t f(u)du = \int_{-\infty}^{z} \frac{1}{2\pi^2} \exp\left(-\frac{v^2}{2} \right) dv = \frac{1}{2} erfc\left(-\frac{z}{\sqrt{2}} \right), \tag{2.12}$$

where $z = \frac{\ln(t) - \ln(t_{50})}{\sigma}$. Figure 2.21 shows a PDF and a CDF plot for lognormal distribution with $\sigma = 0.2$.

Exactly why the lognormal distribution is used is still an open question. Some people believe that the origin of it is that the grain size in metal lines follows a lognormal distribution which itself is not well understood. However, there is also a story that it is simply because Jim Black just happened to have such distribution function at hand when he first plotted the EM failure times in the 1960s [Lloyd, 2002]. In any case, a well-defined analytical function is needed to analyze the failure distribution in order to obtain the targeted end-of-life (EOL) from the measured EM stressed data.

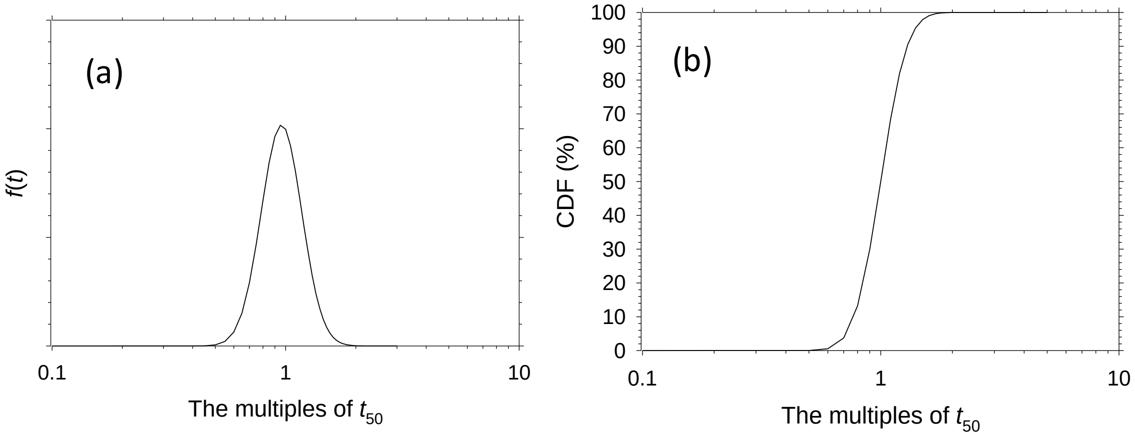


Figure 2.21 (a) PDF and (b) CDF plot of a lognormal distribution with $\sigma = 0.2$. [Lee, 2003]

In a multi-link structure, the link that fails first determines the time to failure of the structure. This is the so called weakest link model. The reliability function of a structure with N links is

$$R(t, N) = R_1(t) \text{ x } R_2(t) \text{ x } R_3(t) \text{ x } R_4(t) \text{ x...x } R_N(t), \tag{2.13}$$

or

$$1\text{-}F(t, N) = (1\text{-}F_1(t)) \text{ x } (1\text{-}F_2(t)) \text{ x } (1\text{-}F_3(t)) \text{ x.....x } (1\text{-}F_N(t)), \tag{2.14}$$

since $R(t) = 1- F(t)$. $F_i(t)$ is the CDF or unreliability function of ith link. Under the weakest link approximation (WLA), each link follows the same failure statistics and $F_i(t)$ is a function independent of i. The CDF of N-link structure can then be simplified as

$$F(t, N) = 1- (1\text{-}F_1(t))^N. \tag{2.15}$$

Figure 2.22 is a representation of CDF based on WLA for multi-link structures when N=1, 10, 100 and 1000. The single link failure distribution $F_1(t)$ is assumed as lognormal. A clear trend can be found: as N increases, the failure time decreases and the deviation of failure time decreases.

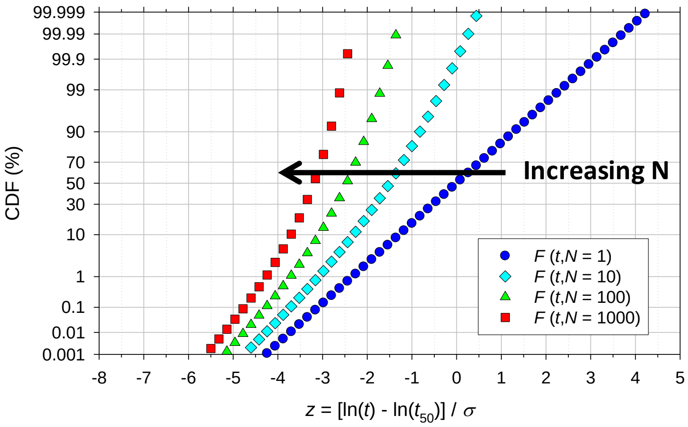


Figure 2.22 CDF plots for N-link structures with N=1, 10, 100, 1000. [Ogawa *et al.*, 2001]

From Figure 2.22 and Equation (2.15), one can find that, in the frame of WLA, $F(t, N)$ cannot be lognormal distribution for $N > 1$ if $F_1(t)$ is lognormal. In other words, t_{50} and σ are usually not well defined for multi-link structures. Because the assumption of lognormal distribution is not extendable to multilink structure, the validity of the analysis has been challenged from time to time. Nevertheless, until now, there is no other analytical distribution having more experimental data support than the lognormal distribution. In this study, the definition of t_{50} and σ based on the lognormal distribution is applied to multi-link structures simply for convenience. In fact, most experimentally observed range of CDF is between 1% and 99%, where the CDF plots approximately follow linear curves in a lognormal distribution plot even for multi-link structures as shown in Figure 2.22 and for the experimental data in Figure 2.29. Therefore, the description of multilink statistics follows that of Ref. [Ogawa *et al.*, 2001] , indicating that as N increases in multi-link structures, t_{50} and σ decreases.

Figure 2.23 shows the cumulative distribution function (CDF) for failures versus time to failure (TTF) plots for 2, 10 and 100 links. In general, the data follow the simulation trend in Figure 2.22 with the 100-link structures having smaller failure time. However, there are 2 data points in the 10-link structures and 1 data point in the 100-link structures (enclosed in 2 dotted ellipses), which seem to fail in a different mode. Several groups have reported such bi-modal failure to occur in EM tests of Cu/oxide [Ogawa *et al.*, 2001, Ogawa *et al.*, 2002] and Cu/low-k interconnects [Pyun *et al.*, 2005, Lee *et al.*, 2004, Oates *et al.*, 2006].

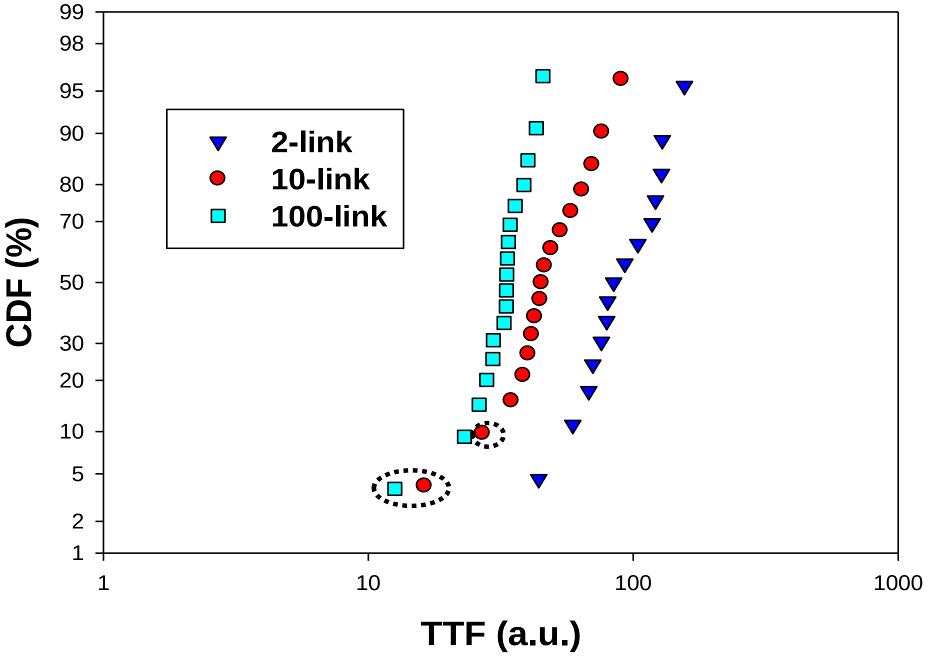


Figure 2.23 Experimental CDF plots for multi-link structures with N=2, 10, 100. The 3 data points in the dotted ellipses are probably failed in a different mode.

The early fails observed in this study were not caused by slit-type void formation under the via as reported in [Oates *et al.*, 2006], because the resistance jump R_{step} observed for these early fails was about 100 Ω corresponding to a trench-type void.

Figure 2.24 shows a typical resistance trace for the early fail with R_{step} as 94 Ω. The origin of such failures may be extrinsic failure induced by process defects.

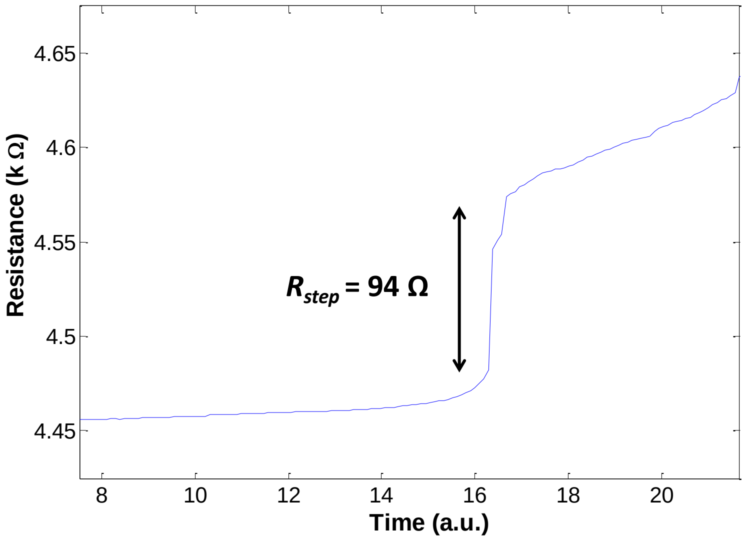


Figure 2.24 Resistance trace for the earliest failure detected for 10-link structures. The resistance jump is 94 Ω.

The early failure usually is a weak mode with a small probability to be detected in a single-link structure. For example, Figure 2.24 shows a Monte-Carlo simulation for CDF plots with bi-modal failure. The probability for the early failure weak mode is set at 1%. In this case, in a single-link structure, only the strong mode can be detected, while in a 100-link structure, more than half of the CDF branch will fail by the weak mode. One can use the simulation in Figure 2.25 to fit the experimental data in Figure 2.23 to determine the t_{50} and σ for two modes. However, the research objective of this study is to investigate the void formation mechanism, instead of the early failure. So, in what follows, the intrinsic strong mode, which has more data points to generate the statistics, will be studied.

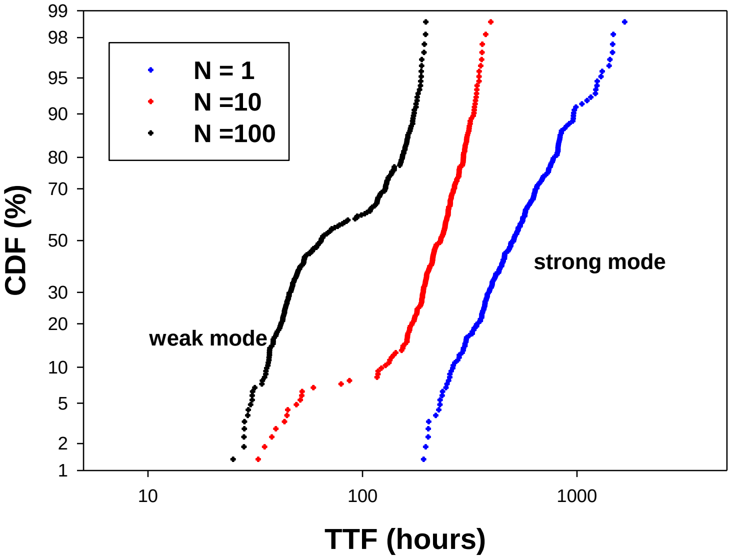


Figure 2.25 Monte-Carlo simulations for a bi-modal failure with N = 1, 10 and 100. The strong mode parameters are t_{50} = 500 hours and σ = 0.5. The weak mode parameters are t_{50} = 50 hours and σ = 0.3. The probability for weak mode is set as 1%.

The statistical probability of the failure modes is not readily determined based on the CDF plots in Figure 2.23. To confirm that the three data points near the bottom of the CDF plot are from a failure mode different from all other data points, one can deconvolute the three CDF plots for N = 2, 10 and 100 to a single hypothetical failure distribution for N = 1. In this way, the data points of the same failure mode will manifest themselves as a single lognormal distribution, while those failed by a different mode will deviate from the expected lognormal distribution. The deconvolution is achieved by using the concept of conditional probabilities (CP), following [Nelson, 1990] and [Gall, 1999]. This is illustrated using the 100-link tests as an example. Initially, 18 100-link structures, i.e., 18 x 100 =1800 links are under test at time $t_0 = 0$. At time t_1, one of the links in the 100 link structure fails, corresponding to 1 out of 1800 links failing within time t_1. Therefore the conditional reliability $R_1^{'}$ at t_1 is (1-1/1800), which equals to the unconditional reliability R_1. After t_1, although the remaining 99 links in the failed structure are still under stressing, no further information can be extracted from the rest of the test links since only the failure time for first failed link is recorded. Therefore these 99 links should be taken out and 1700 links are under test after t_1. At time t_2, one of the links in another structure fails. The conditional reliability at t_2 then is (1-1/1700). It is the survive rate at t_2 under the condition that the survive rate at t_1 is (1-1/1800). Therefore the unconditional reliability at t_2 is (1-1/1700) x (1-1/1800). In this way, the test and analysis for the other 1600 links can be continued in the same manner. The unconditional reliability R_i at t_i are recursively calculated. The unconditional failure rate, i.e., the CDF at t_i is F_i = 1- R_i. Table 2.2 shows the procedures to calculate the conditional and unconditional reliabilities for 18 100-link population.

Table 2.2 Procedures to deconvolute 100-link distribution into 1-link distribution. The method for data analysis follows [Nelson, 1990].

i = # of failed structures	t_i = failure time	n_i = # of links at t_{i-1}	1/ n_i	R_i' = 1- 1/n_i conditional reliability	R_i= R_1' R_2'... R_i' unconditional reliability	F_i=1- R_i unconditional failure
1	12.6	1800	0.000556	0.999444	0.999444	0.000556
2	23.06	1700	0.000588	0.999412	0.998857	0.001143
3	26.209	1600	0.000625	0.999375	0.998232	0.001768
4	28.005	1500	0.000667	0.999333	0.997567	0.002433
5	29.54	1400	0.000714	0.999286	0.996854	0.003146
6	29.63	1300	0.000769	0.999231	0.996087	0.003913
7	32.53	1200	0.000833	0.999167	0.995257	0.004743
8	33.17	1100	0.000909	0.999091	0.994353	0.005647
9	33.21	1000	0.001	0.999	0.993358	0.006642
10	33.33	900	0.001111	0.998889	0.992254	0.007746
11	33.5	800	0.00125	0.99875	0.991014	0.008986
12	33.8	700	0.001429	0.998571	0.989598	0.010402
13	34.32	600	0.001667	0.998333	0.987949	0.012051
14	35.82	500	0.002	0.998	0.985973	0.014027
15	38.64	400	0.0025	0.9975	0.983508	0.016492
16	40.03	300	0.003333	0.996667	0.98023	0.01977
17	43.08	200	0.005	0.995	0.975329	0.024671
18	45.63	100	0.01	0.99	0.965575	0.034425

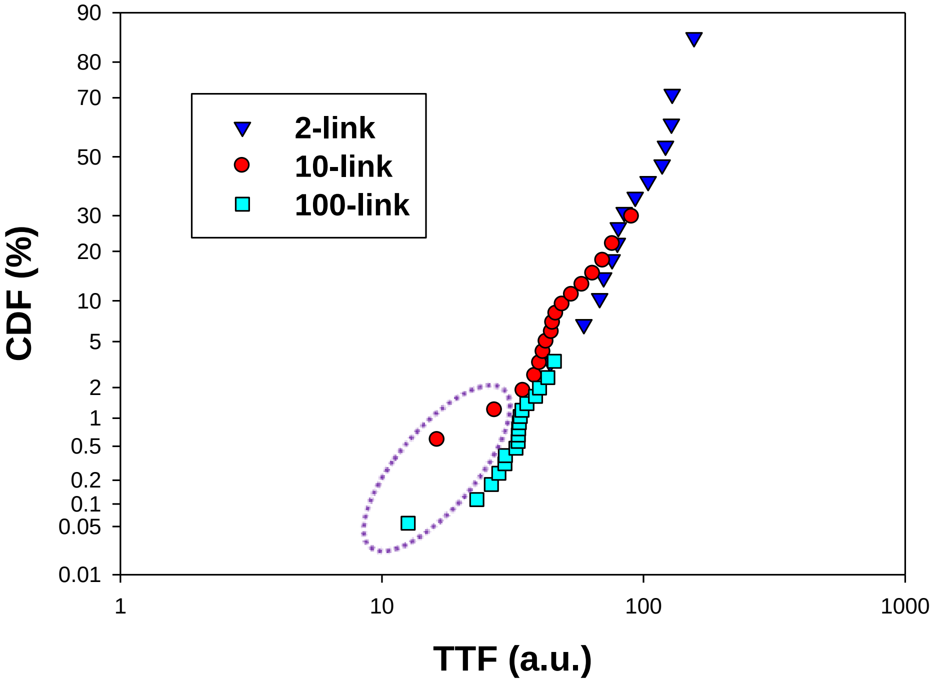


Figure 2.26 Deconvoluted failure time distribution for *N* = 2, 10 and 100, representing a single link distribution. The three data points in the dotted ellipse clearly appear to be a different failure mode.

The deconvolution procedures are performed to 2, 10 and 100-link data depicted in Figure 2.23 and the deconvoluted results are shown in Figure 2.26. Note that from Figure 2.23 to Figure 2.26, only the CDF changed due to the calculation method, but the failure times are identical. It is much clearer now in Figure 2.26 that the three data points in the dotted ellipse are from a different extrinsic failure mode. All the others follow a single distribution well. So these three extrinsic failure times are excluded in the following analysis.

Figure 2.27 shows the deconvoluted failure time distribution with the three extrinsic data points excluded. After deconvolution, the 2-, 10- and 100-link failure times coincide with each other on a single lognormal distribution. This confirms that all the lines under study failed by the same mode except for the three early failure data points.

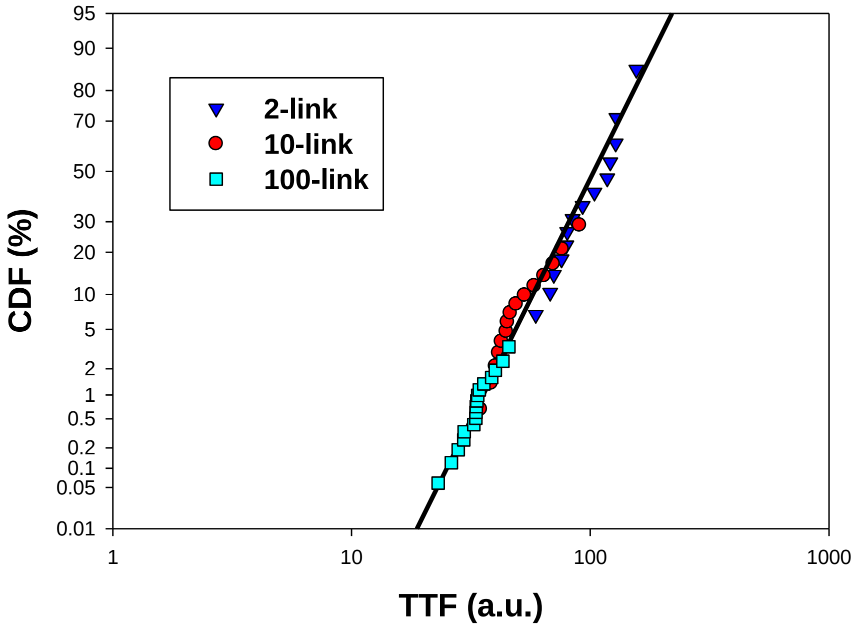


Figure 2.27 The failure time distribution for N = 2, 10 and 100 in the intrinsic failure mode are deconvoluted into N = 1 based on CP. They follow a single lognormal distribution. Deconvolution is performed based on conditional probabilities.

Another simpler way of deconvolution is to use the WLA in Equation (2.15), which was proposed by [Lee *et al.*, 2006]. When the failure time distribution for N-link structure $F(t, N)$ is known from measurement, the failure distribution for single link can be obtained from the inversion of Equation (2.15) as

$$F_1(t) = 1 - (1 - F(t, N))^{1/N}. \qquad (2.16)$$

The decovolution result for the intrinsic failures obtained by this method is shown in Figure 2.28. The result is similar to that in Figure 2.27, which further confirms that all the lines failed by a single intrinsic mode. The last two columns of Table 2.3 list the t_{50} and σ of the distribution for $N = 1$ which are deduced by deconvolution based on conditional probabilities (CP) and WLA respectively. The two methods give similar values for t_{50} and σ.

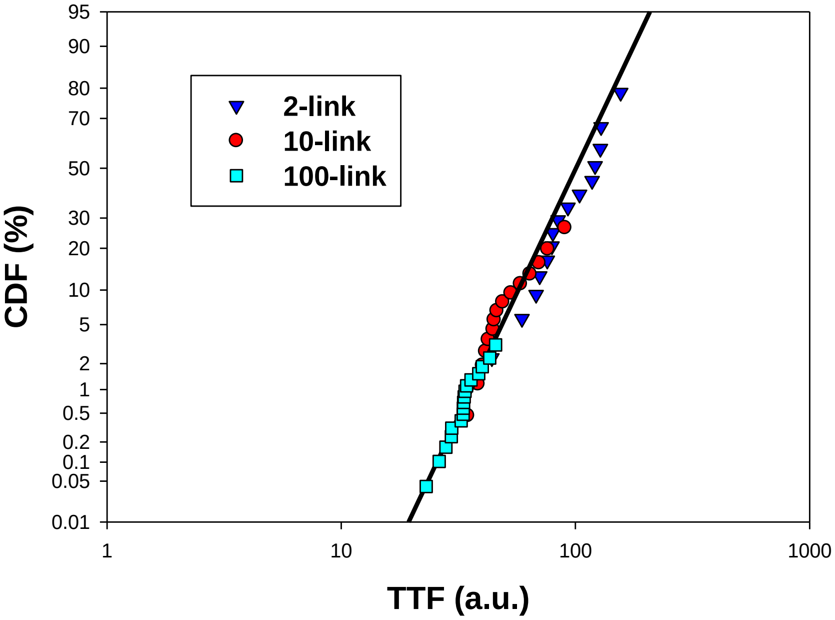


Figure 2.28 The failure time distribution for $N = 2$, 10 and 100 in the intrinsic failure mode are deconvoluted into $N = 1$ based on WLA. They follow a single lognormal distribution. Deconvolution is performed based on WLA.

Table 2.2 The t_{50} and σ of intrinsic failures for N = 2, 10 and 100, and the deconvolution to N = 1 with two methods. CP: conditional probabilities; WLA: weakest link approximation.

	N = 100	N = 10	N = 2	N = 1 CP	N = 1 WLA
t_{50} (a.u.)	31	51	90	110	115
σ	0.19	0.30	0.37	0.44	0.45

Figure 2.29 shows the intrinsic failure time distribution for N = 2, 10 and 100. They follow the WLA and the simulation results in Figure 2.22 very well: as N increases, t_{50} and σ decrease. All the values of t_{50} and σ for different links are listed in Table 2.3.

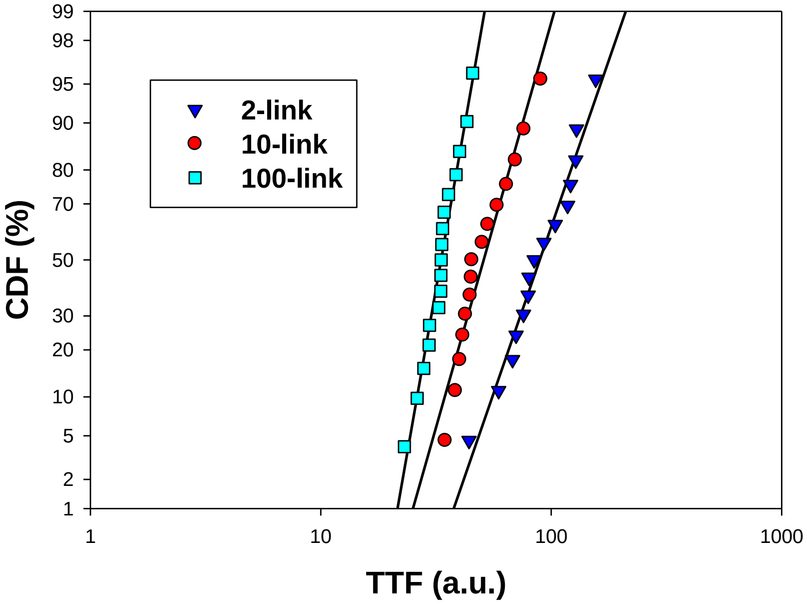


Figure 2.29 Intrinsic failure time distribution for multi-link structure with N = 2, 10 and 100.

2.4.4 Statistics for R_{step} and R_{slope}

The R_{step} and R_{slope} are then extracted from the EM resistance traces and their distributions are plotted in Figure 2.30 and 2.31 respectively. The statistics of R_{step} and R_{slope} exhibit lognormal distributions as well. And a clear trend can be found in the figures: as N increases, R_{step} decreases and R_{slope} increases, which agrees with the previous assumption. Since R_{step} and R_{slope} are proportional to the critical void volume and diffusivity respectively, this indicates that as N increases, the critical void volume decreases while the diffusivity after line failure increases. This trend is also consistent with the weakest link model in that the earlier failure occurring in a line, less mass depletion is required to induce failure while driven by a faster mass transport.

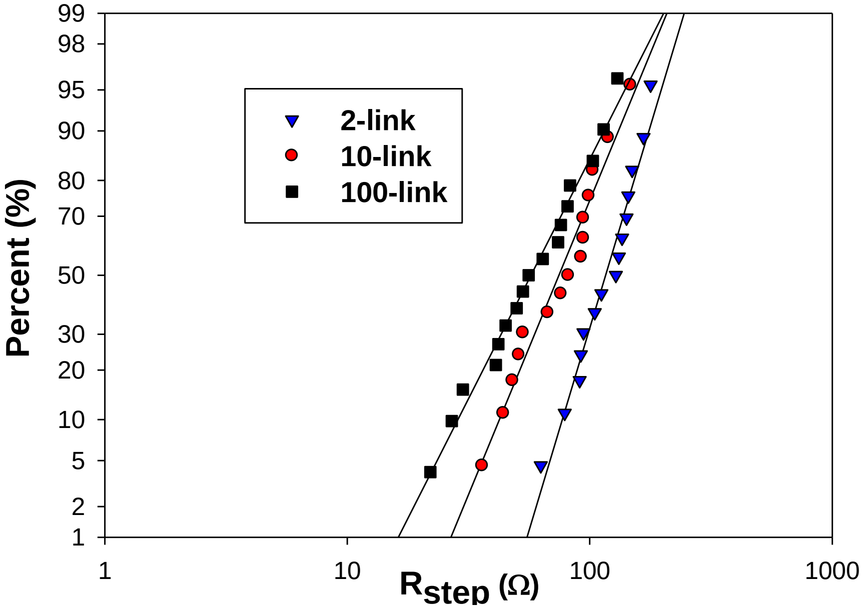


Figure 2.30 R_{step} distribution for multi-link structures with $N = 2$, 10 and 100.

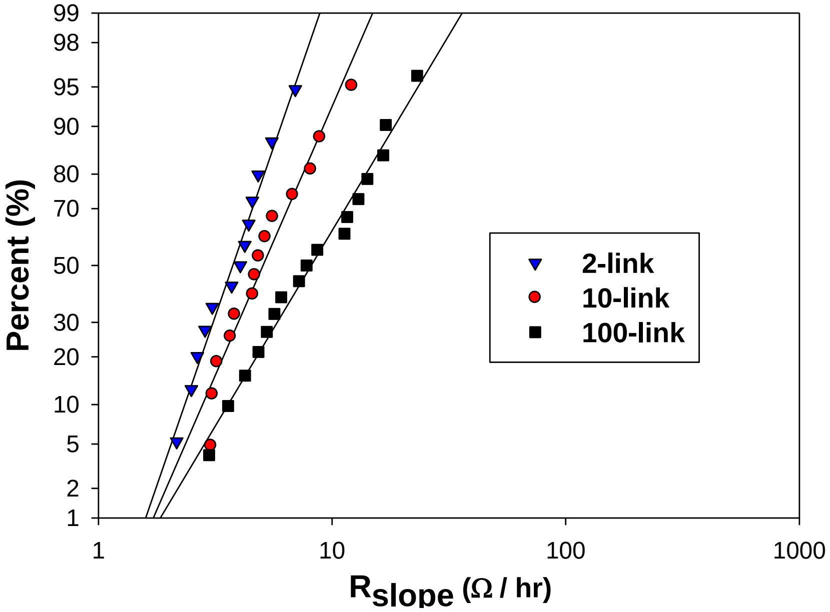


Figure 2.31 R_{slope} distribution for multi-link structures with $N = 2$, 10 and 100.

Note that the critical void volume and diffusivity discussed here are specific to the line which failed the earliest among N links. They are not the average values among N lines. One should expect the average values to be independent of N since each line experienced the same process conditions and any statistical variation should be averaged out if all N lines were taken into account.

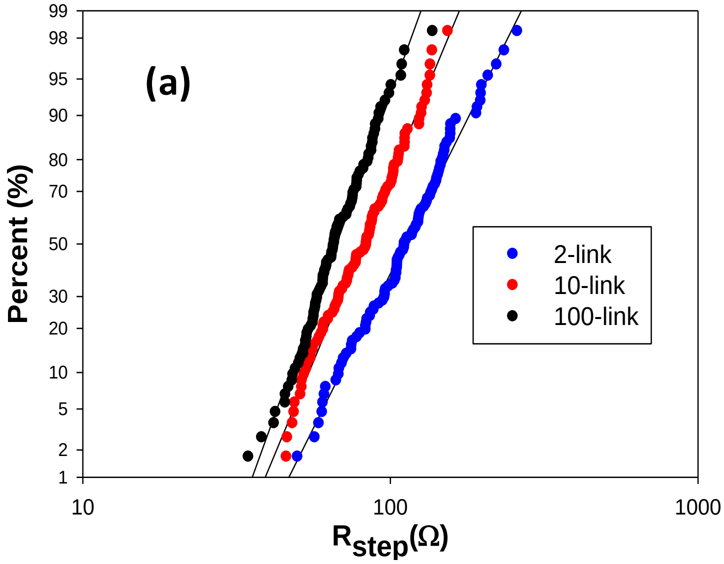
Another trend shown in Figure 2.30 and 2.31 is that the standard deviation σ increases as link number N increases for both R_{step} and R_{slope} distribution. This is different from what has been observed for the failure time distribution such as shown in Figure 2.29. The implication of this result will be further discussed. Table 2.4 tabulates the median values of R_{step} (R_{step_50}) and R_{slope} (R_{slope_50}), and σ for 2-, 10-, and 100-link structures.

Table 2.4 Median value and standard deviation of R_{step} and R_{slope} for $N = 2$, 10 and 100.

		$N = 2$	$N = 10$	$N = 100$
R_{step}	$R_{step\ 50}$ (Ω)	116	73	57
	σ	0.32	0.44	0.54
R_{slope}	$R_{slope\ 50}$ (Ω/hr)	4.0	6.1	11.1
	σ	0.38	0.46	0.64

To better understand the R_{step} and R_{slope} distributions for multi-link structures, Monte Carlo simulations were also performed. In the simulations, R_{step} and R_{slope} were assumed to be independent of each other. In an N-link structure, the weakest link simply means the one with the smallest ratio between R_{step} and R_{slope}. In other words, the link with the smallest ratio between critical void volume and diffusivity fails first. Due to the lack of single-link structure, the 2-link distributions for R_{step} and R_{slope} are used as the base structure. The 10-link and 100-link can be considered as 5 and 50 of 2-link respectively.

The simulation results for R_{step} and R_{slope} shown in Figure 2.32 agrees with the experimental data in at least two aspects. Firstly, if the 2-link base follows a lognormal distribution as assumed, the 10-link and 100-link also follow lognormal distributions closely. Secondly, as N increases, R_{step} does decrease while R_{slope} increases.



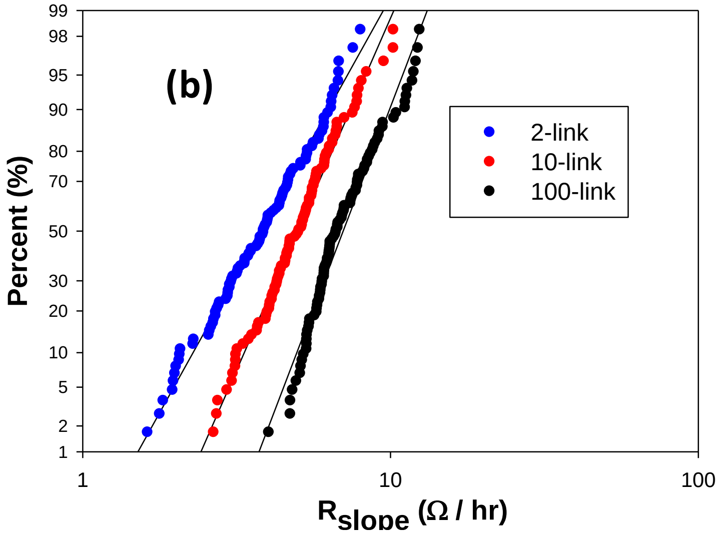


Figure 2.32 Monte-Carlo simulation of R_{step} and R_{slope} distributions for multi-link structures with link number $N = 2$, 10 and 100.

However, the deviation σ has a reversed trend compared to the experimental data: as N increases, σ for both R_{step} and R_{slope} decreases in simulations. The simulations are actually closer to intuition. This can be illustrated using R_{slope} as an example. The R_{slope} or diffusivity of each line in an N-link structure actually follows the same distribution from a 2-link base. When N increases, the R_{slope} of the earliest failed line tends to have a larger value, which is why the line fails first. In other words, one is selecting values for R_{slope} from a higher end of the base distribution, say 70%-100%. Plotting these values in a range of 0-100% certainly makes the curve steeper while leading to a smaller σ. The R_{step} can follow a similar analysis.

Here possible explanations of why the experimental σ increases with N are proposed. From Equation (2.3), R_{step} depends not only on the critical void volume, but also on the barrier cross-sectional area A_b and barrier resistivity ρ_b. Both of the parameters vary from line to line. So the measured R_{step} contains information of critical void volume coupled with noise from variation of A_b and ρ_b. When N increases, R_{step} becomes smaller. A smaller number is more sensitive to a probable constant noise which does not decrease with increasing N. Therefore, σ for R_{step} increases with N.

The fact that R_{slope} becomes larger when N increases may suggest that this parameter is less sensitive to the variation of A_b and ρ_b. However, in a multi-link structure, there are small voids formed in lines besides the one which has the first critical void, as illustrated in Figure 2.33. Each such small noncritical void causes a small resistance increase which is barely detectable. However, the resistance variation caused by a large amount of such small voids in multi-link structures is not negligible. And the number of such voids increases with N, which results in an increased σ for R_{slope}.

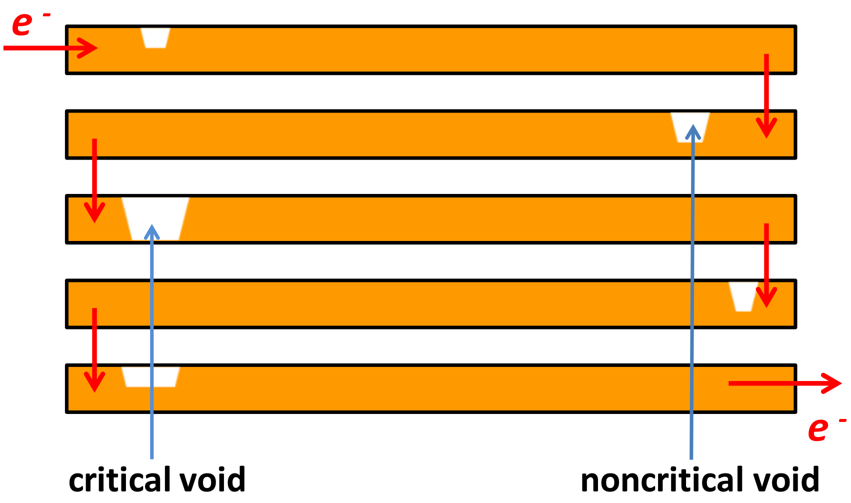


Figure 2.33 Schematic showing small void formation in lines of multi-link structure. The critical void causes line failure. While the noncritical void causes small resistance increase.

Therefore, the change of deviation σ with the increasing N is a result of competition between the decrease due to weakest link statistics and the increase due to processing variations of barriers and small voids formed in the lines. The observed increase of σ, as N increases from 2 to 10 and 100, demonstrates that the noise from barrier variation and small void formation is more important in this range. Due to the lack of single link data, it is difficult to estimate which factor is more important when N increases from 1 to 2. It is reported that the σ of R_{step} and R_{slope} is comparable to that of failure time t_f for single link structures [Arnaud *et al.*, 2011]. However, the 2-link data shows a much smaller σ for R_{step} (0.32) compared to t_f (0.37 for 2-link and 0.44 for deconvoluted single link). This suggests that the weakest link statistics shown in the simulation of Figure 2.32 may be more important in comparison to σ when N changes from 1 to 2.

2.4.5 Comparison between t_{f_calc} and t_f

The above discussion on the failure statistics can be extended to compare the measured failure time t_f with the calculated failure time $t_{f\_calc} = R_{step}/R_{slope}$. As discussed in the last two sub-sections, these parameters are subject to statistical variation. To obtain a meaningful correlation, the median values from the lognormal distributions are used in the comparison as shown in the red curve in Figure 2.34.

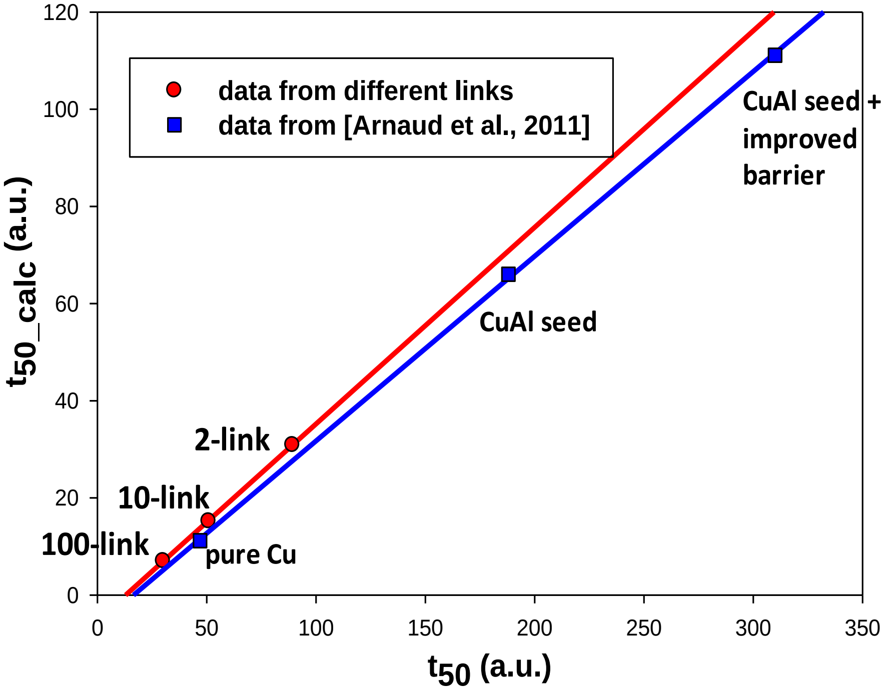


Figure 2.34 Comparison between the calculated median failure time t_{50_calc} based on R_{step}/R_{slope} and the measured median failure time t_{50}.

The correlation fits a linear relation well, indicating that the void growth rate at Stage I, $v_{d,I}$, is linearly correlated to that at Stage III, $v_{d,III}$. However, instead of a direct correlation with a slope of 1, a slope of 0.4 is obtained. And the curve intercepts with the *x*-axis instead of passing through the origin of the coordinates. These two feature suggests that $v_{d,I}$ is smaller than $v_{d,III}$. Also presented in Figure 2.34 are data from another study for Cu single-link structures at 45nnm node with diffusivities changed by Al doping (1%) or barrier improvement [Arnaud *et al.*, 2011]. The line width, height and length used in such studies are 63nm, 140nm and 225 μm respectively, embedded in low-k dielectric with k 2.5. The testing temperature is 300°C. The latter data also show a linear correlation of t_{50_calc} *vs* t_{50}, remarkably similar to the data from the multi-link structures. This suggests that the difference in the void growth rates at Stages I and III is not unique to the samples in this study.

To confirm that the void growth rate is different at Stages I and III, a survey of other explanations is carried out for the curves in Figure 2.34. We assume first that $v_{d,I}$ equals to $v_{d,III}$, then one can follow [Arnaud *et al.*, 2011] to extrapolate the resistance trace at Stage III down to Stage I, where it intercepts the trace at time t_0, as shown in Figure 2.35 (a). Apparently,

$$t_0 = t_f - R_{step} / R_{slope} . \tag{2.17}$$

Since the time required for the void to grow large enough to fail the line is R_{step} / R_{slope}, one can then define an incubation time for dopant to be depleted as time t_0 before the void can be initiated [Arnaud *et al.*, 2011]. However, the multi-link samples used in this study is capped with a standard SiCN layer and there is no doping in the seed layer. However, a similar phenomenon of t_0 is still observed in this study as shown Figure 2.35 (b). This suggests an incubation time for dopant depletion as defined by extrapolation of the resistance trace is not appropriate.

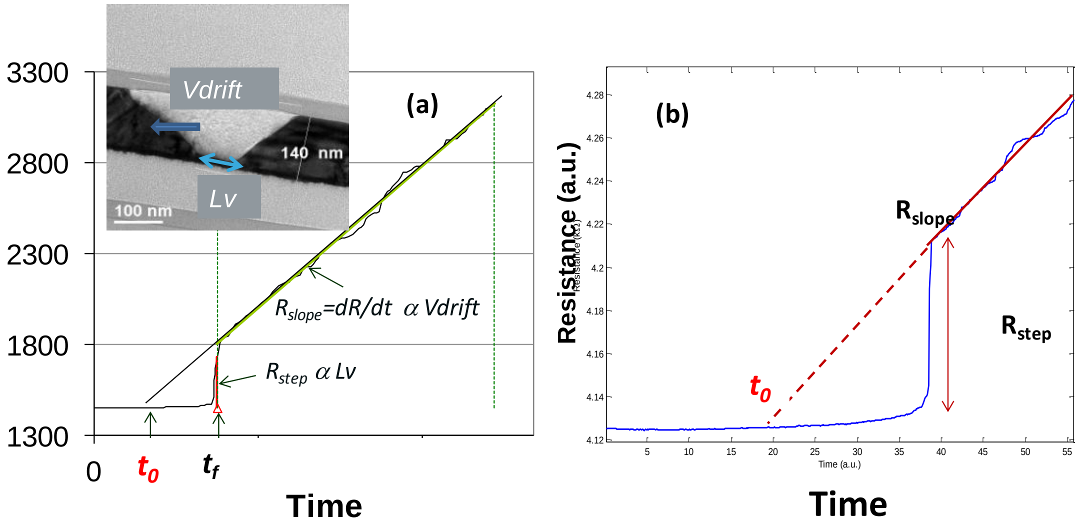


Figure 2.35 (a) Extrapolation of the resistance trace to define incubation time t_0 for dopants. [Arnaud *et al.*, 2011] (b) Extrapolation performed on a resistance trace of the multi-link samples.

Another possibility for t_0 is the void nucleation time which was neglected in the previous analysis. If the line before testing was void-free, the cathode of the line would evolve into a tensile stress state while the anode into compressive stress state, driven by the electron wind force, as illustrated in Figure 2.36. When the tensile stress reaches a critical value σ_{crit}, the metal line yields and a void forms. This time period is so called void nucleation time t_n and it has been calculated that [Korhonen *et al.*, 1993b]

$$t_n = bkT \exp(\frac{E_a}{kT})(\frac{\sigma_{crit}}{j})^2 , \tag{2.18}$$

where E_a is the activation energy, b is a constant. It is easy to show that

$$t_n \propto \frac{1}{D} \propto \frac{1}{R_{slope}} . \tag{2.19}$$

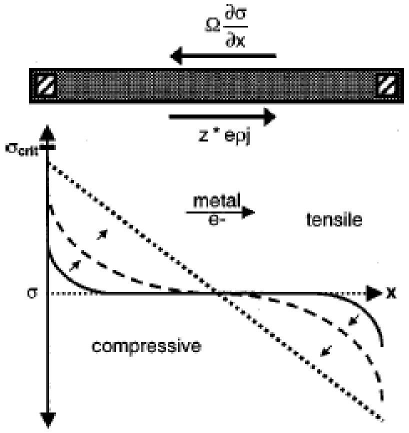


Figure 2.36 Stress evolution of a void-free metal line under EM. [Hau-Riege, 2002]

Therefore, if t_0 observed were the void nucleation time t_n, it should be proportional to $1/R_{slope}$. A plot of t_0 vs $1/R_{slope}$ is shown in Figure 2.37 which does not follow a linear curve. This suggests that void nucleation alone cannot explain the experimental data. Therefore, a different void growth rates at Stage I and III seems to be the only possible explanation to account for the result observed in Figure 2.34.

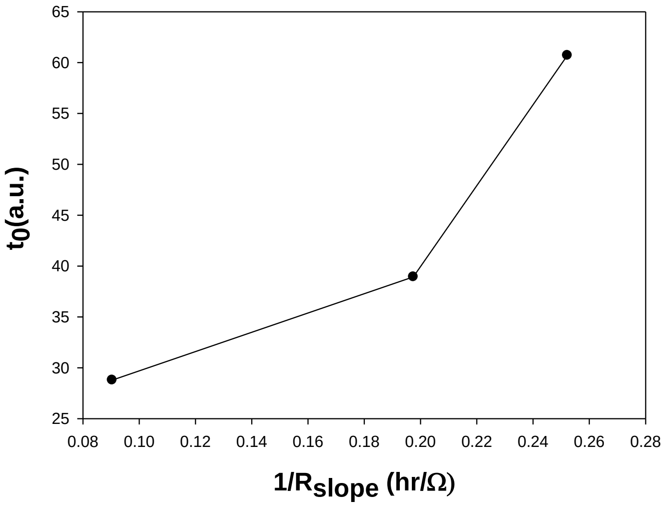


Figure 2.37 The plot of t_0 vs $1/R_{slope}$ showing void nucleation time cannot explain the observed phenomenon.

2.5 CONCLUSIONS

A method has been developed to extract the void growth rate at Stage I (before failure) from resistance traces recorded during EM. Based on the analysis, standard EM test structures can be used to determine the void growth rate and the EM failure time. According to this method, the calculated failure time based on R_{step} and R_{slope} is compared to the measured failure time. The difference between these two failure times reveals the difference of the void growth rates at Stage I and Stage III which can be determined in EM tests.

EM tests were performed on multi-link structures to statistically vary the failure time, R_{step} and R_{slope}. The failure time statistics was found to follow the weakest link approximation. Deconvolution of the multi-link failure time to single-link failure time confirmed that the failures occur via a single intrinsic mode. The TCR and Joule heating measurement ruled out the temperature difference between different structures in the test link. The R_{step} and R_{slope} distributions were obtained from the resistance traces. Both failure analysis and R_{step} values show that the lines failed due to formation of trench type voids. Monte Carlo simulations for R_{step} and R_{slope} show a similar trend as the measured results, except that they do not have similar statistical deviations. Possible explanations were proposed for this result. A comparison between the calculated and the measured failure time shows a linear curve but with a slope of about 0.4 and the curve does not pass the origin. This suggests the void growth rate at Stage I is smaller than that at Stage III. Further modeling study will be performed in the next chapter to understand the experimental results reported here.

Chapter 3: Stress Modeling for Initial Void Growth in Cu Interconnects

A kinetic model is developed in this chapter to analyze the initial void growth induced by electromigration in Cu interconnects. The approach is based on the kinetic model first formulated by Korhonen's analysis on stress evolution in confined metal lines. The Korhonen model is extended to the initial void growth from the Cu/cap interface taking into account the stress effect and the void formation process. The new model shows that the initial void growth rate in Stage I is different from the void growth rate in Stage III after line failure although the two growth rates can be quantitatively correlated. The correlation deduced from the stress model agrees well with the results reported in Chapter 2. Grain structure is a prerequisite for the stress model, which is simulated based on the Potts model considering interconnect structures with both lines and overburdens.

3.1 REVIEW OF EM MODELS

3.1.1 Introduction of EM Models

Before the 1990s, the electromigration (EM) induced voiding was understood as vacancy migrating along grain boundaries and accumulating at flux divergent sites of blocking boundaries, which leads to failure [Shatzkes *et al.*, 1986]. It became clear later that such a model is unreasonable since there are many sinks readily available in the metal conductor for the vacancies to annihilate [Lloyd, 2002]. This led to later analyses taking into account the effect of mechanical stress induced by mass transport under EM. Kirchheim formulated a model to calculate the generation of tensile and compressive stress by annihilation and production of vacancies at the anode and the cathode respectively [Kirchheim *et al.*, 1991, Kirchheim, 1992]. A year later, Korhonen proposed a kinetic model to account for void formation driven by the stress evolution due to EM in confined metal lines [Korhonen *et al.*, 1993b]. The Korhonen model analyzed the void formation kinetics as a result of stress evolution taking into account the effect of grain structure on mass transport in the confined line structure. The interconnect lines are embedded in multi-level structures where the stress in such confined metal lines is primarily hydrostatic and can be quite large. When the stress level in the line is built up beyond a certain threshold, void formation is initiated, leading to eventual line failure. The Korhonen model is a widely used model for EM and was implemented in simulation tools [Hau-Riege *et al.*, 2001].

3.1.2 the Korhonen Model

The model to be developed in this chapter is based on the Korhonen model. So a derivation and introduction of the Korhonen model is included here. The central theme of the model is that the buildup of mechanical stress in the metal line is induced by depletion or accumulation of local atom concentrations. This can be represented by a linear relationship within the linear elasticity range.

$$\frac{dC_a}{C_a} = -\frac{d\sigma}{B}, \tag{3.1}$$

where C_a is atomic concentration, σ the mechanical stress and B the effective bulk modulus of the confined metal line. The atomic concentration is correlated to the atomic flux J through the continuity equation, which in 1-D case is

$$\frac{dC_a}{dt} + \frac{dJ}{dx} = 0. \tag{3.2}$$

Therefore,

$$\frac{d\sigma}{dt} = \frac{B}{C_a}\frac{dJ}{dx}. \tag{3.3}$$

The atomic flux also has a simple relation with atomic concentration as

$$J = v_d C_a, \tag{3.4}$$

where v_d is the drift velocity with $v_d = \mu F$. Here the mobility μ follows the Einstein relation

$$\mu = \frac{D}{k_B T}, \tag{3.5}$$

where D is the diffusivity, k_B the Boltzmann constant, T the absolute temperature. And each atom receives a driving force F consisting of both EM driving force and mechanical stress gradient induced backflow force

$$F = Eq^* + \Omega\frac{d\sigma}{dx}, \tag{3.6}$$

where Ω is the atomic volume having $\Omega = 1/C_a$. E and q^* is electric field and effective charge respectively. Then the atomic flux (3.4) can be expressed as

$$J = \frac{D}{k_B T}(\frac{d\sigma}{dx} + Eq^* / \Omega). \tag{3.7}$$

Substituting Equation (3.7) into Equation (3.3), one has the stress evolution equation in the Korhonen model as

$$\frac{d\sigma}{dt}=\frac{d}{dx}\left[\kappa\left(\frac{d\sigma}{dx}+\gamma\right)\right], \tag{3.8}$$

where the effective diffusivity $\kappa = DB\Omega/k_BT$ and the effective EM driving force $\gamma = Eq^*/\Omega$.

The differential equation for stress evolution in (3.8) is similar to a diffusion equation or heat conduction equation except for the additional driving force term γ. Therefore solutions are readily available in many references [Carslaw *et al.*, 1959] for various boundary conditions. Separation of variables and Laplace transformation are techniques commonly used to solve the equation. Without any void present initially, a blocking boundary condition applies and the stress evolution follows the curves shown in Figure 2.36. Finally voids nucleate when the tensile stress at the cathode is larger than the yield stress. The time to reach that point is the void nucleation time given in Equation (2.18) which was originally deduced by Korhonen [Korhonen *et al.*, 1993b].

3.1.3 Void Growth in the Korhonen Model

When a void is present in the line, the surface or boundary of the void is in a stress free state. In the case as shown in Figure 3.1(a), the boundary condition for $x = 0$ is $\sigma = 0$, while the blocking boundary condition still applies to $x = L$. Then the mechanical stress evolution can be schematically shown in Figure 3.1(b) where the stress over the entire line is in a compressive (negative) stress state. An analytical solution for the stress evolution can be derived as [Korhonen *et al.*, 1993a]

$$\sigma'=-\gamma\left[x-2L\sum_{n=1}^{\infty}(-1)^n\exp(-m^2\kappa t/L^2)\sin(mx/L)/m^2\right], \tag{3.9}$$

where $m = (n - 1/2)\pi$. Assuming a constant thermal stress σ_T existing throughout the line, except at $x = 0$ where $\sigma = 0$, before the start of EM at time $t = 0$, the relaxation of the thermal stress leads to another mechanical stress term evolving as [Korhonen *et al.*, 1993a]

$$\sigma'' = 2\sigma_T \sum_{n=1}^{\infty} \exp(-m^2 \kappa t / L^2) \sin(mx/L)/m \, . \tag{3.10}$$

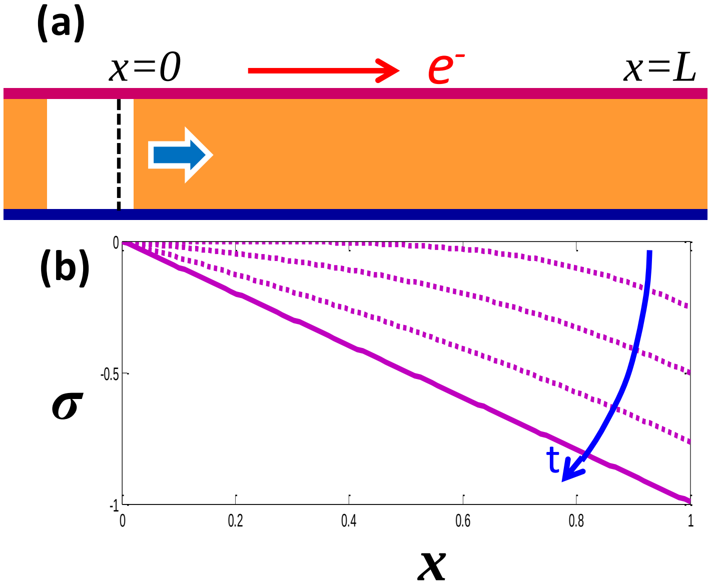


Figure 3.1 (a) Schematic for a metal line with a void at cathode; (b) stress evolution in the metal line as shown in (a).

In the kinetic model, Korhonen associated the void volume with the volume strain. That means the driving force squeezes atoms towards the anode and this atomic redistribution provides space for the void to expand. In this case, the void volume can be expressed as:

$$V(t) = \frac{1}{B} \int_0^L \left[\sigma_i(x,t) - \sigma_f(x,t) \right] dx \, , \tag{3.11}$$

where σ_i and σ_f are the initial stress and the final stress respectively. Note that in the Korhonen's original paper the void volume is written as $V(t) = (1/B)\int_0^L \sigma(x,t)dx$ [Korhonen *et al.*, 1993a] which is probably a typo since in the subsequent analysis, the void volume is defined in accordance of Equation (3.11). Also note that, in Equation (3.11), the void volume is normalized by the line cross-sectional area A. This leads to the following analytical solution for the void volume:

$$V(t) = V_{sat}[1 + 4\sum_{n=1}^{\infty} \frac{(-1)^n}{m^3} \exp(-m^2 \frac{t}{\tau})] + \frac{\sigma_T L}{B}[1 - 2\sum_{n=1}^{\infty} \frac{1}{m^2} \exp(-m^2 \frac{t}{\tau})], \qquad (3.12)$$

where V_{sat} is the saturated void volume and τ is the time for the void grow to volume V_{sat}. These parameters are expressed in the following equations.

$$V_{sat} = Eq^* L^2 / 2B\Omega = Z^* e\rho j L^2 / 2B\Omega. \qquad (3.13)$$

$$\tau = L^2 k_B T / DB\Omega . \qquad (3.14)$$

In Equation (3.13), Z^* is the effective charge number, e the electron charge, ρ the resistivity of the metal line, and j the current density. Figure 3.2 plots the void growth based on Equation (3.12). It clearly shows that the void volume will reach a steady state due to the balance between EM driving force and stress gradient induced backflow force. The saturation volume is larger if there is an initial tensile thermal stress.

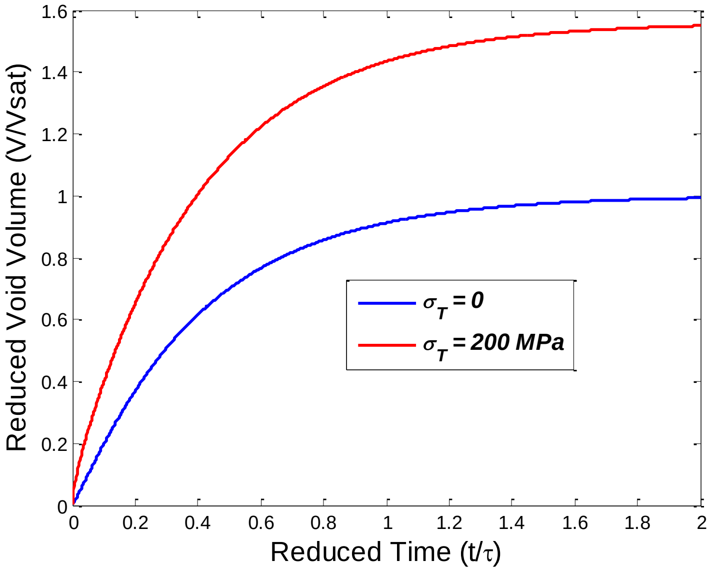


Figure 3.2 Void growth in the Korhonen model with initial stress 0 and 200 MPa.

3.1.4 Microstructure-based Statistical Model

Reliability is a statistical problem, thus, when a group of identical lines are tested, their lifetimes obtained are statistically distributed. This makes the modeling of failure time statistics to be equally important as the modeling of median failure time. Korhonen modeled the EM failure time statistics based on the microstructure distribution [Korhonen *et al.*, 1993a].

When Korhonen developed the statistical EM model, his analysis was aimed at the Al-based interconnect with grain boundaries as the major diffusion path. The Al line usually is composed of a series of multiple bamboo segments mixing with multi-grain segments called clusters, as shown in Figure 3.3. Due to the fact that the diffusivity in cluster segments is much larger, the boundary between a cluster and a bamboo is essentially a blocking boundary. Therefore the Al line can be modeled as a series of independent failure units with each having a cluster and a bamboo. The void growth in each failure unit starts with the mass transport in the cluster first, then extends into the bamboo segment. With a relatively long bamboo segments, a direct correlation between the cluster length and the failure time of the unit can be set, $L = L(t)$. The failure probability $F(t)$ of the unit at time t is the probability that its cluster length is longer than $L(t)$. If $G(L)$ is the statistical distribution of cluster length [Korhonen *et al.*, 1993a],

$$F(t) = 1 - G(L). \tag{3.15}$$

Based on the weakest link approximation for the independent failure units, the CDF of N units in a line is [Korhonen *et al.*, 1993a]

$$F_N(t) = 1 - [1\text{-}F(t)]^N = 1 - [G(L)]^N. \tag{3.16}$$

Equation (3.16) is the relationship correlating the failure time statistics with the microstructure (cluster length) distribution.

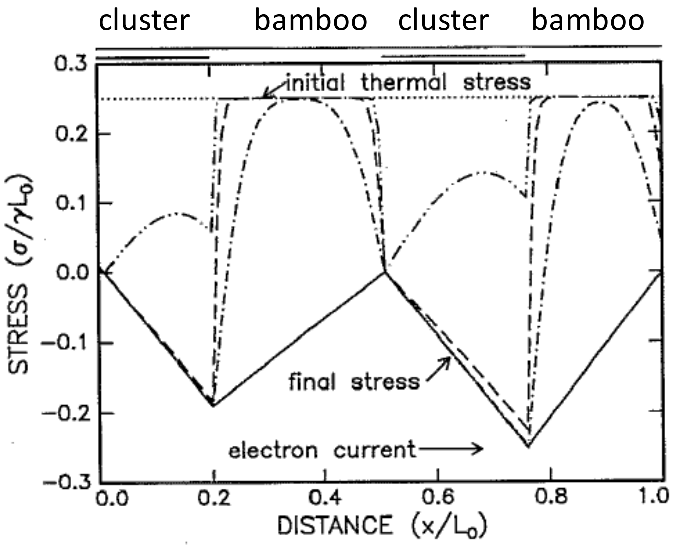


Figure 3.3 Cluster and bamboo segments in a metal line and the stress evolution in each segment. [Korhonen *et al.*, 1993a]

In general, the Cu interconnects are composed of bamboo grains mixing with poly-grain structures when the line width is below 90nm. When the Cu/cap interface diffusion is suppressed by metal capping, the characteristics of the microstructure and mass transport are very similar to that of the Al interconnects. Recently, the statistical model formulated by Korhonen was applied to Cu interconnects with CoWP capping [Zhang, 2010, Zhang *et al.*, 2011].

While this statistical model seems to be able to account for most of the EM statistics observed, some important effects have not been accounted for. For example, the failure units are assumed to be independent of each other so that the weakest link approximation can be used. However, two neighboring clusters can interact with each other by linking through a relatively short bamboo segment [Brown *et al.*, 1995b], as shown in Figure 3.4. This leads to a higher stress level in the cluster pair and can change the failure time and its statistics. Thus the weakest link approximation is no longer valid for such coupling clusters [Brown *et al.*, 1995a, Knowlton *et al.*, 1995] and one has to consider all the clusters in the line and their interaction simultaneously, which makes a simple analytical description not possible. The cluster coupling has been experimentally observed [Joo *et al.*, 1999] and simulated in [Liu *et al.*, 1997, Dwyer *et al.*, 2001].

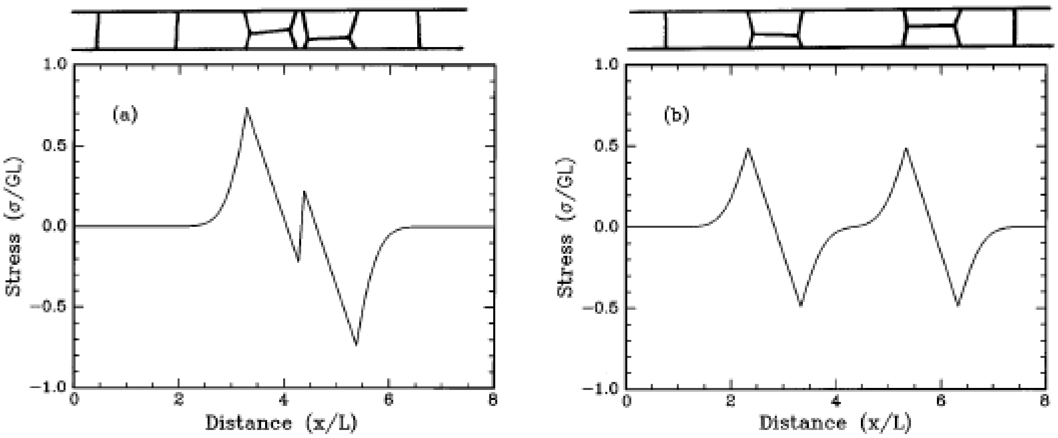


Figure 3.4 Stress profiles for an interacting (a) and non-interacting (b) cluster pairs. [Brown *et al.*, 1995b]

3.2 INITIAL VOID FORMATION MODEL

For a Cu interconnect line with standard SiCN capping, the diffusion at the interface dominates in EM. Rather than a weak coupling in Al interconnects as described in Section 3.1.4, two neighboring clusters in Cu interconnects strongly interact with each other. In fact, the interaction through interface diffusion is so strong that it may be improper to simply define bamboo and cluster segments in terms of the diffusivity difference as a base to apply the Korhonen model. In this sense, the weakest link statistical model (Section 3.1.4) proposed by Korhonen might not be better than that employed in the following analysis which considers the Cu line as a single segment with an effective diffusivity.

All the models described above analyze the void formation problem in 1D to obtain a simple analytical solution. The applicability of a 1D model is restricted to the case where the void evolution in the y (line height) and z (line width) direction is negligible compared with that in the *x* (line length) direction. This happens to be the case for void growth at Stage III described in Figure 2.2 and 2.4 as well as demonstrated in Figure 3.1. Thus the Korhonen's solution in Equation (3.12) should be only applicable to Stage III. For a void at Stage I in Cu interconnect, the void grows initially downward starting from the Cu/cap interface. The void evolution in the *y* direction is clearly not negligible at this critical stage. So the result deduced by Korhonen in Equation (3.12) does not adequately describe the void growth at Stage I for Cu interconnects, although it has been used by a number of authors [Hau-Riege, 2002, He *et al.*, 2004] in EM lifetime analysis without distinguishing the different void growth mode at Stage I and Stage III. In this section and what follows, the modeling of EM lifetime is specifically referred to void growth at Stage I. The void growth rate deduced will be compared with that obtained by Korhonen and verified using EM test data reported in Chapter 2.

In the following analysis, a rectangular void is used to represent the void growth mode shown in Figure 2.4. Such a rectangular void at stage I was also adopted by [Arnaud *et al.*, 2011] to simplify the analysis. Accordingly, consider a void with height *h* as shown in Figure 3.5. The presence of the void divides the Cu line into two regions: A and B. The stress evolutions in region A and region B are treated separately and the total void growth rate is the weighted sum of the void growth rate from region A and region B.

$$\frac{dV_I}{dt} = \frac{h}{H}\frac{dV_A}{dt} + \frac{H-h}{H}\frac{dV_B}{dt}, \qquad (3.17)$$

where *H* is the Cu line thickness.

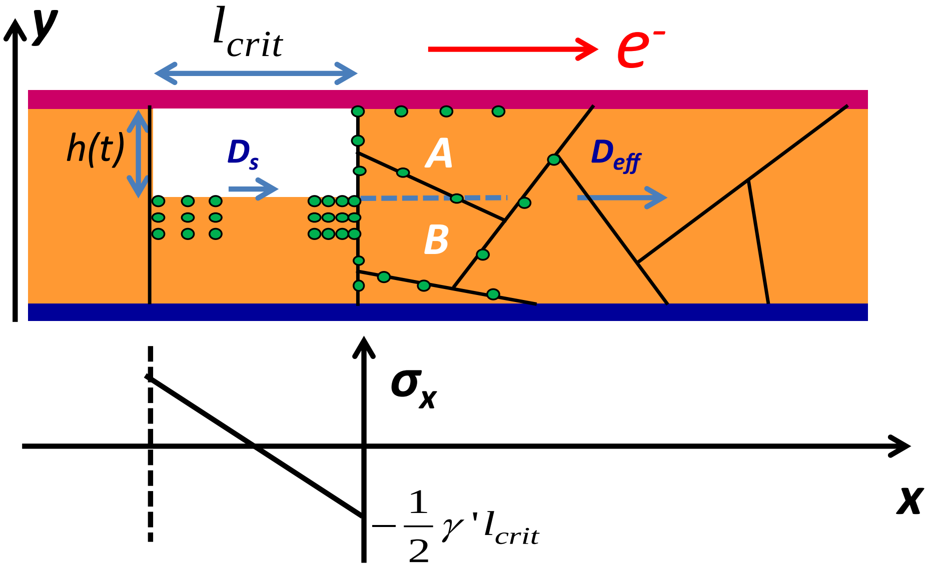


Figure 3.5 Schematic of void growth at Stage I and stress distribution inside the void segment.

The void is an effective sink of atoms, which makes the normal stress at the void boundaries to be zero. Therefore the stress evolution corresponding to void growth at region A is similar to that at Stage III as depicted in Figure 3.1(a). The void volume $V_A(t)$ normalized by h will follow Equation (3.12).

To obtain the stress evolution in region B, the stress inside the void segment is first analyzed. The void exposes a Cu free surface which has a diffusivity D_s much higher than the effective diffusivity D_{eff} inside the Cu line. It was reported that the Cu surface diffusivity is a few orders of magnitude larger than the diffusivity in the interface and grain boundaries [Arnaud *et al.*, 1999, Choi *et al.*, 2008, Choi *et al.*, 2011]. Within the void segment, atoms, represented by green dots in Figure 3.5, are squeezed toward the anode of the void segment. This leads to the presence of a stress gradient, shown in Figure 3.5, in the void segment to balance the EM driving force. One can use Equation

(3.14) to estimate the time to reach the balance. Due to the short length of a void and the high surface diffusivity, this process is estimated to take place within a minute which is negligible compared to EM failure time. The atoms at the anode of the void segment then leak through grain boundaries and interfaces in a relatively slow process, which leads to the growth of void. Any atom leakage is replenished quickly by the faster surface diffusion. So the stress at region B essentially remains at a constant level $-\frac{1}{2}\gamma' l_{crit}$ where $\gamma' = \frac{H}{H-h}\gamma$ due to the increased current density in the decreasing Cu cross-section remaining in the void segment. The solution for the stress evolution with such boundary conditions is readily available. Although a void close to the via is under investigation, the relatively fat cathode, as shown in the layout in Figure 2.6(a), provides enough Cu atom source in the upstream of the void. It is expected that the EM mass flux can provide an equivalent number of atoms to and from the void leading to negligible effect on void growth at region B. Such an analysis is similar to the one used in Ref. [Korhonen *et al.*, 1993a] to deduce the EM mass flux in a line with the bamboo/cluster type of microstructure. Then one can focus on the void growth induced by mechanical stress evolution at region B only, since the line length for $x < -l_{crit}$ is much shorter than $x > 0$. The mechanical stress evolution is then calculated as (for $x > 0$)

$$\sigma'' = (2\sigma_T + \gamma' l_{crit}) \sum_{n=1}^{\infty} \exp\left[-\frac{m^2}{L^2}\kappa t \right] \sin(\frac{mx}{L}) / m. \qquad (3.18)$$

And the void growth induced by this stress evolution is

$$V_B(t) = \frac{(2\sigma_T + \gamma' l_{crit})L}{2B}[1 - 2\sum_{n=1}^{\infty} \frac{1}{m^2} \exp(-m^2 \frac{t}{\tau})]. \qquad (3.19)$$

The void growth rate at Stage I can now be obtained using the expressions of $V_A(t)$ in Equation (3.12) and $V_B(t)$ in Equation (3.19). However, the diffusivity which is implicitly contained in the void volume through time constant τ remains to be specified. Since A and B are two different regions in the line cross-section, the diffusivities associated with them should be different. They are denoted as D_A and D_B respectively.

The effective diffusivity for a Cu line with thickness H is expressed as

$$D_{eff} = \frac{\delta_N}{H} D_N + \frac{\delta_{GB}}{d} D_{GB}, \tag{3.20}$$

where D_N and D_{GB} are diffusivities along Cu/cap interface and grain boundary respectively, δ_N and δ_{GB} are the effective width of the interface and grain boundary, respectively, d is the average grain size. Since the thicknesses of region A and B evolve with time, the diffusivity D_A and D_B should be time or h dependent as well. Only if all the diffusion paths are uniformly distributed along the Cu line, one can have $D_A = D_B$ as a constant. Since the Cu/cap interface is restricted to the top surface which is closer to A, one should expect $D_A > D_B$ assuming that the grain boundaries are uniformly distributed through the line cross section. Quantitatively, the local grain structure is required to determine the diffusivities. In lieu of measured grain structures, Monte Carlo simulations of grain growth based on the Potts model are performed to obtain the grain distribution and the details are described in Section 3.4. The simulation results reveal that there are more small grains located at the bottom of the line, as shown in Figure 3.18(d) and 3.20 as examples. This may partially cancel out the non-uniformity of diffusion paths caused by interface diffusion. To simplify the following analysis, it is assumed that the averaged diffusivities of region A and region B are equal, i.e. $\bar{D}_A = \bar{D}_B = D$.

The average void growth rate required for determining the failure time is obtained by averaging over H to yield a tractable solution. Assuming that there is an ensemble of Cu lines with different void thickness h varied from 0 to H, where the voids in these lines start to grow with different growth rates. The averaging of void growth rate over H

resembles an ensemble average over all these lines. In this way, the average void growth rate in Stage I is represented by the following expression:

$$V_I(t) = \frac{1}{2}V_{sat}\left[1+4\sum_{n=1}^{\infty}\frac{(-1)^n}{m^3}\exp(-m^2\frac{t}{\tau})\right] + \frac{(2\sigma_T+\gamma l_{crit})}{2B}L\left[1-2\sum_{n=1}^{\infty}\frac{1}{m^2}\exp(-m^2\frac{t}{\tau})\right]. \quad (3.21)$$

The first term in Equation (3.21) is the contribution from EM, while the second term is from thermal stress. For convenience, one denotes the terms in the first and second bracket pairs in Equation (3.21) as A_{EM} and A_σ respectively, i.e., $A_{EM} = \left[1+4\sum_{n=1}^{\infty}\frac{(-1)^n}{m^3}\exp(-m^2\frac{t}{\tau})\right]$ and $A_\sigma = \left[1-2\sum_{n=1}^{\infty}\frac{1}{m^2}\exp(-m^2\frac{t}{\tau})\right]$.

To further simplify the solution, one can check the time scale under discussion. With L = 100μm, B = 7.5 GPa [Oates *et al.*, 2009a], $\Omega = 1.18*10^{-29}$ m^3 [He *et al.*, 2004], k_BT = 0.052eV at 330°C, and diffusivity $D = 10^{-12}$ cm^2/s at 330°C [Zhang, 2010], the void saturation time τ can be estimated to be about 2600 hours, according to Equation (3.14). All the failure time t_f measured in the experiments in chapter 2 are less than 200 hours. This indicates that the actual time scale for line failure $t \ll \tau$ the time required to reach the steady state of void growth. At this short time scale, the EM flux term can be approximated as one with linear t dependence and stress flux term can be approximated as one with a square root t dependence. As shown in Figure 3.6, $2*t/\tau$ approximates A_{EM} well when t is within 15% of τ and A_σ coincides with $(2/\sqrt{\pi})*\sqrt{t/\tau}$ in a time scale up to 40% of τ. With this approximation, the void volume normalized by line cross-section A for Stage I ($V_I(t)$) and Stage III ($V_{III}(t)$) are further simplified as

$$V_I(t) \approx V_{sat}\frac{t}{\tau} + \frac{1}{\sqrt{\pi}}[\frac{2\sigma_T}{B} + \frac{\gamma l_{crit}}{B}]L\sqrt{t/\tau}, \quad (3.22)$$

$$V_{III}(t) \approx 2V_{sat}\frac{t}{\tau} + \frac{2}{\sqrt{\pi}}\frac{\sigma_T}{B}L\sqrt{t/\tau}. \quad (3.23)$$

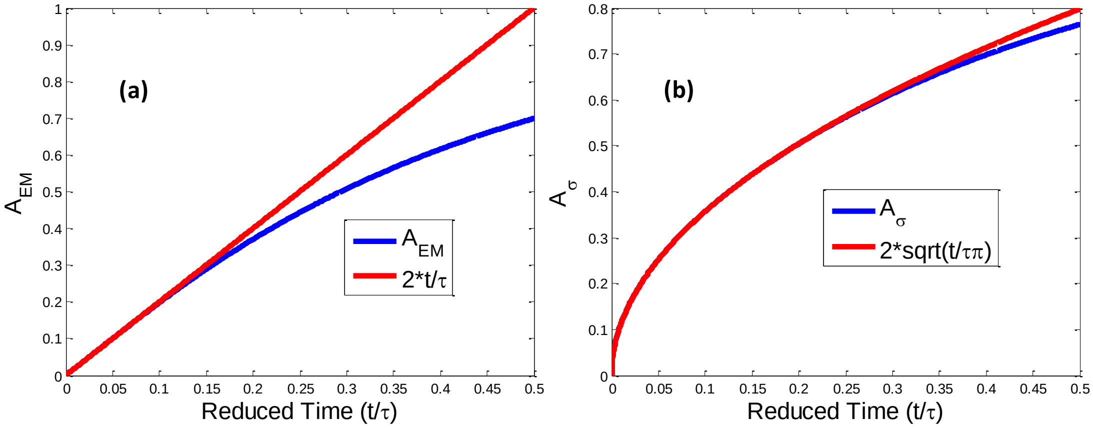


Figure 3.6 Within a short time scale, A_{EM} can be approximated by $2*t/\tau$ (a), and A_σ can be approximated by $(2/\sqrt{\pi})*\sqrt{t/\tau}$ (b).

3.3 INITIAL VOID GROWTH RATE RESULTS AND DISCUSSION

The coefficients of the leading linear term in Equation (3.22) and (3.23) differ by a factor of 2. With the material constant set: $Z^* = 1$, $j = 1$ MA/cm^2, $\rho = 5.8*10^{-6}$ Ω-cm (from measurement at 330°C), $\Omega = 1.18*10^{-29}$ m^3 [He *et al.*, 2004], $L = 100$µm, $B = 7.5$ GPa [Oates *et al.*, 2009a], one has $V_{sat} = Z^* e\rho jL^2 / 2B\Omega =$ 5.25 µm. This is much larger than $\gamma l_{crit}L/B$ due to the relatively small void length l_{crit} of about 100nm. Therefore, for an initial zero stress, the ratio of void growth rates between Stage I and Stage III is about 0.5, i.e., $dV_I/dt \sim 0.5\ dV_{III}/dt$, which is demonstrated in Figure 3.7. This value is very close to the slope of 0.4, observed in Figure 2.34. While this is encouraging, to reach a ratio below 0.5, however, a compressive (negative) thermal stress is required. It is worth noting that such a compressive stress in Cu lines under EM testing at 330°C is highly probable because of the relatively higher coefficient of thermal expansion (CTE) of low-k dielectric compared to Cu (17 ppm/°C). Indeed, a 250MPa compressive stress at this temperature range has been reported [Rhee *et al.*, 2003]. The results obtained by x-ray diffraction (XRD) measurement are shown in Figure 3.8. Finite element analysis has also confirmed the presence of compressive thermal stress in Cu lines along the length direction at EM test temperatures [Rhee *et al.*, 2003].

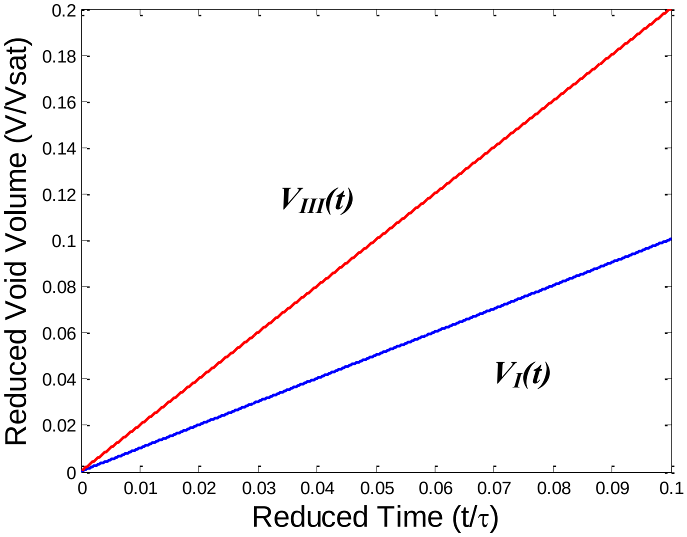


Figure 3.7 Void volume change with time at Stage I (lower curve) and Stage III (upper curve) shows a slope ratio of 0.5 when thermal stress is 0.

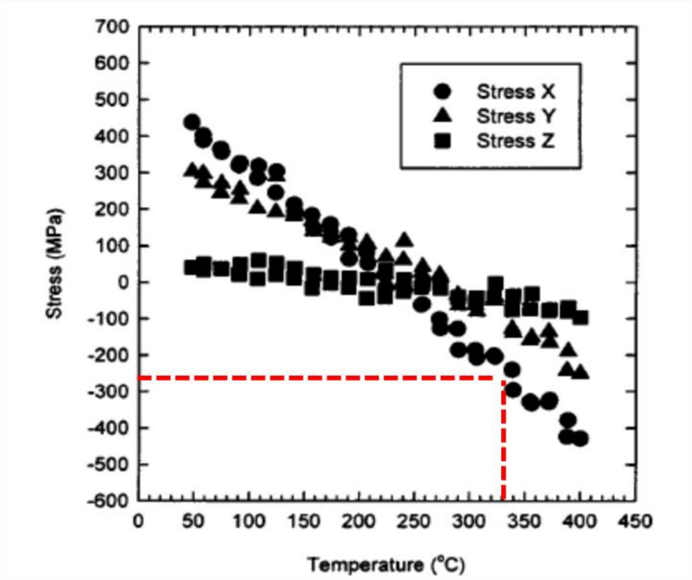


Figure 3.8 Thermal stress components of a Cu/low-k interconnect measured by XRD at different temperatures. X is in Cu line length direction. [Rhee *et al.*, 2003]

Figure 3.9 shows an example of void growth under a compressive stress of 50MPa, achieving a slope ratio between $V_I(t)$ and $V_{III}(t)$ of about 0.4. The effective charge number is chosen as $Z^* = 2$. One interesting feature of $V_I(t)$ shown in Figure 3.9 is that the void does not grow ($V_I(t)<0$) until certain time, t_σ, which represents a stress incubation time for void growth. This corresponds to the time period for the EM-induced stress to overcome the compressive stress so that void growth can begin. It only exists when initial thermal stress is compressive. From Equation (3.22), one can deduce the stress incubation time as:

$$t_\sigma = \frac{1}{\pi}\left(\frac{2\sigma_T + \gamma l_{crit}}{2B}\right)\left(\frac{L}{V_{sat}}\right)^2 \tau \approx b' kT \exp\left(\frac{E_a}{kT}\right)\left(\frac{\sigma_T}{j}\right)^2, \tag{3.24}$$

where b' is a constant and γl_{crit} (in the order of magnitude of MPa) is ignored in the last approximation. This expression is similar to the void nucleation time shown in Equation (2.18). The void nucleation time is the time period required for the EM induced stress to reach a critical stress σ_{crit} so that void can begin to grow. In that sense the formalism of stress incubation time is very similar to that of the void nucleation time. The difference is whether or not there is a preexisting void. This stress incubation time accounts for why the curves in Figure 2.34 do not pass the origin.

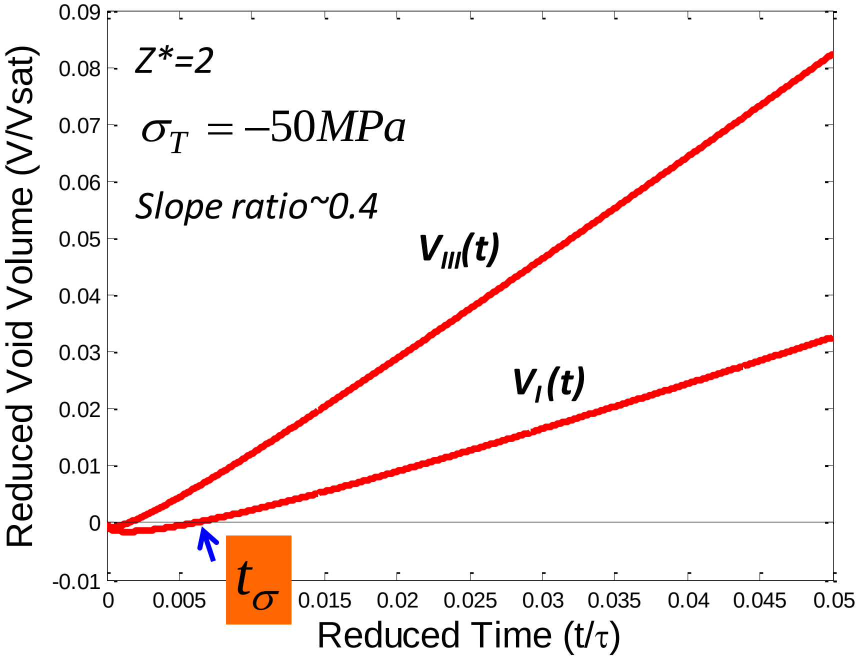


Figure 3.9 Void volume change with time at Stage I (lower curve) and III (upper curve) under compressive line stress.

The results from the void growth model can now be simplified and schematically represented as shown in Figure 3.10. After a stress incubation period, the void first grows from the cap interface downward in a vertical direction with a relatively small growth rate. This reaches essentially the end of Stage I where the line fails. After the line fails, the void growth changes to a horizontal growth mode with a relatively large growth rate. This represents the steady state void growth in Stage III. Note that the averaged void growth rate shown in Figure 3.10 is not a real time void growth rate. That is why the void growth rate shown in the Figure does not have smooth transitions at t_σ and t_f.

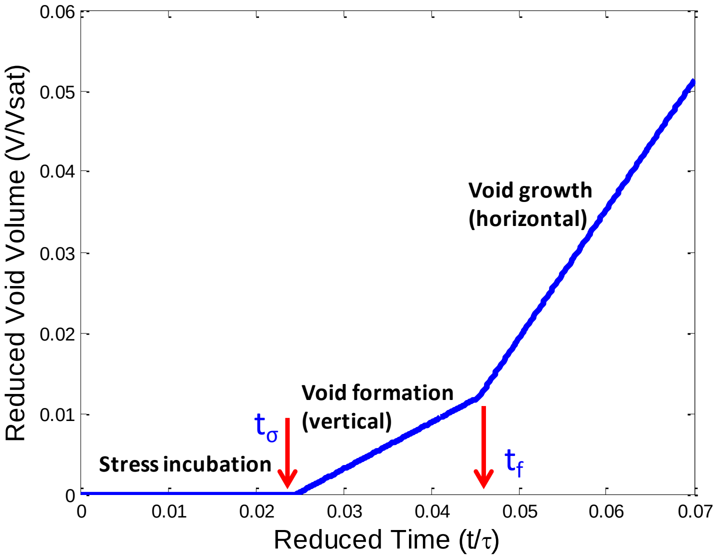


Figure 3.10 Simplified model of void growth at different stages.

Table 3.1 summarizes the EM behaviors of void growth and void nucleation. Equation (2.18) shows the failure time for void nucleation mode has j^{-2} dependence. The failure time for void growth mode depends on drift velocity, therefore it has j^{-1} dependence. A modified Black's equation uses variable current exponents:

$$t_{50} = Aj^{-n} \exp(\frac{E_a}{kT}) . \tag{3.25}$$

A value between 1 and 3 is commonly used for n to fit experimental data. A value for n = 1~2 accounts for the mixing of void nucleation and void growth for EM failure, while n > 2 is attributed to Joule heating [Lloyd, 2007]. Another important parameter for EM is the critical current density below which no EM failure would be observed. If no failure occurs when the back flow stress balances the EM driving force, the line then reaches immortality. For void nucleation, it happens if the current density is not big enough to generate sufficient stress at cathode to nucleate a void at that force balance point. The critical current density is [Oates *et al.*, 2009a]

$$\left(jl\right)_c = \frac{\Omega\sigma_{crit}}{eZ^*\rho}. \tag{3.26}$$

For void growth, immortality happens when the saturated void size is smaller than the critical void size to fail the line. From Equation (3.13), the critical current density can be expressed as [Oates *et al.*, 2009a, Korhonen *et al.*, 1993b]

$$(jl^2)_c = \frac{2\Omega Bl_{crit}}{eZ^*\rho}. \tag{3.27}$$

The thermal stress for both cases is neglected for simplicity. If a thermal stress (σ_T) exists, σ_{crit} in Equation (3.26) should be substituted for ($\sigma_{crit} - \sigma_T$), and l_{crit} in Equation (3.27) should be substituted for ($l_{crit} - \sigma_T L/B$).

Table 3.1 Summary of Failure time and critical current density for void nucleation and void growth.

	Failure time	**Critical current density**
Void nucleation	$t_f \propto j^{-2}$	$\left(jl\right)_c = \frac{\Omega\sigma_{crit}}{eZ^*\rho}$
Void growth	$t_f \propto j^{-1}$	$(jl^2)_c = \frac{2\Omega Bl_{crit}}{eZ^*\rho}$

Although the stress incubation time t_σ is derived from void growth case, its behavior resembles the void nucleation time. Since a fitting parameter (*b* or *b'*) is used in interpreting data, it is difficult to differentiate the nucleation from the growth effects, in spite of the fact that they have different origins. In subsequent study in this research, it is assumed that the failure is dominated by void growth, following Equation (3.22).

With this new model, one can now recalculate the failure time without assuming that the void growth rate at Stage I is identical to Stage III. The measured R_{step} and R_{slope} values are useful in providing critical void length and drift velocity as inputs for modeling calculations, as demonstrated below. The result shown in Figure 3.11 presents a curve approaching a slope of 1 and passing through the origin. This shows that the new model describes the void formation in Stage I well. The fitting parameters used $Z^* = 2.2$, $B = 7.8GPa$, $\sigma_T = -68MPa$ are all in the reasonable range. This indicates that the model developed for initial void growth has provided a valid theoretical base to account for the experimental data obtained from EM tests of Cu interconnects.

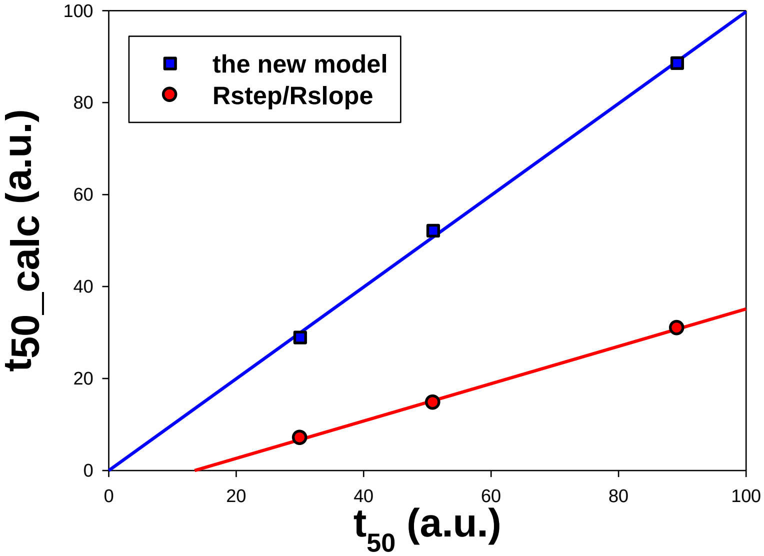


Figure 3.11 Comparison between calculated t_{50} based on the new model and measured t_{50}.

A simulation is then performed to calculate the time to failure (TTF) distribution using the measured R_{step} and R_{slope} statistics as input. The statistics of the simulation based on the new model agrees well with the 2-link experimental data, as shown in Figure 3.12. Also shown in the figure are TTF simulation based on Korhonen model and R_{step}/R_{slope}. They overlap with each other because both of them are concerned with the void growth at Stage III. This simulation also demonstrates that the resistance traces contain valuable statistical information for EM lifetime. This is because the information of critical void volume and the diffusivity contained in R_{step} and R_{slope}, respectively, is directly correlated to the EM failure time. Considering EM tests, the electrical resistance traces are relatively easy to obtain, particularly for a large ensemble of test structures. They provide information that cannot be easily observed by TEM, but also can be used in deducing EM lifetime statistics as demonstrated here.

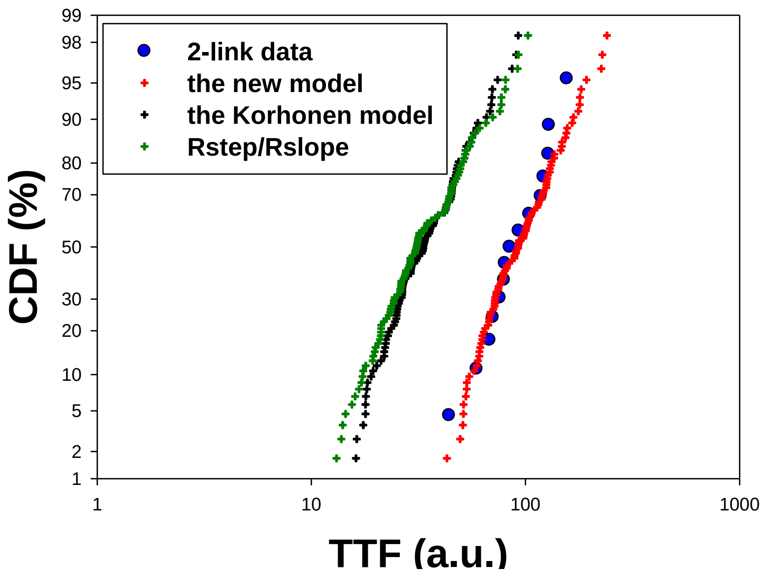


Figure 3.12 Failure time statistics simulation using R_{step} and R_{slope} distributions.

Finally, the stress effect on initial void formation is studied based on the new model. This is important because, although the Cu line may be under compression at EM test temperature, due to CTE mismatch between Cu and low-k, the line will be under tension at room temperature or chip operating temperature. The effect of thermal stress to EM lifetime has also been reported in Ref. [Hauschildt *et al.*, 2012]. Figure 3.13 plots the void growth at Stage I under two different stress states: compress stress of -100 MPa and tensile stress of 100 MPa. The parameters used are $Z^* = 2$, $j = 1$ MA/cm^2, $\rho = 5.8*10^{-6}$ Ω-cm, $L = 100\mu m$, $B = 7.5$ GPa. It demonstrates that the void growth under tension can be very different from that under compression. Overall, the void growth rate is faster since there is no time required to overcome the compressive stress to initiate void growth. This will result in a shorter EM lifetime. For example, if the critical void volume causing the line failure is $0.03*V_{sat}$, the failure time under -100 MPa compressive stress would be about 6 times larger than the failure time under 100 MPa tensile stress. The conventional lifetime extrapolation based on Black's equation considers only the effects due to temperature and current density. The result shown in Figure 3.13 implies that this extrapolation method probably overestimates the lifetime. Thermal stress effect should be considered in a more conservative extrapolation.

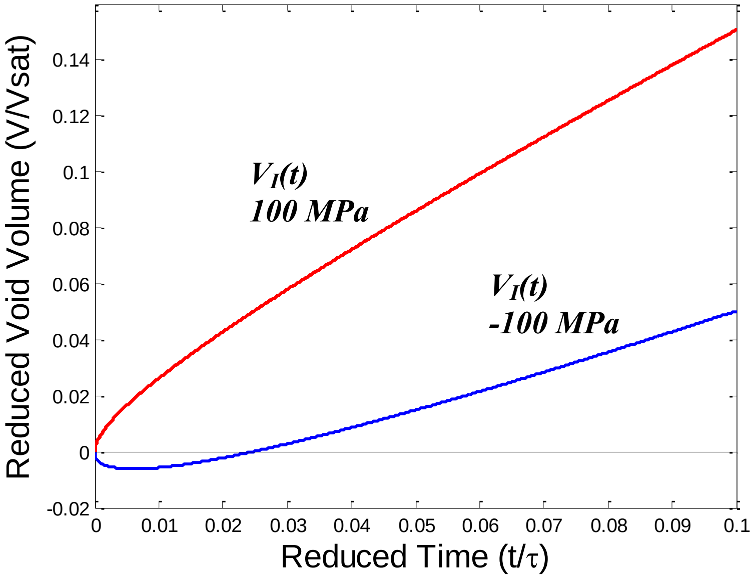


Figure 3.13 Comparison of initial void growth under tensile (upper curve) and compressive stress (lower curve).

3.4 MONTE CARLO SIMULATION OF GRAIN GROWTH

When the line width is below 90nm, bamboo-type grains mixed with small polycrystalline grains are usually observed in Cu interconnects lines [Hu *et al.*, 2007c]. These small grains provide additional EM diffusion paths, raising increasing concerns for EM reliability. TEM provides a direct observation of grain structures in Cu lines. But each observation is limited in one cross-section and it is very time consuming. Furthermore, there are technical difficulties in retrieving quantitative data on fine grain structures, due to the resolution limit of conventional TEM technique and the overlap of the TEM grain images. Computer simulation is employed in this section as a fast and inexpensive supplemental tool to study the grain growth. This approach also enables us to track the evolution of grains during annealing which is very difficult for direct TEM observations. Another motivation of the grain growth simulation is to provide grain structures to support the EM modeling in this chapter.

3.4.1 the Potts Model

The grain growth simulation is performed by a Monte Carlo method based on the modified Potts model. In statistical mechanics, the Potts model [Potts, 1952] describes interacting spins on lattice. It is a generalization of the Ising model [Ising, 1925] which deals with spins having two states (spin up and spin down). In the Potts model, the spins can have an arbitrary number of states. Domains of the same spin state grow over time to minimize the energy of system. The Hamiltonian of the system consisting of N lattice sites can be written as

$$H = \sum_{i}^{N} \sum_{j}^{n} \frac{J_{ij}}{2} (1 - \delta_{S_i S_j}) + \sum_{i}^{N} E_i \, , \tag{3.28}$$

where J_{ij} is the interaction energy between neighboring spins, E_i is the self-energy of a spin, δ is the Kronecker delta, S_i is a specified spin state. In the early 1980s, people recognized that the Potts model can be used to describe the grain structures [Anderson *et al.*, 1984, Srolovitz *et al.*, 1984b, Srolovitz *et al.*, 1984a, Anderson *et al.*, 1989, Grest *et al.*, 1988]. Each grain orientation is represented by a spin state S_i. The interaction energy J_{ij} can be viewed as the grain boundary energy between two neighboring grains. E_i can be used to represent the interface/surface energy for the cells close to interfaces and surfaces. The grain growth is driven by minimizing the system energy in Equation (3.28).

3.4.2 Simulation Details

The Monte Carlo simulation code is written in C/C++ programming language. A desktop computer (Intel dual core) with Cygwin to provide Linux-like environment and an 8-core server with Linux operating system are employed for the simulation. The simulated data is then displayed by a visualization software OpenDX. The code was originally developed by Matthias Kraatz at UT Austin [Kraatz, 2011]. The original code simulates the grain growth in a rectangular line. In this dissertation, it is extended to describe a rectangular line with an overburden, which is usually the structure for a damascene line during annealing. A schematic of the cross-section of the simulated structure is shown in Figure 3.14. Instead of simulating normal grain growth without considering the interface/surface energy as in Ref. [Kraatz, 2011], in this dissertation, energy terms from interfaces and surfaces are taken into account for the abnormal grain growth. With the line width scaling, the interfaces and surfaces should have larger and larger impact on the grain growth due to the increasing surface to volume ratio.

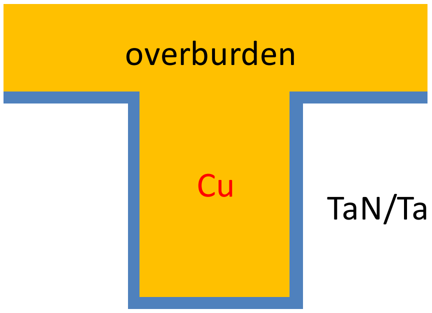


Figure 3.14 Schematic of the cross-section of a simulated Cu line with the overburden and liner.

A cubic lattice structure is employed for the 3D grain growth simulation. The dimensions of the line are represented by the number of cells (lattice sites) in each dimension. A total of 30 orientations are used for Cu grains. Initially each cell is set with a random orientation. Up to the 3rd nearest neighbors are counted for the grain boundary energy calculation. This means $n = 26$ in Equation (3.28) for a cubic lattice. Due to the lack of reported experimental measurements for the grain boundary energy, it is difficult to set different grain boundary energies J_i for different grain boundaries. So an isotropic grain boundary energy $J_i = J$ is used for simplification in this study. An average Cu grain boundary energy 0.559 J/m^2 is reported in [Chattopadhyay, 2001].

It is reported that both PVD Cu seed layer and electro-plated Cu film show strong (111) texture [Rosenberg *et al.*, 2000] due to a relative lower surface energy (1.83 J/m^2) for (111) orientation [Skriver *et al.*, 1992, Yang *et al.*, 2011] as well as a relatively lower interface energy (0.47 J/m^2) between α-Ta and (111) Cu [Abe *et al.*, 1995, Yang *et al.*, 2011]. During simulation, the grain orientations S_i =30, 29, 28 are assumed to have the lower surface energy E_{SL} and interface energy E_{IL} and other orientations have the higher surface energy E_{SH} and interface energy E_{IH}. The ratio between them is set as $E_{SH}/E_{SL} = E_{IH}/E_{IL} = 3$. This ratio was also adopted by Ref. [Jung *et al.*, 2004] previously. Note that all the orientations discussed above are referring to those viewed from the top surface, i.e., along the *z* direction shown in Figure 3.15. A (111) orientation viewed from the top surface cannot be another (111) orientation viewed from the sidewall (*y* direction). Therefore a grain having a low interface energy at the trench bottom cannot also have a low interface energy with trench sidewalls. Grains with orientations S_i =1, 2, 3 are set to have low interface energy with the Ta barrier at the sidewalls, while the other orientations have high interface energy with the sidewalls.

During simulation, the orientation of a cell is changed into one of its randomly selected unlike neighbors. The energy of the system is then recalculated and compared with the one before reorientation. If the energy is reduced, the new orientation is kept. Otherwise, the new orientation is allowed only with the Boltzmann probability

$$p = \exp(-Q / k_B T), \tag{3.29}$$

where Q is the activation energy for grain boundary migration, k_B the Boltzmann constant T the annealing or simulation temperature. Since Q cannot be determined explicitly, it is difficult to convert the energy unit into that of thermal energy k_BT. Therefore the Boltzmann probability is simplified to [Jung *et al.*, 2005]

$$p = \exp(-2\Delta H), \tag{3.30}$$

where ΔH is the energy difference between before and after the reorientation. Since the energy in the Hamiltonian is in an arbitrary scale, it is set that $J = 1$ during simulation and all other energy terms are scaled accordingly.

After the reorientation trial on one lattice site, a new lattice site is randomly selected from the rest of the lattice sites for a reorientation trial. This permutation continues until all the lattice sites go through at least one reorientation trial, which completes one Monte Carlo step (MCS). Then a new permutation starts and finally the simulation stops when a desired number of MCSs is reached.

3.4.3 Simulation Results and Discussion

Figure 3.15 shows a simulated Cu line with overburden and the inter-metal dielectric (IMD) in red. The dimensions for the structure are XxYxZxY_linexZ_line which are illustrated in the Figure as well. The Cu line length, width and thickness are X, Y_line and Z_line respectively. For the structure shown in Figure 3.15, it is 1000x400x300x100x200 with 20 MCS.

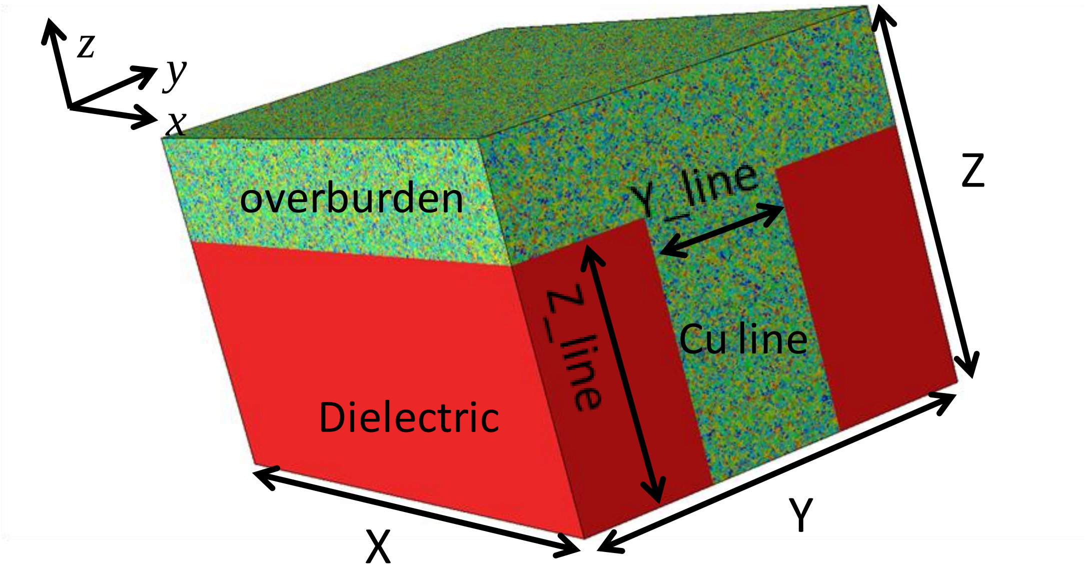


Figure 3.15 A simulated Cu line structure with overburden and dielectric.

Figure 3.16 shows a 500x300x200x100x180 structure after 200 MCS of grain growth simulation. The orange and dark yellow colors correspond to orientations S_i =1, 2, 3. The blue colors correspond to orientations S_i =30, 29, 28. It clearly shows that the grains close to the sidewalls have blue colors, while grains close to Cu line bottom and top surface of overburden have orange and dark yellow colors. This is caused by the abnormal grain growth to reduce the interface and surface energies. Except the grain growth starting from interfaces and surface, normal grain growth starting from the bulk of Cu line to minimize the grain boundary energy is also observed in Figure 3.16.

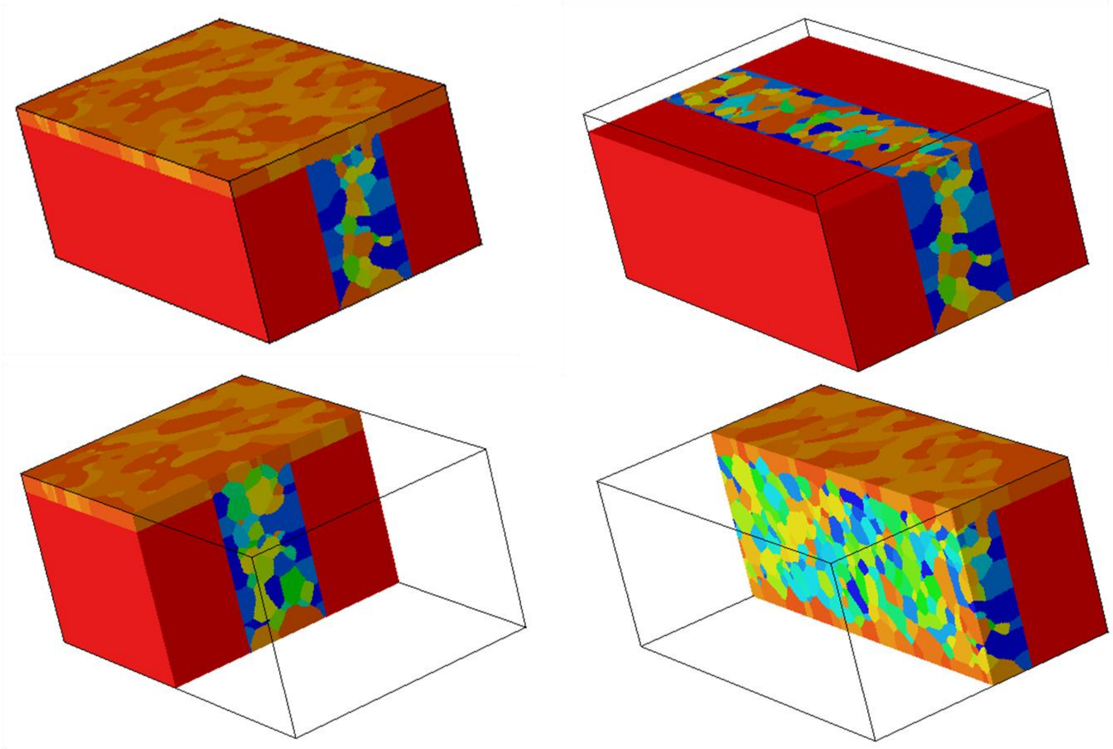


Figure 3.16 Different cross-sections of a simulated Cu line. 500x300x200x100x180; 200 MCS.

The normal grain growth in the bulk of Cu mixing with abnormal grain growth from interfaces and surface can be more clearly observed at the initial stage of the simulation. For example, in Figure 3.17, a Cu structure experiences 50 MCS of simulation. A clear color difference between bulk and interfaces can now be observed.

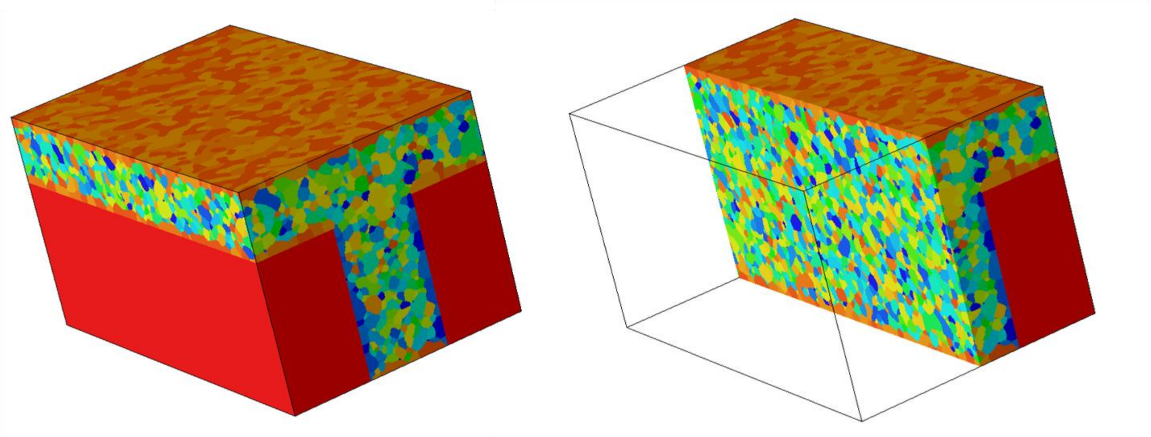


Figure 3.17 Time evolution of grain growth in a Cu line. 500x300x260x100x180; 50 MCS.

Figure 3.18 (a), (b) and (c) demonstrate the time evolution of grain growth. The simulation time is counted in unit of Monte Carlo step (MCS). When the simulation runs from 200MCS to 600MCS, the small grains grow larger. The growth of some grains is accompanied by the shrinking of other grains, which is also observed in Figure 3.18. But overall, the grain size is increasing with disappearing of small grains.

Another phenomenon can be observed is that, as the simulation time elapses, the abnormal grain growth from interfaces and surface becomes more and more dominant. This is particularly true for Cu lines with smaller dimensions due to the increased surface to volume ratio. The simulated Cu structure shown in Figure 3.18(d) has dimensions that are 70% of that shown in (c), standing for one generation of scaling. After experiencing the same 600 units of MCS, the smaller Cu line in (d) shows much more grains in blue, in comparison with (c).

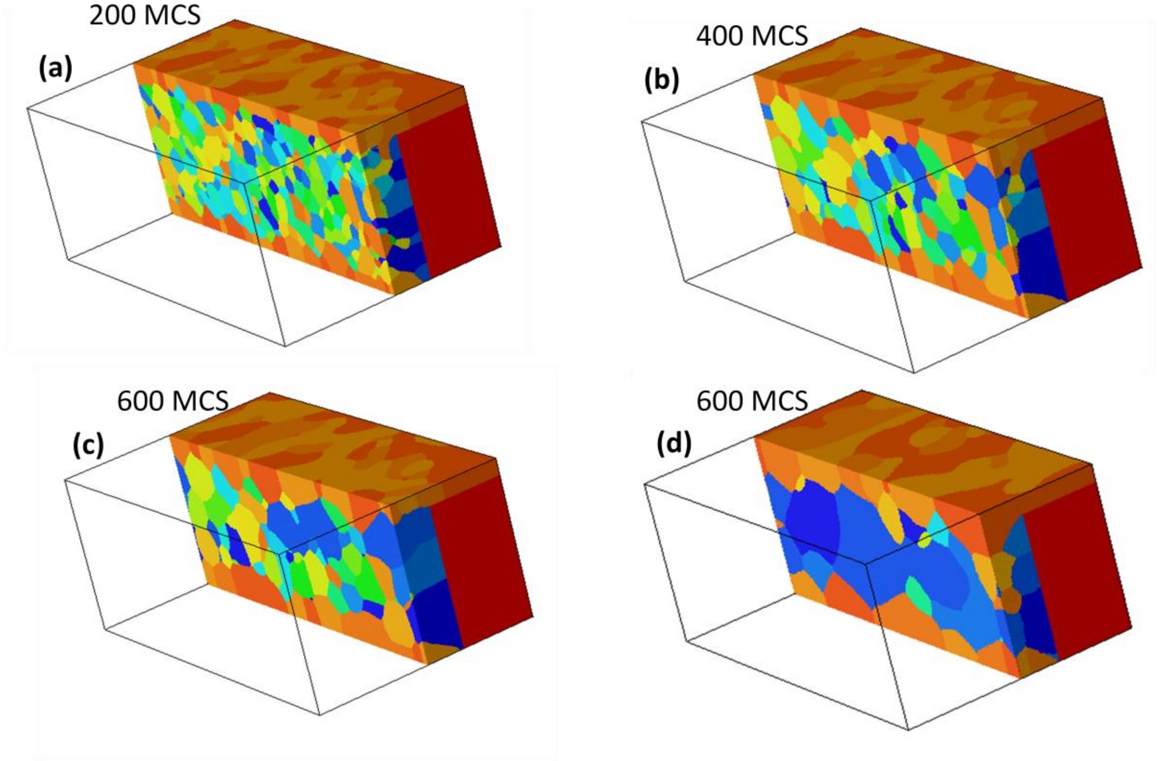


Figure 3.18 (a), (b) and (c) Time evolution of grain growth in a Cu line with dimension 500x300x200x100x180. (d) A Cu line with dimension 350x210x140x70x126, which is 0.7X scaled from those in (a), (b) and (c).

If the orientations S_i =30, 29, 28 in orange and dark yellow stands for (111) orientations, S_i =1, 2, 3 in blues then should be (110) orientations so that they could be perpendicular to each other. The comparison of (c) and (d) in Figure 3.18 indicates that, due to grain growth initiated from sidewalls, Cu lines with smaller line width will show a stronger (110) texture. Such trend has been observed experimentally by high resolution TEM orientation mapping with precession diffraction technique. As shown in Figure 3.19, if looking at the line width direction, the (111) texture can be observed in Cu lines [Kameswaran, 2011]. Such texture is stronger in a 70nm wide line compared to a 120nm wide line. The (111) texture along line width corresponds to a (110) texture along normal (line thickness) direction.

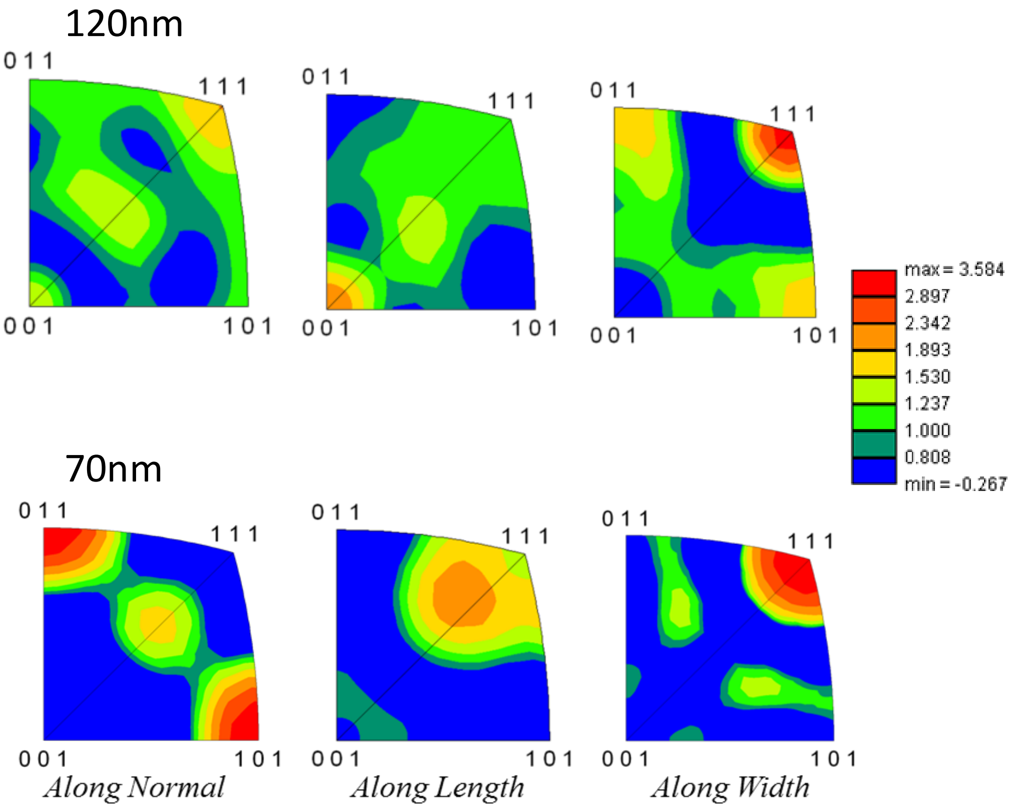


Figure 3.19 Inverse pole figures for a 120nm wide and a 70nm wide Cu interconnect line measured by precession microscopy with TEM. [Kameswaran, 2011]

Also reported in [Kameswaran, 2011] there are many small grains close to the trench bottom, which is also observed in Figure 3.18. To reduce interface energy between Cu and Ta at the trench bottom, (111) grains grow from the trench bottom. This is accompanied by (110) grain growth from sidewalls to reduce the interface energy between Cu and Ta at sidewalls. Due to the relatively high aspect ratio of the trench (a common value of 1.8 is adopted in the simulations), the grain growth at the sidewalls dominates over the growth at the bottom. Once that occurs, the small grains at the trench bottom are frozen kinetically at the bottom. The size of these (111) grains depends on the simulation or the annealing time. As shown in Figure 3.20, from 200 MCS to 400 MCS, these grains grown in size at the expense of disappearing bulk grains. From 400 MCS to 800 MCS and 1200 MCS, these (111) grains decrease in size due to the growth of (110) grains from sidewalls. Eventually these small grains will be consumed by the sidewall grain growth if the simulation time elapsed long enough. However, in a realistic annealing process, due to limited thermal budget there will always be some small grains at the trench bottom. Note that, in an actual Cu interconnect line, small particles trapped in the trench bottom may cause grain pinning to prevent grain growth at bottom [Harper *et al.*, 1999]. This aspect is not included in this study.

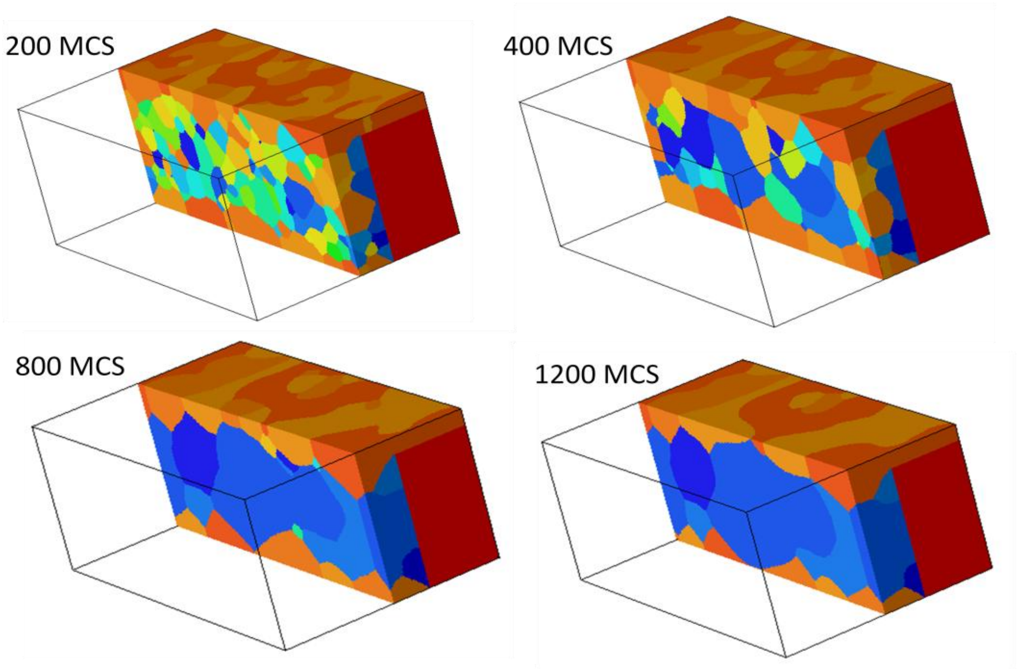


Figure 3.20 Grain size evolutions for grains at trench bottom. Dimensions 350x210x140x70x126.

According to the simulations performed above, the line width and aspect ratio (AR) have great effect on the grain growth inside a line. However, in each technology node, the line width and AR are generally set for lines at one specific metal level. The only tunable dimensional parameter is the overburden thickness. Therefore, it is of interest to investigate the effect of overburden thickness on grain growth [Jung *et al.*, 2004, Dubreuil *et al.*, 2008]. Simulations for two identical Cu lines with different overburden thicknesses were performed to study the potential grain growth promoted by surface energy minimization from overburden. The results are presented in Figure 3.21. With a thin overburden (20-cell thick in (c) and (d)), some (111) grains growing from the overburden surface penetrate into the Cu line but are limited to a region close to the line surface. These (111) grains at the line top surface may cause EM reliability issue, since the diffusivity along (111) Cu and SiCN cap interface is relative larger. With a relative thick overburden (80-cell thick in (a) and (b)), no grain growth penetration from overburden surface is found for 500 MCS. The sidewall growth dominates the Cu grains at regions inside the line as well as at the line surface. This suggests that the role of overburden to grain growth is not critical when it is relatively thick, especially for narrow lines where the interfaces at sidewalls dominate grain growth.

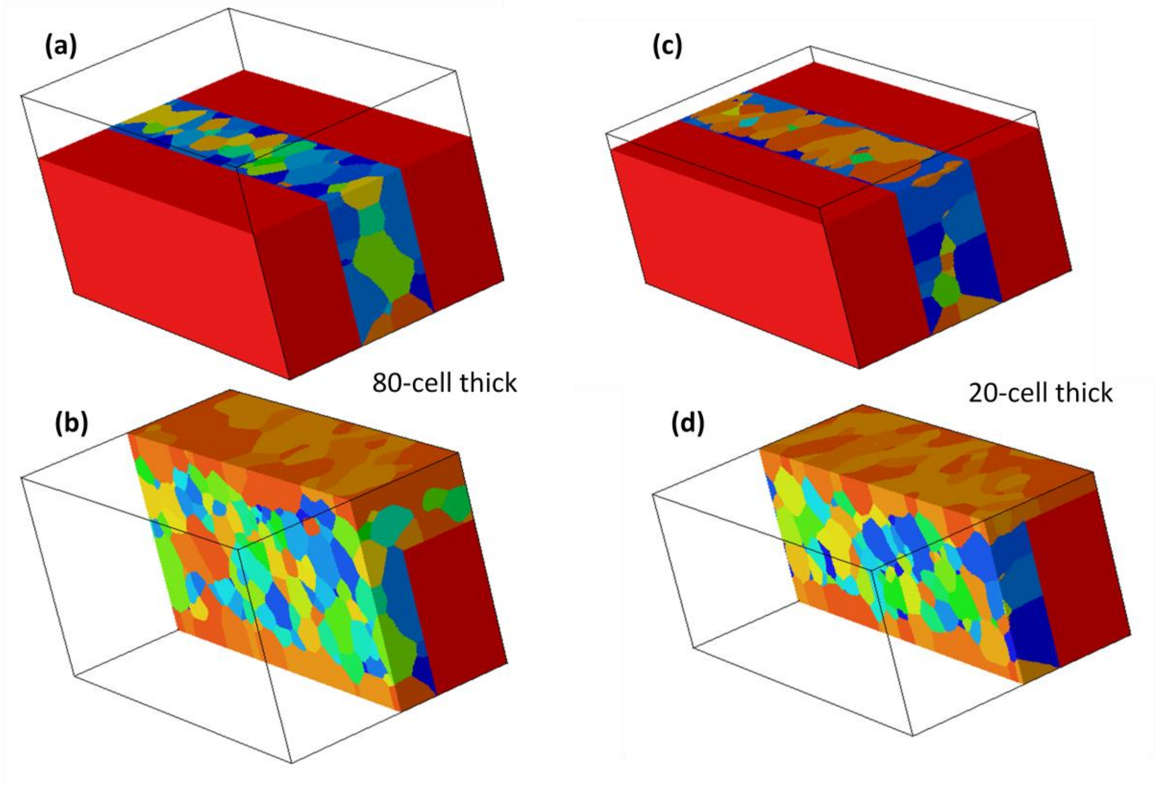


Figure 3.21 Effect of overburden thickness to grain growth. The dimensions for (a) and (b) are 500x300x260x100x180. The dimensions for (c) and (d) are 500x300x200x100x180. The only difference between two structures is the overburden thickness: one 80-cell thick, the other 20-cell thick. 500 MCS for both simulations.

3.5 CONCLUSIONS

In conclusion, the Korhonen model for EM-induced void growth is reviewed and analyzed and it is found that the original Korhonen's solution is only applicable to Stage III (after failure). In this chapter, the Korhonen model was extended to analyze the initial void growth at Stage I leading to line failure. The approach is to divide the Cu line into two regions based on the void segment and calculate the stress evolution in the two regions separately. Approximate analytical solutions were obtained for void growth rates at Stage I and Stage III, which were found to depend on the initial thermal stress in the Cu line. By using a compressive thermal stress which is probable for Cu interconnect line at the EM test temperature, the model generates failure time agreeing well with the experimental data shown in Chapter 2. The model suggests that the conventional failure time extrapolation based on Black's equation probably overestimates the EM lifetime and the effect of thermal stress should be considered in the extrapolation.

Grain growth simulations based on Potts model were also performed considering interconnect structures with overburdens. Both normal grain growth from bulk and abnormal grain growth from surface and interfaces were found in the simulations. Due to the relatively high aspect ratio of a Cu interconnect line, the grain growth from sidewalls was found to play a dominant role. This led to small grains in the trench bottom and small possibility for penetration of grains growing from a relatively thick overburden surface. Such trends become even clearer with further scaling of line dimensions due to increasing surface to volume ratio. The simulated grain structure was used as material input for stress modeling.

Chapter 4: Size Effect on the Electron Wind Force for Electromigration in Nanoscale Interconnects

The minimum width of Cu interconnect line of current technology node is now close to its electron mean free path (39nm at room temperature). This chapter studies the size effect on the electron wind force for a thin film and a rectangular line with dimensions in this size range. The problem is modeled by considering the momentum transfer between electrons and a defect atom on the Cu/cap interface, the dominant EM diffusion path in a Cu damascene line. The analytical result shows that the scaling effect on the effective charge number Z^* can be represented by a size factor S depending on the film/line dimensions. The electron wind force is enhanced due to the dimensional confinement of the interconnect. Interface scattering and grain boundary scattering are found to have opposite effect on electron wind force. The temperature dependence of the electron wind force is analyzed.

4.1 INTRODUCTION

The development of EM theory started more than a half century ago. Ficks developed a model based on ballistic theory [Fiks, 1959] and then a semi-classical formulation was developed by Huntington and Grone [Huntington *et al.*, 1961]. Bosvieux and Friedel [Bosvieux *et al.*, 1962] formulated a quantum mechanical model, which was followed by subsequent models and formulations [Das *et al.*, 1975, Landauer *et al.*, 1974, Sham, 1975, Sorbello *et al.*, 1977]. More detailed review can be found in Ref. [Ho *et al.*, 1989]. For conductors such as Cu, it is generally accepted that the EM driving force is dominated by the electron wind force, which can be expressed as $F = -Z^{*}e\rho j$, where $Z^{*}e$ is the effective charge, ρ is resistivity and j is electric current density. The effective charge $Z^{*}e$ is calculated based on the momentum transfer due to electron scattering on the jumping atom at the "saddle-point", which is half-way along the jumping path to the vacancy.

Cu interconnect was introduced to replace Al by IBM in 1997 due to its lower electrical resistivity and better EM reliability. As scaling continues, EM is once again becoming a limiting factor. The challenge is two-fold. First, as predicted by the International Technology Roadmap for Semiconductors (ITRS) [ITRS, 2011], the maximum current required by high performance devices J_{max} keeps increasing and will soon be beyond the maximum current for targeted EM life time J_{EM}. Second, even if a constant current is assumed, the EM life time still drops half for each generation following a simple geometry scaling relation [Hu *et al.*, 2004b]

$$t = \Delta L_{crt}\, k_B\, T/(D_{eff} F). \tag{4.1}$$

In the above expression, ΔL_{crt} is the critical void length, k_B the Boltzmann constant, T the temperature, D_{eff} the effective diffusivity and F the electromigration driving force. For each generation, ΔL_{crt} decreases and D_{eff} increases by 0.7. This results in a 2x drop of life time if the EM driving force F is taken as a constant when the drive current density j is a constant.

The industry is now entering 22nm node with M1 line width only 32nm which is even smaller than the electron mean free path (MFP) in Cu (39nm at room temperature). In this size region, the transport behavior of electrons is different from that in bulk. For resistance (r), although it still follows a simple geometry relation

$$r = \rho \, l/A, \tag{4.2}$$

where l and A are the length and cross-sectional area of the metal respectively, resistivity ρ is no longer a constant as the line dimension scales. It is well known that the increased interface and grain boundary scattering will significantly enhance the resistivity in this size range, as shown in Figure 4.1.

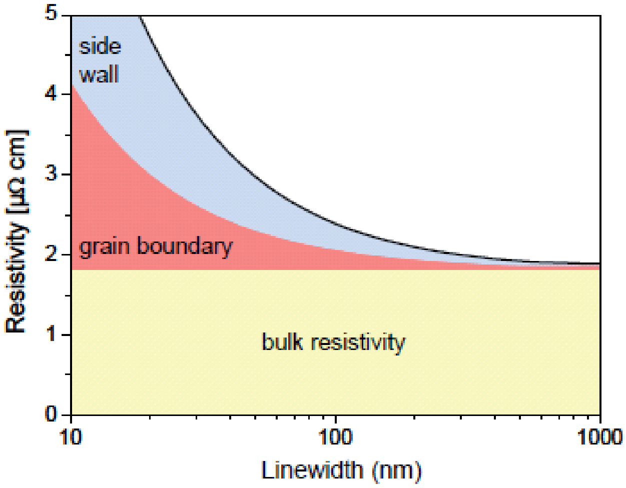


Figure 4.1 Increase of Cu resistivity as the scaling of line dimension due to grain boundary and side wall scattering. [ITRS, 2009]

EM is actually closely related to the electrical resistivity. As schematically demonstrated in Figure 4.2, when electrons flow in a metal under an electric field, they scatter upon colliding with atoms. This scattering process slows down the electrons resulting in electrical resistance. The same scattering process also transfers momentum to the atoms which may cause the atoms to migrate along the diffusion path. The latter phenomenon is called EM. Since the resistivity ρ starts to experience significant size effects in nanoscale interconnects, this raises an important question concerning the electron wind force - Will there exist a similar significant size effect on the momentum transfer as a result of such scattering events? In this sense, Equations (4.1) and (4.2), as well as the parameters in the equations F and ρ are quite similar in their correlation to the electron scattering process. While the increase of resistivity ρ due to increasing interface [Fuchs, 1938, Sondheimer, 1952] and grain boundary scattering [Mayadas et al., 1970] is well established, the size effect on electron wind force F has not been reported in this technology relevant size regime. This chapter studies this size effect for a thin film and a rectangular line.

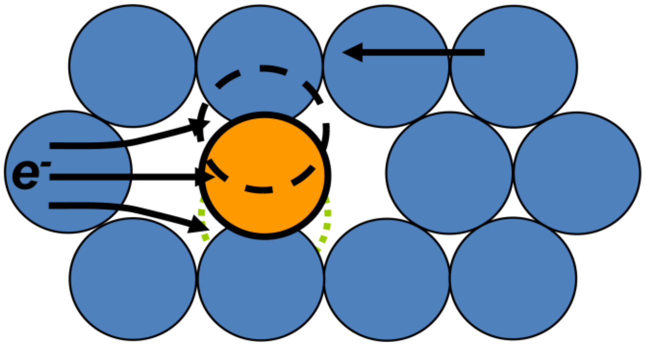


Figure 4.2 Schematic showing the scattering between electrons and atoms causes both electrical resistivity and EM.

4.2 THIN FILM

The top interface is usually the dominant diffusion path for Cu damascene lines after the CMP and capped with a dielectric layer. This diffusion path can be suppressed by metal capping, making the GB diffusion more important for EM. This study is focused on electron wind force on a jumping atom along the interface with a dielectric cap. The objective of this study is not to develop a comprehensive theory for the electron wind force in metal nanolines. Instead, it aims at developing a simple model to estimate the "size effect" on the electron wind force relative to Cu interconnects for current and future technology nodes. Since the film and line dimensions under consideration are much larger than the atomic size, it is assumed that electron screening of the saddle-point atom is not affected by scaling and a classical free electron model can be used for Cu. For dimensions at the atomic scale, one can refer to Ref. [Bevan *et al.*, 2010] for wind force calculation.

For a thin film with thickness *a* as shown in Figure 4.3, electrons in the film gain a net momentum in the positive x direction from the external electric field ε. Part of the momentum of these electrons will be transferred to the jumping atom at the top interface due to scattering. The wind force received by the jumping atom is the momentum transfer rate and can be expressed as

$$F = d(P_{x\_in} - P_{x\_out}) / dt, \tag{4.3}$$

where P_{x_in} and P_{x_out} are the momenta in the x direction of the electrons approaching and leaving the jumping atom during scattering, respectively.

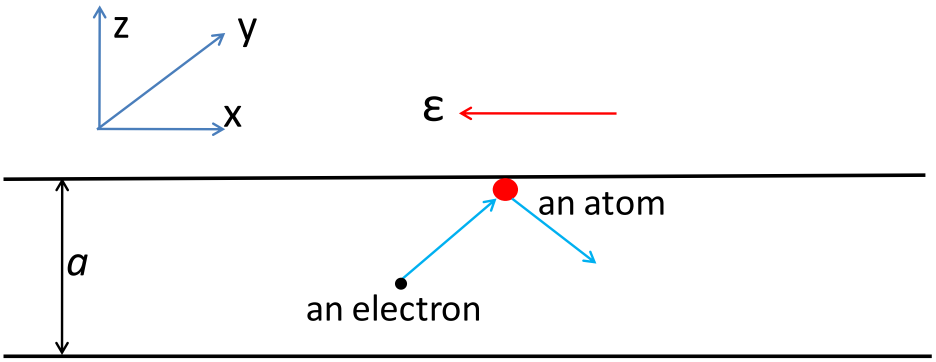


Figure 4.3 Schematic of the model for a thin film with Cartesian coordinates.

To calculate the momentum transfer rate between electrons and the jumping atom, one defines $D(E)$ as the density of state of electrons at the energy level E, σ_i the effective scattering cross-section at the Fermi energy, Ω the solid angle, m the effective mass of an electron, v the velocity of electrons, f the electron distribution function. It can be shown that, in a free electron model, the number density of electrons whose energy lies between E and $E+dE$, and moving in a solid angle $d\Omega$ is

$$f*D(E)dE*d\,\Omega/4\pi. \tag{4.4}$$

Number of such electrons scattered by a defect atom at interface in time interval Δt is

$$\sigma_i*v_z*f*D(E)dE*d\,\Omega/4\pi*\Delta t. \tag{4.5}$$

Each of such electrons carries a momentum in x-direction as mv_x. Momentum carried by such electrons scattered by the defect in time interval Δt is

$$mv_x*\sigma_i*v_z*f*D(E)dE*d\,\Omega/4\pi. \tag{4.6}$$

Then one can integrate the solid angle and explicitly calculate P_{x_in} and P_{x_out} according to the electron moving direction. The electron wind force can be expressed as [Wu *et al.*, 2012]

$$F = \frac{\sigma_i}{4\pi}\int_{4\pi} d\Omega \int_0^\infty mv_x v_z fD(E)dE\,. \tag{4.7}$$

The scattering events at the interface are more complicated than the simplified picture described by Equation (4.7). The scattering cross-section is affected by the bonding environment of the scattering atom. When the jumping atom diffuses halfway to the vacancy, i.e., at the saddle point, it experiences more scattering and hence a bigger wind force than at an equilibrium position. To avoid such a complexity, instead of calculating the value of *F*, this study only focuses on how *F* changes with scaling of the film and/or the line dimensions, with the bonding environment and relative position of the metal atoms at the interface remaining unchanged.

This is done by evaluating the ratio of F / F_0, where F_0 is the electron wind force for the jumping atom at the same interface but with an infinite film thickness $a \to \infty$. The size regime discussed here is comparable to the electron MFP which is much larger than the atomic scale. Thus it is reasonable to assume that the effective scattering cross-section is not affected by the size confinement and canceled out in the ratio of *F* versus F_0.

The electron distribution function *f* can be evaluated based on the Boltzmann transport equation (BTE)

$$\mathbf{v} \bullet \nabla_{\mathbf{r}} f + \frac{-e\boldsymbol{\varepsilon}}{m} \bullet \nabla_{\mathbf{v}} f = -\frac{f - f_0}{\tau}, \tag{4.8}$$

where f_0 is Fermi-Dirac distribution function and τ is the relaxation time. One can follow Fuchs-Sondheimer (F-S) method [Fuchs, 1938, Sondheimer, 1952] to obtain a solution of the BTE by introducing two interface scattering processes: specular scattering where the electron only reverses its momentum in the *z* direction, and diffuse scattering where the electron comes back to the equilibrium state after scattering. The actual scattering process is somewhere between these two ideal cases. An empirical parameter, specularity parameter *p*, describing the probability of an electron to be specularly scattered is usually introduced to obtain a tractable solution. For the case of pure diffuse scattering (*p=0*), the solution of the BTE without considering short length effect is [Sondheimer, 1952]

$$f_1^{+}(v,z)=\frac{e\tau\varepsilon}{m}\frac{\partial f_0}{\partial v_x}[1-\exp(-\frac{z}{\tau v_z})], \tag{4.9a}$$

$$f_1^{-}(v,z)=\frac{e\tau\varepsilon}{m}\frac{\partial f_0}{\partial v_x}[1-\exp(-\frac{z-a}{\tau v_z})], \tag{4.9b}$$

where $f_1 = f - f_0$ and the superscript "+" and "-" is for $v_z > 0$ and $v_z < 0$, respectively.

One can now proceed to calculate the electron wind force and the result is

$$F=-Z_0^{*}Se\rho j. \tag{4.10}$$

In the above expression, Z_0^* is a material constant and can be represented as:

$$Z_0^{*}=\frac{1}{8}D(E_F)E_F\lambda\sigma_i, \tag{4.11}$$

where E_F is the Fermi energy and λ is the electron MFP. The factor *S,* which is called the size factor, can be expressed as

$$S=\int_0^{\pi/2}4\sin^3\theta\cos\theta[1-\exp(-\frac{a}{\lambda\cos\theta})]d\theta. \tag{4.12}$$

When $a\to\infty$, $S=1$ and $F=F_0=-Z_0^{*}e\rho_0 j,$ where ρ_0 is the resistivity for the bulk material. Since $\rho_0\lambda$ is a constant for free electrons, one has $Z_0^*\propto 1/\rho_0$ which agrees with Huntington's result [Huntington *et al.*, 1961]. One can define $Z^*=Z_0^{*}S$ and the electron wind force is expressed in its conventional form $F=-Z^{*}e\rho j$. In this way, *S* represents the scaling effect on the effective charge and the effective charge number Z^* now scales with the film thickness *a*. As shown in Figure 4.4, In this case, Z^* is generally smaller than Z_0^* and decreases with scaling down of the film thickness due to reduced electron drift momentum resulting from increasing interface scattering. Z^* decreases rapidly when the film thickness is smaller than *λ,* the MFP. According to the

F-S model, thin film resistivity is generally increased due to interface scattering with down scaling of the film thickness. Combining these parameters, one has the size effect on the wind force curve as shown in Figure 4.4(b), where a constant current *j* is assumed. The result indicates that the electron wind force in the interface of a nano-scale thin film is generally bigger than that for a film with infinite thickness due to increasing electron scattering at the interface. The increase in the scattering maximizes at 24% when the film thickness is about 0.8λ, then it starts to drop.

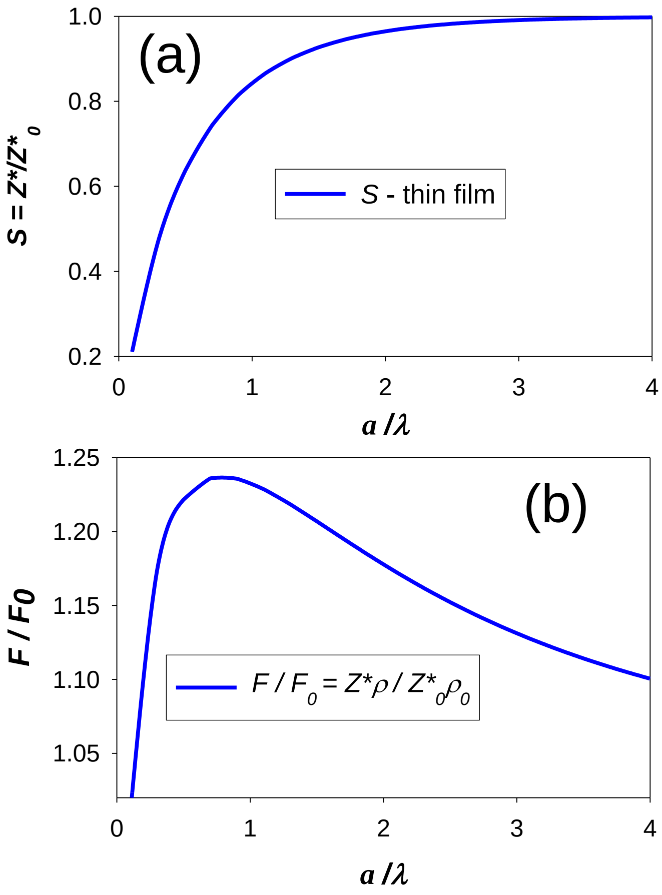


Figure 4.4 (a) Size factor *S* and (b) electron wind force for a thin film as a function of film thickness *a* normalized by electron mean free path λ.

4.3 RECTANGULAR LINE

For a line with a rectangular cross-section as shown in Figure 4.5, a simple kinetic approach is adopted to calculate *f*. Following Chambers [Chambers, 1950], when an electron at point *O* inside the wire travels to point *P* at the surface, the effective mean free path λ_1 can be expressed as: [Chambers, 1950]

$$\lambda_1 = \lambda[1 - \exp(-OP/\lambda)] \,. \qquad (4.13)$$

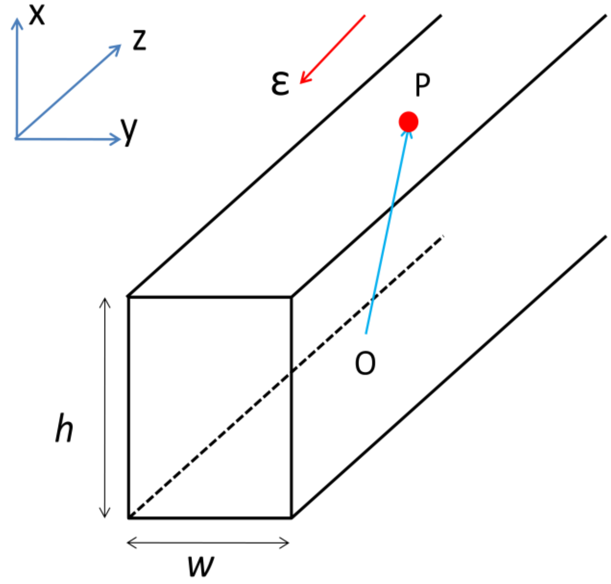


Figure 4.5 Schematic of the model for a rectangular line with Cartesian coordinates.

The electron distribution deviated from equilibrium can be calculated as [Chambers, 1950]

$$f_1(OP) = \frac{\partial f_0}{\partial v_z} \Delta v_z = \frac{e\varepsilon\tau}{m} \frac{\partial f_0}{\partial v_z} (1 - e^{-OP/\lambda}) \,. \qquad (4.14)$$

The electron wind force can be similarly formulated as in the thin film case as in Equation (4.10) with the following size factor:

$$S = \frac{4}{\pi w}\int_0^w dy \int_{-\pi/2}^{\pi/2} \cos\phi d\phi \int_0^\pi \sin^2\theta \cos^2\theta (1 - e^{-OP/\lambda}) d\theta, \tag{4.15}$$

where w and h is the width and thickness of the line, respectively. As shown in Figure 4.6, by projecting OP to a cross-section of the line and dividing the section into 4 sub-sections, the integration in Equation (4.15) can be further deduced [Chambers, 1950]. The integration can then be expressed as

$$S = S_{ED} + S_{DC} + S_{CB} + S_{BA}. \tag{4.16}$$

From symmetry, one has $S_{ED} = S_{BA}$ and $S_{DC} = S_{CB}$, since Equation (4.10) is averaging the electron wind force for an atom at various positions at the interface from point A to E in Figure 4.6.

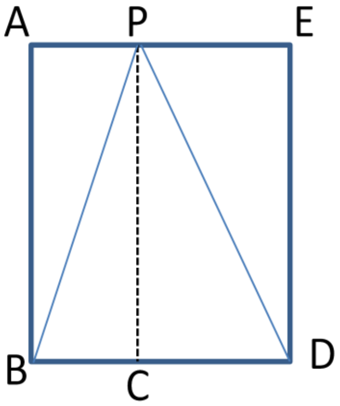


Figure 4.6 Schematics showing the line cross-section divided into 4 subsections for calculation of the size factor for electron wind force.

It is can be shown that

$$S_{CB} = \frac{4}{\pi w}\int_0^w dy \int_0^{\tan^{-1}(y/h)} \cos\phi d\phi \int_0^\pi \sin^2\theta \cos^2\theta [1 - \exp(-\frac{h}{\sin\theta\cos\phi\lambda})] d\theta, \tag{4.17}$$

$$S_{BA} = \frac{4}{\pi w}\int_0^w dy \int_{\tan^{-1}(y/h)}^{\pi/2} \cos\phi d\phi \int_0^\pi \sin^2\theta \cos^2\theta [1 - \exp(-\frac{y}{\sin\theta\sin\phi\lambda})] d\theta. \tag{4.18}$$

Then the scaling of *S* as a function of the line width can be plotted as shown in Figure 4.7, where a MFP of 39nm is used. The trend is similar to the thin film case. When the line width scales down, Z^* decreases. Again the wind force *F* increases to reach a maximum value then starts to drop. For a line with an aspect ratio *AR =5*, the maximum force is smaller than that in a line of 5nm wide, which is not shown in the figure. Quantum effect would become important when the line dimension is close to the electron wavelength (4.6Å for Cu). Therefore Figure 4.7 is only plotted for the line width above 5nm. The maximum value of Z* for a line with *AR=1* is about 28% more than the value for a infinitely wide line, which is slightly larger than the thin film case, due to additional sidewall confinement. In general, at the same line width, a higher aspect ratio implies a thicker line, leading to reduced confinement in the thickness direction and thus a reduction of the electron wind force.

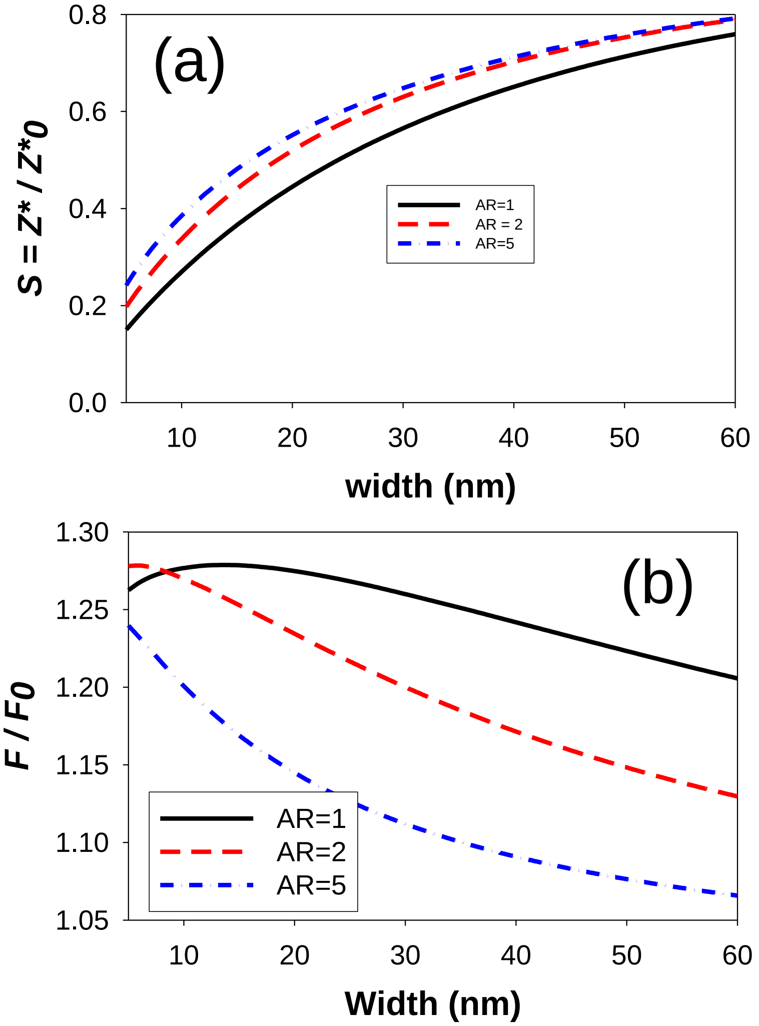


Figure 4.7 (a) size factor *S* and (b) electron wind force for a line with rectangular cross-section as a function of line width for lines with different aspect ratios (*AR*s).

One should note that the electron wind force as shown in Figure 4.7 is averaged along the line width, i.e., the *y* direction. The formalism can also be used to calculate the force variation along the *y* direction. As shown in Figure 4.8, the force along the line width is not uniform due to the non-uniform electron distribution. The atom at the center of the interface receives a larger force than the atoms at the edge of the interface, especially for lower aspect ratio lines. For example, when *AR=0.5*, the force at the center is almost 2 times as large as the force at the edge.

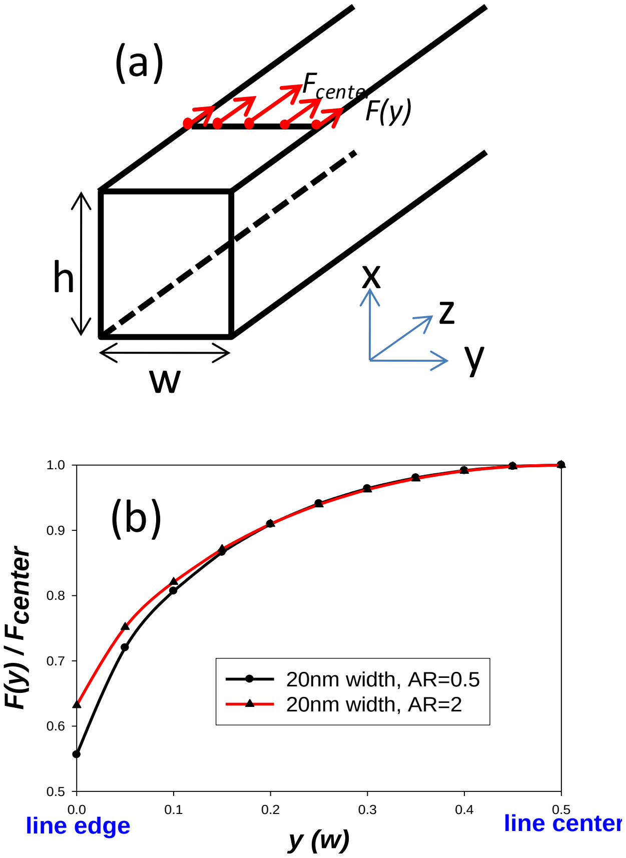


Figure 4.8 (a) Schematic showing the non-uniform distribution of electron wind force along line width direction. (b) Plot of electron wind force at different locations along line width for AR 0.5 and 2. *p=0.*

When $p \neq 0$, electrons are partially mirror-reflected by scattering at the interface. The effective mean free path can be derived as [Chambers, 1950]

$$\lambda_1 = \lambda[1 - \frac{(1-p)\exp(-OP/\lambda)}{1-p\exp(-PP'/\lambda)}], \tag{4.19}$$

where *PP'* is the distance traveled by an electron between two successive reflections. Then following the same procedure as in the $p=0$ case, the electron wind force has a similar form: $F=-Z_0^*Se\rho j$, with $Z_0^*=\frac{1}{8}D_F E_F\lambda\sigma_i(1-p)$. By expanding the denominator in Equation (4.19) and comparing with Equation (4.15), the size factor *S* for $p\neq 0$ can be expressed in term of the *S* for $p=0$

$$S_{p\neq 0}=(1-p)\sum_{n=1}^{\infty}p^{n-1}S_{p=0,\lambda/n}, \tag{4.20}$$

where $S_{p=0,\lambda/n}$ is the size factor when $p=0$ and MFP $=\lambda/n$. In Figure 4.9 (b), the size factor *S* and wind force ratio F/F_0 is plotted with respect to *p* for a 20nm wide line and *AR=2*. It clearly demonstrates a decrease in the size factor but an increase in the wind force when there is more diffuse scattering than specular scattering, corresponding to a smaller *p*. According to the Soffer model [Soffer, 1967], a rough surface can reduce the specularity parameter *p*. This indicates that lines with smooth surfaces have better EM reliability because of a smaller electron wind force.

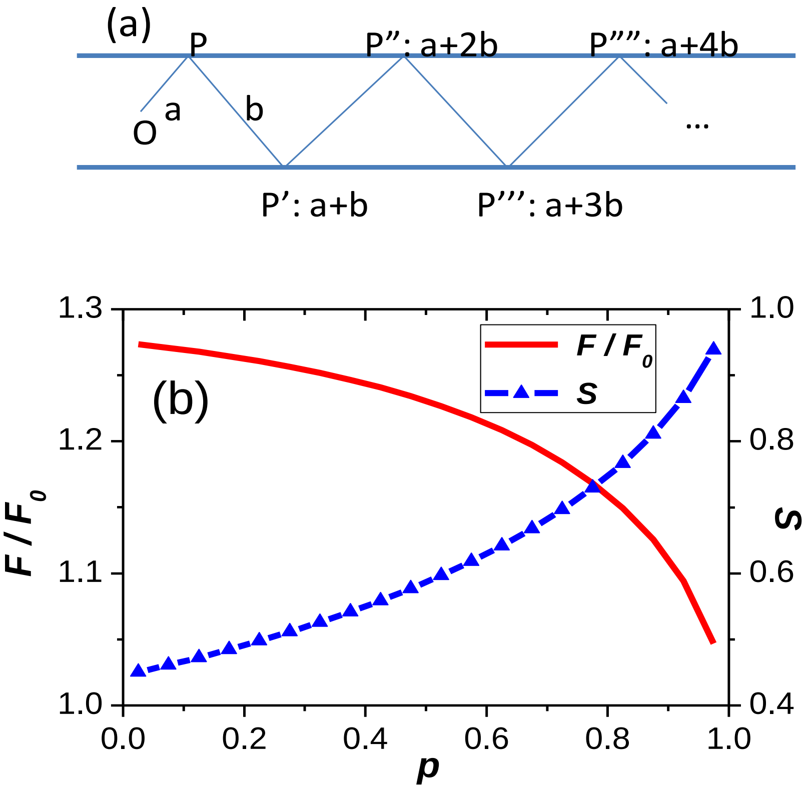


Figure 4.9 (a) Schematic showing successive reflections of electrons at interfaces. (b) F/F_0 and S as a function of specularity parameter p for a line width 20nm and aspect ratio 2.

4.4 GRAIN BOUNDARY SCATTERING

Cu lines in interconnects are composed of multiple grains. As shown in Figure 4.10, other than interface scattering, electrons also experience grain boundary (GB) scattering which can affect the EM driving force for atoms at the top interface. Those GBs parallel to the electron flow provide additional diffusion path for atoms and contribute to EM at the GB, a problem which is beyond the scope of the current study.

Instead, the study here only evaluates how GB scattering would modify the electron wind force for an atom at the interface.

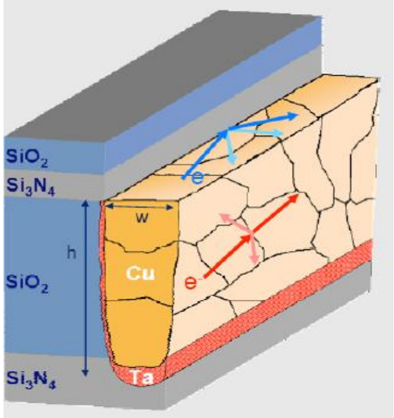


Figure 4.10 A Cu line composed of multiple grains, which provide scattering at grain boundaries in addition to interfaces.

In this study, a bamboo-type grain structure is assumed in order to simplify the analysis. One follows the theory developed by Mayadas and Shatzkes (M-S) [Mayadas *et al.*, 1970] which was formulated to calculate the electrical resistivity of polycrystalline films. When an electron impinges on a grain boundary, it encounters a potential barrier. By assuming this potential be a δ-function, an effective relaxation time τ^* can be deduced as [Mayadas *et al.*, 1970]

$$\tau^* = \tau / \left(1 + \frac{\alpha}{|\cos\theta|}\right), \tag{4.21}$$

where $\alpha = \frac{\lambda}{D}\frac{R}{1-R}$ with *D* as the effective grain size and *R* as the reflection coefficient of the GB. Although this simple expression for the effective relaxation time was initially deduced based on a Gaussian distribution of the grain size, a later study [Marom *et al.*, 2006] shows that it can also be applied to a lognormal or other distributions of the grain size in a few nanometers range or larger. Replacing the relaxation time τ by an effective relaxation time τ^*, the formulation in terms of interface scattering can now be used to estimate the contribution from GB scattering. The size factor and wind force curves obtained are plotted in Figure 4.11 for a line with $AR=1$. A set of parameters $p=0.5$ and $R=0.4$ are used, which fit the resistivity experimental data well [Steinhogl *et al.*, 2002, Sun *et al.*, 2010]. The effective grain size D is chosen as three times of the line width and the resistivity is calculated based on the Matthiessen's rule. As expected, by taking into account the GB contribution, the effective charge Z^*e is further reduced. For a 20nm wide line, Z^*e is reduced to only about 40% of an infinitely wide line. With additional contribution from GB scattering, the maximum electron wind force is found to reduce from 27% to 18% more than that for an infinitely wide line. This results in a partial cancellation of the overall effect and thus benefits EM reliability.

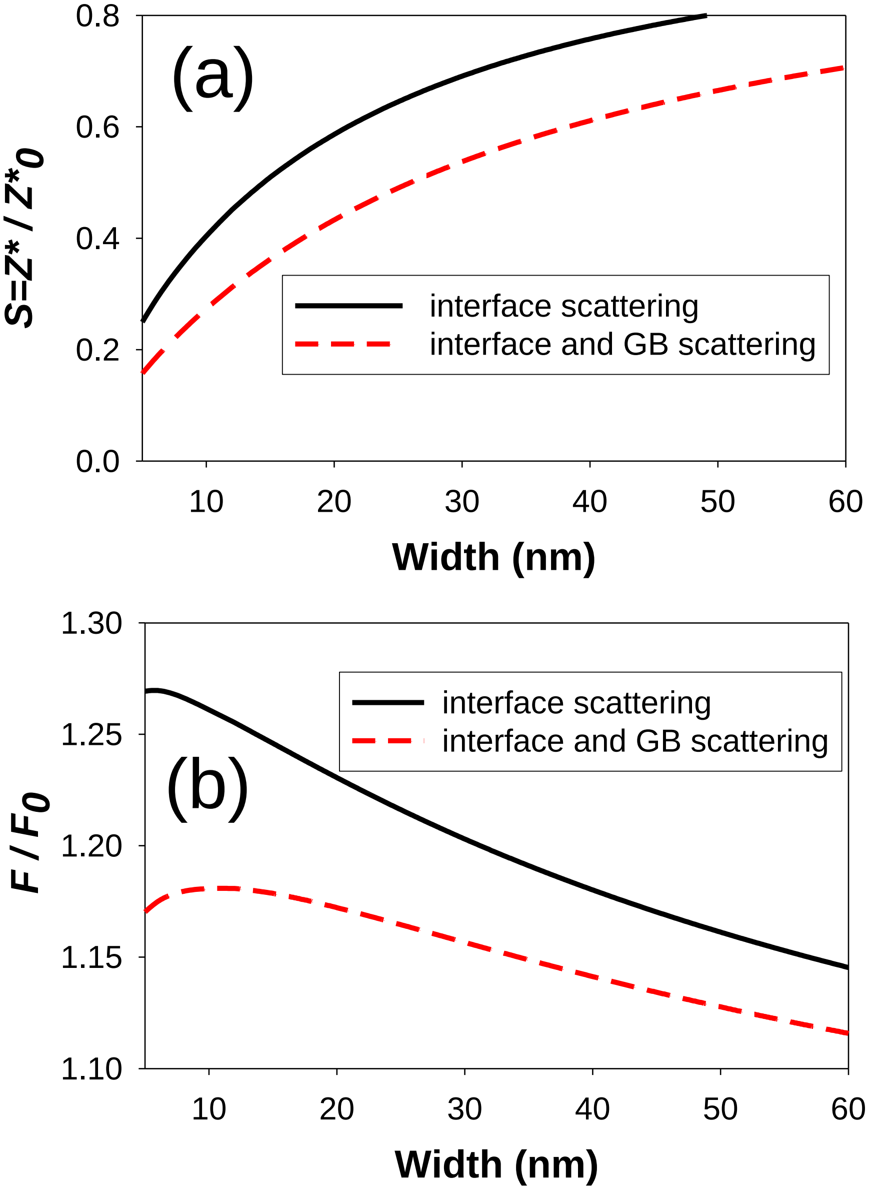


Figure 4.11 (a) Size factor *S* and (b) electron wind force for a rectangular line as a function of line width taking into account interface scattering and grain boundary scattering. *p=0.5*, *R=0.4* , *AR=1*, *D=3*w*.

4.5 TEMPERATURE EFFECT

In the above analysis, room temperature is assumed for the Cu interconnects. However, when a chip is in service, the operating temperature is higher than room temperature. EM test is done at a higher temperature. So it is necessary to study the temperature effect of the electron wind force. Due to phonon scattering, the electron MFP is smaller at higher temperature. From resistivity data as shown in Figure 4.12, it can be deduced that

$$\frac{\partial \rho_0}{\partial T} = 0.00677 \mu\Omega cm / K \, , \tag{4.22}$$

where ρ_0 is the resistivity induced by phonon scattering. In the free electron model, the product of resistivity and electron MFP is a constant independent of temperature

$$\rho_0 \lambda = const \, . \tag{4.23}$$

Therefore, one can deduce the electron MFP for Cu at different temperatures.

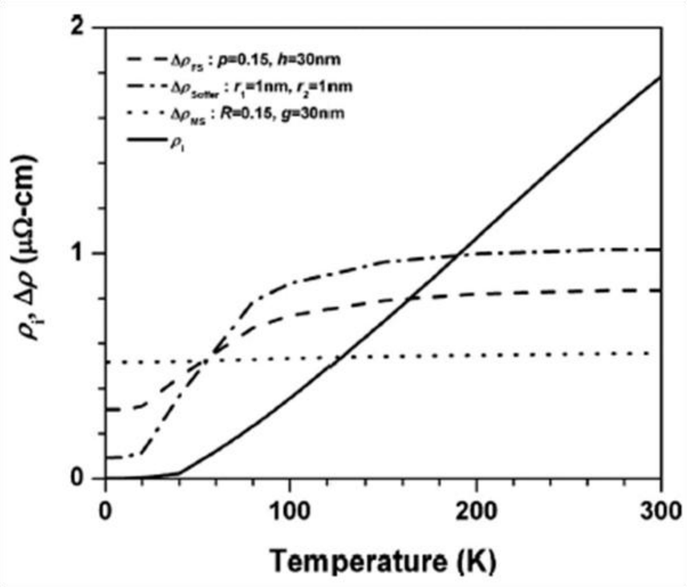


Figure 4.12 Cu resistivity as a function of temperature. [Sun *et al.*, 2010]

Assume the chip operation or service temperature to be at 110 ℃ and the EM test temperature at 300 ℃. One can calculate the electron MPF at these two temperatures to be 29nm and 19nm, respectively. Then the *Z** and wind force for each technology node at these two temperatures can be calculated and they are shown in Table 4.1. The *AR* is chosen as 1.8. The tabulated results show that *Z** can be up to 20% different at the testing temperature and operating temperature. But the electron wind force remains relatively constant with only a small temperature dependence, about 2%, at these two temperatures.

Table 4.1 Temperature effect on Z^* and electron wind force for different technology nodes.

Tech node	32nm	22nm	16nm	11nm
Line width	45nm	32nm	22nm	16nm
S (300°C)	0.80	0.74	0.66	0.58
S (110°C)	0.71	0.64	0.54	0.47
difference	11%	14%	18%	19%
F/F_0(300°C)	1.05	1.06	1.08	1.10
F/F_0(110°C)	1.07	1.09	1.10	1.12
difference	1.9%	2.8%	1.9%	1.8%

4.6 CONCLUSIONS

In conclusion, a size effect on the electron wind force for interface EM in a thin conductor film and a rectangular conductor line with a dielectric cap is evaluated. The analysis is relevant to Cu interconnects for current and the near-future technology nodes. The confinement by the film/line boundaries not only reduces the electrical conductivity, but also affects the effective charge Z^*e. The effective charge for a 20nm wide line is reduced to only 40% of that for an infinitely wide line. The electron wind force in this size region is slightly larger than that for an infinitely wide line even for a constant current density. Due to the fact that EM tests are performed at a relatively higher temperature at which the electron MFP is smaller than at room temperature, the temperature effect on the scaling of the effective charge and wind force is studied. The effective charge can have up to 20% difference for the service condition and EM testing condition. The wind force remains relatively constant at these two temperatures.

In summary, through the study in this chapter, one additional scaling factor for EM in Cu interconnects is evaluated.

Chapter 5: Fabrication of Silicon Nanotrenches by Self-aligned Sub-lithographic Masking Technique

This chapter investigates fabrication methods for making high-quality Si nanostructures. The purpose is to fabricate nanotrenches with well-defined geometry and deposit Cu into these trenches to study their resistivity and electromigration characteristics. Electron beam lithography and Si anisotropic wet etching are employed in the fabrication. To overcome the etching-related problems such as trench widening during etching, a self-aligned sub-lithographic masking technique is developed. This mask is a polymer layer formed along a pre-defined wide trench in fluorocarbon plasma. The subsequent wet etching yields nanotrenches with atomically smooth sidewalls along the two edges of each predefined trench. Si nanotrenches with width down to 20nm and AR up to 20 have been successfully fabricated with such technique. Potential applications of the structure in nanofluidics are discussed.

5.1 INTRODUCTION AND MOTIVATION

Due to the increasing difficulty of experimental study, modeling work is becoming more useful and important in advanced technology nodes. It is commonly assumed that interconnect lines are rectangular to simplify the model. For example, in Chapter 3, a rectangular line is assumed for void growth modeling and grain growth simulation. In Chapter 4, the same assumption is also adopted for electron wind force calculation. Models of resistivity scaling as well as many other studies also use rectangular lines for the sake of simplicity. Figure 5.1(a) shows a schematic of such an ideal rectangular structure. However, the cross-section of an actual Cu interconnect line usually has a taped profile, as shown in Figure 5.1(b). Therefore, a big gap in shape exists between the Cu lines in models and realistic structures. Having Cu lines with rectangular profiles would be of crucial importance to validate the models for resistivity, void growth, electron wind force and grain growth etc..

As scaling continues, the EM of Cu interconnects is ever more sensitive to process variations. A process defect may account for a considerable amount of variation in a Cu line in advanced technology nodes. An example for the line edge roughness (LER) induced line width variation has already been shown in Figure 1.9. Figure 5.1(c) shows an SEM image of a Chromium (Cr) line with LER. The LER does not scale similarly with line width. The current optical lithography reaches resolution limit at 22nm node but the next generation EUV lithography is not yet ready. The LER problem is expecting to have more effect on EM in the coming technology nodes due to the increasing surface to volume ratio. In addition, LER can also be introduced by reactive ion etching (RIE). The LER and other small process variations may easily induce a different failure mode for EM. This poses difficult challenge for the study of EM mechanisms beyond 22nm node. Because process variations are random, the lifetime could yield different distributions for different sets of samples. Therefore, it is highly valuable to develop processes to fabricate well controlled Cu nanolines with smooth sidewalls for study of the intrinsic EM mechanisms.

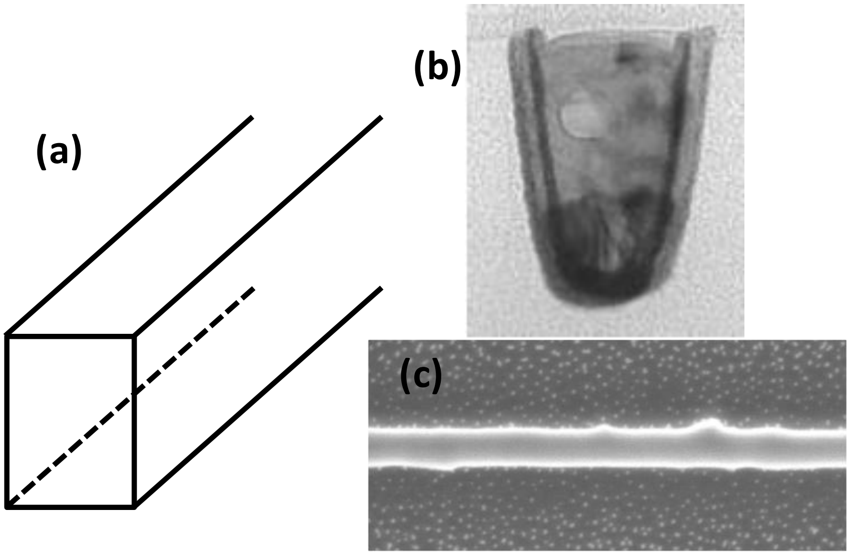


Figure 5.1 (a) Common model structure with rectangular cross-section and smooth side walls; (b) Cu interconnect line cross-section showing a taped profile [Cabral *et al.*, 2010]; (c) Cr line fabricated showing LER.

Since Cu lines are made by the damascene process, the profiles and the sidewalls of the Cu lines are mainly determined by the quality of trenches. The objective of this chapter is to develop methods for fabricating nanoscale trenches with well-defined geometries: rectangular cross-section and smooth sidewalls.

It is well known in Si micromachining that the etching of a single crystalline Si in solutions such as potassium hydroxide (KOH) and tetramethylammonium hydroxide (TMAH) is anisotropic. Different crystalline planes have very different etching rates. Figure 5.2 shows the etching rates for (111), (110) and (100) planes in 40 wt% KOH solution at different temperatures [Marchetti *et al.*, 1998]. The etching for (111) plane is two orders of magnitude slower than the other two planes. Etching virtually stops at the (111) plane and a smooth surface exposes after etching.

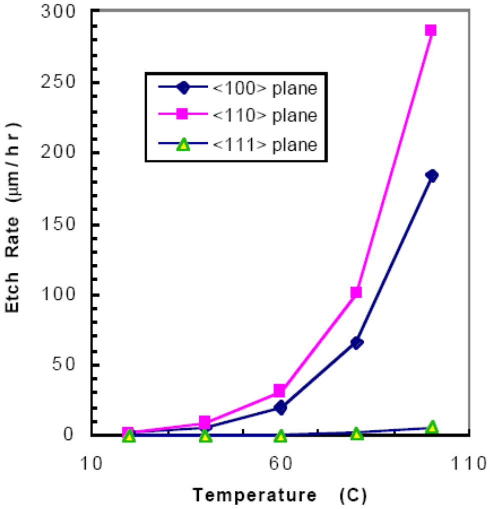


Figure 5.2 Si etching rates in KOH with respect to temperature for different crystalline planes. [Marchetti *et al.*, 1998]

Such feature of anisotropic wet etching (AWE) is widely used for fabrication of test structures for microelectromechanical systems (MEMS) study. A (110) Si wafer can be employed to achieve vertical sidewalls and a rectangular profile. If a trench pattern is defined along <112> direction, the Si wet etching goes vertical and exposes two (111) planes that are perpendicular to the (110) wafer surface. Figure 5.3 shows an SEM image of a microtrench etched on (110) wafer by a TMAH solution. The exposed sidewall is a smooth (111) plane.

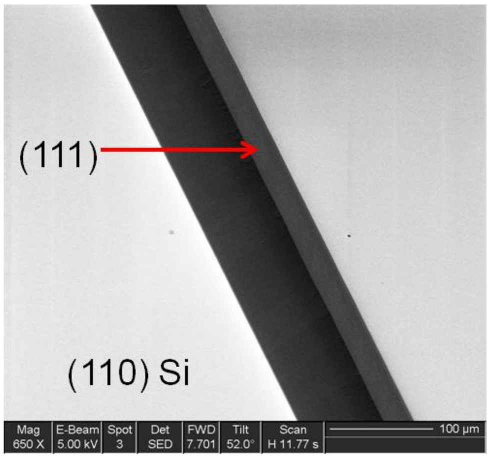


Figure 5.3 Si trench etched on an (110) wafer in TMAH solution. [Wu *et al.*, 2011]

The trench pattern at microscale shown in Figure 5.3 can be defined by conventional optical lithography (hard contact, i-line) with resolution around one micron. To achieve nanoscale trench width, electron beam lithography (EBL) is used in this study.

5.2 FABRICATION OF SI NANOLINES

The work started with fabricating Si nanolines which are reverse patterns of Si nanotrenches. The EBL system used in this study was a JEOL JBX 6000 system with a beam energy of 50 keV. The resist used was ZEP 520A, a mixture of ZEP520 and ZEP A. It has higher sensitivity than Poly(methyl methacrylate) (PMMA) due to the αCl group and higher dry etch resistance due to the α-methylstyrene.

Figure 5.4 shows the basic process flow chart for the fabrication of Si nanolines with EBL and AWE. TMAH was selected as the etchant solution because of its CMOS compatibility. TMAH etching was performed at a temperature of around 82 ℃. The processes started with Si thermal oxide (SiO_2) and Cr deposition in which SiO_2 was used as an etch mask for Si etching in TMAH and Cr a conductive layer for EBL to avoid charging problem. The thickness of these two layers varied in different processes but all about the order of 10nm. After EBL, the pattern was transferred down to Si layer by dry etching of Cr and SiO_2 through RIE. Then the TMAH etching was performed to etch Si. The processes were completed by removal of Cr and SiO_2 using diluted BOE (buffered oxide etchant) and Cr etchant respectively.

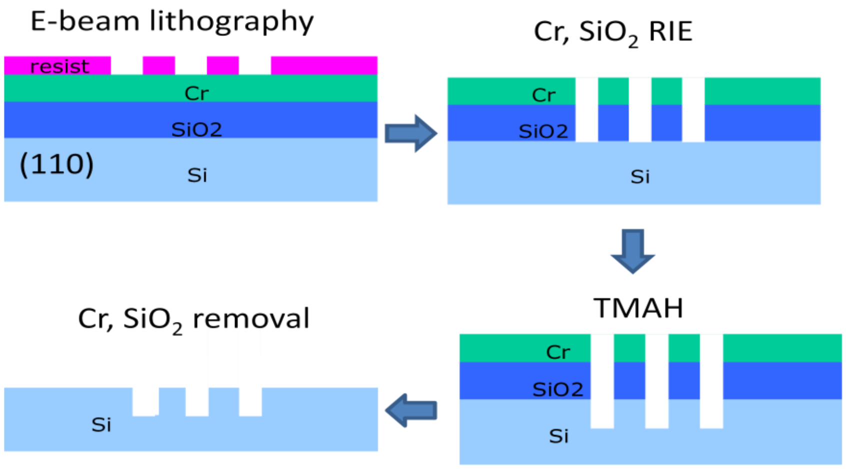


Figure 5.4 Process flow for fabrication of Si nanolines with EBL and TMAH etching.

A dose test for EBL should be performed prior to real pattern writing. The standard dose for the JEOL system is 180μC/cm^2. A dose for actual exposure can vary from -60% to +10%, where -60% means 60% lower than the standard dose and +10% means 10% higher than the standard dose. Figure 5.5 is an example of dose test for 500nm wide lines with 1μm pitch. The SEM images of the e-beam resist are taken after development. In this particular case, -40% is found as the right dose to generate smooth clean patterns reproducing the feature size designed in graphic database system (GDS) files.

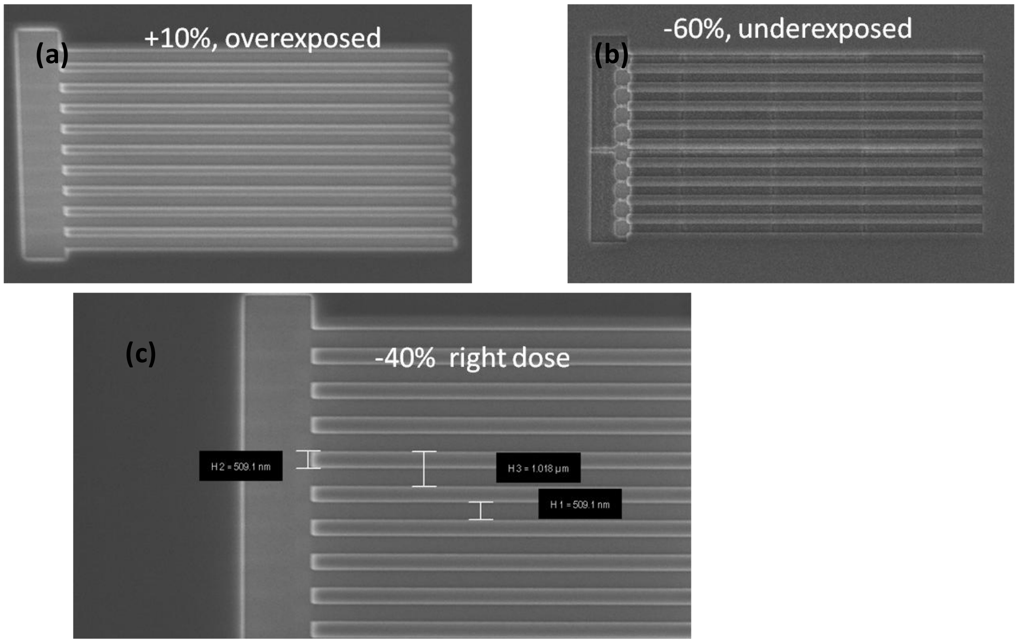


Figure 5.5 An example of dose test for EBL.

One critical issue for the nanoline fabrication is aligning the line to the <112> crystalline direction. The requirement of alignment precision is much more stringent for nanoscale fabrication compared to microscale fabrication. The wafer flat or cleave edge usually has a misalignment of about 2° with <112> direction. A simple estimation indicates that a misalignment of 0.6° will etch away a nanoline initially designed of 100nm wide and 100µm long. To overcome this issue, an alignment technique with precision of 0.01° has been developed at UT Austin [Li, 2007, Luo, 2009]. Figure 5.6(a) shows an alignment test pattern array with angle varying in the range of ±2°. Figure 5.6(b) shows the SEM images of the test pattern after TMAH etching. For those pattern misaligned with <112> direction, the Cr lines peel off because the Si underneath is etched away. The patterns in the red rectangular align better with <112> direction. The best alignment has the widest Si line width under Cr and SiO_2.

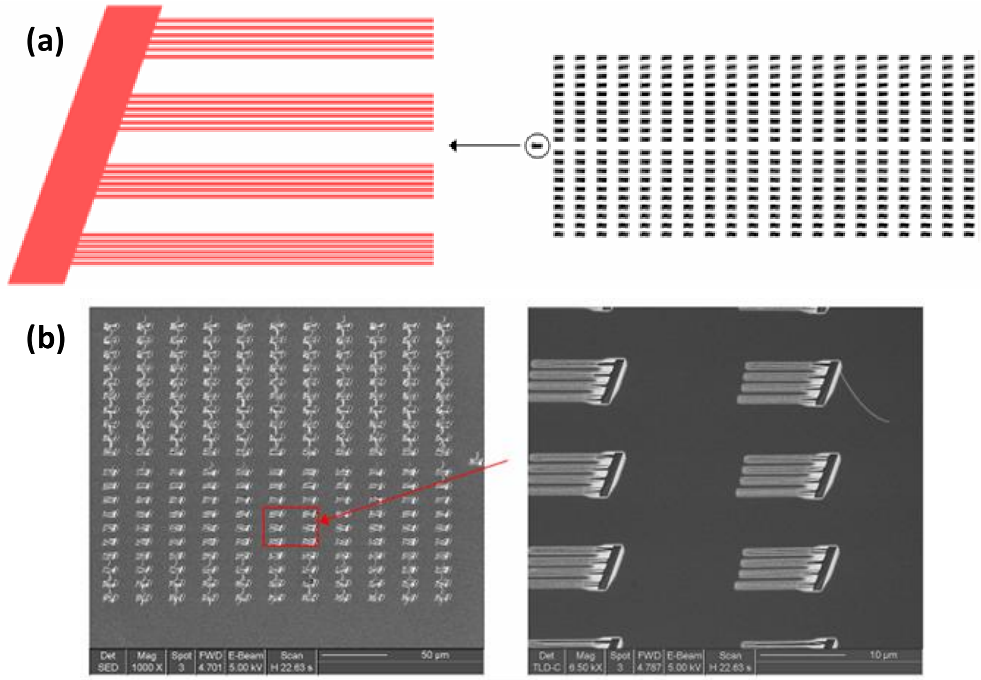


Figure 5.6 (a) The designed angle alignment test pattern. An array contains 401 patterns. The angle between 2 neighboring patterns is 0.01°. (b) The alignment test pattern after TMAH etching.

Figure 5.7 shows SEM images of Si nanolines fabricated with this method. The plan view exhibits clearly that the width of lines is uniform and LER is suppressed. The side view shows the vertical etched profile with atomically smooth sidewalls. The crystalline directions are also marked in the side view image. Si nanolines with such a high quality open up many interesting studies on their mechanical and electrical properties [Li, 2007, Luo, 2009, Li *et al.*, 2008, Li *et al.*, 2009].

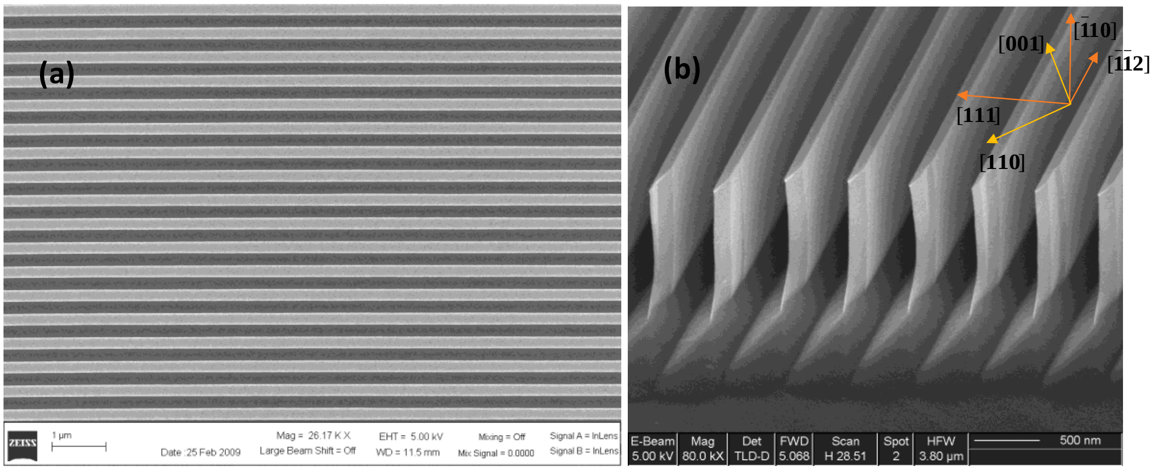

(a)
(b)
[001]
$[\bar{1}10]$
$[\bar{1}\bar{1}2]$
[111]
[110]
ZEISS
1 μm
Date :25 Feb 2009
Mag = 26.17 K X
Large Beam Shift = Off
EHT = 5.00 kV
WD = 11.5 mm
Mixing = Off
Mix Signal = 0.0000
Signal A = InLens
Signal B = InLens
E-Beam 5.00 kV
Mag 80.0 kX
Det TLD-D
FWD 5.068
Scan H 28.51
Spot 2
HFW 3.80 μm
500 nm

Figure 5.6 (a) Plan view and (b) side view (52°) of Si nanolines fabricated by EBL and AWE.

A force-sensor system was developed to measure the mechanical response of the Si nanolines to a lateral force [Niese *et al.*, 2010]. This work is performed in Dr. Michael Hecker's group in Globalfoundries at Dresden in Germany. Figure 5.7 (a) shows an SEM image of a Si nanoline, which is deflected by a tungsten tip. The in-situ observation shows that the nanolines can recover from a relatively large deflection. The finite element analysis (FEA) demonstrates that the maximum strain can be beyond 9% before the nanolines yield, as shown in Figure 5.7(b). This value is much larger than the yield strain for bulk Si (~2%). It also verifies the high quality of the Si nanostructures fabricated by this method.

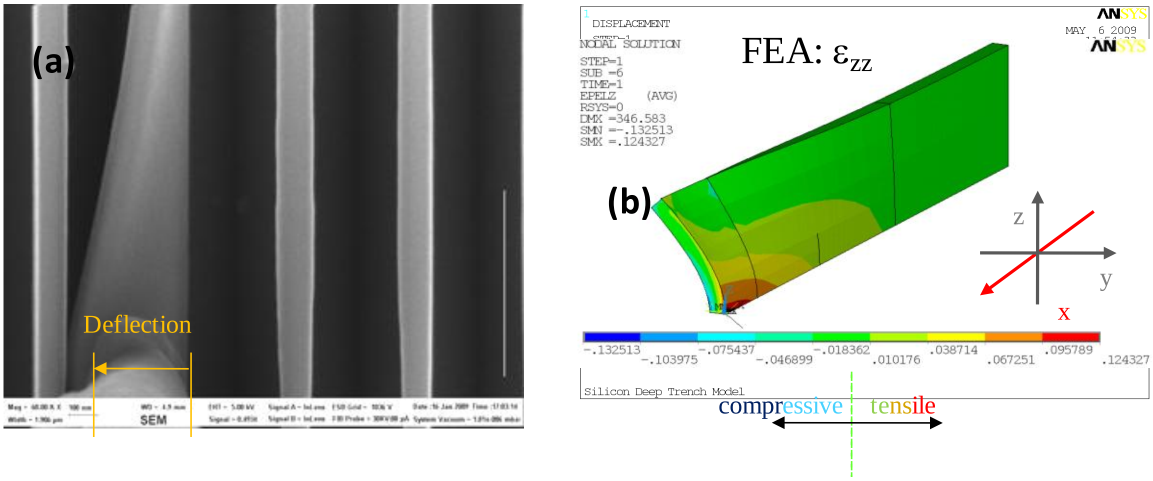


Figure 5.7 (a) Si nanoline deflected by a tungsten tip; (b) FEA shows the strain distribution in a Si nanoline when deflected.

With this fabrication technique, a line width down to 20nm range and with an aspect ratio (AR = thickness over width) as high as 40 has been achieved. Figure 5.8 (a) shows Si nanolines with 30nm width, while Figure 5.8(b) shows Si nanolines with AR of about 40.

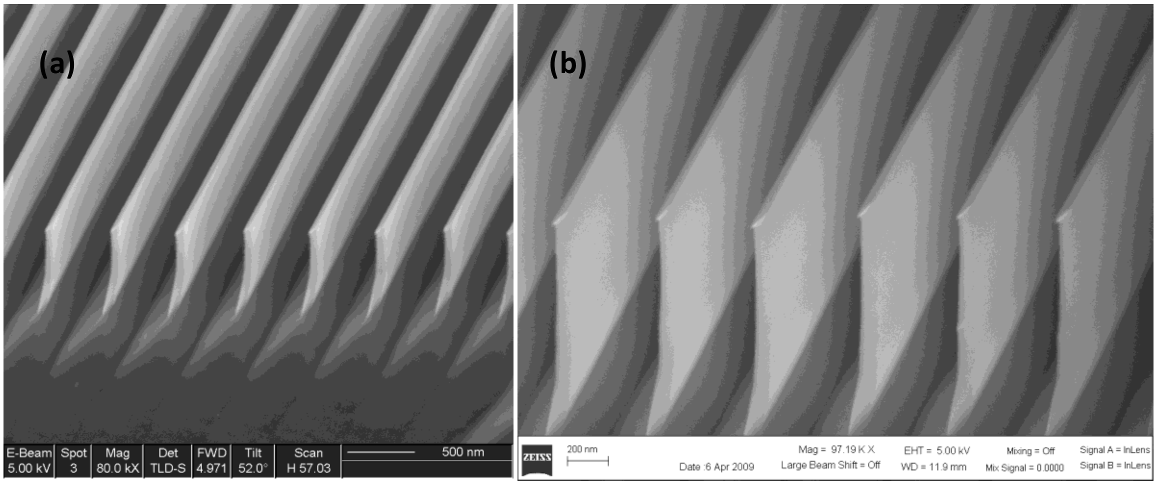
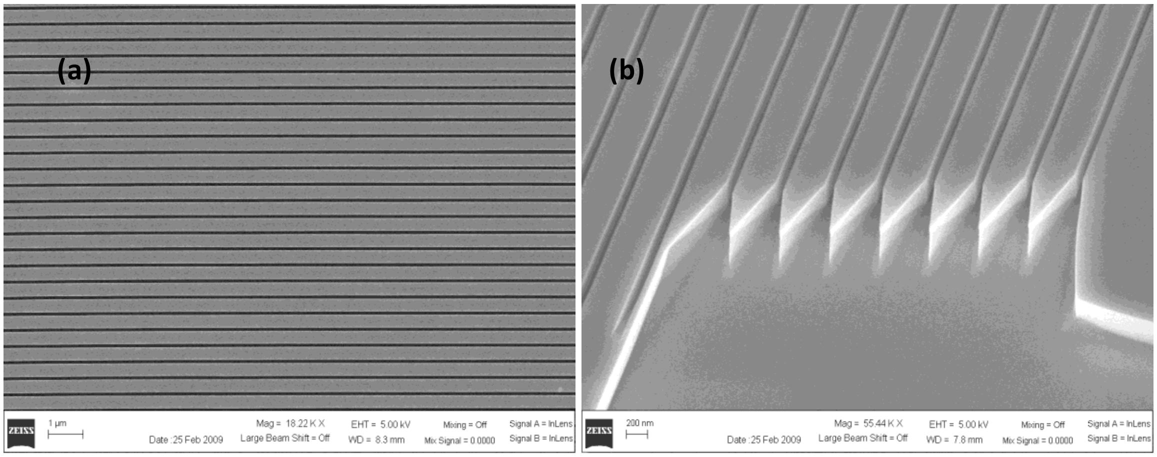

(a)
E-Beam 5.00 kV
Spot 3
Mag 80.0 kX
Det TLD-S
FWD 4.971
Tilt 52.0°
Scan H 57.03
500 nm
(b)
200 nm
Date :6 Apr 2009
Mag = 97.19 K X
Large Beam Shift = Off
EHT = 5.00 kV
WD = 11.9 mm
Mixing = Off
Mix Signal = 0.0000
Signal A = InLens
Signal B = InLens

Figure 5.8 (a) 30nm wide Si nanolines; (b) Si nanolines with AR of 40.

5.3 FABRICATION OF SI NANOTRENCHES WITH CONTACT PADS

Trenches are reverse patterns of lines. So the method for Si nanoline fabrication can be applied to Si nanotrenches as well. Figure 5.9 shows SEM images of an array of 90nm wide Si nanotrenches. The same vertical profile and smooth sidewalls can be observed. The trench depth in this case is about 900nm. It can be better controlled if a silicon-on-insulator (SOI) wafer is used.


(a)
(b)
ZEISS
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ZEISS
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Date :25 Feb 2009
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Large Beam Shift = Off
EHT = 5.00 kV
WD = 7.8 mm
Mixing = Off
Mix Signal = 0.0000
Signal A = InLens
Signal B = InLens

Figure 5.9 (a) Plan view and (b) side view (tilt = 30°) of Si nanotrenches fabricated by EBL and AWE.

The motivation of nanotrench fabrication is to deposit it with Cu and measure the electrical properties. So contact pads need to be integrated with the nanotrenches. Figure 5.10 shows a designed pattern for an array of nanotrenches in which each nanotrench is integrated with four contact pads. The shape of the contact pad is a rhombus with length of 100µm. Due to the relatively large area of the contact pads, a bigger electron beam current is required for exposure of EBL in order to save time. A current of 10nA is selected for the exposure of contact pads, while the current for the exposure of nanotrenches is 100pA to achieve better resolution. Such two-layer exposure requires alignment between two writings. Therefore alignment marks have to be fabricated first on the chip, which requires another lithography step. Figure 5.11 shows the process flow for fabrication of nanotrenches with contact pads. The alignment marks used in this study is Au marks with thickness of around 100nm.

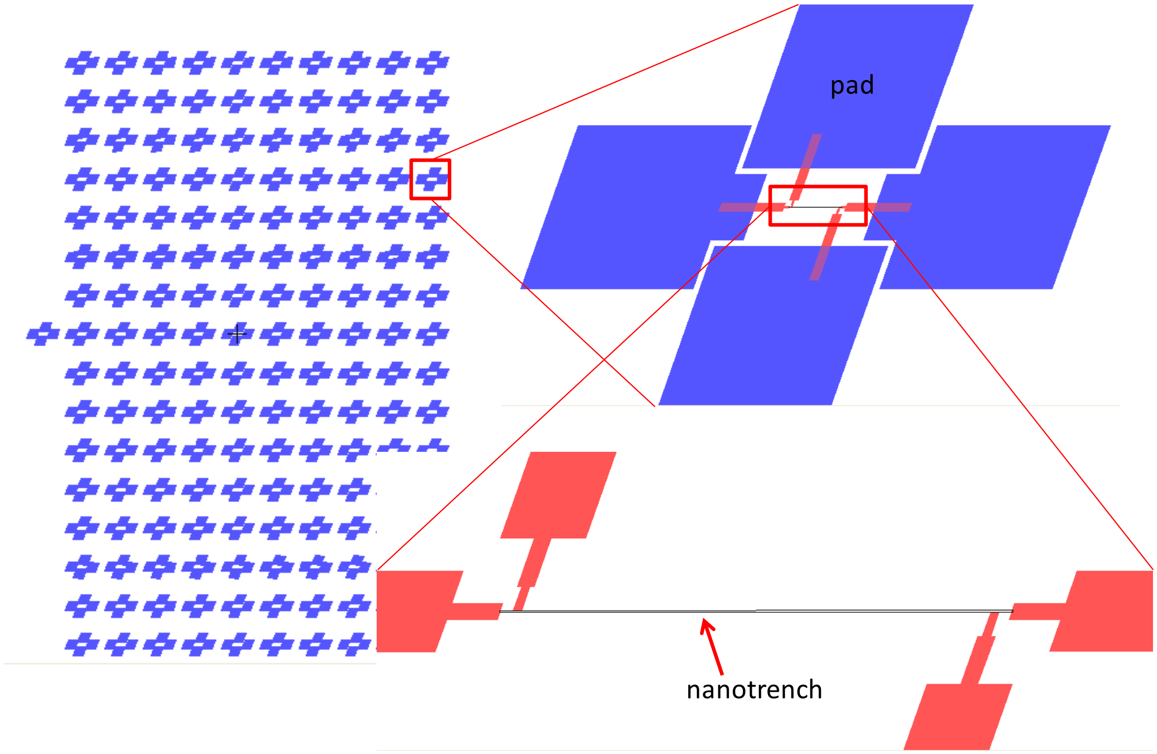

pad
nanotrench

Figure 5.10 Designed pattern for an array of nanotrenches integrated with contact pads.

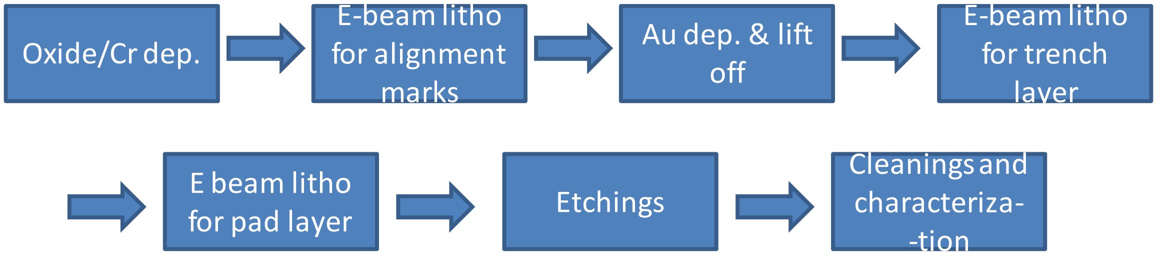

Oxide/Cr dep.
E-beam litho for alignment marks
Au dep. & lift off
E-beam litho for trench layer
E beam litho for pad layer
Etchings
Cleanings and characteriza- -tion

Figure 5.11 Process flow for fabrication of nanotrenches with contact pads.

Figure 5.12 shows a successful implementation of the process flow in which a 160nm wide nanotrench connected with four contact pads are fabricated. The length and depth of the trench are 30μm and 470nm, respectively. The distance between two inner contact probes is 28μm.

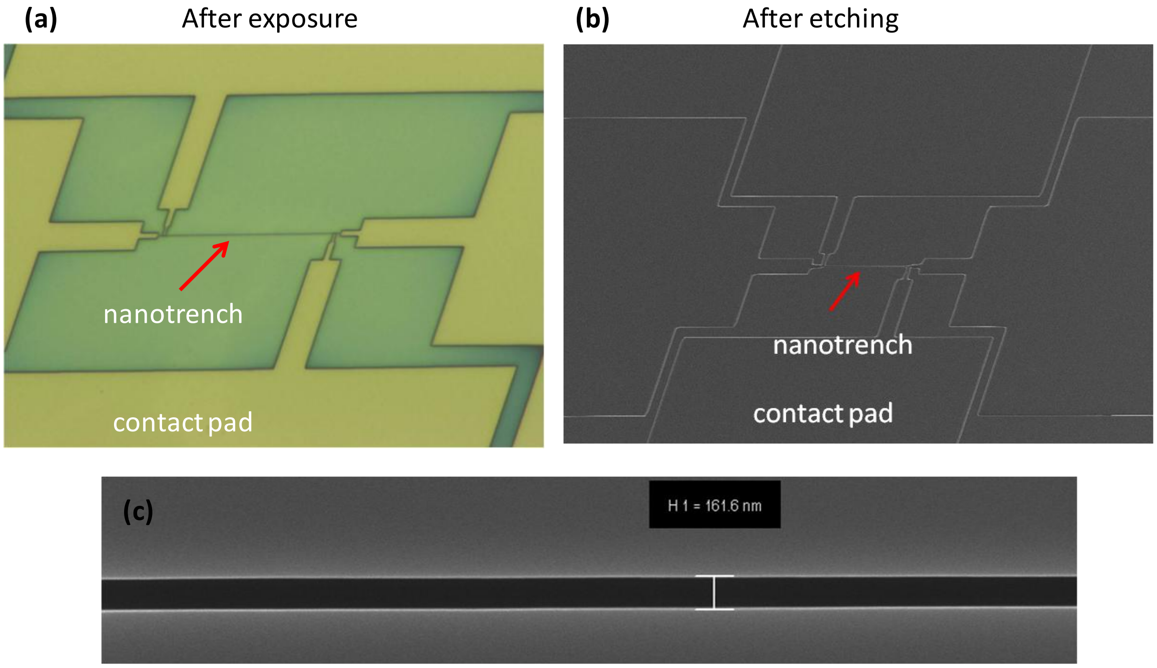


Figure 5.12 (a) Optical microscopy (OM) image of a nanotrench with contact pads after resist development; (b) SEM image of a Si nanotrench with contact pads after etching; (c) SEM image of the Si nanotrench.

Then the barrier deposition and Cu plating were performed in the fabricated Si nanotrenches, in collaboration with J. Bartha's group at Technical University Dresden in Germany. Figure 5.13 shows a cross-sectional view of Si nanotrenches that are filled with electro-chemical deposition (ECD) Cu. Cu was also plated into the Si nanotrenches with contact pads. After Cu filling, the Cu overburden was removed by chemical-mechanical polishing (CMP). Figure 5.14 is an optical microscope (OM) image of a Cu line with contact pads after CMP. Electrical measurement was also performed on the Cu nanolines with contact pads. The resistivity measured is about 2-4 μΩ-cm, which falls in the reasonable range for ECD Cu [Zhang *et al.*, 2007].

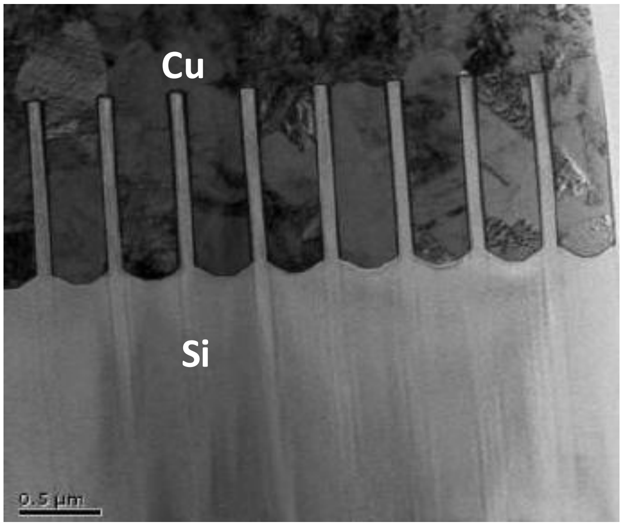


Figure 5.13 TEM image of the cross-section of Si nanotrenches deposited with ECD Cu.

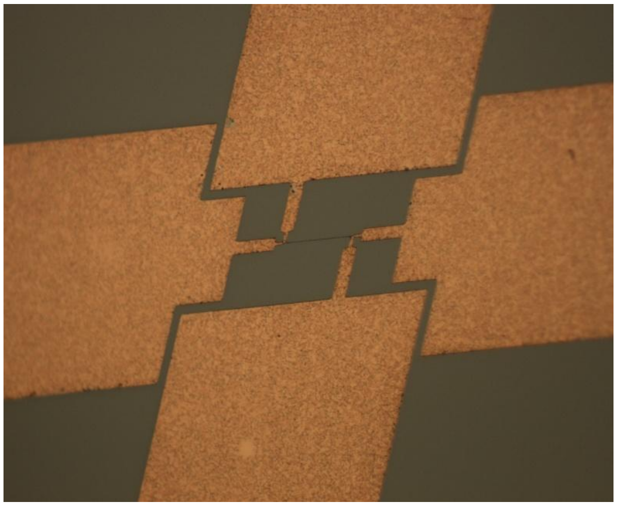


Figure 5.14 OM image of a Cu line deposited in the Si nanotrench connected with contact pads. The image was taken after Cu CMP.

The electron mean free path for Cu at room temperature is 39nm. To observe size effect due to interface or grain boundary scattering, the width of Cu line should be in this range. However, it is difficult to fabricate Si nanotrenches with width down to this range, although the resolution of EBL can be as low as 20nm. This is because the etching induced trench widening effect, as illustrated in Figure 5.15. A native oxide layer is left on Si after the wafer is taken out of the RIE chamber. This oxide layer has to be removed by dipping into BOE before Si etching using TMAH. BOE, which is a diluted HF solution, etches SiO_2 in an isotropic manner. An undercut forms after BOE dipping. The widened pattern is then transferred into the Si layer causing the Si trench widened too. Even if one successfully patterned a 20nm wide trench on the resist, the width of Si trench would still be around 100nm after etching. And this width is not well controlled. A novel technique is to be developed in the next section to eliminate this trench widening effect.

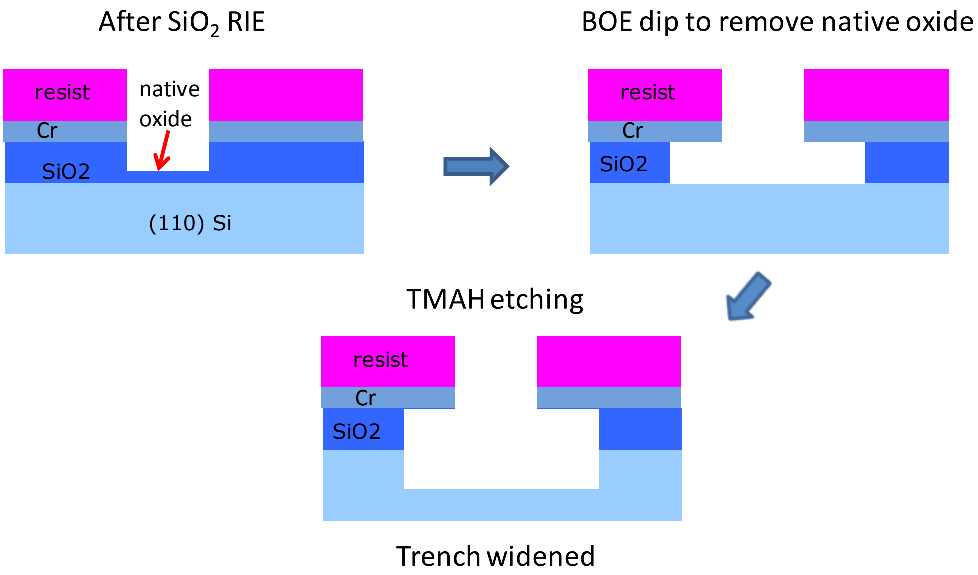

After SiO_2 RIE
resist
native oxide
Cr
SiO2
(110) Si
BOE dip to remove native oxide
resist
Cr
SiO2
TMAH etching
resist
Cr
SiO2
Trench widened

Figure 5.15 Process flows showing the trench widening effect in Si nanotrench fabrication.

5.4 SELF-ALIGNED SUB-LITHOGRAPHIC MASK

5.4.1 Fundamentals of Fluorocarbon Plasma

Fluorine-based chemistries are commonly used in RIE of SiO_2. The reaction $4F + SiO_2 \rightarrow SiF_4 + O_2$ generates very volatile products SiF_4 [Plummer *et al.*, 2000]. The etching of SiO_2 with gases such as SF_6, CF_4 and NF_3 is very isotropic. Carbon content is usually added into the plasma to achieve anisotropic etching, thus, to maintain the critical dimension (CD). High Carbon (C) to Fluorine (F) ratio leads to polymer formation. The polymer on the sidewalls can work as an inhibitor to prevent the undercut induced by lateral etching. Polymer on the bottom of pattern receives ion bombardment and anisotropic etching achieves through a bond-breaking process. Hydrogen is effective in increasing the C to F ratio in plasma by reacting with atomic F to form HF. CHF_3 is a suitable gas to generate plasma with high C to F ratio. Small amount of O_2 is also added to keep the etching vertical. Otherwise, the polymer formed on sidewalls would be too thick, which leads to a taped etching profile. CHF_3 and O_2 mixture are the gases used in this study for SiO_2 RIE.

Another benefit of high C to F ratio is the increased etch selectivity of SiO_2 over Si. The polymer formation is more effective on Si surfaces than on SiO_2 surfaces. The reason is believed to be that the oxygen in SiO_2 reacts with carbon, forming carbon monoxide [Plummer *et al.*, 2000]. This process leads to less polymer accumulation in the SiO_2 surfaces compared to Si surfaces during etching. The polymer residue layer on the Si surfaces should be removed after etching. This is achieved by using an O_2, CF_4 or H_2 plasma treatment at an elevated temperature. The polymer residue can also be removed by wet treatment in a Piranha solution which is a mixture of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2).

5.4.2 Polymer Residue Layer as an Etch Mask

It is found that the polymer residue can work as an etch mask for Si anisotropic wet etching (AWE). As shown in Figure 5.16, the polymer residue, which is called composite material by plasma (CMP) in Ref. [Normand *et al.*, 2001], protects the Si underneath in the etching solution of ethylenediaminepyrocatechol-water (EPW). EPW is another kind of anisotropic etching solution similar to KOH and TMAH.

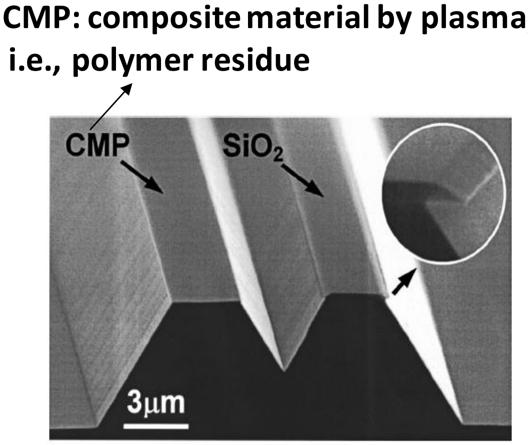
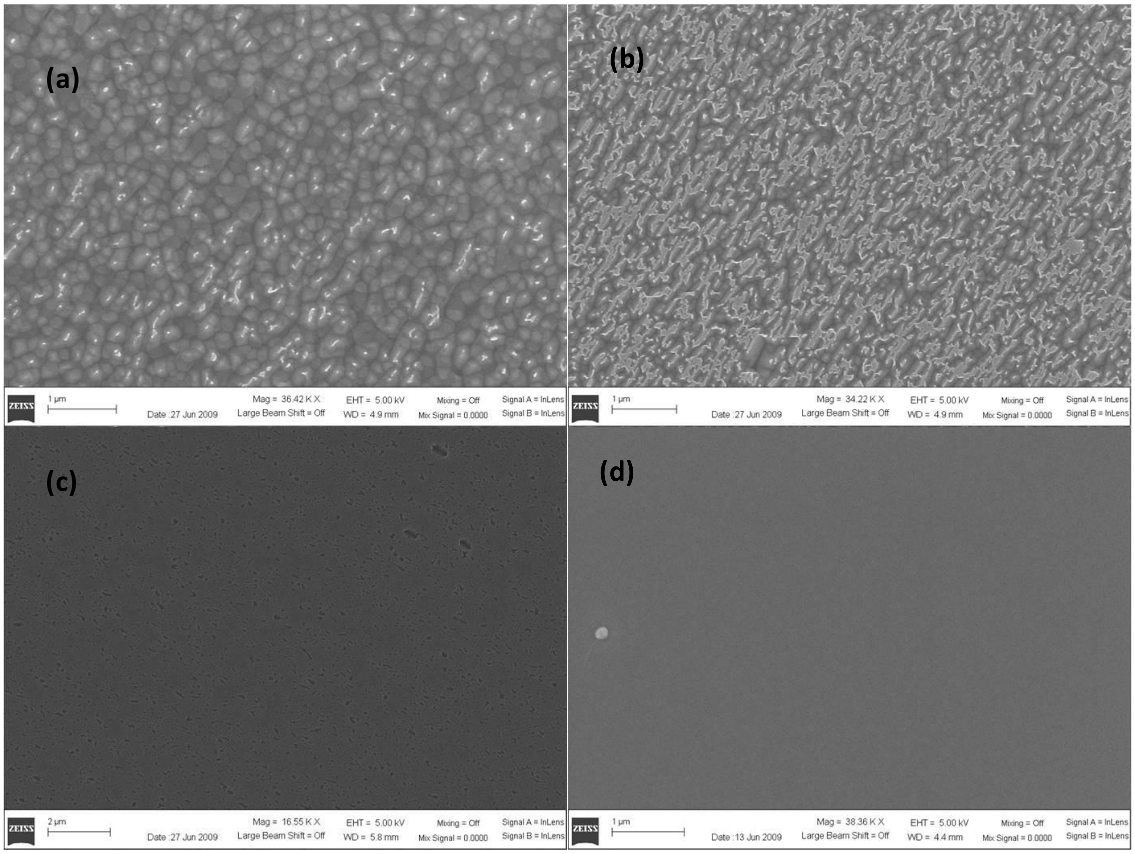

CMP: composite material by plasma, i.e., polymer residue

Figure 5.16 SEM image of mesas on (100) Si anisotropically etched by EPW. Both the polymer residue (CMP) and SiO_2 work as etch masks. [Normand *et al.*, 2001]

The capability of the polymer residue being an etch mask in the TMAH solution is tested in this study. Figure 5.17 shows SEM images of (110) Si treated with CHF_3/O_2 plasma with different plasma conditions and then etched in TMAH. In Figure 5.17(a), the polymer residue only covers isolated areas of Si surface, which leads to formation of Si islands with size in 200nm range after Si etching. The coverage of Si by the polymer is more satisfactory in Figure 5.17(b) and (c). In Figure 5.17(d), the Si surface is masked by the polymer residue well. The plasma condition for Figure 5.17(d) is: 50 mTorr pressure, 40 sccm flow rate for CHF_3, 3 sccm flow rate for O_2 and 360V DC bias.


(a)
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Mix Signal = 0.0000
Signal A = InLens
Signal B = InLens
(b)
1 µm
Date :27 Jun 2009
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Large Beam Shift = Off
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WD = 4.9 mm
Mixing = Off
Mix Signal = 0.0000
Signal A = InLens
Signal B = InLens
(c)
2 µm
Date :27 Jun 2009
Mag = 16.55 K X
Large Beam Shift = Off
EHT = 5.00 kV
WD = 5.8 mm
Mixing = Off
Mix Signal = 0.0000
Signal A = InLens
Signal B = InLens
(d)
1 µm
Date :13 Jun 2009
Mag = 38.36 K X
Large Beam Shift = Off
EHT = 5.00 kV
WD = 4.4 mm
Mixing = Off
Mix Signal = 0.0000
Signal A = InLens
Signal B = InLens

Figure 5.17 Masking capabilities for the polymer residue formed in different plasma conditions in the TMAH solution. The mask protects Si underneath better and better from (a) to (d).

With the plasma conditions described above, the thickness of the polymer residue layer is about 2nm, measured by spectroscopic ellipsometry (SE). The chemical composition in the polymer is analyzed by X-ray photoelectron spectroscopy (XPS). The result presented in Figure 5.18 shows that the polymer is mainly composed of fluorine, carbon and oxygen. This composition and their percentage are found to be relatively independent on the thermal oxide thickness. Even for a blanked wafer with only native oxide on it, the polymer layer after the same plasma treatment is composed of similar chemistry.

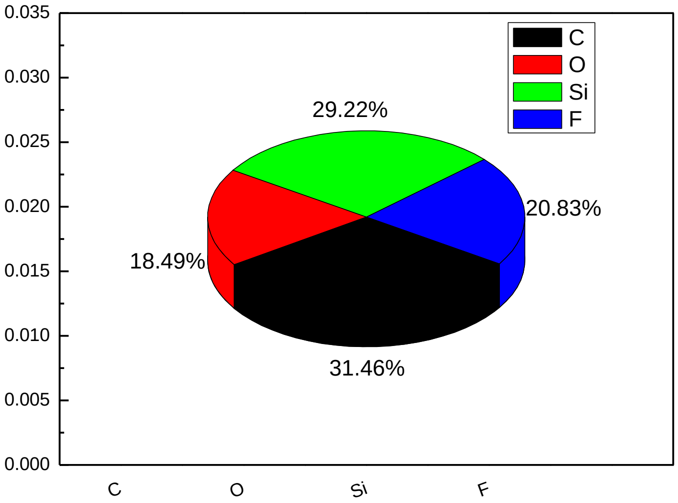

Figure 5.18 Chemical composition analysis of the polymer residue layer by XPS.

5.4.3 Sub-lithographic Mask

Till now, only the masking property of the polymer layer in TMAH has been studied. To achieve sub-lithographic patterning, the polymer has to be removed partially. For this purpose, one can make use of a unique feature observed in RIE – microtrenching effect.

Microtrenching is a phenomenon that the etch rate near the corners of a trench bottom is larger than at the center of the trench bottom. This leads to two smaller mictrotrenches at the corners as shown in Figure 5.19(a). It is caused by non-uniform ion bombardment in the trench. One of the mechanisms proposed is that the energetic ions impinging on the sidewalls at grazing angles (>80°) are reflected towards the bottom of the trench, as shown in Figure 5.19(b). The ion bombardment removes more polymer near the corners of the trench and accelerate the etch rate in that area.

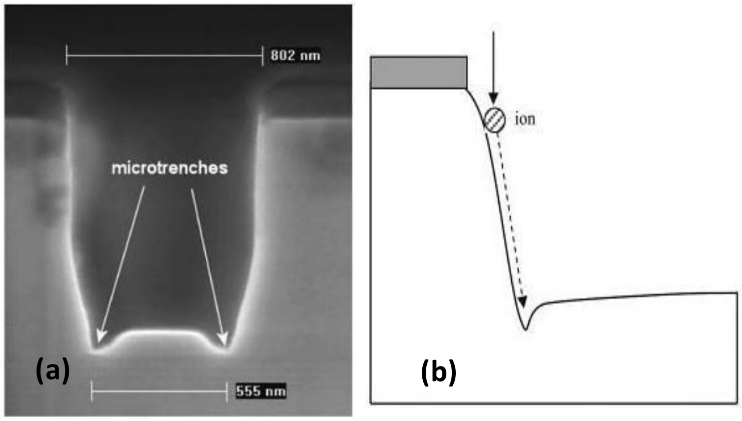

Figure 5.19 (a) Cross-sectional SEM image of microtrenching effect; (b) mechanism of microtrenching—sidewall reflection of ions. [Cui, 2008]

Another mechanism for microtrenching is the negative charging of sidewalls [Shul *et al.*, 2000], as shown in Figure 5.20(a). Due to the lighter masses, electrons in the plasma move much faster than ions, thus the sidewalls of the trench may be charged by electrons. The electric field created by the charged sidewalls deflects the ion flux and attracts more ions close to the corners of the trench. This leads to more ion sputtering and polymer removal, thus, a higher etch rate, near the corners.

With either mechanism, less polymer residue near the corners of a trench compared to the center of the trench is expected after SiO_2 RIE. This has been verified by the high resolution TEM image of the cross-section of a trench after SiO_2 RIE, as shown in Figure 5.20(b). Such non-uniform polymer distribution in the trench can be used as a sub-lithographic mask. As proposed in Figure 5.21, after SiO_2 RIE, the polymer residue covers most of the Si in the trench except the area close to two corners. The wafer is then etched in TMAH without polymer removal (A BOE dipping is still performed to remove oxide formed when the wafer is exposed to the air.). Only two very narrow nanotrenches, which are self-aligned with the original pattern edges, will be etched into Si. Therefore, it is named as self-aligned sub-lithographic mask (SSM).

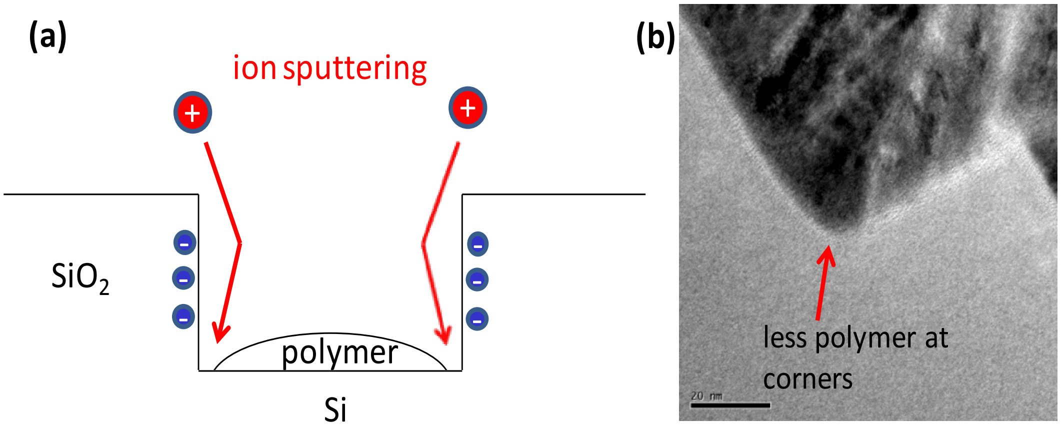
(a)
ion sputtering
+
+
SiO2
polymer
Si
(b)
less polymer at corners
20 nm

Figure 5.20 (a) Schematic of sidewall charging leading to more ion sputtering near trench corners; (b) TEM cross-sectional view of the distribution of polymer residue layer in a trench after SiO_2 RIE.

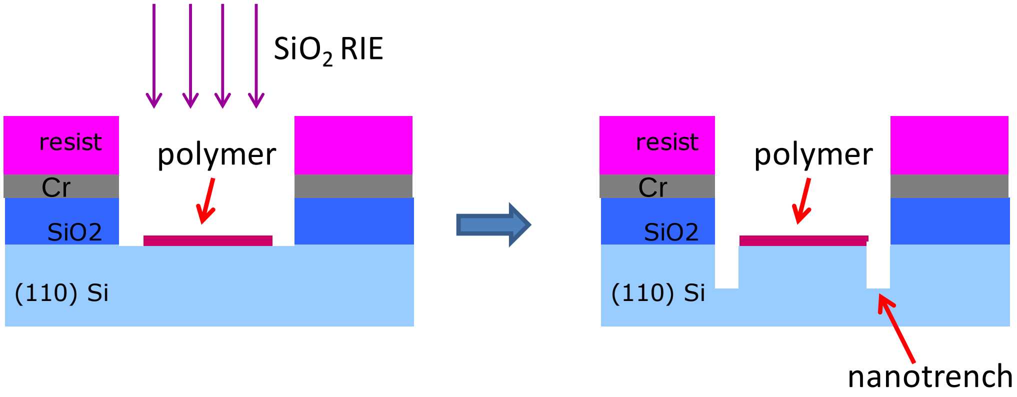
SiO2 RIE
resist
Cr
SiO2
polymer
(110) Si
resist
Cr
SiO2
polymer
(110) Si
nanotrench

Figure 5.21 Process to fabricate nanotrenches by using the polymer residue as SSM.

Figure 5.22 shows SEM images of nanotrenches fabricated by the SSM technique. The initial pattern designed is 200nm wide trenches with 450nm pitch. The Si trench width after fabrication is 60nm. This technique not only overcomes the challenge of trench widening mentioned in last section but also shrinks the trench width compared to lithographic definition. Furthermore, the pitch of the pattern is also doubled, for example, there are two 60nm wide trenches with 450nm spacing. The SEM images clearly show that this method still inherits the high quality (rectangular profile and smooth sidewalls) of trenches. In addition, the yield of such method is surprisingly high as long as the plasma is tuned to a right condition. No defect is found in a large array of nanotrenches.

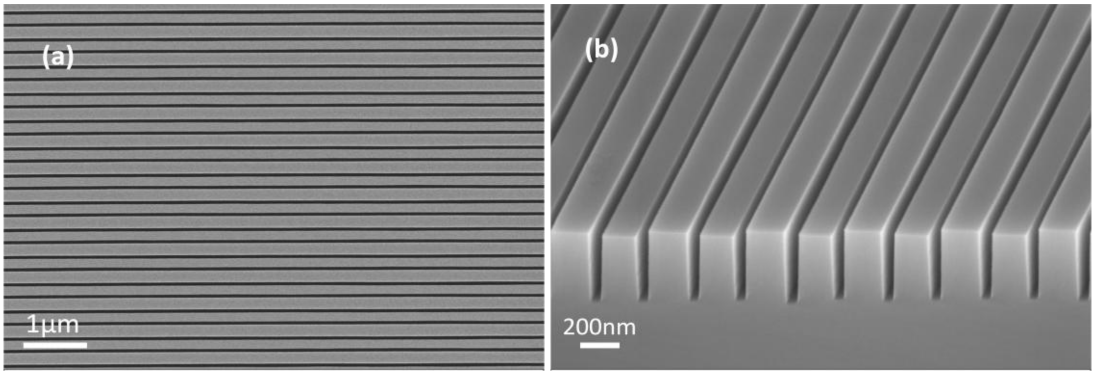

Figure 5.22 Nanotrenches fabricated by SSM technique. Trench width is 60nm. (a) Plane view; (b) Side view (tilt = 45°).

It is interesting to compare the SSM method with the self-aligned double patterning which is widely used in semiconductor manufacturing in advanced technology nodes. As shown in the process flow in Figure 5.23, spacer masks are formed by an additional film deposition and etching, to overcome the resolution limit of optical lithography and to double the pitch. One of the main applications for such technique is to fabricate ultrathin fins for FinFETs. A trench is a reverse pattern of a fin, but the ideas of improving the resolution limit and doubling pattern pitch are similar for these two methods. However, the SSM method in this study does not require any additional thin film deposition and etching steps. The mask is self-formed during the SiO_2 RIE. In fact, it even simplifies the process step, by eliminating the polymer residue removal step, compared to conventional process shown in Figure 5.4.

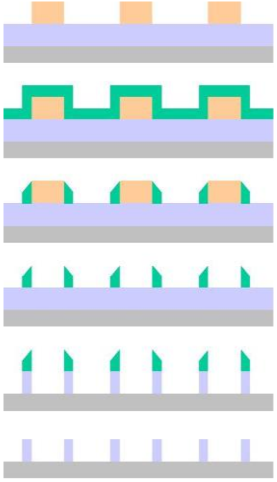

Figure 5.23 Process flow of self-aligned double patterning: first pattern; deposition; spacer formation by etching; first pattern removal; etching with spacer mask; final pattern.

Since the final trench width is independent of the initial trench width designed, one question naturally emerges: how to control the trench width? In principle, it can be controlled by changing plasma conditions and the thickness of SiO_2 layer to tune the ion sputtering distribution. As an example, four samples were prepared under the same processes except the power of plasma for SiO_2 RIE. Varying power of 300W, 400W, 500W and 600W were used. The four samples were from the same wafer and experienced the EBL in a single writing, which ensures their identical crystalline alignments. After RIEs, the four samples were attached to a single substrate and etched in

TMAH at the same time. The width of trenches was measured by SEM and the results are plotted in Figure 5.24. It is found that higher RIE power produces wider trenches. And the relationship between the power and trench width is linearly correlated in the range observed. The polymer residue near the corners is mainly removed by ion bombardment. The ions in the plasma are more energetic to sputter the polymer, when higher RIE power is used. This leads to less polymer coverage close to the two edges of a pre-defined trench, which probably explains why the width if Si trenches is larger with higher RIE power.

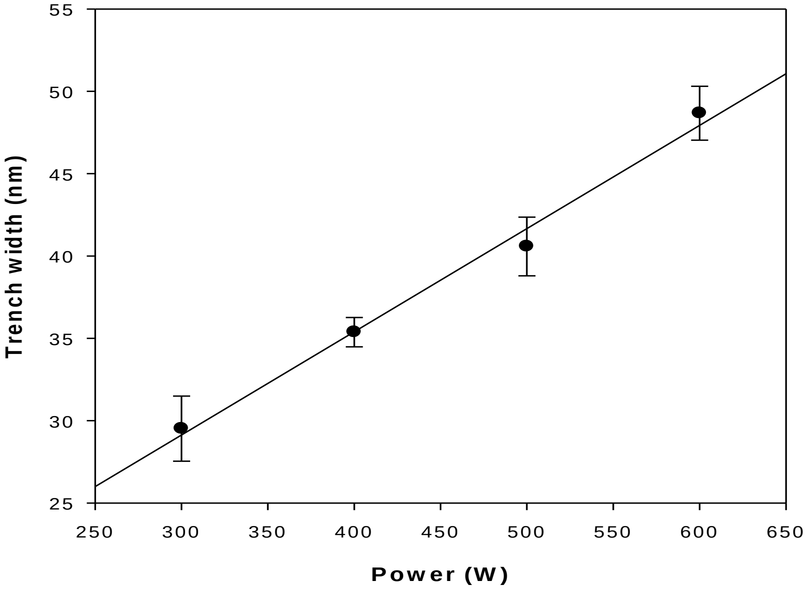

Figure 5.24 Control the width of Si nanotrenches by SiO_2 RIE power.

The width of the nanotrenches fabricated by the SSM technique can be down to 20nm range. Figure 5.25 shows two examples of such ultra narrow nanotrenches: 35nm wide for one; 25nm wide for the other.

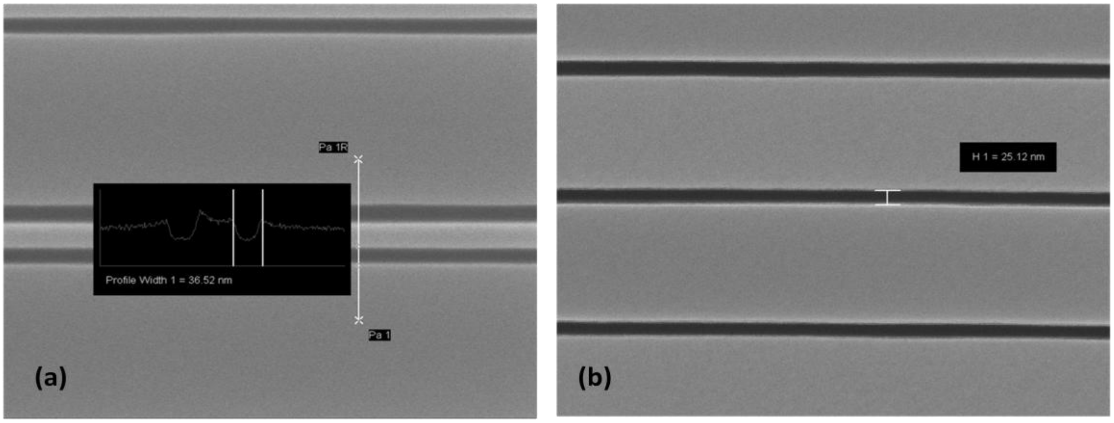

Figure 5.25 Nanotrenches with (a) 35nm width and (b) 25nm width.

The width uniformity of the nanotrenches is also explored. Figure 5.26 shows the width uniformity along a 12mm-long nanotrenches. The measured width variation at different locations of the long trench is only 1.3nm. Figure 5.27 shows the width uniformity along an array of nanotrenches. The measured width variation for different trenches in the array is 1.4nm. Note that the measured variation is mainly caused by the SEM measurement error because it is beyond the resolution limit of the microscope. The actual line width can be even more uniform than the measured.

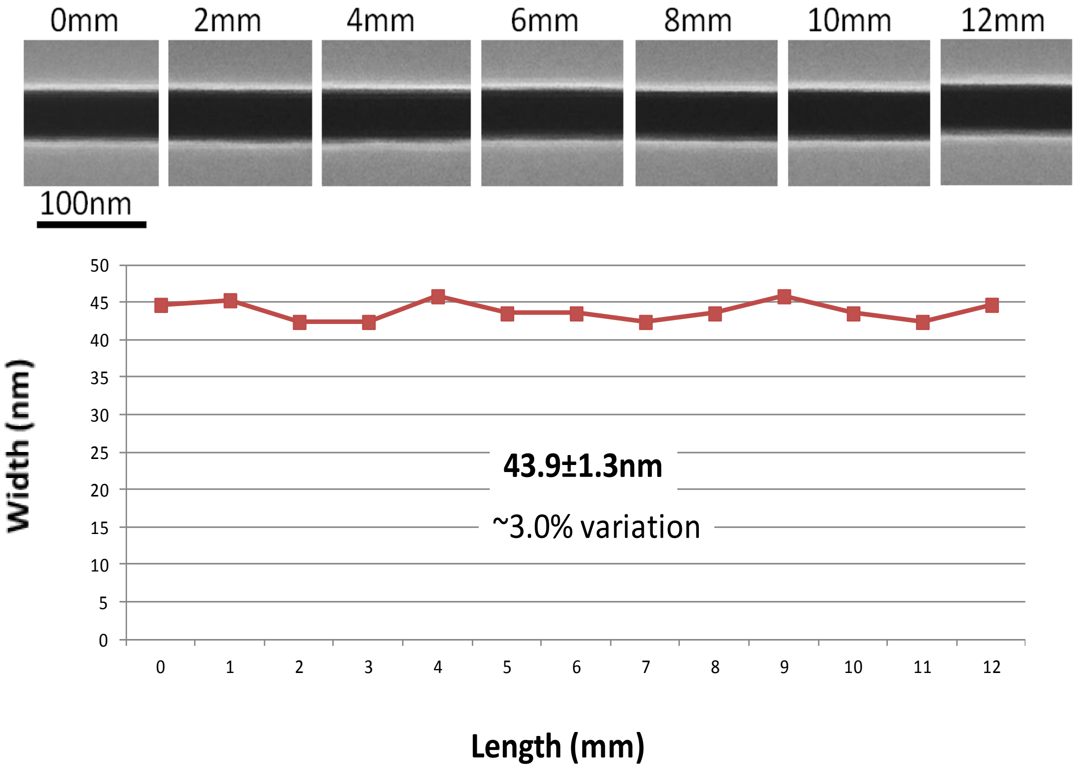

Figure 5.26 Width uniformity along a single nanotrench.

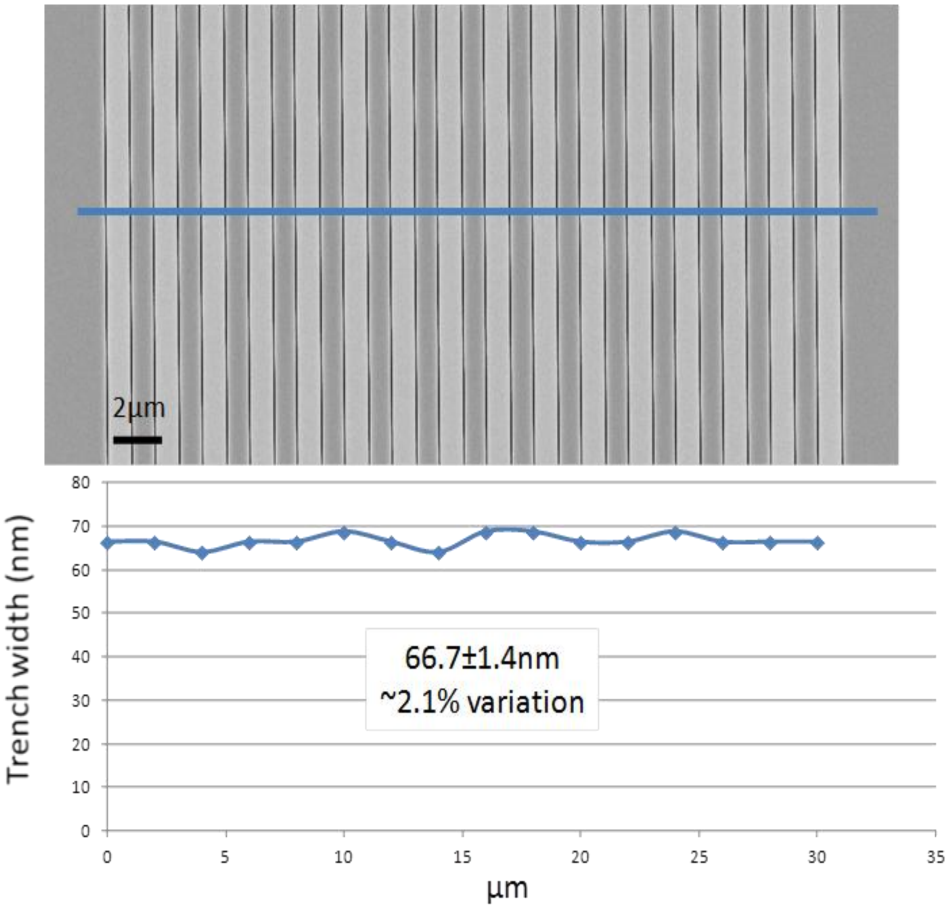

Figure 5.27 Width uniformity along an array of nanotrenches.

It turns out that the polymer residue layer is physically quite tough to withstand a relatively long time during TMAH etching. Figure 5.28 shows that the polymer mask protects the Si underneath well when the nanotrenches are etched to about 2µm deep. The aspect ratios (ARs) for the trenches showing in Figure 5.28(a) and (b) are about 20 and 15 respectively.

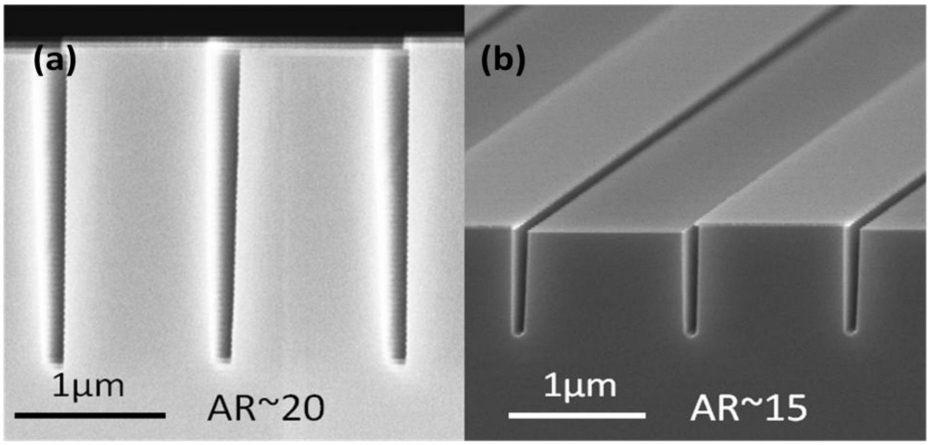

Figure 5.28 (a) Cross-sectional view of nanotrenches with AR~20; (b) Side view of nanotrenches with AR~15 (tilt = 45°).

5.4.4 Potential Applications

The motivation of the nanotrench fabrication is to provide ideal structures for Cu deposition and facilitate proper measurement of Cu line properties. However, the nanotrenches fabricated by the newly developed SSM technique open up possibilities for other potential applications. These applications are briefly discussed below.

One interesting area is nanofluidics. When contacted with an aqueous solution, the surfaces of most solids gain a net (either positive or negative) charge density due to chemical reactions such as protonation or deprotonation, adsorption, or defects [Abgrall *et al.*, 2008, Kirby *et al.*, 2004]. As shown in Figure 5.29(a), the charge is screened in the solution by the so called electrical double layer: a layer of adsorbed ions (Stern layer), and a mobile layer (diffuse layer). The screen length is called the Debye length λ_d. λ_d is typically of the order of 1-100nm which is the width range of the nanotrenches fabricated by SSM. Meanwhile, as shown in Figure 5.29 (b), many bio-molecules are also in the same size range. The comparability of the size range opens up opportunities for nanoscale fluidic transport studies [Schoch *et al.*, 2008] and energy conversions [Daiguji *et al.*, 2004, Liu *et al.*, 2005, Author, 2007, Yang *et al.*, 2003]. It also provides tools for manipulating small molecules [Karnik *et al.*, 2005] and nanoparticles [Abgrall *et al.*, 2008], as well as devices for bio-analysis [Liang *et al.*, 2008, Tegenfeldt *et al.*, 2004], separations [Han *et al.*, 2000] and drug delivery [Sinha *et al.*, 2004], etc..

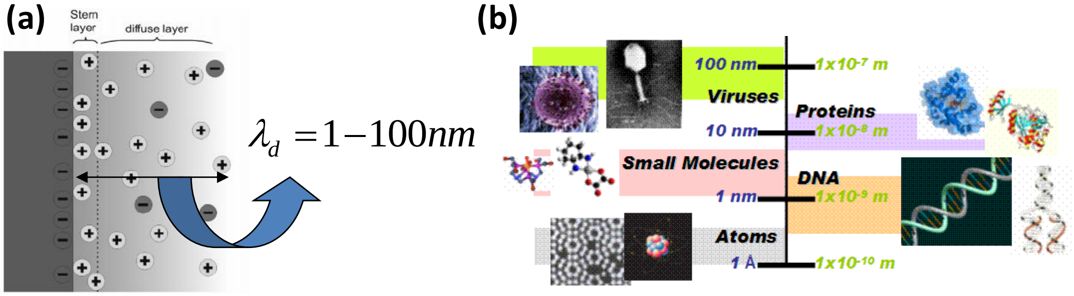
(a)
Stern layer
diffuse layer
$\lambda_d = 1-100nm$
(b)
100 nm
1x10-7 m
Viruses
Proteins
10 nm
1x10-8 m
Small Molecules
DNA
1 nm
1x10-9 m
Atoms
1 A
1x10-10 m

Figure 5.29 (a) Schematic of the electrical double layer at solid/liquid interface [Abgrall *et al.*, 2008]; (b) Size range of bio-molecules.

The nanotrenches need to be sealed to form nanochannels for nanofluidic applications. The sealing can be performed by a plasma-enhanced chemical vapor deposition (PECVD) of SiO_2, as shown in Figure 30.

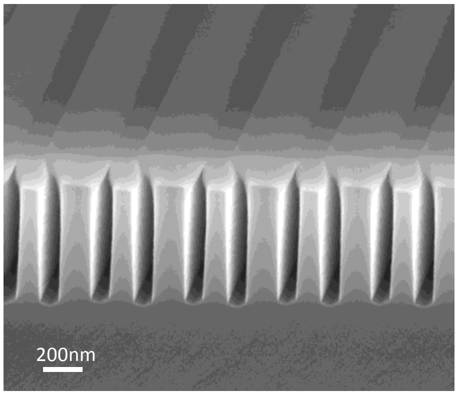

Figure 5.30 Nanotrenches sealed by PECVD SiO_2 to form nanochannels.

As a demonstration, an array of 20 nanochannles with 60nm width and 5µm spacing was fabricated. A solution of bio-molecules labeled with fluorescein flowed through the nanochannel array. Fluorescence microscopy images taken are shown in Figure 5.31. It clearly demonstrates that all the 20 nanochannels are flow-through channels. The solution used was 0.5 mM Biotin-4-fluoroscein, 50 mM Tris-HCl with pH 7.5 and 5 mM EDTA.

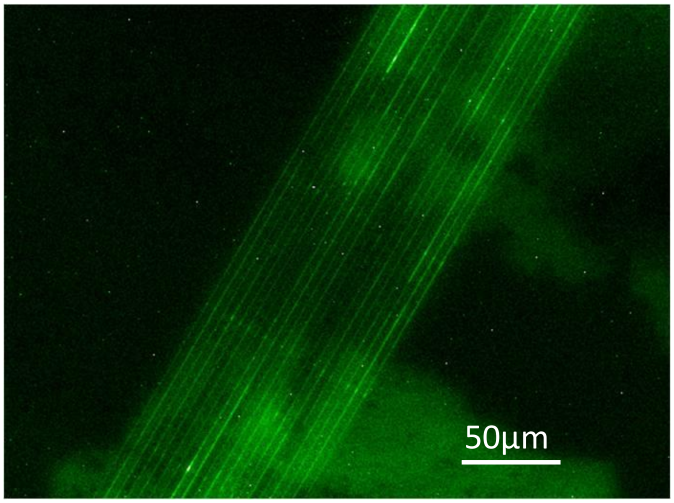

Figure 5.31 Fluorescence microscopy image of nanochannels flowed with solutions.

The Si nanochannels fabricated in this study have atomically smooth sidewalls, which cannot be achieved by other fabrication methods [Perry *et al.*, 2006, Martin *et al.*, 2005, Xia *et al.*, 2008, Tas *et al.*, 2002]. This not only provides uniform surface properties, but also decreases the friction of inner surface of the nanochannels. The latter advantage is important to reduce the adsorption of molecules to the channel walls, thus, reduce the chance for channel clogging, the biggest challenge for nanofluidic applications.

Another critical challenge in developing many innovative nanofluidic devices is to fabricate nanochannels that are narrow in width but long in length. For example, DNA, the most important bio-molecule, has width in nanoscale but length in macroscale (centimeters). To use nanochannels for DNA sequencing, it requires long continuous nanochannels to stretch and stabilize the DNAs. Otherwise, the random motion of the parts of the DNAs outside the nanochannels would result in severe noise. However, the length of nanotrenches defined by direct writing of nanoscale lithography tools is limited by their writing field (about 100µm). For example, the JOEL EBL system employed in this study has a writing field of 80µm. The stitching error between two writing fields would make it difficult to pattern long continuous nanotrenches. With the SSM technique, the nanotrenches are obtained from trenches patterned with relatively larger width. It can overcome the writing field limit. Figure 5.32 shows four arrays of 40nm wide and 9-cm long nanotrenches fabricated in a 4-inch wafer. The ratio between the length and width is $2.2*10^6$. To the best of the author's knowledge, they are the longest Si nanotrenches in the world. Note that, the capability to fabricate arrays of nanochannels with uniform properties is also of great importance to increase the throughput of the device. This is also a key advantage of SSM method.

SSM does not require nanoscale patterning to obtain nanotrenches. Therefore, a conventional optical lithography system with resolution at microns can be used. However, the AWE requires alignment of the trench with <112> direction. The LER induced by low resolution optical lithography may disable the localized pattern to meet the direction alignment requirement. To overcome this issue, an AWE in TMAH can be performed to expose the smooth sidewalls and eliminate the LER. Then an oxidization and SiO_2 RIE can be employed to form the SSMs, followed by another AWE to obtain Si nanotrenches along the sidewalls of the microtrenches, as shown in Figure 5.33. Si nanotrenches with 60nm width were fabricated by using this approach.

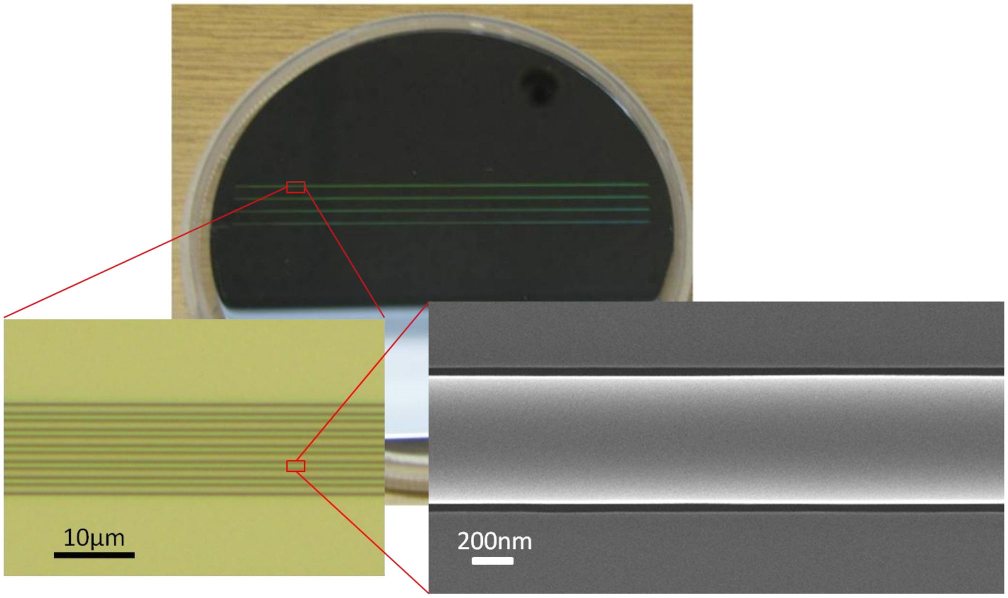

Figure 5.32 Arrays of ultra-long (9cm) nanotrenches.

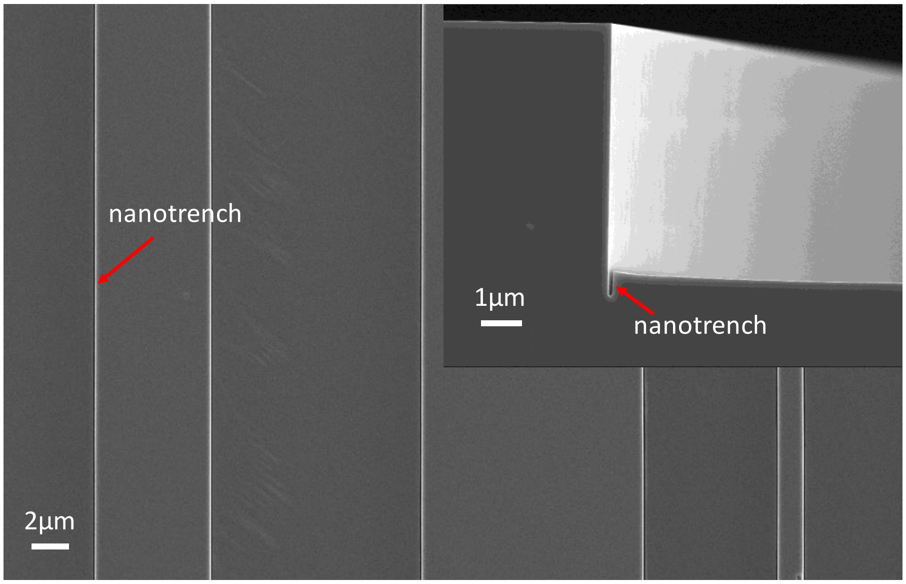
nanotrench
1µm
nanotrench
2µm

Figure 5.33 Nanotrenches fabricated by using a conventional optical lithography. The inset is a cross-sectional view.

5.5 CONCLUSIONS

Motivated by bridging the gap between modeling studies and realistic Cu interconnect structures, this chapter investigated the methods of making Si nanostructures with high qualities. AWE of Si was used to achieve rectangular profiles and smooth sidewalls on (110) Si wafers. With the EBL and crystalline direction alignment, Si nanolines with the width down to 20nm range and AR as high as 40 was fabricated. The same approach was also used to fabricate Si nanotrenches with the width down to 90nm range. Contact pads were also integrated with the nanotrenches. Cu was deposited into the trenches and the Ohmic electrical behavior of the Cu line was measured.

To overcome the trench widening effect during etching, an SSM technique was developed to fabricate ultra-narrow nanotrenches. The method uses the polymer residue formed during SiO_2 RIE in fluorocarbon plasma as an etch mask for Si AWE. Similar to the well-known microtrenching effect in RIE, the area near the edges of a pre-defined trench bottom receives more ion bombardment compared to the center of the trench bottom. It removes more polymers near the edges as well. The subsequent AWE of Si in TMAH only etches the Si close to the edges, leaving the Si underneath the polymer at the center of the trench bottom intact. This forms two nanotrenches along the two edges of the pre-defined trench. Nanotrenches with width down to 20nm range and AR as high as 20 were fabricated with the SSM technique. The width is uniform along both a single trench and an array of trenches. The world's longest (9cm) Si nanotrenches were fabricated with this method overcoming the writing field limitation of EBL. Nanochannels were formed by sealing the nanotrenches with PECVD SiO_2. Their potential applications in nanofluidics were discussed.

Chapter 6: Conclusions and Suggestions for Future Work

6.1 CONCLUSIONS

Although EM reliability has been widely investigated for many years, the continuing scaling poses new challenges to reliability concern in Cu interconnects. New methods were developed in this dissertation to study and understand Cu EM. This includes investigating EM-induced initial void growth by resistance traces analysis, modeling void growth in Cu interconnects, and studying the scaling effect on EM driving force. A method was also developed in the dissertation to produce ideal Si nanotrenches for deposition of Cu nanolines.

Chapter 2 studied the EM-induced void formation mechanism in Cu interconnects. A method to derive the initial void growth rate at Stage I by analyzing the EM resistance traces was developed. The method compares the calculated failure time t_{f_calc} based on R_{step} and R_{slope} with the measured failure time t_f to obtain the difference between the void growth rate at Stage I and Stage III. EM tests were performed on the multi-link structures to statistically vary the failure time, R_{step} and R_{slope}. Failure analysis and R_{step} values both showed that the lines are failed by trench type voids. The plot of t_{f_calc} versus t_f shows a linear curve with slope 0.4 and intercepts with t_f axis, indicating that the void growth rate at Stage I is smaller than at Stage III.

Chapter 3 modeled the initial void growth induced by EM in Cu interconnects. The model extends the Korhonen model which was applicable only to Stage III. The approach taken is to divide the Cu line into two regions based on the void segment and calculate the stress evolution in the two regions separately. Analytical solutions for the void growth rates at Stage I and Stage III were obtained. The modeled void growth rate depends on the initial thermal stress in the Cu line. By imposing a compressive thermal stress, which is probable for Cu interconnect line at EM test temperature, the model generates failure time in good agreement with the experimental data shown in Chapter 2.

In Chapter 3, grain growth simulations based on Potts model were also performed considering interconnect structures with overburdens. Both normal grain growth from the bulk and abnormal grain growth from the surface and interfaces were included in the simulations. The grain growth from sidewalls was found to be dominant, especially for decreasing line width. This is because of the relatively high aspect ratio of a Cu interconnect line and the increased surface to volume ratio when line width scales down. This leads to small grains in the trench bottom, in agreement with experimental observations. The simulated grain structure is used as input of material properties to support the void growth modeling.

Chapter 4 studied the size effect on the electron wind force for a thin film and a rectangular line with dimensions comparable to the electron mean free path in Cu (39nm at room temperature). The problem was modeled by considering the momentum transfer between electrons and a defect atom at the top interface. The result shows that the scaling effect on the effective charge number Z^* can be represented by a size factor S depending on the film/line dimensions. The confinement by the film/line boundaries not only reduces the electrical conductivity, but also affects the effective charge Z^*e. The effective charge for a 20nm wide line is reduced by 60%. In contrast, the electron wind force in a nanoscale line is slightly enhanced. From the study in this chapter, one additional scaling factor for EM in Cu interconnects, the size effect on EM driving force, was discovered.

Chapter 5 described the methods for fabricating high quality Si nanotrenches for bridging the gap between modeling studies and realistic Cu interconnect structures. With EBL and AWE on (110) Si wafer, 90nm wide Si nanotrenches with rectangular profiles and smooth sidewalls were fabricated. Contact pads were also integrated with the nanotrenches for electrical measurements of Cu lines. To overcome the trench widening effect during etching, an SSM technique was developed. This method uses the polymer residue formed during SiO_2 RIE in fluorocarbon plasma as a self-aligned etching mask to protect the Si at the center of the pre-defined trench in AWE. Nanotrenches with width down to 20nm range and AR as high as 20 have been fabricated with the SSM technique. The width along the trenches was uniform for single trenches and an array of trenches. Potential applications of the Si nanotrenches in nanofluidics were discussed.

6.2 SUGGESTIONS FOR FUTURE WORK

In Chapter 2, EM tests were performed on multi-link structures with link number N = 2, 10, 100. When the link number is high, the extraction of R_{step} and R_{slope} becomes more difficult, as described in Section 2.4.1. So samples with relatively smaller link number such as N = 1, 2, 4, 8 would be more suitable for such study. The R_{step} and R_{slope} statistics should be less subjected to noise from the test environment. Especially, the single link, as the base structure, can provide more information. It is also interesting to study the transition of statistics from N =1 to N = 2.

All the samples in this study were under the same stressing conditions. The void growth kinetics at different stress conditions remain to be studied. One recommendation is to test samples at different temperatures. The thermal stress of the Cu lines is expected to change with temperature. According to the stress model in Chapter 3, the void growth rate difference between Stage I and Stage III depends on thermal stress. Therefore tests at different temperatures can provide data to further verify the stress effect in the model. Another stressing condition that can be changed is current density, which in itself can influence the failure time and resistance parameters. But one should be aware of the possibility of encountering different failure modes under different current densities.

Both the method for resistance trace analysis and the void growth model developed assumed a rectangular void shape for simplicity. In experiments, wedge shaped voids are more often observed. Analysis and model based on such void shape should be further developed, since it comes closer to a realistic case.

The EM samples used in this study are fabricated with a standard SiCN cap. As scaling continues, new materials such as metal cap and seed layer doping are introduced in Cu interconnects. These new materials can affect the diffusion paths and void kinetics. It will be interesting and useful to apply the method based on resistance traces analysis to Cu interconnects with those new materials. Especially interesting would be the Cu interconnect with Mn doping, which is the metallization of choice for future technology nodes. Such studies may extract important information about potential incubation time for dopants.

For the grain growth simulations in Chapter 3, a simplified surface and interface energy assumption was used: one high energy and one low energy. It may be more realistic to assume a distribution of energy. Although not included in the dissertation, the author has performed some simulations of the effects of surface passivation and Ru seed layer to the grain growth. It is a direction worth further studies. And since Mn doping is promising, another important direction is to study the effects of Mn (diffusing and pinning) to Cu grain growth.

In Chapter 4, the size effect on electron wind force was calculated for a long line to avoid the complication of potential short length effect. However, in Cu EM, the void usually grows close to the cathode end of the line. This makes the calculation of electron wind force for an atom at the end of a line important. Furthermore, the defect atom was placed at the Cu/cap interface in this dissertation. When the line width scales down below 90nm, small polycrystalline grains are frequently observed. The grain boundaries provide additional diffusion paths which are not negligible compared to interface diffusion. So it will be important to study whether the size effect on electron wind force for atoms within a line and/or at a grain boundary will become more significant.

The Si nanotrenches fabricated in Chapter 5 can be filled with Cu and used to perform mechanical tests, such as nanoindentation, of Cu lines. A more interesting study will be electrical measurements on well-defined ultra-narrow Cu lines. But before that, processes to integrate contact pads with the SSM technique have to be developed, which inevitably requires also process development of Cu plating and Cu CMP. If successful, both mechanical and electrical measurements could be performed on a single line to study possible correlation between them. Other applications of these nanotrenches include nanofluidics, sensors etc., all of which are worth exploring as well, if resources are available.

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