Heterogeneous Devices and Circuits Based on 2D Semiconductors

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Dedication

This dissertation is dedicated to my family.

Abstract

Two-dimensional (2D) semiconductors have been attracting interest for numerous device applications due to their layered crystal structure which allows great thickness scalability down to monolayer and ease of integration onto arbitrary substrates. A multitude of electronic properties of different 2D materials also enables the development of transistors with high-performance and high on/off ratio. Based on previous research, 2D materials can be used to create n-type or p-type MOS transistors without adding dopants. Thus, highly staggered gap heterostructures and integrated CMOS circuits can be realized by combining two different 2D semiconductors. Moreover, given the unique properties distinct from traditional 3D materials, the radiation effect on these materials are worth being studied in order to investigate the suitability as a counterpart of silicon in extreme conditions. In this dissertation, models, design, fabrication, and characterization of devices and circuits built with heterogeneous materials and structures are developed and presented.

Firstly, a general background of 2D materials is introduced, including the history, atomic structure and fabrication technique. The miscellaneous electronic properties of materials are compared and the resulting applications are reviewed leading to the motivation of this dissertation. Secondly the local backgate structure for fabricating 2D MOSFETs is discussed including the fabrication process and the device characteristics. The device performance and radiation tolerance are shown. Thirdly, the fabrication of logic and memory circuits based on heterogeneous 2D materials is introduced, while the DC and AC measurements are reviewed. Fourthly, the $MoTe_2/SnSe_2$ heterostructure is

reviewed along with the characterization of each material. A novel direct synthesized technique for lateral heterostructure is shown. Finally our work is summarized, and future developments are proposed for inspiration.

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CHAPTER 1   INTRODUCTION

In this chapter, an overview of various kinds of 2D materials is provided given their rising significance in post-CMOS device applications due to their scalability down to angstrom level and ease of integration onto arbitrary surfaces. A brief history of these emerging materials is reviewed first followed by the atomic structure of different materials and the fabrication method for them. Secondly, the unique feature of 2D materials, the thickness dependent electronic properties is discussed to show the advantage of them over traditional materials. Next, some possible applications of 2D materials are introduced to emphasize the promising role of them in modern electronics. Finally, an overview of the remainder of this dissertation is also outlined at the end of this chapter.

1.1   Two-dimensional materials

1.1.1   History of 2D materials

Graphene, which is one-atom thick, two-dimensional crystal consisting of carbon atom sheets, was argued to not exist because it was believed that free standing strictly 2D materials are thermodynamically unstable [1, 2]. Nevertheless, graphene was still of interest to researchers for studying the properties of various carbon allotropes since sixty years ago [3, 4]. In 1984, graphene was predicted to have the capacity for current transport with massless charge carriers theoretically [5] when it was brought to attention in the field of electronics. Three years later, graphene was named to distinguish from three-dimensional graphite [6]. Although curved graphene structures such as fullerene or carbon nanotube had previously been experimentally demonstrated, 2D graphene was

only recognized as an integral part of larger 3D structures until it was successfully isolated from graphite by Geim and Novoselov in 2004 [7]. In their work, commercial household tape was used to peel thin flakes from bulk graphite, the thinnest of which are recognized as monolayer graphene. This work dispelled the long-held conventional wisdom and won them the Nobel Prize in physics in 2010. This discovery has led the research of materials into a new era of emerging 2D materials and the excellent electrical, thermal, mechanical, electronic, and optical properties have resulted in a continuously growing market of graphene.

Despite the fact of graphene being a novel highly conductive material, one drawback has limited the use of it in semiconductor technology, the absence of band gap in pristine graphene. Patterning graphene into nanoribbons could create an energy gap up to 400 meV due to quantum-mechanical confinement, but the price such as significant mobility reduction [8, 9] or increased off-state currents resulted from edge roughness is undesirable [10]. In order to be an eligible counterpart of silicon in post-CMOS technology, the capability to switch off sharply is required to suppress the static power dissipation. Quantitatively speaking, an on-to-off ratio between 10^4 and 10^7 is desired, where an energy gap more than 400 meV is preferred [11]. Thus, semiconducting analogues of graphene, transition metal dichalcogenides (TMDs) have drawn great attention because of their finite gap in two-dimensional form. In fact, effort to thin MoS_2, which was previously used as dry lubricant, to a few layers has been made since over fifty years ago [12, 13]. However, the significance of TMDs as semiconductors was not rediscovered until the novel transport properties of strict 2D graphene were

experimentally studied [7]. In the year of 2010, monolayer MoS_2 was first applied in transistors and demonstrated on-to-off ratio comparable to silicon metal–oxide–semiconductor field-effect transistors (MOSFETs), which sparked an explosion in active research in various semiconducting 2D chalcogenides, including and not limited to MoS_2, $MoTe_2$, WS_2, $SnSe_2$ and h-BN.

Black phosphorus (BP), a layered semiconductor consisting of phosphorene, is formed the same way as graphite with van der Waals force, and that is why phosphorene was named. The discovery of BP can be traced back to a century ago when it was first transitioned from white phosphorus [14]. The transition of large crystal of black phosphorus from red phosphorus was published in 1981 [15]. Same as TMDs, the thickness dependent physical properties and the demonstration of monolayer have brought this material back to the public attention. In 2014, few-layer black phosphorus was adopted in field-effect transistor study and proved capability in future nanoelectronic and optoelectronic applications [16]. At the moment, many properties of 2D materials are yet to be discovered and the interest in 2D materials of researchers and semiconductor industries still keeps growing and thriving.

1.1.2 Atomic structure of 2D materials

Monolayer graphene, which is a purely 2D material, consists of carbon atoms arranged in a honeycomb lattice due to the sp^2 hybridization. The hybridization introduces three orbitals which are oriented in the *xy*-plane and have mutual angles of 120°. The $2p_z$ orbital, perpendicular to the *xy*-plane, remains unhybridized. The three in-plane orbitals cause the carbon atoms to form a honeycomb structure, which can be

viewed as tiling of benzene hexagons with hydrogen atoms replaced by adjacent hexagons and the π electrons delocalized. In this structure, each carbon atom is neighbored by three carbon atoms, separated by a = 1.42 Å and forming σ-bonds. Thanks to the strong enough σ-bonds, the stability against thermal fluctuations allows free-standing monolayer to exist.

The honeycomb lattice of graphene in *xy*-plane is shown in Fig. 1-1 where *x*-axis represents the armchair (AC) direction and *y*-axis represents the zigzag (ZZ) direction. The honeycomb lattice itself is not a Bravais lattice and the Bravais lattice of graphene is a hexagonal lattice instead. This is because the red sites and the green sites, although all represent carbon atoms, are not equivalent. However, both green and red sub-lattices are triangular Bravais lattices with the magnitude of lattice vector being $\sqrt{3}a = 2.42$ Å. The unit cell, indicating in blue dashed rhombus in Fig. 1-1, is on a two-atom basis.
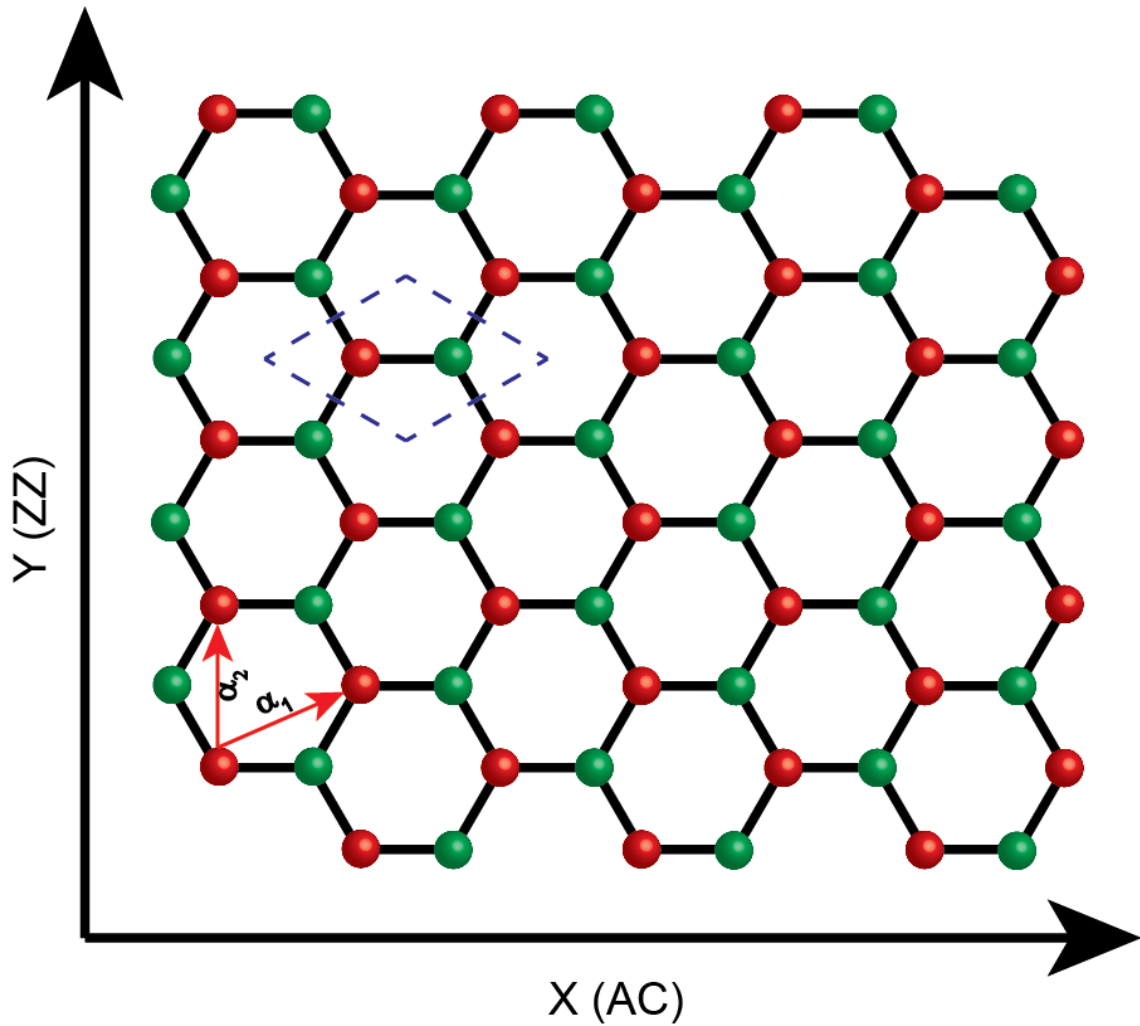
Figure 1-1 Atomic lattice structure of graphene. The green sites and red sites are carbon atoms forming different triangular Bravais lattices whose basis vectors are α_1 and α_2. Blue dashed rhombus stands for the two-atom unit cell of graphene.

Metal dichalcogenides constitute a major class of 2D materials with the formula MX_2, where M stands for a metallic element and X is a chalcogen. Similar to their analogue graphene, MX_2 are also formed in a layer by layer basis but each monolayer is not as strictly 2D as graphene. In each layer, one sheet of metal array is sandwiched between two chalcogen sheets. While the sheets with in each layer are held together with

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strong covalent bonds, the interaction between each layer is held loosely by weak van der Waals force, just like graphene. Due to different stacking orders or metal atom coordination, the bulk MX_2 materials can be formed in various polytypes, as shown in Fig. 1-2. The metal atoms have trigonal prismatic or octahedral coordination and the overall symmetry can be hexagonal or rhombohedral. In either coordination or symmetry, each metal atom is always bonded with six chalcogen atoms. In trigonal prismatic structure, one sheet of chalcogen is stacked right on top of the other, forming trigonal interstices for metal atoms. In octahedral structure, chalcogen planes are slightly disoriented, forming octahedral interstices for metal atoms.

The schematic of 2H, 1T and 3R polytypes are shown in Fig. 1-2 by column, where the letter H, T, R denote the hexagonal, trigonal prismatic and rhombohedral symmetries, and the numbers indicate the number of layers per repeating unit. The top row of Fig. 1-2 shows the side view of unit cell for different polytypes, and the number of metal atoms and chalcogen atoms composing the unit cell are depended on the symmetry type. The middle row of Fig. 1-2 renders the top view of each polytype, with the unit cell represented by black rhombus and lattice vectors by α_1 and α_2. Stacking sequences are shown in the bottom row of Fig. 1-2 where the lattice constant a, varies from 3.1 Å to 3.6 Å for different materials, and the layers are separated by a distance of ~6.5 Å [17, 18, 19, 20, 21, 22, 12], showing surprisingly consistency for this class of materials.
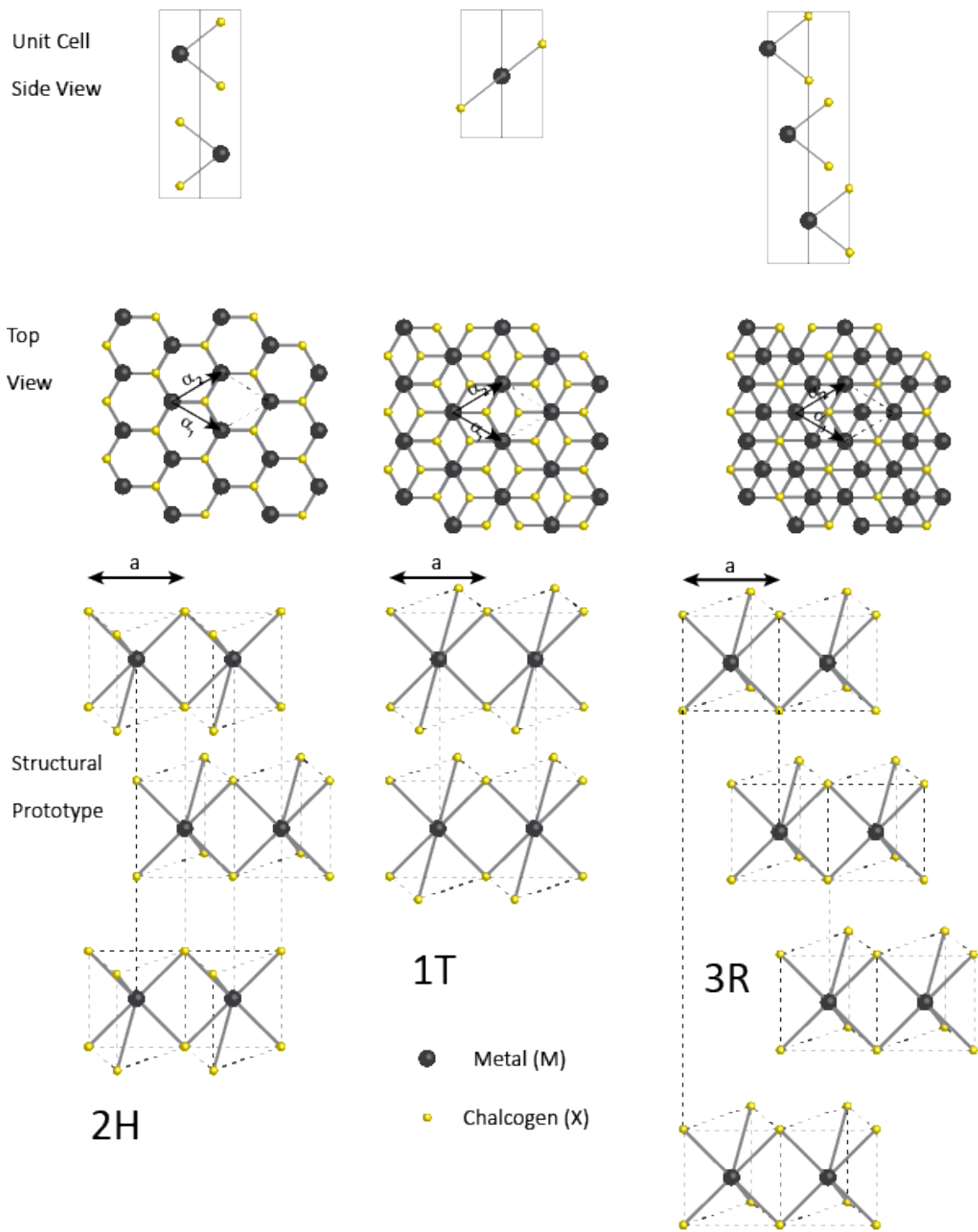
Figure 1-2 Atomic structures of TMDs. Yellow sites stand for chalcogen atoms and grey sites stand for metal atoms.

Unlike graphene or TMDs, though also forming a honeycomb structure, black phosphorus is unique among the 2D family because the structure is anisotropic. In a monolayer of black phosphorus, each phosphorus atom has three adjacent phosphorus atoms which are covalently bonded by sp^3 hybridization. Thus, three valence electrons are occupied to form a puckered honeycomb structure. The atomic structure of black phosphorus is shown in Fig. 1-3, where Fig. 1-3 (a) illustrates the unit cell, consisting of two layers and eight atoms. The lattice is repeating every two layers with each layer shifted from the adjacent layer by half a unit. Inside a monolayer, the phosphorus atoms form two planes and two perpendicular directions, the armchair (AC) and zigzag (ZZ). Fig. 1-3 (b) is a side view of black phosphorus bilayer along the armchair direction in which the bottom layer is separated from the top layer by 5.3 Å. The distance between the nearest atoms in the same atomic plane is 2.222 Å and the bond length between atoms from different atomic planes is 2.277 Å derived from the 3p orbitals of phosphorus [23]. The top view of bulk black phosphorus is shown in Fig. 1-3 (c).

(a)

(b)

2.224Å

2.244Å

~5.3Å

Interlayer(Z)

Armchair (X)

(c)

Armchair (Y)

Zigzag (X)
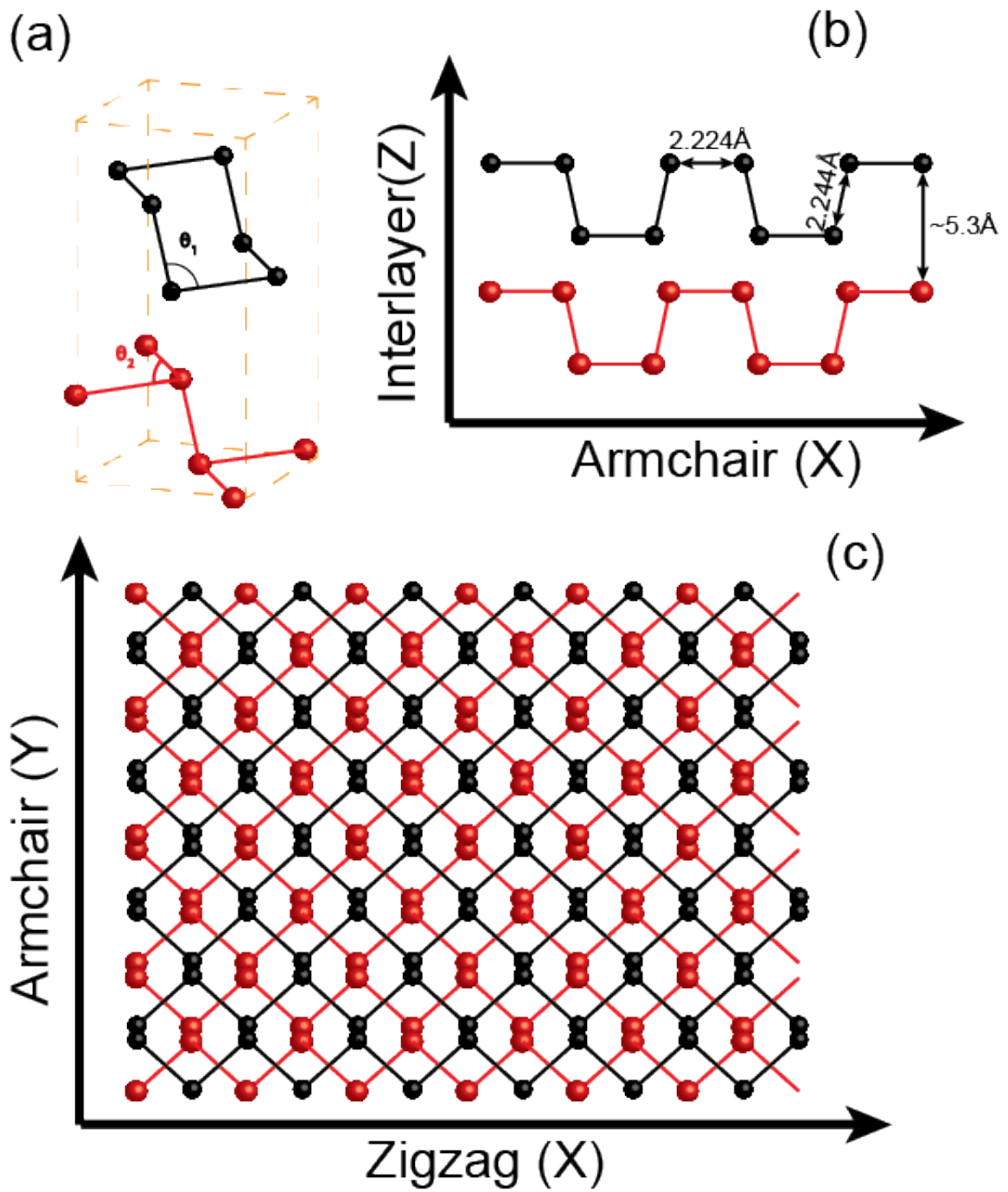
Figure 1-3 Atomic structure of black phosphorus. (a) Unit cell of black phosphorus. θ_1 is equal to 101.9° and θ_2 is 96.5° [23]. (b) Side view of bilayer black phosphorus. (c) Top view of bulk black phosphorus.

1.1.3 Fabrication of 2D material thin films

The first successful attempt to obtain monolayer 2D material was the isolation of graphene from bulk graphite using micromechanical cleavage [7, 24]. This technique is still used by research groups due to the ease, low cost and high quality of film. The size of the graphene flakes produced can reach up to 100 μm which is sufficient for most researches. This technique used is either rubbing the bulk crystal against a solid and visible surface [24] or using adhesive tapes to repeatedly peeling off the bulk crystal until monolayers are acquired [7]. The technique sounds no more sophisticated than just drawing a chalk on a board but there are some features of monolayer graphene produced that prevents it to be discovered earlier. First, isolated few-layer graphene is extremely rare on the substrate and usually hidden in or accompanied by bulk flakes. Secondly, the absence of clear signature for the number of layers under scanning electron microscopy (SEM) invalidates the inspection with SEMs. Thirdly, scanning probe microscopy (SPM) has a notoriously low throughput, which makes this effective method unrealistic. Lastly, monolayers are completely transparent to visible light and cannot be searched with optical microscope on most substrates. The critical breakthrough for finding graphene is the discovery that with a carefully chosen thickness of SiO_2 on top of Si wafer as the substrate, thanks to a weak interference-like contrast to empty wafer, monolayer can be visible in optical microscope. Raman microscopy could be used to confirm the thickness after searching by eyes since it is found that the number of graphene has a clear signature in Raman [25]. Despite the fact that the process need to be very carefully manipulated and great patience is needed for searching monolayers under microscope, this technique

is still favorable to the research of 2D materials, especially beyond graphene, owing to the absence of effective way to fabricate large area monolayers.

Another approach to prepare large scale graphene involves thermal decomposition of silicon carbide (SiC) to produce "epitaxial" graphene on top of SiC wafers [26]. The idea is to evaporate the Si atoms, which are more weakly bonded from the surface, by heating the epitaxial hexagonal SiC wafer to a temperature of ~1300 °C. Thus, via graphitization, the remaining carbon atoms form a graphic layer on the surface whose physical properties depend on the chosen surface of SiC. For the Si terminated (0001) surface, the graphitization process is slow and the electron mobility is also low. For the C terminated surface $(000\bar{1})$, the rate of the graphitization process is high and so is the carrier mobility. Therefore, it is difficult to achieve the high transport performance and good controllability simultaneously. Along with the fact that instead of forming a thin sheet of graphite, independent graphene layers stacked with a rotational disorder are produced, confirmed by X-ray diffraction measurements [27], this method is not preferable.

Chemical vapor deposition of graphene on top of metal substrates is a promising way for producing large-area high quality graphene. Among various materials, Ni [28] and Cu [29] are most popular for the growth. Growth on copper is selected in our laboratory over nickel because the product on copper is mostly monolayer graphene with a small portion of bi- or few layers. In comparison, the number of layers for graphene growth on nickel is various. The main reason of this difference is the low solubility of carbon in copper which causes the process to be self-limiting after a monolayer of

graphene is formed on the surface. In our laboratory, the process is done in a quartz tube with high temperature and well controlled gas flow and pressure. During the process, argon, hydrogen (H_2) and methane (CH_4) are used where Ar is used as purging gas and CH_4 is reduced to graphene by H_2 with metal as the catalyst. After cooling down to room temperature, single layer graphene on the surface of copper is available for transfer onto arbitrary substrates.

The study of TMD fabrication is very similar to that of graphene, as the preparation technique can be classified into top-down from bulk material and bottom-up synthesis methods. At the moment, physical preparation, or micromechanical cleavage is still the dominant or the only way to obtain single-grain thin flakes of TMDs for research purpose due to the cost and feasibility with mass production technique under research.

Most TMDs can be exfoliated from the bulk crystal using adhesive tape, transferred on to target substrates, identified by optical interference and confirmed by SPM. This technique is same as how graphene was first discovered. Same as graphene, the low throughput and lack of controllability make it unappealing. Liquid exfoliation then regained research interest as this method could be used for mass production of thin layer TMDs. MoS_2 monolayers have been produced by intercalation with lithium followed by reaction with water in as early as 1986 [13]. In this method, 2H MoS_2 power was first soaked in the solution of lithium-based compound, n-butyl lithium, in hexane for two days to be intercalated with lithium. Upon washing in hexane and drying, the MoS_2 was immersed in water to allow reaction. The hydrogen gas generated from the reaction of lithium and water rapidly separates the layers of MoS_2 along with sonication.

After being applied to a substrate and drying, randomly stacked monolayers were acquired. This method is also demonstrated for the preparation of $MoSe_2$, WS_2 and SnS_2. An alternative electrochemical lithiation process was also reported with higher yield and controllability [30]. In this method, layered bulk material is incorporated in a test cell as cathode where lithium foil works as anode to provide lithium ions. The following steps involve the exfoliation of intercalated bulk crystal in water by sonication as before.

Given the reactivity of lithium in ambient atmosphere which causes it to require an inert gas environment to carry out the lithiation and the increasing price of lithium, researchers have come up with the exfoliation of layered material in appropriate liquids [31]. The process starts with the sonication of TMD powders in chosen solvents followed by centrifuging the resultant and decanting the supernatant. Typical exfoliated flakes are a few hundred nanometers wide and a few layers thick. MoS_2, WS_2, $MoSe_2$, $MoTe_2$, $TaSe_2$, $NbSe_2$, $NiTe_2$, BN, and Bi_2Te_3 crystals have been exfoliated in to flakes with this technique.

Despite their extensive use in academic research, they still suffer from the drawback of low yield and lack of uniformity. To support wafer-scale electronics and photonics fabrication, bottom-up synthesis, similar to graphene, is under development. Chemical vapor deposition (CVD) synthesis, as a promising way to produce large scale TMD thin films, has two major routes developed to date. Taking MoS_2 as an example, the first one can be classified as a two-step growth route, where a pre-deposited Mo-based precursor is sulfurized or decomposed into MoS_2 in a CVD chamber. Various Mo precursors can be chosen and the results show great variance. Evaporated Mo thin layer

was applied by Zhan et al, which was reacted with sulfur at 750 °C [32] to form thin MoS_2 films. However, owing to the suppressed migration of Mo atoms on the substrate resulted from the high melting point of Mo, polycrystalline MoS_2 with disordered domains were formed, which degrade the mobility. Thus, lower evaporation point Mo precursor, such as molybdenum oxide, was introduced [33, 34], where sulfur vapor was used for sulfurization. The grain size and carrier mobility were effectively improved in their work. Also, precursor containing both Mo and S atoms can be used for decomposing into MoS_2, for example, ammonium thiomolybdate $((NH_4)_2MoS_4)$. The substrate was first coated with $((NH_4)_2MoS_4$ solution, and then annealed at high temperature in a sulfur-rich environment. Although these methods are proved effective for fabricating large area MoS_2 films, the thickness uniformity has yet to be improved, mostly due to the uncontrollability and the low fluidity of the metal precursor. So is the grain size.

Another route, where the gaseous phase metal and chalcogen precursors are introduced and reacted simultaneously, was introduced to effectively produce TMD monolayers [35, 36, 37, 38]. In their work [35, 36, 37, 38], both powder precursors, namely MoO_3 and sulfur, were placed successively in the growth chamber with the substrate facing down. Volatile MoO_x reduced by sulfur and sulfur vapor react in the chamber and few layer MoS_2 (1-3 layers) with micro-meter level domain size could be deposited. This process has a greater potential to produce large-area MoS_2 films with uniform thickness and the domain size could be further improved if the substrate is carefully selected as single crystal with better matched lattice. To date, the CVD process

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has been demonstrated to be suitable for growing a number of TMDs, including but not limited to WS_2 [39], $MoSe_2$ [40], WSe_2 [41], $MoTe_2$ [42], $SnSe_2$ [43] and BP [44].

1.2 Electrical properties of 2D materials

Large-area graphene is a semi-metal with no band gap. The conduction band and valence band cross at the Dirac point, the K point of the Brillouin zone. The cone shaped bands can be expressed by the equation describing the electrons' linear dispersion relation:

$$E(k) = \hbar v_F \sqrt{\left(k_x^2 + k_y^2\right)},$$

(1.1)

where $\hbar$ is the reduced plank constant, v_F is the Fermi velocity in graphene, and k_x and k_y stand for the momentum in *x* and *y* direction. The band structure around the K point is shown in Fig. 1-4 (a). Bilayer graphene is also a gapless material where the low energy dispersion is quadratic rather than linear as in monolayers. The energy-momentum relationship is shown in Fig. 1-4 (b). The absence of gap is undesirable in device applications for the incapability to switch off. However, it is possible to modify the band structure and open a gap between the conduction and valence band by either confine the monolayer graphene into a nanoribbon [45] or by applying electric field to bilayer graphene [46]. The band structure near K point of each case is shown in Fig. 1-4 (c) and (d), respectively.
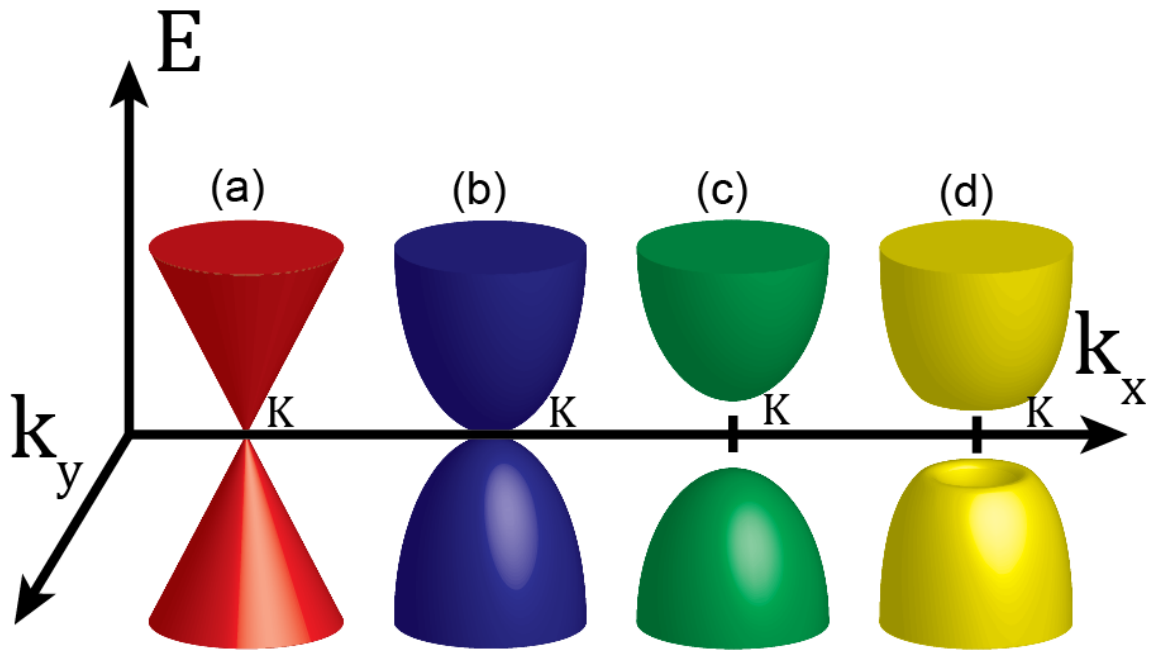
Figure 1-4 Band structures around K point of (a) monolayer graphene, (b) bilayer graphene, (c) graphene nanoribbon, (d) bilayer graphene with applied electric field.

Approximately, in graphene nanoribbons, the gap opened is inversely proportional to the width of the nanoribbon and can be up to hundreds of mili-electron volts. However, even in perfectly fabricated ribbons, the curvature around the conduction band minimum (CBM) and valence band maximum (VBM) decreased with the shrinking of the width. Thus, the carrier mobility is significantly degraded due to the increased carrier mass [47]. Perpendicular electric field was used to create a gap but a small gap of ~250 meV requires a large field (~3×10^7 V/cm) [46]. Strain could be a possible means to create a gap but the magnitude required (>20%) makes it impractical at this moment.

The most mentioned advantage of graphene is the high mobility at room temperature. The high mobility was predicted even before it was first isolated by

Novoselov, *et al*. [7] and mobility larger than 10,000 cm^2/Vs for graphene on SiO_2 substrate was reported in their work. Experimental results keep updating the record and mobilities greater than 100,000 cm^2/Vs are reported for CVD grown graphene [48]. However, the practical application of these high values of mobility needs careful inspection because mostly they are achieved with large area graphene. In graphene devices, reducing static power consumption by increasing energy gap is always at the cost of degrading mobilities.
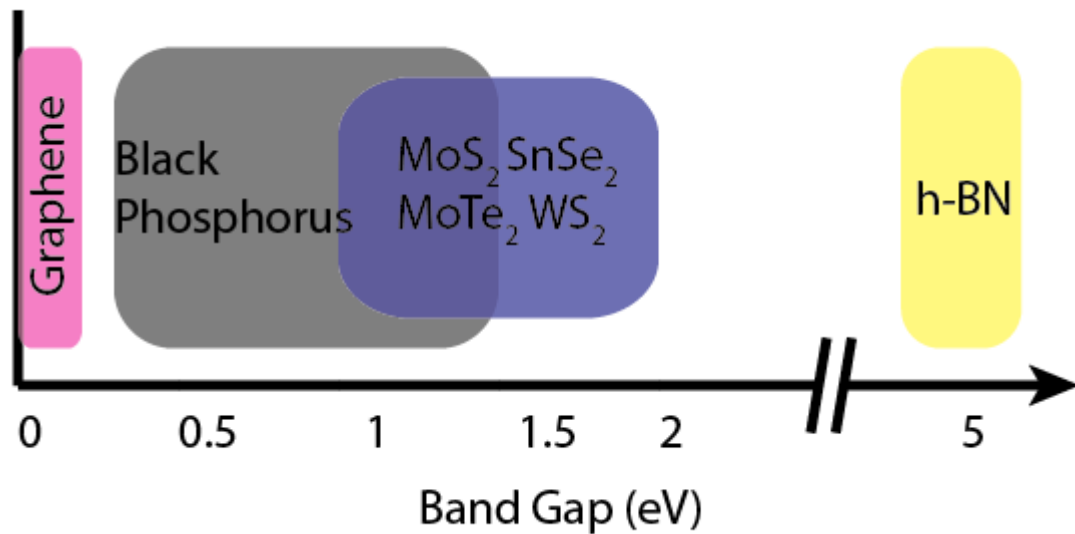
Figure 1-5 Illustration of band gaps of different 2D materials.

Therefore, semiconducting 2D materials with moderate mobilities are of interest to researchers. Fig. 1-5 shows the band gap information of different 2D materials. Typically, TMD semiconductors have a band gap between 1 and 2 eV, which should offer sufficient switching capability to the devices based on them.

MoS$_2$, taken as a benchmarking material in TMDs, is more thermodynamically favorable in the semiconducting 2H phase than the metallic 1T phase. Similar to graphene, the thickness difference between bulk and thin MoS$_2$ flakes can be detected by Raman spectroscopy. Thinner flakes exhibit closer E$_{2g}^1$ and A$_{1g}$ peaks while the spacing for bulk MoS$_2$ is 25 cm^{-1} compared to 19 cm^{-1} for monolayers [49]. A unique feature of MoS$_2$ represented TMDs is the tunable band structure based on number of layers. For bulk MoS$_2$, the indirect band gap is 1.2 eV with work function being 4.90 eV [50]. With decreasing number of layers, the CBM which sits between the the Γ point and K point and the VBM which is at the Γ point are brought closer by quantum confinement. Upon the transition from bilayer to monolayer the CBM and VBM have an abrupt shift to K point, making the material direct with a gap of 2.2 eV. Like graphene, the mobility of monolayer 2H MoS$_2$ is still being updated because it is limited by the interface between the crystal and the substrate the crystal is transferred onto. Mobility of 700 cm^2/Vs has been reported for exfoliated MoS$_2$ [51] and there is still room for improvement.

Being also a Mo chalcogenide, MoTe$_2$ is brought to researcher's attention for its novel properties such as the silicon-like gap and strong spin orbit coupling [52, 53]. These properties are fundamental for optoelectronic devices operating in the near infrared range and efficient spintronic and valleytronic devices. The direct gap of monolayer MoTe$_2$ is 1.1 eV with the gap of bulk MoTe$_2$ being 1.0 eV with the electron affinity being 4.1 eV [54, 55]. The number of layers can also be identified by Raman spectra since it has a clear signature of E$_{2g}^1$ and A$_{1g}$ peaks.

Unlike the Mo chalcogenides, which share close band gap properties, the difference between chalcogenides of Sn is distinct. Being also a layered material, SnS_2 has a relatively wide indirect gap of ~2.3 eV [56]. Yet while transitioning from indirect to direct gap material, the energy gap remains constant [57]. The band gap of $SnSe_2$ is much closer to other TMDs, which is 1.0 eV for the indirect gap [58] and 1.2 eV for the direct gap [59]. Even though the gap properties of the Sn chalcogenides are common in TMDs, they do have a special feature in their band structures, the high electron affinity. The electron affinity of SnS_2 is ~4.96 eV [60] and that of $SnSe_2$ is ~5.18 eV [58]. The large electron affinity makes the Sn chalcogenides uniquely suitable for some given applications. For instance, the electron affinity of ~5 eV is larger than the work function of many metals, and thus Ohmic contacts with negligible Schottky barrier can be formed between the metal and semiconductor. Moreover, the high affinity of Sn chalcogenides provides them the potential to form highly staggered gap or even broken gap when forming heterostructures with other low affinity materials, while the CBM of high affinity materials sits around the VBM of low affinity materials.

The metal chalcogenides typically have an energy gap > 1 eV, and so they are mostly used in applications requiring a silicon-like gap. However, in the case where a narrower gap is required, for example in photo devices, 2D materials are incapable before the discovery of BP filled the vacancy. As shown in Fig. 1-5, BP has a highly thickness-dependent energy gap which ranges from 0.3 eV to ~1.5 eV [61, 62, 63]. Unlike TMDs, which have direct band gaps only for single layers, BP is a direct material at the Γ point regardless the number of layers. Also, its energy gap value depends on the number of

layers and the gap narrows with increasing thickness, unlike TMDs whose gap values change abruptly only for monolayer. Another feature that distinguishes BP from other 2D materials is the high degree of in-plane anisotropy. As illustrated in Fig. 1-3, the lattice structure of BP is anisotropic and the atomic arrangement is highly different along the AC and ZZ direction. This anisotropy in lattice structure leads to anisotropy in the carrier effective mass and further the carrier mobility [64, 65]. In the AC direction, the effective masses of BP is only ~0.08 m_0 while this value is ~10 times larger in the ZZ direction. The resulting conductance and performance difference in directions were discussed in [66]. In fact, the remarkable mobility of BP has made it a promising material for high performance and high frequency applications. Experimentalists have reported hole mobility of >45000 cm^2/Vs at cryogenic temperatures, which is comparable to graphene devices in theory [67]. The symmetry between the electron and hole mobility allows BP to be used in ambipolar or p-type channel transistors. Given the fact that many TMDs favor electron transport more than hole transport, BP is encouraging to be used in a wide range of applications and is a significant complement to 2D material field.

1.3   Applications of integrated heterogeneous 2D materials

For the 2D materials which have been successfully isolated from bulk crystals, field effect transistors using them as channels have been demonstrated with almost all of the materials. These atomic-thin film devices have shown performance with great variation [68, 69, 70, 71, 72, 16]. The most important application and benchmark of these transistors is the compatibility and performance of them in integrated circuits. Since the demonstration of discrete field-effect transistors (FETs), great efforts have been made to

build integrated circuits with 2D MOSFETs. However, the realization of complementary circuits has proven difficult despite the promise of the use of 2D material in discrete high-performance MOSFETs. The reason lies in the difficulty to fabricate high-performance n-MOSFET and p-MOSFETs with homogeneous 2D material simultaneously. Logic circuitry cells have been demonstrated with various materials discussed previously, yet they all suffer from shortcomings that limit the use of them in high-performance complementary logic.

In 2011, Radisavljevic, *et al*. reported all MoS_2 logic [73]. A logic inverter and a NOR gate was fabricated. In the inverter circuit, they used a gate/source connected transistor to serve as the load, which is resistive. Meanwhile, due to the lack of p-MOSFET and the difficulty in fabrication, they used an external resistor as the load in their NOR gate. However, this circuitry is not fully complementary due to the lack of p-type MOSFETs. They engineered the threshold voltage by controlling the work function of the gate metal and 2 types of metals were used to fabricate the enhancement mode and depletion mode transistors. Depletion mode transistors actually worked as resistors to serve as the pull-up load. Predictably, the pull up transistor cannot be switched off and so a high value of standby power is consumed. Thus, this circuit is not suitable for low-power applications.

Similar effort was already made by Wang, *et al*.in 2012 to demonstrate different kinds of logic gates with MoS_2 transistors [74]. In their work, logic gates including inverter, NAND gate, static random-access memory (SRAM) and a 5-stage ring oscillator (RO) were fabricated with MoS_2 MOSFETs based on a direct-coupled transistor logic

technology. In the logic gates, all transistors were fabricated on a single MoS_2 flake to ensure the uniformity of device performance. The circuits also suffer from the stand-by power problem. That is the reason why both p- and n-MOSFETs are critical for high-performance complementary logic.

For the above reasons, researchers on TMD logic circuits which are real complementary and worked on integrating devices with different polarities. Given that certain 2D materials create transistors of only one polarity, $MoTe_2$, WSe_2 and BP have drawn the attention of researchers since they are ambipolar and can thus realize n-MOSFET and p-MOSFET simultaneously. In 2014 Lin, *et al.* realized a logic inverter utilizing the ambipolarity of $MoTe_2$ [75]. Because the devices used for n-MOSFET and p-MOSFET were basically identical and only different operation regions on the device characteristics, both in the linear region were picked, the circuit was far from symmetric and the working regions restricted the performance. Moreover, the lack of individual gate electrodes and the unmatched in/out voltage windows failed the circuit to drive subsequent stages and make it lack the capacity to be integrated in multi-stage circuits, which is essential for practical applications.

WSe_2, as demonstrated by Das, *et al*., has the capability to be fabricated into both n-MOSFET and p-MOSFET with driven current of ~100 $\mu A/\mu m$ [76]. The polarity of the transistors can be tuned by electrostatic doping and contact work function engineering. Upon integrating the complementary MOSFETs, a logic inverter with a gain of ~ 25 was reported. They also reported a BP inverter with similar approach with electrostatic tuning [77]. The results are promising but the circuit sill shared the same problem with ref. [75]

and the electrostatic doping electrodes added the complexity of fabrication and further limited the suitability of this kind of circuit in large scale circuits.

A substrate gate approach has also been used by Zhu, *et al*. to fabricate logic inverters based on BP MOSFETs [78]. The inverter worked by splitting the minimum conduction points of two series transistors. Inverting behavior was seen but as the same reason in [75], the inverter is not suitable for large scale circuits. Besides, since homogeneous material was used and the devices worked near the region of the minimum conduction points, the performance of the circuit is limited.

Utilizing homogeneous 2D materials in complementary circuits is thus highly challenging. Silicon has been dominating the applications in logic circuits. One of the reasons is the symmetry between the n-MOSFETs and p-MOSFETs and various dopants have been proved successful. Hence, researchers are seeking solutions by integrating heterogeneous 2D materials. Cho, *et al*. reported results of integrating MoS_2 n-MOSFET and WSe_2 p-MOSFET on the same chip [79]. On one single substrate, transistors were fabricated separately and connected through metal wires. The substrate worked as the gate and input terminal. As heterogeneous materials were used for n- and p-MOSFETs, the inverter achieved a peak gain > 10.

As the 2D materials are atomically thin and can be transferred onto arbitrary substrates, researchers have demonstrated vertically stacked transistors with heterogeneous materials. Woo, *et al.* fabricated a vertically stacked inverter combing an MoS_2 n-MOSFET and a $Bi_2Sr_2Co_2O_8$ p-MOSFET [80]. In their work, a shared graphene drain terminal is sandwiched between the layers of MoS_2 and $Bi_2Sr_2Co_2O_8$ and the

channel is along the vertical direction unlike most 2D MOSFETs. This structure is novel but it also cannot be integrated due to the reason same as in [75].

Therefore, selecting a set of materials with symmetric performance is essential for realizing all-2D-material circuitry and a device structure allowing the large-scale integration is also required. Thus, in our experiments, MoS_2 and BP are chosen to realize high-performance logic circuit due to their close mobilities and symmetric polarities. In order to enhance the performance and enable the capacity to work in VLSI circuits, a local back gate structure is introduced with thin high-K gate dielectric layers. In the fabricated circuit, the channel and contact were engineered to ensure the symmetry. The results paved the way to 2D semiconducting material based high-performance integrated circuits.

Besides the application of one single material in one transistor, due to the layered nature of 2D materials and the ease of transfer onto arbitrary surfaces, heterostructures with 2D materials have become the focus of many researchers [81, 82]. Thanks to the wide range of band structures of various 2D materials, many different types of heterostructures can be formed between their permutations, which can serve for numerous device applications. Heterostructures can be categorized into three types for different band alignments, namely the symmetric (type I), staggered (type II), and broken gap (type III). When material A and material B form a heterostructure, the heterostructure is type I if $VBM_A < VBM_B < CBM_B < CBM_A$, type II if $VBM_A < VBM_B < CBM_A < CBM_B$, or type III if $VBM_A < CBM_A < VBM_B < CBM_B$. An illustration of the different heterostructure types is shown in Fig. 1-6 and each type has its advantage in different

device applications. Type I heterostructures are most widely used in optical devices, for example light emitting diodes, since electrons and holes can be spatially confined and thus efficient recombination can occur (Fig. 1-6 (a)). Type II heterostructures are suitable for high electron mobility transistors or solar cells due to the strong carrier confinement from the larger offset on one side (Fig. 1-6 (b)). They are also useful for harnessing long-lived interlayer (or indirect) excitons (Fig. 1-6 (c)). Type III heterostructures are ideal for tunneling field effect transistors (TFETs) as they can massively enhance the tunneling current density thanks to the almost non-existing band-to-band tunneling barrier.
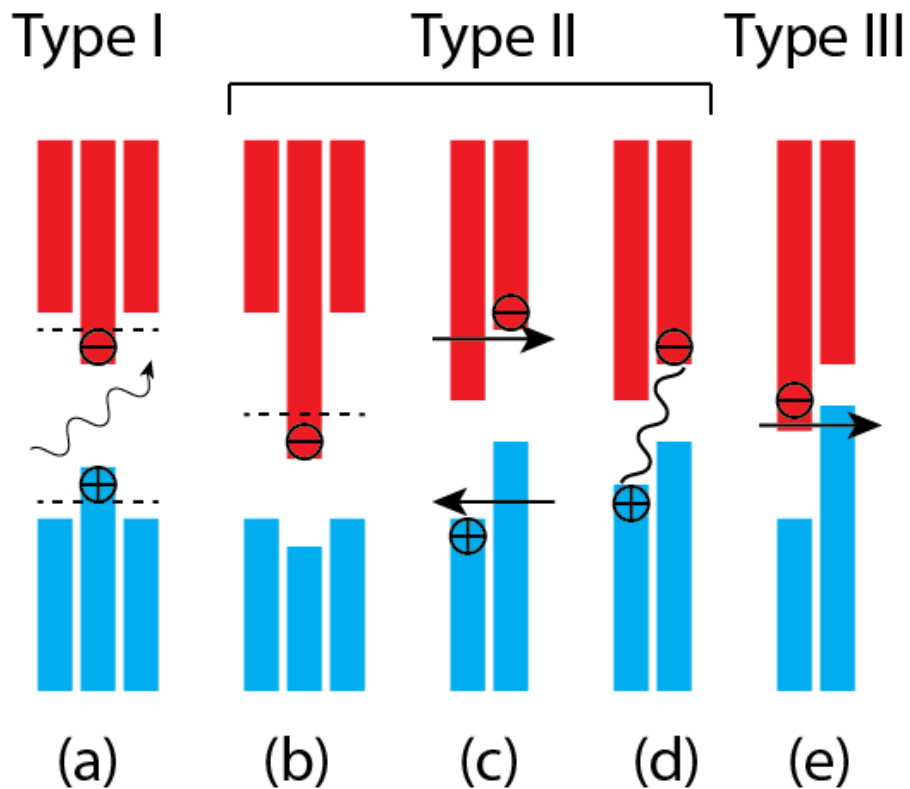
Figure 1-6 Illustration of (a) type I, (b-d) type II and (e) type III heterostuctures and devices based on them. Conduction bands are indicted with red bars and valence bands are in blue.

Although the electronic band structures of many 2D materials have been well studied, the band alignments between different 2D materials are yet to be fully understood. Here, provided is a visible comparison of bands for some common monolayer 2D materials which are calculated with the Perdew-Burke-Ernzerhof (PBE) functional [83] and determined from experiments [84]. The comparative band alignments are shown in Fig. 1-7. Generally, as the atomic number of the chalcogen increases, the CBM and VBM of corresponding MX_2 material become closer, resulting in narrower band gaps. Some materials have high VBMs, such as $MoTe_2$ or WTe_2, which are potential to form broken gap structures with materials whose CBMs are below them, like SnS_2 or $SnSe_2$.
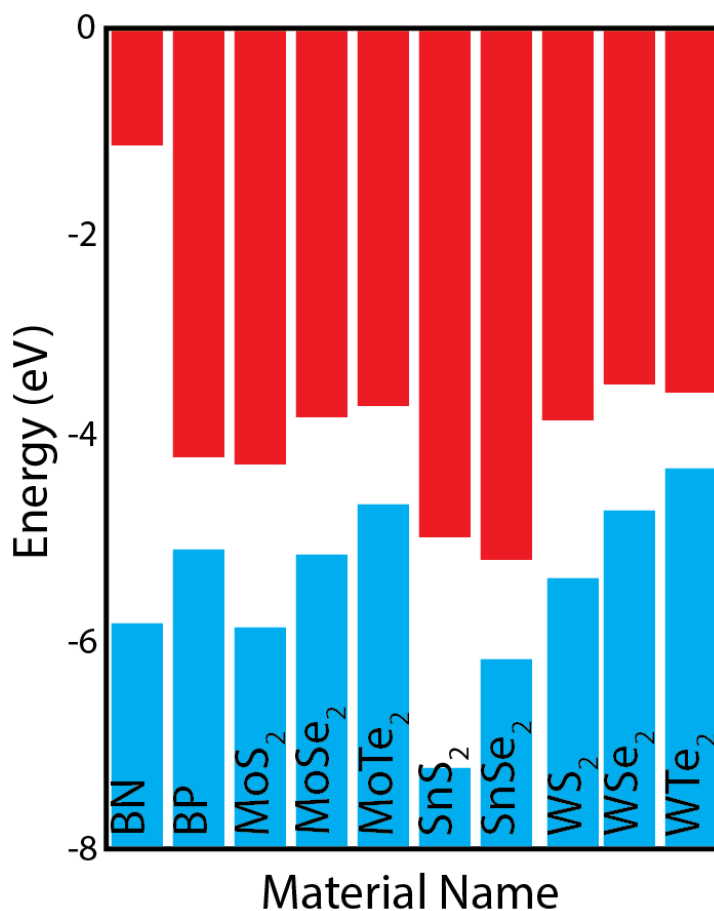
Figure 1-7 Comparative band edges of monolayer 2D materials where conduction bands are shown in red and valence bands are shown in blue with 0 is set for vacuum energies.

1.4 Dissertation overview

There are immense applications that 2D materials could fit in thanks to their excellent and variable properties. They are already of interest of numerous device applications and a great number of devices have been demonstrated using homogeneous 2D materials. However, to better utilize the unique layered feature and flexible properties, integrating heterogeneous 2D materials together or building heterostructures with them are promising and have drawn great attention of researchers. In this

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dissertation, devices and circuits using heterogeneous integration of 2D materials are described.

Chapter 2 will focus on the preliminary device results to establish the way to integrated circuits based on 2D materials. Our approach to boost the device performance by introducing the local backgate structure will be reviewed. The fabrication flow that allows thin high-K gate dielectric and excellent gate/channel interface will be introduced. And the measurement results as well as the discussion will also be made. In addition, the response of the local backgate devices to radiation will be reviewed.

Chapter 3 will provide the readers a thorough introduction of the logic and memory circuits fabricated in our lab. This chapter starts with the explanation of the process steps for the 2D logic inverter made by integrating a MoS_2 n-MOSFET and a BP p-MOSFET. Our set up of the DC measurement will be shown along with the DC measurement results. The suitability of this circuitry in larger scale integrated circuits will be discussed by extracting properties regarding the circuit performance. Transient measurement on the inverter will also be talked about to argue the circuit performance at high frequencies. Another kind of circuits, memory cells which are fabricated in our lab will also be shown including the fabrication technique and the waveform tests will be explained.

Devices based on heterostructures consisting of two different 2D materials will be reviewed in Chapter 4. As for each different device configuration, the fabrication method of the global backgate structure is shown in the beginning. Then the characteristics of transistors made with two materials which compose the heterostructures will be

discussed. The measurement results and band alignment analysis of the vertical stacked heterostructures will be provided. The synthesis of a novel laterally stacked heterostructures will be talked.

Finally, the dissertation will be concluded by emphasizing the motivation of this dissertation, which is to explain the promise of realizing high-performance devices using 2D materials, the potential of integrating heterogeneous 2D materials in large scale logic and memory circuits and building various types of heterostructures with 2D materials. The author hopes that the original efforts reviewed in this dissertation can pave the way for future research in this area. Additionally, some research ideas that may spark the inspiration of other researchers will be provided.

CHAPTER 2   2D DEVICES FOR LOGIC CIRCUITS

In the previous chapter, various 2D materials and mentioned the potential capacity of them to substitute silicon in modern CMOS technology were introduced. These 2D materials are promising because they have layered crystal structure which can be realized in monolayer form, but also have a finite band gap and can thus create high-performance transistors with high on-to-off current ratio. In order to build high-performance logic and memory circuits, devices with high drive current, low contact resistance and sharp subthreshold slope are required. Moreover, good asymmetry between nFETs and pFETs is also preferred. Thus, MoS_2 is selected over other 2D materials for the band gap of 1.2 eV, which is similar to silicon and better carrier mobility than other TMDs. Besides, the 2.2 eV direct band gap of monolayer MoS_2 can effectively suppress the off current, making it promising for low leakage application. However, due to the Schottky barrier heights of common metals being near the conduction band edge, it is challenging to make p-type MoS_2 FETs, making all-MoS_2 logic impractical. But the exploration of BP, a high conductivity p-type material, allows good match-up between p-type and n-type 2D MOSFETs. Thus, MoS_2 and BP are chosen in our experiments [85].

2.1   Local backgate device fabrication

As discussed in Chapter 1, even CVD process has been demonstrated to provide large area thin 2D materials, due to reasons such as lattice mismatch or interface traps, the carrier mobility and film quality are typically worse than pristine 2D material film exfoliated from bulk crystals which are mostly single-grain. Thus, exfoliated and

transferred MoS_2 and BP flakes are used as channel materials in our devices. Also, as shown in Chapter 1, for each sulfur atom in MoS_2, all the valence electrons are covalently bonded with adjacent Mo atoms. Thus, dangling bonds are non-existing in pristine MoS_2 and most TMDs. Hence, the growth of thin, high quality dielectric film on top of 2D materials is proven to be a challenge. In fact, the density of interface traps is a significant factor that impacts the carrier mobility. Therefore, a local backgated design was introduced in our devices which can avoid the growth of oxide on top of 2D films. Since the coverage of grown oxide is out of the consideration, the gate oxide thickness can be reduced, and thus the gate control can be improved. A brief introduction of the process flow is as follows.

As shown in Fig. 2-1 (a), the device fabrication started by using a bulk silicon wafer with 110 nm SiO_2 thermally grown on top of it. Next, the gate electrode was patterned using electron beam lithography (EBL) followed by solution development. A recessed region was created by a mix of dry etch and wet etch in the exposed area. The recessed region was then filled by the deposition of Ti/Pd in electron beam evaporator and lift off, shown in Fig. 2-1 (b). After that, high-K dielectric layer was deposited using atomic layer deposition (ALD) to form the gate oxide. Chosen 2D material flakes were then transferred onto the gate fingers, shown in Fig. 2-1 (c). EBL and evaporation were used again to create Ti/Au metallization which serves as source and drain contact electrodes. Finally, passivation oxide layer was deposited by ALD to provide stability in ambient atmosphere. Greater details will be discussed in the following paragraphs to provide a clearer view of the entire process.
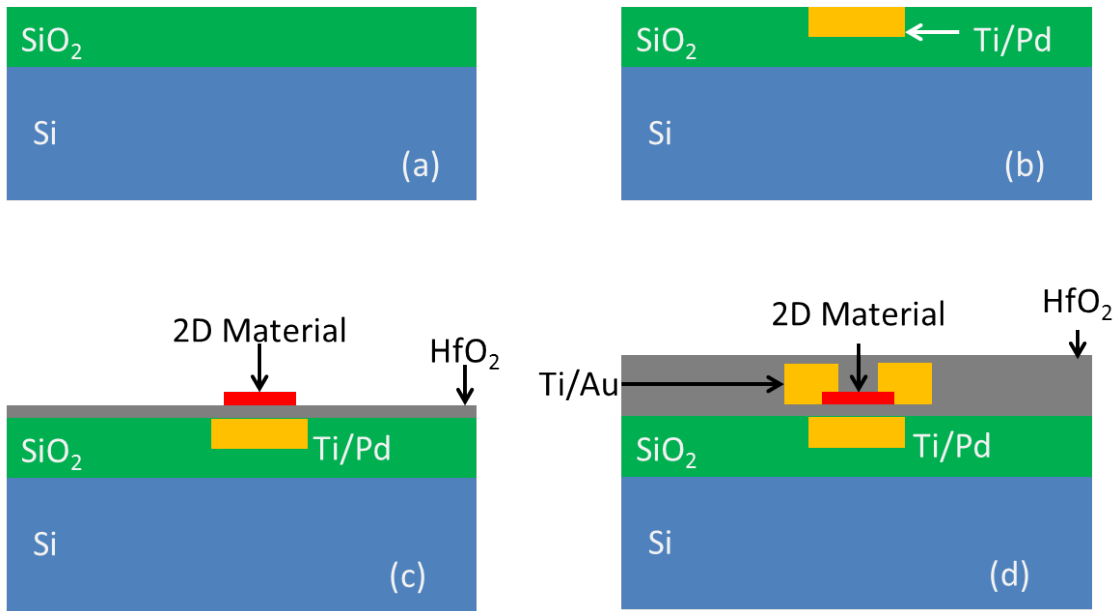
Figure 2-1 Fabrication sequence for 2D material MOSFETs with local back gates.

The process starts with an oxide layer grown on top of plain silicon wafer. Since the devices are built upon the amorphous SiO_2 layer, the doping and the crystal orientation of the silicon substrate are not needed to be specified. In the growth process, 4-inch silicon wafer cleaned in sulfuric acid bath and RCA is placed in an oxidation furnace. The furnace is then heated up to a high temperature (~1000 °C) with adjusted gas flow. Two types of oxide can be grown depending on the gas formation chosen, wet oxide and dry oxide. A mixture of O_2 and H_2 is used for the former and pure O_2 gas is used for the latter. Annealing at high temperature in N_2 gas can be done in the same furnace. In our experiments, dry oxide was used more often because oxide grown in the wet condition tends to be more porous, which causes higher roughness after the recess etching. One drawback of the dry growth process is the grow rate, which is about several times lower than the wet process. Therefore, thinner oxide is usually used when dry oxide

was chosen. For the oxide thickness, the only requirement is that it must exceed the depth of the gate electrode recess. Given that the recess depth is generally ~50 nm, an oxide thicker than 60 nm should be sufficient. However, as argued in [7], in order to better visually identify the atomically thin 2D materials, the substrate thickness needs to be carefully chosen for a good contrast from optical interference. Thus, typically ~300 nm and ~100 nm are chosen for the thickness to be grown by wet and dry process, respectively.

Since exfoliated 2D materials are used as the channel material, the number of devices that can be fabricated in a single fabrication run is quite low, typically ~10 devices on a chip. So, using the entire 4-inch wafer for one batch of devices is not needed. After the oxidation, whole wafer was thus cleaved by diamond scribe into smaller samples which are 1-2 cm in width and length for handling. The fabrication of 2D MOSFET is a multi-step process. In order to achieve good alignment between different lithography layers, global alignment marks are required to be patterned. In our mask design, array of 10×10 μm squares spaced by 1000 μm are exposed in an EBL system. The EBL process can be summarized as follows:

    a) Cleaved substrate is sonicated in acetone,

    b) The sample is then washed with solvents and then dried,

    c) 950 polymethylmethacrylate (PMMA) C4, is spin coated onto the substrate,

    d) The sample is hard baked at 180°C for 8~10 minutes to bake the solvent out,

e) The sample is exposed in the EBL system at a dose of 1200 $\mu C/cm^2$,

f) Exposed sample is developed in a solution of 1:3 methyl isobutyl ketone (MIBK) and isopropanol (IPA) at 20°C for at least 90 seconds. Stirring occasionally is preferred.

After the development, it is best to inspect the exposed wafer under optical microscope to confirm the existence of patterns. Next, the Ti/Au metallization can be carried out in the electron beam evaporator. In our process, titanium layer of 10 nm is deposited first as the adhesive layer followed by the gold deposition. In order to be detected in the SEM of the EBL system, high Z-ratio metal must be used for the alignment mark, and this is why gold is selected. For successful detection, gold layer need to be at least 40 nm thick and for a clean lift off, the metal layer should not exceed one third of the resist thickness (100 nm). After the deposition, the sample is soaked in acetone or NMP for a day to lift the metal off.

Then, with the assistance of the alignment marks, gate electrodes are patterned and exposed as the process explained above. The gate electrodes are stripes with aspect ratio around 5 cascaded in the order of length, finally connected to a 200 $\mu m \times 200$ μm pad for the ease of probing. Unbiased MoS_2 is very resistive, for which the gate finger is designed to be wider than the spacing of source and drain fingers. Normally, the gate finger is patterned as a 2 $\mu m \times 40$ μm stripe, for the tolerance of alignment error of the EBL system and the aligning probe station. After the development and inspection, the sample is loaded into a plasma etch chamber. Brief O_2 plasma clean is carried out for five seconds first to remove any organic residue due to incomplete development. Then the

SiO$_2$ is etched with a standard recipe, which takes two minutes and the etch rate is ~20 nm/min. Though dry oxide is less porous than wet oxide, this process will lead to grass formation at the bottom of the recessed trench. Since the following evaporation metallization and ALD process are both anisotropic processes, this roughness will cause weak spots in the gate oxide and increase the risk of electro-static discharge (ESD) breakdown. A following buffer oxide etch (BOE) is useful to smooth out the grass as it is isotropic. Thus, the sample is then soaked in 1:10 BOE solution for 12 seconds. Given the etch rate of thermal oxide in BOE is 50 nm/min, this mix etch process can create a recess depth of ~50 nm.

It is necessary to confirm the recess profile before the metal deposition since the etch rate is not constant and depended on the equipment configuration. Getting very accurate etching data could be cumbersome and the data can be non-uniform across the sample. Thus, an easier way to extract the approximate data is often used for guidance. Sharp-end tweezers are taken to make several scratches on the resist in different areas of the sample. Then the scratches are measured using a surface-profilometer to get the resist thickness. These numbers are subtracted by the depth measured at the closest recess, which is the sum of the resist thickness and the recess depth. The average number is then used as the deposition thickness.

With the electron beam resist still on, the sample is then loaded into the evaporation chamber for gate metallization. Ti and Pd are selected as adhesive and contact material. The work function of Pd is ~5.5 eV, which can provide good match of the threshold voltage between the n-MOSFET and p-MOSFET. To ensure good film

quality, the deposition is carried out in high vacuum ($< 10^{-7}$ Torr). The sample is then soaked in acetone for more than 12 hours to lift the metal off.

The ALD process is then carried out for good dielectric quality. The ALD chamber is heated up to 300 °C and the solvent-cleaned sample is placed in the center of the chamber and then 20 nm of HfO_2 is deposited followed by ellipsometer characterization.

Next, thin 2D material flakes are exfoliated from the bulk crystal and transferred onto the gate fingers. The exfoliation process, which is illustrated in Fig. 2-2, is summarized in the appendix. After a single flake is successfully transferred onto the substrate, this process can be repeated until the desired number of flakes is reached. Note at this step, the size, shape and thickness are not controllable since this is mostly a random process and relies upon cherry-picking. Due to the imprecisely control of the micro-manipulator and the low resolution of the alignment microscope, transferring the flake exactly is a challenging work. Thus, larger flakes are usually preferred. Fig. 2-3 shows the alignment station and micro-manipulator.
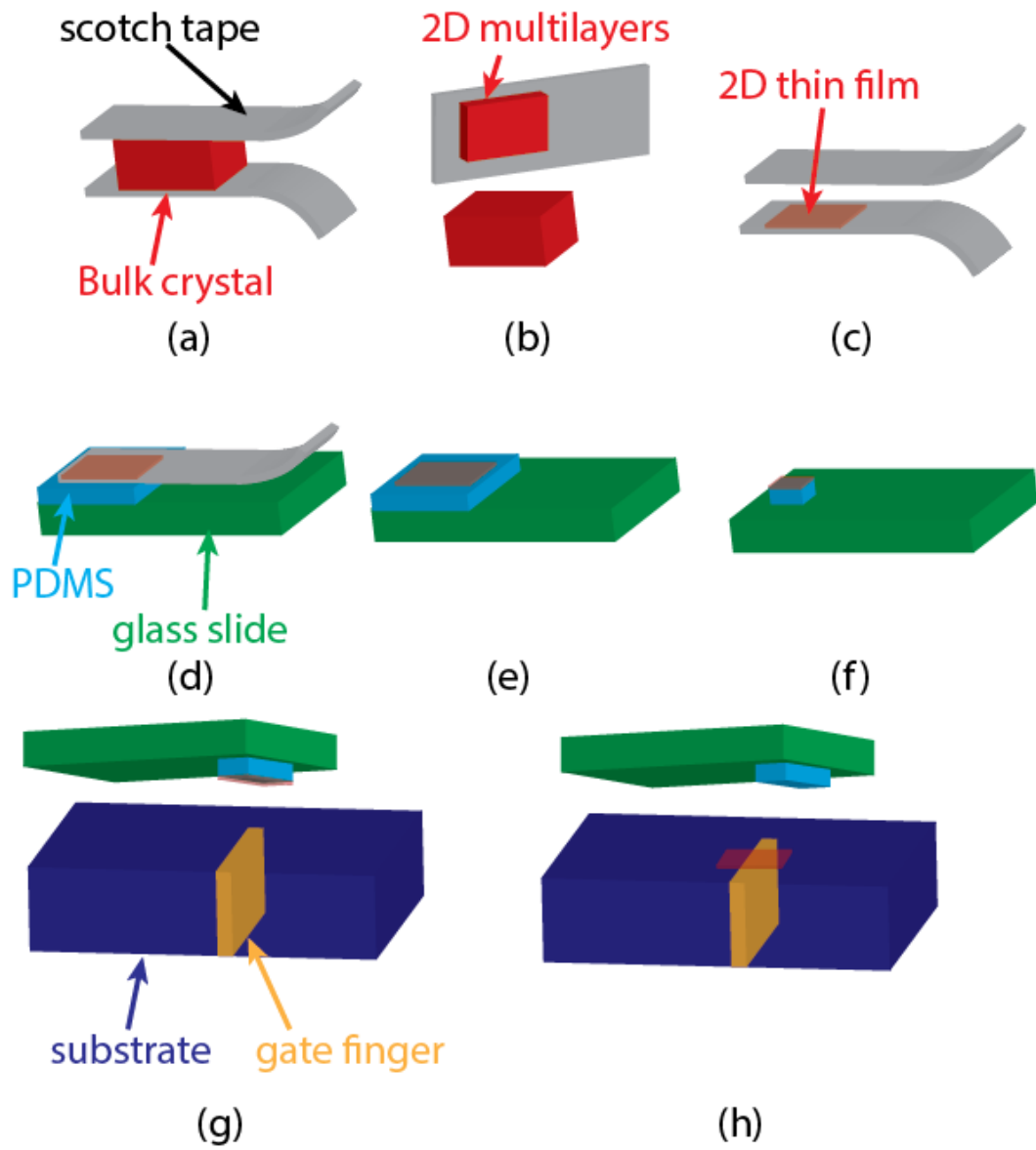
Figure 2-2 The process breakdown of the mechanical exfoliation and alignment transferring of the 2D materials.
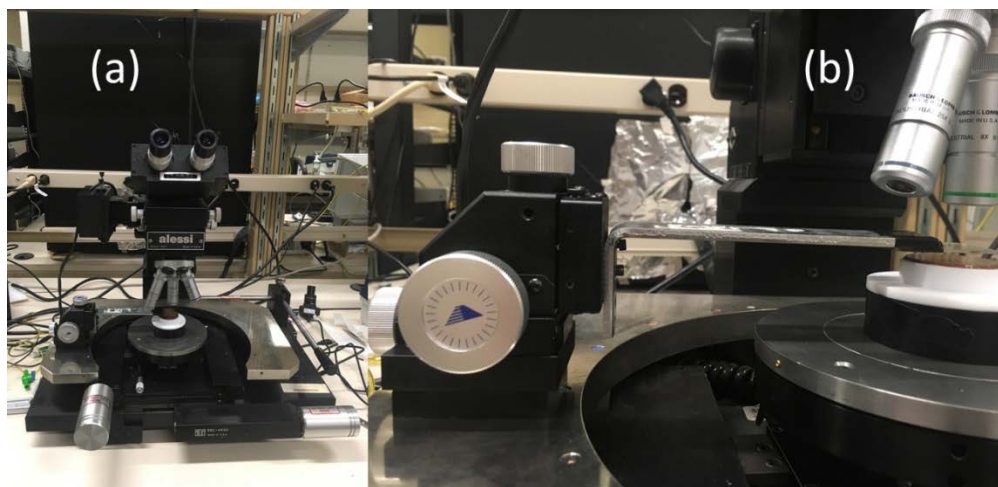
Figure 2-3 Photographs of the alignment stage and micromanipulator utilized for the aligned 2D material transfer process.

Activated polydimethylsiloxane (PDMS) is an achromatic transparent polymer, and thus it is difficult to search for few-layer 2D flakes on it which are also transparent. Fig. 2-4 shows an example of few-layer black phosphorus on PDMS. Even with the right brightness of the light source on the optical and microscope and high magnification, it takes great carefulness, patience and experience in the search of the barely visible flakes.
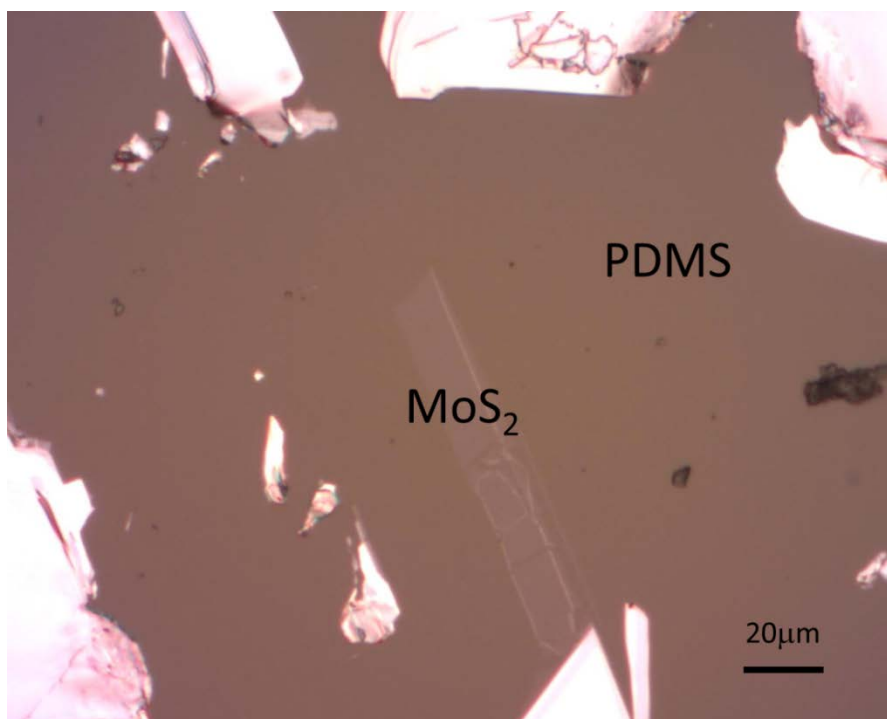
Figure 2-4 Optical micrograph of a few-layer MoS$_2$ flake on PDMS.

The chip with transferred flakes is then photographed under microscope again for the mapping information. Since each flake exfoliated and transferred is unique, and the location of the transferring is to some extent random, the EBL mask needs to be customized for every single device. Fig. 2-5 shows a photograph of a few-layer MoS$_2$ flake transferred on a gate finger. Because the coordination of the gate finger is already known, the size and location information of the flake can be determined.
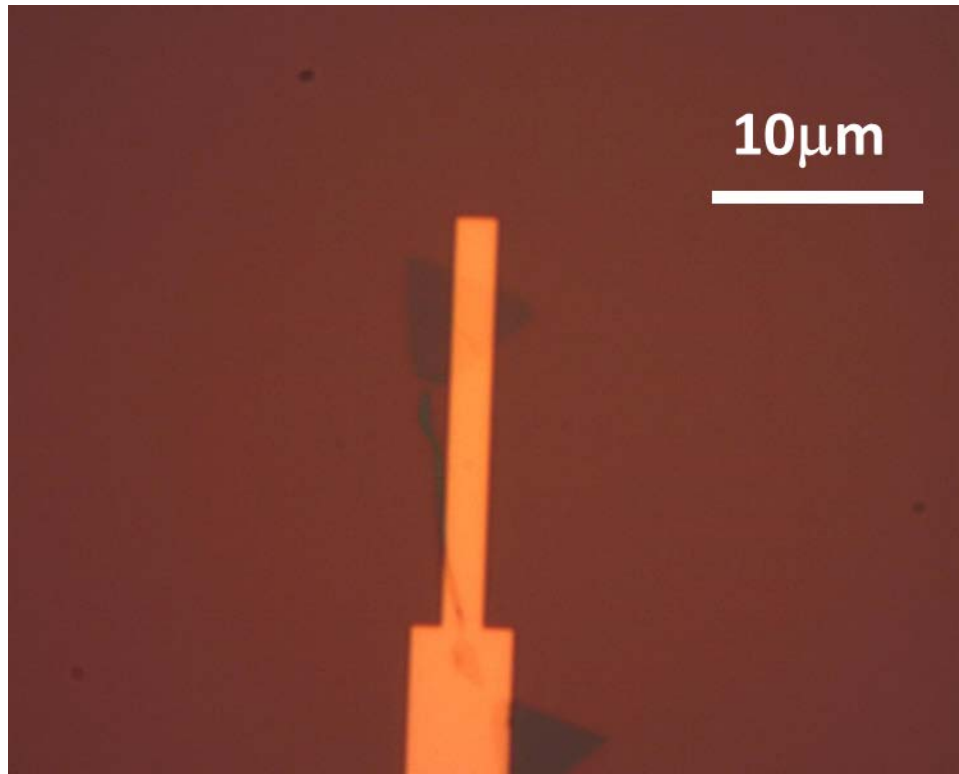
Figure 2-5 Triangular few-layer MoS_2 flake transferred on top of a gate finger, the substrate oxide thickness is 300nm.

With the mask design the source and drain contacts can be fabricated. The EBL and metallization process shall be slightly different than mentioned above. First, since the exfoliated flakes are bonded to the SiO_2 oxide with weak van der Waals force, the loose bond can be easily broken by solvent spay. Thus, to pre-clean the sample before resist spin coating, the solvent should be sprayed in the corner of the chip and streamed to the entire sample. Sonication is definitely not useable at this moment. Second, for TMDs, in order to descum before the metal deposition, brief O_2 plasma etch and BOE dipping can be carried out to improve the contact quality. For BP, since it is water sensitive, brief Ar plasma can be performed instead. Third, BP is air and moisture sensitive. Therefore, except for necessary exposure to atmosphere, i.e. the exfoliation and transferring, the

sample must be always stored in vacuum environment or with desiccant. After the metal evaporation, the sample is lifted off in acetone for more than 4 hours to protect the light sensitive BP device. The beaker filled with acetone need to be placed in dark. After the lift-off, the sample is cleaned with fresh acetone, methanol, IPA spray bottle and blown dry with N_2 gun. Since the contacts can be used to anchor the flakes, the device area can be sprayed directly now.

After the cleaning, the devices are stored in vacuum immediately if the channel material is BP. To provide air stability, an optional passivation layer can be grown with ALD, and the growth temperature is 200 °C. Fig. 2-6 is the photographs taken of passivated MoS_2 and BP MOSFETs.
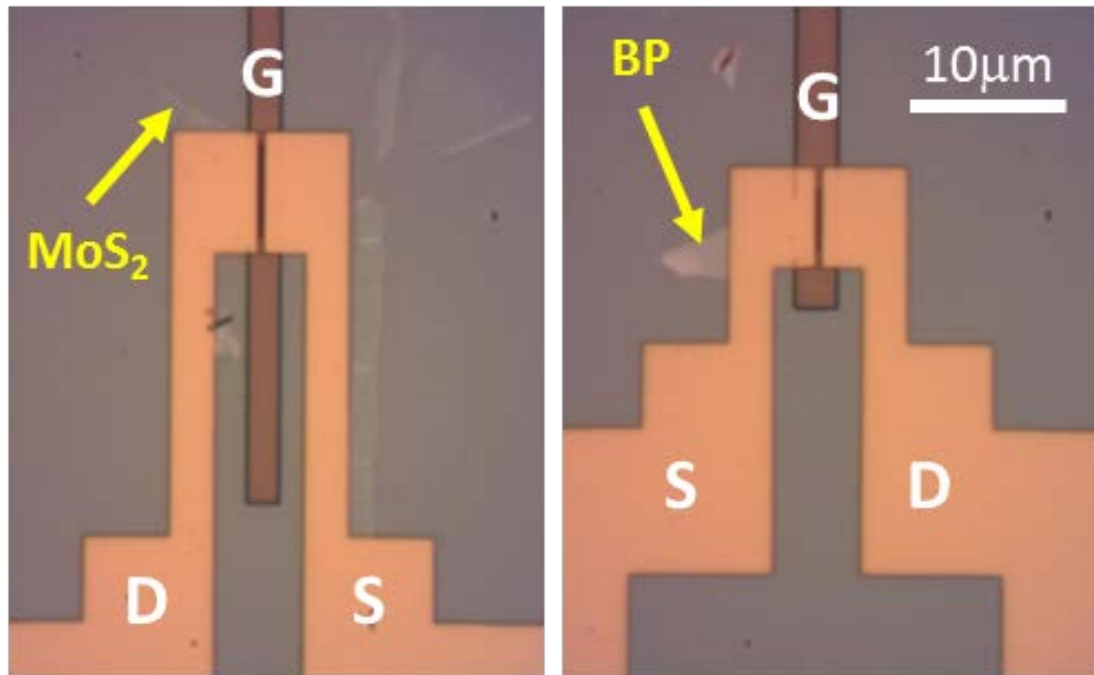
Figure 2-6 Optical micrographs of a MoS_2 n-MOSFET and a BP p-MOSFET. The source/drain contact separation, L_{eff}, is 0.5 μm.

2.2 Device performance

The devices shown in Fig. 2-6 were fabricated simultaneously on the same chip. The effective length of both devices, which equals to the source/drain contact spacing determined by EBL, is 500 nm. The device widths, which are the widths of the flakes sandwiched between the source and drain fingers, are 8 μm and 5 μm, for the MoS_2 and BP FETs, respectively. Since exfoliated 2D material can be transferred onto arbitrary surface, integrating heterogeneous 2D materials together takes no extra effort than utilizing homogeneous 2D material. Owing to the fact that BP decomposes in air with the assistance of light, the devices were measured with an Agilent B1500A semiconductor parameter analyzer in the dark using a cryogenic vacuum probe station at a pressure of $<$ 10^{-5} Torr. The devices were probed on all three contact pads and performed 3-terminal measurements. To start with, drain current, I_D, vs. gate-to-source voltage, V_{GS}, measurements were performed on the devices both before and after 30 nm HfO_2 passivation. The results for the MoS_2 n-MOSFET are shown in Fig. 2-7.

In Fig. 2-7 (a), V_{GS} was swept from -1.0 V to +1.5 V with the drain-to-source voltage, V_{DS} being +0.1 V and +1.5 V for the unpassivated MoS_2 device. From the plot, on-to-off current ratios $> 10^8$ can be seen for both drain biases. Moreover, as noted, due to the limitation of our test equipment, the off-current hit the noise floor, which means the real off current can be even lower, indicating a higher on-to-off ratio. Besides the high on-to-off ratio, another exciting feature is the nearly ideal subthreshold swing (SS). Values of 64 mV/decade and 76 mV/decade were observed at V_{DS} = 0.1 V and 1.5 V, respectively. These results indicate that extremely high quality interface can be achieved

between pristine MoS_2 and HfO_2 using the buried gate electrode design thanks to the lack of necessity of dielectric onto 2D materials. The devices also had negligible drain-induced barrier lowering due to the extremely-thin dielectric utilized. The dielectric constant of HfO_2 grown in our lab is ~17, and it can be calculated that the effective oxide thickness (EOT) with

$$EOT = \frac{t_{OX} * \varepsilon_{SiO_2}}{\varepsilon_{OX}},$$

(2.1)

where t_{OX} represents the oxide thickness, ε_{SiO_2} stands for the dielectric constant of SiO_2 and ε_{OX} indicates the dielectric constant. The EOT of our high-K gate oxide is ~4.4 nm. Using this structure, in our lab 7 nm high-K gate dielectric has been realized which indicates an EOT of ~1.5 nm. The transconductance, g_m was extracted at the drain bias of 1.5 V, as:

$$g_m = \frac{\partial I_d}{\partial V_{gs}},$$

(2.2)

and a peak value of 42 µS/µm was obtained.
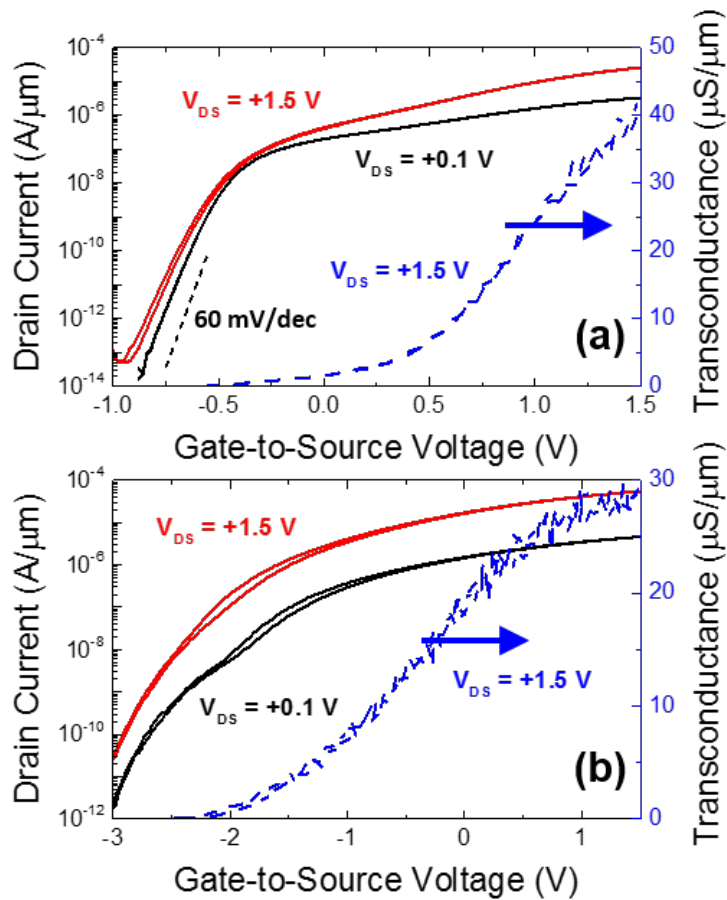
Figure 2-7 I_D and g_m vs. V_{GS} for a MoS$_2$ n-MOSFET (a) before and (b) after ALD HfO$_2$ passivation. V_{GS} was swept from -1 V to 1.5 V in (a) and from -3 V to 1.5 V in (b). V_{DS} was biased at +0.1 V and +1.5 V.

The results for the device after passivation are shown in Fig. 2-7 (b). Nearly identical measurement setup was applied for this measurement except for the larger V_{GS} sweep window owing to the negatively shifted threshold. This degraded subthreshold slope clearly shows the impact of the interface states induced by the growth of oxide on top of the channel. Also degraded is the g_m which is 27 μS/μm at the same bias condition. The threshold shift was also observed in MoS$_2$ and BP FETs with the deposition of Al$_2$O$_3$

dielectric layer on top of the channel [86, 87]. The shift of the threshold was induced by the positive fixed interface charges in the dielectric layer. Negative threshold shift was also observed in MoS_2 FETs with high-k dielectric layer which is explained by the presence of oxygen vacancies at the interface between the high-k dielectric and the channel [88].

The same kind of measurement was also carried out on the BP p-MOSFET and the results are plotted in Fig. 2-8. For the device before passivation as in Fig. 2-8 (a), the V_{GS} was swept from 1.0 V to -1.5 V at V_{DS} of -0.1 V and -1.5 V, to match up with the n-MOSFET. The BP p-MOSFET showed very p-type behavior with on-to-off current ratio of $> 10^2$ because of the narrower energy gap of BP and the transconductance extracted at V_{DS} = -1.5 V was 147 µS/µm. After passivation, as shown in Fig. 2-8 (b), the threshold also shifts to the negative side and the g_m value was degraded to 63 µS/µm. However, for most BP MOSFETs fabricated with this structure, the on-to-off ratio and subthreshold slope did not degrade as a result of the passivation. This is for the reason that the trapped moisture beneath the BP is baked out in the high temperature vacuum chamber of the ALD system.
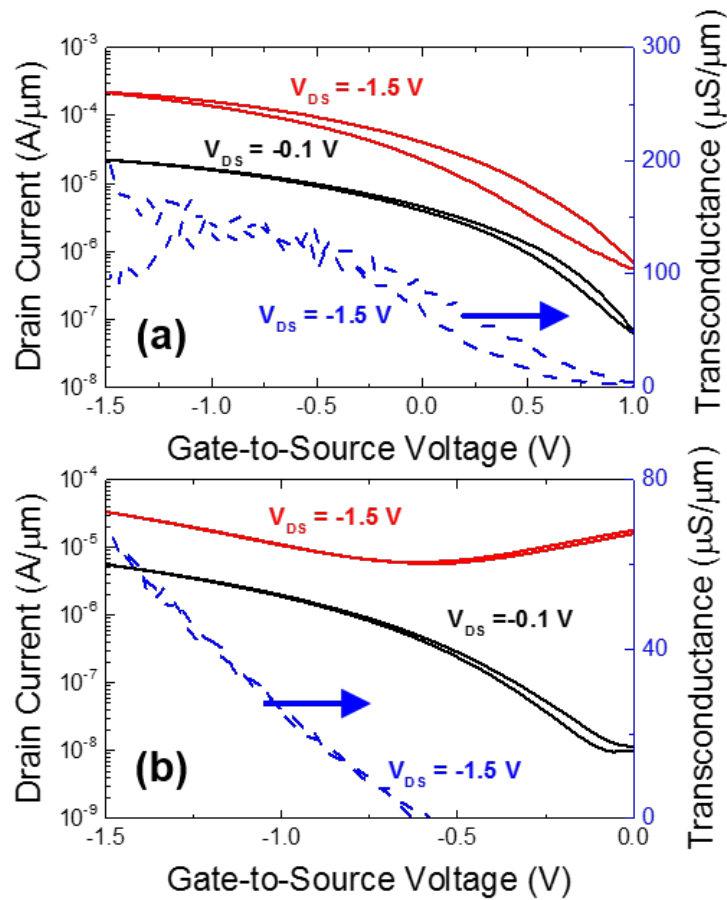
Figure 2-8 I_D and g_m vs. V_{GS} for a BP p-MOSFET (a) before and (b) after ALD HfO$_2$ passivation. V_{GS} was swept from -1.5 V to 1.5 V. V_{DS} was biased at +0.1 V and +1.5 V.

Even though the passivation degraded the subthreshold performance and transconductance of the devices, the matching between the device characteristics was improved. Plotted in Fig. 2-9 are the output characteristics of the passivated devices in which I_D is plotted vs. V_{DS}. For both devices, a maximum value of 1.5 V was applied at both $|V_{DS}|$ and $|V_{GS}|$. At these bias conditions, drive currents of 47 μA/μm and 54 μA/μm were obtained for the n-MOSFET and p-MOSFET, respectively. These results are a clear

indication that this material set is promising for making high-performance complementary circuits.
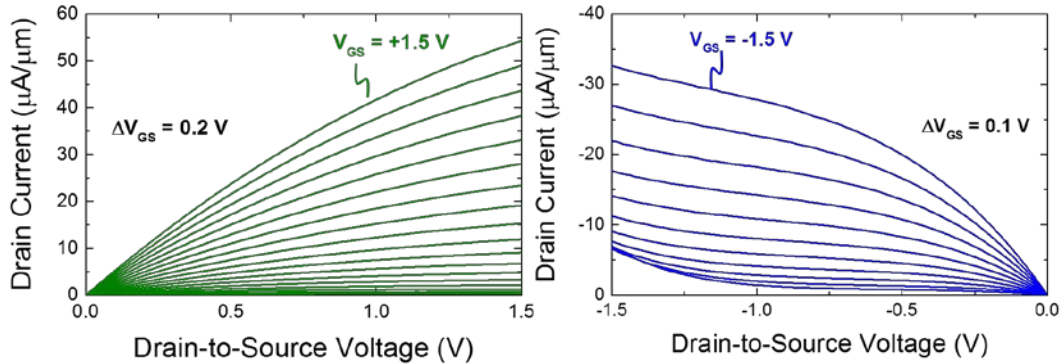
Figure 2-9 I_D vs. V_{DS} characteristics of a passivated (a) MoS_2 n-MOSFET and (b) BP p-MOSFET. $|V_{DS}|$ was swept from 0 V to 1.5 V. V_{GS} was taken from -3 V to 1.5 V at a step of 0.2 V for the n-MOSFET and from -1.5 V to 1.5 V at a step of 0.1 V for the p-MOSFET.

2.3 Radiation response of 2D devices

2D materials are promising for modern device and circuit applications, including space electronics, which is heavily influenced by the commercial semiconductor industry. In space, all the device and circuits in the electronics experience heavy irradiation, which can cause failures both due to total ionizing dose (TID) and single event effects. TID effects occur when charges are generated in the gate oxide and get trapped as a result of ionizing radiation. This build-up of charges shifts the threshold voltage causing errors in logic and memory circuits. Therefore, the radiation tolerance of gate dielectric layers and channel/dielectric interfaces must be evaluated before these devices can be considered for potential application in space radiation environments. The total TID response, which is

characterized as the impact on the device operation as a function of accumulated dose, for MoS$_2$ transistors has been investigated by Zhang *et al.* [89], while the TID response of BP devices had not been studied before this work.

In the experiments, the TID response of BP MOSFETs with HfO$_2$ gate dielectrics to 10-keV x-ray irradiation as a function of applied gate biases was evaluated [90]. Significant current-voltage (IV) shifts, subthreshold swing (SS) and mobility degradation were seen for both positive and negative bias conditions. During post-irradiation switched-bias annealing, the reversibility of these parameters is associated with trapping of compensating electrons during positive-bias annealing, and detrapping of electrons during negative-bias annealing. The charge trapping in these BP transistors with HfO$_2$ gate oxides appears to be dominated by hole trapping in the gate dielectric layer and/or defects at the BP/dielectric interfaces.

The transistors were irradiated with a 10-keV ARACOR x-ray source at a dose rate of 31.5 krad (SiO$_2$)/min at room temperature. Device responses upon radiation exposure were measured in-situ at room temperature with applied positive and negative gate bias. All electrical measurements were performed with a HP 4156A Semiconductor Parameter Analyzer. This radiation testing was performed in collaboration with Vanderbilt University [90].

The stability of the device transfer characteristics under gate stress is plotted in Fig. 2-10, where the ambipolar currents are shown. I_D is plotted with V_{GS} swept from +3 V to -1.5 V at V_{DS} = -0.1 V. For each curve, the measurement was taken after each stress

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period in which the gate electrode was biased at +1 V (Fig. 2-10 (a)) and -1 V (Fig. 2-10 (b)) with other terminals grounded. Each sweep takes less than 10 seconds, so stressing effects are negligible during IV sweeping. An insignificant positive shift in the transfer characteristics is observed, which results from electron trapping at or near the interface of the gate-HfO_2/BP layer. For the negative stress in Fig. 2-10 (b), even less shift is observed. These results indicate that the stability of the p-MOSFET meet the requirements of the radiation experiments.
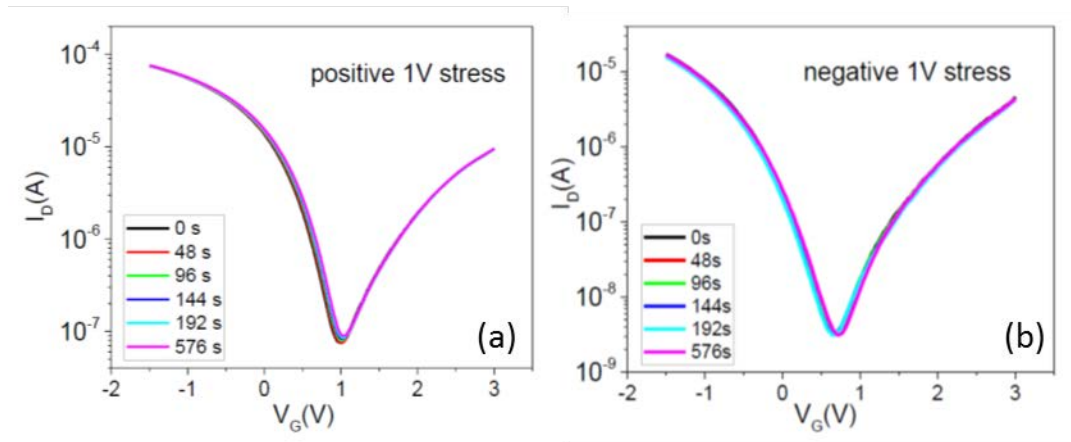
Figure 2-10 Stability under stress over time of BP p-MOSFET under stress voltage of (a) +1V, (b) -1V [90]. V_{GS} was swept from -1.5 V to 3 V.

Fig. 2-11 (a)-(b) shows the transfer characteristics vs. total dose and annealing time at room temperature. The devices were irradiated up to 1 Mrad (SiO_2) at the same bias conditions as in the stability test. The transfer characteristics shifted negatively under both stress voltages, but the subthreshold slope increased with the absorbed dose. During the stressing, due to the high conductivity of BP, the channel can be considered as grounded. Thus, the electric field drop is mostly across the gate oxide, while the top

passivation layer has a negligible effect. Therefore, the voltage shifts in Fig. 2-11 (a) and (b) are primarily due to the net radiation-induced trapped holes in the gate HfO_2 layer. The application of positive gate stress during irradiation results in more charge trapping than negative bias in the gate oxide, owing to both the much higher electric field in the region between the gate Ti/Pd electrode and the BP and the greater effects of hole trapping in the gate HfO_2 layer on ΔV_{th} for positive bias irradiation than under negative bias irradiation. After irradiation, the same gate bias is applied to the devices for 30 minutes to test for room-temperature annealing. Fig. 2-11 (c) and (d) show that very little recovery is observed. After annealing in air for 20 days, the transfer characteristics recovered to the values observed at absorbed dose of 500 krad (SiO_2) approximately, as shown in Fig. 2-11 (a). This indicates that some charges are trapped permanently and charge trapping displays long-term stability at room temperature.
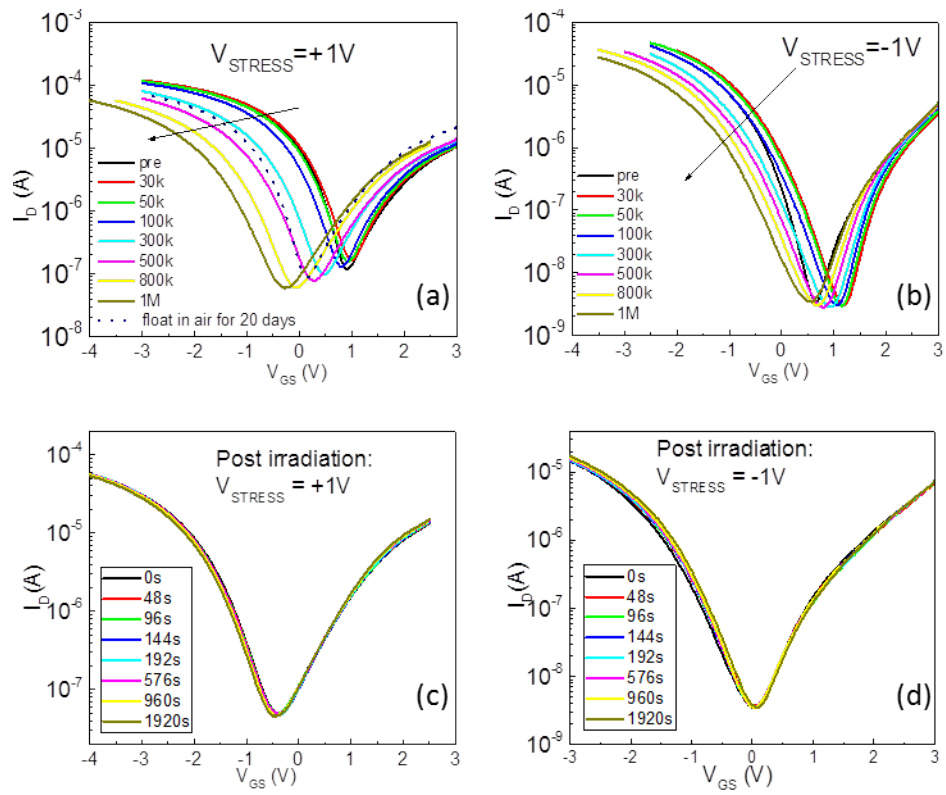
Figure 2-11 Transfer characteristics as a function of total dose with V_{STRESS} of (a) +1 V and (b) −1 V, and as a function of annealing time with V_{STRESS} of (c) + 1 V and (d) − 1 V [90]. V_{GS} was swept in different ranges to ensure full on/off characteristics.

CHAPTER 3 LOGIC AND MEMORY CIRCUITS BASED ON 2D MATERIALS

In chapter 1, potential applications of various 2D materials and the advantage of integrating heterogeneous 2D materials in one device or circuit were reviewed. In the present time, CMOS technology is still dominating in logic and memory electronics industry. However, with the dimension of silicon devices being scaled, various short channel effects and quantum effects have gained significance, which degrade the performance and increase the complexity of fabrication. Thus, 2D materials are studied as a potential substitution of silicon in large scale integrated circuit and lots of efforts have been made on the use of 2D materials in logic and memory circuits. In this chapter, we will take a look at the basic component of which integrated logic and memory circuits consist, logic inverter [91] and 1T or 2T dynamic random access memories (DRAM) [92]. In our experiments, local back gate process was used in the fabrication of MoS_2 and BP MOSFETs in order to boost the performance of devices and enable the larger scale integration. Therefore, the fabrication flow of a logic inverter will be reviewed. The DC measurement results of the devices composing the inverter will be shown and discussed followed by the DC and AC characteristics of the 4-terminal inverter. Next, the fabrication and measurements of 1T/1C and 2T DRAM cells will be introduced.

3.1 Fabrication of logic inverter

The results from the last chapter paved the way for fabrication of symmetric complementary circuits using MoS_2 n-MOSFETs and BP p-MOSFETs. Using similar

techniques and device structures, it was able to create a single inverter which is a true four-terminal device consisting of IN, OUT, V_{DD} and GND. The device schematic illustration is shown in Fig. 3-1.
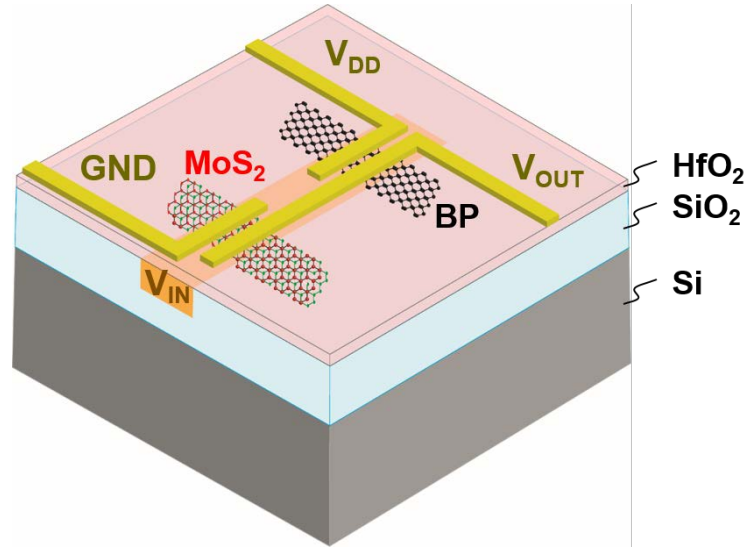
Figure 3-1 Schematic illustration of the integrated BP p-MOSFET and MoS$_2$ n-MOSFET. The devices are fabricated using a common buried gate electrode with thin HfO$_2$ gate dielectric.

Similar to the discrete devices, the device fabrication started by using a bulk silicon wafer upon which a 110-nm-thick SiO_2 film was grown using dry thermal oxidation. After forming alignment marks, local 2-μm-wide gate electrodes were patterned with EBL. The gate finger was designed longer than stand-alone devices for the ease of transferring multiple flakes. The same combination of dry and wet etching was used to recess the SiO_2 before evaporating and lifting off Ti/Pd (10/40 nm) to form a quasi-planarized gate contact. At 300 °C, 20 nm of HfO_2 was deposited using ALD. A MoS_2 flake was transferred onto the gate finger first since MoS_2 is air stable. Following this step, a BP flake whose thickness is approximately same as the MoS_2 flake was transferred. Since the current level driven by the BP transistor is close to that of the MoS_2

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transistor, this criterion can ensure the matching between the complementary FETs. Since it is the normalized drive current of both devices which are close, comparable widths are also required. In our inverter, the width of the n-MOSFET is 10 μm and the width of the p-MOSFET is 16 μm, as shown in Fig. 3-2 (a). Since extra lithography process is necessary for narrowing either flake, the increase of exposure time of the sample to air is inevitable. Moreover, this process increases the risk of losing the flakes during the solvent spraying. Thus, the flakes were kept as transferred. Next, source and drain openings of both transistors were defined with EBL again. The evaporation and lift-off of the metallization are performed as the last step in completing the fabrication. As shown in Fig. 3-1, a shared drain finger is used for both FETs which served as the *OUT* terminal, and the shared local backgate served as the *IN* terminal. The source contacts of the MoS_2 n-MOSFET and the BP p-MOSFET served as the ground (GND) and supply (V_{DD}) terminals of the inverter, respectively. An optical picture of the completed circuit is shown in Fig. 3-2 (b).
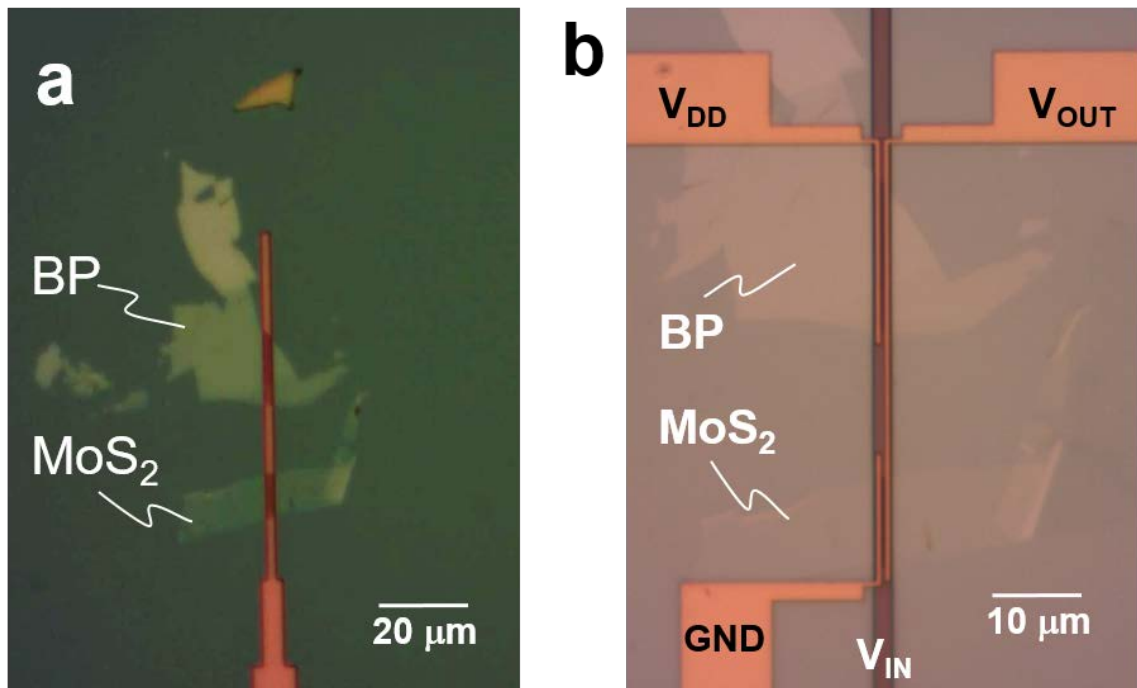
Figure 3-2 Optical micrographs of the inverter (a) before deposition of the final contact layer. (b) after the HfO$_2$ passivation on the completed circuit.

3.2 DC measurement results of circuits

In the device fabrication, multi-layer MoS$_2$ and BP were used as the channel materials, to ensure the performance through drawing enough drive current. In 2D material MOSFETs, drive current increases as the channel thickness and so in order to build a good match between the n- and p-MOSFET, it is ideal to have the MoS$_2$ and BP flakes have comparable thicknesses. In the device fabrication, the flake thickness was approximated with contrast identification, but this only serves as a rough guide. As argued in Chapter 1, the best methodology to test the thickness of 2D films is SPM. In this experiment, atomic force microscopy (AFM) was used to characterize the thickness of both flakes. The scanned pictures are shown in Fig. 3-3. AFM results have proved the

thicknesses of the MoS_2 flake and the BP flake are both ~8 nm, which means due to similar current density, good match up should exist between the transistors.
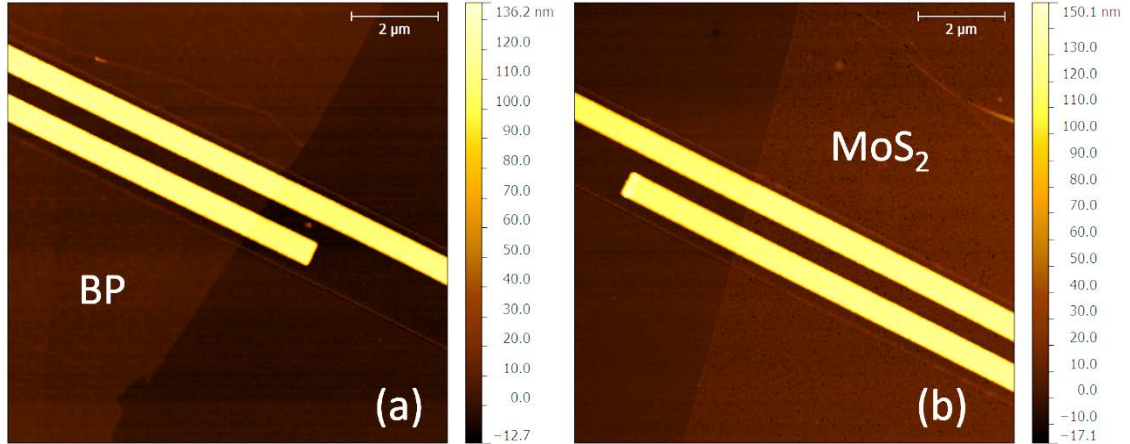
Figure 3-3 micrographs taken under AFM on the inverter in the (a) BP p-MOSFET area and (b) MoS_2 n-MOSFET area

As shown in the device schematic, all the four terminals of the inverter (V_{DD}, GND, V_{IN}, V_{OUT}) are accessible to device parameter analyzers via a probe station. Therefore, the inverter can be measured as two separate transistors or one integrated circuit. As unpassivated BP channel was used, the devices were still measured with an Agilent B1500A semiconductor parameter analyzer in the dark using a cryogenic vacuum probe station at a pressure of $< 10^{-5}$ Torr. The initial measurements were carried out at room temperature. In the previous chapter, device information was extracted from those stand-alone devices. However, the variance between devices can be great enough to impact on the performance or even the functionality of the circuit. Thus, characterization was performed on the cell as separate transistors to begin with. Similar to the stand-alone device measurement, the current vs. voltage characteristics were measured and the results are plotted in Fig. 3-4. In Fig. 3-4 (a) and (b), the drain current, I_D of the MoS_2 n-

MOSFET (BP p-MOSFET) is plotted vs. the drain-to-source voltage, V_{DS}, for terminal voltages between 0 and +2.5 V (0 and -2.5 V). For both plots in (a) and (b), $|V_{DS}|$ was swept from 0 to 2.5 V and the maximum value of the absolute gate-to-source voltage, $|V_{GS}|$, was 2.5 V with a step of 0.2 V and I_D was normalized by the widths of the individual devices. The absolute normalized saturated drive currents for the n- and p-MOSFETs are both ~50 µA/µm, owing to the same channel thicknesses, showing good match-up between the width-scaled pull-up and pull-down transistors. In Fig. 3-4 (a), the device exhibits nonlinear turn-on behavior, which is mainly due to the Schottky barrier at the contacts. Transfer characteristics were also measured for both devices and the results are plotted in the (c-d) part of Fig. 3-4. For the characteristics in (c) and (d), the values of $|V_{DS}|$ are 0.1 V and 1.5 V and V_{GS} was swept from -1.5 V to +1.5 V. The voltage drop between terminals was limited in order to prevent breakdown from high electric field. Both directions of the gate voltage sweep are shown. The linear threshold voltages for n- and p-MOSFETs are approximately -0.8 V and +0.8 V, respectively, which are highly symmetric while they are both in slightly depletion mode. Note the $|V_{DS}|$ applied here is less than $|V_{GS}-V_T|$, and the linear model of drain current of the n-MOSFET can be described as:

$$I_D = \mu_{eff} C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{DS},$$

(3.1)

Where μ_{eff} represents the field effect mobility of the n-MOSFET channel material, C_{ox} stands for the gate oxide capacitance, and W and L are the width and length of the n-MOSFET channel area. Thus, the field effect mobility can be extracted as:

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$$\mu_{eff} = \left| \frac{I_D L}{C_{ox} W (V_{GS} - V_T) V_{DS}} \right|,$$

(3.2).

Here, C_{ox} is the gate oxide capacitance per unit area given by:

$$C_{ox} = \frac{\varepsilon_{OX}}{t_{OX}},$$

(3.3).

The field effect mobility of the BP p-MOSFET can be extracted using (3.2). From these calculations, the field effect electron and hole mobilities of MoS_2 and BP are found to be 4.5 cm^2/Vs and 21 cm^2/Vs, where it is noted that the contact resistance was not subtracted from the measurements. In Fig. 3-4 (c), an on-to-off ratio of $>10^8$ was observed for the MoS_2 n-MOSFET along with a near ideal subthreshold slope of 70 mV/decade (73 mV/decade) at $V_{DS} = +0.1$ V (+1.5 V). An on-off ratio of $> 10^3$ was also seen for the BP p-MOSFET. Thanks to the high mobility of BP, the peak saturated g_m of BP, which is 41 µS/µm at $V_{DS} = -1.5$ V, is higher than that of the MoS_2 n-MOSFET, which is 16 µS/µm at $V_{DS} = -1.5$ V. These results are consistent with the results on the stand-alone devices, indicating a repeatable fabrication process. Though the interface quality between the exfoliated MoS_2 and HfO_2 is still high, the larger hysteresis from the p-MOSFET transfer characteristics indicates possible trapped moisture beneath the BP flake.
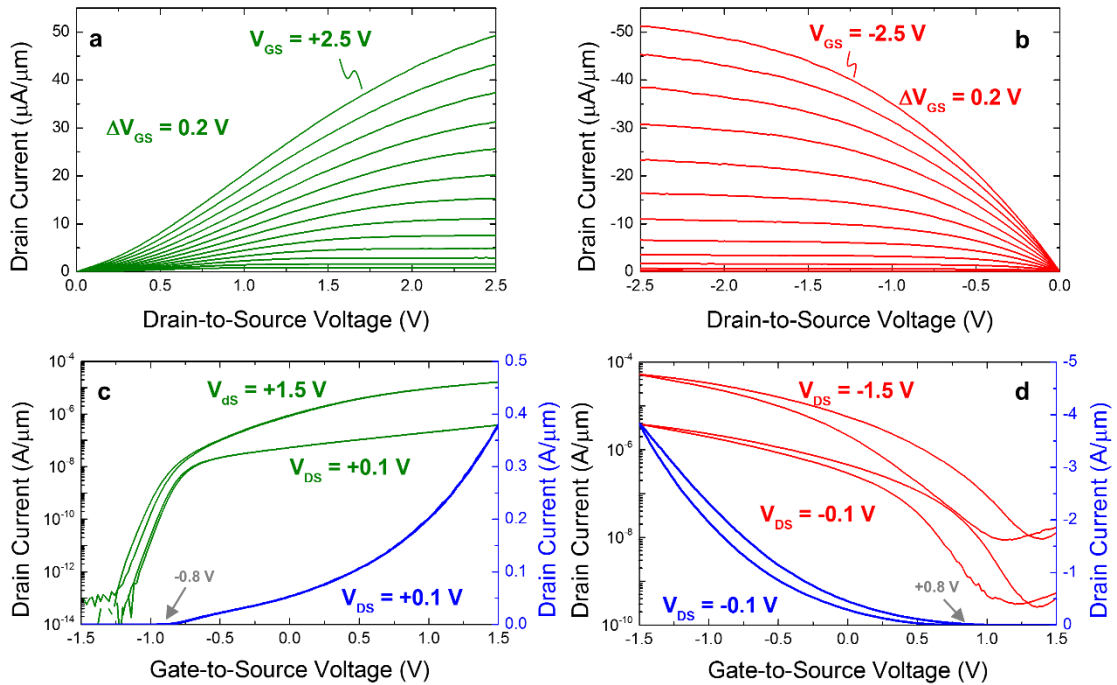
Figure 3-4 Characteristics of the individual devices of the logic inverter. (a) Drain current, I_D, vs. drain-to-source voltage, V_{DS}, characteristic for MoS$_2$ n-MOSFET. (b) I_D vs. V_{DS} characteristic for (BP) p-MOSFET. (c) I_D vs. V_{GS} characteristic of the MoS$_2$ n-MOSFET on both a semi-log (green) and linear (blue) scale. (d) I_D vs. V_{GS} characteristic of the BP p-MOSFET on both a semi-log (red) and linear (blue) scale. $|V_{DS}|$ was swept from 0 V to 2.5 V in (a) and (b). $|V_{GS}|$ was biased from 0 V to 2.5 V at a step of 0.2 V. In (c) and (d), $|V_{GS}|$ was swept from -1.5 V to 1.5 V. $|V_{DS}|$ was biased at 0.1 V and 1.5 V.

Fig. 3-5 shows the load line analysis of the inverter, where the individual I_D vs. V_{DS} characteristics from Fig. 3-4 (a) and 3-4 (b) are utilized. The solid lines indicate the MoS$_2$ n-MOSFET characteristics, while the dashed lines show the BP p-MOSFET curves where the V_{DS} value has been inverted along the x-axis. The crossing points of the characteristics are indicated by the solid dots and these indicate the quiescent operating point of the inverter. The gate voltage values are 0.1 V (grey), 0.7 V (gold), 1.1 V (magenta), 1.3 V (cyan), 1.5 V (blue), 1.7 V (green), 1.9 V (red), 2.3 V (black) for the n-MOSFET, while the p-MOSFET gate voltages are the difference between the n-MOSFET

values and V_{DD} (2.5 V). Because the devices have relatively low threshold voltages, the load lines overlap at high current levels. Of course, despite the fact that the width-scaled drive currents are well-matched between the transistors, the BP p-MOSFET has significantly larger width than the MoS$_2$ n-MOSFET and therefore the pFET is significantly stronger than the nFET in our inverters. These plots are shown both on a log scale (Fig. 3-5 (a)) and linear scale (Fig. 3-5 (b)) where the quiescent operating points at each value of gate bias are indicated by the circles. These plots show several important aspects of the inverter operation. First, the log-scale plot shows that the on-to-off current ratio is roughly 1-2 orders of magnitude and is limited by the low threshold voltage of the MoS$_2$ n-MOSFET when the output is high and by the onset of gate-induced drain leakage (GIDL) in the BP p-MOSFET when the output is low. The plot in Fig. 3-5 (b) further shows that the n-MOSFET drain voltage quickly approaches 2.5 V as the n-MOSFET gate voltage approaches 0, due to the low ON resistance of the BP p-MOSFET. However, the transition of the n-MOSFET drain voltage toward 0 is less abrupt due to its somewhat non-linear turn on.
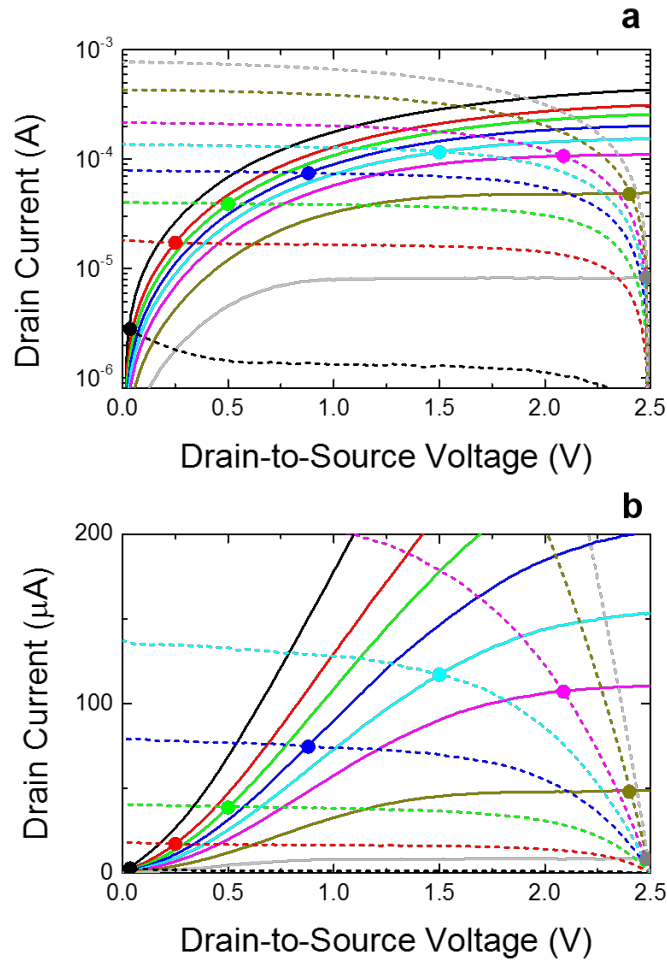
Figure 3-5 Load-line analysis of the logic inverter shown in (a) a log scale and (b) a linear scale for $V_{DD} = 2.5$ V.

In addition to the measurements of the individual devices, the cell was characterized as a 4-terminal logic inverter. In all measurements plotted in Fig. 3-6, the common gate electrode was biased at an input voltage, V_{IN}, the shared drain contact was monitored as the output voltage, V_{OUT}, and the source contact of the BP p-MOSFET was biased at a fixed value of V_{DD}. Finally, all voltages were referred against the MoS$_2$ n-MOSFET source terminal voltage which was held at zero voltage source and is labeled

GND in Fig. 3-1. The inverter was tested at supply voltages ranging from $V_{DD} = 0.25$ V to 2.5 V, in steps of 0.25 V. At each V_{DD} value, V_{OUT} and the inverter current were measured versus V_{IN} between 0 V to V_{DD}. The measurement results are plotted in Fig. 3-6. In the (a) part of Fig. 3-6, the output voltages are plotted versus the input voltages at different supply voltages and the voltage inversion was demonstrated at all supply voltages. The solid symbols indicate values of $V_{IN} < V_{DD}$, while the open symbols show points where $V_{IN} > V_{DD}$. In the meantime, the voltage gains were extracted and plotted in Fig. 3-6 (b). The gain is given by

$$G = \frac{\partial V_{OUT}}{\partial V_{IN}}.$$ (3.4)
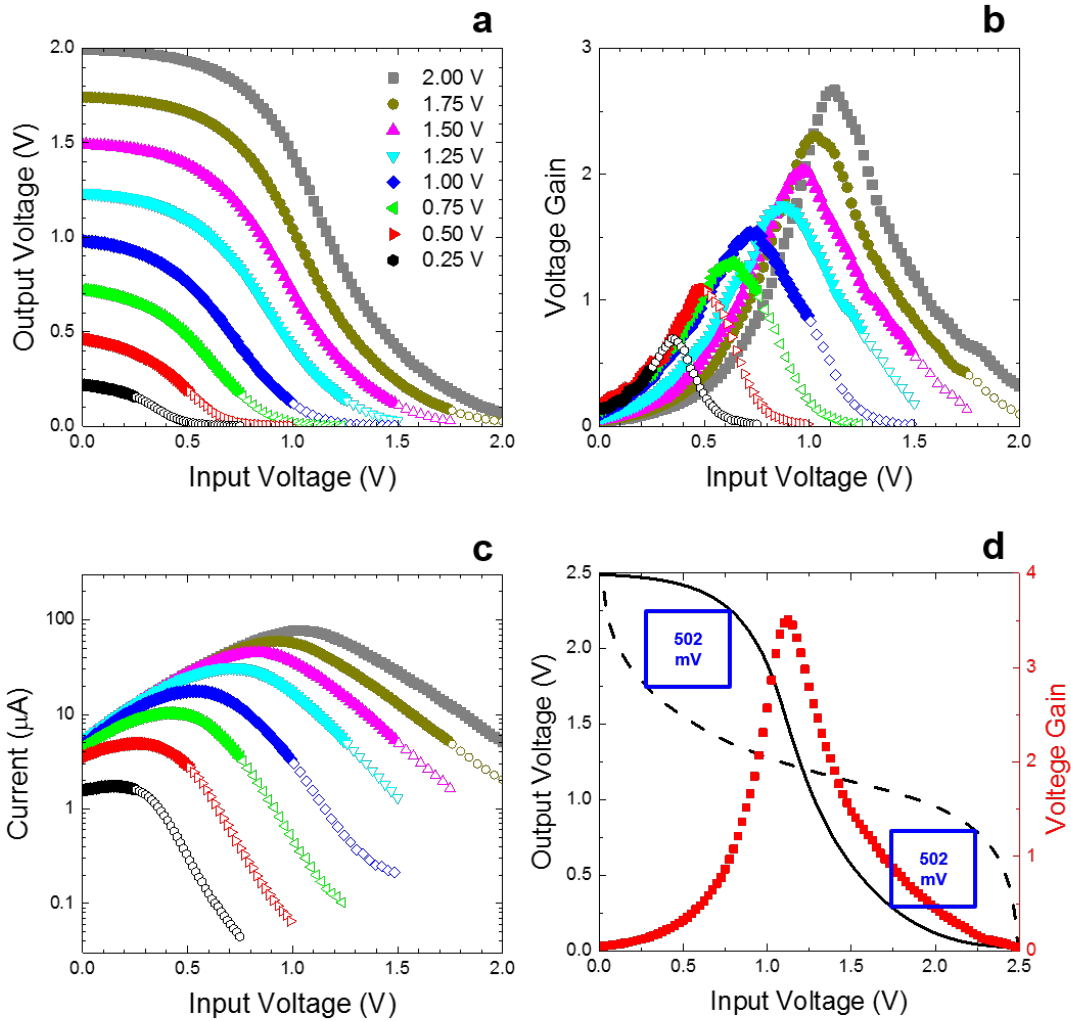
Figure 3-6 Results of measurements on integrated BP p-MOSFET / MoS$_2$ n-MOSFET logic inverter. (a) Output voltage, V_{OUT}, as a function of the input voltage, V_{IN}, at supply voltages, V_{DD}, ranging from 0.25 V to 2.0 V. (b) Voltage gain and (c) current vs. V_{IN} for V_{DD} = 0.25 V to 2.0 V, where the symbol designations are the same as in (a). (d) Inverter V_{OUT} (solid black line) and gain (red symbols) vs. V_{IN} for inverter at V_{DD} = 2.5 V.

The peak gain, G_{peak}, has the value greater than 1 when $V_{DD} \geq 0.5$ V, while $G_{peak} > 2.5$ at V_{DD} = 2.0 V. A key feature of the gain characteristics is that the inversion and voltage gain are achieved in a symmetric input-output voltage window. I_D vs. V_{IN} is shown in Fig.

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3-6 (c), where a peak of driven current can be observed at all supply voltages, demonstrating the complementary nature of the circuit operation. The peaks of the drive currents have values of micron amperes, which means the devices are working in the saturation region, allowing the circuit to work at high frequencies. Finally, in Fig. 3-6 (d), the input-output and gain characteristics at $V_{DD} = 2.5$ V are plotted where the extracted noise margin has been extracted by creating a butterfly curve from the inverted input-output curve. The dashed black curve shows V_{IN} vs. V_{OUT}, and the blue squares indicate the static noise margin of the inverter which is found to be > 500 mV. This plot shows that the peak gain occurs at $V_{IN} = 1.2$ V, which is very close to the half the supply voltage of 2.5 V. The devices also have excellent noise margin, with a value of 502 mV extracted from the open area of the butterfly curve as shown in Fig. 3-6 (d). These results indicate that our hybrid BP/MoS$_2$ inverters are capable of driving subsequent inverter stages.

The V_{DD}-dependence of the inverter operation is summarized in Fig. 3-7. As shown in Fig. 3-7 (a), G_{peak} increases from 1.1 to 3.5 going from $V_{DD} = 0.5$ to 2.5 V, while the max-to-main current ratio (Fig. 3-7 (b)) also increases with increasing V_{DD}, where the minimum current is determined from the average current between $V_{DD} = 0$ and 2.5 V. The delayed onset of the increase is due to the slightly non-linear turn-on of the MoS$_2$ n-MOSFET. Finally, the static noise margin vs. V_{DD} is plotted in Fig. 3-7 (c), where it can be seen that open butterfly characteristics are observed down to $V_{DD} = 1$ V. Once again, reducing the on resistance of the n-MOSFET should allow inverter operation to even lower supply voltages.
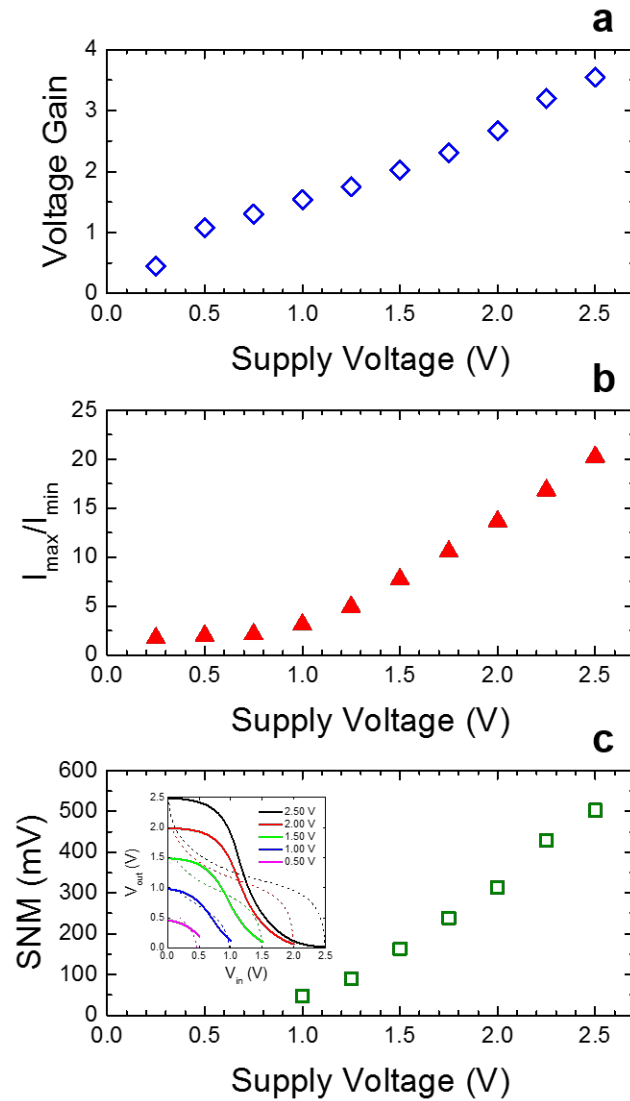
Figure 3-7 Dependence of room-temperature inverter characteristics on supply voltage, V_{DD}. (a) Maximum voltage gain of the inverter vs. V_{DD} for conditions where $V_{IN} < V_{DD}$. (b) Ratio of maximum to minimum inverter current vs. V_{DD}. (c) Static noise margin (SNM) vs. V_{DD} where the SNM value is extracted using the butterfly curve method. Inset: butterfly curves for $V_{DD} = 0.50$ to 2.5 V. Open butterfly characteristics are observed down to $V_{DD} = 1$ V.

In order to evaluate the performance of the inverter in a realistic very-large-scale integration (VLSI) chip, the temperature dependence of the integrated inverter circuit was studied as a function of temperature which was varied between 270 K and 340 K. The

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temperature-dependent measurements were performed with liquid nitrogen cooling and a heated stage feedback loop to stabilize the temperature. Fig. 3-8 (a) shows the in/out characteristics of the inverter, in which V_{OUT} is plotted vs. V_{IN} with a supply voltage of 2.5 V, while the gain and drive current vs. V_{IN} for the same temperatures are shown in Fig. 3-8 (b) and 3-8 (c). The voltage gain is found to be virtually constant with temperature, and only a small decrease in the voltage of the peak gain characteristics is found with increasing temperature. The on-to-off current ratio does decrease somewhat with increasing temperature and this is due to an increase in the gate-induced drain leakage of the BP p-MOSFET. Finally, it can be observed that when the input is high, the low output voltage tends to deviate from zero with higher temperature. This is also due to the off-state current flow in the p-MOSFET, which directly leads a non-zero voltage drop across the n-MOSFET, preventing the output low from reaching 0 V. Note that when the temperature is higher than 340 K, due to the narrow gap of BP, the device can hardly be turned off. Thus, the pFET of the inverter works as a load resistor and the output of the inverter cannot be pulled down.
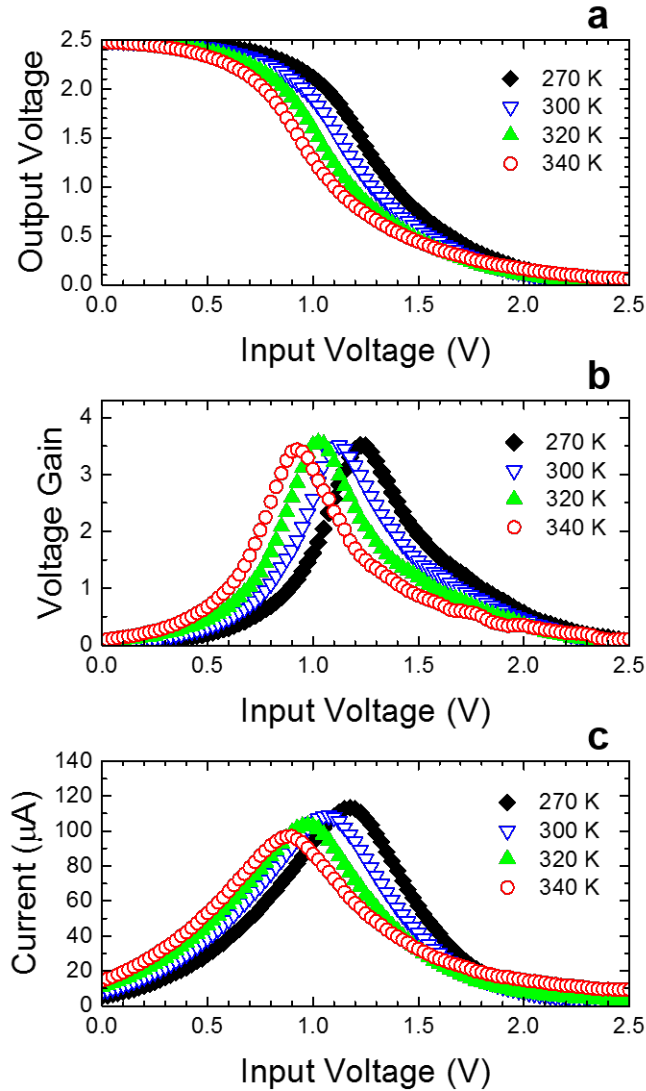
Figure 3-8 Temperature dependence of the inverter characteristics for temperatures ranging from 270 K to 340 K. (a) Temperature dependence of the V_{OUT} vs. V_{IN} characteristics. (b) Temperature dependence of voltage gain vs. V_{IN} characteristics. (c) Temperature dependence of the inverter current vs. V_{IN}. For all measurements, the supply voltage, V_{DD}, is 2.5 V.

In summary, a complementary logic inverter fully based on integrated MoS$_2$ n-MOSFETs and BP p-MOSFETs was demonstrated and characterized. The results show that these devices are capable of reasonably symmetric performance, in that the current

drive and threshold voltages are well matched, without the use of external control gates for threshold adjustment. In addition, the circuit performance is achieved using a common gate metal, dielectric and contact metallization, which could help to streamline future CMOS integration. In addition, while the exfoliation technique is not necessarily an extendable process, the results do show that the process of forming gate electrodes and subsequent transfer of the 2D material onto the pre-patterned substrate can result in high-performance devices and this work could help to spur development of techniques to transfer CVD material for more complex circuit operation.

It is clear that numerous improvements in the performance are possible with design optimization. In particular, while the threshold voltages are matched in our devices, they operate slightly in depletion mode, resulting in relatively high off-state leakage in our inverter. Thinning of the dielectric is likely to increase the threshold voltage in both devices. In addition, thinning the black phosphorus channel of the p-MOSFET should also help to improve the off-state leakage, since the increased band gap should have the effect of shifting the threshold voltage negative, as well as reducing the GIDL current. Improved matching could also be achieved by using a mesa etch to adjust the relative sizes of the MoS_2 and BP transistors.

3.3 Transient measurement of logic inverter

Considering the fact that the logic inverter is most worthwhile being integrated in large scale circuits, such as arithmetic logic units or SRAM units which work at high frequencies, and the DRAM cells are usually operated in dynamic environments, it is necessary to evaluate the response of the circuits to transient signals.

AC measurements on the inverter were performed using a two-channel Keysight 33500B function generator, where one channel was used to supply the square wave or sinusoidal input waveform, while the other was used to provide the constant DC supply voltage. Both the input and output waveform data were monitored with a four-channel Keysight 3014C digital oscilloscope. All the testing channels and the circuit shared a same ground terminal. Here, the function generator was connected between the input gate
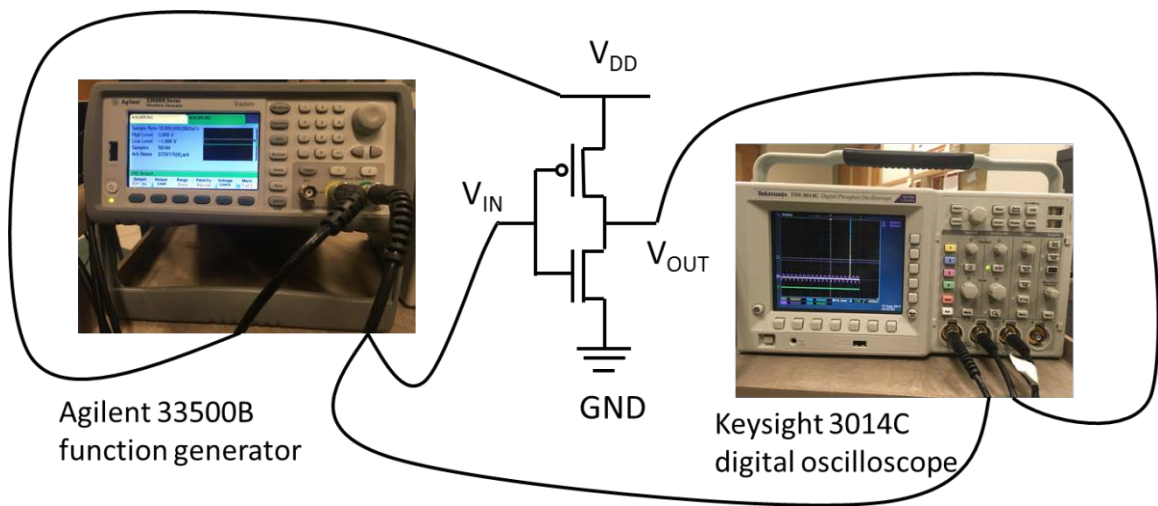
Figure 3-9 Set-up of the AC measurement of the inverter. One channel of the function generator was used to supply the square wave or sinusoidal input waveform, while the other was used to provide the constant DC supply voltage.

electrode and ground and the resulting output signal between the shared drain terminal and ground was monitored using the digital oscilloscope. The measurement setup is as shown in Fig. 3-9.

The results of AC measurements on the inverter are plotted in Fig. 3-10. Fig. 3-10 (a) and 3-10 (b) show V_{IN} and V_{OUT} vs. time at $V_{DD} = 2.5$ V, were $f = 1$ kHz and 100 kHz, for Fig. 3-10 (a) and 3-10 (b), respectively. For the input waveforms, a correction was applied to the data to account for a zero offset in the oscilloscope calibration. The supply

voltage, $V_{DD} = 2.5$ V and V_{IN} was a square wave with minimum and maximum values of 0 and V_{DD}. The results show good logic operation up to 100 kHz, with the speed limited by parasitic capacitances and inductances associated with the vacuum probe station, with much higher speeds expected as will be described below. Small signal analysis was also performed on the devices and the results are shown in Fig. 3-10 (c) and 3-10 (d). Here, a sine-wave input was applied to the input terminals and the small-signal voltage gain, G_{AC} was measured. In Fig. 3-10 (c), G_{AC} is plotted vs. the DC offset voltage, V_{IN-DC}, for different values of V_{DD} ranging from 1 V to 2.5 V at a frequency of 1 kHz. Compared to the DC characteristics performed at the same conditions, the peak AC gain was found to be larger, and this difference could be due to slow trapping effects in the gate dielectric, particularly in the BP p-MOSFET, as evidenced by the hysteretic behavior evident in Fig. 3-4 (d). Fig. 3-10 (d) shows a plot of G_{AC} vs. frequency at $V_{DD} = 2.5$ V, there V_{IN-DC} was adjusted to be at the peak gain condition. The gain roll-off occurs as expected with unity voltage gain reached at $f = 100$ kHz.
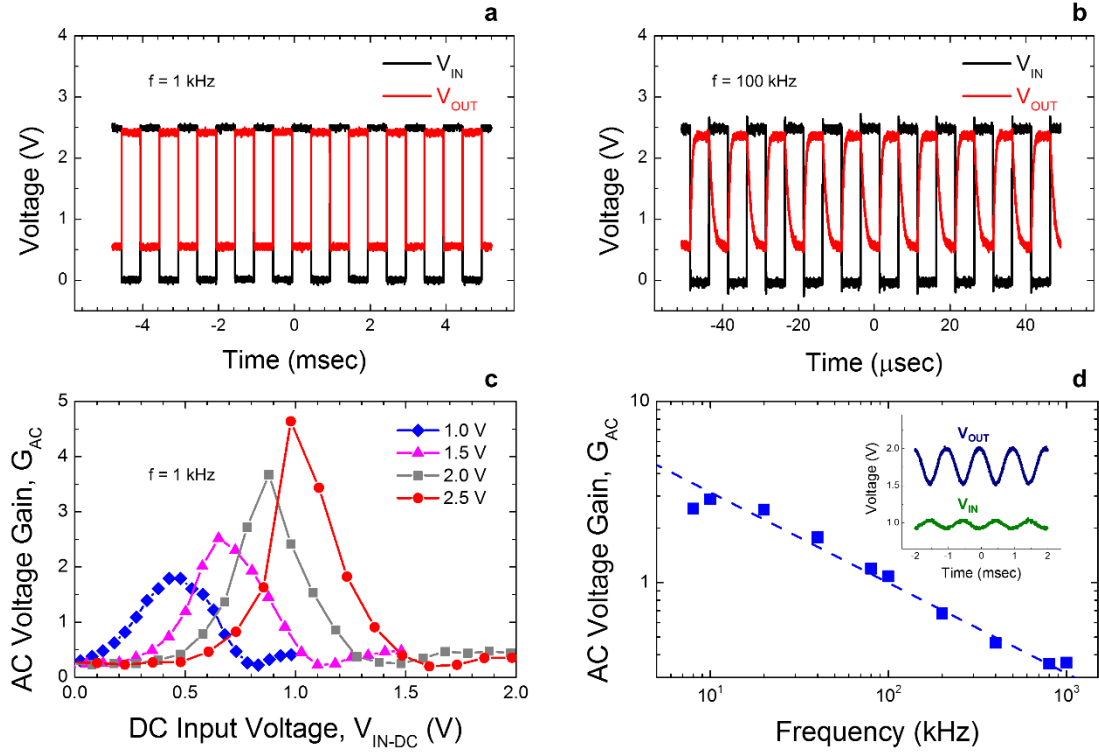
Figure 3-10 Digital and small-signal AC performance of inverter circuit. (a) Plot of input voltage, V_{IN}, and output voltage, V_{OUT} vs. time at a frequency, f = 1 kHz for inverter circuit. (b) Same device as in (a) at f = 100 kHz. (c) Plot of small signal AC voltage gain, G_{AC}, vs. DC input voltage, V_{IN-DC} at V_{DD} = 1.0 V (blue), 1.5 V (magenta), 2.0 V (grey) and 2.5 V (red). The input oscillator had a peak-to-peak voltage of 0.1 V and f = 1 kHz. (d) Plot of G_{AC} vs. f at V_{DD} = 2.5 V, where the device is biased near the peak gain point. The cutoff frequency is ~ 100 kHz, where the speed is dominated by parasitic capacitances associated with the test setup. Inset: Plot of V_{IN} (green) and V_{OUT} (blue) vs. time at f = 1 kHz.

Improved performance can be achieved by eliminated parasitic elements. The intrinsic speed of the devices should be much faster than the current 100 kHz performance, which is attributed to test setup capacitances and inductances as well as substrate coupling of the large probe pads. The intrinsic delay can be calculated as follows. The total capacitance, C_{tot}, of the combined circuit is calculated as:

$$C_{tot} = \frac{LW\varepsilon_{OX}\varepsilon_0}{t_{ox}}, \tag{3.5}$$

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where L = 2 μm is the total length of the gate electrode, W = 26 μm is the combined width of the p- and n-MOSFETs, ε_{OX} = 16.6 is the dielectric constant of our ALD HfO$_2$ as determined from reference [93], t_{ox} = 20 nm and ε_0 is the permittivity of free space. These parameters produce a value of C_{tot} = 0.38 pF. Given the peak drive current, I_{peak}, of 108 μA at V_{DD} = 2.5 V, the intrinsic delay, τ, can be calculated as

$$\tau = \frac{C_{tot}V_{DD}}{I_{peak}} = 8.8ns,$$

(3.6)

corresponding to a maximum frequency of 18 MHz.

Additional challenges that need to be addressed in order to improve the performance include improving the contact resistance, scaling the dielectric thickness and minimizing parasitic capacitance. From Fig. 3-4, the contact resistance is very high, particularly in the MoS$_2$ device, and so reducing resistance arising from the Schottky contacts will be a key component in further enhancing the performance, particular at low supply voltages. Much more aggressive gate dielectric scaling should also be possible, particularly since 2D transistors with 4-nm HfO$_2$ have already been demonstrated in our experiments. In addition to allowing aggressive gate length scaling, dielectric scaling should also improve transmission coefficient of the contacts by increasing the electric field at the metal-semiconductor interface. Finally, utilization of a self-aligned geometry will be important in the future to minimize overlap capacitance between the gate and channel.

Finally, it should be noted that some degradation in the device performance was observed over the course of the measurements. In particular, for the AC data in Fig. 3-10, which was taken several weeks after the DC results, it was found that the low input

voltage was observed to be higher than in the DC shown in Fig. 3-4. It is believed that this degradation is due to an increase in the GIDL current of the BP p-MOSFET, and is attributed to intermittent exposure to atmosphere between the DC and AC measurements. These results show that efficient passivation techniques will be needed for stable circuit operation, and the effect of passivation on the threshold voltages and current matching will be important aspects of future optimization.

3.4   Fabrication of DRAM cells

In the second chapter, we have talked about the high-performance and scalability of MoS_2 devices, which make it attractive in logic circuits. However, there is another aspect of MoS_2 devices that should not be overlooked, their potential for extremely low leakage operation. Due to its large band gap, ultra-thin channel, and high effective mass, short channel effects (SCEs) and gate induced drain leakage (GIDL) are expected to be substantially suppressed compared to silicon, making MoS_2 suitable for extremely-low leakage static and dynamic memories. In last chapter, leakage current less than 10^{-14} A/μm has been reported, indicating that MoS_2 MOSFET is promising in dynamic memory applications.

In our work, two types of DRAMs were fabricated, namely the one transistor/ one capacitor (1T/1C) and the two transistor (2T) configurations were fabricated. The schematic of the devices is shown in the following Fig. 3-11.
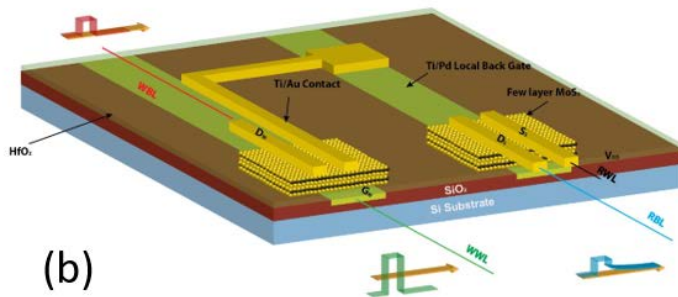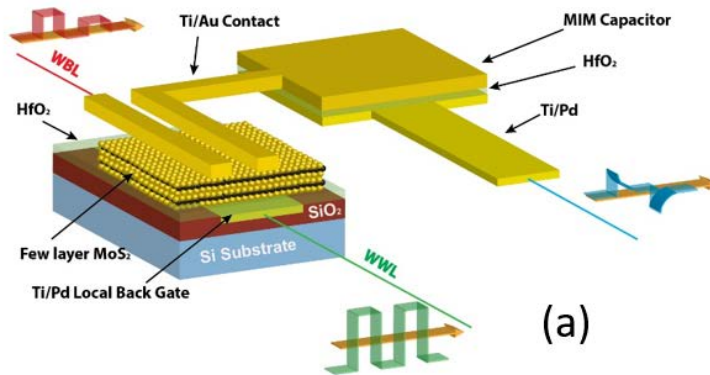
Figure 3-11 Schematic illustration and the terminal nomination of the (a) 1T/1C memory cell and (b) 2T memory cell.

The fabrication process for both devices started with the same substrate, ~110 nm dry SiO_2 thermally grown on top of Si wafer. Ti/Au alignment marks were then patterned with EBL and metallized with E-beam evaporator. Identical combination of dry etch and wet etch was used to create the gate electrode recess patterned by EBL and Ti/Pd was evaporated into the recessed region followed by lift off. Also, 20nm HfO_2 grown by ALD at 300°C served at gate dielectric. Up till this step, 1T/1C cell and the 2T cell share the same process flow, and they differ in the following steps. In the 1T/1C cell fabrication, the bottom plate of the capacitor was patterned and fabricated simultaneously with the

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gate electrode of the transistor. Next, selected MoS_2 flake was aligned transferred onto the gate finger of the transistor and EBL was used to pattern the source/drain contacts, the top plate of the capacitor and wire connection between them. Finally, Ti/Au was evaporated to metalize the contacts with lift-off. The 2T cell fabrication was more complicated since the source terminal of the read transistor and the gate contact of the storage capacitor need to be connected while they are on different metal levels. Thus, via openings need to be made through the HfO_2 gate dielectric layer. In our lab, wet etch is not viable for HfO_2 and the selectivity between EBL resist and HfO_2 is less than 0.01 with plasma etch. Thus, a hard mask process was developed and described in the appendix. Mechanical exfoliation was used to transfer MoS_2 flakes onto the gate electrode of the read transistor and the storage transistor, one for each. The source, drain and wire contacts were then finished by depositing Ti/Au with EBL patterning and Ebeam evaporation. Optical micrographs are shown in Fig. 3-12 for the 1T/1C and 2T cells. In both cells, all the flakes have thicknesses between 6~10 nm and all the devices had a source-to-drain spacing, L_{eff}, of 500nm.
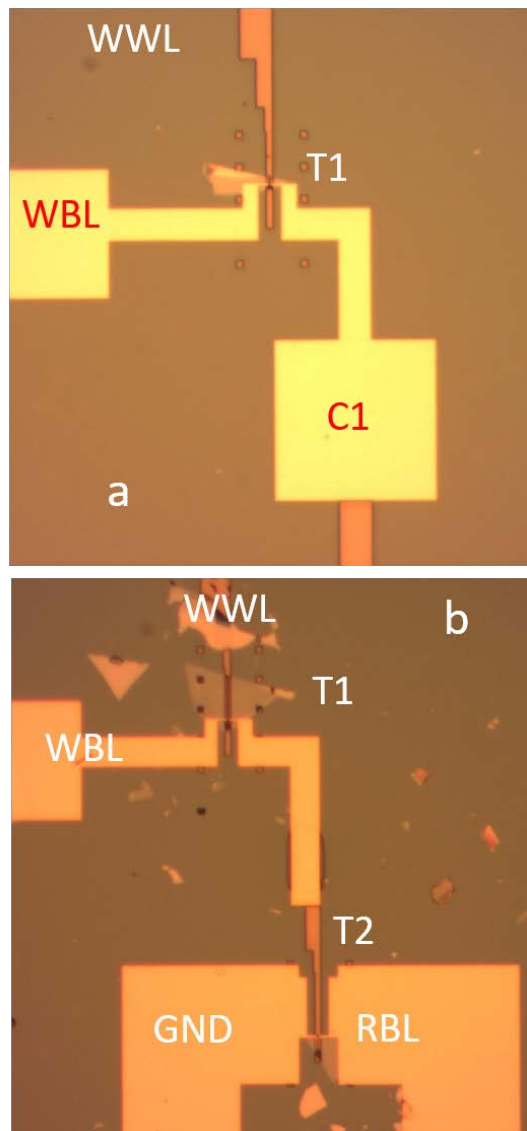
Figure 3-12 Optical micrographs of the (a) 1T/1C memory cell and (b) 2T memory cell.

3.5 Pulsed measurement of DRAM cells

For the DRAM cells, AC measurements were performed using a two-channel Keysight 33522B function generator, where two channels were used to supply the square wave input waveform for word and bit lines. Both the input and output waveform data were monitored with a two-channel Keysight 3014C digital oscilloscope. Both function

generator and oscilloscope were controlled via GPIB port. Matlab and python code was utilized to generate appropriate waveforms, and command / control the measurements respectively. All the testing channels and the circuit shared a same ground terminal.

Initial retention time characterization was performed using a 1T/1C circuit configuration. The pulse sequence can be seen in the oscilloscope traces shown in Fig. 3-13 (a) and 3-13 (b). For the measurements shown in Fig. 3-13 (a), a short interval time of 50 μsec was investigated. For this sequence, a "1" was written during the write cycle and then the value read out during the read cycle. Because of the short time interval, the charge is retained on the capacitor, and therefore, when 0.5 V is applied to the bit line, the capacitor discharges leading to a negative current flow "spike". Here, the current is read out as the voltage across a 20 kΩ resistor placed between the storage capacitor and ground. The situation for a long interval time (~ 1 second) is shown in Fig. 3-13 (b). In this case, the subthreshold leakage causes the charge to leak off of the storage node, leading to a loss of the stored data. Therefore, the voltage across the capacitor drops below the applied voltage of 0.5 V on the bit line during the read operation. This means the current will flow during read will no reverse sign, but instead be the same sign as the original write "1". In this way, the retention time of the 1T/1C cell can be determined. A similar technique can be utilized for the write "0" operation. However, the write "1" situation is more useful for determining the retention time. For a hold voltage value of V_{HOLD} = -1.5 V, a retention time of 251 msec was obtained. The leakage current is observed to decrease to as low as 3 pA/μm at V_{HOLD} = -1.5 V [92].
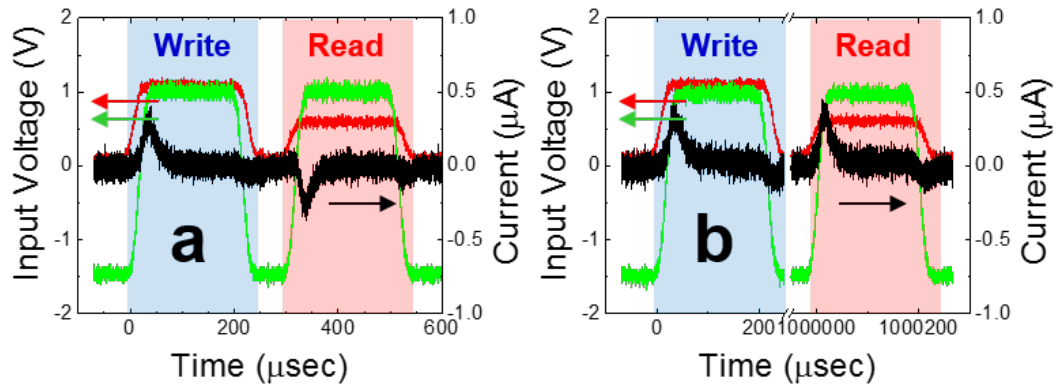
Figure 3-13 1T/1C memory cell AC measurement results. (a) Example of memory operation using a hold time of 50 µs. The bit line pulse is red, the world line pulse is green and the output current is shown in black. The sign of the current is opposite during the read pulse compared to the write pulse, indicating that the charge has been retained. (b) Same measurement sequence as in (a), except for a hold time of 1 s. Here, the readout current has the same sign as the current during the write pulse, indicating charge has been lost.

The 2T cell operates as follows: when the read transistor (write transistor) is turned on, data is written onto the gate of the storage transistor, where this gate performs the same function as the MIM capacitor in the 1T/1C cell. However, in this cell, the charge stored on the gate of the storage transistor changes its conductance, and so the memory state can be read out simply by measuring the current through the storage transistor. This type of cell is typically referred to as a "gain cell" since the charge stored on the gate electrode is amplified by the transistor. The gain cell also separates the read and write functions allowing non-destructive readout.

In our initial set of measurements, synchronized pulses were applied to the bit line and word line, and then the resulting change in current through the storage transistor was observed by measurement the voltage across a 20 kΩ resistor which was connected in series with the read transistor. The retention time measurement results are shown in Fig. 3-14 (a), where the current is plotted vs. time on a log scale for V_{HOLD} = -1 to -1.6 V. For

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these measurements, the 2T retention time was considered, τ_2, to be the time required for the current to drop to 50 % of its original value at the end of the write pulse. This retention time changes based on the value of the hold voltage, V_{HOLD}, applied to the gate of transistor write transistor, as shown in Fig. 3-14 (b). Finally, based upon this extraction method, the leakage current of the write transistor vs. V_{HOLD} was determined and these results are shown in Fig. 3-14 (c). The minimum leakage current is found to be on the order of ~ 1 fA/µm, though lower values of V_{HOLD} could not be probed, once again due to the due to limitations of the synchronous measurement technique [92].
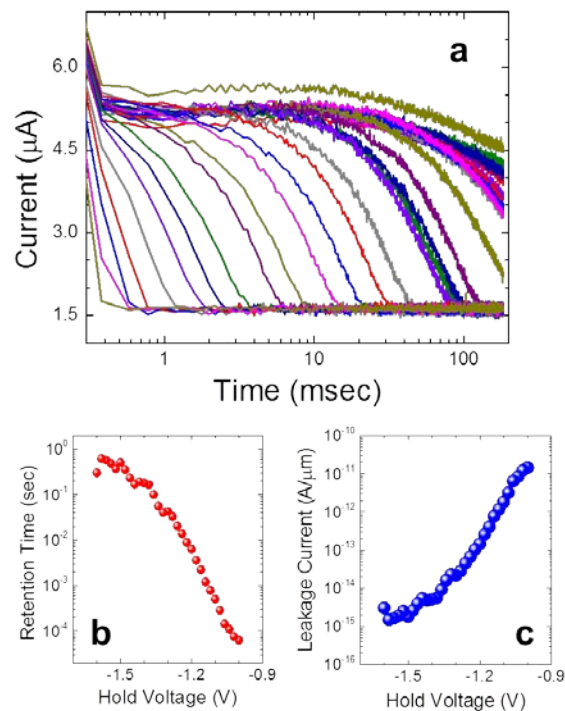
Figure 3-14 (a) Output current with V_{HOLD} varying from -1.6 V to -1V in steps of 20 mV. (b) Retention time extracted based on (a) as function of the V_{HOLD}. (c) Estimated leakage current as a function of V_{HOLD} with 50 % discharge as a criterion for retention time.

CHAPTER 4   HETEROSTRUCTURE DEVICES BASED UPON 2D MATEIRALS

In the previous chapter, the circuit application of 2D materials has been reviewed. However, besides the use in conventional VLSI chips, 2D materials are promising in various novel semiconductor applications. For instance, 2D MX_2 materials with high electron affinity are of particular interest since these materials should allow low barrier heights for n-type electrical contacts.   High affinity 2D materials could also have application for use in TFETs to produce highly staggered or broken-gap 2D heterostructures which enables abrupt change in electronic properties across atomically sharp junctions. Broken gap structures formed with 2D heterojunctions are extremely advantageous in the application of TFETs because the on current from band to band tunneling is highly enhanced with the nearly non-existing tunneling barrier. The off current resulted from direct tunneling is suppressed by the heavy mass of MX_2 materials. The switching of the devices is controlled by the gate field tuning the channel and thus abrupt turn on effects can be achieved. Therefore, the subthreshold swing of broken gap TFETs can exceed the thermal limitations of 60 mV/decade and the on/off ratio could be improved. This makes TFETs ideal for reducing the standby power in modern electronics.

As discussed in the first chapter, broken gap structures can be formed between high VBM and low CBM materials. The ideal scenario is the VBM of one material is only slightly above the CBM of the other material for the best Fermi tail cutting. This restriction makes the filtering for suitable material combinations difficult. Szabó *et al.* has

simulated $MoTe_2/SnS_2$ heterojunctions for tunneling transistors, and the results indicate small staggered gap between the two materials [94]. With the same metal atoms, $SnSe_2$ has even lower CBM than SnS_2 and the value of 5.18 eV is slightly under the CBM of $MoTe_2$, 5.15eV. Thus, the material set of $MoTe_2/SnSe_2$ is promising for forming type III heterostructures. A schematic diagram of an idealized TFET based on a $MoTe_2/SnSe_2$ heterostructure is presented in Fig. 4-1 (a). Here, the device is gated both on top of and below the channel to enhance gate control. N-type $SnSe_2$ serves as the source and p-type $MoTe_2$ serves as the channel and drain. Based on the calculations, a broken gap junction should be formed between the source and channel. Upon the channel modulation by changing the gate bias, abrupt switching could be obtained with this device. The anticipated band structure of this device is shown in Fig. 4-1 (b).
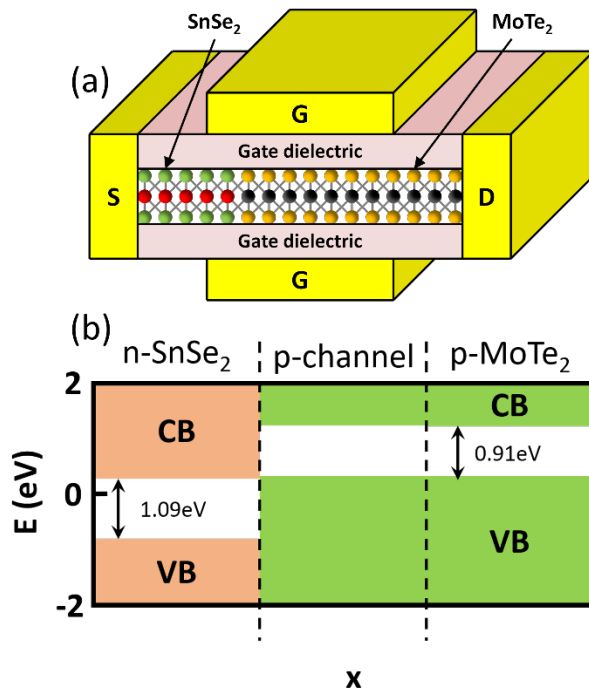
Figure 4-1 (a) Schematic view of the proposed double-gate $MoTe_2$-$SnSe_2$ hetero-TFET. (b) Band profiles in the device along the transport axis without considering self-consistency (flat band condition).

In this chapter, reviewed is the fabrication and characterization of heterostructure devices combining the 2D materials, $SnSe_2$ and $MoTe_2$, with the ultimate goal being the achievement of a device such as the one shown in Fig. 4-1. The individual material parameters and device properties are extracted are evaluated. Characterization is also performed on heterostructures made by vertically stacking $SnSe_2$ and $MoTe_2$. Finally, initial work on preparation of laterally stacked heterostructures is also introduced.

4.1 Fabrication process of for $SnSe_2$ MOSFETs

The starting substrate for the device fabrication was an n+ Si wafer upon which a 110 nm SiO_2 film was grown using thermal oxidation. Here, a global backgate process was used where the entire Si substrate serves as the gate electrode. Thus, a conductive substrate was required and that is why highly doped substrate was used. The global backgate structure also removes the requirement to align the flakes to pre-existing features on the mask. . For this reason, searching for appropriate flakes for device fabrication occurred after the transfer of a group of flakes. So, a specific oxide thickness needs to be used for identifying thin flakes. As explained in the first chapter, an oxide thickness of ~295 nm is critical to recognize monolayer graphene. For 2D materials, due to the difference in monolayer thickness, this criterion could be relaxed where both ~300 nm and ~100 nm thick oxide can serve as the gate dielectric. EBL alignment marks were also patterned and metallized with Ti/Au as reviewed in the second chapter. Next MX_2 flakes were exfoliated onto the substrate from a bulk crystal purchased from a commercial vendor. The exfoliation method coincides with the aligned exfoliation process in the first several steps. Nevertheless, after obtaining transparent flakes on the scotch tape, the tape was

attached directly onto the cleaned substrate. Next, the flakes were located using optical microscopy and then the substrate was mapped out followed by the designing of EBL mask. After that, source and drain contact openings in PMMA were defined using electron-beam lithography. A short O_2 plasma clean and buffered oxide etch (BOE) were performed before metallization to ensure removal of surface oxides and polymers before deposition of contact metallization. Solvent lift-off of the metal completed the device fabrication process. Fig. 4-2 shows an optical micrograph of a typical back-gated transistor. The devices had a contact spacing of 500 nm and the substrate was utilized as the gate electrode. Atomic force microscopy after device fabrication indicated a thickness of 84 nm for the exfoliated $SnSe_2$ film.
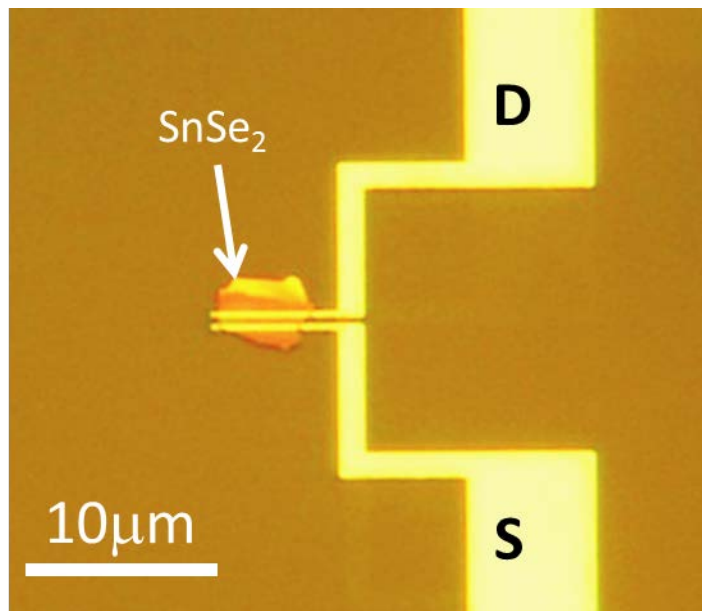
Figure 4-2 Optical micrograph of exfoliated $SnSe_2$ substrated-gated MOSFET. The channel length and width are 0.5 μm and 5.68 μm, respectively. The gate thickness of this device is 100 nm.

4.2 SnSe$_2$ field-effect-transistors

DC current vs. voltage measurements of the SnSe$_2$ FET were performed in a Lakeshore CPX-VF cryogenic probe station using an Agilent B1500A parameter analyzer. All measurements were performed in vacuum at temperatures ranging from 300 K to 4.4 K. The output characteristics of the device in Fig. 4-2 are shown in Fig. 4-3. Here, the drain current, I_D, was measured vs. the drain-to-source voltage, V_{DS}, while V_{GS} was changed from -30 V to +30 V in steps of +10 V. Only the positive V_{DS} results are shown, but similar results were obtained for $V_{DS} < 0$. A drive current of 160 µA/µm at $V_{DS} = +2.75$ V and $V_{GS} = +30$ V was observed at $T = 300$ K, and this value increased to over 340 µA/µm upon cooling to $T = 4.4$ K.   The output characteristic at room temperature showed only slight modulation, a result that is believed to be due in part to screening of the gate potential by the free carriers in the SnSe$_2$. Some surface-related conduction effects may play a role, since no room-temperature current modulation was observed for transistors measured in air, though more studies are needed to understand surface interactions in these samples. Despite the increase in drive current and on-to-off current ratio with decreasing temperature, no devices were observed to completely turn off for the gate voltage range considered here. Below 100 K, partial saturation of the I_D-V_{DS} curves was also observed.
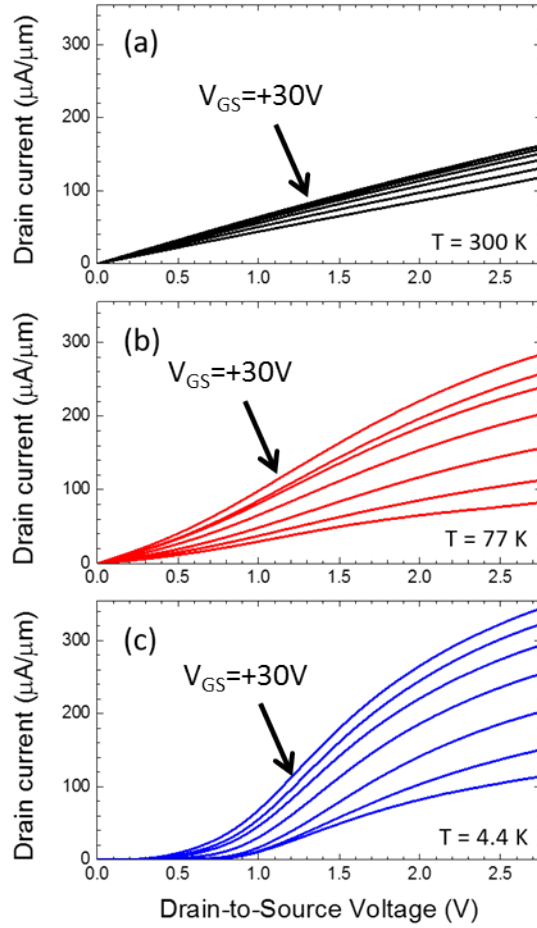
Figure 4-3 Output characteristics of the SnSe$_2$ MOSFET at (a) 300 K, (b) 77 K and (c) 4.4 K. V_{DS} was swept from 0 V to 2.75 V. V_{GS} was biased from -30 V to +30 V at a step of 10 V.

The transconductance values, g_m, vs. V_{GS} at $V_{DS} = + 2V$ at different temperatures are shown in Fig. 4-4 (a). Here, due to hysteresis between the up and down V_{GS} sweeps, the g_m values plotted have been averaged between the two sweeps. The characteristic shows a broad flat region at intermediate gate voltage values, and g_m is seen to increase from 0.9 μS/μm to 4.0 μS/μm from $T = 300$ K to 4.4 K. In Fig. 4-4 (b), the effective

field-effect mobility, μ_{eff}, is plotted vs. temperature. A long-channel, linear-region

transistor model is used where a parallel plate capacitor model is used for the gate
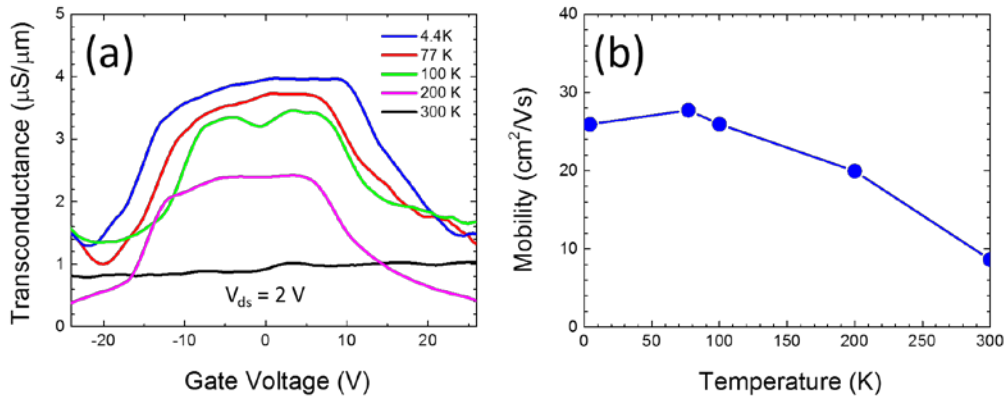
Figure 4-4 (a)Transconductance, g_m, vs. V_{GS} for the SnSe$_2$ MOSFET. Here g_m was determined by averaging between up and down sweeps of V_{GS}, to account for a moderate hysteresis. (b) Effective mobility vs. temperature for an SnSe$_2$ MOSFET extracted from the average transconductance, g_m, between V_{GS} = -5 to +5 V at V_{DS} = +1 V.

capacitance, C_{ox}, and is determined as in equation 3.5, where ε_{ox} = 3.9, t_{ox} = 110 nm.

The effective mobility increases from 8.6 cm^2/Vs to 28 cm^2/Vs, as T is decreased from

300 K to 77 K, and then decreases slightly, likely due to contact resistance effects at

lower temperatures. The mobility results are roughly in agreement with prior reports on

bulk SnSe$_2$ [95]. The low-temperature mobilities are likely to have some uncertainty due

to the non-linearity of the contacts in this regime and further studies are needed using

different gate length devices to de-embed the effect of contact resistance from the device

mobility.

Also, the activation energy of the low-voltage conductivity is extracted. In Fig. 4-

5, the temperature dependence of the drain current at V_{DS} = 50 mV is shown on an

Arrhenius plot. The Arrhenius equation is given as:

$$I_D = Ae^{\frac{-E_a}{kT}},$$

(4.1)

where A is the pre-exponential facter, E_a is the activation energy, k is the Boltzmann constant and T is the temperature. In Fig. 4-5, the natural log of the drain current is plotted vs. 1/kT and thus as the slope of the line the activation energy is found. The extracted activation energy is only 5.5 meV, indicating the virtual absence of a Schottky barrier. This is expected given the low work function of Ti and high electron affinity of $SnSe_2$.
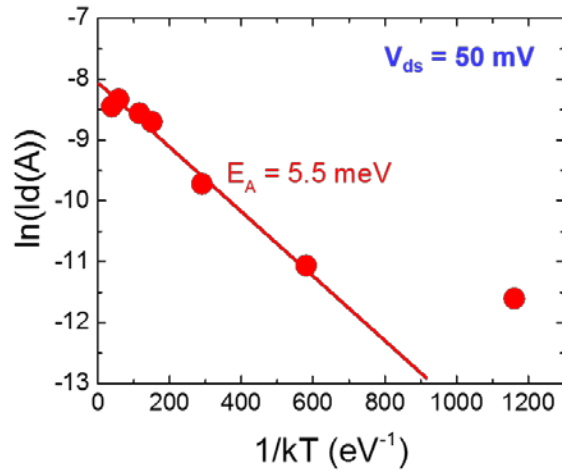
Figure 4-5 Arrhenius plot showing the natural log of the drain current, I_D, vs. 1/kT at V_{DS} = 50 mV.

The conductance and contact quality of $SnSe_2$ were further tested by using a transfer-length method (TLM) structure. The structure was fabricated with the same process flow as that of the $SnSe_2$ FET where multiple contact fingers were patterned in parallel on the same flake instead. Between every two neighboring contacts, the separation length varied in an ascending order. The results of the output characteristics are plotted in Fig. 4-6 (a), where the drain to source current, I_D, of devices with different

channel lengths, is plotted vs. the V_{DS}. The output shows linear characteristics owing to the 2-terminal measurement setup and the total resistance is extracted as the reciprocal of the slope of the curves. Then, the total resistance is plotted vs. the channel lengths in Fig. 4-6 (b), which is calculated as following:
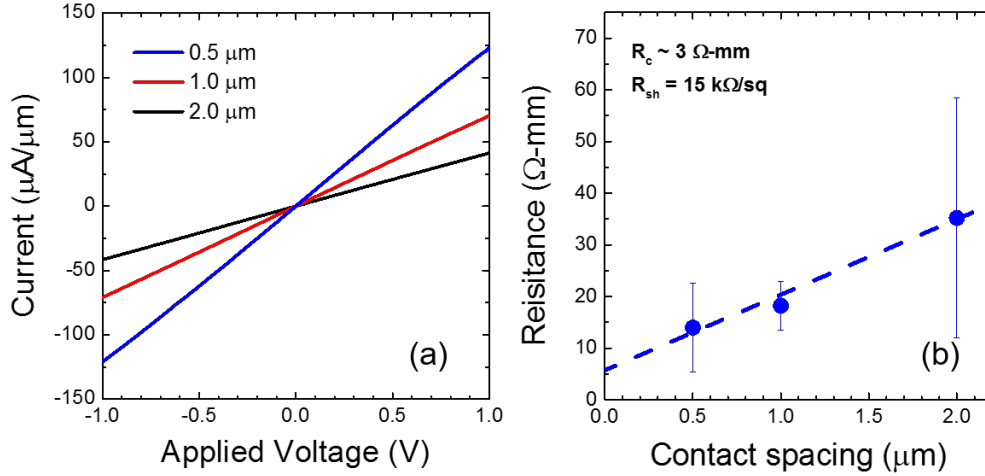
Figure 4-6 (a) Output characteristics of the TLM structure. (b) Total resistance plotted vs. the contact spacing.

$$R_{TOT} = LR_{sh} + 2R_C, \tag{4.2}$$

where L is the channel length, or the spacing between fingers, R_{sh} is the sheet resistance and R_C is the contact resistance. The sheet resistance of SnSe$_2$ is 15 kΩ/sq, indicating high conductance of this material. And the contact resistance extracted is ~3 Ω·mm, which means Ohmic contacts with low contact resistance can be achieved.

Despite the reasonable low-temperature performance, the devices show only a small modulation at room temperature. It is expected that improved modulation can be achieved if thinner SnSe$_2$ layers can be achieved as well as by utilizing a top-gate electrode. Thus, more SnSe$_2$ MOSFETs were fabricated using the local backgate

technique introduced in Chapter 2. By using the aligned exfoliation process, thinner film can be obtained and better MX_2-dielectric interface. Fig. 4-7 shows the measurement results of a local backgate $SnSe_2$ MOSFET of which the channel thickness is ~5 nm, with the channel length being 0.5 μm and the width being 4 μm. 20-nm-thick HfO_2 serves as the gate dielectric in this device. The device was measured with the same experimental setup as the MoS_2 MOSFET characterization in section 2.2. In Fig. 4-7 (a), V_{DS} was swept from 0 V to +1.5 V with the drain-to-source voltage, V_{GS} increasing from -1.5 V to +1.5 V in a +0.5 V step. The device shows a current level of ~55 μA/μm, which is slightly lower than the device with thick $SnSe_2$ channel. Nevertheless, given that the channel is about an order thinner than the global backgate device, the current level is mostly independent of the channel thickness. This indicates that the carrier transport in the transistor takes place mostly in the surface layers and the lateral conductance of $SnSe_2$ is much higher than the vertical conductance. Plotted in Fig. 4-7 (b) is the transfer characteristics of the device in which I_D is plotted vs. V_{GS} at V_{DS} = 0.1 V and 1.5 V. An on-off ratio of <10 is observed under room temperature. Thus, the impact of the channel thickness on the channel modulation is limited.
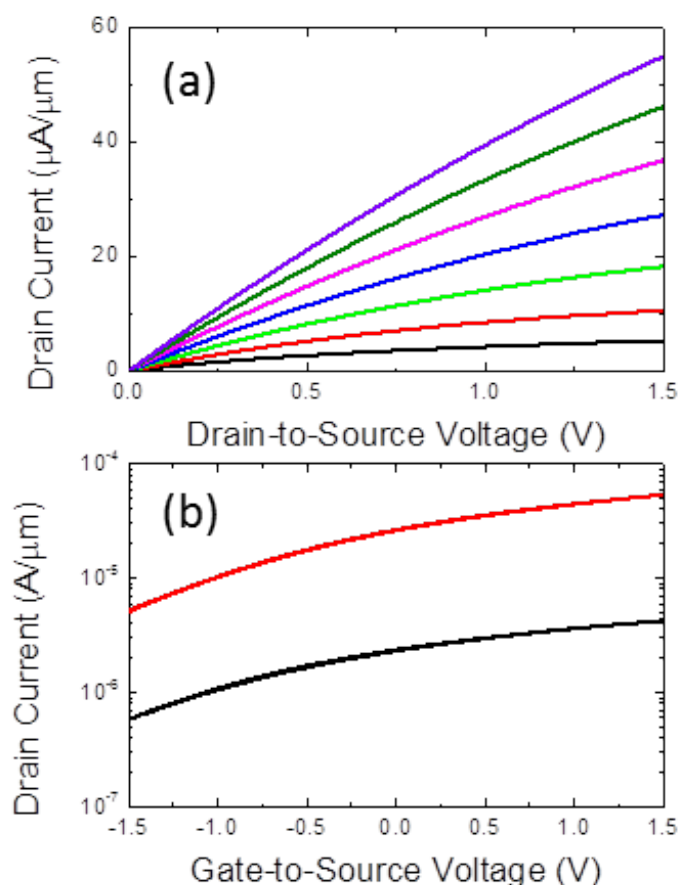
Figure 4-7 (a) output characteristics of a local backgate SnSe$_2$ MOSFET. V_{DS} was swept from 0 V to +1.5 V and V_{GS} values are -1.5 V (black), -1 V (red), -0.5 V (green), 0 V (blue), +0.5 V (magenta), +1 V (olive), +1.5 V (purple). (b) transfer characteristics of the device. Gate voltage was swept from -1.5 V to 1.5 V and V_{DS} was biased at +0.1 V (black) and +1.5 V (red).

It is also believed a portion of the room-temperature leakage is due to surface conduction as no drain current modulation was observed when the devices were measured in air. Therefore, improved surface passivation or p-type counter doping could also be helpful to eliminate parallel conductance in the ungated regions of the device.

4.3 MoTe$_2$ field-effect-transistors

Unlike SnSe$_2$, which is a high electron affinity material and favoring electron transport, electron and hole transport are both feasible in MoTe$_2$, making MoTe$_2$

applicable in both n-type and p-type MOSFETs. The low electron affinity of $MoTe_2$ also makes it promising for forming highly staggered or broken gap heterojunctions if combined with high electron affinity materials such as $SnSe_2$. In order to characterize the electronic properties of $MoTe_2$, MOSFETs were fabricated with $MoTe_2$ as the channel material. The fabrication process was identical to that of the $SnSe_2$ MOSFET where global backgate structure was used. However, the contact material of source/drain was Pd instead of Ti to favor hole injection and form Ohmic contact due to the low electron affinity of $MoTe_2$.

In Fig. 4-8, the room temperature transfer characteristics of the device are plotted. In that measurement, V_{GS} was swept from -20 V to +20 V at V_{DS} = -1 V and +1 V. The device showed ambipolar behavior, which is due to the narrow energy gap. The narrow gap also limited the on-off ratio of the device, which is ~10^2 at room temperature.
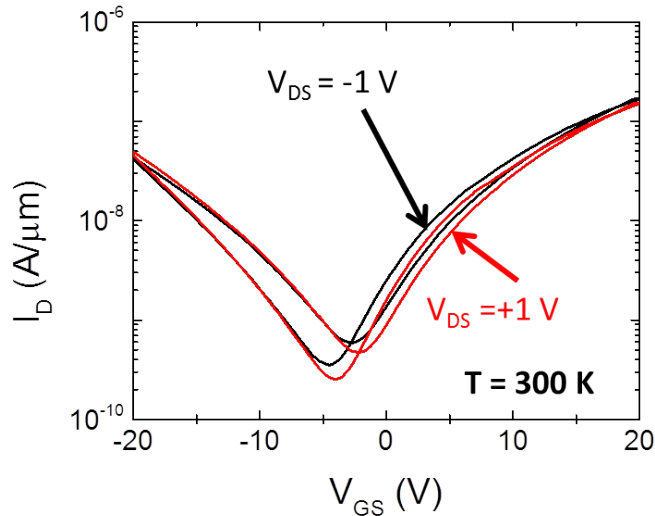
Figure 4-8 Transfer characteristics of $MoTe_2$ MOSFET at room temperature. V_{GS} was swept from -20 V to 20 V. V_{DS} was biased at -1 V and +1 V.The width of the device is 6 μm, and the length of the device is 2 μm. The gate dielectric is 100nm SiO_2.

The temperature dependent output characteristics is shown in Fig. 4-9 where I_D is plotted vs. V_{DS} at V_{GS} = -20 V and +20 V while the temperature varies from 140 K to 300 K.
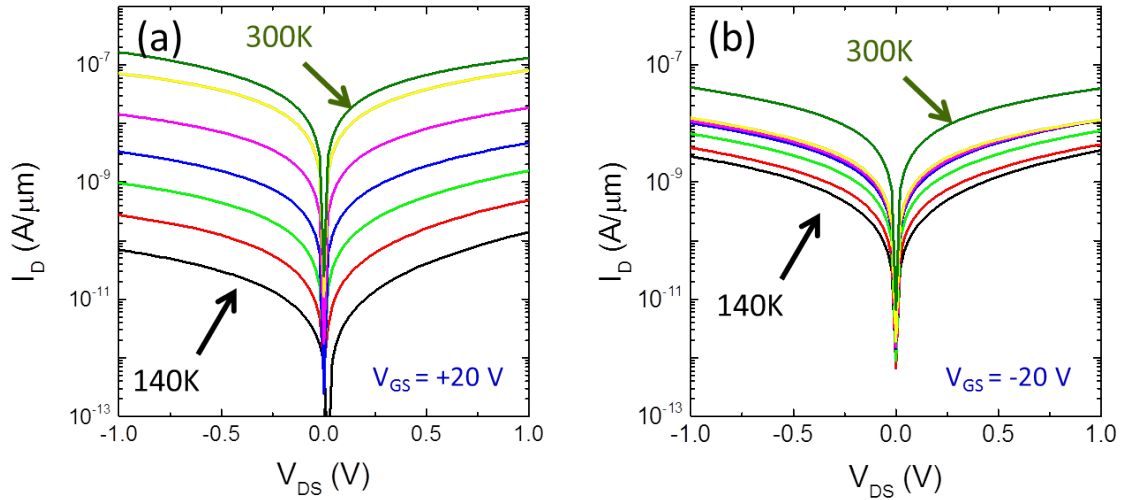
Figure 4-9 Output characteristics of MoTe$_2$ MOSFET shown in Fig. 4-8 at different temperatures. V_{DS} was swept from -1 V to +1 V. V_{GS} was biased at -20 V and +20 V. Curves stand for different temperature as 140K (black), 160K (red), 180K (green), 200K (blue), 230K (magenta), 260K (yellow), 300K (olive).

It is observed in Fig. 4-9 (a) that the on current of the device has strong temperature dependence at positive gate bias, indicating the existence of Schottky barrier at the Pd/MoTe$_2$ interface. However, the temperature dependence is less significant at negative gate bias as in Fig. 4-9 (b), which suggests that the Schottky barrier for hole injection is much lower than for electron injection. Therefore, upon contacting, the work function of Pd is pinned closer to the valence band of MoTe$_2$ than the conduction band. The Schottky barrier height is then extracted as the activation energy from previous results. Similar to the extraction in the SnSe$_2$ MOSFET analysis, Arrhenius plots under different bias

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conditions are shown in Fig. 4-10. The results at V_{GS} = -20 V and +20 V are shown in Fig. 4-10 (a) and (b), respectively, where red dots indicate positive drain bias and black dots indicate negative drain bias. Since Schottky barrier exists at the contact interface, the activation energy needs to be extracted with thermionic emission theory as:

$$I_D = AT^2 \exp(-\frac{1}{kT}(E_a - \frac{qV_{DS}}{n})), \tag{4.3}$$

Here, the extracted slope in Fig. 4-10 is equal to $E_a - \frac{qV_{DS}}{n}$, where E_a is the activation energy at V_{DS} = 0, and n is the ideality factor that determines the effective barrier height under bias. From the analysis, it can be seen that under negative gate bias, the effective barrier height of ~27 meV is much lower than under positive gate bias (~130 meV). The activation energies extracted are nearly independent of the polarity of drain bias. This indicates that with Pd contact, the Schottky barrier for hole injection is lower than that for electron injection, providing strong evidence of the p-type contact. Even though the barrier is still relative high, it is still encouraging compared to other TMDs thanks to its low electron affinity.
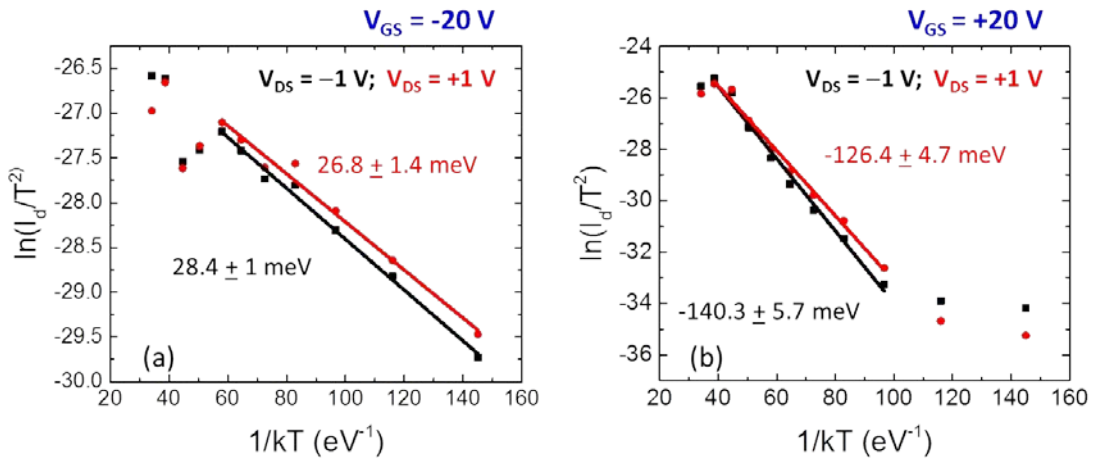
Figure 4-10 Activation energy extraction of Pd/MoTe$_2$ contacts from Arrhenius plots under different bias conditions.

4.4 Vertically stacked heterostructures

As argued in [84], highly staggered gap or broken gap heterostructure can be formed at the interface between high electron affinity and low electron affinity MX_2 materials. Among various material sets, $SnSe_2/MoTe_2$ is a promising combination because upon contacting, the valence band of $MoTe_2$ has the same energy as the conduction band of $SnSe_2$ based on calculation. Thus, $SnSe_2/MoTe_2$ heterostructure was fabricated by vertical stacking these two materials together.

The fabrication started with the same substrate as the global backgated $SnSe_2$ MOSFETs. Multiple $MoTe_2$ flakes were exfoliated onto the substrate from which a thin flake with acceptable size was selected. Then, a selected $SnSe_2$ flake was transferred on top of the $MoTe_2$ flake with the aligned transfer station. A micrograph of the exfoliated heterostructure is shown in Fig. 4-11 (a). Similarly, contact openings were defined using EBL and the metallization were performed with evaporation and lift off. Two separate lithography steps were used for the $SnSe_2$ contacts and $MoTe_2$ contacts because of the different metals as the contact materials. Ti and Pd were deposited on $SnSe_2$ and $MoTe_2$, respectively. Fig. 4-11 (b) shows the completed device.
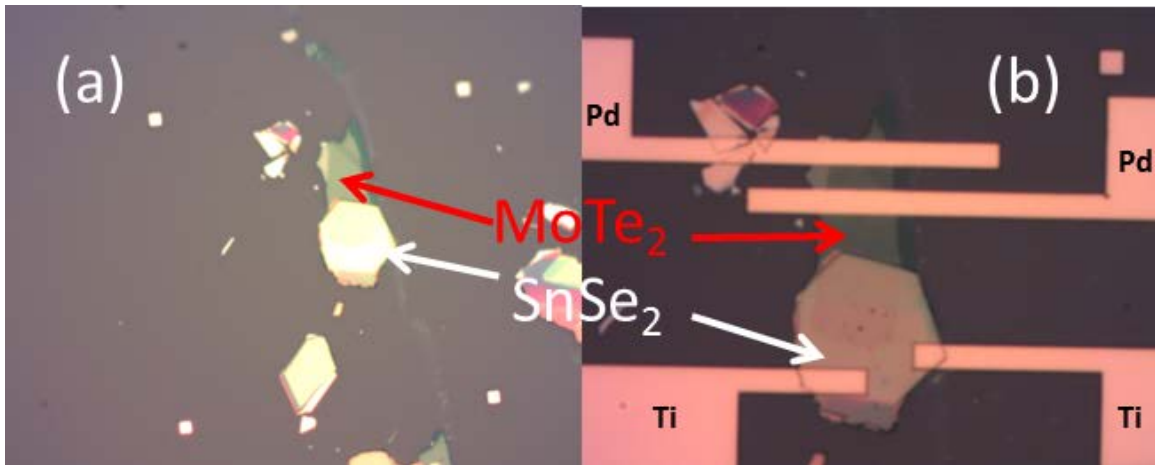
Figure 4-11 Micrographs of (a) exfoliated $SnSe_2$/$MoTe_2$ heterostructure and (b) completed heterostructure device.

The transfer characteristics of the single heterostructures FET are shown in Fig. 4-12. The $MoTe_2$ and $SnSe_2$ are defined as the drain and source, respectively. Here, the drain current, I_D, was measured vs. V_{GS}, between -20 V and +20 V, at $V_{DS} = +1$ V and -1 V. The data was taken at different temperatures to extract the barrier heights and the results at 300 K, 230 K and 140 K are shown. Significant asymmetry is observed and the results is consistent with the fact that the activation energies are different for the two types of contacts.

Figure 4-12 Transfer characteristics of the heterostructure device shown in Fig. 4-11 at different temperatures. V_{GS} was swept from -20 V to 20 V. V_{DS} was biased at -1 V and +1 V.

Activation energy analysis was carried out as the same method of the $MoTe_2$ MOSFET to extract the barrier heights. The Arrhenius plots are shown in Fig. 4-13. Due to that high carrier concentration and minimum band bending were observed in $SnSe_2$ devices, it can be considered as metal here. Similarly, the barrier height under negative bias is lower than that under positive bias. Thus, the electron affinity of $SnSe_2$ is closer to the valence band of $MoTe_2$ than to the conduction band. However, the sums of the activation energy of the Pd contact and the $SnSe_2$ contact are not symmetric, which needs further study. Moreover, even though the results indicate that the electron affinity of $MoTe_2$ is lower than that of $SnSe_2$, there is no evidence that the junction is broken gap. Thus, further investigation is needed.
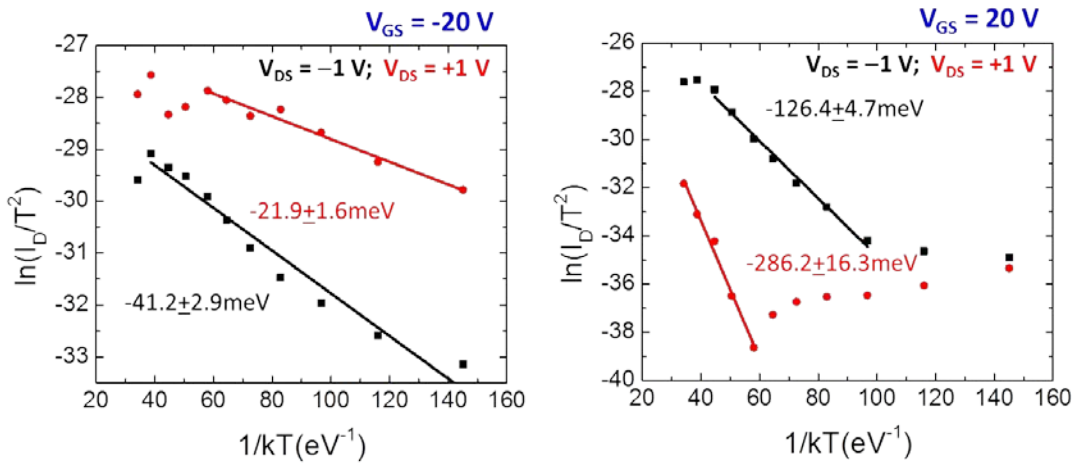
Figure 4-13 Activation energy results of the single heterostructure device.

In order to examine the band line-up between these two materials, a double heterostructure was fabricated and the micrographs are shown in Fig. 4-14. As shown in the picture, two $SnSe_2$ flakes were exfoliated on top of one $MoTe_2$ flake via aligned exfoliation and Ti was used to contact both $SnSe_2$ flakes. In the measurement of this

device, the two Ti contacts are probed as source and drain and the substrate serves as the gate.
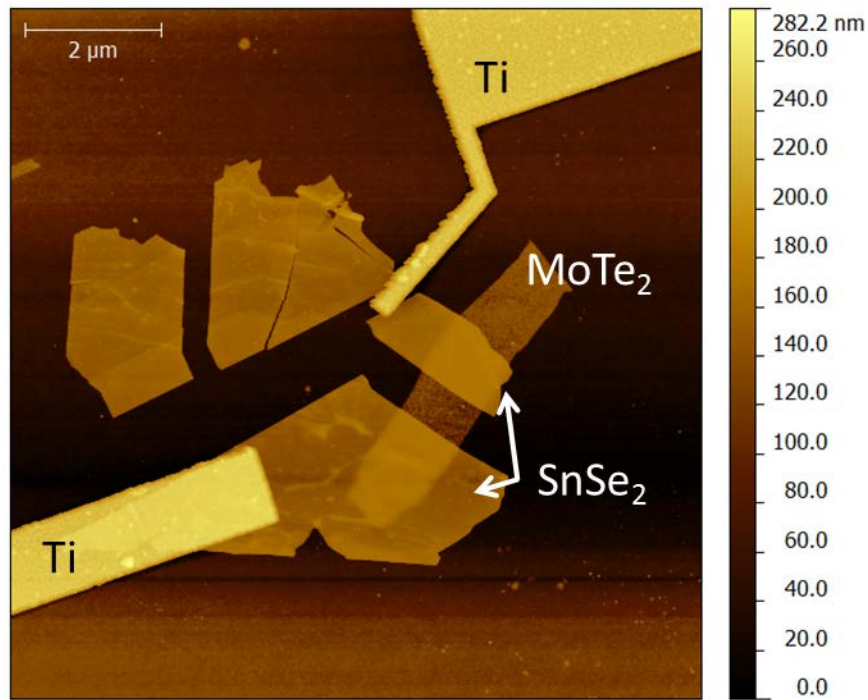
Figure 4-14 AFM picture of exfoliated $SnSe_2$/$MoTe_2$/$SnSe_2$ double heterostructure device.

With the same measurement set up as the single heterostructure, the transfer characteristics are plotted in Fig. 4-15. At room temperature, the device showed ambipolar current with negative gate bias. However, at low temperature the ambipolar current disappears, which indicates that the current results from thermionic emission. In conflict with the hypothesis, barely any band to band tunneling current is observed at negative gate bias. Thus, the heterostructure results in a staggered gap where the bands of $SnSe_2$ is below the bands of $MoTe_2$. With positive gate bias, electrons can be injected through the Schottky barrier at the $SnSe_2$/$MoTe_2$ interface. Under positive gate bias, the

barrier is much higher since it adds both the band of $SnSe_2$ and the overlap between the bands. Therefore, the heterojunction is a staggered gap junction instead of a broken gap structure. It should be noted that in the vertical stacked structure, the interface quality between the two materials is unknown and the material could be strained on the edge. Also, the band structure could be different along vertical or lateral lattice directions. All these factors may result in a change of the band lining. It is expected that if a horizontal heterostructure can be fabricated with high quality interface, more accurate band lining information can be obtained.
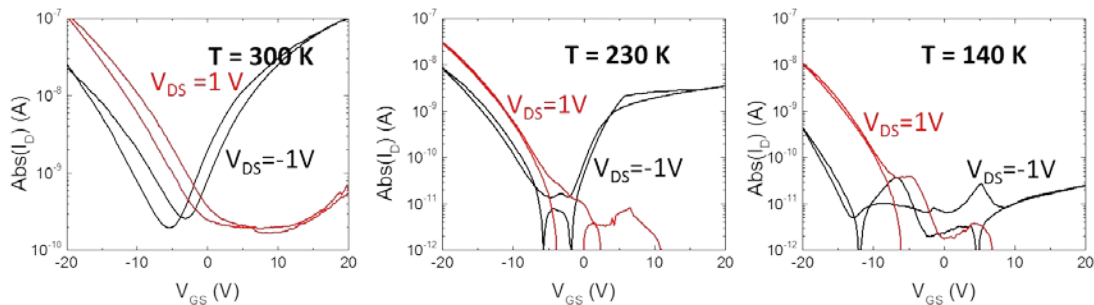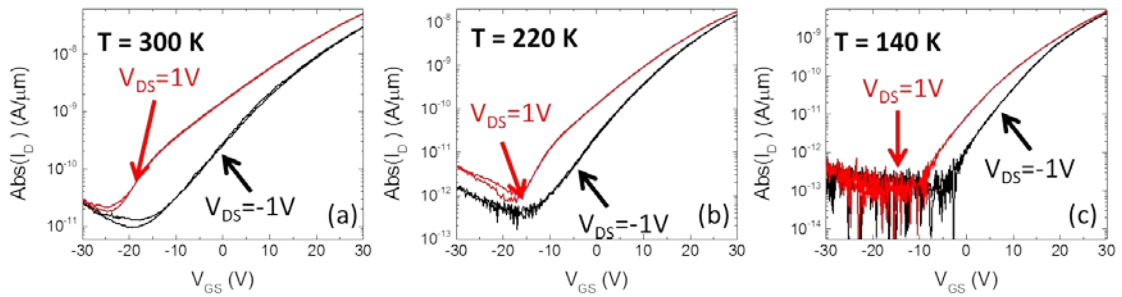

Figure 4-15 Transfer characteristics of the double heterostructure device at different temperatures. V_{GS} was swept from -30 V to 30 V. V_{DS} was biased at -1 V and +1 V.

4.5 Lateral heterostructures

Since lateral heterostructures are advantageous in studying the electronic properties of the junction between 2D materials, many efforts have been made in the fabrication of in-plane 2D heterojunctions. MoS_2/WS_2 and MoS_2/WSe_2 horizontal heterostructures have been synthesized with atomically sharp junctions [96, 97]. Metal-semiconductor heterojunctions with two phases of $MoTe_2$, the 2H and 1T' phase was also been demonstrated via strain or laser illumination, forming extremely low charge injection barrier and highly conductive Ohmic contacts [98]. To better reduce the

fabrication complexity, a direct synthetic approach for creating in-plane heterostructures with two phases of one 2D material was demonstrated with $MoTe_2$ in our work [99].

As introduced in the first chapter, 2D TMDs can be synthesized by directly oxidizing metal with chalcogen, and in our experiment that means tellurizing Mo in a CVD chamber. The phase of the few-layer $MoTe_2$ can be controlled by changing the flux of Te, while 2H $MoTe_2$ is synthesized with high Te flux and 1T' with low Te flux. With medium flux, a mix of 2H and 1T' $MoTe_2$ nano-islands can be formed where the phase of $MoTe_2$ can be confirmed with Raman spectroscopy. With our phase-selective synthetic strategy, patterns with heterojunctions can be fabricated instead of random grains. This flux-controlled phase engineering technique could be used in producing 2D heterostructures for next generation electronic and optoelectronic devices.

The CVD chamber used for the synthesis is a horizontal hot-wall single-zone furnace. As shown in Fig. 4-16 (a), the process started with depositing thin Mo layer on
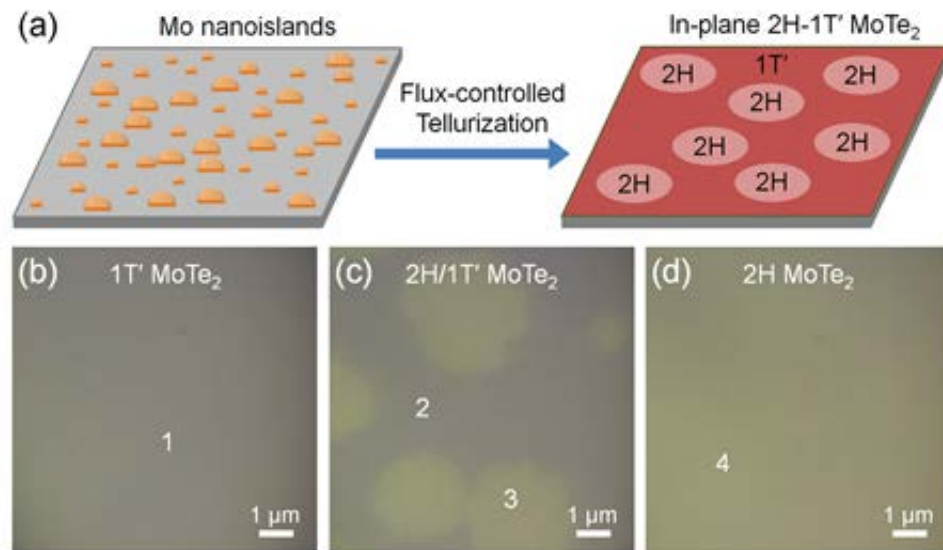
Figure 4-16 Growth of in-plane 2H-1T' $MoTe_2$ homojunctions from Mo nanoislands. a) Schematic illustration showing the growth process. Micrographs of (b) 1T', (c) 2H/1T' and (d) 1T' $MoTe_2$. [99]

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Si/SiO$_2$ substrates using Electron beam evaporation. Mo tends to nucleate as nano-islands instead of uniform sheets with a short deposition time and low deposition rate. Typical Mo nano-islands are 1~3 nm in heights and a few hundred nanometers in width. As introduced in chapter 1, the substrate was then placed facing down on top of an alumina boat containing Te, followed by annealing in Ar/H$_2$ at 585 °C. After the reaction, continuous films with smooth surface were obtained with roughness same as the underlying SiO$_2$ layer, most likely due to the reflow. The thickness of the film is consistent with five layers of MoTe$_2$, which is ~3.5 nm. The flux of Te, which is the controlling factor of the phase, is determined by the temperature. 585 °C is used for the synthesis for the homojunctions, while 635 °C and 535 °C are used for the 2H and 1T', respectively. The atomic ratio of Te/Mo in 2H MoTe$_2$ is 2.0 with being 1.86 in 1T' MoTe$_2$. Thus, MoTe$_2$ tends to form in the 1T' phase in Te deficient environment with low Te flux. Optical micrographs of 2H, 2H-1T' and 1T' MoTe$_2$ are shown in Fig. 4-16 (b-d), respectively, showing sharp contrast between the 2H phase (marked by 1, 2) and 1T' phase (marked by 3,4).

With our phase-selective synthesizing strategy, Few-layer 2H/1T' MoTe$_2$ patterns were also fabricated. This process started with the synthesis of few-layer 1T' MoTe$_2$
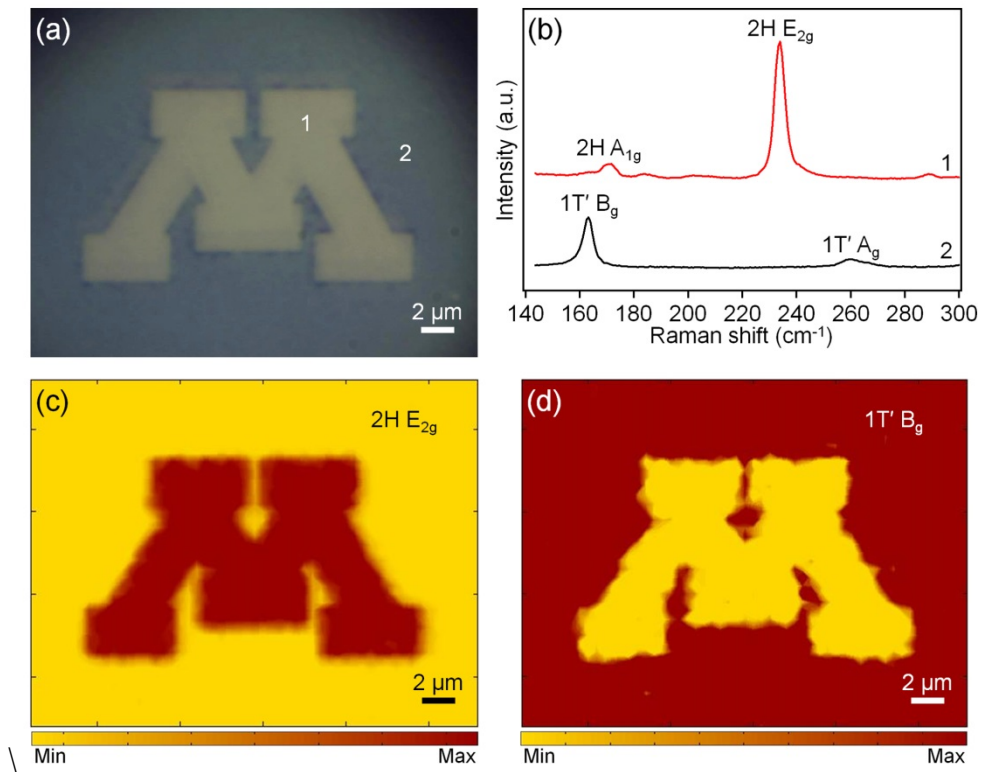
Figure 4-17 Fabrication of few-layer 2H-1T' MoTe$_2$ patterns. (a) Optical image of 2H-1T' MoTe$_2$ patterns. (b) Raman spectra taken from the points marked by 1 and 2 in (a). (c) Raman intensity map of the E$_{2g}$ mode of 2H MoTe$_2$. d) Raman intensity map of the B$_g$ mode of 1T' MoTe$_2$. [99]

sheet from Mo nano-islands deposited by evaporation. Then patterns were defined using EBL followed by the etching in 30% hydrogen peroxide to remove the MoTe$_2$ for 3 minutes. Next, Mo nano-islands were deposited with evaporation using the same recipe and lifted off. The sample was then annealed with high Te flux to obtain patterns with heterojunctions. Note that the phase of the few-layer 1T' MoTe$_2$ was conserved during the high Te flux annealing, indicating that MoTe$_2$ is thermodynamically stable in the phase as deposited under the reaction conditions. The patterns are shown in Fig. 4-17 where sharp optical contrast can be observed in (a) and the phase can be further confirmed with Raman, while different peak positions can be observed, as shown in (b).

Raman mapping confirms that the domains of the pattern are comprised of 2H and 1T'

and interfaces are abrupt between 2H and 1T' MoTe$_2$ domains (Fig. 4-17 (c) and (d)).

CHAPTER 5   CONCLUSION AND FUTURE WORK

5.1   Conclusion

2D materials are of interest for numerous electronic and optoelectronic device applications. The numerous electronic properties of this class enable a wide range of 2D material based devices and circuits serving different purposes. Integrating devices based on heterogeneous materials improves the performance of complementary circuitry and building junctions with heterogeneous materials allows the formation of broken gap heterostructures. In this dissertation, heterogeneous devices based on $SnSe_2$ and $MoTe_2$ are reported along with the realization of heterogeneous circuits based on MoS_2 and BP MOSFETs.

First the fabrication process of local backgate structure for 2D MOSFETs was designed and realized. This structure allows the use of thin high-K material as the gate dielectric layer. MoS_2 and BP MOSFETs were fabricated with this technique and the electronic characteristics were measured. The results showed that high on-off ratio and sharp subthreshold slope can be achieved with MoS_2 FETs and n-type doping was observed with passivation oxide layers. The output characteristics of BP p-MOSFET and MoS_2 n-MOSFET showed excellent match can be achieved between them. TID radiation response was also studied for BP MOSFETs, indicating radiation-tolerable devices can be made with BP. Based upon these results, logic inverter and DRAM cells were proposed and designed.

Then the fabrication process was developed for logic inverter using the local backgate technique. The inverter was measured as individual transistors and the results

exhibited consistency with discrete FETs. Upon measuring as 4-terminal inverter, the circuit showed functionality and gain larger than unity for various bias conditions along with high drive currents. Parameters were extracted from the results indicating encouraging performance of the inverter. Then the operation of the inverter at different temperatures and frequencies was tested and discussed. The fabrication and read/write operation of 1T/1C and 2T DRAM cells were introduced.

Next $MoTe_2$ and $SnSe_2$, which can potentially form a broken gap heterostructure, were characterized. As the platform for the experiments, FETs with those materials were fabricated. Test results showed $SnSe_2$ is a high conduction material which can form good Ohmic contact with metal. $MoTe_2$ is an ambipolar material which forms p-type Schottky contacts with metal. To evaluate the band alignment between them, single and heterostructures were fabricated by vertically stacking the filmed together. Results indicated staggered gap instead of broken gap was formed at the interface. However, with the in-plane heterostructure synthesis technique which is introduced at last, more accurate band line-up information can be achieved. Overall, the results show that heterogeneous circuits based on 2D materials are promising for high-performance large scale integration complementary circuits and heterostructures with 2D materials have the potential to be used in tunneling transistors.

5.2 Proposed future work

5.2.1 Further approach on logic circuits

The delay of the inverter measured with the current set-up in the third is much larger than the intrinsic delay because the large capacitance load brought in by the

measurement equipment. In real circuitry, the resistive and capacitive load of successive stages are mostly the same order as the logic gates driving them. Thus, the ring oscillator method is an effective way to characterize the speed performance of a logic inverter. Ring oscillator, which is a device consisting of n logic inverters in a ring (n is an odd number), oscillates between high and low voltage levels (representing "0" and "1") at each stage. In the inverter chain, the output of each stage is connected to the input terminal of the next stage while the output of the last stage is fed back to the first. The supply voltage and ground terminals are shared between the stages. One advantage of the RO characterization is that the delay of the ring oscillator is the sum of the delay time of all stages and thus the frequency of the ring oscillator, f_{RO}, is much lower than the single inverter, given as following:

$$f_{RO} = \frac{1}{2\tau n},$$

(5.1)

while τ is the intrinsic delay of each inverter, n is the number of the stages. The more stages a ring oscillator composes of, the lower frequency it operates at compared to a single inverter. Thus, the impact of the load RC on the measurement results are suppressed. Meanwhile, an extra inverter can be loaded after the last stage to rectify the signal. At the price of adding an insignificant amount of delay, the load from the measurement equipment is isolated from the RO. Therefore, a much more accurate intrinsic frequency could be extracted.

In our experiment, a ring oscillator was designed and fabricated. To maintain the uniformity between each stage, monolithic single-grain exfoliated MoS_2 and BP flakes were used. That means all devices were fabricated on the same film and the carrier

conduction through the flake need to be taken into account. The designed schematic of a 7-stage ring oscillator is shown in Fig. 5-1. The left part of Fig. 5-1 shows the schematic of the fabrication layout, where different colors represent different fabrication layers. Blue, green, grey and red stripes are the mesa layer, source/drain layer, gate layer and via layer, respectively. The circuit schematic is shown on the right part of the figure, and to form a ring oscillator, the output of inverter No. 7 is fed back to the input of inverter No. 1 with inverter No. 8 being a signal stabilizer. All the inverters share the common supply voltage, V_{DD} and ground, GND. In the layout schematic, inverters can be distinguished by finding the gate electrode on top of which the individual source terminals and common drain terminals are fabricated. Note unlike the circuit schematic, where all inverters are arranged in numerical order, the sequence of inverters in the layout schematic is 2->1->3->4->6->5->7->8. This is due to the fact that all inverters are fabricated on the same flake, and thus neighboring drains of inverters must have the same parity to minimize the conduction between nodes.
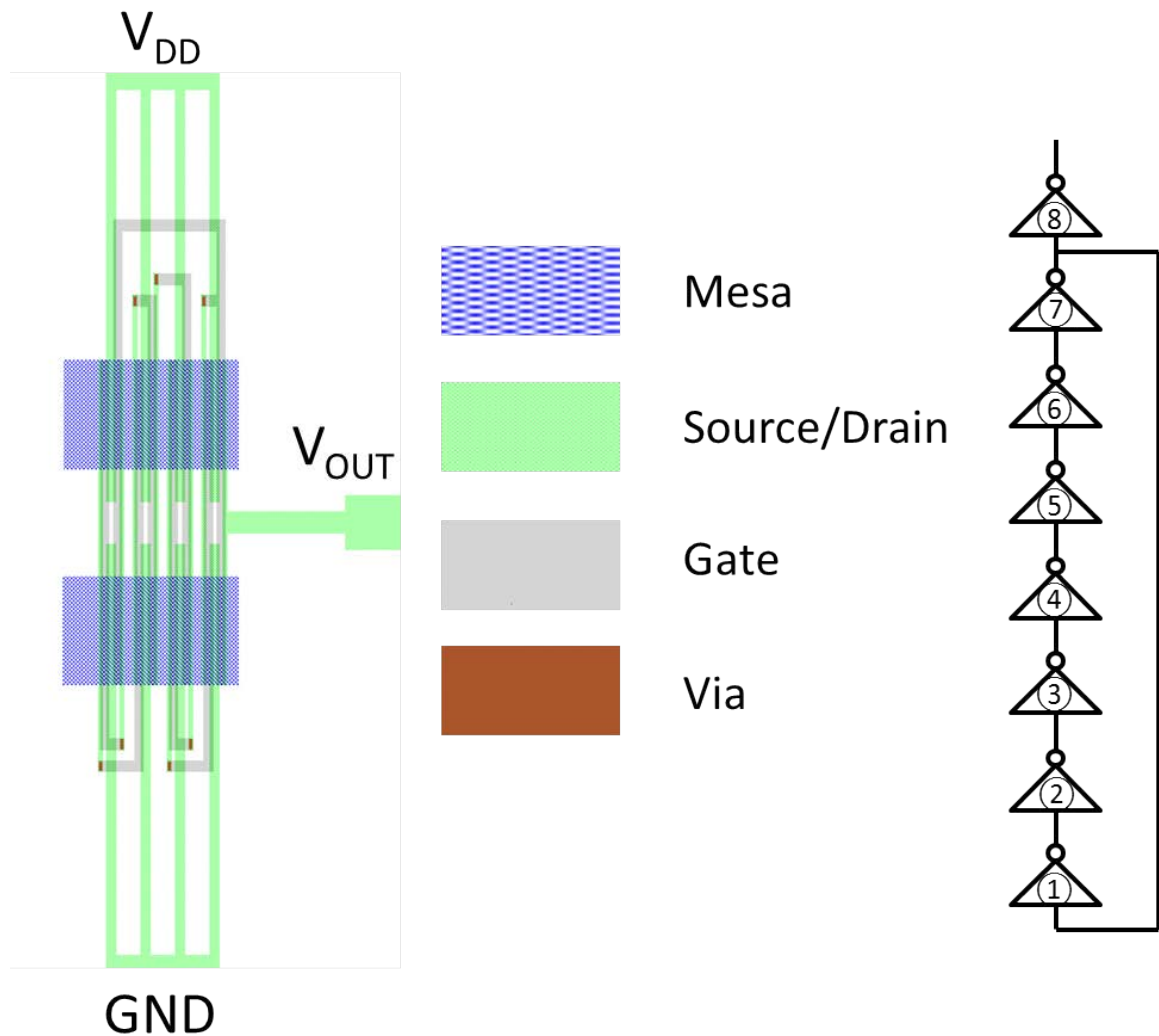
Figure 5-1 Layout schematic and circuit schematic of a 7-stage 2D ring oscillator.

The fabrication process is based on the fabrication of the single inverter. A Si wafer with 110 nm thermally grown oxide was used to start with. Ti/Au was deposited to form the EBL patterned alignment marks followed by gate electrodes exposure by EBL. After the development, the electrodes were recessed by the combination of dry/wet etch same as in the inverter process. Next the gate electrodes were metallized with Ti/Pd by Ebeam evaporation and lift off. Then 20 nm HfO_2 gate dielectric was deposited at 300 °C

using ALD. As the connection between the gate metal layer and the source/drain metal layer is necessary and hence the vias were opened the same way as in the DRAM fabrication. A MoS_2 flake and a BP flake were then exfoliated and transferred to cover all the gate fingers using the optical aligning system. After transferring the BP flake, it can be chosen either to narrow the MoS_2 or the BP flake by dry etching. Following the mapping of the sample, excessive parts of either flake were patterned and exposed with EBL. To etch the BP flake, Ar plasma etch is used in the plasma etcher. The BP flake is physically bombarded away with an etch rate of 2~3 layer/min. To remove MoS_2, reactive ion etching is used and MoS_2 can be oxidized with chlorine. Afterward, EBL was again used to define the source and drain openings of all the transistors. Finally, Ti/Au (10/80 nm) metallization was evaporated and lift-off, completing the fabrication process. The micrographs of completed ring oscillators are shown in Fig. 5-2.
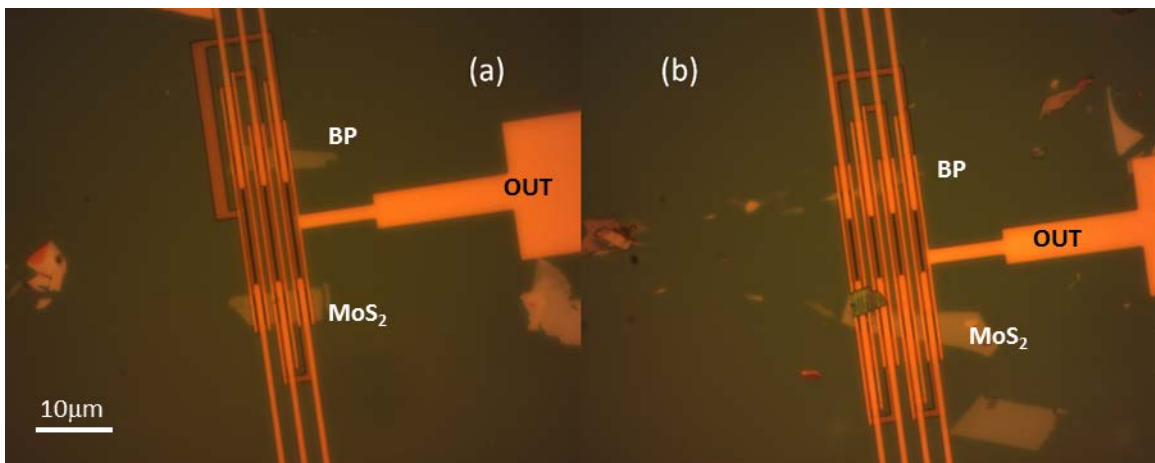
Figure 5-2 Micrographs of (a) a 5-stage ring oscillator (b) a 7-stage ring-oscillator.

Due to the lack of an effective failure-analysis method for ring oscillators, functional ring oscillators have yet to be demonstrated. However, it is still a promising way to characterize the performance of 2D based logic circuits.

5.2.2 Circuits with higher level of integration

Unlike 3D semiconductors, whose band gaps widen as the dimension shrinks, 2D materials have excellent scalability because their band structure remains the same upon scaling. This unique feature makes 2D materials promising candidates for next generation electronics as scaling becomes the main challenging issue in semiconductor industries. Even though fabricating 2D device with minimum critical dimensions can improve the density of devices, the scalability of 2D materials in the Z-direction, which is even more essential, has not been fully exploited. Here, a vertically stacked inverter structure is proposed and fabricated which is illustrated in Fig. 5-3.
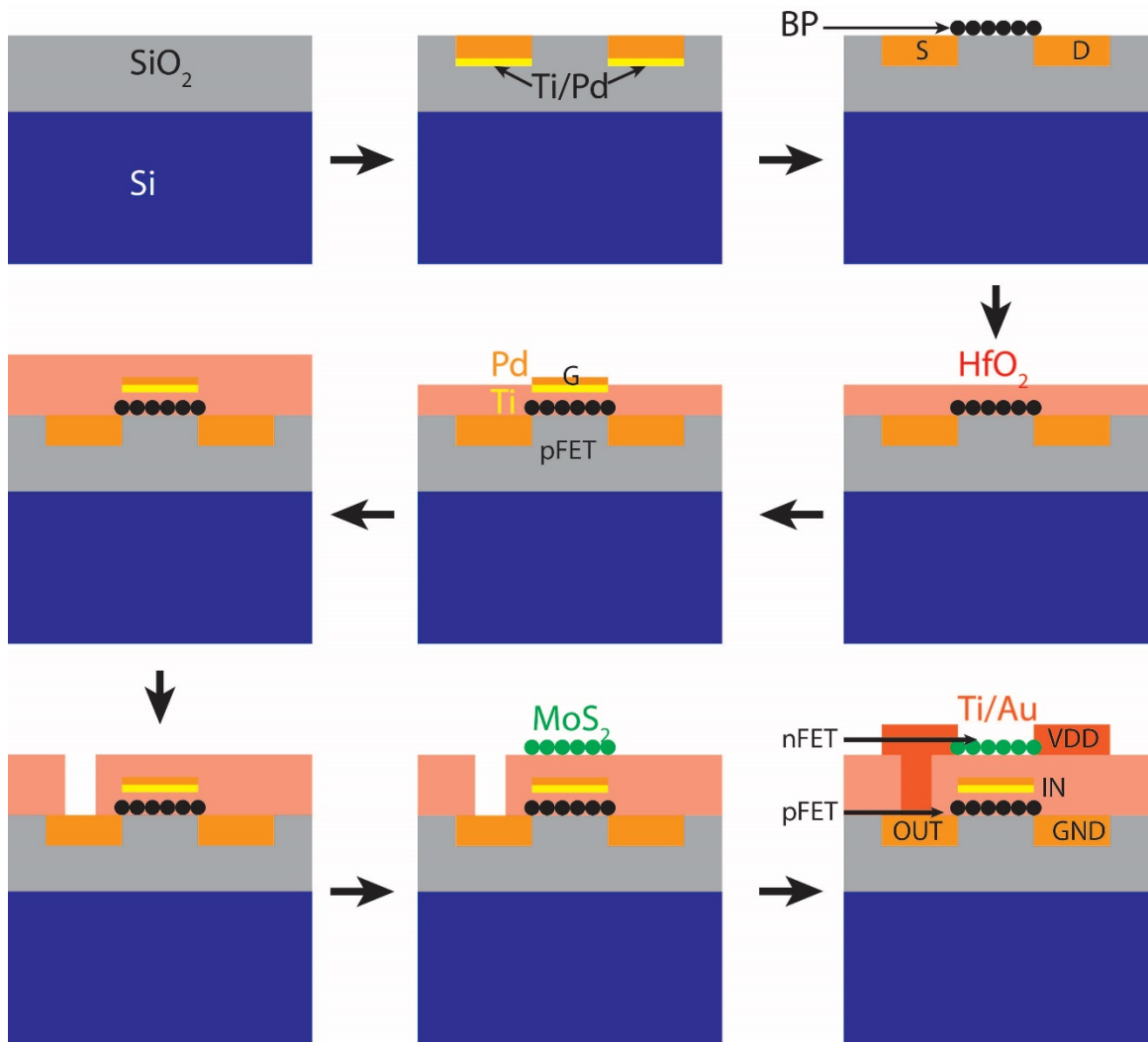
Figure 5-3 Fabrication sequence for 3D integrated 2D inverter.

The fabrication starts with the Si/SiO_2 substrate as reviewed before. Then, source/drain contacts of the BP p-MOSFET are deposited into a recess created by etching the EBL-defined pattern. A selected BP flake is transferred between the source and drain contact fingers followed by the deposition of HfO_2 using ALD which serves as the gate dielectric of the p-MOSFET. Then Ti/Pd is deposited into EBL defined gate openings where Ti and Pd work as the gate contact for p-MOSFET and n-MOSFET, respectively.

The selection of metals is based on the consideration of both fabrication feasibility and the work function engineering. Then ALD is used again to deposit HfO_2 layer as the gate oxide for the n-MOSFET. Vias are created with the process discussed in the third chapter over the common drain electrode. Next, selected MoS_2 flake is transferred on top of the gate finger. Finally, Ti/Au are deposited as the source/drain terminal of the n-MOSFET with evaporation plus lift off, completing the fabrication process.

The micrograph of a stacked inverter before the last metal deposition is shown in Fig. 5-4. On top of the gate finger, the darker flake is the BP and the brighter flake is MoS_2. Upon testing, the top MoS_2 n-MOSFETs performed consistent with other MoS_2 devices fabricated using a conventional local-backgate process, but the p-MOSFETs were open-circuit between source and drain. This is most likely due to the oxide forming on bottom-side of BP suring transfer, which prevents Ohmic contacts form forming between the source/drain electrode and BP channel. Fabricating these devices in a glove box is a potential solution to resolve this problem.
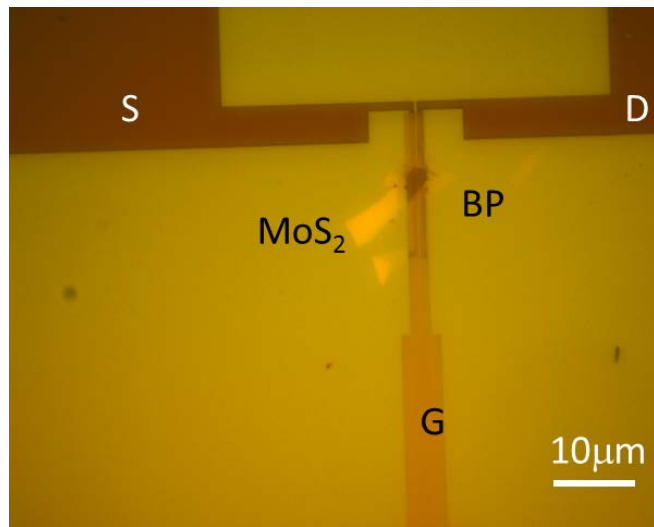
Figure 5-4 Micrograph of fabricated stacked inverter before S/D deposition.

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5.2.3 In-plane heterostructures between MoTe$_2$ and SnSe$_2$

As discussed, forming an in-plane abrupt heterojunction with MoTe$_2$ and SnSe$_2$ may rule out non-idealities and get real band offsets of the heterostructure. The synthesis of the lateral MoTe$_2$ heterojunctions builds a useful step toward building junction with heterogeneous materials. The synthesis of SnSe$_2$ nano disks were reported with nano structures randomly stacking together [100]. However, to build abrupt horizontal heterostructures, uniform and controllable film fabrication technique need to be developed. The combination with the existing MoTe$_2$ synthesis process is promising for building broken gap heterostructures serving for next generation tunneling field effect transistors.

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APPENDIX

EBL PMMA process for patterning resist with EBL:

1) Cleaved substrate is placed in a beaker half-way filled with acetone, in order to be cleaned in a sonication machine,

2) The sample is then washed with fresh acetone, methanol, IPA spray bottles successively, and blown dry by N_2 gas,

3) 950 PMMA C4, where C stands for chlorobenzene formulated PMMA and 4 stands for the PMMA concentration, is spin coated onto the substrate at 3000 rpm for 1 minute,

4) The sample is hard baked at 180°C for 8~10 minutes to bake the solvent out. ~300 nm thick polymer will remain on the sample,

5) The sample is exposed in the EBL system at a dose of 1200 μC/cm^2,

6) Exposed sample is developed in a solution of 1:3 MIBK and IPA at 20℃ for at least 90 seconds. Stirring occasionally is preferred.

Equipment make and models

1) oxidation furnace (Model: titian)
2) electron beam evaporator (Model: CHA SEC 600)
3) plasma etch chamber (model : AV vision 320)
4) surface-profilometer (Model: Kla-Tencor P7)
5) ALD chamber (Model: Savannah)
6) EBL system (Model: Vistec EBPG5000+)

Etching recipes for substrate oxide and gate dielectrics:

1) O_2 clean recipe: the flow of O_2 = 99sccm, the pressure = 100 mTorr, the power = 100 Watts.

2) SiO_2 ething recipe: the flow of argon = 50 sccm, CHF_3 = 50 sccm, CF_4 = 25 sccm, the pressure = 75 mTorr, the power = 150 Watts.

3) Argon plasma etch recipe: Ar flow = 80 sccm, pressure = 150 mTorr, power = 80 W.

4) HfO_2 plasma etch recipe: flow of Ar = 5 sccm, flow of SiF_6 = 30 sccm, pressure = 100 mTorr, power = 100W

Aligned exfoliation process for transferring 2D material flakes:

1) The bulk 2D crystal is sandwiched between two pieces of adhesive scotch tapes and each side is rubbed gently with fingers or Q-tips,

2) The scotch tapes, which now have crystals stuck on it, are removed from the bulk crystal source,

3) Another fresh piece of scotch tape is put on one of the piece of tape which has crystal flakes on it. Then the face-to-face tapes are rubbed gently with fingers before peeling apart. This step is repeated multiple times until the remaining crystals on the tape look semi-transparent.

4) Then the tape is put on a PDMS covered glass slide. To prepare the PDMS, silicone base and activator are mixed at a 10:1 ratio, then drop-cast on to glass slides. The glass slides are then placed at room temperature for 48 hours or at 60°C for 1 hour for activation,

5) The tape on PDMS is then rubbed with Q-tip with moderate force, and peeled off quickly, thin crystal flakes will remain on the PDMS,

6) The PDMS is inspected under optical microscope to identify few-layer flakes, after cherry-picking the desired flake, excessive PDMS is cut off with razor blade,

7) The glass slide is then put upside down and stuck on the micro-manipulator of the alignment station in our lab. The substrate chip is solvent cleaned and baked to get rid of moisture on the surface, and then placed on the chuck of the alignment station,

8) The selected flake and gate finger are aligned under the microscope, and then brought together by the micro-manipulator until contacted. Let it stand for several seconds, and peel off. Repeat this for several times if the flake is not transferred.

Hard mask via process for creating vias through HfO_2:

1) After the deposition of HfO_2 gate dielectric layer, with the chip kept in the ALD chamber, deposit 60nm Al_2O_3 at 300℃,

2) Use EBL to pattern the vias and develop the patterns,

3) Dip the chip into 1:10 BOE for 150 seconds for slightly over etching the Al_2O_3 in the via area, the etch rate of ALD Al_2O_3 is ~30nm/min, rinse the chip in DI water for 3 minutes.

4) Etch the HfO_2 in the plasma etcher for 4 minutes. The etch rate is ~6 nm/min,

5) Soak the chip in acetone for 5 minutes to remove possible organic residue followed by an oxygen plasma descuming,

6) Strip the remaining Al_2O_3 hard mask with BOE soaking as described in (3).