DESIGN AND FABRICATION OF A MICROCHIP TO GENERATE SEQUENTIAL PULSE OUTPUT FOR ARTIFICIAL SKIN SENSOR ARRAY

A THESIS

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ABSTRACT

In this project, we have designed and implemented the circuit, which basically generates sequential shifted pulse sequences. The circuit is a part of the pressure sensor system for colonoscopy. The other parts of the sensing system include the artificial skin sensor array and a data acquisition (DA) system. The circuit will be connected with sensor array to detect the signal at each dot of the sensing array grid.

The artificial skin sensor array has been designed by our research partner in MIE department. The designed circuit will be integrated with the pressure sensor array to convert the pressure value into electrical signal, which should be readable from the computer terminal through a DA System. The designed circuit is expected to provide multiple outputs from a single input signal. Each output should be distinguishable. The work we reported in this thesis is the second version of the circuit design. The circuit designed in the first version has the problem of too much offset from our expected output. In this version, we improved this through adding additional noises and offset. We implemented the designed circuit on both breadboard and printed circuit board (PCB). Testing results on each board shows expected performance.

In addition, we also made effort to fabricate the circuit on a microchip in order to minimize the size of the circuit and make it finally fit into the sensor system for practical application. We applied the very large scale integrated-circuit (VLSI) technique on the implementation of the microchip. We went through the procedure of creating the scheme of microchip fabrication through VLSI software Cadence® and verify the layout using Calibre® physical verification software. We used the free service from MOSIS, Inc for

the fabrication process. The fabricated circuit is expected to arrive in a couple of months. Testing of the circuit will be one of our subsequent tasks of this project.

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Chapter 1 Introduction

In this chapter, we will review the background of this research project, give a summary of the previous work carried out and identify the goal and scope of our thesis work.

1.1 Background

Colorectal or colon cancer is a disease in which abnormal cells in the colon or rectum divide uncontrollably, ultimately forming a malignant tumor [1]. There are several methods to screen people for colon cancer. One of the standard tests is colonoscopy [2] as shown in Figure 1.1.

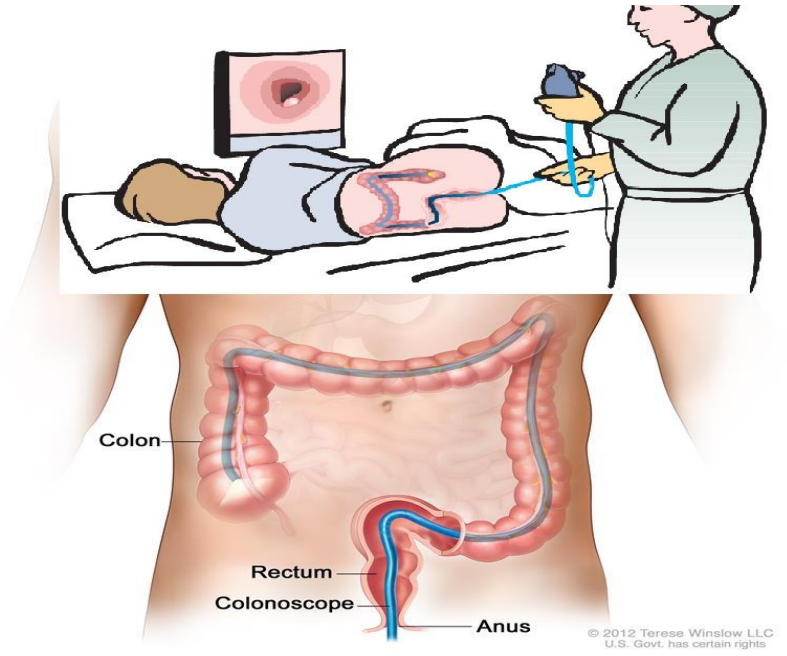


Figure 1.1: Colonoscopy and screening process.

This thesis research we reported is part of the project on the artificial skin-like pressure array for colonoscopy application. In the skin-like pressure sensor array project, a sensing system is developed in order to measure the contact force between the colon wall and the

colonoscopy tube. The artificial skin-like sensor array is arranged in outer surface of the colonoscopy tube. The pressure measurement will help to reduce the perforation risk and increase the comfort level of the patient during the colonoscopy procedure.

The advantage of the test is high sensitivity than other test method. Also, the doctor can view the whole rectum and colon; can also perform additional testing (like biopsy or polypectomy) along with the test, if necessary. However, there is a serious issue involved during the test. Colonoscopies lead to "serious medical complications" in 5 out of every 1000 patients (0.5%), according to a 2006 report in the Annals of Internal Medicine [3], which is quite a large number for only diagnostics of cancer. Moreover, 0.1% perforation occurs during the diagnosis test [4]. The pressure applied to the tube inserted through the rectum during the test is relied only upon the doctor's experience, without any live pressure reading.

Our research reported in this thesis is part of the project of skin-like pressure sensor array. We aim to develop a circuit to provide the driving voltage to the sensor array. The sensor array has been developed by another group of students in our research group. With the integration of the circuit and sensor array, the DA module in the system will be able to measure the contact pressure between colon wall and colonoscopy tube. The measured pressure acts as the feedback to the doctor during colonoscopy in order for the doctor to adjust applied force accordingly in the procedure to avoid perforation. To make a compact integrated system, the circuit we designed are expected to be built on a microchip finally. Our thesis work is part of the effort leading to this goal.

1.2 Previous work

We would like to call the circuit design reported here as the second-version design (design V2). The first version of the circuit design (design V1) was conducted by two of our previous colleagues in this group [5][6]. They have implemented the designed circuit on the breadboard and PCB, respectively. The circuit should sequentially provide 5Vpp voltage pulses to multiple contact terminal of the sensor. Each pulse should keep constant 5V for at least 500ms in order to provide enough time of pressure measurement by DA module. To get reading from more surface contact, supplying voltage pulses to more contact terminals of the sensor is necessary.

Figure 1.2 shows the breadboard implementation whereas Figure 1.3 shows the PCB implementation. In breadboard implementation, three different circuits were connected together to get the total 24 output pulse sequence. In PCB implementation, on-off voltage levels were optimized with one output lead.

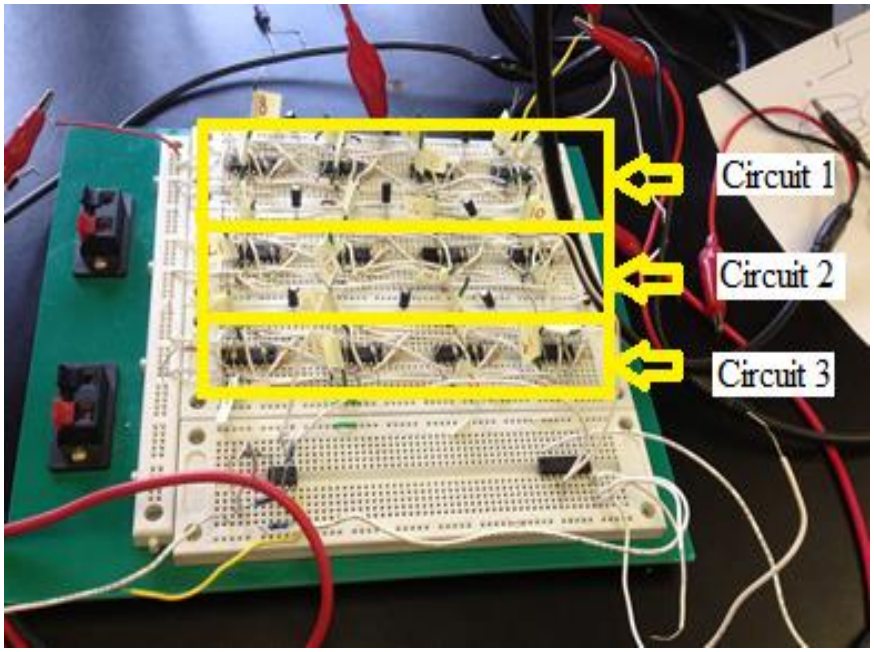


Figure 1.2: Breadboard circuit from previous implementation.

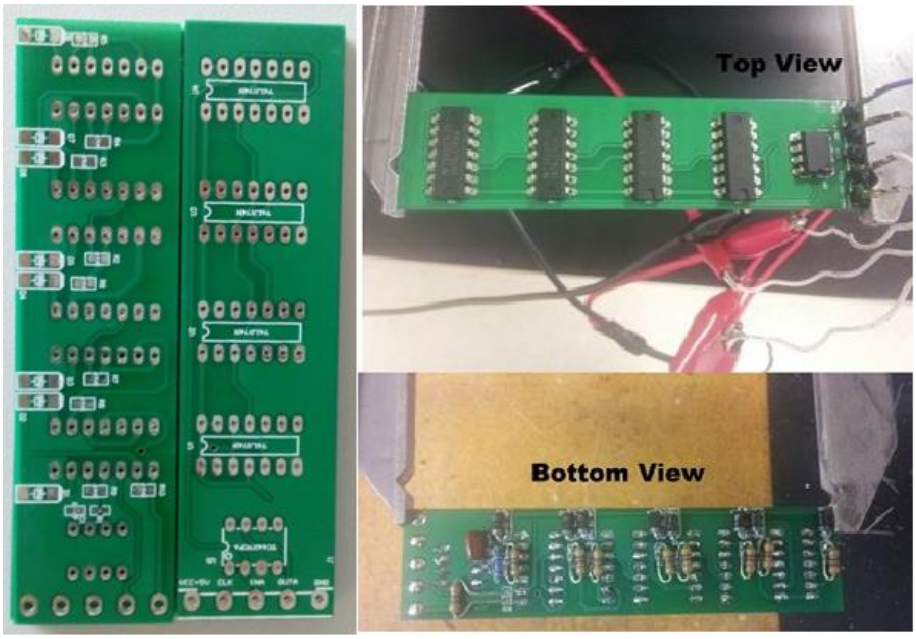


Figure 1.3: PCB from previous implementation.

However, in earlier design there are some drawbacks. The circuit has too much offset from our desired output. The off mode voltage is 0.3V as they have used diodes. It also has high noise in the output waveforms.

1.3 Motivation

With the understanding of the deficiencies of the first design, we need to further improve the circuit to make the output more approaching to the ideal pulse form. As single output of desired response is achieved from earlier research; we have concentrated on making more output leads so that more reading from pressure sensor grid will be available. As each output is distinguishable, the task is a bit challenging. In order to ensure the proper performance of the re-designed circuit, testing will be performed by integrating the modified PCB implemented circuit with the other part the sensing system. Moreover, to make the whole system more compactible, reducing the size of the circuit board is

necessary. Based on the dimension of the sensor array, VLSI technology will be employed to fabricate the re-designed circuit.

1.4 Scope

Based on the motivations mentioned above, the scope of our project focuses on three aspects: (1) Further improving the circuit design through offset-reduction technique; (2) implementing the re-designed circuit on the PCB and perform the testing with the sensing array and DA system; (3) Toward the implementation of the circuit on microchip, prepare the necessary design scheme and documentation based on the requirement of the fabrication foundry.

The microchip should be working with single input and provide multiple outputs. Also depending upon the output requirements there should be option to cascade multiple chips to meet higher number of outputs. We have implemented the prototype of 16 outputs using cascading of two modified PCBs, each of 8 outputs. The circuit is working as expected.

The designed microchip can also be implemented in similar fashion. We have kept 16 outputs in a single micro-chip. We will be needing 16 micro-chips to supply the planned future skin like sensor array of 256 outputs.

Chapter 2 Literature Survey on Sequential Pulse Generation

The goal of our current research is to generate sequential pulse for the voltage supply of the sensor array. Here we provide a review on the literature of the sequential pulse generation technique as the preparation of our circuit design task.

Sequential pulse can be obtained from many different techniques. One of the implementation technique was using pulse generator with a pulse width modulator (PWM) and ring oscillator [7,8] to generate output with different duty cycle. To generate pulse with 50% duty cycle, they have used JK flip flops and logic OR gates. The output from OR gate can later be shifted to get the sequential outputs. Figure 2.1 shows different pulse signals in implemented circuit.

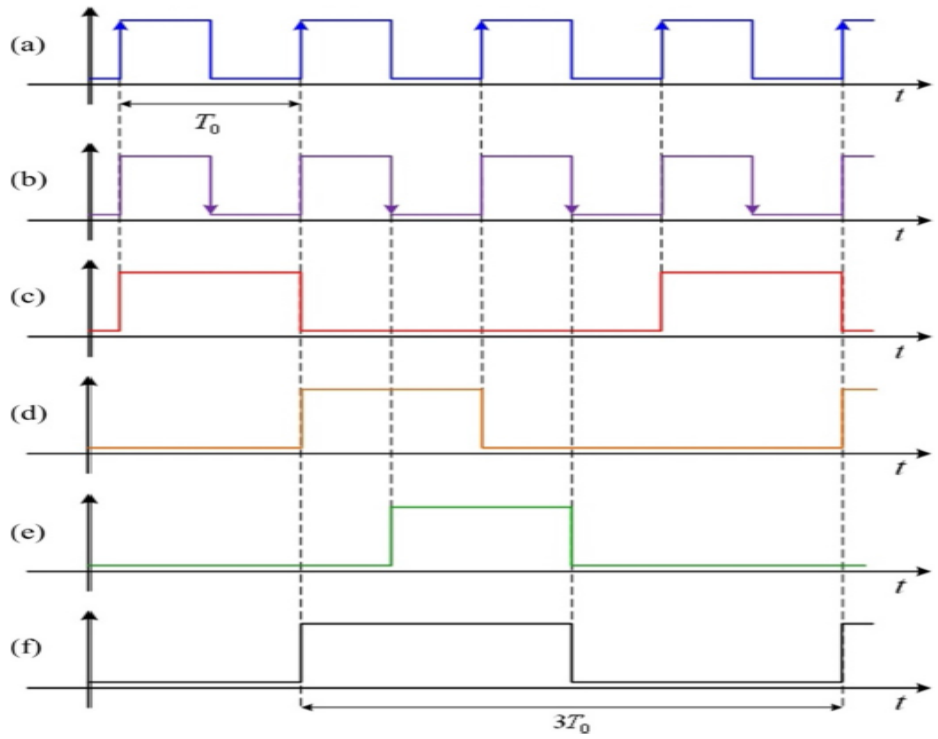


Figure 2.1: (a) clock rising edge (b) clock falling edge (c) Output from 1st JK Flip Flop d) Output from 2nd JK Flip Flop e) Output of 3rd JK Flip Flop (f) Output signal of logic OR of (d) and (e).

Another implementation was with comparator circuit, NAND gate and OP-AMP [9]. The circuit has very low noise margin. A small interference can change the output state.

Pulse generation can be also implemented based on microcontroller [10] or optical micro ring. But it can't be implemented on colon tube as for the size limitation. Micro ring based optical pulse generator is also available [11]. Implemented for almost similar application is also found [12]. They have implemented the circuit with VLSI technology which is similar to us. VCO and PLL (Phase Lock Loop) is used to generate bit streams (pulses) [13]. The implementation is for single output and input signal must have to match the clock frequency. PLL based clock generation [14] is necessary in this case. In our implementation we don't have to worry about the matching. Depending upon the clock frequency the output 16 pulses scaled to fit in the time period.

People also implemented using CPLD (Complex Programmable Logic Device), built from basic gates through programmable interconnections [15,16,17]. A CPLD typically has thousand to tens of thousands of logic gates. A program activates the required gates and output can be taken from MUX (Multiplexer). Figure 2.2 shows a typical CPLD structure.

The speed will be way less than full custom design, although there are other techniques available for speed optimization [18]. The size of CPLD based implementation will also become an issue to integrate with colonoscopy tube.

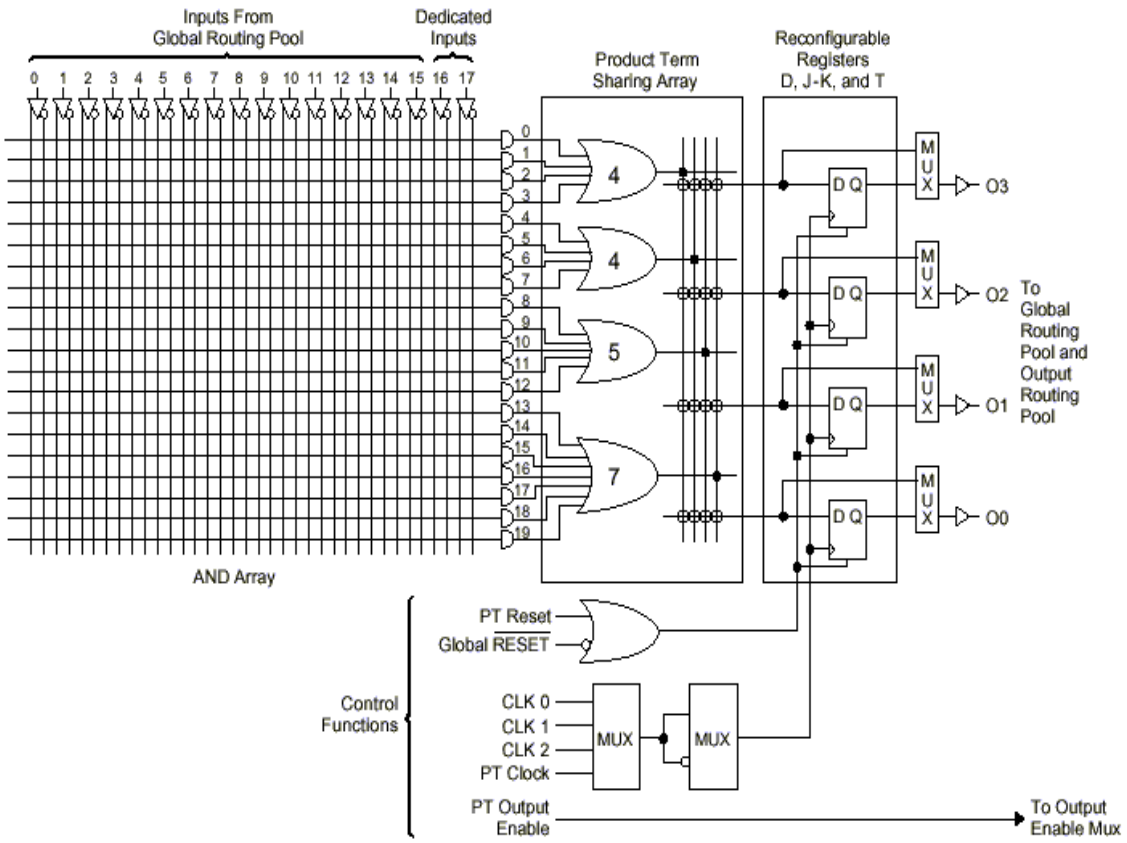


Figure 2.2: A typical CPLD structure.

Using JK, SR and D FFs, low power SIPO was implemented [19,20]. The high logic level was 3.3V and cannot be used with our particular project. The circuit was also bulky.

Another type was chaotic pulse generation [21]. High speed clock generation for Microprocessor application [22] and clock grating synthesis [23] technique can be applied in this case. It will generate pulses with constant amplitude but different width, which isn't also suitable in our application.

Chapter 3 Design Improvement and Testing on the Printed Circuit Board (PCB)

The ultimate goal is to implement the whole circuit into tiny micro-chip with 16 outputs. Before starting the design of micro-chip, we had to improve the design for sixteen output leads and test the modified PCB circuit to make sure everything is working properly.

3.1 Design Improvement

Available from previous research group, the PCB has only one output. We had to extended the output leads in PCB. The PCB provides housing for all CMOS chips. The different components in the circuit are also connected on the PCB through connecting wires. We have used two PCBs and modified them to get 8 outputs from each PCB. Then we have cascaded two PCBs to get the total sixteen outputs. We have also used LED in each output terminal to visualize the circuit operation in low frequency.

Figure 3.1 illustrates the modified PCB board connected with different components.

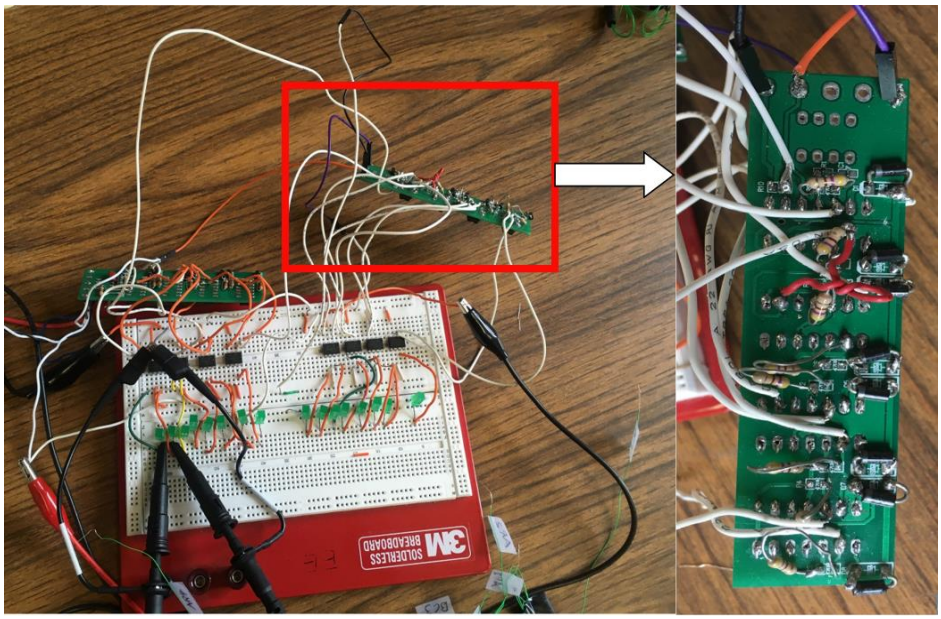


Figure 3.1: Modified PCB implementation.

3.2 Setup of the experimental testing system

Testing contains two different steps. First step was testing the modified PCB for proper operation. The PCB testing of the circuit was done in MWAH 257 optoelectronics research lab using the available equipment.

Second step was integrating the PCB with the artificial skin sensor array and DA system to ensure proper functionality. It was done in same research facilities with colon simulator. Following equipment is used during the testing. The testing system includes function generation, the power supply, the digital oscilloscope, the sensor array, the circuit on PCB as well as the DA reader.

Function generator (Protek B8003FD) shown in Figure 3.2, was used to provide the clock signal to the circuit. The function generator had a range of 3 MHz We have used a clock signal ranging from 1Hz-1MHz to test the circuit. It was necessary to make sure that the circuit can work with very low frequency. Faster operation is also available in case of any future requirement.

Figure 3.2: Function Generator.

The power supply (BK precision 1670A), shown in Figure 3.3 was used to give power to all the flip-flop IC 74LS74N chips in PCB boards. It was also used to create the pulse that will move through the circuit to get the required results.

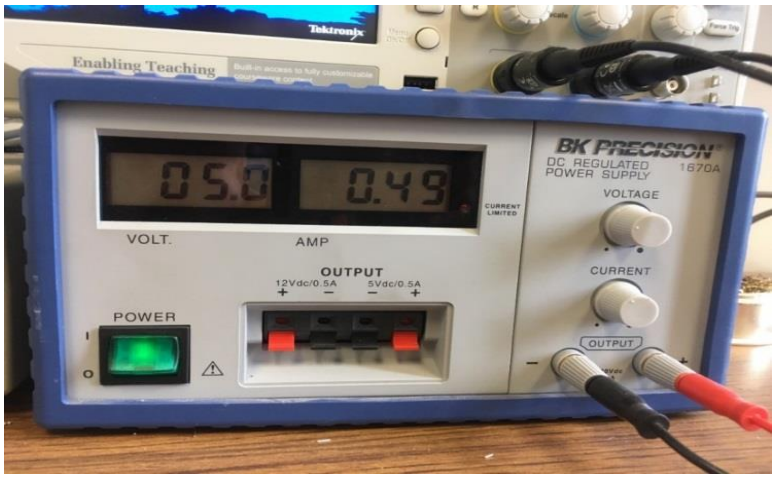


Figure 3.3: Power Supply.

It was used to view the final signal outputs in real-time. We have used two different oscilloscopes (TBS 1052B and TBS 3012B). Figure 3.4 shows the oscilloscope (TBS 1052B).

Figure 3.4: Digital Oscilloscope.

The testing setup used in the lab is shown in Figure 3.5. It shows the cascaded two PCBs to get 16 pulses as power supply to the sensor array grid and DA System to test the circuit as mentioned in the sections above. Figure 3.6 shows the testing setup with colon simulator.

The tested setup was successfully demonstrated and we have found the corresponding color change on computer terminal while the pressure sensor was measuring the contact pressure in the sensor array grid.

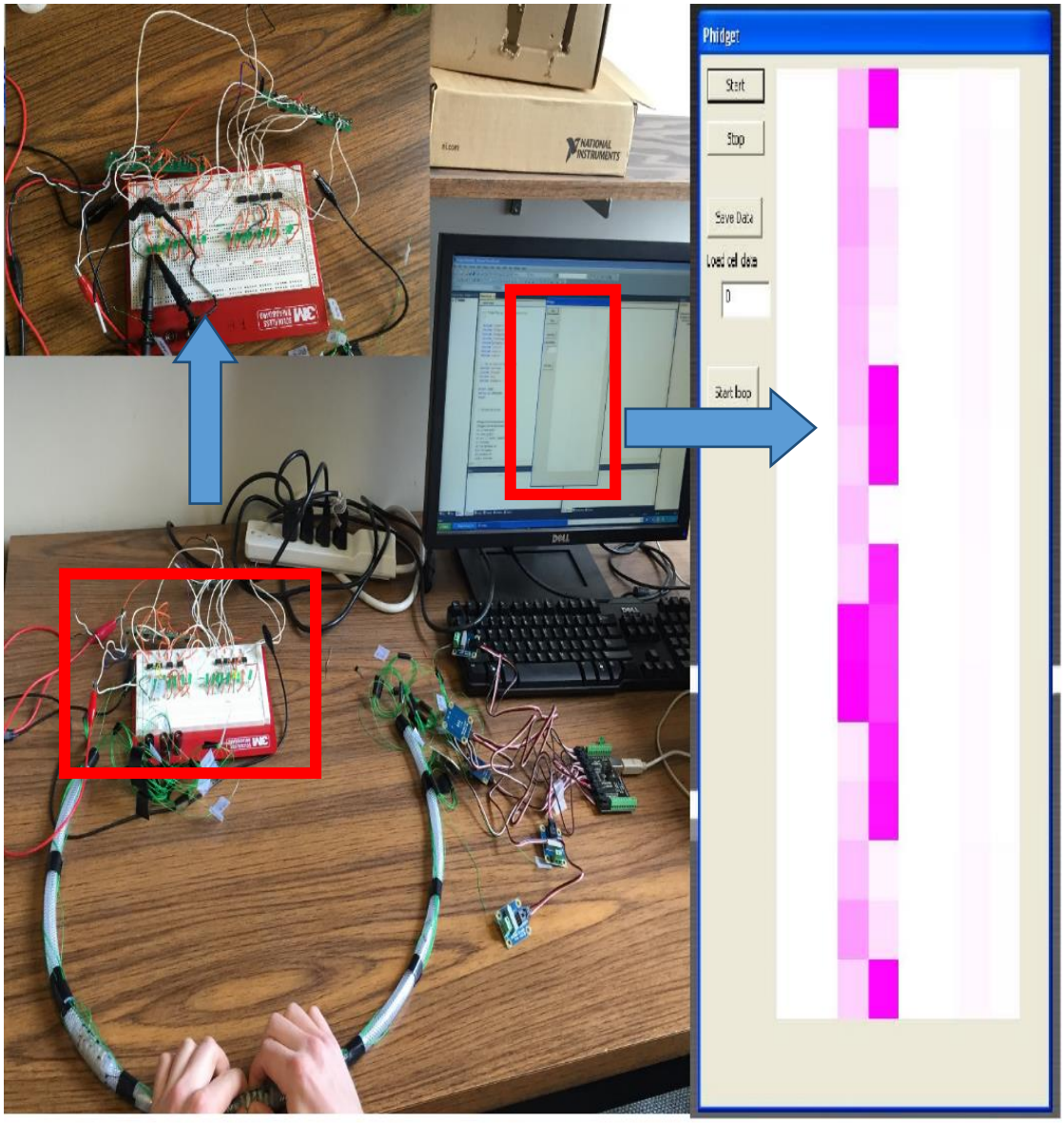


Figure 3.5: Testing setup.

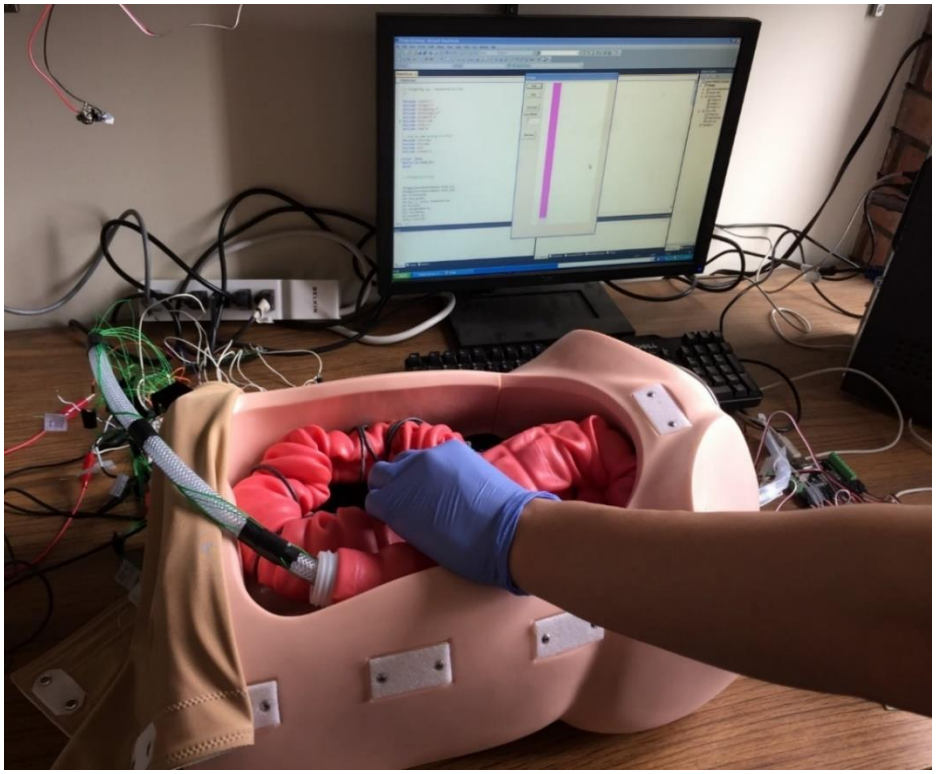


Figure 3.6: Colon simulator shows contact pressure demonstrate the color change in computer terminal.

3.3 Testing Procedure

We performed the testing with the following steps:

1) The function generator, power supply, the Digital Oscilloscope and artificial skin like sensor array were used to test the circuit.

2) The components were assembled on the PCB board and were connected using wires.

3) The supply to the circuit was given through a power supply.

4) The function generator was used to give the clock signal to the circuit.

5) The working of the circuit was verified through LEDs installed in breadboard and also from computer terminal where applying pressure corresponds to the color change.

3.4 Testing Results

We have found the expected response from testing. From modified PCB implementation, we have got desired output pulse sequences. Figure 3.7 shows the output waveform displayed in oscilloscope with low clock frequency. X-axis belongs to time interval whereas Y-axis represents the voltage. We can see that channel1 displays a voltage pulse with amplitude 5.0V and the width is equal to period of one clock pulse.

However, the pulse has some noise added to it. This is due to the soldering, to place the components in PCB and can be avoided in microchip design. Soldering in PCB, increases contact resistance and output is susceptible to noise.

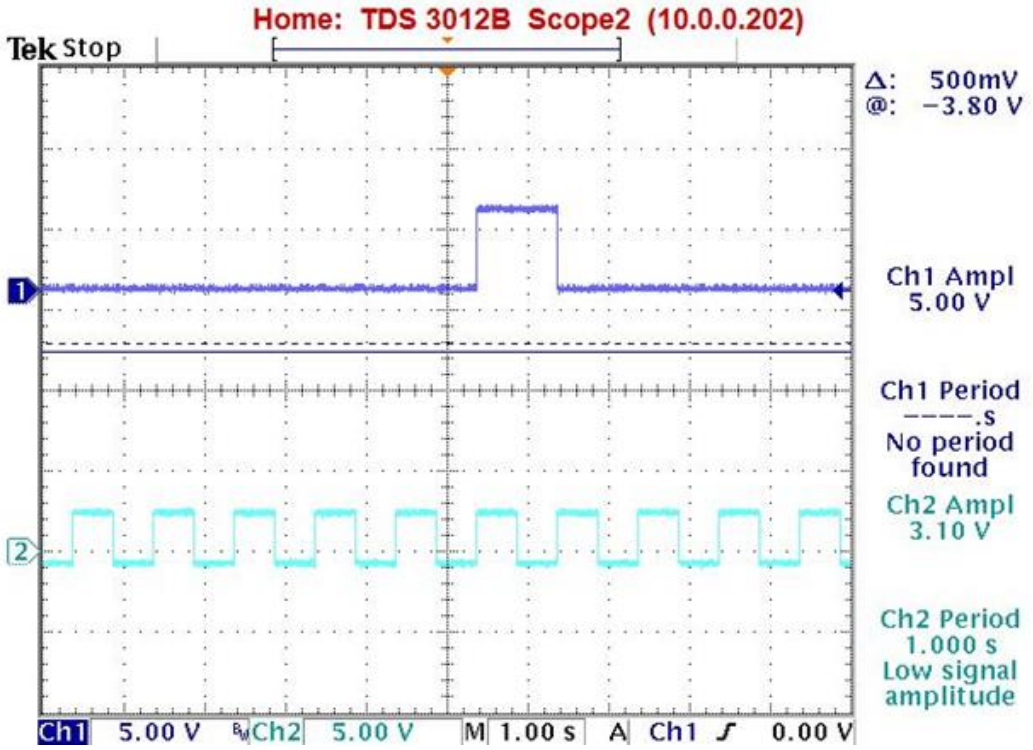


Figure 3.7: Oscilloscope screenshots for 5V amplitude in 1 Hz clock pulse.

The width of each pulse is equal to the width of each clock pulse. The frequency of the clock is 1Hz. The time of each clock pulse is 1.0sec (T=1/f).

Chapter 4 Design of the Microchip for Sensor Array

In this chapter, we demonstrate the circuit design methodology, the major function of the components in the circuit, the software support for designing and making layout of the circuit. Each output pulse should give 5V as High level and 0V as Low level. We have used two different technologies (tsmc025 & AMI0.5) to make the micro-chip and adopted the one which meets the best project requirements. When we designed the circuit for micro-chip, interestingly we found that some property of the semiconductor is different than the long channel devices. We had to adjust some components to get the desired response.

There are some approaches in designing Integrated Circuits. One is full custom design and another one is semi-custom design. In full custom design, the increase in complexity of Integrated Circuit raises the design challenge enormously. There are some design automation tools to implement complex circuits. However, if we had to use the design automation tools, we will lose some customize features like speed, performance to save design time. In fact, in very complex circuits it's pretty impossible to make the layout using full custom design. Fortunately, our designed circuit is not very complex. We have designed the integrated circuit using full custom approach to meet the specific design requirements.

The core part of our design is D flip flops. We have cascaded D flip flops to get the shifted pulse sequences. The primary circuit is adopted from basic serial in parallel output (SIPO) shift register [24].

4.1 Design Requirement

The circuit should provide 5Vpp voltage pulses sequentially to multiple contact terminals of the sensor. Each pulse should keep constant for 500ms in order to provide enough time to the DA system to read the data from the sensor array grid. Below are the key factors which we followed in our circuit design-

i) 5Vpp output pulse sequence.

ii) There should be 16 outputs in each microchip which is based on our current sensor array grid.

iii) If necessary, microchips can be cascaded to meet the flexible grid sensors array.

iv) It should operate in a very low frequencies i.e. 1~5 Hz

v) If faster DA system is available (i.e. in MHz range), the microchip should also support that.

The expected output patterns are shown in Figure 4.1. A number of such circuits, when connected in series, should follow the sequence. The main challenge was to synchronize the pulse sequences. The second output pulse should start only after the first one stops and so on. At the end, when the 16^{th} output pulse stops, then the first circuit will start back again and the sequences continue.

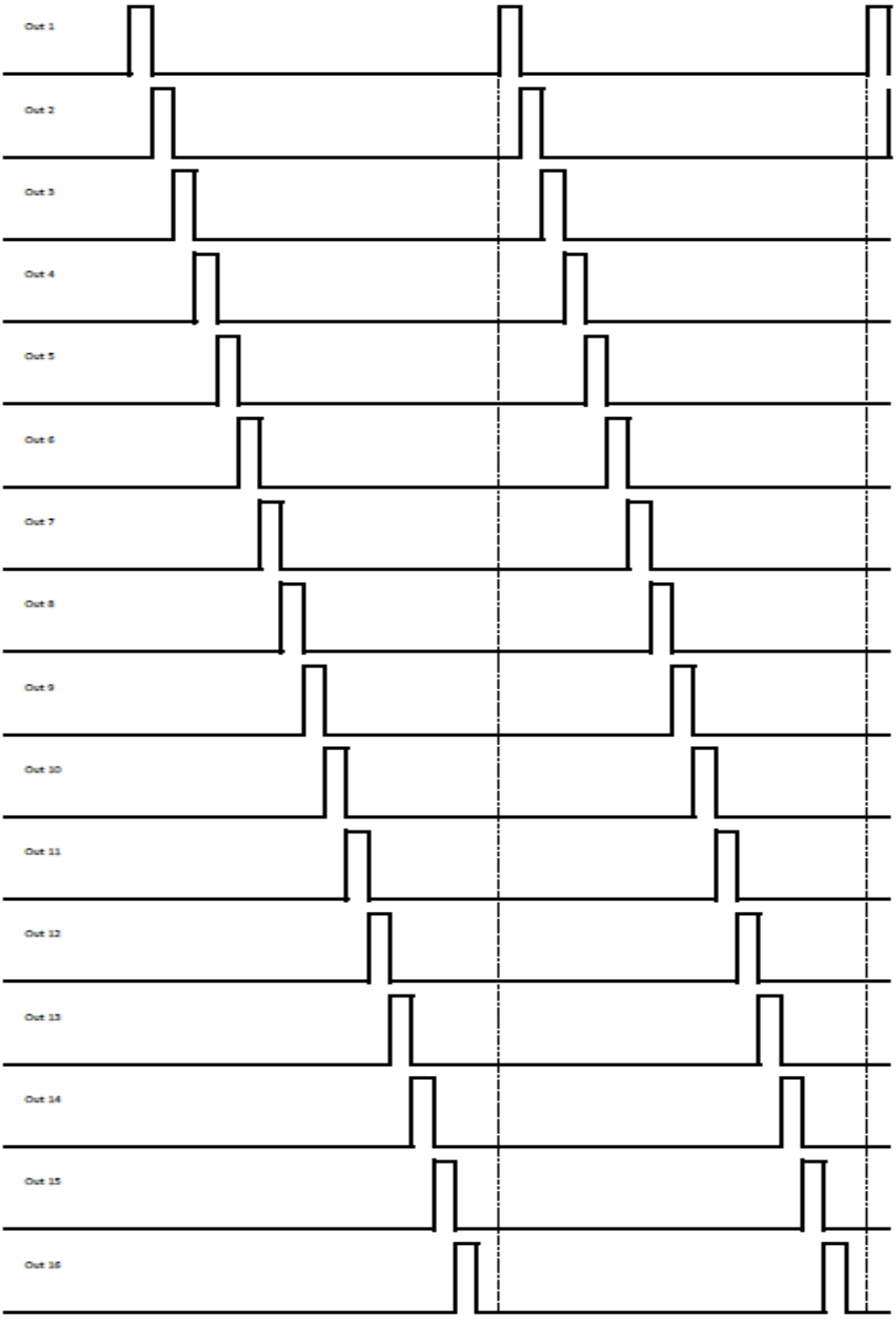


Figure 4.1: Expected 16 outputs.

4.2 Design Methodology

The main function of the circuit was to give a series of pulses. So D flip-flops were used in the circuit. D FF consists of NMOS and PMOS transistors shown in Figure 4.2.

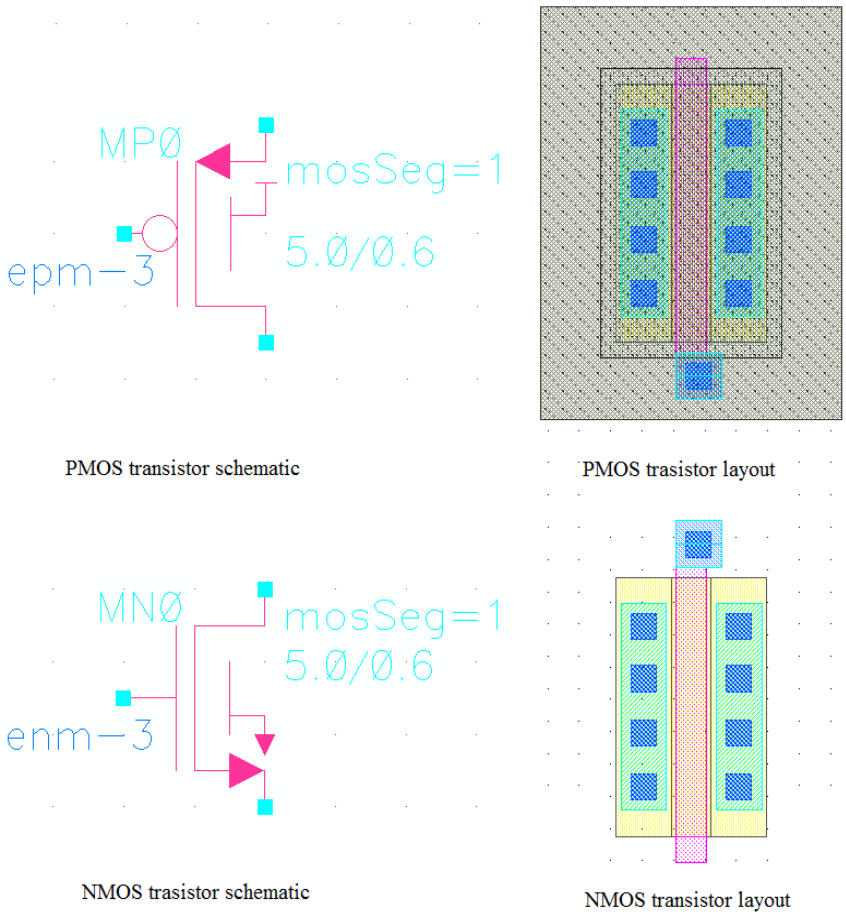


Figure 4.2: NMOS, PMOS transistor in schematic and layout.

As it is required that one pulse should stop before the start of the next pulse, it is necessary to use some kind of switch so that the pulse will remain ON only for one clock cycle and will go down to zero at the next cycle. In earlier version of the design, they have used diode instead of NMOS switch. Although the diode is one-way switch, the issue with diode was to drop 0.3V across the diode itself to activate this switch and output low level comes to 0.3V. This problem gives poor logic low value of the pulse.

Ideally we intended to bring the pulse to or as close as possible to zero. That's why we have used NMOS transistor as switching device to control the pulse sequences.

The amplitude of the pulses was required to be 5Vpp, so we used the ON SEMI C5 (previously known as AMI0.5) technology shown in Figure 4.3.

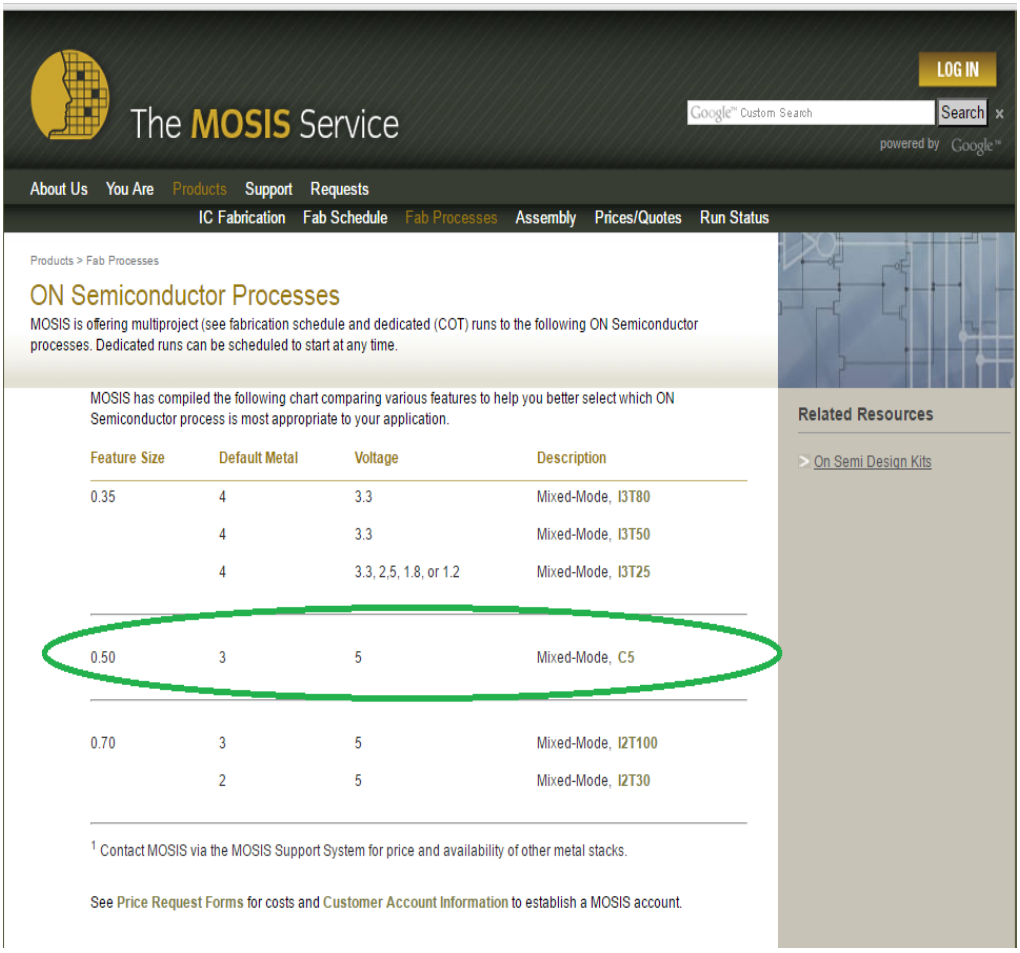


Figure 4.3: ON SEMI featured technology with operated voltage.

There is one resistor to limit the input current into first D FF to control the pulse to get the desired sequence. The value of the resistor has chosen between 10~ 20 KΩ in order to bring the input of D FF to zero after first clock cycle. Further, we will analyze details of D FF.

4.2.1 Designed D Flip Flop with high noise margin

Figure 4.4 shows the transistor level circuit design of our designed D FF. It is modified from C^2MOS. It serves the features from C^2MOS i.e. clock-skew elimination, as well as having high noise margin [25].

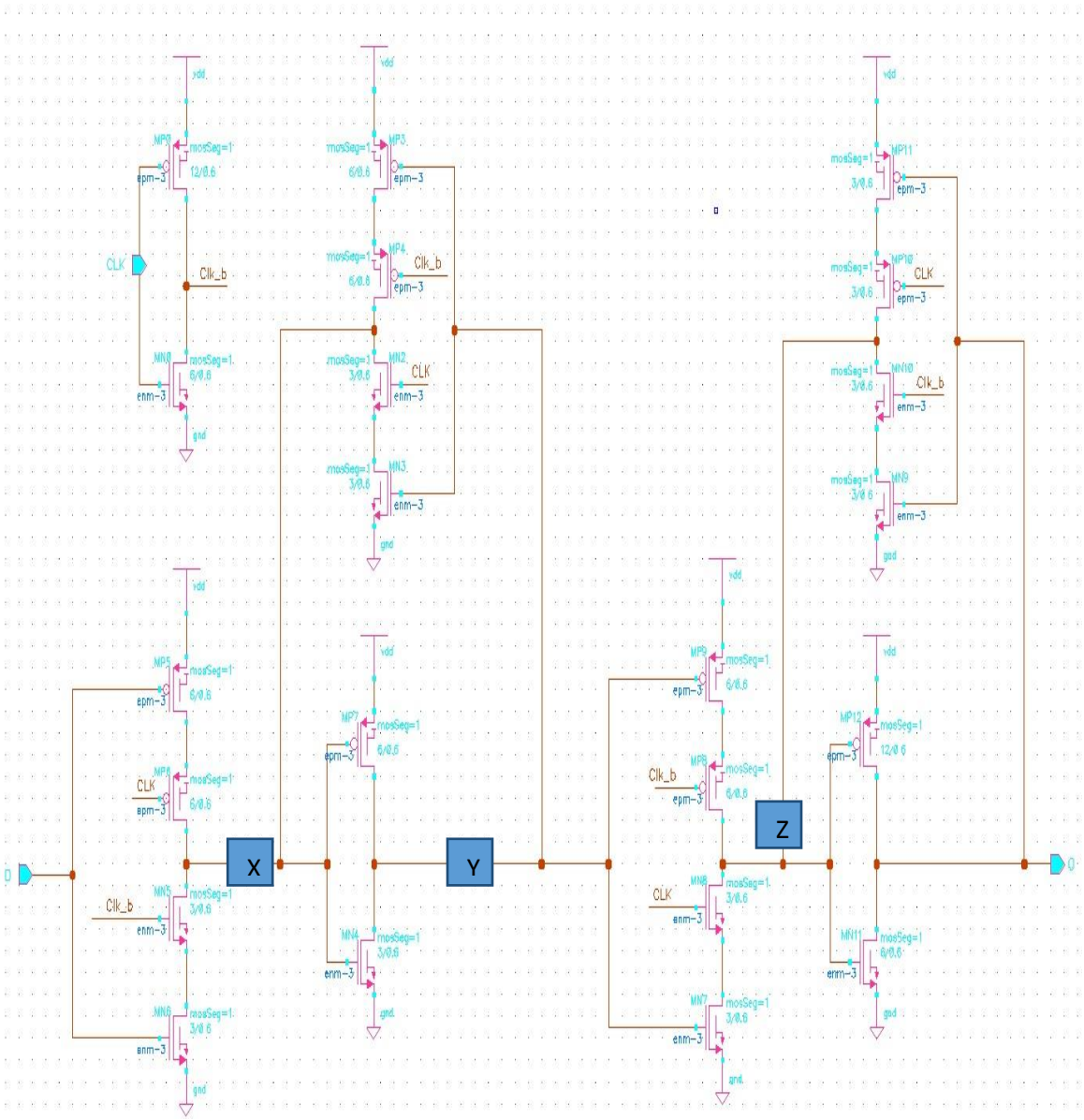


Figure 4.4: Standard D FF used in our designed circuit.

When CLK=0 (CLK_b=1), the master stage act as transparent and inverted version of input D will be available at point X, which will be inverted again and point Y will get the

original D input. When CLK=1 (CLK_b=0), the master stage will be cut off and the value at point Y will propagate to output Q.

Now there are several cases we have to analyze to ensure proper circuit operation.

1. During the 0-0 overlapping period CLK_b will turn on MP4 transistor and if Y (i.e. input D) has low value, it will charge the point X to high and further maintains the low value at Y after inverting. This will bring the point Z to become high and output Q will be low. Low value at point Q will activate the upper configuration of point Z and Q, and will keep high value at point Z. Thus ensuring the output Q to be stayed at low.
2. During 0-0 overlapping period and if Y (i.e. input D) has high value- the upper configuration of point X-Y will be cut off and X will stay at low value ensuring point Y having high value. The slave stage will be isolated from Y (i.e. input D). The output will hold the value through the upper configuration of point Z and Q.
3. During the 1-1 overlapping period, if the input D has low value, the master stage as well as the upper configuration of point X and Y will be cut off, ensuring un-impacted low value at point Y. This will cut off the slave stage and output will hold it previous value.
4. During 1-1 overlap and D has high value- X will have low and Y will have high value, which further ensures the value at X point to stay low. As Y has high value, it will activate the slave stage and at point Z will be low and Output Q will be high. This will further bring the point Z to low through the upper configuration and stabilize output Q to high value.

Hence, the clock overlapping is not an issue with this standard C^2MOS design and we have decided to proceed in our microchip design with this D FF.

4.3 Design Schematic with Cadence®

Cadence® is an industry standard and used commercially in VLSI micro and nano fabrication. Before making the layout for fabrication, one should simulate the circuit so that a number of prototype iterations can be saved and better circuit can be finalized.

We have designed the circuit with only two output pulses to ensure the working logic, as shown in Figure 4.5. The input to the first flip-flop is connected to the power supply through a 10KΩ pull-up resistor. So, initially it goes high because it is connected to the power supply. After the first clock cycle, output of the first flip-flop (output1) goes high. The high value is fed to the gate of NMOS transistor. The source of NMOS is connected to ground while drain is connected to D of 1st FF named '**ForceNode'**. As gate is high, the drain and source of NMOS will be conducting. This makes the **'ForceNode'** to become low; which causes the first output to go low.

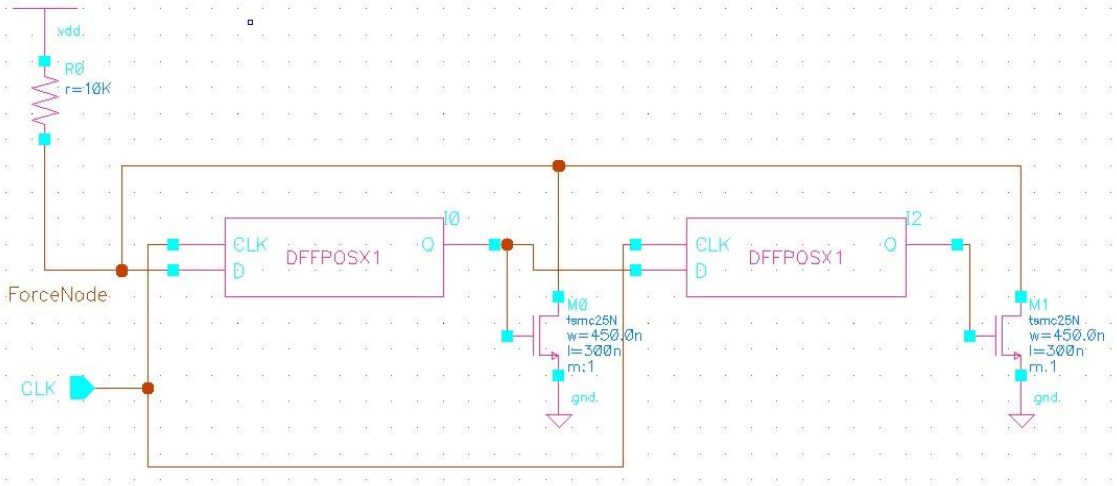


Figure 4.5: First two blocks of the designed circuit.

So, we have a pulse generated from the first flip flop, which is high for one clock pulse. Next, this output pulse is fed as input of second flip flop. Now, we will get the one clock cycle shifted version of out1 as out2. The 2nd NMOS switch after 2nd flip flop will keep the input D of first flip flop in low. Keeping the same operation, we have used total 16 D FFs. With every clock cycle, the pulse generated from 1st FF proceeds through the entire circuit and there is a pulse at each output in a sequence. The corresponding NMOS will turn on, making the ground conducting through Source and Drain, making input D low, not allowing the first output to go high unless the pulse is supposed to go back.

Thus we get the sequential pulses through out1 to out16. At the end of (16+1)=17th clock pulse, the out16 will go low; drain and source of 16th NMOS transistor will not be conducting. So, ground is cutoff from the 1st D input, which allows the **'ForceNode'** to go high again and repeats the sequences.

Figure 4.6 and Figure 4.7 shows the schematic of the designed circuit with flat Transistor level and with D FF blocks, respectively. Figure 4.8 shows the whole circuit block with I/O pins only.

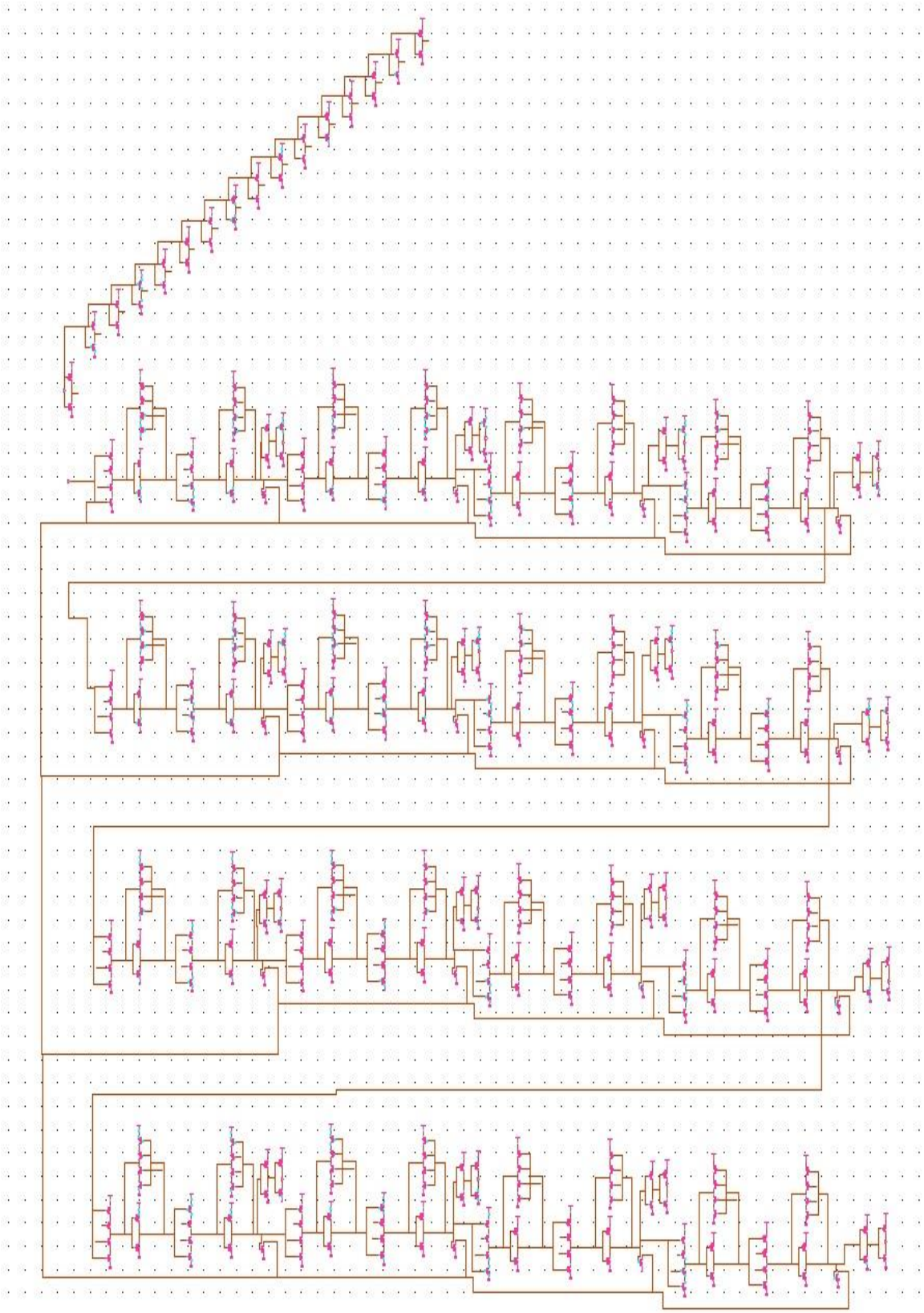


Figure 4.6: Transistor level schematic of the designed circuit in Cadence®.

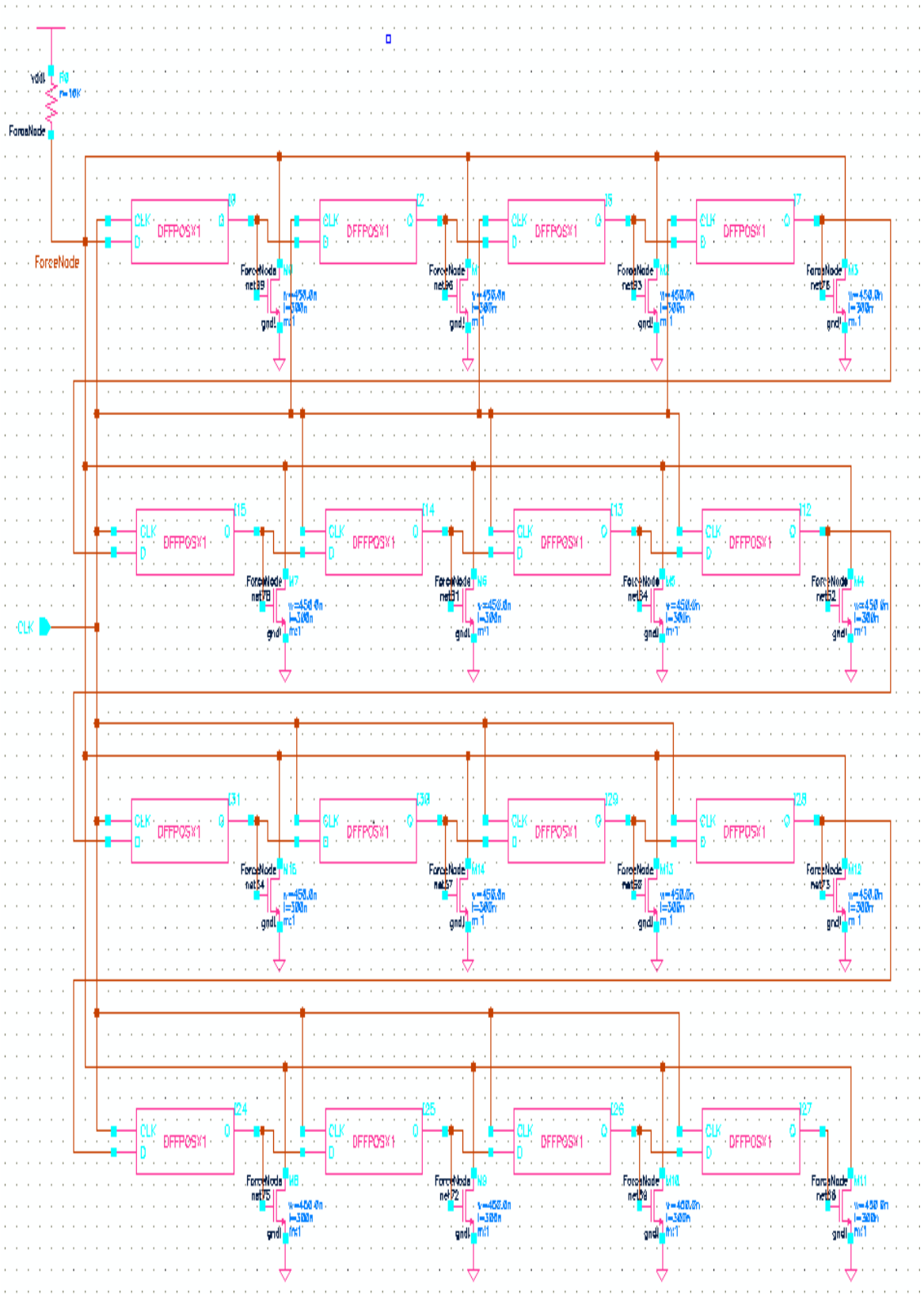


Figure 4.7: Cadence® schematic with DFF blocks.

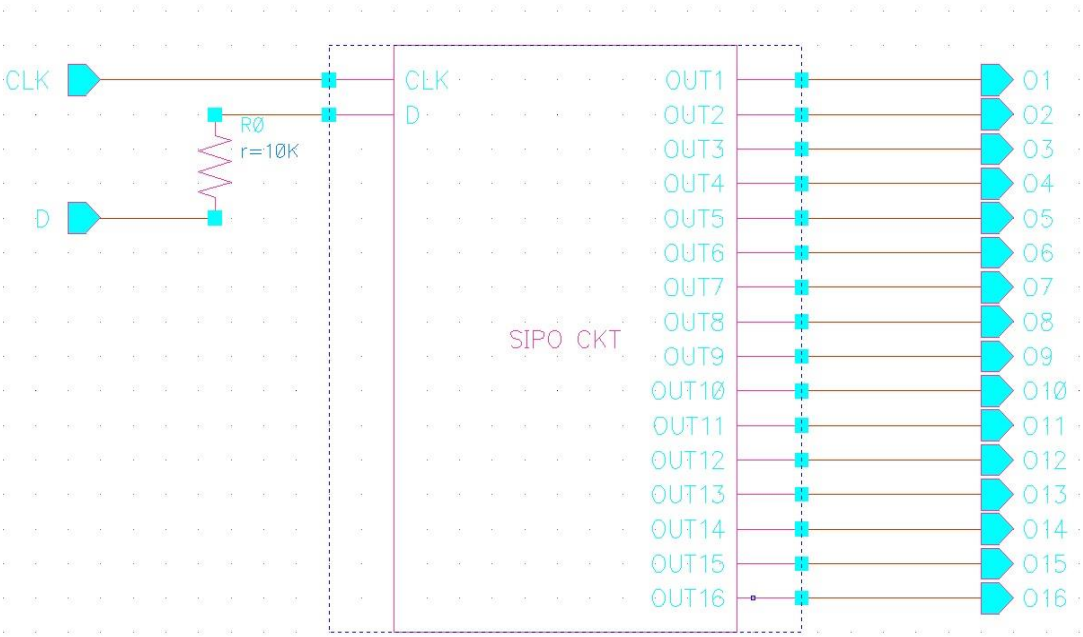


Figure 4.8: Designed SIPO block with I/O pins only.

4.4 Design Layout

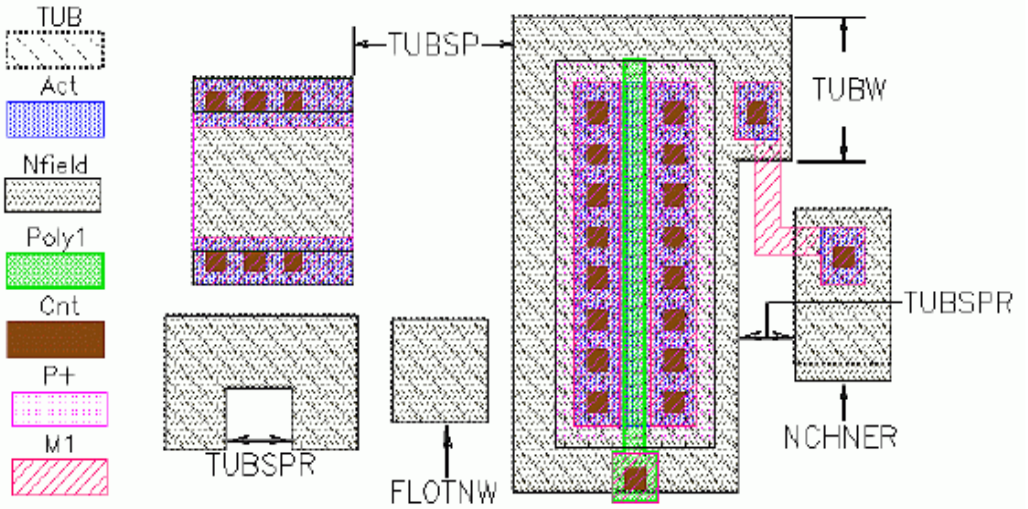
Cadence® layout can be done using Cadence® virtuoso layout editor. There are different technology files, available to fabricate into micro or nano chip. Basics of layout design are almost same in every technology system, except some layer color and naming conventions. The layout discussion we will conduct to follow is for On Semi C5 (previously known as AMI0.5).

Before starting the layout, we have to understand the design rule files. There are some constraints we have to follow throughout the layout design. These constraints are given in the design rule files. For our mentioned On Semi C5 technology, the design rule file is given as "C5X_4500099_RevT" in the provided files from MOSIS (a commercial fabrication company). These constraints are basically saying the minimum distance between edges, minimum width of an object or spacing between two objects etc.

Screenshot of few important rules are given in Figure 4.9 and Figure 4.10.

C5X (0.5 Micron) N-WELL Layout Rules

Layer/level #1 (TUB)



Note 1: TUB layer is drawn to define areas that will be implanted with n-tub implant. (ie N-Well is drawn and implanted over P-substrate).

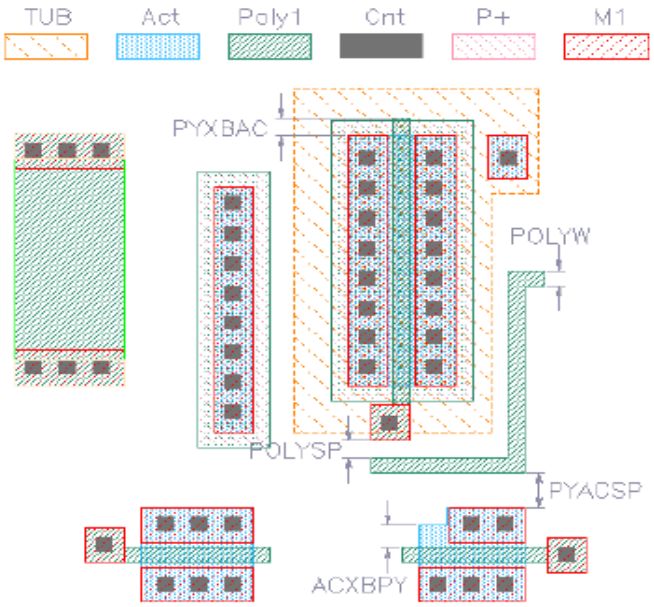
Rule Name	Rule Description	Rule	Units	Rule Type	Notes
FLOTNW	FLOaTing N-Wells			*	Floating N-Wells are those that contain P+ Active contacted to metal that do not have a corresponding N+ well-tie contacted to metal.
FLOTPW	FLOaTing P-Wells			*	A continuous N-Well ring or moat defines a separate island of P-Well, that is floating if it contains N+ active contacted to metal without a corresponding P+ well-tie contacted to metal. (Not shown in graphic above)
NCHNER	NCHaN ERror if nchan is not identical to tub			*	With the exception of the Extended drain devices and N-Field generated for NI Devices.
TUBSP	Min TUB SPacing	4.00	µm	*	
TUBSPR	Min TUB Spacing related	2.00	µm	*	
TUBW	Min TUB Width	2.50	µm	*	Resistor less than 5.00 µm wide do not meet models

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

Figure 4.9: N-well layout design rules.

C5X (0.5 Micron) POLY Layout Rules

Layer/level #4 (POLY1)



Note 1: Poly (aka: P1, PY1, Poly1 or Gate) layer is used to define interconnect, Poly(1) transistor gates, Floating gates in EE devices, resistors and Bottom Cap plates of double poly capacitors.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
ACXBPY	Min ACtive eXtension Beyond PolY	0.65	µm	*	S/D Dimension, must be checked when using butted contacts
POLYSP	Min POLY SPacing	0.60	µm	*	
POLYW	Min POLY Width	0.60	µm	*	
PY1ANT	PolY1 ANTenna check (100:1 ratio)	100.00		*	The ratio of Ply-not(Act) to Ply-Act for a single Poly polygon should not exceed 100:1. (not shown in graphic above)
PYACSP	Min PolY to ACtive SPacing	0.20	µm	*	
PYXBAC	Min PolY eXtension Beyond ACtive	0.50	µm	*	Poly End-Cap Rule

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

Figure 4.10: Polysilicon layout rules.

After studying the rules, we can go to Cadence® Virtuoso layout editor to build the circuit layout. While open a new file in virtuoso layout editor it should have the LSW (Layer Select Window), which represents the layer definitions. Figure 4.11 shows the LSW along with our designed D FF layout.

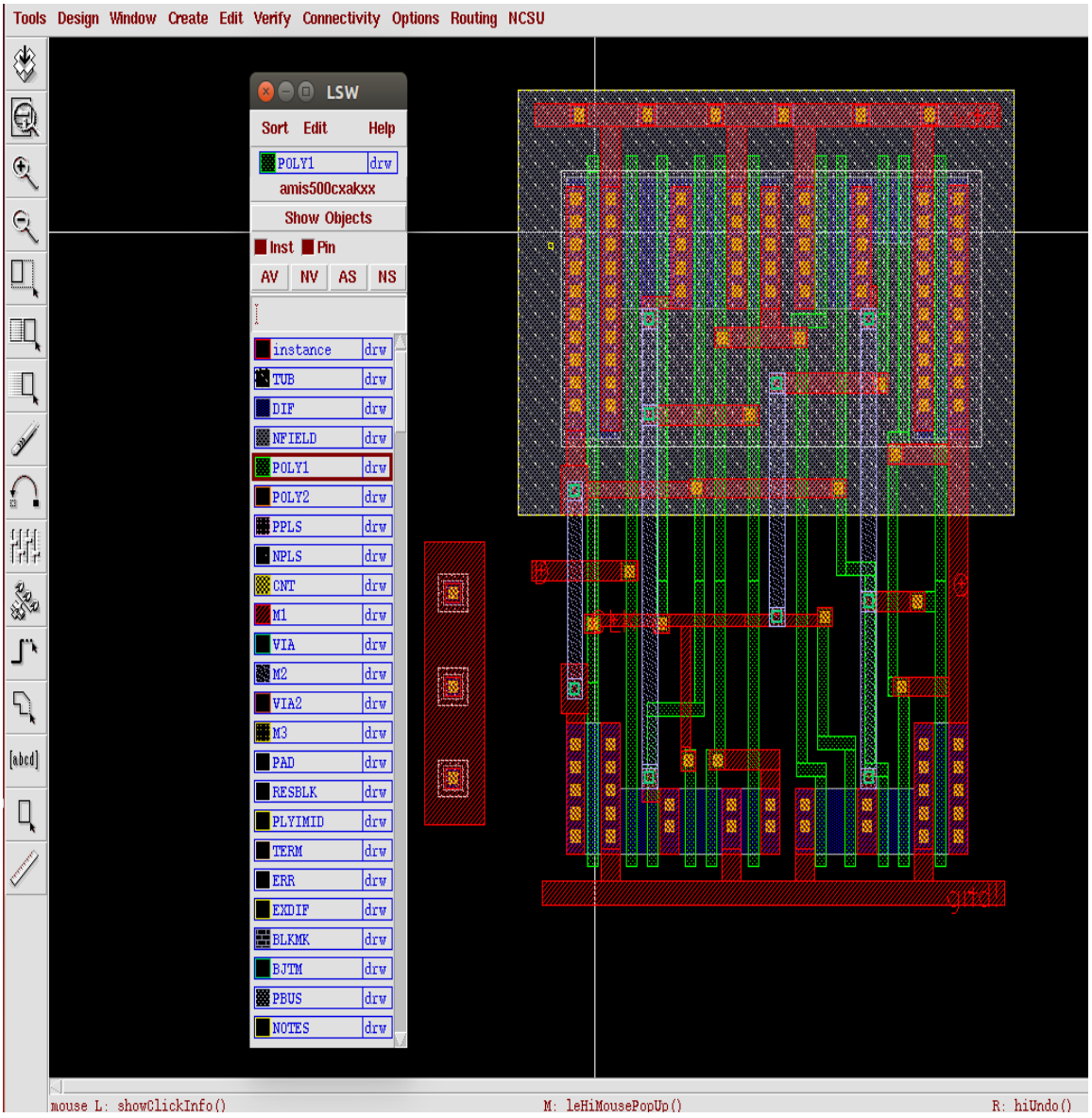


Figure 4.11: Cadence® Virtuoso Layout outlook.

From LSW we have to build each and every transistors consisting POLY as gate; DIF for drain and source. We also have to make substrate connections. To connect them we have to use metal1, metal2 or metal3 and contact holes (i.e. VIA and VIA2). Our first step is to build the basic D FF. Figure 4.12 and Figure 4.13 indicate the D FF schematic and symbolic view whereas Figure 4.14 and Figure 4.15 show the layout and extracted view, respectively.

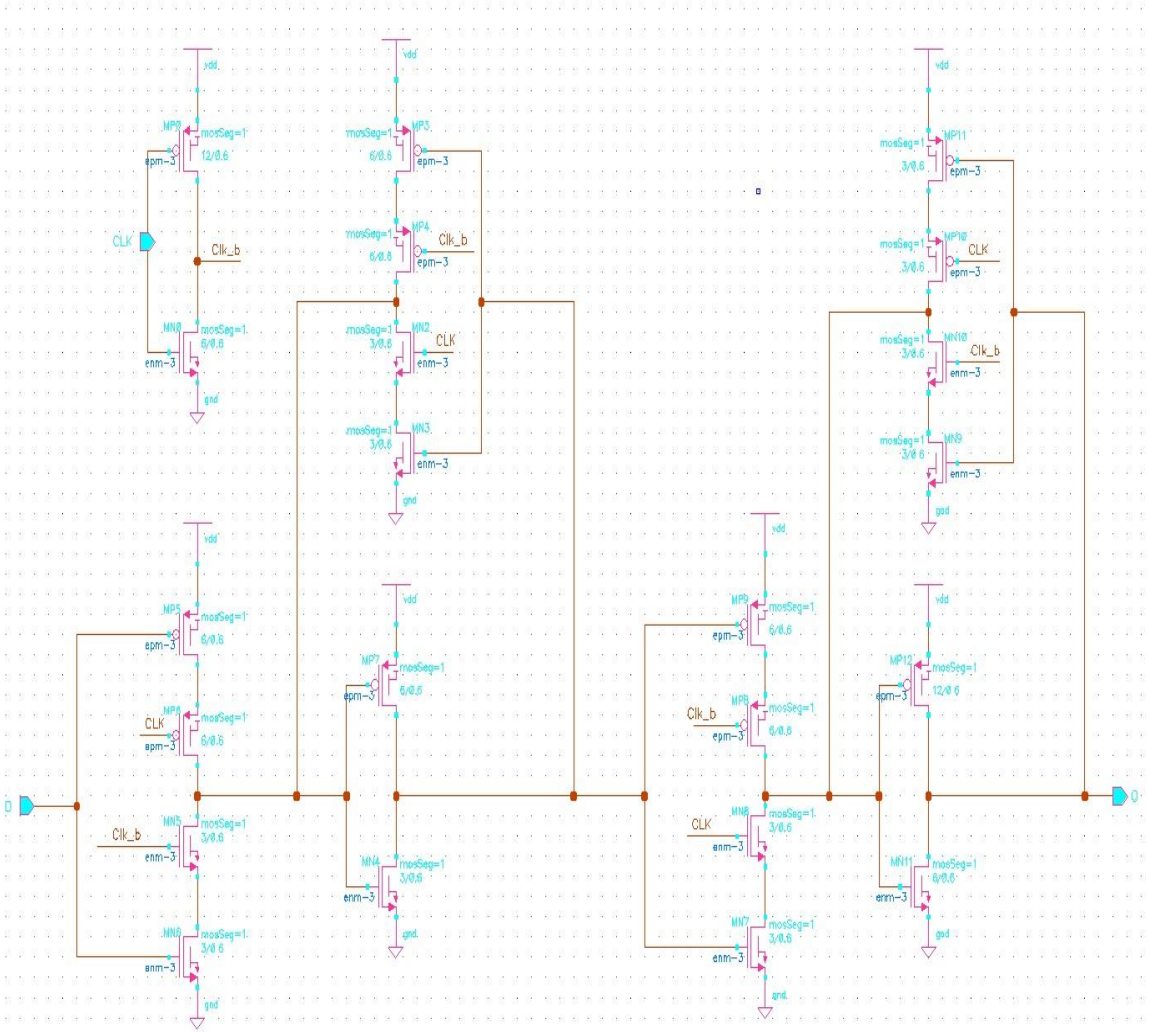


Figure 4.12: D FF schematic.

Figure 4.13: D FF symbol.

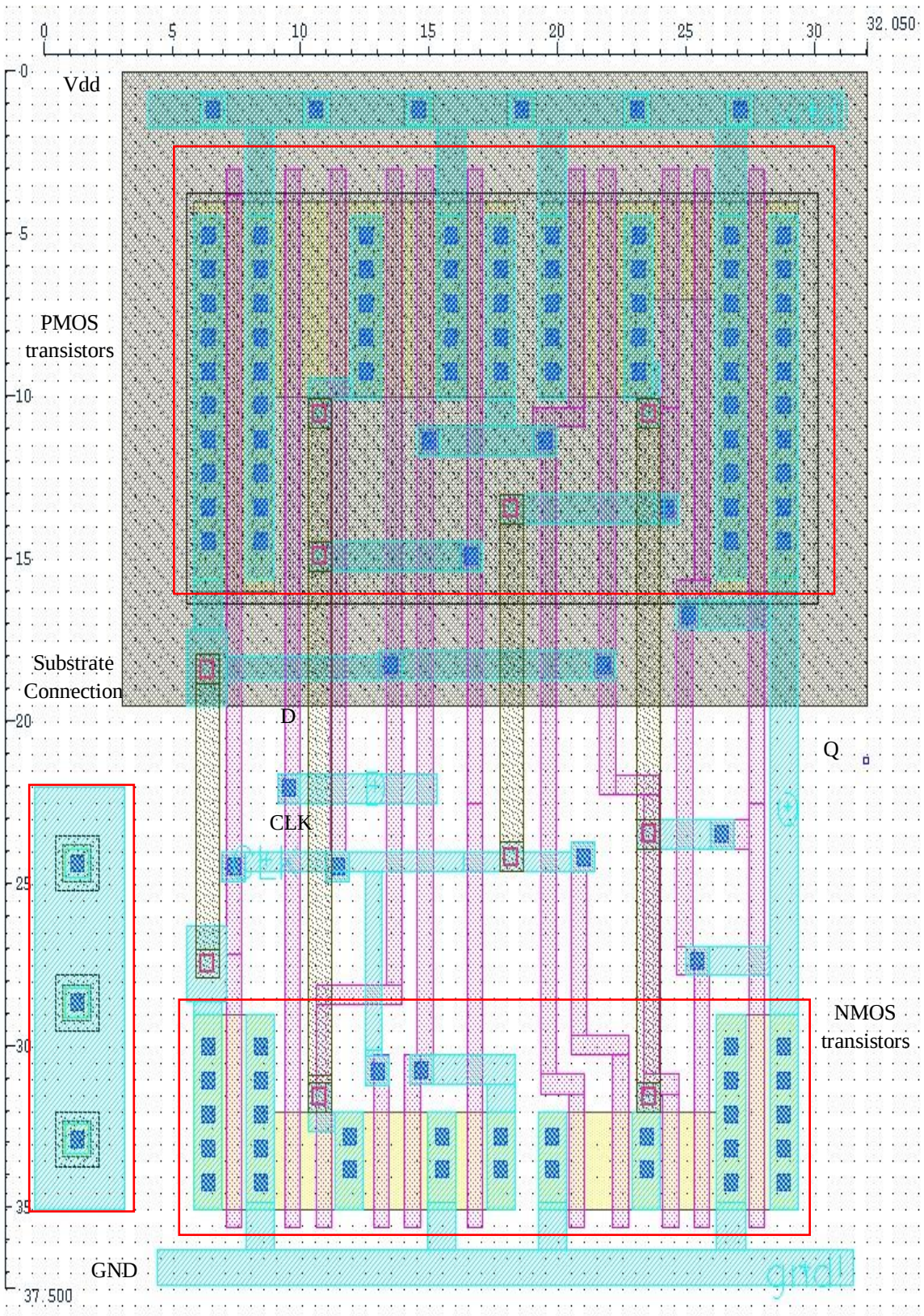


Figure 4.14: D FF layout.

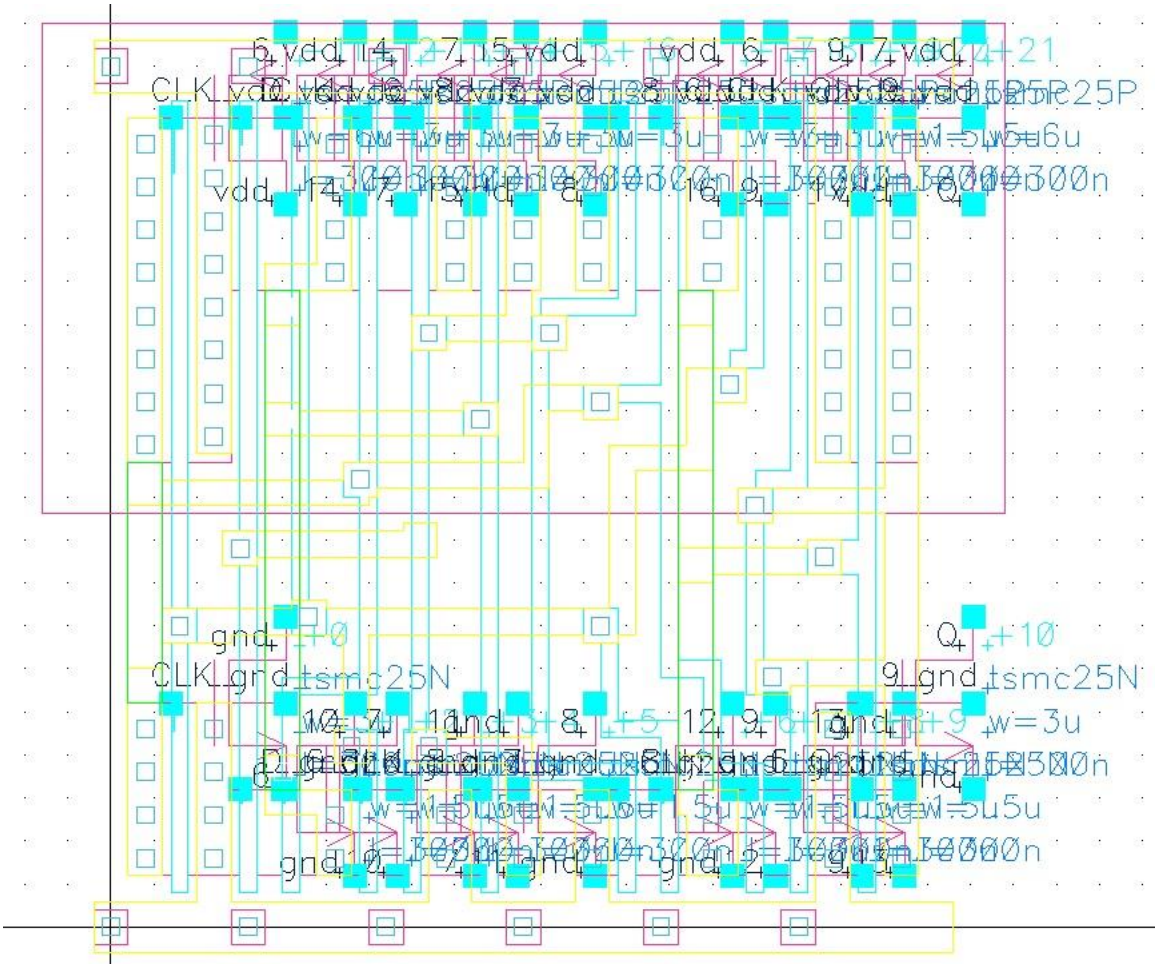


Figure 4.15: Parasitic Extracted view of D FF.

Once D FF layout block is finished, we can use the block to build up the whole circuit. Detail attention has to give while interconnecting the blocks.

After finishing the whole layout for the designed circuit, it looks like as Figure 4.16. Once the layout is finished, the next steps will be design verification, using DRC (Design Rule Check), LVS (Layout Verses Schematic) and PEX (Parasitic Extraction). We will explain the DRC, LVS and PEX process next.

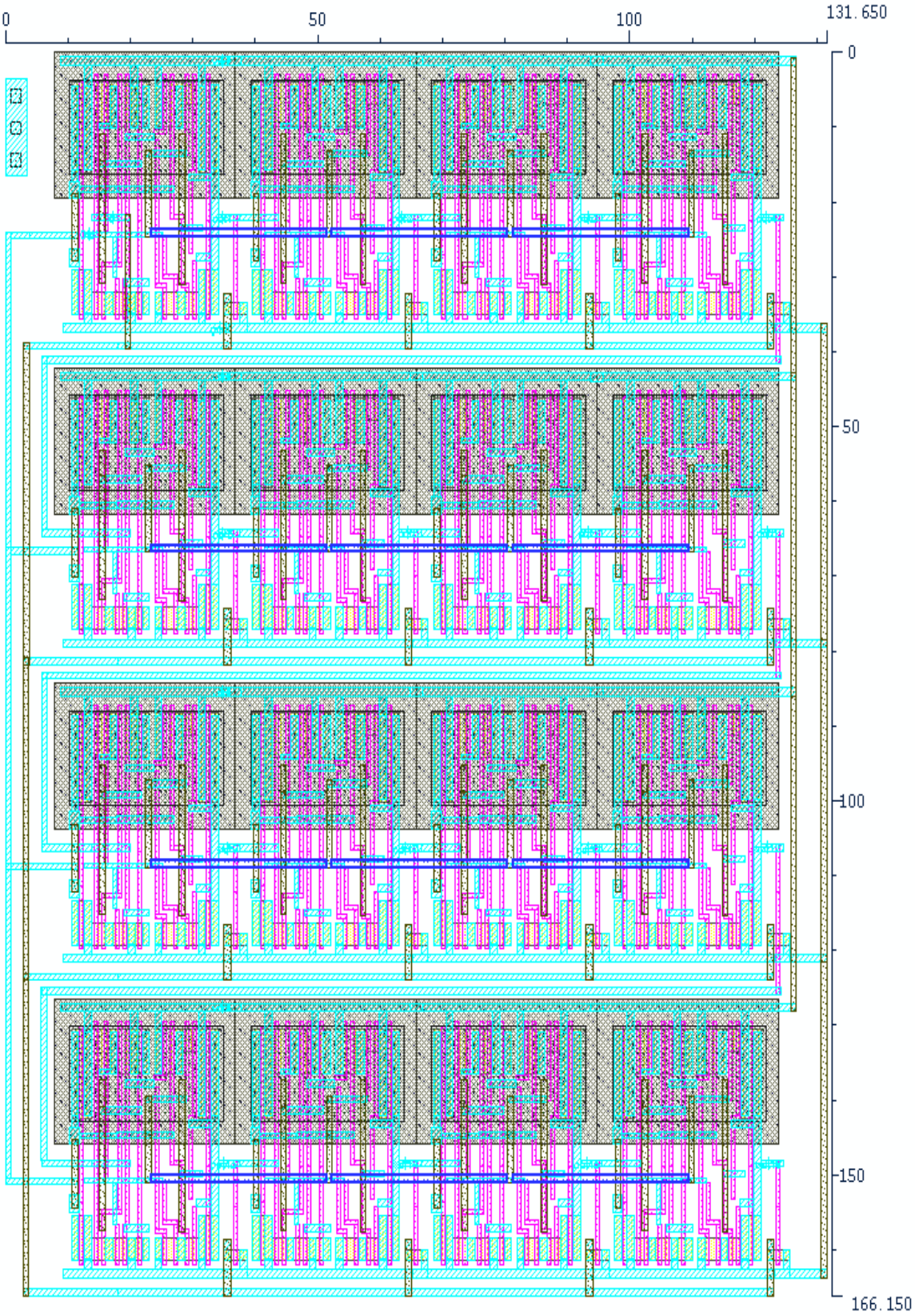


Figure 4.16: Layout of the designed circuit.

4.5 Design Verification

The industry standard for design verification is to use Calibre®, a very powerful software tool from Mentor Graphics. Calibre® performs the physical design verification tasks i.e. DRC, LVS, PEX. Calibre® uses gds files as input to run the verification. The first step will be generating the gds file form Cadence® virtuoso.

Figure 4.17 demonstrates the process.

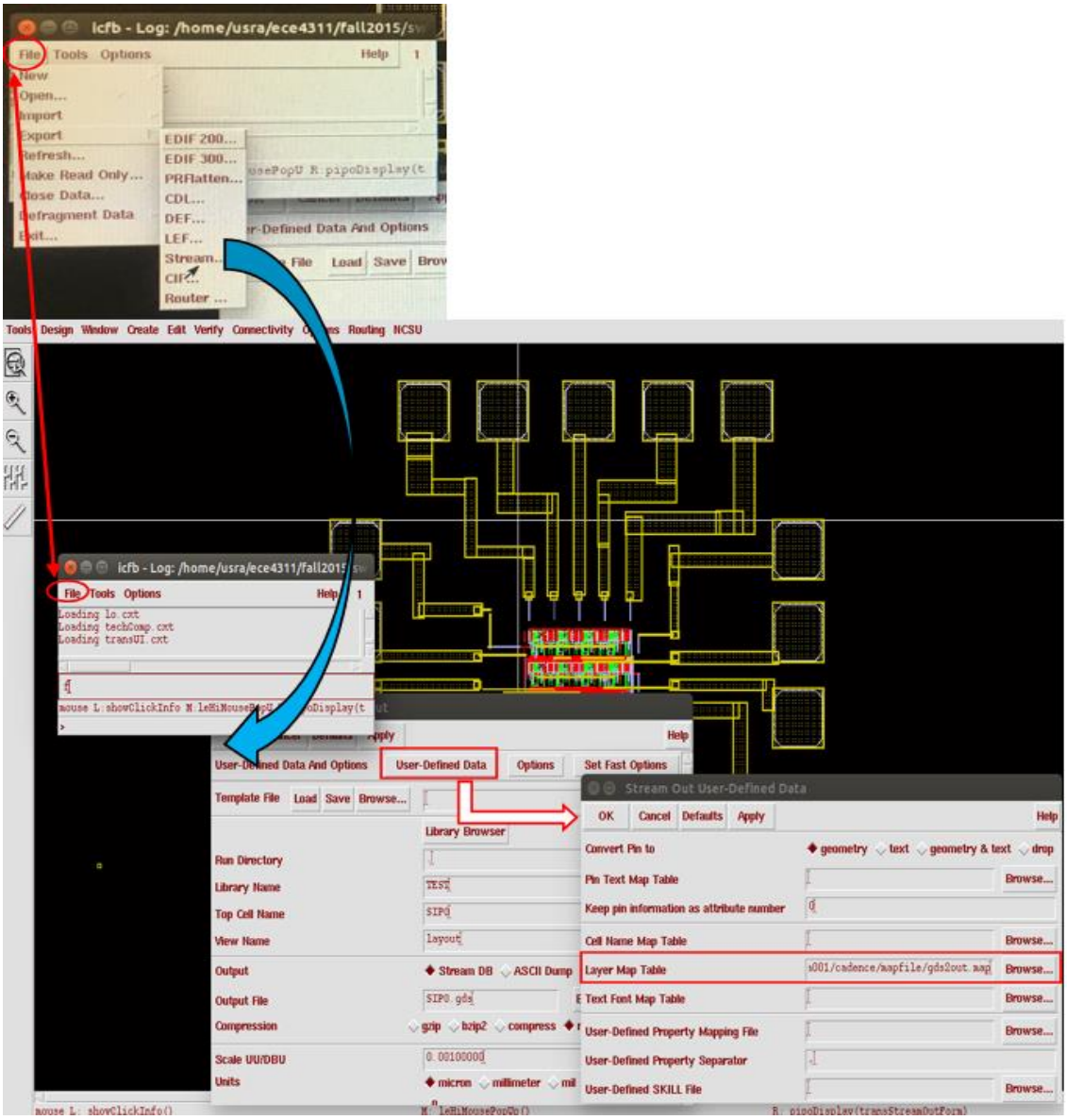


Figure 4.17: Generating gds file from Cadence® virtuoso.

To create gds file we need the layer definition map file, which is ‘gds2out.map’ in our case. Inside of the ‘gds2out.map’ file is shown in Figure 4.18.

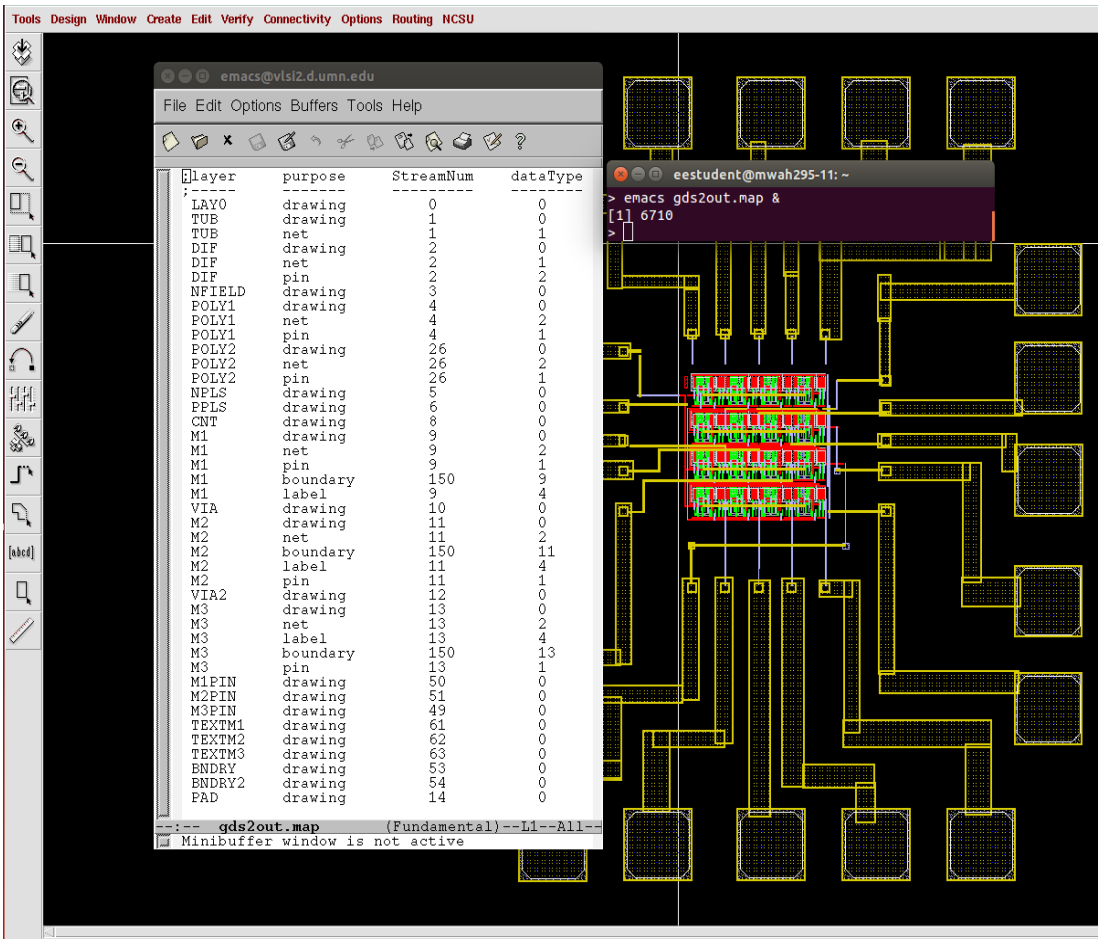


Figure 4.18: Layer mapping into gds map file.

Each layer has its definition as net, drawing, pin or boundary. From Cadence® virtuoso, using the layer map definition we can get the gds file, which can be used with Calibre® software in verification process. While running Calibre®, the interface looks like Figure 4.19.

Figure 4.19: Calibre® interactive interface.

We can start DRC, LVS, PEX by selecting the option from the interface.

4.5.1 DRC-Design Rules Check:

Calibre® will check the design rules against the gds file, and summaries the error into a file. To start, we have to provide the rule file for the specific technology and load the gds file. Then run DRC will check the design rule constraints of gds file. If any constraints are violated, it will return the errors with the specific coordinates, so that we can find the location and correct accordingly.

Typical DRC process is shown in Figure 4.20 to Figure 4.22.

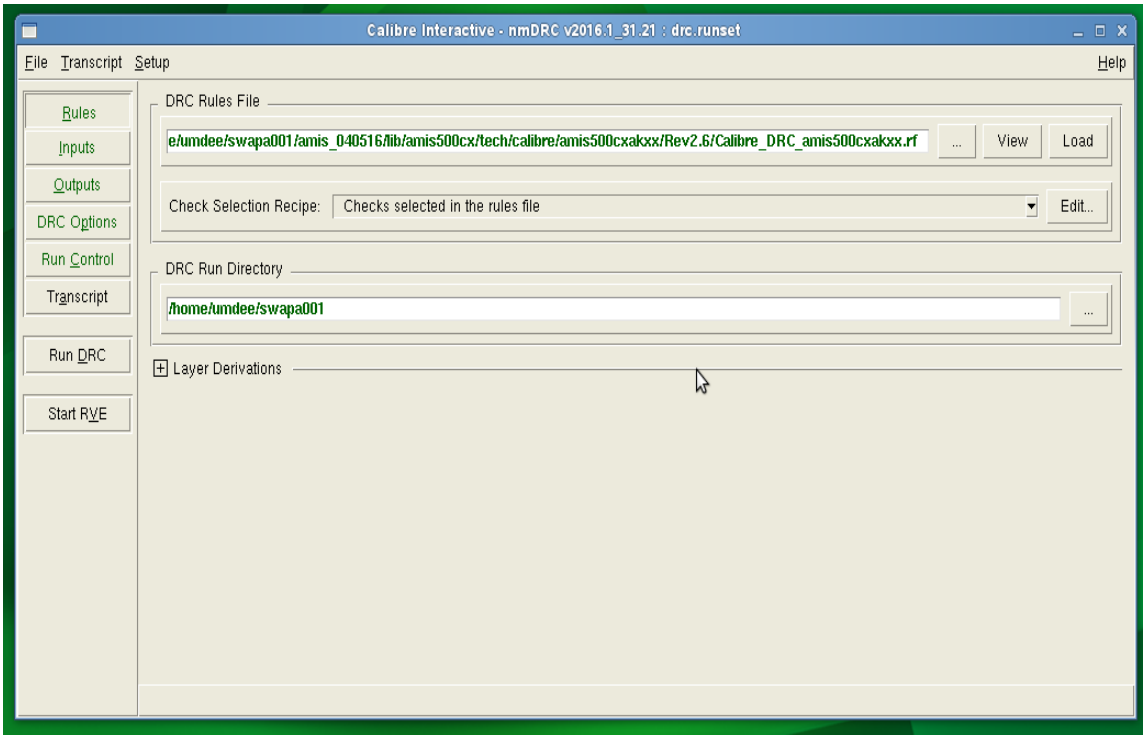


Figure 4.20: DRC setup (rule file insertion).

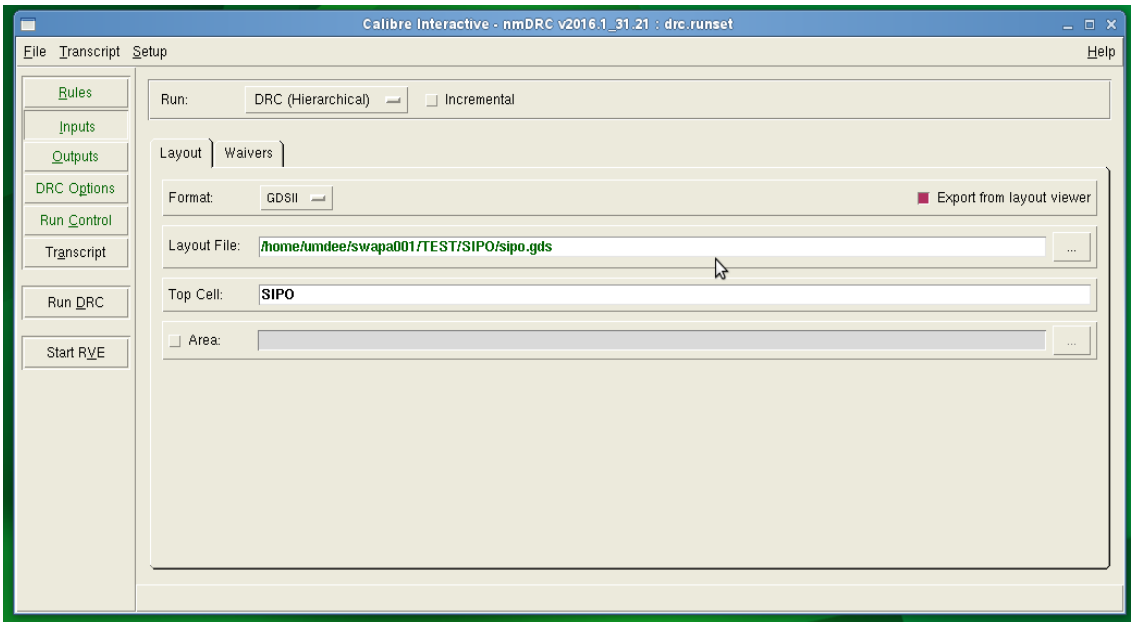


Figure 4.21: DRC setup (input gds file).

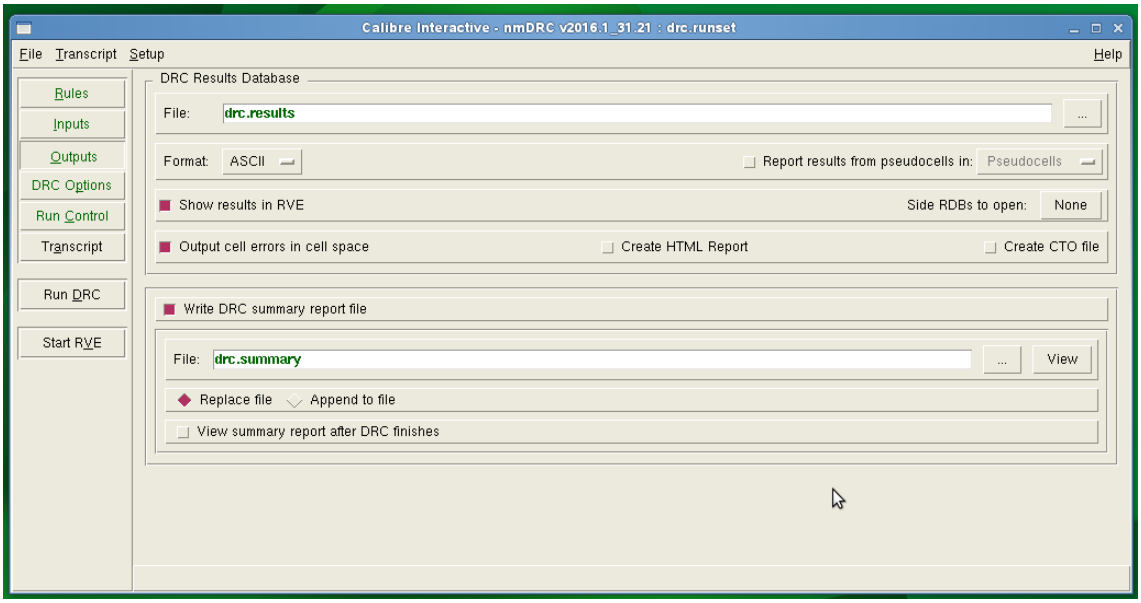


Figure 4.22: DRC setup (output file summary).

While there are errors, caliber RVE will refer to the error type along with the coordinates. Figure 4.23 and Figure 4.24 shows typical DRC errors.

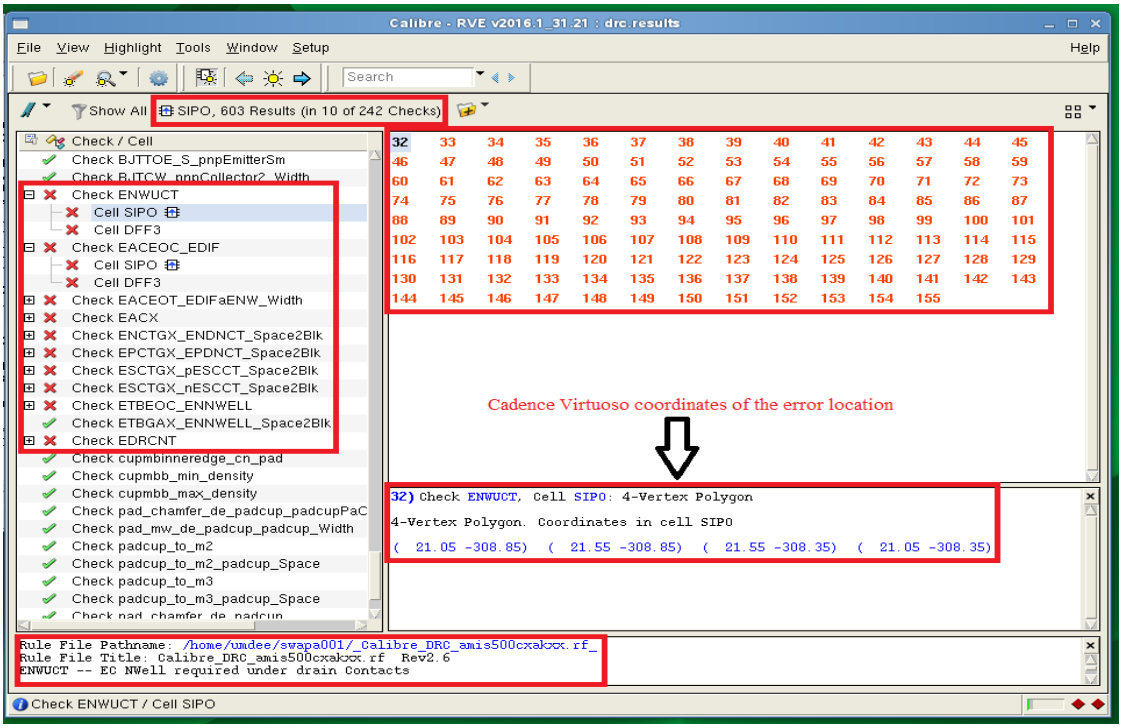


Figure 4.23: Typical DRC error1.

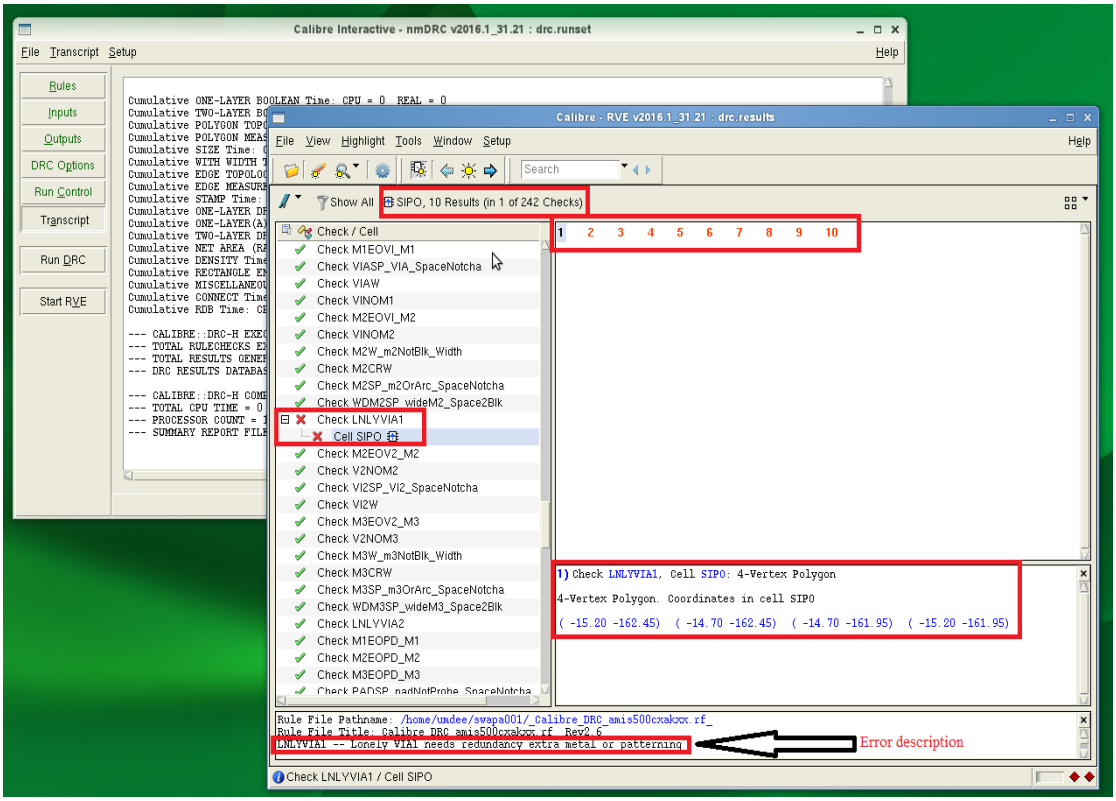


Figure 4.24: Typical DRC error2.

We have to click on the error in ‘check/cell’ and then the number on right window to get error description and coordinates of Cadence® Virtuoso layout. Then, we have to go to the layout, fix the error and follow the same procedure to create gds and run DRC in Calibre® again. We will illustrate the error fixing of the typical DRC error2.

From the error we have the coordinates of the 1st error location as:

(-15.20 -162.45) (-14.70 -162.45) (-14.70 -161.95) (-15.20 -161.95)

The error description says that lonely VIA1 needs redundancy extra metal1 or patterning. If we want to explore the error, we may go back into design rules, where it also suggests the steps to fix the error.

For instance, the design rules file defined LNLYVIA1 as: “Via in a corner or at the end of a wire with minimum metal surround, has no redundancy, has no metal patterns within 8u.” The suggestion to fix the issue: “extend metal past via in opposite directions by 0.7u or place metal wires or patterns within 8u from the edges of the via or place a non-lonely redundant via.” Figure 4.25 shows, the LNLY VIA1 error location. Figure 4.26 shows the redundant extra metal1 layer to fix the error.

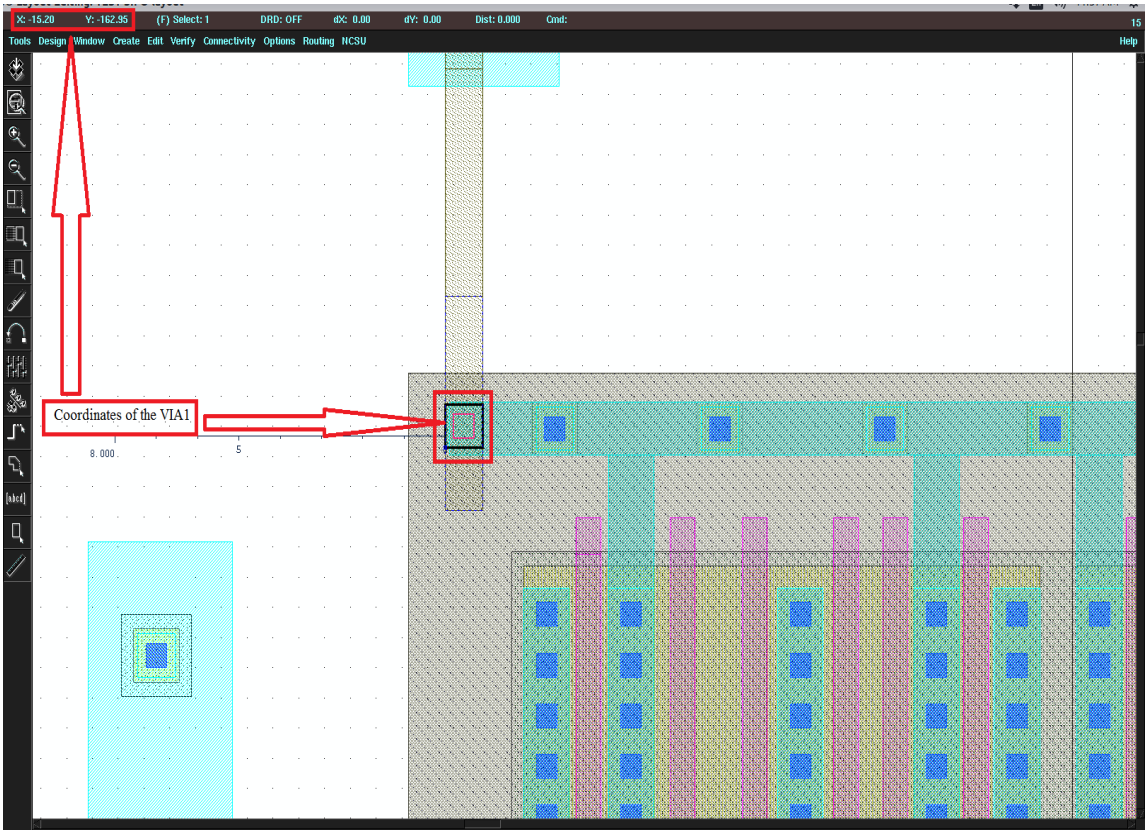


Figure 4.25: DRC error (LNLY VIA1).

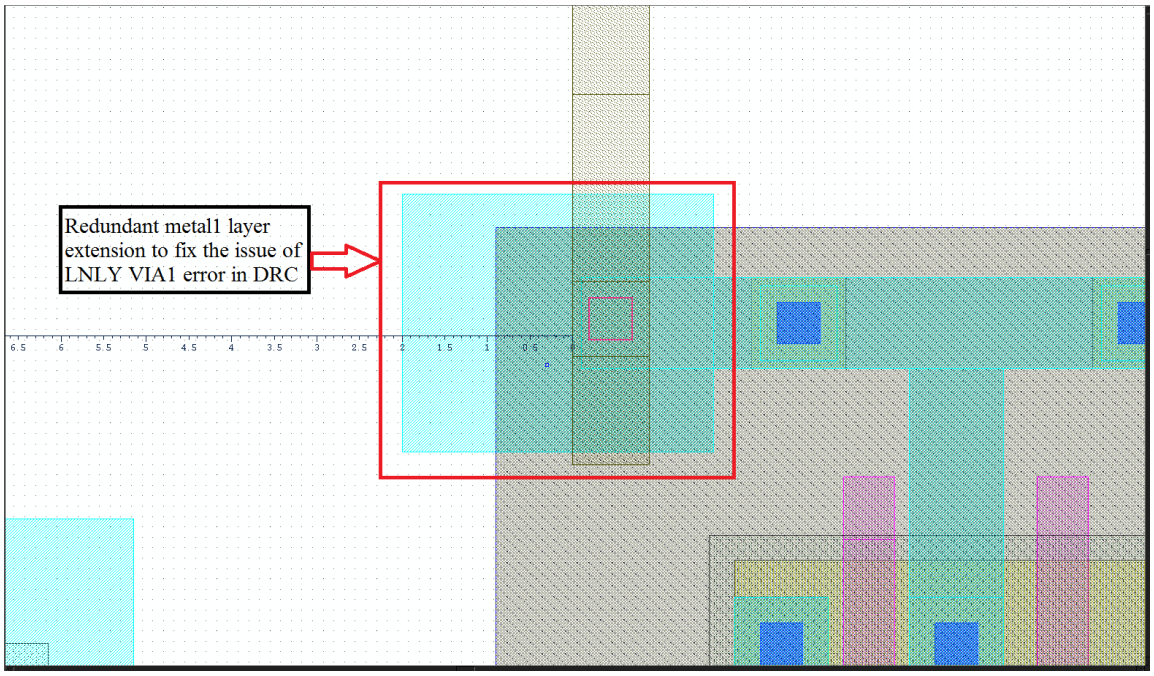


Figure 4.26: Fixing DRC error (LNLY VIA1).

After fixing all the errors, the DRC should give clean RVE as Figure 4.27.

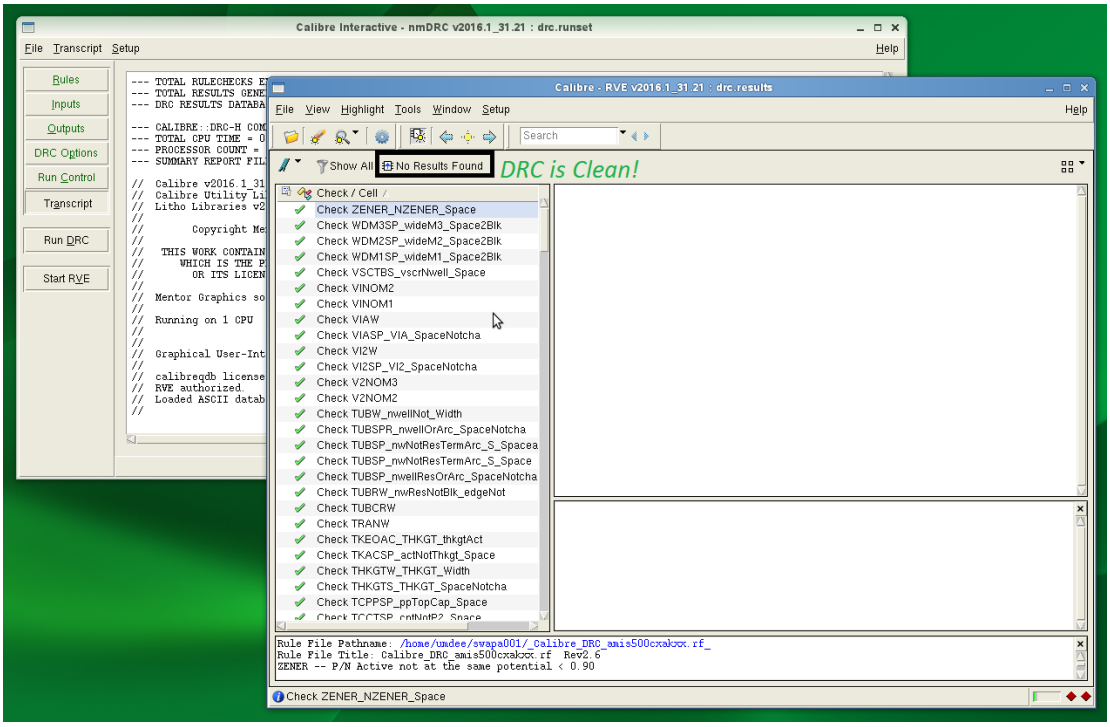


Figure 4.27: Clean DRC.

4.5.2 LVS-Layout Versus Schematic

Calibre® will compare the layout against schematic netlist. We have to create netlist from schematic and compare between netlist and gds file in Calibre® LVS. Also, we have to set the rule file. Similar to DRC, Calibre® summaries the error into a file. If any mismatch is found, it will return the LVS errors with the detail description, so that we can correct accordingly.

We have shown typical LVS process (Figure 4.28~Figure 4.32) in Calibre®.

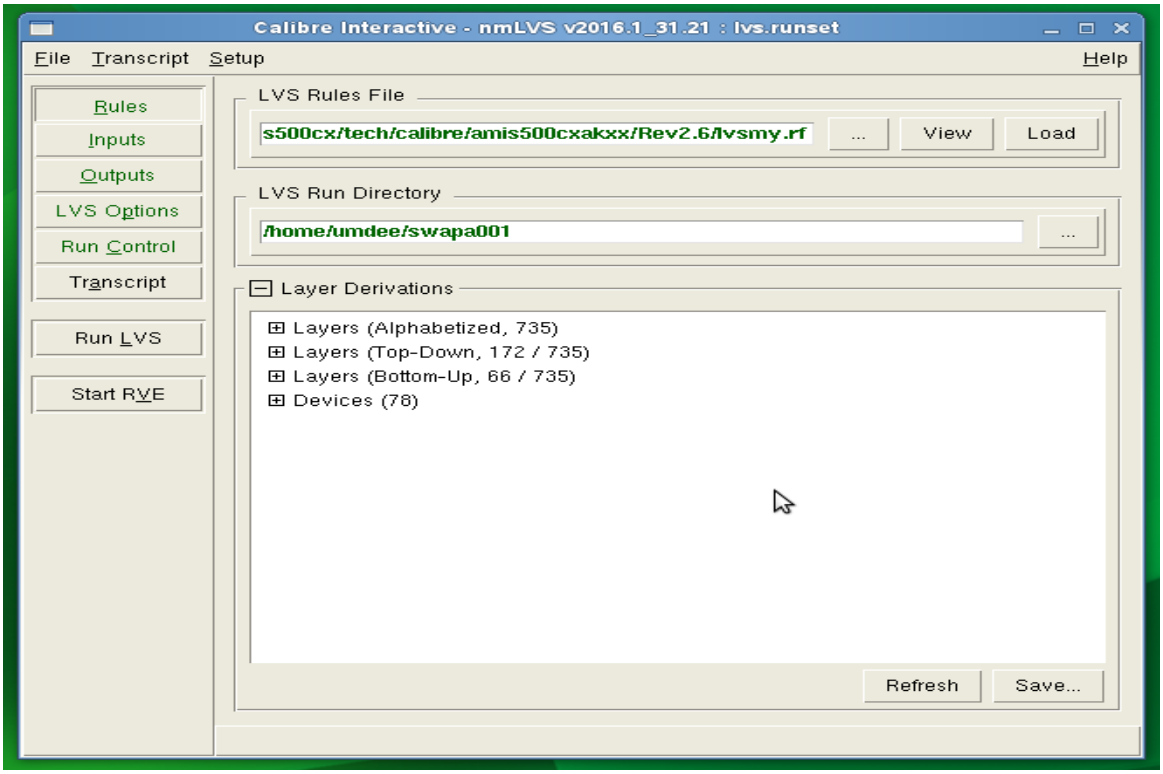


Figure 4.28: Load the LVS rule run file.

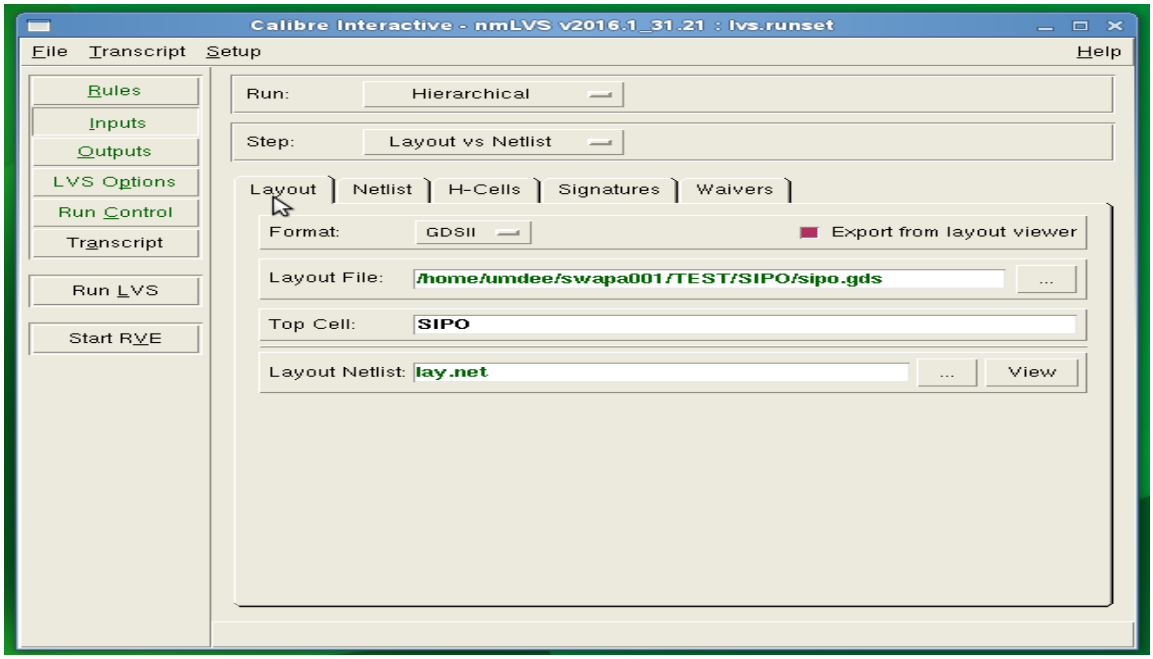


Figure 4.29: Input gds file.

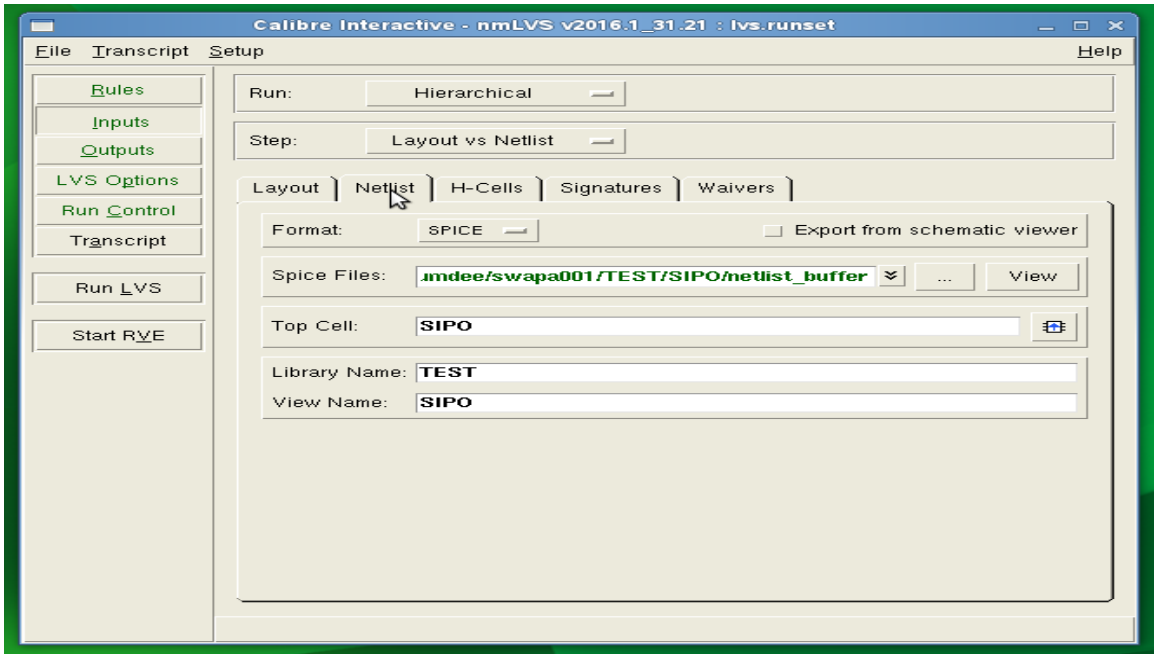


Figure 4.30: Input schematic netlist file.

While there are errors, caliber RVE will refer to the error type along with the description as shown in Figure 4.31.

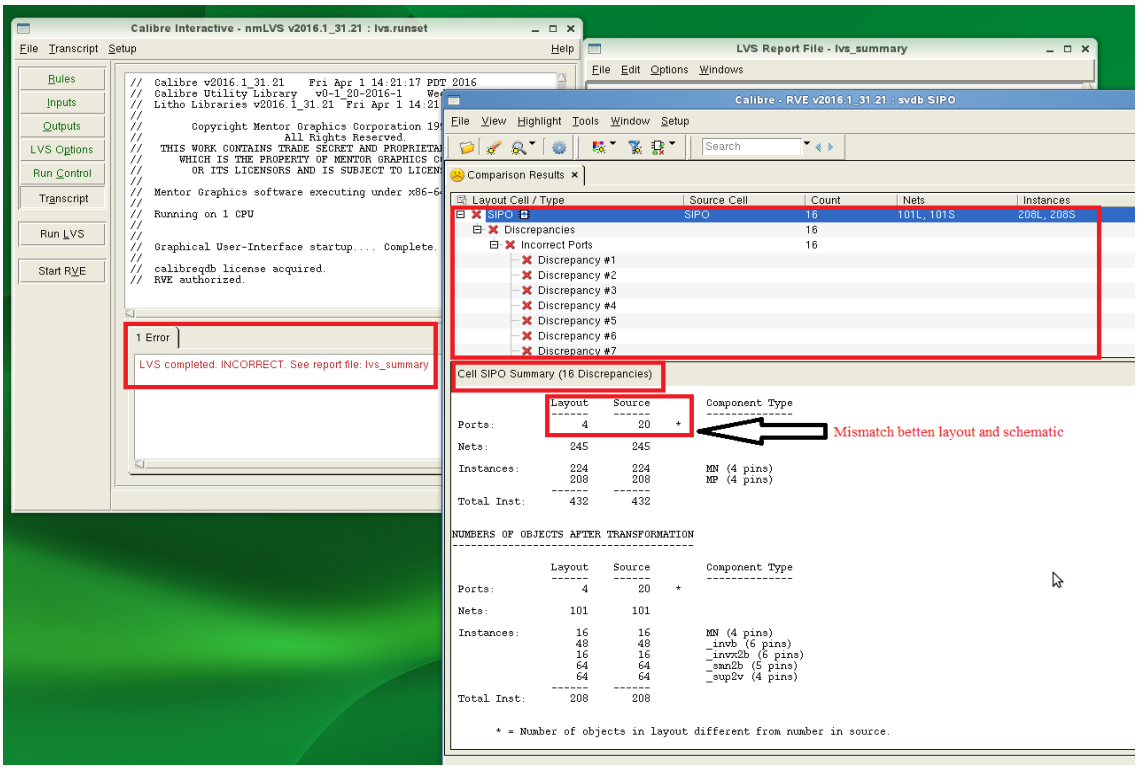


Figure 4.31: Typical LVS error.

By checking the LVS summary file, we can get the detail description of the discrepancy. For instance, Figure 4.31 demonstrates that there is mismatch between ports (I/O). Layout has only 4 ports, while from schematic netlist LVS is expecting 20 ports.

To fix this error, we can check two different options in design. First, there might be actually port missing in the layout. If so, inserting the missing ports will fix the issue. Second, there might be short circuit connections in the design. That's why, two or more ports will merge together and create LVS mismatch. In this case, removing the short circuit connection will take care of the issue.

Successful LVS returns the RVE window with green smiley face as shown in Figure 4.32.

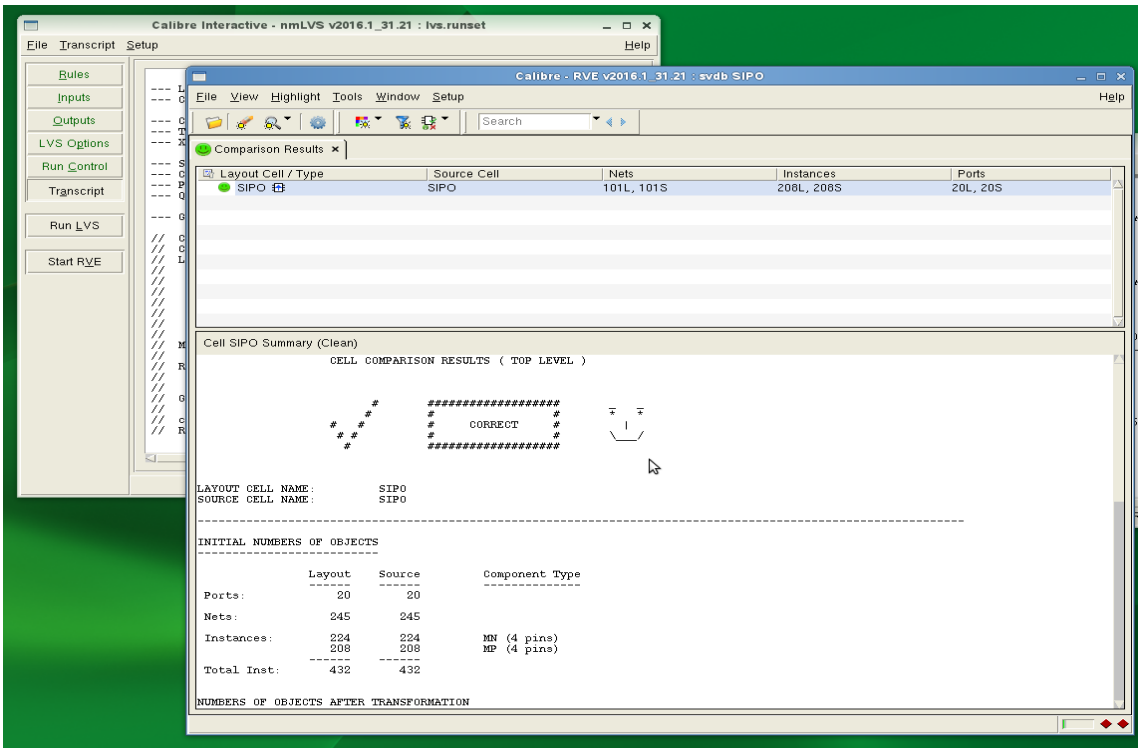


Figure 4.32: RVE window with green smiley face implicating successful pass of LVS.

4.5.3 PEX- Parasitic Extraction

Parasitic Extraction is necessary for post layout simulation to ensure that circuit is operating as expected. We have also extracted our circuit using Calibre® PEX. The process is similar to DRC. Setup the parasitic extraction rule file, load the gds file and run. It will generate netlist file with parasitic components.

4.6 Final File Creation with Bonding PADs

After all the verification check and successful simulation, we can proceed for the fabrication into microchip. As the external pin connection needs extra layer of support so that it will not break, we have to use glass layer aka PAD for the pins. External I/O pins will be connected to these PAD frames.

PAD frame includes METAL3, METAL2, VIA2 (to connect METAL2 and METAL3), NREC, FILLBACK and PAD layers.

Figure 4.33 shows the details of a PAD frame. PAD frame normally available in technology library. Otherwise, we have to manually create PAD frame.

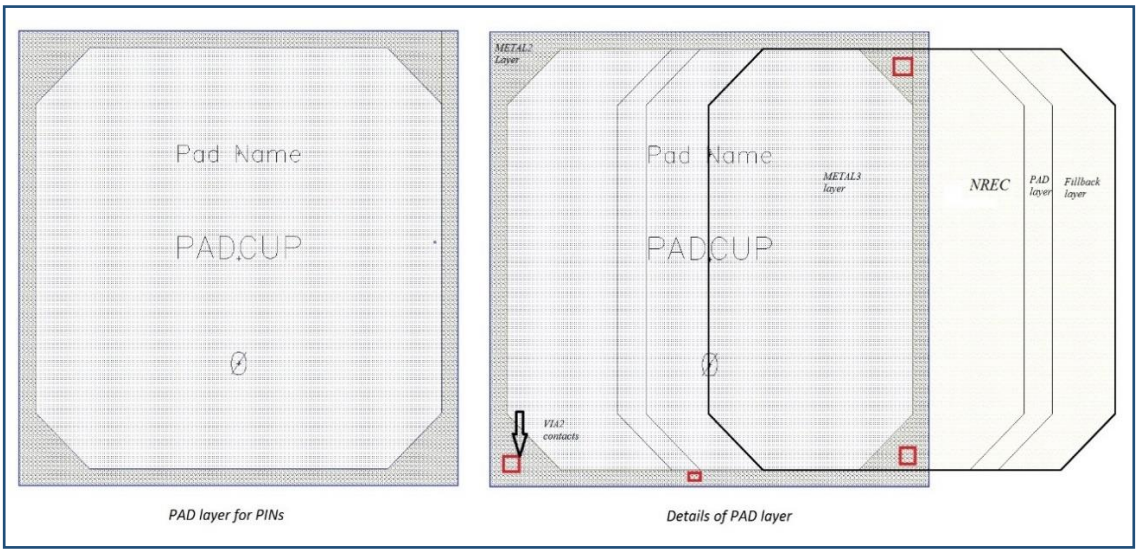


Figure 4.33: PAD frame to connect the I/O PIN.

If PAD layer is not defined in the LSW (Layer Select Window), we have to modify the layer map file as well. As mentioned before, layer map file is used while creating gds file from Cadence® Virtuoso layout. Layer map file serves as the translation between the layout description and the schematic circuit.

Figure 4.34 shows the details of a layer map file.

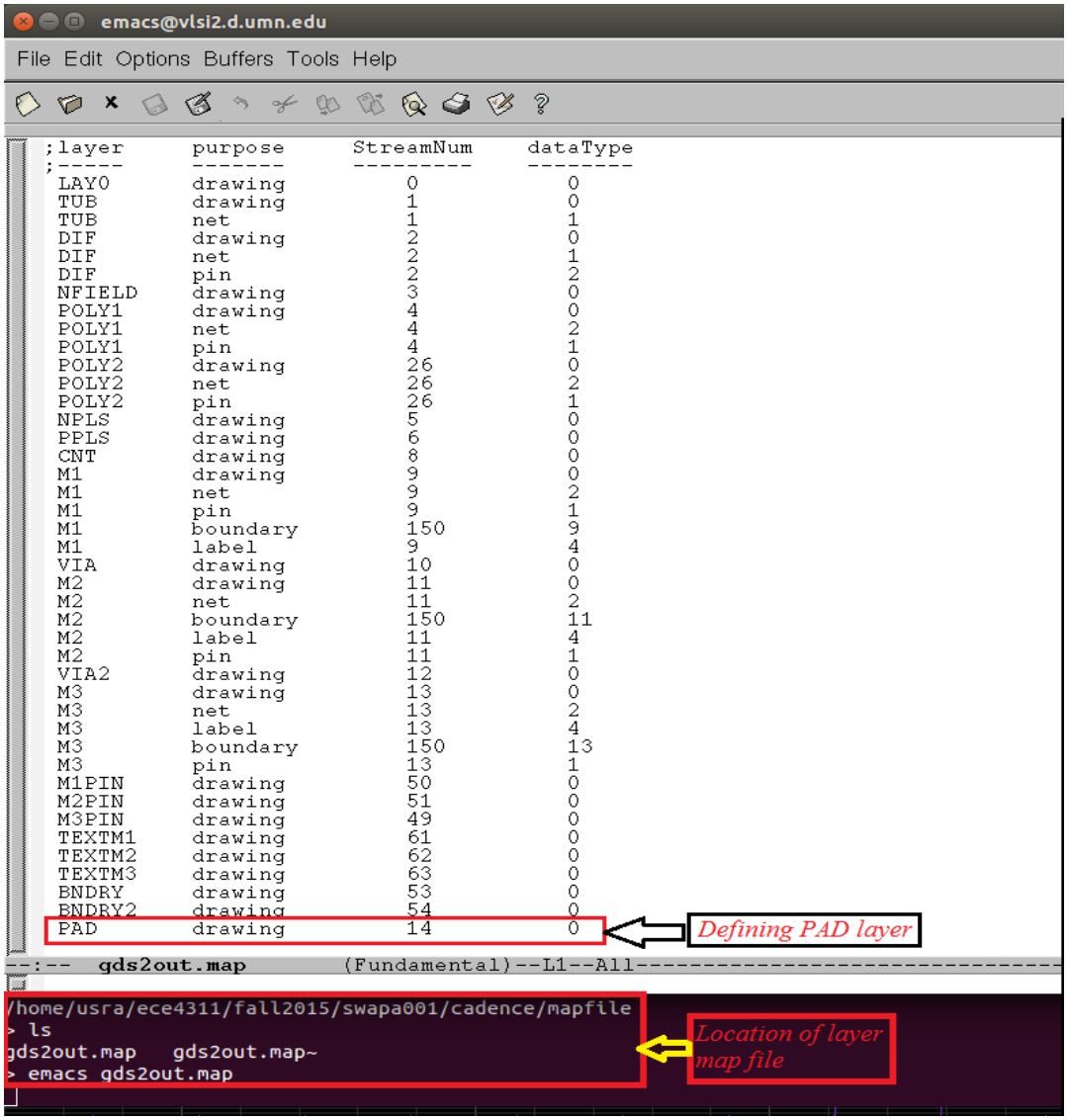


Figure 4.34: Layer map details.

Once the PAD frame is defined, we can use them to identify the I/O pins. In our case, there are twenty I/O pins and we have used twenty PAD frames. From layout then we have to connect the I/O pins to the PAD frames, using appropriate metal layers (usually top layer metal i.e. METAL3 in our case). After that, the design is ready to fabricate into micro-chip.

Figure 4.35 shows the final layout, which is ready for commercial fabrication.

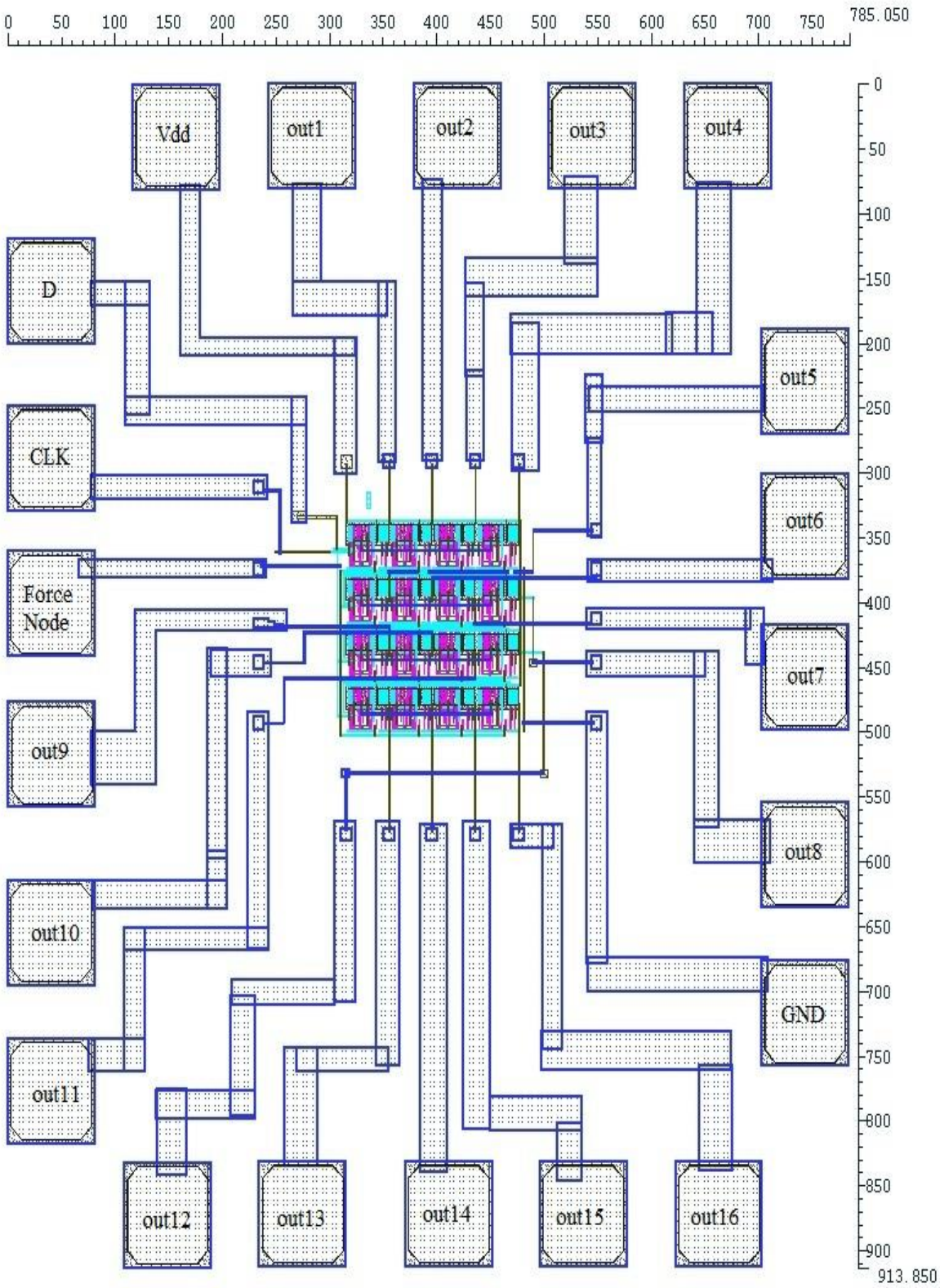


Figure 4.35: Layout including bonding PADs for fabrication.

To package the micro-chip, we have selected DIP (Dual Inline Plastic) packaging. The top view of the packing is shown in Figure 4.36.

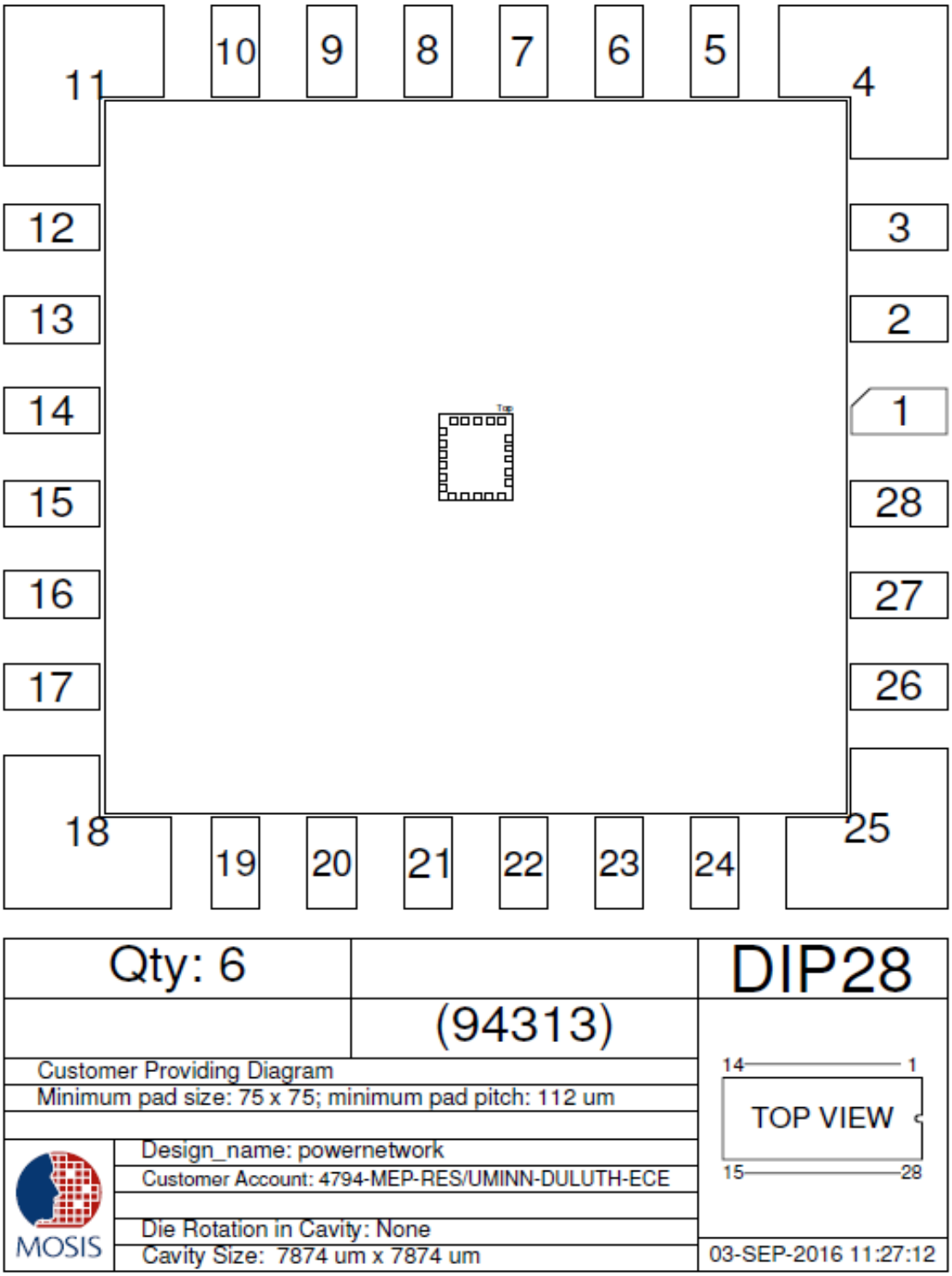


Figure 4.36: Preliminary bonding package layout (top view).

Chapter 5 Simulation of Microchip Design

The simulation results for the designed microchip is shown in Figure 5.1 to Figure 5.4. The sequence of 16 pulses from out1 to out16 are given in four different figures.

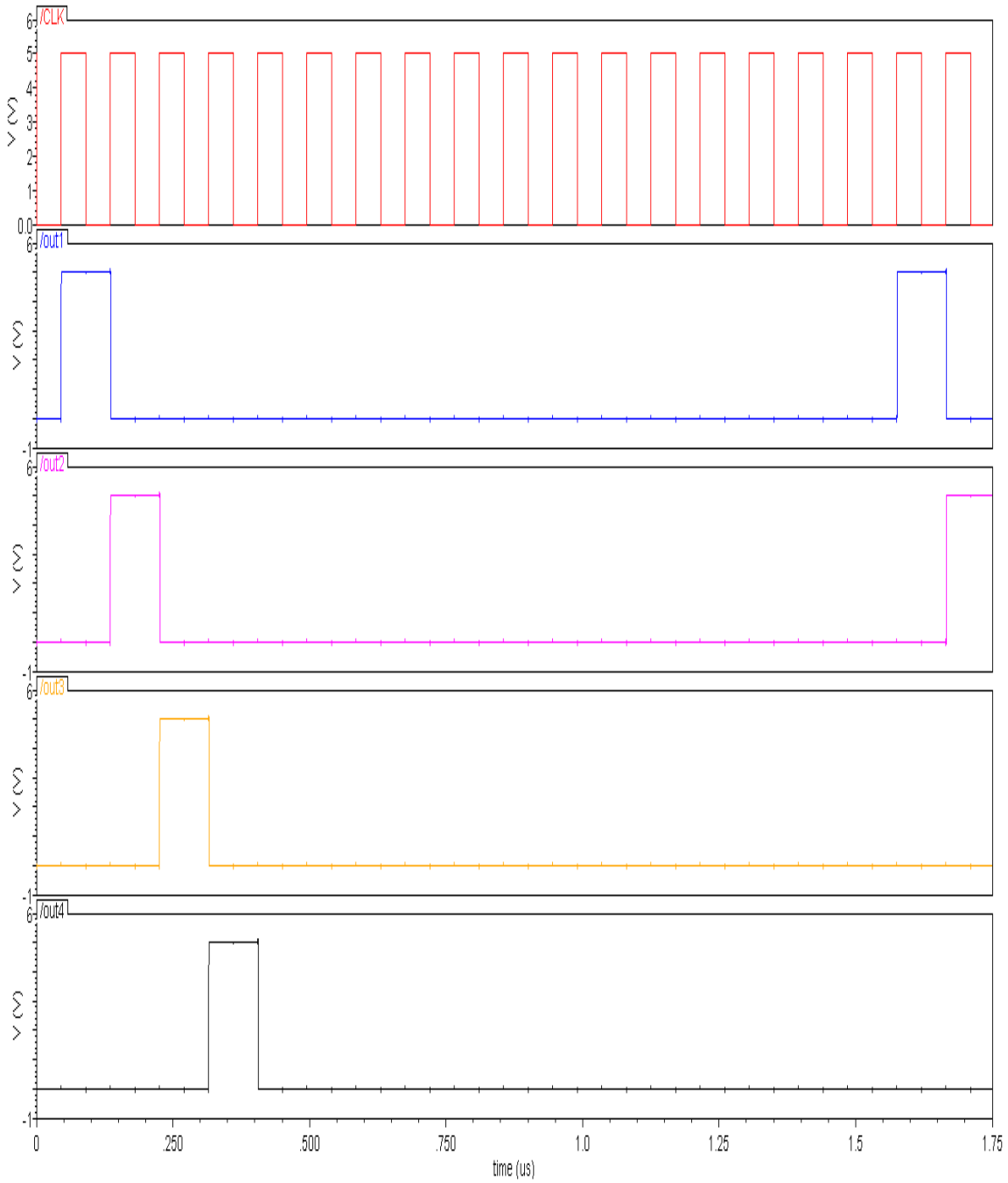


Figure 5.1: CLK, out1, out2, out3, out 4 wave shape.

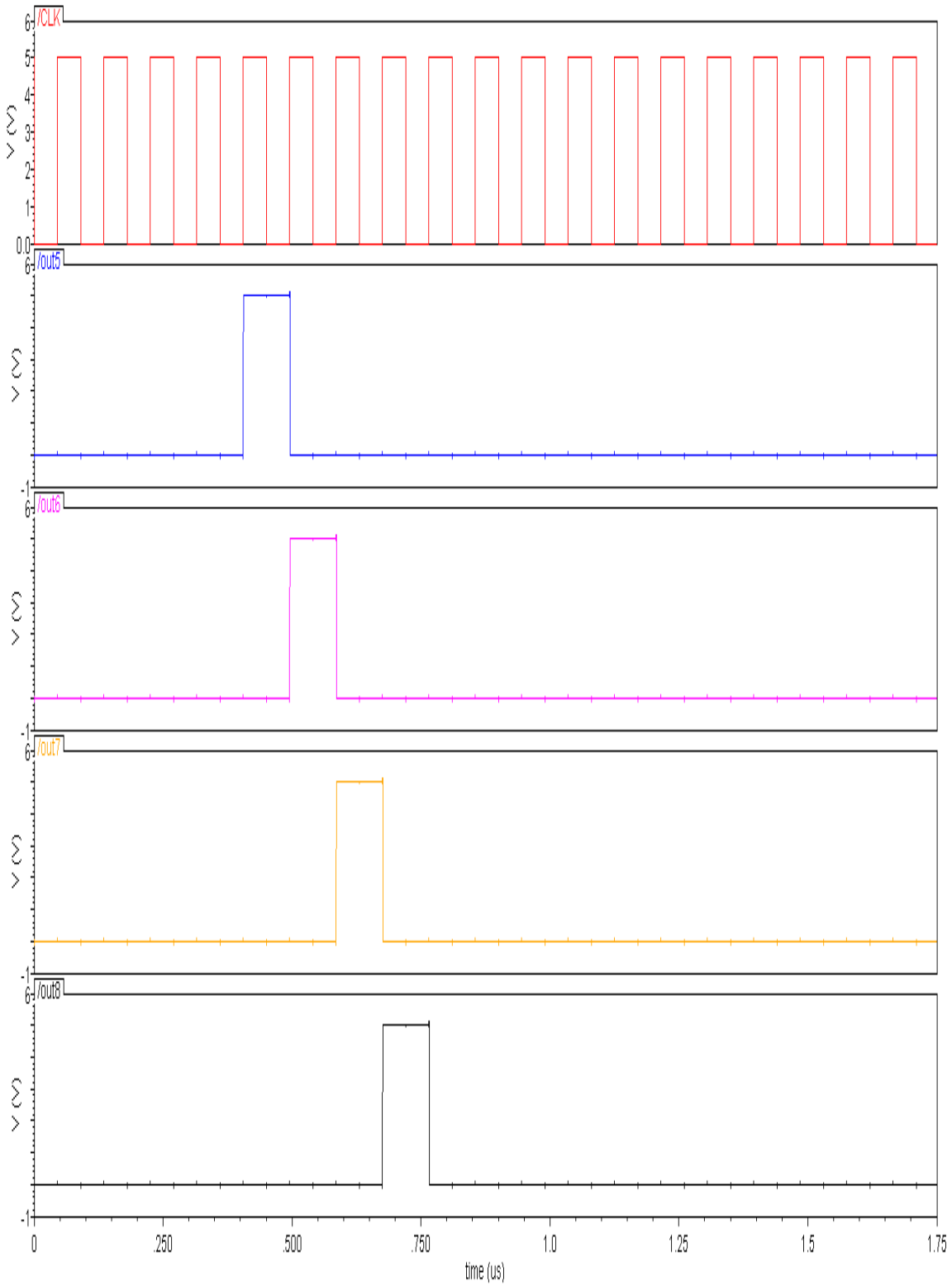


Figure 5.2: CLK, out5, out6, out7 and out 8 wave shape.

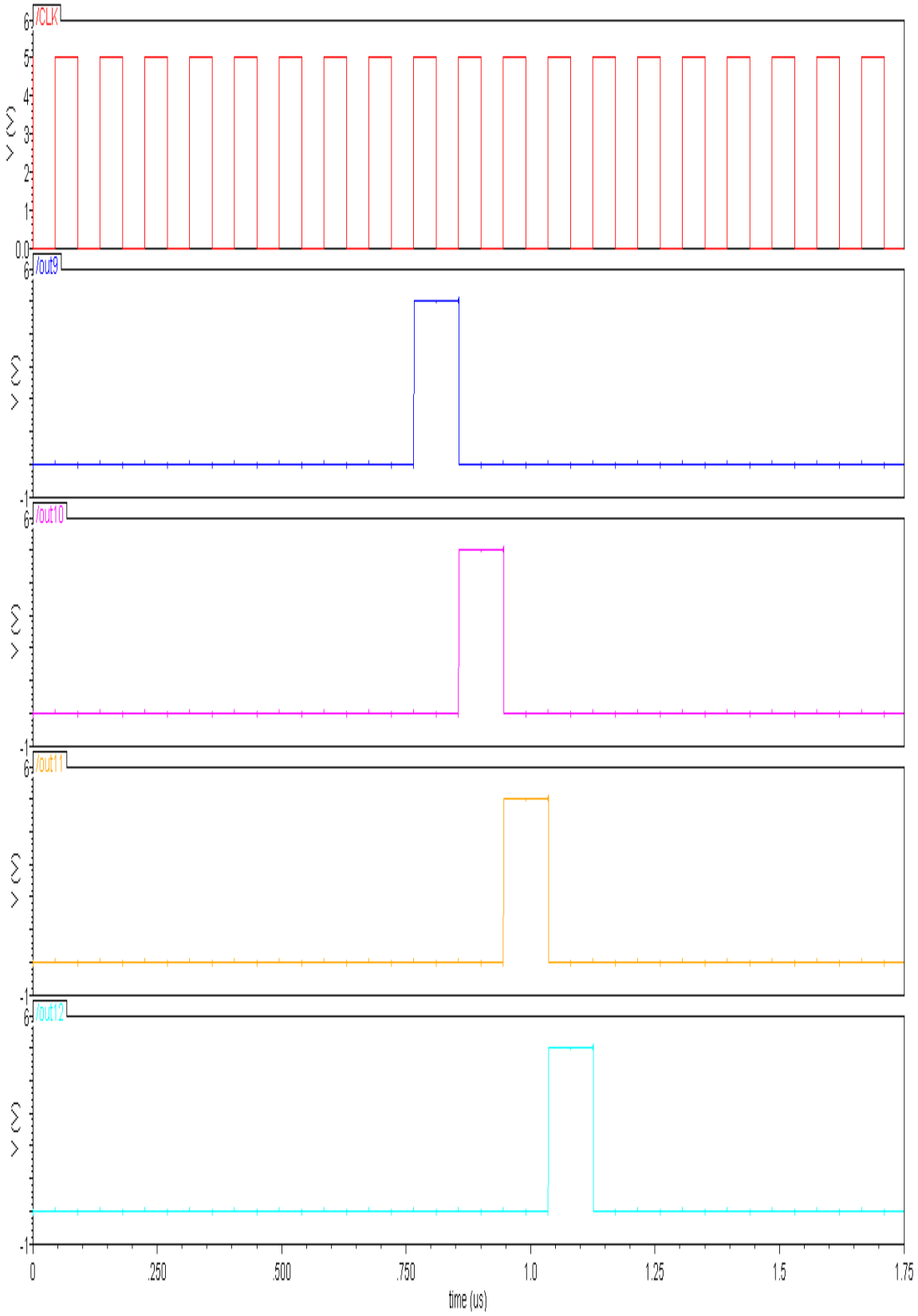


Figure 5.3: CLK, out 9, out 10, out11 and out12 wave shape.

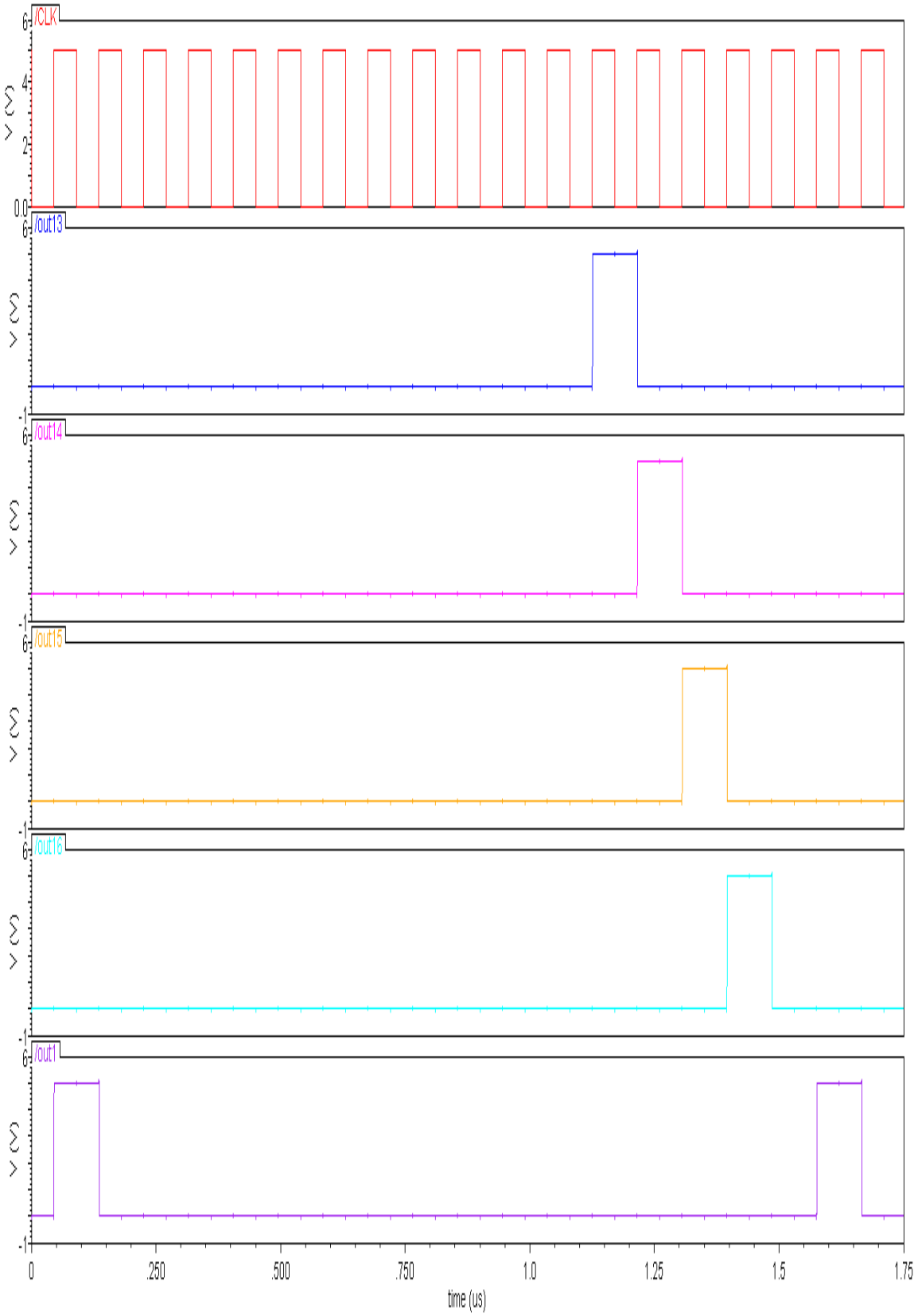


Figure 5.4: CLK, out13, out14, out15, out16 wave shape.

The simulation results of the designed microchip ensure proper functionality. It was done in MWAH 291A, VLSI lab. The results showed from the circuit, were consecutive pulses with width equal to the time of one clock cycle and amplitude of 5Vpp. The circuit shows similar results for 1Hz to 1 MHz frequencies. Though the application requires that the frequencies should be low, the circuit is also capable of working at higher frequencies.

Chapter 6 Conclusions and Future Work

In this chapter, we will give an overall summary of the part of the completed project and initiatives for the future work.

6.1 Conclusion

The main goal of the ongoing research was to extend the number of output from PCB to sixteen and fabricate the whole circuit into microchip. The main strategy to design the circuit for fabrication was to understand the thorough fabrication process and follow the ON Semi C5 technology files. The D flip-flop is the most useful component of the design. Researching of the D flip-flop with different implementation techniques enable us to choose the best one for this particular project.

The testing of the modified PCB as well as the simulation result from the Cadence® software ensures the successful operation of the circuit. We have also submitted the necessary design scheme and required documentation to MOSIS based on their fabrication requirements. The micro-chip fabrication has scheduled to 12th Sep 2016.

Once the fabricated microchip is available the next step will be testing the chip. For this purpose, we have requested few microchip in DIP (dual in-line plastic package). We can place them on breadboard and perform the functionality test.

Finally, the netlist of the schematic design is also provided in Appendices and hope this will be beneficial in future studies.

6.2 Future Recommendations

There is a major issue pending about the project. Currently the fabricated microchip from MOSIS will be available in two options-

1) Standard Dual Line Plastic Packaging
2) Microchip only (without any packaging)- size: 1mm×1mm(roughly), using AMI0.5 technology

With Standard Dual Line Plastic Packaging, we can insert the microchip into bread board or PCB to test and integrate with the sensor array and data acquisition system. Our desired system should be bendable. If we go with plastic packaging, durability as well as flexibility of the system will be compromised. Also physical wire connection will make the whole system bulky.

On other hand, if we go with microchip only; integration of the microchip with sensor array and DA system will be challenging. Because the connection pins will be in micrometer range (typically 0.6 um i.e. 3/5 of a hair) and manual connectivity of wires will be impossible. The goal will be microchip interconnection with sensor array without compromising flexibility and durability of the system.

Our sensor array system can be treated as Microelectromechanical system (MEMS). MEMS are typically transducer systems that sense or control physical, optical or chemical quantities; such as acceleration, radiation, pressure or fluids. To enable the MEMS transducer to perform useful functions, the electrical interface with the outside world is realized through integrated circuits (ICs) that provide the system with the necessary intelligence. In our system, designed IC will provide sequential pulse to read

data from sensor array through the data acquisition system. MEMS and ICs can be integrated using two basic methods:

1) system-on-chip (SoC) solution [26]: MEMS and IC components are manufactured on the same substrate, using consecutive or interlaced processing schemes.

2) multi-chip solution [27]: MEMS and IC components are manufactured on separate substrates using dedicated MEMS and IC processes and are subsequently hybridized in the final system.

In SoC, the first step would be integrating different kind of wafers (for sensor array and for IC) together. It would be really challenging as we have to use high budget thermal treatment or any other technique to combine the wafers. After carefully developing the combined fabrication process, we can ensure the interconnectivity and finally, get an integrated product.

Typically, it is not permitted for pre-processed wafers to be brought into standard CMOS fabrication facilities. Organizations who have their own CMOS fabrication can use SoC technique. If we have different sizes (say one in cm/mm and another one in um/nm range), it would be quite difficult to build up the system form pre-processed wafers.

In Multi-chip integration technique, MEMS and IC wafers are designed, manufactured and tested independently. The wafers are then separated into discrete chips and eventually integrated into multi-chip systems at the board or package level using wire and/or flip-chip bonding.

In wire bonding, a highly automated micro-welding process for metal wires is employed to create chip-to-chip and chip-to-package interconnects. In flip-chip bonding, solder balls or stud bumps are placed on pads on the topside of a chip. The chip is then flipped upside down and aligned with and attached to the package substrate or another chip via pick-and-place soldering. Both the wire and flip-chip bonding process employ temperature, force and ultrasonic energy in the joining process. As this technique decoupled the sensor array and IC; we will have more freedom in designing the sensor and IC separately.

References

[1] "Tests to detect colorectal cancer and polyps", National Cancer Institute, 2016. [Online]. Available: http://www.cancer.gov/types/colorectal/screening-fact-sheet. [Accessed: 6- May- 2016].

[2] T. Levin, "Complications of colonoscopy in an integrated health care delivery system", Annals of Internal Medicine, vol. 145, no. 12, p. 880, 2006.

[3] "Colonoscopy", Niddk.nih.gov, 2016. [Online]. Available: https://www.niddk.nih.gov/health-information/health-topics/diagnostic-tests/colonoscopy/Pages/diagnostic-test.aspx. [Accessed: 5- May-2016 and 21- Jun- 2016].

[4] G. Arora, A. Mannalithara, G. Singh, L. B. Gerson, and G. Triadafilopoulos, "Risk of perforation from a colonoscopy in adults: A large population-based study," Gastrointestinal Endosc., vol. 69, no. 3, pp. 654–664, 2009.

[5] Sayali A. Kulkarni, "Design of a constant voltage-source to array of sensors to optimize heart-beat detection", Master's Thesis, University of Minnesota Duluth, June 2013.

[6] Nawjif Md Anamul Hasan, "Optimization of off-on voltage levels of a -voltage-supply circuit for pressure sensor array", Master's Thesis, University of Minnesota Duluth, May 2015.

[7] C. Chuang and C. Lin, "Synthesizing genetic sequential logic circuit with clock pulse generator", BMC Systems Biology, vol. 8, no. 1, p. 63, 2014.

[8] F. Veirano, P. Perez, S. Besio, P. Castro and F. Silveira, "Ultra low power pulse generator based on a ring oscillator with direct path current avoidance", Proceedings of the Fourth IEEE Latin American Symposium on Circuits and Systems (LASCAS), 2013. [Online]. Available: http://iie.fing.edu.uy/investigacion/grupos/microele/papers/lascas2013_UlpVCO.pdf [Accessed: 13-Nov-15].

[9] A. Mitz, D. Reed and D. Humphrey, "A sequential pulse generator for producing true biphasic stimuli", Electroencephalography and Clinical Neurophysiology, vol. 57, no. 6, pp. 587-590, 1984.

[10] F. Jaw, S. Liu, T. Kuo and C. Wang, "Microcomputer-based pulse stimulator", Journal of Neuroscience Methods, vol. 62, no. 1-2, pp. 193-197, 1995.

[11] S. Wang and H. Wu, "Experimental demonstration of microring-based optical pulse train generator", Opt. Express, vol. 19, no. 17, p. 16259, 2011.

[12] J. Jeong, J. Lee and J. Burm, " A 0.18 μm CMOS multi-Gb/s 10-PAM transmitter ", Proceedings of the 2009 12th International Symposium on Integrated Circuits, pp. 85-88, 2009.

[13] A. Wortmann, S. Simon, M. Muller, "A high-speed transceiver architecture implementable as synthesizable IP core", Proceedings of the Design, Automation and Test in Europe Conference and Exhibition Designers' vol. 4 pp. 1530-1591, 2004.

[14] D. Jeong, G. Borriello, D. Hodges and R. Katz, "Design of PLL-based clock generation circuits", IEEE J. Solid-State Circuits, vol. 22, no. 2, pp. 255-261, 1987.

[15] Z. Gao, Y. Xu, P. Sun, E. Yao and Y. Hu, "A Programmable high-speed pulse swallow divide-by-n frequency divider for PLL frequency synthesizer", in International Conference on Computer Application and System Modeling (ICCASM 2010), 2010.

[16] W. Wang, X. Zhang, H. Wang, Z. Liu, X. Li, "The pulse sequence generator based on CPLD in the application of pulse nuclear magnetic resonance system", in The Ninth International Conference on Electronic Measurement & Instruments ICEMI, 2009.

[17] W. Wang, C. Liang, J. Wu, Z. Shang, "Design of a pulse sequence generator in P-NMR based on single-chip microcomputer and CPLD", in Second Asia-Pacific Conference on Computational Intelligence and Industrial Applications, 2009.

[18] Q. Huang and R. Rogenmoser, "Speed optimization of edge-triggered CMOS circuits for gigahertz single-phase clocks", IEEE J. Solid-State Circuits, vol. 31, no. 3, pp. 456-465, 1996.

[19] D. Jennifer Judy and V.S. Kanchana Bhaaskaran, "Ultra low power, high performance negative edge triggered ECRL energy recovery sequential elements with power clock gating", Research Journal of Applied Sciences, Engineering and Technology 7(16): 3312-3319 ISSN: 2040-7459; e-ISSN: 2040-7467, Apr 2014.

[20] M. Casu, M. Graziano and M. Zamboni, "A fully differential digital CMOS UWB pulse generator", Circuits, Systems & Signal Processing, vol. 28, no. 5, pp. 649-664, 2009.

[21] T. Zhang, S. Li, R. Ge, M. Yuan, G. Gui and Y. Ma, "A chaotic pulse sequence generator based on the tent map", IEICE Electron. Express, vol. 12, no. 16, pp. 20150530-20150530, 2015.

[22] V. von Kaenel, "A high-speed, low-power clock generator for a microprocessor application", IEEE J. Solid-State Circuits, vol. 33, no. 11, pp. 1634-1639, 1998.

[23] S. Paik, I. Han, S. Kim and Y. Shin, "Clock gating synthesis of pulsed-latch circuits", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 31, no. 7, pp. 1019-1030, 2012.

[24] A. Kumar,Fundamentals of digital circuits. New Delhi: Prentice-Hall of India, 2004.

[25] J. Rabaey, A. Chandrakasan and B. Nikolić, Digital integrated circuits, 2nd ed. Upper Saddle River, N.J.: Pearson Education, 2003.

[26] A. Fischer, F. Forsberg, M. Lapisa, S. Bleiker, G. Stemme, N. Roxhed and F. Niklaus, "Integrating MEMS and ICs", microsystems & nanoengineering, vol. 1, p. 15005, 2015.

[27] A. Fischer, J. Korvink, N. Roxhed, G. Stemme, U. Wallrabe and F. Niklaus, "Unconventional applications of wire bonding create opportunities for microsystem integration", J. Micromech. Microeng., vol. 23, no. 8, p. 083001, 2013.

Appendix

A.1 Netlist of the circuit

```
********************************************************************************
* auCdl Netlist:
*
* Library Name:  TEST
* Top Cell Name: SIPO
* View Name:     schematic
* Netlisted on:  May 23 18:51:48 2016
********************************************************************************

*.BIPOLAR
*.RESI = 2000
*.RESVAL
*.CAPVAL
*.DIOPERI
*.DIOAREA
*.EQUATION
*.SCALE METER
*.MEGA
.PARAM

*.GLOBAL gnd!
+        vdd!

*.PIN gnd!
*+    vdd!
```

```
********************************************************************************
* Library Name: TEST
* Cell Name:    SIPO
* View Name:    schematic
********************************************************************************

.SUBCKT SIPO CLK D ForceNode out1 out2 out3 out4 out5 out6 out7 out8 out9 out10
out11
+ out12 out13 out14 out15 out16
*.PININFO CLK:I D:I ForceNode:I out1:O out2:O out3:O out4:O out5:O out6:O out7:O
out8:O
*.PININFO out9:O out10:O out11:O out12:O out13:O out14:O out15:O out16:O
MMN191 net0654 Clk_b14 net0672 sub! nenm W=3u L=0.6u m=1.0
MMN190 out14 net0654 gnd! sub! nenm W=6u L=0.6u m=1.0
MMN189 net0651 net0663 gnd! sub! nenm W=3u L=0.6u m=1.0
MMN188 net0654 CLK net0651 sub! nenm W=3u L=0.6u m=1.0
MMN187 net0666 CLK net0660 sub! nenm W=3u L=0.6u m=1.0
MMN186 net0660 net0663 gnd! sub! nenm W=3u L=0.6u m=1.0
MMN185 net0663 net0666 gnd! sub! nenm W=3u L=0.6u m=1.0
MMN184 net0666 Clk_b14 net0669 sub! nenm W=3u L=0.6u m=1.0
MMN183 net0669 out13 gnd! sub! nenm W=3u L=0.6u m=1.0
MMN182 net0672 out14 gnd! sub! nenm W=3u L=0.6u m=1.0
MMN181 ForceNode out14 gnd! sub! nenm W=1.5u L=0.6u m=1.0
MMN180 ForceNode out13 gnd! sub! nenm W=1.5u L=0.6u m=1.0
MMN179 net0681 out13 gnd! sub! nenm W=3u L=0.6u m=1.0
MMN178 net0684 out12 gnd! sub! nenm W=3u L=0.6u m=1.0
MMN177 net0687 Clk_b13 net0684 sub! nenm W=3u L=0.6u m=1.0
MMN176 net0690 net0687 gnd! sub! nenm W=3u L=0.6u m=1.0
```

MMN175 net0693 net0690 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN174 net0687 CLK net0693 sub! nenm W=3u L=0.6u m=1.0

MMN173 net0699 CLK net0702 sub! nenm W=3u L=0.6u m=1.0

MMN172 net0702 net0690 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN171 out13 net0699 gnd! sub! nenm W=6u L=0.6u m=1.0

MMN170 net0699 Clk_b13 net0681 sub! nenm W=3u L=0.6u m=1.0

MMN169 ForceNode out15 gnd! sub! nenm W=1.5u L=0.6u m=1.0

MMN168 net0714 out15 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN167 net0717 out14 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN166 net0720 Clk_b15 net0717 sub! nenm W=3u L=0.6u m=1.0

MMN165 net0723 net0720 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN164 net0726 net0723 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN163 net0720 CLK net0726 sub! nenm W=3u L=0.6u m=1.0

MMN162 net0732 CLK net0735 sub! nenm W=3u L=0.6u m=1.0

MMN161 net0735 net0723 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN160 out15 net0732 gnd! sub! nenm W=6u L=0.6u m=1.0

MMN159 net0732 Clk_b15 net0714 sub! nenm W=3u L=0.6u m=1.0

MMN158 net0753 Clk_b16 net0771 sub! nenm W=3u L=0.6u m=1.0

MMN157 out16 net0753 gnd! sub! nenm W=6u L=0.6u m=1.0

MMN156 net0750 net0762 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN155 net0753 CLK net0750 sub! nenm W=3u L=0.6u m=1.0

MMN154 net0765 CLK net0759 sub! nenm W=3u L=0.6u m=1.0

MMN153 net0759 net0762 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN152 net0762 net0765 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN151 net0765 Clk_b16 net0768 sub! nenm W=3u L=0.6u m=1.0

MMN150 net0768 out15 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN149 net0771 out16 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN148 ForceNode out16 gnd! sub! nenm W=1.5u L=0.6u m=1.0

MMN147 ForceNode out12 gnd! sub! nenm W=1.5u L=0.6u m=1.0

MMN146 net0780 out12 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN145 net0783 out11 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN144 net0786 Clk_b12 net0783 sub! nenm W=3u L=0.6u m=1.0

MMN143 net0789 net0786 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN142 net0792 net0789 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN141 net0786 CLK net0792 sub! nenm W=3u L=0.6u m=1.0

MMN140 net0798 CLK net0801 sub! nenm W=3u L=0.6u m=1.0

MMN139 net0801 net0789 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN138 out12 net0798 gnd! sub! nenm W=6u L=0.6u m=1.0

MMN137 net0798 Clk_b12 net0780 sub! nenm W=3u L=0.6u m=1.0

MMN136 net0819 Clk_b11 net0837 sub! nenm W=3u L=0.6u m=1.0

MMN135 out11 net0819 gnd! sub! nenm W=6u L=0.6u m=1.0

MMN134 net0816 net0828 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN133 net0819 CLK net0816 sub! nenm W=3u L=0.6u m=1.0

MMN132 net0831 CLK net0825 sub! nenm W=3u L=0.6u m=1.0

MMN131 net0825 net0828 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN130 net0828 net0831 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN129 net0831 Clk_b11 net0834 sub! nenm W=3u L=0.6u m=1.0

MMN128 net0834 out10 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN127 net0837 out11 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN126 ForceNode out11 gnd! sub! nenm W=1.5u L=0.6u m=1.0

MMN125 net0852 Clk_b9 net0870 sub! nenm W=3u L=0.6u m=1.0

MMN124 out9 net0852 gnd! sub! nenm W=6u L=0.6u m=1.0

MMN123 net0849 net0861 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN122 net0852 CLK net0849 sub! nenm W=3u L=0.6u m=1.0

MMN121 net0864 CLK net0858 sub! nenm W=3u L=0.6u m=1.0

MMN120 net0858 net0861 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN119 net0861 net0864 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN118 net0864 Clk_b9 net0867 sub! nenm W=3u L=0.6u m=1.0

MMN117 net0867 out8 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN116 net0870 out9 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN115 ForceNode out9 gnd! sub! nenm W=1.5u L=0.6u m=1.0

MMN114 ForceNode out10 gnd! sub! nenm W=1.5u L=0.6u m=1.0

MMN113 net0879 out10 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN112 net0882 out9 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN111 net0885 Clk_b10 net0882 sub! nenm W=3u L=0.6u m=1.0

MMN110 net0888 net0885 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN109 net0891 net0888 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN108 net0885 CLK net0891 sub! nenm W=3u L=0.6u m=1.0

MMN107 net0897 CLK net0900 sub! nenm W=3u L=0.6u m=1.0

MMN106 net0900 net0888 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN105 out10 net0897 gnd! sub! nenm W=6u L=0.6u m=1.0

MMN104 net0897 Clk_b10 net0879 sub! nenm W=3u L=0.6u m=1.0

MMN76 net0990 net0987 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN83 out5 net0963 gnd! sub! nenm W=6u L=0.6u m=1.0

MMN85 net0963 CLK net0966 sub! nenm W=3u L=0.6u m=1.0

MMN102 out6 net0918 gnd! sub! nenm W=6u L=0.6u m=1.0

MMN73 net0999 net0987 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN69 out8 net01017 gnd! sub! nenm W=6u L=0.6u m=1.0

MMN81 ForceNode out7 gnd! sub! nenm W=1.5u L=0.6u m=1.0

MMN98 net0924 net0927 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN99 net0930 CLK net0924 sub! nenm W=3u L=0.6u m=1.0

MMN93 ForceNode out6 gnd! sub! nenm W=1.5u L=0.6u m=1.0

MMN96 net0930 Clk_b6 net0933 sub! nenm W=3u L=0.6u m=1.0

MMN97 net0927 net0930 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN92 ForceNode out5 gnd! sub! nenm W=1.5u L=0.6u m=1.0

MMN103 net0918 Clk_b6 net0936 sub! nenm W=3u L=0.6u m=1.0

MMN67 net01017 CLK net01014 sub! nenm W=3u L=0.6u m=1.0

MMN68 net01014 net01026 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN63 net01029 Clk_b8 net01032 sub! nenm W=3u L=0.6u m=1.0

MMN82 net0963 Clk_b5 net0945 sub! nenm W=3u L=0.6u m=1.0

MMN87 net0957 net0954 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN79 net0981 out6 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN80 net0978 out7 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN86 net0951 CLK net0957 sub! nenm W=3u L=0.6u m=1.0

MMN70 net01017 Clk_b8 net01035 sub! nenm W=3u L=0.6u m=1.0

MMN64 net01026 net01029 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN74 net0996 CLK net0999 sub! nenm W=3u L=0.6u m=1.0

MMN75 net0984 CLK net0990 sub! nenm W=3u L=0.6u m=1.0

MMN77 net0987 net0984 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN60 ForceNode out8 gnd! sub! nenm W=1.5u L=0.6u m=1.0

MMN90 net0948 out4 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN91 net0945 out5 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN95 net0933 out5 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN101 net0915 net0927 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN100 net0918 CLK net0915 sub! nenm W=3u L=0.6u m=1.0

MMN94 net0936 out6 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN59 ForceNode out4 gnd! sub! nenm W=1.5u L=0.6u m=1.0

MMN58 net0129 out4 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN57 net0132 out3 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN56 net0135 Clk_b4 net0132 sub! nenm W=3u L=0.6u m=1.0

MMN55 net0138 net0135 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN54 net0141 net0138 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN53 net0135 CLK net0141 sub! nenm W=3u L=0.6u m=1.0

MMN52 net0147 CLK net0150 sub! nenm W=3u L=0.6u m=1.0

MMN51 net0150 net0138 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN50 out4 net0147 gnd! sub! nenm W=6u L=0.6u m=1.0

MMN49 net0147 Clk_b4 net0129 sub! nenm W=3u L=0.6u m=1.0

MMN48 net0168 Clk_b3 net0186 sub! nenm W=3u L=0.6u m=1.0

MMN47 out3 net0168 gnd! sub! nenm W=6u L=0.6u m=1.0

MMN46 net0165 net0177 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN45 net0168 CLK net0165 sub! nenm W=3u L=0.6u m=1.0

MMN44 net0180 CLK net0174 sub! nenm W=3u L=0.6u m=1.0

MMN43 net0174 net0177 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN42 net0177 net0180 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN41 net0180 Clk_b3 net0183 sub! nenm W=3u L=0.6u m=1.0

MMN40 net0183 out2 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN39 net0186 out3 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN24 Clk_b3 CLK gnd! sub! nenm W=6u L=0.6u m=1.0

MMN62 net01032 out7 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN2 Clk_b2 CLK gnd! sub! nenm W=6u L=0.6u m=1.0

MMN25 Clk_b4 CLK gnd! sub! nenm W=6u L=0.6u m=1.0

MMN26 Clk_b7 CLK gnd! sub! nenm W=6u L=0.6u m=1.0

MMN27 Clk_b6 CLK gnd! sub! nenm W=6u L=0.6u m=1.0

MMN28 Clk_b5 CLK gnd! sub! nenm W=6u L=0.6u m=1.0

MMN61 net01035 out8 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN72 out7 net0996 gnd! sub! nenm W=6u L=0.6u m=1.0

MMN71 net0996 Clk_b7 net0978 sub! nenm W=3u L=0.6u m=1.0

MMN65 net01023 net01026 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN66 net01029 CLK net01023 sub! nenm W=3u L=0.6u m=1.0

MMN78 net0984 Clk_b7 net0981 sub! nenm W=3u L=0.6u m=1.0

MMN84 net0966 net0954 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN88 net0954 net0951 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN89 net0951 Clk_b5 net0948 sub! nenm W=3u L=0.6u m=1.0

MMN29 Clk_b8 CLK gnd! sub! nenm W=6u L=0.6u m=1.0

MMN30 Clk_b9 CLK gnd! sub! nenm W=6u L=0.6u m=1.0

MMN31 Clk_b10 CLK gnd! sub! nenm W=6u L=0.6u m=1.0

MMN32 Clk_b14 CLK gnd! sub! nenm W=6u L=0.6u m=1.0

MMN33 Clk_b15 CLK gnd! sub! nenm W=6u L=0.6u m=1.0

MMN34 Clk_b16 CLK gnd! sub! nenm W=6u L=0.6u m=1.0

MMN35 Clk_b13 CLK gnd! sub! nenm W=6u L=0.6u m=1.0

MMN36 Clk_b12 CLK gnd! sub! nenm W=6u L=0.6u m=1.0

MMN37 Clk_b11 CLK gnd! sub! nenm W=6u L=0.6u m=1.0

MMN38 ForceNode out3 gnd! sub! nenm W=1.5u L=0.6u m=1.0

MMN10 net15 Clk_b1 net33 sub! nenm W=3u L=0.6u m=1.0

MMN11 out1 net15 gnd! sub! nenm W=6u L=0.6u m=1.0

MMN7 net12 net24 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN8 net15 CLK net12 sub! nenm W=3u L=0.6u m=1.0

MMN5 net27 CLK net21 sub! nenm W=3u L=0.6u m=1.0

MMN3 net21 net24 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN4 net24 net27 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN6 net27 Clk_b1 net30 sub! nenm W=3u L=0.6u m=1.0

MMN9 net30 D gnd! sub! nenm W=3u L=0.6u m=1.0

MMN12 net33 out1 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN1 ForceNode out1 gnd! sub! nenm W=1.5u L=0.6u m=1.0

MMN13 ForceNode out2 gnd! sub! nenm W=1.5u L=0.6u m=1.0

MMN14 net42 out2 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN15 net45 out1 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN16 net48 Clk_b2 net45 sub! nenm W=3u L=0.6u m=1.0

MMN17 net51 net48 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN18 net54 net51 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN19 net48 CLK net54 sub! nenm W=3u L=0.6u m=1.0

MMN20 net60 CLK net63 sub! nenm W=3u L=0.6u m=1.0

MMN21 net63 net51 gnd! sub! nenm W=3u L=0.6u m=1.0

MMN22 out2 net60 gnd! sub! nenm W=6u L=0.6u m=1.0

MMN23 net60 Clk_b2 net42 sub! nenm W=3u L=0.6u m=1.0

MMN0 Clk_b1 CLK gnd! sub! nenm W=6u L=0.6u m=1.0

MMP175 out14 net0654 vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP174 net01243 out14 vdd! vdd! pepm W=3u L=0.6u m=1.0

MMP173 net01249 net0663 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP172 net01240 net0663 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP171 net0666 CLK net01234 vdd! pepm W=6u L=0.6u m=1.0

MMP170 net01234 out13 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP169 net0666 Clk_b14 net01240 vdd! pepm W=6u L=0.6u m=1.0

MMP168 net0654 CLK net01243 vdd! pepm W=3u L=0.6u m=1.0

MMP167 net0663 net0666 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP166 net0654 Clk_b14 net01249 vdd! pepm W=6u L=0.6u m=1.0

MMP165 net0699 Clk_b13 net01252 vdd! pepm W=6u L=0.6u m=1.0

MMP164 net0690 net0687 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP163 net0699 CLK net01258 vdd! pepm W=3u L=0.6u m=1.0

MMP162 net0687 Clk_b13 net01261 vdd! pepm W=6u L=0.6u m=1.0

MMP161 net01267 out12 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP160 net0687 CLK net01267 vdd! pepm W=6u L=0.6u m=1.0

MMP159 net01261 net0690 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP158 net01252 net0690 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP157 net01258 out13 vdd! vdd! pepm W=3u L=0.6u m=1.0

MMP156 out13 net0699 vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP155 net0732 Clk_b15 net01282 vdd! pepm W=6u L=0.6u m=1.0

MMP154 net0723 net0720 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP153 net0732 CLK net01288 vdd! pepm W=3u L=0.6u m=1.0

MMP152 net0720 Clk_b15 net01291 vdd! pepm W=6u L=0.6u m=1.0

MMP151 net01297 out14 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP150 net0720 CLK net01297 vdd! pepm W=6u L=0.6u m=1.0

MMP149 net01291 net0723 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP148 net01282 net0723 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP147 net01288 out15 vdd! vdd! pepm W=3u L=0.6u m=1.0

MMP146 out15 net0732 vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP145 out16 net0753 vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP144 net01333 out16 vdd! vdd! pepm W=3u L=0.6u m=1.0

MMP143 net01339 net0762 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP142 net01330 net0762 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP141 net0765 CLK net01324 vdd! pepm W=6u L=0.6u m=1.0

MMP140 net01324 out15 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP139 net0765 Clk_b16 net01330 vdd! pepm W=6u L=0.6u m=1.0

MMP138 net0753 CLK net01333 vdd! pepm W=3u L=0.6u m=1.0

MMP137 net0762 net0765 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP136 net0753 Clk_b16 net01339 vdd! pepm W=6u L=0.6u m=1.0

MMP135 net0798 Clk_b12 net01342 vdd! pepm W=6u L=0.6u m=1.0

MMP134 net0789 net0786 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP133 net0798 CLK net01348 vdd! pepm W=3u L=0.6u m=1.0

MMP132 net0786 Clk_b12 net01351 vdd! pepm W=6u L=0.6u m=1.0

MMP131 net01357 out11 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP130 net0786 CLK net01357 vdd! pepm W=6u L=0.6u m=1.0

MMP129 net01351 net0789 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP128 net01342 net0789 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP127 net01348 out12 vdd! vdd! pepm W=3u L=0.6u m=1.0

MMP126 out12 net0798 vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP125 out11 net0819 vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP124 net01393 out11 vdd! vdd! pepm W=3u L=0.6u m=1.0

MMP123 net01399 net0828 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP122 net01390 net0828 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP121 net0831 CLK net01384 vdd! pepm W=6u L=0.6u m=1.0

MMP120 net01384 out10 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP119 net0831 Clk_b11 net01390 vdd! pepm W=6u L=0.6u m=1.0

MMP118 net0819 CLK net01393 vdd! pepm W=3u L=0.6u m=1.0

MMP117 net0828 net0831 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP116 net0819 Clk_b11 net01399 vdd! pepm W=6u L=0.6u m=1.0

MMP115 out9 net0852 vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP114 net01423 out9 vdd! vdd! pepm W=3u L=0.6u m=1.0

MMP113 net01429 net0861 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP112 net01420 net0861 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP111 net0864 CLK net01414 vdd! pepm W=6u L=0.6u m=1.0

MMP110 net01414 out8 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP109 net0864 Clk_b9 net01420 vdd! pepm W=6u L=0.6u m=1.0

MMP108 net0852 CLK net01423 vdd! pepm W=3u L=0.6u m=1.0

MMP107 net0861 net0864 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP106 net0852 Clk_b9 net01429 vdd! pepm W=6u L=0.6u m=1.0

MMP105 net0897 Clk_b10 net01432 vdd! pepm W=6u L=0.6u m=1.0

MMP104 net0888 net0885 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP103 net0897 CLK net01438 vdd! pepm W=3u L=0.6u m=1.0

MMP102 net0885 Clk_b10 net01441 vdd! pepm W=6u L=0.6u m=1.0

MMP101 net01447 out9 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP100 net0885 CLK net01447 vdd! pepm W=6u L=0.6u m=1.0

MMP99 net01441 net0888 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP98 net01432 net0888 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP97 net01438 out10 vdd! vdd! pepm W=3u L=0.6u m=1.0

MMP96 out10 net0897 vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP72 net0984 Clk_b7 net01531 vdd! pepm W=6u L=0.6u m=1.0

MMP70 net0984 CLK net01537 vdd! pepm W=6u L=0.6u m=1.0

MMP93 net01489 net0927 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP68 net01522 net0987 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP57 net01026 net01029 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP66 out7 net0996 vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP67 net01528 out7 vdd! vdd! pepm W=3u L=0.6u m=1.0

MMP73 net0996 CLK net01528 vdd! pepm W=3u L=0.6u m=1.0

MMP91 net0930 CLK net01474 vdd! pepm W=6u L=0.6u m=1.0

MMP92 net01480 net0927 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP87 net0927 net0930 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP94 net01483 out6 vdd! vdd! pepm W=3u L=0.6u m=1.0

MMP88 net0918 CLK net01483 vdd! pepm W=3u L=0.6u m=1.0

MMP69 net01531 net0987 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP74 net0987 net0984 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP77 net01498 out5 vdd! vdd! pepm W=3u L=0.6u m=1.0

MMP78 net01492 net0954 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP80 net0951 CLK net01507 vdd! pepm W=6u L=0.6u m=1.0

MMP61 net01029 CLK net01564 vdd! pepm W=6u L=0.6u m=1.0

MMP62 net01570 net01026 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP64 net01573 out8 vdd! vdd! pepm W=3u L=0.6u m=1.0

MMP59 net01029 Clk_b8 net01570 vdd! pepm W=6u L=0.6u m=1.0

MMP82 net0951 Clk_b5 net01501 vdd! pepm W=6u L=0.6u m=1.0

MMP83 net0963 CLK net01498 vdd! pepm W=3u L=0.6u m=1.0

MMP85 net0963 Clk_b5 net01492 vdd! pepm W=6u L=0.6u m=1.0

MMP58 net01017 CLK net01573 vdd! pepm W=3u L=0.6u m=1.0

MMP76 out5 net0963 vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP71 net01537 out6 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP75 net0996 Clk_b7 net01522 vdd! pepm W=6u L=0.6u m=1.0

MMP95 out6 net0918 vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP89 net0930 Clk_b6 net01480 vdd! pepm W=6u L=0.6u m=1.0

MMP90 net01474 out5 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP79 net01501 net0954 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP81 net01507 out4 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP63 net01579 net01026 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP65 out8 net01017 vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP56 net01017 Clk_b8 net01579 vdd! pepm W=6u L=0.6u m=1.0

MMP60 net01564 out7 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP84 net0954 net0951 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP86 net0918 Clk_b6 net01489 vdd! pepm W=6u L=0.6u m=1.0

MMP55 net0147 Clk_b4 net0307 vdd! pepm W=6u L=0.6u m=1.0

MMP54 net0138 net0135 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP53 net0147 CLK net0313 vdd! pepm W=3u L=0.6u m=1.0

MMP52 net0135 Clk_b4 net0316 vdd! pepm W=6u L=0.6u m=1.0

MMP51 net0322 out3 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP50 net0135 CLK net0322 vdd! pepm W=6u L=0.6u m=1.0

MMP49 net0316 net0138 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP48 net0307 net0138 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP47 net0313 out4 vdd! vdd! pepm W=3u L=0.6u m=1.0

MMP46 out4 net0147 vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP45 out3 net0168 vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP44 net0358 out3 vdd! vdd! pepm W=3u L=0.6u m=1.0

MMP43 net0364 net0177 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP42 net0355 net0177 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP41 net0180 CLK net0349 vdd! pepm W=6u L=0.6u m=1.0

MMP40 net0349 out2 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP39 net0180 Clk_b3 net0355 vdd! pepm W=6u L=0.6u m=1.0

MMP38 net0168 CLK net0358 vdd! pepm W=3u L=0.6u m=1.0

MMP37 net0177 net0180 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP36 net0168 Clk_b3 net0364 vdd! pepm W=6u L=0.6u m=1.0

MMP22 Clk_b3 CLK vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP21 Clk_b2 CLK vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP23 Clk_b4 CLK vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP24 Clk_b7 CLK vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP25 Clk_b6 CLK vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP26 Clk_b5 CLK vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP27 Clk_b8 CLK vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP28 Clk_b9 CLK vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP29 Clk_b10 CLK vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP30 Clk_b14 CLK vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP31 Clk_b15 CLK vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP32 Clk_b16 CLK vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP33 Clk_b13 CLK vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP34 Clk_b12 CLK vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP35 Clk_b11 CLK vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP12 out1 net15 vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP11 net97 out1 vdd! vdd! pepm W=3u L=0.6u m=1.0

MMP9 net103 net24 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP3 net94 net24 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP6 net27 CLK net88 vdd! pepm W=6u L=0.6u m=1.0

MMP5 net88 D vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP4 net27 Clk_b1 net94 vdd! pepm W=6u L=0.6u m=1.0

MMP10 net15 CLK net97 vdd! pepm W=3u L=0.6u m=1.0

MMP7 net24 net27 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP8 net15 Clk_b1 net103 vdd! pepm W=6u L=0.6u m=1.0

MMP1 net60 Clk_b2 net106 vdd! pepm W=6u L=0.6u m=1.0

MMP2 net51 net48 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP13 net60 CLK net112 vdd! pepm W=3u L=0.6u m=1.0

MMP14 net48 Clk_b2 net115 vdd! pepm W=6u L=0.6u m=1.0

MMP15 net121 out1 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP16 net48 CLK net121 vdd! pepm W=6u L=0.6u m=1.0

MMP17 net115 net51 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP18 net106 net51 vdd! vdd! pepm W=6u L=0.6u m=1.0

MMP19 net112 out2 vdd! vdd! pepm W=3u L=0.6u m=1.0

MMP20 out2 net60 vdd! vdd! pepm W=12u L=0.6u m=1.0

MMP0 Clk_b1 CLK vdd! vdd! pepm W=12u L=0.6u m=1.0

.ENDS