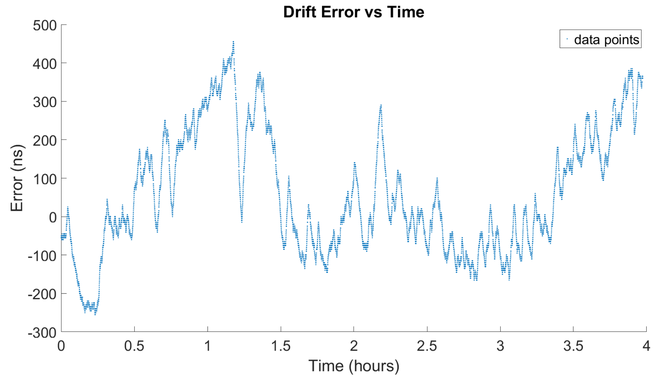
An exploration of a method to use GPS to limit the drift errors in crystal oscillators

Author: Gaurav Manda, University of Minnesota – Twin Cities, Department of Electrical and Computer Engineering
Faculty Advisers: Dr. Demoz Gebre-Egziabher, University of Minnesota – Twin Cities, Department of Aerospace Engineering & Mechanics
Dr. Thomas Posbergh, Dr. Gerald Sobelman, University of Minnesota – Twin Cities, Department of Electrical and Computer Engineering

Abstract : This research will explore a method for using GPS to limit the drift errors in crystal oscillators used to make precise timing measurements in astrophysical experiments. This will use the pulse per second (PPS) signal generated by global positioning system (GPS) receivers as the "heartbeat" for oscillator. The method will be tested out on a detector built at the University of Minnesota to measure the energy and time of arrival of x-ray/gamma-ray photons from astrophysical sources.

Introduction : All digital electronics use clocks to coordinate actions between processes. The basic architecture of all clocks includes an oscillator and a counter which keeps track of the oscillator's frequency. Oscillators change with age and are also affected by various environmental factors including but not limited to temperature, mechanical vibrations and magnetic fields [1].

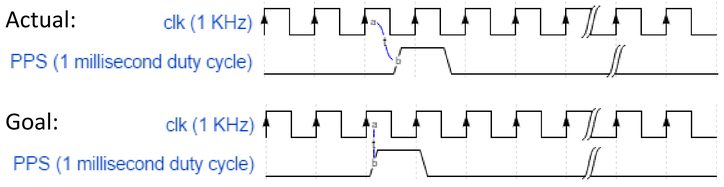


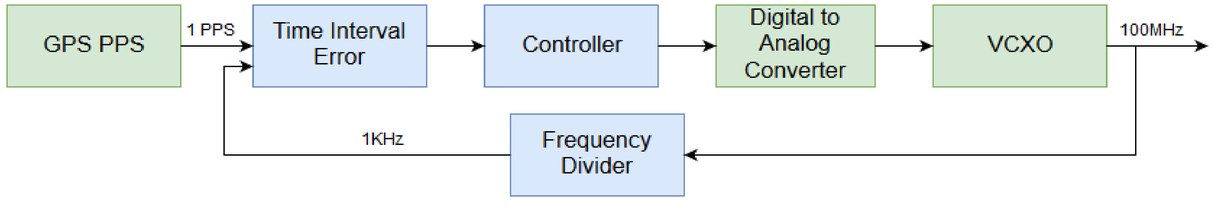
Consequently, this leads to clock drifts which, over of period of time accumulate and become significant. Through the method proposed subsequently, the effort will be to minimize this error by recalibrating the clock using the pulse per second signal from a GPS receiver.

The figure on the left shows the amount of drift the oscillator used for this research produced over a period of 4 hours. This was collected from the timing unit in the FPGA described later. From this data, it can be seen that the oscillator has a maximum absolute drift of about 500 ns.

Design : The basic idea of this system is very similar to that of a phase locked loop. The system consists of the following elements:

- GPS receiver: Gives the PPS signal
- Time Interval Error Measurement unit: This gives the phase error between the 1KHz divided clock and the PPS as shown. The error is calculated by a coarse counter that counts up every rising edge of the 100MHz clock and resets every rising edge of the 1KHz clock. With the input of the PPS signal, the count at the instance is registered as the phase difference. This gives a resolution of 10ns.





- Digital to Analog Converter (DAC): Used to change the control voltage to the VCXO. It has a 16-bit resolution.
- VCXO: Voltage controlled crystal oscillator with center frequency 100MHz is modeled as:

$$Phase(rad), \theta(s) = \frac{2\pi * (2500\ Hz/V) * V_{control}(s)}{s}$$

Control voltage ranges from 0 to 3.3V. Converting this to match the DAC's digital value for simulation purposes and transforming to discrete time (sampling time = 1s):

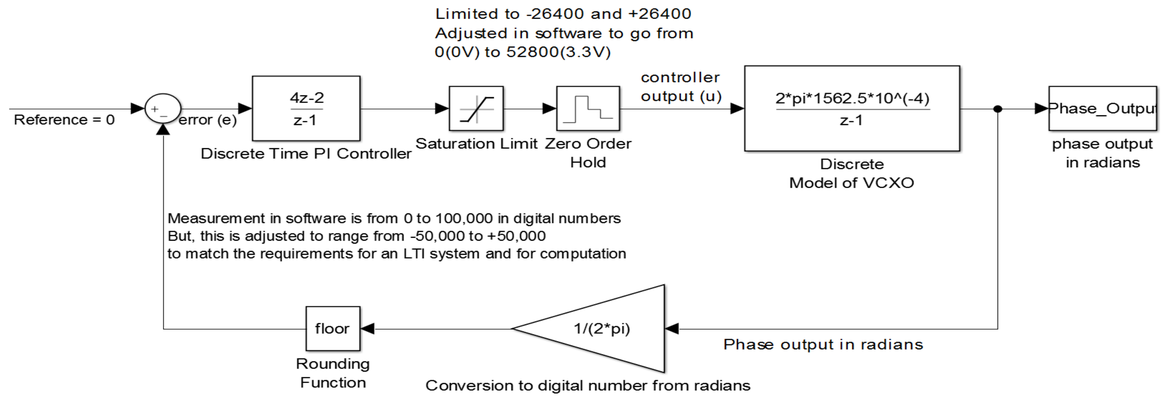
$$Phase(rad), \theta(z) = \frac{2\pi * 1562.5 * 10^{-4} * V_{control}(z)}{z - 1}$$

- Frequency Divider: Divides the 100 MHz clock to a 1KHz clock with a parallel load of 50,000. This is needed to match the PPS high time which is 1ms.
- Controller: A PI (Proportional-Integral) controller with discrete time transfer function was used:

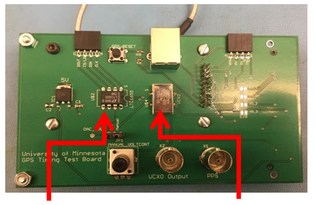
$$K(z) = \frac{4z - 2}{z - 1}$$

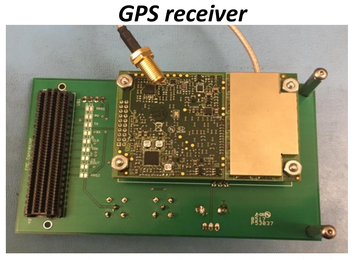
  - Proportional constant, $K_p = 4$, Integral constant, $K_i = 2$
  - Response Time of Controller = ~20 seconds

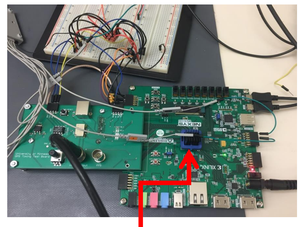
Control System : This is the control loop with all the conversions made for simulations.



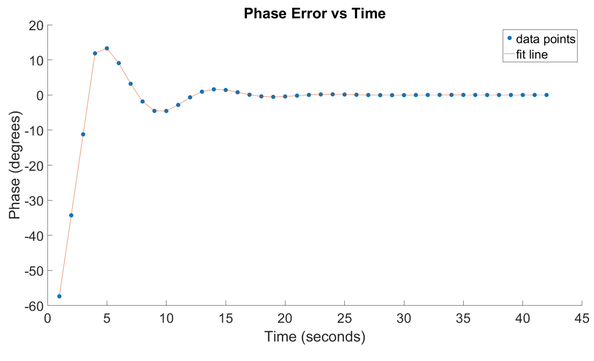
Experimental Setup : As shown below, a Xilinx Artix-7 FPGA was the target device for implementing this algorithm. The device was on development board called Nexys Video. The development board connected to a laptop and MATLAB was used for real time data collection and plotting.
The GPS Receiver used is an OEMStar615.

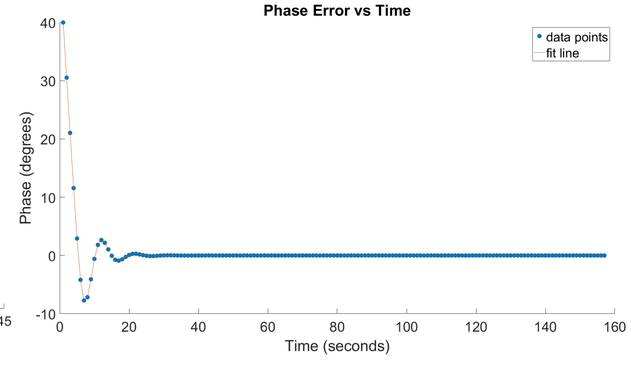






Results : The goal of the controller is to synchronize the clock with the PPS as shown before and to maintain that lock throughout. The phase difference appears only at start up and a couple of plots from data collected from two different experiments using the setup is shown below. It can be seen that the controller has a response time of about 20 seconds and at steady state the absolute error is 20ns as opposed to the 500ns shown before.





Next Steps :

- Improve resolution of Time interval Error Measurement Unit.
- Improve time of response of the controller to a few seconds or milliseconds.

References :

[1] Guoping Liu, Ziyuan Ouyan, Chunlai Li, Jianfeng Liu, "The Importance of Time Synchronization in the Local Networks of the Science and Application Center for Lunar and Deep-space Exploration," Acta Geologica Sinica, Vol.78 No. 5, October 2004, pp.1104-1108.
[2] Y. S. Shmaliy, O. Ibarra-Manzano and L. Arceo-Miquel, "Efficient predictive steering of local clocks in GPS-based timekeeping," 2009 IEEE International Frequency Control Symposium Joint with the 22nd European Frequency and Time forum, Besancon, 2009, pp. 727-732.
[3] Y. Diao, Meng Li, Xiuqing Zhang and Xiaojun Wang, "Satellite disciplined crystal oscillator system based on Kalman filter and PI algorithm," 2014 9th IEEE Conference on Industrial Electronics and Applications, Hangzhou, 2014, pp. 624-628.