

**ULTRA-WIDEBAND TRANSCEIVER DESIGN AND
OPTIMIZATION**

A DISSERTATION

**SUBMITTED TO THE FACULTY OF THE GRADUATE SCHOOL
OF THE UNIVERSITY OF MINNESOTA**

BY

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**IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE DEGREE OF
Doctor of Philosophy**

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July, 2015

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Acknowledgements

I would like to take this opportunity to express my gratitude to the people who have been instrumental in helping me reach this juncture of my life.

I would like to thank Prof. Ramesh Harjani for believing in me and giving me the opportunity to work in his lab. His guidance was extremely valuable. At his lab, I not only got the freedom to work in my area of interest but also experienced how he subtly guided and steered students in the right direction. I learnt from him how to give optimum time in the required area, and how not to debilitate my work by irrelevancy and seek more meaningful research goals. I have been very fortunate to have optimum testing facilities at my disposal. At Dr Harjani's lab, I not only gained technical knowledge but also learnt important presenting and writing skills. As this journey comes to an end, I fondly remember all the get togethers Prof Harjani and Savita Ma'am hosted for us at their beautiful home. I will miss them and the lively discussions I used to have with him and Savita ma'am.

I also extend my gratitude to Prof. Anand Gopinath, Prof. Ted Higman and Prof. Hubert Lim for agreeing to be the part of my defense and preliminary oral committee. Their inputs during the oral exam were valuable for my Phd completion. I am also glad that Prof. Higman and Prof. Harjani gave me the opportunity to teach EE4111 course in Spring 2014. This experience was remarkable because it helped me gain unique

insight into the subject and helped me improve my public speaking skills.

I feel that a lot of academic work depends on the support of your peers. There were many instances when I felt time crunched or when I did not understand something well. I am glad to say that I was blessed to have a very supportive set of people in the lab who inspite of their own commitments, were always there to pitch in. I am indebted to Sudhir for helping me with any doubts related to circuit design, debugging tool related issues, providing a helping hand during the tape outs and just being there for all my irrational and petty questions. I am thankful to Bodhi for the being the senior and guiding me through rough waters in both research and life. I am indebted to Martin for starting the work on my research topic and laying down some strong foundation, teaching me how to solder, operate some of the test equipments and debugging during testing. I am highly grateful to Taehyoun without whose help the chip would not have been taped out. I was just a student right out of school. These people taught me everything that I know about design, test and life. I want to especially thank Sachin and Mohammad for being friends to me, throughout this journey. I also had a brief but great overlap with Satwik, and I am grateful to him for his advice. I had the privilege of neighboring Xingyi in the lab. Naser and Saurabh are great additions to the lab and I want to thank them for their friendship.

I am grateful to Advanced Medical Electronics (AME) for supporting my project. I am thankful to all the team members who have played valuable role in keeping this project alive. Dan Hedin, Tim Riehle, Paul Gibson, thanks a lot for all the effort you have put over the years.

There are many people in the ECE department who silently work behind the scenes and ensure that students always have the best possible facilities. They make sure that we spend minimum time on administrative work and focus most of the time on our

research. I would like to thank Carlos Soria, Chimai Nguyen, Dan Dobrick, Becky Colberg, Linda Jagerson, Kyle Dukart, Jim Aufderhar, Paula Beck and Linda Bullis. I would miss conversations, especially with Carlos and Dan!

I learnt a lot during my two internships at LSI and Broadcom. I was able to imbibe some of the design methodology and practices that ensure success of design in my project as well. I am indebted to my managers Dave Grover, Seong Ho Lee, Duke Tran and Michael for giving me the opportunity to work in their teams. I have had the privilege of knowing some really good people during the internships. I want to especially thank Vaibhav Pandey for making it possible for me to work at Broadcom and also for being there for me, as a true friend. I am also thankful to him for introducing me to some really wonderful people in Irvine.

A special mention to CJ Loosbrock for giving me an opportunity to work at CTS. I have learnt a lot and I have always received respect and appreciation from this wonderful lady.

I want to thank Jon Werder and Michael Stilley for giving me the opportunity to work at Medtronic. The organization is motivating me to do my little bit in alleviating pain, restoring health and extending life, through my knowledge of engineering science.

Outside the lab, many people helped me when I came to Minneapolis. I am extremely thankful to Pratibha aunty and Navin uncle for opening their home to me when I first came here. I also want to thank Abhijit, Gaurav, Akshay, Tanvi, Swayambhoo and Ram for their friendship and affection. I also want to thank Marwah uncle who has always been there, any time of the day, answering my questions on life and health and giving me invaluable guidance. I have found some really good friends at the squash courts at the U - Sunil, Shyam, John. Looking at John play, I get re-energized about life.

I would also like to thank Raunak, Jayant, Sauvik, Priyesh and Vineet, for making

high school such a great experience. Their company made me more determined towards engineering and they still inspire me through life.

Pilani has always been the ground zero. The friends I have made there have time and again proven that no matter the distance and the time, they are always there to lend a hand. It would be hard not to mention some names - Gulli, Salil, Luniya, Chhavi, Yadav, Hardeep and Mandal and the JiNxD. Pilani has given me a fearless and courageous attitude. Pilani teaches you how to live!

Finally, I will be ever grateful to my parents for believing in me and supporting me in every endeavor that I undertook. They always ensured the best for me and gave me all the freedom to do what I liked the most. My brother has been the pillar of strength and has always stood by me in spite of me getting angry at him sometimes.

In Amrita, I have always found peace and love. It has been 12 years of knowing her and I still cant believe how lucky I got. I have always found solace with her, whether it was sitting on a school bench a decade ago, or talking across the Atlantic and Europe. I am happy to have her undying support and patience.

My grandmother owns a special place in my heart that no one else can ever fill. She has fed us, cared for us and loved us like no other. I will always be indebted to her. She is the strength that I have watched all my life. I cannot be more thankful to anyone.

Thank you.

Dedicated to my Grandmother,

राज रानी

my Parents, my brother,

अलका । अनूप । अभिषेक

and my wife

अमृता

Abstract

The technology landscape has quickly changed over the last few years. Developments in personal area networks, IC technology, DSP processing and bio-medical devices have enabled the integration of short range communication into low cost personal health care solutions. Newer technologies and solutions are being developed to cater to the personal operating space(POS) and body area networks(BAN). Health care is driving towards using multiple sensor and therapeutic nodes inside the POS. Technology has enabled remote patient care where the patient has low cost on-body wearables that allow the patient/physician to access vital signs without the patient physically visiting the clinic. Big semiconductor giants want to move into the wearable health monitor space. Along with the developments in fitness based health wearables, there has been a lot of interest towards developing BAN devices catering to the ‘mission-critical’ wearables and implants. Hearing aids, EKG monitors, neurostimulators are some examples. This work explores the use of the 802.15 ultra wideband (UWB) standard for designing a radio to operate in the a wireless sensor network in the BAN. The specific application targeted is a hearing aid. However, the design in this work is capable of working in a low power low range application with the ability to have multiple data rates ranging from a few kHz to 10’s of MHz.

The first radio designed by Marconi using spark-gap transmitters was an impulse radio (IR). The IR UWB technology boasts of low power, low cost, high data rates, multiple channels, simultaneous networking, the ability to carry information through obstacles that more limited bandwidths cannot, and also potentially lower complexity hardware design. The inherent timing accuracy associated with the technology gives

UWB transmissions immunity to multipath fading and are hence make them more suitable for a cluttered indoor environment. The key difference with the traditional narrowband transceiver is that instead of using continuous wave (CW) transmission, impulses in time are used. The timing accuracy associated with these impulses require synchronization in time, rather than synchronization in frequency for carrier-based CW systems.

A complete fully integrated system is presented in thesis. This work presents a low-power noncoherent IR UWB transceiver operating at 5GHz in 0.13- μ m CMOS. A fully-digital transmitter generates a shaped output pulse of 1GHz 3-dB bandwidth. DLLs provide a PVT-tolerant time-step resolution of 1ns over the entire symbol period and regulate the pulse generator center frequency. The transmitter outputs -31 dBm (0.88pJ/pulse at 1Mpulse/s) with a dynamic (energy) efficiency of 16pJ/pulse. The transmit out pulse is FCC part 15 compliant over process voltage and temperature (PVT) variations. The transmitter is semi-compliant with IEEE 802.15.6 and IEEE 802.15.4 standards and will become completely compliant with minor modifications.

The receiver presented in this work is a non-coherent energy detect IR UWB receiver. The receiver has an on-chip transformer preceding the LNA, which is followed by a super-regenerative amplifier (SRA), envelope detector, sample-and-holds, and a bank of comparators. The design is SRA based energy-detection receiver. Measured results show a receiver efficiency of 0.32nJ/bit at 20.8Mb/s and operation with inputs as low as -70 dBm. The SRA based energy-detection receiver utilizes early/late detection for a two-step baseband synchronization algorithm.

An integrated solution to the issue of synchronization is also proposed. The system proposed is capable of synchronization and tracking control. The system in this work utilizes early/late detection for a two-step baseband synchronization algorithm. The

algorithm is implemented in Matlab and the time to synchronization is observed to be between $250\mu s$ to a few couple of ms. Measurements have also been made using the receiver and manually implementing the algorithm. This work addresses all aspects time synchronization in an IR transceiver. The initial mismatch is addressed by two methods. Beyond the initial synchronization, the system presented in this system is also capable of tracking. This would mean that once the transceiver has been synchronized, the timing generation would continue to track the phase and the frequency changes depending upon crystal drift over time or movement between the receiver and the transmitter.

A test was also performed on the complete transceiver system with two radios talking to each other over a highly attenuated wired channel.

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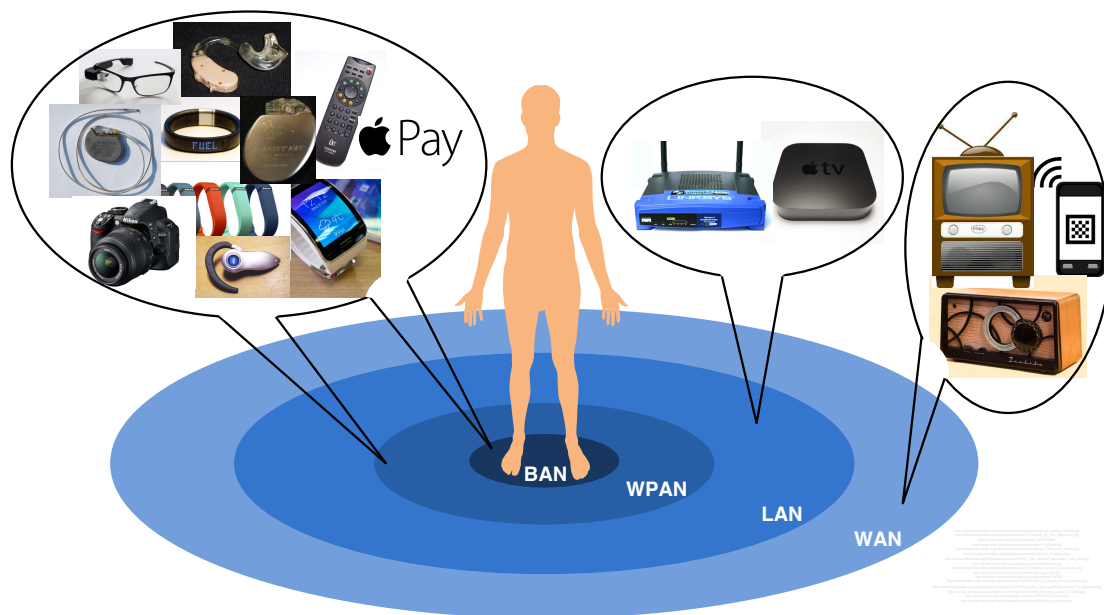
Chapter 1

Introduction

1.1 Wireless Communication

The development of wireless technology has seen a big surge in recent times. The products using wireless technology has seen a boom and the trending path is even steeper. Internet of Things (IoT) as a concept has developed into an amalgamation of multiple varied disciplines fueling the product growth trend even further. Wireless is becoming ubiquitous in the true sense of the word. [3] mentions that the number of active cell phones exceeded the total population (7.3 Billion) in 2014. According to another report [4], in 2013, 80 things per second were connecting to the internet, increasing to almost 100 per second in 2014, and by 2020, more than 250 things will connect each second. The IoT is expected to connect 28 billion things to the internet by 2020 [5]. The number of devices connected to a cellphone via wireless links in also increasing leaps and bounds. The number of devices will only increase in the future. The primary reason for this growth being ease of integration through CMOS and the drive towards integrating multiple devices to a network through single or multiple standards.

Although the first commercially successful radio was developed by Marconi in late



Wireless communication standards are majorly divided into categories depending on the rate of data throughput and range of operation. Fig. 1.6 compares the different standards on basis of power, data throughput and range. Although Body Area Network

Table 1.1: Comparison of a few commercial wireless communication standards

Commercial name	Standard	Theoretical data rates	Nominal range	Frequency
Bluetooth LE	IEEE 802.15.1	1Mb/s	10m	2.4GHz
Zigbee	IEEE 802.15.4a	250kb/s	10-100m	868/915MHz; 2.4GHz
MedRadio	IEEE 802.15.6	200kb/s	10-50m	403.5MHz
UWB	IEEE 802.15.3a	110Mb/s	10m	3.1-10.6GHz
UWB	IEEE 802.15.4a		100m	249.6-749.6MHz; 3.1-4.8GHz; 6.0-10.6GHz
MBAN	IEEE 802.15.4j	250kb/s		2.38GHz
WiFi	IEEE 802.11a	54Mb/s	120m	5.5GHz
WiFi	IEEE 802.11b	11Mb/s	140m	2.4GHz
WiFi	IEEE 802.11g	54Mb/s	140m	2.4GHz
WiFi	IEEE 802.11n	248Mb/s	250m	2.4/5.5GHz
WiMAX	IEEE 802.16a	70Mb/s	50km	2.5/3.5/5.8GHz

(BAN) and Wireless Personal Area Network (WPAN) are generally used interchangeably, there is a distinction. While WPAN looks for communications in the personal operating space (POS) of around 10m [8], BAN is a more tighter radius around the body. A Body Area Network is formally defined by IEEE 802.15 as,

A communication standard optimized for low power devices and operation on, in or around the human body (but not limited to humans) to serve a variety of applications including medical, consumer electronics / personal entertainment and other [9].

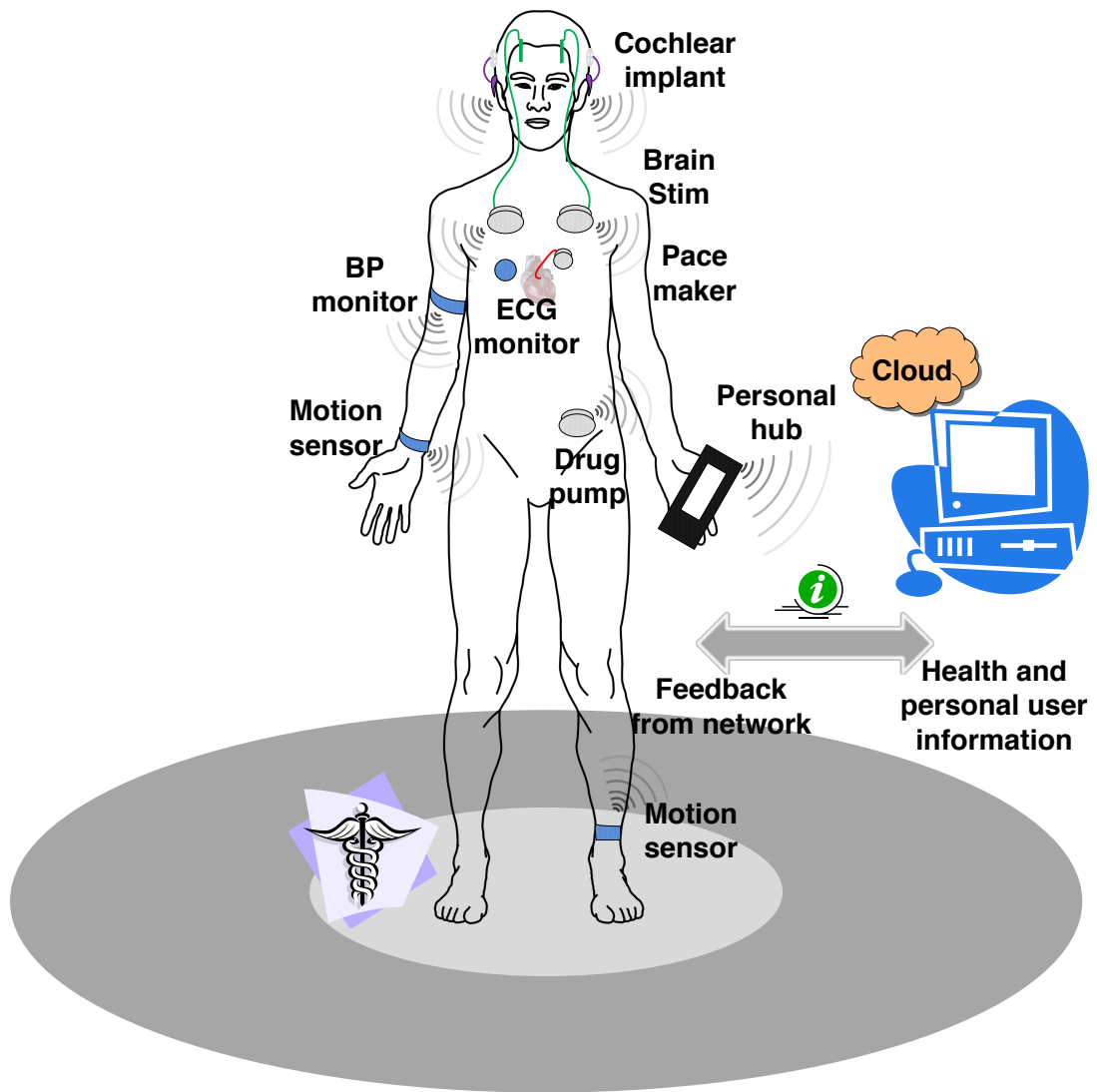


Figure 1.2: Health care and body area network

1.2 Target Application

1.2.1 Background

The health care facilities in U.S. are considered by many to be one of the best in the world. Health care facilities are largely owned by private sector. According to the World Health Organization (WHO), the United States spent more on health care per capita (8,608), and more on health care as percentage of its GDP (17.2%), than any other nation in 2011 [10]. Despite the availability of resources, record levels of health care spendings and health care reforms, the cost of health care is excessive, leading to almost 50 million people without health insurance in 2007. According to the “United States Registered Nurse Workforce Report Card and Shortage Forecast” published in the January 2012 issue of the American Journal of Medical Quality, a shortage of registered nurses is projected to spread across the country between 2009 and 2030 [11]. A combination of high costs and shortage of primary care providers has causes a human crisis. Primary care and health monitoring are key to avoiding bigger health risks.

Recent developments in personal area networks, IC technology, DSP processing and bio-medical devices have enabled the integration of short range communication into low cost personal health care solutions. Technology has enabled remote patient care where the patient has low cost on-body wearables that allow the patient/physician to access vital signs without the patient physically come in for an appointment. Multiple body monitors are now available and innovation is on a growth curve. Fitbit [12] activity and heart rate tracker, QardioCore -EKG/ECG monitor [13] for iPhone, IntelliVue MX40 wearable patient monitor [14] and InfraV No-Blood, Glucose Vital Signs Monitor Watch [15], made for iPhone hearing aids [16] shown in Fig. 1.3 are only some examples.



Figure 1.3: Some examples of wearable health monitors

Big semiconductor players Apple, Google and Samsung are rushing to the emerging market.

A target application where the innovation, miniaturization and health solution integration will prove beneficial is wireless hearing aids. According to the National Institute of Health, National Institute of Deafness and Other Communication Disorders, about 2 to 3 out of every 1,000 children in the United States are born with a detectable level of hearing loss in one or both ears [17] and approximately 15% of American adults (37.5 million) aged 18 and over report some trouble hearing [18]. The technology advancement and the need for hearing aids translates to development of a device that can not only primarily address the medical requirement of hearing impairment, but also answer other connection demands including but not limited to consumer devices like iPhone, iPod, etc. Wireless hearing aids with integrated transceivers can serve multiple radio links such as ear-to-ear, ear-to-consumer device, and between the ear and a distant base station [19].

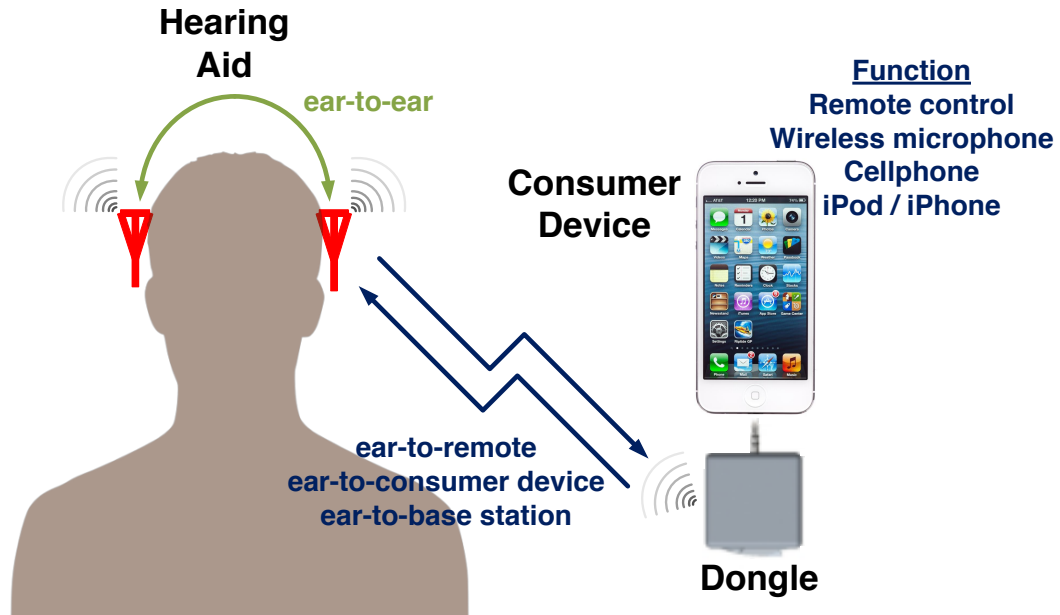


Figure 1.4: Target application - Hearing aids with different channels

This work aims at developing a low power radio solution for these target applications. The audio streaming around the head and body is faced with multiple challenges as shown in Fig. 1.4. The radio needs to be capable to provide variable data rate to support specific target applications -

1. Low data rate control application for ear-to-ear and ear-to-remote
2. High data rate voice streaming application for ear-to-consumer device and ear-to-base station

1.2.2 State of Art

State-of-art hearing aids and companion microphones shown in Fig. 1.5 are generally implemented using narrowband FM techniques. Phonak Smartlink [20], Sonovation Logicom [21] are examples of narrowband FM radios used for hearing aids. FM is highly



Figure 1.5: State of art hearing aids and wireless microphones

susceptible to eavesdropping and any interference can distort the signal resulting in reduced performance. SoundID, Beltone [22] and Starkey [16] systems use bluetooth(BT) to establish wireless link. Although BT is an upcoming technology, it does come with it's drawbacks including high power drain and low data rate for the low energy(LE) version. BT also suffers from co-existence in the ISM band at 2.4GHz, which under the most extreme of circumstances can completely lose connectivity.

1.2.3 Limitations

The constraints of small form factor, low power, low cost are coupled together with bandwidth, frequency and protocol of operation, and design of the wireless radio.

Size

A small form factor coupled with low power and low cost is essential for an integrated solution for a hearing aid. As a key constraint on the final product, the integrated radio needs to be placed inside a hearing aid. The wireless transceiver along with the antenna needs to comfortably fit into a small device with convenient form factor, which

restricts the length of the antenna and puts the choice of the radio in the high MHz to GHz range. Often, the antenna size is referred to relative to the wavelength. As the frequency increases, the wavelength drops. Designing a transceiver in the high MHz to GHz range gives a reasonable antenna size which can be optimized for more directional and optimum performance.

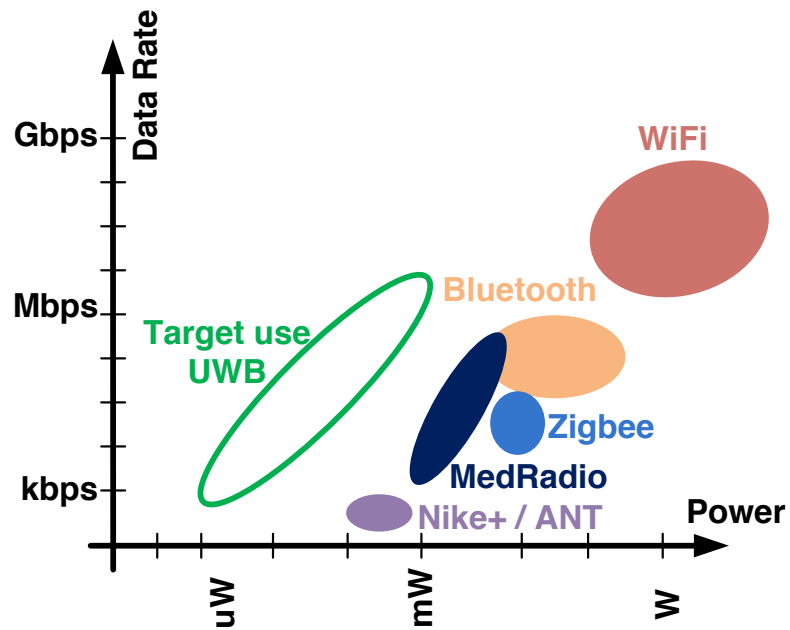


Figure 1.6: Technology categories

Power

Due to the restricted size on the battery, a low power sub-mW radio is required. As described above, there are multiple standards even in the frequency range of interest, that can be analyzed to come to an optimum radio design. Fig. 1.6 differentiates standards on basis of power and data throughput. From the comparison of standards on the power

versus data rate scale, there is a part the spectrum that needs to be filled. A low power low data rate standard needs to be established to answer questions where extremely low power and low-to-mid rate data throughput solution is required. The FCC UWB 802.15 standard allows a maximum of -41.3dBm/MHz power spectral density [23] which makes it an extremely viable choice for such transceivers. The allowed power constraint is shown in Fig. 1.11. This limit is the same as the Part 15 limit that is allowed for the noise emissions of an electronic design, thus essentially re-using the noise floor [24].

IR UWB has a very high resolution in time. The time based impulses used to send and receive data are about a nanosecond or shorter in duration. This gives a unique opportunity to the radio to have a highly duty cycled system. For a data rate of 100kb/s and a bandwidth of 2GHz i.e. impulse duration of 500ps, the system can be duty cycled by as much as 0.005%. This duty cycling should be expected to give very low power dissipation, because almost all the time is spent in idle or sleep mode. Fig. 1.7 shows a basic difference in the IR and the CW approaches. The continuous wave radios however need to continuously operate the frequency synthesizers.

Cost

There are different methods that the FCC uses to make spectrum available for wireless services, including licensed and unlicensed spectrum. Licensing spectrum from FCC can be complex as well as very financially intensive. Unlicensed spectrum comes in multiple categories - dedicated, shared and opportunistic unlicensed. Different unlicensed standards include WiFi, Bluetooth, Zigbee, WiMax and WiMedia utilizing majorly either the dedicated Industrial, Scientific and Medical(ISM) band, dedicated Unlicensed National Information Infrastructure (U-NII) or the shared 802.15 ultra wideband standard [25]. The ISM band at 2.4GHz and the 5GHz U-NII band are lucrative choices. The

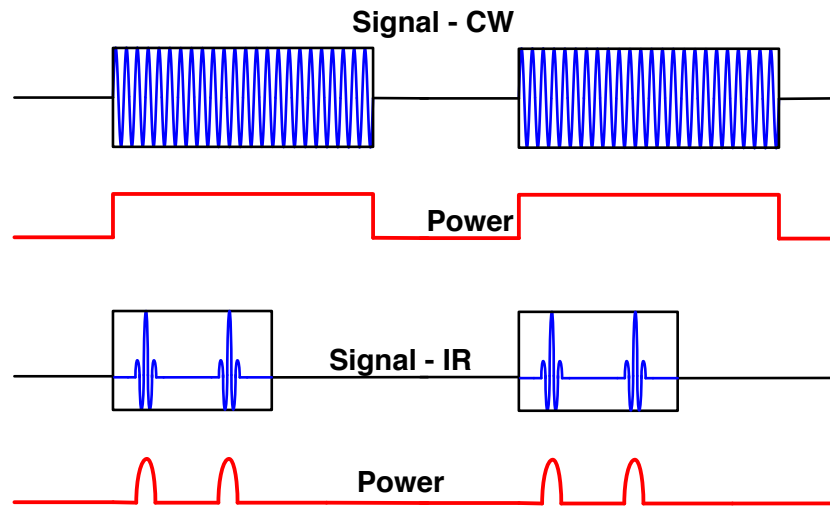


Figure 1.7: Duty cycling in IR UWB

2.4GHz ISM band is a highly occupied band being shared between WiFi, microwave ovens, cordless phones and bluetooth. Power and silicon area intensive techniques like direct sequence spread spectrum (DSSS) and orthogonal frequency-division multiplexing (OFDM) are used by radios to be tolerant to interference in this band. With WiFi becoming almost omnipresent, it will be a major source of in-band interference at both 2.4GHz as well as 5GHz. The FCC allows unlicensed use of UWB spectrum space. Ultra-wideband(UWB) radio systems do not need basestations and complex radio networks. This ad hoc network provides the benefits of cost reduction while simultaneously saving on power.

Design Complexity

Traditionally impulse radio has been the simplest of the radio architectures. Fig. 1.8, 1.9 compares a superheterodyne architecture to an impulse radio system. A superheterodyne system uses frequency conversion to move the signals up - for transmission - or

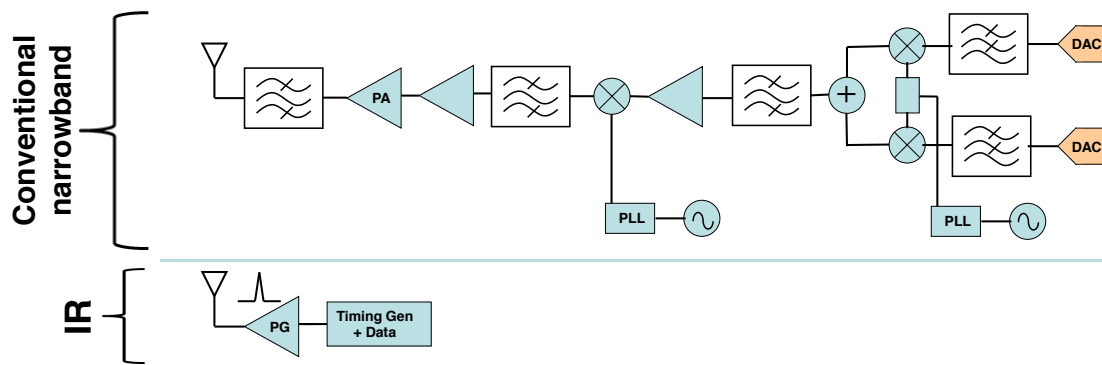


Figure 1.8: Comparing traditional narrowband heterodyne and IR UWB transmitter

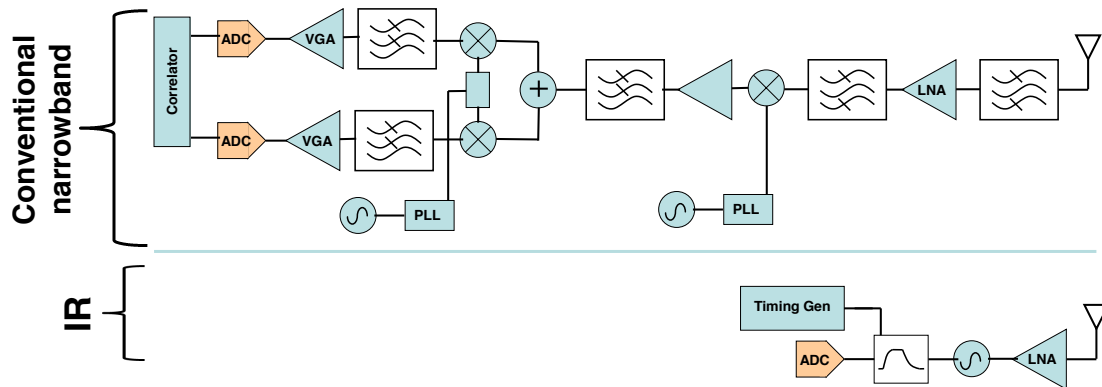


Figure 1.9: Comparing traditional narrowband heterodyne and IR UWB receiver

down - for reception - in frequency. It is easier to handle signals at lower frequency, however, a higher frequency signal is required for better utilization and sharing of the frequency spectrum. For example a signal of bandwidth 50MHz has a spectral occupation % of 10 at 500MHz, but has a spectral occupation of 1% at 5GHz, thus accommodating more users. These systems tend to be narrowband.

A carrier based transceiver scheme requires more complex blocks like mixers and frequency synthesizers to frequency translate the signals. These blocks are extremely power hungry. There are numerous filters required in the system, since the detection or transmission is in frequency and the system does not want to receive or transmit unwanted signals outside the frequency spectrum of interest. These filters generally have an inductive component which gives them the narrowband nature. Inductors are huge structures and occupy a lot of expensive silicon real estate. IR UWB on the other has very simple systems to offer, thus avoiding design complexity, large silicon area and heavy power consumption.

1.3 Ultrawideband: The Solution

1.3.1 Timeline and Definitions

Fig. 1.10 shows the history of the development of UWB. From 2002-2015, it is interesting to note that out of a total of 16,130 publications on ‘uwb’ or ‘ultra wideband’, only 541 referred to ‘synchronization’. Only a handful present an integrated solution [26–33].

Guglielmo Marconi who is considered to be the inventor of radio used spark-producing radio transmitter in his quest to achieve telegraphy without wires. This first radio transmission served as the base that Marconi used to transmit data impulses across the

Table 1.2: Comparison of narrowband and UWB systems

Narrowband	UWB
Advantages	
Stable longer range communication Efficient spectral occupation allowing multi-user access Well know frequency based synchronization	Low complexity architecture Highly duty-cycled with extremely high time resolution Ultra-low power High channel throughput at low range Immunity to multi-path fading Tolerant to narrowband interferers
Disadvantages	
Complex architecture Use of power hungry components - Mixer, PLL, VCO, PA Multiple filters required to satisfy out-of-band emissions Limited channel throughput LO pulling	Intersymbol interference because of delay spreading Time synchronization for non coherent system Jammer tolerance for energy detect system

Atlantic ocean. However, the benefit of a large bandwidth and the capability of implementing multiuser systems provided by electromagnetic pulses were never considered at that time. The spectrum sharing was more in terms of wavelengths.

Simultaneously, Reginald Fessenden and Armstrong were working on developing the now more commonly used heterodyne receiver and variations serving as the backbone of continuous wave (CW) radiotelegraphy in opposition to the spark gap radio transmitters which were short duration bursts of radio waves. With the advent of arc converter, CW transmitters were adopted. Arc converters allowed the generation of undamped

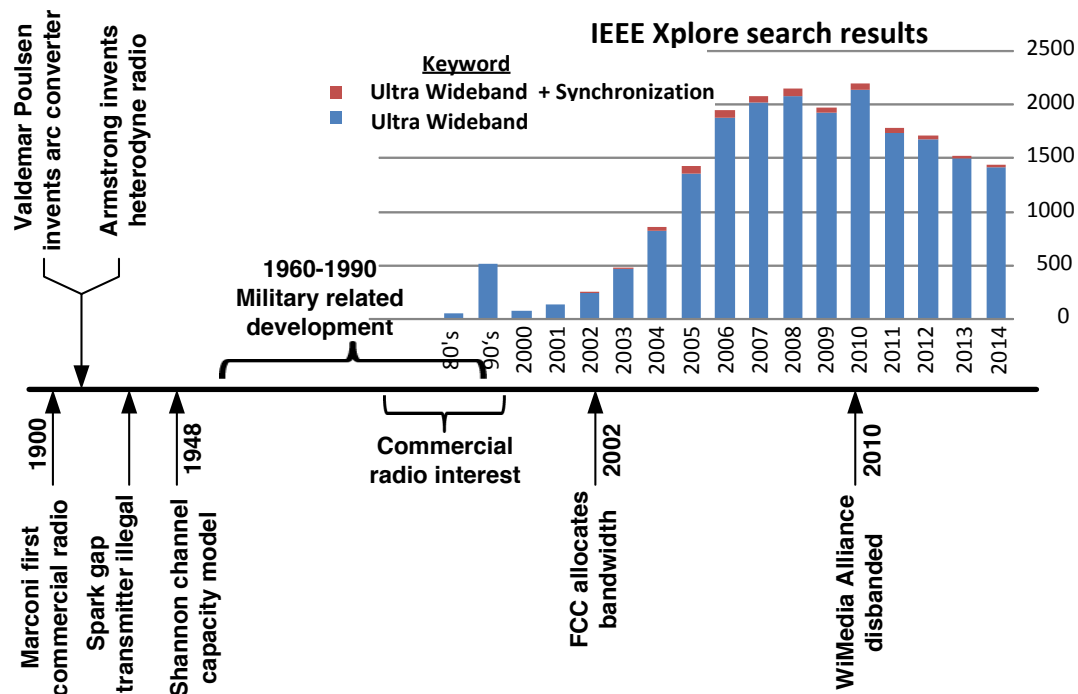


Figure 1.10: UWB technology timeline

sinusoids allowing narrowband applications. Arc converters can be thought of as the CW frequency generators from the early 20th century.

The Communications Act of 1934 established the Federal Communications Commission (FCC) giving regulatory powers in both wire-line and radio based communications. Stations were to be licensed and separated by wavelength, or frequency, and stations were to use a “pure wave and a “sharp wave (sine wave carriers) in the words of the FCC. Sine wave communications and narrow band signals were now mandated. Unfiltered spark emissions, dubbed class B damped sine wave emissions, were prohibited [34].

In 1948, Shannon [35] talks about a mathematical model of communications and the relation between channel capacity and signal bandwidth. The channel throughput,

$$C = B * \log_2(1 + \frac{S}{N}) \quad (1.1)$$

where,

C is channel capacity

B is the bandwidth

S/N refers to the signal-to-noise or carrier-to-noise ratio

One thing to note is that, although channel capacity is directly proportional to the bandwidth, the logarithmic term becomes significant at larger distances and narrowband performs better than UWB.

Interest in ultra-wideband impulse based radios was re-established in the mid 20th century primarily due to the work that was undertaken by the US military into defining the behavior of microwave networks to impulse or transients. In the later 20th century, ultra-wideband technology was pioneered by Robert Scholtz and others for short range, high bandwidth communications.

In February, 2002, the FCC authorized unlicensed use of the UWB in the frequency range of 3.1GHz to 10.6GHz. According to the Code of Federal Regulations Title 47, Part 15, Subpart F, ultra-wideband (UWB) transmitter is defined as *An intentional radiator that, at any point in time, has a fractional bandwidth equal to or greater than 0.20 or has a UWB bandwidth equal to or greater than 500 MHz, regardless of the fractional bandwidth.* The UWB bandwidth of a UWB system operating under the provisions of this section must be contained between 3100 MHz and 10,600 MHz.

The FCC allocates 3.1GHz - 10.6GHz for the ultra-wideband standard, providing bandwidth control from 500MHz to 7.5GHz. The data throughput can be controlled by monitoring the bandwidth for a fixed data rate or by monitoring the data rate for a fixed bandwidth. UWB is capable of supporting very high data rates due to large available

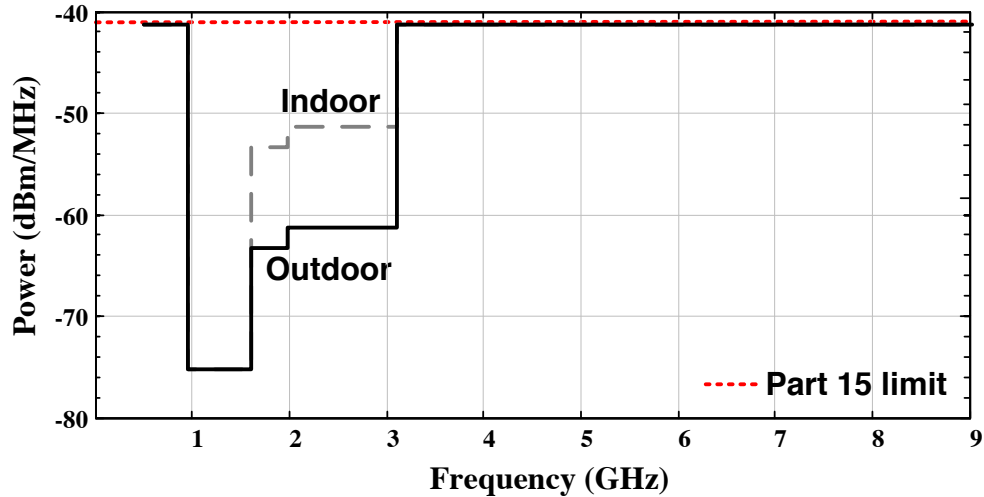


Figure 1.11: FCC power density restrictions on UWB

bandwidths. After the the spectrum was allocated in 2002, IEEE set out to develop an international technical standard for UWB. The two standards being investigated were IEEE 802.15.3a for high rate WPAN and IEEE 802.15.4a for low rate WPAN.

For the formulation of technical standard for the 802.15.3a, two industrial conglomerates emerged - the UWB Forum backing direct sequence spread spectrum and WiMedia Alliance endorsing multiband orthogonal frequency division multiplexing. The solutions being mutually exclusive never found common ground, and lead to a stalemate of the process and finally concluding into withdrawal of the 2002 project authorization in 2006. The task group (TG3a) was disbanded by the IEEE standards association. The WiMedia Alliance transferred the UWB specifications to Bluetooth Special Interest Group (SIG) and formally terminated all work in 2010 [36].

However, the 802.15.4a standard has received more success in the radar, ranging and positioning target applications. UWB continues to have the advantages it boasted of. UWB benefits include low power, low cost, high data rates, multiple channels, simultaneous networking, the ability to carry information through obstacles that more

limited bandwidths cannot, and also potentially lower complexity hardware design [37]. The duration of each pulse in UWB-IR system is extremely short (100s of ps to a few ns), thus giving UWB transmissions immunity to multipath fading and are hence more suitable for a cluttered indoor environment. The impulses are limited by intersymbol interference because of the delay spreading.

1.3.2 UWB Systems - Design and Techniques

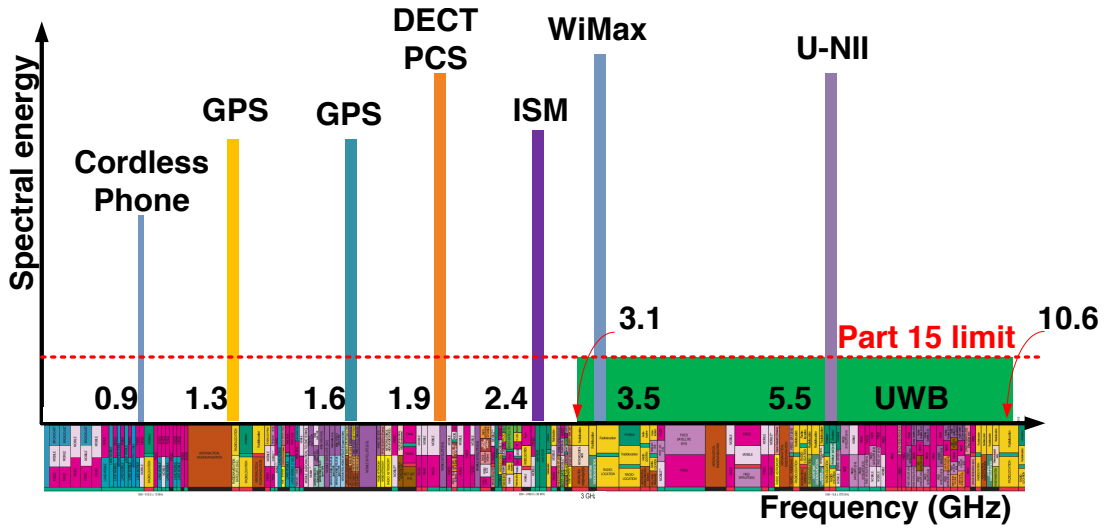


Figure 1.12: Frequency spectrum [2]

The approaches of designing an UWB transceiver can be split on a matrix of two independent features. The two key design categorization principles are

1. Carrier-based vs carrierless UWB

This method of generating UWB signals uses more traditional spreading techniques that are based on either single carrier (Direct Sequence Spread Spectrum DSSS, Frequency Hop Spread Spectrum FHSS) or multi-carrier techniques (Orthogonal Frequency Division Multiplexing OFDM) or combinations of both. Such

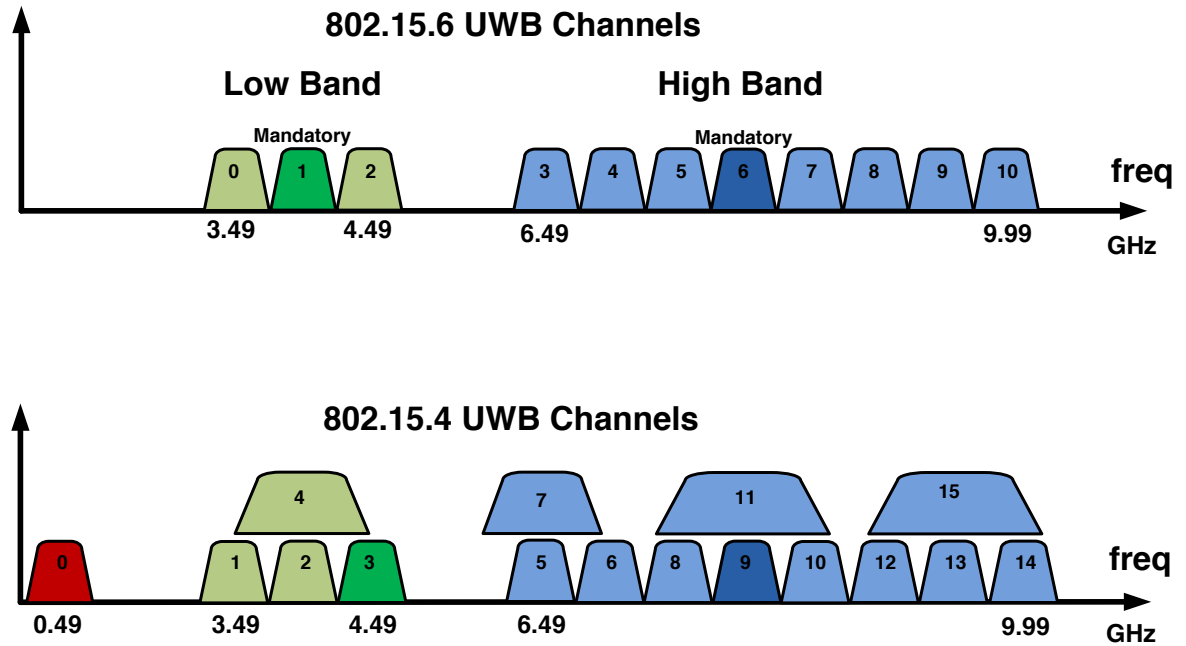


Figure 1.13: UWB bands

systems use traditional heterodyning architectures and can be realized as either single band or multi-band designs Fig. 1.13.

In the case of impulse radio based UWB the signal is generated using very short, low duty-cycle, baseband electrical impulses. As no carrier is used to up-convert the signal such systems are often called carrierless communications systems.

2. Coherent vs non coherent UWB

Carrier phase information is needed for Coherent systems. Receiver use matched filters (or correlation receiver) to detect and decide the transmitted data.

Non-coherent systems do not need carrier phase information and use methods like square law (push detection or energy detection) to recover the transmitted data at receiver end.

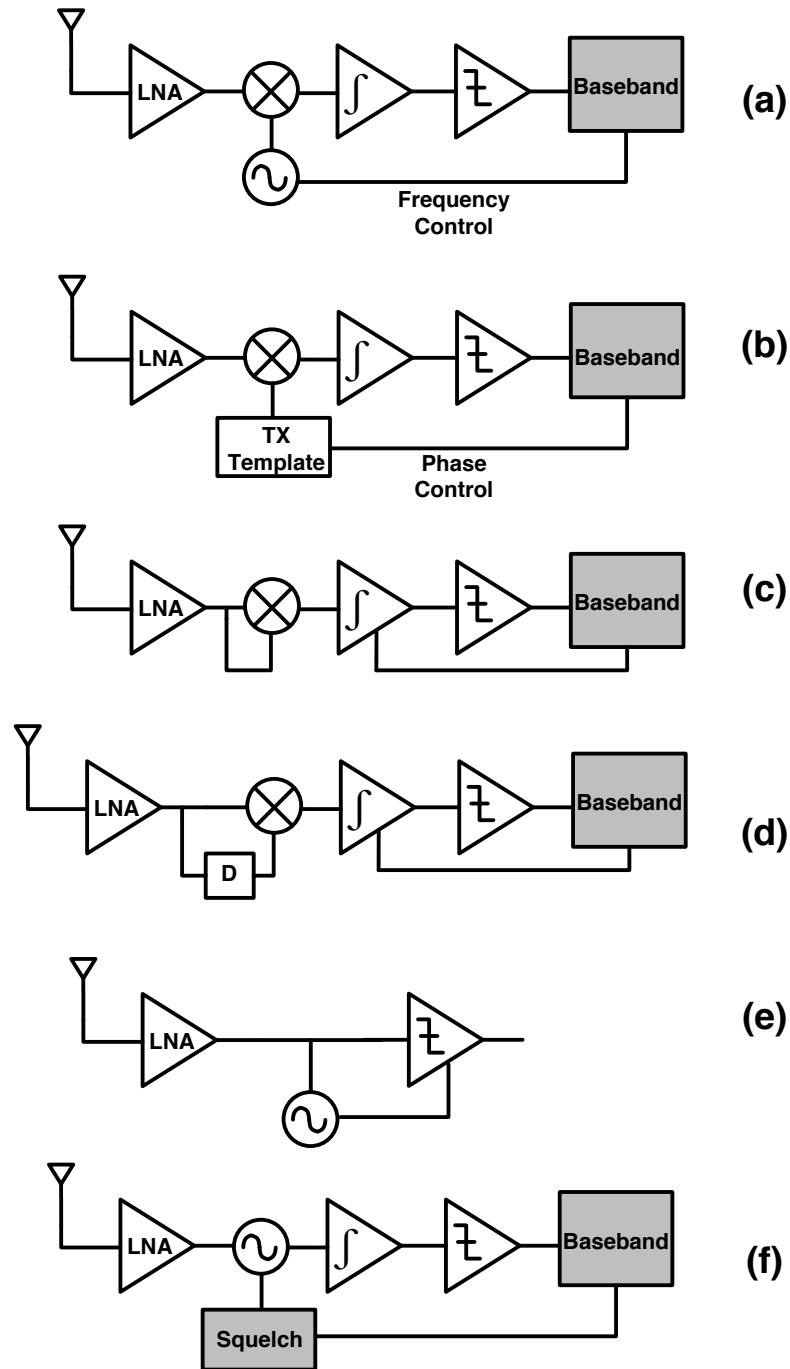


Figure 1.14: UWB architecture

A carrier based transceiver scheme requires mixers and frequency synthesizers to frequency translate the signals. Multi-Band (MB) OFDM UWB, Frequency Modulation(FM) UWB and Direct Sequence(DS) UWB transceivers are carrier based designs, and use power hungry complex blocks like mixers, frequency synthesizers to translate the signals Fig. 1.14. MB-OFDM UWB is very similar to the traditional narrowband system [38], and is not a very attractive low power, low area architecture.

IR-UWB receivers are implemented in both coherent and non-coherent architectures. Coherent systems are generally employed in high data-rate applications, as compared to the non-coherent UWB systems which are more adept towards low data-rate applications like wireless sensor networks. **This work focuses on developing a variable data-rate UWB system.** IR UWB are well geared towards solving this problem statement.

In Fig. 1.14, various different varieties of UWB radios are shown, both coherent and non-coherent.

Fig. 1.14 (a) shows a simple heterodyne receiver, the RF chain contains mixers for up/down conversion. The system also contains frequency synthesizer or local oscillator that would need to be continuously ON for the mixer to operate correctly. The frequency synthesizer needs to be programmable to deal with any multi-band UWB signals as well as any mismatches in frequency. For a CW UWB, the frequency synthesizer needs to have a lot of control as the signal is detected in frequency rather than time. Along with complexity in the frequency synthesizer, the RF front end needs to be extremely wideband and programmable for detecting multi-band signals adding design complexities. For an IR UWB application, this method simplifies the synchronization process but at the cost of increased power consumption, since the frequency synthesizers need to be continuously ON.

Fig. 1.14 (b) shows a coherent IR receiver using the pulse template for signal

detection. Although this design saves on frequency synthesizer power, complexity and area, it has pulse generation and timing operations as complexity and design overheads. It also has not eliminated the power hungry mixer block. Coherent UWB systems can have a higher data-rate at the cost of power consumption due to continuous operation of the mixer and design complexity.

Fig. 1.14 (c)-(e) illustrate different varieties of non-coherent UWB systems.

Designs **Fig. 1.14(c-d)** are conventional non-coherent receivers which use self-mixing with the received signal or a delayed version of the received signal. Although these have some reduction in power consumptions, these systems still contain the complex and power hungry mixer block.

Fig. 1.14 (e) is another alternative using injection locking. Injection locking needs a power hungry local oscillator/frequency synthesizer.

A carrierless UWB-IR scheme allows for transmission of data in bursts (energy impulses) giving the circuit adequate sleep time during transmissions, hence lowering the power consumption and increasing the battery life. Due to the difficulty of controlling the exact shape of the impulse, and consequently the overall frequency response, such systems tend to use the overall frequency band and are sometimes also called single-band systems [38]. Impulse radio utilizes short pulses without the use of a carrier. This method is more cost effective and power efficient. As a general rule of thumb, carrierless noncoherent UWB systems are less complex and less power intensive systems than their coherent or carrier-based counterparts.

An impulse radio, as the name implies, is sending or receiving data as a time domain pulse. As compared to the traditional architectures IR tries to be precise in time rather than frequency. The data can be random in time thus enabling time modulation or pulse-position modulation. IR can be used to transmit/receive data for low power

applications. Unlike carrier-based radios which operate on periodic waveforms, this transceiver sends and detect the reception of bursts of energy (impulses). This allows circuits to be switched off or to low-power modes in between communication activity.

UWB-IR systems are time-based, i.e. detect sequences in time, hence timing synchronization between the transmitter and receiver is critical for demodulation.¹ Due to high time resolution, the timing constraints associated with IR systems are extremely accurate and hence synchronization in time becomes a critical issue driving IR transceivers. A mismatch in timing can be cause either by a phase inaccuracy or a frequency inaccuracy. A phase mismatch may be a result of start-up offset between 2 radios, or movement of the radios causing the impulses to reach at different times and hence different phases of the system clock. A mismatch in frequency may be a result of crystal offsets. In spite of the timing constraints, the advantages of using an UWB-IR architecture determined using a non-coherent energy detection based carrier-less radio for addressing the target application of a universal hearing aid, where the hearing aid is also used to connect to consumer devices. On the academic front, transceivers for wireless hearing aid have been implemented using either a narrowband [39] or using carrier based UWB [19]. In this thesis, a carrierless UWB-IR based transceiver for wireless hearing aid applications is presented. Traditional narrowband systems require extremely high frequency clocks capable of sampling sub-nanosecond time delays for optimal utilization of the timing accuracies inherent to an impulse radio system. These clock generation blocks contribute tremendously to the power and elimination of these blocks simplify the complexity of the architecture along with alleviating the power issues caused by clock generation blocks. Power reduction can be achieved by going to simple radio architectures.

¹ In carrier-based systems frequency synchronization between the transmitter and receiver is critical.

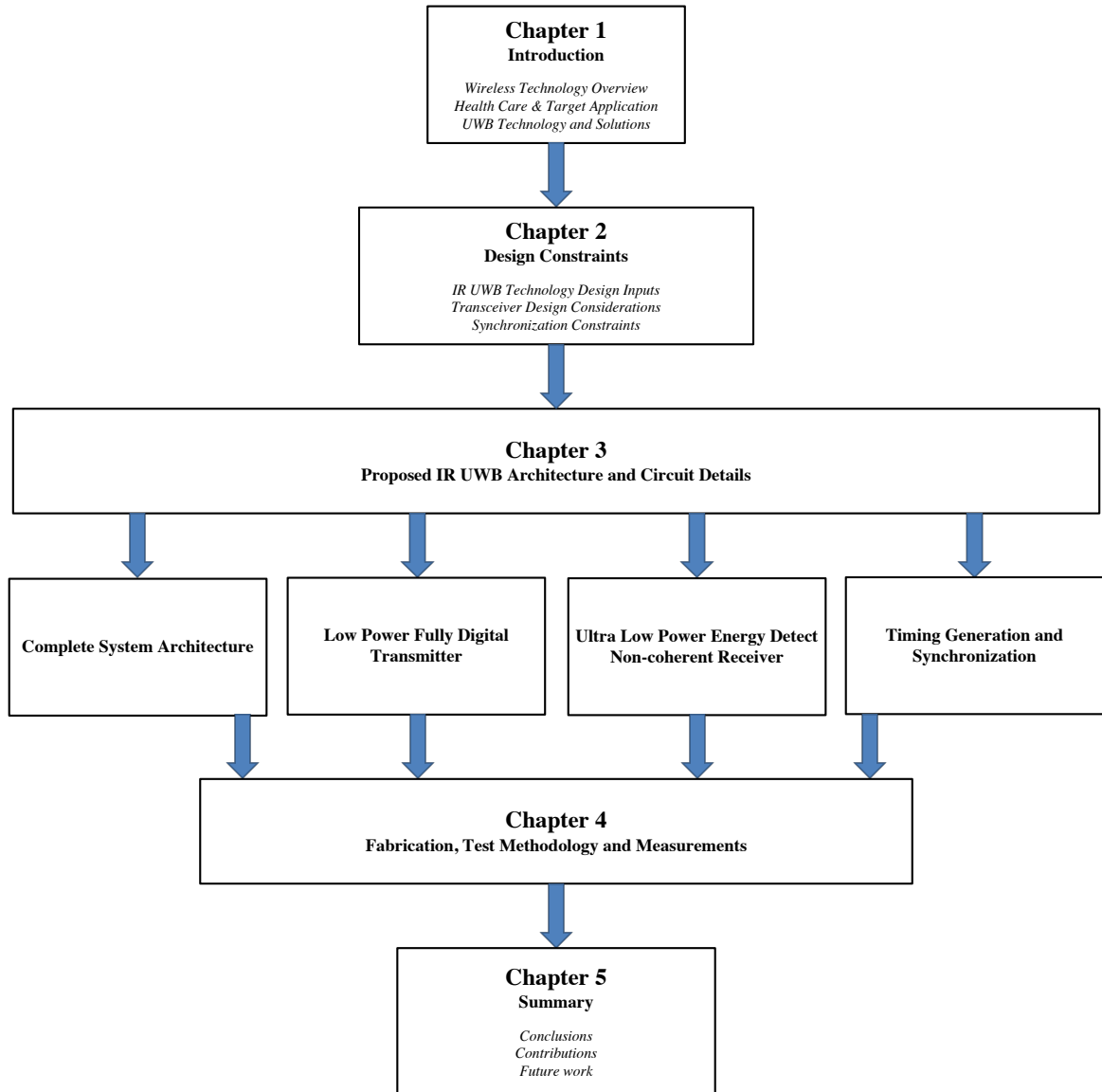


Figure 1.15: Thesis organization

1.4 Organization

This work is organized as follows in Fig. 1.15.

Chapter 1 discusses the background and the motivation for this work. The development of wireless technology has seen a big surge in recent times. Recent developments in personal area networks, IC technology, DSP processing and bio-medical devices have enabled the integration of short range communication into low cost personal health care solutions. Technology has enabled remote patient care. This work aims at developing a low power radio solution for BAN therapeutic and monitoring health care products. Different wireless standards are considered, narrowband and UWB compared and contrasted. UWB emerges as a possible solution to the ultra low power, low range, low-to-mid data rate gap on the wireless technology spectrum.

Chapter 2 talks about the design constraints involved in completing a UWB system architecture. The first issue that will be addressed in the modulation schemes available and what the system designed system hardware is capable of. A complete link analysis is also presented. This chapter also describes other transceiver design optimizations and decisions made to narrow down circuit blocks to be used in this design. Timing constraints are also described in this chapter.

Chapter 3 presents a combined transceiver to support a wide bandwidth range maintaining an extremely low power consumption. The design has been taped out in IBM 130nm CMOS process. This chapter is divided into two major sections. The architecture and circuit details of a fully digital carrier less transmitter and an energy detect carrier-less non-coherent early-late receiver are presented. A fully digital carrier less transmitter consisting of a pulse generator (PG) is proposed. A differential implementation of inverter type transmitter architecture is described in Section 3.3. An early-late

energy detect non-coherent IR UWB receiver architecture and the circuit implementation of the RF frontend and backend is described in Section 3.4. Section 3.5 describes the architecture and the baseband circuit techniques used to complete synchronization. The physical layer protocol and the synchronization algorithm used in this work is presented in Appendix A.

Chapter 4 discusses testing and measurement results followed by conclusions. Measurements are presented for various blocks in the proposed system. System measurements are also discussed. The antenna design, simulations and measurements are illustrated in Appendix B.

Chapter 2

Technology and Design Constraints

2.1 Introduction

This chapter gives an overview of the design constraints for the IR UWB system. The first issue addressed is the modulation schemes available and what the designed system hardware is capable of. Different channel models are discussed and the link budget analysis is also presented. The use-condition for the system is majorly transmitter on-body near head and the receiver is on the wrist. This chapter also describes other transceiver design optimizations and decisions made to narrow down circuit blocks to be used in this design. Timing constraints are also described in this chapter.

As described in Chapter 1, the advantages of carrierless noncoherent IR UWB system can be summarized into the following,

1. Data communication speed higher than the conventional narrowband systems in the body area network

2. Simple system architecture
3. Extremely low power dissipation because of elimination complex and power hungry mixers and frequency synthesizers. The output power is extremely low, and hence the need of a power amplifier can be eliminated. Power amplifiers are output drivers consuming large power
4. Higher immunity to interference because of being extremely wideband in frequency
5. Exploit the benefit of being extremely short in time which gives the system immunity from multipath fading, highly advantageous for indoor communications

We have looked at the different UWB system classification in Chapter 1. This chapter describes other transceiver design optimizations. With the timing accuracy associated with the IR UWB system, timing constraints become highly critical.

2.2 Modulation

Transceiver parameters like data rate and complexity are directly related to the modulation scheme used by the system. Because of UWB standard being shared unlicensed, it needs to comply well within limits as it shares its band-space with licensed and dedicated unlicensed standards. The spectral occupation of the system is highly dependent on the modulation scheme in-use. It becomes critical to discuss different modulation schemes. Power consumption and complexity of the system are a few more concerns that directly or indirectly are affected by the modulation scheme used.

There are several modulation schemes for UWB-IR communication systems, majorly categorized by either amplitude, phase, time of arrival or frequency. The common modulation schemes include pulse amplitude modulation (PAM), on-off keying (OOK),

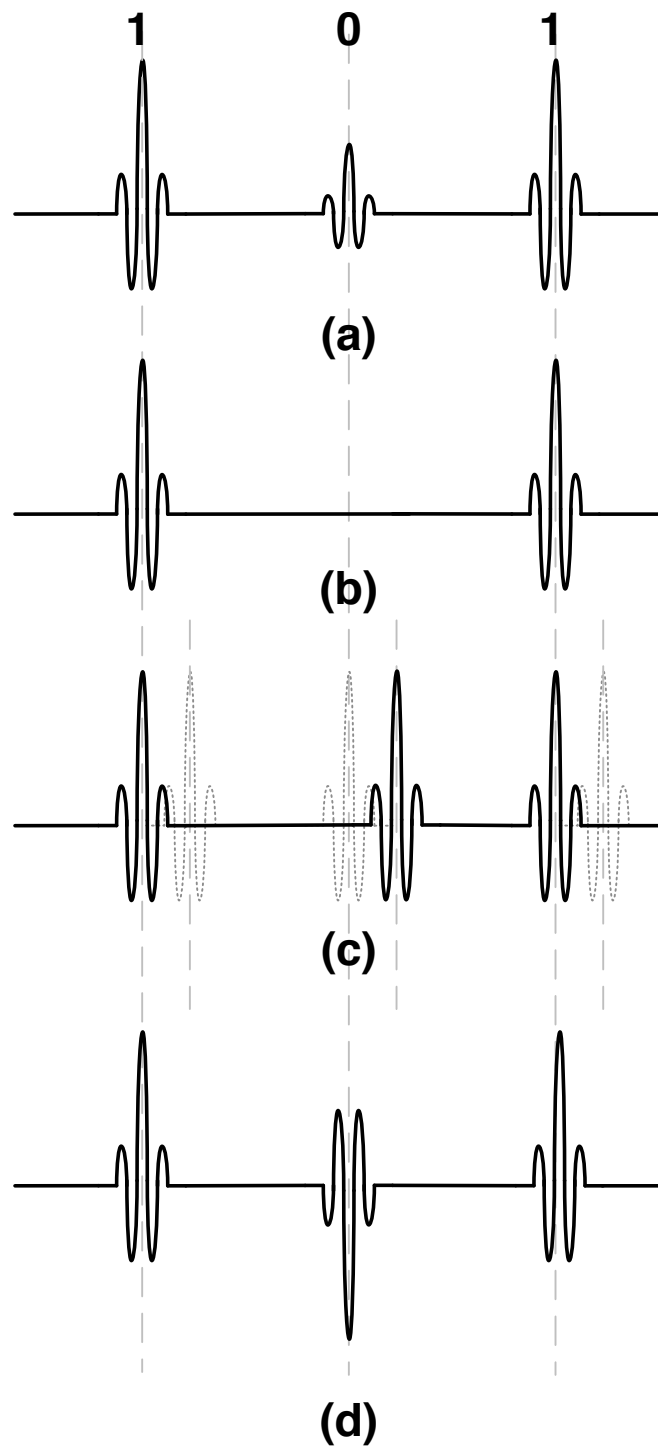


Figure 2.1: UWB Modulation - (a) PAM, (b) OOK, (c) PPM, (d) BPSK

pulse position modulation (PPM), binary phase shift keying (BPSK) and pulse shape modulation (PSM) as shown in Fig. 2.1.

PAM uses the amplitude level of the impulse to contain the data. OOK is a type of PAM, where the two discrete levels of amplitude are either 0 or full scale.

PPM uses slight differences in time of arrival to conclude a digital 0 or a 1. For instance, a digital 1 can be an impulse at occurrence of the baseband data, however a digital 0 can be expressed as an impulse a delay of δ from the occurrence in baseband. This modulation scheme is shown in Fig. 2.1 (c). For an IR UWB, to avoid inter-pulse interference, the time between pulse positions should be greater than the delay spread of the channel.

For the fixed time of arrival, the phase of the impulse can also be modulated to represent data. A two step representation would be BPSK, where an opposite phase is used to express the digital 0 and 1. A four step representation would be called a Quadrature PSK (QPSK). The phases used would be 0, 90, 180 and 270 degrees.

Slight tweaks in frequency can also be used to represent data. PSM would do something very similar to this. [40] uses orthogonal pulse shapes of very similar pulse width to do PSM.

These modulations are expandable, as described in phase modulation. These can also be used together to have a more complex modulation scheme. The design presented in this work is capable to modulate OOK and PPM. Analysis was performed between OOK and PPM schemes. The parameters considered were design considerations, power consumption, BER and output spectrum. OOK is an amplitude modulation shift keying and hence needs output decision comparators, comparing the signal with a reference. Assuming that for a DC offset, the 0 bit gives out a voltage V_1 following receiver detection and the bit 1 gives out a voltage V_2 , a threshold voltage of V_{ref} between V_1

and V_2 would be required to make a decision of whether a 0 or 1 was detected. Hence for OOK, a reference voltage V_{ref} will need to be generated in the design. On the other hand, for PPM there is no need to generate a voltage V_{ref} since the PPM signals are the same in amplitude but different in time of arrival. Instead, the voltage outputs for two time slots are compared for each data point measurement. How the voltages are generated in either scenario would be described later in this work.

In modern wireless applications, energy budget is often one of the biggest concerns. The PPM transmitter transmits one pulse per bit while the OOK transmitter transmits, on average, one-half pulse per bit. Thus, given the same energy consumption of the transmitter for both OOK and PPM, the radiated power (or energy) per pulse for OOK is two times that for PPM, assuming the hardware implementations are identical for both OOK and PPM. In other words, $E_{\text{p;OOK}} = 2E_{\text{p;PPM}}$. Similarly, the PPM receiver operates twice as often as the OOK receiver. For a given receiver energy consumption per bit, the power consumption allowed for the PPM is therefore only half that of the OOK receiver.

As will be described later in this work, the design presented is capable of modulating both OOK and PPM. The results published here have used OOK modulation scheme due to an easier synchronization protocol. The design is capable of comparing the detected signals to a generated threshold and well comparing signals spread in time. This also gives an opportunity to implement time hopping. Time hopping is minimal pulse position scrambling in time. Although time hopping will increase the synchronization time it helps prevent collisions with multiple IR running at the same pulse rate. It also prevents slaves bonding to a wrong master and helps the transmitter to meet FCC mask better by making it less spiky. The continuous impulse train would have spikes in the spectrum repeating at the pulse repetition frequency. In summary, time hopping signal

codes provide channelization and also suppresses undesirable spikes in the spectrum by randomizing the impulse positions in time. The time hopping code allows for multiple user access along with enhancing the security of the UWB-IR link.

2.3 Link Analysis and Channel Model

The Federal Communication Commission (FCC) specifies the spectral mask for UWB systems in terms of the effective isotropic radiated power (EIRP). EIRP is the total power radiated by an isotropic antenna that would be needed to produce a peak power density observed in the direction of the maximum antenna gain. The EIRP limit is specified in dBm/MHz and are shown in Fig. 2.2. The peak power level of emission - 0dBm in a 50MHz bandwidth is also specified. The maximum transmitter output power is determined by a combination of EIRP and peak power restrictions.

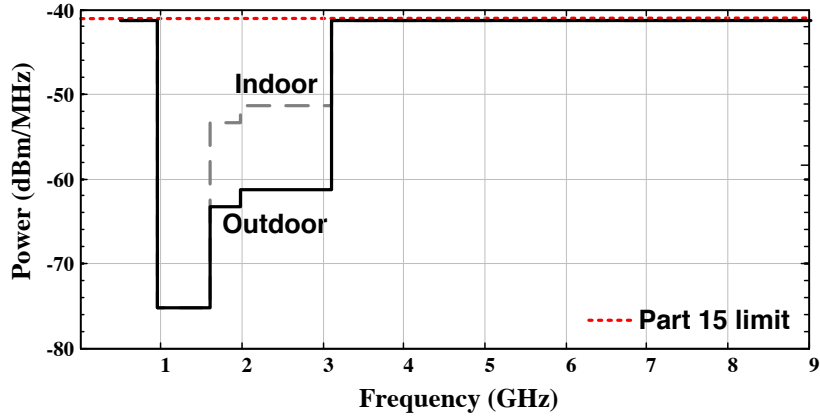


Figure 2.2: FCC power density restrictions on UWB

The maximum allowed total power for the entire bandwidth from 3.1GHz to 10.6GHz is calculated in Eqn. (2.1).

$$P_{max} = 10 \log_{10} \left(\int_{(3.1)10^3}^{(10.6)10^3} 10^{-41.3/10} df \right) \cong -2.55 \text{ dBm} \cong 0.56 \text{ mW} \quad (2.1)$$

For a bandwidth of 7500 MHz the total allowed power is 0.56 mW, hence for a bandwidth of 1000 MHz, the maximum allowed total power is $0.56 \text{ mW} / 7.5 = 74.66 \text{ uW}$ or -11.3 dBm.

Link budget analysis was performed to better understand the system requirements. The link budget will provide a measure of the ratio of the signal at the receiver to the signal required to achieve reception with specified performance, and therefore the robustness of the communication link.

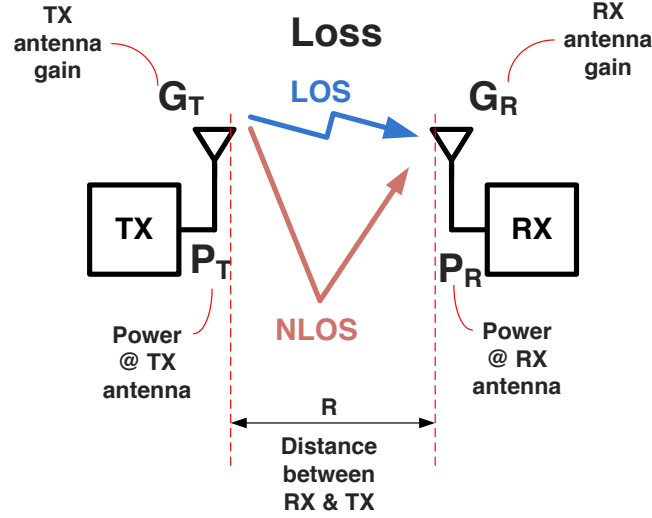


Figure 2.3: Path loss models for LOS and NLOS

Path loss is the reduction in power as the transmitted signal propagates through space. According to Friiss transmission equation, the received power can be expressed in terms of frequency of the signal and distance as

$$P_R = \frac{P_T G_T G_R c^2}{(4\pi R f)^2} \quad (2.2a)$$

$$P_{RdB} = P_{TdB} + G_{TdB} + G_{RdB} - 20\log R - 46.42dB \quad (2.2b)$$

Here,

P_R is the received signal power at the receiver antenna

P_T is the signal power at the output of the transmitter antenna

G_T and G_R are antenna gains for transmitter and receiver respectively

c is the speed of light

f is the frequency of the signal of interest

R is the physical spacing between the transmit and receive antennas

46.42dB is obtained by using 5GHz as frequency

The propagation path loss has two dependencies - frequency and distance. It can be seen from the Friis transmission equation that the the path loss is

$$L = \frac{(4\pi f)^2}{c^2} R^2 \quad (2.3a)$$

$$L_{R;dB} = L_{R0;dB} + 20\log\left(\frac{R}{R0}\right) \quad (2.3b)$$

L is the path loss

$R0$ is reference distance

n is the path loss exponent whose value is 2 for propagation in free space

Note that this does not consider the effect of the antenna aperture

The antenna aperture is described by the formula

$$A = G \frac{\lambda^2}{4\pi} \quad (2.4)$$

A is the antenna aperture

G is the antenna gain

λ is the wavelength of the RF signal

The path loss as defined by the equations above are meant for narrowband radios communicating in free space. The channel parameters greatly depend on environment, distance, antenna efficiency and frequency. The large bandwidth of the UWB channels gives rise to new effects compared to the traditional narrowband channels. For example, only few multipath components overlap within each resolvable delay bin, so the central limit theorem is no longer applicable and the amplitude fading statistics are no longer Rayleigh [41]. A lognormal distribution is superior. Body area networks exhibit unique radio propagation characteristics. The diffraction around the human body and the absorption by the human body are the main source of variations along with multiple reflections from the indoor surfaces. A non coherent IR UWB with a duty cycled energy detect receiver would be immune to reflections outside the time bin used for detection. Channels are distinguished as line-of-sight, in which there is an unobstructed path from the transmitter to the receiver and non-line-of-sight.

In the 2-6 GHz range, the human body obstruct the EM field and no energy penetrate through the body. The transmitted pulses diffract around the body . Thus, distances between the transmitter and receiver in the path loss model should be the distance along the body rather being a straight line. Many different channel models and respective parameters are proposed in literature [41–46]. For the purpose of this work, a channel model for around-the-head body area network is required. [45] presents model parameters for transmitter on the head and the receiver on the wrist. A summary of path loss evaluations are shown in Table 2.1. Using the line of sight(LOS) Friis Eqn. (2.2), the path loss at a distance of 3m is 55.96dB. Using the model described in

[45], the path loss exponent for transmitter on the head and receiver on wrist application is 1.78. From other models, an educated guess for the L_{R0} can be made, -36.4dB . Using these numbers, the path loss obtained at a distance of 3m is 44.9dB .

Table 2.1: Channel model parameters

Channel model	Path loss(dB), L_{R0}	Path loss exponent, n
Friis FSPL	-46.42	2
Indoor residential LOS [43]	-43.9	1.79
Indoor residential NOS [43]	-48.7	3.51
Indoor office LOS [43]	-35.4	1.63
Indoor office NLOS [43]	-57.9	3.07
Kanan et. al. LOS [43]	-36.6	1.8
Around-the-head model [45]	-42	1.78
Reference distance = 1m		
Reference frequency = 5GHz		

Table 2.2: Link budget analysis

Thermal noise floor		
Boltzman constant k	$1.38\text{e}-23$	J/K
Temperature T	300	K
Thermal noise N_0	-174	dBm/Hz
Center frequency f_c	5	GHz
Bandwidth B	1000	MHz
Noise floor	-84	dBm
Transmitter power		
Power spectral density	-41.3	dBm/MHz
Spectral efficiency	50	%
Transmit power	-14.3	dBm
Bit rate	1	Mb/s
Transmitted energy/bit	36.2	pJ

Using a spectral efficiency of 50% and the signal bandwidth of 1000MHz, the transmitter power output evaluates to -14.3dBm . Considering antenna gains for 3dB, and the above calculated path loss, the received power is -64.2dB for the free space path

Table 2.3: Channel model based path loss computations

Channel parameters				
	Channel model			
	FSPL LOS	Indoor residential LOS	NLOS	Around-the-ear TX - head; RX - wrist
Path loss @ 1m (dB)	46.4	43.9	48.7	42
Path loss exponent	2	1.79	3.51	1.78
Path length (m)	3	3	3	3
Additional path loss (dB)	9.5	8.5	16.7	8.5
Antenna gain (dB)	3	3	3	3
Received power (dB)	-64.3	-60.75	-70.7	-58.8
Data rate is 1Mb/s				
TX out is -14.3dBm @ 50% spectral efficiency				

loss(FSPL) and -56.2dB for the around-the-head model. These calculations demonstrate that for the target use condition, the sensitivity of the receiver does not require to be extremely low. For a sensitivity of -70dBm (as measured in Chapter. 4, the link budget is higher than 13dB at a 3m communication distance for the around-the-head model. This illustrates conclusively the robustness of the transceiver link.

2.4 Band Selection

For the single band operation as discussed in Chapter 1, the UWB spectrum is divided between two bands. A low band of $3\text{-}5\text{GHz}$ and high band of $6\text{-}10\text{GHz}$. The spectrum from $5\text{-}6\text{GHz}$ has a major interference from WiFi in U-NII band. Fig. 1.13 illustrates the different channels and bands available for UWB in the 80.15.4 and 802.15.6 standards. This design focuses on the low band. The lower band has steeper sideband requirements. The target spectrum discussed above in Fig. 2.2 and the emission power limits force the transmit frequency spectrum to at least be 30 dB lower on the side-bands when using the lower band. However, as we go to the high band, the power consumption on the

transceiver increases. As a compromise to have lower power consumption, yet operate in the UWB standard, the low band is chosen.

2.5 The UWB Pulse

Various pulse shapes have been suggested in literature to optimally fill the UWB spectrum in both the IC as well as the communications fields of research. The Gaussian pulse is the most common pulse shape used in conventional UWB systems since the time and frequency properties of a Gaussian pulse are highly desirable. The standard constraints are expressed in terms of frequency and power content per unit of frequency. However, we are looking for a time domain solution. Every signal has properties in time domain and frequency domain can be related by the Fourier principle as mentioned in Eq. (2.5) based on the observation that - *All oscillations/signals can be understood as consisting of nothing but sinusoidal signals of differing frequency and amplitude.*

$$G(f) = \int_{-\infty}^{\infty} g(t)e^{-i2\pi ft} dt \quad (2.5)$$

As a progressive intuitive understanding, let's look at Fourier pairs in Fig. 2.4. The first signal in Fig. 2.4 (a) is a sinusoid. Looking at only single side band, the frequency representation of a sinusoid is a delta function. Consider the second signal on the time column, a rectangular pulse. The frequency response of a rectangular pulse is a Sinc function. Mathematically, a Sinc function is $\text{Sinc}x/x$. Although the major power content is in the main lobe, the side lobes also contain limited quantities and the difference in power between the main and the side lobes can be evaluated. In terms of power, the frequency spectral content would look like $20\log \frac{\text{Sinc}x}{x}$ implying that the first side lobe would be 13.26 dB below the main lobe. This suppression is still not enough to meet the FCC spectral mask requirements. The third signal on the time

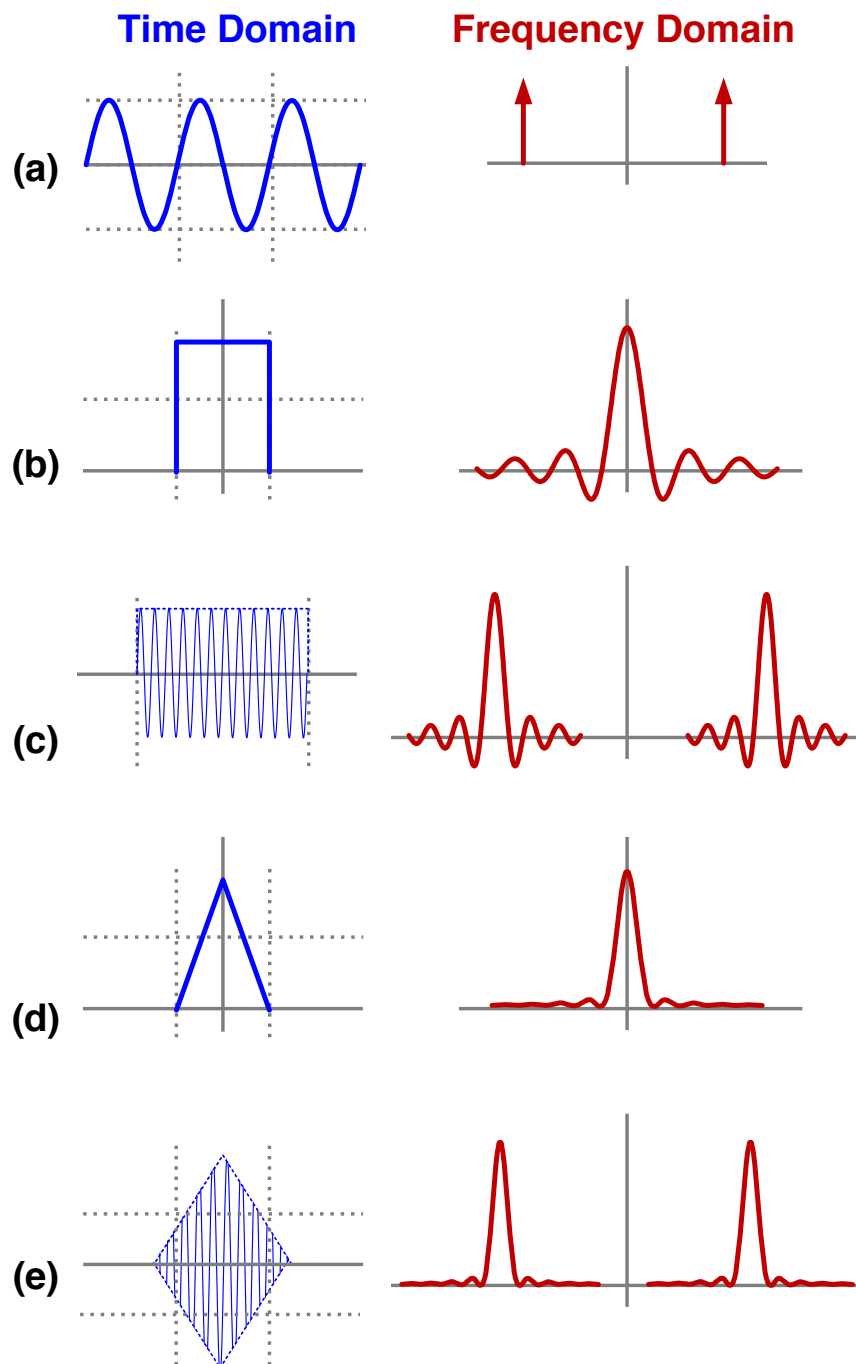


Figure 2.4: Fourier pairs

column is a multiplication of the sinusoid and the rectangular impulse. The resultant convolution on the frequency domain simply shifts the Sinc function to frequency of the sinusoid. Let's examine a triangular time domain pulse now. The frequency domain representation of this function is Sinc squared response, and the spectral power content can be simply evaluated as $40\log\frac{\text{Sinc}x}{x}$. The side lobe reduces to -26.5 dB which is very close to the required side lobe suppression of approximately 30 dB. Now, consider a Gaussian time domain impulse. The frequency response of Gaussian is a Gaussian. The resultant on the frequency spectrum does not contain any side lobes and an infinite side lobe suppression is obtained. However, the primary lobe of a Gaussian may not optimally fill the FCC and hence resulting in loss of possible transmittable energy. Some publications have tried to answer this by considering N^{th} order derivatives of a Gaussian pulse [47–49].

To have a more optimum UWB pulse design, this work used the FCC spectral restriction mask as the frequency response. Using the FCC spectral mask as the frequency response of the desired pulse shape will help in coming up the most optimum pulse that can efficiently use the spectrum, such that no usable power is wasted. Considering the mask as a DSB frequency response, we get Eq. (2.6)

Frequency

$$G(f) = \sum K_i * \text{rect}f_i \quad (2.6)$$

Time

$$g(t) = \sum K_i * \frac{\text{Sin}(2\pi f_i t)}{\pi\sqrt{f_i t}} \quad (2.7)$$

where,

K_i is the scaling coefficient obtained from the spectral power requirements

f_i is the frequency of the band of the interest

Eq. (2.6) uses the DSB of the FCC mask and comes up with rectangular functions

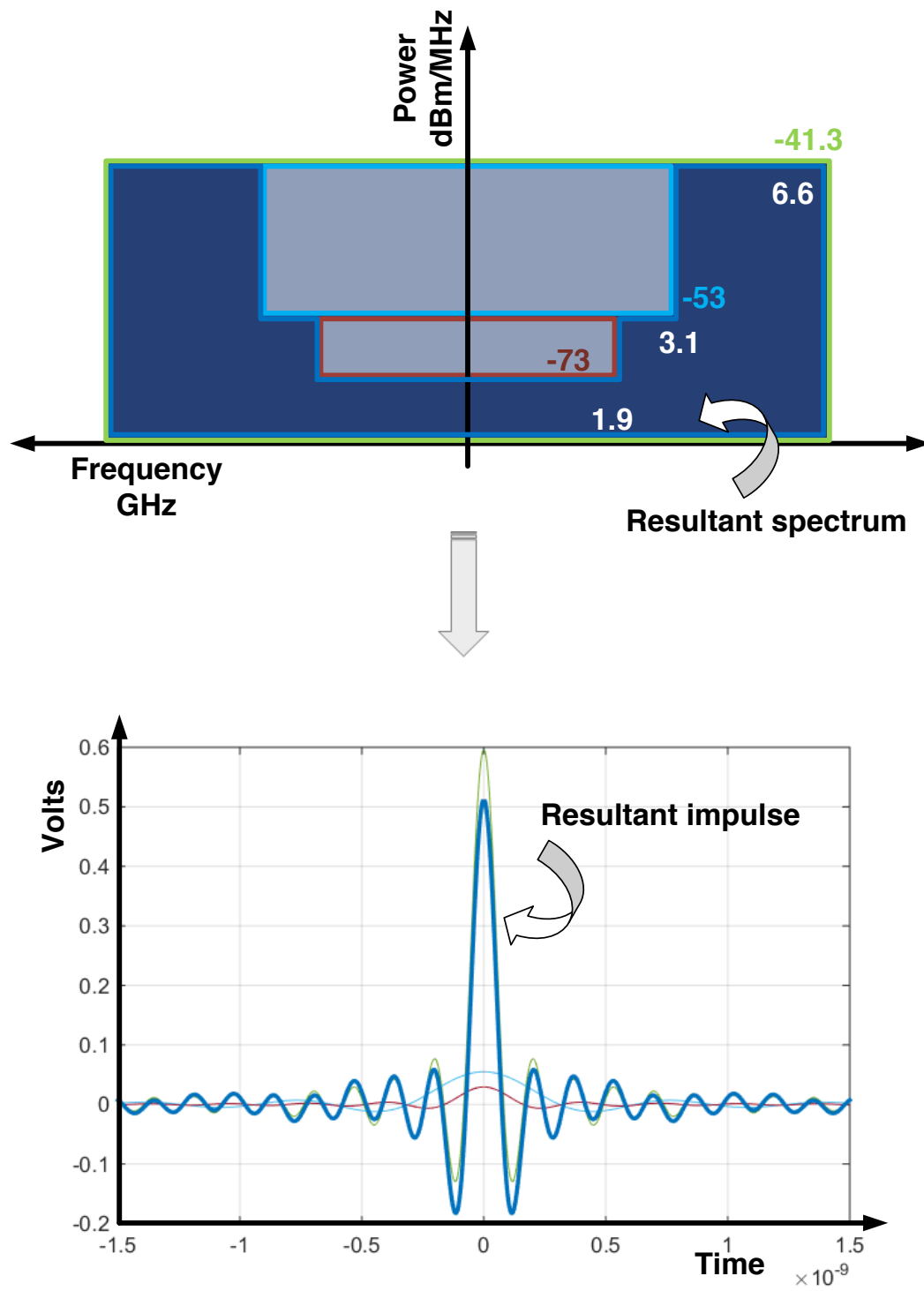


Figure 2.5: Optimum pulse design

with a power coefficient and a frequency. As shown in 2.5, the optimum pulse (dark blue) is obtained by subtracting the light blue and the red rectangles from the green rectangle function.

Evidently, the spectral properties of the UWB modulation along with the power consumption and design complexity are affected by pulse shaping. [50] synthesizes an optimal UWB pulse using digital FIR filters. However, with the targets of low power and low complexity, this synthesis would probably not be the right way forward. Many topologies make use of a Gaussian pulse and its derivatives [47–49], or more complex shapes as Hermite pulse [51], Bessel pulse [52] and Prolate Spheroidal Functions. These shapes although very lucrative, cost a lot in design complexity and are difficult to generate. Analog techniques have been used to generate impulses both at baseband and directly at the frequency of interest [53]. These designs take up a lot of area because of the presence of an inductor either to generate, up-convert or filter the impulses to be FCC compliant.

A more elegant and optimum way of generating the impulses would be digitally [54, 55]. This work presents an all digital IR UWB transmitter which is optimized of area, power and compliance.

2.6 Transmitter Design Constraints

Pulse based transmitters can be grouped in two major categories as mentioned in the Chapter 1 -

1. Carrier based, that generate the impulse at baseband which needs to be upconverter using a carrier generated using a frequency synthesizer, like a local oscillator
2. Carrier less, that generates the impulses directly at the frequency of interest and

do not need power hungry frequency synthesizers to generate carrier signals

The carrier based up-conversion has more frequency control, however at the cost of power and area. This is because the frequency synthesizers need to be operating at the high frequency.

The UWB-IR transmitter generates impulses, optimally like the waveform we just evaluated. Earlier work use analog techniques generating FCC compliant pulse. An impulse is obtained by momentary excitation of an LC tank and it's subsequent ringing [53]. Because of the inductor, this is a narrow band impulse generation technique. The damping in the ringing gives the impulse a wideband nature. A high order filter is required to follow for the generated impulse to be FCC compliant. The presence of an inductor in the tank causes area concerns. With silicon becoming an expensive real estate, a best design practice is to optimize area. A similar negative effect on area is due to the presence of a high order band pass filter for generating the RF impulse.

A digital approach will lead in eliminating this effect and optimize area. Previous work have also implemented digital transmitters for ultrawideband radios. This work presents a fully programmable modular transmitter that generates RF impulses using linear approximation of the desired FCC compliant pulse. The digital transmitter is pulse shaping pulse generator.

2.7 Receiver Design Constraints

Looking at the different UWB systems, this work narrowed down it's focus to a carrier-less receiver. For a carrier-less receiver, a coherent version of the system using the DSSS still uses complex design blocks including a mixer. To eliminate these, this work emphasizes a non-coherent design. A non-coherent IR UWB serves architecturally as the simplest receiver system involving generally only an input amplifier followed by an

envelope detector on the frontend and a decision making comparator on the backend. The energy levels of the UWB signals to be detected however are extremely small which restricts the input amplifier to have very high gain over a very large bandwidth. The design should also have a large dynamic range to accommodate any narrowband interferer that can saturate or probably harm the components.

The receiver needs to be wideband and capable of sensing low energy RF impulses. A super regenerative amplifier provides for high gains in the proposed receiver. Because of the extreme duty cycling, there is enough time for the receiver to make a decision before the next impulse comes in. This feature is utilized by using a super regenerative amplifier (SRA). The SRA is essentially an oscillator on the verge of starting up. The SRA consists of a cross-coupled NMOS pair, a de-Q'ed inductor tank, and a tank-shortening squelch switch. A small amount of input energy can start the oscillator and essentially provide a gain of ∞ if given enough time to settle. The bandwidth is increased by de-Q'ing the tank by adding a resistive element to the tank. This answers the constraint of achieving high gain on the input amplifier. A common gate low noise amplifier preceded the SRA.

Another constraint is the timing. IR UWB has a high resolution in time. The signals to be detected can be as short as a nanosecond, even shorter for larger bandwidths. The receiver needs to have a fast sleep to start time, so that power can be optimized and the receiver is active for the least time possible. Critical timing generation blocks allow the receiver sleep time and optimize power.

2.8 Timing Constraints

Traditional narrowband architectures, where the transmitted baseband data is riding on a carrier frequency and receiver demodulates the signal by down-converting the receiver signal to baseband, require frequency synthesizers to generate continuous wave carrier

signals which are used in mixer. The detection is only as good as the frequency synchronization between the transmitter carrier frequency and received carrier frequency. The synchronization is achieved by some control on the frequency generation in the synthesizer. Oscillators are generally used to generate these continuous wave carrier signals. As in Fig. 2.6, the local oscillator generates the frequency as an input to the down-converting mixer. A synchronization is required between the carrier frequency of the received signal at the antenna and the receiver frequency generated by the local oscillator.

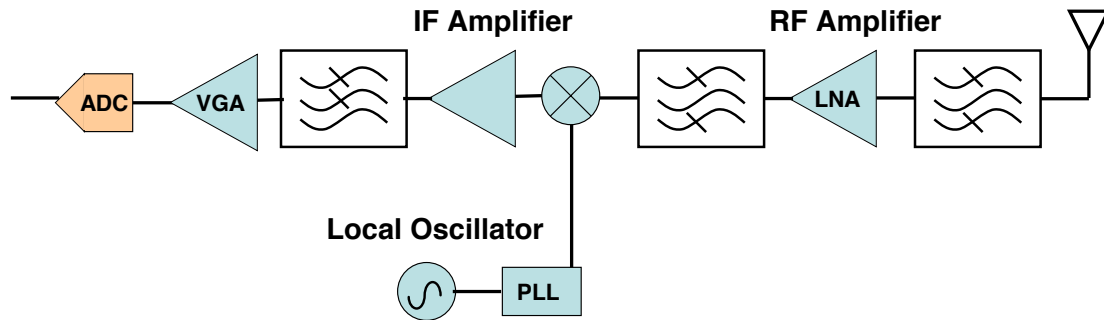


Figure 2.6: Traditional heterodyne architecture

Unlike these traditional heterodyne architectures, the IR UWB, as the name implies, is sending or receiving data as a time domain pulse. As compared to the traditional architectures IR tries to be precise in time rather than frequency. The inherent timing accuracy associated with IR UWB is extremely high - nanoseconds. The impulses received are based on time of arrival. Due to the high time resolution, the timing constraints associated with IR systems are extremely accurate and hence synchronization in time becomes a critical issue driving IR transceivers. IR UWB radios are extremely optimized in power consumption because the duration for which the receiver needs to ON is minimal i.e. only during receiving an impulse. The impulse can be very short in time, however the rate at which this impulse is received, the data rate has a wide

range. For a lower data rate, the IR UWB system will be able to be duty cycled to larger extent, hence saving more power. However, since the system is duty cycled, and the timing resolution is extremely high, the receiver needs to be synchronized to the time of arrival of the impulses and the high time resolution makes this task difficult and complex.

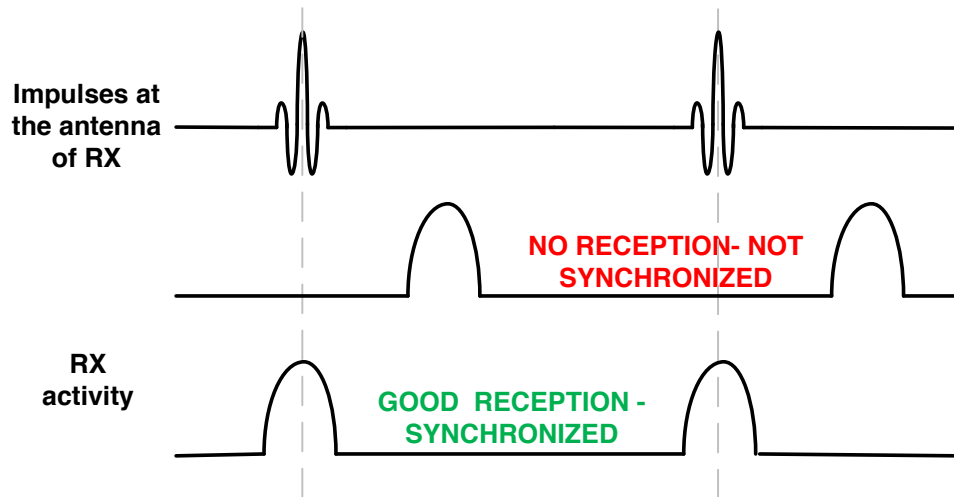


Figure 2.7: Time synchronization in IR UWB

A mismatch in timing can be caused either by a phase inaccuracy or a frequency inaccuracy as shown in Fig. 2.8. A phase mismatch may be a result of start-up offset between 2 radios, or movement of the radios causing the impulses to reach at different times and hence different phases of the system clock. A mismatch in frequency may be a result of crystal offsets. In spite of the timing constraints, the advantages of using an IR-UWB architecture determined using a non-coherent energy detection based carrier-less radio for addressing the target application of a universal hearing aid, where the hearing aid is also used to connect to consumer devices.

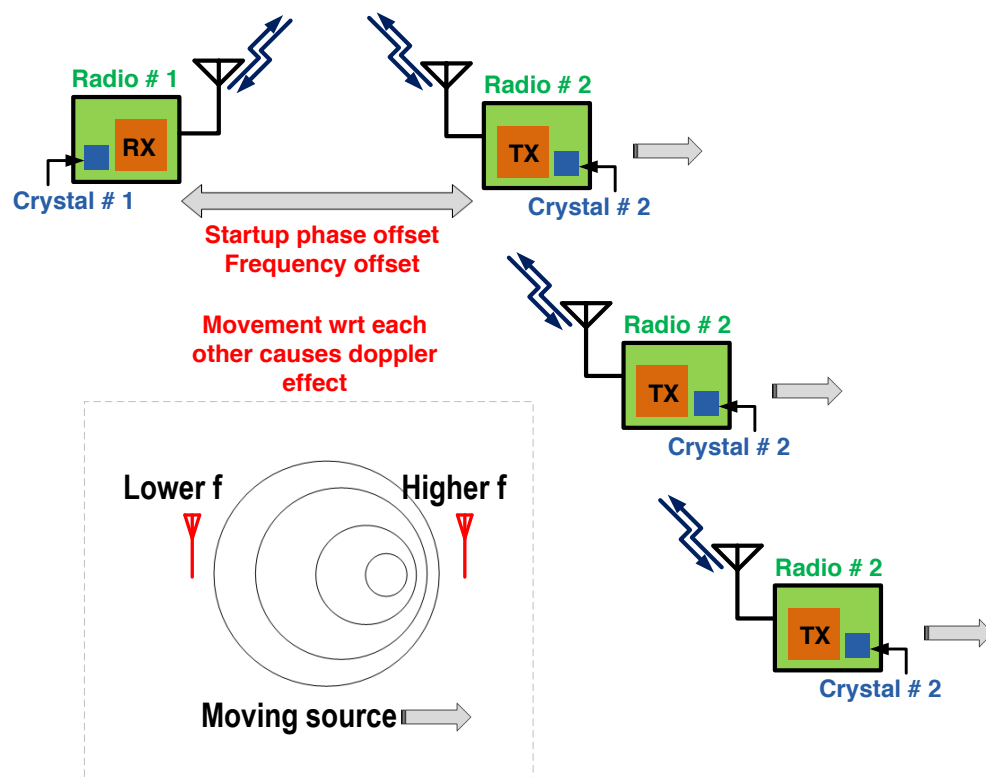


Figure 2.8: Sources of offsets between two radios

2.9 Antenna Design Constraints

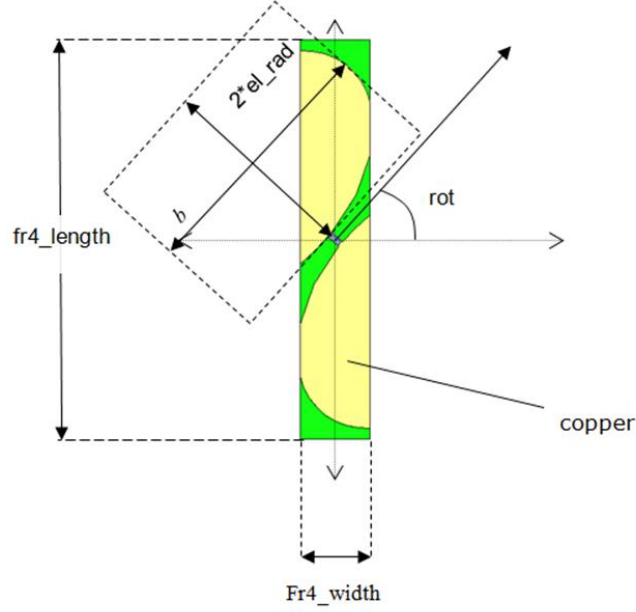


Figure 2.9: Antenna design parameters

Owing to the product size constraints, the antenna needs to be small with an isotropic RF field. Different antennas were looked at, and a differential bowtie antenna configuration was chosen. The reason for choosing this design is that the bowtie has a wider bandwidth for its small form factor. HFSS simulations were performed with a head model to optimize the design.

The elliptical dipole antenna is illustrated in Fig. 2.9. The primary design parameters that affect impedance and gain include b , el_rad , and rot . A dipole antenna structure was chosen for its omnidirectional pattern. The elliptical shape provides a wide impedance bandwidth. While a full ellipse provides a wideband input impedance, the antenna gain suffers as the S_{11} is too high. A full ellipse would have a larger footprint.

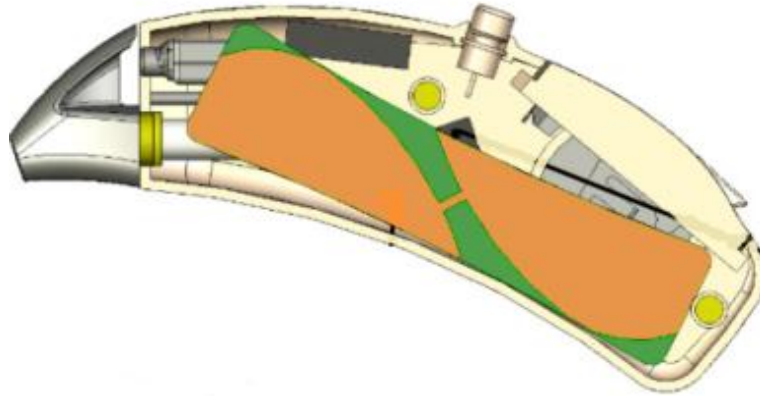


Figure 2.10: Antenna placement in the hearing aid

Refer to Appendix B for more details and measurement results.

2.10 Summary

This chapter gives an overview of the design constraints for the IR UWB system. The first issue addressed is the modulation schemes available and what the system designed system hardware is capable of. An OOK scheme has lesser energy dissipation per bit and since power consumption is one of the major design parameters OOK is chosen. The design presented in this work is also capable of PPM. Different channel models are discussed in literature. For this work, an around-the-head model is chosen. The channel model is described and the link budget analysis is also presented. According to the modeling and the sensitivity measurements, the system appears to be robust and the use condition (transmitter near head, and receiver on wrist) has a good link margin of more than 10dB. This chapter also describes other transceiver design optimizations and decisions made to narrow down circuit blocks to be used in this design. Timing constraints are also described in this chapter.

Chapter 3

Proposed Architecture and Circuits

3.1 Introduction

This chapter presents a combined transceiver to support a wide bandwidth range maintaining an extremely low power consumption. The design has been taped out in IBM 130nm CMOS process. An optimized solution for receiver and transmitter is proposed. Timing circuits are shared between the transmitter and the receiver.

Chapter 1 and 2 discussed UWB as a possible solution to the ultra low power, low range, low-to-mid data rate technology solution. IR UWB is an efficient low power solution for the UWB technology standard. This chapter presents an optimum transmitter and receiver solution, and combines these to make an efficient IR UWB system.

3.2 System Architecture

The block diagram for the proposed IR UWB based transceiver is shown in Fig. 3.1.

The system is designed for a 100Ω differential antenna (description and measurements in Appendix B) and contains a pulse-generation based transmitter, a receiver supporting phase and frequency synchronization, a digital baseband, and a synchronization and tracking control block.

A DLL provides a PVT tolerant time step resolution of 1ns and regulates the pulse generator center frequency. The antenna is shared between transmit and receive. The transmit output is always connected because it is in high impedance state when not transmitting. A switch is used to connect the receiver to the antenna while receiving.

The die is packed in a QFN package efficiently re-utilizing the bondwire into band-pass filtering.

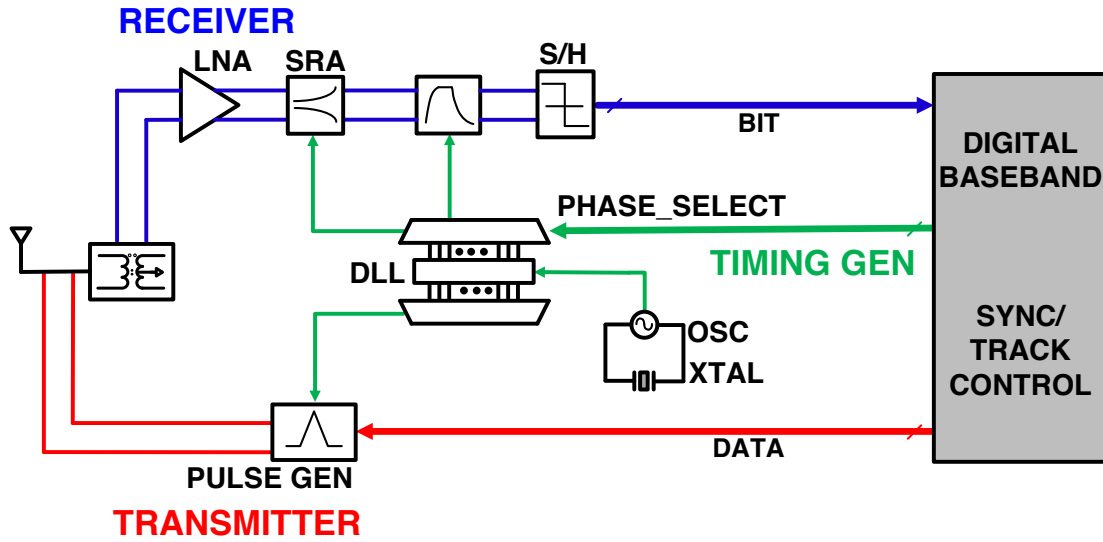


Figure 3.1: Noncoherent UWB-IR Transceiver Architecture

Transmitter

A fully digital carrier less transmitter consisting of a pulse generator (PG) is proposed. The PG implements a piece-wise linear approximation of the optimum FCC compliant

pulse shape by implementing an inverter type logic. A differential implementation is used to have more control of the output waveform. Section 3.3 describes detailed architecture and circuit implementation for the transmitter.

Receiver

A carrier based transceiver scheme requires mixers and frequency synthesizers to frequency translate the signals. Auto-correlation techniques for reception can eliminate the frequency synthesizers but the mixers remain. These increase the area and power consumption of the implementations. A carrierless UWB-IR scheme allows for transmission of data in bursts (energy impulses) giving the circuit adequate sleep time during transmissions, hence lowering the power consumption and increasing the battery life.

This chapter presents an energy detection based early-late receiver.

The receiver needs to be wideband and capable of sensing low energy RF impulses. A super regenerative amplifier provides for high gains in the proposed receiver. Section 3.4 describes detailed architecture and circuit implementation for the receiver.

3.3 Low Power Fully Digital Transmitter for IR UWB

3.3.1 Proposed Architecture

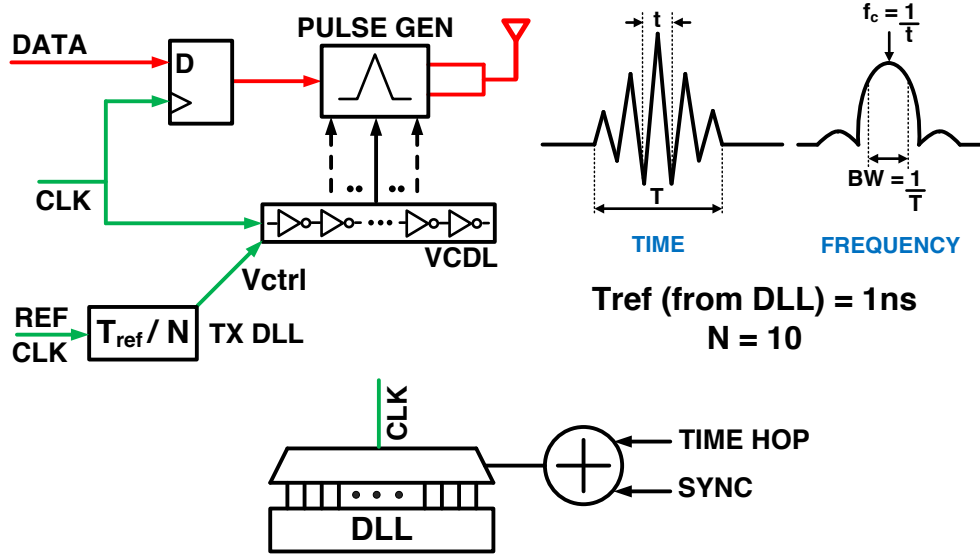


Figure 3.2: Transmitter block diagram

The transmitter architecture including a fully digital carrier less transmitter consisting of a pulse generator (PG) and PVT tolerant delay generation is proposed and is shown in Fig. 3.2. The transmitter clock is determined from a delay line, whose outputs are multiplexed based on the control signals - time hopping and synchronization.

The PG implements a piece-wise linear approximation of the an FCC [23] compliant pulse shape. A compliant and optimum pulse shape has been discussed in the Chap. 2. The programmable digital PG generates a pulse shape that is compliant with the FCC mask for 802.15 UWB communication between 3.1-10GHz.

The fully digital transmitter generates pulses that are FCC mask compliant, without the use of any on-chip filtering. In comparison to the analog technique and the up-conversion techniques, where use of an inductor becomes critical, this all digital design

save a lot of chip real estate by omitting the high-order on-chip bandpass filters or high-speed frequency synthesizers. Since the transmitter is completely digital, it also helps saving on power. The static power consumption that is common in analog techniques for biasing and circuit operation is almost non-existent in a digital inverter based circuit.

A T/R switch is used by transceivers to multiplex between the receiver and the transmitter. In order to avoid the transmit/receive (T/R) switch, the output is held in a high impedance state when not transmitting. While receiving, the transmitter is disconnected from the antenna and vice versa. However, because of the high impedance of the transmitter while not transmitting, the T/R switch can be eliminated.

The transmitter needs a matching network to go from the design's output to the antenna [6]. The use of the bondwires as part of the matching network helps decrease the area required for the transmitter and also provides for some band pass filtering. A couple of surface mount components are required on the hybrid outside to complete the matching network, however, they take up minimal space, and the contribution to the bill of materials (BOM) is exceptionally low.

Although the target impulse is optimum UWB pulse we calculated in Chapter 2, let's take a step back to understand a few parameters. For simplicity let's assume that the time for charge/discharge is fixed. In other words, every cycle inside the pulse envelope is split in time equally, by a parameter t . This parameter t determines the central frequency of spectral occupation of the impulse, $f_c = 1/t$. Another important parameter is the total time the pulse occupies in time and is represented by T . This parameter determines the bandwidth of the spectral occupation of the impulse, $BW = 1/T$. This makes sense intuitively, as the time duration of a pulse increases, the bandwidth of its frequency spectrum reduces. An infinite time signal is a delta function in frequency. This concept of a simple pulse is represented in Fig. 3.2.

The PG implements a piece-wise linear approximation of the an FCC compliant pulse shape by implementing an inverter type logic, sequentially spread out in time. Generating the time based parameters accurately, t and T are key in making sure that frequency content remains compliant. The vital piece of the transmit algorithm puzzle is the delay cell which guarantees the accurate generation of time delay over different conditions. The generation of this delay will be more elaborately addressed in the timing generation section of this chapter. Using the delay generated by a delay locked loop, the transmitter uses sequential drivers to charge and discharge the output.

3.3.2 Circuits

Pulse Generator

The pulse generator uses static digital CMOS logic elements limiting power consumption to pulse transitions. A piecewise linear approximation of the desired pulse is generated by clock timing (to switch between up and down directions) and driver weighting (to change the charging/discharging strength) as shown in Fig. 3.3. A differential implementation is used to have more control of the output waveform. Digital gates have been meticulously designed to switch the drivers ON and OFF depending upon activity.

The PG circuit gives two major controls

1. Amplitude control
2. Time control

The time control is obtained by using multiple sequential drivers with timed activity provided by a delay line which is used to generate glitches in time, which are propagated over the digital gates to switch the driver ON. A weighting scheme is applied to the drivers to obtain amplitude control. The design is highly modular and easily scalable to

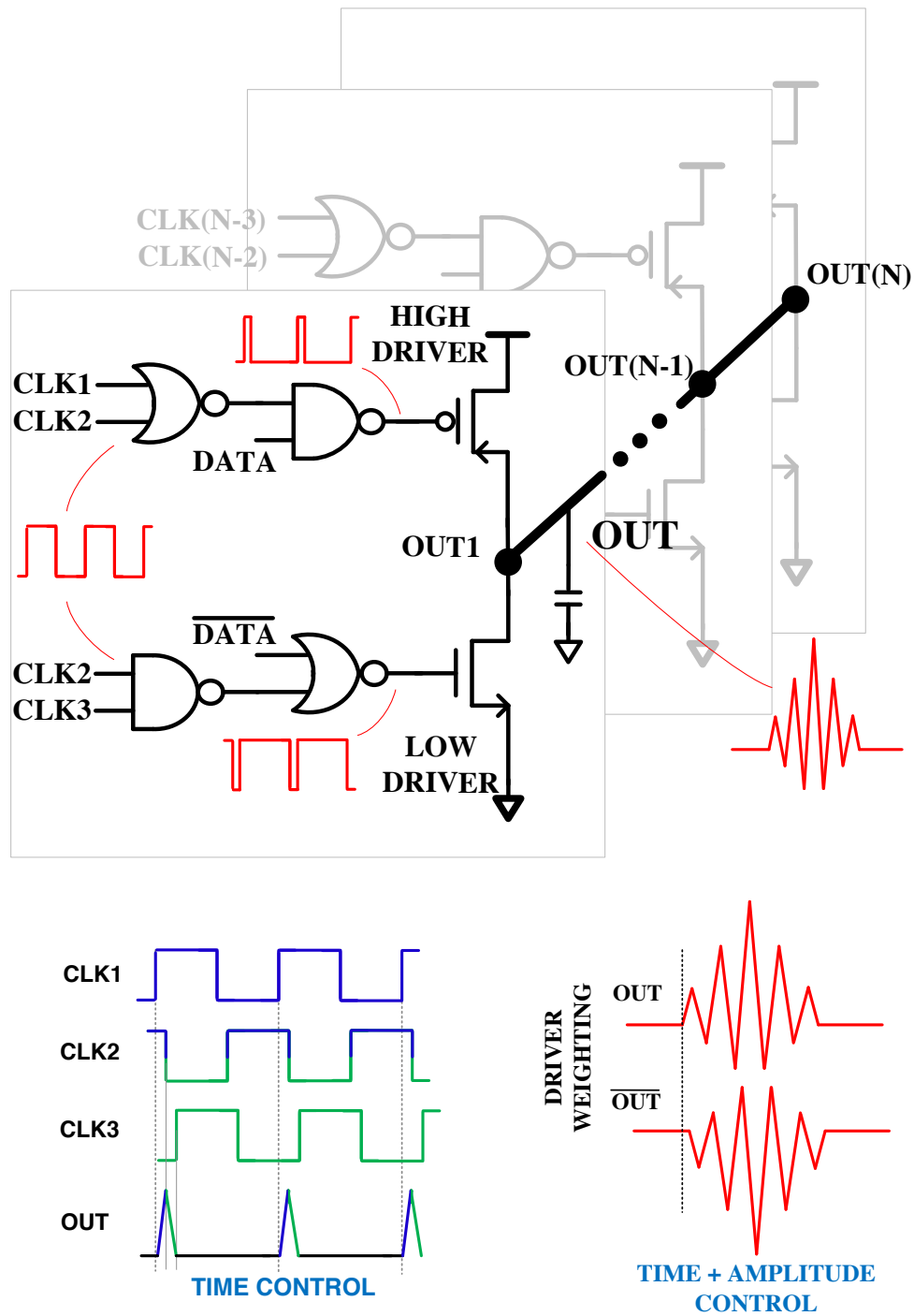


Figure 3.3: Pulse generator timing, schematic, and output waveform

other technologies. The transmitter has slight control on output power by controlling the power supply voltage. The pulse generated by this PG has large enough magnitude to avoid usage of any power amplifier to generate output. When transmitting, the PG is directly connected across the antenna, otherwise it is in high impedance mode and does not affect the receive performance.

While designing the PG, different digital methods were explored, some similar to prior art [54]. In [54], the authors use a stacked driver stage. This has the drawback of the design complexity involved in scaling the individual FETs in the driver and ensure that no one particular gate forms a bottle neck. We ensure that only one FET per driver is controlled by the timing generation and that any timing that needs to be generated is done with smaller digital gates preceding the single control driver. Using this approach, the design is more modular. The switching activity of larger capacitive nodes (from the driver FETs, which would to large so that they can drive the output) is reduced and charge sharing is avoided.

3.3.3 Summary

In this section we discussed the advantages of a digital transmitter. We evaluate the performance and efficiency of a fully digital pulse generator. The output can be placed in a high-impedance state, removing the need for a T/R switch during reception. Timing is generated from the DLL to accommodate PVT. The shape of the spectrum can be easily controlled by controlling the transmit pulse simply by sizing the devices. Delay cells are used and, using control signals from the timing generation block, will take into account the effect of process, voltage and temperature.

3.4 Ultra Low Power Energy Detect Receiver

3.4.1 Proposed Architecture

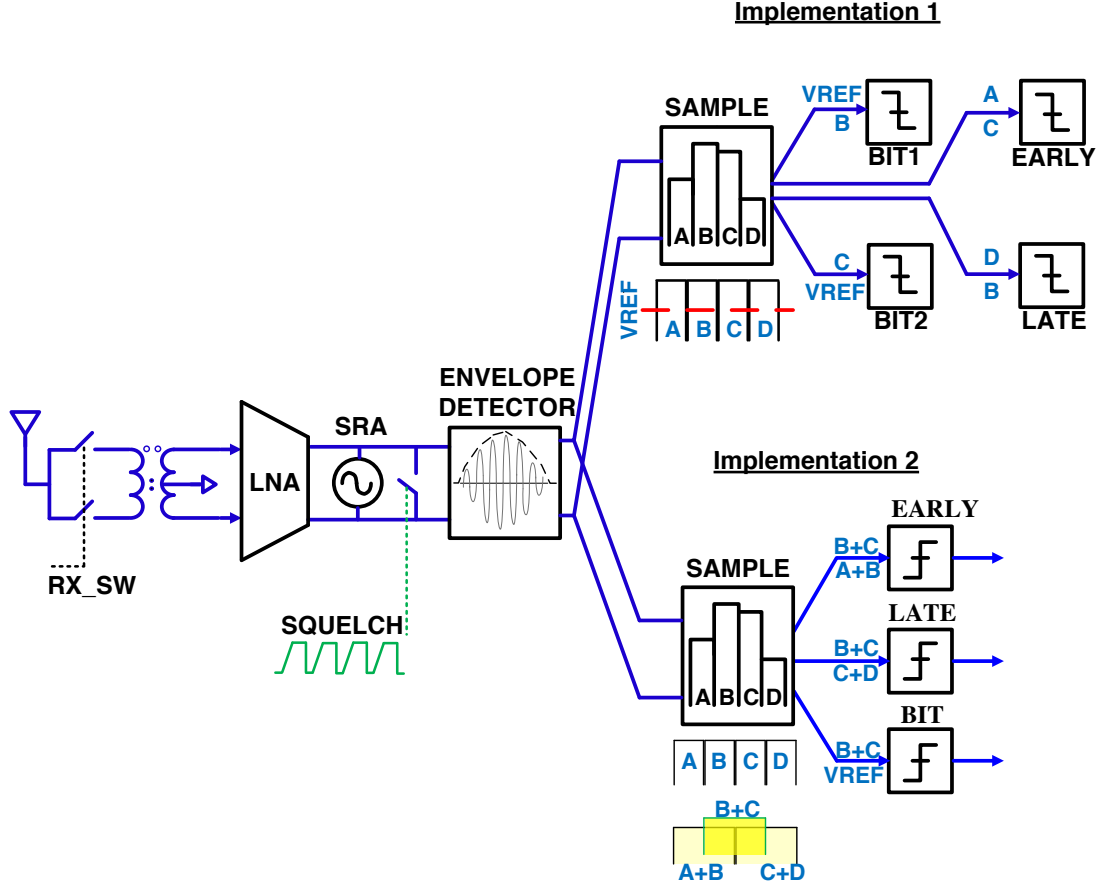


Figure 3.4: Receiver block diagram

The receiver has an on-chip transformer preceding the LNA, which is followed by a super-regenerative amplifier (SRA), envelope detector, sample-and-holds, and a bank of comparators as shown in Fig. 3.4.

The energy detection based receiver determines the presence of a pulse by the amount of energy captured within a specific period, which we call the pulse detection window

(PDW). The on-chip transformer is used for LNA input matching and filtering. The LNA amplifies the signal from the antenna, while presenting matched impedance to the input. The SRA provides an energy efficient way of signal detection. If a signal is present within the PDW, the SRA oscillates and the oscillation is detected by an envelope detector. A sample-and-hold allows the integration of the envelope detector's output within the PDW. Comparators then give digital outputs.

3.4.2 Circuits

On-chip Transformer

The receiver has an on-chip transformer preceding the LNA as shown in Fig. 3.5. The transformer provides a broadband impedance transform from the antenna (100Ω differential) to the LNA input (150Ω differential). It also helps in providing some basic bandpass filtering and provide minimal signal shaping. It isolates the LNA from the antenna to provide biasing to the input LNA. The transformer doubles up as the drain biasing inductors in the common gate LNA. DC biasing is provided through transformer inductance, while still allowing the RF input energy to ride on top of the DC bias. Since it isolates the receiver from the package, it reduces the bondwire inductance effects along with removing the parasitic capacitance of the pads and nodes that effect the receiver input stage.

The transformer is 5:4 turns ratio, with a match (S_{11}) between 4.5 - 5.5GHz of better than -11dB. The insertion loss is about 0.5dB at 5GHz. These values were simulated using ADS Momentum.

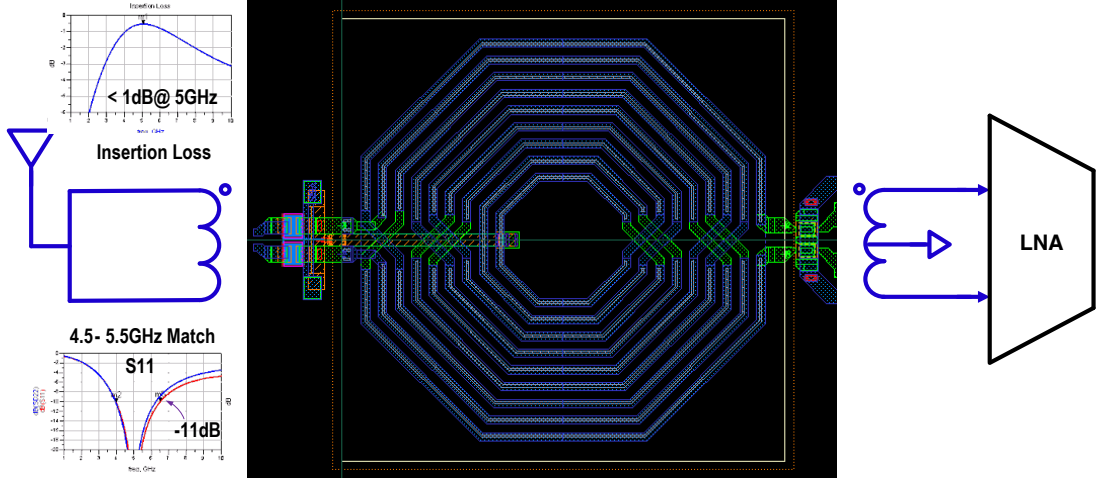


Figure 3.5: On-chip transformer

Low Noise Amplifier

The low input impedance of the common-gate amplifier makes it an attractive option for this design. Although a conventional common-gate design takes a hit on the noise figure as compared to its conventional common-source counterpart, it helps in maintaining a broadband match. It also directly stimulates the SRA.

A passive capacitor coupled gain-boosting technique is used in design the common-gate LNA. The passive amplification, A , reduces the noise figure of the amplifier by a factor of $(1 + A)$. It also increases the effective transconductance of the amplifier by the same factor while reducing the intrinsic transconductance, hence reducing the power consumption [57].

The LNA gain is limited due to the high input impedance selected for lower power in combination with the de-Q'ing of the SRA's tank for wideband sensitivity.

A casoded structure is used to implement the capacitor coupled gain-boosted common-gate amplifier. Cascoding provides reverse isolation from signal leakage back towards the antenna.

A 3-bit digital control register is used to tweak the bias current of the common-gate LNA. This helps setting the input impedance of the wideband LNA by changing the transconductance of the input devices.

The function of the common-gate amplifier is to ease the process of injecting RF energy into the SRA by facilitating the impedance matching. The amplifier also isolates the SRA from the antenna, so that the oscillations don't leak out the antenna.

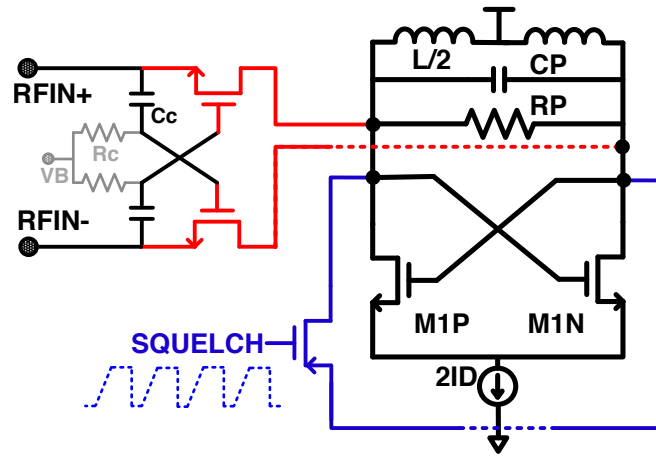


Figure 3.6: Receiver circuit - LNA followed by SRA

Super Regenerative Amplifier

The super regenerative amplifier(SRA) dates back to 1922 [58]. The SRA can be thought of as an oscillator on the verge of starting up *with the control being startup ready or not*. It consists of a cross-coupled NMOS pair providing the positive feedback in the oscillator. The principle is to get the SRA oscillations build-up periodically and quench these oscillations periodically. A squelch switch, which shorts the differential outputs of the SRA, is switched OFF for allowing the oscillations to build. Another important signal required for the oscillations to build-up is the injected RF energy. The frequency of the SRA oscillation should be near or equal to the signal frequency. The frequency

of quenching is much lower than the natural frequency of the SRA. This important difference allows the RF oscillations to build and be usable.

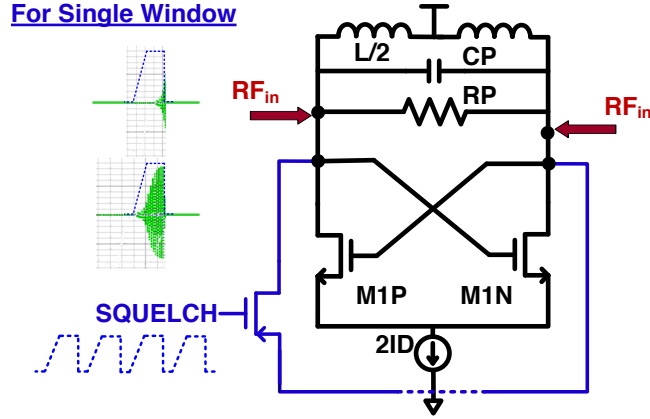


Figure 3.7: Receiver circuit - SRA

The SRA consists of a cross-coupled NMOS pair, a de-Q'ed inductor tank, and a tank-shorting squelch switch. A squelch generation circuit controls the switch to form distinct time windows where the receiver is sensitive. The startup time of the SRA is influenced by the received signal energy and frequency during the operating windows. The oscillation is then quenched so that another detection in interval can begin.

Multiple quench signals have been evaluated in literature [59] where different signal shapes have been analyzed. The authors suggest an optimal quench signal that is more complex to generate. They have also talked about sawtooth, square and sine shapes. A very similar shape to the optimal shape proposed in [59], has been used in this design. This design uses a trapezoidal shaped squelch signal. The squelch signal is designed to allow the SRA to be able to oscillate in 4 distinct time intervals at a frequency of the data rate. In other words, every data period has 4 distinct opportunities for oscillation.

Multiple digital control bits are used in the design as shown in 3.8 -

- SQ-WIDTH - 3 bits set the width of the squelch waveform un-squelched time in

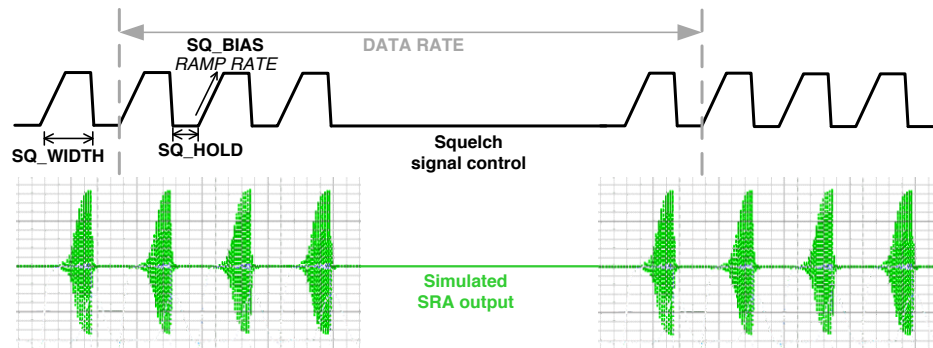


Figure 3.8: Squelch signal with control bits and simulated SRA output

1ns steps. This period also includes the ramping period

- SQ-HOLD - 2 bits control the hold time (SRA output shorted) of the squelch waveform
- SQ-BIAS - 4 bits control the ramp rate of the squelch waveform going to the squelch switch gate (PMOS)
- SRA bias current - 3 bits set the bias current of the SRA. Adjusted for oscillation to occur and to adjust the speed at which it grows in amplitude (startup-time) depending on the bias and the input energy

The process is shown as an inset in Fig. 3.4.

This kind of receiver is dedicated to short distance data exchange for which super regeneration offers an excellent trade-off between simplicity, low-power and overall receiver performances [60]. SRA is not very selective and any signal at the frequency of detection would cause a reception.

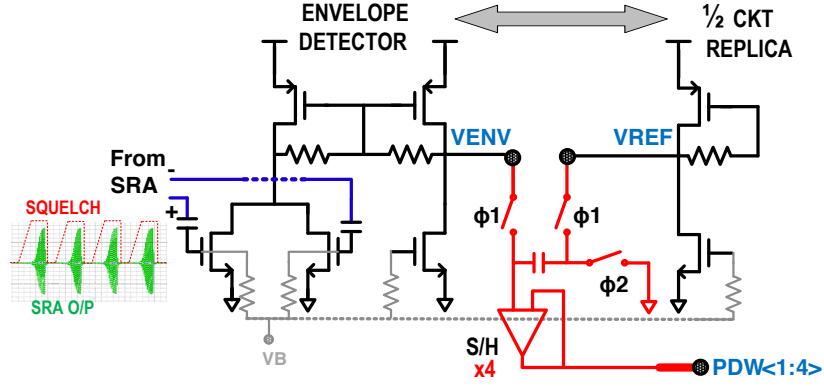


Figure 3.9: Receiver circuit - Envelope detector

Receiver Backend

A bank of four sample-and-holds record the envelope detector output at the end of each squelch window. The four sample-and-held values are averaged onto a capacitor to provide a running threshold voltage for comparing with the center two windows to determine if the a bit was received. Clocked comparators are used to generate early, late, and bit digital baseband indicator outputs.

Envelope Detector

The envelope detection of the super regenerated signal is achieved with a squarer circuit followed by a low pass filter. The drains of two NMOS devices with differential inputs are tied together. The odd order harmonics are canceled because of opposite signs. However, the even order harmonics add up as they are in phase, hence resulting in squaring. A current mirror provides the low pass filtering. It was noticed during testing that the single ended output of the envelope detector was noisy primarily because of supply current and clock transitions. A pseudo differential configuration is proposed here with better power supply rejection ratio(PSRR) and common mode rejection ratio(CMRR). At a slight cost of power, a half circuit replica is added to the envelope

detector mimicking the environment and producing signals that would be generated only because of noise. As the output of the pseudo differential envelope detector, the two outputs - (signal+noise) generated by the squarer and (noise) generated by the half circuit replica - are used to obtain a clean signal, which is used by the baseband circuit to obtain digital bit output.

Sample and hold

The squelch signal samples the output of the envelope detector at the end of each PDW as shown in Fig. 3.9. The sample and hold is designed to accommodate the pseudo differential signal originating from the envelope detector as shown in Fig. 3.10. In the first phase ϕ_1 , the two outputs are put on the top and the bottom plate of the capacitor. In the second phase ϕ_2 , the bottom plate is shorted to ground which is compensated on the top plate, thus obtaining a difference of the two signals. The output of the sample and hold is a set of four clean sampled voltages at end of each PDW.

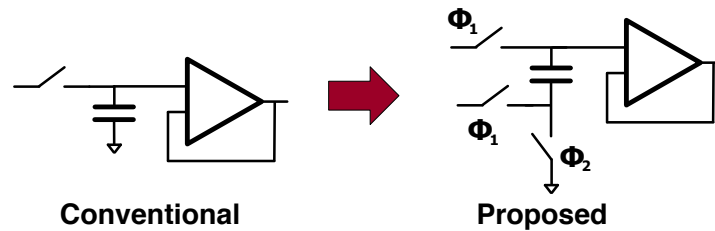


Figure 3.10: Receiver circuit - Sample and hold

Comparator

The comparator is implemented as a preamp followed by a latch [61]. The preamp is implemented as a common source differential amplifier. The latch is a cross coupled inverter pair as shown in Fig. 3.11.

In the preamp, switches are added between the supply and the circuit core, to allow

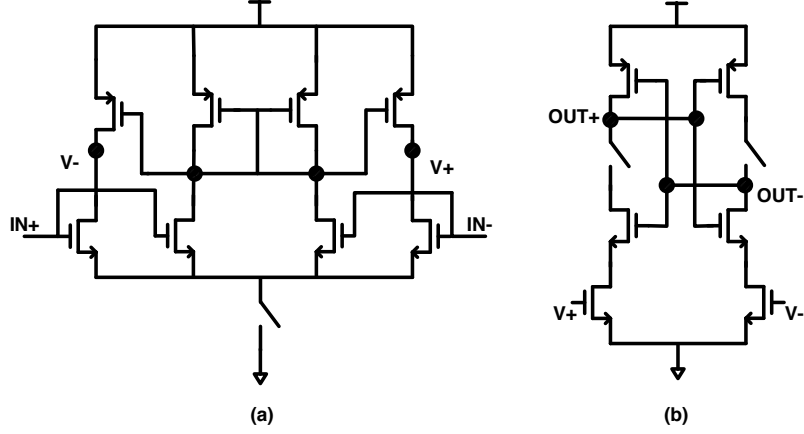


Figure 3.11: Receiver circuit - Comparator (a) Pre-amplifier, (b) Latch

the voltage to float, and help in achieving faster settling. The outputs are shorted together instead of shorting to the supply for faster settling. A g_m load is also added to the output for compensating gain for higher bandwidth. Adding the g_m load also reduces the output impedance and hence reducing the latch kick-back. The latch is designed to reduce offset by increasing the size the cross-coupled core FET sizes.

3.4.3 Summary

In this section we discussed the proposed receiver architecture and circuits. The system proposed in this work is a non-coherent energy detect receiver. The receiver uses the principle of super regeneration. A wideband common gate LNA is preceded by an on-chip transformer. The LNA feeds RF energy into the SRA which is periodically switched ON and allowed to oscillate. The SRA oscillates in presence of the electrical energy. A pseudo differential envelope detector follows the SRA, and feeds into the RF backend sample and hold. Clocked comparators are used to generate early, late, and bit digital baseband indicator outputs. Different control signals are also discussed in this section.

3.5 Timing Generation and Synchronization

3.5.1 Introduction

Unlike the traditional heterodyne architectures, the IR UWB transmits data in time. There is an inherent timing accuracy associated with IR UWB, since it has to occupy a large bandwidth in frequency it has a very sharp and short time response. For a 1GHz bandwidth, the response needs to be as short as a nanosecond. Due to the high time resolution, the timing constraints associated with IR systems are extremely accurate and hence synchronization in time becomes a critical issue driving IR transceivers. The receiver needs to be synchronized to the time of arrival of the impulses and the high time resolution makes this task difficult and complex

This section describes the architecture and the baseband circuit techniques used to complete synchronization. Since this is baseband and can be relatively easily worked out on a FPGA board, a decision was made not to add this with the design, as a step taken to avoid adding more circuits that could cloud errors and their debugging. This algorithm was implemented in MATLAB as a part of work done by [1].

3.5.2 Timing Generation

DLL

As described in the section above, the timing accuracy for the transmitter is very critical. The timing generation block in this prototype is driven by an external low frequency clock which will be substituted by a low power crystal oscillator with precise frequency control. It performs fine-phase control of timing signals used by transceiver blocks. The delay-locked loop (DLL) consists of a voltage-controlled delay line (VCDL), a phase detector (PD), and a charge-pump (CP) as shown in Fig. 3.12. CP uses feedback

techniques to ensure that the up and down currents for the charge pump are the same.

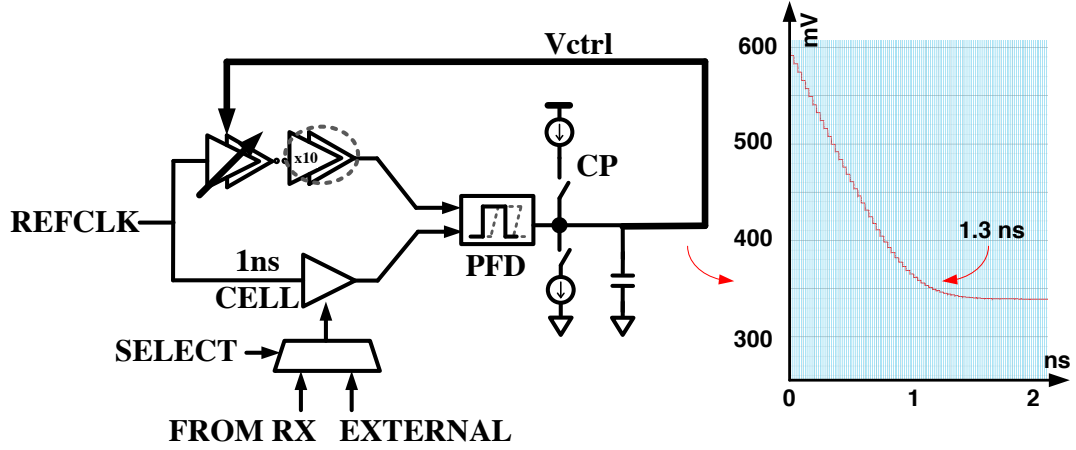


Figure 3.12: Transmitter DLL and control voltage settling (simulated)

The clock phases are selected by selecting signals from within the VCDL using a multiplexer. The phases of these signals are equally spaced within the total delay of the complete VCDL. The output clock is used as the timing reference for the pulse generator during transmission (another DLL in the receiver is used to control PDW). The resolution of the DLL in the transmitter is 100ps (and the receiver is 1ns).

3.5.3 Synchronization

For synchronization four fully programmable¹, equal sized, PDWs are used to locate and capture the data. Four windows A, B, C and D are combined using the logic shown in Fig. 3.4 to generate the early, bit and late signals. The data is located by traversing the entire clock period through PDW resizing and delaying/advancing the entire windowing sequence in steps of 1ns, obtained using the DLL. A larger PDW leads to higher power dissipation in the receiver whereas a smaller window might result in

¹ Duration between PDWs and their width independently adjustable

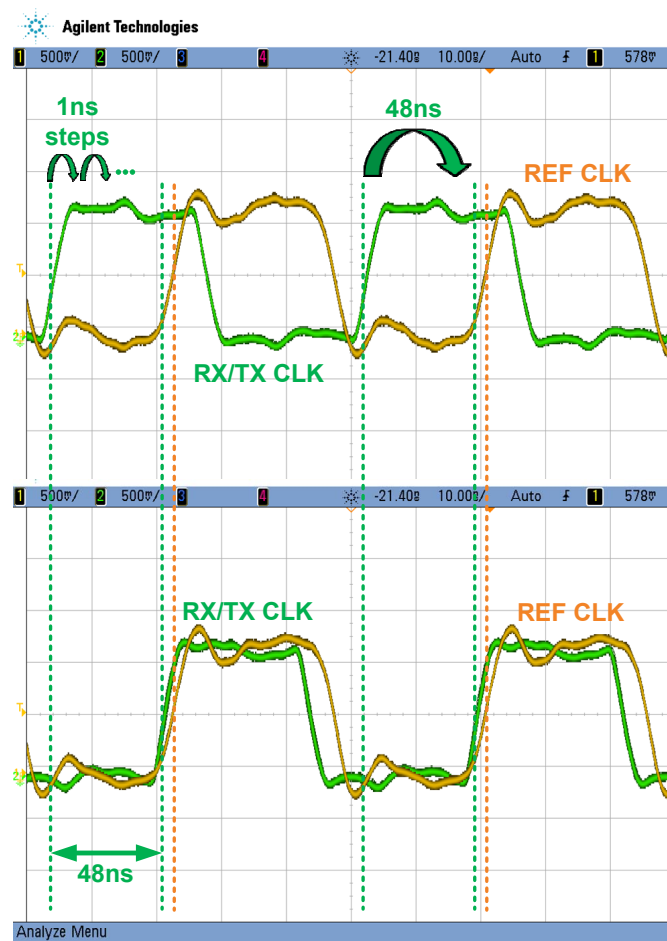


Figure 3.13: Measured Receiver/Transmitter clock phase control

erroneous detection due to incomplete SRA startup. An optimal PDW is decided by the signal energy level and the adjustable SRA bias current. Fig. 4.14 shows the width control on PDWs, with full power SRA to ensure startup.

The energy detect impulse radio based system requires initialization and synchronization phases before data can be transferred. The protocol was designed to efficiently accommodate synchronization and data transfer as well as meet the system specifications. The goal is to keep the power as low as possible while maintaining robustness and high quality audio transfer.

Refer to Appendix A for more details on physical layer protocol and synchronization algorithm.

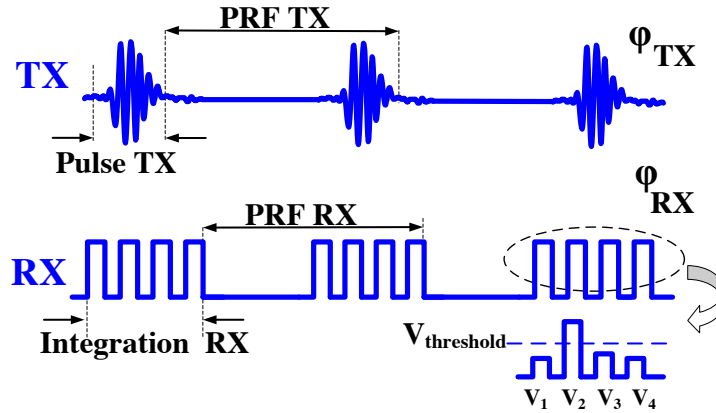


Figure 3.14: Synchronization design input summary and requirements

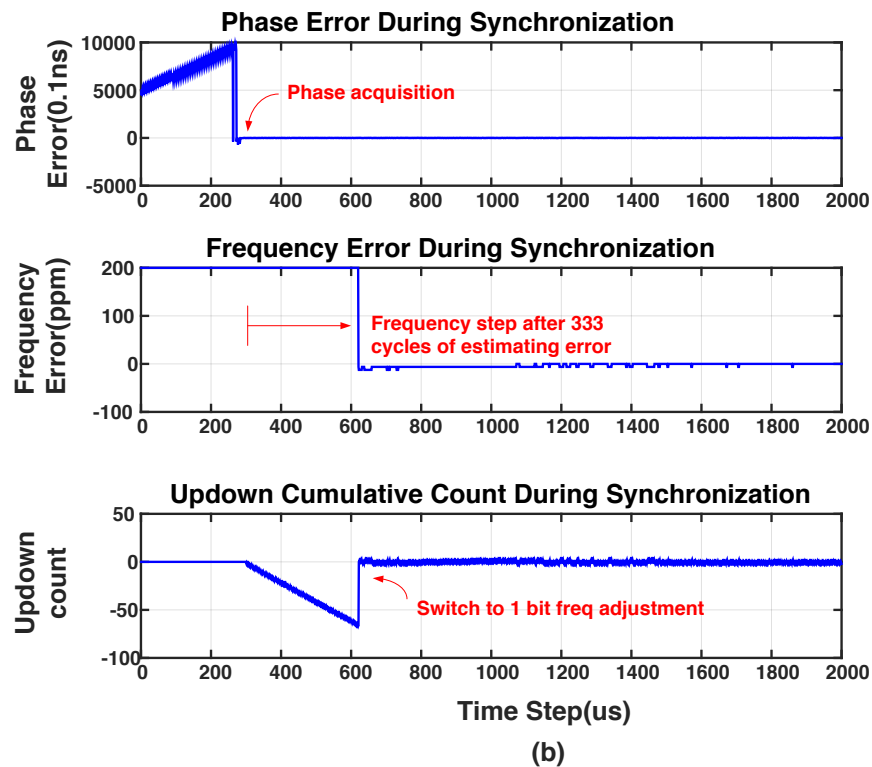
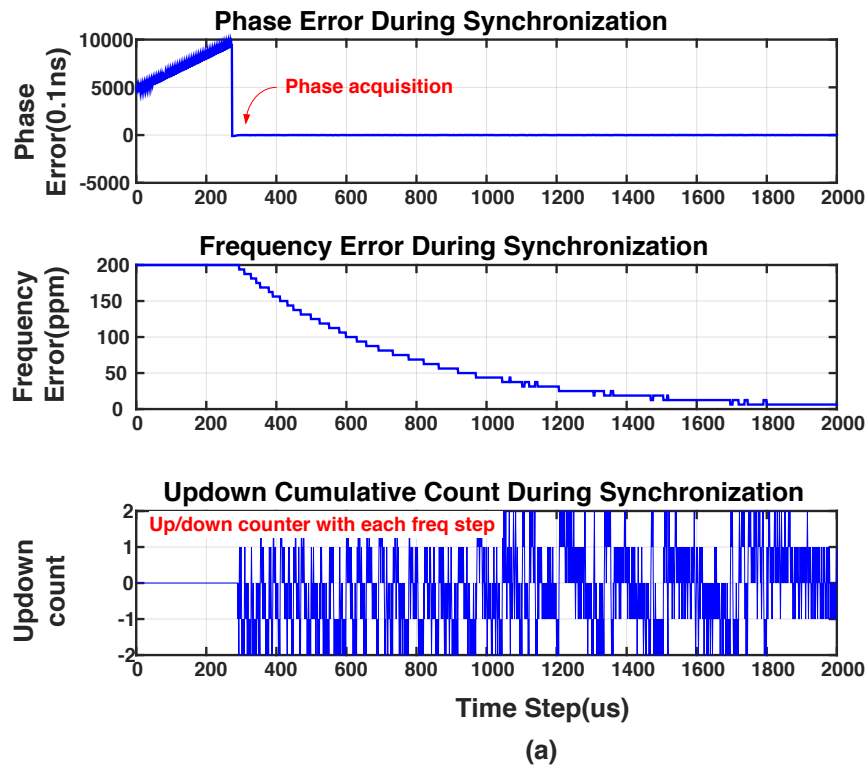


Figure 3.15: Phase and frequency synchronization - (a) Method 1, (b) Method 2

Table 3.1: Synchronization use conditions and system implementation solutions

Use condition	Remarks	System simulation	
		Method 1	Method 2
Phase mismatch	Worst case phase mismatch is T/2 (500ns)	253μs	253μs
Frequency mismatch	Assume 200ppm initial mismatch	1.5ms	341μs
Phase + Frequency mismatch	Simulation	>1.5ms (272μs for phase lock)	621μs (274μs for phase lock)
Tracking	Crystal drift over time Movement	For a 1ppm change in frequency, the radios need to travel at relative velocity of 300m/s	
All simulations performed for a time hop length 5 and data rate of 1Mb/s			
500 tap delay line is used in this simulation to provide a 1ns resolution			
Crystal oscillator parameters - low power 1MHz oscillator with +/-200ppm pulling			
Pierce oscillator presented here [62] -			
Base frequency 1.0048MHz			
Tuning range(Max/Min) ±800ppm			
Power 130nW			

Table 3.2: Simulated cycles to synchronize for given initial mismatches

Case	Inputs		Cycles to sync	
	Initial phase offset (ns)	Initial freq offset (ppm)	Method 1	Method 2
1	500	100	>1200	606
2	980	0	503	503
3	0	200	>1200	341
4	980	200	>1200	896
5	500	10	616	591

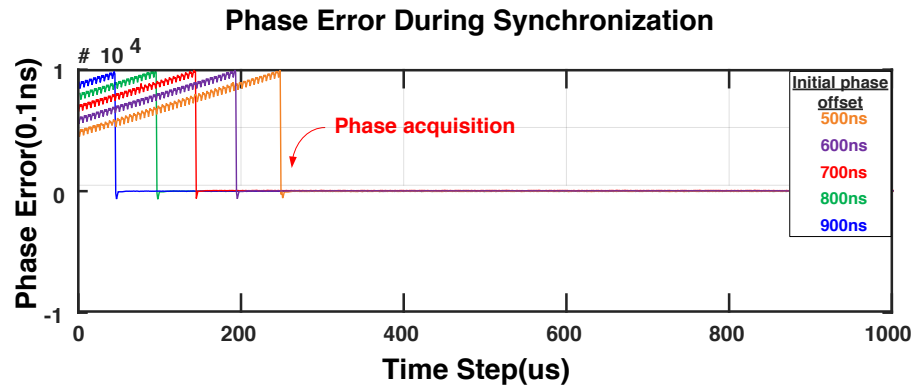


Figure 3.16: Phase offset sweep and lock time

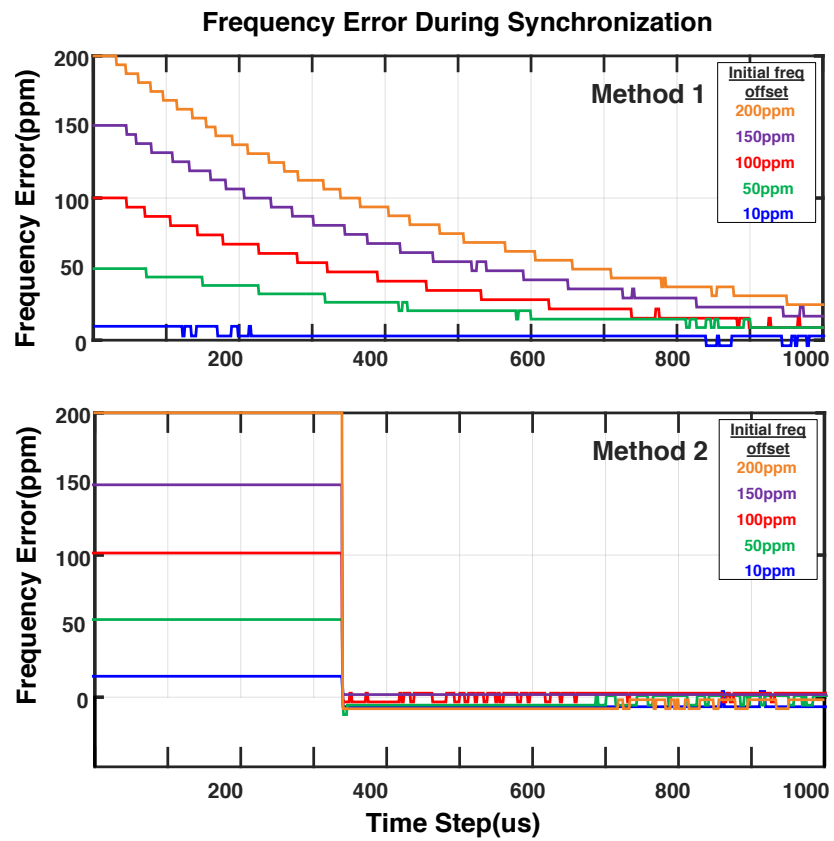


Figure 3.17: Frequency offset sweep and lock time

Chapter 4

Fabrication, Test Methodology and Measurements

4.1 Overview

This chapter presents the fabrication process and timeline, test preparation, test methodology and measurement results. The design in this work has been taped out in IBM 130nm CMOS process through MOSIS. The technology had a turn around time of 3 months. This time was generally taken for test planning. The first complete design was taped out in 2011 and a subsequent re-spin in 2012. The measurement results from both tapeouts are presented in this chapter. The package used and chip pinouts along with the hybrid design are also presented.

4.2 Design for Test and Test Preparation

The design has been carefully analyzed and test points have been added to the circuit with minimal loading and to give a clear understanding of circuit functioning. As

mentioned above the technology used for this is the IBM CMOS 130nm from MOSIS. The chips were packaged in a QFN (Quad Flat No-Leads) package locally at Dimation, Burnsville, MN.

The chips are generally coated with a glass top surface. Design test windows, pads, on the chip are metal structures connecting to the top metal of the process stack and the a glass window is made to allow access to the test point. Although majority of the signals are brought out through gold pins and wire bonds, there are signals that need access to debug test issues if and when they come up. Because silicon real estate is expensive, increasing the number of output pads is also restricted as that would increase the perimeter of the die. Putting the test windows ($50\mu\text{m}$ by $50\mu\text{m}$) also take up valuable silicon area. Hence, good engineering judgment dictates the number of vital test points and are shown for the receiver and synchronization blocks in Fig. 4.1 4.2. The design also tries minimizing the window size by using high impedance probes [65].

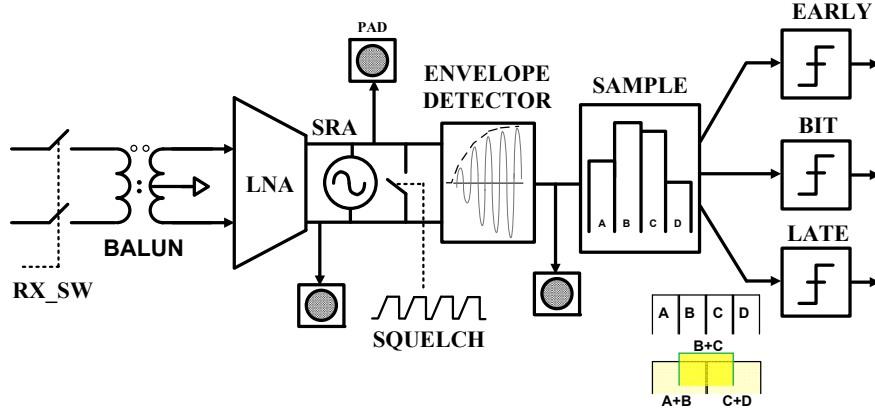


Figure 4.1: Test points in Receiver

Once the chips were designed and sent out for fabrication, time was taken to plan the testing activity. Hybrids were drawn in Altium [66]. A populated hybrid is shown in Fig. 4.3 being tested on the probe station.

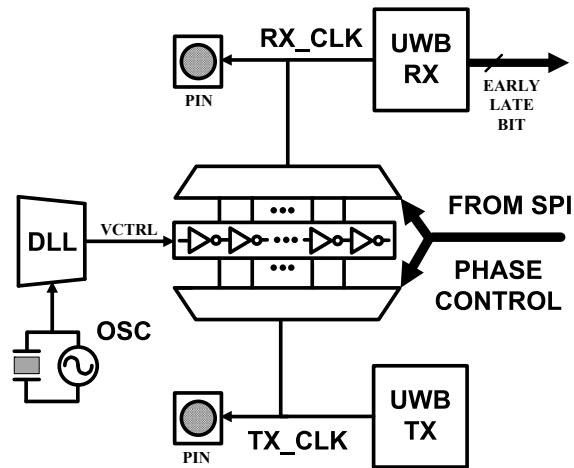


Figure 4.2: Test points in Synchronization

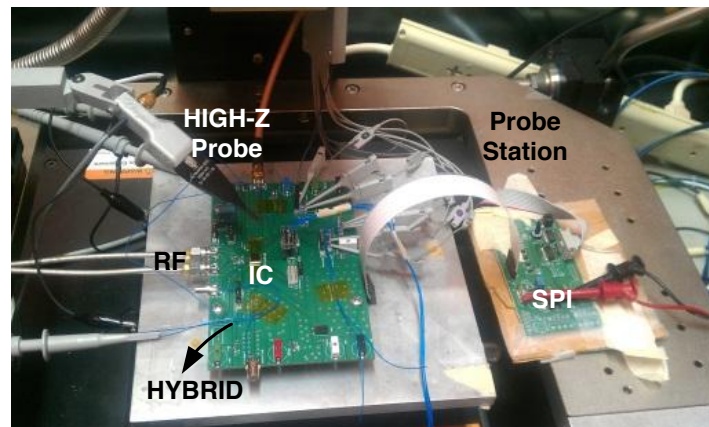


Figure 4.3: Populated hybrid on the probe station

Fig. 4.5 shows the bonding diagram for the package. Different signals originating from the die are marked. The differential RF signals on the bottom of the design are signals at high frequency, 5GHz. Care was taken to make these signals along with the ground signal beside them as symmetric as possible. We desire short bondwires for low inductance, care was taken to place the die closer to the QFN package boundary of the edge with the RF signals. The mutual inductance of the bondwires reduces the effective inductance due to the differential output.

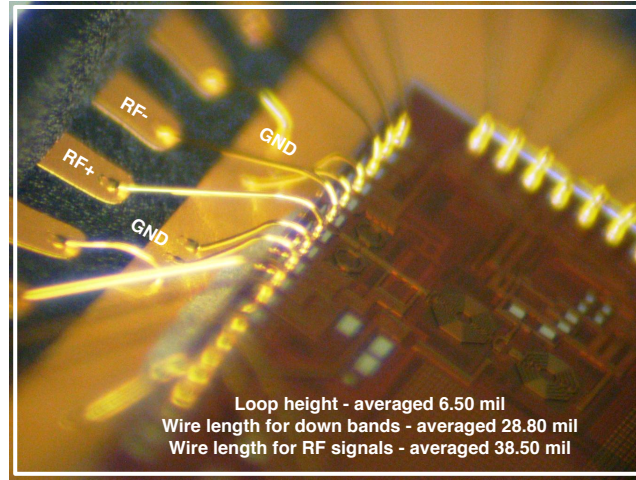


Figure 4.4: Bond wire dimensions

The transceiver is packaged in the QFN and the RF output bond-wires in combination with additional on-chip inductors form half of a double-tee resonant matching network [6] as shown in Fig. 4.6. We have used a double T matching network for a 100Ω differential antenna. Depending upon the bondwire the discrete components in the matching network were decided. Rather than differential shunt inductors and capacitors, they are split into two devices each. The input lines from the antenna on the PCB are differential microstrip. It is made in a way where we can test the S-parameters for the network with or without discrete components.

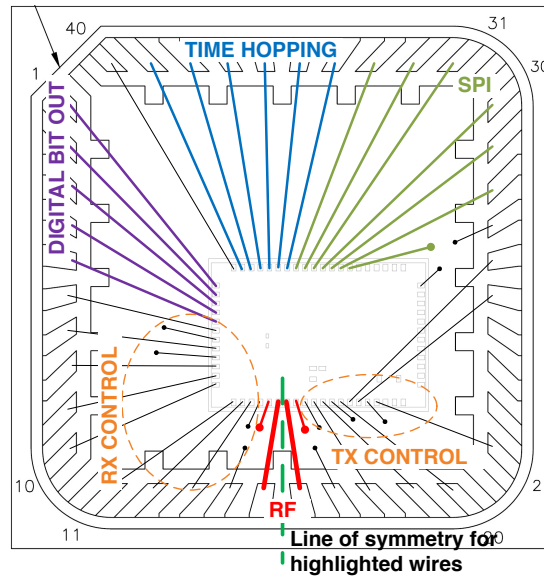


Figure 4.5: Bonding diagram

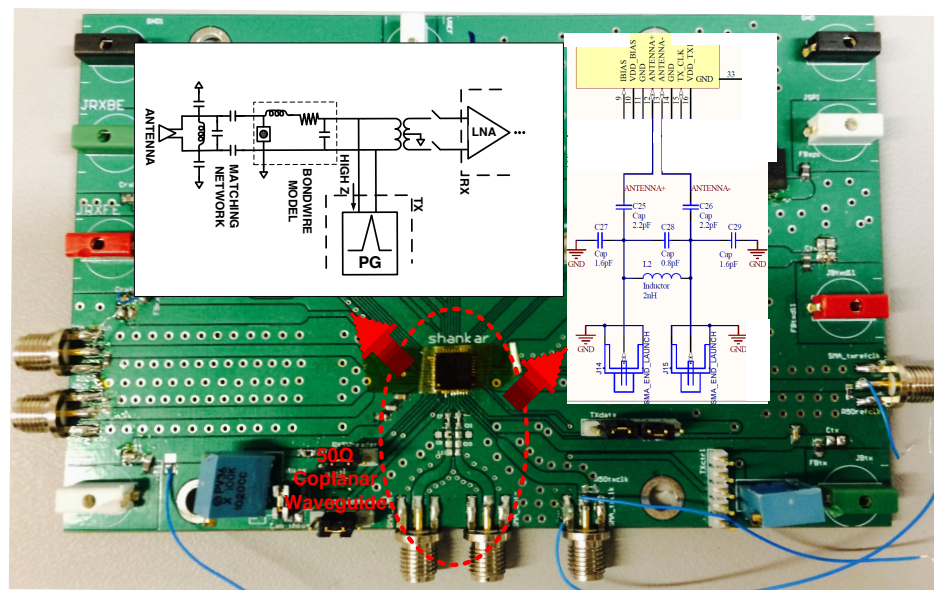


Figure 4.6: Hybrid design with the Altium schematic model and matching network design

The matching network is designed with low Q for wide bandwidth and the bandpass characteristic aids the RF input filtering and TX output pulse shaping. External SMT capacitors form the remaining half of the network, provide DC isolation, and allow control of two remaining degrees of freedom: the center frequency, and the impedance. This is important as both packaging inductance and the on-chip parasitic loading of the transceiver input may not be precisely known or may vary.

4.3 Test methodology

This design is a comprehensive and a complex transceiver architecture with multiple blocks and design elements. A test plan was devised to complete testing in the least resistive direction starting from critical blocks and building bottom-up. The stack up of the things to be tested were

1. High speed SPI register
2. Matching network to set external surface mount components
3. Timing generation circuit for receive and transmit
4. Digital transmit block
5. Integrated on-chip transformer
6. Receive architecture

SRA functionality

Receive back-end functionality specially the envelope detectors and S/H

Full receive system function

7. Combined transceiver measurements

8. Antenna measurements and using it measure over the air performance

Along with multiple test points as described in the section above, the design was also highly controllable with knobs and control signals. Some of the control signals have been described while talking about the circuit details in Chapter 3.

The list of testable structures is listed by chronology of tests, the reason for which was that if an item listed higher up did not work as expected, the lower items will probably not work as expected. As we move down in the list, the items get more complex and bigger.

4.4 Measurements

4.4.1 Overview

Shankar (IC tapeout in 130nm IBM CMOS process in 2012)

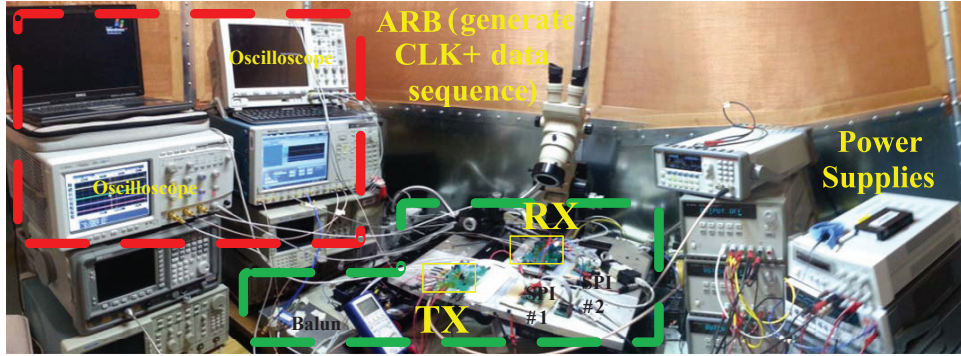


Figure 4.7: Measurement setup inside RF shield room

The prototype design was implemented in IBM's $0.13\mu\text{m}$ CMOS process. The chip occupies an active area of 0.67mm^2 including probe pads. The chip micrograph is shown in Fig. 4.8.

The IC is wire-bonded in a QFN leadless package and mounted on an 4-layer FR4

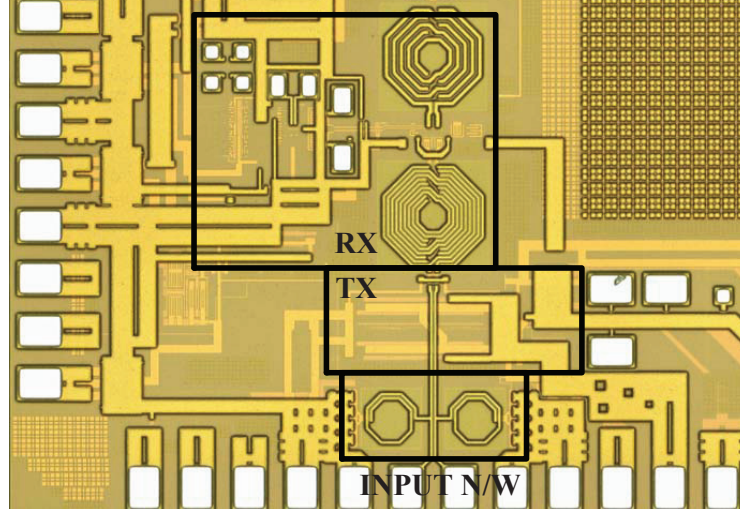


Figure 4.8: Die photo

PCB. SMA connectors mate with two 50Ω microstrip lines which transition into a 100Ω differential grounded coplanar waveguide (GCPW). Ground via strapping provides a reliable connection between the coplanar and inner ground planes. The GCPW traces nearly match the 0402 SMT capacitor pads for minimal transition disturbances and the coplanar grounds are used by the shunt capacitors in the matching network.

In this prototype testing, the transmitter and the receiver were tested separately. The testing can be majorly categorized as - testing the transmitter independently, testing the receiver independently and testing the integrated radio system.

4.4.2 Transmitter - Measurements

As aforementioned in the transmitter design, the UWB transmitter is a pulse generator simulating RF impulses at data rate. For the transmitter to generate PVT tolerant RF impulses centered at desired frequency and having desired bandwidth, 2 delay locked loops (DLL) provide PVT tolerant time delays. These time delays are in the order of 80 - 120ps. The DLL is also controllable manually by adjusting control voltage. Test

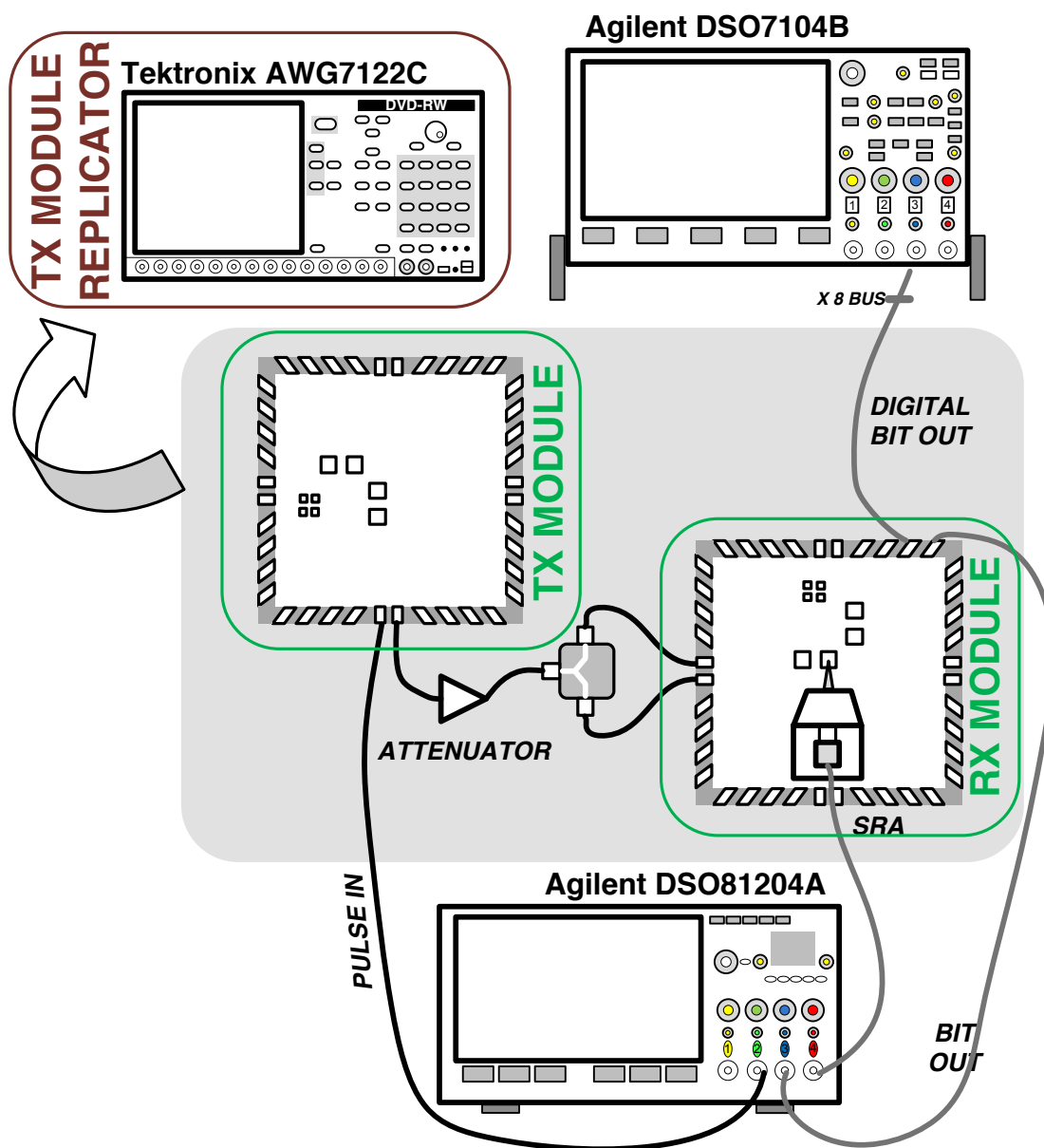


Figure 4.9: Measurement setup

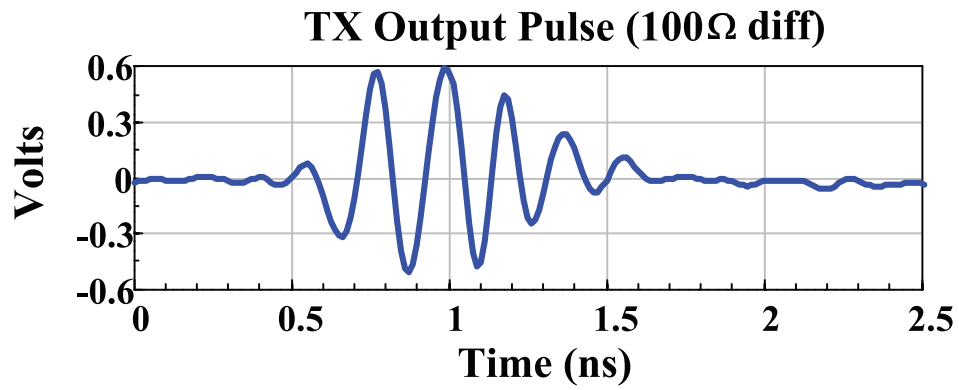


Figure 4.10: Measured transmitter pulse through package and PCB

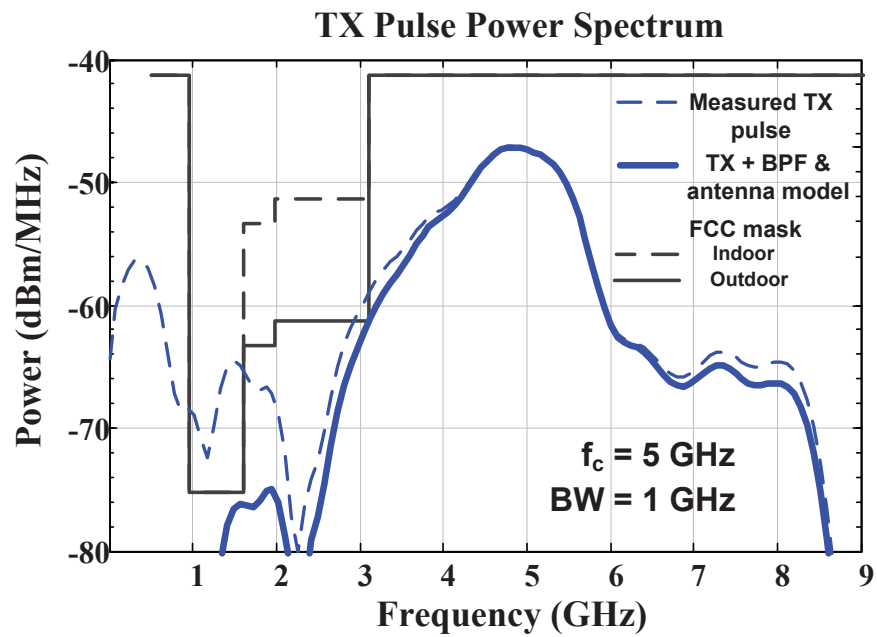


Figure 4.11: Measured transmitter output spectrum including antenna and matching network model with FCC mask

points were also provided to measure this time delay by XOR-ing reference clock with the delay divided clock.

To test the transmitter, an external clock of 50kHz is provided to the DLL. The data rate is set to 1Mb/s. 2 key measurements need to be performed for the transmitter. The average power spectral density of the transmit pulse stream needs to meet the FCC constraints. The power spectral density was measured on the spectrum analyzer (Agilent 85052D).

Fig. 4.11 shows the measured output spectrum of the pulse. The expected output with modeled off-chip antenna response and matching network (including package bond wires) is also shown. It can be seen that the pulse is FCC compliant, centered at 5GHz, and has a 3dB bandwidth of 1GHz. The transmitter output pulse was captured using a 12GHz oscilloscope (Agilent DSO81204A) as shown in Fig. 4.10.

4.4.3 Receiver - Measurements

Instead of using an ideal RF impulse to test the receiver, the captured transmitted output pulse waveform is used as the RF input to the receiver to take into account the non-idealities introduced by the modulation of transmitter. The measured transmitter output is used as an input data file to an arbitrary waveform generator (Tektronix AWG-7122C). The AWG is used to create pulse patterns, including modulation and phase shifts, for receiver testing.

The receiver in this work is a energy detection based non-coherent early-late detector. Individual blocks of the receiver were tested before testing the complete receiver demodulation chain. Testing probe pads were added to the receiver. The first test performed on the receiver was to analyze the functionality of the super regenerative amplifier (SRA). Initial testing of the SRA was done using a loop antenna connected onto

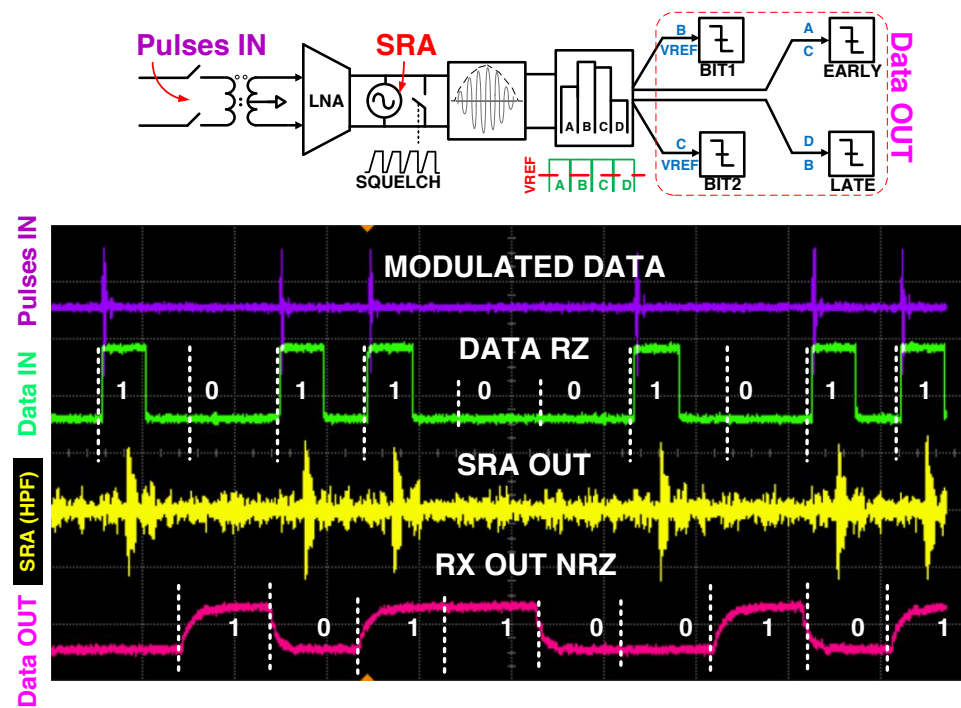


Figure 4.12: Measurement of OOK input pulses and data, followed by synchronized SRA response and received data

the Agilent spectrum analyzer. The loop antenna measurement is shown in Fig. 4.13. Internal SRA operation was observed using a high-impedance probe on the test probe pad (Picoprobe Model 35 - input capacitance 50fF and input resistance of 1.25M Ω). The high-Z probe provides insight into the control of the pulse detection windows (PDW). The PDWs are fully controllable - the integration time, the hold time and the rise time. Each pulse width is equal to the integration time when the receiver is sensitive to the input RF energy. The hold time is the dead time between consecutive PDWs. The ramp for the integration window is also controllable - this is the rise time. Fig. 4.14 shows the width control on PDWs, with full power SRA to ensure startup.

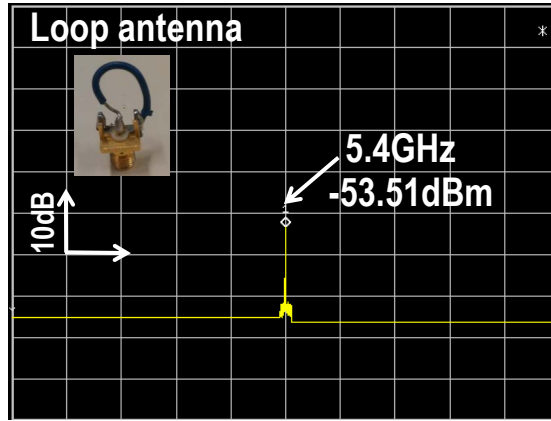


Figure 4.13: Measured SRA frequency spectrum using loop antenna

Receiver operation was evaluated over an input range of -30dBm (full power TX output) to approximately -70dBm using attenuators. In this test, the RF input was provided using the AWG. Receiver baseband digital outputs were monitored using a mixed-signal oscilloscope (Agilent MSO7104B). Since the RF input energy is not continuous, i.e. the input signal is not a continuous wave (CW), the receiver needs to be synchronized with the input data stream to be able to demodulate the signal. The receiver phase synchronization timing selection was performed manually depending on

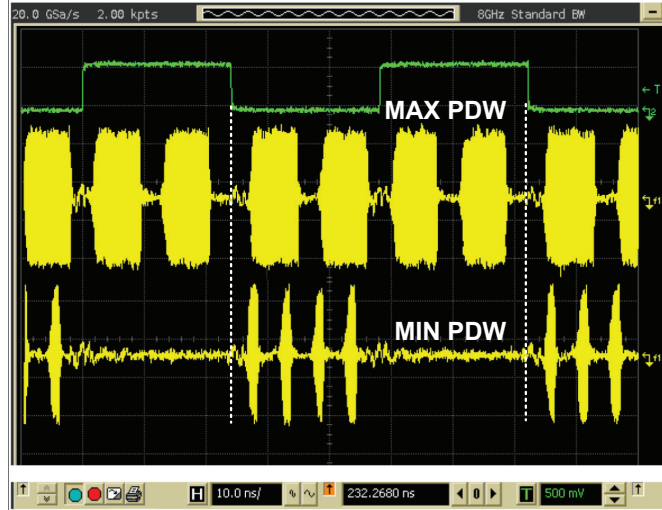


Figure 4.14: Superimposed plot of forced SRA startup showing 4 consecutive windows of maximum and minimum size

the test case and AWG waveforms. The algorithm followed to achieve synchronization is mentioned in 4.4.5.

Fig. 4.12 shows the demodulated output (red waveform) for an OOK input (green waveform). The figure also shows the modulated input pulse stream that was generated using the AWG (violet waveform). A repetitive (10110) pulse stream is used for this purpose. The corresponding SRA output is shown in yellow. The SRA amplifier output is measured using the high-Z probe. The high-Z probe has a single ended tip, hence allowing for only single ended measurement as a time. The low frequency noise on the output of the probe had to be high pass filtered to show the yellow plot in the figure. Note that this noise is common-mode and does not effect the functionality of the receiver since the SRA is differential. The bottom part of the figure shows the demodulated output over a longer time period. The input power is set to -30dBm for this measurement.

To measure the receiver sensitivity, the same test is performed again using a -70dBm

Table 4.1: RX measurements at 20.8Mb/s

Input (dBm)	V_{fe} (V)	I_{fe} (mA)	V_{be} (V)	I_{be} (mA)	V_{dll} (V)	I_{dll} (mA)	Power mW	FOM nJ/bit
-30	1.2	4.28	1.2	0.723	1.2	0.470	6.57	0.316
-30	1.0	4.25	1.0	0.628	1.0	0.348	5.23	0.251
-70	1.2	5.07	1.2	0.723	1.2	0.470	7.52	0.361
-70	1.0	5.12	1.2	0.723	1.2	0.470	6.55	0.315
-70	1.0	5.12	1.0	0.628	1.0	0.348	6.10	0.293

Notes: The signal generated by the AWG provided 0.0912pJ/pulse at the pcb. At 20.8Mpulse/s this is $1.9\mu\text{W}$ or -27.2dBm. The SMA connectors, FR4 PCB, and matching network imperfections conservatively provide a 3dB loss, hence the -30dBm spec.

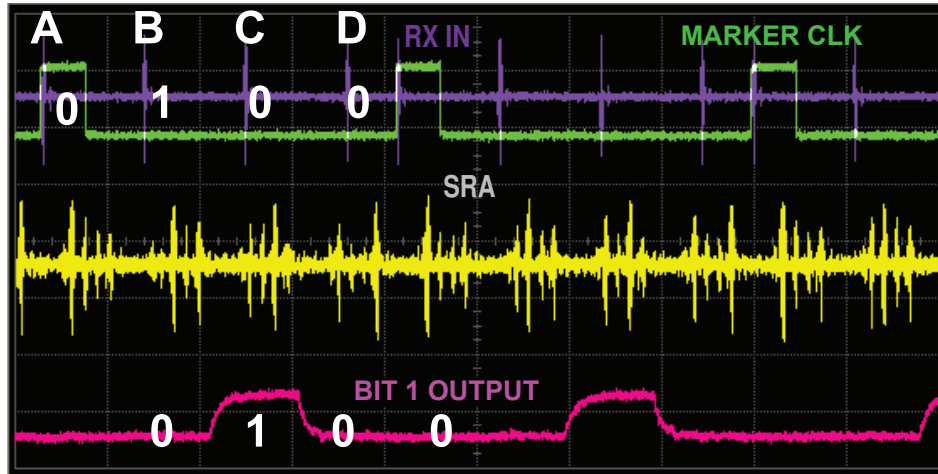


Figure 4.15: Measured sensitivity

input signal with successful demodulation. This measurement was done as a part of testing the early/late bit detection. Since the input energy has significantly reduced from the previous measurement, the SRA needs to be made more sensitive. This can be done in 2 ways - (1) by controlling the bias current of SRA and (2) by controlling the pulse width of the PDWs. As mentioned earlier the receiver is sensitive to the input RF energy only during the 4 integration windows. As the pulse width of the PDWs is increased, the available integration time for the input energy also increases, hence the sensitivity improves. Also, increasing the bias the SRA puts it closer to being able to oscillate, hence even a small input energy can make the SRA oscillate. The receiver becomes more sensitive to input RF energy as the bias current of the SRA is increased. By moving these 2 knobs, it can be made sure that in the programmed pulse width the SRA does not begin to oscillate by itself, at the same time providing adequate sensitivity to input RF energy. The RF input to the receiver is programmed into the AWG. The green plot in the Fig. 4.15 shows the marker clock from the AWG. Each frequency of the marker clock was $1/4$ times the frequency of the system clock, hence having 4 receiver clock edges in a marker clock period. The RF impulse is programmed such that the first RF impulse denoted by 'A' falls in the first integration window, the second RF impulse denoted by 'B' falls in the second integration window, the third RF impulse denoted by 'C' falls in the third integration window and the fourth RF impulse denoted by 'D' falls in the fourth integration window. The pink plot on the bottom shows the digital bit output of 'BIT 1'. The SRA output (yellow plot) is also shown in the Fig. 4.15. This is more noisy than the previous measurement owing to the fact that to achieve this measurement the current of the SRA was increased. The receiver is still able to demodulate this since the energy of the 4 windows is integrated onto 4 capacitors and compared. The PDW with the RF input energy will always have higher integrated

energy than the other 3 PDWs. The corresponding waveforms for this measurement are shown in Fig. 4.15, clearly indicating successful demodulation. It is to be noted that a different pulse stream in the green plot(0010).

With the same test setup, another set of measurements show the early/late bit output. Fig. 4.16 shows how the programmed RF impulses are aligned to the receiver clock. The input power is set to -40dBm for this measurement. The bottom plot shows sequential early/late signal. The early bit is followed by bit1 ('thresh1' in the figure). Bit1 precedes bit2 ('thresh2' in the figure) which is finally followed by the late bit. This measurement is taken using the 1GHz mixed signal oscilloscope (Agilent DSO7104B).

4.4.4 Integrated transceiver - Measurements

After independently testing the transmitter and the receiver, in this measurement the combined transceiver is measured. For measuring the integrated radio, the transmitter and receiver are switched ON on 2 separate dies. The transmitter from the first chip is used to generate modulated signal from input digital data stream. The modulated output from the transmitter is connected to the receiver through a wired connection. The receiver on the second chip is used to demodulate the RF input into digital bit output. In Fig. 4.17 the green plot is the digital data input to the transmitter. The transmitter output (yellow plot) is also shown. Pink plot is the demodulated receiver output. The figure shows the operation of the integrated transceiver for 3 data patterns with the data high percentages between 40% and 60%. As mentioned in the receiver description, the energy detection technique requires a reference voltage that is generated by averaging the 4 PDWs. The design is capable of providing this reference externally. For the purpose of these tests, the reference is set externally and is not changed for the 3 measurements. The demodulation of different data patterns for the same reference

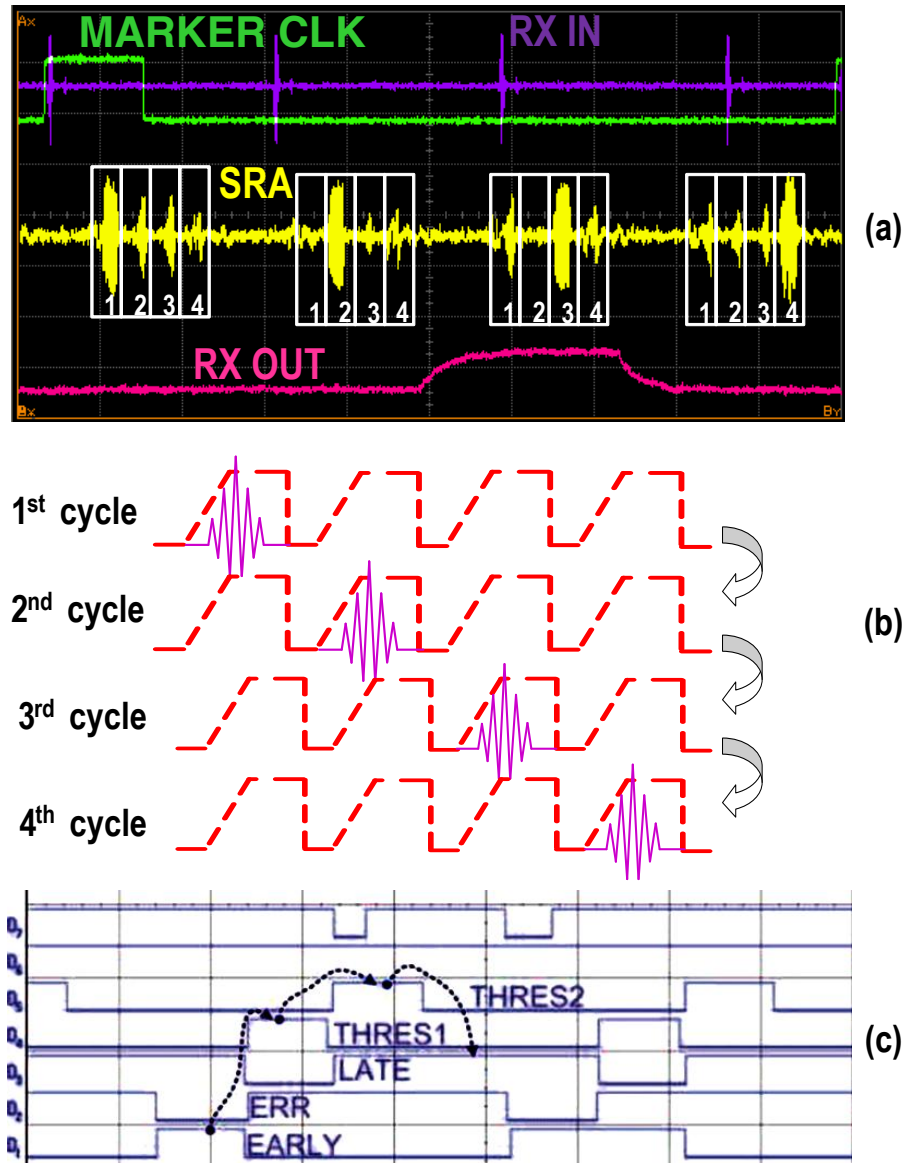


Figure 4.16: Early-late measurement control setup

voltage demonstrates the robustness of the receiver system.

4.4.5 Synchronization - Measurements

An algorithmic implementation of the synchronization procedure is performed manually as shown in Fig. 4.18. In absence of synchronization, none of the PDWs show SRA oscillations. Using the DLL control, the data was located by traversing through the clock period by changing the phase of the receiver clock. In the first step, a strong startup is obtained in the fourth PDW (Late), indicating of lagging receiver clock with respect to data. Hence, in the subsequent steps the clock phase is advanced to align data to the central PDWs (PDWs 2 and 3) by moving 1ns in each step. After alignment, a very strong startup is obtained in the second PDW (bit). The proposed synchronization algorithm lends itself well to automation and has been verified manually (Fig. 4.18).

4.4.6 Previous Design Iterations

Integrated Balun

The integrated balun was taped out separately and tested. Special test structures were created on the silicon die to measure the balun in short, 50Ω loaded, isolation and through test conditions. The test structures along with the balun are shown in Fig. 4.19 and the measurements are shown in Fig. 4.20.

Lhotse (IC tapeout in 130nm IBM CMOS process in 2011)

The initial balun was designed to be a differential to single ended design. However, during the design progression, it became more logical to design a differential to differential balun - transformer. The antenna was designed a differential elliptical bow tie antenna and both the receiver as well as the transmitter designs were completely differential.



Figure 4.17: Measured output for different data patterns

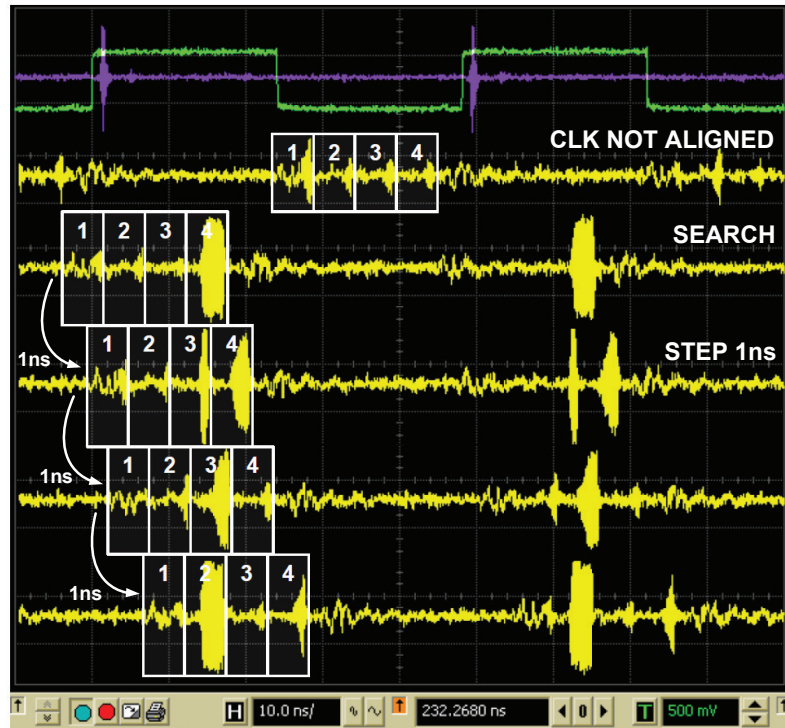


Figure 4.18: Synchronization algorithm (with manual control)

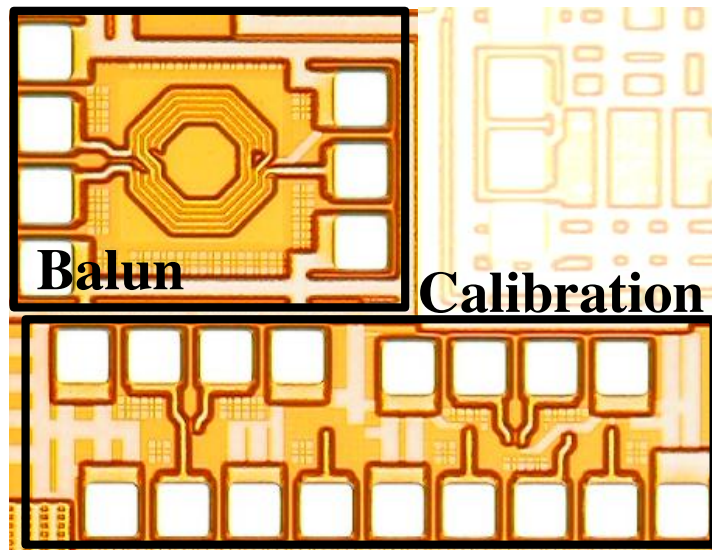


Figure 4.19: Die photo

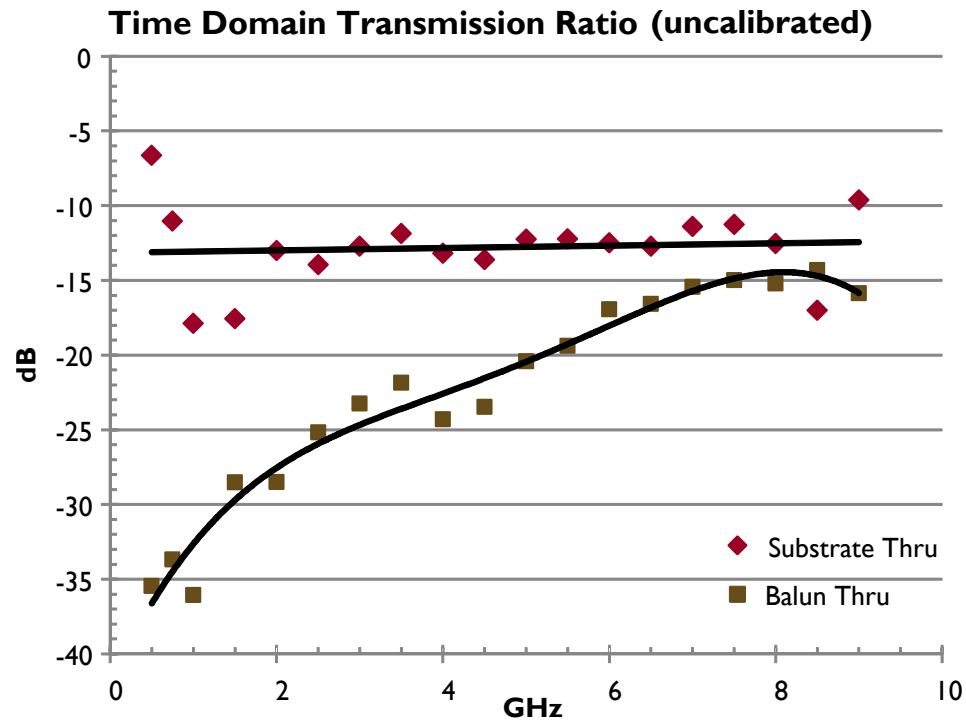


Figure 4.20: Balun through measurement

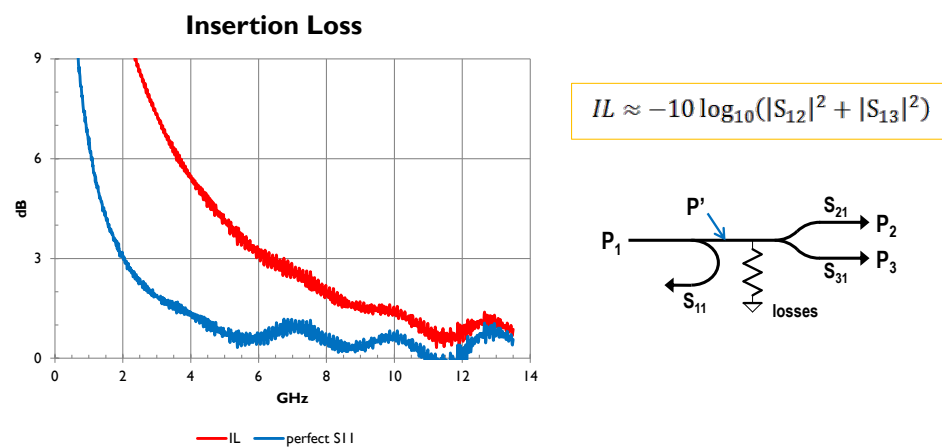


Figure 4.21: Balun insertion loss measurement

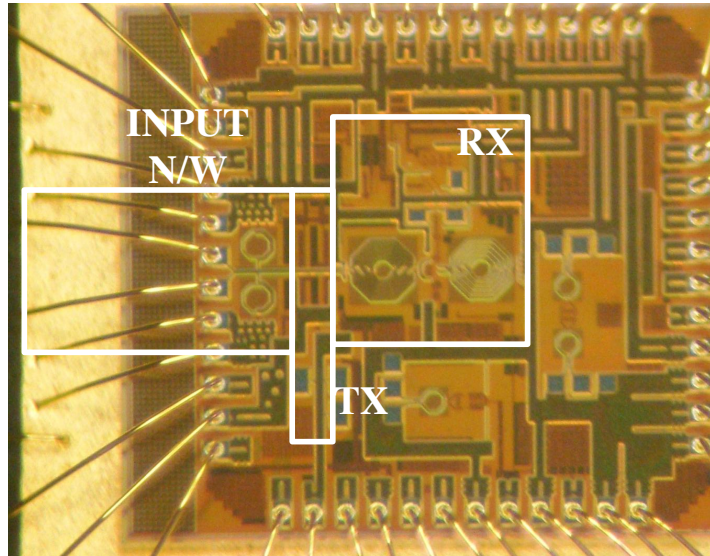
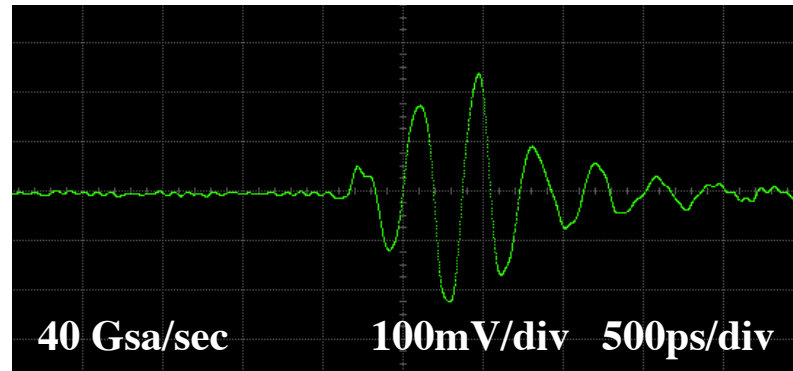


Figure 4.22: Die photo - Lhotse

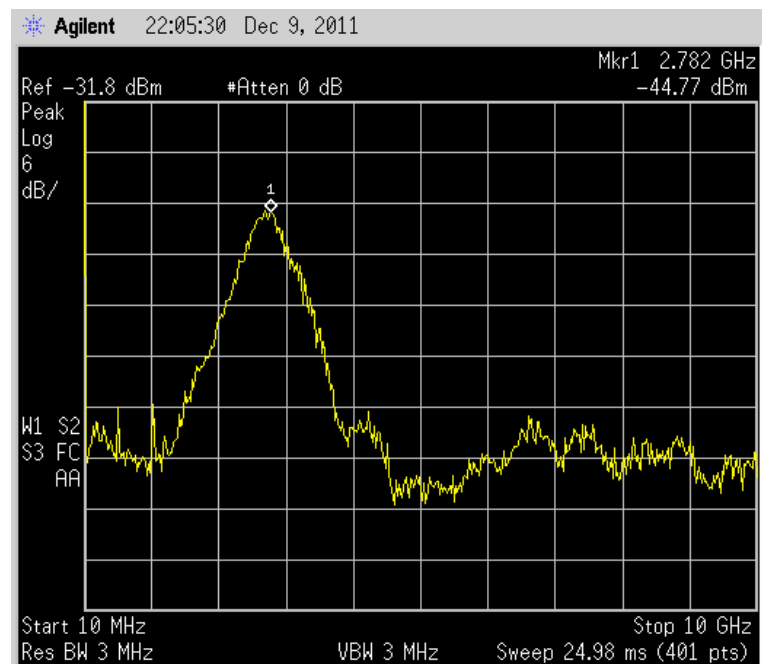
The complete design was taped out in IBM 130nm CMOS process through MOSIS in 2011. The design contained the all digital transmitter and the energy detect receiver along with the on-chip transformer. The design was tested following the methodology as described in the section above. The test results although promising did not meet the system requirements.

The high speed SPI bus and timing generation block worked as per requirement. The timing generation blocks including the phase selection on the transmit and receive blocks worked well and the test performed is shown in Fig. 3.13.

The transmitter measurements were performed as the next step. To test the transmitter, an external clock of 50kHz is provided to the DLL. The data rate is set to 1Mb/s. 2 key measurements need to be performed for the transmitter. The average power spectral density of the transmit pulse stream needs to meet the FCC constraints. The power spectral density was measured on the spectrum analyzer (Agilent 85052D). The measurements from the transmit block in Lhotse are shown in Fig. 4.23. However,



(a)



(b)

Figure 4.23: Transmitter measurement from Lhotse - (a) Time domain, (b) Frequency domain

the central frequency of the pulse was measured at 2.78GHz instead of the designed frequency of around 5GHz. This design issue was debugged and fixed in the next iteration, the measurements for which will follow in this section.

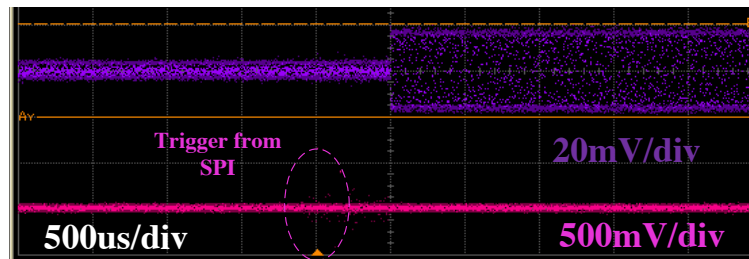
The receiver measurements were performed on the Lhotse design. The timing generation and high speed SPI demonstrated expected functionality. The next block tested was the SRA. The control bits allow for the SRA to have boosted current, which forces the SRA to start up, irrespective of the input RF power. The measurements are shown in Fig. 4.24. Fig. 4.24 (f) demonstrates which of the test points were probed to obtain the measurements. GGB Picoprobe [65] high impedance probe is used to probe these signals. The Fig. 4.24 (a,b) show the startup of the SRA. These subfigures have the SRA test point probed, with the squelch switch OFF allowing the SRA to oscillate by not shorting the tank. A control bit from the high speed SPI directs boosted current through the SRA, which make the SRA oscillate. A 500 μ s delay can be seen between the trigger and the SRA oscillation startup. A similar test was also performed by switching back to normal bias current from the boosted mode. This switches the oscillation off. Another test point probed is the envelope detector. Fig. 4.24 (d) shows the probed output of the envelop detector. Fig. 4.24 (c) shows the SRA startup by controlling boost current mode and the squelch switch signal. Two different settings are shown for both SRA and it's envelope.

When testing the complete receiver chain, the digital bits output which were expected to be the demodulated output did not produce expected results.

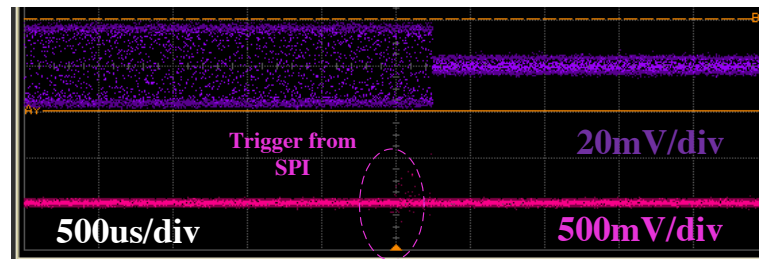
Design Debug

Transmitter

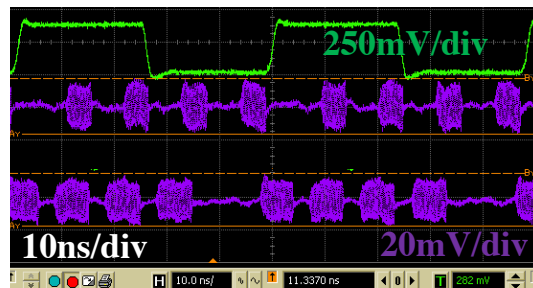
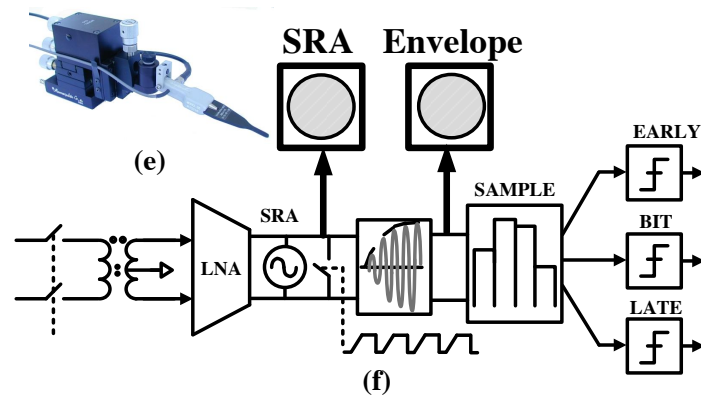
The transmitter operating frequency was measured and performed lower (2.8GHz)



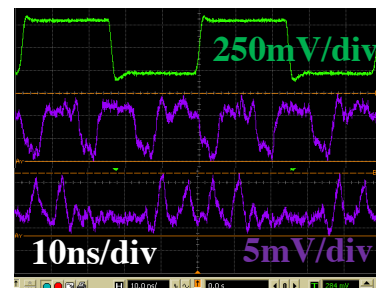
(a)



(b)



(c)



(d)

Figure 4.24: Receiver measurement from Lhotse

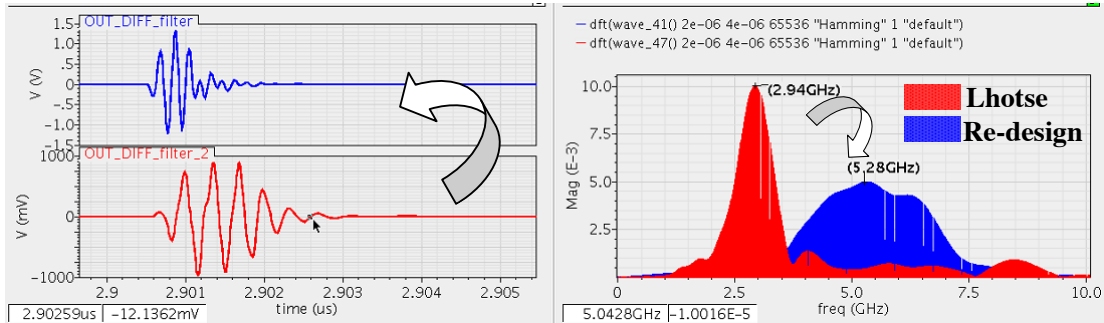


Figure 4.25: Transmitter re-design extracted simulations

than designed (5.3GHz), ratio of the measured to expected being **1.9**. The possible errors can be

1. Delay generation may be faulty and is not able to process the desired delay over the range of control voltage
2. Delay line replicating the delay from the DLL is not accurate by mismatches
3. Input matching network mismatch

Extracted simulations were performed and measurements results were replicated. The error was found on the delay replication (Fig. 4.25) because of differences in loading. A buffer was added to the design to fix this error and the re-design measurements worked as expected.

Receiver

The lack of demodulated output inspite of testing the functionality of the RF frontend seems to be pointing design issues in the receiver backend. However, the possible errors can be

1. Input matching network mismatch, which would result in filtering out any RF input energy

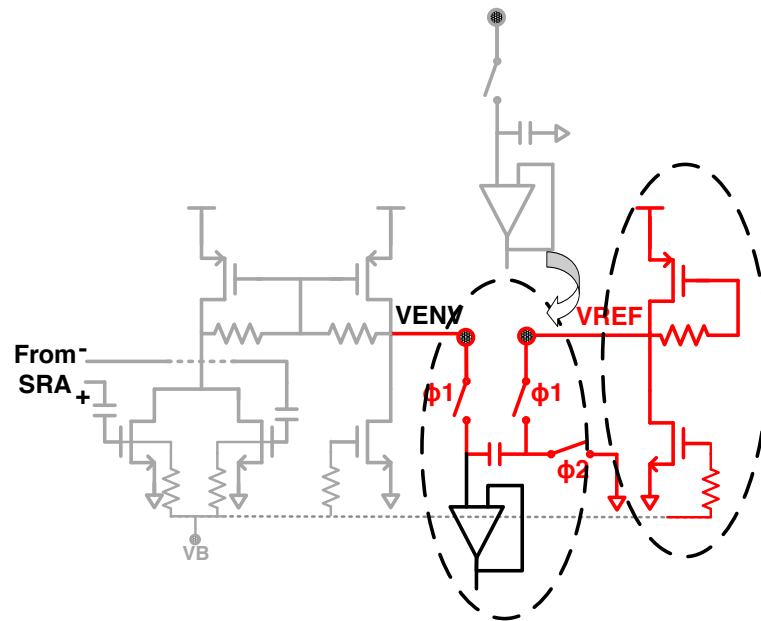


Figure 4.26: Receiver re-design

2. Receiver backend - S/H and comparator offset
3. Other possible receiver frontend design issues

Although this was a low risk item, the input scattering parameters for the receiver were observed to ensure that the input matching network was in-band to make sure that the matching network worked well. The measurements that we did have, the test point for the envelope detector gave some insight that was investigated further. The probed output from the envelope detector shows more noise (power supply, clock) than expected. The envelope detector is a simple squaring circuit with differential input. However, the design is not essentially differential. The following changes were made to the receiver

1. The re-design was updated and a half-circuit replica was added to make the envelope detector pseudo differential. The half-circuit replicates the noise sources

and is used to cancel the noise from the actual squarer to get a cleaner output response.

2. The S/H was updated from a single ended system to a differential input S/H.
3. For the preamp in the comparator, isolation was added from latch kick-back and latch's input referred offset was minimized. Along with this, the preamp outputs were shorted to power rail to clear memory. The preamp load was reduced for faster settling.
4. Comparator design optimized for faster response, outputs shorted together instead of shorting to power rails.

4.4.7 Summary

Transceiver performance, as well as comparison with prior art, is summarized in Table 4.2. As compared to [29] [31] (fabricated in lower technology nodes) we achieve comparable RX FOM with higher data rate and better TX power. While [26] has better sensitivity, the design is not fully integrated and has a higher RX FOM.

This work [33] uses simple digital circuit to achieve phase and frequency recovery for synchronization and tracking. Other works either use more complex schemes for synchronization, [29] uses automatic threshold recovery and [31] uses a pulse coupled oscillator, or use self mixing techniques for reception [30] which suffers from larger area and complex mixer design as discussed in Chapter 1.

Table 4.2: Comparison with other UWB-IR designs

Feature	This work [33]	ISSCC'13 JSSC'14 [29]	RFIC'11 TCAS-I'13 [31]	JSSC'07 [26]	VLSI'08 JSSC'09 [67]	RFIC'05 [30]
Modulation	OOK/PPM	OOK	OOK	PPM	OOK	
Synchronization	Yes	Yes	Yes	No	No	No
Technology (nm)	130	65	90	90	90	180
Antenna	Yes				Yes	
Pulse Repetition Frequency (Mbps)	0 - 20.8	2	0.15	0 - 16.7	0.12	50
Power (mW)	6.6 (20.8 Mbps)	0.75	0.086	35.8	0.4	41
RX FOM (nJ/bit)	0.32	0.38	0.5	2.5*	3.3	0.58
Sensitivity (dBm)	≈ -70	-76.5	-86	-99^*	-93	-72
TX FOM (pJ/bit)	16^\dagger		59		2900	252
Area (mm^2)	0.47-RX 0.05-TX	0.5 (RX)	1.7 (RX+TX)		2 (RX+TX)	3.8-RX 0.86-TX

* 0.85nJ/bit at 0.5V with -84 dBm sensitivity † Dynamic power at 1Mpulses/s

Chapter 5

Conclusions & Contributions

The technology landscape has quickly changed over the last few years. Developments in personal area networks, IC technology, DSP processing and bio-medical devices have enabled the integration of short range communication into low cost personal health care solutions. Technology has enabled remote patient care where the patient has low cost on-body wearables that allow the patient/physician to access vital signs without the patient physically visiting the clinic. Big semiconductor giants want to move into the wearable health monitor space. Along with the developments in fitness based health wearables, there has been a lot of interest towards developing BAN devices catering to the ‘mission-critical’ wearables and implants. Hearing aids, EKG monitors, neurostimulators are some examples.

This work aims at providing a ultra low power design for on-body medical BAN devices, more specifically hearing aids. Hearing aids have been around a for a long time now. They started of as a simple horn shaped mechanical and have now developed into small wireless devices. Wireless hearing aids with integrated transceivers can serve multiple radio links such as ear-to-ear, ear-to-consumer device, and between the ear and

a distant base station. This work aims at developing a low power radio solution for the aforementioned applications.

Previous designs employ narrow band systems like bluetooth, MedRadio. Multiple standards are present in the BAN. From the comparison of standards on the power versus data rate scale, there is a part of the spectrum that needs to be filled. A low power low data rate standard needs to be established to answer questions where extremely low power and low-to-mid rate data throughput solution is required. This work focuses on developing a radio for ultra low power, low-mid data rate transceiver. The ultra wideband benefits include low power, low cost, high data rates, multiple channels, simultaneous networking, the ability to carry information through obstacles that more limited bandwidths cannot, and also potentially lower complexity hardware design.

This work focuses on testing the impulse radio transceiver at high data rates capable of supporting audio data connection to consumer device via an dongle. This little dongle with the radio will plug into the audio jack of portable devices like music players, iphone, etc.. Another channel of interest in this work is the low data rate control channel for ear-to-ear and ear-to-remote control applications. The results presented establish functionality of the UWB radio at a data rate of 20.8Mb/s with high receiver and transmitter efficiencies. A variable data rate (10kb/s - 20Mb/s) transceiver is presented is presented in this work.

A complete fully integrated system is presented in thesis. This work presents a low-power noncoherent ultrawideband (UWB) impulse-radio (IR) transceiver operating at 5GHz in 0.13- μ m CMOS. A fully-digital transmitter generates a shaped output pulse of 1GHz 3-dB bandwidth. DLLs provide a PVT-tolerant time-step resolution of 1ns over the entire symbol period and regulate the pulse generator center frequency. The transmitter outputs -31dBm (0.88pJ/pulse at 1Mpulse/s) with a dynamic (energy)

efficiency of 16pJ/pulse. The transmit out pulse is FCC part 15 compliant over PVT variations. The transmitter is semi-compliant with IEEE 802.15.6 and IEEE 802.15.4 standards and will become completely compliant with minor modifications.

The receiver presented in this work is a non-coherent energy detect IR UWB receiver. The design is super-regenerative amplifier (SRA) based energy-detection receiver and the RF frontend contains the an input common gate amplifier and an on-chip transformer preceding the SRA. The SRA is followed by a pseudo differential envelope detector followed by a differential sample and hold circuit. Measured results show a receiver efficiency of 0.32nJ/bit at 20.8Mb/s and operation with inputs as low as -70dBm .

The system in this work utilizes early/late detection for a two-step baseband synchronization algorithm. The algorithm is implemented in Matlab and the time to synchronization is observed to be between $250\mu\text{s}$ to a few couple of ms. Measurements have also been made using the receiver and manually implementing the algorithm. A test was also performed on the complete transceiver system with two radios talking to each other over a highly attenuated wired channel.

5.1 Contributions

In this thesis, the following major contributions were made:

Rediscovering UWB

This work exploits the benefits associated with IR UWB for ultra-low power PAN/BAN. The large bandwidth is used to channelize the radio and also increase data throughput for PAN/BAN applications. IR UWB provides a highly advantageous alternative to the conventional narrowband radios that suffer from high power consumption.

Complete picture

A complete fully integrated system is presented in thesis. The design integrates optimizations in both transmitter and receiver to propose an extremely low power solution for low range low-mid data rate applications. This thesis integrates the most optimum transmitter and receiver into a complete system with timing generation and wideband antenna.

Along with the above work, this design is tolerant over process, voltage and temperature changes in the environment.

Digitizing the transmitter

A completely digital simplified low power transmitter is presented in this work. The digital pulse shaping eliminates the need of area consuming filters, thus optimizing silicon usage. The area of the transmitter presented in this work is $0.05mm^2$. The design is highly scalable and can be ported easily to newer and more efficient technology nodes. The transmitter pulse generator presented in this thesis is also easily scalable in frequency and bandwidth, thus catering to multiple solutions - IEEE 802.15.6, IEEE 802.15.4 - at the same time.

System level solution

Although the IR goes way back in time, certain system level concerns continue to plague the IR UWB. Fig. 1.10 shows the history of the development of UWB. From 2002-2015, it is interesting to note that out of a total of 16,130 publications on ‘uwb’ or ‘ultra wideband’, only 541 referred to ‘synchronization’. Only a handful (< 10) present an integrated solution [26–32]. This work [33] provides an integrated system level solution.

This work addresses all aspects time synchronization in an IR transceiver. The initial mismatch is addressed by two methods. Beyond the initial synchronization, the system presented in this solution is also capable of tracking. This would mean that

once the transceiver has been synchronized, the timing generation would continue to track the phase and the frequency changes depending upon crystal drift over time or movement between the receiver and the transmitter.

Circuit design

Innovative circuit design techniques have been used in completing the IR UWB system. The envelope detector has been implemented as a pseudo-differential block to counter any noise insertions due to the clock, supply or other environment factors. Some techniques have been employed to increase the speed of the latch and the comparator in the receiver RF backend. Specially placed FETs are used to improve settling time. Care is also taken to make highly symmetric circuits. Current matching is incorporated to match the up and down currents in the charge pump.

The work presented in this thesis had been adapted by industry liaisons and are in the process of developing it into a product.

5.2 Future work

Although the UWB momentum of 2002 is slowly losing steam, the original conceptualization has found way in other IEEE standards. The WiMedia Alliance and UWB Forum have ceased to exist. However, the low power, high data rate benefits of IR UWB can still be used as a part of a different standards, especially the UWB PHY of the IEEE 802.15.6 is quite interesting. UWB provided answers to the unanswered gaps on the power, throughput and range metric, and will continue to do so. The new MedRadio at 2.38GHz is an interesting development, however it is a narrowband solution with limited data rates and power consumption concerns.

Other avenues of research include optimizing algorithms for synchronization. Time

synchronization is a critical and a tricky issue to handle in IR UWB due to the extreme inherent time resolution of the technology. This work presented a simple algorithm to achieve phase and frequency match. There are more optimized search algorithms that are used in data analysis, which can be adapted in this system to improve synchronization time and hence improve power consumption even further.

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Appendix A

Synchronization

A.1 Synchronization

For synchronization four fully programmable¹, equal sized, PDWs are used to locate and capture the data. Four windows A, B, C and D are combined using the logic shown in Fig. 3.4 to generate the early, bit and late signals. The data is located by traversing the entire clock period through PDW resizing and delaying/advancing the entire windowing sequence in steps of 1ns, obtained using the DLL. A larger PDW leads to higher power dissipation in the receiver whereas a smaller window might result in erroneous detection due to incomplete SRA startup. An optimal PDW is decided by the signal energy level and the adjustable SRA bias current. Fig. 4.14 shows the width control on PDWs, with full power SRA to ensure startup.

The energy detect impulse radio based system requires initialization and synchronization phases before data can be transferred. The protocol was designed to efficiently

¹ Duration between Pulse Detection Windows (PDWs) and their width independently adjustable

accommodate synchronization and data transfer as well as meet the system specifications. The goal is to keep the power as low as possible while maintaining robustness and high quality audio transfer.

A.2 Physical Layer Protocol [1]

The impulse radio can achieve very low powers by shutting down in between impulses. In order for the receiver to know when the transmitter will be transmitting, the receiver and transmitter must be synchronized. The level of synchronization needed is difficult to maintain over a long period of time. Therefore the data is and synchronization overhead is partitioned into beacons. Each beacon contains a synchronization period followed by a fixed amount of data. Since the pulse repetition rate of the radio is much higher than the audio bit rate this forms a burst of data followed by a low power sleep.

The synchronization is operated in a master/slave system. Master sends out connection request beacons to the slave. The slave periodically wakes up to listen for connection requests and responds with an acknowledgment. Once the master and the slave have synchronized, the data packets are sent over the channel with periodic standard sync beacons. If the synchronization is lost, the master will continue to send sync beacons to resynchronize.

The beacon contains five parts. The beginning of each beacon contains a preamble. During the preamble the master sends a continuous string of “1”s. The length of the preamble is determined by whether or not the slaves synchronized to the master on the previous beacon. If the hearing aid(s) were previously synchronized the master sends a shorter standard preamble. If the hearing aid(s) were not previously synchronized the microphone will send a longer sync preamble.

The circuits required to achieve this synchronization consists of a delay locked loop

with 1ns taps, a 5-bit oscillator, overlapping integrators, and digital control logic. The synchronization design inputs are shown in 3.14. The delay locked loop with 48 1ns taps allows the slave to adjust the phase in one clock cycle by simply selecting a different tap via a multiplexer. The 5-bit oscillator allows the slave clock to adjust its frequency to match that of the master. The overlapping integrators look a little ahead and behind of the main integrator to see if the phase is early or late and adjusts accordingly. If the phase is continuously being adjusted in the same direction the frequency is adjusted accordingly.

The hardware design also accommodates time hopping. Time hopping is used to prevent multiple wireless microphones in the same vicinity to have catastrophic collisions. If the phases of two systems without time hopping aligned the slaves could synchronize to the wrong master and cause interference. Time hopping moves the location of the pulse within the bit window. The locations are at set delays and the sequence of delays is a predetermined code that the master and slave are programmed to follow. Once the slaves find the correct phase and time hop sequence, they do not have to find the time hop sequence again.

A.3 Synchronization Algorithm [1]

The necessary clock frequency and phase adjustments can be controlled by a digital synchronization control using counters as shown in Fig. A.1. Synchronization is achieved using the early/late impulse detection timing queues from the receiver. The phase is adjusted by selecting a different tap of the multiplexer. The N-bit counters are used for phase control unless they overflow in which case frequency control is initiated through the frequency counter. Frequency corrections are made every $2N$ consecutive early/late signals, taking care of the progressive phase mismatch. Tracking capability is achieved

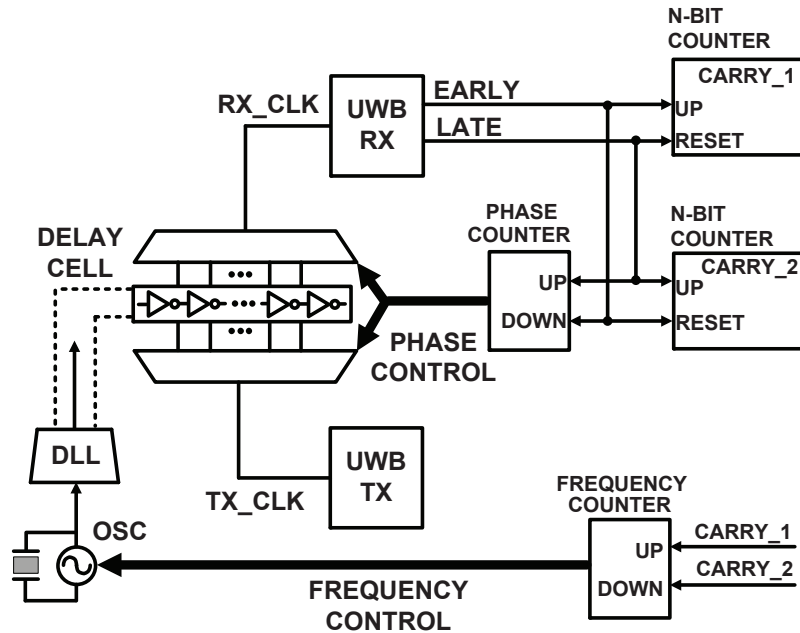


Figure A.1: Synchronization algorithm diagram

since early/late data continues through signal reception.

The proposed system has a 2-step synchronization algorithm. The system uses a brute force coarse phase acquisition scheme for finding the phase and then a fine phase adjust to improve the BER and track the phase. Finally the frequency is adjusted by watching the phase shift in order to prevent the need for full synchronization each time. This system is described below with the corresponding protocol. The design also allows for time hopping. Time hopping is minimal pulse position scrambling in time. Although time hopping will increase the synchronization time it helps prevent collisions with multiple IR running at the same pulse rate. It also prevents slaves bonding to a wrong master and helps the transmitter to meet FCC mask better by making it less spiky. The continuous impulse train would have spikes in the spectrum repeating at the pulse repetition frequency.

A delay locked loop as described above adjusts the delay elements to make the 48 tap delay line equal to half the clock period ($f_{CLK} = 20.8\text{MHz}$). The delay line is only half the clock period in order to save power. The other half of the delays can be used by using the inverse of the clock signal. The delay elements use well known current starved inverters that are controlled by their current. The DLL control adjusts the current to their delay elements. This loop only runs on startup and after the oscillator has been updated.

1. The first synchronization step is coarse phase acquisition. The PDWs described above are combined to generate 3 overlapping integration pulses, each with a duration of twice the programmable PDW. These 3 overlapping integration pulses are compared to a moving threshold to generate “1” for the presence of a signal and “0” for absence of the signal. It searches through the delay line looking for a “1” out of the 3 - early, bit, late - comparators as shown in 3.4. If it doesn’t find a “1” the slave phase jumps by 2 times the PDW length to check the next phase. Once it finds a “1” it searches for another “1” at the next pulse adjusting for the 2nd pulse time hop. It continues through the full sequence. If it gets a “1” at each of the time positions it assumes it has found the master and continues to the fine phase acquisition phase. Otherwise it continues to search for the master.
2. Once the phase has been found with coarse 10ns steps the phase will continue to be adjusted using the fine adjustment. In this phase, the loop is the same as Loop 2 except the time hop sequence and master phase have been found. Another difference is that instead of looking at comparators A, B, and C, only comparators B and AC will be used. The others will be turned off to save power. The A and C integrator outputs are compared directly in the AC comparator instead of comparing to a fixed reference. This tells the logic if the phase is early or late.

The logic will adjust the multiplexer to adjust the phase by 1ns increments this time. This loop continues to adjust the phase during the preamble and the rest of the beacon.

The oscillator is adjusted by “watching” the phase adjustments that are being made. Since the frequencies are different the phase will continue “moving” down the delay line. The fine phase adjustment will cause the multiplexer to switch back and forth between two delays usually but eventually move in one direction more than the other. Two methods were analyzed to adjust the frequency. The 2 methods used in this design are changing the frequency by an LSB after waiting for a threshold to hit on the up-down counter and watching the phase for a longer time before adjusting the phase. The former is proposed because if the difference in the initial frequencies of the master and slave is large enough (>100 s of LSB), it might take a very long time before a frequency lock is obtained.

Appendix B

Antenna

B.1 Antenna Design

Owing to the product size constraints, the antenna needs to be small with an isotropic RF field. Different antennas were looked at, and a differential bowtie antenna configuration was chosen. The reason for choosing this design is that the bowtie has a wider bandwidth for its small form factor. HFSS simulations were performed with a head model to optimize the design.

This section briefly describes the design and measurement of the elliptical dipole antenna. The antenna is illustrated in Fig. 2.9. The primary design parameters that affect impedance and gain include b , el_rad , and rot . A dipole antenna structure was chosen for its omnidirectional pattern. The elliptical shape provides a wide impedance bandwidth. While a full ellipse provides a wideband input impedance, the antenna gain suffers as the S11 is too high. A full ellipse would require too large of an antenna. We will define the ellipse aspect ratio as $2 * el_rad/b$. An ellipse aspect ratio closer to 1 yielded a more omnidirectional pattern footprint. Truncating the edges of the ellipse reduces the size but the bandwidth is too narrow. In this design, a compromise between

bandwidth and antenna gain was found by rotating the ellipse so that just enough of the curved portion of the ellipse is realized. This antenna was designed to operate in the vicinity of 5 GHz with a differential input impedance of 100Ω . The design was carried out using Ansys HFSS. Simulations confirmed that the resonant frequency of the antenna impedance increased with a smaller antenna aperture, or el_rad and b .

To facilitate measurement on a single ended system, a monopole version of the antenna was fabricated over a circular ground plane. In this arrangement, the input impedance gets cut in half and the directivity goes up by a factor of two. Fig. B.2 shows acceptable agreement between measurement and simulation of the antenna $|S_{11}|$.

Impedance and Gain measurements were performed using an Anritsu network analyzer and a SWH-24 Horn antenna in an anechoic chamber. Antenna Gain and impedance data was used to de-embed the path loss, horn antenna gain and cable loss. Antenna gain measurement and simulation data are plotted in Fig. B.4 (a-b). Fig. B.4(b) shows measurement data for different cuts at 5 GHz. Refer to Fig. B.1 for the orientation.

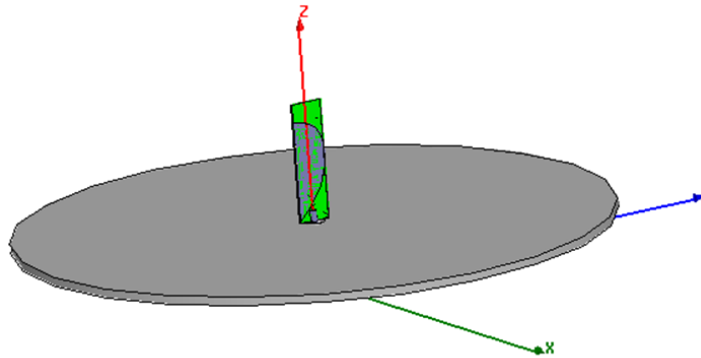


Figure B.1: Dipole antenna configured in a monopole configuration over a circular ground plane

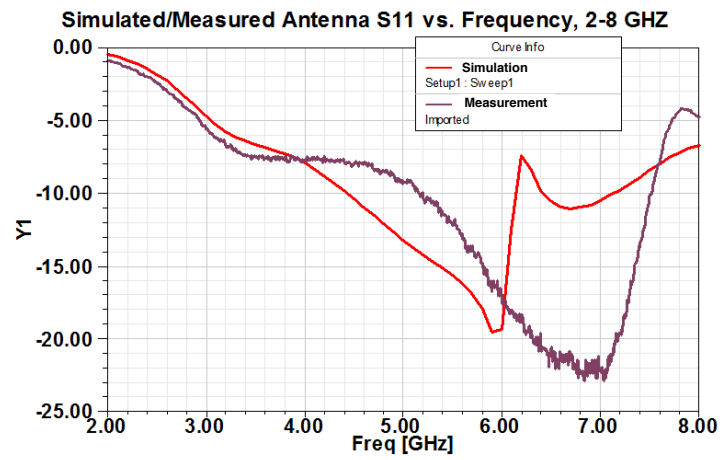


Figure B.2: Antenna performance over frequency

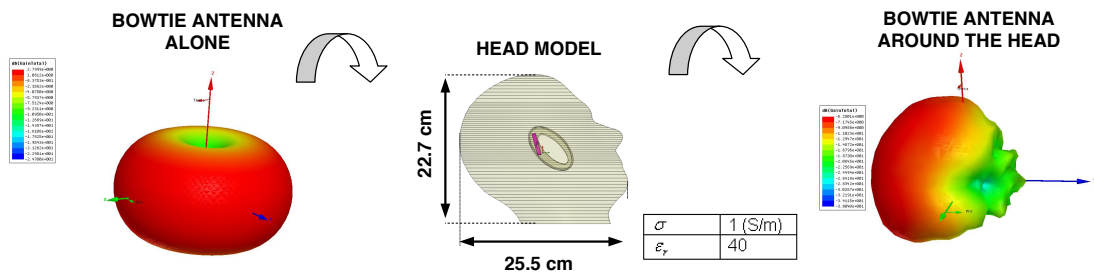
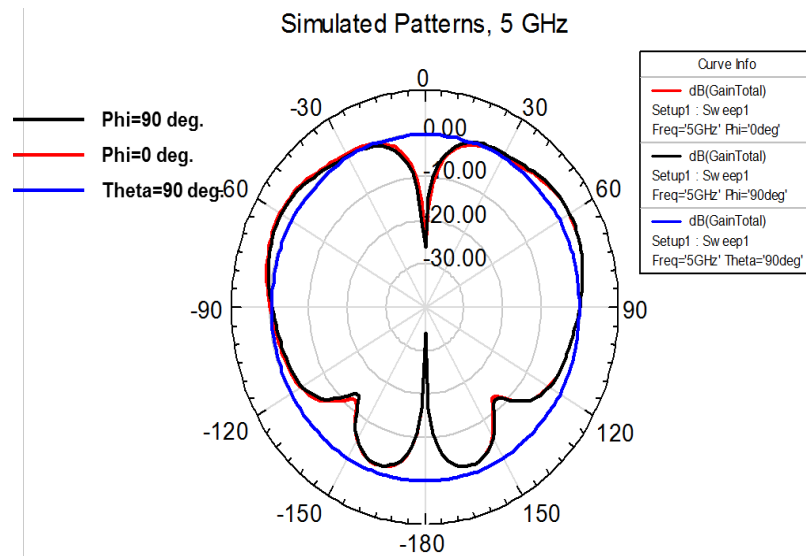
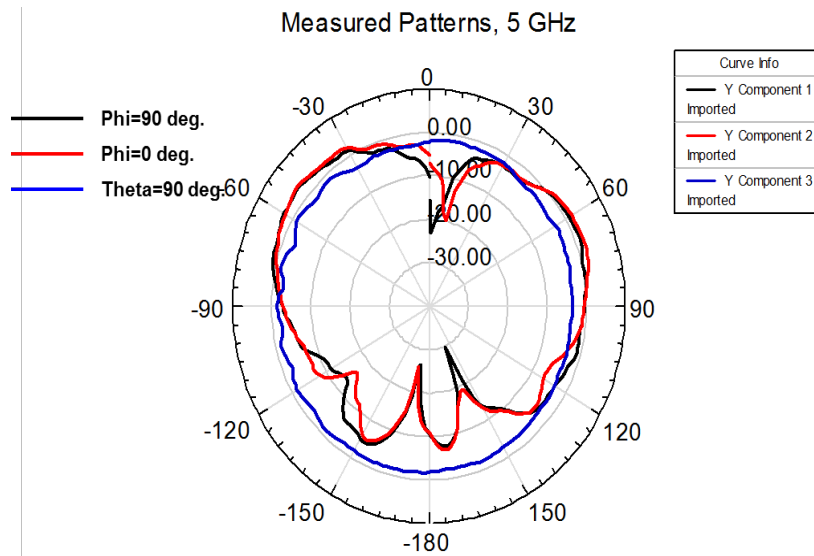


Figure B.3: Antenna radiation pattern in air and around the head model



(a) Simulated antenna patterns



(b) Measured antenna patterns

Figure B.4: Antenna radiation pattern at 5GHz - (a) Simulated, (b) Measured