Stress-Induced Delamination Of Through Silicon Via Structures

Suk-Kyu Ryu, Kuan-Hsun Lu, Jay Im, Rui Huang, and Paul S. Ho

Citation: AIP Conference Proceedings **1378**, 153 (2011); doi: 10.1063/1.3615702

View online: http://dx.doi.org/10.1063/1.3615702

View Table of Contents: http://scitation.aip.org/content/aip/proceeding/aipcp/1378?ver=pdfcov

Published by the AIP Publishing

Stress-Induced Delamination Of Through Silicon Via Structures

Suk-Kyu Ryu[a], Kuan-Hsun Lu[b], Jay Im[b], Rui Huang[a] and Paul S. Ho[b]

[a]*Department of Aerospace Engineering and Engineering Mechanics, University of Texas, Austin, TX 78712, USA*
[b]*Microelectronics Research Center, University of Texas, Austin, TX 78712, USA*

Abstract. Continuous scaling of on-chip wiring structures has brought significant challenges for materials and processes beyond the 32 nm technology node in microelectronics. Recently three-dimensional (3-D) integration with through-silicon-vias (TSVs) has emerged as an effective solution to meet the future interconnect requirement. Thermo-mechanical reliability is a key concern for the development of TSV structures used in die stacking as 3-D interconnects. This paper examines the effect of thermal stresses on interfacial reliability of TSV structures. First, the three-dimensional distribution of the thermal stress near the TSV and the wafer surface is analyzed. Using a linear superposition method, a semi-analytic solution is developed for a simplified structure consisting of a single TSV embedded in a silicon (Si) wafer. The solution is verified for relatively thick wafers by comparing to numerical results obtained by finite element analysis (FEA). Results from the stress analysis suggest interfacial delamination as a potential failure mechanism for the TSV structure. Analytical solutions for various TSV designs are then obtained for the steady-state energy release rate as an upper bound for the interfacial fracture driving force, while the effect of crack length is evaluated numerically by FEA. Based on these results, the effects of TSV designs and via material properties on the interfacial reliability are elucidated. Finally, potential failure mechanisms for TSV pop-up due to interfacial fracture are discussed.

Keywords: 3D interconnect, TSV, Thermo-mechanical reliability, FEA, Crack driving force

INTRODUCTION

Continuous scaling of microelectronic devices has brought serious challenges to the material and process development of on-chip interconnects beyond the 32 nm technology node [1]. The 3-D integration presents an effective solution as a system approach, which has generated significant interests recently to develop 3-D interconnects [2-4]. A critical structural element in the 3-D interconnects is the through-silicon via (TSV), which directly connects stacked structures die-to-die. Use of TSVs in 3-D integration can effectively improve system performance and reduce manufacturing costs [5-7].

The TSVs may assume various structural configurations such as fully filled TSV, annular TSV, TSV with 'nail head', and TSV with buffer layers (Fig. 1). Due to the mismatch in the coefficients of thermal expansion (CTEs) of the via materials and Si, thermal stresses are ubiquitously induced during processing and thermal cycling of TSV structures, which can degrade the performance of stress-sensitive devices around

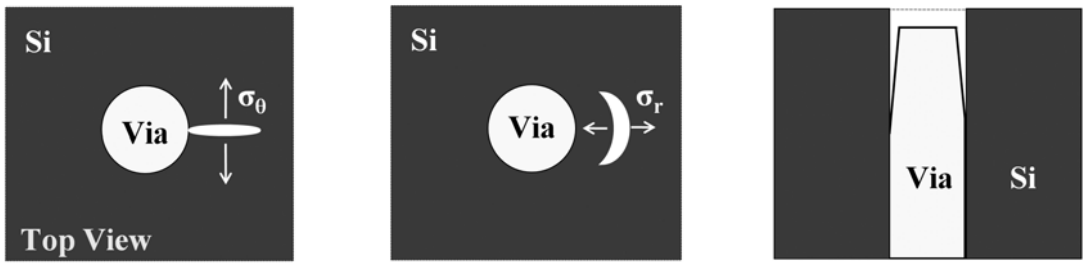
Stress Management for 3D ICs Using Through Silicon Vias
AIP Conf. Proc. 1378, 153-167 (2011); doi: 10.1063/1.3615702

the TSVs [8, 9] or drive various types of crack growth in 3-D interconnects [9-13] such as R- or C-crack on Si substrate, and interfacial crack (Fig. 2).

(a) Fully filled TSV (b) Annular TS

(c) TSV with a dielectric layer (d) TSV with a nail head

FIGURE 1. Schematics of through-silicon vias (TSVs) in various structural forms.



(a) R-Crack (b) C-Crack (c) Interfacial Crack

FIGURE 2. Schematics of various types of cracks near TSVs

The characteristics of the thermo-mechanical stresses developed in the system play a major role in controlling the structural reliability of the 3-D integrated structure. Finite element methods have been used to numerically analyze the thermo-mechanical stresses, which were found to depend on the materials, processes and structural designs of the 3-D integrated structures [9-13]. To assess the thermo-mechanical reliability of TSV structures, the driving forces for the growth of both cohesive and interfacial cracks were calculated based on the concepts of facture mechanics [12, 13]. In addition to these numerical studies, a simple analytical approach based on a two-dimensional (2-D) model was used to analyze the thermomechanical interactions in TSV arrays away from the wafer surface [14]. Here, the 2-D solution does not capture

the 3-D nature of the stress field near the wafer surface around a TSV. On the other hand, determination of the stresses near the wafer surface is critical due to the fact that the active devices are usually located there. A systematic understanding of the near-surface thermal stress distribution and its impact on TSV reliability has not been established.

In this paper, a semi-analytic 3-D solution is first developed for the near-surface stresses of an isolated TSV embedded in the silicon wafer (Fig. 1a). This compares closely with numerical results obtained by finite element analysis (FEA) for TSV structures with relatively thick wafers. We then focus on the interfacial reliability of TSV, for which an analytical solution is obtained for the steady-state energy release rate as an upper bound for the fracture driving force. Based on these results, the effects of the TSV designs and materials on interfacial reliability are investigated.

THREE-DIMENSIONAL STRESS ANALYSIS

Consider a single TSV embedded in an infinite Si wafer (Fig. 1a). The stress field induced by differential thermal expansion in the via and Si is three-dimensional in nature. As a prerequisite for the study of stress-related phenomena, we assume in the present study that all materials are isotropic and linear elastic. Under the assumption of linear elasticity, the stress field in the TSV structure can be obtained by superposition of the two problems sketched in Fig. 3. In Problem A, the system is subjected to a thermal loading (ΔT) and a uniform stress (σ_z) on the surfaces of the via, where the stress field is homogeneous in the via. The exact solution to Problem A in Fig. 3 is identical to the 2-D plane-strain solution to the classical Lame problem [15]. The 2-D solution does not satisfy the traction-free boundary condition on the surfaces in the original problem (Fig. 1a) because of the presence of the axial stress (σ_z^A) in the via. To recover the traction-free boundary condition, the normal stress on the surface is removed by superimposing Problem B, in which the via is subjected to a pressure of the same magnitude ($p = \sigma_z$) at both ends, but no thermal load [16]. The stress field due to the surface pressure is typically localized near the ends of the via. Thus, the stress distribution from the 2-D solution is an accurate solution far away from the TSV ends, especially for high aspect-ratio (height/diameter, H/D_f) TSVs embedded in a thick wafer. However, the correction due to Problem B renders a very different stress distribution near the wafer surface around the TSV. For a relatively thin wafer, the stress in the entire via and its surrounding can be affected and thus comes out different from the 2-D solution. This can impact the near-surface thermal stress distribution and the device characteristics surrounding the TSV.

Problem A can be solved analytically, while an approximate solution to Problem B can be obtained semi-analytically. The thermal stress in the via is uniform and tri-axial. The detailed solutions can be found in our previous research [17].

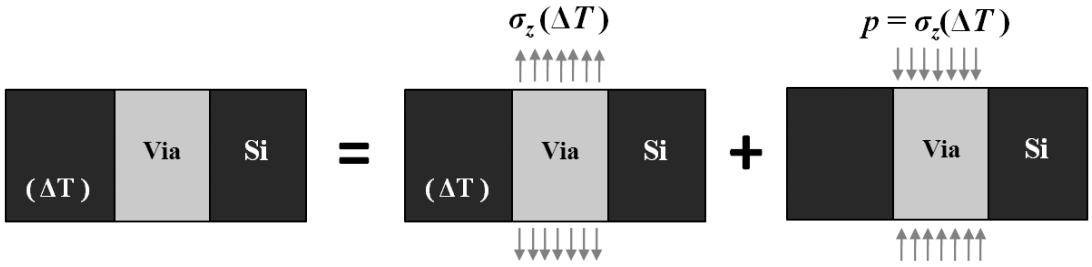
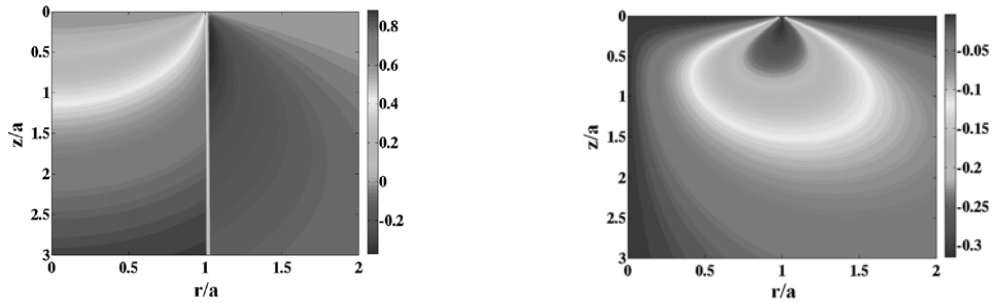
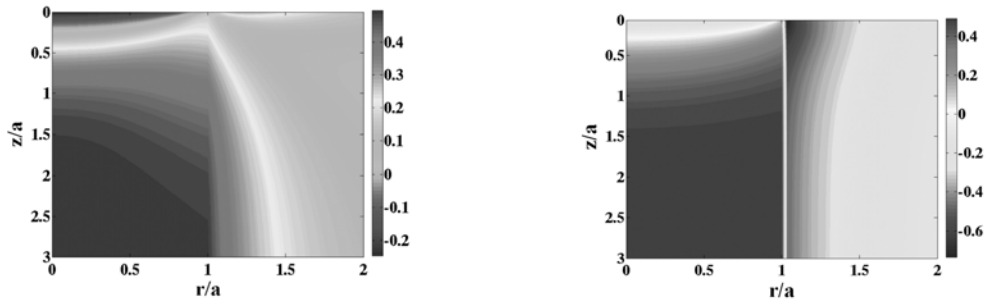


FIGURE 3. Illustration of the method of superposition to obtain the semi-analytical solution for the thermal stresses in a TSV structure: (a) the original problem, with a thermal load and traction-free surfaces; (b) Problem A, with a thermal load; (c) Problem B, with surface load only.

Figure 4 shows distribution of various stresses in the model structure for the negative thermal load, $\Delta T = -250$ ºC. Figure 4a shows that the normal stress σ_z is zero on the surface ($z = 0$), as required by the traction-free boundary condition. The normal stress is non-uniform in the via and Si near the surface. Unlike the 2-D solution, the shear stress (σ_{zr}) is not zero near the end of the via (Fig. 4b). In fact, a concentration of the shear stress is predicted at the junction between the surface ($z = 0$) and via/Si interface ($r = D_f / 2$), which can contribute to the driving force to cause interfacial delamination. The distributions of the radial stress (σ_r) and the circumferential stress (σ_θ) near the end of TSV (Figs. 4c and 4d) are also very different from the 2-D solution. Depending on the sign of the thermal mismatch strain, $\varepsilon_T = (\alpha_f - \alpha_m)\Delta T$, the stresses can be either tensile or compressive where the subscripts *f* and *m* refer to the TSV and Si, respectively. For example, if $\alpha_f > \alpha_m$, $\varepsilon_T > 0$ for heating ($\Delta T > 0$) and $\varepsilon_T < 0$ for cooling ($\Delta T < 0$). For the case of cooling, the radial stress is tensile along the via/Si interface, which can contribute to the driving force for interfacial delamination. The radial stress is also tensile in Si near the surface, which may cause circumferential cracking (C-cracks, Fig. 2b) of the Si. During heating, the circumferential stress is tensile in Si, which may cause radial cracks (R-cracks, Fig.1a) to form in Si. For both heating and cooling, the presence of the shear stress (σ_{rz}) along the TSV/Si interface can induce interfacial failure by delamination. In the present study we focus on interfacial delamination as the critical failure mode under both heating and cooling conditions.



(a) Axial stress (σ_z) (b) Shear stress (σ_{rz})

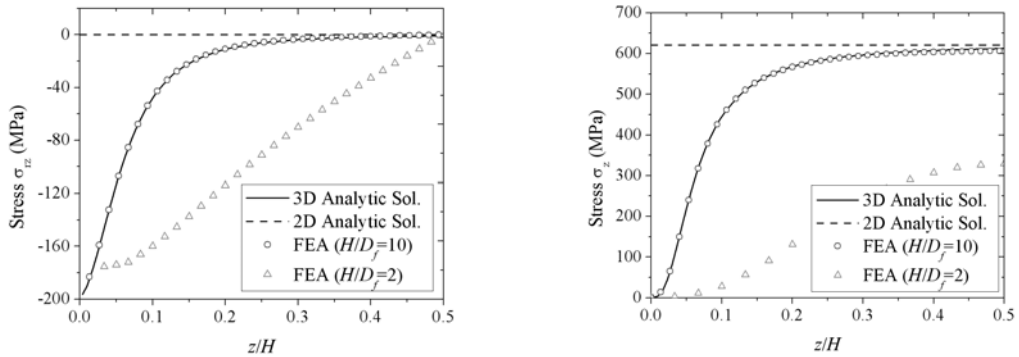


(c) Radial stress (σ_r) (d) Circumferential stress (σ_θ)

FIGURE 4. Near-surface stress distributions predicted by the semi-analytical solution for thermal load, $\Delta T = -250$ ºC. The stress magnitudes are normalized by $p = -E\varepsilon_T/(1-\nu)$.

To verify the semi-analytic solution developed, finite element analysis (FEA) is performed using the commercial package, ABAQUS (v6.8). Since the thickness of the Si wafer is one of the key design parameters for the TSV structure, the effect of wafer thickness on thermal stress distribution is examined by FEA models with two different thicknesses. The model structure is shown in Fig. 1a, with the TSV diameter $D_f = 30$ μm and the wafer thickness H=300 μm and 60 μm. A negative thermal loading (cooling), $\Delta T = -250$ ºC, is assumed. The material properties are: $E_f = E_m = 110$ GPa, $\nu_f = \nu_m = 0.35$, and $\alpha_f = 17$ ppm/ºC and $\alpha_m = 2.3$ ppm/ ºC. The model is an approximation to a Cu TSV in Si, neglecting the elastic mismatch between Cu and Si. In practice a thin barrier layer is typically placed between the Cu via and Si, which has minimal effects on the stress distribution and is thus ignored here.

In Figure 5, the results from the FEA are compared with those obtained by the semi-analytical solution. First, the axial stress (σ_z) along the center line of the TSV (r = 0) shows a transition from zero stress at the surface (z = 0) to a tensile stress away from the surface (Fig. 5a). For the thick wafer ($H/D_f = 10$), the FEA result shows excellent agreement with the analytical solution, both approaching the 2-D solution (the dashed line) away from the surface. Similarly, the radial stress (σ_r) at the interface approaches a finite value at z = 0 and the 2-D solution far away from the surface (Fig. 5b).



(a) σ_z at the via center $(r = 0)$ (b) σ_r at the TSV/Si interface $(r = D_f/2)$

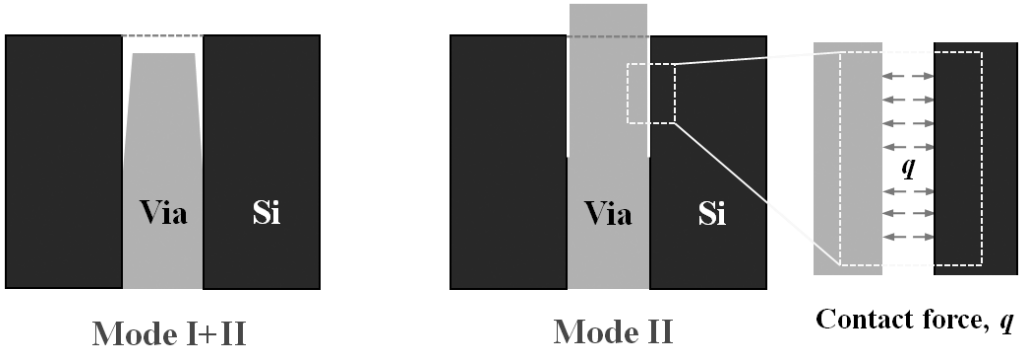
FIGURE 5. Effect of wafer thickness on stress distributions ($D_f = 30$ μm, $\Delta T = -250$ ºC).

It is important to recognize the variation of the near-surface stresses in the *z*-direction. Since the Raman measurement typically averages over certain depth from the surface, the present results with distinct 3D characteristics for the surface stresses will have to be taken into account in analyzing the Raman data. In addition, channeling cracks may grow at the Si surface near the TSV in either the radial or the circumferential direction, depending on the magnitudes and signs of the stresses. Understanding the characteristics of the near-surface stresses in Si is essential for the determination of a keep-out zone [9, 14] around the TSV to mitigate the impact of stresses on device performance.

THE ANALYSIS OF INTERFACIAL DELAMINATION FOR VARIOUS STRUCTURAL DESIGNS AND MATERIALS

Fully Filled TSV

The stress analysis in the previous section suggests a potential failure mechanism of the TSV structure due to interfacial delamination. Figure 6 depicts two modes of interfacial delamination for a fully-filled TSV structure. With a negative thermal load ($\Delta T < 0$), the radial stress along the via/Si interface is tensile (assuming $\alpha_f > \alpha_m$). Consequently, the interfacial delamination crack may grow in a mixed mode (peeling and shearing). With a positive thermal load ($\Delta T > 0$), however, the radial stress is compressive which does not contribute to the driving force for delamination. This results in an interfacial crack with a pure shearing mode (mode II). In this case, the two crack faces are in intimate contact and may be subject to friction. For simplicity, we assume a frictionless contact in the present study and develop analytical solutions for the steady-state energy release rates of the interfacial crack, under both cooling and heating conditions. The analytical solutions are then compared to finite element analysis, which is extended to study the effects of crack length and wafer thickness on the fracture driving force.



(a) Cooling ($\Delta T < 0$) (b) Heating ($\Delta T > 0$)

FIGURE 6. Schematics of interfacial delamination of TSV under cooling and heating conditions.

For a TSV with a relatively high aspect ratio (H / D_f), the energy release rate for interfacial delamination reaches a steady state when the crack length is several times greater than the via diameter. Since the energy release rate is usually lower for shorter cracks, the steady-state value sets an upper bound for the fracture driving force, which may be used as the critical condition for conservative design of reliable TSV structures.

Consider an infinitely long fiber (TSV) in an infinite matrix (Si wafer), with a semi-infinite, circumferential crack along the interface and subjected to a thermal load ΔT. The steady-state energy release rate (ERR) for the interfacial crack growth (per unit area) is obtained by comparing the elastic strain energy far ahead of the crack front and that far behind the crack front. While the stress field near the crack front is complicated with singularity and 3D distribution, it translates in a steady state as the crack front advances. Far ahead of the crack front, the stress field can be obtained analytically by solving the 2D plane-strain problem (Problem A in Fig. 3). Far behind the crack front, since the TSV is debonded from Si, the stress is relaxed in both the via and Si. For the case of cooling ($\Delta T < 0$), the stress is zero in both TSV and Si. For heating ($\Delta T > 0$), however, the contact between the crack faces induces a stress field similar to Problem A, but the axial stress (σ_z) in the via is zero under the assumption of frictionless contact. If the elastic mismatch is neglected (i.e., $\alpha = 0$ and $\nu_f = \nu_m = \nu$), the steady state energy release rate can be expressed in a simple form:

$$G_{cooling}^{SS} = \frac{E\varepsilon_T^2 D_f}{4(1-\nu)}. \tag{1}$$

Under heating with $\Delta T > 0$, due to the contact of the crack faces (Fig. 6b), the stress state in the TSV far behind the crack front is equibiaxial. As a result, the steady state ERR under heating can be obtained by neglecting the elastic mismatch, namely

$$G_{heating}^{SS} = \frac{1+\nu}{8(1-\nu)} E\varepsilon_T^2 D_f . \tag{2}$$

To verify the steady state ERR solution, a FEA model of the TSV structure is constructed, and the energy release rates are calculated by the method of J-integral. As expected, the energy release rate increases with the crack length and approaches the steady-state solution when the crack length is about 2-3 times the via diameter (Fig. 7).

Several interesting results can be deduced based on the analytical solutions for the steady-state energy release rates. First, the steady-state ERR for interfacial delamination is linearly proportional to the TSV diameter, which may set an upper bound for the via diameter in order to avoid delamination. Second, the ERR is proportional to the square of the thermal mismatch strain, $\varepsilon_T = (\alpha_f - \alpha_m)\Delta T$. Thus the delamination driving force can be reduced by either using TSV materials with smaller

thermal expansion mismatch ($\alpha_f - \alpha_m$) and/or by reducing the thermal loads (ΔT). Third, the energy release rate for interfacial delamination increases with the elastic modulus of the TSV material, however, the effect is less important than the effect of the thermal expansion mismatch. Finally, a comparison between Eq. (1) and (2) indicates that, with the same thermal load ΔT, the driving force for interfacial delamination under cooling is about twice that under heating, a result that can be attributed to the presence of a tensile radial stress (σ_r) across the interface (opening mode) for the case of cooling.

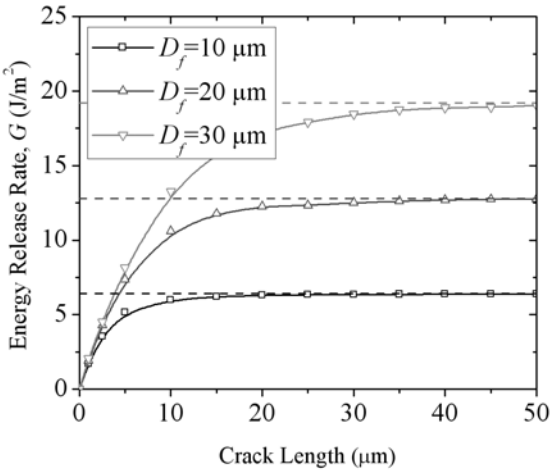


FIGURE 7. Effect of crack length on the energy release rate for interfacial delamination of TSVs (H = 300 μm and $\Delta T = -250$ ºC).

Several metals including aluminum (Al), nickel (Ni), and tungsten (W) have been considered to replace Cu as alternative materials for TSVs. The effect of materials on interfacial fracture driving force for the fully filled TSVs is evaluated using the thermo-mechanical properties listed in Table I.

TABLE 1. Thermomechanical properties of the TSV materials used in the present study.

Material	*CTE (ppm/°C)*	*Young's Modulus (GPa)*	*Poisson's ratio (v)*
Si	2.3	130	0.28
Cu	17	110	0.35
Al	20	70	0.35
Ni	13	207	0.31
W	4.4	400	0.28
BCB	40	3.0	0.34

The steady-state energy release rates, *Gss,* for the four TSV materials are compared in Fig. 8 under both cooling ($\Delta T = -250$ ºC) and heating ($\Delta T = 250$ ºC) conditions, for the same TSV diameter of 30 microns. Compared to Cu, Al has a lower Young's modulus but a larger mismatch in CTE with Si. This results in a driving force for interfacial delamination higher for Al under the same thermal load. In contrast, Ni has a higher Young's modulus than Cu but a lower thermal mismatch, resulting in a lower driving force for delamination. Despite the highest Young's modulus, W has a very

small CTE mismatch with Si, and thus the delamination driving force is significantly lower than that for the Cu TSV. This renders W a particular attractive metal for TSV applications from the interfacial reliability perspective.

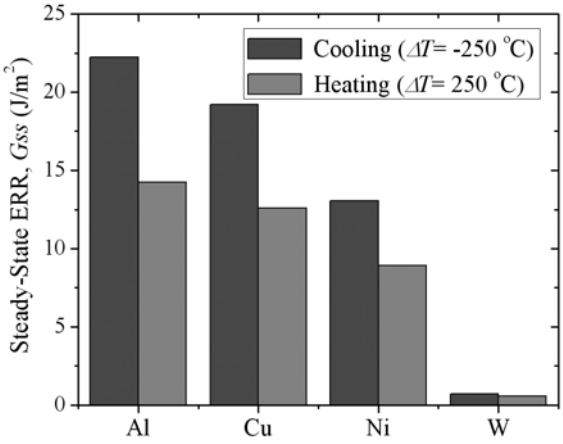


FIGURE 8. Comparison of the steady-state energy release rates for interfacial delamination in TSV structures of different materials, under the same thermal load for cooling and heating ($D_f = 30\,\mu\text{m}$).

To evaluate the material effect on the TSV reliability, other factors have to be considered in addition to the fracture driving force. These include the processing temperature for the specific metal, the TSV diameter and the interfacial adhesion energy. Since different TSV materials may require processes with different thermal loads, this can affect the delamination driving force, which is proportional to the square of the thermal mismatch strain. Among the four metals considered here, the CVD process for W deposition has the highest temperature at around 400˚C, and thus the highest thermal load. This has to be balanced by the use of relatively small diameters for the W TSV. For each material, the ERR has to be compared with the interfacial adhesion energy, i.e., $G(a_c) = \Gamma$, to determine a critical crack length (a_c), beyond which the delamination crack grows unstably. The interfacial adhesion varies with the TSV material and can be enhanced by using thin adhesive barrier layers between the TSV and Si [18]. In addition, plastic deformation of the TSV metals has not been considered in the present study. Plastic yielding could partly relax the thermal stress in the via and the Si, thus reducing the fracture driving force. Moreover, the energy dissipation during plastic deformation could contribute to the overall fracture energy [19]. Therefore, the interfacial reliability may be improved by plasticity in the via. However, plastic deformation is irrecoverable and could lead to other reliability issues such as dislocations, stress voiding and fatigue. Further studies are required to understand the effect of plasticity on thermo-mechanical reliability of TSVs.

Annular TSV

The annular TSV structure (Fig. 1b) is an attractive solution to reduce the impact of the thermal mismatch on interfacial reliability by means of reducing the metal volume.

With a traction-free boundary condition on the inner surface of the annular TSV, the stress distribution in the via becomes non-uniform, different from that in a fully filled circular TSV. The effect of the diameter ratio of the annular TSV ($\eta = D_i / D_f$) on the steady-state energy release rate is shown in Figure 9 for Al, Cu, Ni, and W TSVs with the same outer diameter ($D_f = 30\,\mu\text{m}$) and the same thermal loading ($\Delta T = -250$ ºC), where D_i represents the inner diameter of the annular TSV, and $\eta = D_i / D_f$ is the diameter ratio.

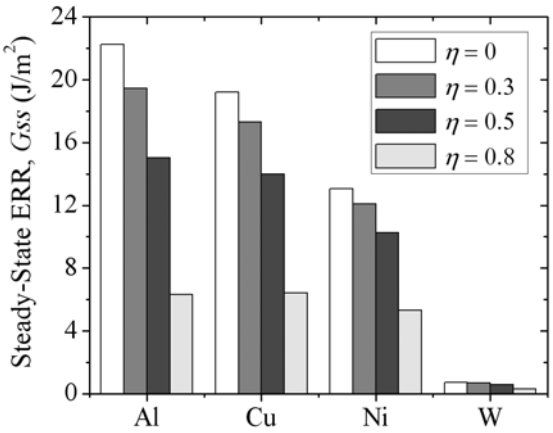


FIGURE 9. Effect of TSV materials for annular TSV on ERR ($D_f = 30\,\mu m$, $\Delta T = -250\,^{o}C$)

Clearly, the driving force for interfacial fracture decreases with increasing diameter ratio (η), suggesting improved interfacial reliability for the annular TSVs relative to the fully filled circular TSVs ($\eta = 0$) under the same thermal loading. A similar result can be obtained for the steady-state energy release rate under heating condition ($\Delta T > 0$), which is typically lower than that under cooling.

TSV with dielectric buffer layers

The study so far has considered a simplified structure with a single TSV embedded in Si. In practice, a thin barrier layer and/or a dielectric buffer layer may be needed between the TSV and Si. For example, to fabricate Cu TSVs, a dielectric or a nitride barrier layer is typically deposited on the via sidewall before Cu electroplating. The dielectric layer, which is often made of silicon dioxide with 1~2 μm thickness, provides a barrier for the silicon substrate against Cu diffusion. Similar to the Cu damascene interconnects, the barrier layer is usually made of metallic materials such as Ti, Ta, and their respective nitrides, TiN and TaN, with a thickness less than 0.1 μm [20-22]. FEA was performed and found that the relatively thin barrier layer has little effect on the thermal stresses and the interfacial fracture driving force, but it may play an important role by enhancing the interfacial adhesion [23]. With a thicker dielectric buffer layer it could serve as a stress buffer to reduce the thermal expansion mismatch between the TSV and Si, thus reducing the thermal stress and the fracture driving force. For this purpose, polymeric materials such as Parylene and BCB

(Benzocyclobutene) have been used to replace the oxide layer [24, 25]. By using a 2~5 μm thick polymer buffer layer, the thermal stress in the TSV structure can be considerably reduced [13] while its electrical performance can be improved by reducing the capacitive coupling [25].

As an example, we consider a Cu-TSV of 30 μm diameter with a 5 μm BCB buffer layer (Fig. 1c). Figure 10 plots the steady-state energy release rates versus the crack length for delamination along the two interfaces, in comparison to the Cu/Si interface without the buffer layer. The energy release rates for all four interfaces considered are consistently lower than the Cu/Si interface of fully filled TSV (19 J/m^2).

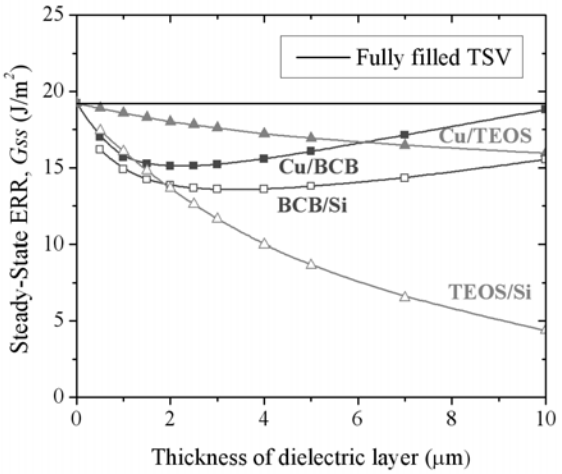


FIGURE 10. Effect of dielectric layer thickness and material property on *Gss, w*here filled symbol represents *Gss* at the first interface and unfilled symbol is for *Gss* at the second interface. The dash line represents the ERR for the Cu/Si interface in a fully filled TSV. ($D_f = 30\,\mu m$, $\Delta T = -250\,^oC$).

Whether these levels of driving forces in Fig. 10 are sufficient to cause delamination depends on the adhesion strength of the particular interfaces. For example, previous measurements of adhesion on flat films [26] have reported 12.2 J/m^2 for the Cu/BCB interface and over 24 J/m^2 for the Si/BCB interface. Therefore, the Cu/BCB interface is deemed more vulnerable to delamination than the Si/BCB interface in the TSV configuration.

TSV with a Nail Head

In practice, a hard mask for etching Cu TSVs in silicon substrate often results in a ledge or overhang called 'nail head' over the TSV (Fig. 1d). Or the nail head could be allocated to facilitate connection to the upper die on purpose. The presence of the nail head changes the boundary conditions at the crossing point of Cu/Si/Nail head and interfacial end of Si/Nail head, which in turn affects the stress distribution around both the TSV and Si. In particular, under negative thermal loading ($\Delta T = -250\,^oC$), the concentration of the shear stress along the TSV/Si and nail head/Si is increased due to the constraint exerted by the nail head. In addition, the opening stress at the end of the nail head/Si interface possesses singularity. As a result, the concentration of stresses contributes to interfacial failures. Before discussing further about interfacial failure,

the steady-state energy release rate for the TSV structure with nail head under a cooling condition was calculated. For the analytic inducement, the dimensions of thickness and diameter for nail head simply were assumed sufficiently large. The relevance of the assumption was verified by the comparison with FEA. The radial and circumferential stresses far behind the crack tip are zero, while the out-of plane stress exists due to the constraint by the nail head.

For the effect of nail head on energy release rate, we compared ERR between fully filled TSV ($D_f = 30\,\mu\text{m}$) and TSV with a nail head ($H_n = 0.5D_f$) under cooling ($\Delta T = -250$ ºC). Cooling condition contributes to failure of only the vertical surface, so that we varied vertical crack length (c_1) with zero horizontal crack ($c_2 = 0$). As crack propagates along the vertical interface, the ERR approaches the steady-state solution. The steady-state ERR for TSV with a nail head drops about 30% due to the constraint effect of the nail head (Fig. 11). In conclusion, the nail head can be helpful to improve the TSV reliability.

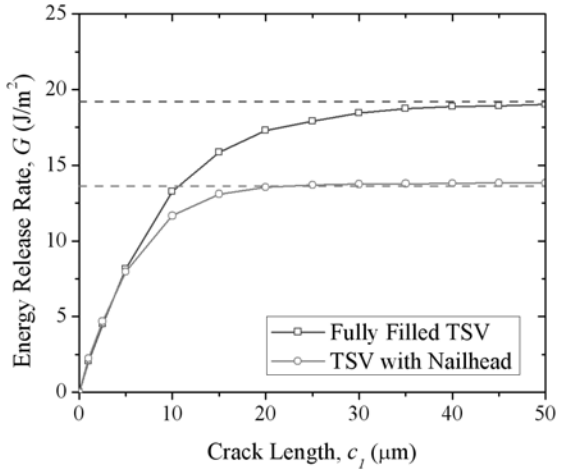


FIGURE 11. Comparison of steady-state ERRs between a fully filled TSV and a TSV with nail head ($D_f = 30\mu\text{m}$, $H_n = 0.5D_f$, $c_2 = 0$, and $\Delta T = -250$ ºC).

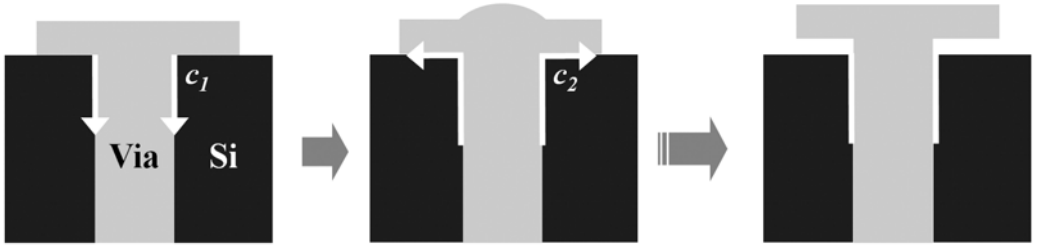
THE DISCUSSION ON TSV POP-UP

TSV pop-up describes a phenomenon of TSV lifting off from the surrounding matrix as schematically depicted in Fig. 12. The interface between the nail head and Si is subjected to shearing near the edge of the nail head, which may cause delamination at that location. Therefore, analysis of the interfacial reliability of TSVs with nail head should consider both interfaces, vertical and horizontal. If both interfaces fail during thermal cycling, TSV can be extruded from the Si substrate. Here, we will describe two scenarios for thermal processing to cause TSV pop-up.

First, by comparing the energy release rates under cooling and heating, we observe that the interface is more prone to delamination under cooling than under heating. During cooling, a vertical crack (c_1) initiated at the TSV/Si interface can reach a stationary crack through repeated thermal cycles. Then, during the ensuing heating

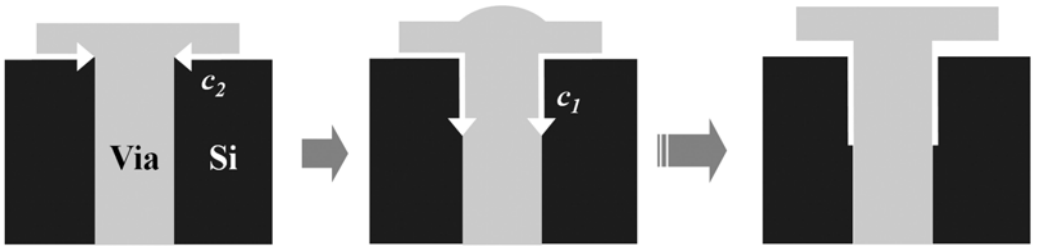
cycling, a horizontal crack (c_2) can be generated at the Si/nail head interface from inside toward the outside of the nail head (Fig. 12a). Finally, the delamination at both interfaces can bring about TSV pop-up. Alternately, after vertical crack failure, horizontal crack could start from outside toward the inside of the nail head. However, the ERR for this failure mode is relatively small, i.e. below 1 J/m^2. Thus, we rule out this possibility from consideration.

Another possibility for TSV pop-up comes from the concentration of opening and shearing stress under cooling (Fig. 12b). The driving force can cause initial crack growth at the free end of the nail head/Si interface, followed by the interfacial crack expanding inward due to the positive opening stress. Then, after fully debonded at the nail head/Si interface, a vertical crack propagates along the TSV/Si interface under an ERR corresponding to that of the fully filled TSV.



(i) Cooling (ii) Heating (iii) TSV pop-up (Heating)

(a) A first scenario for TSV pop-up



(i) Cooling (ii) Cooling (iii) TSV pop-up (Heating)

(b) A second scenario for TSV pop-up

FIGURE 12. Two scenarios for TSV pop-up

CONCLUSIONS

In the present study, the thermo-mechanical reliability in a TSV structure is investigated by a semi-analytical approach and FEA calculations. The stress characteristics are inherently 3D in nature with the near-surface stress distributions distinctly different from the analytical solution based on a simple 2D model. The energy release rate for interfacial delamination of TSV is evaluated under both cooling and heating conditions, using an analytical solution for a steady-state crack growth and numerical solutions by FEA models. Based on these results, the effects of TSV

designs and via material properties on the interfacial reliability are elucidated. Finally, several mechanisms for TSV pop-up are discussed. Together, the potential of materials and structure optimization for improving TSV reliability is envisaged as the key for the development of 3D interconnects.

ACKNOWLEDGMENTS

The authors gratefully acknowledge Semiconductor Research Corporation for the financial support of this work.

REFERENCES

1. International Technology Roadmap for Semiconductors (ITRS), 2009.
2. M.S. Bakir and J.D. Meindl, Integrated interconnect technologies for 3D nanoelectronic systems. Artech House, Norwood, MA, 2009.
3. J.U. Knickerbocker, P.S. Andry, B. Dang, R.R. Horton, M.J. Interrante, C.S. Patel, R.J. Polastre, K. Sakuma, R. Sirdeshmukh, E.J. Sprogis, S.M. Sri-Jayantha, A.M. Stephens, A.W. Topol, C.K. Tsang, B.C. Webb and S.L. Wright, Three-dimensional silicon integration, IBM J. Res. & Dev. 52, 553-569 (2008).
4. J. Lu, 3-D hyperintegration and packaging technologies for micro-nano systems, Proc. IEEE 97, 18-30 (2009).
5. L.W. Schaper, S.L. Burkett, S. Spiesshoefer, G.V. Vangara, Z. Rahman and S. Polamreddy, Architectural implications and process development of 3-D VLSI Z-axis interconnects using through silicon vias, IEEE Trans. Advanced Packaging 28, 356-366 (2005).
6. K. Sakuma, P.S. Andry, C.K. Tsang, S.L. Wright, B. Dang, C.S. Patel, B.C. Webb, J. Maria, E.J. Sprogis, S.K. Kang, R.J. Polastre, R.R. Horton and J.U. Knickerbocker, 3D chip-stacking technology with through-silicon vias and low-volume leadfree interconnections, IBM J. RES. & DEV. 52, 611-622 (2008).
7. K. Sakumar, N. Nagai, M. Saito, J. Mizuno and S. Shoji, Simplified 20-μm pitch vertical interconnection process for 3D chip stacking, IEEJ Trans. on Electrical and Electronic Engineering 4 , 339-344 (2009).
8. S. Thompson, G. Sun, Y. Choi and T. Nishida, Uniaxial-Process-Induced Strained-Si: Extending the CMOS Roadmap, IEEE Trans. On Electron Devices 53, 1010-1020 (2006).
9. A.P. Karmarker, X. Xu and V. Moroz, Performance and reliability analysis of 3D-integration structures employing through silicon via (TSV), Proc. IEEE 47th Annual International Reliability Physics Symposium, Montreal, 2009, pp. 682-687.
10. C.S. Selvanayagam, J.H. Lau, X. Zhang, S.K.W. Seah, K. Vaidyanathan and T.C. Chai, Nonlinear thermal stress/strain analyses of copper filled TSV (Through Silicon Via) and their flip-chip microbumps, Electronic Components and Technology Conference, 2008, pp. 1073-1081.
11. N. Ranganathan, K. Prasad, N. Balasubramanian and K.L. Pey, A study of thermo-mechanical stress and its impact on through-silicon vias, J. Micromech. Microeng. 18, 1-13 (2008).
12. X. Liu, Q. Chen, P. Dixit, R. Chatterjee, R. Tummala and S. Sitaraman, Failure mechanisms and optimum design for electroplated copper through-silicon vias (TSV), Electronic Components and Technology Conference, 2009, pp. 624-629.
13. K. Lu, X. Zhang, S. Ryu, J. Im, R. Huang and P. Ho, Thermo-mechanical reliability of 3-D ICs containing through-silicon-vias, Electronic Components and Technology Conference, 2009, pp. 630-634.
14. K. Lu, X. Zhang, S. Ryu, R. Huang and P. Ho, Thermal stresses analysis of 3-D interconnect, 10th International Workshop on Stress-Induced Phenomena in metallization, Proc. American Institute of Physics Conference 1143, 2009, pp. 224-230.
15. A.E.H. Love, The stress produced in a semi-infinite solid by pressure on part of the boundary, Philos. Trans. A 228, 377-420 (1929).

16. T.C. Lu, J. Yang, Z. Suo, A.G. Evans, R. Hecht and R.Mehrabian, Matrix cracking in intermetallic composites caused by thermal expansion mismatch, ACTA Metall. Mater. 39, 1883-1890 (1991).
17. S. Ryu, K. Lu, X. Zhang, J. Im, P. Ho and R. Huang, IEEE Trans. TDMR, 2010.DOI:10.1109/TDMR.2010.2068572.
18. M.W. Lane, R.H. Dauskardt, N. Krishna and I. Hashim, Adhesion and reliability of copper interconnects with Ta and TaN barrier layers, J. Mater. Res. 15, 203-211 (2000).
19. M. Lane, A. Vainchtein, H. Gao and R.H. Dauskardt, Plasticity contributions to interface adhesion in thin-film interconnect structures, J. Mater. Res. 15, 2758-2769 (2000).
20. O. Luhn, C.V. Hoof, W. Ruythooren and J. Celis, Barrier and seed layer coverage in 3D structures with different aspect ratios using sputtering and ALD processes, Microelectronic Engineering 85, 1947-1951 (2008).
21. G. Druais, G. Dilliway, P. Fischer, E. Guidotti, A. Radisic and S. Zahraoui, High aspect ratio via metallization for 3D integration using CVD TiN barrier and electrografted Cu seed, Microelectronic Engineering 85, 1957-1961 (2008).
22. S. Lee, R. Hon, S. Zhang and C. Wong, 3D stacked flip chip packaging with through silicon vias and copper plating or conductive adhesive filling, Electronic Components and Technology Conference, 2005, pp. 795-801.
23. M.W. Lane, R.H. Dauskardt, N. Krishna and I. Hashim, "Adhesion and reliability of copper interconnects with Ta and TaN barrier layers", J. Mater. Res. 15, 203-211 (2000).
24. B. Majeed, N. Pham, D. Tezcan and E. Beyne, Parylene N as a dielectric material for through silicon vias, Electronic Components and Technology Conference, 2008, pp. 1556-1561.
25. D. Tezcan, F. Duval, H. Philipsen, O. Luhn, P. Soussan and B. Swinnen, Scalable Through Silicon Via with polymer deep trench isolation for 3D wafer level packaging, Electronic Components and Technology Conference, 2009, pp. 1159-1164.
26. J. Im, E.O. II, J. Theodore Stokich, A. Strandjord, J. Hetzner, J. Curphy and C. Karas, On the mechanical reliability of photo-BCB-based thin film dielectric polymer for electronic packaging applications, J. Electronic Packaging 122, 28-33 (2000).