Generation of Spin Currents for Spintronic Logic Applications

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Dedication

This dissertation is dedicated to my family and friends, especially my husband, whose support helped my dreams become a reality.

Abstract

Current complementary metal oxide semiconductor (CMOS) technologies currently suffer drawbacks such as increased power consumption and device variability with scaling as well as volatility. In order to further advance computation technologies in the future, new and alternative devices are being explored to overcome these limitations. One promising approach is spintronic devices in which information is stored and computed based on the spin of electrons rather than the absence or presence of charge such as in CMOS. Spintronics offers many possible benefits including fast operational speed, low power consumption, and nonvolatility. This dissertation explores methods of generating spin polarized currents for the operation of logic devices and the fabrication of these devices for logic applications.

The first device explored is a non-local lateral spin valve which can be used to generate a pure spin current and is the basic building block for the concept of all-spin logic. A unique top-down fabrication approach for lateral spin valves is created and demonstrated. Sub 100nm Co nanopillar devices are fabricated on a Cu channel using a top down approach that allows the entire material stack to be deposited initially under vacuum as opposed to devices fabricated using shadow beam lithography or lift-off techniques for ferromagnetic strips. A non-local signal is measured in these devices which indicates the top-down approach can successfully be used for integration of these devices. This demonstration is essential for these devices to be successfully implemented and scaled in computer applications at the industrial level.

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In the second part of the dissertation, my research on spin Hall effect devices and the application of these devices for a spin Hall majority gate logic device are presented. The spin Hall effect is explored in bulk perpendicular TbFeCo/Ta devices which lays the groundwork for the following experiments. Then, a composite spin Hall structure is developed in order to switch perpendicular magnetization using the spin Hall effect without the need for an externally applied field. To demonstrate the ability to tune the material properties of a spin Hall channel, studies are also presented on a variety of multilayer spin Hall devices. Last, a three-input MTJ device is proposed for a spin orbit torque combined with spin transfer torque majority gate. Three MTJ devices are fabricated on Ta and three distinct switching states are shown corresponding to switching of the individual input elements. Additionally, simulation work is presented to verify the concept of the majority gate.

Table of Contents

List of Tables .... **VIII**

List of Figures .... **IX**

Chapter 1 Introduction **1**

1.1 Motivation for Beyond CMOS Technology 1
1.2 Overview of Spintronic Based Logic 4
1.3 Dissertation Overview 9

Chapter 2 Introduction to Spintronics **11**

2.1 Giant Magnetoresistance 11
2.2 Tunneling Magnetoresistance 12
2.3 Spin Transfer Torque 14
2.4 Spin Injection, Accumulation, and Detection in Nonlocal Lateral Spin Valves 18
2.5 Spin Orbit Interactions 21

Chapter 3 Nonlocal Spin Valves for All-Spin Logic Applications **25**

3.1 Introduction 25
3.2 All-Spin Logic Device 28
3.2.1 Device Proposal and Benchmarking *29*
3.2.2 Fabrication Requirements for All-Spin Logic *32*
3.3 Development of a Top-Down Approach for Non-Local Lateral Spin Valves 34
3.3.1 Overview *34*
3.3.2 Film Preparation *34*
3.3.3 Defining the Channel *38*
3.3.4 Defining the Magnetic Pillars *38*
3.3.5 Via Formation *39*
3.4 Electrical Characterization 42
3.4.1 Electrical Characterization Techniques *42*
3.4.2 Results and Discussion *43*
3.5 Summary 45

Chapter 4 Spin Hall Effect **47**

4.1 Introduction 47
4.1.1 Spin Hall Effect Background and Motivation *47*
4.1.2 Motivation for Spin Hall Effect Logic and Memory Devices *48*
4.2 Spin Hall effect in Bulk Perpendicular Ta/TbFeCo Bilayers 52
4.2.1 Motivation *52*
4.2.2 Film Preparation and Device Fabrication *54*
4.2.3 Electrical Characterization Techniques *57*
4.2.4 Results and Discussion *57*
4.3 Composite Spin Hall Multilayer Design for External Field Free Switching of Perpendicular Magnetization 62
4.3.1 Introduction and Motivation *62*
4.3.2 Composite Structure Development and Magnetic Properties *65*
4.3.3 Device Fabrication and Electrical Characterization *67*
4.3.4 Results and Discussion *69*

4.3.5 Summary *73*
4.4 TA/W MULTILAYERS FOR MATERIAL ENGINEERING SPIN ORBIT CHANNELS 74
4.4.1 Introduction *74*
4.4.2 Material Stack Preparation and Device Fabrication *75*
4.4.3 Summary *83*
4.5 SPIN HALL ASSISTED SPIN TORQUE MAJORITY GATE 83
4.5.1 Introduction and Motivation *83*
4.5.2 Spin Hall Magnetic Tunnel Junction Majority Gate Proposal *85*
4.5.3 SHE MTJ Majority Gate Simulation *89*
4.5.4 Fabrication of Three Input MTJ Design for Majority Gate Applications *96*
4.5.5 Results and Discussion *100*
4.5.6 Summary *104*

Chapter 5 Summary and Future Work 105

5.1 SUMMARY 105
5.2 ONGOING WORK 106

Bibliography 108

List of Tables

TABLE 4.1 SUMMARY OF VARIOUS MULTILAYER SPIN HALL CHANNELS SUMMARIZING RESULTS OF H_P, J_S, Θ_{SH}, AND Σ_{SH}. 77
TABLE 4.2 MATERIAL PARAMETERS USED FOR SOT-ST MAJORITY GATE SIMULATION. 91

List of Figures

Figure 1.1 Benchmarking efforts conducted in Ref. [4] comparing various emerging research devices (a) NAND2 EDP and (b) logical effort 3

Figure 1.2 Magnetic logic devices identified as potential candidates for beyond-CMOS technology including (a) spin wave logic[6], (b) nanomagnetic logic[7], (c) all-spin logic[8], (d) spin-torque majority gate[9], (e) domain wall logic[10], and (f) magnetoelectric logic[11]. 5

Figure 2.1 Two-channel model of GMR devices showing equivalent resistor circuits for the case of (a) parallel magnetic alignment corresponding to a low resistance state and (b) antiparallel magnetic alignment corresponding to a high resistance state. 12

Figure 2.2 Density of states diagram representing TMR for the case of (a) parallel magnetization corresponding to low resistance and (b) antiparallel alignment corresponding to high resistance. 14

Figure 2.3 Schematic diagram illustrating the concept of spin transfer torque magnetization switching where in (a) electrons are passed from the fixed layer to the free layer. In (b), the spin polarized electrons along the direction of the fixed layer exert a torque on the free layer which can result in magnetization reversal from the antiparallel state to the parallel state. (c) Electrons are passed from the free layer to the fixed layer and (d) electrons of opposite polarization from the fixed layer are reflected and exert a torque on the free layer which can result in magnetization reversal from the parallel to the antiparallel state. (e) Representation of the torque terms associated with magnetization dynamics according to the LLG equation with spin transfer torque term. 15

Figure 2.4 Schematic representation of a NLSV consisting of two FM connected by a NM spin channel. Current is injected across FM1, resulting in a diffusion of pure spin current between FM1 and FM2 which can be detected as a voltage across FM2. 18

Figure 2.5 Density of states diagram showing spin injection from FM1 to the NM spin channel and corresponding shift in spin chemical potential and detected nonlocal voltage for (a) parallel orientation and (b) antiparallel orientation. 19

Figure 2.6 Spin current generation due to the spin Hall effect where electrons of opposite spin orientation are defelcted in different directions due to the spin orbit interaction in the spin Hall channel. 21

Figure 3.1 (a) Proposed design for an all-spin logic unit and (b) design for a majority logic gate based on multiple all-spin logic units connected together. 30

Figure 3.2 Bottom-up fabrication techniques commonly used for NLSV fabrication including (a) lift-off and (b) shadow beam evaporation. 33

Figure 3.3 PMGI/PMMA bilayer resist process. After spinning on and baking of resist (a) the bilayer resist is exposed and (b) developed in two different steps to achieve an undercut of the bottom PMGI layer. (c) During the metal deposition, sidewall coverage is reduced and (d) the resist is removed and metal lifted off, resulting in a patterned feature depending on the pattern transferred from the top PMMA layer. 37

Figure 3.4 Top-down fabrication flow for patterning of NLSV devices with defined channel and nanopillar dimensions. 41

Figure 3.5 SEM images of NLSVs fabricated with the top-down approach showing (a) device contact pads for electrical measurement and (b,c) individual patterned NM spin channel, injector and detector FMs, and top electrodes. 42

Figure 3.6 (a) Testing set-up for NLSV measurement of nanopillar devices and (b) schematic representation of a typical NLSV signal showing different signal levels and corresponding relative magnetization states...43

Figure 3.7 NLSV signal for a device with FM1 and FM 2 dimensions of 175 x 200 nm and 200 x 225 nm, respectively and a spacing of 500 nm measured at (a) room temperature and (b) 60K. 44

Figure 3.8 NLSV signal for device with dimensions of FM1 and FM2 of 400 x 500 nm and 440 x 500 nm measured at room temperature with the external field applied along the hard axis of the FMs. 45

Figure 4.1 Schematic design of an MTJ integrated with a spin Hall channel for switching of magnetization using spin orbit interactions combined with spin transfer torque. 49

Figure 4.2 (a) Thin film material stack for bulk perpendicular spin Hall effect device and (b) VSM results confirming perpendicular magnetic anisotropy of the thin film sample. 55
Figure 4.3 Fabrication flow for patterning of spin Hall effect devices. 55
Figure 4.4 (a) Schematic design of spin Hall device with Ta spin Hall channel and TbFeCo ferromagnet showing electrical measurement set-up and (b) magneto-optical Kerr image of the Hall bar where the dark and bright contrast correspond to the magnetization direction pointing upward and downward, respectively. 56
Figure 4.5(a) RH results under application of a perpendicular external field for -0.5 mA and -8 mA current applied to the spin Hall channel. (b) Coercivity dependence on spin Hall channel current for externally applied magnetic fields. (c) Phase diagram showing required in-plane external field and spin Hall channel current combinations required for magnetization reversal. 58
Figure 4.6 Anomalous Hall measurement with 10 mA current pulses demonstrating (a) complete magnetization reversal with the application of a perpendicular field ±50 Oe and (b) incomplete magnetization switching with the application of a perpendicular field of ±20 Oe. 59
Figure 4.7 Anomalous Hall resistance as a function of the applied field along the (a) y direction and (b) x direction for a spin Hall channel current of ±2 mA. 61
Figure 4.8 (a) Schematic design of a composite structure consisting of a perpendicular magnetic layer, spacer layer, and in plane magnetic layer for achieving external field free switching of perpendicular magnetization and (b) proposed design for how the composite structure can be incorporated into a full perpendicular MTJ structure. 65
Figure 4.9 VSM results for the composite film sample and reference film sample comparing (a) in-plane and out-of plane results and (b) out-of-plane results for a narrow field scan. 66
Figure 4.10 Fabrication flow for composite spin Hall device with magnetic pillar on the spin Hall channel. 67
Figure 4.11 (a) Schematic design of composite device and (b) and optical image of fabricated device showing the testing configuration. 69
Figure 4.12 RH loop of (a) reference sample and (b) composite sample. 70
Figure 4.13 RH loops for various current amplitudes of spin Hall channel for (a) positive and (b) negative polarities of spin Hall channel current. 70
Figure 4.14 (a) RH loop with 1 mA current applied to spin Hall channel and (b) 8 mA and (c) anomalous Hall resistance measured with 1 mA read current after ±8 mA write current under 0, +63, and -63 bias fields. 71
Figure 4.15 Perpendicular magnetization switching by sweeping a DC current without the application of an external field. 73
Figure 4.16 Schematic diagram of multilayer Ta/W spin Hall devices. 76
Figure 4.17 IV curves for the various multilayer Ta/W spin Hall devices. 76
Figure 4.18(a-c) Planar hall resistance, R_{PHE}, (left axis) and corresponding differential resistance, R_{DIFF}, (right axis) for multilayer channels of Ta(5nm), Ta(2nm)/W(3nm), and [Ta(0.5)/W(1)]3/Ta(0.5) and (d-f) corresponding R_{DIFF} curves for various current amplitudes measured as a function of varying angle of externally applied in-plane magnetic field. 79
Figure 4.19 (a) R_{DIFF} measured at 4 mA current applied to the spin Hall channel for the various multilayer Ta/W devices and (b) R_{AHE} measured as a function of varying angle of magnetic field perpendicular to the film. 80
Figure 4.20 Results for the various multilayer spin Hall devices for (a) H_P, (b) Θ_{SH}, and (c) Σ_{SH} calculated for different testing currents applied to the spin hall device. 81
Figure 4.21 Schematic device of proposed SOT-ST majority gate with three input MTJs connected in parallel by a giant spin Hall electrode and connected in serious to an output MTJ. 87
Figure 4.22 Schematic illustrating the step by step operation of the SOT-ST majority gate. 88
Figure 4.23 (a) Diagram of spintronic modules utilized for simulation of a single SOT-ST MTJ element. (b) Schematic image of single SOT-ST MTJ that represents the device simulated. 90

FIGURE 4.24 MAGNETIZATION DYNAMICS OF X, Y, AND Z COMPONENT FR THE CASE OF (A) SOT CURRENT ONLY SWITCHING, (B) STT CURRENT ONLY SWITCHING, AND (C) SOT COMBINED WITH STT SWITCHING. 92
FIGURE 4.25 CIRCUIT MODEL FOR 3 INPUT MTJS OF SOT-ST MAJORITY GATE USED TO MODEL SETTING OF THE INPUT STATES. 93
FIGURE 4.26 (A) TIMING DIAGRAM SHOWING THE APPLICATION OF THE SOT AND STT CURRENT PULSES FOR MAGNETIZATION SWITCHING IN THE SIMULATION, (B) PARALLEL RESISTANCE ACROSS THE THREE INPUT MTJS AS A FUNCTION OF INCREASING STT CURRENT FOR GIVEN SOT CURRENTS, AND (C) PHASE DIAGRAM INDICATING REQUIRED SOT AND STT CURRENT COMBINATIONS FOR SETTING THE VARIOUS INPUT STATES OF THE SOT-STT MAJORITY GATE. 95
FIGURE 4.27 FABRICATION FLOW OF 3 MTJ INPUTS FOR APPLICATION OF SOT-STT MAJORITY GATE. 99
FIGURE 4.28 SEM IMAGES OF (A) HALL BAR WITH TOP ELECTRICAL CONTACTS ALLOWING FOR BOTH SPIN HALL/ANOMALOUS HALL MEASUREMENTS AND TOP ELECTRICAL CONTACTS FOR APPLICATION OF CURRENT ACROSS THE MTJS AND MR MEASUREMENT AND (B) INDIVIDUAL MTJ PILLARS OF VARYING ASPECT RATIO. 99
FIGURE 4.29 VSM RESULT OF TA/TBFECO/MGO/TBFECO MTJ STRUCTURE. 101
FIGURE 4.30 (A) SCHEMATIC DESIGN OF THE EXPERIMENTAL SPIN HALL DEVICE WITH THREE MTJ PILLARS. (B) R_{AHE} OF DEVICE WITH 140X70 NM, 124X80 NM, AND 110X90 NM AND (C) 400X160 NM, 310X200 NM, AND 275X225 NM CONTROLLED BY APPLICATION OF AN EXTERNAL PERPENDICULAR FIELD. 102
FIGURE 4.31 R_{AHE} FOR THE APPLICATION OF (A) 0.2 MA CURRENT APPLIED TO THE SPIN HALL CHANNEL AND (B) 2.2 MA CURRENT APPLIED TO THE SPIN HALL CHANNEL. 102
FIGURE 4.32(A) SCHEMATIC OF THE TESTING SET-UP FOR IN-PLANE MTJ SPIN HALL DEVICE FOR MR MEASUREMENT AND (B) MR OF THEE MTJ DEVICE SWITCHED USING EXTERNALLY APPLIED PERPENDICULAR MAGNETIC FIELD. 103

CHAPTER 1 INTRODUCTION

1.1 MOTIVATION FOR BEYOND CMOS TECHNOLOGY

Recently there has been a significant increase in the amount of research dedicated to exploring and developing new computing paradigms as alternative technologies for conventional complementary metal oxide semiconductor (CMOS) devices. For over 40 years, CMOS has followed scaling trends predicted by Moore's law that states the number of transistors per chip will double roughly every 18 to 24 months. It has been predicted that Moore's law will reach its end and CMOS scaling will saturate, which has resulted in an increase in development of beyond-CMOS devices to overcome the limitations with CMOS scaling.

While early predictions forecasted that we would have already seen an end to Moore's law, CMOS has continued to scale. It was initially believed that factors such as lithography limitations or gate oxide thickness would be the limiting factors; however, processing and materials research has helped to overcome these issues[1]. While it was believed that feature sizes below the wavelength of the exposure tool were not possible and would limit the device size, novel patterning techniques such as pitch division, phase shift lithography, and the development of new exposure techniques such as extreme ultra violet exposure have allowed for the patterning of even smaller devices. Additionally, it was believed that as the device sizes were reduced, the gate oxide thickness would also need to be reduced resulting in large leakage currents and eventually gate oxide breakdown. With the introduction of high-k dielectric materials as the gate oxide instead of SiO_2, it is possible

to achieve the large capacitances required for fast switching while maintaining thicker gate oxides.

Although there does not appear to be an immediate end to scaling in CMOS, it is generally agreed upon that there is the necessity to develop beyond-CMOS devices to overcome issues associated with the scaling. The most likely end to scaling will come from the physical device dimensions as the devices approach the atomic scale. As devices are already approaching dimensions on the order of only several atomic layers thick, it will be increasingly difficult to reduce the size. Another issue is device performance as devices are continually scaled. While device scaling increases the capacitance and decreases the voltage, there are drawbacks such as an exponential increase in leakage current as well as device variability. Due to the thin gate oxides, leakage current in recent generations of devices has significantly increased and accounts for a major portion of the energy required for operation. Additionally, as devices are scaled, they become more susceptible to slight variations in processing which can result in large changes in device performance[2].

Beyond-CMOS devices are being explored to overcome the approaching end of Moore's Law. Devices currently being explored aim to improve computing performance in ways other than a continual decrease in size such as including additional functionality, interconnect improvements, or architecture design improvements[3]. It is important that the proposed devices can meet certain performance demands such as switching delay, energy consumption, and device size as well as compatibility with current fabrication techniques. Additional merits that need to be considered include the ability to realize standard Boolean functions such as NOT, AND, and OR functions, amplifications,

feedback prevention, low signal-to-noise ratios, and room temperature operation[4]. The International Technology Roadmap for Semiconductors (ITRS) as well as the Nanoelectronics Research Initiative (NRI) work to provide possible beyond-CMOS technologies with benchmarking efforts to compare and contrast their performance in hopes of identifying the most viable technologies for the future[3], [5].

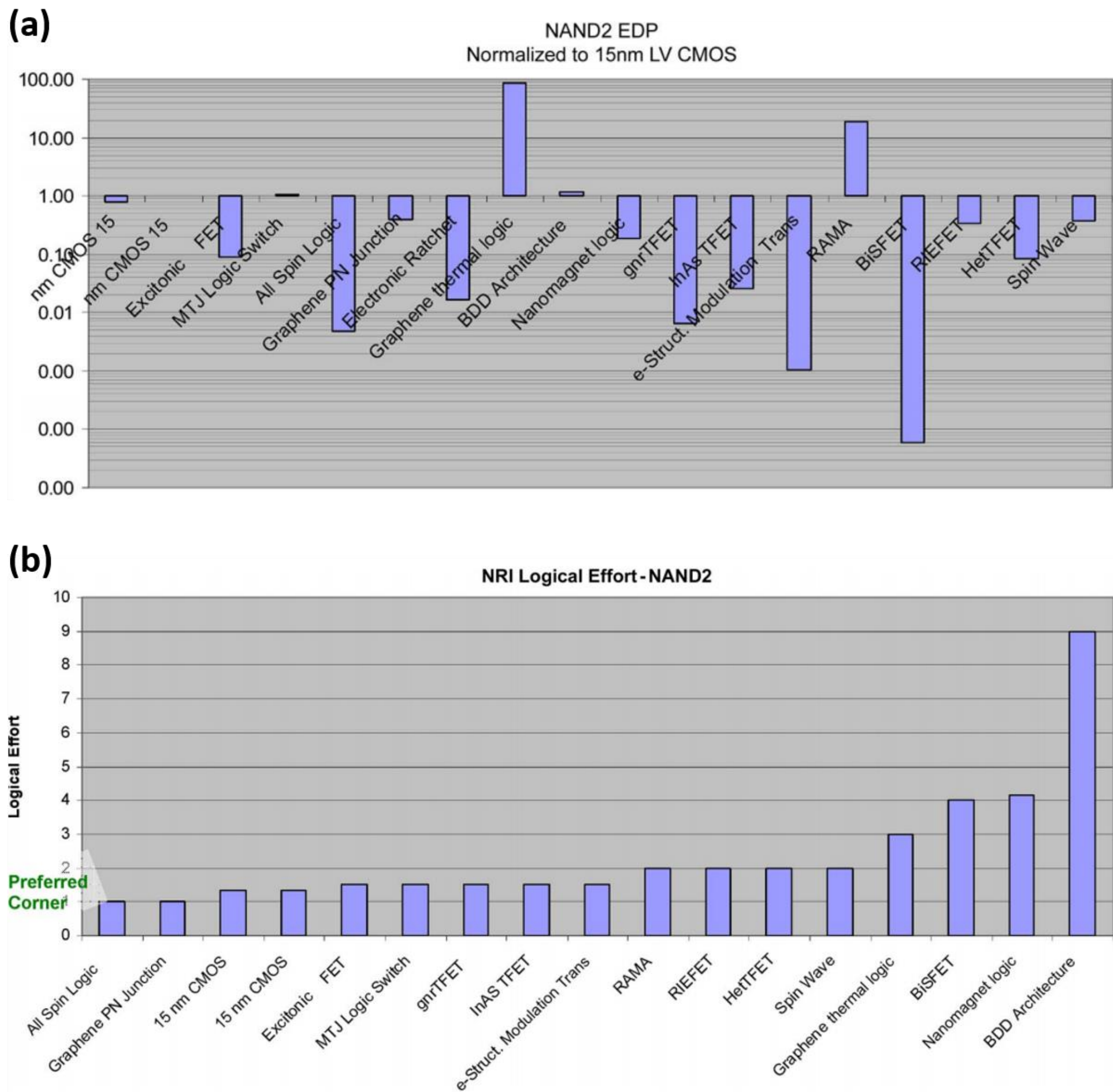

Figure 1.1 Benchmarking efforts conducted in Ref. [5] *(© 2010 IEEE) comparing various emerging research devices (a) NAND2 EDP and (b) logical effort*

Some recent devices identified as promising candidates for beyond-CMOS technologies include devices with an internal state variable of charge (i.e. III-V tunneling field effect transistors (TFETS), graphene nanoribbon TFETs), orbital states (bilayer pseudospin FETs (BiSFETs)), electric polarization (ferroelectric FETs), and magnetization (spin wave devices (SWD), spin torque (ST) majority gates, nanomagnetic logic (NLM), all-spin logic devices (ASLD)). It can be difficult to identify an individual technology as the most promising candidate since certain technologies may excel in certain categories while performing less efficiently in other categories. Certain devices may be preferential for a specified application space than others (i.e. the requirement for fast switching speeds vs the need for low power consumption). Also, certain technologies may be more easily scalable as they are combined for logic functions. For instance, a single logic unit for all-spin logic is about double the size CMOS, but due to the structure of the all-spin logic unit, it can be about 30 times smaller when implemented in a 32 bit adder[4]. Additional benchmarking efforts to compare a variety of emerging technologies are presented in Figure 1.1(a,b)[5]. Figure 1.1(a) compares the energy delay product of a wide variety of devices normalized to a 15 nm CMOS device. Figure 1.1(b) calculates logical effort of a variety of devices where the logical effort is described as a way to quantify how well logic can be evaluated using a certain circuit and is compared to that of a CMOS inverter.

1.2 Overview of Spintronic Based Logic

Spintronics provide a promising technology option for beyond-CMOS devices. While many device concepts are still in an early stage of research, it is anticipated that the chance for improvements based on the optimization of material properties, discovery and increased understanding of new spintronic concepts, etc. can result in a decrease in energy delay product and have the abilities to rival the performance of CMOS devices. Additionally, magnetic devices offer benefits such as long life-times, nonvolatility, and radiation hardness. Several promising candidates for spintronic logic as identified by ITRS[3] include spin torque (ST) majority gates, nanomagnetic logic (NML), all-spin logic devices (ASLD), and spin wave devices (SWD). Additionally, new spintronic device concepts are continually being proposed as research in the field of spintronics advances. In

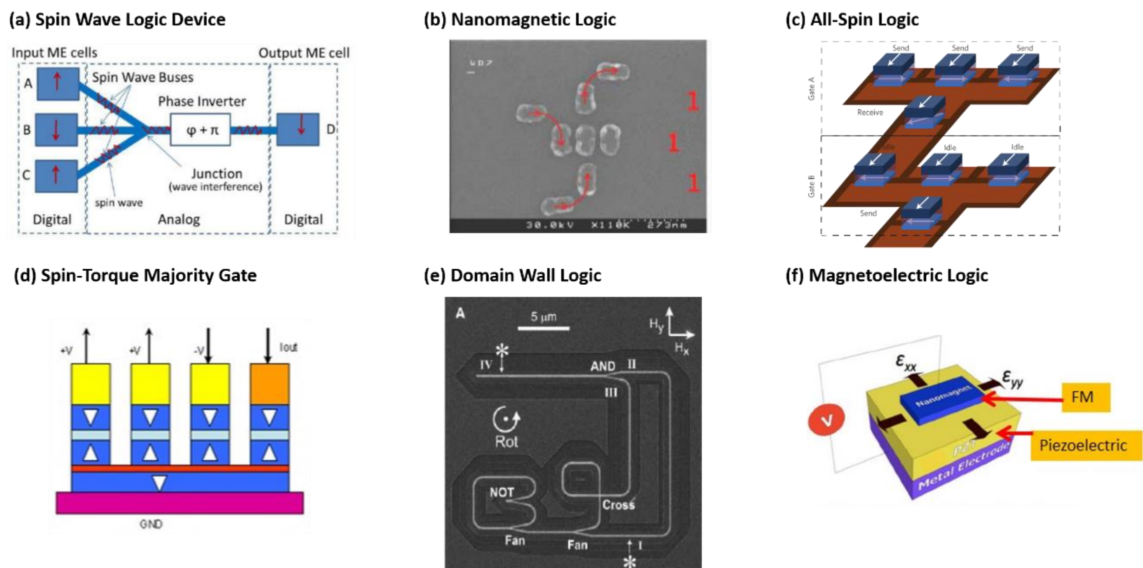

Figure 1.2 Magnetic logic devices identified as potential candidates for beyond-CMOS technology including (a) spin wave logic[4]*(© 2013 IEEE), (b) nanomagnetic logic*[11]*, (c) all-spin logic*[12]*, (d) spin-torque majority gate*[14]*(© IEEE 2012), (e) domain wall logic*[15]*, and (f) magnetoelectric logic*[21].

this section, several concepts for proposed spintronic devices will be briefly described.

Spin wave devices for logic applications were proposed in Refs. [6], [7]. The information in SWD is stored in the phase of the spin wave, which is an appealing way to transmit data since at room temperature the coherence length of spin waves can be on the order of several microns. For logic operation, ferromagnetic strips are used to excite the spin waves and transmitted through the device to the output. Then, depending on the phase of the spin wave, the output magnet is either switched or not. Additionally, by operating the SWDs at different frequencies, it is possible to achieve parallel data processing. Additionally, SWDs are predicted for both Boolean and non-Boolean applications and could be well suited for tasks such as image processing[3]. A schematic of a spin wave logic gate is shown in Figure 1.2(a)[8]. However, there are several drawbacks to spin wave devices. They are very sensitive to defects which can affect device performance and reliability. Furthermore, additional circuitry is required for amplification since spin wave devices to not have inherent gain. With future research advances, SWDs have been identified as one promising spintronic logic scheme.

Another proposed spintronic logic device is called nanomagnetic logic (NML), which relies on the dipole interactions between closely spaced nanomagnets. Initially, the array of nanomagnets are clocked so that their magnetization lies along a quasi-stable state. The input nanomagnets state is set by a method such as current-generated magnetic field or spin transfer torque. Due to the dipole interactions, the adjacent nanomagnets will settle into a stable state determined by the input magnet and the output can then be determined at the end of the nanomagnet array by electrical readout via magnetoresistance[9], [10].

Additionally, majority gate operation has been shown for NML using magnetic force microscopy to determine the state of the nanomagnets (Figure 1.2(b))[11]. Since the data is transmitted through coupled nanomagnets, the device and interconnect elements are interchangeable and no additional energy source is required for data transmission. Data does not require a spin to charge conversion for a logic operation. However, a difficulty in NML is being able to direct the data flow and therefore achieve nonreciprocity in the NML circuit. Additionally, it suffers from errors due to coupling reliability between all of the bits in a logic circuit as well as achieving complex geometries such as 90 degree turns. Due to these limitations, there has been a decrease in research efforts in NML devices.

All-spin logic, which relies on spin diffusion between two ferromagnets in a nonmagnetic channel, is another promising spintronic logic device[12], [13]. An injector ferromagnetic is used to generate a spin accumulation between the ferromagnet and a spin channel. The resultant spin current then diffuses to a detector ferromagnet. Spin torque from the pure spin current can be used to switch the magnetization of the detector, and a nonlocal voltage is measure at the detector ferromagnet to determine the state of the device. A schematic majority gate design utilizing all-spin logic is shown in Figure 1.2(c)[12].

An additional proposed spintronic logic is a spin torque majority gate. A spin torque majority gate consists in three input and one output magnetic tunnel junctions (MTJs) connected by intersecting ferromagnetic wires. The three input MTJs are used to exert a torque on the connecting ferromagnetic wires in which the magnetic information will propagate. At the intersection, the "majority" magnetization direction will then propagate to the output MTJ where the state can be determined by the magnetoresistance. A schematic

spin torque majority gate is shown in Figure 1.2(d)[14]. The ST majority gate can be used to compactly realize other functions. For instance, a one-bit adder can be realized with three ST majority gates[4].

Domain wall logic is another proposed spintronic device. Domain wall logic that relies on field driven domain walls to move data and the magnetization direction to encode bits of data was proposed in 2005(Figure 1.2(e)[15]). Since then, there have been several variations of proposed domain wall logic schemes. In 2008, a domain wall logic that relies on current-driven domain wall motion due to the spin transfer torque effect was demonstrated[16]. This then led to the proposal for logic devices consisting of MTJs connected by domain walls where the free layer of the MTJs are composed of the magnetic wire in which the domain wall propagates by Lyle, *et al.*[17]. A current is applied along the ferromagnetic wire to move the domain wall via spin transfer torque and therefore change the magnetization state of the MTJ. Current is applied across the MTJ and used to drive the next device. Depending on the orientation of the free and fixed layers of the MTJ, the current level will either be high or low. In 2012, this concept was expanded to illustrate how a magnetic adder could be constructed using MTJs connected by a domain wall[18]. A three terminal domain wall logic gate was also proposed by Currivan, *et al.* in 2012[19] and was experimentally demonstrated in 2015[20].

Magnetoelectric logic devices provide an additional concept for spintronic logic devices. A magnetoelectric device consists of a ferromagnet and a piezoelectric material such as shown in Figure 1.2(f)[21]. When a voltage is applied across the device, it results in an electric field that generates a strain on the magnetic material which can in turn modify

the magnetic properties and rotate the magnetization direction. One type of magnetoelectric based logic device (called MESO, proposed by Manipatruni, *et al.*[22]), a magnetoelectric field is used to switch the magnetization direction and spin orbit interactions are used to convert spin signals to charge signals. These devices have the benefit of being able to be operated by voltage instead of charge current.

1.3 Dissertation Overview

In this dissertation, my research efforts on spin current generation for spintronic logic devices will be presented. The work will focus on my efforts in nonlocal lateral spin valve (NLSV) development for all-spin logic applications and topics in spin Hall effect for spin current generation and logic device applications.

Chapter 2 will provide a brief introduction to spintronic topics related to devices discussed in this dissertation. It will provide the background of device concepts and theory necessary for the reader to understand the topics discussed. The first two sections will discuss giant magnetoresistance and tunneling magnetoresistance. Then spin transfer torque and the magnetization dynamics associated with the switching process is introduced. After that, an introduction to nonlocal lateral spin valves including topics of spin accumulation and detection is presented. In the final section of Chapter 2, an introduction to spin orbit interactions and the spin Hall effect is presented.

In Chapter 3, my research efforts in NLSVs for all-spin logic applications is presented. After an introduction to NLSVs and the concept of all-spin logic, my work on developing a top-down fabrication approach for NLSVs is presented. This work presents

the details of the top-down fabrication approach and verifies that it is compatible for NLSVs. This is an important step required for integration of NLSVs and addresses issues that are associated with current fabrication methods.

Chapter 4 focuses on my research contributions regarding the spin Hall effect and optimization for spin current generation for logic applications. In the first section, the groundwork for spin Hall effect experiments is laid out using TbFeCo perpendicular magnets. In the second section, I develop a composite material stack which can be used to switch perpendicular magnetization without the need for an external field. The next section focuses on my research to develop a multilayer spin Hall channel for tuning the magnetic properties such as spin Hall angle and resistivity, which is important for energy efficient devices. In the final section, I propose a majority logic gate combining the spin Hall effect and spin transfer torque effect and I present both simulation work to verify the device concept as well as initial experimental work to lay the foundation for the spin Hall spin torque majority gate.

A summary of my research is presented in Chapter 5 as well as on-going research efforts related to these topics and the proposed next research steps.

CHAPTER 2 INTRODUCTION TO SPINTRONICS

2.1 GIANT MAGNETORESISTANCE

A critical development for magnetic technologies occurred in 1988 with the discovery of giant magnetoresistance (GMR). Fert, *et al.* and Grunberg, *et al* discovered the resistance of a multilayer magnetic structure (in this case, Fe/Cr/Fe multilayer systems) depends on the relative magnetic orientation of the magnetic layers. The difference in the resistance of the different magnetic orientation states for GMR can be explained using a two-channel model. Consider the case of parallel alignment between the two ferromagnetic layers. Spins of one orientation experience a lower resistance, while spins of the opposite direction experience additional scattering and therefore a higher resistance. This can be modeled as the resistor circuit shown in Figure 2.1(a) with two low resistances connected in series and two high resistances connected in series. Both of these are then connected in parallel and the overall effect is a low resistance. Then, considering the case for the magnetic layers aligned in the antiparallel configuration, both spin up and spin down electrons would see a high resistance and low resistance state travelling through the device due to the two different magnetic orientations. This can be modeled as a high and low resistor connected in series for each spin direction. These are then connected in series as shown in Figure 2.1(b). Due to the different resistances associated with the different magnetic layer orientations, information can be stored as the different resistance states. The difference in resistance of the two states is quantified as the magnetoresistance value and is given as

$$MR = \frac{R_{AP} - R_P}{R_P} \times 100\%$$

where R_{AP} and R_P are the resistance states for the antiparallel and parallel configurations, respectively.

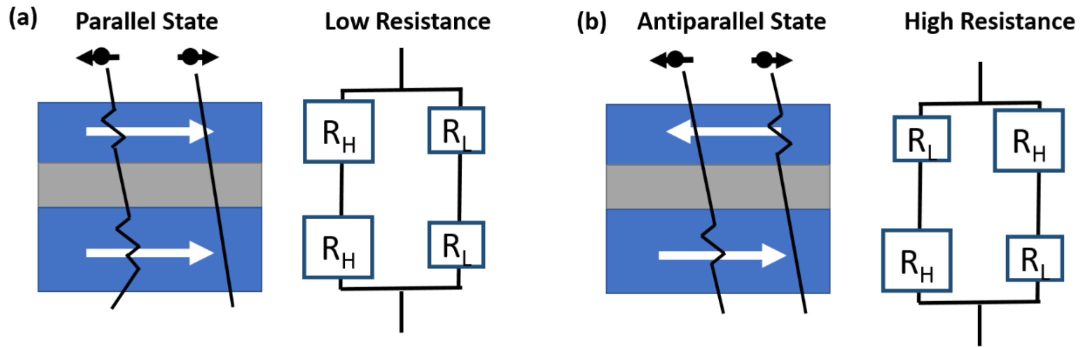

Figure 2.1 Two-channel model of GMR devices showing equivalent resistor circuits for the case of (a) parallel magnetic alignment corresponding to a low resistance state and (b) antiparallel magnetic alignment corresponding to a high resistance state.

2.2 Tunneling Magnetoresistance

In 1975, tunneling magnetoresistance (TMR) was discovered in magnetic tunnel junctions (MTJs) that consist of two ferromagnets separated by a tunneling barrier as opposed to a metallic layer in GMR structures. Like GMR, the resistance in an MTJ depends on the relative orientation of the two magnetic layers; however, the fundamentals of why this happens are slightly different. The basic concepts behind TMR can be explained using the Julliere model[23] and density of states of the ferromagnetic materials. Unlike nonmagnetic materials which have an equal number of spin up and spin down states at the Fermi level, magnetic materials have a majority spin of one direction at the Fermi

energy as depicted in Figure 2.2. Considering the case of parallel aligned ferromagnets where the spin up states are the majority spins at the Fermi level as depicted in Figure 2.2(a). As current is passed through the device, electrons from the spin up majority state will tunnel to the spin up majority state in the second ferromagnetic layer while the spin down minority states will tunnel to the spin down minority states in the second ferromagnet to fill the available states. Since there are a large number of available states for the majority spins of the first ferromagnet to tunnel into, this results in a low resistance. For the case of antiparallel magnetization orientation, there is a limited number of available states for the first ferromagnets majority states to tunnel into which results in a high resistance as depicted in Figure 2.2(b). This model has been fairly accurate for predicting TMR behavior in amorphous tunnel barriers such as aluminum oxide. However, this model assumes the tunnel barrier has little effect on the device operation and also assumes that spins of electrons are conserved in the tunneling process and that the spins act in two separate spin channels. Since this model was introduced, it has been shown that the tunnel barrier can have a significant impact on the MR seen in TMR devices and is more accurately described by Slonczewski's model. In Slonczewski's model, the tunnel barrier is taken as a rectangular barrier potential and uses a free-electron approach and shows that the polarization and TMR behavior can strongly depend on the tunnel barrier. Due to a spin filtering effect of the tunnel barrier, much higher MR percentages can be achieved with proper choice of tunnel barrier material such as MgO[24].

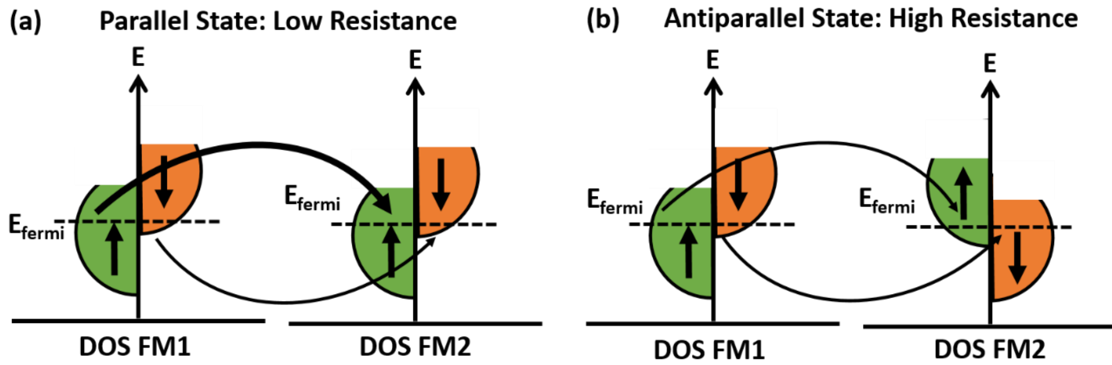

Figure 2.2 Density of states diagram representing TMR for the case of (a) parallel magnetization corresponding to low resistance and (b) antiparallel alignment corresponding to high resistance.

2.3 Spin Transfer Torque

Spin transfer torque (STT) is another phenomena of GMR and TMR devices which was first predicted in 1996 by Slonczewski[25] and Berger[26]. Unlike external field switching of magnetization, STT provides a direct electrical way to change the magnetization of a free layer in a GMR or TMR device and is highly appealing for device applications such as memory or logic. When charge current is passed through a ferromagnetic material, it acts as a spin polarizer (or spin filter) and to align the majority of the electrons so that their spin is in the same direction as the magnetic moments of the ferromagnet due to a transfer of angular momentum. This transfer of angular momentum can result in magnetization reversal for GMR or TMR devices. Take, for instance, an MTJ in an antiparallel configuration. When electrons pass through the fixed (polarizing) layer of the MTJ, the majority of electrons become oriented in the direction of the fixed magnetic

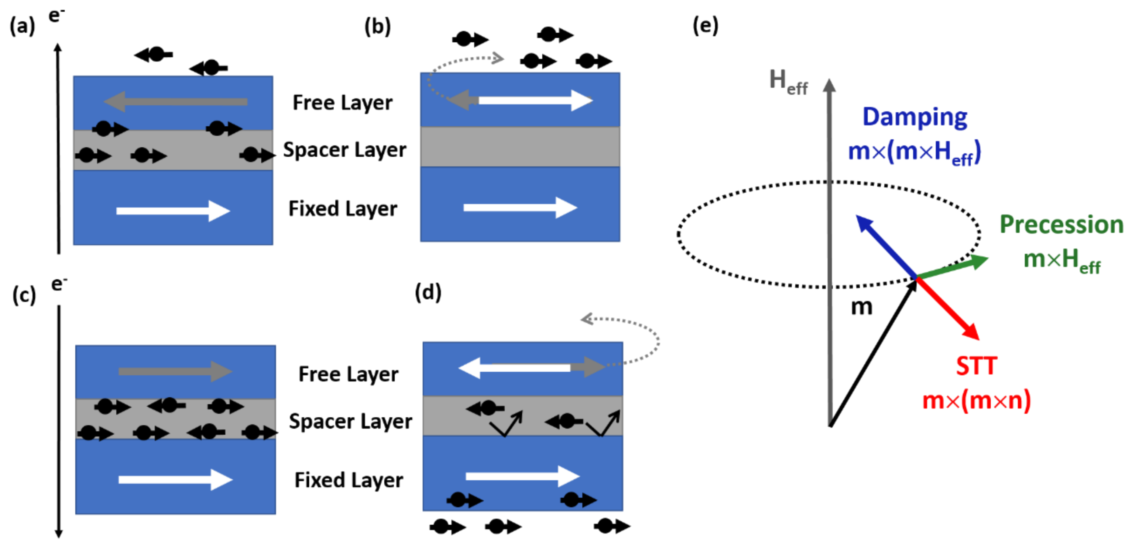

Figure 2.3 Schematic diagram illustrating the concept of spin transfer torque magnetization switching where in (a) electrons are passed from the fixed layer to the free layer. In (b), the spin polarized electrons along the direction of the fixed layer exert a torque on the free layer which can result in magnetization reversal from the antiparallel state to the parallel state. (c) Electrons are passed from the free layer to the fixed layer and (d) electrons of opposite polarization from the fixed layer are reflected and exert a torque on the free layer which can result in magnetization reversal from the parallel to the antiparallel state. (e) Representation of the torque terms associated with magnetization dynamics according to the LLG equation with spin transfer torque term.

layer (Figure 2.3(a)). However, when the electrons reach the free layer, their spin orientation is opposite to the spin of the magnetic moment. When the electrons pass through the free layer, there is a transfer of angular momentum to reorient the spins in the direction of the magnetic moment. However, due to conservation of angular momentum, the electrons also exert a torque back on the magnetic layer. When the charge current density

passing through the MTJ is large enough, this torque can cause the magnetization direction of the free layer to reverse, as schematically shown in Figure 2.3(b). A similar process happens for magnetization reversal from an initially parallel state to an antiparallel state. The direction of the charge current is reversed so that it flows from free layer to the fixed layer(Figure 2.3(c)). When the charge current reaches the fixed layer interface, some electrons with opposite spin orientation are reflected which can then exert a torque on the free layer causing magnetization reversal when the current density is large enough (Figure 2.3(d)). The required current density for magnetization reversal for in-plane MTJs can be calculated with the following equation:

$$J_{c,0} = \frac{2e\alpha M_s t_F (H_{K\parallel} + H_{ext} + 2\pi M_s)}{\hbar\eta}$$

where α is the gilbert damping constant, M_s is the saturation magnetization, t_f is the free layer thickness, $H_{K\parallel}$ is the effective in-plane anisotropy field which includes the shape anisotropy and crystalline anisotropy, H_{ext} is the externally applied field, and η is the spin transfer efficiency.

The first experimental observation of STT in a GMR stack was demonstrated in 2000 by Katine, *et al.*[27] in a Co/Cu/Co multilayer structure. STT was subsequently demonstrated in 2004 for an aluminum oxide tunnel barrier by [28]–[31]. Many experimental demonstrations with various material stacks have been demonstrated since and magnetoresistance values of over 600% have been demonstrated[32].

STT in perpendicular magnetic structures has also been demonstrated. Perpendicular MTJs offer benefits compared to in-plane structures. One benefit is that magnetic materials with perpendicular crystalline anisotropy can have higher anisotropy

values and therefore higher thermal stability. Additionally, perpendicular MTJs remove the requirement for shape anisotropy and are beneficial for scaling and high density applications. Perpendicular devices also provide the potential for reduced energy required for switching. The critical current required for switching in perpendicular MTJs is given by:

$$J_{c,0} = \frac{2e\alpha M_s t_F (H_{K\perp} + H_{ext} - 4\pi M_s)}{\hbar\eta}$$

where $H_{K\perp}$ is the perpendicular anisotropic field. Spin transfer torque in perpendicular spin valves was demonstrated in 2006 by Mangin, *et al.*in Pt/[Co/Pt]$_4$/[Co/Ni]$_2$/Cu/[Co/Ni]$_4$/Pt spin valves[33] and Meng and Wang in [CoFe/Pt]$_5$/CoFe/Cu/[CoFe/Pt]$_7$ spin valves[34].

An understanding of how magnetization dynamics and how the magnetization reversal process happens can be given by the LLG equation with a modification for Slonczewski's STT term. The change in magnetization is described as follows:

$$\frac{\partial \boldsymbol{m}}{\partial t} = -\frac{g\mu_B}{\hbar}\boldsymbol{m} \times \boldsymbol{H}_{eff} + \alpha \boldsymbol{m} \times \frac{\partial \boldsymbol{m}}{\partial t} - \gamma\left(\frac{g\mu_B}{2e}\right)\left(\frac{\eta J}{\mu_0 M_s H_K t_F}\right)\boldsymbol{m} \times (\boldsymbol{m} \times \hat{\boldsymbol{n}})$$

where g is the Landé factor, μ_B is the Bohr magneton, J is the injected current density, and $\hat{\boldsymbol{n}}$ is the current polarization direction.

The equation consists of three main terms that act on the magnetization and include a precessional term due to the effective field, a gilbert damping term, and an antidamping (or damping, depending on the direction of current) term associated with the spin transfer torque. A schematic diagram of the magnetization dynamics and associated torque terms is given in Figure 2.3(e).

2.4 Spin Injection, Accumulation, and Detection in Nonlocal Lateral Spin Valves

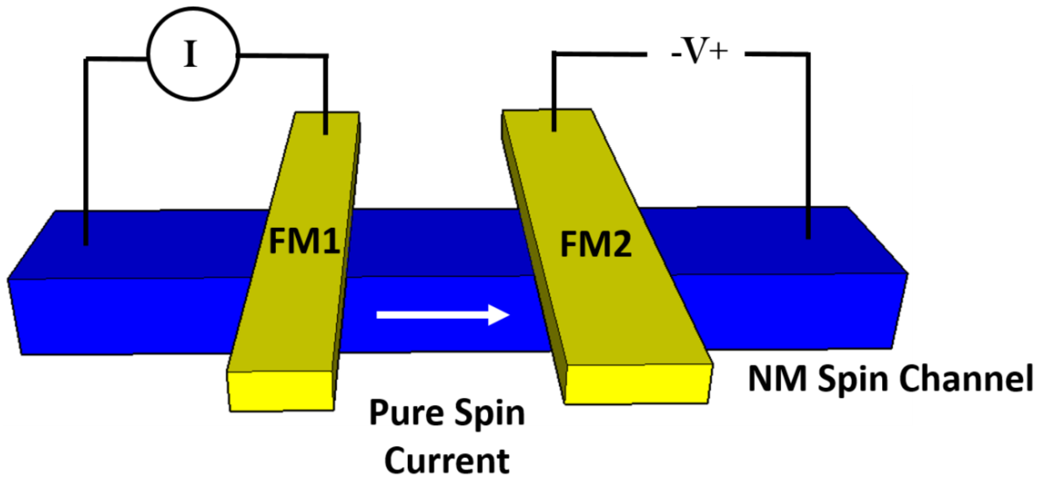

Figure 2.4 Schematic representation of a NLSV consisting of two FM connected by a NM spin channel. Current is injected across FM1, resulting in a diffusion of pure spin current between FM1 and FM2 which can be detected as a voltage across FM2.

A nonlocal lateral spin valve (NLSV) consists of two ferromagnetic contacts (FM1 and FM2) connected laterally by a nonmagnetic "spin channel" which can be metallic, semiconducting, or a two-dimensional material such as graphene. A schematic diagram of a NLSV is shown in Figure 2.4. A current is applied across FM1 and one end of the channel and acts as the injector. Charge current passed through the ferromagnet results in a polarized current that depends on the density of states of each spin at the Fermi level of the ferromagnet. This results in a spin accumulation at the interface between FM1 and the channel. The spin injection results in an increase in the majority spin chemical potential and a decrease in the minority spin chemical potential in the nonmagnetic spin channel

material as depicted by the density of states diagram shown in Figure 2.5(a). The shift in the spin dependent chemical potential is given as $\Delta\mu$.

Due to the non-equilibrium spin states, spin polarized electrons will diffuse in the channel in all directions. While the spin current flow from FM1 to the end of the channel is due to both drift and diffusion, spin current flow between FM1 and FM2 is purely diffusion and decays exponentially as function of $\exp(-d/\lambda_s)$ where d is the distance from the injector and λ_s is the spin diffusion length of the channel material. Due to the lack of

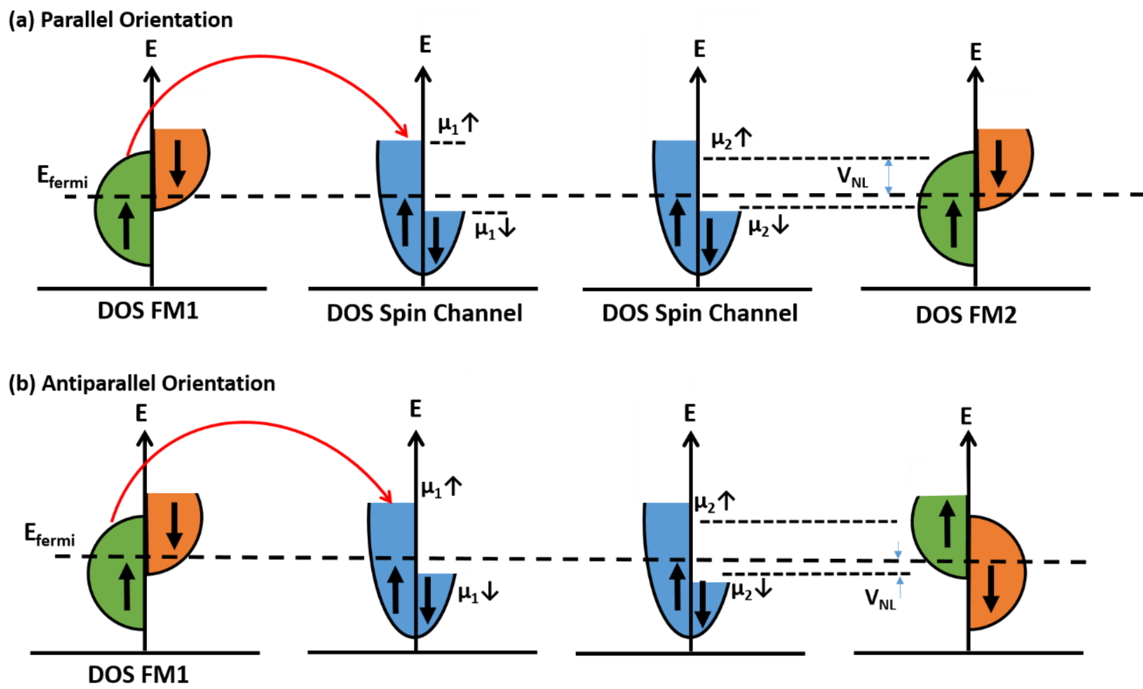

Figure 2.5 Density of states diagram showing spin injection from FM1 to the NM spin channel and corresponding shift in spin chemical potential and detected nonlocal voltage for (a) parallel orientation and (b) antiparallel orientation.

charge current flowing between FM1 and FM2, the spin diffusion current between FM1 and FM2 is referred to as a "pure spin current" and is due to a movement of spin transfer

angular moments in the channel.

The spin accumulation can then be detected by measuring the voltage across the detector ferromagnet, FM2, and the other end of the channel. The voltage state detected is due to the spin dependent chemical potential and depends on the relative orientations of FM1 and FM2. For the case of FM1 and FM2 in a parallel alignment, the chemical potential of the majority spins is probed and detected, resulting in a positive nonlocal voltage signal (Figure 2.5(b)), while for the case of FM1 and FM2 in an antiparallel alignment, the chemical potential of the minority spins is probed resulting in a negative nonlocal.

The nonlocal voltage signal, ΔV_{NL}, can then be converted to a nonlocal resistance, $\Delta R_{NL} = \Delta V_{NL}/I_{inj}$ where I_{inj} is the charge current injected across FM1. The nonlocal resistance for transparent interfaces can be approximated as follows[35]:

$$\Delta R_S = \frac{P_{FM}^2 R_{S,FM}^2}{2R_{S,FM}\exp\left(\frac{d}{\lambda_{NM}}\right) + R_{S,NM}\sinh d/\lambda_{NM}}$$

where P_{FM} is the polarization of the ferromagnets and $R_{S,FM}$ and $R_{S,NM}$ are the spin resistances of the ferromagnetic and non-magnetic spin channel materials, respectively. The spin resistance is defined as:

$$R_s = 2\rho\lambda/[(1-P^2)A]$$

where ρ is the resistivity and A is the cross-sectional area between the ferromagnet and nonmagnetic spin channel. Additionally, the spin current that reaches the detector, FM2, can be calculated as follows[35]:

$$I_s = \frac{\frac{\left(\frac{\Delta V_{NL}}{I}\right) I_{DC}}{R_{S,FM} P_{FM}} \left(\left(1 + \frac{R_{S,FM}}{R_{S,NM}}\right) e^{\frac{t}{\lambda_{NM}}} - \left(1 - \frac{R_{S,FM}}{R_{S,NM}}\right) e^{-\frac{t}{\lambda_{NM}}} \right)}{\left(1 + \frac{R_{S,FM}}{R_{S,NM}}\right) e^{\frac{t}{\lambda_{NM}}} + \left(1 - \frac{R_{S,FM}}{R_{S,NM}}\right) e^{-\frac{t}{\lambda_{NM}}} - 2}$$

where t is the thickness of the ferromagnets.

2.5 Spin Orbit Interactions

The Hall effect, discovered in 1879[36], results in a measurable electrical voltage transverse to a charge current when a perpendicular magnetic field is applied to a conductor. Since then, additional contributions to the Hall effect have been discovered with

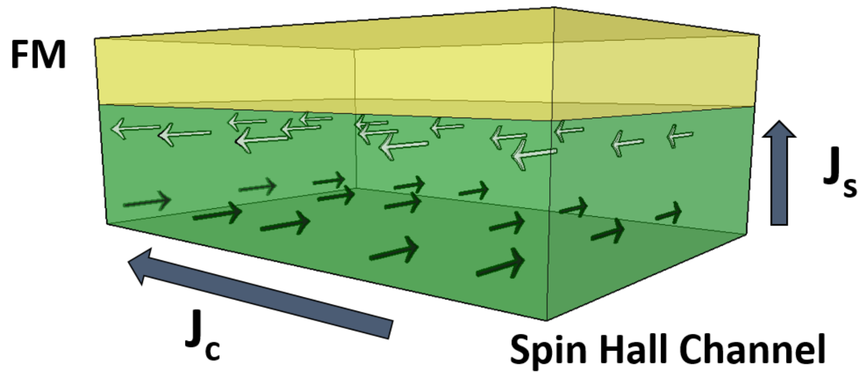

Figure 2.6 Spin current generation due to the spin Hall effect where electrons of opposite spin orientation are deflected in different directions due to the spin orbit interaction in the spin Hall channel.

the incorporation of magnetic materials which can be explained by spin orbit interactions. Spin orbit interactions have recently become an appealing and increasing area of research in spintronics due to its possibility to manipulate the magnetization direction in devices.

The spin Hall effect is one example of spin orbit interactions where electrons of

different spin orientations are deflected in opposite directions, resulting in a transverse voltage. The concept of the spin Hall effect was first introduced in 1971[37], [38] and reintroduced to the scientific community in 1999[39]. Extrinsic effects such as skew scattering[40] or side jump scattering[41] are thought to be dominant sources of spin orbit interactions in the spin Hall effect. When charge current is passed through a material with large spin orbit interactions, spins of opposite orientation are deflected in opposite directions. This results in a spin imbalance and effective spin current transverse to the applied charge current. A schematic illustration of the spin current generation due to the spin Hall effect is shown in Figure 2.6. The generated spin current is given by

$$J_s = \frac{\theta_{SHE} 2e}{\hbar} (\boldsymbol{J}_c \times \boldsymbol{\sigma})$$

where θ_{SH} is the spin Hall angle, J_c is the applied charge current density, and $\boldsymbol{\sigma}$ is the spin polarization vector. Additionally, a spin current can result in a charge current due to the same scattering effects and the corresponding charge current is given by

$$J_c = \frac{\theta_{SHE} 2e}{\hbar} (\boldsymbol{J}_s \times \boldsymbol{\sigma})$$

The above spin current generated from the spin Hall effect corresponds to a perpendicular effective field given by:

$$H_P = -\hbar J_s / 2e M_s t (\hat{\sigma} \times \hat{m})$$

which corresponds to a torque given by:

$$\tau_P = -\hbar J_s / 2e M_s t (\hat{m} \times (\hat{\sigma} \times \hat{m})$$

where M_s is the saturation magnetization, t is the thickness of the ferromagnet, $\hat{m}$ is the direction of the magnetic moment[42]. The effective field acts as a torque on an adjacent

magnetic material which can result in changes in the magnetization direction.

Another contribution to SOTs is the field-like torque due to effects such as Rashba field effect. The discovery and prediction of the Rashba effect is attributed to Dresselhaus[43] and Rashba[44]. Rashba effects arise in structures with inversion asymmetry. When electrons move orthogonal to an electric field, they experience an effective magnetic field resulting in spin polarization of the electrons. The effective field generated due to the Rashba effect is given by[45], [46]:

$$H_{RA} = \frac{\alpha_R P}{\mu_B M} (\hat{\boldsymbol{z}} \times \boldsymbol{J_c})$$

where α_R is the coefficient of Rashba interaction, P is a factor that depends on the strength of the s-d coupling strength, μ_B is the Bohr magneton, and M is the magnetization. The generated transverse effective field can then exert a torque on the adjacent magnetic layer to cause changes in the magnetization direction which corresponds to an effective field-like torque in the longitudinal direction.

Spin orbit coupling due to the Rashba effect was demonstrated in two-dimensional electron gasses in 1979 by Vas'ko[47] and in 1984 by Bychkov and Rashba[48]. It has also been demonstrated that the strength of the Rashba effect can be tuned using a gating voltage. This was first demonstrated in HgTe quantum wells in 1996[49] and InGaAs/InAlAs structures in 1997[50]. Since the spin orbit coupling due to the Rashba effect is related to the potential drop across an interface, it is possible to tune the strength through a gating voltage. Later, this idea was incorporated into the Datta-Das spin field effect transistor design[51], [52]. Rashba effect has since been demonstrated in heavy metal/ferromagnetic/oxide [45], [46], [53]–[58]. These spin orbit interactions remain a

heavily researched topic due to its potential applications in spintronics such as for magnetic logic or memory.

CHAPTER 3 NONLOCAL SPIN VALVES FOR ALL-SPIN LOGIC APPLICATIONS

3.1 INTRODUCTION

Nonlocal spin valves (NLSVs), which are introduced in section 2.4, are devices commonly used to study spin injection and transport in metallic and semiconductor systems. Recently, NLSVs have also been proposed as a building block for a type of spintronic logic called all-spin logic[12], [13]. NLSVs provide a way to generate and detect a spin signal using ferromagnets as well as transport the spin information using a nonmagnetic spin channel. This is appealing since it does not rely on the transfer of charge current and removes effects such as Joule heating and Oersted field generation.

There are several key factors that can affect the spin current, and in turn the nonlocal resistance signal in NLSVs. One significant parameter is the spin diffusion length of the channel material, λ_N. As the pure spin current passes through the channel, it has the possibility to undergo spin flipping. The smaller the spin diffusion length of the channel, λ_N, the more likely the spins are to lose their orientation, and the smaller the detected signal will be for a given spacing between ferromagnetic contacts. Another important factor is the spacing between the ferromagnetic contacts, L. Both of these parameters play a significant role in the NLSV since the spin current decays as $\exp(-L/\lambda_N)$.

The interface quality between the ferromagnet and nonmagnetic channel is also a key aspect to device performance. Not only is the quality of the interface such as roughness and impurities important to reduce the spin flip scattering at the interface, but previous results have shown that the insertion of a tunnel barrier can be used to increase the nonlocal

signal[59], [60]. For ohmic junctions without the insertion of a tunnel barrier, maximum ΔR_s is typically on the order of 1 mΩ. The insertion of a tunnel barrier is to help overcome the problem of conductivity mismatch, which is a well-known issue, especially in semiconductor devices. It has been experimentally demonstrated that the nonlocal signal can be increased by two orders of magnitude with the insertion of a tunnel barrier. Vogel, et al demonstrated this by inserting an aluminum oxide tunnel barrier between NiFe ferromagnets and an Al channel[60]. By changing the thickness of the Al_2O_3, they studied how the nonlocal resistance signal changes as a function of the conductivities of the cross-sectional area. Additional results with AlO_x tunnel barriers showing increased spin injection have also been demonstrated[61]–[64]. The use of MgO as a tunnel barrier with Py/Ag/Py lateral spin valves has also been demonstrated[65], [59]. By increasing the interface resistance from 0.0005 $\Omega\mu m^2$ to 0.2152 $\Omega\mu m^2$ through the insertion of the MgO tunnel barrier, an order of magnitude increase in non-local signal is achieved[59]. Similar results have been achieved in other studies for MgO tunnel barriers[65], [66].

In 2008, it was demonstrated that high spin accumulation signals could be achieved in structures using nanopillars in lateral spin valves[35]. This design is appealing for applications of all spin logic devices since it will be crucial for scaling of logic devices as well as allow better control over magnetic switching properties and reduce domain wall formations. This design can also help to reduce the amount of injected current required to achieve switching of the detected state. Such devices each consist of a copper channel with two Py ferromagnetic pillars contacted by gold electrodes. The Cu/Py/Au nanopillars are deposited using a shadow beam evaporation technique in vacuum to produce high quality

interfaces. The ferromagnet sizes are 80 nm x 170 nm and 75 nm x 170 nm with a spacing between the ferromagnets of 270 nm. The nonlocal resistance signal, ΔV/I, for these devices are as high as 21 mΩ at 10 K. For room temperature, ΔV/I is reduced by a factor of about 1/3 of the value at low temperature.

It is necessary for individual FMs to be reliably controlled and switched for logic applications. In order to ensure scalability, it is also desirable to do so using spin current rather than techniques such as externally applied field. It is possible to change the magnetization states of the detector using the injected current without any application of field in a similar way as spin transfer torque. This is important to all spin logic applications since current can be used as the driving mechanism, as opposed to utilizing externally generated fields which can limit scalability. When a larger current is passed through the injector device, a larger pure spin current will propagate through the channel and reach the detector side. The pure spin current will exert a torque through transfer of angular momentum to the detector ferromagnet. If the pure spin current is large enough, this torque will cause the magnetization direction to change. The required current to induce switching for lateral spin valve structures is given by the following equation[35]:

$$I_s = \frac{\alpha e M^2 V_{vol} \mu_0}{\hbar}$$

where α is the damping factor of the ferromagnetic material, e is the electronic charge, M is magnetization, V_{vol} is the volume of the ferromagnet, μ_0 is permeability in vacuum and $\hbar$ is Plank's constant.

Several cases of magnetization control using pure spin currents have since been demonstrated[63], [64], [67]. In Ref. [64], switching occurs with the application of a

varying DC current amplitude with the assistance of an external field. Ref. [67] demonstrates magnetization reversal in one direction or with the assistance of and external field, and dipolar interactions play a role in the switching of the magnetization in Ref. [63]. A significant factor affecting the ability to demonstrate pure spin current inducing magnetization reversal is the complex fabrication required to obtain small, individual FM pillars as opposed to multidomain FM strips.

In 2008, Yang, *et al.* demonstrated magnetization reversal due to torque generated from the pure spin current in NLSVs[59]. Using a shadow beam evaporation technique (described in more details in Section 3.2.2), a Cu channel and Py FMs are deposited. The resist mask is designed such that the Py FMs form individual nanopillars compared to the long FM strips commonly used in NLSVs. The Py FMs have dimensions of 80x170 nm and 75x170 nm for the injector and detector, respectively, and the channel width and thickness are 170 nm and 65 nm, respectively. A variable DC current is applied across the injector to the end of the channel and at a current of about 5mA (corresponding to a current density of 2.5×10^{10} A/m^2) and a sharp change in the nonlocal resistance signal is detected, indicating magnetization reversal due to the torque from the pure spin current. Since this demonstration, there have been no additional reports of complete magnetization reversal due to the pure spin current generated in a non-local spin valve. Fabrication difficulties in achieving nanopillar structures, control over interface quality and therefore the spin injection efficiency, and spin diffusion length are all challenges needed to be overcome to realize efficient magnetization reversal using the pure spin current.

3.2 All-Spin Logic Device

3.2.1 Device Proposal and Benchmarking

It has been proposed to use NLSV devices for logic applications in the form of all-spin logic devices(ASLD) in 2010[12], [13]. All-spin logic offers benefits of nonvolatility and built-in memory capabilities, potential for lower power consumption, transmission of data through pure spin current rather than charge current, and use of spin as the internal state variable which eliminates the need for spin-to-charge conversion at each stage of data transmission.

In ASLDs, it is proposed that the spin current generated in a NLSV structure can be used to exert a torque on a FM to cause magnetization reversal. This FM can in turn act as an input for the next stage of the logic operation, inject spin current, and result in switching of the next FM and so forth. The schematic design of the proposed ASLD unit is shown in Figure 3.1(a). An ASLD gate consists two FM regions connected by a spin channel, similar to a NLSV. One half of each interface between the FMs and channel consists of a tunneling layer which acts to help improve the spin injection as well as prevent back absorption of spins. There is also an isolation layer in the channel region below the FMs. The isolation layer and tunneling layers help to ensure that each half of the FM can be used as either an injector or detector. The half without the tunneling layer can easily absorb the spin current and be used as a detector while the half with a tunneling layer will prevent absorption and enhance spin injection. Additional design proposals for all-spin logic were proposed which contain inbuilt reciprocity were presented[13] to demonstrate how the issue of feedback can be addressed. In this way, it can be ensured that information in the logic system will be transmitted in one direction of the circuit. This ensures

nonreciprocal behavior and eliminates feedback of the logic circuit where it is ensured that the input will influence the output but the output state will not change the input state. By connecting multiple of these ASLD units together, different logic gates can be achieved and data can be transmitted throughout a circuit, such as shown in Figure 3.1(b).

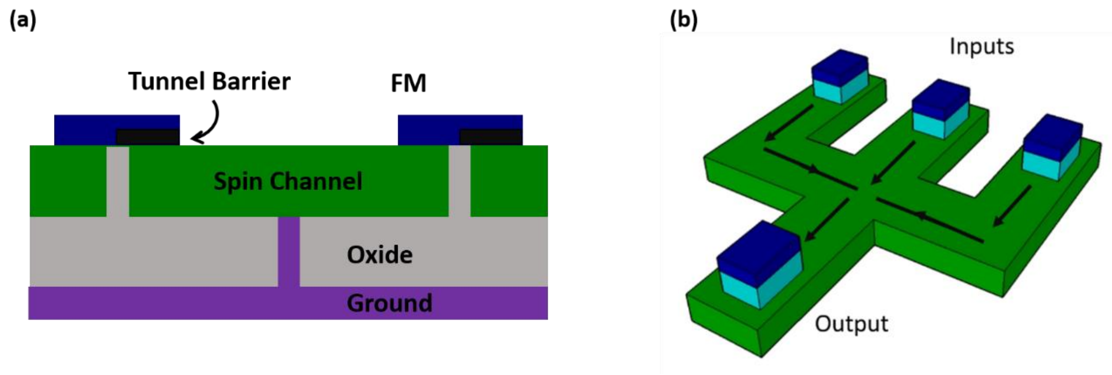

Figure 3.1 (a) Proposed design for an all-spin logic unit and (b) design for a majority logic gate based on multiple all-spin logic units connected together.

Achieving high signal levels with easy detection schemes is important for any future logic technologies. One drawback of typical NLSVs is a low signal level at room temperature and is typically on the order of a few mΩ. Furthermore, signals are commonly detected using methods such as lock-in amplifiers. For all-spin logic applications, it is possible to overcome these limitations by incorporating GMR or MTJ ferromagnetic pillars as opposed to the typical single ferromagnetic layers in lateral spin valves. Switching of the output states would still occur using spin transfer torque from the pure spin current, but instead of reading out the nonlocal resistance signal, the GMR or MTJ resistance signal could be used for readout of the output state. This will allow for higher signal levels and easier measurement techniques similar to magnetic random access memory.

Theoretical predictions show much promise for all spin logic in terms of energy consumption compared to current CMOS devices. In Ref. [68], three different designs for all-spin logic are considered and compared to 15nm technology node CMOS. They examine what is referred to as FEASL (functionality enhanced all-spin logic) for the cases of without a clocking field (NC), with a clocking field (C), and with a clocking field and biaxial anisotropy (CB). The FEASL design architecture uses majority logic functions to realize digital functions and low power, low delay, low area adder, and multiplier functions.

Based on simulation framework developed in Ref. [69], energy predictions were made for the three FEASL designs of NC, C, and CB. The simulation work combines transport behavior based on the Valet-Fert model with magnetization behavior based on the Landau-Lifshitz-Gilbert equation with spin-transfer torque. In Ref. [68], they chose to analyze the system using the discrete cosine transform (DCT) algorithm due to its wide use in digital signal processors. The results are compared to 15nm technology mode CMOS and show that FEASL with clocking can achieve the lowest power consumption while FEASL with clocking and biaxial anisotropy is most promising for applications requiring both low power and delay.

Additionally. Kim, *et al* performed a system level calculation for the power consumption of ASLD compared to CMOS for several different parameters used for ASLD. CMOS and ASLD based cores for a Core i7 processor were considered for the case of four cores active and one core active with 3 cores clock gated. It is predicted that for ASLD that use high polarization materials (which can potentially be achieved through the use of Heusler alloys) and hybrid interconnects of materials with spin diffusion lengths >1

μm (such as graphene), ASLDs can be competitive and even offer improvements over CMOS power consumption. This work demonstrates the system level capabilities of ASLDs and provides more insight into the energy comparison of ASLD and CMOS than can be achieved through comparison of individual gates.

These works provide initial predictions for the capabilities of all-spin logic devices and are valuable for evaluating its potential as a beyond-CMOS technology.

3.2.2 Fabrication Requirements for All-Spin Logic

Conventional fabrication approaches for NLSVs typically consist of bottom-up processes of either shadow-mask evaporation or lift-off processes. The simplified lift-off fabrication approach for lateral spin valves is shown in Figure 3.2(a). Typically, a patterning step (either photolithography or electron beam (e-beam) lithography) is first performed for the FM region. Then, the FM is deposited using e-beam evaporation. Once the resist is removed from the substrate, it removes the FM material over the resist region and leaves the FM in only the regions patterned to be the FM contacts. Then, a second patterning step is performed to define the channel region. A second step of e-beam evaporation is performed to deposit the channel and the resist is removed to leave only the defined channel region over the FM contacts. Additional lithography and deposition steps may be performed to form larger contacts for electrical testing. This process has the benefit of being able to directly pattern the FM and channel features in dimensions and geometries within the limitations of the lithography system. However, there is a limitation to the thicknesses of FM and channel films that can be used. Since one layer is being deposited over the other, it is necessary that the thickness of the top layer is thicker than the bottom

layer to ensure continuity of the top film over the edge of the second film. Another drawback is that the material depositions are performed in two steps. Interfacial properties play a key role in the spin injection efficiency and polarization of NLSV devices. Multi-step depositions that break vacuum between deposition steps can suffer from oxidation, contamination and impurities, and roughness which can significantly decrease device performance.

Shadow-beam evaporation provides an alternative bottom-up fabrication technique for NLSVs. A schematic process for shadow-beam evaporation is shown in Figure 3.2(b). With shadow-beam evaporation, a single resist mask is used for the patterning and deposition of both of the FMs and the channel regions. First, the FM regions are e-beam

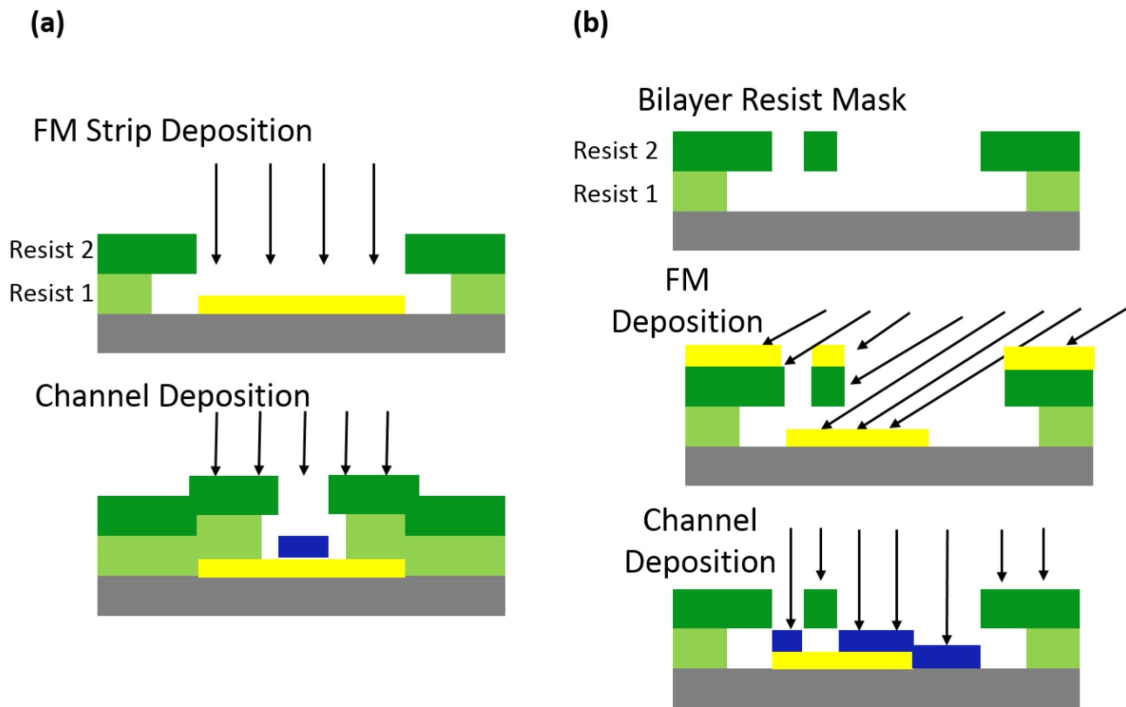

Figure 3.2 Bottom-up fabrication techniques commonly used for NLSV fabrication including (a) lift-off and (b) shadow beam evaporation.

evaporated at an angle. Next, the channel material is deposited at normal incidence. Due to the mask design and different angles of deposition, separate FM and channel regions are defined and the depositions can be done without breaking vacuum. This allows for cleaner interfaces and improved device performance. However, geometries of the final devices are limited by the mask and multi-angle deposition design and it is difficult to achieve highly scalable devices with this technique. Similar to the lift-off technique, film thicknesses are also limited due to the requirement to have significant step coverage for continuous films.

3.3 Development of a Top-Down Approach for Non-Local Lateral Spin Valves

3.3.1 Overview

In this section, a new fabrication approach for nonlocal lateral spin valves is developed. Developing this fabrication technique and demonstrating working devices is critical to future development of logic circuits which require complex layouts and geometries. Additionally, the top-down approach demonstrated here is compatible with current fabrication technologies and can be integrated with CMOS devices. The entire top-down NLSV fabrication process includes the following four main parts: 1) spin channel definition, 2) magnetic pillar definition, 3) pillar isolation and contact via formation, and 4) top electrode definition. The details of the procedure are given in the following sections.

3.3.2 Film Preparation

The entire film stack was deposited in a Shamrock sputtering system. The initially

deposited film stacks for which results are presented in this dissertation have a structure of Si/thermally oxidized SiO_2 (100 nm) substrate / MgO (3nm) / Cu (100 nm) / Co (20 nm) / Pd (3 nm). MgO is used to improve adhesion of the Cu film to the Si/SiO_2 substrate. Cu is chosen as the metallic spin channel due to Cu having a relatively large spin diffusion length of >300 nm at room temperature, and Pd is used as a capping layer to prevent oxidation of the magnetic material. All of the layers are deposited consecutively without breaking vacuum as opposed to conventional NLSV fabrication processes that rely on lift-off fabrication techniques as described in Section 3.2.2. This allows for a high level of control over the interface quality between layers which is critical to the operation of NLSV devices. Additionally, it paves the way for future development of more complex material stacks to be developed such as full GMR or MTJ stacks or magnetic materials that depend on interfacial anisotropy or specific crystalline structures.

Next, alignment marks are patterned and deposited on the sample in order to ensure alignment between the multiple steps of e-beam lithography required for the fabrication process. The alignment marks are patterned and Au is deposited to form the alignment marks. Au is chosen for the alignment marks since it has a high atomic number Z which provides good contrast for detection in the Vistec system. After solvent cleaning of the sample, a prebake is done at 150°C for 2 minutes to remove any residual moisture. Then, polydimethylglutarimide (PMGI) SF9 resist is spun on the sample at 5000 RPM for 60 seconds corresponding to a resist thickness of ~550 nm. A second bake is done at 150°C for 5 minutes in order to remove solvent from the PMGI SF9 resist. Then, C4 495 polymethyl methacrylate (PMMA, with 4% chlorobenzene solvent) resist is spun on the

sample at 3000 RPM for 60 seconds corresponding to a resist thickness of ~330 nm. An additional bake is done at 180°C for 2 minutes to remove solvent from the resist. For the resist exposure, a Vistec e-beam system with 100keV accelerating voltage is used. The resist is exposed at a dose of 1350 to 1475 $\mu C/cm^2$ depending on the feature size being exposed. After exposure, the resist is developed in two steps. First, the PMMA layer is developed in MIBK:IPA 1:3 for 25 seconds and then rinsed in IPA for 60 seconds. After drying the sample with N_2, the PMGI layer is developed in CD26:DI 3:2 for 40 seconds and then rinsed in DI for 60 seconds. Then, an O_2 plasma clean is performed in a parallel plate reactive ion etcher (either a Surface Technologies System, STS, or Advanced Vacuum, AV, system) for 8 seconds to remove any residual resist from the patterned area. E-beam evaporation is performed in either a CHA or Temescal evaporation system. 10 nm of Ti is first deposited at a rate of 1 Å/sec as an adhesion layer followed by 100 nm of Au deposited at a rate of 3 Å/sec. After deposition, the resist is removed in a n-methyl-2-pyrrolidone (NMP) based remover for 1 hour on a hotplate set at 110°C for ~1 hour followed by ~10 minutes in a sonicator.

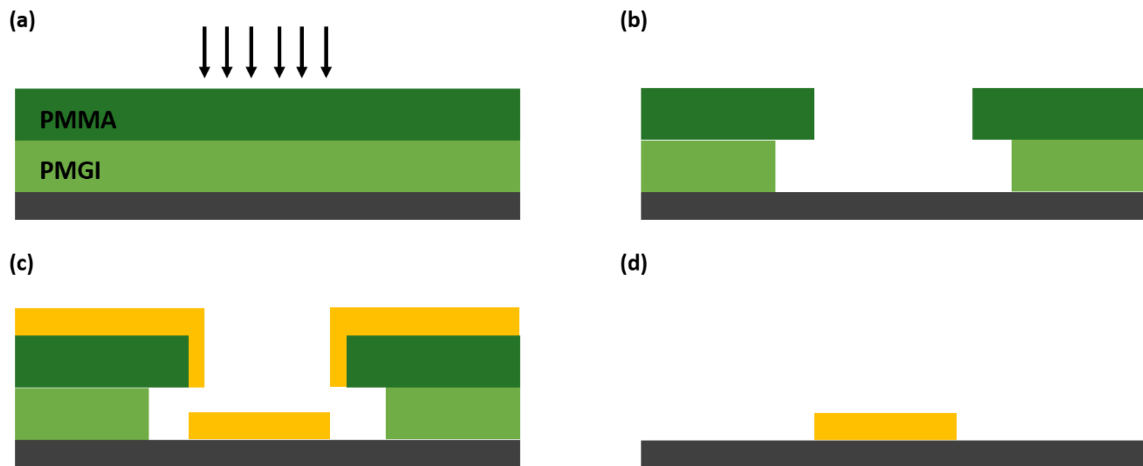

Figure 3.3 PMGI/PMMA bilayer resist process. After spinning on and baking of resist (a) the bilayer resist is exposed and (b) developed in two different steps to achieve an undercut of the bottom PMGI layer. (c) During the metal deposition, sidewall coverage is reduced and (d) the resist is removed and metal lifted off, resulting in a patterned feature depending on the pattern transferred from the top PMMA layer.

The PMGI/PMMA bilayer positive resist process used here and in later steps allows for high resolution patterning as well as clean lift-off for metals deposited after resist patterning. A schematic process of the bilayer patterning, lift-off and resist removal process is shown in Figure 3.3. The PMMA layer is used as the pattern transfer layer and defines the geometry of the features (Figure 3.3(a)). After development of the PMMA, the PMGI layer is developed so that it is slightly more developed than the PMMA layer to create an undercut (Figure 3.3(b)). During the metal deposition, side will coverage can occur which makes lift-off processes difficult. By introducing the undercut from the PMGI layer, this reduces sidewall coverage and creates a space between the deposited metal and PMGI under layer (Figure 3.3(c)) allowing the resist removal agent to reach the resist and aid in

the lift-off process. The final result is shown in Figure 3.3(d).

3.3.3 Defining the Channel

The channel is patterned using negative ma-N 2403 resist and ion milling to define the channel region as schematically demonstrated in Figure 3.4(b). First, the sample is prebaked at 110°C for 60 seconds to remove moisture from the surface of the sample. Next, ma-N 2403 resist is spun on the sample at 5000 RPM for 60 seconds resulting in a resist thickness of ~390 nm. The sample is then baked at 90°C for 60 seconds to remove solvent from the resist. E-beam lithography exposure is performed with the Vistec system and an exposure dose of 750 μC/cm2 is used. Channels with length of 5 μm and varying widths from 100 nm to 500 nm were patterned. After exposure, the resist is developed in MF-319 for 70 seconds followed by DI water rinse for 60 seconds. The resist acts as the etch mask and the channel region is etched with an Intelvac Ar^{+} ion milling system. The sample is milled at an incident angle of 15° for 13 minutes to pattern the channel region. After etching of the channel region, the ma-N 2403 resist is removed in 1165 at 110°C for ~1 hour followed by ~10 minutes in the sonicator (Figure 3.4(c)).

3.3.4 Defining the Magnetic Pillars

Negative MaN-2403 resist and ion milling are used again to pattern and define the pillars. The same resist preparation for the channel region described above is performed for the pillars. An exposure dose of 825 μC/cm2 is used for patterning of the pillars. Pillars of sizes varying from 75 x 100 nm to Figure 450 x 500 nm are patterned. The same development process as described above for the channel region is used. After development,

the magnetic pillars are etched using Ar^+ ion milling at an incident angle of 15° for 11 minutes (Figure 3.4(d)). In order to ensure the entire magnetic stack is etched, the device is slightly over-etched into the Cu channel. This step introduces concerns about surface defects at the spin channel interface and implantation of magnetic impurities in the channel which would result in increased scattering events causing a significant reduction in spin diffusion length and therefore NLSV signal. Before the e-beam resist is removed, SiO_2 is deposited using a Varian e-beam evaporation system to isolate the pillars, prevent oxidation of the magnetic materials and channel, and to prevent shorting between top electrodes and the channel, as shown in Figure 3.4(e). To ensure the SiO_2 is sufficient to provide complete step coverage over the channel region, 150 nm of SiO_2 is deposited, and the deposition is performed at a rate of 2 Å/sec. The e-beam resist is then removed and SiO2 lifted off from the tops of the pillars to expose the tops of the pillars for electrical contact (Figure 3.4(f)). For the lift-off process, an NMP based solution is used heated on a hot plate to 110°C for ~12 hours followed by ~10 minutes in a sonicator. Additionally, a foam brush may be used to gently brush the sample to assist with the lift-off process followed by additional time in the sonicator.

3.3.5 Via Formation

In order to make electrical contact to the channel region, it is necessary to pattern and etch vias through the SiO_2 in the contact region. E-beam lithography and RIE is performed to pattern vias as shown in Figure 3.4(g). Positive PMGI/PMMA bilayer resist prepared as described above in Section 3.3.2 for patterning of the via regions. Exposure is performed with the Vistec e-beam lithography system using a dose of 1400 $\mu C/cm^2$. The

resist is developed as described previously (Figure 3.4(g)). Following development of the resist, RIE using the STS etcher is performed. The gas species used were 70 sccm Ar, 47 sccm CF4, and 5 sccm CHF3 at a pressure of 75 mTorr and power of 100 W and was etched for 6 min and 30 sec. The recipe selectively etches the SiO_2 while not having a significant impact on the Cu channel region. After RIE of the contact vias, the resist is removed in NMP:Acetone 1:1 in the ultrasonic for ~15 minutes heated to 50°C(Figure 3.4(h).

3.3.6 Top Electrode Patterning and Deposition

A final step of e-beam lithography is performed to pattern the top electrodes. Bilayer PMGI/PMMA resist is prepared as described 3.3.2. Precise alignment within 50 nm between the electrodes and magnetic pillars is required to ensure electrical contact to the magnetic pillars. The electrodes are exposed at two different doses of 1400 and 1200 μC/cm2 for the narrow electrode contact region and larger electrode pads for electrical probe contacts, respectively. Following the development procedure outlined for the alignment marks in the previous section, O_2 plasma RIE is again performed to remove any residual resist from the contact region. Then, e-beam evaporation is performed to deposit Ti (20nm) at a rate of 1 Å/sec followed by Au (120 nm) at a rate of 3 Å/sec for the top electrodes. Lift-off is performed in NMP at 110°C for ~ 1 hour followed by ~10 minutes in the sonicator (Figure 3.4(i)). Scanning electron microscope (SEM) images of the fabricated devices are shown the device electrical contacts in Figure 3.5(a) as well as high magnification images showing the individual top electrodes, channel, and FMs for 175 nm x 200 nm and 200 m x 225 nm FM injector and detector in Figure 3.5(b) as well as for 400 nm x 500 nm and 460 nm x 500 nm FM injector and detector in Figure 3.5(c).

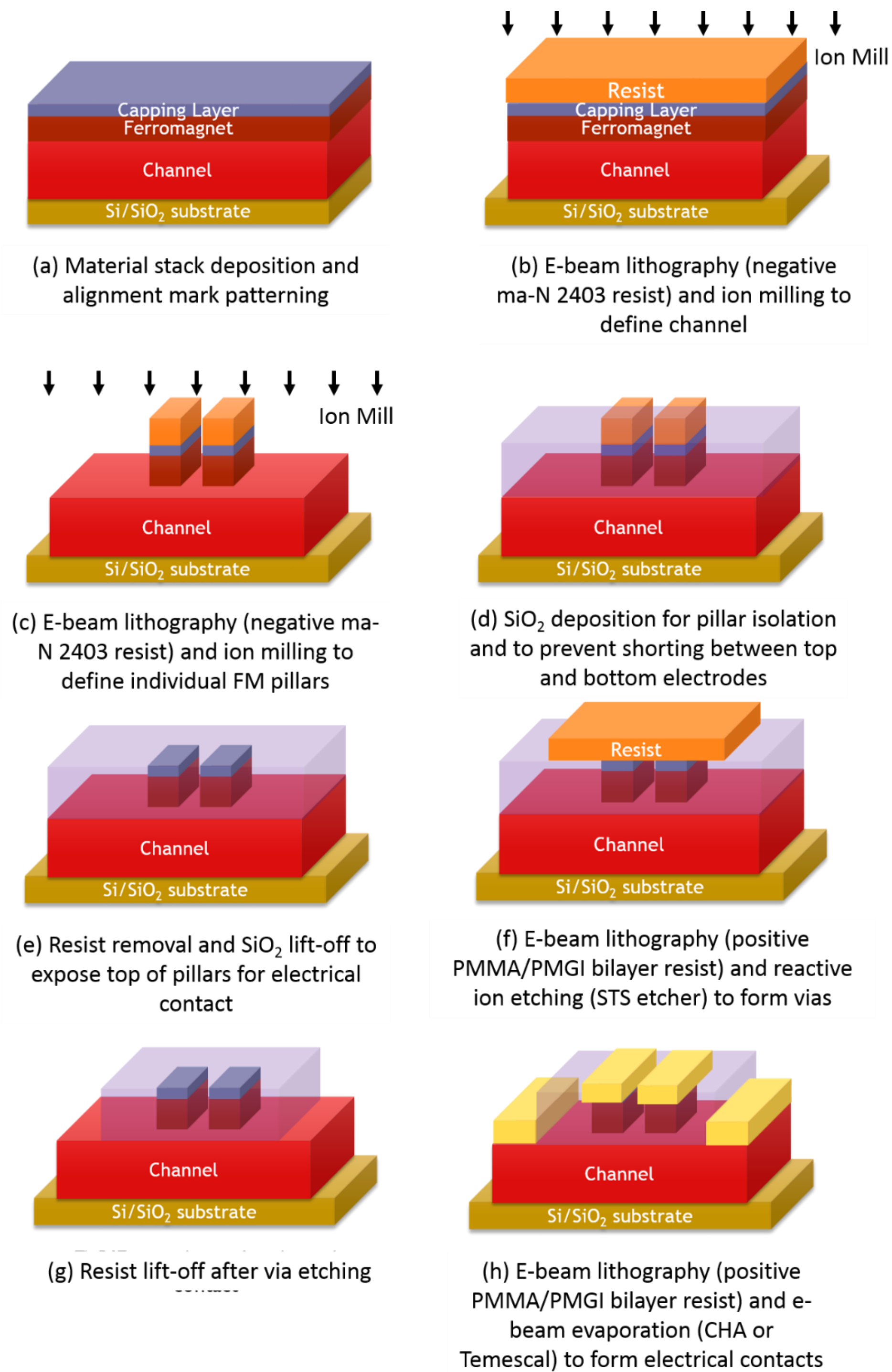

Figure 3.4 Top-down fabrication flow for patterning of NLSV devices with defined channel and nanopillar dimensions.

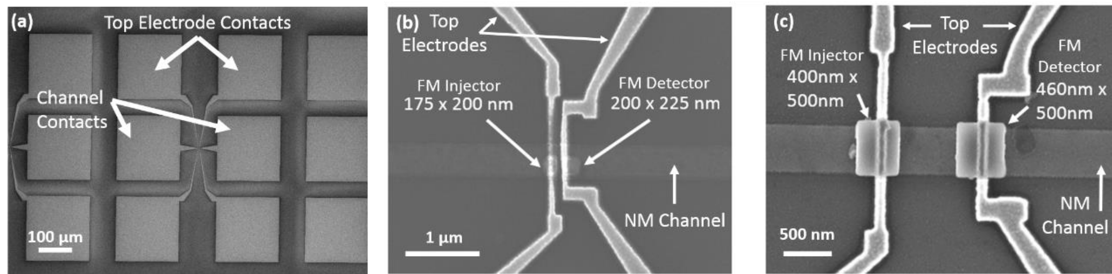

Figure 3.5 SEM images of NLSVs fabricated with the top-down approach showing (a) device contact pads for electrical measurement and (b,c) individual patterned NM spin channel, injector and detector FMs, and top electrodes.

3.4 Electrical Characterization

3.4.1 Electrical Characterization Techniques

Using a nonlocal measurement setup and sweeping an external in-plane field, a non-local voltage signal corresponding to the parallel and antiparallel orientations of the two FM nanopillars is observed. For the non-local measurement, a Keithley 6221 current source is used for injection of current and generation of the pure spin current. The current is applied across the top electrode for FM1 to the end of the channel as shown in Figure 3.6(a). A nanovoltmeter was used for detection of the non-local signal due to the diffusion of the pure spin current diffusion between FM1 and FM2. An external magnetic field is applied along the long (easy) axis of the ferromagnetic nanopillars and the amplitude of the field is swept during the measurement. When the alignment of FM1 and FM2 changes from parallel to antiparallel due to the application of the external field, a decrease in the NLSV signal is expected. As the applied field is further increased, the alignment of FM1 and FM2 changes back to a

parallel configuration and results in an increase in the NSLV signal again and the same behavior happens as the applied field sweep is reversed. A schematic illustration demonstrating what a typical NLSV signal looks like and the corresponding magnetization orientations is shown in Figure 3.6(b).

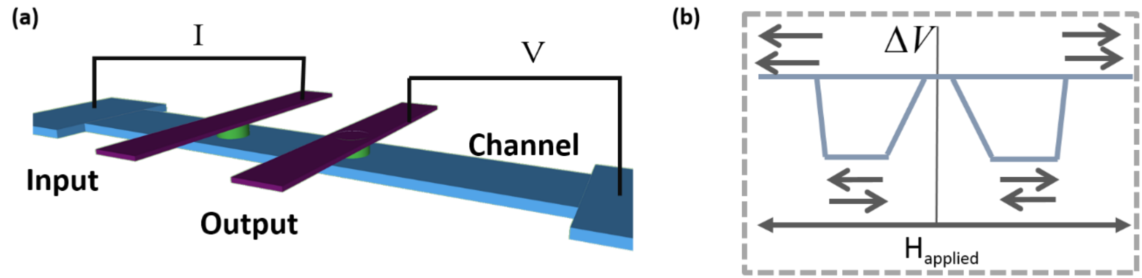

Figure 3.6 (a) Testing set-up for NLSV measurement of nanopillar devices and (b) schematic representation of a typical NLSV signal showing different signal levels and corresponding relative magnetization states.

3.4.2 Results and Discussion

For our experiment, we fabricated FM pillars of sizes 75 nm x 100 nm to 450 nm x 500 nm. Accurate alignment is required between the four main e-beam lithography steps of the device fabrication in order to ensure contact between the channel, magnetic pillars, and individual top electrodes for each magnetic pillar as can be seen in Figure 3.5.

Results for a 175 nm x 200 nm and 200 nm x 225 nm injector and detector with an edge to edge spacing of 500 nm are shown in Figure 3.7. A current density of 1.4×10^7 A/cm^2 (corresponding to a charge current injection of 5 mA) was applied for the measurements. Figure 3.7(a) and (b) correspond to measurements taken at room temperature and 60K, respectively. It is seen that at room temperature, the non-local signal

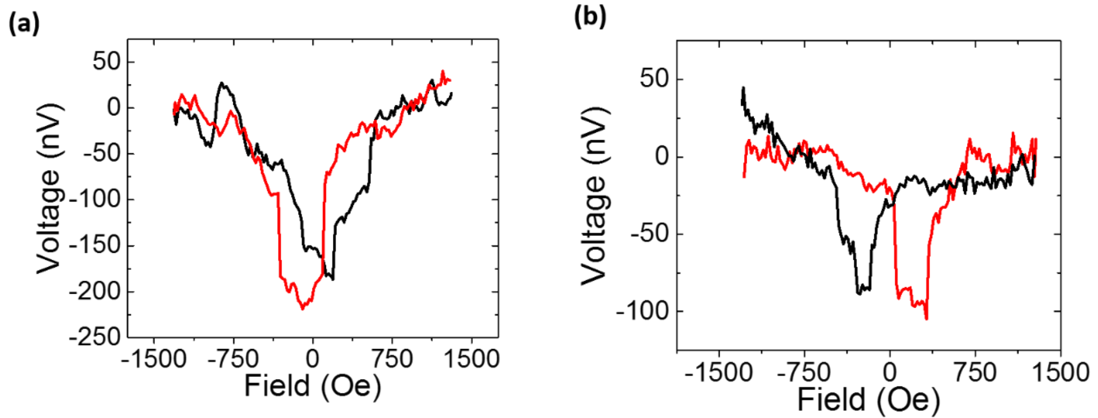

Figure 3.7 NLSV signal for a device with FM1 and FM 2 dimensions of 175 x 200 nm and 200 x 225 nm, respectively and a spacing of 500 nm measured at (a) room temperature and (b) 60K.

is about half of that at 60K. This temperature dependence of the NLSV signal is well documented and can be attributed to the increase in the spin-relaxation rate with increasing temperature[24].

The switching behavior of our devices shows magnetization reversal beginning before the externally applied magnetic field polarity changes and a gradual change in the non-local signal as seen in Figure 3.7, as opposed to the sharp switching typically observed in other studies. This is hypothesized to be due to the low aspect ratio of the FM nanopillars in the FMs in contrast to the very high aspect ratio FM strips in most other studies. Due to the low aspect ratio (as low as ~1.1 in some devices), it is possible that there are not well-defined easy and hard axes and therefore a lack of strong preference of magnetic orientation direction in the plane of the field. This can result in the rotation of the magnetization before reaching the opposite polarity of applied external field. To verify this in our devices, we repeated the measurement with the external magnetic field applied along the nominal hard

axis of the nanopillars for a device with pillars of 400 nm x 500 nm and 440 nm x 500 nm with a spacing of 430 nm at room temperature. Figure 3.8 shows the switching results for the magnetic field applied along the hard axis of the devices. As seen from the results, very similar behavior is observed for the nonlocal signal whether the external field is applied along the easy or hard axis. Since a NLSV signal is still observed when the field is applied along the hard axis, this also indicated that the magnetization direction can be aligned along that axis. It is predicted that this issue can easily be overcome in future devices by changing the FM nanopillar shapes to have a high aspect ratio, therefore increasing the shape anisotropy and resulting in well-defined easy and hard axes. Future studies are incorporating higher aspect ratio devices to further investigate the properties of the NLSVs fabricated using the top-down fabrication method such as spin diffusion length, spin injection efficiency, scaling effects, and pure spin current induced switching. The etch-back fabrication approach described here enabled the patterning sub 100 nm nonlocal spin valve devices with nanopillars.

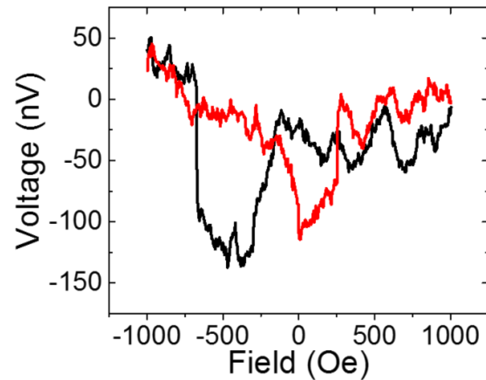

Figure 3.8 NLSV signal for device with dimensions of FM1 and FM2 of 400 x 500 nm and 440 x 500 nm measured at room temperature with the external field applied along the hard axis of the FMs.

3.5 SUMMARY

We have demonstrated a new fabrication approach for nonlocal lateral spin valve devices with applications for all-spin logic. We fabricated devices with pillar sizes ranging from 75 nm x 100 nm to 450 nm x 500 nm with various spacing. Room temperature results of the NLSVs show correct operation and verify this fabrication method as a valid approach for NLSV applications. It confirms that fabrication steps such as ion milling the magnetic material and stopping on the spin channel does not have a detrimental effect on the device operation. The fabrication process described in this paper allows for the entire material stack to be deposited under vacuum followed by a series of patterning, etching, and deposition steps to form FM nanopillar structures on a defined channel. The process will allow for the control of device dimensions and help improve scalability. This method also provides a fabrication process that is compatible with current industry methods and should allow for easier integration with CMOS devices or current read-head fabrication processes.

CHAPTER 4 SPIN HALL EFFECT

4.1 INTRODUCTION

4.1.1 *Spin Hall Effect Background and Motivation*

Spin orbit torques (SOTs) provide an alternative option for the manipulation of magnetization compared to conventional spin transfer torque (STT) generated from the transfer of angular momentum of spin polarized electrons passing through magnetic layers (as described in Section 2.3). Unlike STT, which relies on a magnetic layer for spin polarization and a transfer of spin, angular momentum from spin polarized electrons to an additional magnetic layer which results in a change of magnetization, SOT arises from spin polarization generated in a non-magnetic layer and ferromagnetic exchange coupling between the spin polarized electrons and magnetic layer. The torque generated from the non-equilibrium spin states at the interface act as an effective magnetic field whose orientation depends on the source of the SOT. With SOTs, it is possible to change magnetization orientations without passing charge current through a magnetic layer. While the presence of SOTs is well known, there is still a lack of understanding of the different origins and magnitude of contribution due to different mechanisms contributing to SOTs.

One contribution to SOTs is the spin Hall effect, which has gained significant interest since the demonstration of large spin Hall angles in heavy metals such as Ta[70][71][72], W[73], and Pt[71][74][58] as well as other 4d and 5d transition metals such as Pd, Nb, and Mo[71]. The spin Hall effect is a method utilizing spin-orbit interactions to generate a spin current by passing a charge current through a spin Hall

material. The generated spin current can then be used to exert a torque on an adjacent magnetic material and result in changes in the magnetization direction. When charge current is passed through a material with large spin orbit interactions, spins of opposite orientation are deflected in opposite directions. This results in a spin imbalance and effective spin current transverse to the applied charge current

The spin Hall effect has been demonstrated in both in-plane[70] and perpendicular materials. However, complete magnetization reversal can only be achieved in in-plane structures unless external fields or unique design criteria are implemented. Perpendicular materials require an additional effect such as an external field or STT for magnetization switching since the in-plane torque produced from the SOT interactions cannot induce deterministic switching itself for perpendicular materials[57], [58]. In general, application of an external field is required for switching of perpendicular magnetization through spin orbit interactions generated from the spin Hall effect. There have been several proposed methods to achieve switching in perpendicular materials without the assistance of an externally applied field[75], [76]. In these designs, a wedge structure is utilized to achieve external-field free switching; however, this limits scalability as it will become increasingly difficult to create and reliably control the wedge structure at required dimensions for high density and at wafer level. The wedge structure also creates difficulties in creating more complex material stacks such as for magnetic tunnel junctions.

4.1.2 Motivation for Spin Hall Effect Logic and Memory Devices

Spin orbit torques (SOTs) provide an additional method for switching magnetization direction and have been proposed for magnetic random access memory

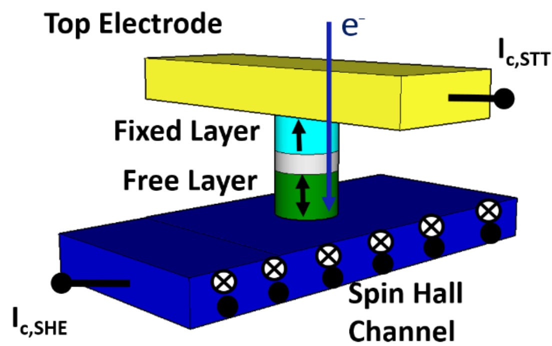

Figure 4.1 Schematic design of an MTJ integrated with a spin Hall channel for switching of magnetization using spin orbit interactions combined with spin transfer torque.

applications[77], [78]. Combining SOT with STT in MTJ devices provides a solution to overcome many of the issues with MTJ devices. A schematic design of a MTJ utilizing both SOT and STT for switching is shown in Figure 4.1. SOT exerted by an additional spin-orbit lead placed in contact with the device storage layer provides an additional torque that may lead to lower power consumption and a reduction in the amount of current applied across the tunnel barrier, thus increasing device lifetime. Due to the direction of the torque generated from spin orbit interactions, the incubation delay in switching is reduced and fast switching speeds can be achieved. It has also been theoretically demonstrated that at short pulse widths, SOT may be more beneficial for power consumption[79]. However, there are gaps in the fundamental understanding of how SOTs and the magnetization dynamics are influenced by SOT when combined with spin transfer torques in MTJs, knowledge gaps that must be filled for these devices to be used in computing applications.

Spin transfer torque generated in an MTJ structure by passing a charge current across the MTJ is one method to achieve deterministic switching in perpendicular magnets combined with SOT. Combining SOT with STT switching in MTJs has many advantages

compared to switching based only on SOT or STT. Incorporating MTJs with SOT allows for magnetoresistive readout as opposed to the anomalous Hall effect which is commonly used for measuring changes in perpendicular magnetization for spin Hall. This provides a more scalable approach as well as large signal levels. Another significant advantage for SOT STT MTJs is that the read and write paths can be separated which results in a lower read write disturbance and can enhance device reliability. Using the combined effects, it is possible to switch perpendicular magnetization, which cannot be achieved by the spin Hall effect alone. Due to the torque generated from SOT, the required current passing through the MTJ to generate the STT in order to achieve switching is reduced. This reduces the amount of current passing across the tunnel barrier of the device and allows for a portion of the current to pass through a lower resistive path. Additionally, it will reduce the chance of tunnel barrier breakdown of the MTJs and enhance device endurance and lifetime.

Multiple theoretical studies have been done that explore the performance benefits of SOT-STT MTJ devices. It has been shown that the orthogonal direction of SOT in perpendicular MTJ structures reduces the amount of magnetization precession, resulting in a much shorter incubation delay[77]. The magnetization dynamics are simulated and shown for the cases of a) a DC current for STT only, b) 0.5 ns pulse current for SHE only and c) STT combined with SHE. The corresponding magnetization in the **z** direction as a function of time is also presented and indicates that a combination of SHE with STT can significantly reduce the amount of time needed for switching perpendicular magnetization. It is theoretically shown that SOT combined with STT can result in four times faster switching than STT alone due to this reduction in the incubation delay. It is also predicted

that for write speeds of 1 ns, using SOT-STT, the current across the tunnel barrier can be reduced by up to eight times which results in a 50 times decrease in the overall write energy for the structure.

Switching of perpendicular magnetization with spin Hall effect and an external field has been demonstrated to occur at speeds of less than 200 ps[80]; however, this has yet to be shown combined with STT and without the assistance of an external field. Other simulation studies have looked at different amplitudes and pulse widths of applied current for SOT and STT to see what combinations are required to achieve certain probabilities of switching [77], [78], [81]. Modeling work done by Wang, et al., has shown that for a 4-terminal MTJ device, magnetization switching can be achieved with SOT combined with STT with 456 fJ of energy for a delay time of 2.5 ns[81]. The same device was also modeled for STT switching only and for an equivalent delay time, 1.01 pJ is required for writing. This demonstrated the possible energy benefits of SOT STT MTJs compared to conventional STT MTJs.

Lee, et al., analytically determined how the thermal energy barrier differs for SOT-activated MTJs from conventional STT MTJs, giving an important physical understanding of how these additional torques change the thermal stability, switching energy, and switching probability in MTJ devices[79]. They showed that while conventional STT MTJs thermal energy barriers exhibit a quadratic dependence as the pulse width is reduced on a log scale, the thermal energy barrier of SOT MTJs has a linear behavior. Based on the results presented, at sub-2 ns write times, it becomes more energy favorable to rely on SOT currents for switching rather than STT. However, all of these performance factors have yet

to be demonstrated experimentally.

4.2 Spin Hall effect in Bulk Perpendicular Ta/TbFeCo Bilayers

4.2.1 Motivation

In this section, spin-orbit torques are studied in Ta/TbFeCo patterned structures with a bulk perpendicular magnetic anisotropy (bulk-PMA) for the first time. This work is used to initially demonstrate the spin Hall effect in our research group and lay the foundation for future studies.

Recently, current-induced spin-orbit torques have been intensively studied in magnetic ultra-thin films due to their potential for memory and logic devices[70], [73], [74], [77], [82]. Researchers have reported that the magnetization of ferromagnetic structures with interfacial perpendicular magnetic anisotropy (PMA) including Pt/Co/Oxide[57], [74], [83], [84], Pt/Co/Pt[85], Ta / CoFeB / MgO [54], [86]–[89], and Ta / CoFe / MgO [90] can be switched by in-plane current-induced spin-orbit torques (SOT), namely, the spin Hall effect (SHE) and the Rashba effect. SHE provides an efficient way of generating spin current that provides potential to significantly reduce the current required for switching PMA nanomagnets. However, interfacial PMA typically suffers from lower perpendicular anisotropy values and is usually not strong enough to preserve the thermal stability of nanomagnets for applications in memory and logic devices at sub-20 nm[91]. Although different methods have been developed to enhance the interfacial PMA[92], [93], bulk PMA materials, including L10-ordered alloys (FePt, FePd, CoPt, etc.)[94], [95], and Heusler alloys[96], [97], exhibit a much larger anisotropy ($\sim 10^7$

erg/cm^3) and therefore higher thermal stabilities; however, the manipulation of magnetization with bulk-PMA using SOT has only been studied in a limited number of cases[98].

The utilization of bulk-PMA materials in SOT/spin Hall systems also has unique advantages for understanding the underlying physics of SOT. In SOT systems, the contributions of the interfacial effects such as the Rashba effect and the bulk effects such as the spin Hall effect are controversial and not well understood[58], [74], [99]. In magnetic materials with bulk-PMA, magnetic anisotropy originates from the bulk rather than the interface; hence, it is a suitable system for investigation of SOT. On the contrary to the interfacial-PMA structures, the materials with bulk-PMA are much more robust to thickness or interface variation. This makes it possible to do a comparison study with the same bulk-PMA material and different heavy metals. Additionally, it also enables the study of changing the thickness of the magnetic layer, which is restricted when using interfacial-PMA structures.

In this section, spin Hall effect induced switching of perpendicular magnetization which relies on crystalline anisotropy rather than interfacial anisotropy to achieve the perpendicular magnetization is demonstrated. Ta/TbFeCo structures are used to study the magnetization switching in materials with strong intrinsic perpendicular anisotropy. Additionally, in this study, the development of the sputtering process for Ta films exhibiting strong spin orbit interactions paves the way for experiments relying on the spin Hall effect presented in later sections of this dissertation. The current-induced magnetization switching is investigated in the presence of a perpendicular field, a

longitudinal in-plane field, or a transverse in-plane field and determine the strength of the associated spin Hall effect in this material system.

4.2.2 Film Preparation and Device Fabrication

The films are deposited on a thermally oxidized silicon wafer with 100 nm of SiO_2. DC and RF magnetron sputtering is used to deposit the film stacks at room temperature. The film stack consists of, from the substrate, Ta (5 nm) / $Tb_{20}Fe_{64}Co_{16}$ (1.8 nm) / MgO (2 nm) / Ta (4 nm) shown schematically in Figure 4.2(a). A ternary alloy target is used for the deposition of the TbFeCo layer. The composition of the TbFeCo is determined using Rutherford backscattering spectrometry and x-ray photoelectron spectrometry measurements. The as-deposited films demonstrate a strong perpendicular anisotropy as shown in Figure 4.2(b). The 1.8 nm-thick TbFeCo film shows a square hysteresis loop in the out-of-plane direction indicating a perpendicular magnetic anisotropy with a coercivity field H_C = 70 Oe. The in-plane hysteresis loop is saturated at about 10 kOe indicating a strong perpendicular anisotropy field of 1.5 T. With the thickness of TbFeCo increasing, the PMA is maintained with good and sharp switching from the VSM measurements and the coercivity increases with increasing TbFeCo thickness, which is characteristic of bulk PMA materials.

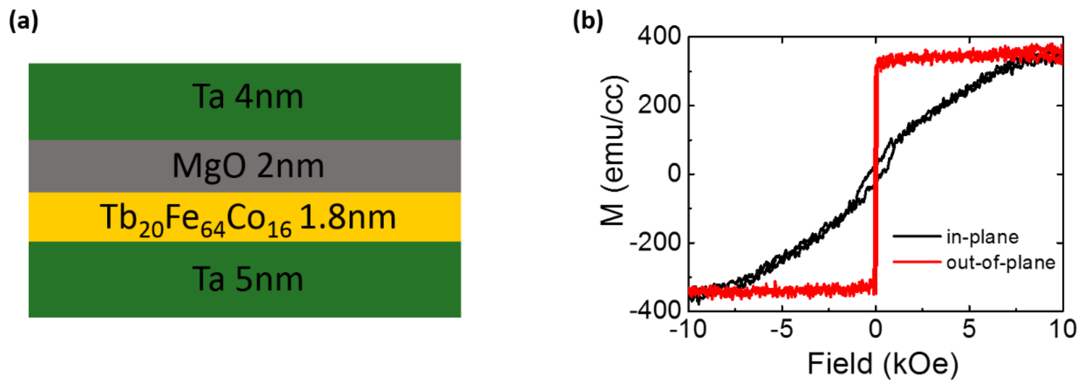

Figure 4.2 (a) Thin film material stack for bulk perpendicular spin Hall effect device and (b) VSM results confirming perpendicular magnetic anisotropy of the thin film sample.

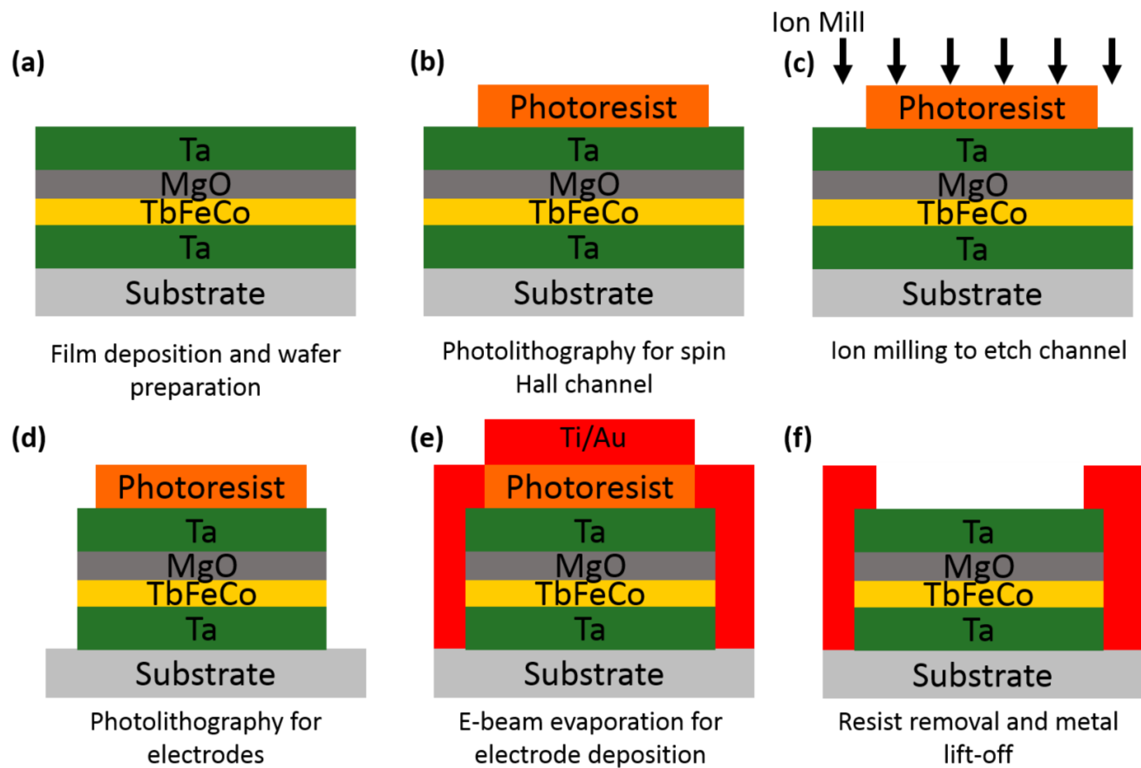

Figure 4.3 Fabrication flow for patterning of spin Hall effect devices.

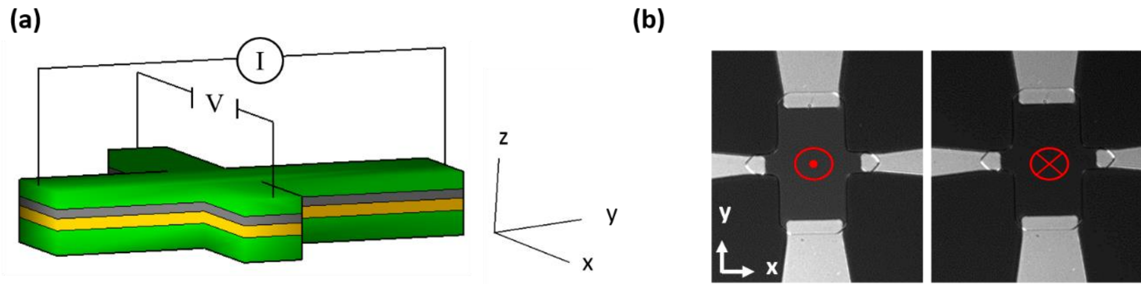

Figure 4.4 (a) Schematic design of spin Hall device with Ta spin Hall channel and TbFeCo ferromagnet showing electrical measurement set-up and (b) magneto-optical Kerr image of the Hall bar where the dark and bright contrast correspond to the magnetization direction pointing upward and downward, respectively.

For the device fabrication, the film stack is patterned into Hall bars with a width of 10 µm and length of 65 µm using optical lithography and Ar-ion etching. The fabrication process is shown in Figure 4.3. After the film deposition (Figure 4.3(a)), the sample undergoes a solvent cleaning process. Then, the sample is prebaked at 200°C for 5 minutes. Next, negative NR71-1500P resist is spun on the sample at 300 rpm for 3 seconds followed by 3000 rpm for 45 seconds. The sample is then baked at 150°C for 1 minute. The sample is exposed using photolithography for 30 seconds. After exposure, a post-exposure bake is performed at 100°C for 70 seconds to complete the cross-linking process of the resist that is initiated during the exposure. The sample is then developed in RD6 for 15 seconds(Figure 4.3(b)). Then the sample is etched to the Si / SiO_2 substrate using ion milling to define the Hall bars(Figure 4.3(c)). After resist removal, the electrical contacts are patterned using photolithography. The sample is prebaked at 115°C for 60 seconds. Microposit S1813 resist is then spun on at 4000 rpm for 30 seconds followed by a bake at

110°C for 60 seconds. After exposure, the resist is developed in 351 Developer:DI 1:5 for 30 seconds(Figure 4.3(d)). Electrodes are deposited using an e-beam evaporation system and 10 nm of Ti followed by 100 nm of Au is deposited for the electrodes(Figure 4.3(e)). The resist is then removed and results in the structure in Figure 4.3(f). Figure 4.4(a) shows a schematic of the device and Figure 4.4(b) shows the optical Kerr image of a fabricated device for the two magnetization directions perpendicular to the plane of the film. The brightness of the color reflects the direction of the magnetization which is pointing along the +z axis (left image) or the -z axis (right image).

4.2.3 Electrical Characterization Techniques

For the electrical device measurements, a DC current, I, is injected into the Hall bar along the longitudinal direction (y direction) using a Keithley 6221 current source, and the anomalous Hall voltage (V_H) is detected by a nano-voltmeter in the transverse direction (x direction) (Figure 4.4(a)). The anomalous Hall resistance, $R_H = V_H/I$, is proportional to the perpendicular component of the magnetization, M_Z, and is measured to determine the magnetization direction of the TbFeCo layer. During the measurement, an external field generated from an electromagnet is applied either perpendicular to the plane of the film (± z), transverse (± x) or longitudinal (± y). Both DC current measurements as well as pulse current measurements are conducted. A schematic image of the electrical testing set-up is shown in Figure 4.4(a).

4.2.4 Results and Discussion

First, the changes in the hysteresis loop while gradually changing the current is

studied. The anomalous Hall resistance is measured as a function of perpendicular magnetic field, H_z, for different amplitudes of injected DC current. When the current flowing through the device is less than 0.5 mA, a square hysteresis loop with coercivity of 240 Oe and a Hall resistance with the amplitude of 4.0 Ω is obtained. Once the current is increased to 8 mA, the coercivity reduces dramatically to 50 Oe, and the amplitude of R_H also decreases to 3.65 Ω. The reduction of both the coercivity and the Hall resistance results from the increase of current-induced torque related with the spin Hall effect expressed as

$$\tau_{\parallel} = \tau_{\parallel}^{0}\boldsymbol{m} \times (\boldsymbol{m} \times \hat{\boldsymbol{\sigma}})$$

where $\hat{\boldsymbol{\sigma}}$ denotes the spin polarization unit vector, and the magnitude of the torque is $\tau_{\parallel}^{0} = \frac{\hbar}{2eM_s t}|J_s|$, where J_s represents the spin current. For a positive charge current flowing through the Hall bar (along +y), $\tau_{\parallel}$ is along +x. The resulting torque tilts the magnetization from the z direction towards the y direction in the y-z plane and decreases the energy barrier

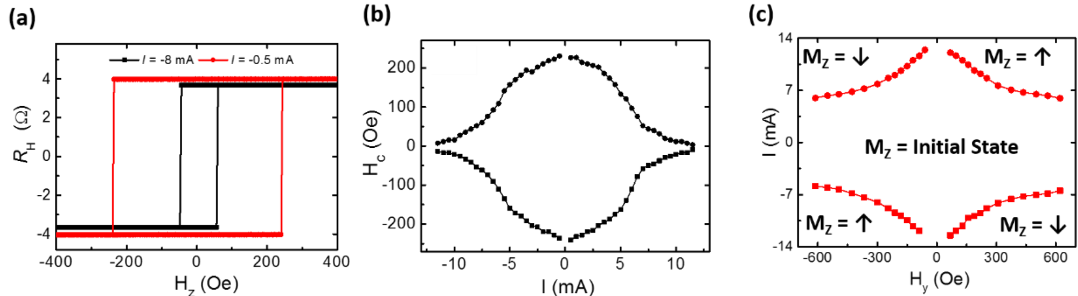

Figure 4.5(a) RH results under application of a perpendicular external field for -0.5 mA and -8 mA current applied to the spin Hall channel. (b) Coercivity dependence on spin Hall channel current for externally applied magnetic fields. (c) Phase diagram showing required in-plane external field and spin Hall channel current combinations required for magnetization reversal.

for switching. As shown in Figure 4.5(a), the coercivity can be modulated from 240 Oe to 10 Oe by varying the current from 0.5 mA to 8 mA. The coercivity for various spin Hall currents from 0.5 mA to 12 mA is shown in Figure 4.5(b)These changes in the coercivity indicate a strong spin Hall interaction in the Ta/TbFeCo system.

The influence of the SHE on the magnetization can also be studied by sweeping the current in the presence of various in-plane fields along the ±y direction. When the current is applied parallel with H_y, the direction of the effective field generated due to the spin Hall effect, $H_{\parallel} = \tau_{\parallel}^{0}(\boldsymbol{m} \times \widehat{\boldsymbol{\sigma}})$, is oriented parallel with H_y for $M_z < 0$ and anti-parallel with H_y for $M_z > 0$; therefore the upward magnetization is favored. Similarly, when the current is applied anti-parallel with the H_y field, downward magnetization is favored. By sweeping the DC current, switching of the magnetization can be observed for constant H_y. The H_y and spin Hall current combinations required for switching of the perpendicular magnetization are shown in Figure 4.5(c) with the final magnetization direction shown. In the center region of the graph, the combination of H_y and current is not sufficient to switch

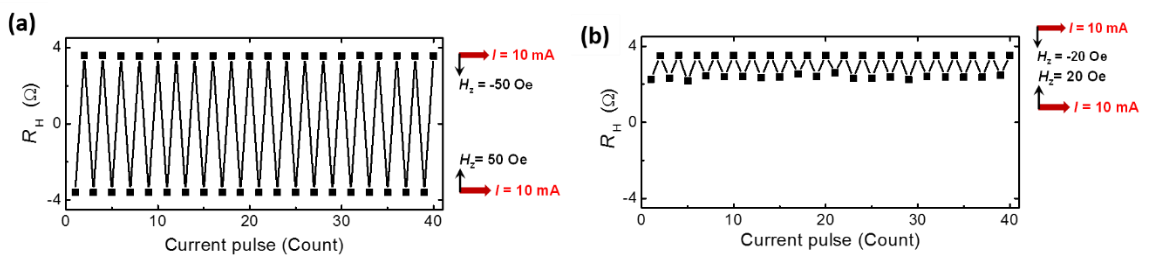

Figure 4.6 Anomalous Hall measurement with 10 mA current pulses demonstrating (a) complete magnetization reversal with the application of a perpendicular field ±50 Oe and (b) incomplete magnetization switching with the application of a perpendicular field of ±20 Oe.

the magnetization from the initial state.

Additionally, switching of magnetization is demonstrated with pulse currents along with the application of an external field. Pulse currents are used in the experiment to reduce effects such as generated Oe fields or Joule heating. First, an external field with amplitude of 50 Oe is applied. During field application, a pulse current of 10 mA is applied. After relaxation of the current pulse and external field, the field direction is reversed and another 10 mA pulse current is applied. This is repeated for alternating polarities of the external field to induce switching between the two different stable perpendicular magnetization states. In this experiment, the Hall resistance of the device can be reproducibly switched back and forth between +3.6 Ω and -3.6 Ω after each reversal of the field polarity which indicates complete magnetization reversal of the device. The results are shown in Figure 4.6(a). An additional experiment is performed where the amplitude of the field was decreased to 20 Oe for the same current pulse. In this experiment, the Hall resistance only oscillated between +3.6 Ω and +2.5 Ω. Such small variation in R_H indicates only one or more small reverse domains are nucleated in the presence of a perpendicular field of 20 Oe, but the field and current are not strong enough for the expansion of the reversed domains. Therefore, for the case of ±20 Oe external field application with 10 mA pulse amplitudes, complete magnetization reversal is not achieved. This is consistent with the switching diagram in Figure 4.6(b) where it is shown that for the current of 10 mA, H_z = 20 Oe is located near the boundary of the switching diagram and thereby barely enough for domain wall nucleation; Furthermore, 50 Oe is located in the reversal area in the diagram and thereby results in a completed switching of magnetization.

Additionally, the strength of current-induced torques is determined for the Ta/TbFeCo system. An in-plane field is applied and the field sweeps are compared for the same magnitude of current at opposite polarities Figure 4.7(a) shows the result for when the field is applied along the longitudinal direction with a current of ±4 mA. In this case, the differences in the Hall resistances for positive current and negative current are attributed to the anti-damping torque related with spin Hall effect, following the equation

$$\Delta H_y = \tau_{\parallel}^{0} / \sin\theta$$

where θ denotes the angle between the magnetization and x-y plane[74]. Using this equation, it is calculated that $\frac{\tau_{\parallel}^{0}}{I} = \frac{1.5mT}{mA}$ and the spin Hall angle is estimated to be about $\frac{J_s}{J_c} = 0.12$. This measurement is repeated with the field applied along the transverse direction as shown in Figure 4.7(b). The lack of difference between the R-H curves for the transverse direction at I = +4 mA and I = - 4 mA indicates the field-like torque related with

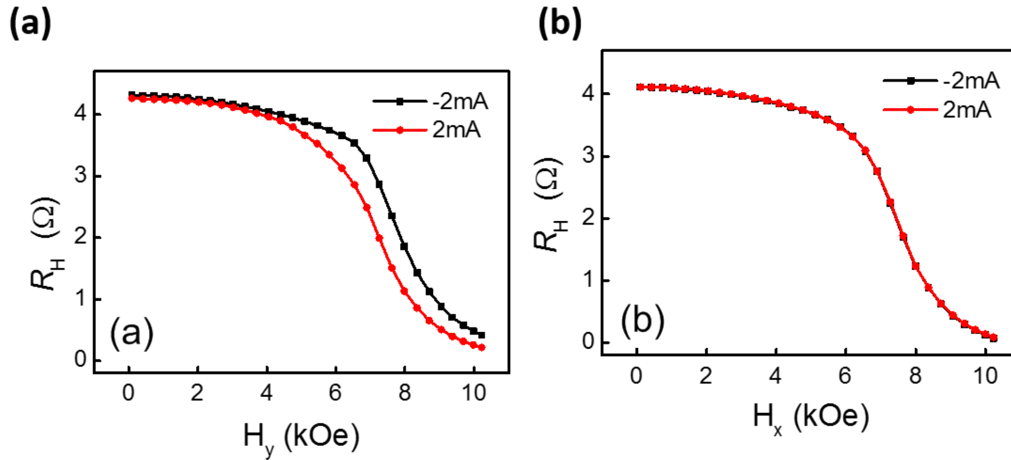

Figure 4.7 Anomalous Hall resistance as a function of the applied field along the (a) y direction and (b) x direction for a spin Hall channel current of ±2 mA.

the Rashba effect is negligible in the Ta/TbFeCo system.

In summary, bulk PMA structures can overcome the limitations of interfacial PMA structures. To understand the spin orbit interactions in bulk perpendicular systems, a Ta/TbFeCo device is fabricated. Additionally, this structure verifies strong spin orbit interactions in the Ta deposited via our Shamrock sputtering system allowing us to use this for future SOT studies and device applications presented in the following sections. The spin Hall effect in Ta/TbFeCo structures with bulk-PMA is studied for the first time. The current-induced magnetization switching is studied in the presence of a longitudinal field while the "half-switching" phenomenon is obtained in the presence of a transverse field. The strength of anti-damping torque and spin Hall angle is in accordance with that in Ta/CoFeB/MgO systems reported previously, and the field-like torque (Rashba torque) is negligible in our Ta/TbFeCo system.

4.3 Composite Spin Hall Multilayer Design for External Field Free Switching of Perpendicular Magnetization

4.3.1 Introduction and Motivation

Spintronic devices that rely on the reversal of magnetization states for data storage and computation have gained significant interest due to limitations in scaling of conventional semiconductor devices for traits such as device reliability and increased power consumption. While spin transfer torque (STT) switching of perpendicular MTJs has allowed for improvements in device operation for STT-RAM applications[100]–[106], STT-RAM still suffers from issues such as dielectric breakdown of the tunnel barrier at

high current densities required for write operations as well as low magnetoresistance ratio due to very thin MgO layer thickness (~ 1 nm)[107]. The spin Hall effect (SHE[39]) is one proposed solution to overcome several issues in STT-RAM[70], [108]. Unlike the case of a STT-RAM cell in which current for writing is required to pass through a high resistance tunnel barrier, the current passes through the metallic material of the spin orbit channel. Spin Hall-based memory devices provide the possibility to increase device lifetime by reducing the chance of tunnel barrier breakdown and having the potential to lower the energy of operations due to the switching current passing through a lower resistive path. Moreover, due to the lower resistivity of metals, less Joule heating may be involved during the write process and it can save energy. Additionally, since the read and write passes are different, each can be independently optimized for better performance such as developing MTJs can have a much larger tunneling magnetoresistance ratio. Spin Hall based devices can also potentially be more efficient in spin transfer torque due to geometrical gain[70].

Since the experimental demonstration of large spin Hall angles in Ta[70], spin-orbit torques induced by charge currents in heavy metal/magnetic structures have attracted a wide attention among researchers[73], [74], [109]. For in-plane magnetic materials, the spin Hall effect can be sufficient to cause magnetization reversal[70]; however, structures without crystal inversion asymmetry require the application of an in-plane field in order to achieve deterministic switching using the SHE[82], [108]. In order to ensure scalability of spin Hall effect devices for high density and thermally stable memory applications, it is necessary to use perpendicular materials due to their high magnetic anisotropy values[33]. However, it is also necessary to achieve switching without an external field.

There have been several proposed methods to achieve switching in perpendicular materials without the assistance of an externally applied field[75], [76], [110], [111]. One approach is to use a wedge to achieve external-field free switching[75],[76]; however, this limits scalability as it will become increasingly difficult to create and reliably control the wedge structure at required dimensions for high density and at wafer level. The wedge structure also creates challenges in creating more complex material stacks such as those required for MTJs. Additional proposals utilize exchange biased coupling[110], [111]. However, due to the material stack design, it is unclear how to build up an entire perpendicular MTJ structure using this method. Our proposal allows for uniform design across the device and integration with full MTJ stacks.

In this study, a new material structure is proposed and demonstrated that utilizes the spin Hall effect to switch perpendicularly magnetized materials in the absence of any externally applied field. The structure consists of a multilayered material stack including a magnetic layer with perpendicular magnetic anisotropy that serves as the storage layer and a magnetic layer with in-plane magnetic anisotropy that assists switching of the magnetization of the storage layer through stray fields. We develop a composite structure of substrate / Ta (5 nm) / CoFeB (1.2 nm) / MgO (2 nm) / CoFeB (3 nm) / MgO (2 nm) and demonstrate the spin Hall effect arising from the Ta spin orbit channel can switch the magnetization of CoFeB (1.2 nm) with perpendicular magnetic anisotropy. This new composite structure could enable more widespread use of the spin Hall effect for memory and logic applications.

4.3.2 Composite Structure Development and Magnetic Properties

For the proposed composite structure, we incorporate an additional spacer layer and in-plane magnetic (IPM) layer on top of the spin Hall channel and perpendicular magnetic (PM) layer as show in Figure 4.8(a). The IPM layer generates a stray field that provides the necessary field to break the symmetry of the structure and deterministically switch the PM layer. This replaces the need for an external field or the requirement of a wedge structure for engineering a tilted anisotropy. Additionally, it allows for a uniform material stack thickness that will allow the devices to be scaled to small dimensions, fabricated uniformly across wafers, and integration of full MTJ stacks. Figure 4.8(b) illustrates how this concept can be incorporated with a full perpendicular MTJ structure for memory or logic applications. The MTJ is developed on top of the spin Hall material with the IPM layer for biasing the free PM on top of the full MTJ separated by a spacer layer. The

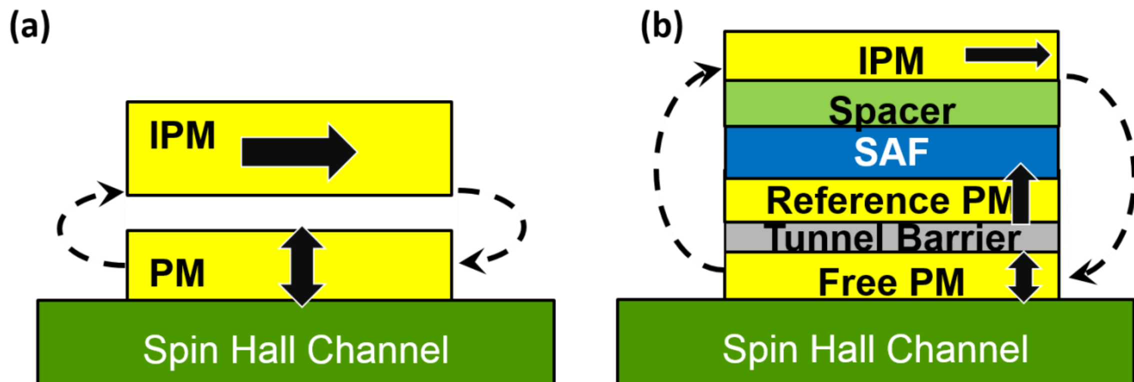

Figure 4.8 (a) Schematic design of a composite structure consisting of a perpendicular magnetic layer, spacer layer, and in plane magnetic layer for achieving external field free switching of perpendicular magnetization and (b) proposed design for how the composite structure can be incorporated into a full perpendicular MTJ structure.

thickness and material of the IPM can be tuned to obtain optimal interaction with the free layer for a given device configuration.

For the composite structure, we used a Shamrock magnetron sputtering system to deposit the following material stack on a Si / thermally oxidized SiO_2 substrate: Ta (5 nm) / CoFeB (1.2 nm) / MgO (2 nm) / CoFeB (3 nm) / MgO (2 nm). The CoFeB (3 nm) layer has in-plane anisotropy and provides a stray field to the CoFeB (1.2 nm) layer sufficient to break the structural inversion symmetry required for switching of the PM using the SHE. For reference, a single PM layer was also deposited with the following structure: Si / thermally oxidized SiO_2 substrate / Ta (5 nm) / CoFeB (1.2 nm) / MgO (2 nm) / Ta (5 nm). The vibrating sample magnetometry results for the reference and composite films are shown in Figure 4.9. The results confirm the perpendicular anisotropy of the 1.2 nm thick CoFeB layer as well as the 3.0 nm thick IPM layer designed to provide the stray field.

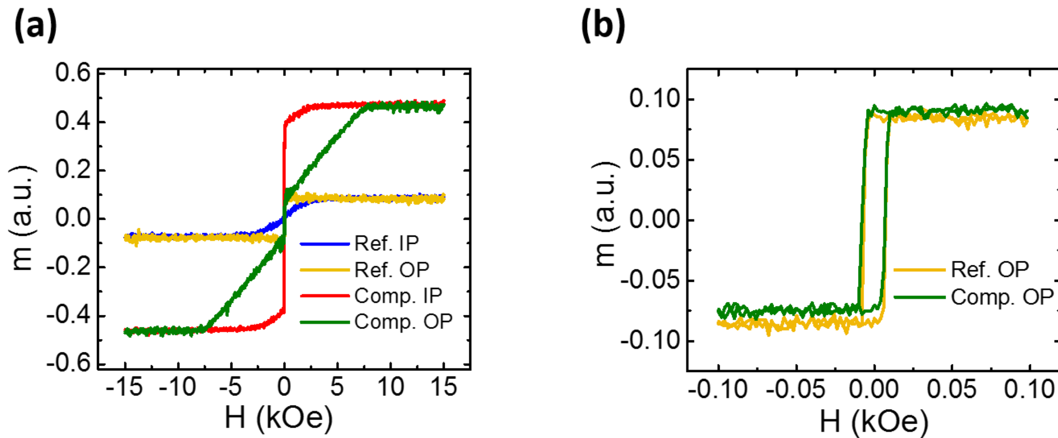

Figure 4.9 VSM results for the composite film sample and reference film sample comparing (a) in-plane and out-of plane results and (b) out-of-plane results for a narrow field scan.

4.3.3 Device Fabrication and Electrical Characterization

Device fabrication is conducted using, photolithography, ion milling, and e-beam evaporation techniques. The fabrication process is shown in Figure 4.10. After the film deposition, the samples undergo a solvent cleaning process. Then, the sample prebaked at 115°C for 60 seconds. Microposit S1813 resist is then spun on at 4000 rpm for 30 seconds followed by a bake at 110°C for 60 seconds. The sample is exposed using photolithography for 5 seconds and then developed in 351 Developer:DI 1:5 for 30 seconds. Next, ion milling is done to etch the spin Hall channel region, as shown in Figure 4.10(b). After resist removal, photolithography is performed to pattern the magnetic pillars. The Microposit

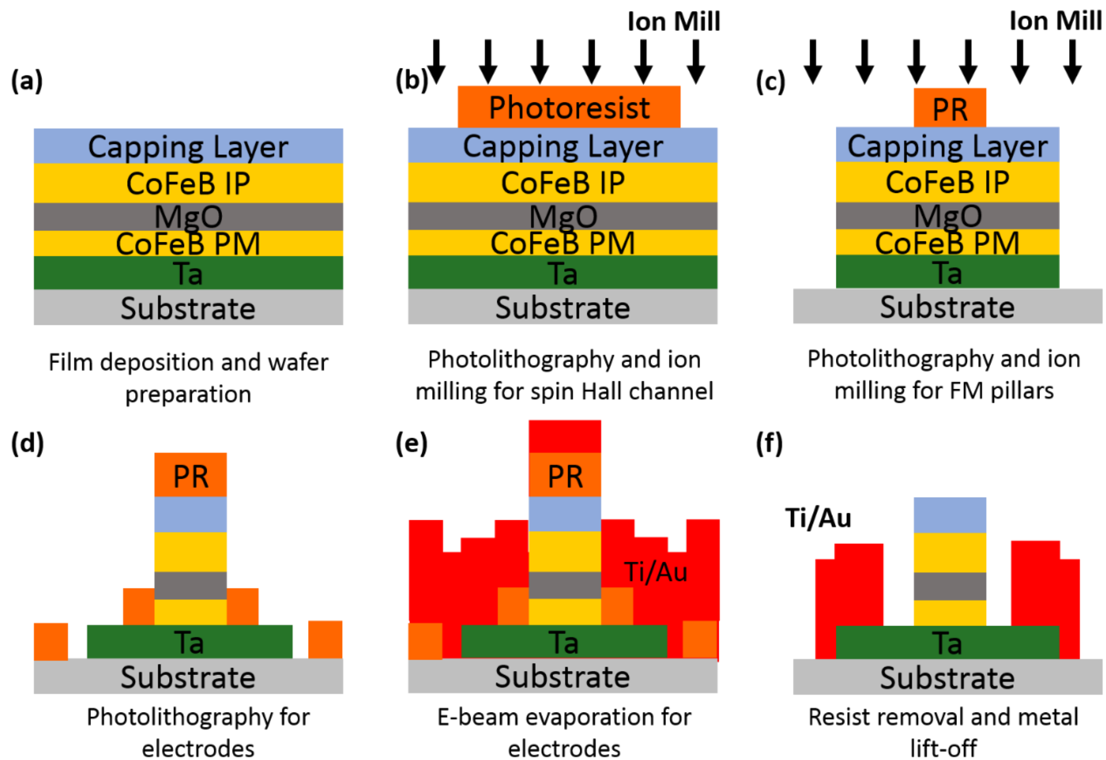

Figure 4.10 Fabrication flow for composite spin Hall device with magnetic pillar on the spin Hall channel.

S1813 resist preparation, exposure, and development is performed as described above. The pillars are patterned in the center of the Hall bars and have dimensions varying from 3 μm to 8μm. After development, the samples are ion milled to etch through the magnetic material but stop on the Ta spin Hall channel as shown in Figure 4.10(c). Once the resist is removed after ion milling, the above Microposit S1813 resist process is again repeated to pattern the region for patterning the electrodes (Figure 4.10(d)). After resist development, Ti (10 nm) / Au (100 nm) electrical contacts are deposited using e-beam evaporation at a rate of 1 Å/sec and 3 Å/sec, respectively (Figure 4.10(e)). The resist is then removed and metal is lifted off to form the top electrodes as shown in Figure 4.10(f).

A schematic image of the final fabricated device design is shown in Figure 4.11(a). A four probe configuration is used for the measurement. The measurement set-up is shown on the optical image of the fabricated device in Figure 4.11(b). For the measurement, either a pulse current or constant DC current is along the spin orbit channel (in *y* direction) applied using a Keithley 6221 current source while the resultant anomalous Hall signal is measured transversely (along *x* direction) using a nanovolt meter. The anomalous Hall effect (AHE) is used to measure and determine changes in the perpendicular magnetization. Changes in the measured anomalous Hall resistance, R_{AHE} are indicative of changes in the perpendicular component of the magnetization since R_{AHE} (= V_{AHE}/I) is directly proportional to the perpendicular component of the magnetization, M_z. For the field-

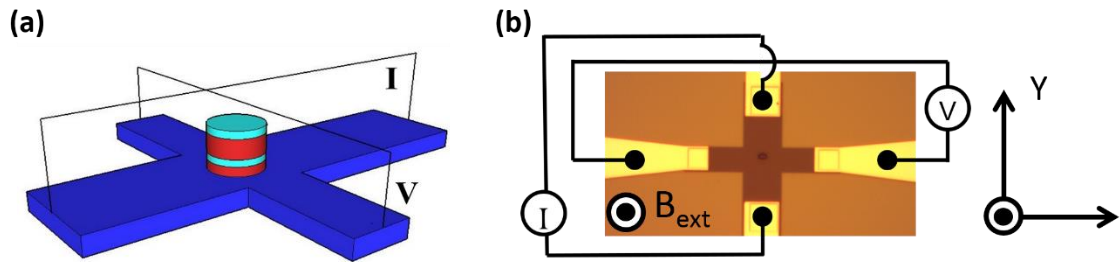

Figure 4.11 (a) Schematic design of composite device and (b) and optical image of fabricated device showing the testing configuration.

switched measurements, an external magnetic field is applied perpendicular to the plane of the film (z axis).

4.3.4 Results and Discussion

Figure 4.12(a,b) shows R_{AHE} for the reference and composite samples, respectively, when an externally applied perpendicular field is swept from –650 Oe to +650 Oe and back. There is a significant reduction in the coercivity of the composite structure compared to the reference structure, even though the VSM results of the films indicate similar perpendicular magnetic properties. This reduction indicates strong interaction between the PM and IPM layers of the patterned composite structure. Additionally, the reference samples have hysteresis loops centered around zero field while the composite devices show a shift in the hysteresis loop which can be attributed to interactions between the PM and IPM layers.

To verify a strong spin Hall effect for the Ta spin Hall channel, R_{AHE} was measured for varying amplitudes of current applied to the spin orbit channel while an external field is swept along the z axis. Current pulses of 1 ms are applied to the spin orbit channel. The

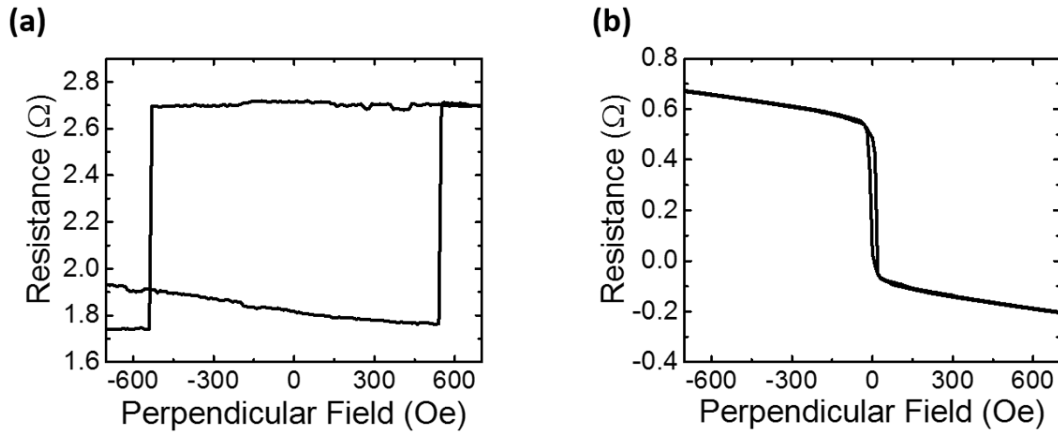

Figure 4.12 RH loop of (a) reference sample and (b) composite sample.

pulse current measurements were used to reduce effects such as joule heating and Oersted field contributions. The results for varying amplitudes of negative and positive current pulses are shown in Figure 4.13(a.b), respectively for a 4 µm x 8 µm magnetic pillar. The decrease in coercivity indicates a strong spin Hall effect is generated in the Ta spin orbit channel and is consistent with previous results[74], [112]. Additionally, it is observed that at high current values (typically greater than 8 mA) the switching behavior changes from

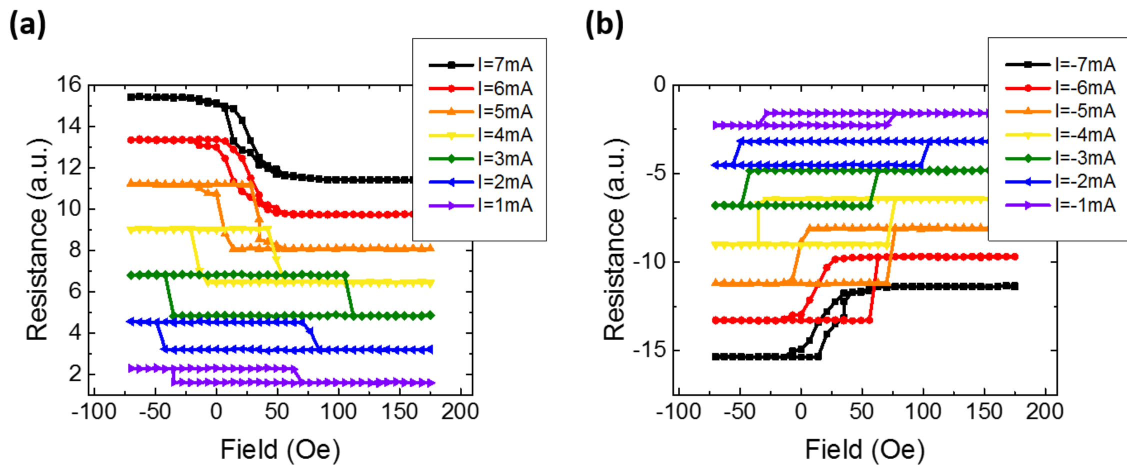

Figure 4.13 RH loops for various current amplitudes of spin Hall channel for (a) positive and (b) negative polarities of spin Hall channel current.

a sharp, easy axis switching to a more gradual switching common for hard axis switching behavior. This can be explained due to the larger spin orbit torque at larger current values. When the torque is large enough, it acts to bring the magnetization into the plane of the film. When the external field is swept, it competes with the torque holding the magnetization into the plane of the field, and as the field strength changes, the magnetization begins to slowly rotate out of the plane of the film as opposed to sharp switching between the two perpendicular states (which are bi-stable at lower spin Hall currents).

Initial current-induced switching experiments were performed with pulse currents. Due to the value of R_{AHE} varying for varying magnitudes of spin Hall current, a constant read current is used to determine if full perpendicular switching has occurred. First, R_{AHE} is measured for a pulse current with a 1 mA amplitude and 1 ms pulse width applied to the spin orbit channel while a perpendicular external field is swept. The results are shown in Figure 4.14(a). Additionally, the results for a pulse current with an 8 mA amplitude is

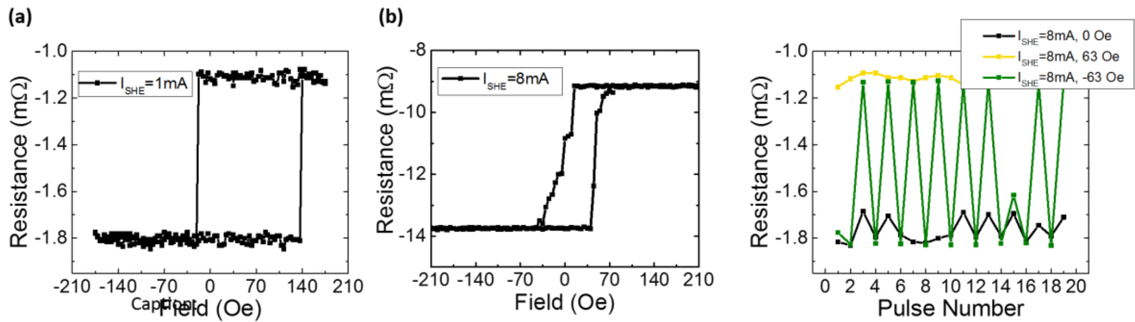

Figure 4.14 (a) RH loop with 1 mA current applied to spin Hall channel and (b) 8 mA and (c) anomalous Hall resistance measured with 1 mA read current after ±8 mA write current under 0, +63, and -63 bias fields.

shown in Figure 4.14(b). To demonstrate switching, a writing pulse current of positive polarity is applied. Then, the read current pulse of 1 mA is applied and R_{AHE} is measured to determine the magnetization state. This is followed by an additional write current of the opposite polarity followed by a read pulse. The write and read pulses are repeated to determine the switching of the composite device. The results for 8 mA writing current are shown in Figure 4.14(c) where the R_{AHE} values correspond to the 1 mA write pulses applied in the sequence. With the increase in spin Hall current, the coercivity is reduced and due to the shift in the hysteresis loop, the magnetization reversal process begins before the field polarity is changed. Due to the shift, it is possible that at zero applied field the hysteresis loop is shifted so that only one stable state is available. As seen from the results, for the case of zero externally applied field, complete switching is not observed between the two magnetic states. However, when a small biasing field of -63 Oe is applied to account for the shift in the hysteresis loop, full switching can be achieved through the current pulse applications. Full magnetization reversal is confirmed as opposed to only bringing the magnetization to an intermediate state with the magnetization along the plane of the film since R_{AHE} for the 1 mA read pulses is in agreement with the values for R_{AHE} induced by field switching at 1 mA applied current. The biasing field acts to center the hysteresis loop so that two stable states are available rather than as the switching mechanism. In future structures, the biasing in-plane magnetic layer can be optimized by changing the thickness as well as material (and therefore saturation magnetization) to ensure that there are two stable states at zero applied field. In this way, the external bias field to center the hysteresis loop can be eliminated.

In order to confirm switching can be achieved without the application of the external biasing field, measurements were performed using a constant DC current applied to the spin orbit channel while monitoring R_{AHE}. Figure 4.15 shows the results for zero external applied field. It was observed that by sweeping a constant DC current, R_{AHE} changes indicating magnetization reversal. The magnitude of ΔR_{AHE} is comparable to the field switched measurements; therefore, full magnetization reversal has occurred as opposed to only brining the magnetization state along the plane of the film. Due to the composite structure of the magnetic film stack, perpendicular magnetization switching is successfully achieved without the use of any externally applied fields.

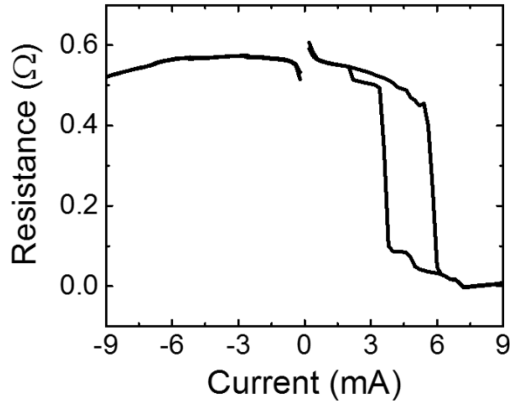

Figure 4.15 Perpendicular magnetization switching by sweeping a DC current without the application of an external field.

4.3.5 Summary

We proposed and developed a composite material stack with a CoFeB perpendicular magnetic free layer that can be switched using the spin Hall effect without the aid of an externally applied field. An in-plane CoFeB layer provides a stray field sufficient to break the symmetry required for switching of perpendicular magnetization using the spin Hall effect. This structure can easily be scaled to dimensions required for memory and logic applications and is not limited by the requirement of a wedge structure

or shape anisotropy. This initial demonstration provides a gateway to developing more complex structures such as the incorporation of magnetic tunnel junctions with perpendicular magnetization that can be switched using the spin Hall effect for high reliability, low energy devices.

4.4 Ta/W Multilayers for Material Engineering Spin Orbit Channels

4.4.1 Introduction

Magnetic based solid state nonvolatile memory known as spin transfer torque random access memory (STT-RAM) has been proposed as a universal storage that could bring superior attributes to the conventional semiconductor storage devices. There are several obstacles such as thermal stability while maintaining low write energies and achieving fast switching speeds with MTJs that should be addressed to make them more appealing for device applications such as STT-MRAM and spintronic logic. Spin-orbit torques (SOT) are an alternative method for switching of the magnetization and have been proposed for STT-RAM applications [77], [113] and logic devices [114], [115] and could provide a solution to most of the issues related to the conventional writing of the information to MTJ devices. Since the torque is generated in a nonmagnetic tunnel and isn't required to be passed vertically through a tunnel junction device, it reduces the risk of the tunnel junction breakdown thus increasing device lifetime. Additionally, it separates the read and write paths required for operation. For perpendicularly magnetized MTJs, the incubation delay using SOT for magnetization reversal is predicted to be significantly

reduced due to the fact the torque generated from spin orbit interactions is perpendicular to the direction of magnetization and fast switching speeds are predicted[80]. However, there is still a lacking of fundamental understanding of SOTs including how to improve the efficiency of SOTs, the mechanisms that contribute to SOTs, and the role each play in the magnetization reversal.

Due to the high resistivity of materials such as Ta used for SOT devices, it would be desirable to engineer spin-orbit channel to have control over the charge-to-spin conversion as well as channel resistivity to increase the spin torque efficiency. In this paper, we present our results on multilayered Ta/W spin Hall channels in an attempt to improve the performance of the spin-orbit channel. Utilizing the planar Hall effect characterizations, we analyze and compare the effective field generated from the spin orbit torque as well as the spin Hall angle for a variety of multilayer channels with different resistivity.

4.4.2 Material Stack Preparation and Device Fabrication

In this section, multilayered spin-orbit channel stacks are developed and the effect of different stacks on the spin Hall angle and conductivity is studied. A schematic image of the device is shown in Figure 4.16. The stacks are deposited on a thermally oxidized Si/SiO_2(300nm) substrate using a dc and rf Shamrock magnetron sputtering system. In this section, experimental results for the following stack structures are presented: Ta(5), Ta(2)/W(3), $[Ta(0.5)/W(0.5)]_5$, $[Ta(1)/W(0.5)]_3$/Ta(0.5), $[Ta(0.5)/W(1)]_3$/Ta(0.5), $[Ta(0.5)/W(0.5)]_3$, and $[Ta(0.5)/W(0.5)]_{10}$ where all thickness are given in nm. On top of these stacks CoFeB(5)/MgO(2)/Ta(4) is deposited directly after the spin Hall channel without breaking of the vacuum. Utilizing photolithography, ion milling, and e-beam

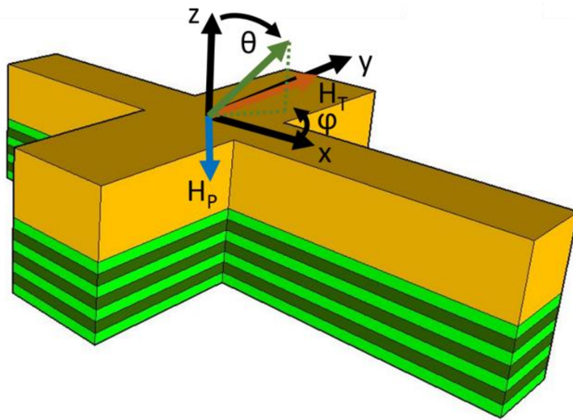

Figure 4.16 Schematic diagram of multilayer Ta/W spin Hall devices.

evaporation similar to the method described in detail in section 4.2.2, the Hall bar and electrical contacts are defined. The length and width of the fabricated Hall bars are 30 and 15 μm, respectively.

Vibrating sample magnetometry is used to determine the saturation magnetization, M_s, of the thin film, and the value is found to be 1000 emu/cc. The resistivity of CoFeB (5 nm) and Ta (5 nm) are found to be about 219 and 203 μΩ-cm, respectively, using 4-probe measurements. The effective resistivity for the structure CoFeB(5nm)/MgO(2nm)/Ta(5nm) (which is used in all of the device structures) is determined to be about 211.5 μΩ-cm. Figure 4.17 shows the I-V measurements performed on the multilayer devices. As seen in the current range of -5 to +5 mA, the I-V curves are linear suggesting a constant resistance and negligible Joule

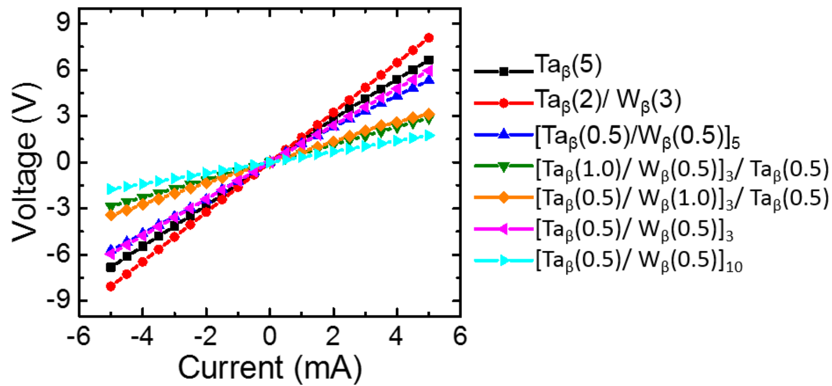

Figure 4.17 IV curves for the various multilayer Ta/W spin Hall devices.

heating. Using the resistivity for the entire stacks, the effective resistivity for the multilayer Ta/W spin Hall channels are determined. Table 4.1 presents a summary of the resistivity for different spin Hall channel stacks.

Channel (Thickness in nm)	Ta(5)	Ta(2)/ W(3)	[Ta(0.5)/ W(0.5)]$_5$	([Ta(1)/ W(0.5)]$_3$/ Ta(0.5)	([Ta(0.5)/ W(1)]$_3$/ Ta(0.5)	[Ta(0.5)/ W(0.5)]$_3$	[Ta(0.5)/ W(0.5)]$_{10}$
Current (mA)	4	4	4	8	4	4	4
Resistivity (μΩ-cm)	203.31	377.22	123.88	58.5	46.16	52.73	43.06
J_c (× 10^6 A/cm^2)	5.86	3.80	7.79	24.51	11.50	15.26	6.76
H_p (×10^{-4} T)	-4.53	-6.07	-5.63	-3.97	-1.66	-7.62	-8.37
θ_{SH} (J_s/J_c)	0.12	0.24	0.11	0.025	0.022	0.076	0.19
σ_{SH} (Ω-cm)$^{-1}$	590.23	636.23	887.96	427.35	391.74	1441.30	4412.45

Table 4.1 Summary of various multilayer spin Hall channels summarizing results of H_p, J_s, θ_{SH}, and σ_{SH}.

A DC measurement analysis technique utilizing the planar Hall effect (PHE) is used to characterize the different torque components by analysis of the equilibrium magnetization configuration under externally applied magnetic fields as well as spin-orbit torques. This measurement technique has previously been demonstrated in Refs. [22]–[24] for characterization of the spin Hall torque and associated effective field, H_p. The Hall

resistance, R_H, of the fabricated devices is measured as a function of varying externally applied field angles. The anomalous Hall resistance (R_{AHE}) and planar Hall resistance (R_{PHE}) both contribute to the measured Hall resistance.

For characterization of the SOT in the multilayer devices, R_H is measured at positive and negative current polarities as a function the angle between the current and the field directions. Under the application of large H_{ext}, $H_{T,total}$ will be along the direction of H_{ext} with a slight deviation due to the SOT. The differential resistance, R_{diff}, is then calculated as the difference between R_{PHE} for both polarities of current such that $R_{diff} = R_{PHE}(+I) - R_{PHE}(-I)$. Effects not dependent on the current direction such as Joule heating are then canceled out in R_{diff}. R_{diff} can be expressed as[42]

$$R_{diff}(I) = R_{PHE}\big(\varphi(+I)\big) - R_{PHE}\big(\varphi(-I)\big) + 2\frac{dR_{AHE}}{dH_{perp}} H_{P0} \cos\theta + C$$

where $\phi(\pm I)$ is expressed as

$$\tan^{-1}(\frac{\sin\theta \pm \delta}{\cos\theta})$$

with $\delta = H_T/H_{ext}$. Through fitting of these equations over the experimental data, H_P can be determined. Using the relationship

$$H_P = -\hbar J_s/2eM_s t(\hat{\sigma} \times \hat{m})$$

the spin Hall angle, $\theta_{SH}=J_s/J_c$, and spin Hall conductivity, $\sigma_{SH}=\theta_{SH}\times\sigma$, can be estimated.

R_{PHE} is measured for various current amplitudes while the sample is rotated in the presence of an in-plane external field. From the results for both polarities of current, R_{diff} is calculated. The results are shown in Figure 4.18(a-c). The results for R_{PHE} are shown

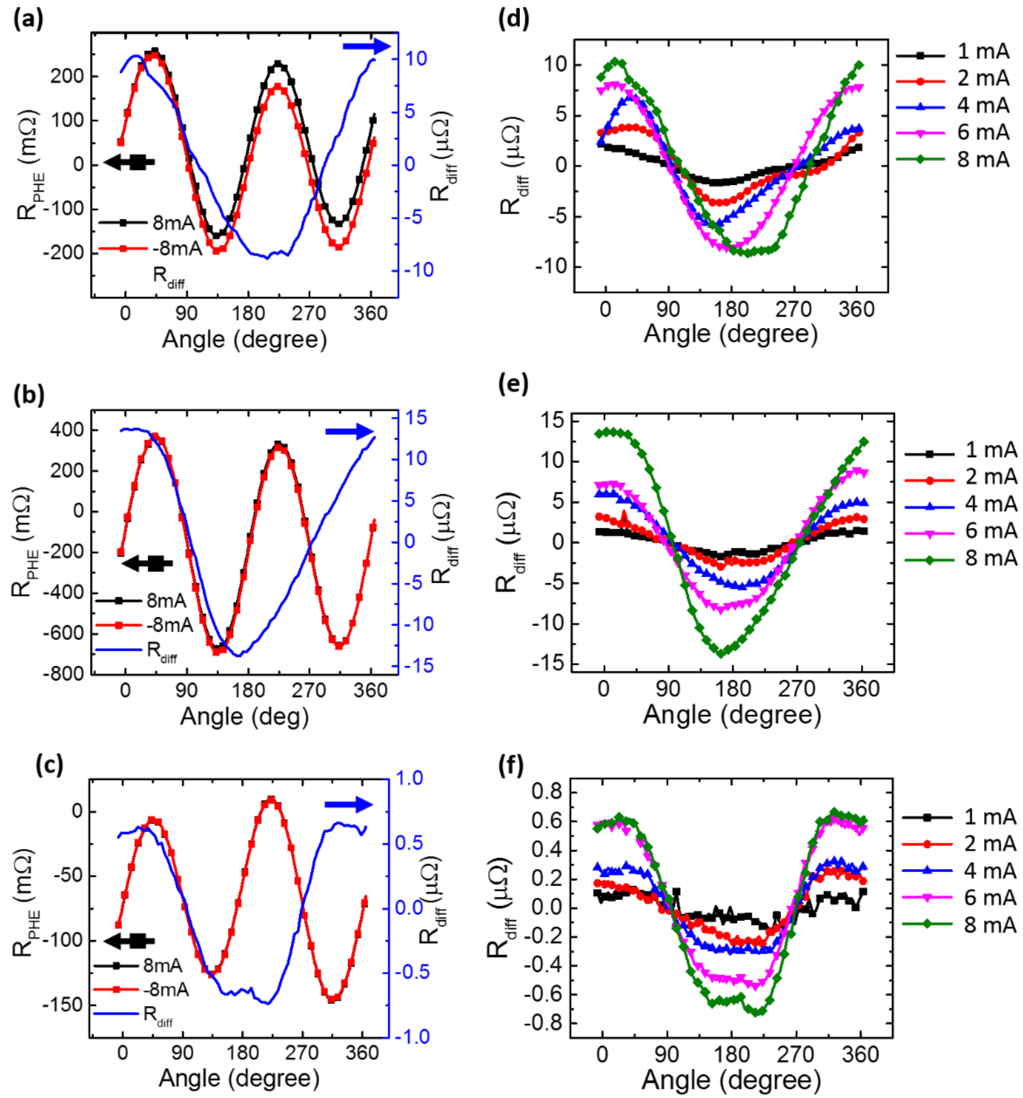

Figure 4.18(a-c) Planar hall resistance, R_{PHE}, (left axis) and corresponding differential resistance, R_{diff}, (right axis) for multilayer channels of Ta(5nm), Ta(2nm)/W(3nm), and [Ta(0.5)/W(1)]3/Ta(0.5) and (d-f) corresponding R_{diff} curves for various current amplitudes measured as a function of varying angle of externally applied in-plane magnetic field.

along the left axis for a current amplitude of ± 8 mA. R_{diff}, is calculated and shown along the right axis of Figure 4.18(a-c).

The measurement is also performed at various current amplitudes ranging from ±1 mA to ±8 mA. The results are summarized in Figure 4.18(d-f). The results for the Ta(5nm) channel are shown in Figure 4.18(a,d). As the current amplitude is increased, an increase in R_{diff} is observed, which is expected due to an increase in the SOT at larger currents. Additionally, Figure 4.18(b,e) shows the results for the Ta(2nm)/W(3nm) channel structure. An increase in R_{diff} is observed compared to the Ta(5nm) channel structure. Figure 4.18(c,f) shows the results for the $[Ta(0.5)/W(1)]_3/Ta(0.5)$ structure which exhibits a very small R_{diff} compared to the other results. Additionally, Figure 4.19(a) shows the results for R_{diff} for all samples measured at a current of ±4 mA.

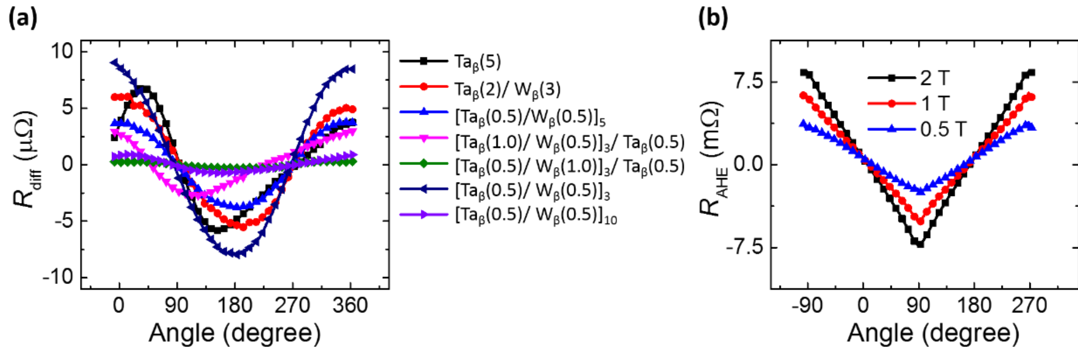

Figure 4.19 (a) R_{diff} measured at 4 mA current applied to the spin Hall channel for the various multilayer Ta/W devices and (b) R_{AHE} measured as a function of varying angle of magnetic field perpendicular to the film.

In order to perform the analytical fitting to determine H_{p} and the spin Hall angle and conductivity, it is necessary to determine the change in R_{AHE} with respect to the change in perpendicular field strength. R_{AHE} was measured while a constant perpendicular field strength was applied (at values of 0.5, 1, and 2 T) and the sample was rotated from -θ=90◦ (perpendicular to the plane of the field) through θ=0◦ (in the plane of the field) to θ=270◦.

The results for R_{AHE} as a function of the field angle, which corresponds to different perpendicular field strengths, is shown in Figure 4.19(b) for the channel structure of $[Ta(1)/W(0.5)]_3/Ta(0.5)$. Based on the angle, the strength of the perpendicular field component is determined. dR_{AHE}/dH_{ext} is calculated is calculated from the results. Through fitting of the R_{diff} curves, H_p is determined for the various samples at different current strengths. As the measurement current is increased, the amplitude of Hp also increases. Table 4.1 summarizes the results for the various structures. Figure 4.20(a) shows the dependence of H_p on the various multilayer channel structures. The values obtained for H_p varied from -1.66×10^{-4} T for the structure of $[Ta(0.5)/W(1)]_3/Ta(0.5)$ to -8.37×10^{-4} T for the structure of $[Ta(0.5)/W(0.5)]_{10}$.

For an accurate determination of the spin Hall angle and conductivity, it is necessary to determine the charge current density, J_c, in each multilayered spin Hall channel structure. This is necessary since the resistivity of the multilayers vary and therefore results in a non-equal current distribution throughout the film thickness. Utilizing

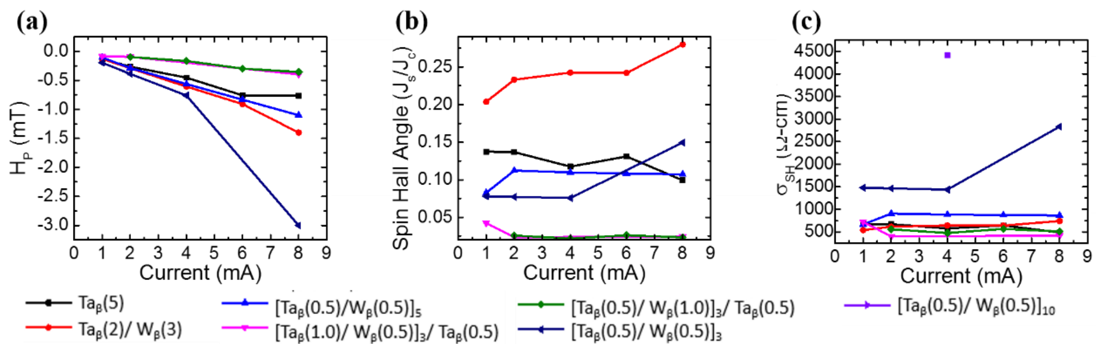

Figure 4.20 Results for the various multilayer spin Hall devices for (a) H_p, (b) θ_{SH}, and (c) σ_{SH} calculated for different testing currents applied to the spin hall device.

the resistivity of the multilayer Ta/W spin Hall channels, the charge current density is calculated for the spin Hall channel. The charge current densities of the channel layers are given in Table 4.1. Using the relationship $H_P = -\hbar J_s/2eM_s t(\hat{\sigma} \times \hat{m})$, J_s, θ_{SH}, and σ_{SH} are determined and summarized in Table 4.1. Figure 4.20(b,c) shows the dependence of θ_{SH} and σ_{SH}, respectively, as a function of measurement current. For the reference sample with channel structure Ta(5nm), a spin Hall angle of about 0.13 is obtained. A spin Hall angle as large as 0.28 is achieved for the Ta(2)/W(3) channel at 8mA measurement current which corresponds to a value of H_p=-6.07 × 10^{-4}. While this structure results in the largest spin Hall angle, different channel structures result in larger σ_{SH}. For instance, σ_{SH} is 1441.30 and 4412.45 $(\Omega\text{-cm})^{-1}$ for the $[Ta(0.5)/W(0.5)]_3$ and $[Ta(0.5)/W(0.5)]_{10}$ multilayers, respectively for a measurement current of 4 mA, while it is only 636.23 $(\Omega\text{-cm})^{-1}$ for the Ta(2)/W(3) structure. While the $[Ta(0.5)/W(0.5)]_3$ and $[Ta(0.5)/W(0.5)]_{10}$ structures have smaller spin Hall angles of 0.076 and 0.188 compared to 0.24 for Ta(2)/W(3), they have the potential for improved device performance due to the lower resistivity and higher spin Hall conductivity. This confirms that through further optimization of multilayer spin Hall channels, the spin Hall conductivity can be tuned to optimize the structure for a given application requirement.

It is also worth noting that for certain multilayer channels ($[Ta(1)/W(0.5)]_3$/Ta(0.5), $[Ta(0.5)/W(1)]_3$/Ta(0.5)), the spin Hall angle is almost negligible with $\theta_{SH} < 0.03$. It is interesting to note that while the these multilayer channels resulted in larger spin Hall conductivities, the multilayered stacks of ($[Ta(1)/W(0.5)]_3$/Ta(0.5) and $[Ta(0.5)/W(1)]_3$/Ta(0.5) have low spin Hall conductivities even though they all have

similar resistivity values (from 43.1 to 58.8 μΩ-cm). It is possible that these difference could be due to changes in the phase of the channel materials in the various stacks and/or due to enhanced interfacial effects in the thinner multilayers; however, further investigation is required to fully understand the cause behind these differences.

4.4.3 Summary

In summary, the planar Hall effect was used to experimentally study the spin orbit torques in multilayered $[Ta(x)/W(y)]_n$ samples. A spin Hall angle as large as 0.28 was observed for Ta(2)/W(3) but with a relatively moderate spin Hall conductivity of 636.23 $(\Omega\text{-cm})^{-1}$. $[Ta(0.5)/W(0.5)]_n$ multilayers were demonstrated to have relatively low resistivity (43.1 to 58.8 μΩ-cm) while still maintaining spin Hall conductivities as large as 4412.45 $(\Omega\text{-cm})^{-1}$ with spin Hall angles up to 0.188. This is important to consider for device applications where higher conductivities are desired and it is more beneficial to have higher conductivity at the cost of a slightly lower spin Hall angle. In this way, the $[Ta(x)/W(y)]_n$ structures provide a way to optimize spin orbit torque devices based on the device application requirements. This work demonstrates how multilayer spin Hall channels can be developed in order to tune the resistivity, spin Hall angle, and spin Hall conductivity in order to meet application requirements.

4.5 SPIN HALL ASSISTED SPIN TORQUE MAJORITY GATE

4.5.1 Introduction and Motivation

Spintronic devices have recently been a hot topic in research due to the need to

develop beyond-CMOS technologies. In 1996 it was demonstrated that the magnetization of a MTJ can be switched using electrical current passed through the MTJ, known as the spin transfer torque (STT) effect[25]. This eliminates the need for an external magnetic field for switching of magnetization and is currently being used for STT-RAM applications. However, combining the STT effect, which occurs when a charge current is passed across the MTJ, with spin orbit torques for MTJs results in numerous advantages compared to STT switching alone. Spin orbit torques can be generated by passing a charge current through a non-magnetic heavy metal material such as Ta, Pt, or W. This provides a potentially lower resistive path than across the ferromagnetic/tunnel barrier structure of the MTJ and in turn can result in lower energy for operation of the device. Additionally, by reducing the amount of current required to be passed across the tunnel barrier, it reduces the chance of tunnel barrier break down and can increase device life time. The MTJ structure allows for magnetoresistance readout of the device as opposed to techniques such as anomalous Hall effect measurement of single magnetic layers and can be used to achieve high MR signals to determine the device state. Additionally, fast write times of less than 200 ps have been demonstrated using spin orbit torques[80].

It was recently demonstrated using single layered ferromagnetic nanopillars that the spin Hall effect can be used to clock perpendicularly magnetized structures for logic applications[116]. In the design presented in Ref. [116], multiple single layered perpendicular magnetic pillars are placed on a single spin Hall channel. All of the nanopillars are spaced close enough such that the dipole interactions are significant to allow neighboring magnetic pillars to couple to each other. Additionally, one of the nanomagnets

is larger than the others and is used for setting the initial states of the coupled magnetic pillars. For clocking, a charge current is applied to the spin Hall channel. Due to the SOT generated, the magnetization of the perpendicular magnets is brought into the plane of the film. For setting of the states, a small external field is applied to state of the larger input magnet while leaving the smaller adjacent pillars mostly unaffected. Once the field and current is released, the nanomagnet next to the input magnet will couple according to the dipole interaction. The adjacent nanomagnets will couple in a domino-like fashion, similar to the operation of nanomagnetic logic. This demonstrates the feasibility of using SOTs and the SHE for clocking of magnetic devices; however, this design limits the state of the inputs to alternating states (i.e. up/down/up or down/up/down). Therefore, it is not possible to develop more complex logic circuits required for computation.

In 2010, it was shown that two and three input logic gates could be developed utilizing MTJs switched through the STT effect generated from a voltage applied across the input MTJs connected in parallel[117], [118]. Due to changes in the resistance of the parallel input states, the amount of voltage required to switch an MTJ varies. Through careful selection of the voltage swing applied for switching, AND, NAND, OR, NOR, and NOT were demonstrated for a two-input device in additional to the majority function for a three-input device. However, since the device is controlled solely through STT switching, it suffers from the limitations described above for STT switched MTJ devices.

4.5.2 Spin Hall Magnetic Tunnel Junction Majority Gate Proposal

In this section, I propose and demonstrate a magnetic based majority gate logic design capable of being integrated with assisted magnetization switching techniques such

as the spin Hall effect, electric field controlled magnetization, spin transfer torque effect, or strain induced switching. The proposed design consists of three individual MTJ nanopillars spaced sufficiently far apart to prevent dipole coupling with a top electrode that connects the three MTJs in parallel and which can be used to apply an additional mechanism for deterministically individually switching each nanopillar. In this way, all possible states of the majority gate (000, 001, 011, and 111) can be achieved. By combining the above mentioned assisted switching techniques with the presented MTJ majority gate design, it has the potential for benefits over current technology such as lower power consumption, non-volatility, and logic-in-memory. In this section, I focus on integrating the MTJ majority gate with spin-orbit torque (SOT) assisted switching. Due to the combined effects of SOT and STT for switching, the device will be referred to as a SOT-ST majority gate.

The proposed SOT-ST majority gate consists of input MTJs connected in parallel by both a bottom SOT material electrode and a top electrode for applying current across the MTJs. The three MTJs in parallel are then connected in series to an output MTJ. A schematic of the device configuration is shown in Figure 4.21. In the proposed design, the three inputs are spaced sufficiently far enough apart so that they do not rely on dipole interactions to control the magnetization direction. Additionally, to ensure that the coercivity of each of the inputs is different, two different approaches are utilized for the experimental demonstrations: maintaining a constant aspect ratio while changing the area of each nanopillar or maintaining a constant area while changing the aspect ratio. For the case of maintaining a constant area while changing the aspect ratio, there is the added

benefit of ensuring the current density passing through each MTJ is the same for similar orientations since the cross-sectional area is the same. By combining SOTs for clocking with STT for deterministically switching the three input MTJs as well as ensuring different coercivity of each input, we can control each input state allowing us to realize the majority

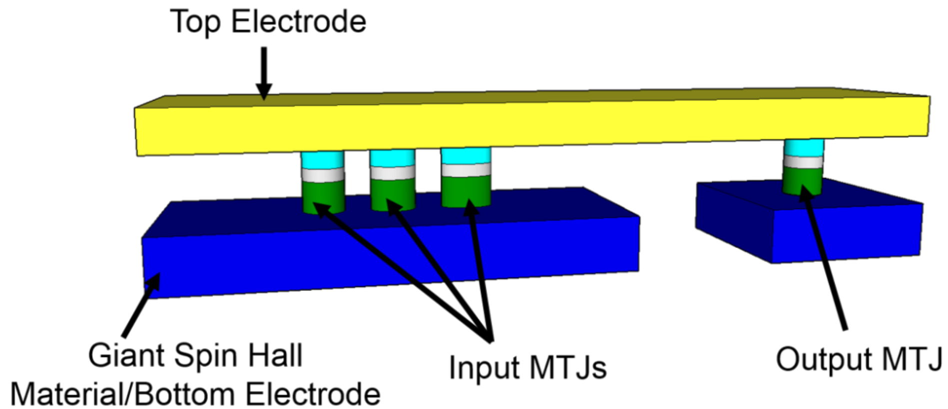

Figure 4.21 Schematic device of proposed SOT-ST majority gate with three input MTJs connected in parallel by a giant spin Hall electrode and connected in serious to an output MTJ.

function.

The operation of our proposed majority gate is shown in Figure 4.22. Initially, the clocking current, $I_{cl,1}$, is applied to the SOT material(Figure 4.22(a)). Due to the SOT exerted on the perpendicularly magnetized materials, the magnetization will rotate from the easy axis (perpendicular to the plane of the film) to the hard axis (in the plane of the film). However, SOT alone is not enough to deterministically switch perpendicular magnetization so an additional mechanism (i.e. STT, voltage/electric field control of magnetic anisotropy, strain) is necessary to set the input state. As shown in Figure 4.22(b), an additional current for writing, I_w, or voltage associated with the chosen switching

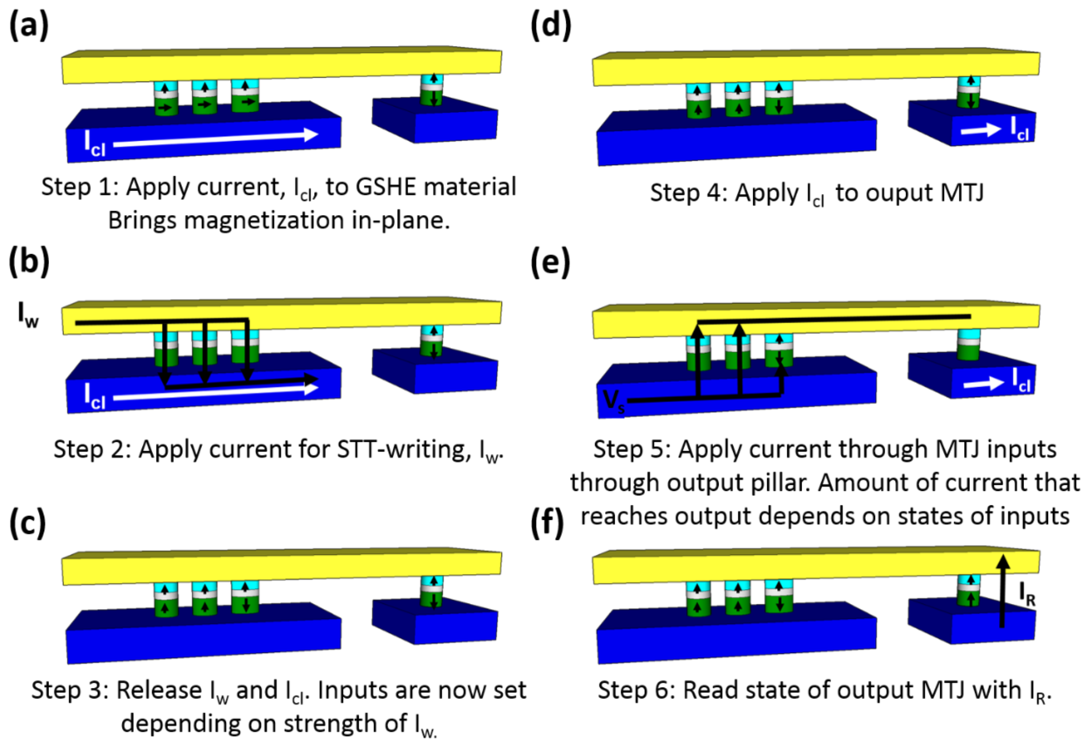

Figure 4.22 Schematic illustrating the step by step operation of the SOT-ST majority gate.

mechanism is applied across the three input MTJ's while $I_{cl,1}$ is applied. In the next step, $I_{cl,1}$ and then I_w are released to set the input states(Figure 4.22(c)). Since the nanopillars are designed to have different coercivity, they can be set individually by changing the strength of the applied current or voltage. To determine the output state, a clocking current is applied to the output MTJ structure. For instance, to change the magnetization of only one input, a small current would be applied that is sufficient to only switch the MTJ with the lowest energy barrier. If two MTJs need to be switched, a moderate current value would be applied and to switch all three MTJs, a large current. In this way, the input of each MTJ pillar can be controlled individually. Next, a second clocking current, $I_{cl,2}$ is applied to the SOT material for the output MTJ to clock the output magnetization and bring the magnetization direction into the plane of the film(Figure 4.22(d)). Then a sensing voltage, V_s, is applied

across the three MTJ structure to the output MTJ(Figure 4.22(e)). Depending on the orientations of the three input MTJs, different values of I_s will be seen by the output MTJ. For instance, if zero or one MTJs are in the parallel state and the rest are antiparallel, not enough current to induce switching of the output MTJ will pass through the three parallel inputs. However, if two or all three are in the parallel state, a larger current can easily pass through and will be significant to change the output state. After $I_{cl,2}$ and V_s are released, a read current, I_r, is applied to the output to determine the state of the majority logic gate(Figure 4.22(f)).

4.5.3 SHE MTJ Majority Gate Simulation

In this section, the concept of the SOT-ST majority gate design is simulated utilizing the *Modular Spintronics Library* developed at Purdue University by Supriyo Datta's group[119] combined with H-Spice. The simulation includes module units to represent various aspects of spintronic devices including the spin Hall effect, LLG magnetization dynamics, spin diffusion, dipole coupling, and various methods of spin polarization and injection. The developed *Modular Spintronics Library* allows for simulations to be performed that are otherwise difficult or impossible to implement with other simulation packages due to its inclusiveness of recent topics in spintronics.

To gain an initial understanding of the effects of combining the spin Hall effect with spin transfer torque for switching of MTJs as well as verify the proper use and development of the simulation work, single MTJs are initially studied. In H-Spice, the spintronics modules are combined to represent the MTJ and spin Hall channel. The simulation combines a FM module to represent the fixed layer of the MTJ, free magnetic

layer to represent the free layer of the MTJ, an LLG module for determining the magnetization dynamics for different spin torque terms, and a giant spin Hall effect (GSHE) module to represent the spin current generated from the spin Hall effect. Details of how the individual modules are modeled and computer can be found at https://nanohub.org/groups/spintronics. Figure 4.23(a) shows a representation of the various elements connected in the simulation to represent the entire single MTJ SOT-ST

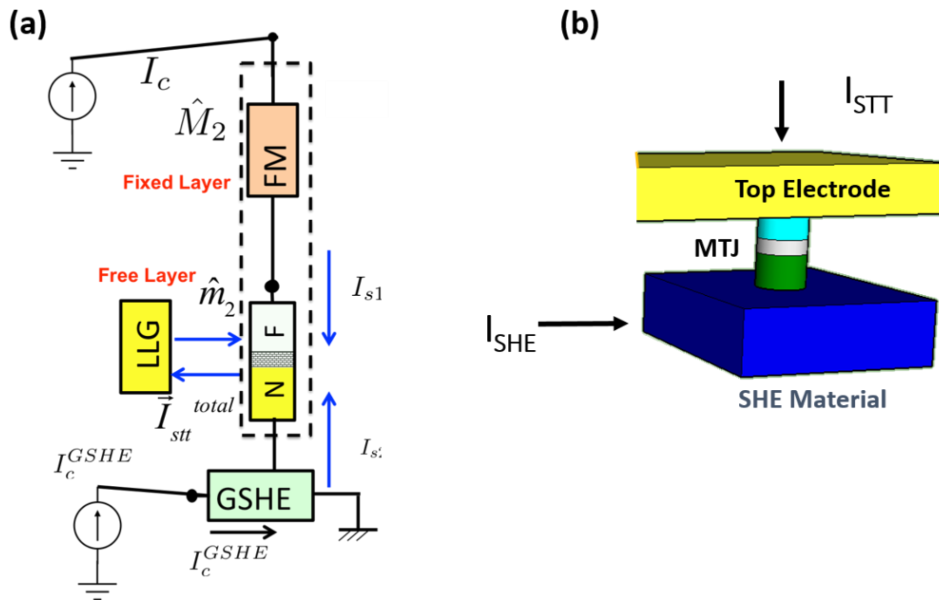

Figure 4.23 (a) Diagram of spintronic modules utilized for simulation of a single SOT-ST MTJ element. (b) Schematic image of single SOT-ST MTJ that represents the device simulated.

device circuit and Figure 4.23(b) shows a schematic image of the device.

For the simulation, a saturation magnetization, M_s, of 780 emu/cc, damping value, α, of 0.007, polarization of 0.5 and spin Hall angle, $\theta_{SH}=J_s/J_c$, of 0.12 are assumed. A MTJ pillar with dimensions of 80 nm x 170 nm is used and the coercivity is assumed to be 80 Oe. These and additional details of the simulation parameters are presented in Table 4.2.

The magnetization components M_x, M_y, and M_z are simulated for spin Hall and/or spin transfer torque currents applied to the device. For the magnetization dynamics associated with spin orbit torque, and pulse current with amplitude of 1 mA for 5 ns is applied and for the STT across the MTJ a pulse current of 3 mA for 5 ns is applied to the device. Results for the various magnetization directions are plotted in Figure 4.24(a-c) for SOT only, SHE only, and STT combined with SOT, respectively. For the SOT-ST simulation, the 5ns STT current pulse is applied 1 ns after the 5 ns pulse for SOT. While this initial simulation is done to demonstrate the effect of the two combined effects, this simulation can be used to optimize the pulse amplitude, width, and delay of each pulse to optimize switching speed and energy. This provides a framework for achieving optimal performance in these devices which is valuable for logic and memory applications.

M_s	**780 emu/cc**	**Spin Hall angle**	**0.12**
α (damping)	0.007	ρ (resistivity)	170 μΩ-cm
P (polarization)	0.50	λ_s (spin diffusion length)	2 nm
H_c (coercivity)	50, 70, and 80 Oe	L (length)	80 nm
Volume	22400 nm^3	W (width)	170 nm

Table 4.2 Material parameters used for SOT-ST majority gate simulation.

Additionally, the resistance states for parallel and antiparallel states of the MTJ are simulated with this approach. Using the developed simulation, a low (parallel) and high (antiparallel) resistance state is determined to be 798 Ω and 1332 Ω, respectively. This corresponds to a TMR % of about 67%, which is reasonable given the material parameters and based on experimental results.

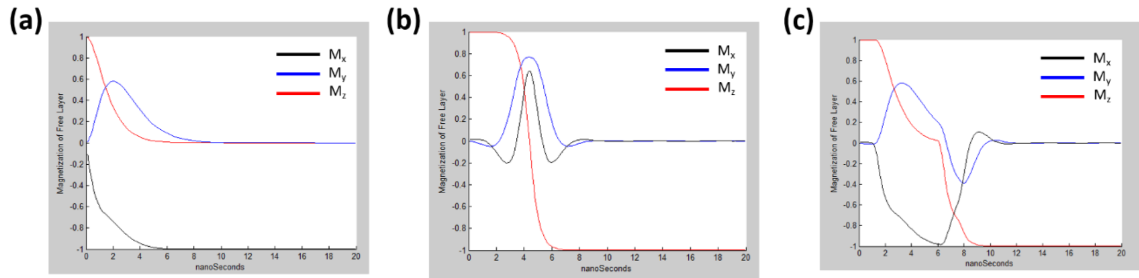

Figure 4.24 Magnetization dynamics of x, y, and z component for the case of (a) SOT current only switching, (b) STT current only switching, and (c) SOT combined with STT switching.

Following the initial simulation results, the device circuit is designed to incorporate all three input MTJs combined in parallel. A schematic of the device circuit for the inputs is shown in Figure 4.25. In order to verify the correct design and operation of the three input MTJs connected in parallel, the simulation is set up to connect three inputs but monitor the magnetization of only the first input magnet with the same dimensions and coercivity as the above simulated single MTJ pillar. Identical results are obtained in this circuit configuration and verify the circuit design. Additionally, the magnetization dynamics for M_x, M_y, and M_z are simulated for the other two MTJs in the circuit for the instances of SOT only, STT only, and SOT-ST and slight differences can be seen in the switching characteristics between the 3 MTJs with different dimensions/coercivities as expected.

Next, the operation of the SOT-ST majority gate is examined and setting of the 3 individual input states is explored. Using the circuit design for the 3 MTJs connected in parallel, various SOT and STT currents are applied to device and the final parallel resistance state is measured to determine the final state. The timing diagram for the

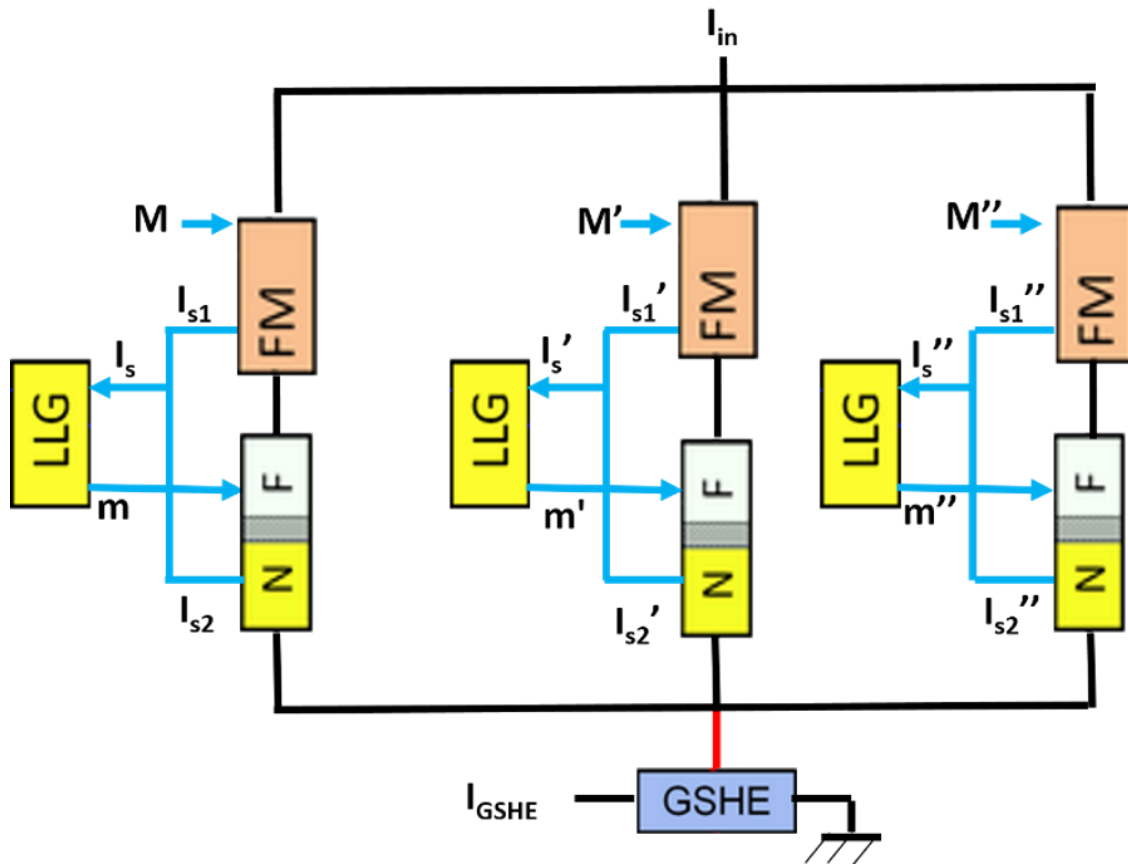

Figure 4.25 Circuit model for 3 input MTJs of SOT-ST majority gate used to model setting of the input states.

application of the SOT, STT, and read current pulses is shown in Figure 4.26(a). First, a 5 ns pulse current is applied to the SOT bottom electrode. After 1 ns, a 5 ns pulse current for STT across the MTJ is applied. Then, the magnetization is allowed to settle in to its final state. After a period of time to ensure the magnetization has settled to the final state, a 10 ns wide pulse current of 1 μA is applied to determine the final resistance state of the 3 MTJs connected in parallel.

The results for sweeping the amplitude of the STT current for various applied SOT current strengths is shown in Figure 4.26(b). The arrows indicate the direction of the free

layer magnetization for each MTJ assuming that the fixed layer is pointed in the "up" direction. As the STT current is gradually increased, there are distinct jumps in the parallel resistance of the 3 MTJs. This indicates switching of the individual inputs occurring at different current strengths. The switching of each MTJ occurs at a different current strength since the MTJs are designed to have a difference coercivity and therefore require different amounts of energy for switching. The first jump in resistance (changing from ~266 to 307 Ω) corresponds to the first MTJ with the lowest energy barrier switching from the parallel state to the antiparallel state. As the current is increased, a second jump in resistance occurs (changing from ~307 to 363 Ω) which corresponds to the MTJ with the second lowest energy barrier. A final jump in resistance is seen at larger currents (changing from ~363 to 454 Ω) indicates the last MTJ has switched to the antiparallel state. To confirm these changes in resistance are due to the switching of each MTJ, the expected resistance values of the three MTJs in parallel for the different states are calculated based on the resistance

values obtained from the single MTJ simulation. For the single MTJ with a parallel and antiparallel resistance of 798 and 1332 Ω, the changes in resistances for the three MTJ configuration matches well with what is expected.

From Figure 4.26, it is also seen that as the value of SOT current is increased, there is a reduction in the amount of STT current required for switching the individual MTJs. This can also be used to significantly reduce the total amount of current necessary to switch the MTJs. For instance, take the switching with no SOT current compared to with 0.05 mA of SOT current applied. For the case without any SOT, ~2 mA of current is required to achieve switching of the MTJs. However, with the application of just 0.05 mA SOT current, the STT current required for switching is significantly reduced down to about 1.2 mA. This demonstrates great potential for the reduction of energy required to operate the SOT-ST majority gate devices.

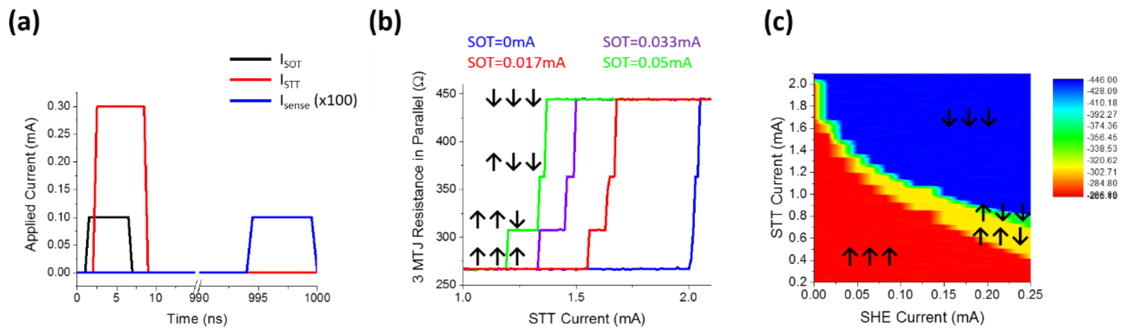

Figure 4.26 (a) Timing diagram showing the application of the SOT and STT current pulses for magnetization switching in the simulation, (b) parallel resistance across the three input MTJs as a function of increasing STT current for given SOT currents, and (c) phase diagram indicating required SOT and STT current combinations for setting the various input states of the SOT-STT majority gate.

Additionally, the SOT and STT current combinations are swept to obtain the required values necessary to switch each of the 3 MTJs individually for a wide variety of current combinations. Figure 4.26(c) shows the phase diagram indicating the required current combinations to obtain each input state of the MTJ. This can be used to determine the operational window for the SOT-ST majority gate and can be used to further optimize the current combinations for minimal energy consumption. Additionally, the MTJ parameters, such as coercivity, can be modified to change the range of current combinations that a given state can achieved from. For instance, with the parameters used in the simulation presented here, there is a fairly narrow window to achieve the "up down down" state; however, by increasing the coercivity of the final MTJ, this write window can be increased and optimized for device applications.

4.5.4 Fabrication of Three Input MTJ Design for Majority Gate Applications

For the experimental results presented here, I focus on the three input MJT portion of the SOT-ST majority gate device. The fabrication process is shown in Figure 4.28. Both perpendicular and in-plane MTJ structures were fabricated. The film stacks are deposited in the Shamrock magnetron sputtering system and consisted of material stacks of Si / SiO_2 substrate / Ta (10 nm) / TbFeCo (1.5 nm) / MgO (2 nm) / TbFeCo (2.5 nm) / Ta (4 nm) and Si / SiO_2 substrate / Ta (10 nm) / CoFeB (2 nm) / MgO (2 nm) / CoFeB (5 nm) / Ta (10 nm) for the perpendicular and in-plane structures, respectively (Figure 4.28(a)). The sample undergoes a solvent cleaning process before beginning the fabrication.

E-beam lithography and ion milling are used to define the Hall bar region. For the e-beam resist, negative ma-N 2403 resist is used and prepared and developed as described in Section 3.3.3. The Hall bar region is then defined using ion milling with the ma-N 2403 acting as the etch mask. The samples are ion milled at an incident angle of 15° for 7 minutes. This process is shown in Figure 4.28(b).

After resist removal, a second step of e-beam lithography is used to pattern the three nanopillars. Again, ma-N 2403 resist is used for the nanopillar patterning and prepared as described above. The samples are ion milled to etch through the entire magnetic material stack but stop on the bottom Ta spin Hall channel. This is illustrated in Figure 4.28(c).

Before resist removal, SiO_2 is deposited to prevent oxidation of the nanopillars and to isolate the bottom SOT material from the top electrodes as shown in Figure 4.28(d). 70 nm of SiO_2 is deposited at a rate of 2 Å/sec using the Varian e-beam evaporation system. The SiO_2 is then removed from the tops of the nanopillars when the e-beam resist is removed using NMP at 110°C for ~12 hours followed by sonication for ~10 minutes.

After resist removal, a third step of e-beam lithography is performed to pattern vias to contact the SOT material. A positive bilayer PMGI/PMMA resist is used and prepared and developed as described in Section 3.3.5. After resist development, reactive ion etching is performed. The gas species used were 70 sccm Ar, 47 sccm CF4, and 5 sccm CHF3 at a pressure of 75 mTorr and power of 100 W and was etched for 6 min and 30 sec to selectively etch through the SiO_2 and stop on the Ta region to make contact to the Hall bar as shown in Figure 4.28(e).

A final e-beam lithography step is then performed to pattern the top electrodes to

contact the three nanopillars. The PMGI/PMMA resist is prepared and developed as above. An O_2 plasma clean is performed in either the STS or AV RIE system in order to remove any residual resist in the electrode region. Then e-beam evaporation in the CHA or Temescal is used to deposit Ti(10nm)/Au(100nm) electrodes as shown in Figure 4.28(f). An SEM of the final device contacts is shown in Figure 4.27(a) and the individual nanopillars are shown in Figure 4.27(b).

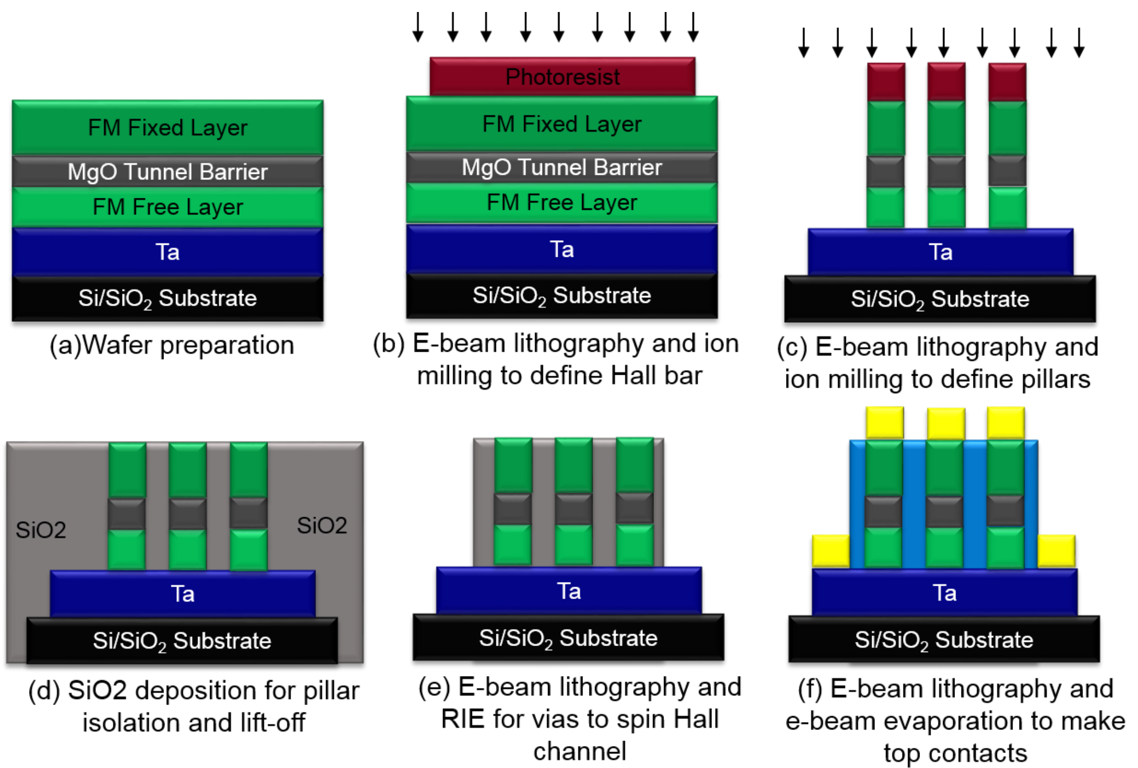

Figure 4.28 Fabrication flow of 3 MTJ inputs for application of SOT-STT majority gate.

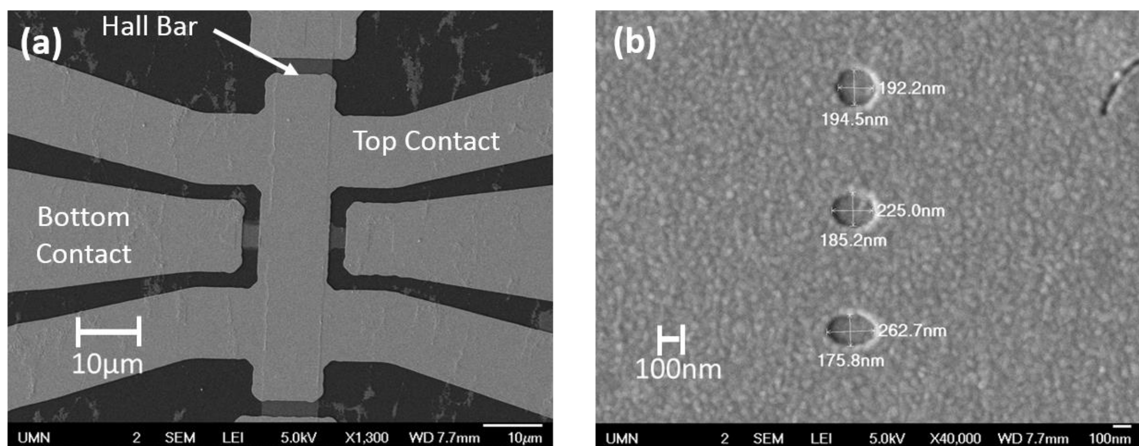

Figure 4.27 SEM images of (a) Hall bar with top electrical contacts allowing for both spin Hall/anomalous Hall measurements and top electrical contacts for application of current across the MTJs and MR measurement and (b) individual MTJ pillars of varying aspect ratio.

4.5.5 Results and Discussion

In the following experiments, an external magnetic field was used to switch the magnetization of the free layers. For the perpendicular devices, a film structure of Si /SiO_2 substrate / Ta (10 nm) / TbFeCo (1.5 nm) / MgO (2 nm) / TbFeCo (2.5 nm) / Ta (4 nm) is deposited using a Shamrock sputtering system. The VSM result for the MTJ stack is shown in Figure 4.29. The anomalous Hall effect was used to determine the magnetization state since the anomalous Hall resistance, R_H, is directly proportional to the perpendicular component of magnetization, M_z. A schematic of the device testing set-up is shown in Figure 4.30(a). A DC charge current was passed along the Ta bar to generate the SOT and anomalous Hall voltage was measured transversely to the current while an external magnetic field is swept along the ±z axis. Figure 4.30(b) shows the anomalous Hall resistance for a device with different circular nanopillars with diameters of 400, 300, and 200 nm. Three distinct resistance states are measured which correspond to the switching of each of the individual nanopillars. Figure 4.30(c) shows the results for a device with different aspect ratios but constant areas with dimensions of 1.0 x 1.0, 1.25 x 0.80, and 1.44 x 0.72 μm^2. Again, distinct resistance states are observed corresponding to switching of each of the nanopillars. The three steps in resistance as the field is swept can be understood in the following way: As the field changes from negative to positive polarity, some initial field strength will be sufficient to switch the magnetization direction of the pillar with the lowest coercivity. A change in resistance is seen since the total perpendicular component of the magnetization from all three pillars is different. As the field is continually increased, it will be strong enough to switch the pillar with the second lowest coercivity which again

leads to a jump in the resistance state corresponding to a change in the perpendicular magnetization. At higher fields, all three of the devices are able to be switched. The same switching behavior happens as the field is swept back from positive polarity to negative polarity. To further confirm a strong spin Hall effect is present in these samples, devices with one magnetic pillar were also patterned and tested using the anomalous Hall effect for detection of magnetization reversal. As a larger current is applied to the Ta bar, we notice a significant decrease in the coercivity, which verifies that this method can be used to reduce the switching field and be used to clock the magnetization. Additionally, the currents applied to verify spin Hall effect for the Ta Hall bars were kept relatively low. It is expected at higher currents the effect would be increased and an even larger change in the coercivity would be observed. However, for the sake of this measurement, the currents were kept at lower values to avoid device breakdown. The results measured by the anomalous Hall effect for a single magnetic pillar are shown in Figure 4.31(a,b) for currents of 0.2 mA and 2.2 mA, respectively, applied to the Ta bar.

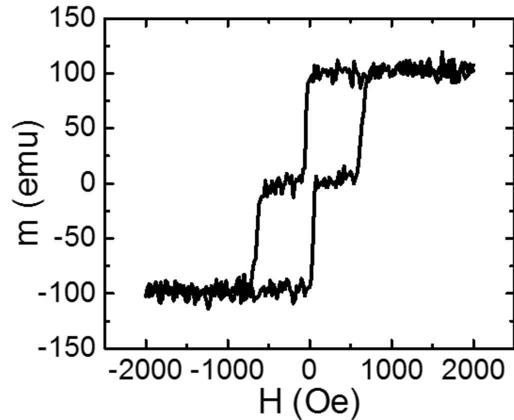

Figure 4.29 VSM result of Ta/TbFeCo/MgO/TbFeCo MTJ structure.

For the in-plane samples with structure Si / SiO_2 substrate / Ta (10 nm) / CoFeB (2

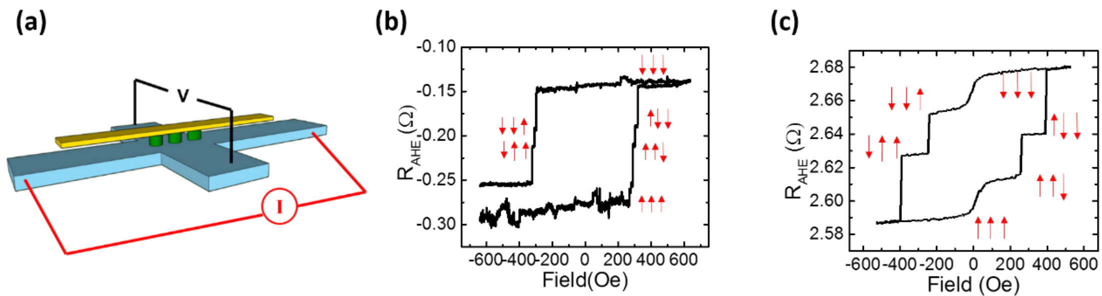

Figure 4.30 (a) Schematic design of the experimental spin Hall device with three MTJ pillars. (b) R_{AHE} of device with 140x70 nm, 124x80 nm, and 110x90 nm and (c) 400x160 nm, 310x200 nm, and 275x225 nm controlled by application of an external perpendicular field.

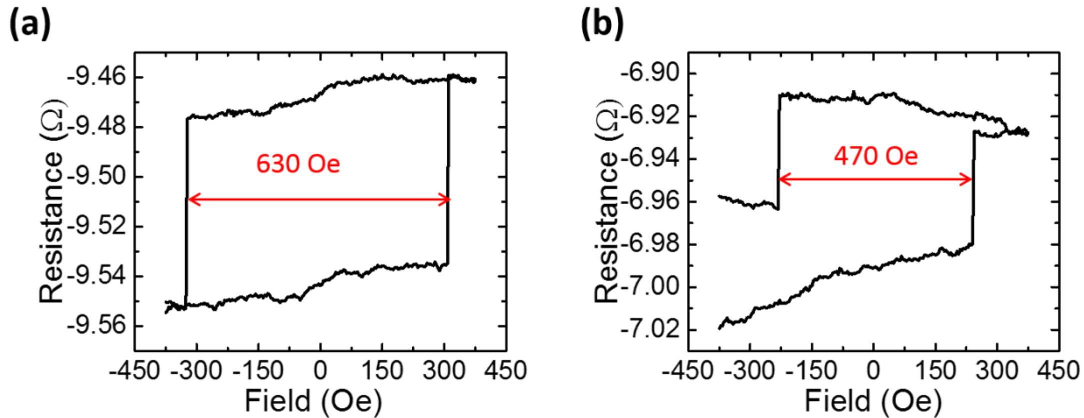

Figure 4.31 R_{AHE} for the application of (a) 0.2 mA current applied to the spin Hall channel and (b) 2.2 mA current applied to the spin Hall channel.

nm) / MgO (2 nm) / CoFeB (5 nm) / Ta (10 nm), a three terminal measurement of the TMR signal was required since the anomalous Hall effect will not detect changes of in-plane magnetization. A current was applied along the Ta bar to generate the SOT and the magnetoresistance across the MTJs in parallel was measured as the external magnetic field

was swept. The measurement set-up is shown in Figure 4.32(a). Again, three distinct changes in the resistance are noticed as the external magnetic field is swept. Figure 4.32(b) shows the results with MTJ pillars of dimensions 140x70 nm, 124x80 nm, and 110x90 nm. Figure 4.32(c) shows the results with MTJ pillars of dimensions 400x160 nm, 310x200 nm, and 275x225 nm. However, the switching behavior does not exhibit the sharp square hysteresis loops expected for typical MTJ measurements. Instead, as the field is decreased, there is a gradual increase in the resistance even before the field polarity is altered. It is believed that the two ferromagnetic layers in the MTJ structure are coupled such that they prefer the antiparallel state at zero field, corresponding to the higher resistance state near zero field. This is possibly due to the top ferromagnetic layer not being sufficiently pinned, leading to the switching behavior seen. Due to this switching behavior, it is difficult to determine the spin Hall effects interaction and its impact on the switching of the three magnetic pillars. Through future material stack development for a strong top-pinned MTJ

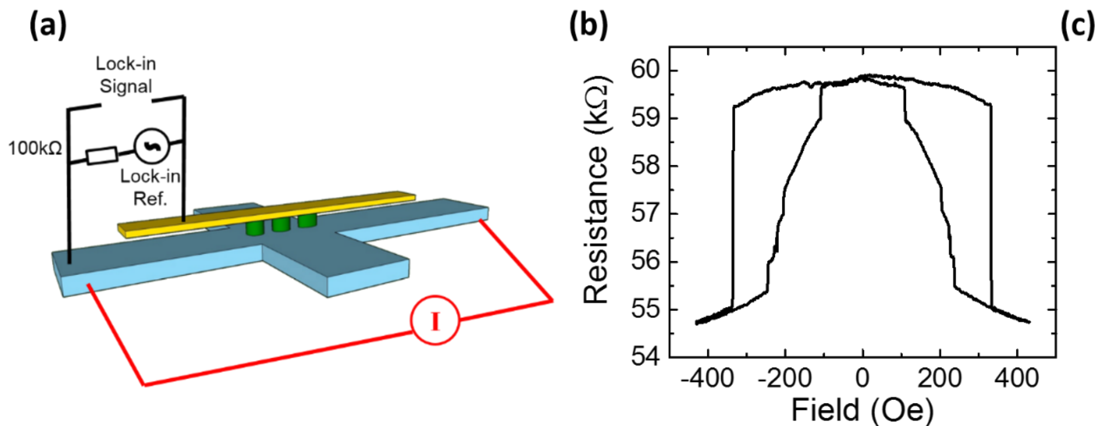

Figure 4.32(a) Schematic of the testing set-up for in-plane MTJ spin Hall device for MR measurement and (b) MR of the MTJ device switched using externally applied perpendicular magnetic field.

structure, experiments can be done to obtain clearer, sharper switching events which will allow for experiments to control all three magnetic pillar inputs via spin transfer torque and the spin Hall effect without the need for an external field.

4.5.6 Summary

We demonstrated that each of the three individual nanomagnets can be switched. A current is applied along the Hall bar and the anomalous Hall effect is used to determine an output voltage which is proportional to the perpendicular magnetization. An external perpendicular field is swept to change the magnetization direction. Due to different shape anisotropies of the individual nanomagnets, each switches at a different field strength. Distinct output levels are observed that correspond to possible different states of the majority gate design. These initial demonstrations of the majority logic gate design will enable future experiments to integrate the majority gate with STT switching. This will provide a possible new majority gate design that can be used to construct other Boolean logic functions that has potential for logic-in-memory, low energy, high endurance computing.

CHAPTER 5 SUMMARY AND FUTURE WORK

5.1 SUMMARY

This dissertation focused on my research efforts in spin current generation for spintronic logic device applications. Advancements in understanding of methods for generating spin currents for logic applications are critical for determining what types of devices will be potential candidates for beyond-CMOS applications.

A top-down fabrication approach for non-local lateral spin valves that can be used to integrate non-local spin valves with logic devices was developed. Using this approach, individual ferromagnet pillars with dimensions down to 75 nm were fabricated. Non-local spin signal was detected with the devices made using this approach, which is a valuable confirmation that this technique is compatible with the devices. This finding is important because it provides an alternative fabrication method which overcomes issues associated with commonly used techniques such as lift-off or shadow beam evaporation. Using the top-down approach, it is possible to pattern complex geometries, ensure scalability, and have a high level of control over material and interfacial properties.

The spin Hall effect was studied as a method to generate spin currents that can be applied to spintronic logic devices. Initially, the spin Hall effect was demonstrated in bulk perpendicular TbFeCo samples with a Ta spin Hall channel. Additionally, a composite ferromagnetic material stack structure was developed to overcome the fundamental limitation of not being able to switch a perpendicular ferromagnet solely via the spin Hall effect. The developed structure consists of a perpendicular ferromagnet, a spacer layer, and an in-plane ferromagnet where the in-plane ferromagnet provides a stray field allowing the

perpendicular layer to be switched using the spin Hall effect alone. To engineer the properties of spin Hall channels to change the spin Hall angle and conductivity, multilayer spin Hall channel stacks of Ta and W were developed. It was shown that the properties of the spin Hall channel can be tuned by varying the thickness of each multilayer as well as the number of repetitions. Finally, a majority logic gate is proposed that utilizes spin orbit torques combined with spin transfer torque for operation. Simulations were performed to verify the device concept and determined the required current values necessary to set the input states of the logic gate. Additionally, experimental work was presented which demonstrates the capability of being able to switch three ferromagnets that can act as inputs to the majority gate.

5.2 Ongoing Work

In non-local lateral spin valves, we have yet to demonstrate the switching of the detector ferromagnet using the pure spin current for our devices fabricated with the top-down approach. This demonstration is key to implementing all-spin logic. The fabrication approach presented in the dissertation allows for patterning of individual ferromagnetic pillars, which will aid in future studies using pure spin current for switching. This technique is being used to make devices for experiments to achieve switching of the detector ferromagnet. Furthermore, due to the control over the material properties with this approach, ongoing studies are being performed with more complex material stacks that have to potential to greatly enhance the performance of non-local lateral spin valves.

Additionally, there are ongoing research efforts to switch a perpendicular MTJ structure using the spin Hall effect without an external field. Using the idea of the composite structure presented in this dissertation, a full MTJ stack is being developed. Demonstration of perpendicular switching without an external field in MTJs is critical is the spin Hall effect is to be implemented in future devices such as STT-RAM or logic devices.

The development of the SOT-ST majority gate is also an ongoing research effort in our group. Currently, devices are being designed and fabricated with a strong top-pinned structure that should allow us to utilize MR readout of the MTJs as well as use SOT and ST for switching. Then, the devices can be fabricated into a majority gate to experimentally demonstrate setting and transferring information from the inputs to the output. Additionally, we are currently extending the simulation framework to include the output state of the device. Once this is implemented, we plan to implement the SOT-ST majority gate with CMOS nodes in order to perform benchmarking studies. This can be used to optimize the device in several ways. The pulse amplitudes and widths can be optimized to achieve the fastest operation speed as well as to find the most energy efficient current combinations and architecture for device operation. This will provide valuable information about the capabilities of the SOT-ST majority gate and allow us to compare it to current technologies as well as other possibilities for beyond-CMOS devices. With these benchmarking efforts, we hope to show the SOT-ST is a strong candidate and has many benefits as a spintronic logic device.

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