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Electromigration Modeling and Layout Optimization for Advanced VLSI

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Electromigration Modeling and Layout Optimization for Advanced VLSI

by

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To Sangman and Yoon

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Electromigration Modeling and Layout Optimization for Advanced VLSI

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Electromigration (EM) is a critical problem for interconnect reliability in advanced VLSI design. Because EM is a strong function of current density, a smaller cross-sectional area of interconnects can degrade the EM-related lifetime of IC, which is expected to become more severe in future technology nodes. Moreover, as EM is governed by various factors such as temperature, material property, geometrical shape, and mechanical stress, different interconnect structures can have distinct EM issues and solutions to mitigate them. For example, one of the most prominent technologies, die-stacking technology of three-dimensional (3D) ICs, can have different EM problems from that of planer ICs, due to their unique interconnects such as through-silicon vias (TSVs).

This dissertation investigates EM in various interconnect structures, and applies the EM models to optimize IC layout. First, modeling of EM is de-

veloped for chip-level interconnects, such as wires, local vias, TSVs, and multi-scale vias (MSVs). Based on the models, fast and accurate EM-prediction methods are proposed for the chip-level designs. After that, by utilizing the EM-prediction methods, the layout optimization methods are suggested, such as EM-aware routing for 3D ICs and EM-aware redundant via insertion for the future technology nodes in VLSI.

Experimental results show that the proposed EM modeling approaches enable fast and accurate EM evaluation for chip design, and the EM-aware layout optimization methods improve EM-robustness of advanced VLSI designs.

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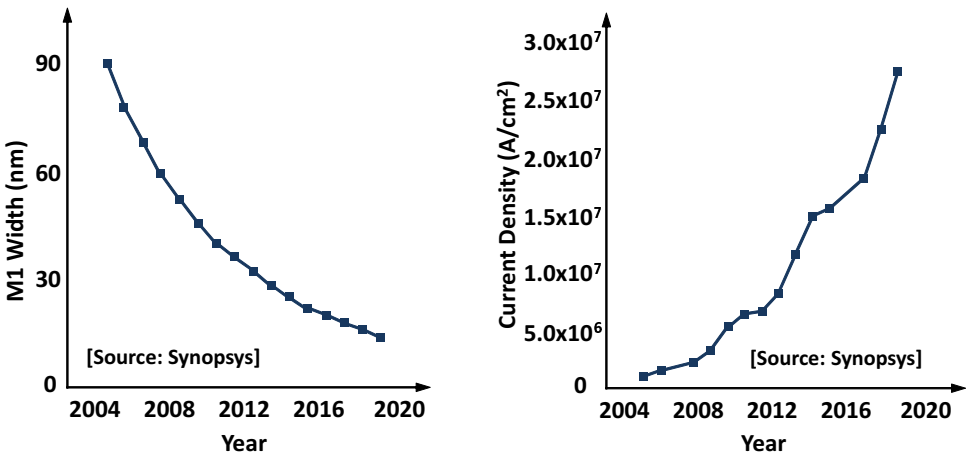
Chapter 1

Introduction

Electromigration (EM) is one of the major reliability concerns in advanced IC technology [28, 61]. EM is the transport of metal atoms due to the high current density [13], therefore a reduction in cross-sectional area of interconnects in advanced technology can aggravate EM-related failure time. Figure 1.1 shows the trends of wire width and current density as we move toward more advanced technology nodes. Moreover, since the total wire length within the unit area increases as the feature size shrinks, there can be a higher probability to have EM problems in the same area of ICs [27].

In advanced VLSI design, different parts of interconnects need different modeling approaches for EM analysis. For example, EM of via-wire interface in Figure 1.2(a) and EM in the wire in Figure 1.2(b) can have dissimilar void developments due to EM because of distinct geometrical shapes and material properties. Under the mechanical stress effect from the through-silicon-vias (TSVs) in 3D IC design [15,22,31], the gap of EM phenomena between various interconnects can be even larger, depending on the relative position from the TSVs. Thus, for each interconnect in the advanced VLSI using either smaller feature sizes or 3D IC technology, it is needed to have proper EM estimation

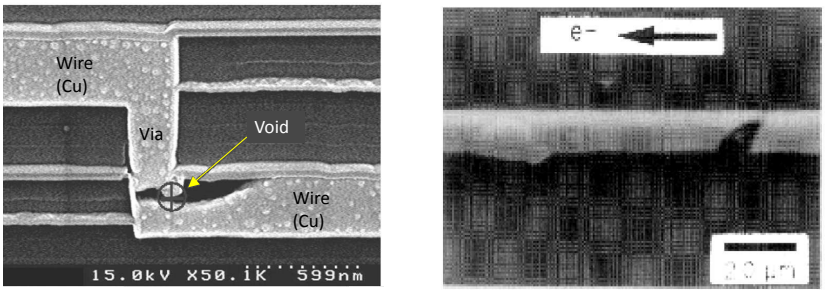


(a) (b)

Figure 1.1: Trends of wire width, length, and current density for the advanced technology nodes; (a) wire width scaling, and (b) current density trends [27].

methods for reliable chip designs. To enable EM estimation during chip design, the EM models should be fast enough to analyze billions of interconnects during design stages, and accurate enough to identify the EM characteristics of different interconnecting parts. After finding EM-hot spots, EM-aware design should be made for the physical design stage, for example, to make EM-aware routings or post-routing optimization.

In spite of the importance of EM estimation and EM-aware physical design in advanced IC design, there are very few studies that examine compact and accurate EM modeling or EM-aware layout optimization for full-chip level interconnects. Regarding the EM modeling part, some previous works focus on finite-element-analysis (FEA) with many parameters to predict an



(a) (b)

Figure 1.2: Scanning Electron Microscope (SEM) image of interconnects with EM problem, (a) EM at the via-wire interface [70], and (b) EM in a wire structure [55].

accurate lifetime from EM [23, 63, 72], but that causes a very long run time (a few hours) even for a single interconnect structure, thus they are not applicable for full-chip level evaluation with billions of interconnects. On the other hand, to achieve a reasonable run time for EM prediction, IC designers use simple empirical equations such as Black's equation as appeared in Eqn (1.1), estimating mean-failure time (MTTF) as a function of current density J and temperature T [13].

$$MTTF = \frac{A}{J^n} e^{\frac{-Ea}{kT}} \tag{1.1}$$

Although the Black's equation can give the upper bound of the reliability, it is neither applicable to various interconnect structures, nor counting the mechanical stress effect on EM. For the full-chip EM analysis, SysRel [7] is developed based on the tree-based cell analysis of EM. This work suggests the basis for the full-chip level EM analysis, but it does not consider mechanical

stress effect for the 3D ICs, and does not apply their EM analysis to the layout optimization such as routing or redundant via insertion. In terms of the EM modeling for the 3D ICs, there are initial works to study EM of TSVs through modeling [23,25,65] or measurement [20,25,26], but they do not cover EM modeling considering stress effects, nor EM of multi-scale vias (MSVs) combining TSVs and local vias, which can be used in the power network of 3D ICs.

For the EM-aware physical design side, there are few papers that study EM-aware routing considering current density [4,30,40,74], but none of these studies consider the mechanical stress effect, which is unavoidable for TSV-based 3D ICs. In the case of redundant via insertion after the routing stage, there are some papers that deal with redundant via insertion [8,35–37,41], but to the best of our knowledge, they do not considered EM as the key factor to decide redundancy of local vias.

Thus, the research motivation of this dissertation can be stated as follows:

- How can we estimate EM for various structures, fast and accurately?
- How can we apply EM study to chip design, to make a more robust design?

To answer above questions, this dissertation proposes fast and accurate EM prediction models for wires and vias, and suggests design optimization methods

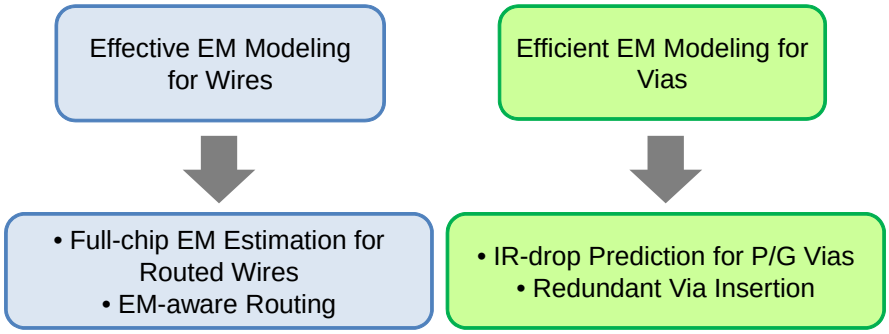


Figure 1.3: Scope of research in this dissertation.

to achieve EM-robustness, as illustrated in Figure 1.3. For the modeling part, EM models for both wire and via structures (e.g. TSVs, local vias and MSVs) are suggested. To achieve both high accuracy and a fast run time, look-up tables (LUTs) are utilized for the EM modeling. Because the LUT matches instantly parameterized input factors to the pre-simulated FEA results, the suggested method can estimate EM-induced lifetime fast and accurately. In case of via structures, for the voids developed under the via/TSV structures due to EM, transient void growth model is developed, and resistance LUTs are utilized to attain an accurate resistance value according to the void growth.

By utilizing the suggested EM models, the EM-hot spot can be detected for the routed wires for the full-chip level, and also the IR-drop of the power/ground networks can be evaluated, which is affected by EM. Furthermore, optimization of the layout is examined by EM-aware routing and EM-aware redundant via insertion, to achieve more robust IC designs. Here, EM-aware routing can be applied in place and route (P&R) stage, and via insertion technique can be applicable for post-layout optimization.

Overall, the contributions of this dissertation are summarized as follows:

- Modeling of EM with various structures such as metal wires, local vias, through-silicon vias (TSVs), and multi-scale vias (MSVs)
- Proposal of a method to perform fast and accurate full-chip EM simulation, to predict EM-hot spots in the design
- Suggestion of an effective EM-aware routing, considering current density, temperature and mechanical stress effect
- Analysis and modeling of EM for various redundant via layout, and optimize via insertion in the post-routing stage

The remainder of this dissertation is organized as follows. Chapter 2 and Chapter 3 introduce efficient EM modeling methods for TSVs and for wires. And then, EM modeling methods for MSVs in power/ground nets and for the local vias are suggested in Chapter 5 and Chapter 6, respectively. The proposed models start from the single wire/via structure, but they show potential extension for the full-chip analysis of EM-robustness. Based on the modeling, EM-aware routing for 3D IC design is suggested in Chapter 4. After that, EM-aware redundant via insertion for layout optimization is investigated in Chapter 6, and the dissertation is summarized in Chapter 7.

Chapter 2

Modeling of Electromigration in TSV Structures

2.1 Introduction

Electromigration (EM) can cause more reliability issues with 3D IC technology. While 3D IC technology has beneficial features such as realization of a small footprint, high bandwidth and suitability to heterogeneous systems [34], it also brings additional reliability issues such as mechanical stress from coefficient of thermal expansion (CTE) mismatch of TSV and silicon [45], higher temperatures due to the stacked structure [10], and higher current density to drive multiple dies. These problems in 3D ICs, higher current density, mechanical stress and temperature are the factors that can aggravate the EM phenomenon even further. Especially mechanical stress can be much more severe near the TSV region, and it can act as a crucial driving factor for EM.

There have been active studies on EM modeling of interconnects in traditional 2D ICs, especially for metal wires, local vias, bump metallization and solder joints [15, 22, 31]. However, in 3D ICs, despite the importance of EM which can shorten the lifetime of the system, only a few papers have been published regarding this issue. Shayan et al. considered mean time to failure

(MTTF) due to the EM based on Black's equation, for a power distribution network (PDN) for 3D ICs [60]. Trigg et al. demonstrated test chips for evaluation of 3D packaging reliability including EM [68]. However, these two works were not based on the EM model of the TSV. Chen et al. showed the EM model of the TSV structure with landing pads and a copper cylinder, but did not consider the effect on the wires, which can be connected to the landing pad [17]. Tan et al. showed that a TSV may fail due to thermo-mechanical stress and showed the modeling of TSVs in the interposer [65]. These works provided the initial basis for EM modeling of TSV. However, none of these works studied the detailed EM modeling of the TSV including metal wires connected to the landing pad, or the relationship between TSV sizing parameters and EM.

In this chapter, EM modeling with a detailed TSV structure and connected metal wires is proposed. The structure for our modeling includes materials such as interlayer dielectric (ILD), silicon dioxide and benzocyclobuten (BCB). With our model, we look into the impact of mechanical stress gradients and current crowding on the EM-induced lifetime of TSV structure, and have experiments with various geometries of the TSV structure.

2.2 Background

Electromigration (EM) can be defined as the mass transport of atoms due to various driving forces such as current density, mechanical stress gradient, and temperature [31, 42]. EM can be expressed by the mass balance

equations of vacancy concentration [15, 64],

$$\nabla \cdot \vec{q} + \frac{\partial c}{\partial t} = 0 \tag{2.1}$$

where

$$\vec{q} = \frac{Dc}{kT} Z^* e \rho \vec{j} + \frac{Dc}{kT} Q^* \frac{\nabla T}{T} - \frac{Dc}{kT} f \Omega \nabla \sigma - D \nabla c, \tag{2.2}$$

$$D = D_0 \cdot exp\left(\frac{\Omega\sigma - Ea}{kT}\right). \tag{2.3}$$

Here, $\vec{q}$ is total vacancy flux, c is vacancy concentration, $\vec{j}$ is current density vector, T is temperature, σ is hydrostatic stress, Q^* is the heat of transport, and D is diffusivity with initial diffusivity D_0. Table 2.1 shows the parameter values that we use.

The transport of atoms in a structure induces back-stress and it affects EM again; back-stress acts to compensate EM [21]. We note that stress gradient $\nabla\sigma$ makes EM compensating term from Eqn. (2.2). According to work in [69], although back-stress is induced by EM, externally applied stress can affect EM similarly. Thus, if TSV-induced stress has the same polarity

Table 2.1: Parameter values for EM modeling of TSV and neighboring wires

Parameter	Representation	Value
Ea	Activation energy	1.3e-19
k	Boltzmann constant	1.38e-23
Z^*	Effective charge	4
e	Electron charge	1.6e-19
Ω	Atomic volume	1.6e-29
f	Atomic volume coefficient	0.8
D_0	Initial diffusivity	1e-8
ρ	Resistivity of copper[Ωm]	2.2e-8

of stress gradient as back-stress, which is the positive stress gradient with respect to current flowing direction, it can help in compensating EM. On the other hand, if a negative stress gradient with respect to current direction is applied due to TSV, it can aggravate EM. We use a finite-element-analysis (FEA) solver named ANSYS, to get stress data of a wire near a TSV. To consider multiple TSV effects, we use a single TSV stress data and superposition method [47]. For simulation of EM as a form of transient vacancy concentration of structures, we use an FEA solver named COMSOL Multiphysics to solve Eqn. (2.1)-(2.3) for TSV and wire structure. The current crowding effect at the interface of a TSV landing pad and a connected wire is also considered during FEA simulation of the TSV structure. We define 5% deviation of vacancy concentration as *failure* [31], and get the minimum time to reach 5% deviation of vacancy concentration for time-to-failure (failure time) of various locations of metal wire during our FEA simulation.

2.3 EM Modeling of TSV

2.3.1 TSV Structure for EM Evaluation

So far, TSVs of various sizes have been proposed by different papers [29, 45, 58, 65]. We assume the TSV diameter as 4um, the landing pad size as 5um by 5um, and the thickness of the silicon substrate as 30um, similar to that by IMEC [29]. For the via-first approach, the top landing pad of the TSV is connected to the first metal layer, while the bottom landing pad touches the top metal layer. We also vary the size of the TSV diameter to see its impact

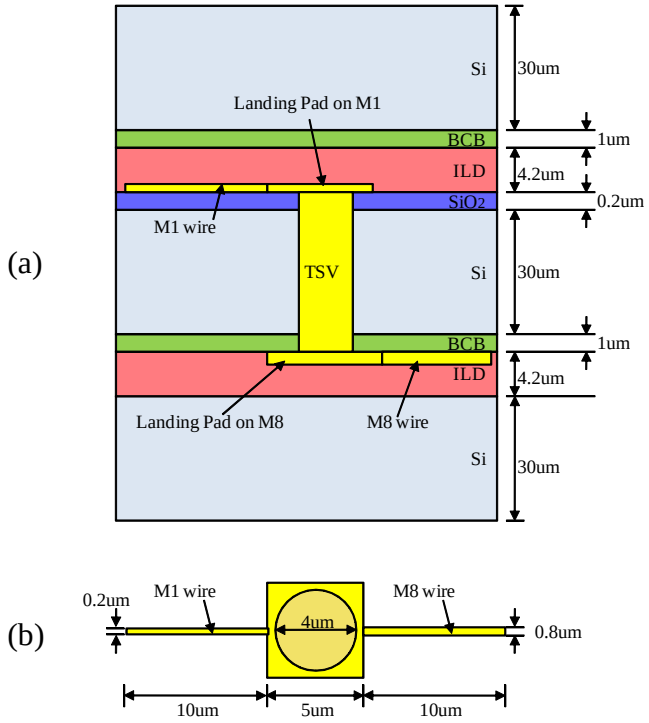


Figure 2.1: (a) Cross subsection of 3-die stacking structure with a via-first TSV. (b) Top-down view of the TSV, landing pads and connected wires.

on EM.

Figure 2.1(a) describes the TSV structure we use to simulate the thermo-mechanical stress due to the coefficient of thermal expansion (CTE) mismatch. The properties of the materials are shown in Table 2.2. In Figure 2.2, we show the testing points in the TSV structure; we test the ends of the connected wires, on the top and bottom landing pads, and inside of the TSV cylinder. For the experiments, we assume that a current density of $1e10A/m^2$ enters through the M1 wire from point 'A'. To clearly show the stress effect on EM, we display the stress profile along the certain paths in Figure 2.2. Figure 2.3

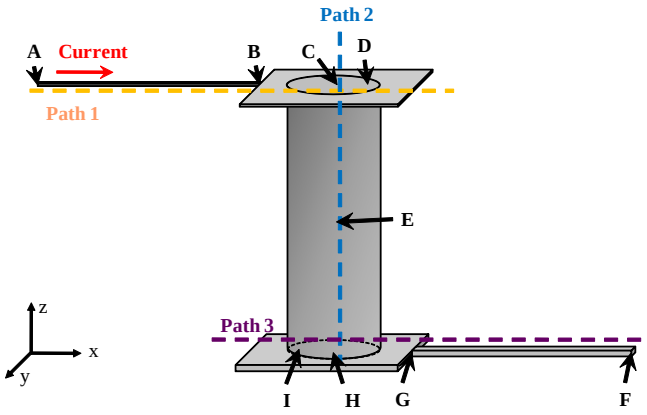


Figure 2.2: TSV structure and testing points for experiments. A, F are the ends of the wire; B, G are the interface between the landing pad and the wire; C and H are in the center of the TSV on top and bottom side; D, I are 0.75×radius point from the TSV center; E is in the middle of the TSV cylinder. Path 1 and path 3 lie along the x-axis while path 2 lies along the z-axis.

is the stress profile along these three paths.

2.3.2 Impact of TSV Radius on EM

To measure the degradation EM caused, we define a time metric, called 'failure time (Tf)', to measure how long it takes for vacancy concentration

Table 2.2: Material Properties of TSV structure

	Youngs Modulus (GPa)	Poisson's Ratio	CTE (1/K)
Silicon	162	0.28	3.05e-6
Copper	111.5	0.343	1.77e-5
Silicon Oxide	71.7	0.16	5.1e-7
ILD	9.5	0.3	2.0e-5
BCB	6.1	0.35	3.3e-5

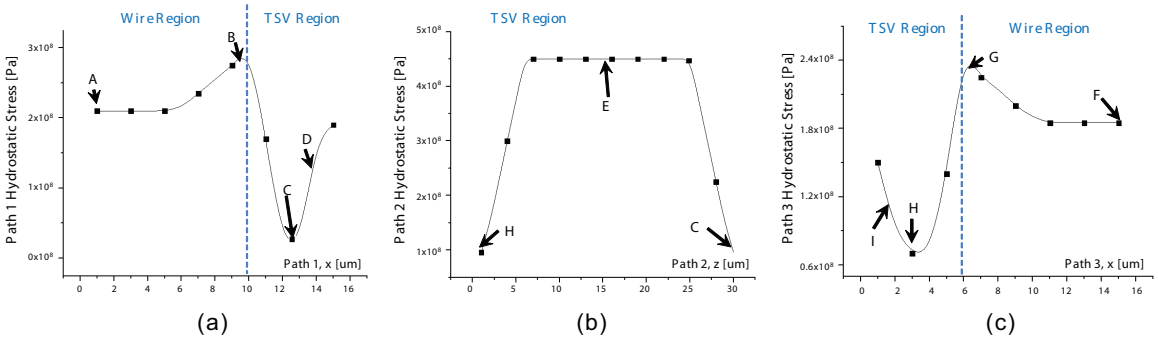


Figure 2.3: Stress profile along the paths shown in Figure 2.2. (a), (b), and (c) shows stress along the path 1, 2, and 3.

Table 2.3: Normalized failure time (Tf) for different TSV radius

radius	A	B	C	D	E	F	G	H	I
2um	11.1	6.75	0.25	1	>83	>83	10.7	1	3.17
3um	11.0	5.83	0.15	0.51	>83	>83	8.67	0.53	1.25
4um	11.0	5.00	0.11	0.38	>83	>83	8.17	0.31	0.58

variation to reach a certain threshold. In this model, we use 5% deviation of vacancy concentration [31] as the threshold, and compute the fastest time that reaches such deviation. Depending on the failure criteria, current density, magnitude of TSV-induced stress, and the values of various constants, the actual value of Tf can vary. However, the overall trend remains the same. Thus, we use a normalized Tf to show the trends.

We change the TSV radius from 2um to 4um, and see the impact on Tf. We also increase the landing pad size from 5um to 10um to keep the ratio of landing pad over the TSV diameter as a constant. Table 2.3 shows the normalized Tf for different TSV radius.

In all cases, point 'C' tends to fail first, and points 'D', 'H', 'I' fail relatively early. These four points tend to have the maximum stress gradients around them. Due to difference in the thickness of the top landing pad and the bottom landing pad, and also due to the difference in the properties of the materials surrounding them, points 'C' and 'D' tend to have a higher stress gradient as compared to points 'H' and 'I'. Thus, points 'C' and 'D' tend to fail before points 'H' and 'I'. Points 'B' and 'G', the interface of the landing pad and the wire, fail next. Here, the amount of stress gradient is less than that of the TSV center, but these points still have a higher stress gradient compared to the other points. Due to the higher stress gradient at 'B', it tends to fail earlier than 'G'.

The failure at points 'A' and 'F' is impacted only by the amount of current density in these regions. Since the wire connecting to point 'F' has greater width and thickness, it has lower current density, thus it tends to fail slower compared to 'A'. Point 'E' is typically the most robust point, not only does it not have any stress gradients, but also the current density inside of the TSV cylinder is low enough. In general, we observe that TSV-induced stress can increase the number the number of points where failure may occur.

By increasing the TSV radius, the amount of stress gradient around the stress-hot region gets larger, therefore 'B', 'C', 'D', 'I', 'H', 'G' fail earlier than the smaller radius of TSV. The failure time (Tf) of other points does not change much. We can see that Tf of the TSV structure is largely dominated by the TSV-induced stress gradient. Figure 2.4 shows the atomic concentra-

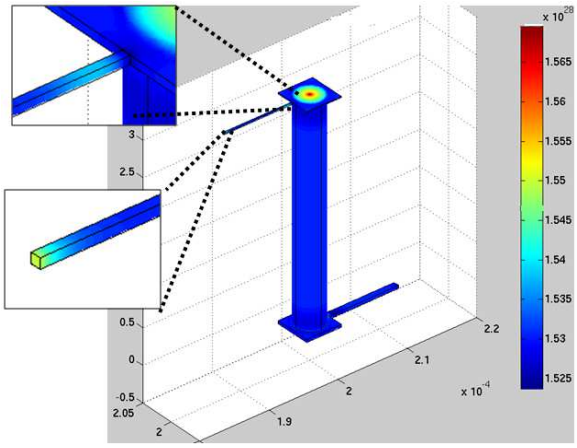


Figure 2.4: Atomic concentration on the TSV structure at normalized time=8.3.

tion on the TSV structure. In this figure, point 'C' has the highest atomic concentration.

2.3.3 Impact of Landing Pad Size on EM

Using the via-first structure as shown in Section 2.3, we investigate the impact of the landing pad size of the TSV. In this case, we use the same TSV radius, 2um, and change the landing pad size from 5um to 15um as shown in Table 2.4. Here, the landing pad size refers to the width or the height of the landing pad. As the landing pad size increases, the Tf of points 'B' and 'G' increases. This is because the increase in distance from the TSV center causes a smaller stress gradient at points 'B' and 'C'. However, points 'C', 'D', 'H', 'I' tend to fail earlier. This occurs because the greater mismatch in the landing pad size and the TSV radius causes larger stress gradients.

Table 2.4: Normalized failure time Tf for different landing pad size

LP size	A	B	C	D	E	F	G	H	I
5um	11.1	6.75	0.25	1	>83	>83	10.7	1	3.17
10um	11.1	19.4	0.13	0.42	>83	>83	38.2	0.39	1.21
15um	12.8	39.1	0.10	0.26	>83	>83	78.1	0.22	0.61

2.3.4 Study of Via-last Structure

In this subsection we study the EM impact on the via-last structure. In the via-last structure, both the top and bottom landing pads are on the top metal layer. Typically the via-last structure has much a larger TSV cylinder and landing pad size due to its fabrication process. Figure 2.5 shows the via-last structure used in our simulations. We assume the TSV radius to be 10um and the TSV height to be 150um. The landing pad size is assumed to be 25um by 25um.

Table 2.5 shows the normalized Tf for each test point. In the via-last structure, points 'D', 'H', 'I', fail earlier than a via-first case, due to the large amount of stress gradient caused by the bigger TSV structure. Point 'C' tends to fail later as compared to the via-first structure. Because point 'C' is far away from the interface of landing pad and TSV cylinder, we have a smaller stress gradient at the center of the TSV (point 'C') compared to the via-first structure. The point on the lower wire and landing pad interface, 'G', does not show much difference between the via-first and via-last case, because the structure of lower wires are the same in both cases. Meanwhile, the points on the upper wire, 'A' and 'B' have a larger Tf in the via-last structure because

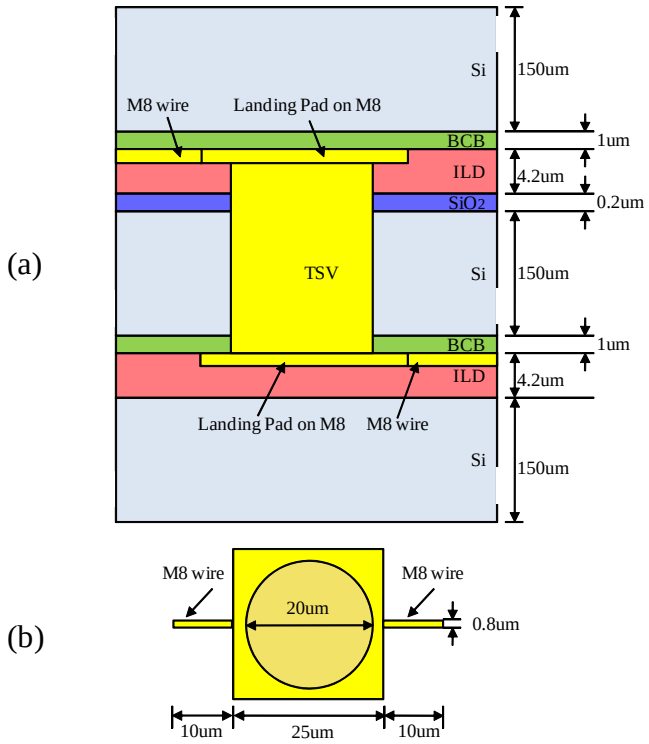


Figure 2.5: (a) Cross subsection of 3-die stacking structure with a via-last TSV for simulation. (b) Top-down view of the TSV, landing pads and connected wires. Note that the figure is not to scale.

they have a smaller current density and a lower amount of stress gradient than the via-first case.

2.3.5 Summary

So far, we have investigated EM and the EM-induced lifetime of a TSV for 3D IC designs. First, we found that TSV-induced mechanical stress can play a great role of EM-related lifetime. For example, TSVs with a smaller size lead to smaller stress gradients from CTE mismatch, thus they are less

Table 2.5: Normalized Tf for via-last versus via-first TSV

	A	B	C	D	E	F	G	H	I
Via-First	11.1	6.75	0.25	1	>83	>83	10.7	1	3.17
Via-Last	55	12.5	0.54	0.53	>83	>83	10.8	0.39	0.4

likely to fail due to TSV-induced stress. If the wire and landing pad interface is close from the TSV structure, the interface can have early failures due to the stress effect. Finally the via-last TSV structure tends to have a greater stress gradient but lower current density, thus the via-last structure may cause more failures due to TSV-induced stress than due to the high current density. In the following chapter, we will further investigate the TSV-stress impact on the EM lifetime of wires.

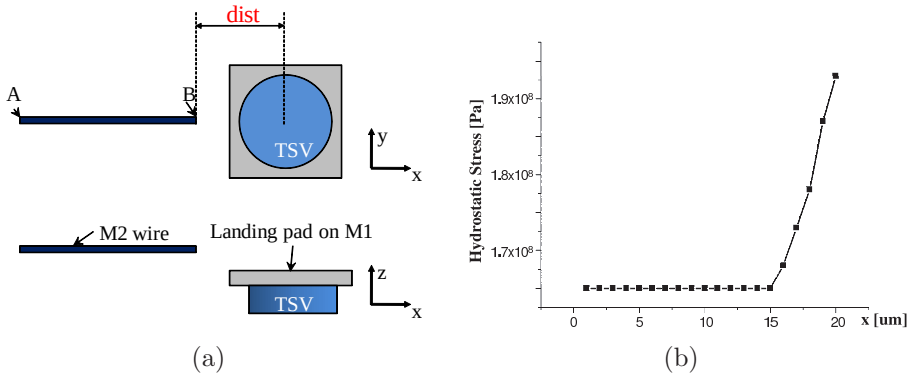
Chapter 3

EM Modeling of Wire Structures and Full-chip EM Prediction for 3D ICs

3.1 Introduction

In Chapter 2, we model EM of TSV structures. In this chapter, we propose stress-aware EM modeling of metal wires in 3D ICs, and show full-chip level EM prediction for 3D IC. TSV causes a significant amount of mechanical stress, due to different coefficient of thermal expansion (CTE) of silicon and copper [45], and it can affect EM of neighboring wires [69]. As we explain in Section 2.2, such stress can either degrade or improve the lifetime of the wires depending on the stress gradient of the wire [21], in other words, depending on the relative position from the TSV and the current direction. Overall, the contributions of this chapter are summarized as follows:

- We model EM of metal wires in 3D ICs while TSV-induced stress consideration
- We predict failure time (Tf) of wires in 3D ICs with considering temperature, current density and TSV-induced stress gradient
- We propose a method to perform fast full-chip simulation, to determine the various EM related hot spots in the design.



(a) (b)

Figure 3.1: (a) Structure to investigate a wire in normal direction of TSV, top-down view and cross-subsectional view. (b) Stress profile along the wire when $dist = 3.5um$. $x = 0$ is point A, and $x = 20um$ is point B.

3.2 Impact of Relative Position of Wires and TSV on EM

3.2.1 EM Modeling of Wires Near the TSV

For the EM modeling of wires in TSV-based 3D ICs, we use the same modeling approach as discussed in Section 2.2. Figure 3.1(a) shows the wire in a normal direction with respect to the TSV center, and Figure 3.1(b) shows the stress profile along the wire. We can see that TSV-induced stress level is the highest at point B along the wire. Therefore, if the current flows from A to B, a positive stress gradient exists with respect to the current flowing direction. On the other hand, if the current flows from B to A, a negative stress gradient exists. As we discussed earlier, positive stress with respect to current direction helps to compensate EM, while a negative stress gradient aggravates EM. Thus we measure failure time with two different current directions; from A to B and from B to A.

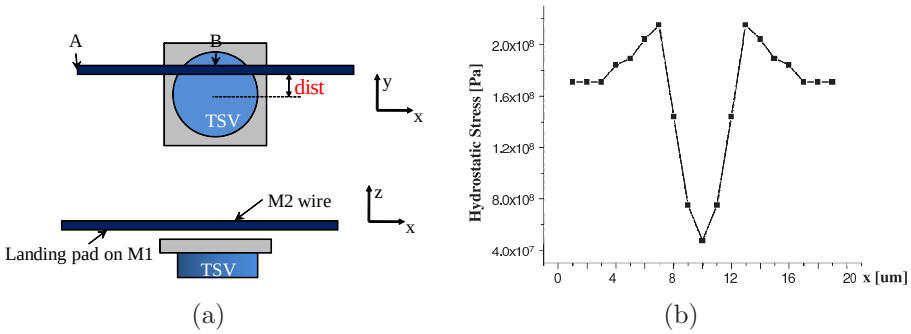
Table 3.1: Normalized failure time for wire in a normal direction, with two different current directions.

dist	current A to B		current B to A	
	Tf_A	Tf_B	Tf_A	Tf_B
3.5um	1	2.12	1	0.49
4.5um	1	1.37	1	0.73
5.5um	1	1.13	1	0.88
6.5um	1	1.01	1	0.98

For the two different current directions, we measure failure time with FEA simulation. The normalized failure time of test points with two opposite current directions are shown in Table 3.1. Here, *dist* is the distance between a wire and a TSV center. As expected, when the current flows from A to B, a positive stress gradient exists according to the current direction, which helps to compensate EM. Hence test point B lives longer than A. However with the opposite current direction, and the current flowing from B to A, a negative stress gradient appears with respect to current flowing direction on point B, and it can worsen EM at B. Therefore B can fail earlier than A. If *dist* increases, the mechanical stress from TSV becomes smaller, and its impact on EM gets weaker for both current directions. We use wire width and height as 0.2um, TSV radius as 2um, and landing pad size as 5um by 5um. Temperature is assumed as $50°C$, and current density is $1e10[A/m^2]$.

3.2.2 EM Modeling of Wires Go Across the TSV

Figure 3.2(a) shows the structure when a wire goes across a TSV, and Figure 3.2(b) shows the stress profile along a wire. In this case, the TSV-



(a) (b)

Figure 3.2: (a) Structure to investigate a wire goes across the TSV, top-down view and cross-subsectional view. (b) Stress profile along the wire when $dist = 0um$. $x = 0$ is point A, and $x = 10um$ is point B.

induced stress level goes up around the TSV-silicon interface, and goes down in the middle of the TSV. Since we have a drastic change of stress including a negative stress gradient at point B in Figure 3.2, the failure time of B is shorter than A. We note that stress tendency is symmetrical according to TSV center. Therefore, a similar tendency can be expected for the opposite current direction in this case. In our experiment, we use current flows from A to B with current density as $1e10[A/m^2]$, and assume the temperature of wire as $50°C$.

Without TSV-induced stress, EM mostly occurs at the boundary of the structure, in other words, at both ends of the wire. However as TSV-induced stress generates additional stress gradient on the wire, the middle of the wire can fail earlier than the ends of the wire. In our results in Table 3.2, the normalized failure time of point B is shorter when the $dist$ is smaller than the TSV radius, which is 2um. From $dist = 3um$, the wire goes outside of the

TSV region, thus the middle of the wire (=point B) starts to live longer than the end of the wire (=point A).

Table 3.2: Normalized failure time when wire runs over TSV.

dist	Tf_A	Tf_B
0um	1	0.22
1um	1	0.22
2um	1	0.31
3um	1	1.47

3.3 Impact of Routing Layers on EM

The magnitude of the TSV-induced stress on a wire depends on the distance between the wire and TSV center as shown in the previous subsections. Thus, for the higher metal layers, the impact of the stress becomes smaller. In addition, current density can vary depending on the metal layer. Figure 3.3 describes our experimental structure to observe the impact of different metal layers on EM of 3D IC. The wire is lying along the tangential direction as discussed in Section 3.2.1, and we change the metal layers. To see the reduced stress effect and current density effect more clearly, we design two sets of experiments.

First, we assume the same current density on the metal wire for all layers to solely see the impact of vertical distance from the TSV. In other words, as the vertical distance from the 'stress-hot region' gets larger, a wire becomes more robust to EM. Simulated Tf results are shown in Table 3.3. At point 'B', Tf is shorter than other regions. This is because the stress gradient

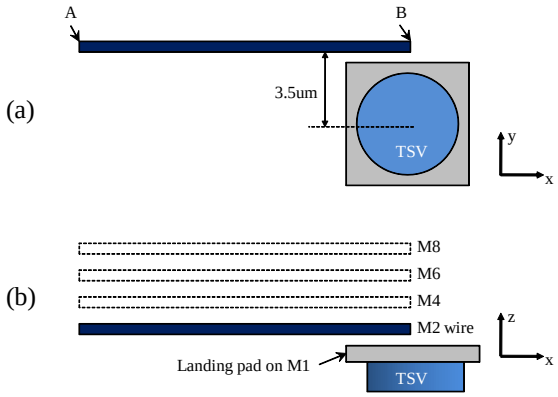


Figure 3.3: Structure to investigate the metal layer impact: (a) top-down view, (b) cross-subsection view of the structure. A is the farthest point and B is the closest point from the TSV.

accelerates atomic movement as discussed in Section 3.2.1. However, as the metal layer goes up, the absolute value of the stress gradient gets smaller, and Tf becomes longer. It means a wire in a higher metal layer is less likely to fail than the lower metal wire due to lower TSV-induced stress.

Table 3.3: Normalized Tf and stress gradient for different metal layers, where the current density is same across layers

	Normalized Tf		Stress gradient [Mpa/um]		Current Density [A/m^2]
Metal Layer	A	B	A	B	Both A and B
M2	1.00	0.37	0.00	-11.9	1e10
M4	1.00	0.39	0.00	-7.12	1e10
M6	1.00	0.68	0.00	-1.49	1e10
M8	1.00	0.76	0.00	-0.37	1e10

Second, we see the impact of different current density in the different metal layers on EM in addition to the distance effect. As a wire in the upper metal layer becomes thicker and taller, the cross area of the wire increases

Table 3.4: Wire width, height and current density values used

Metal Layer	Width	Height	Cross Area $[m^2]$	Current [A]	Current Density $[A/m^2]$
M2	0.07um	0.14um	9.8e-15	9.8e-5	1e10
M4, M6	0.14um	0.28um	3.92e-14	1.96e-4	5e9
M8	0.4um	0.8um	3.2e-13	3.92e-4	1.225e9

Table 3.5: Normalized Tf and stress gradient for different metal layers, current density is different across layers

	Normalized Tf		Stress gradient [Mpa/um]		Current Density $[A/m^2]$
Metal Layer	A	B	A	B	Both A and B
M2	1.00	0.37	0.00	-11.9	1e10
M4	3.95	0.94	0.00	-7.12	5e9
M6	3.95	1.98	0.00	-1.49	5e9
M8	>33	>33	0.00	-0.37	1.225e9

and it can reduce the current density. Meanwhile, global interconnects are preferred on higher metal layers [6,9]. Long global nets with higher capacitance on higher metal layers tend to have a greater current than the lower metal layers [59]. We assume that the M8 wire delivers a 4 times larger current, and the M4/M6 wire delivers a 2 times larger current than the M2 wire. Current density for each layer is calculated based on the 45nm technology standard as shown in Table 3.4. We observe that the M8 wire has a lower current density compared with the M1 wire.

The Tf with different current densities according to the metal layer is shown in Table 3.5. Higher metal layers tend to be more robust due to lower current density and lower stress gradients. The Tf of the M8 wire is much larger than the M2 wire for the specified current density.

Table 3.6: Normalized stress gradient values for different TSV radius and distance from TSV

TSV radius	1x dist	2x dist	3x dist	4x dist
2um	1.000	0.380	0.097	0.010
3um	1.000	0.423	0.112	0.007
4um	1.000	0.405	0.087	0.001

3.3.1 Impact of TSV Radius on Safe Margin

If the TSV radius is large, the stress-hot region around the TSV is also large and it affects EM robustness for a wider area around the TSV. To see the relationship between the TSV radius and the distance from the TSV that guarantees the low stress gradient, we measure the stress gradient on a wire by changing the radius of the TSV. The simulation structure is the same as shown in Figure 2.1 in Section 2.3. We change the TSV radius and measure the stress gradient by changing the distance from the TSV.

Results are shown in Table 3.6, if the distance between the wire and the TSV center is more than 3 times the radius (3x dist.), TSV-induced stress falls to about 10% of the value observed at 1x point. Lower stress gradient levels can reduce the impact of stress induced failure. We observe that for larger TSVs, a larger distance from the TSV may be needed to achieve increased robustness.

3.4 Full-chip Level EM Risk Prediction

Based on our discussion in Section 3.2.1, we observe that stress can have a significant impact on the EM reliability of a metal interconnect. We extend our EM modeling to full-chip level design [54]. With TSV-induced stress, Black's equation is no longer valid to predict the failure time, and we need to solve Eqn. (2.1)-(2.3) using an FEA simulator to estimate the failure time [42]. However, it is very time consuming and impractical to use for full-chip level design. For fast EM estimation of interconnects during routing, we use an *EM library*. An *EM library* is a look-up table to get the failure time from inputs such as current density, temperature and stress gradient. We build the *EM library* by solving Eqn. (2.1)-(2.3) for a simple wire using an FEA simulator. Because we exhaustively simulate Tf values with possible combinations of current density, temperature and stress gradient for *EM library*, fast estimation of the failure time of each wire can be made for full-chip level design. Figure 3.4 shows the flow of our full-chip level EM prediction method.

To predict failure time of interconnects from a given layout, we need to estimate stress gradient value, temperature, and current density, which are inputs of our *EM library*. For estimating stress level of a certain point with given TSV locations, we use an FEA simulation result for a single TSV and a superposition method to consider multiple TSV effects [47]. From Eqn. (2.2), EM is a function of stress gradient $\nabla\sigma$, which is the rate of increase of stress. Because we can reasonably assume that a wire is a one-dimensional structure, the direction of the current in a routed wire is a decisive factor to select stress

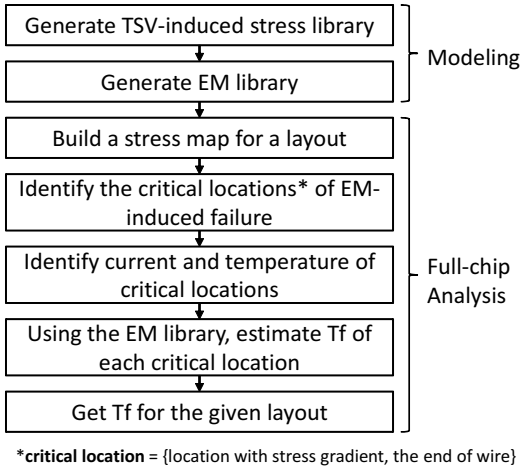


Figure 3.4: Flow of full-chip EM estimation of wires for 3D ICs.

gradient vector. For example, if a wire is positioned along the $+x$ direction and current flows in $+x$ direction, stress gradient is interpreted as $\nabla\sigma = \frac{\partial\sigma}{\partial x}\hat{\mathrm{x}}$. Temperature is simulated with ANSYS FLUENT with logic power dissipation information, and current density is extracted with a method in [59] from a design exchange format (DEF) file. With stress map, temperature and current density information, failure time of any wire can be predicted with the *EM library*. All our experiments are performed on a Linux 2.4 GHz processor and our algorithms are implemented in C++. We analyze the impact of TSV on M2 wires near the TSV with 4-die stacked system.

3.4.1 Full-chip EM Prediction for 3D ICs

In Figure 3.5 (b), we plot the result of how hydrostatic stress would vary for vertical wires of given circuits. The result would be different for horizontal wires, however, it can be computed easily using symmetry. We observe that

Table 3.7: Comparison between CST, CT, and ST consideration on EM analysis. EM_f is the number of EM failed wires.

ckt	#TSV	Total wire length [um]	EM_f		
			CST	CT	ST
ckt1	934	3.33×10^5	503	418	150
ckt2	1034	3.95×10^5	384	294	123
ckt3	1107	7.95×10^5	497	436	98
ckt4	1336	2.19×10^6	713	628	138

variation in stress, which causes a stress gradient, occurs in regions that are close to the TSVs. To see the impact of different factors of EM, i.e. current, stress and temperature, we perform a full-chip analysis with different driving factor considerations. The results are shown in Figure 3.5 and Table 3.7. In Figure 3.5 (d) we plot the failure map when we consider current, stress, and temperature (CST). The effect of stress and temperature (ST), current and temperature (CT) on EM is shown in Figure 3.5 (e), (f) respectively. We observe that under ST consideration, EM failure is detected especially near the TSV location. Detailed results are shown in Table 3.7. We show the number of TSVs, total wire length, and number of critical wires found using each driving factor consideration, CST, ST and CT.

3.4.2 Effect of Routing Blockage Around TSVs on EM

To improve the EM-reliability of M2 wires in 3D ICs, we add routing blockages around TSVs. The routing blockages ensure that no metal wires go near a TSV location, thus can prevent stress-induced EM failure. The results are shown in Table 3.8. We compare the number of wires likely to fail (EM_f)

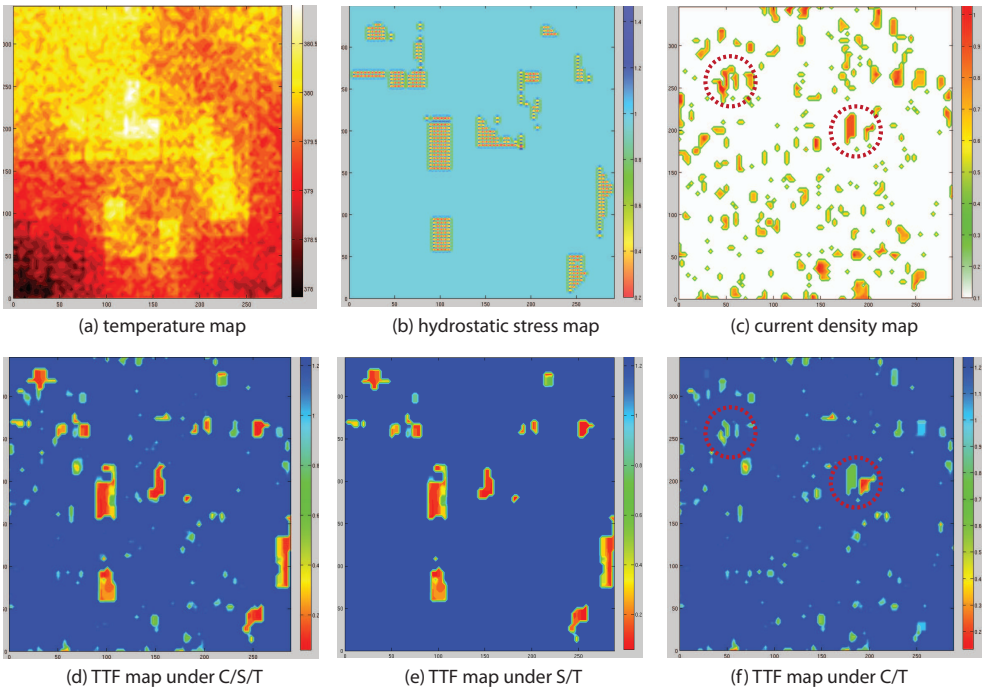


Figure 3.5: (a) Temperature map. (b) Map of variation of hydrostatic stress for vertical wires. (c) Map of current density. (d) Map of critical wires when considering current, stress, and temperature. (e) Map of critical wires when considering stress, and temperature. (f) Map of critical wires when considering current, and temperature. Circled regions in (c) and (f) show that high current density region correspond to critical locations.

and the wire length. As presented in Table 3.8, adding routing blockages reduces the number of wires that may fail. With routing blockages there are fewer wires that get affected by TSV induced stress, thus we can increase the reliability. The impact on total wire length is less than 1%.

Table 3.8: Impact of routing blockages on EM reliability of 3D IC. EM_f is number of EM failed wire and WL is total wire length in μm.

		No Routing Blockage		Routing Blockage	
ckt	# Gate	EM_f	WL	EM_f	WL
ckt1	14864	503	3.33×10^5	435	3.34×10^5
ckt2	19895	384	3.95×10^5	224	3.96×10^5
ckt3	29706	497	7.15×10^5	378	7.17×10^5
ckt4	103991	713	2.19×10^6	587	2.22×10^6

3.5 Summary

Electromigration (EM) problems can be more severe and complex in 3D ICs due to TSV-induced stress, higher temperature and current density that affect EM. In this chapter we show that TSV-induced stress can impact on EM reliability of metal wires in 3D ICs. We model EM with TSV-induced stress consideration, and show how TSV-induced stress can affect the EM failure time of nearby metal wires. In addition, we propose a method to perform fast full-chip EM analysis for 3D ICs while considering the effect of TSV stress. Our work shows that TSV-induced mechanical stress can play a crucial role on EM reliability of interconnects in 3D ICs.

Chapter 4

Electromigration-aware Routing in 3D ICs

4.1 Introduction

As we mentioned in Section 2.1 , EM can cause more reliability issues with 3D IC technology, due to the higher power from interconnects [34], thermal issues [10] and mechanical stress from TSV structures [45, 47]. Especially, mechanical stress can influence electromigration (EM) significantly; applied stress can either retard or accelerate EM depending on the stress gradient and the current direction [69]. We note that significant mechanical stress can be caused by TSVs after annealing process due to the different CTE between copper and silicon [45]. Thus, TSV-induced stress can be a driving force for EM, and can affect the EM of interconnects in 3D ICs [17, 53, 54, 65]. We observe unique characteristics of EM in metal wires in 3D ICs from recent works in [53, 54]:

1. TSV-induced stress affects EM near the TSV region
2. EM can be either mitigated or aggravated near the TSV region depending on routing direction because the stress gradient has an impact on EM, and the stress gradient varies with routing direction

3. The lowest metal layer (M1) can be the most dangerous layer on EM due to not only the highest current density and temperature, but also the highest stress gradient among all metal layers

If TSV-induced stress had only a negative effect on EM, avoiding TSV region could be the only solution in mitigating EM problem, and it could waste a large routing resource. However, as EM-induced lifetime can be varied depending on the routing direction, EM-aware routing can further improve EM-robustness and utilize routing resources more effectively near the TSV region. Moreover, since each metal layer has different TSV-induced stress, current density and temperature profiles, a smarter routing scheme can accommodate better reliability across multiple metal layers.

In traditional 2D ICs, a simple and effective way to reduce EM is decreasing current density. Hence, previous works to enhance EM-robustness focused on routing with optimization of wire width, or current-driven routing to achieve reliability [4, 30, 40, 74]. Although these works provide reasonable ways to raise EM-robustness in 2D ICs, 3D ICs raise additional issues like mechanical stress and higher temperature on top of higher current density, thus wire width adjustment or current-driven routing are no longer sufficient to guarantee EM-robustness. For 3D ICs, new methodologies are needed to make EM-aware routes, with consideration of TSV-induced mechanical stress and temperature, as well as current density.

In this chapter, we propose an EM-aware routing that can effectively choose EM-safe paths for multiple routing layers. To achieve the goal, we model EM in 3D ICs and build an *EM library* for quick estimation of EM for a certain layout. After that, we order the nets with EM criticality and wire length. Finally we estimate EM criticality for each routable grid during maze routing, and search the EM-safe path using the cost function. Because most of signal nets are AC nets, we use the *equivalent DC current* for AC nets. As a result, our EM routing can deal with both DC and AC signal nets in 3D ICs.

4.2 Stress-aware EM Modeling for 3D ICs

4.2.1 Modeling of EM with Stress Consideration

As we discussed in Section 2.2, with TSV-induced stress, Black's equation [13] is no longer valid to predict MTTF, and we need to solve Eqn. (2.1)-(2.3) using a finite-element-analysis (FEA) simulator to estimate the MTTF [42], which can be very time consuming. For fast MTTF estimation of interconnects during routing, we use the EM library introduced by [54]. An EM library is a look-up table to get MTTF from inputs such as current density, temperature and stress gradient. We build the EM library by solving Eqn. (2.1)-(2.3) for a simple wire using FEA simulator. Because we exhaustively simulate MTTF with possible combinations of current density, temperature and stress gradient for the EM library, a fast estimation of MTTF can be made during the routing stage. Meanwhile, we use linear interpolation for intermediate values to maintain a reasonable library data size and to avoid computational overhead.

4.2.2 Generating Stress Gradient Maps

Near the TSV region, mechanical stress is generated from the coefficient of thermal expansion (CTE) mismatch of silicon and copper [45]. To estimate the stress level of a certain point with given TSV locations, we use an FEA simulation result for a single TSV and a superposition method to consider multiple TSV effects [47]. We assume a planar stress model as introduced in [45]. Figure 4.1 shows a stress map of one of our benchmarks. From

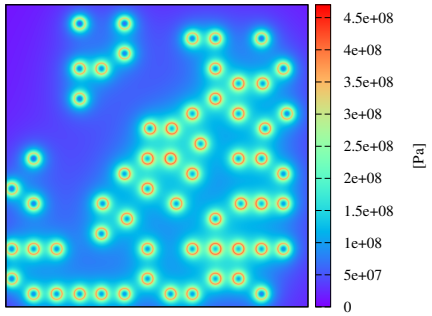
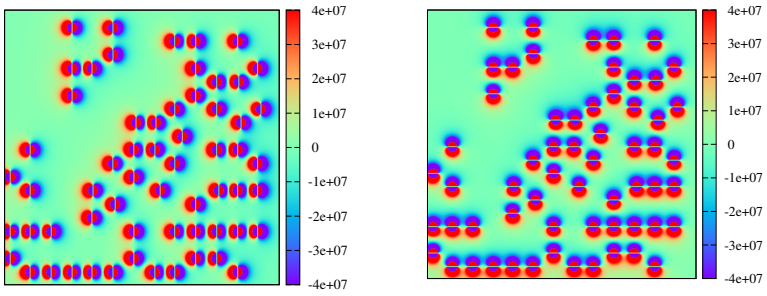


Figure 4.1: Stress map of one of the benchmark circuits. A circular shape represents a TSV.

Eqn. (2.2), EM is a function of stress gradient $\nabla\sigma$, which is the rate of increase of stress. Because we can reasonably assume that a wire is a one-dimensional structure, the direction of the current in a routed wire is a decisive factor to select the stress gradient vector. For example, if a wire is positioned along the $+x$ direction and current flows in the $+x$ direction, the stress gradient is interpreted as $\nabla\sigma = \frac{\partial\sigma}{\partial x}\hat{\mathrm{x}}$. As we need to search every routable direction, we generate a stress gradient map for each direction from the stress map, as shown in Figure 4.2. To handle multiple routing layers, we generate stress and



(a) (b)

Figure 4.2: Stress gradient map of a benchmark circuit for each direction; (a) $+x$ direction, (b) $+y$ direction. $-x$ and $-y$ directional stress gradient maps are symmetric with these two, having same magnitude but opposite polarity.

stress gradient maps for each layer. The further from the device layer, the lower stress level we get.

4.2.3 Modeling Equivalent DC Current for AC Nets

Most of the signal nets in VLSI are AC nets with bi-directional current. In the past, AC nets were considered as invulnerable nets to EM, because the opposite direction of current can compensate EM to some degree. However, if a current imbalance exists between two directions of the current, EM cannot be entirely canceled out [43, 48]. Moreover, unlike power/ground nets, every segment of signal routing is critical to failure; even if a small part of the interconnect fails, the entire signal net fails. Hence in deep sub-micron technologies, designers have taken account of AC nets for EM-awareness [5,61]. In 3D ICs, AC nets can be more vulnerable due to TSV stress-driven migrating factors [54].

To analyze EM for AC nets, we convert AC current waveform into

equivalent DC current, similar to work in [11, 12, 48, 67]. As we are interested in the effect of TSV stress on EM, we consider average current, instead of root-mean-square (RMS) current for Joule heating. However the RMS current can be analyzed similarly.

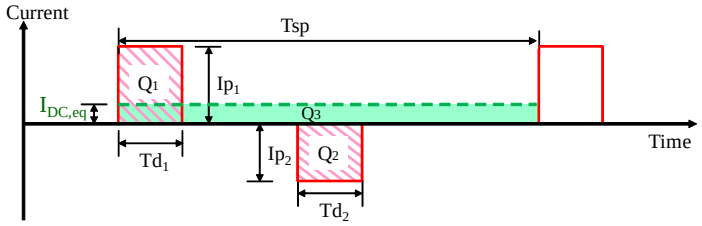


Figure 4.3: AC and its equivalent DC waveforms using charge model. Red solid line and green dotted line represent AC and equivalent DC current waveforms, respectively.

We model AC current waveform as a series of rectangular pulses as shown in Figure 4.3. In the figure, Td_1 and Td_2 stand for current pulse duration of positive and negative direction, respectively. Ip_1 and Ip_2 are peak current for positive and negative direction, Tsp is average switching period, $I_{DC,eq}$ is equivalent DC current value. We extend average current recovery (ACR) model [11] into charge form. Then, positive charge Q_1, negative charge Q_2 and charge for equivalent DC Q_3 for a single cycle can be expressed as,

$$\begin{aligned} Q_1 &= Td_1 \times |Ip_1| \\ Q_2 &= Td_2 \times |Ip_2| \\ Q_3 &= Tsp \times |I_{DC,eq}| = \begin{cases} Q_1 - c_h Q_2 & \text{if } Q_1 \geq Q_2 \\ Q_2 - c_h Q_1 & \text{otherwise.} \end{cases} \end{aligned} \tag{4.1}$$

Here c_h is the empirical healing coefficient of EM for the opposite direction of the current. If $c_h = 1$ and $Q_1 = Q_2$, the positive and negative charge can be

perfectly cancelled out and the equivalent DC current becomes zero. Because migrated atoms cannot perfectly fill the vacancy, c_h is slightly less than 1 in general [11]. To get the c_h value, we use FEA-based EM modeling using COMSOL Multiphysics. First, we measure MTTF by sweeping DC current value, and then measure MTTF with sample AC current waveforms. If the MTTF of AC is the same as that of certain DC, we can reasonably assume it as *equivalent DC* for EM. With the AC current waveform and equivalent DC value from FEA simulation, we get Q_1, Q_2 and Q_3 values, and we get $c_h = 0.95$ on average using Eqn. (4.1).

Next, we check the accuracy of the charge model in Eqn. (4.1). We generate 40 test AC waveforms with random Td_1, Td_2, Ip_1 and Ip_2. While we directly simulate MTTF with an FEA simulator and get an equivalent DC by comparing the MTTF value, we also calculate equivalent DC using Eqn. (4.1) with $c_h = 0.95$. The equivalent DC values from the two methods are shown in Figure 4.4. The average error rate between the two methods is 1.4% for 40 test cases. As the charge model is reasonably accurate, we convert the AC current into an equivalent DC current using the charge model in Eqn. (4.1) with $c_h = 0.95$ in our work.

To get the current profile of the benchmark circuits, we use Synopsys NanoSim. For AC nets, we get Ip_1, Ip_2, Td_1, Td_2 from NanoSim and convert it into an equivalent DC current with a charge model. This equivalent DC can be used as an input for EM library to estimate MTTF. For DC nets, we use the current value directly. As a result, we can evaluate EM reliability for both

AC and DC nets using the *EM library*.

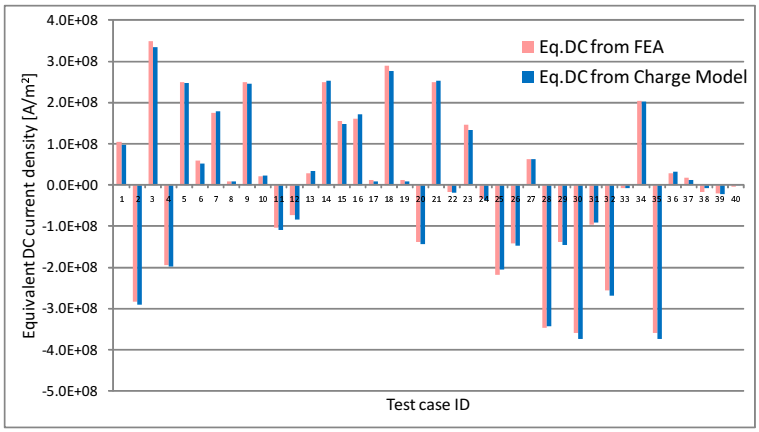


Figure 4.4: Comparison of equivalent DC between FEA simulation and charge model for 40 test cases. Wire dimension of M1 in 45nm technology is used to get *current density*.

4.2.4 Thermal Consideration

Temperature affects EM by changing diffusivity D in Eqn. (2.3) and through temperature gradient in Eqn. (2.2). Actual temperature in a circuit can fluctuate according to time, with the input vector patterns and switching activity. Although EM analysis with time-varying temperature has been shown in work [46], it would make EM analysis too complex to do during routing. Hence, we limit our scope to static EM and assume reasonable static thermal distribution. Figure 4.5 shows the thermal map we used for our experiments. The average temperature in this map is $353°K$ $(80°C)$, and the standard deviation is 23. During EM evaluation of each grid during routing, we ignore the effect of the temperature gradient in Eqn. (2.2) because the tem-

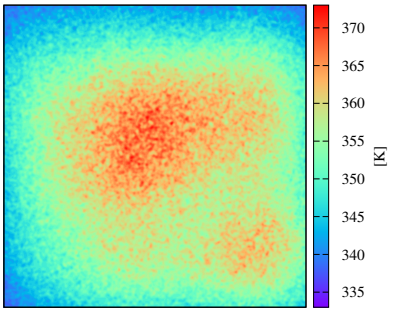


Figure 4.5: Thermal map used in our experiments.

perature difference between adjacent grids is negligible. Still we consider the static temperature effect of diffusivity term in Eqn. (2.3) and Eqn. (2.2). In general, a high temperature of interconnects results in a short MTTF because of higher diffusivity D, if all the other conditions are the same. For routing across multiple metal layers, we generate a temperature map for each layer. We assume the temperature in the lowest metal (M1) is the highest among routing layers, and is decreased by $2°C$ per routing layer.

4.3 EM-aware Routing for 3D ICs

As we discussed in Section 4.2.2, EM-robustness can depend on the relative orientation of TSVs and wires, and it makes the EM-aware routing problem in 3D ICs to be unique. Figure 4.6 illustrates an example of EM-aware routing of 3D ICs. For this example, let us consider a simple case where temperature and current do not vary on a routed path, and MTTF is a function of stress gradient only. As we discussed in Chapter 3, the normal directional current access *toward* a TSV is helpful to enhance MTTF at the

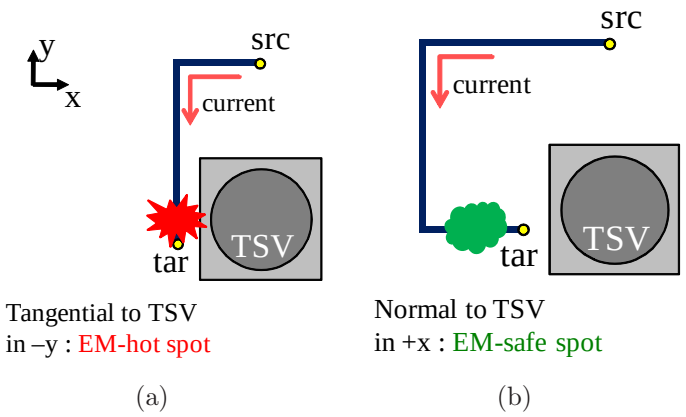


Figure 4.6: Example of an EM-aware routing based on stress gradient; (a) a routing without EM-awareness, (b) a routing with EM-awareness.

point near the TSV because of the increasing stress gradient, while tangential directional access near the TSV can degrade MTTF due to the decreasing stress gradient. Thus around the target pin location in Figure 4.6, (b) can be more robust to EM than (a). Note that (b) has more wire length to detour the EM-hot spot instead. From this example, we can see that a new routing methodology is needed to achieve EM-awareness for 3D ICs, considering for the directional property of EM. In our work, we calculate MTTF for every direction during EM-aware maze routing, with the stress gradient toward each routable direction at a certain point. By doing this, we consider the effects of the directional property of EM, as a form of *stress gradient* of each routable direction. Also, we consider the effect of current density and temperature on EM. In the following subsections, we will present the overall flow of EM-aware routing, and then explain the MTTF prediction during routing, net ordering and maze routing algorithms in detail.

4.3.1 Overall Flow

Figure 4.7 shows the overall flow of our EM-aware routing for 3D ICs. Initially, we need TSV placement information to calculate a TSV-induced stress profile, as described in Section 4.2.2, as well as a thermal profile of a circuit and current density of each net. To analyze EM of AC nets we use equivalent DC current density as explained in Section 4.2.3. Since our routing considers one net at a time, net ordering for routing can affect the final routing result. We order nets based on the expected MTTF of pre-routed nets and half-perimeter wire length (HPWL), presented in Section 4.3.3. And then during EM-aware maze routing, we predict the MTTF for each routable direction at the grid subject to search with the EM library, as depicted in Section 4.3.2. Once MTTF is predicted for every direction of the grid, EM cost is calculated during maze routing to find EM-safe paths, as explained in Section 4.3.4. Finally, EM-aware maze routing can be made based on the cost function. If a net is failed to be routed, a rip-up and reroute technique is used.

4.3.2 Lifetime Prediction with EM Library

To predict the MTTF of a grid effectively, we deploy the EM library that uses pre-simulated MTTF with varying stress gradients, current density and temperature as introduced in [54]. This EM library can work as a look-up table that helps in retrieving the expected MTTF of a certain grid toward a certain direction during routing, which enables us to make an immediate prediction of MTTF.

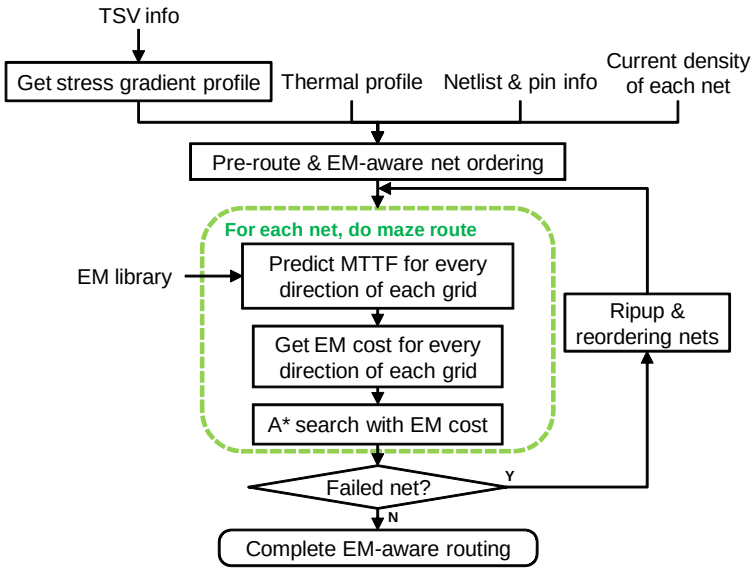


Figure 4.7: Overall flow of EM-aware routing for 3D ICs

As we explain in Section 4.2.2, 4.2.3 and 4.2.4, we already have a stress gradient for each direction in the xy-plane, $\{+x, -x, +y, -y\}$, as well as temperature and current information. Therefore, we can easily predict MTTF for these four directions with the EM library. To transit to the upper or lower metal layer, $+z$ or $-z$ direction, we consider various factors; depending on the metal layer, current density varies due to the different wire thickness and width, temperature and TSV-induced stress also change because the distance from the device layer is different. Current densities in different metal layers are calculated based on the 45nm technology rule by assuming minimum wire dimension. The stress profile of each metal layer is generated using the damping ratio from the FEA simulation result using ANSYS. We assume temperature decreases by $2°C$ per metal layer, as distance from the device layer increases.

Using stress profile, current density and temperature for each metal layer, we get the *expected MTTF* for both the $+z$ and $-z$ direction, similar to other directions in the xy-plane. As a result, we get six MTTF values around the grid, toward the $\{+x, -x, +y, -y, +z, -z\}$ direction. In general, upper metal layers tend to be more robust to EM due to the smaller level of TSV-induced stress, lower temperature and lower current density than the M1 metal layer.

4.3.3 EM-aware Net Ordering for Routing

Our routing makes routing of nets sequentially, thus net ordering can affect the final result. To achieve two competing goals during net ordering, which are minimization of wire length and improvement of EM-robustness, we use a heuristic *grade-based EM criticality consideration* method. In our approach, wire length is the first criteria for net ordering, and for wires with similar length, we consider the EM-criticality for the net ordering. To be more specific, we first sort nets with half-perimeter wire length (HPWL), in an increasing order as in [18] to prevent the unnecessary detour of short nets. Then, we group nets with HPWL and make nets in the same group have a similar HPWL. Once grouping finishes, the *first-grade group* has the smallest HPWL on average, and the last-grade group has the largest HPWL. Then we perform pre-routing to approximate MTTF of a route of each net. Pre-routing is maze routing with A* search without EM-awareness, and we measure MTTF of pre-routed paths to identify EM-critical nets using the method described in Section 4.3.2. After pre-route, from the first-grade group, the most EM-

Table 4.1: Example of EM-aware net ordering.

Net id	Pre-route result			Routing order
	HPWL	Grade	$MTTF_{net}$	
net1	49	1	$2.2e8$	2
net2	72	1	$4.2e8$	3
net3	87	1	$7.6e7$	1
net4	113	2	$8.3e7$	6
net5	148	2	$5.3e6$	4
net6	185	2	$9.4e6$	5

critical net with the shortest expected MTTF is routed first within a group. If a net has a short MTTF, it means that the net will have a high probability of EM-induced failure if we do not make an EM-aware routing. Therefore we put high priority in routing to the EM-critical nets among all the other nets within the same group. The rationale of *grade-based EM criticality consideration* is to limit the EM-criticality based net sorting within the group with similar wire length only, so that we can still take advantage of the *shorter net first* method overall.

Table 4.1 illustrates an example of our EM-aware net ordering. Let us assume that we have a two-level grade for HPWL in this example. Here, net1 through net3 are in the first-grade group, so they need to be routed earlier than the nets in the second-grade group. Among the three nets in the first-grade, because net3 has the shortest MTTF, our routing makes a route of net3 first, and then net1 and net2 are routed sequentially. After that, routing for the second-grade group is started, and net5, net6, net4 are routed sequentially based on their MTTF. If there is any case that the routing needs to do a rip-up

and reroute, we re-order the nets to put the failed net to the first priority.

4.3.4 Cost Function for EM-aware Maze Routing

EM cost is the key factor for EM-awareness during maze routing. We define EM cost at a grid g toward direction i as a ratio of threshold MTTF ($MTTF_{ref}$) and $MTTF(g, i)$ as Eqn. (4.2) [44]. Intuitively, for the EM-critical grid that has a shorter MTTF in a certain direction, the EM cost increases toward that direction.

$$r(g, i) = \frac{MTTF_{ref}}{MTTF(g, i)} \tag{4.2}$$

Next, we need to make a reliable cost function that can handle both EM-awareness as well as traditional routing constraints. We use a *negotiation-based A* search* for this problem.

A negotiation-based A* search is an idea to have robustness in routing by balancing the historical cost and currently congested cost, i.e., present cost [19, 44]. We adopt this method to our detailed maze routing. Instead of using historical cost h and present cost p for each iteration of an edge in a global router [19], we calculate and update h and p for each grid. In Eqn. (4.3), for a grid g toward direction i, $h(g)$, $p(g, i)$, $dist(g, tar)$ are historical cost, present cost, and distance between g and target pin, respectively. As a path is constructed, $h(g)$ becomes larger based on Eqn. (4.5), thus choosing the high present cost can be cheaper than choosing high historical cost. It means the history of a path - whether it passed EM hot spots or not - can affect

the construction of a path at a present grid. We note that the expected cost from the current grid to target, $dist(g, tar)$, affects the routing cost as well. Balancing between historical, present and expected cost is made by α and δ.

$$cost(g, i) = h(g) + \alpha \cdot p(g, i) + \delta \cdot dist(g, tar) \tag{4.3}$$

$$p(g, i) = dist(src, g) \cdot \left(1 + \frac{r(g, i)}{\beta}\right) \tag{4.4}$$

$$h(g) = \sum_{\forall (g,i) \in RP(g)} p(g, i) \tag{4.5}$$

Adding the EM cost effect to the present cost in Eqn. (4.4) is the key part of the cost function of EM-aware detailed maze routing. As we explained in Eqn. (4.2), $r(g, i)$ is the EM reliability cost to show the ratio of current MTTF and the reference MTTF. In Eqn. (4.4), $dist(src, g)$ is distance between a source and current grid g, and β is a parameter to balance between distance-based routing cost and EM cost. As β increases, the impact of EM cost on the total routing cost decreases.

The decision of α and δ is important to balance between historical, present and expected cost. Inspired by the work in [19], we pick α as a ratio between maximum historical cost and maximum present cost that a wire can have. From Eqn. (4.4) and Eqn. (4.5), the upper bound maximum historical

cost of a path is expressed as Eqn. (4.6),

$$h_{max} = \sum_{\forall g \in RP} p_{max} \tag{4.6a}$$

$$= \sum_{\forall g \in RP} \left\lceil dist(src, g) \cdot \left(1 + \frac{r_{max}}{\beta}\right) \right\rceil \tag{4.6b}$$

$$= K \cdot \sum_{\forall g \in RP} \lceil dist(src, g) \rceil \tag{4.6c}$$

$$= K \cdot \left\{ \frac{dist(src, tar) \cdot \{dist(src, tar) + 1\}}{2} \right\} \tag{4.6d}$$

where

$$K = 1 + \frac{r_{max}}{\beta}. \tag{4.6e}$$

Similarly, the upper bound of maximum present cost of a path can be shown as Eqn. (4.7).

$$p_{max} = \left\lceil dist(src, g) \cdot \left(1 + \frac{r_{max}}{\beta}\right) \right\rceil = K \cdot dist(src, tar) \tag{4.7}$$

With Eqn. (4.6) and Eqn. (4.7), we pick α as Eqn. (4.8). It guarantees balancing between the worst historical cost and the worst present cost. Since α is a function of distance between a source and a target, it should be calculated for each wire. We use HPWL for $dist(src, tar)$ of each net.

$$\alpha = \frac{h_{max}}{p_{max}} = \frac{dist(src, tar) + 1}{2} \tag{4.8}$$

For δ in Eqn. (4.3), we use dynamic adjustment according to the wire length. While finding EM-safe routes, we also want to have a reasonably short wire length. To prevent *over-avoiding* EM-hot spots which spend an extremely long

wire length, we assign a penalty to a longer wire than a pre-routed wire length, L_{ref}. We note that pre-routing is done without EM-awareness, thus it can provide a good reference for the wire length of each net. During routing with EM-awareness, once the wire length grows longer than the L_{ref}, we increase δ exponentially. In this way, as the wire length becomes longer than the L_{ref}, the weight of the expected cost becomes larger, and the driving force toward the target pin becomes larger. Eqn. (4.9) shows the dynamic adjustment of δ according to the current wire length, L_{cur}. To have the same impact of present cost and expected cost to the total routing cost, we pick δ_o as the same as α in this work.

$$\delta(L_{cur}) = \begin{cases} \delta_o & \text{if } L_{cur} \leq L_{ref} \\ \delta_o \cdot \eta^{\frac{L_{cur}-L_{ref}}{L_{ref}}} & \text{if } L_{cur} > L_{ref} \end{cases} \tag{4.9}$$

4.3.5 Routing Algorithm

Algorithm 1 describes our method to route a net with EM-awareness, which is briefly presented in a green dotted box of Figure 4.7. For a grid subject to search during maze routing, we predict the MTTF for each direction as depicted in Section 4.3.2, and calculate EM cost and total cost as explained in Section 4.3.4. Using total cost, an A*-based maze routing is made. The inputs of this algorithm are current density of a net J_n, source pin src, target pin tar, EM library, thermal and stress gradient profile.

Start from *src*, do A* search of neighbor grids
for *each grid subject to search* $g = (x_g, y_g, z_g)$ **do**
  PredictMTTF(x_g, y_g, z_g, J_n);
  for *each direction* $i \in$ {*xinc, yinc, zinc, xdec, ydec, zdec*} **do**
    $r(g, i)$=Calculate-EM-Cost(MTTF(g, i)));
    $cost(g, i)$=Calculate-Total-Cost;
  end
end
Continue maze routing until arriving to *tar*

Algorithm 1: EM-aware maze routing of a net

4.4 Experimental Results

We implemented our proposed algorithm with C++, and performed experiments on 2.93GHz Intel Quad Core Linux Machine. Benchmark circuits described in Table 4.2 are the ones by [34]. In Table 4.2, the first three rows are three stacked dies in the same circuit *uP*, one of the industrial microprocessors. The next three rows in the table show another industrial circuit *IDCT*, which performs inverse discrete cosine transformations. We use part of the circuits instead of the whole circuits. Originally each system had four stacked dies after 3D placement from work [34], but we did not use the bottommost dies because they do not include any TSVs which can differentiate EM in 3D and 2D ICs. The TSV cell size is $4um \times 4um$ for all cases. We use 20 grades for the *grade-based EM criticality consideration* approach for the net ordering.

To get the current waveform and its equivalent DC, we use gate-level information of benchmarks. For generating stress data from the TSV, we use placement information of benchmarks generated by [34]. We regard *EM-*

Table 4.2: Benchmark circuits.

	Size[um^2]	#Metal	#Nets	#Pins	#TSVs
uP Die0	10000	6 layers	803	1831	33
uP Die1	10000	6 layers	882	2125	42
uP Die2	10000	6 layers	627	1545	50
IDCT Die0	10000	6 layers	579	1383	39
IDCT Die1	10000	6 layers	814	2152	61
IDCT Die2	10000	6 layers	663	1694	58

violation as the interconnect failure earlier than $MTTF_{ref}$, which is $1e8$ seconds (9.5 years) in this chapter. Here we define *failure* as 5% deviation of atomic concentration [31, 53], and define *EM-violated wire* as a wire which has at least a single *EM-violated grid*. We assume a routing grid is the same as a grain structure of the wire, thus each grid can be the unit of EM analysis. We use η as 25 for Eqn. (4.9) in our experiments.

We can change the weight of EM cost by tuning β, as we discussed in Eqn. (4.4). With increased β, the weight of EM cost in the entire cost decreases, and routing becomes *less EM-aware*. In Table 4.3, we show the trade-off between EM-awareness and routing resources with different β values, for *uP Die1*. As we change β from 100 to 10000, the percentage of EM-improvement gets smaller, but we have a smaller wire length and via overhead instead. In case of β being 100, wire length overhead and via overhead are larger than the other cases because our algorithm tries to choose EM-safe paths more aggressively. By tuning β, we can balance between MTTF and routing overheads, and can achieve improved EM-robustness within certain routing constraints. For the rest of experimental results, we use β as 1000.

Table 4.3: Trade-offs between EM-awareness and wire length, local via in *uP Die1*. WL-driven, EMAR, % represent wire length-driven routing (baseline), EM-aware routing, and difference divided by the baseline in percentage, respectively.

	#EM-violated wires			#EM-violated grids			Wire length[1]			#Local via		
	WL-driven	EMAR	%	WL-driven	EMAR	%	WL-driven	EMAR	%	WL-driven	EMAR	%
$\beta = 100$	176	59	-66.5%	3729	243	-93.5%	68689	69490	1.17%	1063	1276	20.0%
$\beta = 1000$	176	89	-49.4%	3729	1040	-72.1%	68689	68996	0.45%	1063	1146	7.81%
$\beta = 10000$	176	96	-45.5%	3729	1503	-59.7%	68689	68856	0.24%	1063	1108	4.23%

Table 4.4 shows the experimental results of our EM-aware routing, with comparison of wire length (WL)-driven routing. First, we investigate a number of EM-violated wires at a threshold time, in the first column of the Table 4.4. The definition of an *EM-violated wire* is a wire which has at least an EM-violated grid. All the benchmark circuits show a decreased number of EM-violated wires at the $MTTF_{ref}$, -36.3% on average with our EM-aware routing. Figure 4.8 shows the cumulative distribution function (CDF) of EM-violated wires according to time for one of our benchmarks, *uP Die1*. In this graph, the y-axis represents the number of EM-violated wires at a certain time divided by the total number of wires, and the x-axis is time in seconds. We can see that the MTTF is significantly improved with our EM-aware routing, compared to wire length-driven one. Figure 4.9 shows a zoom-in shot of Figure 4.8, to examine the lower MTTF region.

Next, we study a number of *EM-violated grids* along routed paths at $MTTF_{ref}$ as shown in the second column in Table 4.4. The number of EM-violated grids decreases substantially with our EM-aware routing, -66.4% on average. The effect of constructing EM-safe paths and increasing MTTF of each grid in the routed path is displayed more clearly at the CDF graph for *uP Die1* in Figure 4.10. A red line represents the baseline results of a cumulative number of EM-violated grids normalized by total number of routed grids, and a blue line represents that of EM-aware routing. We can see that the normalized number of EM-violated grids is much lower with our EM-aware routing. We

[1]One local via is counted as three grids. Wire length unit is [0.1um].

Table 4.4: Experimental results of EM-aware routing compared with wire length (WL)-driven routing. WL-driven, EMAR, % represent wire length-driven routing (baseline), EM-aware routing, and difference divided by the baseline in percentage, respectively.

	#EM-violated wires			#EM-violated grids			Wire length[1]			#Local via			Run time[s]	
	WL-driven	EMAR	%	WL-driven	EMAR	%	WL-driven	EMAR	%	WL-driven	EMAR	%	WL-driven	EMAR
uP Die0	55	37	-32.7%	1167	486	-58.4%	39602	39647	0.11%	614	642	4.56%	484	525
uP Die1	176	89	-49.4%	3729	1040	-72.1%	68689	68996	0.45%	1063	1146	7.81%	1909	1888
uP Die2	146	112	-23.3%	3135	1424	-54.6%	43613	43740	0.29%	736	770	4.62%	1209	855
IDCT Die0	91	62	-31.9%	2452	943	-61.5%	39182	39260	0.20%	477	474	-0.63%	863	1014
IDCT Die1	184	114	-38.0%	4780	1220	-74.5%	79521	79793	0.34%	1216	1285	5.67%	2645	2725
IDCT Die2	183	118	-35.5%	4469	1523	-65.9%	65225	65382	0.24%	970	1014	4.54%	1898	2042
Total	835	532	-36.3%	19732	6636	-66.4%	335832	336818	0.29%	5076	5331	5.02%	9007	9049

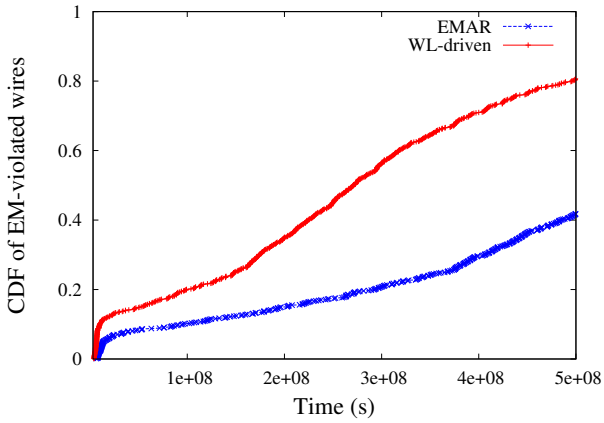


Figure 4.8: CDF of EM-violated wires according to the time in *uP Die1*. Our EM-aware routing has a significantly lower number of EM-violated wires than a wire length-driven one.

note that by calibrating $MTTF_{ref}$ at the cost function in Section 4.3.4, we can adjust the threshold MTTF that we are interested in. The third and the fourth column in Table 4.4 show wire length and number of local vias of routed paths, respectively. For wire length, we count one local via as three grid units. There are overheads of wire length, 0.29% on average, and number of local vias, 5.02% on average, still these overheads are reasonably acceptable.

The TSV-induced stress level decreases as the distance from TSV increases. Thus simply having a larger routing keep out zone (KOZ) from TSVs can be helpful for EM-robustness [54]. However as we observed in the earlier sections, TSV-induced stress is not always something to avoid; it can either mitigate or aggravate EM depending on the stress gradient. Hence our routing does not just avoid near the TSV region, rather it chooses more EM-safe routes than the one without TSV. Thus, we actively take advantage of the *directional*

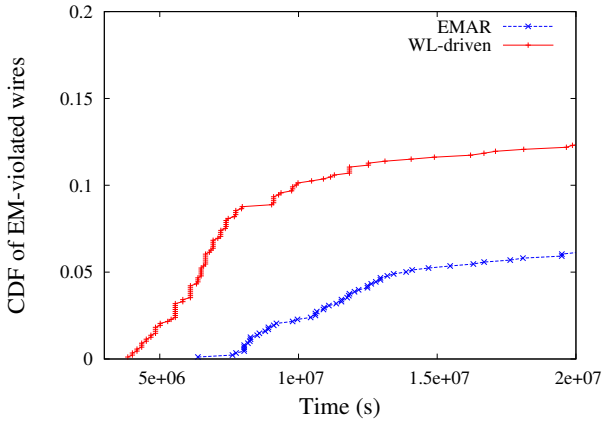


Figure 4.9: Zoom-in shot of Figure 4.8. Our EM-aware routing has a much lower number of EM-violated wires than the wire length-driven one.

property of EM in 3D ICs and improve MTTF even further around the TSV region. We compare our EM-aware routing result and WL-driven one with larger KOZ sizes in Table 4.5. Compared with WL-driven routing with $0.1um$ KOZ, $1um$ and $0.7um$ KOZ show only a slightly lower number of EM-violated wires. On the other hand, our EM-aware routing reduces it significantly even with $0.1um$ KOZ. In terms of EM-violated grids, $1um$ and $0.7um$ KOZ cases help to have lower number of EM-violated grids than the one with $0.1um$ KOZ, for example having 15249 and 17282 total grids respectively instead of 19732. However our EM-aware routing is superior to a large KOZ scheme, having only 6636 total EM-violated grids. We note that a smaller KOZ means better routability. As a result, our EM-aware routing can have significantly better EM-awareness with better utilization of routing resources than a simple routing blockage scheme. The experiments in Table 4.4 are performed with

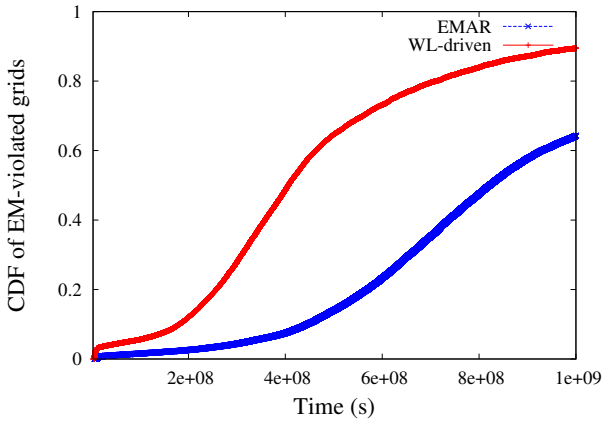


Figure 4.10: CDF of EM-violated grids according to the time in *uP Die1*. Normalized EM-violated grids are substantially lower with proposed EM-aware routing.

$0.1um$ KOZ for both EM-aware routing and WL-driven routing.

4.5 Summary

In this chapter, we model EM for both AC and DC signal nets under TSV-induced stress, temperature, and current density consideration. AC signals are converted into *equivalent DC* and then analyzed for EM criticality. We effectively predict MTTF of a grid toward any routable direction across multiple routing layers, with consideration of the stress gradient from TSV, temperature and current density of nets. Based on our EM modeling, we propose an effective EM-aware routing algorithm that performs net ordering with grade-based EM criticality consideration, which gives high priority to EM-critical nets while achieving the advantage of the shorter net first method.

Table 4.5: Comparison of EM-aware routing (EMAR) and WL-driven routing with various routing keep out zones (KOZ). $1um$, $0.7um$ and $0.1um$ represent routing KOZ from TSV. EMAR shows superior EM-robustness compared to WL-driven routing with a larger KOZ.

	#EM-violated wires				#EM-violated grids				Wire length[1]				#Local via			
	WL-driven			EMAR	WL-driven			EMAR	WL-driven			EMAR	WL-driven			EMAR
	$1um$	$0.7um$	$0.1um$	$0.1um$	$1um$	$0.7um$	$0.1um$	$0.1um$	$1um$	$0.7um$	$0.1um$	$0.1um$	$1um$	$0.7um$	$0.1um$	$0.1um$
uP Die0	54	56	55	37	892	1066	1167	486	39619	39604	39602	39647	620	614	614	642
uP Die1	174	177	176	89	3117	3524	3729	1040	68757	68721	68689	68996	1075	1063	1063	1146
uP Die2	145	145	146	112	2455	2760	3135	1424	43608	43626	43613	43740	736	739	736	770
IDCT Die0	87	91	91	62	1937	2167	2452	943	39141	39165	39182	39260	468	481	477	474
IDCT Die1	174	185	184	114	3222	3871	4780	1220	79581	79517	79521	79793	1224	1207	1216	1285
IDCT Die2	180	179	183	118	3626	3894	4469	1523	65230	65200	65225	65382	959	953	970	1014
Total	814	833	835	532	15249	17282	19732	6636	335936	335833	335832	336818	5082	5057	5076	5331

A 3D EM-aware maze routing procedure is also proposed with effective cost function using predicted MTTF, and we present techniques to balance between EM-awareness and wire length during routing. Experimental results show that our EM-aware routing algorithm improves EM-reliability, having a 66.4% lower number of EM-violated grids with little sacrifice of conventional routing objectives.

Chapter 5

Electromigration Study with Multi-scale Power/Ground Via Structures

5.1 Introduction

For Electromigration (EM), local vias in between metal layers of IC have been regarded as EM-prone structures, and have been actively studied [28, 38, 39]. Meanwhile, EM for through-silicon-vias (TSVs) in 3D IC technology has drawn lots of attention as well, both for modeling [23, 25, 53, 62, 65] and measurement [20, 25, 26].

In a 3D power distribution network (PDN), local vias often bridge power and ground TSVs, particularly with a via-first/middle approach. Jung et al. [32] showed that an array of stacked local vias can exist on top of the TSV landing pad for a 3D PDN as appears in Figure 5.1. Because this *multi-scale via* (MSV) including a TSV and array of local vias is essential to 3D PDN system, EM issues of MSV needs to be fully studied for reliable 3D ICs. Nonetheless, there has been little effort to study the EM issue of the MSV structure in 3D PDN. Frank et al. [26] showed measured data of EM failure in via-first/middle TSV samples, but they used extended M_1 wires to connect the local vias with the landing pad rather than directly placing the local vias

on top of the TSV landing pad, which can cause a higher IR-drop for PDN. Choi et al. [20] showed that EM can occur at the MSV structure, but did not analyze EM failure time as a combined effect of EM of local via and TSV. To the best of our knowledge, there has been no work to model EM of MSV considering both EM in local vias and that in TSV.

In this chapter, we study EM robustness of 3D PDN with the MSV structure that includes via-first/middle TSV and stacked local vias. Overall, our contributions are summarized as follows:

- We propose an efficient EM modeling flow for multi-scale vias (MSVs) in 3D PDNs.
- We investigate the impact of material property, number and size of local vias, and initial void condition on EM-induced failure time of the MSV structure.
- We study the interplay between the EM of local vias and EM of TSV, and analyze its impact on the EM of the MSV structure.
- We suggest a full-chip level EM simulation flow of 3D PDNs with MSVs, and investigate the impact of initial void condition, temperature and current density on the IR-drop of full-chip level 3D PDNs.

5.2 Preliminaries

5.2.1 Structure of 3D Power Distribution Network

Figure 5.1 presents the power distribution network (PDN) of 3D ICs with via-first/middle TSVs [32]. Unlike via-last TSVs which go through all the metal layers, via-first/middle TSVs do not penetrate metal layers. Therefore, a TSV can have one landing pad on the global metal layer (M_{10}) and the other landing pad on the local metal layer (M_1) as shown in the Figure 5.1. Since the power/ground meshes can be located in the global (M_7-M_{10}) and intermediate metal layers (M_4-M_6), the M1 landing pads need stacked local vias to reach power meshes on the upper metal layers. To reduce the IR-drop and improve EM reliability, stacked local vias can be as many as possible. On the other hand, stacked local vias can be routing blockages, thus it is necessary to determine the proper number of local vias on each landing pad.

We define a *multi-scale via*, or *MSV*, as a structure composed of multiple local vias and a TSV. In an MSV, local vias are connected to a TSV landing pad in one of the BEOL layers, as shown in Figure 5.3. On M_1 landing pad of a via-first/middle TSV, an array of local vias (V_1) is directly connected. MSV structures frequently appear in 3D PDN because local vias directly bridging power mesh and TSVs can achieve minimal IR-drop, especially with via-first and via-middle TSVs. With via-last TSVs, on the contrary, MSVs are unnecessary because TSV landing pads abut power mesh on the top metal. In this work, we limit our scope to 3D PDN with MSV structures.

5.2.2 Basics of EM of Multi-scale Via (MSV)

Electromigration (EM) is a wear-out failure mechanism for metal interconnects [39]. EM failures are often caused by the interconnect voiding from metal atomic diffusion. This diffusion is driven by the strong flow of electrons, and the strength of electron flow, denoted as current density, is intensified as feature size shrinks, thereby aggravating the EM problem [39]. The vacancy flux due to EM can be expressed with multiple driving forces such as current density, stress gradient and vacancy concentration, as shown by Eqn. (5.1) [57].

$$\vec{J_v} = -D_v \left(\nabla C_v - C_v \frac{eZ^*}{kT} \rho \vec{j} + C_v \frac{f\Omega}{kT} \nabla \sigma \right), \tag{5.1}$$

Here, J_v is vacancy flux, D_v is effective vacancy diffusivity, C_v is vacancy concentration, ρ is electrical resistivity of the material, $\vec{j}$ is current density, e is electron charge, f is vacancy relaxation ratio, Ω is atomic volume, σ is hydrostatic stress, k and T are Boltzmann constant and absolute temperature, respectively. The effective vacancy diffusivity D_v is expressed by Arrhenius equation [57],

$$D_v = D_o \cdot exp(\frac{-Ea}{kT}) \tag{5.2}$$

where Ea is activation energy and D_o is initial diffusivity.

On the right side of Eqn. (5.1), the second term is the most dominant one that is affected by the current density $\vec{j}$, while the other two factors are of secondary importance. Usually the first term can be assumed to be negligible [23]. Moreover, if current density and wire length jL is larger than critical

Blech product $(jL)_c$ (which is usually true in PDN mesh), we can safely neglect the third stress effect term [14]. Thus, vacancy flux can be simplified as

$$\vec{J_v} = D_v C_v \frac{eZ^*}{kT} \rho \vec{j}. \tag{5.3}$$

Eqn. (5.3) will be used for our EM model to simulate void growth in Section 5.3.

Within dual-damascene copper interconnects, wire-via interface is the most EM-critical spot [39]. Depending on the current direction, there are two distinctive categories of EM failure [38]; 1) downstream EM (i.e. *line depletion*) and 2) upstream EM (i.e. *via depletion*). With downstream EM, electrons flow from via top to bottom (current flows from bottom to top), and voids are generated beneath the barrier, at the interface of via trench and the lower metal wire [28, 38]. An example of voids from downstream EM is shown in Figure 5.3. On the other hand, with upstream EM, electrons and migrated atoms flow from the bottom to the top of a via, and voids appear inside the via trench [28, 38].

Previous studies showed that via-wire interface indeed is a site where EM-induced voids appear frequently [26, 56], as shown in Figure 5.2. With downstream EM, both local vias and TSV can have voids under the via structure, right under the barrier structure. Figure 5.3 illustrates the downstream EM of the MSV structure, with voids under the local vias as well as the TSV. Although our algorithm can be utilized to analyze both upstream and downstream EM, in this work, we focus on downstream EM for the MSV structure.

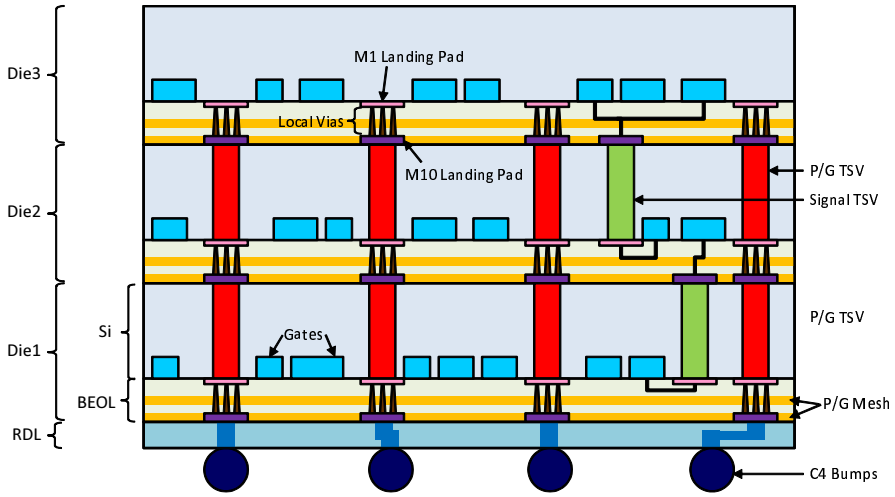
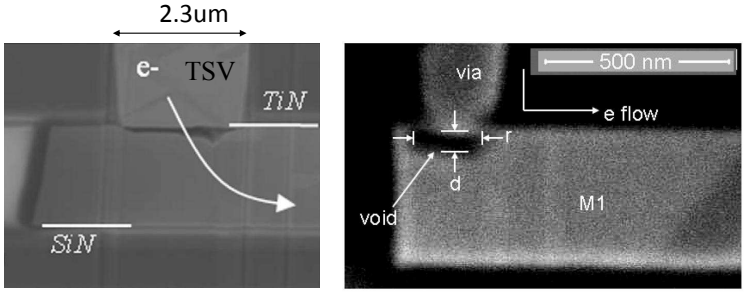


Figure 5.1: Power distribution network of 3D ICs with via-first/middle TSVs [32]. Three dies are stacked with face-down, and power/ground TSVs are vertically connected with stacked local via arrays [32].



(a) (b)

Figure 5.2: Void from downstream EM by Focus Ion beam-Scanning Electron Microscopy (FIB-SEM); (a) a void under the TSV [26], (b) a void under local via (V_1) [56].

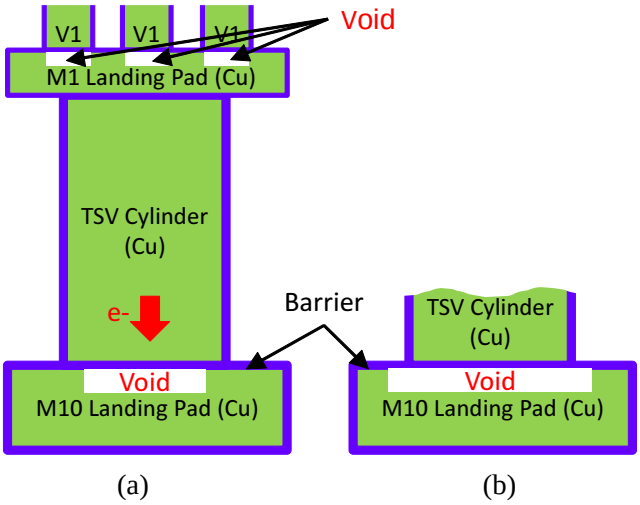


Figure 5.3: MSV structure and voids from downstream EM. EM-induced voids are located under the bottom barrier of each TSV and local via. (a) a TSV void smaller than a TSV cylinder, (b) a larger TSV void.

For the failure criterion, we use a 10% resistance increase from the initial resistance value of the MSV structure. Previous EM work used either percentage resistance increase (e.g. 10%) [23, 25] or a fixed amount resistance increase (e.g. 10Ω) as their failure criteria [24]. We use percentage resistance increase because it provides a more comparable failure time for vias with different initial resistance. Although a 10% increase of resistance of structure may not lead to a shut-down of the entire power/ground network, it means that the EM problem has already been initiated and EM-induced problem of the PDN, such as an IR-drop increase, can be expected at this point.

EM is generally explained as a two-phase process, void nucleation followed by void growth. However for deep sub-micron copper interconnects, it

is reasonable to assume a very short void nucleation time because it is nearly impossible to have void-free adhesion between copper and barrier/liner material [28]. Thus entire failure time can be largely dominated by void growth rather than void nucleation.

5.3 Modeling of Electromigration for Multi-scale Vias in 3D PDN

This section discusses our modeling algorithm for the EM-related lifetime of multi-scale vias (MSVs) in 3D PDN. We present our EM modeling algorithm summarized in Figure 5.4. This algorithm uses discrete time with small time step, and calculates the degree of void growth under a via using a function named *Calculate Void Growth* (Section 5.3.1). Once we get the vector of void radius for each TSV and local vias, we calculate the resistance of the entire MSV structure using the function *Calculate Resistance* (Section 5.3.2). Since the failure criterion is a 10% increase of resistance from the initial resistance, as we explained in Section 5.2, we check the resulting resistance to see whether it exceeds our failure criterion at each time step. Once it is over the failure criterion, our algorithm reports current time step as the *failure time*. Otherwise, we re-calculate current density of each via, and repeat the cycle.

5.3.1 Calculating Void Growth

The *Calculate Void Growth* function accepts its input as current time step, void size and current density of each via from previous time. The output

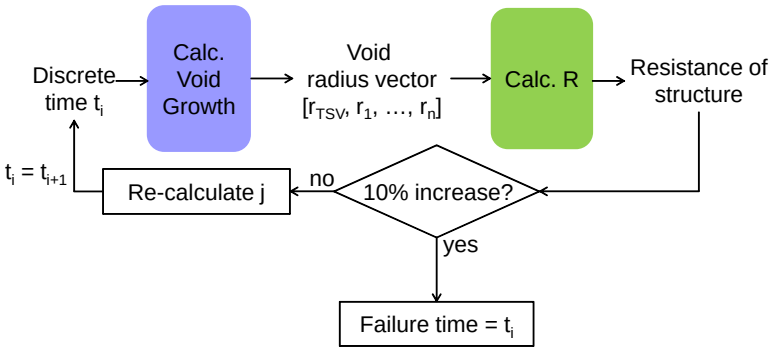


Figure 5.4: Flowchart of proposed EM modeling algorithm.

of this function, void radius vector, contains radius of a cylindrical void under the barrier of the MSV structure as shown in Figure 5.3. For example, if an MSV contains four V_1 local vias, void radius vector becomes $[r_{TSV}, r_1, r_2, r_3, r_4]$, where r_{TSV} and r_i represent void radius of TSV and i^{th} V_1, respectively.

For void growth beneath the TSV barrier, previous work [23, 25] used cylindrical void models. Because slit-like voids under the via tend to grow in a radial direction, we can assume that cylindrical voids have fixed thickness and grow toward a radial direction only, which is similar to other works [23, 25].

For void location, we assumed the worst case, the case when the initial void is located at the center of a via, similarly to previous work [23, 25]. This case is the worst in terms of EM reliability because the void blocks the entire via area in the shortest time.

According to work in [23, 25], void growth can be expressed by the rate of vacancies captured by a void. Void volume formed by infinitesimal time dt

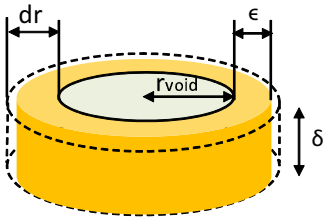


Figure 5.5: Cylindrical void under the via. r_{void} is current void radius, dr is infinitesimal void radius growing during time dt, ϵ is effective radius that governs effective cross area A for absorbing vacancies.

can be expressed as the following:

$$dV = \alpha f \Omega A J_v dt \tag{5.4}$$

where α is the ratio of vacancies captured by the void, A is area under flux effect, and J_v is the vacancy flux [23]. In Eqn. (5.3), de Orio et al. [23] assumed a constant area, A, no matter how big the void radius is. However, the area under the vacancy flux that contributes to void growth should change as void size grows. Because we assume the cylindrical void grows just in radial direction, only the area around the circumference of a void should be responsible for absorbing vacancies, since that is the *front line of void growth*. Figure 5.5 shows our concept of cylindrical void growth. Unlike previous work [23], we put *vacancy absorbing area* A in Eqn. (5.4) as follows,

$$A = 2\pi r_{void} \epsilon. \tag{5.5}$$

Thus, vacancy absorbing area A becomes a function of void radius r_{void}.

dV at Eqn. (5.4) should be equal to the infinitesimal void volume rep-

Table 5.1: Parameter values for EM modeling of MSVs.

Parameter	Description	Value
r_{TSV}	TSV Cu radius	$1.15um$ [25]
l_{TSV}	TSV height	$15.0um$ [25]
$tb_{TSV,side}$	TSV TaN thickness, side	$25.0nm$ [25]
$tb_{TSV,bot}$	TSV TaN thickness, bottom	$45.0nm$ [25]
δ_{TSV}	TSV void thickness	$5.0nm$
LP_{TSV}	TSV landing pad size	$3.6um \times 3.6um$
$t_{LP,M1}$	TSV M_1 landing pad thickness	$0.13um$ [49]
$t_{LP,M10}$	TSV M_{10} landing pad thickness	$2.0um$ [49]
$r_{V1,total}$	V_1 total radius	$32.5nm$ [49]
l_{V1}	V_1 height	$120.0nm$ [49]
$tb_{V1,bot}$	V_1 TaN thickness	$5.0nm$
$r_{V1,Cu}$	V_1 Cu radius	$27.5nm$
δ_{V1}	V_1 void thickness	$1.0nm$
T	Temperature	$453K = 180\ ^\circ C$
ρ_{Cu}	Cu resistivity	$2.73 \times 10^{-8}\Omega m$ at $180\ ^\circ C$
ρ_{TaN}	Barrier (TaN) resistivity	$3.0 \times 10^{-6}\Omega m$ at $180\ ^\circ C$
k	Boltzmann const.	1.38×10^{-23}
α	Ratio of captured vacancies	1.0 [23]
f	Ratio of vacancy volume	0.4 [57]
Ω	Atomic volume	1.182×10^{-29} [57]
D_o	Initial diffusivity	0.0047
Ea	Activation Energy	$0.9eV = 1.44 \times 10^{-19}V$ [25]
Z^*	Effective charge const.	1.0 [23]
e	Electron charge	$1.6 \times 10^{-19}C$
j_o	Initial current density of TSV	$2.5 \times 10^{10}A/m^2$ [25]

resented with a dotted line in Figure 5.5, then it can be expressed as

$$dV = \alpha f \Omega A J_v dt = 2\pi \delta r_{void} dr, \tag{5.6}$$

and thus

$$dr = \frac{\alpha f \Omega A J_v dt}{2\pi \delta r_{void}}, \tag{5.7}$$

where J_v and A are given by Eqn. (5.3) and Eqn. (5.5), respectively. All the parameters we use are presented in Table 5.1.

Unlike other work [23, 25], we re-calculate current density of each via

for each time step to get feedback from the grown voids.

5.3.2 Calculating Resistance of Multi-scale Via

Next step of our EM modeling algorithm is to calculate resistance of the MSV, given the void sizes from the previous step. Here we suggest an *LUT–based resistance network* model for the MSV. Our approach contains two steps. First we build look-up tables (LUTs) with a finite element analysis (FEA) tool to derive resistance of TSV and local via with voids, and then we use the resistance network to calculate the total resistance of MSV. We use two different sets of LUTs for TSV and local via, and then utilize them for the resistance network. The advantages of our LUT-based resistance network approach are: 1) easy extension to various conditions such as a different number of vias, because we use accurate FEA results and superpose them for entire resistance 2) fast and accurate results, because LUTs can enable fast reference and interpolation from simulation results. Use of LUTs provides several orders of magnitude faster access to simulation results than doing simulation with FEA for every input void size. Accuracy loss with LUT is limited because the range of input void size is mostly confined to the size of a via and resistance can be assumed to be a continuous function of the void size. To derive resistance of a MSV with certain void size, we use an industrial FEA tool, COMSOL Multiphysics. Figure 5.6 shows an example of void radius and resistance of a TSV and a local via (V_1) from the FEA simulation. All the other parameters are from Table 5.1.

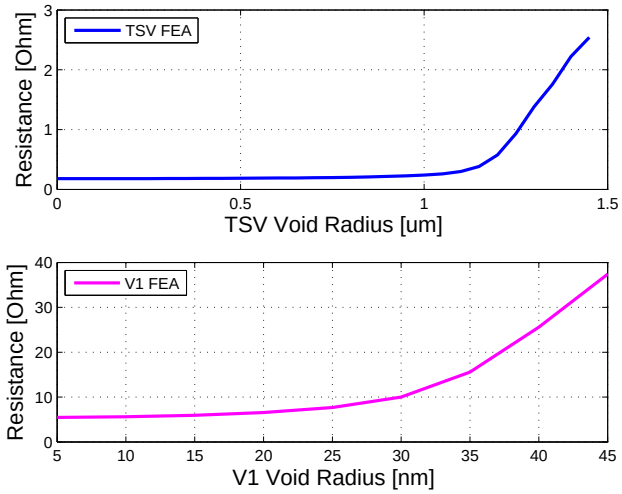


Figure 5.6: Relationship between void radius and resistance, for the TSV (top) and for the V_1 (bottom) from FEA simulation. We use TSV radius as 1.15um, and V_1 radius as 27.5nm, thus a void larger than via radius increases the resistance dramatically.

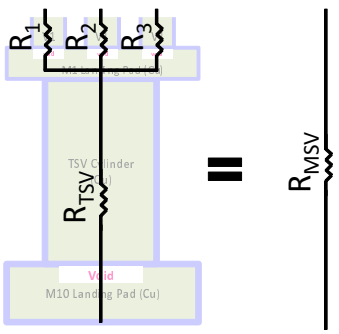


Figure 5.7: Resistance network of the TSV and the local via array. Since local vias are connected to the same TSV landing pad, they can be represented as a parallel resistance network.

To derive resistance of the whole structure, we construct a simple resistance network as illustrated in Figure 5.7. Since local vias are on the same TSV landing pad, they can be represented as parallel resistance network.

With resistance values of vias retrieved from LUTs, we can now calculate the resistance of the entire MSV structure. For resistance values derived by referring to LUTs (R_i for a local via, and R_{TSV} for TSV), total resistance of the MSV (R_{MSV}) with a single TSV and n local vias is as follows:

$$R_{MSV} = \frac{\prod_{i=1}^{n} R_i}{\sum_{i=1}^{n} R_i} + R_{TSV} \ , i \in [1, n] \tag{5.8}$$

Note that this method can calculate the resistance of the entire structure well regardless of void size distribution among vias. For instance, our algorithm can even be applied to an extreme case where some vias do not have any void at all while others have large voids.

5.3.3 Evaluation of Our Model

We evaluate our modeling method by benchmarking its results against previous measurements of EM-induced failure time for TSV [25] and local via [24]. To the best of our knowledge, no such measurement study has been done for the entire MSV structure that we can compare our result to. However, we can expect that our modeling approach can provide a reasonable estimate of failure time for the entire structure if the modeled failure time of individual components (i.e. TSV and the local via) corresponds with the measured time.

For the comparison of TSV modeling, we apply the parameters used for modeling that are the same as the experimental condition in [25]: temperature as $300°C$, current density as $2.5\text{MA}/cm^2$, TSV shape as square of $2.3um \times 2.3um$. Since the work in [25] extracts *effective barrier resistivity* values from their measurement samples, we use their extracted barrier resistivity values to give variation of failure time, similarly to a previous modeling work [23]. Other parameters are as shown in Table 5.1. Figure 5.8 shows EM-induced failure time distributions from measured data and from our modeling. Although our modeling deviates from the measurement results at both extremes, the modeled results around the median corresponds well with the measured data.

Similar to TSV, we compare our modeled failure time of local vias to the measured data [24]. We use the same physical structure as the measurement: we use an additional local via and an M_1 wire, set temperature as $295°C$, set failure criterion as a 10Ω increase from the initial resistance. We model failure time with the same current density they use, $2.50\text{MA}/cm^2$. Other parameters

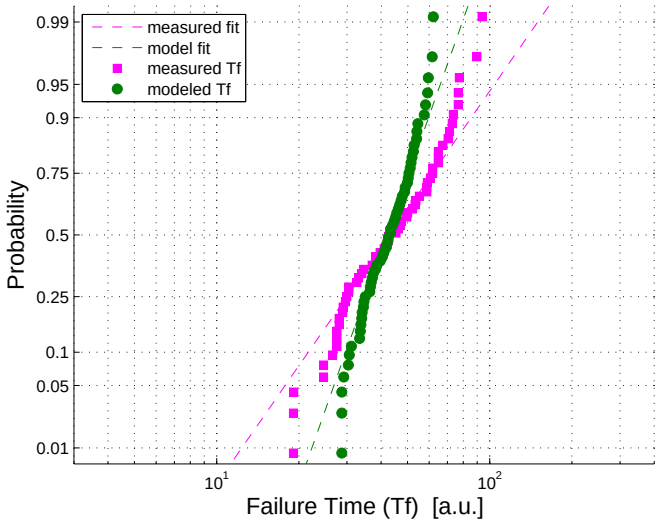


Figure 5.8: Comparison of modeled EM-induced failure time against measured data [25] on a log-normal probability plot.

Table 5.2: Comparison of modeled failure time and the median of measured data [24], when $j = 2.50\text{MA}/cm^2$.

	Ours	Measured [24]
t_{50} [hr]	89.0	90.5

for the EM model remain same as in Table 5.1. Table 5.2 shows a comparison of our modeling results against a median failure time t_{50} of measurement [24]. The failure time values closely follow the modeled data.

Together with the TSV comparison result, this result suggests that our model is effective in estimating EM-induced failure time with various types of vias, thus it could provide reasonable estimation with MSV structure. For the rest of this chapter, we will use this model to evaluate EM induced failure

time, with parameters shown in Table 5.1, unless specified otherwise.

5.4 Study on EM of Multi-scale Vias with Various Factors

This section explores several factors that affect EM-induced failure time. One factor of our interest is the material property, more specifically barrier resistivity. We also discuss other structural factors, such as the number of local vias on a TSV, and the size of a local via that is subject to the via design rule of the technology node. Lastly, we study how initial void size of a TSV can affect the failure time of an entire MSV structure. Throughout the section, we assume 45nm technology [49].

Our EM modeling algorithm has been implemented with Python programming language, and all the experiments are performed on a machine with 2.93GHz Intel quad-core Xeon X5670 CPU, 71GB of memory, Red Hat Enterprise Linux 5.9. Its running time is dependent on the time step size and the detected failure time. In our experiments, we set the step size so that the number of time steps until the failure time is in between a thousand and ten thousand. This provides comparable results across simulation runs and a running time of maximum 30 seconds for each simulation.

5.4.1 Study on Barrier Resistivity

Figure 5.9 shows a schematic view of vias in the dual-damascene copper process [26, 71]. For both TSVs and local vias, tantalum (Ta) or tantalum

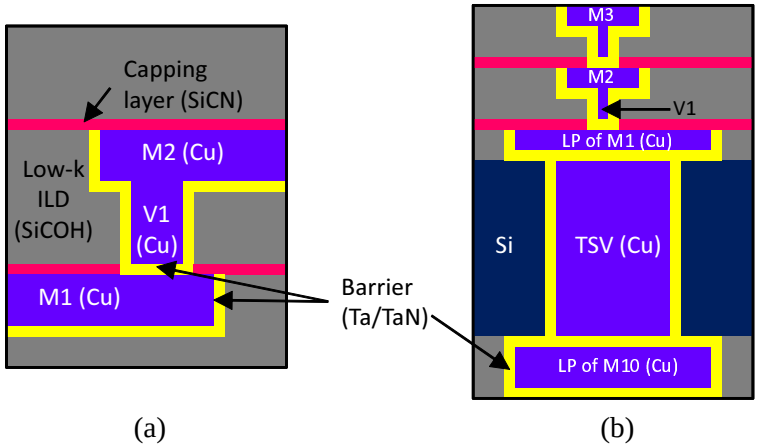


Figure 5.9: Schematics of via structures: (a) local via between M_1 and M_2 [71], (b) MSV including via-first/middle TSV [26] and local vias stacked on top of landing pads. The barrier layer (yellow in this figure) is located at the bottom of both local vias and the TSV.

Table 5.3: Resistivity of TaN according to partial pressure of nitride during manufacturing [50]

N_2 pressure	0.0%	5.0%	10.0%	20.0%	30.0%
ρ_{TaN} [1e-8Ωm]	95	254	702	2810	14800

nitride (TaN) can be used as barrier material at the sidewall and the bottom of the via structure. This barrier prevents diffusion of copper to inter-layer dielectric, and enhances the adhesion of copper. Although various materials may be used as the barrier material, such as Ta/TaN, TaC, TiN, TiC, WC [28], we limit the scope of our study to TaN due to its wide use. Because the barrier acts as the physical obstacle to atomic flux (zero atomic flux at the boundary [28]), migrated copper atoms from the via trench cannot cross the barrier, which facilitates void growth under the barrier with downstream EM.

The resistivity of barrier material is difficult to express with a constant. In Table 5.3, we show resistivity variation of barrier material TaN which is usually generated by partial pressure of nitride during manufacturing [50]. We note barrier resistance can vary greatly depending on the partial pressure of nitride. In fact, it is hard to express the barrier resistivity value of a certain barrier structure with a single number because of the variation in the material proportion of compounds as well as in the microstructure such as the grain size and the orientation [28]. Instead of looking at certain values, we observe the impact of a wide range of barrier resistivity values on EM failure time of MSV structures.

Based on our model discussed in Section 5.3, we observe the effect of TaN barrier resistivity on EM failure time of MSVs. For the experiments, we set an initial void radius as $0.1um$ for a TSV, $1nm$ for local vias, and assume 676 local vias on top of the TSV landing pad[1]. Other parameters are specified

[1]676 is the maximum number of V_1 local vias that can be packed within 3.6um×3.6um

Table 5.4: The effect of barrier resistivity ρ_{TaN} on failure time Tf of MSV.

ρ_{TaN}[1e-8Ωm]	Tf [a.u.]
200	1300
300	1214
500	1136
1000	1042
2000	992
3000	967
5000	939
10000	917

in Table 5.1.

The result, presented in Table 5.4, shows decreasing failure time, i.e. more vulnerability to EM, as the resistivity of the barrier increases. With the existence of a void under barrier of a via, the current has to detour through the barrier to avoid the void. This detour creates a concentration of the current in a smaller area of the barrier, which magnifies the effect of barrier resistivity, and contributes to the overall resistance increase from void growth. Since our failure criterion involves the relative amount of resistance change, increased resistivity reduces the time to failure.

5.4.2 Impact of Void-free Local Vias

Because a dual-damascene copper interconnect is known to have zero or a small nucleation time, we have assumed that all the local vias and the TSV have nucleated voids that can be grown. However, it is meaningful to see how

TSV landing pad, assuming 45nm technology for V_1.

Table 5.5: The effect of barrier resistivity ρ_{TaN} on failure time Tf of MSVs with varying ratio of void-free local vias.

ρ_{TaN}[1e-8Ωm]	Tf by V_1 voids only [a.u]	Tf by both TSV void and V_1 voids [a.u.] (%: V_1s w/o void)						Tf by TSV void only [a.u]
		0%	10%	20%	50%	80%	90%	
200	1311	1300	1594	4806	6658	7189	7269	7328
300	1222	1214	1411	2856	5839	6456	6561	6650
500	1150	1136	1264	1544	4825	5644	5792	5914
1000	1053	1042	1136	1294	3550	4711	4919	5089
2000	1006	992	1058	1167	2533	4075	4286	4444
3000	989	967	1038	1125	2247	3792	4075	4250
5000	967	939	1017	1092	2025	3561	3842	4075
10000	942	917	997	1072	1850	3406	3683	3911
avg. ratio of Tf	1	0.98	1.10	1.73	3.42	4.49	4.68	4.82

failure time of MSV changes according to the number of local vias without a void because sets of local vias may exhibit diverse void growth tendency, and a more advanced technology may be able to suppress void nucleation.

Our study with void-free local vias is shown in Table 5.5. Each value represents failure time with a given barrier resistivity and void-free ratio. The results shown in the previous section (Table 5.4) correspond to the column with 0% void-free ratio. The second column represents an extreme case when all the local vias have growing voids while TSV has no such void, and the last column shows another extreme when only the TSV has growing voids and all the local vias do not have voids at all. The columns in between show failure time of MSV when both local vias and TSV have growing voids due to EM, with varying ratio of void-free local vias.

If all the local vias and the TSV have their own void due to the EM, we get the worst failure time as shown in the column with 0%. In this case, the overall failure time is driven by the local via voids rather than the TSV void. However, with more void-free local vias, the influence of the TSV void gets stronger. Since failure time of the TSV void-only case (last column) is much longer than the failure time of the local via voids-only case (second column), if more and more vias do not have any void at all, the entire MSV would become much more robust and can achieve EM reliability close to a TSV.

Our findings evince the advantage of our approach. Depending on the void condition of vias, the failure time of MSVs can range from the failure time of the case with local via voids only to that of the TSV void only. Because

these diverse void conditions cannot be addressed by other EM models, such as models that only concern local vias or those only for TSVs, our proposed EM modeling for MSV structures is essential to understand the interplay between multiple voids across local vias and the TSV.

5.4.3 Study on Number of Local Vias

The size of a TSV is gigantic (a few um) in comparison to a local via (a few tens of nm). If we use just a single local via to connect to the TSV landing pad for power delivery, extremely high current crowds to the tiny local via and can have immediate failure from EM even at room temperature. For current load balancing, it is proper to assume multiple local vias on the TSV landing pad for a MSV. In this section, we examine the impact of the number of local vias connected to a TSV. We use 676 vias as the maximum number of local vias in a MSV, observing the design rules [49]. Other than the number of local vias, all the other parameters are still the same as Table 5.1. Here we assume a Gaussian distribution for current density between testing MSVs[2].

More local vias on a TSV mean more load balancing of the current, which eventually extends the failure time of a MSV. This tendency is shown in Figure 5.10, which is estimated by our EM model (Section 5.3). Increased reliability with more local vias indicates that we can achieve more robust 3D PDN system if we have more local vias connected to the TSV landing pads. We note that the failure time is improved by orders of magnitude when we

[2] $j = j_o \times \frac{N(100,\sigma^2)}{100}$ where $\sigma = 4$

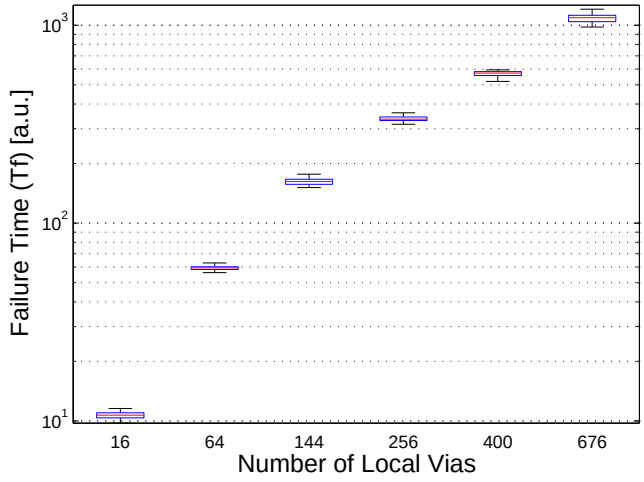


Figure 5.10: Impact of the number of local vias on failure time. For each case, 30 samples are used with current density variation. Boxes denote 25 and 75 percentile, while bars are min/max values.

increase the number of local vias from 16 to 676.

5.4.4 Trade-off Between Via Size and Number

We have investigated the impact of the number of vias on failure time in Section 5.4.3, assuming local vias have the minimum size in V_1 layer. The underlying premise is that a TSV landing pad is located on an M_1 layer if we have a via-first/middle approach for TSV manufacturing. However, via-middle TSV technology makes it possible to build a TSV during the BEOL process, which places the landing pad somewhere between M_1 and M_{10}. With this process, vias connected to a TSV landing pad may become much larger, which may reduce the number of vias, as shown in Figure 5.11. In this section, we

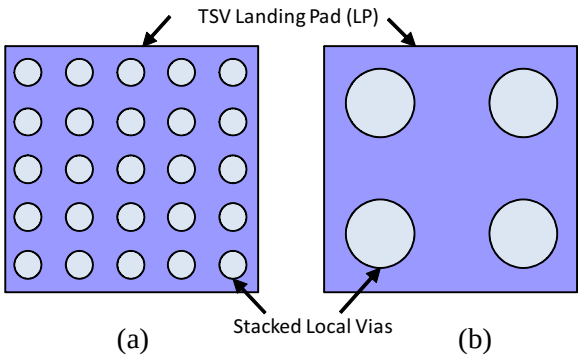


Figure 5.11: Example of trade-off between the size and the number of local vias. (a) has a large number of small-sized local vias on top of the TSV landing pad, while (b) has a small number of large-sized local vias.

explore the impact of this trade-off between size of local vias[3] (subject to via layer) and the number of vias connected to a TSV landing pad on the failure time from EM.

In our study of this trade-off, the diameter of vias d_{via} and the space between vias follows the 45nm design rule [49]. These parameters from the design rule give us the maximum number of vias within the 3.6um×3.6um landing pad. Then the maximum current density of each local via $j_{o,via}$ is

$$j_{o,via} = \frac{I_{o,TSV}}{n \times A_{via}} = \frac{j_{o,TSV} \times A_{TSV}}{n \times A_{via}}, \tag{5.9}$$

where $I_{o,TSV}$ and $j_{o,TSV}$ are total current and current density of TSV, n is the number of local via, and A_{via} is area of local via. We show $j_{o,via}$ of each layer in the third column of Table 5.6. Although V_1 is much smaller than V_8, up to

[3]Here we use the terminology *local via* as a via in the BEOL metal layers (V_1–V_9), as a distinct one from the TSV.

Table 5.6: Trade-off between the size of via with different via layers (V_1–V_8) and the number of local vias. Via size is based on 45nm technology [49].

Via Layer	d_{via}/ Space	# via / LP	$j_{o,via}$	Init. r_{void}	Crit. r_{void}	Tf [a.u]	Area [um^2]	Block Area[um^2]	Tf / Area	Tf / Block Area
V_1	65/75 nm	676	6.47MA/cm^2	5 nm	36.8 nm	1078	1.61	1.61	670 (1)	670 (1)
V_2	70/85 nm	529	6.95MA/cm^2	5 nm	38.0 nm	1044	1.50	5.65	696 (1.03)	185 (0.27)
V_4	140/160 nm	144	5.44MA/cm^2	5 nm	64.8 nm	2411	1.91	14.37	1261 (1.88)	168 (0.25)
V_8	400/440 nm	16	5.44MA/cm^2	5 nm	144 nm	5583	1.91	31.0	2923 (4.36)	180 (0.27)

676 V_1 vias can be packed in a landing pad while 16 vias with V_8, and current density of each local via does not show a significant difference.

In Table 5.6, *Init.* r_{void} and *Crit.* r_{void} represent the radius of an initial and critical void at the local via. We estimate the failure time of the MSV by our model as appears in the seventh column of the Table. *Area* is the area occupied by n local vias at the via layer, and *Block Area* indicates the potential area penalty that includes area occupied by the TSV when the TSV landing pad is located at the metal layer higher than M_1. Area and block area are defined as,

$$\text{Area} = n \times A_{via} \tag{5.10a}$$

$$\text{Block Area} = n \times A_{via} + (i_{VL} - 1) \times A_{TSV}, \tag{5.10b}$$

where n is number of local vias, and i_{VL} is via layer number (i.e. 1 for V_1, and 4 for V_4). From the seventh column of Table 5.6, we can see that failure time (Tf) improves as the via layer is located in the higher metal layer. This is mainly due to the larger critical void size to reach the failure criterion, and also due to the lower current density in V_4 and V_8.

In the last two columns, we show failure time per via area. Although Tf *per Area* for V_8 shows better robustness than V_1, if we consider all the blockage area occupied by TSV up to M_7, Tf *per Block Area* of V_8 becomes shorter than V_1. In sum, vias in a higher metal (e.g. M_8) provide better robustness then M_1 vias, when we pack as many vias as possible on the landing pad. However, in terms of failure time vs. block area efficiency, a higher metal

layer is not as good as a lower metal area if we consider the total blockage area that takes up the space of the TSV.

5.4.5 Analysis of Initial Void Size

In an MSV, both TSV and local vias can have an initial void. First, TSV can have a crack due to the thermo-mechanical stress generated by a coefficient of thermal expansion (CTE) mismatch [33]. For local vias, as the feature size becomes smaller and the aspect ratio of the via trench increases, unsuccessful filling inevitably leaves nano-size voids, which grows with time [28]. Since the initial void size of TSV and local vias can affect the failure time of MSV, we examine how much impact they have through our EM model. First we reveal the impact of void size of TSV and local via (V_1) on failure time of MSV. The top figure of Figure 5.12 shows the impacts of the TSV void size on failure time, when only TSV is responsible to the failure time of MSV. The bottom figure describes impacts of local void size on failure time, when the lifetime of MSV is driven by void growth of local vias only. As the initial void size increases, both cases show degraded robustness by having a shorter lifetime, because it is easier to reach the critical void size with a large initial void.

In general, if only a TSV void governs failure time of MSV (top figure), it is more robust than the opposite case driven by local via voids only (bottom figure). However, we find out that if the TSV has a very large initial void, and V_1 has a smaller initial void, TSV void can dominate the MSV failure time

even if both TSV and local vias have growing voids. The relationship between TSV initial void size and failure time of MSV is shown in Figure 5.13. In the figure, the red line represents that only the TSV void grows and V_1 does not have any void; in the green line, only the V_1 voids grow with fixed initial void (5nm); and in the blue dotted line, both TSV and V_1 voids grow, with V_1 initial void as $5nm$. We can see that if the diameter of a TSV initial void is larger than 0.9um and that of a local via void is 5nm, and both TSV void and local via voids grow due to EM, it follows that the TSV void induced failure trends. Although 0.9um of the TSV initial void seems to be an extreme case, it implies that a TSV crack can have a visible impact on the EM robustness of a MSV.

5.5 Electromigration of Full-chip 3D PDNs with Multi-scale Vias

In this Section, we extend our EM analysis of a single multi-scale via (MSV) to the full-chip level 3D power distribution networks (PDNs). First, we describe the overall flow of our EM analysis, and then show the impact of EM on IR-drop of 3D PDNs.

5.5.1 Overall Flow of EM Analysis for 3D PDNs

Figure 5.14 shows the overall flow EM analysis for 3D PDNs. Similar to the single MSV case, we have inputs, such as initial void condition (e.g. void location and initial void size), number of local vias per an MSV, number

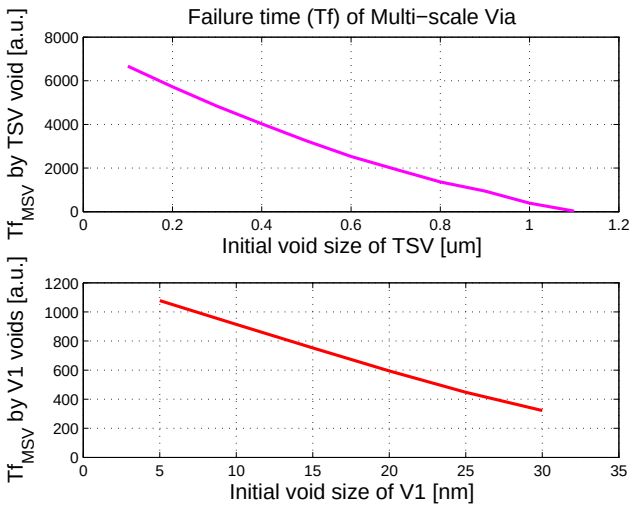


Figure 5.12: Impact of initial void size on failure time of MSV; (Top) impact of TSV void size, when MSV failure time is driven by the TSV only, and (bottom) impact of V_1 void size, when MSV failure time is driven by the V_1s only.

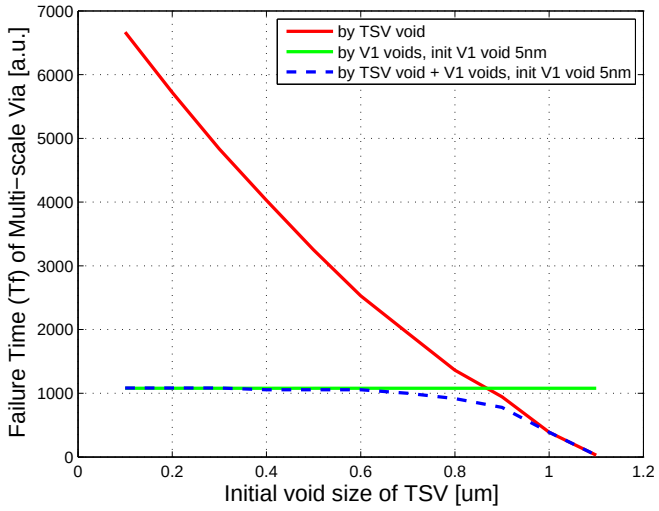


Figure 5.13: Impact of a large void (crack) of TSV on failure time of MSV via structure. If a TSV initial void is larger than 0.9um and a local via void is 5nm, and both the TSV void and the local via voids grow due to EM, it follows the TSV void induced failure trends.

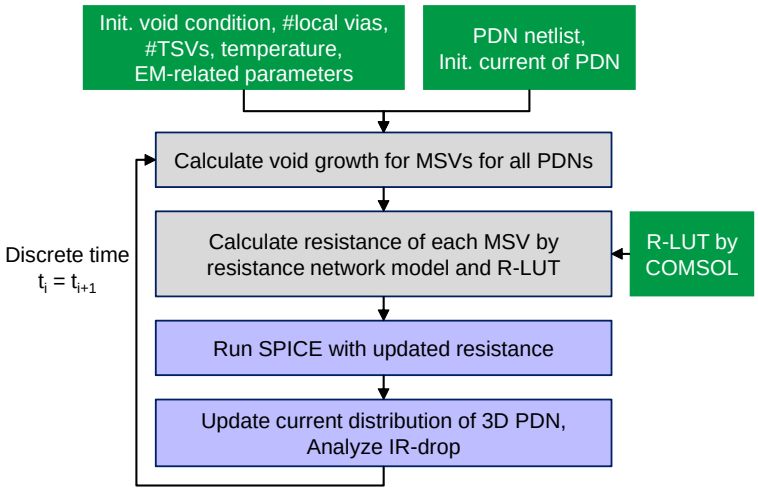


Figure 5.14: Flow for EM analysis of full-chip level 3D PDNs using MSVs.

of TSVs per die, temperature distribution, and EM-related parameters as we shown in Table 5.1. On top of it, we need PDN netlists and initial current distribution of a PDN as inputs for the full-chip analysis. We assume power consumption from gates remains the same as time goes by, meanwhile that from the interconnects can be varied due to the change of resistance of a PDN.

As illustrated in Figure 5.14, the first step of full-chip EM analysis is calculating void growth of all MSVs, for a discrete time step. In the previous Section 5.3.1, we described that we can calculate void growth for a single MSV when we assume cylindrical void growth beneath the barrier, under the vias. Here we extend that methodology to the multiple MSVs. For the multiple MSVs, the basic void growing algorithm is used, but we use different current values for the different MSVs, according to the current distribution informa-

tion. If we have information on geometric temperature distribution according to time, we can use it in this stage as well. Next, we calculate the resistance of each MSV. Similar to the single MSV case in Section 5.3.2, we use the resistance network model (Figure 5.7) and resistance look-up tables (R-LUT) generated by COMSOL. And then, we run spice simulation with updated resistance of the PDN. After that, we can get the new current distribution for the entire PDN, by reflecting the void growth of each MSV during the time step. We update the current distribution of MSVs accordingly, analyze the IR-drop, and then repeat the process for the next time step.

5.5.2 EM and IR-drop Analysis of MSV-based PDNs

For a single MSV structure, we use a *5% change of resistance* as the failure criteria. However in case of a full-chip PDN, the single-number of failure time can be less meaningful, because we may have a different lifetime for different MSVs, depending on their current distribution and void condition. Thus, we analyze the IR-drop of MSVs according to time, and use it for our reliability metric due to EM.

We measure average IR-drop of the MSVs in the benchmark circuits with our transient simulation, and show the results in Table 5.7. All the benchmark circuits include 2-tier stacked dies with array-time TSVs [75]. Combining the benchmark meshes with our MSV model, we exemplify a 2-tier 3D PDN in Figure 5.15. In this figure, two dies are faced down, thus the MSV structure is also upside-down; we can see local via arrays under the TSV cylinder, which

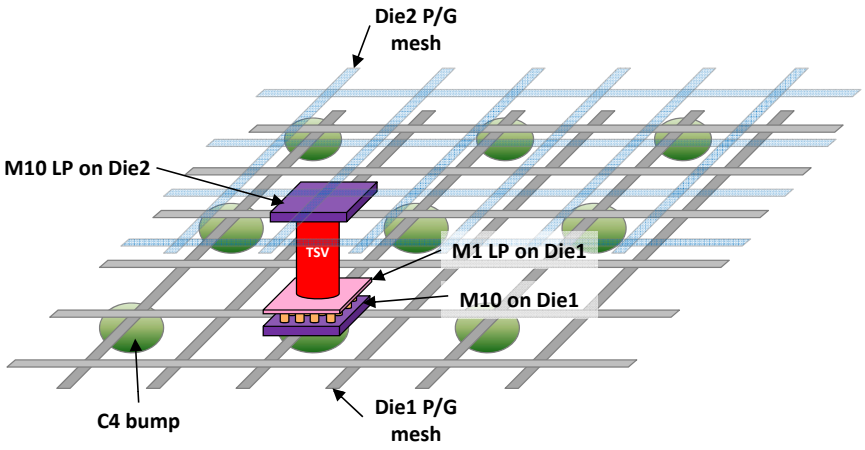


Figure 5.15: Illustration of a 2-tier 3D PDN with MSV structures. For simplification we display only one MSV in this Figure.

is the opposite as we showed in Figure 5.3. For Table 5.7, we assume that the temperature is set to 130°C, and all the local vias and TSVs have void seeds. In other words, we assume nano-scale initial voids are already nucleated under the local vias and TSVs, and make them grow accordingly as time goes by. We use 676 local vias per MSV structure, which is the maximum number of local vias in our setting from 45nm technology node, as we discussed in Section 5.4.3.

During our experiments for Table 5.7, we use the same PDN meshes as the previous work [75]. The differences between our work and the work in [75] are as follows: 1) the work in [75] used via-last TSVs without any local vias while we consider multi-scale vias with local via array and via-first/middle TSVs, and 2) we use different modeling of EM, we consider resistance change based on the void growth, whereas the work in [75] is based on the change

of atomic concentration without considering void growth. The footprint area, number of TSV and C4 bumps, and power density of benchmark circuits are described in the first seven columns of Table 5.7. We note that the other EM-related parameters such as temperature may set differently since the work [75] does not show temperature value, therefore we would like to emphasize that this table is not intended for comparison of reliability between via-last TSVs in [75] and MSV structures in our work.

From table 5.7, we can see that the average IR-drop of MSV structures increase for the long-term simulation. Compared to the initial IR voltages, there is a 31.8% of IR voltage increase after 2e8 seconds ($\approx$ 6.3 years) passed due to EM. Once EM has occurred, due to the voids developed under the local vias and TSVs, each MSV structure can have a higher resistance than before, and that increases the IR-drop of MSVs and the entire PDNs. In this experiment, we assume that all the C4 bumps are aligned with the TSV locations to minimize IR-drop loss, so a current crowding analysis between TSVs and C4 bumps was not needed, which the previous work [75] performed. The average run time is less than 30 seconds per iteration (i.e. time step) for the largest benchmark, *PDN5*. In our experiments, we use 50 iterations per case for each design.

Figure 5.16(a) and Figure 5.16(b) show transient IR-drop change due to EM. For illustration we use a smaller circuit than the benchmarks in Table 5.7, it has only 16 MSV arrays. Each MSV has 676 local vias and a single TSV. Comparing between Figure 5.16(a) and Figure 5.16(b), we can see that

Table 5.7: Full-chip EM evaluation of 3D PDNs using multi-scale vias. Benchmark circuits are the same as the work in [75].

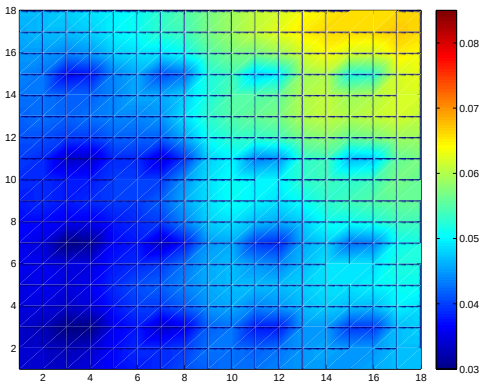
Design	Area [mm^2]	Pwr dens top [W/mm^2]	Pwr dens bot [W/mm^2]	Pwr grid [#×#]	# TSVs	# C4	Avg. IR-drop of MSVs in mV (%increase) t=0s	t=5e7s≈1.6yrs	t=1e8s≈3.2yrs	t=2e8s≈6.3yrs	Avg. runtime per iter. [sec]
PDN1	5x5	0.57	0.57	50x50	144	144	33.96	38.33 (12.9%)	39.93 (17.6%)	41.45 (22.1%)	0.82
PDN2	6x6	0.80	0.75	60x60	225	225	44.82	52.38 (16.8%)	53.11 (18.5%)	57.50 (28.7%)	4.89
PDN3	9x9	0.80	0.80	90x90	484	484	45.60	53.30 (16.9%)	54.08 (18.6%)	59.98 (31.5 %)	7.84
PDN4	11x11	0.71	0.91	110x110	729	729	45.67	53.38 (16.9%)	54.17 (18.6%)	60.60 (32.7%)	13.63
PDN5	15x15	0.47	0.49	150x150	1369	1369	26.66	28.90 (8.4%)	31.40 (17.8%)	39.81 (49.3%)	26.29

maximum and average IR-voltages increased significantly.

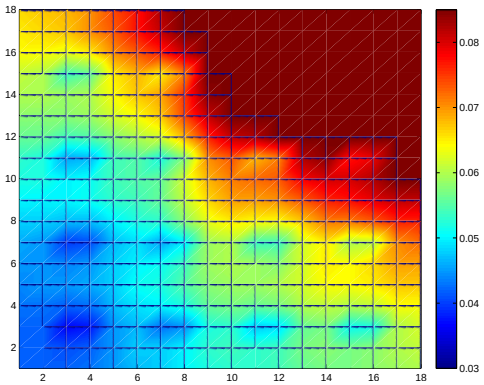
5.5.3 Full-chip EM Analysis on Initial Void Condition of MSVs

With the suggested full-chip EM analysis flow, we investigate the impact of the initial void condition on MSVs. Table 5.8 shows the average IR-drop of MSVs when t=2e8 seconds, under the same condition as Table 5.7 except the initial void condition. For this experiment, we changed the ratio of local vias without initial voids, from 0% to 90%, similarly to the study in Section 5.4.2. In other words, 0% means that all the local vias have initial voids to grow, and 90% means that 90% of local vias in the MSV structures are void-free. From the table, the average IR voltage increases slower with a higher percentage of void-free local vias. This implies that the *importance of perfection in manufacturing*; if we have a larger number of *imperfect* vias with initial defects, we can have a higher IR-drop in a PDN due to EM.

We plot transient IR voltage changes in Figure 5.17. According to the time, IR-drop increases, and it rises faster if we have imperfect local vias only (i.e. 0%). Also from the graph, we can see the two-phase of IR-drop increase. The first part is *local via dominant phase*. As we discussed in Section 5.4.5, local vias can contribute more than a TSV to the resistance change of an MSV, when the initial void of TSV is not very big. In this phase, we can see that the IR-drop differs largely depending on the ratio of immortal local vias. However once the local via voids are developed enough, the TSV can dominate the resistance change of an MSV. That appears in the second phase,



(a)



(b)

Figure 5.16: IR voltage distribution of top die of a small 3D PDN with MSVs; (a) initial distribution, (b) after t=1.8e8 seconds. We use 4x4 TSV arrays for illustration. Here we use temperature as 130° C, and assume that all the local vias and TSVs have initial voids, to show the worst case scenario.

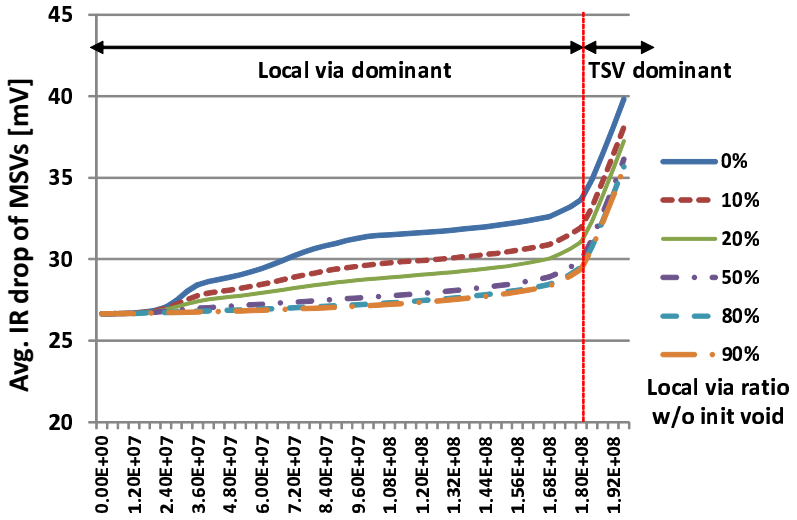


Figure 5.17: Effect of initial void condition on average IR-drop of MSVs, when t=2e8 seconds. Here percentage stands the ratio of void-free local vias.

TSV dominant phase in this graph. Here we can see the steep increase of IR voltage on average, because some of the MSVs now have very large resistance, not only due to the local vias voids, but also due to the TSV voids.

5.5.4 Temperature and Current Density Impact on EM Reliability of Full-chip 3D PDNs

Lastly, the impact of temperature and current density of EM is studied, in terms of IR voltages of MSV-based 3D PDNs. First, we investigate that the higher temperature can make EM-induced IR-drop worse. Figure 5.18 evinces the temperature effect on average IR-drop voltages. For five benchmark circuits, we test IR-drop voltages when t=2e8 seconds for two different temperatures, 100°C and 130°C. All the other settings are same as Table 5.7. From the

Table 5.8: Impact of initial void condition on average IR-drop voltages of full-chip 3D PDNs using multi-scale vias. Percentage refers to the ratio of void-free local vias. Benchmark circuits are the same as the Table 5.7.

Design	t = 0	Avg. IR-drop of MSVs in mV at t = 2e8 sec ≈ 6.3 years (%increase)					
		0%	10%	20%	50%	80%	90%
PDN1	33.96	41.45 (22.1%)	39.27 (15.6%)	38.15 (12.3%)	36.72 (8.1%)	36.14 (6.4%)	36.02 (6.1%)
PDN2	44.82	57.70 (28.7%)	54.83 (22.3%)	53.35 (19.0%)	51.46 (14.8%)	50.70 (13.1%)	50.53 (12.7%)
PDN3	45.60	59.98 (31.5%)	57.08 (25.2%)	55.59 (21.9%)	53.67 (17.7%)	52.91 (16.0%)	52.74 (15.7%)
PDN4	45.67	60.60 (32.7%)	57.69 (26.3%)	56.20 (23.1%)	54.28 (18.9%)	53.51 (17.2%)	53.34 (16.8%)
PDN5	26.66	39.81 (49.3%)	38.12 (43.0%)	37.25 (39.7%)	36.13 (35.5%)	35.68 (33.8%)	35.59 (33.5%)

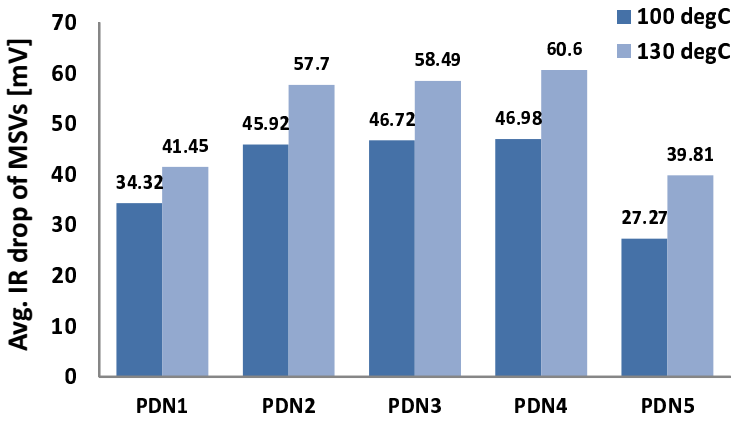


Figure 5.18: Graph to show temperature effect on IR-drop of MSVs in 3D PDNs. We changed the temperature from 100°C, 130°C and 160°C, and get the average IR-drop of MSVs. Here we assume that all the local vias and TSVs have initial voids, to show the worst case scenario.

figure, IR voltage increases by 28.2% in the higher temperature (130°) on average. Because temperature is in the exponent of diffusivity in Eqn. (5.2), there can be exponentially worse EM effects with increased temperature. Therefore, it is important to have lower temperature in the operating circuits to reduce EM.

EM is also tightly related with the current density as we discussed in the Eqn. (5.1). To study current density impact on IR voltages of PDNs, we change input current to 90% and 110%, simulate EM-induced IR-drop voltages of 3D PDNs. The average IR-drop values of MSVs at t=2e8 seconds appear in Figure 5.19. Comparing to the original current density, 10% decrease of current density shows -14.6% of IR voltages, while 10% increase of current density raises IR voltage by 21% on average.

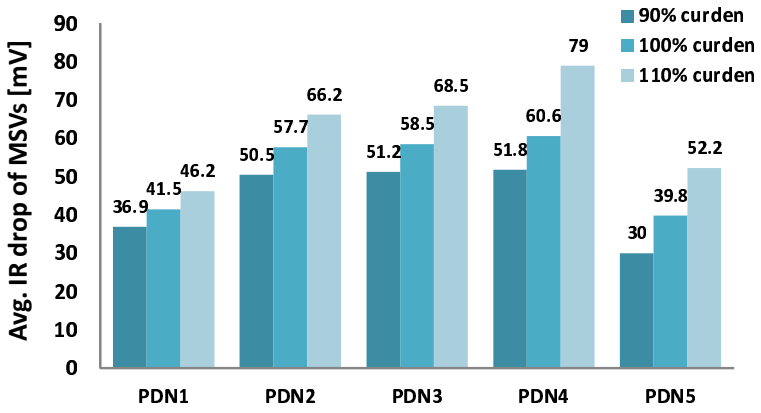


Figure 5.19: Impact of current density on average IR-drop of MSVs, when t=2e8 seconds. We changed injected current density of each current source, 90%, and 110% from the original values for spice simulation. Here we use temperature as 130° C, and assume that all the local vias and TSVs have initial voids, to show the worst case scenario.

5.6 Summary

In this chapter, we propose an efficient EM modeling flow for multi-scale via (MSV) structure in 3D PDN. Our experimental results show that EM modeling approaches only for TSVs or those for local vias may not be able to estimate the EM reliability of the entire MSV, and that our integrated EM modeling approach is essential for MSV structures in 3D PDN.

We also investigate the impact of structure, material, and pre-existing void condition on EM-critical time of MSV of 3D PDN. For the material impact on the EM-induced failure time of MSV, we show that barrier resistivity can have significant effect on the lifetime of the MSV. Also, as many as possible local vias can be necessary to achieve robustness of the MSV structure.

Out of the trade-off space between local via size and the number of local vias in the MSV, we find that a small number of large vias can be more preferable to many small vias in terms of EM. However, large vias on upper metal layers may have disadvantages of an increased blockage area for routing.

We find that barrier resistivity and a pre-existing void condition can play a great role in EM lifetime of an MSV structure. Depending on the pre-existing void condition, the lifetime of an MSV can be dominated by either TSV or the local via array. In many cases, EM reliability is more likely to be dependent on local vias than TSV. However, if we have local vias without voids, or the pre-existing void of the TSV is large enough, the EM of TSV can also dominate the failure time of MSV.

Finally we extend our study on EM of an MSV structure to the full-chip level 3D PDNs. With the suggested EM-evaluation algorithm, we can get the IR-drop of a 3D PDNs with a reasonable run time. Since EM increases resistance of MSVs in a PDN, the IR-drop of a 3D PDN increases as time goes by, and we study the impact of initial void condition, temperature and current density on EM of full-chip level 3D PDNs.

Our experimental results demonstrate that our EM modeling can efficiently estimate the EM reliability of the entire MSV structure in 3D PDN, and we expect this model to analyze reliability with EM in more complex structures.

Chapter 6

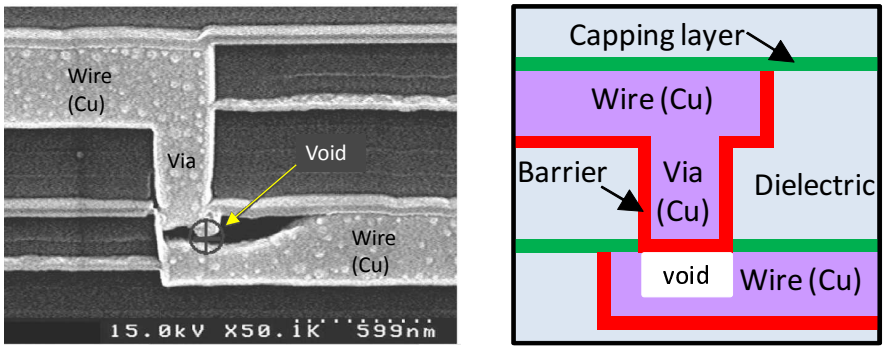
Redundant Via Insertion in Future Technology nodes

6.1 Introduction

Vias are critical structures of advanced IC design that help expanding the design space by connecting layers vertically. Despite its importance in circuit design, vias are often considered as one of the major sources of process and reliability issues that may degrade circuit performance, or may even fail the circuits [38].

One major source of via reliability issues is Electromigration (EM), diffusion of metal atoms induced by electron current. As IC technology advances, current density increases due to the reduction of cross-sectional via area, which negatively affects failure time. Reduction in the failure time from EM can be worsened even further by high temperatures and mechanical stress around the vias.

By inserting redundant vias, we can mitigate the adverse effect of electromigration, because it can reduce the current density of each via. Since via redundancy has been known to improve yield and reliability, much work has been done to maximize insertion of redundant vias during post-layout opti-



(a) (b)

Figure 6.1: (a) SEM image of via structure with a void under the via, due to EM [70], and (b) schematic view of the structure.

mization [8, 35–37, 41] or during the routing stage [16, 73].

However, those studies mostly focused on the quantity of redundancy, not on the quality of redundancy. Though some work addressed via yield issue by considering line end extension and redundant vias altogether in the context of EM reliability [41], there has been little work that focuses on the EM related lifetime as the main objective of via insertion.

In this chapter, we propose an EM-aware redundant via insertion approach that can be applicable for the post-layout optimization. Our contributions are summarized as follows:

- We model and analyze electromigration (EM) for various redundant-via structures. Our model includes a holistic failure model on how the early

failure of one via can affect the lifetime of the remaining vias in a structure with multiple vias.

- Based on the model, we find that current imbalance in redundant vias affects EM reliability of the whole structure. Also, unlike previous work that preferred on-track double-via layouts [37], our modeling results suggest that off-track layouts may benefits EM reliability.

- We propose a via-insertion algorithm that chooses the best redundant via layout for the EM-prone nets, which can maximize the EM reliability compared to the conventional redundant via insertion. To the best of our knowledge, this study is the first one to focus on EM-aware redundant via insertion.

- We present a set of speed-up techniques to achieve better trade-off between runtime and performance during via-insertion.

6.2 Preliminaries

6.2.1 EM and Via Structure

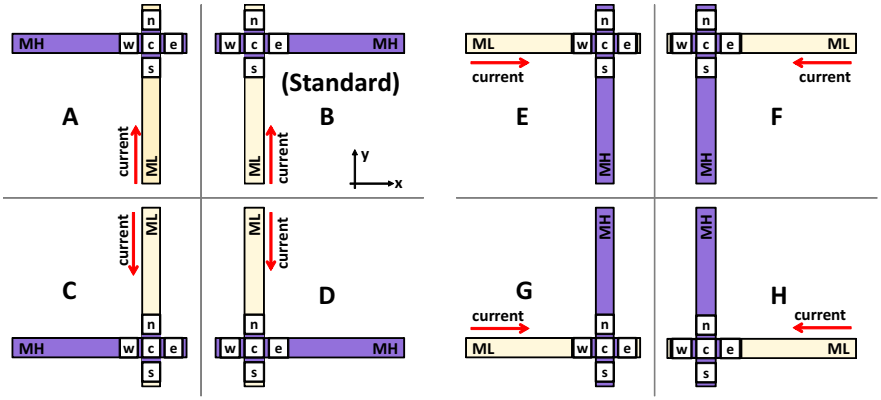
With EM, the interface of the via and the metal wire is one of the weakest points to EM. We can see this phenomenon in Figure 6.1(a) with an SEM image of the local via and wires [70]. To be more specific, Figure 6.1(b) shows the schematic view of metal wires, local via structure and a EM-induced void with Cu dual-damascene process. In the figures, we assume that the current flows from the bottom to the top of the via; electrons and migrated Cu atoms move from the upper metal layer to the lower layer, which we call

downstream EM in general. According to the previous studies, downstream EM shows worse failure time than upstream ones [51], and in our work, we assume all the EM flows in the vias as downstream. With downstream EM, the barrier under the via trench acts as the physical barrier for the Cu flow, hence we can have divergence of flux at under the barrier, and the voids tend to be nucleated and grown as illustrated in Figure 6.1(b). If the void under the via spans larger than the via size, the interconnect becomes an open circuit, and we regard it as the *failure of a via* in our work.

6.2.2 Layout Cases with Redundant Vias

In the actual layout, redundant vias can be realized in the various combinations of different wire/via locations. To clearly see the impact of different layouts on EM in the following sections, we first examine the possible wire position cases and redundant via (RV) cases.

Figure 6.2 shows eight possible wire position cases, which can be made from the two orthogonal wires in the adjacent routing layers. Here *MH* and *ML* stand for higher metal and lower metal wire, respectively. For the wire position cases, we assume 1) two wires are located in the adjacent metal layers, and 2) current flows from the lower metal to the higher metal (=downstream EM) as we discussed in Section 6.2.1. Assuming *case B* as the *standard layout*, we note that the EM of a certain via position in any wire position case can be equivalent to that of another via position in the standard layout. For example, considering current direction, via position of *(w,n,e,s)* of *case A* can



(a) (b)

Figure 6.2: Wire position cases that can be generated from the two orthogonal wires.

be considered as *(e,n,w,s)* of *case B* respectively when we calculate EM. We call this conversion as *transposition* in this work.

Definition 1 *Transposition is a conversion from any wire position case to the standard layout (wire position case B) to get the equivalent EM lifetime.*

Observation 1 *There are eight wire position cases from the two orthogonal wires in the adjacent routing layers, and the EM analysis of any of them is equivalent to the EM analysis of the another case. In other words, all the wire position cases are transposable with each other.*

As all the wire position cases are transposable with each other, we will analyze EM for *case B* in the rest of this chapter, which we call the *standard layout*.

Table 6.2 indicates the original via positions in each layout case and the corresponding via position in the standard layout. *Mir. Y* means mirroring to Y axis, and *Rot. X* means rotating X degrees in the counter clockwise

Layout case	Transpose to the standard layout	Via position	Corresponding via in the standard layout
A	Mir. Y	[w, n, e, s, c]	[e, n, w, s, c]
B (Standard)	-	[w, n, e, s, c]	[w, n, e, s, c]
C	Rot. 180	[w, n, e, s, c]	[e, s, w, n, c]
D	Rot. 180 & Mir. Y	[w, n, e, s, c]	[w, s, e, n, c]
E	Rot. 90	[w, n, e, s, c]	[s, w, n, e, c]
F	Rot. -90 & Mir. Y	[w, n, e, s, c]	[n, w, s, e, c]
G	Rot. 90 & Mir. Y	[w, n, e, s, c]	[s, e, n, w, c]
H	Rot. -90	[w, n, e, s, c]	[n, e, s, w, c]

Table 6.1: Transposition to the standard layout.

direction in this table. For instance, EM failure time of vias *(c,w)* in *case C* is the same as that of via *(c,e)* in the standard layout.

Next, we introduce the *unit structure* as a unit of evaluating the EM-failure in the following sections.

Definition 2 *A unit structure is the one with 1) two orthogonal wires with standard layout, and 2) a center via* c.

As we add redundant vias on top of the unit structure, depending on the combination of redundant vias, we can have various layout cases. Figure 6.3(a) shows possible redundant via positions for double/triple via cases from the unit structure. At the cross point of the wires in a unit structure, the original via c is located. Additional redundant vias occupy positions closer to c first to minimize blockage penalty. Thus $\{s,\ e,\ n,\ w\}$ are the possible candidates

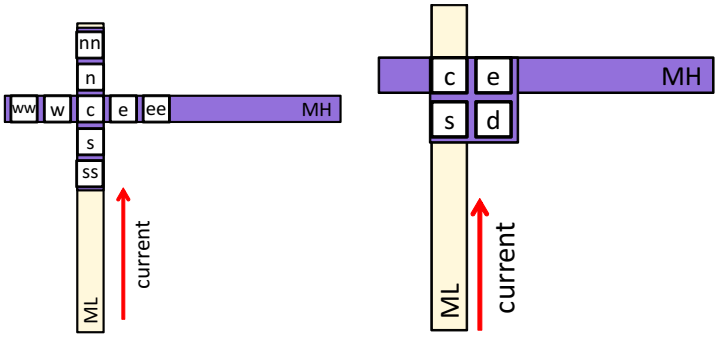
#Via	1	2	3	4
RV case	c	cs, ce, cn, cw	css, cse, csn, csw, cee, cen, cew, cnn, cnw, cww	cesd

Table 6.2: Redundant via (RV) cases for EM analysis.

for the first redundant via. If we consider s as the next redundant via, for example, we may choose one among the closest candidates for each direction, $\{ss,\ e,\ n,\ w\}$ positions. We call it a '*css*' layout case if we choose three vias *(c, s, ss)*, and call it '*cse*' for a *(c, s, e)* selection. This way, we can have ten possible layout cases for triple vias, *css, cse, csn, csw, cee, cen, cew, cnn, cnw* and *cww*. For double vias, *cs, ce, cn, cw* are four possible layout cases for our redundant via scheme. We note that stubs can be needed depending on the redundant via position. For example, in the *cs* structure, a higher metal (MH) stub should exist to connect with an *s* via. In the case of quadruple via cases, we consider only a single case, which consists of a 2 by 2 array, with a stub structure for both MH and ML, as shown in Figure 6.3(b). Here d is the diagonal via from the center via *c*.

Table 6.2 summarizes the single via and redundant via (RV) cases that we consider during redundant via insertion. We will use these RV cases for the rest of the chapter.

There has been much work on insertion of redundant vias, and most of them focused on double vias, which creates four different cases–(*cs, ce, cw, cn*). Previous work [37, 73] classified *cs* and *ce* as *on-track* vias and *cn* and *cw* as *off-track* vias depending on whether the redundant via requires an



(a) (b)

Figure 6.3: (a) Redundant via positions of the unit structure, for double/triple via cases. (b) Quadruple via position in our work.

additional routing resources. The post-layout via insertion method that Lee and Wang [37] suggested has preference on on-track vias over off-track vias due to less routing resource and better electrical property. Later in this chapter (Section 6.3.2), we will re-examine these cases in the context of EM reliability.

6.3 EM modeling for Redundant Vias with Various Layouts

Unlike a single via that has to accept all the current, redundant vias can load-balance the current that goes through the interconnect. This load-balancing on current can slow down the effect of EM, which may delay the time of failure further. Meanwhile, because current distribution of redundant vias varies depending on the relative position of vias, a certain layout of redundant vias may have a relatively beneficial effect on the failure time than the other types of layouts. In this section, we model and estimate how different layouts

of redundant vias can affect the time to failure.

6.3.1 EM Modeling Flow of Redundant Vias

In a multiple via case, if a current imbalance exists between vias, the growth of one via becomes faster than the other. The larger void size in a via increases resistance of the via, and it affects current distribution between the entire structure, creating a feedback loop. To simulate this, we model void growth time of redundant via structure considering the transient void growth effect on the current distribution.

Algorithm 2 presents our EM modeling flow. Input of our modeling is the initial current density of the wire, before any growth of voids occurred. For the discrete time step, we calculate the void growth of each via for the current time step. Inspired by the previous studies [23,52], we use a cylindrical void model under the via, and calculate the void radius dr that grows during the time step dt. Assuming vacancy flux during time dt generates void growth with volume dV [23, 52],

$$dV = \alpha f \Omega J_v dt = \alpha f \Omega \frac{DC}{kT} Ze\rho j \cdot dt = 2\pi r_{void} \delta dr \tag{6.1}$$

where J_v is vacancy flux, δ is thickness of void and r_{void} is radius of the cylindrical void. The parameter values in our model is shown in Table 6.3. Our EM failure criteria is based on the size of the voids. If one of the vias, say via_i, has a larger than the critical void size (=via size), we report the current time step as the failure time of via_i. Still, if we have other vias alive, the unit

```
foreach case;                    /* redundant via position case */
do
    ti = 0;                                  /* discrete time */
    Initialize-Void-Size();
    while (1) do
        foreach via_i in case do
            VoidSize[case][via_i]=GetVoidGrowth(dt);
            Resistance[case][via_i]=Read-R-
            LUT(VoidSize[case][via_i]);

            if VoidSize[via_i] ¿ CritSize then
                TfVia[case][via_i] = ti;
            end
        end
        if all the vias in case failed then
            return TfVia[case];
        end
        UpdateCurrent(Resistance[case]);
        ti = ti + dt                          /* dt=time step */
    end
end
```

Algorithm 2: EM modeling flow for redundant vias

structure is functionally working. Thus the ultimate failure time of the unit structure is the time when all the vias fail in it.

The next step is to update the current distribution to reflect the void growth in the current time step. Once the void under one via gets larger, the other via can experience more current crowding. To simulate current distribution for each time step, we use the resistance network model and look-up table, similar to the work in [52]. Redundant vias can be modeled as a parallel resistance network, and the amount of current flowing to one via is

Parameter	Description	Value
T	Temperature	$423K = 150\ ^{\circ}C$
k	Boltzmann const.	1.38×10^{-23}
α	Ratio of captured vacancies	1.0 [23]
f	Ratio of vacancy volume	0.4 [57]
Ω	Atomic volume	1.182×10^{-29} [57]
D_o	Initial diffusivity	0.0047
Ea	Activation Energy	$0.9eV = 1.44 \times 10^{-19}V$
Z^*	Effective charge const.	1.0 [23]
e	Electron charge	$1.6 \times 10^{-19}C$

Table 6.3: Parameter values for EM modeling.

inversely proportional to the resistance of the via. To get the resistance of each via with a void, we build an resistance look-up table (R-LUT) that gives us a resistance value of a single via, when we have the size of the void as the input. This R-LUT is built by pre-simulating the via resistance by changing the void radius with an FEA simulator. In this way, we can re-distribute the current for the next time step, and model transient void growth of all the redundant vias in the unit structure.

6.3.2 Current Distribution of Redundant Vias

Different layouts of redundant vias have different current distribution, therefore they affect failure time from EM. Figure 6.4 exemplifies it: *on-track* redundant vias have more balanced current density. Although some previous work has looked at different layouts of redundant vias during the post-layout stage [35, 37], to the best of our knowledge, they have not quantitatively estimated the failure time of different layouts, and EM reliability has not been their major consideration for preference of one case to others.

As we depicted in Table 6.2 in Section 6.2.2, we model EM for a single

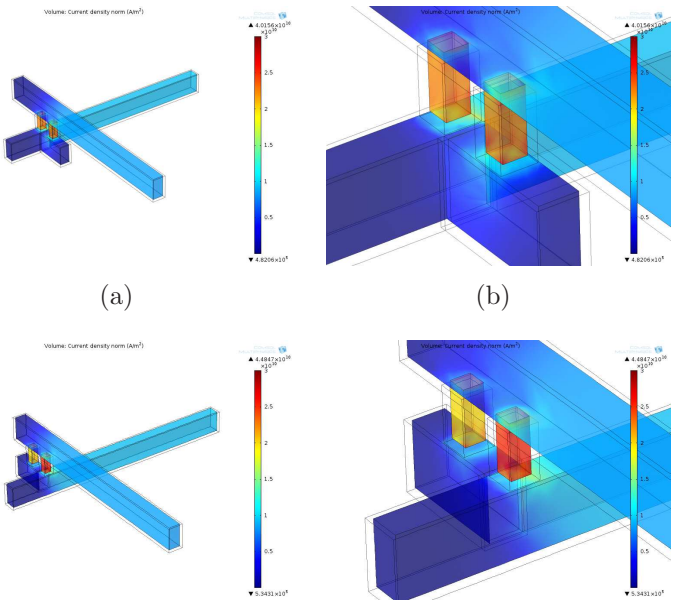


Figure 6.4: Example of current density distribution for different layouts. (a) and (b): *on-track* redundant vias. (c) and (d): *off-track* redundant vias.

via case, four cases of double via layout, ten for triple via layout, and one case for quadruple via layout, and observe how differently current is distributed over vias. We use an FEA simulator to get the current distribution of each via. Among 16 different RV layout cases, we show two triple via cases in Figure 6.5. It displays the 75 percentile of current density of each via within different layout cases, *css* (on-track case) and *cnn* (off-track case), when the input current density of the lower wire is $1e10[A/m^2]$. In the figure, we can see that on-track cases show a similar current density between vias, while off-track cases show a more uneven distribution. Double via cases have a similar trend, off-track cases show more uneven current density. During the

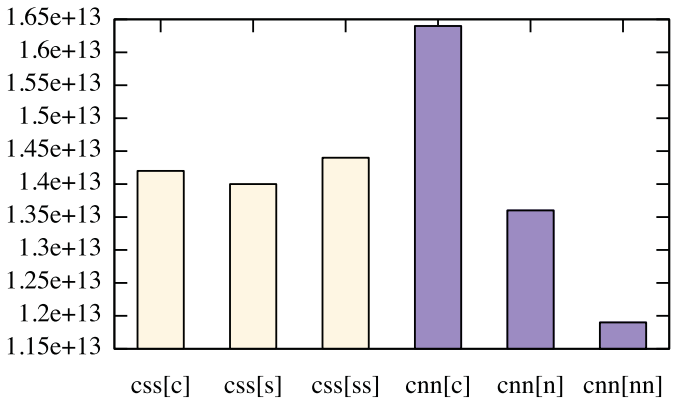
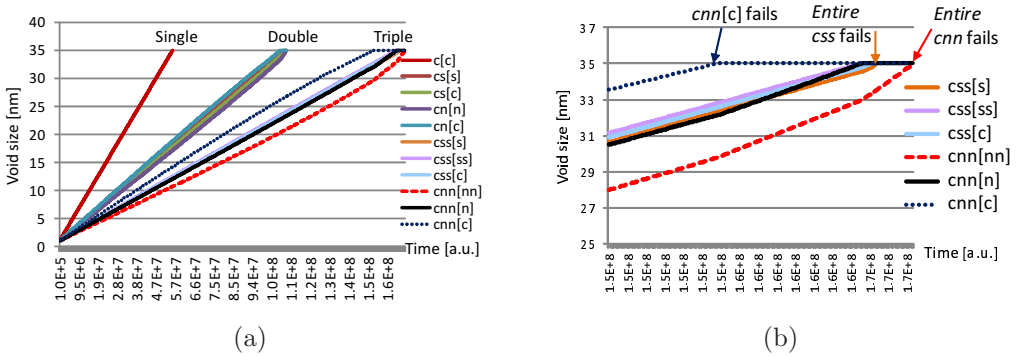


Figure 6.5: Current density of each via with different layouts. On-track redundant vias in *css* using on-track redundant vias shows more balanced current density between vias.

EM modeling that we discussed in Section 6.3.1, we use *effective resistance* of each of redundant vias to consider the current balancing effect from different layouts. As an example, if current density of triple vias are $a : b : c$ from our simulation, effective resistance of them can be the inverse value of it, $1/a : 1/b : 1/c$. On top of the effective resistance from current imbalance, we consider the resistance change due to the voids as we discussed in Section 6.3.1.

6.3.3 Effect of Current Imbalance in Void Growth

Figure 6.6 shows void growth time of a few example RV cases from our model. We get the failure time (Tf) from our model, for single, double, triple and quadruple vias, and show an excerpt of the values in this figure. The critical void radius for failure is $35nm$ in this example. As expected, the single



(a) (b)

Figure 6.6: (a) Void growth time of redundant vias with different redundant via cases. Off-track *cnn* case shows different Tf for each via position. (b) Zoom-in shot of (a).

via fails first, followed by double and triple layout cases from Figure 6.6(a). Within each layout case, larger current imbalance of a case often correlates with larger reliability. The *cnn* case is an example. From Figure 6.6(b), one of its via *cnn[c]* fails earlier than the other vias in triple via layouts due to current imbalance. However it helps the off-track via *cnn[n]* remain relatively unaffected by EM. As a result, *cnn* can have a longer lifetime than the on-track layout *css* case. Although the difference between the lifetime of *css* and *cnn* may not be very significant, it still shows that on-track redundant vias do not have any advantages in terms of EM reliability at least. The double via case shows a similar trend: the off-track RV case *cn* shows an equal or larger lifetime than the one with on-track vias, *cs*.

6.3.4 EM Library for Layout Optimization

Since the evaluation of the lifetime should be done quickly and accurately during our optimization, we pre-generate the EM library to store failure time of each layout case by sweeping the current density of the wire. The failure time of each case is calculated by our EM estimation, as discussed in Algorithm 2. The inputs of the EM library is current density, and the output is failure time. With the EM library, we can estimate the lifetime of the structure with known input current, with minimum runtime. Although we do not show the temperature difference in this chapter, our EM library can be easily expandable to the temperature dimension as well, since our model considers temperature as shown in Eqn. (2.2).

6.4 Post-layout Optimization for EM-aware Redundant Via Insertion

Figure 6.7 illustrates our EM-aware redundant via insertion flow, which is a four-step process. (1) Redundant via candidate generation by selecting vias vulnerable to EM (Section 6.4.1); (2) Conflict graph construction (Section 6.4.2); (3) ILP based redundant via insertion (Section 6.4.3); (4) Maximize the number of the via after EM-optimization (Section 6.4.4). It shall be noted that independent component and articulation point are speed-up techniques, and will be discussed in Section 6.5.

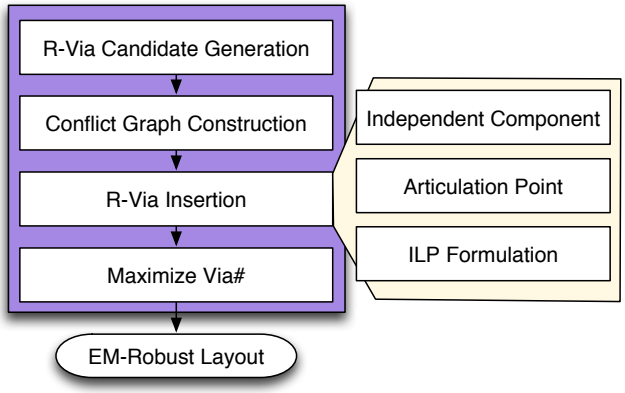


Figure 6.7: Overall flow of EM-aware via insertion.

6.4.1 Redundant Via Candidate Generation

The first step of EM evaluation of redundant vias is to transpose the wire positions to the *standard layout* case, as discussed in Figure 6.2. For each unit structure, we estimate the failure time of each redundant via (RV) case. In our work, $Tf_{(id,case)}$ stands for the failure time of RV case *case* of the unit structure id *id*. Evaluation of EM-failure time is done by utilizing pre-generated look-up table that we discussed in Section 6.3.4, based in EM model described in Section 6.3.

We evaluate the *potential improvement ratio* (PIR) of failure time, as in Eqn. (6.2).

$$PIR_{(id,case)} = \begin{cases} Tf_{(id,case)}/Tf_{th}, & \text{if } Tf_{(id,case)} \leq \alpha \times Tf_{th} \\ 0, & \text{otherwise} \end{cases} \tag{6.2}$$

Our goal of EM-aware redundant via is to maximize the number of unit structures that are EM-robust. Thus, if an RV case has already achieved long

enough failure time than the threshold, additional vias are not needed in terms of EM; it may be better to reserve the routing area for more redundant vias of EM-dangerous nets. Therefore, only if the lifetime is shorter than the certain target, we consider the redundant via case as a candidate for optimization. In Eqn (6.2), we set the *target* lifetime as α times of threshold lifetime. Hence, if a certain RV case has longer than $\alpha \times Tf_{th}$, PIR becomes zero, and the case will not be chosen during optimization, to prevent *over-inserting* redundant vias for EM-safe nets. For the rest of this chapter, we use $\alpha = 1.5$.

6.4.2 Conflict Graph Construction

After evaluating EM failure time of all the possible RV layout cases, we construct the conflict graphs. A conflict graph is an undirected graph with a single set of vertices **V**, and two sets of edges, **IE** and **EE**, which contain the internal edges and external edges, respectively. For each unit structure and each of its possible RV layout cases, we generate a vertex $(id, case) \in V$. Here *id* and *case* refer to the unit structure id and one of its possible RV layout cases, respectively. In our experiments, we can have up to 16 vertices for a unit structure, according to the RV cases as we discussed in Table 6.2. An edge is introduced if and only if the two corresponding vertices are conflict with each other. In other words, if two vertices are connected by an edge, we can choose only one of them as the final solution. If both cases are with the same id, this edge belongs to internal edges IE. Otherwise, two vertices are from the different unit structures, and this edge belongs to external edges EE.

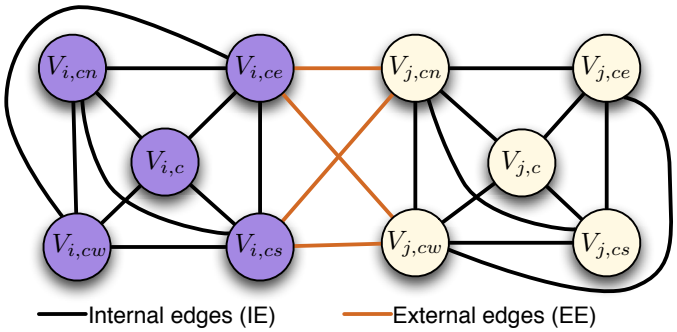


Figure 6.8: Example of a conflict graph.

It shall be noted that for one unit structure, any two cases would be connected by one internal edge.

Figure 6.8 illustrates an example conflict graph with two unit structures i and j. Each unit structure has five cases, and there are totally four external edges. During conflict graph construction, to save search space, we use *bins* to limit the neighbor search space. Bins are big grids in the x-y plane, and we check conflicts in the current and neighboring bins only while checking the conflicts. In our algorithm, a single via case c is assigned as one of the RV cases. In case of a vertex having an external edge with neighboring single via case, the vertex should not be selected. Therefore, during conflict graph construction, we prune edges and vertices that have external conflicts with single via case. Table 6.4 shows an example of pruning process to prevent zero-via cases. In the example, $(3, cs)$ should not be selected because it has an external edge with neighboring single via, $(1, c)$ case. So we remove $(3, cs)$ from the V. In the set of edges, all the edges connecting to $(3, c)$ are now obsolete, thus they need to be removed. In this example, an edge $((2, c), (2, cn))$ is not

pruned, because it is an internal edge originated from the same unit structure id.

Table 6.4: Example of conflict edge pruning.

Before pruning		After pruning	
Vertices	Edges	Vertices	Edges
(1,c)	((1,c),(3,cs))	(1,c)	–
(3,cs)	((2,cn),(4,cww))	–	((2,cn),(4,cww))
(2,cn)	((1,c),(1,cs))	(2,cn)	((1,c),(1,cs))
(4,cww)	((1,c),(1,cn))	(4,cww)	((1,c),(1,cn))
(1,cs)	((5,cne),(3,cs))	(1,cs)	–
(1,cn)	((3,c),(3,cs))	(1,cn)	–
(5,cne)	((2,c),(2,cn))	(5,cne)	((2,c),(2,cn))
(3,c)		(3,c)	
(2,cn)		(2,cn)	

6.4.3 ILP Formulation

The EM-aware redundant via insertion is formulated as an integer linear programming (ILP).

$$\begin{aligned} &\text{Max} \sum_{(id,case)\in V} PIR_{(id,case)} \cdot R_{(\text{id,case})} \\ &\text{s.t.} R_{(id,case)} + R_{(id,case')} = 1, \forall((id,case),(id,case')) \in IE \\ &R_{(id,case)} + R_{(id',case')} = 1, \forall((id,case),(id',case')) \in EE \end{aligned} \tag{6.3}$$

where the objective is to maximize the benefit of redundancy on the potential improvement ratio of lifetime as we defined in Eqn. (6.2). Since we have already limited over-inserting redundant vias by adjusting PIR to 0 in Eqn. (6.2), we can just focus on maximizing PIR in this step. We represent the possible redundant via insertions using a binary variable $R_{(id,case)}$, and id and

case represent unit structure id and redundant via position case, respectively. $R_{(id,case)} = 1$ indicates that vertex $(id, case)$ is selected for the design. The constraints are based on both the internal edges and the external edges in the conflict graph.

6.4.4 Maximizing Vias After EM-optimization

From the design for manufacturing (DFM) perspective, it is always good to have more redundant vias, to increase yield. Thus [35] focused on maximizing the total number of redundant vias. Since the first priority in our work is to improve EM so that the lifetime can be longer than the threshold, we may achieve that goal with smaller number of redundant vias than the conventional DFM-aware RV insertion, because we do not *over-insert* RVs for the safe enough unit structures. However, if we put smaller number of redundant vias than the DFM-aware RV insertion, that may be bad for yield, although it can be good enough for EM. Thus, to increase yield, which is our second goal, we suggest a post via insertion technique to maximize the number of vias *after* the initial EM-aware via insertion of Section 6.4.3. The basic idea is to insert as many as possible additional vias on top of the EM-aware optimized RV solution. By this way, we can achieve both EM-awareness and yield improvement.

6.5 Speed-Up Techniques

For practical design, solving ILP may suffer from runtime overhead problem. In this section we present several techniques to speed-up the expensive ILP. The main idea is that instead of solving the whole conflict graph, we can divide the whole graph into a set of components. Then each component can be solved independently.

6.5.1 Simplified Conflict Graph

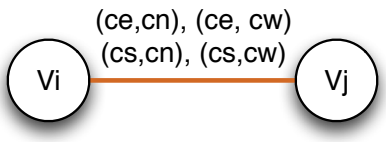


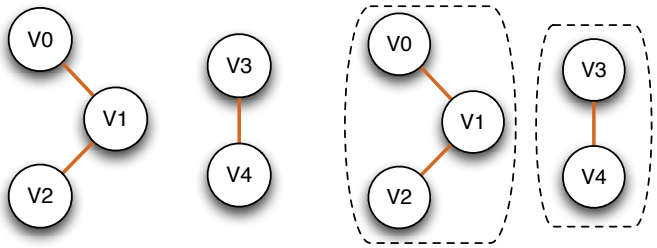
Figure 6.9: Simplified conflict graph.

To provide more flexibilities to achieve further speed-up, we introduce a simplified conflict graph model. For the initial conflict graph in Figure 6.8, the corresponding simplified conflict graph is illustrated in Figure 6.9. It shall be noted in the simplified graph, to connect two via units, some hyper edges would be introduced. The motivation of the simplified conflict graph is twofold: 1) In the simplified conflict graph only external conflict edges are maintained, thus the graph size can be significantly reduced. For example, instead of 24 edges in initial graph in Figure 6.8, only one edge is left in simplified conflict graph. 2) Due to the simplification, more articulation points can be identified. More discussion regarding the articulation point detection appears in Section 6.5.3. Based on simplified conflict graph, we introduce two techniques to further

divide and simplify the graph.

6.5.2 Independent Component Computation

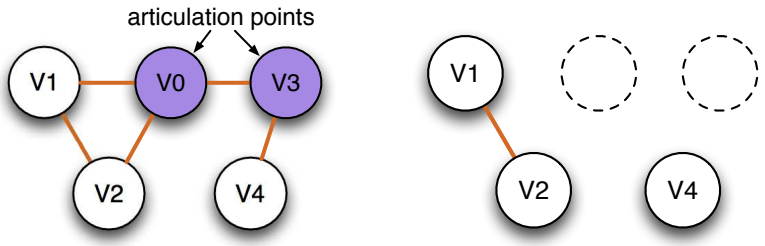
Our first technique is called *independent component computation*, similar to that of the work [35]. In a conflict graph of real design, we observe many isolated subgraphs. By breaking down the whole conflict graph into several independent components, we partition the initial graph into several small components or subgraphs. Since no edge exists between any two components, the redundant via insertion problem can be solved independently for each component, and the final solution can be obtained by taking the union of sub-solutions.



(a) (b)

Figure 6.10: Example of the independent component computation.

Figure 6.10 illustrates one example of independent computation computation. Given the conflict graph, we can detect two independent components, and can apply ILP formulation to solve them separately. All the components can be calculated in linear time $O(|V|+|E|)$, where $|V|$ and $|E|$ are the vertex number and the edge number, respectively.



(a) (b)

Figure 6.11: Example of the articulation point computation.

6.5.3 Articulation Point Computation

Our second technique is called *articulation point computation*. In the conflict graph, a vertex is an articulation point if and only if removing it (and edges through it) disconnects the graph into two or several components. For example, as illustrated in Figure 6.11 (a), in the conflict graph vertices $v0$ and $v3$ are articulation points, since removing either of them would divide the whole conflict graph into two components. In our simplified conflict graph, each vertex represents one via unit. For each articulation point, we apply a process to check whether one redundant via case can be pre-selected. If yes, then the vertex would be temporally removed from conflict graph, and the conflict graph can be divided. To the best of our knowledge, this study is the first one to introduce articulation point computation to redundant via insertion; this method can be only applied to the redundant vias with different costs (e.g. failure time) because we need to pre-select the via case based on that.

To find all articulation points in a conflict graph, we apply a depth-first search (DFS) algorithm presented by Tarjan [66]. Note that all articulation

points can be detected during only one DFS in linear time $O(|V|+|E|)$, where $|V|$ and $|E|$ are respectively the number of vertices and the number of edges in a conflict graph.

6.6 EM-aware Redundant Via Optimization Results

We implement our algorithm in Python and C++ languages. All the experiments are performed on a 2.93GHz Intel Quad Core Linux Machine. For benchmark generation, Design Compiler [3] is applied to synthesize OpenSPARC T1 designs based on Nangate 45nm standard cell library [2]. We choose GUROBI [1] as the ILP solver. As we mentioned in Section 6.2, we use the unit structure to count the EM-violations. Temperature is assumed to be $150°C$ and the initial current density of the wire in each unit structure is randomly chosen between $1e8$ and $3e9[A/m^2]$. We set the temperature higher than the most of the normal conditions to accelerate the EM failure, similar to that of oven test of fabricated chips. Thus the failure time in our results may be shorter than that of normal temperature. In EM-aware modes, we limit the insertion of redundant via when the system is robust enough, by setting α as 1.5 from the Eqn. (6.2).

Table 6.5 shows our experiment results that compare with our proposed method (EM-RV) against the conventional RV insertion. We limit the maximum number of total vias of a unit structure to four in our experiments, for both conventional RV mode and EM-RV modes. In the conventional RV mode, we put as many as possible, similar to the approach in Work [35]. Here

Table 6.5: EM-aware via insertion results.

Ckts	Mode	# Unit	# Failed Unit	# Via	WNΔTf	TNΔTf	runtime
alu	conventional RV	5661	2746 (48.51 %)	21346	-1.80e+08	-2.31e+11	2.9s
	EM-RV	5661	942 (16.64 %)	14480	-1.46e+08	-2.33e+10	2.5s
	EM-RV(SpeedUp)	5661	953 (16.83 %)	14398	-1.53e+08	-2.52e+10	0.9s
	EM-RV(SpeedUp+MaxVia)	5661	625 (11.04 %)	21056	-1.53e+08	-1.52e+10	0.9s
byp	conventional RV	24383	11863 (48.65 %)	90166	-1.90e+08	-1.01e+12	19.8s
	EM-RV	24383	4370 (17.92 %)	61275	-1.52e+08	-1.19e+11	14.8s
	EM-RV(SpeedUp)	24383	4402 (18.05 %)	60650	-1.54e+08	-1.36e+11	5.1s
	EM-RV(SpeedUp+MaxVia)	24383	2788 (11.43 %)	88280	-1.54e+08	-8.24e+10	5.3s
div	conventional RV	11635	5574 (47.91 %)	43807	-1.86e+08	-4.64e+11	6.1s
	EM-RV	11635	1896 (16.30 %)	29570	-9.99e+07	-4.57e+10	5.1s
	EM-RV(SpeedUp)	11635	1895 (16.29 %)	29364	-1.54e+08	-5.03e+10	1.9s
	EM-RV(SpeedUp+MaxVia)	11635	1202 (10.33 %)	43146	-1.54e+08	-2.95e+10	2.0s
ecc	conventional RV	4068	1943 (47.76 %)	15470	-1.72e+08	-1.64e+11	1.7s
	EM-RV	4068	651 (16.00 %)	10488	-9.70e+07	-1.47e+10	1.5s
	EM-RV(SpeedUp)	4068	655 (16.10 %)	10432	-1.52e+08	-1.61e+10	0.5s
	EM-RV(SpeedUp+MaxVia)	4068	432 (10.62 %)	15295	-1.52e+08	-9.60e+09	0.5s
efc	conventional RV	3130	1489 (47.57 %)	11977	-1.72e+08	-1.24e+11	1.2s
	EM-RV	3130	466 (14.89 %)	8072	-9.34e+07	-1.05e+10	1.0s
	EM-RV(SpeedUp)	3130	473 (15.11 %)	8020	-1.53e+08	-1.12e+10	0.4s
	EM-RV(SpeedUp+MaxVia)	3130	313 (10.00 %)	11858	-1.53e+08	-6.83e+09	0.4s
ffu	conventional RV	5078	2421 (47.68 %)	19347	-1.88e+08	-2.02e+11	2.1s
	EM-RV	5078	807 (15.89 %)	13054	-9.50e+07	-1.79e+10	1.8s
	EM-RV(SpeedUp)	5078	803 (15.81 %)	12987	-1.50e+08	-1.93e+10	0.7s
	EM-RV(SpeedUp+MaxVia)	5078	526 (10.36 %)	19140	-1.50e+08	-1.17e+10	0.7s
mul	conventional RV	44085	20891 (47.39 %)	165912	-1.83e+08	-1.77e+12	29.2s
	EM-RV	44085	7522 (17.06 %)	111381	-1.50e+08	-1.81e+11	19.8s
	EM-RV(SpeedUp)	44085	7526 (17.07 %)	110671	-1.54e+08	-1.99e+11	7.3s
	EM-RV(SpeedUp+MaxVia)	44085	4816 (10.92 %)	163443	-1.54e+08	-1.18e+11	7.6s

the target is to maximize the total number of vias. In EM-RV, we follow the steps described in Section 6.4.1 to 6.4.3, mainly targeting to improve EM lifetime. In this way, we can compare conventional redundant via insertion to our EM-aware one. To clearly see the effect of EM-awareness, we use parameter ΔTf as we defined in Eqn. (6.4).

$$\Delta Tf_{(id,case)} = Tf_{(id,case)} - Tf_{th} \tag{6.4}$$

If ΔTf is positive, it indicates that the unit structure is EM-safe, and

otherwise it is EM-failed. We also check the worst negative (WN) ΔTf and total negative (TN) ΔTf as metrics of EM-violation. In our experiments, we use $Tf_{th} = 2e8$ seconds.

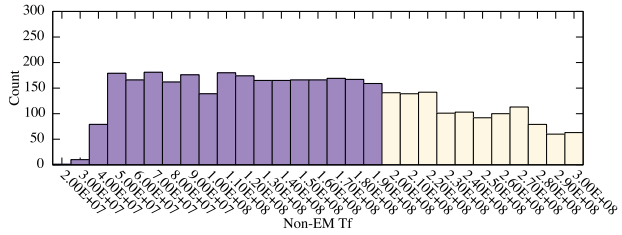
In Table 6.5, we show that our proposed EM-aware redundant via insertion can reduce the number of failed unit, as well as WNΔTf and TNΔTf. For example, with *alu* design, EM-RV shows 942 failed unit structures while conventional RV mode has 2746. Since we insert redundant vias only to the EM-prone nets to satisfy the lifetime criteria, we can achieve better EM reliability with smaller number of total vias (14480 vs. 21346). On the other hand, in case of conventional RV mode, because the goal is to maximize the total number of redundant vias, EM-prone nets may not be selected to insert more redundant vias, and EM-safe nets can have more unnecessary vias in terms of EM.

The runtime of ILP can be a problem if the problem size is huge. Thus we apply speed-up techniques as we discussed in Section 6.5, for EM-RV(SpeedUp) mode. In case of *alu*, now the number of failed units are increased a little bit than the EM mode, but we achieve much faster runtime compared to EM mode. With *articulation point computation* described in Section 6.5.3, we divide a conflict graph into subgraphs to achieve faster runtime. The penalty of smaller runtime is loosing the optimality, however, because our method can utilize different PIR costs of vertices during resizing graphs, the amount of EM degradation between EM-RV and EM-RV(SpeedUp) is very small. For example, in terms of number of failed unit of *alu*, there are 942

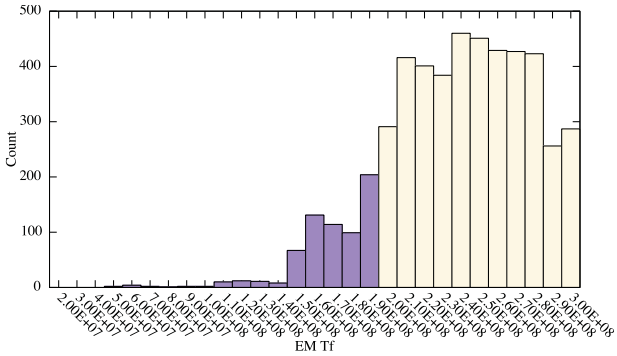
units in EM-RV mode and 953 in EM-RV(SpeedUp) mode.

Since we prevent to insert excessive vias for case with long enough lifetime by Eqn. (6.2), we can have room to improve EM by putting more redundant vias. Hence we maximize the number of vias *after EM-RV(SpeedUp)*, as discussed in Section 6.4.4. The result appears in EM-RV(SpeedUp+MaxVia) mode in the table. We note that this second step of maximizing the via number is not only useful for the EM, but also beneficial to yield during manufacturing. Because our first goal is improving EM and the second one is maximizing the via numbers, the total number of vias with EM-RV(SpeedUp+MaxVia) mode is little bit less than the conventional RV mode. In terms of EM, we have similar WNΔTf for EM-RV(SpeedUp) and EM-RV(SpeedUp + MaxVia), but even more improved results for the number of failed units and TNΔTf. It means that the suggested two-step EM-aware redundant via insertion can achieve much better EM reliability than conventional RV mode, with little sacrifice of yield.

Figure 6.12 shows the effect of the EM-aware redundant via for one of our target circuit designs,*alu*; upper figure shows conventional RV mode, and the lower one represents EM-RV(SpeedUp+MaxVia) mode. Here x axis is lifetime (or EM failure time), and y axis is the count of unit structures. As shown with blue-violet bars, EM-aware via insertion can significantly reduce unit structures vulnerable to EM, compared to the conventional RV insertion method. The benefit mostly comes from insertion of additional vias for the EM-prone nets first. Also as we explained in Section 6.3, our method chooses



(a)



(b)

Figure 6.12: Histograms with EM failure time of alu; (a) with conventional RV mode and (b) EM-RV(SpeedUp+MaxVia) mode.

the EM-optimal cases out of the cases with the same redundancy, and it helps avoid some worse choices, especially in a congested area.

6.7 Summary

With advanced manufacturing technology, reliability becomes one of the most important issues that requires careful planning. In this work, we suggest a design methodology to enhance EM-robustness.

Our modeling of EM with diverse layouts of redundant vias shows that the current imbalance in different vias of a unit structure affects the reliability.

We suggest that off-track via layouts could be preferable in terms of EM, deviating from the previously conventional view of redundant via insertion.

We also propose a post-layout optimization method that can improve the EM reliability of redundant vias by exploiting the diverse design space of them, such as the via placement or the number of vias. Because the suggested method inserts the right amount of redundant vias for the EM-risky nets first to satisfy the target failure time, we can achieve much better EM reliability than the conventional redundant via insertion technique. To reduce runtime of solving ILP, we investigate a set of speed-up techniques. Also, by maximizing the total number of vias after the initial EM-aware redundant via insertion, we achieve not only better EM, but also better yield during manufacturing.

Our results suggest that even with the similar number of total redundant vias as the conventional method, we can achieve better EM reliability by smart allocation of vias. Because EM problems are getting severe with smaller interconnect dimensions, we expect that the EM-aware via insertion would have more importance in the future.

Chapter 7

Conclusion

With advanced manufacturing technology, reliability becomes a limited resource that requires careful planning. This dissertation proposes efficient and accurate EM modeling methods for various interconnect structures, and applies the suggested EM models to optimize IC layout.

First, in Chapter 2, modeling of EM for TSV structures is proposed. Due to the intrinsic thermo-mechanical stress during TSV manufacturing, mechanical stress appears around the TSVs, and the TSV-induced stress can play an important role in the EM-robustness of TSV.

For wire structures, Chapter 3 models a wire as a one-dimensional structure, and solves partial differential equations for it using finite-element-analysis (FEA) to achieve failure time. With simplified input factors, an look-up table (LUT)-based EM model is suggested, to instantly get the EM lifetime of the wire with certain values for current, temperature and stress. Because the LUTs stores pre-simulated the EM-related lifetime of wires in different conditions, it is possible to detect the EM-hot spots for full-chip level design with manageable run time. Specifically, the suggested modeling approach turns out to be more efficient under stress impact, such as at the neighbor of

TSV structures in 3D ICs.

By applying the EM-modeling approaches, Chapter 4 suggests full-chip scale layout optimization, such as EM-aware routing. EM-aware routing includes two parts, 1) EM-aware net ordering for a global routing stage, and 2) EM-aware detailed maze routing. The net ordering part uses the prediction of failure time of the estimated routing path, so that EM-critical nets can be routed earlier than non-critical nets. During the detailed routing stage, based on the EM cost of each grid, the suggested routing scheme automatically finds the paths to satisfy both the EM lifetime criteria and routing resources.

Chapter 5 further investigates the interplay between TSV and local vias in the multi-scale via (MSV) structures for power/ground nets. The relationship between EM and various factors are studied in this chapter, such as the condition of nucleated voids, material property, and the trade-offs between local via sizes and number of local vias from an EM reliability perspective. The modeling uses look-up tables (LUTs) for resistance change with different void conditions, and it is possible to estimate the resistance increase due to EM-induced voids during a certain time period, fast and accurately. Based on EM model for a single MSV, this chapter suggests a flow to study transient IR-drop of full-chip level 3D PDNs with MSVs, and evinces that the initial void condition, current density and temperature can affect IR-drop of chip-level 3D PDNs.

Chapter 6 models EM of redundant via structures in the advanced technology nodes. First, it shows that off-track via layouts can be prefer-

able in terms of EM. This finding suggests that more constraints on reliability could affect some conventional design principles, and those principles should be reevaluated under more stringent reliability constraints. Based on the investigation regarding EM of redundant via structures, a post-layout optimization method is proposed which can enhance the EM reliability of redundant vias, by selecting more EM-robust redundant via layouts within limited routing resources.

Throughout these studies, it is found that a good EM reliability model can enhance the robustness of the system. To be more specific, if the physical design resources can be allocated within a manageable design time with the good EM model, the EM reliability of a design can be under control. The future challenges of this work can be 1) improving the accuracy of the models, 2) collecting the right information of input factors, such as current density, temperature, and stress information, and 3) co-optimization with the traditional design constraints such as timing and power. As EM can be a very important reliability issue in both 3D IC technology and advanced technology nodes, this dissertation can be helpful for EM-aware physical design in the near future.

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Vita

Jiwoo Pak was born in Daejeon, South Korea in June 1984. She received a Bachelor of Science degree and Master of Science degree in Electrical Engineering from Korea Advanced Institute of Science and Technology (KAIST), in 2007 and 2009, respectively, in South Korea. The thesis title for her master's degree was "Impact of Noise Isolation Design of SiP on Performance of T-DMB communication system". She started her Ph.D. program at the University of Texas (UT) at Austin in 2009, with research advisor David Z. Pan.

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