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Design, Fabrication and Characterization of Field-Effect Transistors Based on Two-dimensional Materials and Their Circuit Applications

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Design, Fabrication and Characterization of Field-Effect Transistors Based on Two-dimensional Materials and Their Circuit Applications

by

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Dedication

To my parents, wife and daughter

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Design, Fabrication and Characterization of Field-Effect Transistors Based on Two-dimensional Materials and Their Circuit Applications

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The field of two-dimensional layered materials has witnessed extensive research activities during the past decade, which commenced with the seminal work of isolating graphene from bulk graphite. In addition to providing a rich playground for scientific experiments, graphene has soon become a material of technological interest for many of its fascinating electrical, thermal, mechanical and optical properties. The controllability of carrier density with electric field in graphene, along with very high carrier mobility and saturation velocity, has motivated the use of graphene channel in field-effect devices. Also, the two-dimensional layered materials family has grown very rapidly with the application of the graphene exfoliation technique and many of these elemental and compound materials are considered useful for transistor applications.

In this work, various aspects of the use of two-dimensional layered materials for transistor applications were analyzed. Starting with material synthesis, field-effect transistors (FETs) were designed, fabricated and tested for their DC and high frequency performances. Through the detailed electrical and spectroscopic investigations of several processing techniques for enhanced FET performance, numerous insights were obtained into the FET operation and performance bottlenecks. The reduction of charged impurity

scattering in graphene FET by Hexamethyldisilazane interaction improved field-effect mobility and reduced residual carrier concentration. This technique was also shown to be promising for other two-dimensional materials based FET. A useful technique for reducing the thickness of black phosphorus flake with oxygen plasma etching was developed. Both back-gated and top-gated FETs were implemented with good performances. Secondary ion mass spectroscopy and x-ray photoelectron spectroscopy revealed vital structural information about layered black phosphorus. Lastly, these exotic materials based FETs were characterized for their high frequency performance, resulting in gigahertz range transit frequency and operated in a variety of important circuit configurations such as frequency multiplier, amplifier, mixer and AM demodulator.

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Chapter 1: Introduction

1.1 Motivation

Computing and electronics have been playing an ever increasing role in the advancement of civilization for the past fifty years. The semiconductor industry has been consistently delivering innovative products and solutions with ever increasing functionalities and reduced cost by keeping pace with the famous Moore's law, which dictates that the transistor count in a chip doubles every 18-24 months.[1] The sustenance of this rapid progression has largely been enabled by making silicon based transistors smaller, faster and power efficient. Performance and density improvements had been accomplished by classical geometric scaling according to Dennard's law till the beginning of this millennium and recently, several additional technological breakthroughs such as strained channel, high κ – metal gate, FinFETs etc. have been employed.[2] However, with device dimensions approaching sub-10 nm and device operation hitting fundamental physical and quantum mechanical barriers, researchers have been rigorously deliberating at alternative materials, devices and architectures to deliver exciting new systems with unprecedented functionality and performance.

Two-dimensional layered materials have recently gained enormous interest for transistor applications, which were initially motivated by the ultrahigh carrier mobility and ultimate thickness scalability of graphene.[3] Within a few years, the number of two-dimensional materials has literally exploded with various elemental and compound materials such as MX_2 (M = Mo, W etc. and X = S, Se, Te etc.), silicene, phosphorene etc., among others. The family of two-dimensional materials is a rich one with diverse properties and field-effect transistors (FETs) have been demonstrated with many of its members.

Although these FETs are at their nascent stage in the research labs at present, they are envisioned to be widely integrated into future electronic systems in varying capacities. One long term goal is to use the best suitable material / materials combination as a replacement of silicon for beyond CMOS device applications. In reality, this seems to be a distant goal due to the inertia of the multibillion dollar Silicon industry dominated by digital applications and other comparatively matured candidates, such as III-V materials and germanium, in queue. Heterogeneous integration of these materials and FETs with existing CMOS to deliver enhanced functionality is a more promising application. While digital applications almost exclusively use silicon, analog/mixed signal systems use variety of materials and devices and they are more open towards new technologies.[3] Several two-dimensional materials show excellent high frequency performance. For example, ~500 GHz cut off frequency for graphene FET has already been demonstrated with projected performance in the terahertz frequency range.[4] One of the greatest promises of these FETs lies in the area of flexible and wearable electronics due to their superior electrical and mechanical properties compared to their existing counterparts.[5]

In summary, the initial results with two-dimensional materials based FETs show substantial promises and a variety of prospective applications have been identified. However, in order to fully realize the potential of these materials and their FETs, it is imperative to thoroughly understand their operating mechanisms and performance limiting factors and also develop processing technology solutions to mitigate these factors. To this end, several important issues of technological importance regarding two-dimensional materials based FETs are addressed in this dissertation through the design, fabrication and characterization of these FETs and their circuit applications.

1.2 Outline

This dissertation is organized as follows.

In chapter 2, a wet transfer procedure for large area, CVD grown graphene is described and several observations are made to improve the quality of the process.

In chapter 3, a performance enhancement technique is reported for graphene FETs with Hexamethyldisilazane (HMDS) treatment. Room temperature electrical characteristics with statistical distribution of performance metrics and low temperature transport characteristics are analyzed with and without HMDS treatment. Raman spectroscopic analysis data are presented in support of proposed performance enhancement mechanism. This technique is extended to MoS_2 devices as well.

An Oxygen (O_2) plasma etching process for black phosphorus flake thickness reduction is presented in chapter 4. After detailed optical and atomic force microscopy (AFM) analysis of the flake thinning process, its impact on electrical characteristics are analyzed by characterizing back-gated and top-gated transistors fabricated with plasma processed flakes. To assess the chemical impact of the flake thinning process, Raman spectroscopy, secondary ion mass spectroscopy and X-ray photoelectron spectroscopy analyses are presented.

The high frequency performance of graphene and black phosphorus based FETs fabricated in GSG structures are investigated in chapter 5. After initial DC characterization, transit or cut-off frequencies are measured for these devices. Useful circuit operations are demonstrated using these devices as well.

Finally, the key results of the above mentioned works are summarized in chapter 6 and suggestions for future works are presented based on these results.

Chapter 2: CVD Graphene Transfer to Arbitrary Substrates

Graphene, a single layer of sp^2 bonded carbon atoms arranged in two-dimensional honeycomb lattice, has been regarded as the wonder material of 21st century for its exceptional electronic, thermal, mechanical and optical properties.[6–10] Extremely high charge carrier mobilities, high saturation velocity, high current carrying capacity etc. have made graphene a material of great interest for electronic applications.[11,12] Graphene was first isolated from bulk graphite crystal using scotch tape based exfoliation technique and it has remained a popular method for obtaining pristine, high quality crystals.[6] Typically small graphene flakes of few tens of micrometers in size are produced by this method. While these flakes are sufficiently big for scientific research and proof of concept device demonstrations, commercial and technological applications require large area graphene films with a quality comparable to exfoliated flakes.

One successful and widespread pathway to large area graphene is growth via chemical vapor deposition (CVD) on metallic substrates such as copper, nickel etc. However, in order to make field-effect transistors (FET), this large area graphene needs to be transferred to desired insulating substrate with minimal degradations. In this chapter, a wet transfer method of CVD grown graphene to arbitrary substrate is developed. The transfer process is illustrated in Figure 2.1 and optimized based on the structural and electrical qualities of transferred graphene.

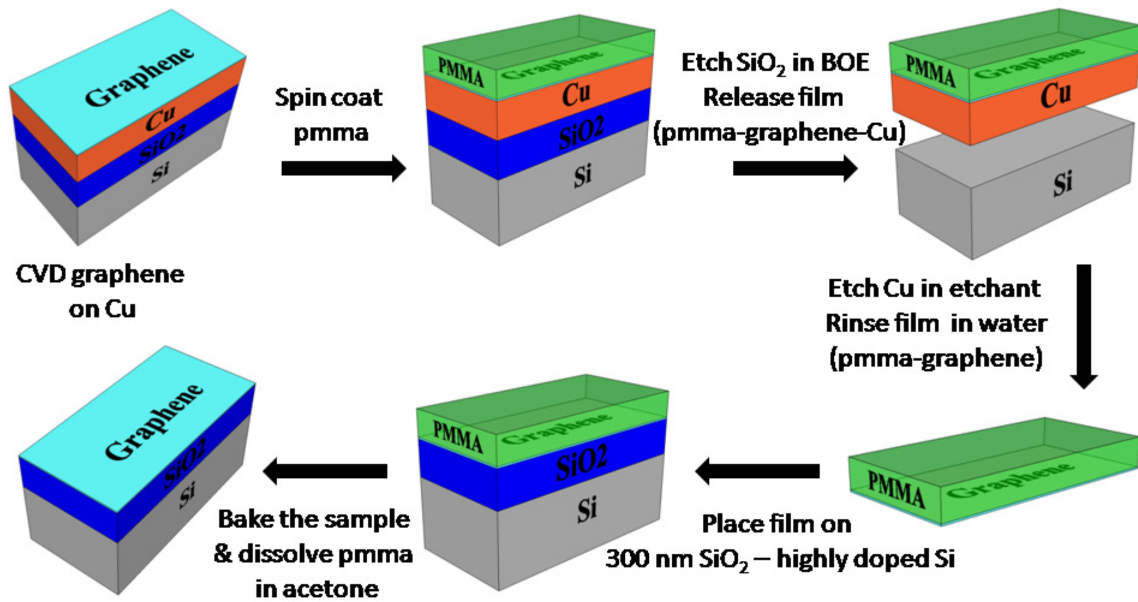

Figure 2.1: Process steps for transferring CVD grown graphene.

2.1 Process Steps for Graphene Transfer

- Monolayer graphene is grown by CVD on a 1µm thick copper (Cu) film evaporated on top of 300 nm thick SiO_2, thermally grown on a Si substrate.[13]
- The transfer process begins by spin coating PMMA on the growth substrate (graphene-Cu-SiO_2-Si). The sample is left in a desiccator overnight in order to drive off solvent.
- The sample is then immersed in 6:1 buffered oxide etch (BOE) to etch the SiO_2 which leaves PMMA-graphene-Cu film detached from the growth substrate. A piece of clean Si is placed at an inclined angle in the BOE solution to gently take the film out of the solution and rinse it with Di-Ionized (DI) water.
- The PMMA-graphene-Cu film is then placed in 10:1 H_20 : Ammonium Persulfate (APS-100, Transene INC.) solution to etch Cu. After Cu is completely etched

within ~10 minutes, the clean Si is used to take the floating PMMA-graphene film from etchant solution and rinse it in DI water several times. Finally, the target substrate (300 nm SiO_2 – highly doped Si or any other arbitrary substrate) is partially immersed in DI water at an inclined angle to place the PMMA-graphene film on the substrate.

- The substrate is left in desiccator box for several hours. After the sample has dried and PMMA-graphene film is visibly lying dry and flat on the substrate, the sample is heated at 130°C for 2-3 minutes on a hotplate in order to remove remaining moisture and improve the adhesion between the film and substrate.
- The sample is left in acetone for several hours to remove the PMMA on top of graphene. Finally, the sample is rinsed with Isopropyl Alcohol (IPA) and blown dry with nitrogen which leaves graphene on SiO_2-Si substrate.

Figure 2.2(a) shows an optical image of graphene transferred on SiO_2-Si which demonstrates successful transfer of large area, smooth graphene with very few cracks and tears. Raman spectroscopy is a versatile tool graphene characterization.[14] A representative Raman spectrum of transferred graphene with characteristic peaks is shown in Figure 2.2(b). Negligible defect peak intensity at ~1350 cm^{-1}, a narrow (~32 cm^{-1}) 2D peak at 2680 cm^{-1} and modest intensity ratio (~ 2) between 2D and G (at ~1590 cm^{-1}) peaks demonstrate high quality of transferred graphene film.

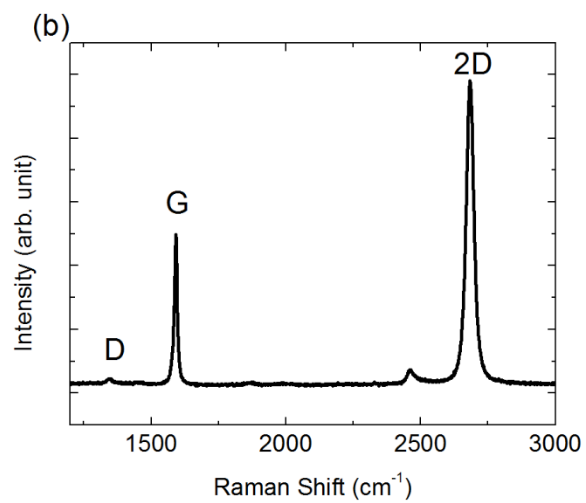

Figure 2.2: (a) Graphene transferred on 300 nm SiO_2-Si substrate. Scale bar is 10 µm. (b) Representative Raman spectrum from the sample showing high quality graphene.

2.2 Empirical Observations

We can make several empirical observations based on numerous transfer runs spanning over few years.

- The concentration of PMMA used for the transfer process impacts the final graphene quality. Higher concentration PMMA leaves more residues after removal in acetone compared to lower concentration PMMA. On the other hand, higher concentration PMMA results in higher thickness which makes the manual transfer process more robust. This observation has been reported in literature.[15]
- It should be mentioned that the transfer process described above is a two-step transfer process: SiO_2 on the growth substrate is etched first in BOE, and then Cu is etched in dilute Cu etchant. It is possible to put the growth substrate directly in as supplied Cu etchant. However, Cu etching and the release of PMMA-graphene film takes several hours in this case and graphene is immersed in Cu etchant for the whole time period. This results in degraded graphene quality which shows up in the poor electrical characteristics and Raman spectra.
- The PMMA baking temperature after PMMA-graphene film has dried on target substrate seems to have important effect. Baking is necessary to improve the adhesion between the film and substrate. Also, baking the sample above the glass transition temperature (T_g) of PMMA (95-100°C) results in PMMA reflow which smoothens the film. However, baking at high temperature also leaves more residues after PMMA removal in acetone. Considering this aspect, we have chosen to bake the sample at 130°C, slightly above the T_g of PMMA.
- Careful and proper rinsing of PMMA-graphene film in DI water after Cu etching is crucial to avoid defective and doped graphene with lower mobility.

Chapter 3: Transistor Performance Improvement by Surface Treatment

Since its isolation, graphene has triggered a tremendous amount of interest for its exceptional electronic properties making it potentially interesting as a channel material for field-effect transistors (FET), especially for analog and RF applications.[16–19] Among other things, carrier mobility is an important performance metric for FET application. FETs made by suspending graphene have reached mobility values in excess of ~ 200,000 cm^2/Vs under high vacuum and low temperature condition revealing the intrinsically high mobility of charge carriers in graphene.[11] The use of hexagonal boron nitride (h-BN) as a substrate for graphene FET has yielded mobility values comparable to this under similar conditions.[20] However, the current prospect of h-BN is limited by the challenge of growing large area, high quality films with controllable thickness. The most practical and technologically viable substrate is still the widely used SiO_2/Si.[a]

Typical room temperature mobility values for graphene devices fabricated on SiO_2 are below or around 10,000 cm^2/Vs.[21] Various intrinsic and extrinsic performance limiting factors for graphene FETs have been identified.[22,23] In graphene, optical phonon energies are too high to participate at room temperature. Carrier interaction with graphene's acoustic phonon and remote interfacial phonon scattering by SiO_2 optical phonons indicate room temperature mobility upper limits of ~200,000 and ~ 40,000 cm^2/Vs respectively, which are still very high compared to experimentally achieved mobility values for graphene devices. Coulomb scattering from impurities has been largely accepted to be the dominant scattering mechanism for experimental graphene FETs at room temperature. Hence, minimizing impurity scattering is a matter of

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[a] Part of this chapter is reprinted with permission from [Sk. F. Chowdhury, S. Sonde, S. Rahimi, L. Tao, S. Banerjee, and D. Akinwande, "Improvement of graphene field-effect transistors by hexamethyldisilazane surface treatment", *Applied Physics Letters*, vol. 105, no. 3, 2014.]. Copyright 2014, AIP Publishing LLC.

substantial importance for high performance graphene FET. One widely used approach is to passivate the graphene surface with different organic or inorganic materials, which enhance the electrostatic characteristics.[15,24,25]

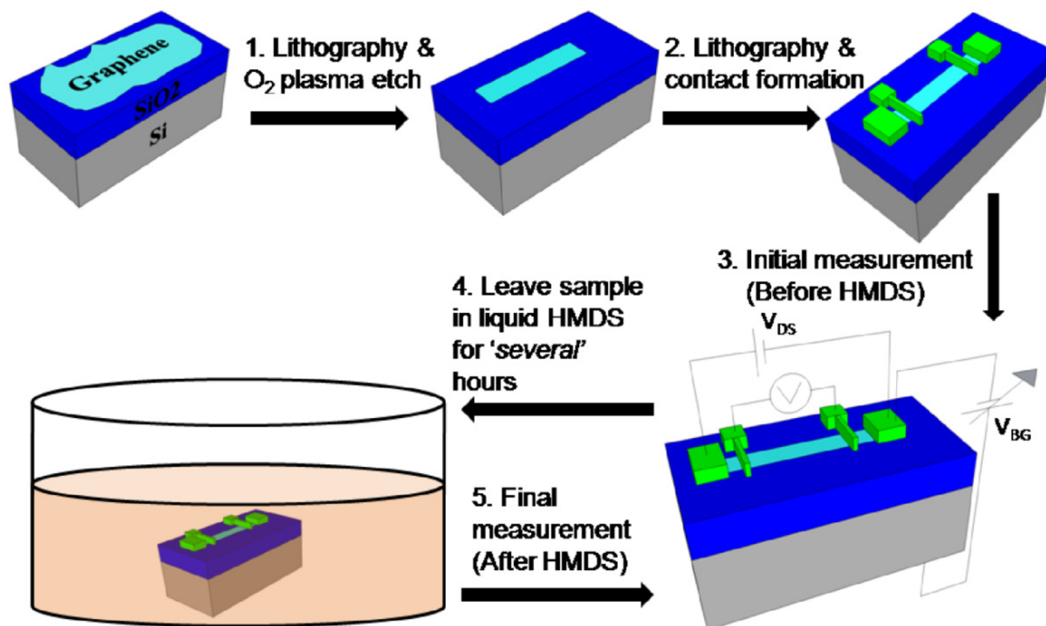
In this work, we report the improvement of graphene FET characteristics by treating the graphene surface with hexamethyldisilazane ($NH(Si(CH_3)_3)_2$), commonly known as HMDS.[26] One unique aspect of HMDS compared with many other passivation layers is that it can react with the surface of SiO_2 to form a self-assembled monolayer and transform the hydrophilic surface to hydrophobic.[27] It should be mentioned here that HMDS has been previously used to construct hydrophobic SiO_2 surface before graphene exfoliation, which makes the graphene-SiO_2 interface free of adsorbed water.[28] Our approach is unique because we apply HMDS on graphene rather than SiO_2, thus taking care of the adsorbed impurities on the top surface of graphene after device fabrication, which is not possible by the previous approach. Also in our case, we expect the HMDS molecules to form an adsorbed layer or clusters. But in the SiO_2 surface treatment method, HMDS molecules actually react with the silanol groups on SiO_2 surface. As will be discussed later, we applied HMDS on the top surface of graphene FETs fabricated on a HMDS treated, hydrophobic SiO_2 substrate and also observed improvement in characteristics. Hence these two techniques are different and, in principle, both of them should be combined for best performance improvement.

3.1 Device Fabrication and Measurement Procedure

Figure 3.1(a) shows the fabrication steps and measurement procedure for our experiment. We start with CVD grown graphene transferred on 300 nm SiO_2 - highly doped Si substrate, as described in chapter 2. Clean, continuous device active regions

were patterned using electron beam lithography and subsequent oxygen plasma etching. Contacts to active region were defined by electron beam lithography, electron beam

(a)



(b)

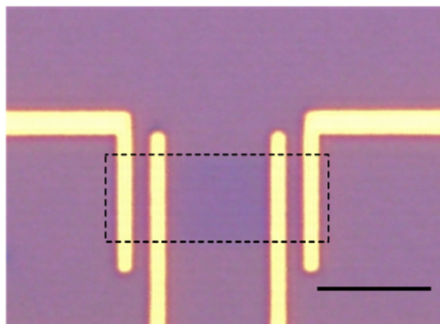


Figure 3.1: (a) Fabrication steps and measurement procedure for HMDS surface treatment method. (b) Optical image of a fabricated back-gated graphene FET with four contacts. Patterned graphene area is outlined with dashed line. Scale bar is 5 μm.

evaporation of Ti-Au metal stack (typically 1nm Ti - 49 nm Au) and liftoff. This completed the fabrication of back-gated field-effect transistors (BGFET) with four contacts where the highly doped Si and 300 nm SiO_2 acted as gate terminal and gate oxide, respectively. After initial measurement, the BGFET samples were immersed in liquid HMDS for several hours. Samples were then taken out of HMDS and dried in air. Figure 3.1(b) shows an optical micrograph of a fabricated BGFET.

3.2 Room Temperature Electrical Transport

The resistance of a representative device as a function of back-gate voltage before and after HMDS treatment is shown in Figure 3.2. The slopes of resistance versus gate voltage curve in the linear regime on both sides of maximum resistance point became sharper after HMDS application which indicates that both electron and hole field-effect mobilities were improved. We calculated mobility values along with residual carrier concentration based on a well-established diffusive transport model.[29] For this particular device, electron (hole) mobility increased from 2989 (2511) cm^2/Vs to 4872 (5596) cm^2/Vs. The maximum resistance point, also known as the Dirac point, moved from ~25 V to ~0 V. This indicates that initial p-type doping of as-fabricated device was reduced after HMDS application. The residual carrier concentration, n_0 was reduced from 4.26×10^{11} cm^{-2} to 2.12×10^{11} cm^{-2}, which is close to the theoretical intrinsic limit ~1.6×10^{11} cm^{-2}.[30] We also saw similar improvement for FETs made with exfoliated graphene.

The statistics of fabricated devices before and after HMDS application is presented in Figure 3.3. The data include devices made from several different batches. The general trend in electron and hole mobility improvement and reduction in residual carrier concentration is clear. However, the improvement factor is diverse for different

devices, which can be attributed to the initial and local graphene quality of fabricated devices. We usually observe mobility improvement of 1.5-2 times (50-100%) for most of our devices. Dirac voltage usually moves closer to 0 V. Hysteresis was usually suppressed after HMDS application but most of our devices had low hysteresis to begin with. There was no significant change in the ratio between maximum and minimum resistance values in transfer characteristics with HMDS treatment.

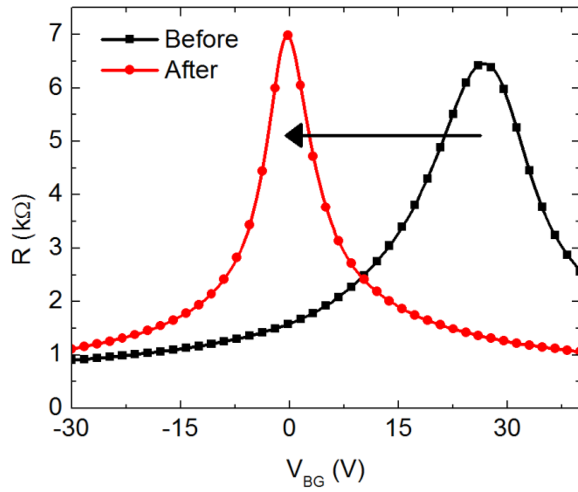


Figure 3.2: Resistance, R versus back-gate voltage, V_{BG} plot of a representative device before (black square) and after (red circle) HMDS treatment.

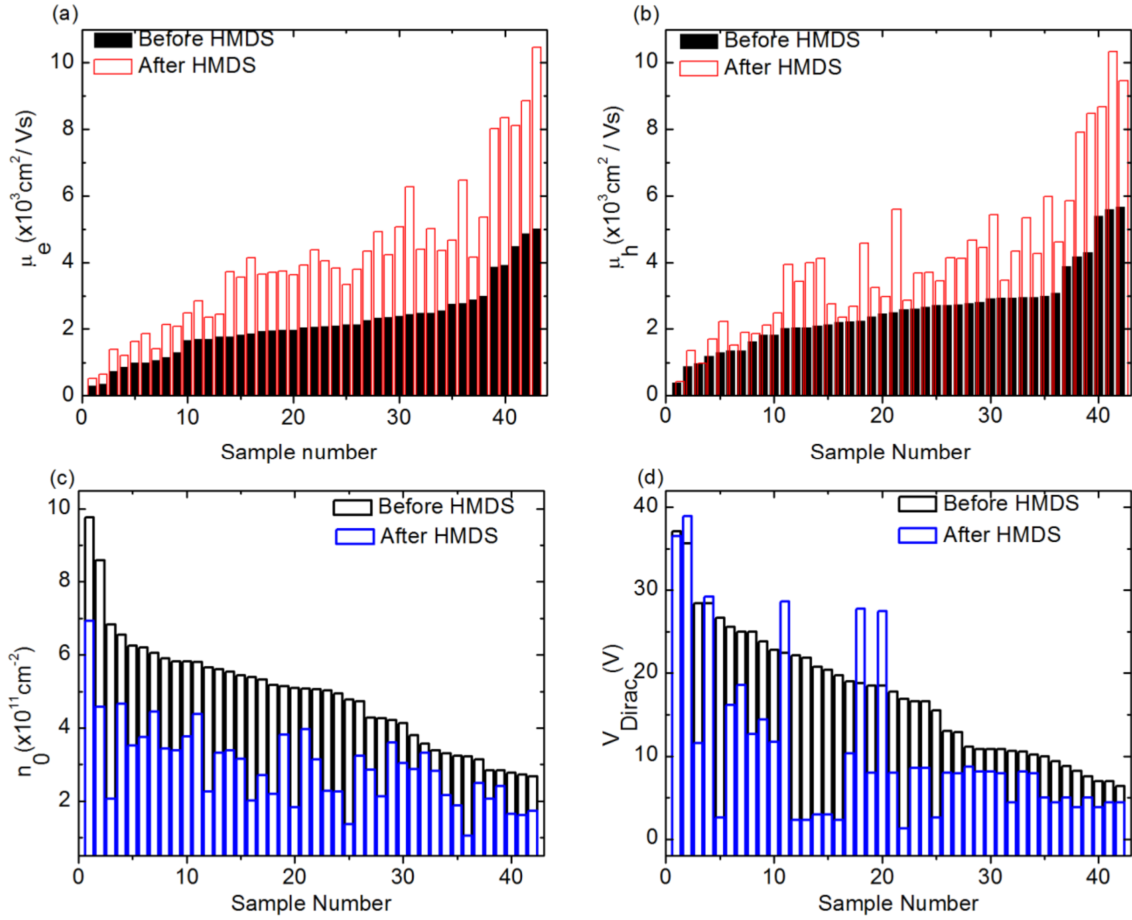


Figure 3.3: Statistics of fabricated devices before and after HMDS application, (a) electron mobility, μ_e (b) hole mobility, μ_h (c) residual carrier concentration, n_0 and (d) Dirac voltage, V_{Dirac}.

3.3 Time Evolution of Characteristics

Evolution of electrical characteristics at different stages of HMDS application is shown in Figure 3.4. The sample was taken out of HMDS and measured after certain time periods. Changes in electrical characteristics were observed even after 5 minutes and the mobility values saturated within ~ 6 hours. The improvement factor was similar in range even for a week of soak time.

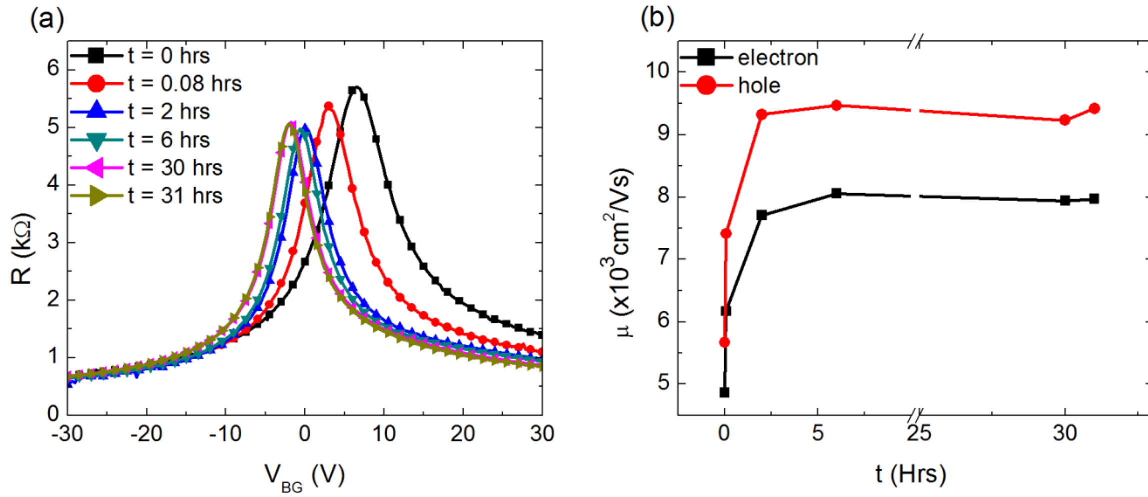
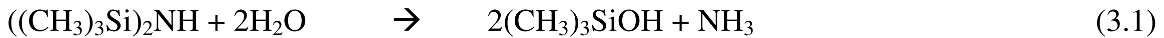


Figure 3.4: Evolution of the electrical characteristics with HMDS soak time. (a) Resistance, R versus back-gate voltage, VBG plots at different times, and (b) electron (black square) and hole (red circle) mobility, μ evolution with time, t.

3.4 Performance Improvement Mechanisms

Being a two-dimensional material, graphene is strongly influenced by its environment. Several atmospheric species such as moisture and oxygen molecules can adsorb on graphene's surface.[31,32] Moreover, there can be polymer and organic residues during device fabrication. For example, PMMA used for graphene transfer and device fabrication cannot be completely removed by solvent or even by annealing.[15,33] These adsorbed molecules and residues can serve as scattering sources and/or dopants resulting in an uncontrolled shift of the Dirac point with degraded mobility. The experimental results indicate that some of these degradation mechanisms are neutralized to varying degree upon HMDS treatment. For example, HMDS is widely used as hydrophobization agent, especially in biological science[34,35] and it is efficient in removing water molecules present on a sample's surface. It has been shown that HMDS can react with water to form Trimethylsilanol (TMS) according to the following reaction[36,37]:



$$((CH_3)_3Si)_2NH + 2H_2O \rightarrow 2(CH_3)_3SiOH + NH_3 \quad (3.1)$$

The conversion of HMDS vapor in air at 50% relative humidity and 25^0C to TMS has been verified experimentally by Fourier Transform Infrared Spectroscopy (FTIR).[37] HMDS may also modify the PMMA residues present on sample surface.[38] The reduction in residual carrier concentration upon HMDS treatment, as shown in Figure 3.3(c), supports our hypothesis.

Performance improvement is also likely to come from dielectric screening of charged impurities.[39,40] Charged impurities in the vicinity of graphene can cause long range Coulomb scattering. The presence of HMDS (dielectric constant, $\kappa = 2.27$) instead of air ($\kappa = 1$) increases the local dielectric constant. This, in turn, decreases the dimensionless fine structure constant which determines the interaction strength of charge carriers in graphene and charged impurities. Both theoretical and experimental studies have shown that reduction in fine structure constant results in improved carrier mobility along with reduced residual carrier density.[24,40]

In contrast, it has been shown in some Hall measurement experiments that the presence of high-κ dielectric on graphene can significantly enhance the effective back-gate capacitance and the change in electrostatic characteristics is mainly due to enhanced effective capacitance rather than mobility.[41,42] It is difficult to conclude the extent of this mechanism from our electrostatic measurement. First of all, HMDS is a low-κ liquid ($\kappa = 2.27$) and HMDS treated samples are completely dried in air before measurement, which should leave a very thin residual layer or trace amount of HMDS molecules. On the other hand, high-κ liquids used in those experiments ($\kappa > 25$) were applied in droplets during measurement and capacitive enhancement was found to be proportional to the size of droplet.[41] Also in those experiments, mobility was increased up to 100% which is consistent with our results.[42] It has been proposed that these high-κ polar solvents can

degrade mobility by additional Coulomb scattering from charged ion and dipole moment, which are not significant for HMDS.[25] More importantly, device capacitance measured for suspended graphene sample in non-polar (κ<5) liquid was found to be close to geometric capacitance of 300 nm SiO2, while for high-κ solvents, capacitance increases by orders of magnitude compared to that.[25] Therefore, in light of previous studies and our current results, we attribute the enhancement in electrostatic characteristics to mobility improvement rather than capacitive enhancement.

3.5 Temperature Dependent Transport Characteristics

The temperature-dependent electrostatic measurements before and after HMDS application are shown in Figure 3.5. As-fabricated graphene FET shows small variation in the characteristics between 77K and room temperature, as shown in Figure 3.5(a). This is expected because transport is limited by relatively temperature insensitive charge impurity scattering in this temperature range.[23] On the other hand, there is a large variation in electrical characteristics between 77K and room temperature after HMDS treatment, as shown in Figure 3.5(b). Extracted electron and hole mobility values are shown as a function of temperature before and after HMDS application in Figure 3.5(c) and Figure 3.5(d), respectively. Carrier mobility increases by small amount only with decreasing temperature before HMDS application. But mobility at 77K is almost 2 times higher than room temperature mobility after HMDS treatment.

The reduction of charged impurities upon HMDS treatment may allow the relative contribution of rather temperature dependent phonon limited process to increase. As temperature is reduced, there is less thermal agitation of lattice, hence less scattering, which, in turn, causes mobility to improve with decreasing temperature. However, as mentioned before, remote oxide phonon scattering from SiO_2 substrate is the next

mobility limiting factor after charged impurities, which imposes an upper limit of 40,000 cm^2/Vs at room temperature. This value is almost an order of magnitude higher than the device mobility in Figure 3.5. Hence this device is likely to be in the charged impurity limited regime for the temperature range of interest.

Mobility improvement with decreasing temperature can be attributed to temperature dependent dielectric constant of HMDS and/or TMS.[43] These are slightly polar molecules consisting of atoms with different electronegativities which can lead to dipole formation.[44,45] These dipoles align with electric field under applied bias. However, random thermal motion prevents good alignment at ambient temperature. As temperature is lowered, there is less thermal motion allowing the dipoles to align more perfectly with the field. This phenomenon, in effect, increases the orientational polarization and hence, the dielectric constant. Increase in dielectric constant leads to improvement of electrical characteristics with decreasing temperature by improved dielectric screening. Dielectric constant can also change at phase transition since material structures are usually different at different phases. The freezing points of HMDS and TMS are 193K and 214K, respectively. Hence these materials go through phase transitions in the temperature range of interest.

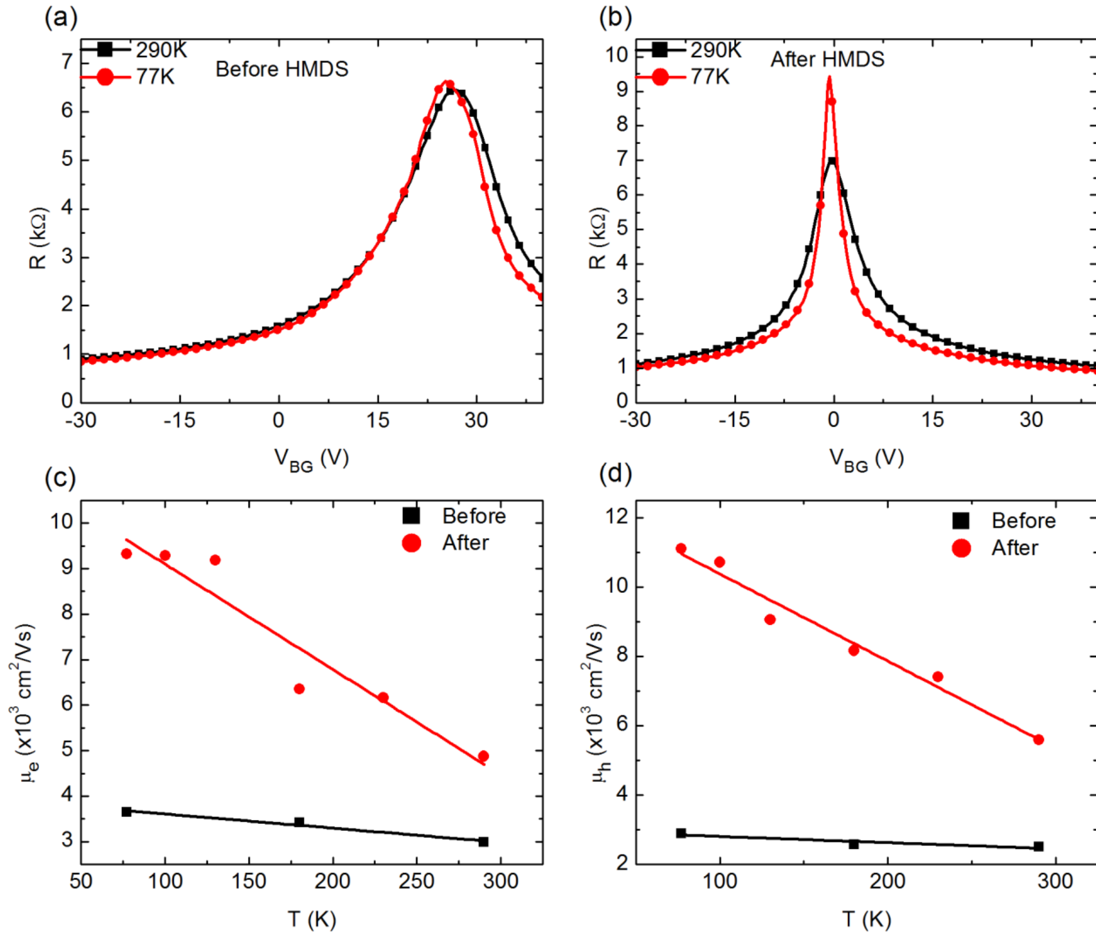


Figure 3.5: Temperature dependent electrostatic measurements. Resistance, R versus back-gate voltage, V_{BG} plot at 295K (black square) and 77K (red circle). (a) Before HMDS application, and (b) after HMDS application. (c) Electron mobility, μ_e and (d) hole mobility, μ_h. The straight lines serve as visual guides only.

3.6 HMDS Treatment of FET Fabricated on Hydrophobic Surface

In order to further understand the effect of HMDS, back-gated graphene FETs were fabricated on hydrophobic SiO_2 substrate and HMDS treatment was applied after device fabrication. Before transferring graphene, the Si-SiO_2 target substrate was cleaned with piranha solution known to have silanol (Si-OH) terminated hydrophilic substrate.[46] In order to achieve a robust hydrophobic substrate, we applied HMDS vapor in an oven at

150°C ensuring proper dehydration prior to HMDS treatment, which results in a hydrophobic surface with methyl termination.[27] BGFETs were fabricated with graphene transferred on this hydrophobic substrate and we applied HMDS with our solution phase process after device fabrication. Figure 3.6 shows the characteristics before and after HMDS application for both forward and reverse sweeps of back-gate voltage. The Dirac point shifted from 9.3V to 1.8V, initially low hysteresis reduced slightly and electron (hole) mobility changed from 1330 (1768) to 1818 (2100) cm^2/Vs. A total of 6 devices were measured and they all showed changes in electrical characteristics. This was not a high quality sample to begin with. We expect higher values for mobilities in good samples.

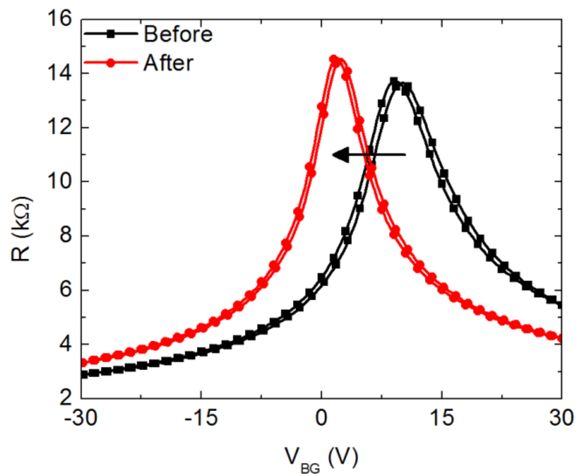


Figure 3.6: Resistance, R versus back-gate voltage, V_{BG} (both forward and reverse sweeps) plot for a representative device fabricated with graphene transferred on hydrophobic SiO_2 substrate with HMDS treatment prior to graphene transfer. Data for before and after HMDS treatment of top surface of fabricated device are represented by black squares and red circles, respectively.

3.7 Raman Spectroscopic Analysis

In addition to electrical measurements, we also performed Raman spectroscopic analysis of graphene transferred on SiO_2. Raman spectroscopic data were gathered with a Renishaw In-Via Raman Microscope using a 532 nm laser. 121 high resolution data points were gathered for both before and after HMDS application dataset from a nominally identical 10µm × 10µm area of a CVD fabricated device. Figure 3.7(a), 3.7(b) and 3.7(c) shows the position of the G peak, width of the G peak and intensity ratio between the 2D and G peaks (I(2D) / I(G)), respectively, before and after HMDS application. As seen from the data, position of the G peak downshifted (from 1587.33±1.14 cm^{-1} to 1586.47±0.44 cm^{-1}), width of the G peak increased (from 17.05±2.19 cm^{-1} to 22.71±1.25 cm^{-1}) and the I(2D)/I(G) increased (from 2.81±0.38 to 3.56±0.21). More pronounced changes in these parameter were observed for an exfoliated flake (for e.g. I(2D)/I(G) increased from 2.02±0.05 to 4.94±0.11). Decrease in I(2D)/I(G), decrease in G peak width and up shift of G peak position have been associated with increased doping by impurities.[14,32,47] Therefore, our Raman data suggest that impurities are getting screened or mitigated after HMDS application.

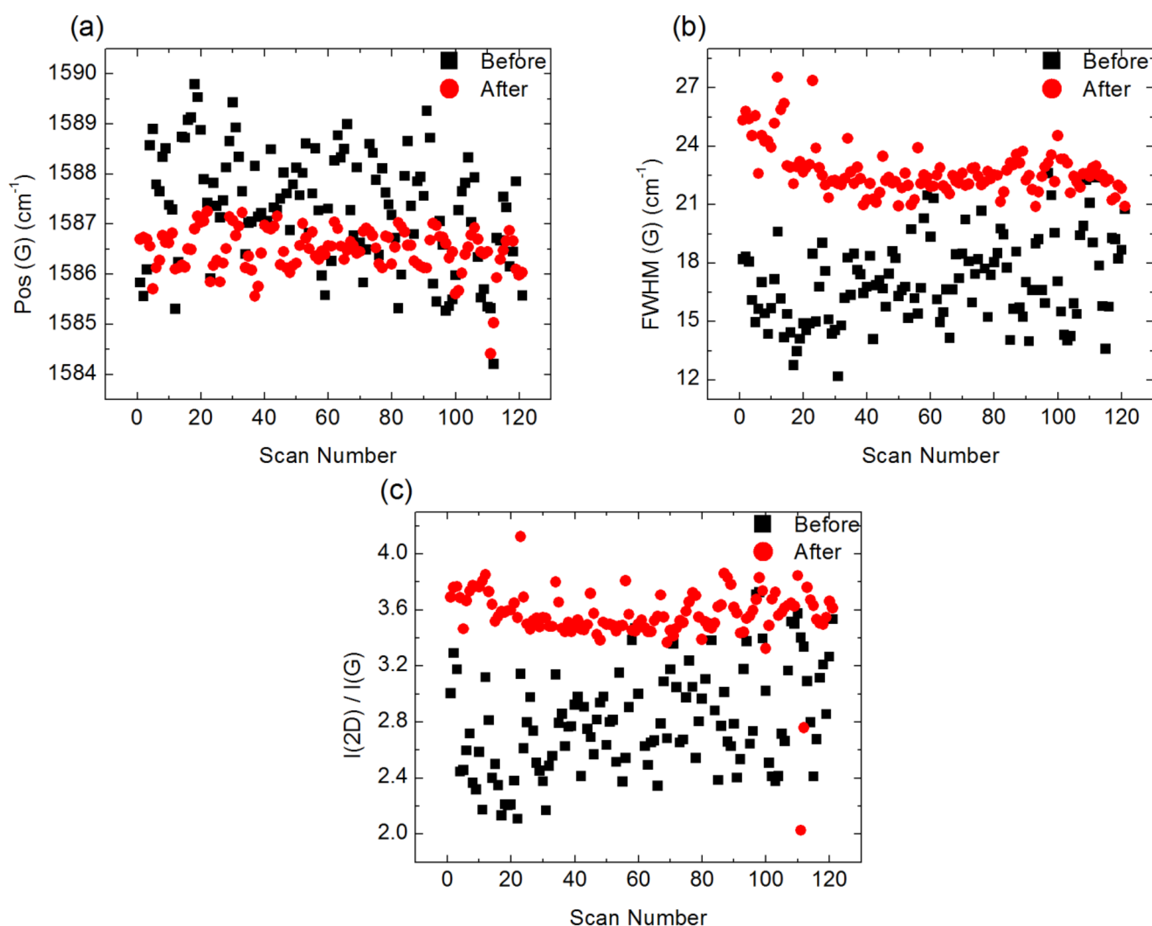


Figure 3.7: Raman Spectroscopic Analysis (a) G peak position, Pos(G) of graphene Raman spectra for 121 scans before (black square) and after (red circle) HMDS treatment. (b) G peak full width half max, FWHM(G) before (black square) and after (red circle) HMDS treatment. (d) Intensity ratio between 2D and G peaks, I(2D) / I(G) before (black square) and after (red circle) HMDS treatment.

3.8 Stability Considerations

One obvious issue with this type of solution process is the stability of the mechanism with time. HMDS treated devices usually returned to their initial state within ~ 3 days when left in ambient, as shown in Figure 3.8(a). HMDS is known to degrade in humid air due to hydrolysis and TMS is a volatile compound.[37] In order to preserve the improvement by HMDS treatment, samples should be protected with suitable capping

layer formed by vapor deposition or atomic layer deposition which does not degrade the HMDS and graphene quality. Unfortunately, graphene is usually degraded with most type of common depositions on it. We have tried several capping scheme with no success. For example, we tried to encapsulate the device with spin coating PMMA after HMDS treatment, as shown in Figure 3.8(b). Unfortunately, the device returned almost to its initial state after PMMA encapsulation. Development of suitable capping process will come with its own set of challenges and will need considerable further research.

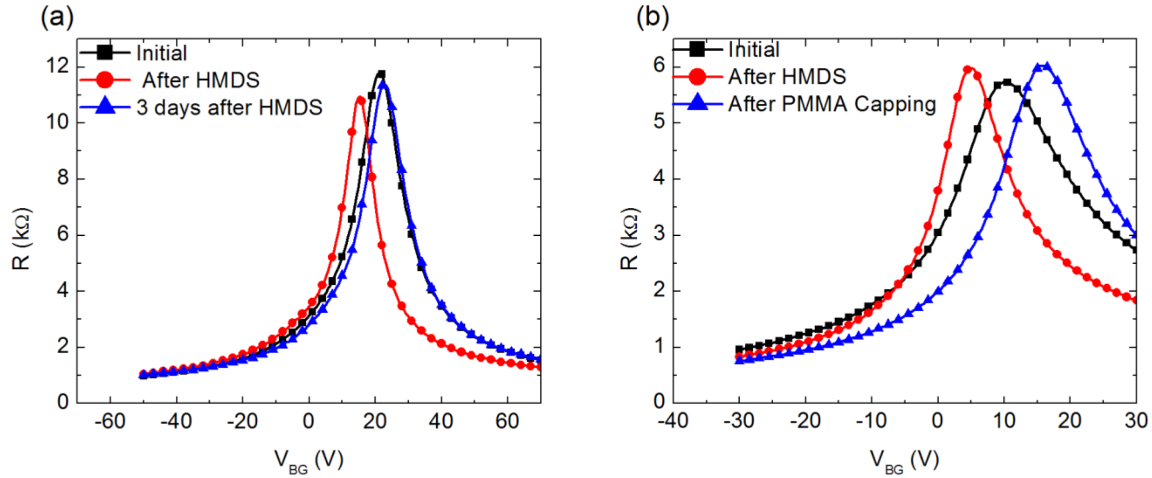


Figure 3.8: (a) Evolution of transfer characteristics with time for a sample stored under ambient conditions. (b) Transfer characteristics for PMMA encapsulation.

3.9 HMDS treatment of MoS_2 based FET

In addition to improving graphene based FET performance, we wanted to examine if HMDS treatment can be used in general to improve two-dimensional materials based FET characteristics. Like graphene, other two-dimensional materials such as MoS_2, WSe_2 etc. are also expected to be perturbed by atmospheric impact, if the flakes are very thin. For example, it has been experimentally demonstrated that adsorbed moisture can degrade monolayer MoS_2 based FET performance.[48] To this end, we treated

MoS_2 based BGFET with HMDS and compared the transfer characteristics before and after HMDS treatment. Both monolayer and multilayer MoS_2 flakes were used for device fabrication.

Monolayer MoS_2 was grown by a vapor transport technique using MoO_3 and S powder on 285-300 nm SiO_2 – highly doped Si substrate. Thickness of the grown film was confirmed by Raman spectroscopy and photoluminescence measurement. The details of the growth process and characterization have been reported in another study.[49] In order to find suitable device area in the film and ensure proper alignment for subsequent lithography steps, 1 nm Ti – 49 nm Au metal stack were deposited as alignment marks using e-beam evaporation and lithography. The active area was patterned by etching the superfluous MoS_2 with chlorine plasma (75Watt, 1 minute, 10 sccm chlorine in Plasma-Therm 790 RIE system). The patterned MoS_2 region was contacted with ~30 nm Ni – ~20 nm Au stack. This completed the fabrication of a simple back-gated monolayer MoS_2 based FET. An optical picture of a fabricated FET with 10 µm channel length is shown in Figure 3.9. The HMDS treatment procedure is same as stated in section 3.1.

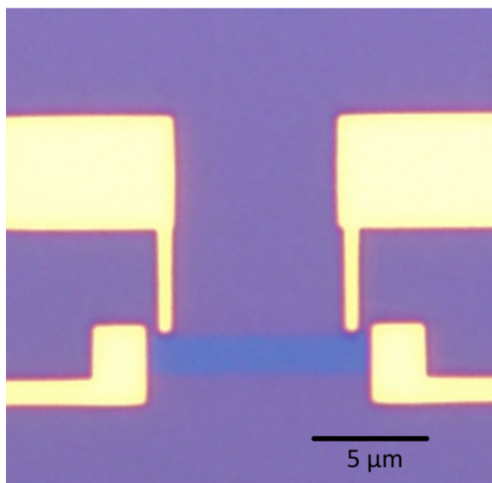


Figure 3.9: Optical image of a fabricated BGFET with monolayer MoS_2 channel.

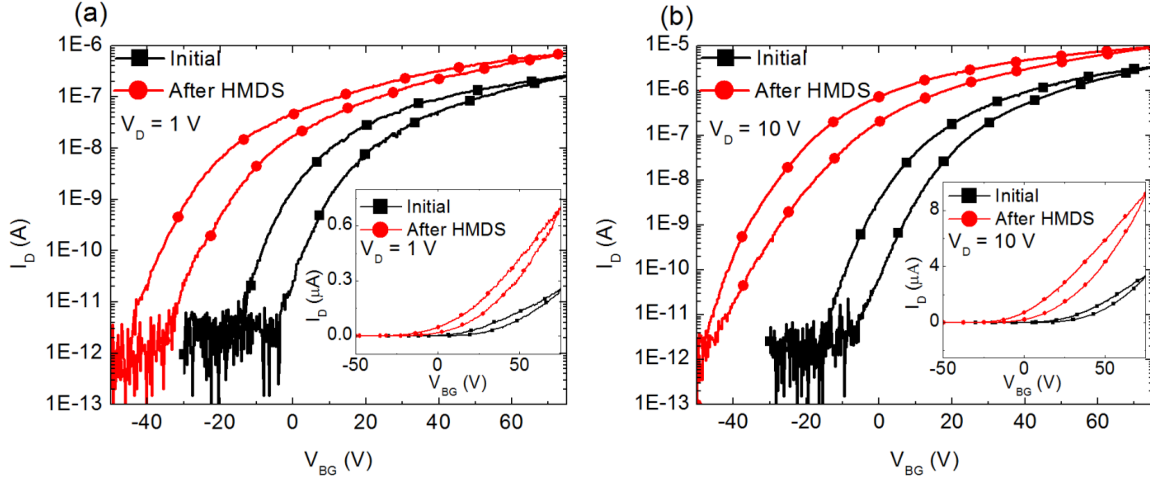


Figure 3.10: Transfer characteristics (log scale) of fabricated BGFET on monolayer MoS_2 before and after HMDS treatment. Insets show same characteristics in linear scale. (a) $V_D = 1$ V. (b) $V_D = 10$ V.

The transfer characteristics of the fabricated BGFET before and after HMDS treatment are shown in Figure 3.10.The on-off ratio increased and threshold voltages shifted towards more negative values after HMDS treatment. However, after adjusting for the threshold voltage shift, the drive current after HMDS treatment is higher than the initial case for same amount of overdrive (V_{BG}-V_{TH}). We extracted the field-effect mobility values using the equation: $\mu = \frac{dI_D}{dV_{BG}} \frac{L}{W*C*V_D}$, where L = channel length, W = channel width, C = gate capacitance (300 nm SiO_2 in this case), V_D = drain bias, I_D = drain current, V_{BG} = back-gate voltage and $\frac{dI_D}{dV_{BG}}$ is trans-conductance, whose peak value is used for mobility extraction. The field-effect mobility with $V_D = 1$ V increased from 3.63 cm^2/Vs to 6.83 cm^2/Vs after HMDS treatment. For $V_D = 10$ V, it increased from 4.6 cm^2/Vs to 8.1 cm^2/Vs. Several other FETs were fabricated and they all showed similar degree of improvement. Thus, like in the case of graphene, HMDS treatment can also improve monolayer MoS_2 based FET performance.

Unlike monolayer system, where current flow is confined in one single layer, multilayer BGFETs can have their current distributed among several layers and based on

the flake thickness, one or two layers located in middle of the flake can carry the bulk of the current.[50,51] Therefore, surface treatment methods like HMDS treatment may not be effective for multilayer system as it is for monolayer FETs. To verify this conjecture, multilayer MoS_2 based FETs were fabricated and treated with HMDS. Indeed, there was no improvement in field-effect mobility.

Multilayer MoS_2 flakes were exfoliated from bulk crystal using scotch tape method and transferred onto 300 nm SiO_2 – highly doped Si substrate. Suitable flakes were identified for device fabrication and were contacted with Ag-Au metal to serve as source and drain electrode. An optical image of a fabricated BGFET with multilayer MoS_2 channel is shown in Figure 3.11. The height of the flake was measured with Atomic Force Microscopy (AFM) and it was ~ 6 nm, which constitutes roughly 10 monolayers of MoS_2.

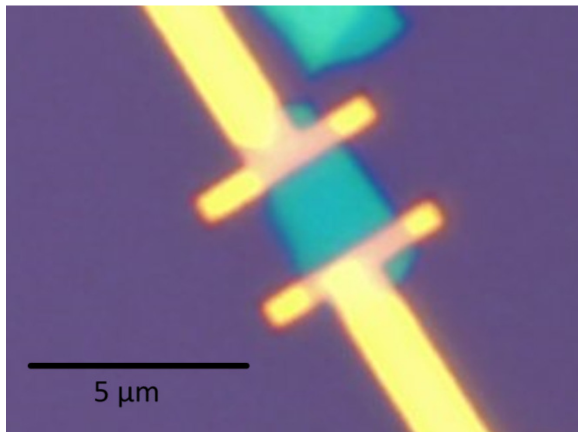


Figure 3.11: BGFET with multilayer MoS_2 channel.

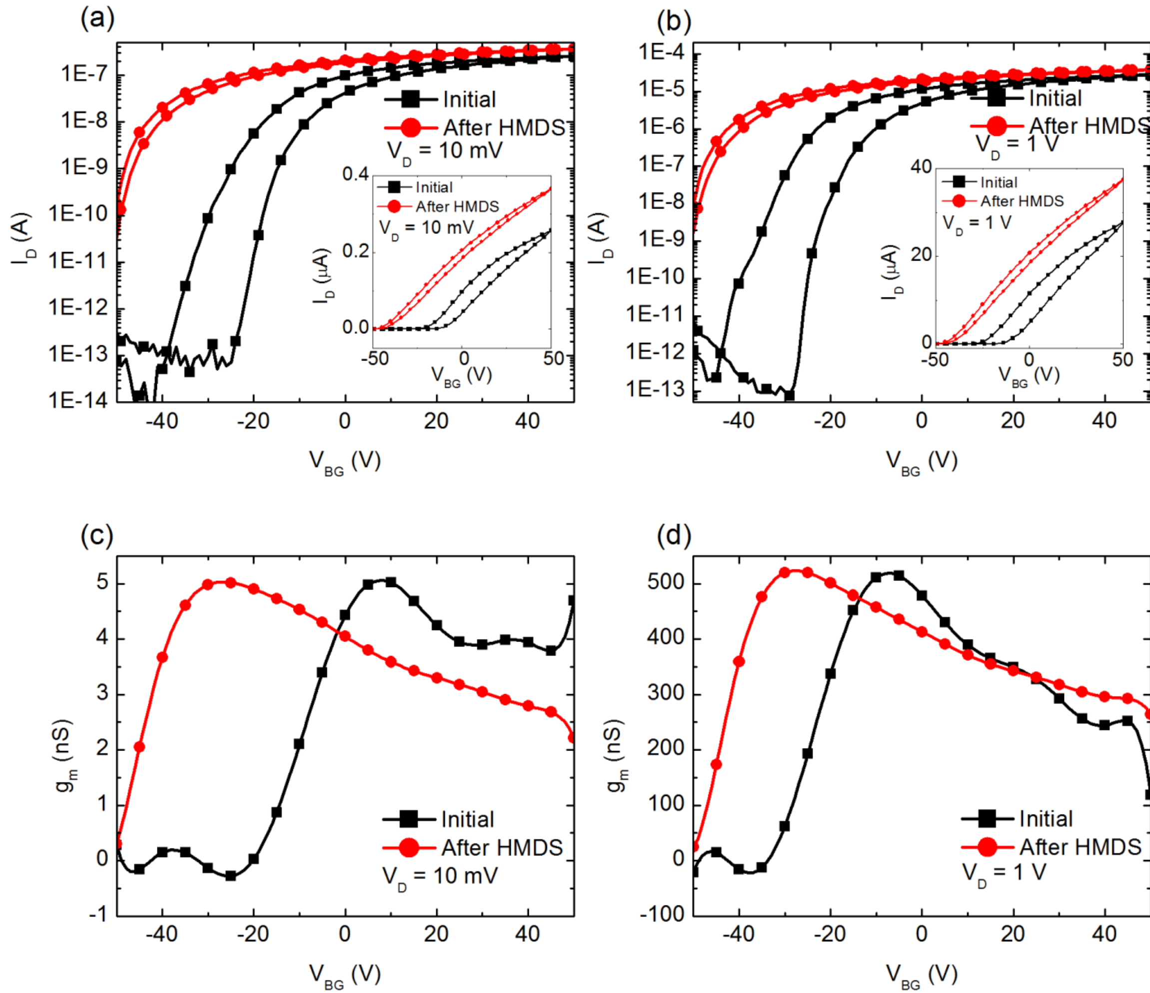


Figure 3.12: Transfer characteristics (log scale) and corresponding trans-conductance plots of a multilayer MoS_2 based FET before and after HMDS treatment. (a) I_D-V_{BG} plot for V_D = 10 mV. (b) I_D-V_{BG} plot for V_D = 1 V. Insets of (a) and (b) show the characteristics in linear scale. (c) Trans-conductance, g_m plot for V_D = 10 mV. (d) Trans-conductance, g_m plot for V_D = 1 V.

The transfer characteristics and corresponding trans-conductance plots before and after HMDS treatment are shown in Figure 3.12. Like the monolayer case, threshold voltage shifted towards more negative value after HMDS treatment. However, from the trans-conductance plot, it is evident that field-effect mobility remained almost exactly the same before and after HMDS treatment. Extracted field-effect mobility for this device is

~55 cm^2/Vs. Thus, unlike monolayer case, HMDS treatment was not effective in improving performance of FETs with multilayer channel.

Chapter 4: Thickness Tuning of Black Phosphorus Flakes by Plasma Treatment

Two-dimensional layered materials have gained a renewed scientific and technological interest in the last decade, thanks to the isolation of graphene from bulk graphite. Graphene has been regarded as a promising material for next generation electronic applications for its numerous fascinating properties such as high carrier mobility and thermal conductivity, high current carrying capacity and ultimate transistor scalability for being an atomically thin material.[11,52,53] However, transistors employing graphene as a channel material exhibit a poor ratio of on state current to the off state current (on-off ratio) due to lack of band gap in graphene. This prohibits the use of graphene based conventional FETs as digital switches. Graphene is more suitable for high frequency analog/RF applications which can be operated with the transistors always on, hence they do not need a channel material with band gap. Nonetheless, it is not possible to attain current saturation in graphene by conventional pinch off mechanism due to the lack of a depletion region (which is, again, a consequence of zero band gap). With the exception of few reports of current saturation via velocity saturation, most graphene based FETs show linear output characteristics.[54,55] The high value of output conductance reduces the intrinsic gain (ratio of trans-conductance and output conductance) and makes it difficult to get power gain out of a graphene FET based amplifier. These challenges have motivated researchers to explore various other two-dimensional materials beyond graphene for use in FET applications.

Black phosphorus (BP) has recently emerged as a new member in the two-dimensional materials family for electronic applications.[56–58] It is popularly known as Phosphorene. BP is an elemental semiconductor of phosphorus atoms and structurally

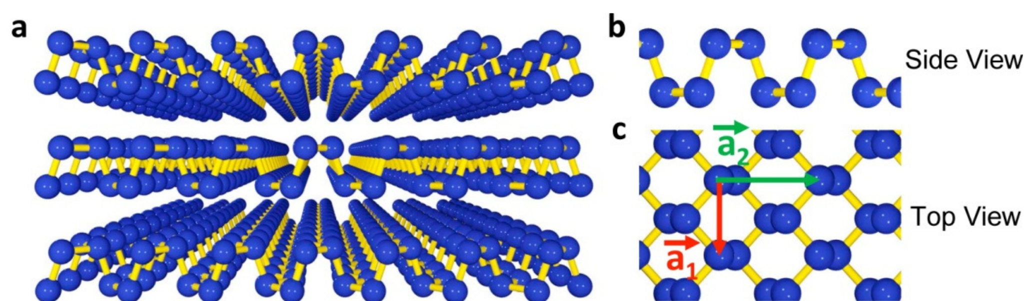


Figure 4.1: Crystal structure of few-layer phosphorene. (a) Perspective side view of few-layer phosphorene. (b) Side and (c) Top views of few-layer phosphorene. Adapted with permission from reference[56]. Copyright (2014) American Chemical Society.

similar to graphene, but with a puckered structure. The crystal structure of BP is shown in Figure 4.1. It has decent carrier mobility value up to ~1000 cm^2/Vs. It has a band gap of 0.3-0.36 eV in the bulk limit which can be tuned up to 1-2 eV for monolayer. It is a direct band gap semiconductor material which makes it useful for both electronic and opto-electronic applications.

Controlling the thickness of exfoliated BP flakes is of utmost technical importance for several reasons. First, the thickness dependent band gap of BP increases with decreasing thickness. Band gap directly affects the device off state current, hence on-off ratio which is an important performance metric for FET applications.[3] In addition, it is very important to maintain good electrostatic control of the channel by gate terminal over drain terminal in scaled MOSFETs in order to overcome several short channel effects (SCE).[59] Therefore, monolayer channel is desirable from the on-off ratio and SCE perspectives. On the contrary, charge carriers are most adversely affected by the surrounding environment in a monolayer. For layered materials, it has been suggested that the effective field-effect mobility in back-gated or embedded-gate FET structures reaches maximum value for a certain flake thickness; usually 5-10 nm.[51,56,57,60,61] The

layers closest to the gate dielectric are the ones which are most affected by the gate field (hence the substrate also). If the flake is too thin, charge carriers are affected by impurities or fixed charges present in the substrate. On the other hand, source and drain metal electrodes directly contact the top most layer only and charge carriers need to overcome finite interlayer resistance in order to be injected to the layers beneath the top most layer. If the flake is too thick, high interlayer resistance can lower the amount of injected carriers and hence current. This is not the case for a top-gated FET where the same top most layer is concurrently in the closest proximity of the gate and contacted by the source and drain electrodes. Even so, proper flake thickness is critical for optimum screening, electrostatics and SCE control.

In this chapter, we report our experimental work on tuning the thickness of few-layer BP by oxygen plasma treatment. Detailed optical and Atomic Force Microscopy (AFM) analyses are presented for the thickness reduction process. Plasma treatment on fabricated BGFETs shows proper device functionality with little or no degradation. Most significantly, we have fabricated well behaved, top-gated FET with good performance on the plasma treated surface of BP for the first time. In addition to the electrical data, we have performed Raman Spectroscopy, Time of Flight Secondary Ion Mass Spectrometry (TOF-SIMS) and X-Ray Photoelectron Spectroscopy (XPS) in order to understand the physical and chemical impacts of the thickness reduction process.

4.1 Experimental Methods

Few-Layer BP flakes were exfoliated from layered bulk BP crystal using scotch tape method and transferred onto 300 nm SiO_2 – highly doped n type Si substrate.[6] Flake thinning process was carried out in Plasma-Therm 790 RIE system using Oxygen plasma (150 watt RF power, 200 mTorr chamber pressure, 18 sccm flow rate; unless otherwise

stated). For optical and AFM characterization, idle times between etching and microscopy processes at successive etching steps were minimized in order to avoid any environment induced degradation of BP flakes.[62,63] In order to make back-gated FET (BGFET), the SiO_2-Si substrate was treated with HMDS before transferring the flakes to make the surface hydrophobic, which prevents water accumulation at the interface between the substrate and flake.[64] The substrate was spin coated with PMMA right after transferring the flakes, again to avoid ambient exposure. Suitable flakes in the thickness range of ~ 10-20 nm were identified for device fabrication. The contacts were defined by electron beam lithography. Ni (~ 50-60 nm) or Ni (~30-40 nm) – Au (20 nm) metal stack was deposited as contact metal using electron beam evaporation and liftoff process in acetone. For top-gated device, the gate area was patterned using electron beam lithography. Aluminum Oxide (~30 nm) – Ni (~40 nm) gate stack was deposited in a single electron beam evaporation process. The experimental details of the Raman, XPS and TOF-SIMS analyses will be discussed along with the data.

4.2 Optical and AFM Characterizations of Flake Thinning Process

Figure 4.2 shows the optical images of two adjacent flakes at different stages of the flake thinning process. A total of 9 successive etch runs were performed, each with a duration of 1 or 2 minutes. As can be seen from the images, the flakes are getting thinner uniformly, maintaining the relative thickness differences between different portions of the flake. This is more evident from the relatively non uniform bottom flake. The thinner portions of the flakes are faintly visible after the 8th etch and become optically invisible after the 9th etch.

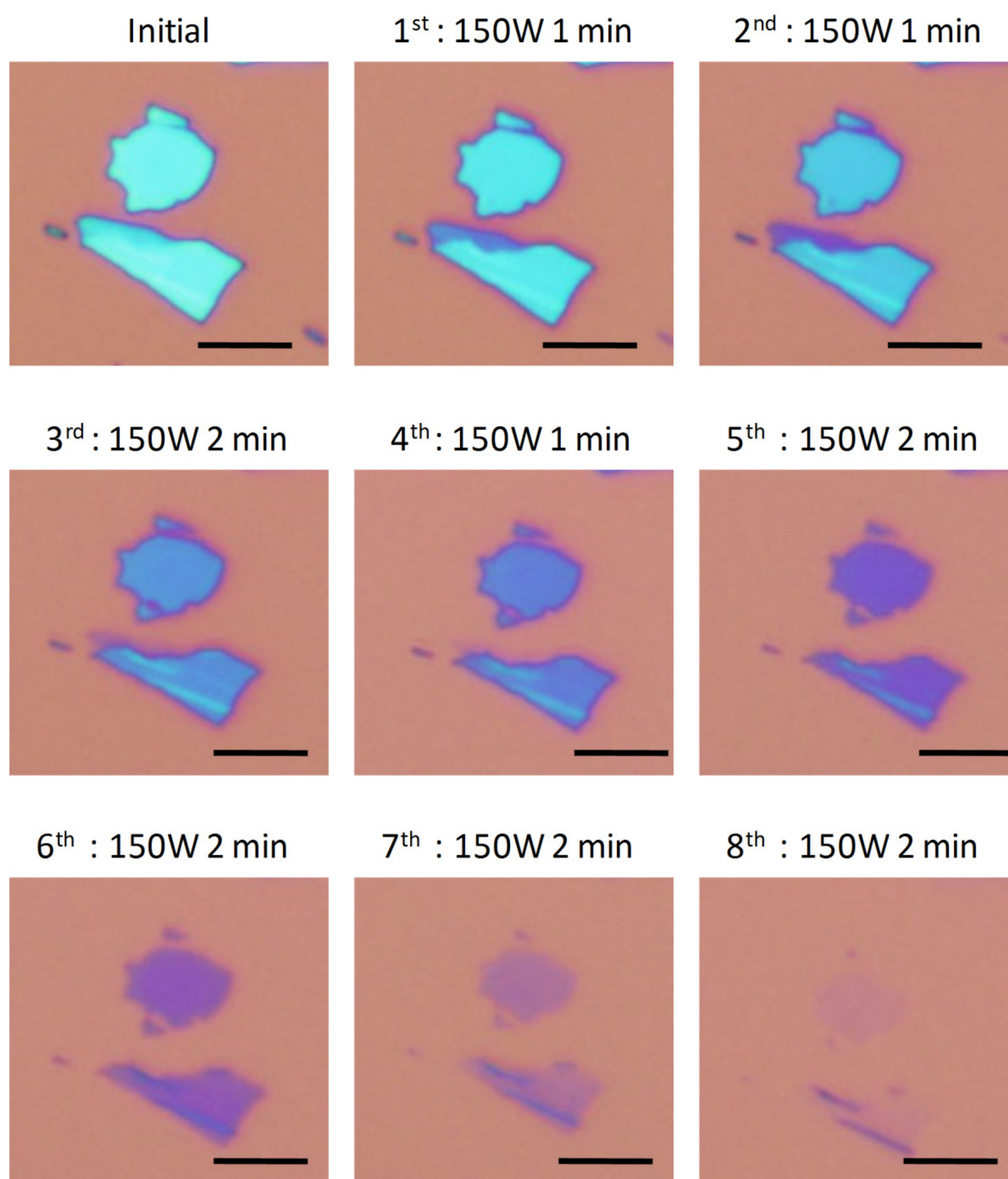


Figure 4.2: Temporal sequence of flake thinning process. Caption on each optical image include etch number, plasma power and duration. Scale bar is 5 μm.

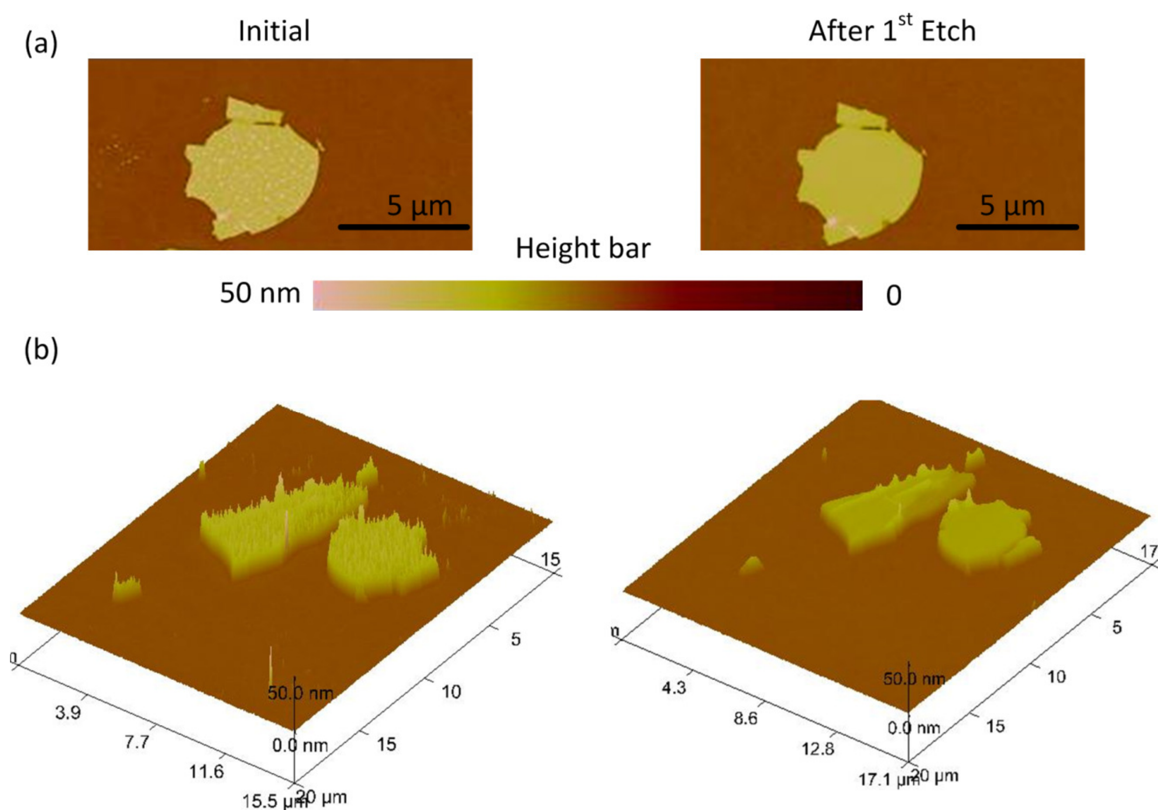


Figure 4.3: AFM images of the BP flakes shown in Figure. 4.2. before and after plasma treatment. (Left: as exfoliated, right: after first etch) (a) Top view of the top flake in Figure 4.2. (b) 3D view of the flakes.

AFM images before and after plasma treatment of the flakes shown in Figure 4.2 are presented in Figure 4.3. It is evident from the initial AFM image that as-exfoliated BP flakes may have rough surfaces with protrusions which are not visible in the optical images. Similar findings have been reported in other studies.[62,63] It has been suggested that ambient species such as H_2O and O_2 can react and degrade BP by forming phosphorus oxides or oxoacids. For example, BP can react with ambient O_2 to produce P_4O_{10} (also written as P_2O_5), which, in turn, can readily react with ambient moisture to produce phosphoric acid due to hydrophilic nature of P_4O_{10}.[65]

$$P_4 + 5O_2 \rightarrow P_4O_{10} \quad (4.1)$$

$$P_4O_{10} + 6H_2O \rightarrow 4H_3PO_4 \quad (4.2)$$

As shown in Figure 4.3, O_2 plasma etching can remove the chemical degradation from the surface of the BP flakes, resulting in a smooth surface. The RMS surface roughness decreased from 3 nm for as-exfoliated case to 0.3 nm after the first etching. Therefore, in addition to thickness reduction, this O_2 plasma treatment can clean the surface of BP flake by removing the ambient degradations as well as the process induced organic residues during device fabrication. It should be mentioned that the cleaning effect is also observed for lower power, shorter duration etch (e.g. 75W, 30s) and not all as-exfoliated flakes have such high roughness.

Detailed AFM analysis of the top flake of Figure 4.2 is shown in Figure 4.4. The line scans after some of the etch steps are shown in Figure 4.4(a). The scan of the as-exfoliated flake has numerous spikes which are removed by the initial etch. The flake has a smooth surface at an intermediate stage of 4th etch. After the 8th etch, flake thickness was reduced below 5 nm, however, surface roughness became significant. The temporal evolutions of flake height and surface roughness with each consecutive etch are shown in Figure 4.4(b) and 4.4(c), respectively. The height decreases in a monotonic manner with each etch step. The data point at t = 15 minutes corresponds to the 9th etch where the flake became optically invisible. However, AFM scan shows presence of ~ 0.8 nm flake with significant roughness and discontinuity. After the initial decrease for as-exfoliated flake, surface roughness increased steadily with each etching step, but the value remained below 0.75 nm till 11th minute (7th etch). As mentioned before, it increased to ~1.5 nm after the 8th etch. Careful calibration and lower plasma power with shorter duration of etch step should be employed for thickness scaling below 5 nm. For example, using 75W plasma power instead of 150W resulted in reduction of etch rate roughly by 50%.

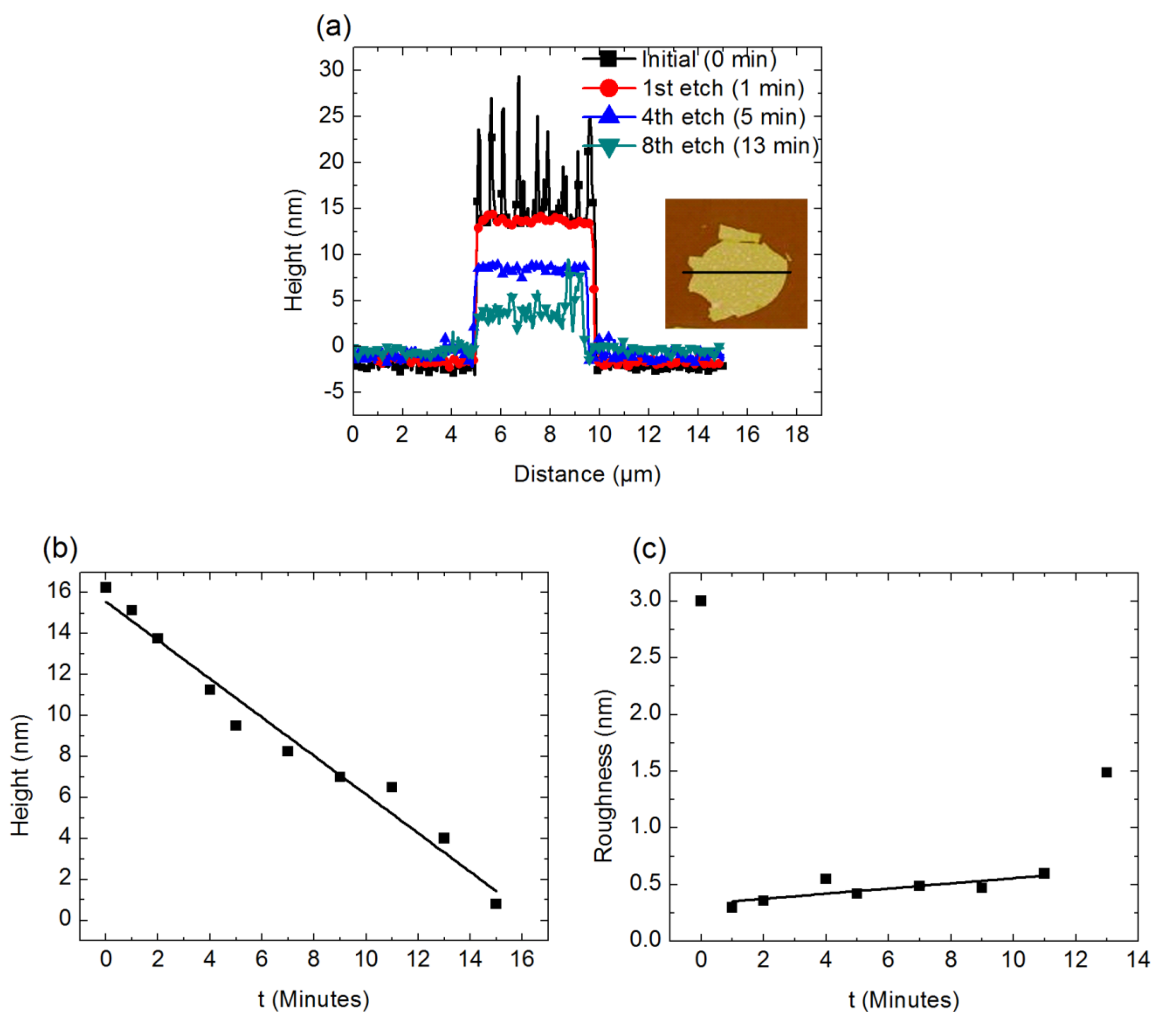


Figure 4.4: AFM analysis for flake thinning process. (a) Line scan across the flake. Time in parenthesis is cumulative time of current and all previous etch steps. (b) Temporal evolution of flake height. (c) Temporal evolution of flake roughness. The straight lines serve as visual guides only.

Since the BP etching was carried out with O_2 plasma in a RIE system, there can be both physical and chemical etching processes by O_2^+ ions and O radicals, respectively. O radicals can readily react with phosphorus to form oxidized species. P_2O_5 formation is likely due to abundance of oxygen and P_2O_5 sublimes at relatively low temperature of ~360 ^{0}C at atmospheric pressure.[66] Therefore, the oxide layer is expected to have a

tendency to volatize at ~200 mTorr chamber pressure. In addition, the O^{2+} ions can participate in the etching process by physical ion bombardment. Determination of the exact etching mechanism and relative contribution of physical and chemical etching will require considerable further study.

Optical images of thinning process for couple of other flakes along with their temporal evaluation of thickness are presented in Figure 4.5.

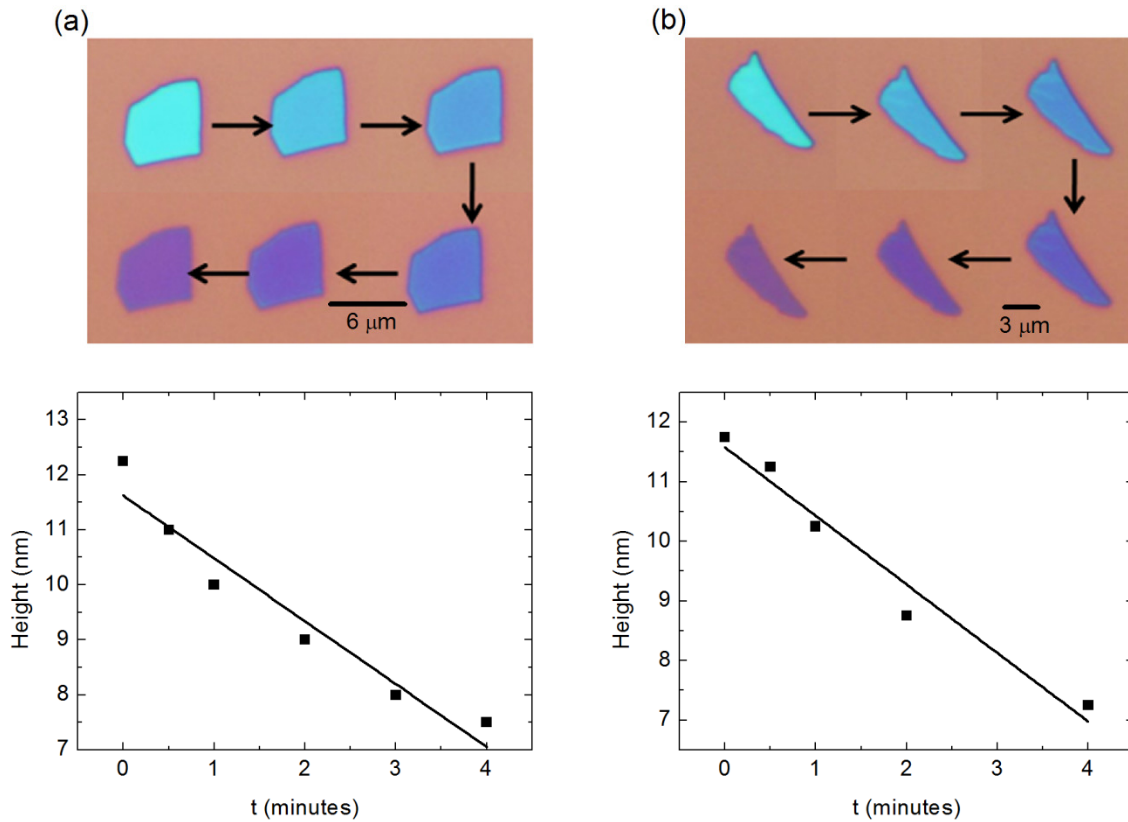


Figure 4.5: Flake thinning process for couple of other flakes. Height evaluation data obtained from AFM are placed below corresponding flakes.

4.3 Impact of Thinning Process on Field-Effect Transistor

4.3.1 Back-gated FET

In order to assess the impact of flake thinning process by O_2 plasma on transistor characteristics, fabricated BGFET was subjected to plasma treatment. After fabrication and initial electrical measurements, the device was treated with O_2 plasma twice for 30s (1st etch) and 60s (2nd etch). Optical images of the BGFET after fabrication and after each of the etching steps are shown in Figure 4.6. The uniform change of BP contrast after each step clearly demonstrates reduction of flake thickness with plasma treatment.

The transfer characteristics before and after the plasma etching steps are shown in Figure 4.7. The measurements were carried out in a vacuum probe station at room temperature. It is evident that the device is completely functional after the plasma treatments. The device turn-on or threshold voltage shifted towards zero gate voltage with each etching step. The on-off ratio is expected to increase with decreasing thickness. This is indeed the case for the back-gate voltage (V_{BG}) range of -50V to 50V, as shown in Figure 4.7(b). However, we cannot comment about the absolute values of on-off ratio since the off state for some of the cases (especially initial) are outside the V_{BG} range. The range of V_{BG} was limited to ensure safe operation of the device.

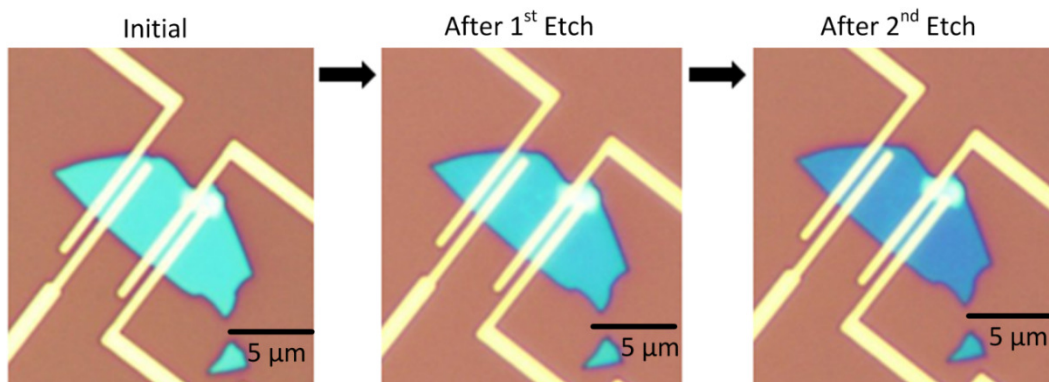


Figure 4.6: O_2 plasma treatment of fabricated BGFET.

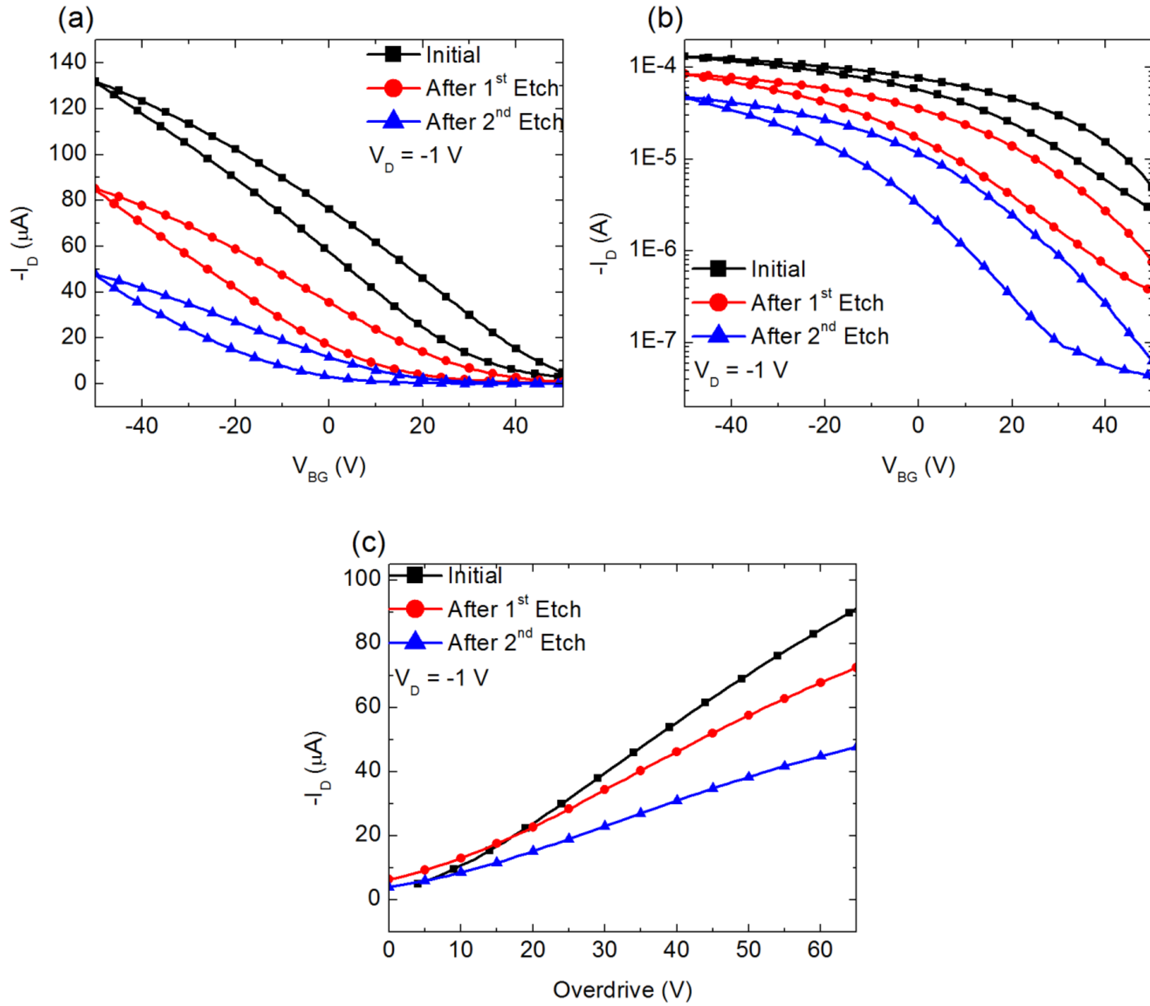


Figure 4.7: Transfer Characteristics of BGFET at different stages of plasma treatment. (a) $-I_D$ Vs V_{BG} (linear scale) for bidirectional sweep of V_{BG} (b) $-I_D$ Vs V_{BG} (log scale) for bidirectional sweep of V_{BG} (c) $-I_D$ Vs overdrive voltage (V_{BG}-V_{TH}) for +50V to -50V V_{BG} sweep.

In order to account for the threshold voltage shift, it is necessary to compare current levels for same amount of overdrive voltage (V_{BG} - V_{TH}) rather than back-gate voltage (V_{BG}). As shown in Figure 4.7 (c), current decreased by roughly 20% with each etching step. It should be noted that there are some small currents at zero overdrive for couple of traces due to small discrepancies in threshold voltage extractions. Ideally, current should be zero for zero overdrive. The reductions in current levels with etching

are expected since the number of current conducting layers in the BP flake decreases with each etching step. The increase in current level due to mobility improvement with thinning has not been realized in this device for several reasons. First of all, the thickness was varied by a small amount only since etching steps were short. Most importantly, the BP regions under the metal contacts had not been etched during the etching steps because they were protected by metal. Therefore, the interlayer resistance did not decrease during the flake thinning process. Our goal was to analyze the impact of O_2 plasma on a device with known performance before plasma processing. In order to realize the benefit of interlayer resistance reduction with flake thinning, BP flake should be thinned before device fabrication. The extracted field-effect mobility values are 141, 106 and 71 cm^2/Vs for initial, after 1st etch, after 2nd etch cases, respectively. The reduction of mobility can be explained by the same argument for current reduction. It should be mentioned that channel length of this device was 5 µm and it was characterized using -1 V drain bias. A lower drain bias is expected to result in better mobility values.

The output characteristics of the BGFET at different steps of the etching process are shown in Figure 4.8. Reduction of current levels with thinning is also reflected in output characteristics. Drain currents are seen to be varying linearly with drain voltage. We did not observe current saturation for the BGFET, primarily because of high gate dielectric thickness and voltage level mismatch between gate and drain.

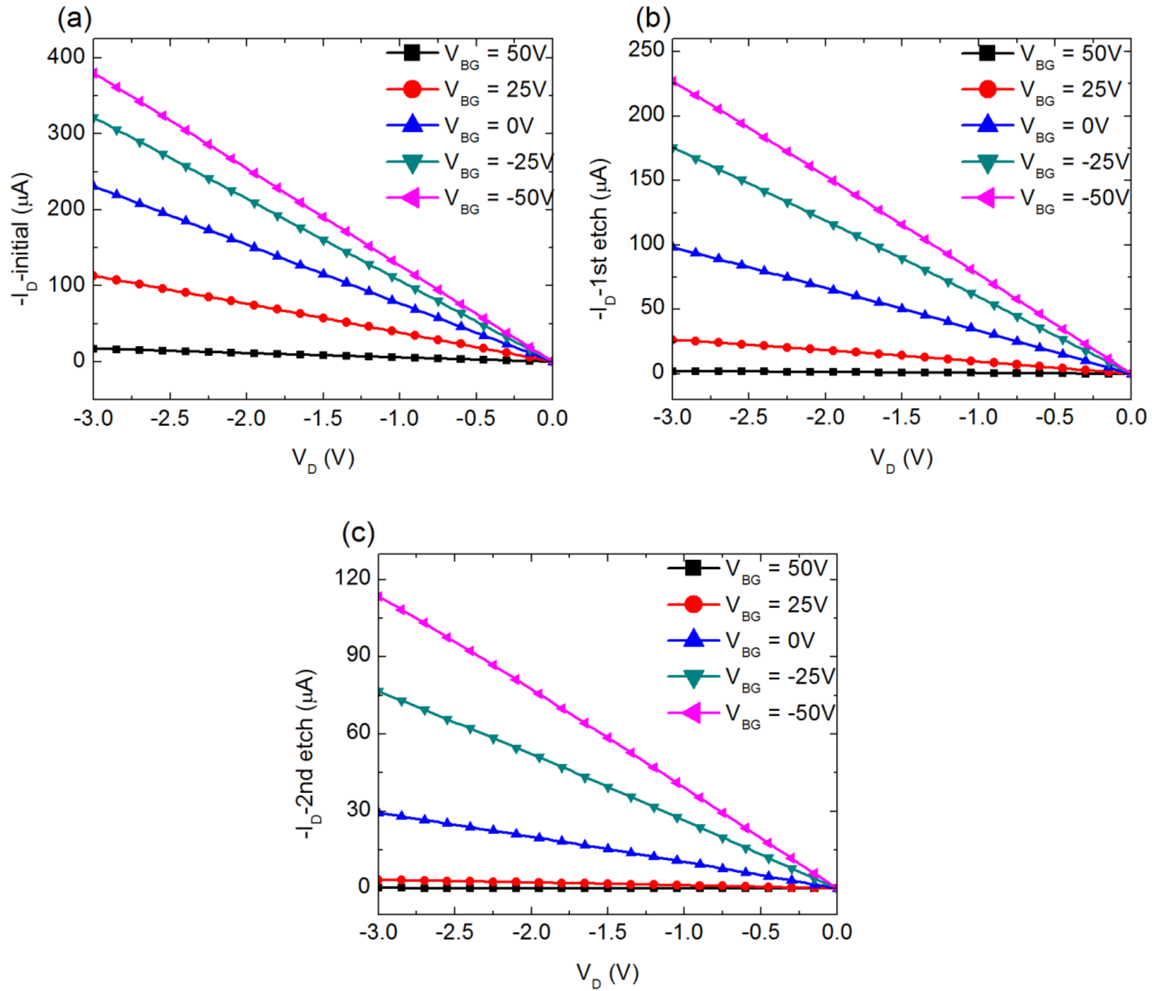


Figure 4.8: Output Characteristics (drain current, -I_D Vs drain bias, V_D) of BGFET for different back-gate voltages at different stages of plasma treatment. (a) Initial (b) After 1st etch (c) After 2nd etch.

4.3.2 Top-gated FET

For a flake used in a back-gated configuration, mostly the layers closest to the substrate are influenced by the back-gate due to screening. On the other hand, plasma processing impacts the layers on top and may not impact the layers which are under greater control of gate. Hence, in order to assess the true impact of O_2 plasma thinning on electrical performance, it is necessary to fabricate top-gated device on plasma treated

surface. We have successfully fabricated top-gate stack on the above mentioned BGFET and demonstrated well-behaved top-gated operation. To our knowledge, this is the first demonstration of TGFET fabricated on any flake of 2D layered materials of recent interest (graphene, TMDs etc.) which has gone through any type of flake thinning process.[67–71]

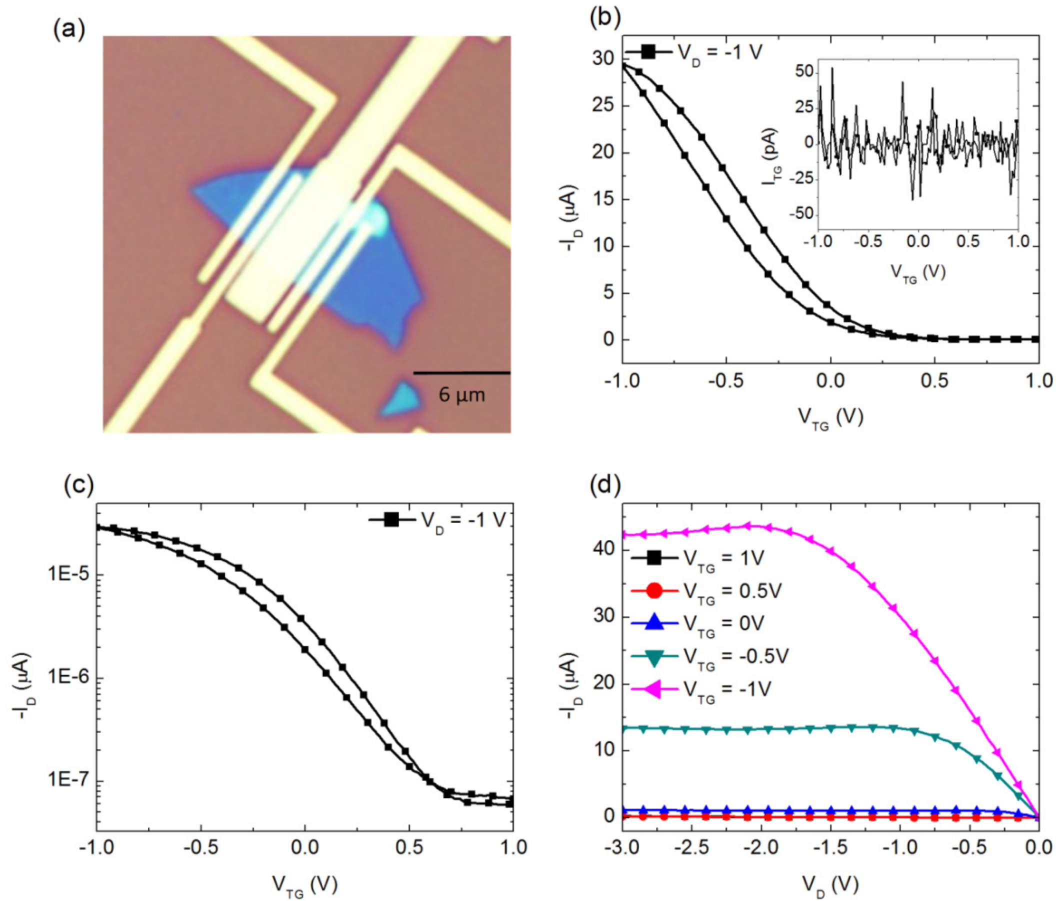


Figure 4.9: Electrical characteristics of top-gated FET (TGFET) with unbiased back-gate. (a) Optical Image of the TGFET. (b) Transfer characteristics for V_D = -1V in linear scale for bidirectional V_{TG} sweep. Inset shows top-gate leakage current. (c) Transfer characteristics for V_D = -1V in log scale for bidirectional V_{TG} sweep. (d) Output characteristics for different top-gate voltages.

The optical image of the fabricated TGFET is shown in Figure 4.9 (a). The transfer characteristics are shown in Figure 4.9 (b) with an unbiased back-gate. The device turn-on voltage is close to 0V. The hysteresis is relatively small. The inset of Figure 4.9 (b) shows top-gate leakage current, which is negligible (maximum ~50 pA) compared to both device on-state and off-state currents. The small values of gate leakage and hysteresis are suggestive of a robust top-gate with low interface and bulk traps in gate oxide. The deviation of I_D-V_{TG} characteristics from linearity at high negative gate voltage is due to (i) mobility degradation as a function of vertical gate field and (ii) source/drain access resistance.[72] The top-gate capacitance value was extracted to be 318 nF/cm^2 from separate MIM structures and this value is similar to value reported in another study using the same dielectric.[73] The extracted field-effect mobility for TGFET is 57 cm^2/Vs, which is also close to the mobility value of BGFET after 2nd etch (71 cm^2/Vs). This suggests that the top layers of the flake are of the same quality as the bottom layers and our top-gate processing does not introduce any significant damage to the device performance. The transfer characteristics are plotted in log scale in Figure 4.9 (c). The on-off ratio is close to 10^3 for the gate voltage range of -1 to 1 V. The output characteristics are plotted in Figure 4.9 (d) for different top-gate voltages. There are distinct linear and saturation regions. The characteristics are similar to long channel, square law device.

For the top-gated characteristics discussed above, the back-gate terminal was kept unbiased / floating. The back-gate terminal assumed some unintentional potential level based on its surrounding electrostatics. More controlled measurements were carried out in a dual-gated configuration, where the top-gated transfer and output characteristics were evaluated under different back-gate bias conditions.

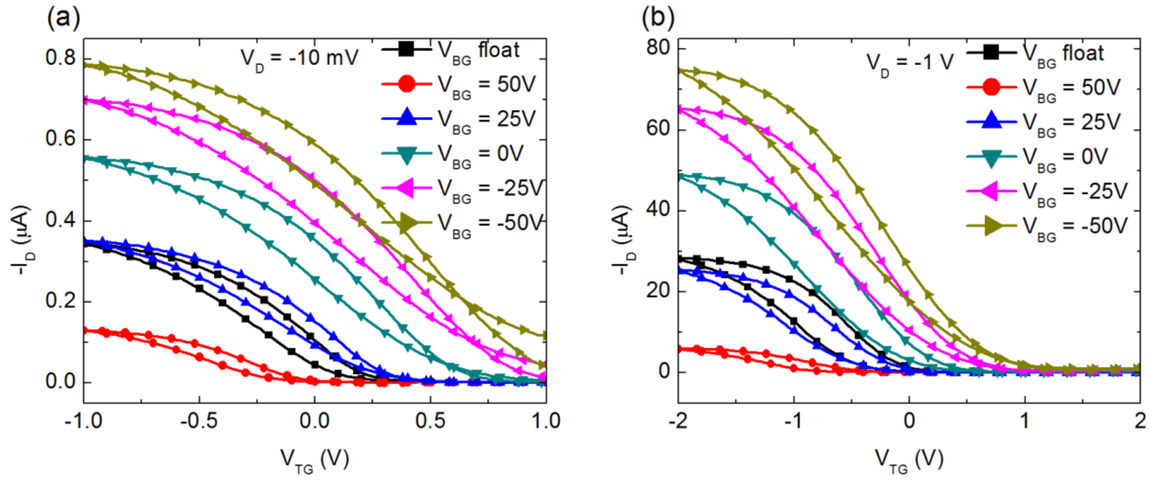


Figure 4.10: Top-gated transfer characteristics under different back-gate bias conditions. (a) V_D = -10 mV (b) V_D = -1V.

The top-gated transfer characteristics under different back-gate bias conditions are shown in Figure 4.10 (a) and 4.10 (b) for -10 mV and -1 V drain bias, respectively. As can be seen from both figures, the characteristics for floating back-gate condition roughly coincides with V_{BG} = 25 V. As the back-gate voltage is becoming more negative, it is assisting the top-gate more to draw holes in the channel of this p type FET. Thus, threshold voltage for top-gated characteristics is becoming more positive and the current level is higher due to higher available overdrive. The top-gated output characteristics for different top-gate and back-gate voltage configurations are presented in Figure 4.11.

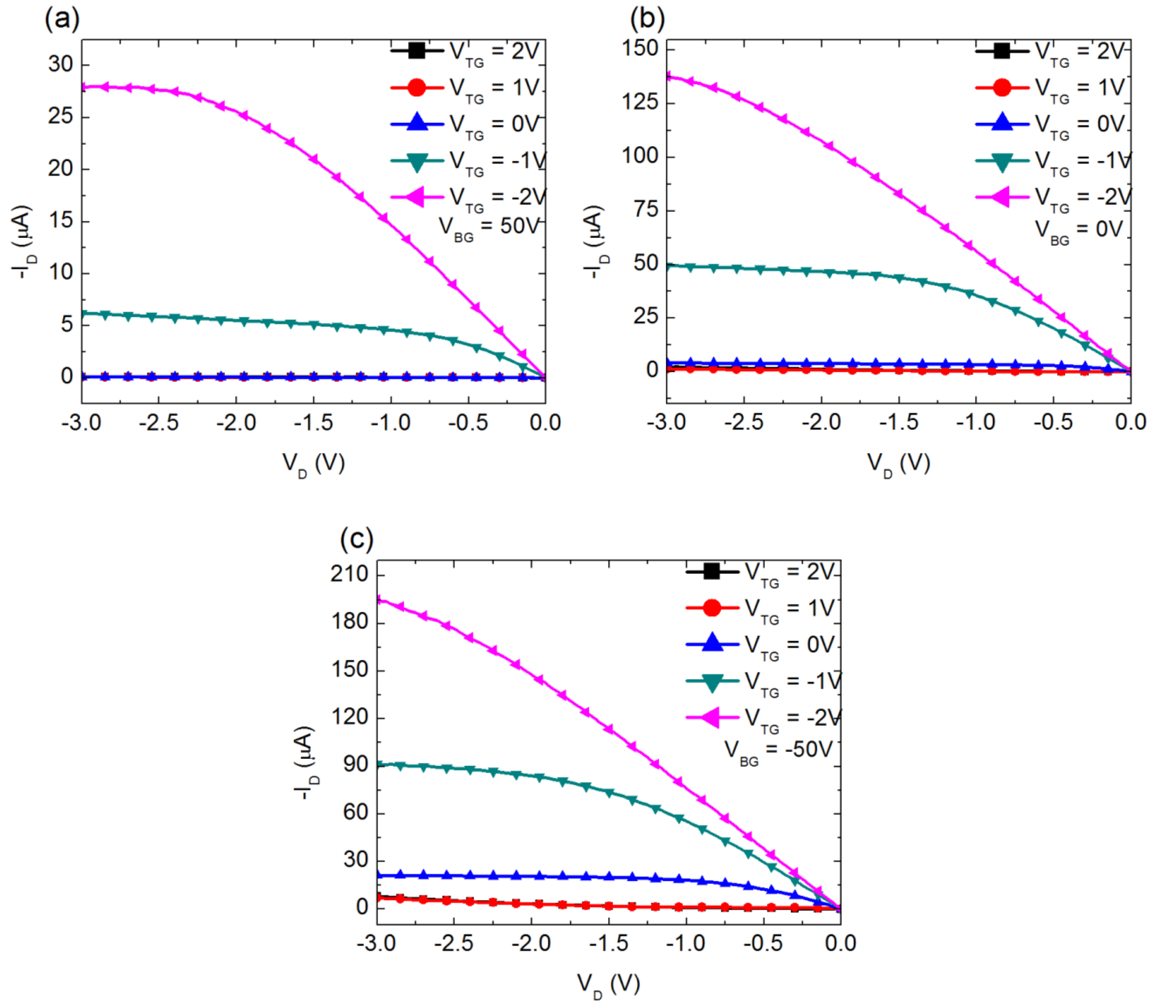


Figure 4.11: Output characteristics for different top-gate voltage, V_{TG} under different back-gate voltage, V_{BG} conditions. (a) V_{BG} = 50 V, (b) V_{BG} = 0 V, and (c) V_{BG} = -50 V.

Electrical Data from another high quality device are shown in Figure 4.12. The optical images before and after plasma treatments are shown in Figure 4.12 (a). The reduction in thickness after plasma treatment is clear from the contrast change. Transfer characteristics before and after plasma treatment are shown in Figure 4.12(b). The drain bias is -10 mV. Threshold voltage moved towards zero back-gate voltage from negative

value after plasma treatment. For the initial transfer curve, the peak trans-conductance (g_m) value is not available due to high negative value of threshold voltage. The maximum available value of g_m is used to extract the field-effect mobility and it is 176 cm^2/Vs. The field-effect mobility after plasma treatment is 213 cm^2/Vs. Even though we cannot compare these mobility values directly (due to unavailability of peak g_m value), the drive current increased after plasma treatment for same amount of overdrive, as shown in Figure 4.12 (c), which suggests better mobility value after plasma treatment. We also fabricated functional and well-behaved top gate stack successfully, as shown in Figure 4.12 (d). The extracted field-effect mobility is 208 cm^2/Vs, which is almost same as the value after etching. The transfer characteristics are plotted in log scale in the inset of Figure 4.12 (d). An excellent on-off ratio of ~ 10^5 is achieved for the TGFET.

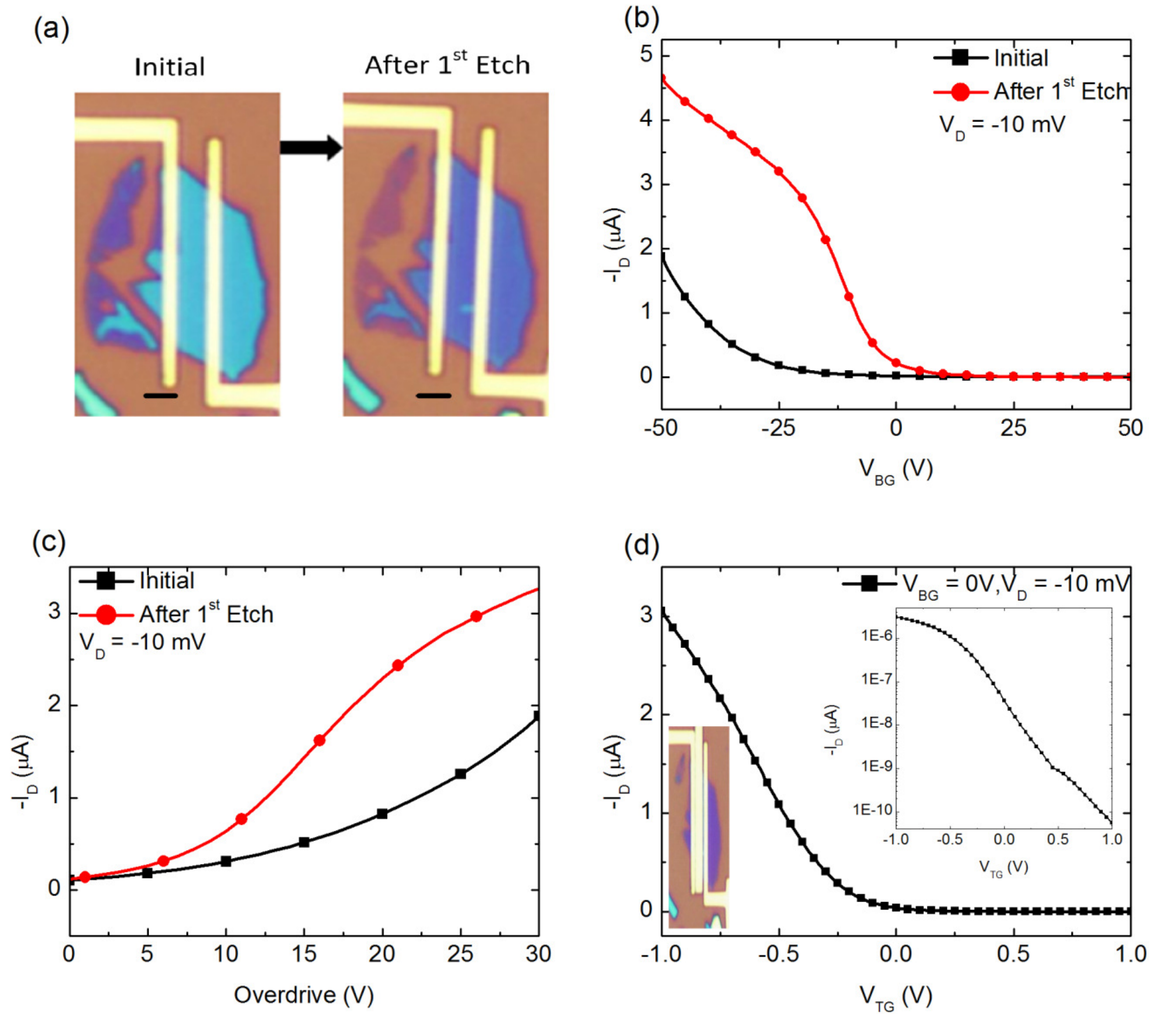


Figure 4.12: Transistor data for another device with thinned flake. (a) Optical images before and after O_2 plasma etch. Scale bar is 1 μm. (b) Back-gated transfer characteristics before and after etching at V_D = -10 mV. (c) Device current plotted with available overdrive for BGFET. (d) Top-gated transfer characteristics with V_{BG} = 0 V and V_D = -10 mV. Inset shows the same plot in log scale. An optical image of the TGFET is included at the bottom left corner.

4.4 Spectroscopic Analysis

In addition to the microscopic and electrical analysis, several other spectroscopic analyses such as Raman, XPS and TOF-SIMS were carried out, which have helped us to understand the chemical impact of O_2 plasma treatment on BP. The results of these analyses are presented below.

4.4.1 Raman Spectroscopic Analysis

Raman analysis was carried out in a Renishaw In-Via Raman microscope using 532 nm laser excitation. The laser power was kept at a low value in order to avoid any laser induced heating and damage. Optical images of a BP flake at different stages of the thinning process are presented in Figure 4.13 along with their associated Raman spectra. The scans were carried out in the nominally same position at all the stages of the thinning process. The Raman spectra at all stages of the thinning process show the characteristic BP peaks at ~365 cm^{-1}, ~440 cm^{-1} and ~470 cm^{-1}, which correspond to A_g^1, B_{2g} and A_g^2 peaks, respectively.[74] There is another peak at ~521 cm^{-1}, which corresponds to Si and originates from the underlying substrate. The gradual increase in Si peak intensity is an indication of the flake getting thinner after each etching step. The preservation of all characteristic peaks after the etching steps indicates that overall crystalline structure of the flake is preserved after O_2 plasma etching. However, it should be noted that the depth of penetration of the Raman laser is higher than the flake thickness at all stages, which is evident from the presence of Si peak signal from the substrate. Hence, these spectrums may not show surface sensitive features, since signals are averaged out for the total flake thickness.

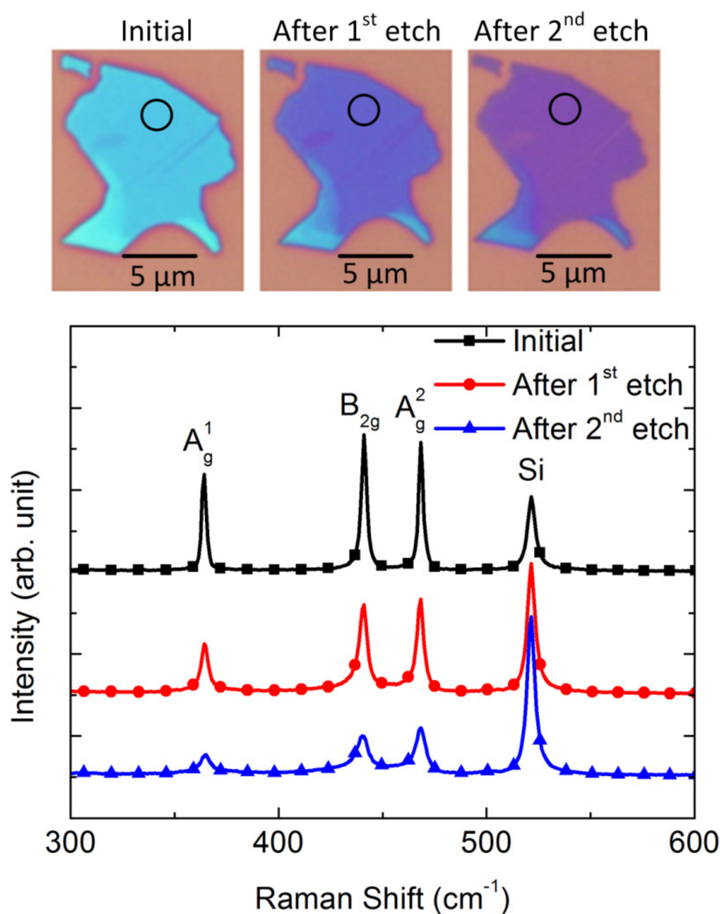


Figure 4.13: Raman Analysis of a thinned BP flake at different stages. The black circles in the optical images indicate the scan spot. The associated Raman spectra are shown below the optical images.

4.4.2 TOF-SIMS Analysis

The O_2 plasma etching process affects the topmost remaining layer of the BP flake to the greatest extent and may not affect the bulk of the flake at all. Therefore, in order to understand the chemical impact of plasma treatment, it is critical to analyze the surface of the flake with minimal interference from bulk. TOF-SIMS is a widely used, highly surface sensitive technique, which is capable of analyzing surface layers without interference from bulk. We have analyzed exfoliated BP flakes with TOF-SIMS (ION-

TOF GmbH TOF.SIMS5) before and after O_2 plasma treatments. A 30 kV Bi^{1+} analysis ion beam was used for sample probing, while a Cs^{1+} sputter ion beam with 1 kV energy was used for removing sample material layer-by-layer. The analysis ion beam was rastered over an area of 150 x 150 μm^2, whereas the sputter ion beam was rastered over an area of 250 x 250 μm^2 to prevent any crater-edge effects in the collected data.[75] The sputter ion beam was used for 5 second duration, when indicated.

The TOF-SIMS maps of 5 different ionic species (P-, O-, PO-, PO_2-, PO_3-) from a BP flake were tracked to illustrate the changes in the flake surface through processing. As-exfoliated BP flake shows high yield for chlorine (Cl-), which obstructs signal from other ionic species. Chlorine contamination from atmosphere is very common in TOF-SIMS analysis for many different materials.[76] Negative ion yield is highest for Chlorine due to its highest electronegativity. Therefore, the BP flake was sputtered with Cs^{1+}beam to remove chlorine contamination and expose the BP surface, which was then analyzed with Bi^{1+} ion. The secondary ion maps, after Cs^{1+} sputter beam treatment to remove surface contamination, are shown in Figure 4.14 before the O_2 plasma treatment.

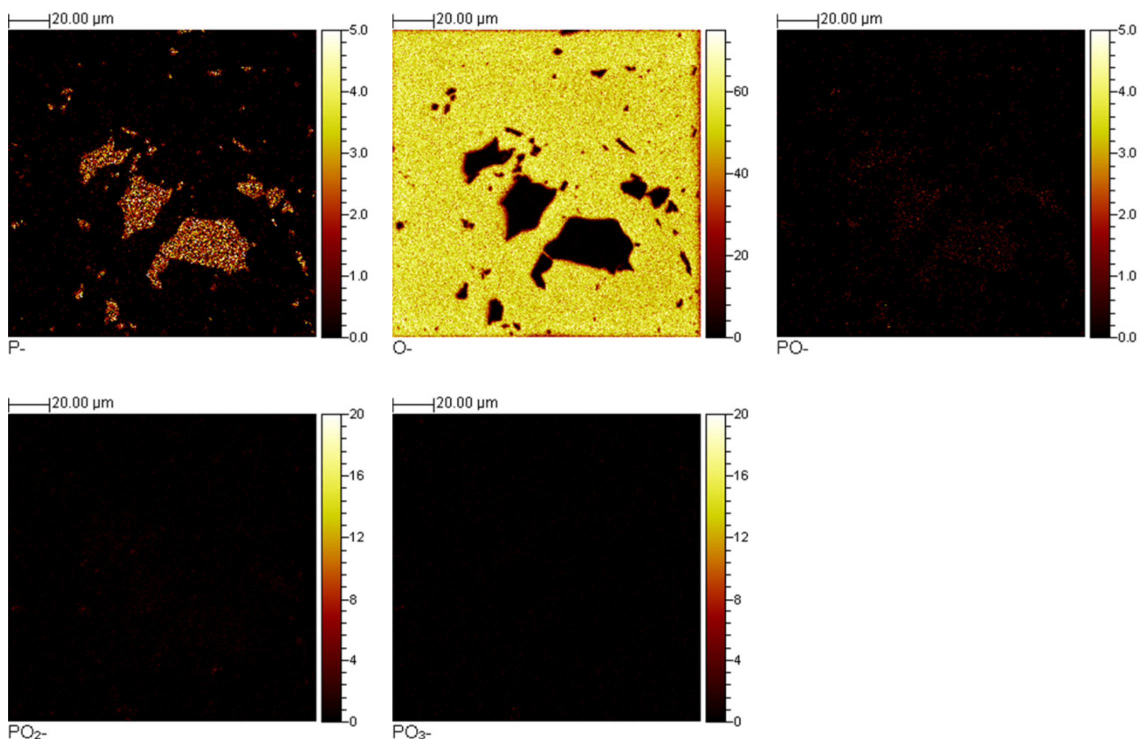


Figure 4.14: TOF-SIMS mapping for BP flakes before O_2 plasma treatment.

There are significant counts for P- on the BP flakes, which are expected from elemental phosphorus of BP. There are also small, but distinct counts for PO-, suggesting the presence of oxidized species on as-exfoliated BP surface. There are no detectable amounts of O-, PO_2- and PO_3- on the flakes. It should be noted that counts in ion maps cannot be directly correlated with concentration since the former depends on ionization probability. For example, trace amount of chlorine contamination gives very high count in ion maps because of its high ionization probability.

The TOF-SIMS mapping after plasma treatment of the BP flakes are presented in Figure 4.15. There was no chlorine contamination after plasma treatment; hence no sputtering with Cs^{1+} was necessary and the topmost layer of the plasma treated flake was analyzed. There are obvious changes in all five analyzed ion species. There is no

detectable P- signal, which suggests that the topmost layer is not BP. The O- signal is almost uniform across the flakes and SiO_2 substrate. Signal count for PO- did not increase significantly, but the areal density increased by a small amount on the flake. Most importantly, there are significant increases in signal counts for PO_2- and PO_3- species compared to the respective ion maps before plasma treatment. The complete absence of P- and strong signals from PO_2- and PO_3- demonstrate the fact that the top surfaces of BP flakes oxidize upon O_2 plasma treatment. More elaborate TOF-SIMS analysis and study are necessary in order to know the exact chemical composition of the oxidized species, which is beyond the scope of this work.

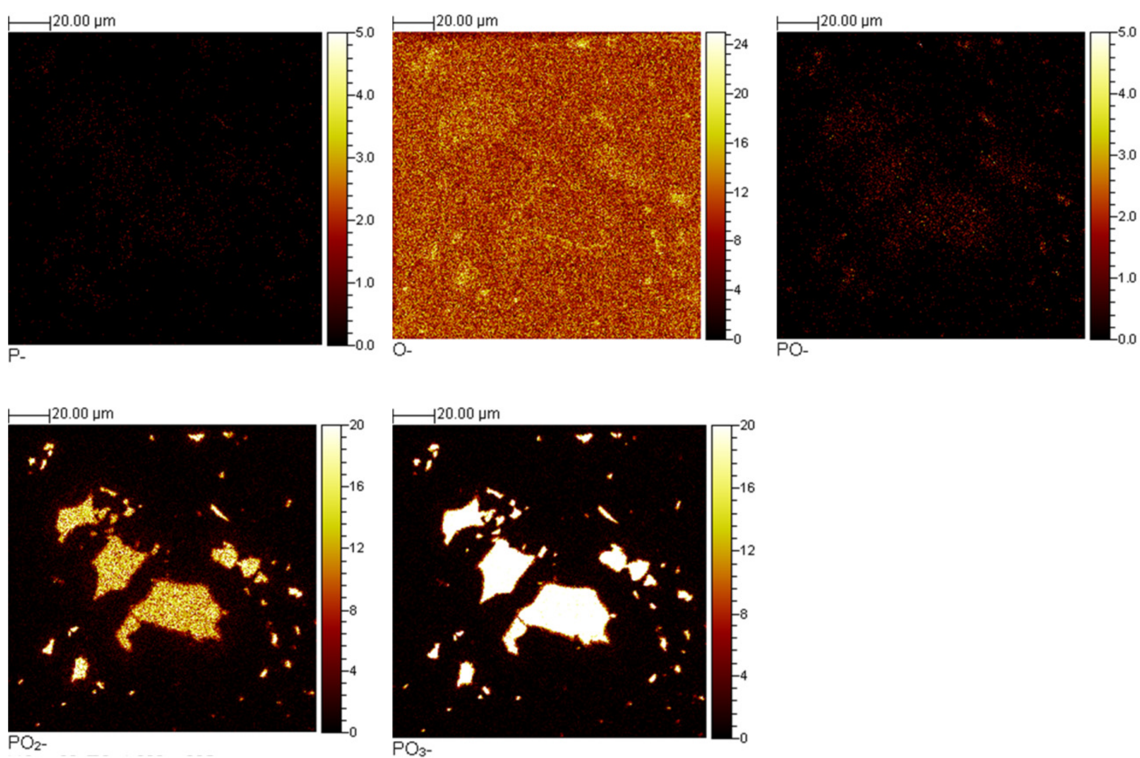


Figure 4.15: TOF-SIMS mapping for BP flakes after O_2 plasma treatment.

Operational FETs with good drive currents were fabricated on thinned flakes. The relatively small change in drive current for BGFETs with thinning suggests that the oxidized layer formed after thinning is not very thick. To further verify this conjecture, we sputtered the O_2 plasma treated flakes with 1 kV Cs^{1+} beam for a short duration (5 seconds) and analyzed them afterwards. The TOF-SIMS mapping of the plasma treated flakes after sputtering are shown in Figure 4.16. There is significant increase in counts for P- map compared to after plasma treatment case (Figure 4.15). The PO- signal count did not change much, but all other maps (O-, PO_2- and PO_3-) show significantly or completely diminished signal counts. These maps qualitatively look similar to the corresponding maps in Figure 4.14, which suggests that the oxidized layer formed after O_2 plasma treatment is thin and we can recover pristine BP with a short sputtering.

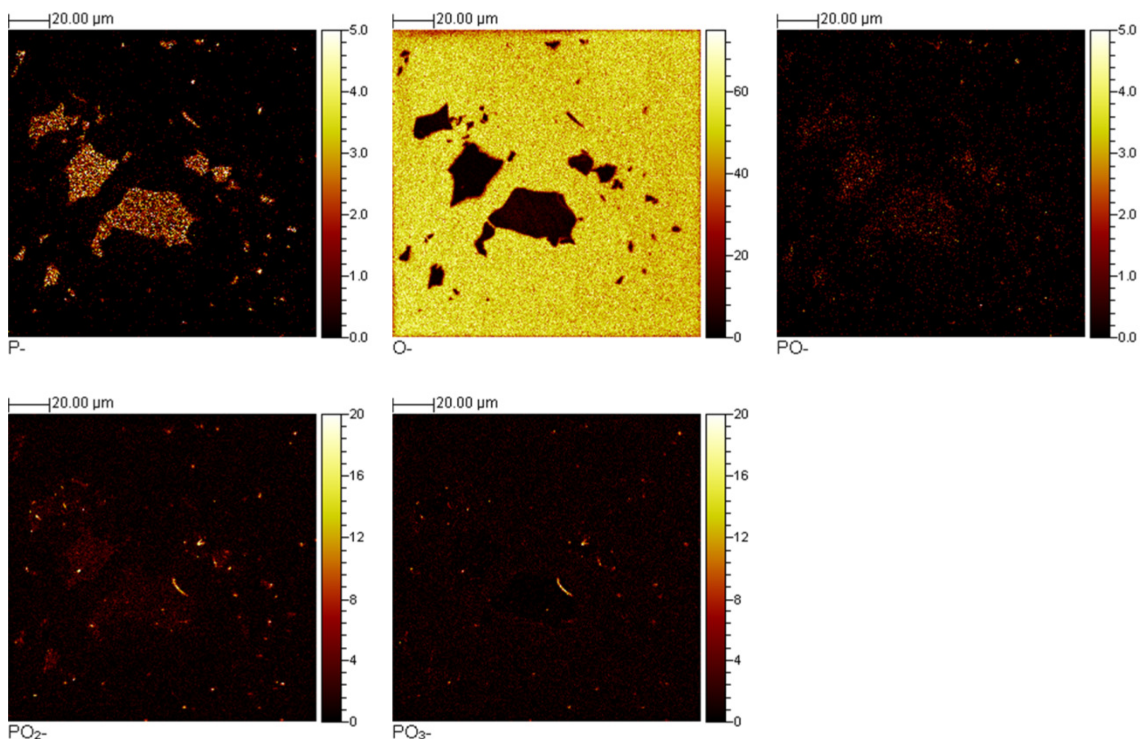


Figure 4.16: TOF-SIMS mapping for O_2 plasma treated BP flakes after sputtering with 1 kV Cs^{1+} beam for 5 seconds.

Determination of the oxidized layer thickness from TOF-SIMS analysis will be challenging. The etch rate of the oxide layer for the Cs^{1+} beam conditions is necessary to determine the thickness. However, to put things in perspective, 6 seconds of Cs^{1+} ion bombardment with 25% of the dose (charge/area) used in this experiment was required to etch one monolayer (~0.34 nm) of graphene.[77] All other beam conditions were very similar. Etch rate could be determined for graphene because of different carbon isotopes used in graphene growth. Direct comparison of graphene etch rate with BP is not possible due to different materials involved in these two cases. Nonetheless, we can make a rough and conservative estimate of the upper limit of the oxide layer thickness to be 1-2 nm.

4.4.3 XPS Analysis

In support of TOF-SIMS analysis, we also performed XPS analysis on BP before and after O_2 plasma treatment. XPS was carried out in a MULTIPROBE system from Omicron NanoTechnology GmbH with a monochromatic Al-Kα source. Our system does not support local or reduced area scan, so it was not possible to analyze particular flakes. Also, typical exfoliation process yields sparse distribution of flakes and the signal count is absent or insufficient for these samples. In order to have high density of flakes, a thin bulk flake was repeatedly pressed and slid on the substrate with a pair of tweezers. The sample surface was densely covered with relatively thick, quasi-bulk flakes. XPS analysis results before and after O_2 plasma treatment are presented in Figure 4.17. All spectra were calibrated to the binding energy of carbon (~284.8 eV). A charge neutralizer was used to compensate for electrostatic charging. These XPS spectra are very similar to the ones reported in previous studies of BP.[62,78]

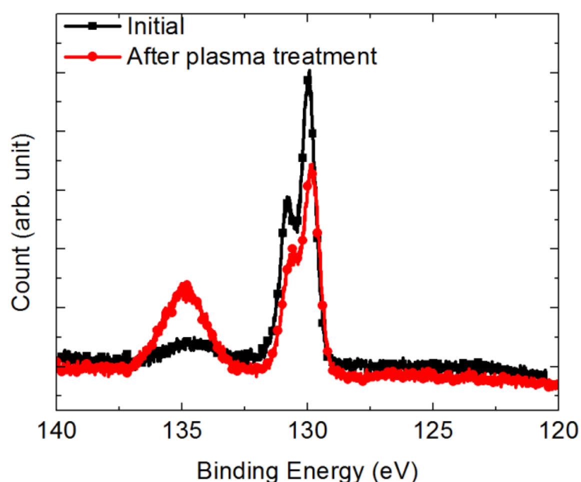


Figure 4.17: XPS spectrums of BP before and after O_2 plasma treatment.

P-2*p* spin-orbit splitting in high resolution XPS spectra is clearly observed in Fig. 4.17. It shows two peaks near ~129.5 eV and ~130.3 eV, corresponding to P-2$p_{3/2}$ and P-2$p_{1/2}$ peaks.[62,78–80] The rather broad peak near ~135 eV can be assigned to oxidized phosphorus species, PO_x.[62,81,82] Largely dominant fraction of the oxidized species is expected to be P_2O_5.[78]As can be seen from the spectra, area under the curve decreased for P-2*p* peak and increased for PO_x peak. These findings are consistent with the TOF-SIMS analysis results and clearly demonstrate the fact that some of the top layers of BP flakes are oxidized after O_2 plasma treatment. In order to have quantitative estimates, P-2*p* peak at ~130 eV was fitted with two separate peaks, corresponding to $2p_{1/2}$ and $2p_{3/2}$ peaks and the PO_x peak was also fitted with two corresponding peaks. Percentage concentrations of P-2*p* and PO_x were evaluated in order to estimate the relative percentage of P and PO_x in the analyzed materials.

Before plasma treatment, compositional analysis shows 82% phosphorus content and 18% PO_x content. The presence of PO_x species in as-exfoliated BP suggests that BP can readily oxidize in ambient. After plasma treatment, phosphorus content decreased from 82% to 60% and PO_x content increased from 18% to 40%. Hence, ~20% more of the analyzed material was oxidized after the plasma treatment.

These percentage concentrations can be correlated to the oxidized layer thickness. XPS is also a surface or near surface sensitive analysis technique. The emitted electrons are ejected only from the upper 0.5-5 nm, despite the high penetration depth of primary x-ray beam.[83]This has been verified in our system using Molecular Beam Epitaxy (MBE) grown layered material on Si substrate, where no signal from substrate could be detected for a 4 nm thick film. Therefore, the upper limit of the oxidized layer thickness can be estimated to be ~ 1nm, considering 5 nm as analyzed depth and 20% oxidation. A 40%

oxidation will result in 2nm oxidized layer. Thus, the XPS and TOF-SIMS results are in good agreement.

4.5 Stability of O_2 Plasma Treated BP

From the TOF-SIMS and XPS analysis, it is confirmed that there is a thin oxide layer formed on the BP surface after O_2 plasma treatment. This oxide layer can potentially serve as a barrier to BP degradation. To investigate this scenario, we analyzed the stability of an O_2 plasma treated BP flake. The optical images and corresponding AFM images are presented in Figure 4.18. The initial flakes have sharp 3D structure, as shown in Figure 4.18(b) and the thinner flake is ~13 nm. Unfortunately, the flake degraded after 28 hours of storage in ambient. This is not evident from the optical image of Figure 4.18(a) but AFM scan reveals that the corner of the flakes rounded and the ~13 nm flake became ~20 nm. This type of volume expansion has been reported previously and attributed to moisture absorption.[63] The degradation is more severe after ~100 hours and showed up even in the optical image. The uniformly thick initial flakes became more like dome shaped and the flake height became ~45 nm. Thus from our data, we conclude that the few nm thin oxidized layer resulting from O_2 plasma treatment is not capable to act as a protective barrier.

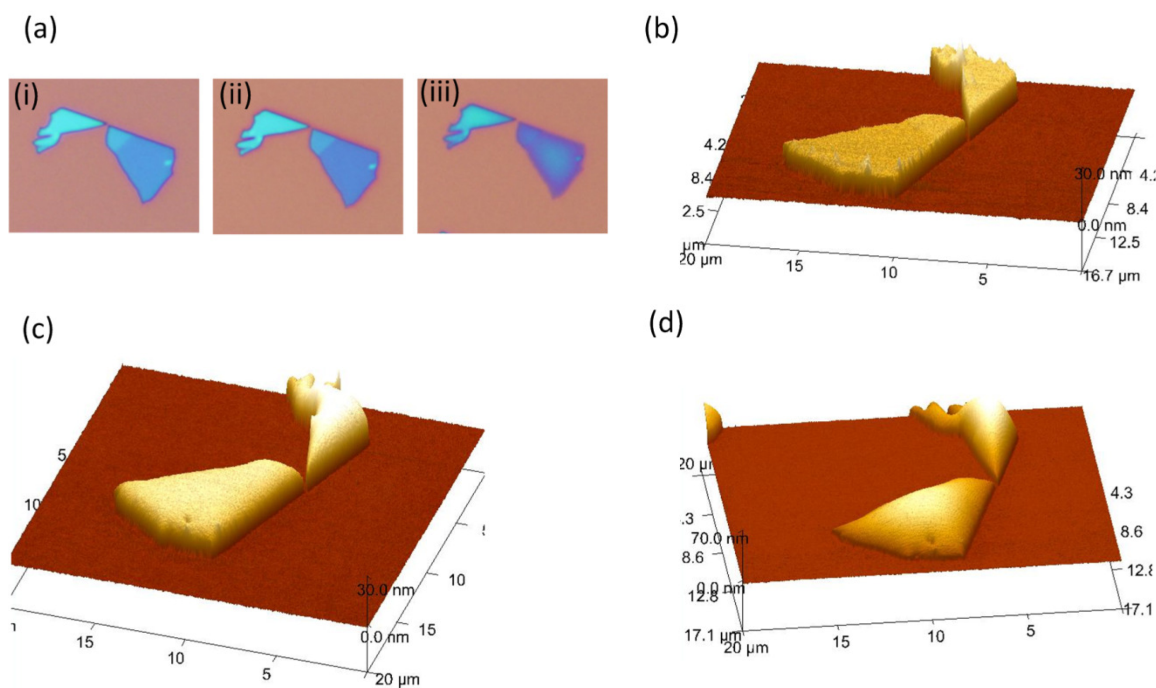


Figure 4.18: Plasma treated BP flake stability. (a) Optical images at different stages; (i) Initial, (ii) After 28 hours (iii) After 100 hours. (b) 3D AFM image of initial BP flakes. (c) 3D AFM image of BP flakes after 28 hours. (d) 3D AFM image of BP flakes after 100 hours.

Chapter 5: High Frequency Performance of Two-Dimensional Materials Based FETs and Their Circuit Applications

The work presented in the previous chapters encompassed various processing techniques which were employed to improve DC performance of two-dimensional materials based FETs. However, two-dimensional materials such as graphene, BP etc. also hold great potential for high frequency applications. Recently, graphene based radio frequency receiver has been fabricated in 200 mm silicon fabrication facilities, which shows the viability of commercial applications of graphene based RF circuits.[84] Ultra-high carrier mobility and sub-THz transit frequency make graphene FET a promising candidate for high frequency applications. In addition to using graphene as a channel material for FET in conventional circuits like amplifier or LNA, the ambipolar transfer characteristics of graphene FET makes it possible to perform useful circuit operations with simpler implementation. Frequency multiplication is one such application which is going to be investigated in this chapter. Frequency multiplier operating in GHz frequency range was demonstrated with the simplicity of a single FET and high spectral purity.[b]

As mentioned in the previous chapter, with graphene's isolation, many other two-dimensional (2D) layered materials have got renewed interest for FET applications. Layered black phosphorus (BP) is a recent addition to the 2D materials family. Moderate band gap and comparatively higher mobility than other semiconducting 2D layered materials have the potential to make BP a leading candidate for next generation FET for digital and high frequency applications. In this chapter, the high frequency performance

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of BP based FET is also discussed. Several circuit operations such as amplifier, FET mixer, demodulator were demonstrated with BP based FET.

5.1 High Frequency Characterization and Circuit Applications of BP FET

5.1.1 Device Fabrication

Few-Layer BP flakes were exfoliated from layered bulk BP crystal using scotch tape method and transferred onto 300 nm SiO_2 – lightly doped Si substrate. The sample was spin coated with PMMA right away to minimize environmental exposure related degradations. Suitable flakes for device fabrication were identified using optical microscope. The source drain contacts were patterned in ground-signal-ground (GSG) structure with electron beam lithography. 45 nm Ni – 20 nm Au stack was deposited as contact metal using electron beam evaporation and liftoff. Two-finger gate structure was patterned using electron beam lithography. ~25 nm Alumina + ~45 nm Ni was deposited as the gate stack by electron beam lithography in the same deposition run and liftoff process.

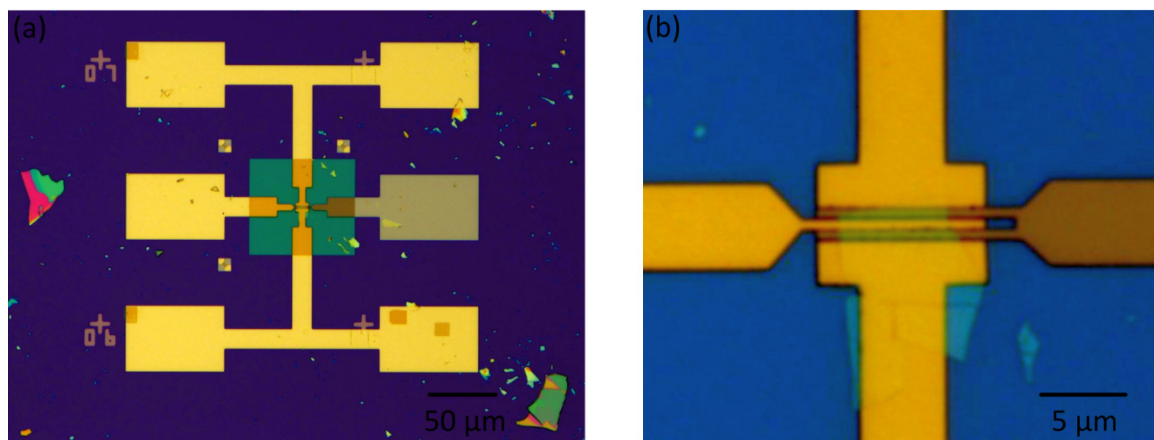

Figure 5.1: Optical images of fabricated BP FET (W / L = 13 µm / 0.5 µm). (a) Complete device. (b) Magnified image of channel area.

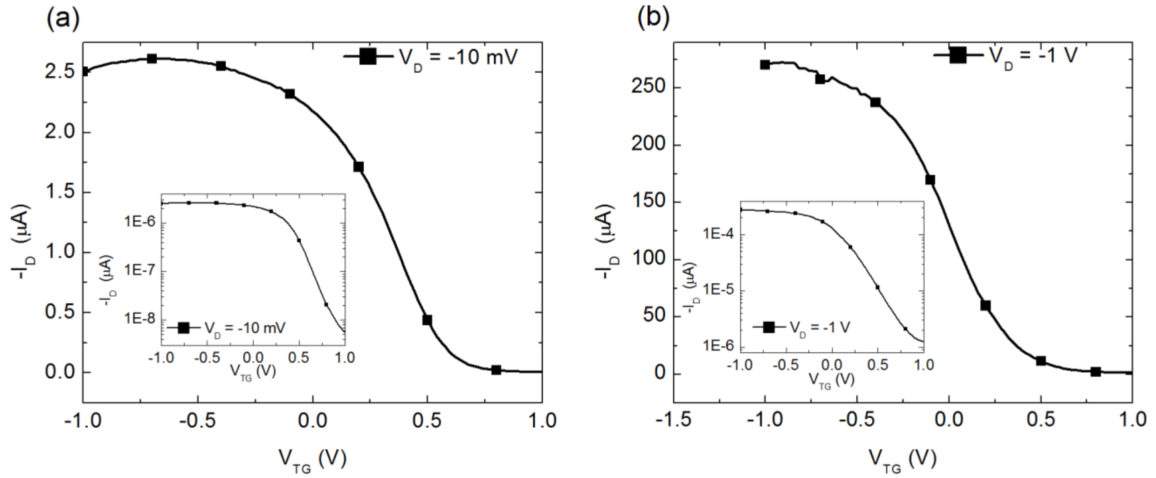

Figure 5.2: DC transfer characteristics. (a) V_D = -10 mV. (b) V_D = -1 V. Insets show corresponding log scale plots.

. Since the gate dielectric is locally deposited on the channel area only, the access regions between contacts and gate are exposed. Therefore, another ~40 nm Alumina layer was deposited covering the access and other exposed regions of the BP flake. Optical images of a fabricated BP FET with 500 nm channel length are shown in Figure 5.1.

5.1.2 DC and High Frequency Characterizations

The DC transfer characteristics of the fabricated BP FET for V_D = -10 mV and V_D = -1 V are shown in Figure 5.2 (a) and 5.2 (b), respectively. This is a p-type, depletion mode FET with positive threshold voltage around 0.5 V. The transfer characteristics plotted in log scale reveals decent on-off ratio of 100. The maximum trans-conductance is extracted to be ~ 380 μS/ μm with V_D = -1 V. The gate capacitance is ~308 nF / cm^2, which was obtained from separate MIM structures fabricated along with gate stack. The field-effect mobility is evaluated from the peak value of trans-conductance and its value is ~90 cm^2/Vs for V_D = -10 mV and ~78 cm^2/Vs for V_D = -1 V.

For benchmarking high frequency performance of transistors, two of the most widely used metrics are unity current gain frequency, f_t and unity power gain frequency,

f_{max}. The former is also known as transit frequency and the latter is also known as maximum oscillation frequency. Transit frequency, f_t is defined as the frequency at which current gain (ratio of output signal current at drain and input signal current at gate for a common source amplifier configuration) becomes unity for a short circuit output. Maximum oscillation frequency, f_{max} is the frequency at which maximum available power gain becomes unity. Both f_t and f_{max} depend on intrinsic device parameters, as well as extrinsic factors. For example, transit frequency of a MOSFET is given by the following expression, including extrinsic effects[85]:

$$f_t = \frac{g_m}{2\pi\sqrt{C_{gs}^2+2C_{gs}C_{gd}}}\{1-\frac{C_{gs}+C_{gd}}{C_{gs}^2+2C_{gs}C_{gd}}\,[g_{ds}\big(C_{gs}R_s+C_{gs}R_d+C_{gd}R_d\big)+g_m\big(C_{gd}R_d-C_{db}R_s\big)\,]\} \tag{5.1}$$

where, g_m and g_{ds} are intrinsic trans-conductance and output conductance, respectively, C's and R's denote capacitances in between two designated terminals and resistances of a terminal, respectively, g, d, s, b denote gate, drain, source and body terminals, respectively. Maximum oscillation frequency, f_{max} also has a complex expression like f_t. However, a simplified expression is given by the following equation[85]:

$$f_{max} = \sqrt{\frac{f_t}{8\pi R_g C_{gd}}} \tag{5.2}$$

where, R_g denotes gate resistance.

Transit frequency was measured for the BP FET using an Agilent Microwave Network Analyzer (VNA-E8361C) and cascade probe station with GSG probes. The device was biased around the maximum trans-conductance region with V_D = -2V and V_{TG} = 0V. Maximum oscillation frequency, f_{max} was extracted from the S parameter data obtained from the VNA using Agilent ADS software. Current gain (h_{21}) and power gain

(U) of the BP FET are plotted as a function of signal frequency in Figure 5.3 (a) and Figure 5.3 (b), respectively. The f_t and f_{max} values are ~ 3 GHz and ~ 7 GHz, respectively. It should be noted that both f_t and f_{max} values include effects of extrinsic parasitic components. Proper de-embedding structures are needed to be fabricated and measured to get the intrinsic values of f_t and f_{max}.

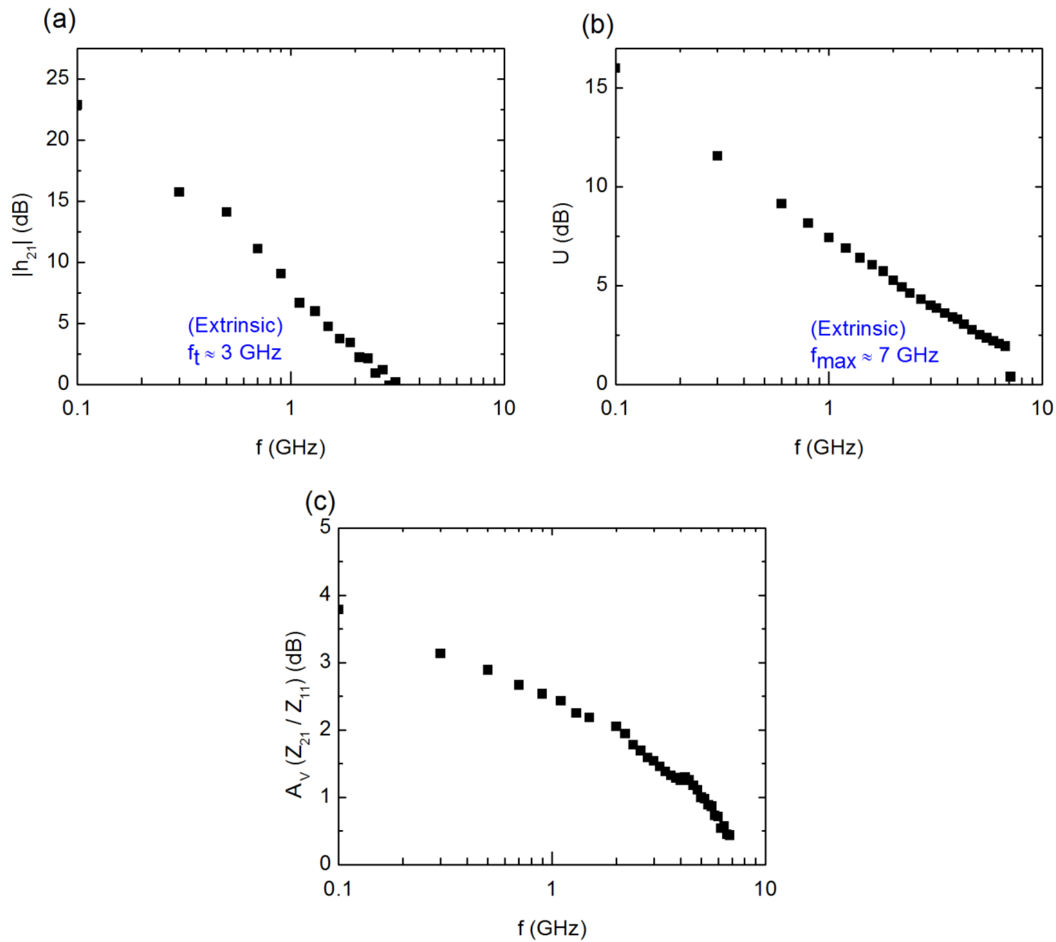

Figure 5.3: (a) Short circuit current gain, $|h_{21}|$ plotted as a function of frequency, f. Extrinsic transit frequency is ~ 3 GHz. (b) Power gain, U plotted as a function of frequency, f. Extrinsic maximum oscillation frequency is ~ 7 GHz. (c) Intrinsic voltage gain, A_v plotted as a function of frequency showing availability of voltage gain upto ~ 7 GHz.

The value of voltage gain, A_v can also be evaluated by converting measured scattering (S) parameters to impedance (Z) parameters. $A_v = Z_{21} / Z_{11}$ are plotted as a function of frequency in Figure 5.3 (c). The gain is 3.8 dB at 100 MHz and voltage gain is available till ~ 7 GHz.

5.1.3 High Frequency Circuit Applications of BP FET: CS Amplifier

A FET can be configured to be used as a signal amplifier. For a common source amplifier configuration, input signal is applied to gate terminal and output signal is collected at drain terminal, with proper DC biasing for the terminals. In general, the signal component at the drain terminal, v_{ds} can be expressed in terms of input signal at gate, v_{gs} by the following expression:

$$v_{ds} = c_0 + c_1 * v_{gs} + c_2 * v_{gs}^2 + c_3 * v_{gs}^3 + \text{other higher order terms} \qquad (5.3)$$

where, c_0, c_1 etc. are co-efficients of expansion. The second term gives rise to a signal which is proportional to the input signal frequency. Therefore, c_1 should be maximized for signal gain. This is achieved by biasing the device at peak trans-conductance point which is related to c_1.

The schematic of a common source amplifier is presented in Figure 5.4 (a). The RF input signal is combined with the DC gate bias with the help of a bias tee (inductor-capacitor combination). Drain side also has a bias tee to properly route DC and ac signals. The signal output is directly fed to an oscilloscope, which also acts as a high impedance (1 MΩ) load for the amplifier. The output signal waveform, obtained from the oscilloscope, is plotted in Figure 5.4 (b). The input is a 100 mV peak to peak, 1.42 MHz sinusoidal signal. The output is 200 mV peak to peak signal of same frequency. Thus, a voltage gain of 6 dB is achieved.

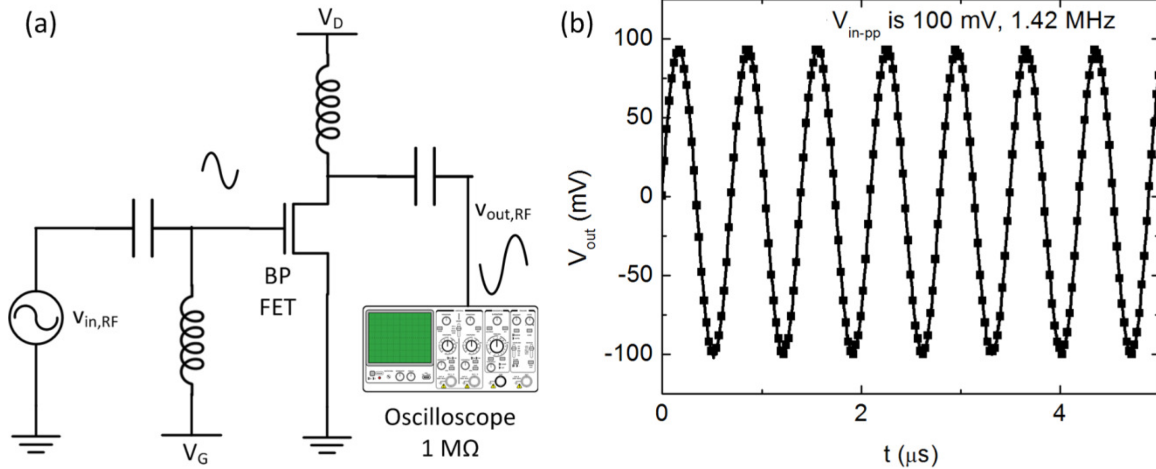

Figure 5.4: (a) Schematic of a common source (CS) amplifier configuration. (b) Output waveform of the CS amplifier for 1.42 MHz input signal, revealing 6 dB gain.

5.1.4 High Frequency Circuit Applications of BP FET: Mixer

A FET can be operated as a frequency mixer due to its non linear characteristics. Time domain multiplication of the RF signal with a Local oscillator (LO) signal results in sum and difference frequencies (Intermediate Frequency, IF) of the two signals, along with other harmonics and inter-modulation products. The schematic of a FET mixer is shown in Figure 5.5 (a). The LO signal is added to the RF signal using a power combiner and the composite (RF + LO) signal is fed to the gate terminal along with DC biasing through a bias tee. The output from drain terminal is fed to an oscilloscope with high impedance (1 MΩ).

If only the first and second order terms from equation 5.3 are considered, it becomes $v_{ds} = c_1 * v_{gs} + c_2 * v_{gs}^2$ with $v_{gs} = V_{RF}\cos(\omega_{RF}t) + V_{LO}\cos(\omega_{LO}t)$, where V and ω represent amplitude and angular frequency (= 2π * frequency) of the subscripted signal. The first order term in v_{ds} simply results in scaled RF and LO signal. The second term is:

$$v_{ds\text{-}2nd\ order} = c_2 * (V_{RF}\cos(\omega_{RF}t) + V_{LO}\cos(\omega_{LO}t))^2$$

$$= 2c_2 * (V_{RF}\cos(\omega_{RF}t)) (V_{LO}\cos(\omega_{LO}t)) + c_2*(V_{RF}\cos(\omega_{RF}t))^2 +$$

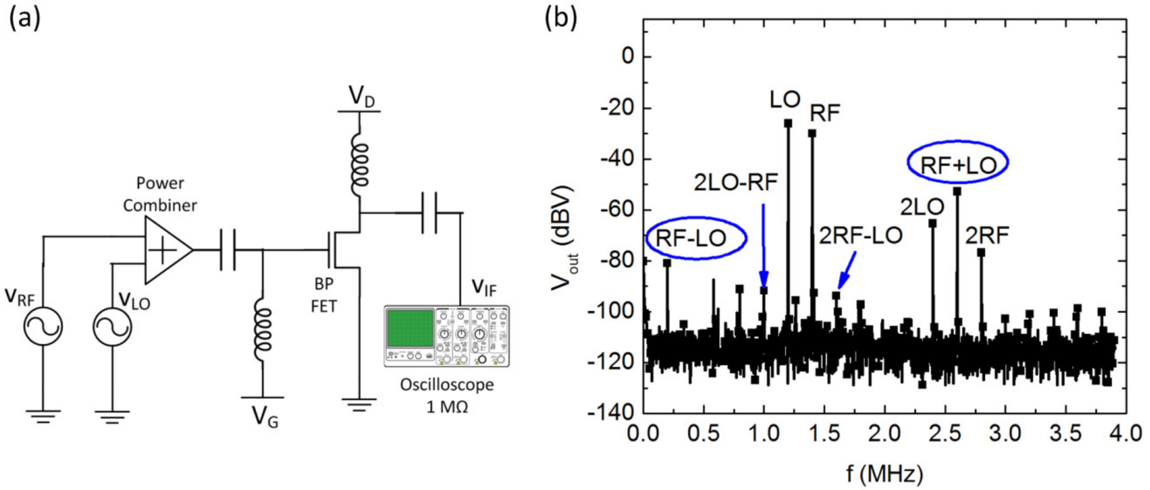

Figure 5.5: (a) Schematic of a single FET mixer configuration. (b) Output FFT spectrum obtained from oscilloscope. Both up-converted ($\omega_{RF} + \omega_{LO}$) and down-converted ($\omega_{RF} - \omega_{LO}$) frequency components are clearly present.

$$c_2*(V_{LO}\cos(\omega_{LO}t))^2$$

$$= c_2* V_{RF} * V_{LO}* [\cos(\omega_{RF} + \omega_{LO})t + \cos(\omega_{RF} - \omega_{LO})t] + \text{dc and } 2^{nd} \text{ harmonics}$$

Thus, desired IF signals ($\omega_{RF} + \omega_{LO}$ or $\omega_{RF} - \omega_{LO}$) are generated at the drain terminal. In reality, there are dc, higher order harmonics of RF and LO signals and their inter-modulation products ($p*\omega_{RF} \pm q*\omega_{LO}$ where p,q are integers) due to higher order terms in FET characteristics, along with the IF signal. Ideally, the device should be biased in non linear regime of transfer characteristics to maximize the second order component.

The FFT spectrum of the mixer output was obtained from oscilloscope and is presented in Figure 5.5 (b). The RF input is -10 dBm, 1.4 MHz and LO input is 300 mV, 1.2 MHz. The spectrum clearly demonstrates mixer operation with $\omega_{RF} + \omega_{LO}$ = 2.6 MHz and $\omega_{RF} - \omega_{LO}$ = 0.2 MHz. Some of the harmonics and inter-modulation products are designated in the figure; for example, $2\omega_{RF}$ = 2.8 MHz, $2\omega_{LO}$ = 2.4 MHz, $2\omega_{LO} - \omega_{RF}$ = 1 MHz, $2\omega_{RF} - \omega_{LO}$ = 1.6 MHz. It should be noted that all inter-modulations products have

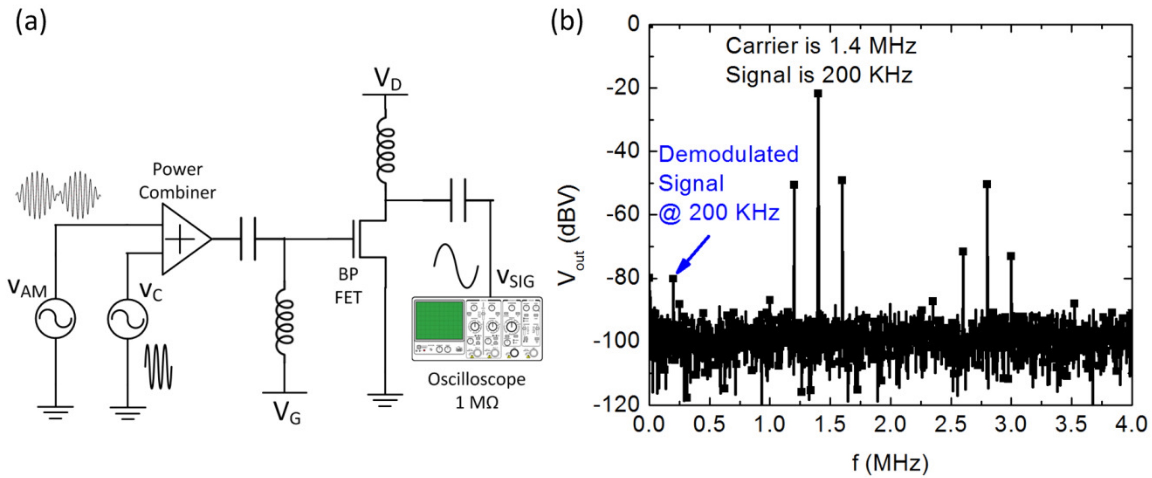

Figure 5.6: (a) Schematic diagram of AM demodulator. (b) Output spectrum of AM demodulator showing the recovered AM signal at 200 KHz along with other generated frequency components.

relatively lower values compared to the up-converted (ω_{RF} + ω_{LO}) and down converted (ω_{RF} - ω_{LO}) signals. The up-converted signal has high amplitude, thereby revealing a good conversion gain. The down-converted signal at ω_{RF} - ω_{LO} = 0.2 MHz is attenuated more mainly because of measurement setup. For example, 0.2 MHz is exactly at the lower limit of the available bias tee's frequency specification (pass-band).

5.1.5 High Frequency Circuit Applications of BP FET: AM Demodulator

The schematic of FET based AM demodulator is presented in Figure 5.6 (a). This is same as the mixer configuration discussed in the previous section with proper inputs for demodulator. One input is the incoming amplitude modulated signal and the other one is the carrier signal which is used for amplitude modulation in the first place. For an information signal of s(t) = V_S cos(ω_St) and carrier signal of V_C cos(ω_Ct), the generated AM signal is v_{AM} = V_C (1 + m V_S cos(ω_St)) cos(ω_Ct), where m = modulation index, which is 1 for 100% modulation. In our experiment, the AM signal is generated by signal generator using in-built AM function generator. This AM signal is combined with the

carrier signal using power combiner. This combined signal V_C (1 + m V_S cos(ω_St)) cos(ω_Ct) + V_C cos(ω_Ct) is fed to the gate of BP FET. Similar to the mixer analysis, the second order term in the FET characteristics generates a product term [V_C (1 + m V_S cos(ω_St)) cos(ω_Ct)] * [V_C cos(ω_Ct)] , which, in turn, recovers the signal [0.5*V_C^2 (1 + m V_S cos(ω_St))] through the trigonometric identity 2(cosX)(cosY) = cos(X+Y) + cos(X-Y).

The FFT spectrum of a BP based mixer output is obtained from the oscilloscope and presented in Figure 5.6(b). The information and carrier signal frequencies are 200 KHz and 1.4 MHz, respectively. The presence of signal component at 200 KHz clearly demonstrates that information signal is recovered from the AM input signal through demodulation. The signal level at 200 KHz is greatly attenuated mainly due to measurement setup limitations as mentioned before.

5.1.6 Impacts of Device Design and Measurement Setup on Performance

The device design and measurement setup are needed to be properly optimized in order to realize the full potential of black phosphorus in RF applications. There are several issues pertaining to both design and measurement setup, which are limiting the high frequency performance of the BP FET at present.

On the device side, channel length scaling for the BP FET will result in better RF performance with higher f_t and f_{max}. The fabricated devices in this work have 500 nm channel lengths with 150 nm spacing (access region) between the gate and source-drain terminals. Reduction of channel length should also be accompanied with a reduction in access region lengths. The best possible result will be obtained by a self aligned structure, but fabricating such a structure is challenging. Also, gate dielectric thickness can also be scaled down in order to have better electrostatic control of the channel and contact resistance should be minimized.

Thermal stress was found to be a significant reliability concern during high bias, continuous device operation. This is especially true for circuit measurements, when the device is operated continuously, while tuning the bias in order to improve performance. Devices which ceased to function during measurement usually had small black spots on the metal electrodes, suggesting damage due to self heating. Proper thermal management schemes should be incorporated in the device design.

Device and circuit performances are significantly impacted by measurement setup, at present. First of all, there is no matching network present at the input and output interface of the device. High frequency RF instruments, such as signal generator, network analyzer etc. usually have a standard 50Ω impedance termination. In absence of proper matching, there are significant signal reflections on both input and output ports of the device. Hence, the amount of signal power received at the input, as well as power delivered to the network analyzer from output, is reduced. The output side issue is alleviated during circuit measurements by using high impedance (1 MΩ) oscilloscope. Nonetheless, proper impedance matching is necessary to improve performance metrics such as gain. Possible implementation schemes include designing PCB board for matching and using external impedance tuner at the ports.

Another drastic impact on circuit performance stems from the frequency limitations of cables and equipments. The s parameter (f_t) measurements are robust to this since only high frequency coaxial RF cable and RF network analyzer are used. However, some equipments and cables had to be used during circuit measurements which were not designed to be used in the frequency range of experimental interest. As mentioned before, the down converted signal for mixer output and demodulator output, both 200 KHz, are highly likely to be attenuated by bias tees used in the experiment. A direct connection between signal generator and oscilloscope revealed 50% attenuation of signal at 350

MHz (upper frequency limit for oscilloscope), which is likely due to cable loss. During the circuit measurements, even though low loss RF cables were connected to the RF probe tips, the use of connectors and BNC cables to interface with the oscilloscope inevitably degrades signals. Therefore, the RF frequency used in the circuit measurements is limited to 1.4 MHz by the measurement setup issues, not the BP FET.

The detrimental impacts of the measurement setup are validated by the RF performance metrics for the BP FET used in amplifier measurement, which are presented in Figure 5.7. The device has an extrinsic transit frequency of ~ 2 GHz and extrinsic maximum oscillation frequency of ~ 6 GHz. More importantly, the device provides a gain of ~ 3.25 dB at 100 MHz and capable of producing signal amplification till 3-4 GHz. The gain curve is extrapolated in Agilent ADS software till 1 MHz and the gain value is 6.8 dB at 1 MHz, which is consistent with our experimental gain of 6 dB at 1.4 MHz. Therefore, with proper measurement setup, GHz range circuit performance can be expected from this BP FET.

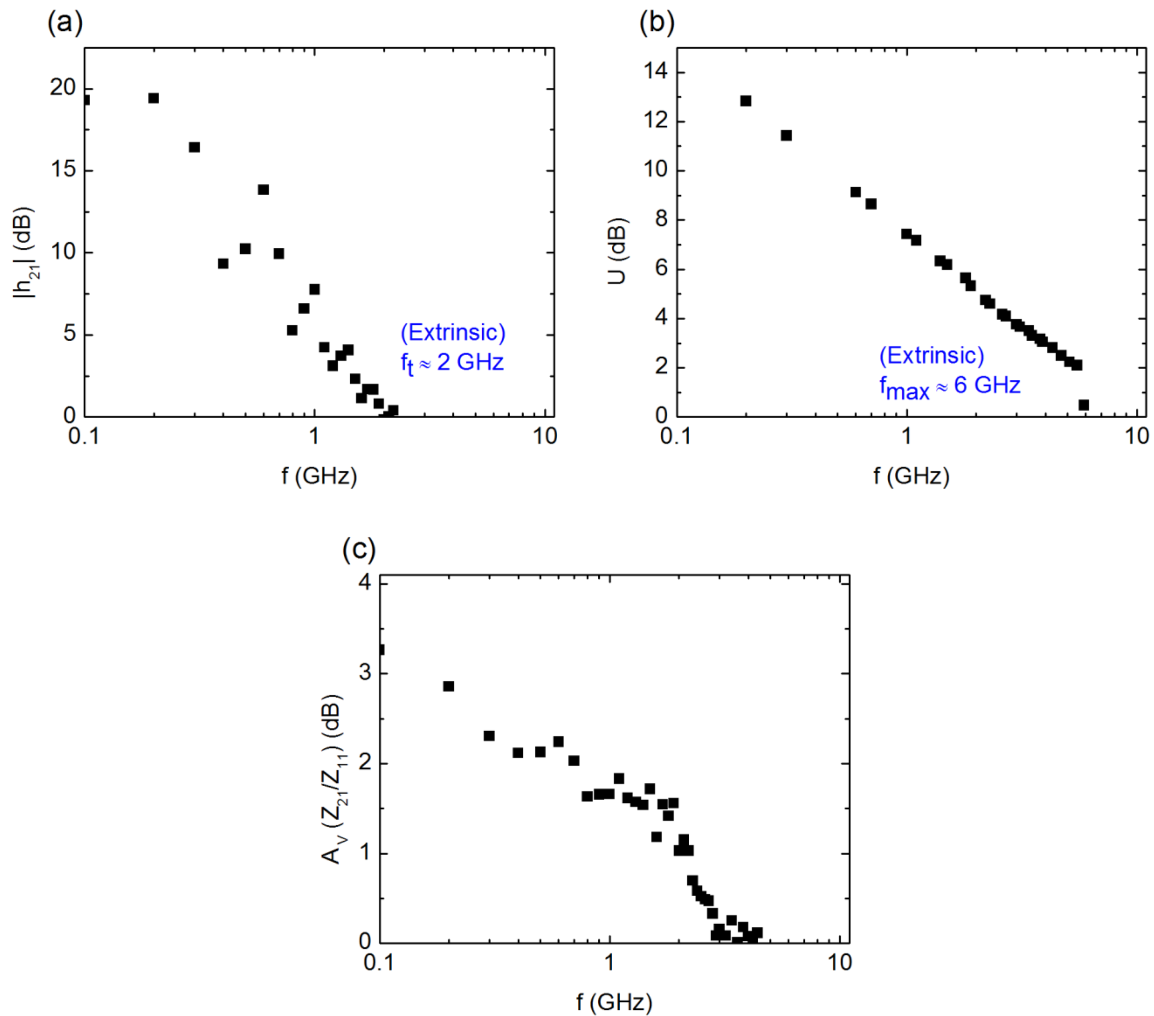

Figure 5.7: RF characterization of BP FET used in CS amplifier. (a) Short circuit current gain, $|h_{21}|$ plotted as a function of frequency, f. Extrinsic transit frequency is ~ 2 GHz. (b) Power gain, U plotted as a function of frequency, f. Extrinsic maximum oscillation frequency is ~ 6 GHz. (c) Intrinsic voltage gain, A_v plotted as a function of frequency showing availability of voltage gain upto ~ 3-4 GHz.

5.2 Frequency Multiplier with Graphene FET

In order to employ a graphene FET as a frequency multiplier, the FET is biased at minimum conduction point and a sinusoidal signal is superimposed on the DC bias. Therefore, in the positive half cycle of the sinusoidal signal, current is conducted by electrons while in the negative half cycle of the signal, current is conducted by holes in the same direction as electrons. Thus, the resultant signal at the drain will have a frequency component which is twice the input signal frequency.

In general, the drain voltage can be expressed in terms of gate voltage by the following expression[86]:

$$v_{DS} = c_0 + c_1(v_{GS}-V_B) + c_2(v_{GS}-V_B)^2 + c_3(v_{GS}-V_B)^3 + \ldots \qquad (5.4)$$

Where v_{DS}, v_{GS},V_B are total (signal + bias) drain voltage, total gate voltage and DC bias at gate, respectively and c_0, c_1, c_2 are polynomial co-efficients determined from FET transfer characteristics. Now if a sinusoidal signal $V_A \cos(\omega t)$ is superimposed at the gate terminal biased at $V_B = V_{Dirac}$,

$$v_{DS} = c_0 + c_1\, V_A \cos(\omega t) + c_2(V_A \cos(\omega t))^2 + c_3(V_A \cos(\omega t))^3 + \ldots \qquad (5.5)$$

The third term $c_2(V_A \cos(\omega t))^2$ can be expanded as $0.5*c_2V_A^2(1+ \cos(2\omega t))$, which gives rise to doubled frequency component. The co-efficient c_2 should be maximized and other coefficients should be suppressed in order to maximize spectral purity. The co-efficient c_2 is maximum when the device is biased at Dirac point, which is the most non-linear region of the transfer characteristics.

5.2.1 Device Fabrication

The fabrication flow of the top-gated graphene FET used in this study is illustrated in Figure 5.8(a). Monolayer graphene was grown on Cu foil and transferred to quartz substrate by wet transfer method.[87,88] Insulating quartz substrate was chosen for its atomically smooth surface and lower parasitic contribution compared to typical SiO_2-Si

substrate. The active area was patterned with EBL and O_2 plasma RIE. The second EBL step was used to pattern the source drain contacts in a ground-signal-ground structure. 50 nm Ni was deposited as contact metal by e-beam evaporation and liftoff process. After that, 1.5 nm Al was evaporated on the sample and oxidized in air which served as a nucleation layer for the subsequent ALD of 20 nm Al_2O_3 gate dielectric. Device fabrication was completed by defining the gate electrode by EBL and electron beam evaporation of 50 nm Ni. Fig. 5.8(b) shows an optical image of the fabricated GFET with channel length of 500 nm.

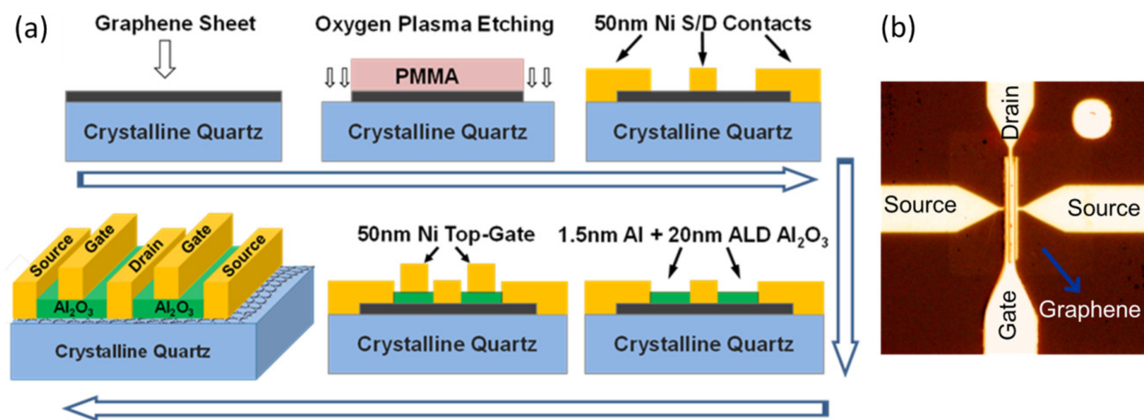

Figure 5.8: (a) Process flow for top-gated Graphene FET. (b) Optical image of a fabricated GFET in ground-signal-ground (GSG) structure, W/L = 50 µm/0.5 µm. © 2012 IEEE.

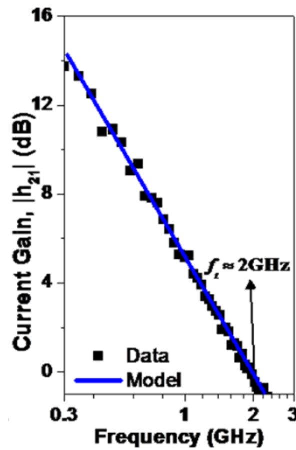

Figure 5.9: Short circuit current gain plot for GFET showing (extrinsic) transit frequency of 2 GHz.. © 2012 IEEE.

5.2.2 High Frequency Characterization and Frequency Doubler Operation

The short circuit current gain, measured as a function of input frequency, is shown in Figure 5.9. The data is fitted with a circuit model based on validated graphene compact model. The measured transit frequency, f_t is 2 GHz, which was obtained at peak trans-conductance point and includes all parasitic capacitances and resistances. The carrier mobility for this device is ~500 cm^2/Vs. The unity power gain frequency, f_{max} for this device is extracted to be ~1.8 GHz.

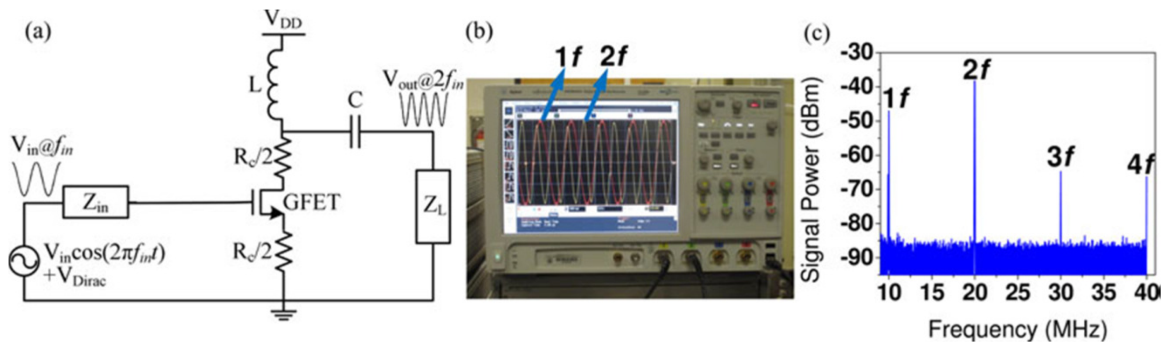

Figure 5.10: (a) Schematic of GFET frequency doubler. (b) Real time oscilloscope output showing frequency doubling operation with 1f = 1 MHz and 2f = 2 MHz. (c) Spectrum analyzer output with 10 MHz, 0 dBm input. © 2012 IEEE.

The schematic of the GFET frequency doubler is shown in Figure 5.10(a). The impedances seen by the GFET at both input (signal generator) and output (spectrum analyzer) sides were 50 Ω and no impedance matching network was used. Real time oscilloscope picture showing 1 MHz input signal and 2 MHz doubled signal is presented in Figure 5.10(b). The spectrum analyzer output with 10 MHz input signal, shown in Figure 5.10(c), also reveals frequency doubling operation with high spectral purity. More than 90% of the available power is at the doubled frequency.

Conversion gain (CG) is an important performance metric for frequency doubler. It is defined as the ratio between power available at doubled frequency and input power at fundamental frequency. The maximum achievable CG for this doubler is ~ -35 dB. The frequency response of the doubler is plotted in terms of the normalized CG with respect to its maximum value in Figure 5.11. The -3 dB frequency for the doubler is 3 GHz, which exceeds the transit frequency by 50%.

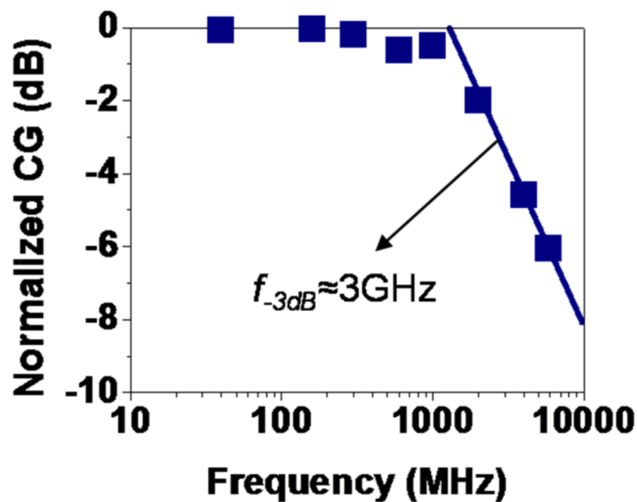

Figure 5.11: Normalized CG plotted with input frequency, revealing 3 GHz Bandwidth. © 2012 IEEE.

Chapter 6: Conclusion

6.1 Summary

In this work, several two-dimensional materials of recent interest have been explored for transistor applications. In the first part of this dissertation, the transfer process of CVD grown graphene was established and a number of empirical observations were made aiming towards improving that process. It was followed by the discussion of a performance improvement technique for FETs fabricated with the transferred graphene by HMDS surface treatment. 1.5× – 2× improvement in field-effect mobility was achieved, along with residual impurity reduction. The electrical data were supported by Raman spectroscopic analysis. The HMDS treatment results for monolayer and multilayer molybdenum disulfide based FETs suggest that this technique, in general, should be effective in improving electrical characteristics of ultrathin, two-dimensional layered materials based FETs. In the next part of the dissertation, an oxygen plasma etching technique was developed for thinning black phosphorus flakes in order to achieve good electrostatic control and enhanced performance. Detailed optical and atomic force microscopy measurements were used to characterize the process. Most significantly, well behaved, top-gated transistors were fabricated on thinned flake which demonstrates the usefulness of this process for getting flake of desired thickness for transistor application. Raman, TOF-SIMS and XPS analyses results reveal that a thin ~ 1-2 nm layer is oxidized upon the oxygen plasma treatment, while keeping the bulk of the flake intact. Lastly, high frequency performance of graphene and black phosphorus based FETs were investigated. Cut off frequencies in the gigahertz range were achieved for both graphene and black phosphorus based FETs. A number of circuits such as graphene transistor based frequency doubler, black phosphorus transistor based amplifier, mixer and demodulator were demonstrated and various performance bottlenecks from both device and

measurement setup perspectives were identified. In summary, through the investigation of several performance enhancing processing techniques and high frequency performance evaluation, this work achieved its goal by addressing a broad area encompassing material synthesis, device design, characterization and circuit implementations using two-dimensional layered materials of contemporary interest. The outcomes of this work also motivate the exploration in several new research directions and extensions, which are discussed in the next section.

6.2 Suggestions for Future Works

6.2.1 CVD Grown Graphene Transfer

The process described in chapter 2 has been extended to wafer scale graphene transfer. However, this wet transfer process can degrade the grown graphene quality due to interaction with several liquids such as acids and etchants. Also, this is a totally manual transfer process which depends on human skill and introduces inevitable sample to sample variations and uncertainties. Therefore, it is highly desirable to establish an automated or semi-automated dry transfer process with minimal manual manipulation and degradation. To this end, techniques such as wafer bonding, de-lamination of graphene from growth substrate etc. should be investigated.

6.2.2 Transistor Performance Improvement by HMDS Treatment

The biggest challenge in the HMDS treatment technique is the stability of the improved performance. HMDS treated samples return to their initial state after few days in ambient. Therefore, it is necessary to develop suitable capping technique to stabilize the improved performance. To this end, near room temperature physical vapor deposition or atomic layer deposition methods should be rigorously investigated to develop the capping layer. Capping mechanisms are complicated by the fact that most of the

overlayers deposited on graphene degrade the FET performance. It will also be interesting to compare the relative degradations with respect to initial device performances with and without HMDS treatment prior to overlayer deposition. Lastly, in order to conclusively establish the HMDS treatment as a general performance improvement technique for 2D layered materials based FET family, significant number of FETs based on a variety of available 2D materials need to be tested with HMDS treatment.

6.2.3 Black Phosphorus Flake Thinning with O_2 Plasma Treatment

Firstly, we concentrated our study on a particular plasma condition of 150 Watt, 200 mTorr pressure, 18 SCCM flow rate. It is instructive to explore the impact of varying these process conditions, especially plasma power. It may be possible to scale down the thickness of BP flake down to single layer with carefully tuned plasma conditions.

Secondly, as mentioned before, spectroscopic analysis reveals that a very thin oxide layer is formed on BP after O_2 plasma treatment. Formation of a high quality native oxide had been one of key enabler of Silicon electronics. Therefore, it will be very interesting to examine whether such an existing oxide layer can improve the interface between channel and gate stack. To this end, carefully controlled experiments need to be carried out with and without plasma treatment of BP channel before gate stack deposition. Uncertainty due to flake to flake variation can be eliminated by making both plasma treated and control device on the same flake.

Thirdly, the results of this O_2 plasma treatment process suggest that much weaker plasma conditions can be employed in a descum process in order to get rid of resist residue after lithography step, without adversely affecting the device performance. This can help to clean both the contact and channel area after their respective lithography.

6.2.4 High Frequency Characterization and Circuit Applications of 2D materials

As mentioned previously, improvement of device design and measurement setup will result in improved high frequency performances. Multi-finger FET layout, channel length and gate dielectric scaling, contact optimization, measurement components and cables capable of handling RF frequencies are some of the things to be implemented. Circuits using multiple FETs, such as cascade amplifier, differential amplifier etc., should be explored. Since BP has a thickness dependent finite band-gap, it offers the possibility of implementing both digital and analog circuits using same material. To this end, controlled fabrication of n-type BP FET is desired. For graphene based frequency multiplier, bi-layer graphene should be investigated in order to have larger second order term in FET transfer characteristics, thereby concentrating more power in the doubled frequency. Lastly, reliable device and circuit level simulation tools should be developed in order to optimally design FETs and circuits.

Appendix

A.1 CVD Graphene Transfer to Arbitrary Substrates

Step	Details
1	Monolayer graphene growth on 1 μm (nominal thickness) thick electron beam evaporated Copper (Cu) + 300 nm thermal SiO_2 + Si substrate. - Verify as-grown graphene quality with Raman spectroscopy.
2	Spin coat PMMA on the growth substrate. - 950 A4 PMMA from Microchem, 4500 rpm, 1000 rpm/sec, 45seconds. - PMMA with different molecular weight and/or concentration can be used. - Leave the sample in a desiccator overnight (~ 15 hours) to drive off solvent.
3	Put the sample in 6:1 Buffered Oxide Etch (BOE) for ~ 2-3 hours to etch SiO_2 and release PMMA-graphene-Cu film. - Sometimes the film is still attached to the growth substrate, especially at the corners and it is necessary to carefully use a pair of tweezers to help the release process.
4	Use a piece of clean Si wafer to gently take the film out of BOE and put it in De-Ionized (DI) water beaker for rinsing, typically for 2-3 minutes.
5	Place PMMA-graphene-Cu film in Cu etchant to etch Cu. - 10:1 H_20 : Ammonium Persulfate (APS-100, Transene INC.) solution. - ~ 10-15 minutes to etch Cu completely
6	Take PMMA-graphene film out of Cu etchant with a piece of clean Si wafer

	and rinse the film in DI water. - Rinse twice in two different DI water beakers, each for ~ 10 minutes.
7 Optional	Prepare a hydrophobic target substrate (Usually, 300 nm SiO_2 + highly doped Si). - Clean the target substrate with piranha solution (1:2 H_2O_2:H_2SO_4) for ~20-30 seconds. - Place the cleaned target substrate in HMDS oven for a 2 minute HMDS priming at 150 ^{0}C.
8	Put the target substrate in DI water beaker at an inclined angle and place the floating PMMA-graphene film on the target substrate. - In case of hydrophobic target substrate, the film usually tends to deflect away from target substrate. - The film can be gently pushed closer to beaker wall in order to reduce its available place to deflect before placing it on target substrate.
9	Leave the sample in a desiccator for ~ 3 hours to drive off moisture.
10	Bake the sample on a hotplate at ~130 ^{0}C for ~2-3 minutes.
11	Leave the sample in acetone for ~ 24 hours to dissolve PMMA. - The acetone may be replaced with fresh acetone 2-3 times.
12	Rinse the sample with isopropyl alcohol (IPA) and blow dry with N_2.
13	Inspect the sample with optical microscope and Raman spectroscopy. - Good Raman spectra may not guarantee good electrical characteristics.

A.2 Hexamethyldisilazane (HMDS) Treatment of Two-Dimensional Materials

Step	Details
1	Pour sufficient amount of HMDS in a glass beaker. The sample should be submerged in HMDS when lying flat in the beaker.
2	Put the sample inside the beaker.
3	Cover the beaker partially with aluminum foil.
4	Leave the beaker in a solvent hood for desired time. Typical duration is ~ 15-20 hours.
5	After the treatment period, take the sample out of the beaker with a tweezer.
6	Place the sample on a flat surface and let it completely dry in air.
7	Subsequent electrical or spectroscopic analysis should be performed immediately in order to avoid environmental degradation.

A.3 Black Phosphorous (BP) Thickness Reduction by Oxygen Plasma Treatment

Step	Details
1	Equipment: Plasma Therm 790 RIE. Place sample on a Si/Quartz carrier wafer and place it at the center of chamber
2	Pump chamber (Pressure: 50 mTorr, 10 sec).
3	Purge chamber with N_2 (Pressure: 800 mTorr, 10 sec).
4	Evacuate chamber (Pressure: 10 mTorr, 10 sec).
5	Purge chamber with N_2 (Pressure: 800 mTorr, 10 sec).
6	Evacuate chamber (Pressure: 10 mTorr, 10 sec).

7	Process step 1: Reactant gas: Oxygen (O_2), flow rate 18 sccm, Pressure 200 mTorr, duration 30 sec, RF power 0 watt.
8	Process step 2: Reactant gas: Oxygen (O_2), flow rate 18 sccm, Pressure 200 mTorr, duration 30/60/120 sec, RF power 150 watt.
9	Evacuate chamber (Pressure: 10 mTorr, 10 sec).
10	Purge chamber with N_2 (Pressure: 800 mTorr, 10 sec).
11	Evacuate chamber (Pressure: 10 mTorr, 10 sec).
12	Purge chamber with N_2 (Pressure: 800 mTorr, 10 sec).
13	Evacuate chamber (Pressure: 10 mTorr, 10 sec).

A.4 Top-Gated Black Phosphorous (BP) FET Fabrication

Step	Details
1	Exfoliate BP flakes from bulk crystal using scotch tape and transfer them onto 300 nm SiO_2 – Si substrate. - Highly doped Si if back-gated operation desired. - Highly resistive Si for RF FET.
2	Immediately spin coat the sample using PMMA. - 950 A4 PMMA from Microchem, 4500 rpm, 1000 rpm/sec, 45seconds. - Bake at 180 ^{0}C for 1 min on hotplate.
3	Identify suitable flake(s) for device fabrication.
4	Electron Beam Lithography (EBL) for source drain contact patterns.

	- Carl ZEISS (Neon 40) SEM with EBL capability - 20 KV beam, 350 $\mu C/cm^2$ - 15 sec development in 1:3 MIBK: IPA, followed by 20 sec IPA rinse.
5	Ni (~ 45 nm) + Au (~ 20 nm) metal stack deposition using Electron Beam Evaporation.
6	Leave the sample in room temperature acetone for liftoff process. Required time can vary, typically ~ 2 hours. Rinse with IPA and blow dry with N_2.
7	Immediately spin coat the sample with PMMA after liftoff process. See step 2 for details.
8	Electron Beam Lithography (EBL) for Top-Gate patterns. See step 4 for details.
9	Al_2O_3 (~ 20-30 nm) + Ni (~ 35 nm) gate stack deposition using Electron Beam Evaporation.
10	Liftoff in room temperature acetone. Liftoff is typically completed within few minutes. Rinse with IPA and blow dry with N_2.
11 Optional	Immediately spin coat the sample with PMMA after liftoff process. See step 2 for details.
12 Optional	Electron Beam Lithography (EBL) for exposed BP encapsulation; For example, access region between gate and source/drain. See step 4 for details.
13 Optional	Al_2O_3 (~ 40 nm) deposition using Electron Beam Evaporation.

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