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Scanning Probe Microscopy Study of Thin Film Solar Cells

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Scanning Probe Microscopy Study of Thin Film Solar Cells

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Scanning Probe Microscopy Study of Thin Film Solar Cells

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Thin film solar cells, such as CdTe, $CuIn_xGa_{1-x}Se_2$ (CIGS), Cu_2ZnSnS_4 (CZTS) and $Cu_2ZnSnSe_4$ (CZTSe), have been intensively studied for their unique features and excellent prospect of mass production in industry. The p-n junction is the most critical part of the thin film solar cell and greatly influences the performance. In this thesis work, the p-n junctions and the device layers of multiple kinds of thin film solar cells have been studied by using scanning probe microscopy based techniques.

The scanning spreading resistance microscopy (SSRM) has been developed on the cross-section of CdTe solar cells to study the resistance and carrier concentration distribution in different layers of the device. The CdTe sample was cleaved and milled with the argon ion beam to get a flat cross-section. The multiple device layers of the device were identified by the resistance mapping. A high-resistance region around the junction on the CdTe side due to carrier depletion was measured. With the AFM laser illumination, the resistance in the deep depletion region dropped and the resistance across

the entire CdTe layer became relatively uniform due to domination of photo-excited carriers. With carriers injected by applying a forward-bias voltage to the working device, the resistance in the deep depletion region decreased and the region moved toward the CdS/CdTe interface. These observed trends and observations are consistent with device physics.

We also measured the surface potential and the electric field across the junction using scanning Kelvin probe force microscopy (SKPFM) in the cross-section of the standard CIGS, ZnS(O,OH)/CIGS and the standard CZTSe devices. Both the heterojunction and homojunction situations of the three solar cells were simulated using the PC1D software. The simulation results were compared with the experimental results to analyze the properties of the junction. The comparison results provided the possible ranges of the thickness and carrier concentration of n-CIGS/n-CZTSe layer.

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Chapter 1

Introduction to Solar Cells

The energy consumption has increased dramatically in recent decades. The world's total energy consumption in 2010 is 524 quadrillion Btu[1], increased with 47.6% compared with 355 quadrillion Btu in 1990 [1]. The fossil energy, such as coal, oil and natural gas, supplies over 80% of the world's energy. However, considering the finiteness of the fossil energy, it will be exhausted and cannot fulfill the demand of the world's energy consumption sooner or later in the future. Burning fossil fuels causes the contamination of the air and water, which leads to serious environmental pollution. One of the severe problems is the increase of the average temperature on the earth due to the CO_2-emission by fossil fuels — known as the global warming. Thus, it is urgent to develop an alternative clean energy which can be used continuously without damaging the environment. Solar energy, wind energy, hydrogen fuel energy, etc., are such kind of clean and renewable energy.

Solar cell is one of the most promising techniques for renewable energy as the solar energy is inexhaustible and enough to cover the world's energy consumption. The power of the sun absorbed by the biosphere is about 122 PW among the 174 PW received by the planet [2]. It means that less than one hour of the sun power absorbed by earth is enough to supply the entire year's demand of the global energy consumption. However, only 0.305 quadrillion Btu of the solar energy is generated in 2010 [3]. There is still large potential for the development of solar energy generation. The research about the solar

[1] $1 \text{ quadrillion Btu} = 1.055 \times 10^{18} \text{ joules}$

cells is demanded to enhance the efficiency and lower the price per kW. Figure 1.1 summaries the best research-cell efficiencies for various photovoltaic techniques since 1976 [4].

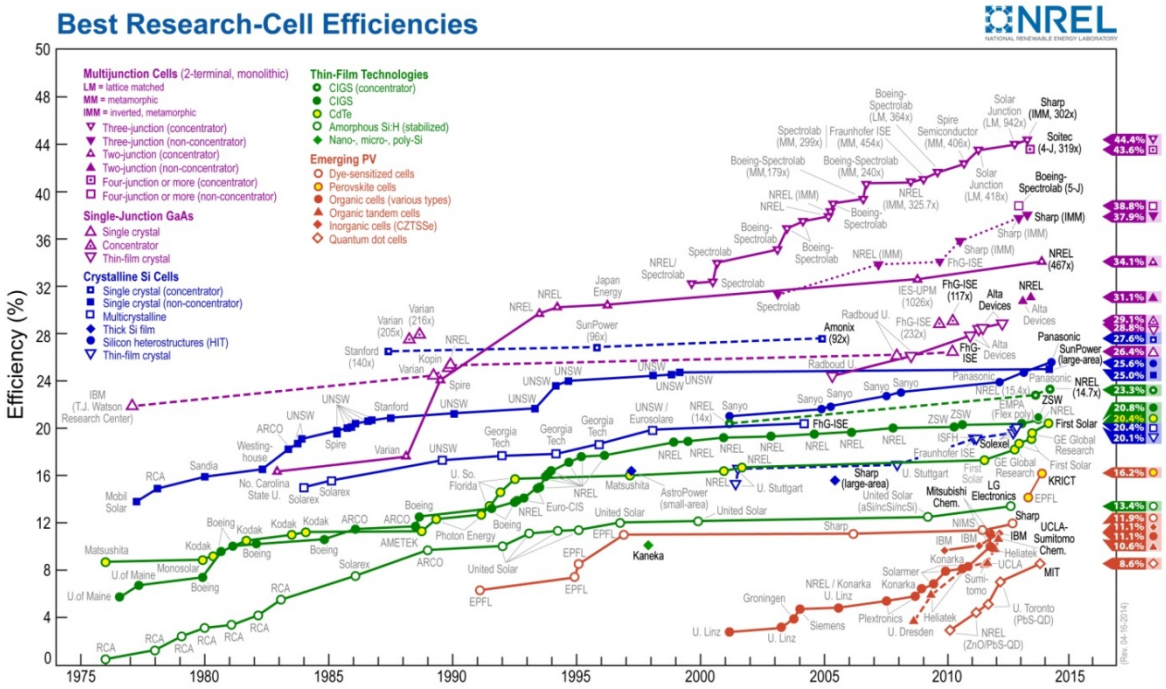

Figure 1.1 Timeline of the conversion efficiencies of the best research solar cells worldwide from 1976 to 2014 for various photovoltaic techniques [4].

1.1 Theory of solar cells

Solar cells use the photovoltaic effect to convert solar energy to electrical energy. When the solar cell is exposed to light, the light radiation generates electron-hole pairs in absorber layer of the solar cell. The p-n junction structure of the solar cell separates the electrons and holes to reduce the recombination rate. If the solar cell is connected to an

external circuit, the carriers generated by the solar cell will be transferred and provide energy to the other part of the circuit.

1.1.1 Solar spectrum

The solar radiation of the sun is similar to the black body radiation with the surface temperature at about 5800 K. The yellow area in Figure 1.2 [5] represents the spectrum of sunlight on top of the atmosphere of the earth. It is slightly different from the black body spectrum as presented by grey line, because the sun is not an ideal black body. The peak of the solar spectrum is around $\lambda = 500\,\text{nm}$, which corresponds to the photon energy of $\hbar\omega = 2.48\,\text{eV}$. The radiation power on top of the atmosphere is 1353 W/m^2. [6]

As the sunlight passes through the atmosphere, a fraction of it is absorbed by gas, water vapor, carbon dioxide, etc., as shown in the red area of Figure 1.2. Therefore, the absorption increases with the distance that sunlight passes through the atmosphere. The pass length L can be calculated as

$$L = \frac{L_0}{\cos\alpha} \tag{1.1}$$

where L_0 is the pass length normal to the earth's surface, and α is the incident angle of the sunlight. The ratio L/L_0 is called air mass coefficient. It varies with the time, the seasons and the latitude. The zero air mass coefficient (AM0) is defined as the spectrum outside the atmosphere. AM1 denotes the spectrum when the sunlight incident perpendicular on earth's surface. Because most of the world's population is in temperate latitudes, AM1.5 with the corresponding incident angle $\alpha = 48°$ is most commonly used. The radiation power of the AM1.5 spectrum is about 1000 W/m^2 [6].

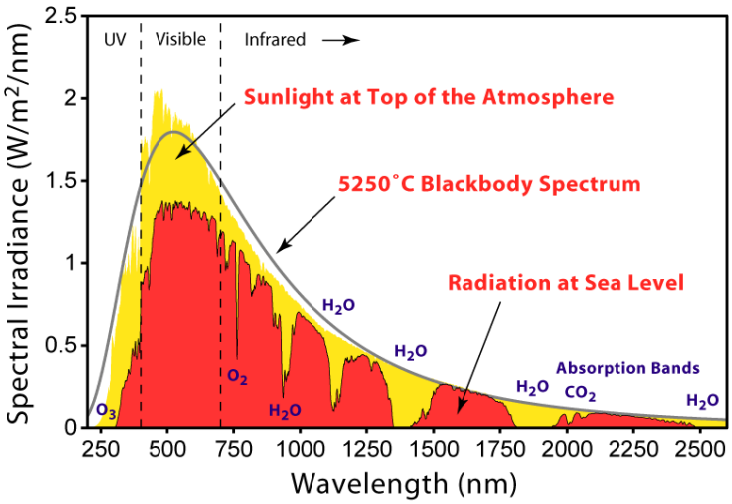

Figure 1.2 Solar spectrum above the atmosphere and at sea level compared to blackbody spectrum [5].

1.1.2 p-n junction diodes

The essential part of the most common solar cells is the p-n junction diode. In this section, the properties of p-n junction in dark and in light will be analyzed.

The diode equation in dark is:

$$I = I_0\left(e^{qV/kT} - 1\right) \tag{1.2}$$

where I_0 is the saturation current density:

$$I_0 = qA\left(\frac{D_p}{L_p}p_n + \frac{D_n}{L_n}n_p\right) \tag{1.3}$$

where p_n and n_p are the minority carrier concentration in n-type and p-type side, respectively. D_n and D_p are the electron and hole diffusion coefficient, respectively. L_n and L_p are the diffusion length of electron and hole, respectively.

When the p-n junction diode is illuminated by light, the electrons in valence band

are excited to the conduction band by absorbing energy from photons and become free. Assume that the volume rate of generation of electron-hole pairs by the light, G, is constant throughout the device, and neglect the effect of recombination in depletion region. The light-generated current I_L has the value

$$I_L = qAG(L_n + W + L_p) \tag{1.4}$$

where W is the depletion length of the p-n junction. Thus, the current-voltage relation of the p-n junction diode under illumination is

$$I = I_0(e^{qV/kT} - 1) + I_L \tag{1.5}$$

The I-V curves of the diode in dark and in illumination are plotted in Figure 1.3. The illuminated I-V curve is just the curve in dark shifted down by a current I_L

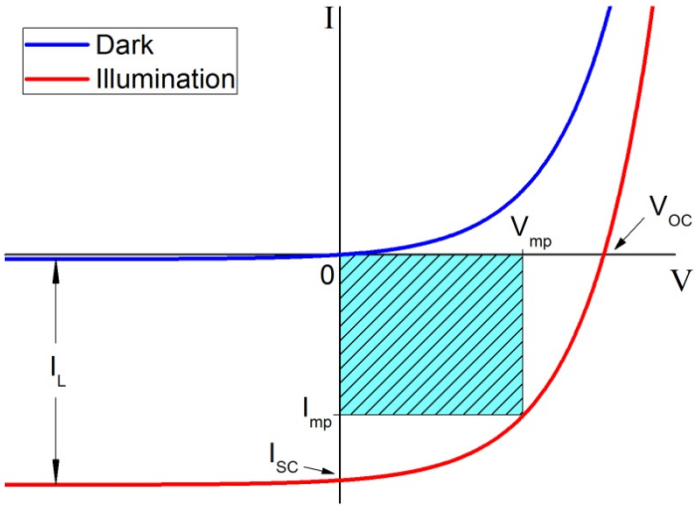

Figure 1.3 I-V curves of p-n junction diode in dark and illumination

1.1.3 Solar cell output parameters

There are three parameters usually used to characterize solar cell outputs. When a solar cell is operated in a short circuit under illumination, the current through the

terminals is the short-circuit current I_{sc}. Ideally, this is equal to the light-generated current I_L. When the solar cell is operated in an open circuit under illumination, the voltage across the output terminals is defined as open-circuit voltage V_{oc}. It can be obtained by setting $I = 0$ in equation (1.5):

$$V_{oc} = \frac{kT}{q} \ln\left(\frac{I_L}{I_0} + 1\right) \tag{1.6}$$

When the solar cell is in a circuit, it will have both current and voltage. The power output of an operating point on the I-V curve is the shaded light green area of the rectangle shown in Figure 1.3. There exists one operating point (V_{mp}, I_{mp}) on the curve that can maximize the power output. The ration between the theoretical power $V_{oc}I_{sc}$ and the maximum possible power $V_{mp}I_{mp}$ is defined as the fill factor FF:

$$\text{FF} = \frac{V_{mp}I_{mp}}{V_{oc}I_{sc}} \tag{1.7}$$

Ideally, the fill factor is the function only of V_{oc}. By defining a normalized voltage v_{oc} as $V_{oc}/(kT/q)$, an empirical expression describing the FF and v_{oc} can be represented as

$$\text{FF} = \frac{v_{oc} - \ln(v_{oc} + 0.72)}{v_{oc} + 1} \tag{1.8}$$

The efficiency of a solar cell, i.e. the ratio of the power generated by the solar cell to the power of the incoming light, is

$$\eta = \frac{V_{mp}I_{mp}}{P_{in}} = \frac{V_{oc}I_{sc}\text{FF}}{P_{in}} \tag{1.9}$$

1.1.4 Limitation on efficiency

To excite an electron from valence band to conduction band, the energy of the photon must be larger than the band gap of the material. Thus, the photons with long

wavelength will not contribute to energy conversion. For example, the band gap of silicon is 1.1 eV. The photon with 1.1 eV energy has the wavelength of 680 nm, corresponding to red light. Therefore the photons with the wavelength shorter than 680 nm in the spectrum in Figure 1.2 can be absorbed by the silicon solar cell and convert to electric energy, while the photons with the wavelength longer than that such as infrared, microwaves and radio waves can not. About 19% of the efficiency is lost in this way. Another major contributor to the efficiency loss is that each photon absorbed by the solar cell creates only one electron-hole pair regardless of its energy. The photons with the energy larger than band gap can excite the electron with higher energy, but the electron loses its extra energy when it travels to the bottom of the conduction band. The wasted energy is dissipated as heat. This causes 33% of the efficiency loss. Thus, considering the spectrum losses, the theoretical maximum efficiency of a solar cell is 48%.

Figure 1.4 is the maximum efficiency as a function of band gap for a single-junction solar cell [7], known as Shockley–Queisser limit [8]. It is calculated with the consideration of blackbody radiation, radiative recombination, spectrum losses, etc. The maximum efficiency of 33.7% occurs for a 1.34 eV band gap. The most common material used in solar cell, silicon, has the band gap of 1.1 eV, which results in the theoretical maximum efficiency of 29%. GaAs has a near-optimal band gap of 1.4 eV. For the materials used in thin film solar cells, CIGS has a tunable band gap range from 1.0 eV to 1.7 eV which is decided by the content of indium and gallium. CdTe has a band gap of 1.44 eV. The band gap of CZTS and CZTSe are 1.0 eV and 1.5 eV, respectively. The solar cells with multiple junctions can exceed the maximum of efficiency in Figure 1.4.

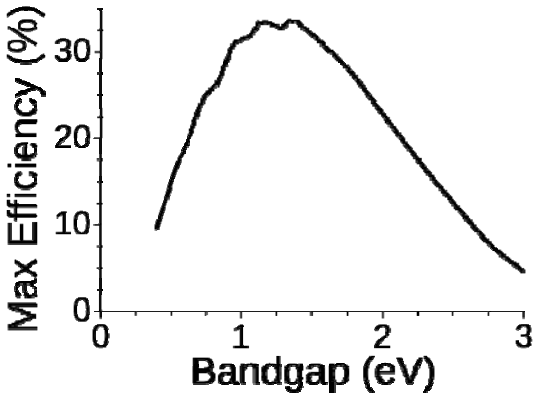

Figure 1.4 The maximum efficiency as a function of band gap for a single-junction solar cell in AM1.5 [7].

2.1 Thin film solar cells

Silicon crystalline and multicrystalline solar cells are the most developed solar techniques and are widely used in the market. Other types of solar cell, such as thin film solar cells, multi-layer solar cells, and organic solar cells, are also under development in both academic and industry. Figure 1.5 lists the different categories of solar cell technologies.

Although the thin film solar cells do not have as high efficiency as crystalline silicon solar cells or multi-layer solar cells, they are intensively studied for their unique features. One of the advantages of thin film solar cells is the cheaper manufacturing cost, because only a small amount of materials is needed comparing with crystalline silicon solar cells. Another advantage is that it can be used on large modules to produce large area solar panel. Also, thin film solar cells can be deposited on multiple choices of substrates, such as glass, steel foil, or plastic, to have the flexible or transparent features. In this section, CdTe, CIGS and CZTSe solar cells are introduced.

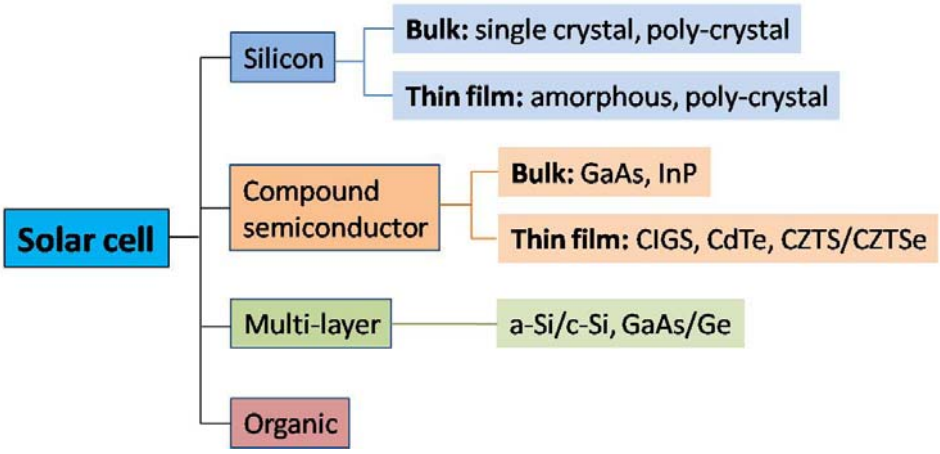

Figure 1.5 List of categories and materials of solar cells

1.2.1 Cadmium Telluride solar cells

Cadmium telluride (CdTe) is a group II^B-VI^A compound semiconductor. The band gaps of CdTe is 1.44 eV, which is very close to the optimum band gap in the solar spectrum for energy conversion efficiency (see Figure 1.4). CdTe also has high absorption coefficient of 5×10^5 /cm for photons with energy larger than the band gap.

High-efficiency CdTe solar cells to date have the superstrate structure [9]. The light incidents through the glass to the device in this structure. The n-type TCO and CdS layers are deposited first on the glass and then followed by the p-type CdTe layer. The substrate structure, with which the light incidents from the device side to the glass side, does not have high efficiency yet. The main reasons for the low efficiency in substrate structure are the low quality of CdTe/CdS junction and the high resistance of the electrical contact to CdTe [10].

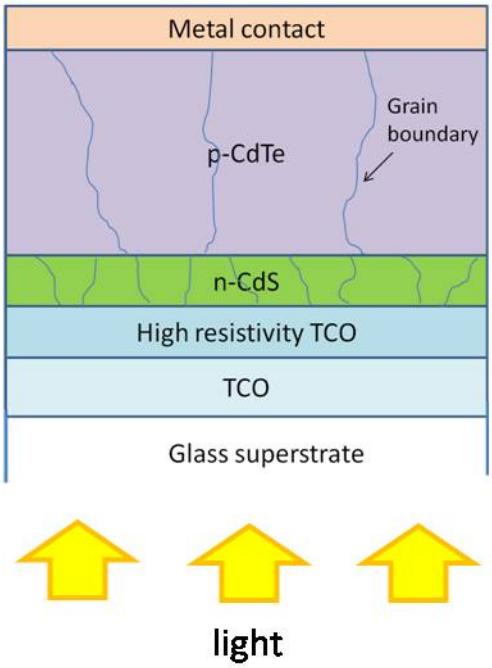

Figure 1.6 Schematic of CdTe solar cells with superstrate structure

Figure 1.6 is a typical superstrate structure of the CdTe solar cell. It is composed with transparent conducting oxide (TCO), high resistivity TCO, n-type CdS, p-type CdTe and back contact. The TCO layer, such as SnO_2, In_2O_3:Sn (ITO), or indium-tin oxide, works as the front contact. The n-type CdS layer should be thin enough to transmit the photons of the light so that the photons can reach to CdTe absorber layer. However, the ultra-thin CdS layer is difficult to be controlled during deposition. It may cause the problems such as shunting due to the direct contact between CdTe and TCO. Thus, a highly resistive TCO layer (HRT) is deposited between TCO and CdS to improve the junction quality. The material of the HRT layer could be SnO_2 [11, 12], In_2O_3 [13], etc. The band gap of TCO, HRT and CdS layers should be relatively large to transmit most of the photons of the light.

A lot of methods have been developed to deposit p-type CdTe absorber layer [10,

14], such as physical vapor deposition (PVD) [13, 15, 16], close-space sublimation (CSS) [17-23], vapor transport deposition (VTD) [24], sputter deposition [25, 26], electrodeposition [27-29], and metal organic chemical vapor deposition (MOCVD) [30, 31]. The "$CdCl_2$ treatment", which is the post-deposition processing of CdTe layer with exposure to $CdCl_2$, can improve the performance of the device by considerably increasing the open-circuit voltage and fill factor [32].

1.2.2 Cu(InGa)Se_2 solar cells

Cu(InGa)Se_2 (CIGS) solar cells have been the most promising compound thin film solar cells. Compared with CdTe, the four elements of CIGS are nontoxic. The band gap of CIGS can be tunable from 1.0 eV to 1.7 eV by adjusting the ratio of indium and gallium in CIGS. The high absorption coefficient of CIGS makes 95% of the light to be absorbed within 1 μm material, so that the device can be fabricated with every thin layer of CIGS to lower the cost. A few years earlier, a CIGS solar cell with efficiency of 20% was made by the National Renewable Energy Laboratory (NREL) with the three step co-evaporation deposition method [33]. In industry, large area modules with efficiencies of 12~14% on 3459 cm^2 and >15% efficiencies on 1000 cm^2 was demonstrated [34].

Figure 1.7 shows the schematic cross-section of the standard CIGS solar cell. In contrast to CdTe solar cell, the high efficient CIGS solar cell has the substrate structure. Light incident from the device to the glass in this structure. The CIGS solar cell is composed of a molybdenum layer as the contact, a p-type CIGS absorber layer, an n-type CdS buffer layer, a heavily doped n-type ZnO layer, and the metal grid on top.

The CIGS doped by native defects, such as Se, has the carrier concentration of about

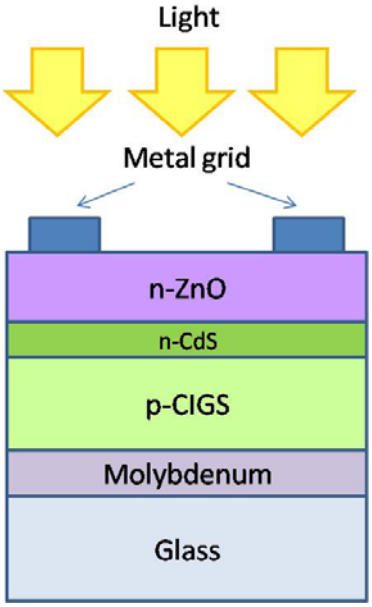

Figure 1.7 Schematic structure of CIGS solar cells with substrate structure

10^{15}-10^{16}/cm^3 [35]. The soda-lime glass substrate provides sodium in the process of growing CIGS. The Na diffuse to CIGS through the Mo back contact layer, resulting larger grains and better grain orientation of CIGS thus improve the performance of the solar cell [36].

Above the CIGS layer there is an ultra-thin n-type CdS layer formed with chemical bath deposition. The CdS layer acts as a buffer layer with the function of band alignment and lattice matching between ZnO and CIGS layer [37, 38]. It is usually as thin as 50nm to maximize the optical transmission. Because of the toxic of Cd, development of the device with alternative buffer material such as ZnS(O,OH) is necessary. On top of the buffer layer, a ZnO layer and the metal grid are used for lateral current collection. The band gap of ZnO is very large to increase the transmission of the light.

1.2.3 Cu_2ZnSnS_4/$Cu_2ZnSnSe_4$ solar cells

Although CIGS solar cells is widely manufactured in industry with high efficiency, the availability of the indium is a big problem. Cu_2ZnSnS_4(CZTS) and $Cu_2ZnSnSe_4$ (CZTSe) are the alternative material of CIGS. The material of copper, zinc, tin, and sulfur are all sufficiently abundant in earth. The structure and the properties of CZTS/CZTSe solar cells are similar with CIGS solar cells. It also composed with substrate, molybdenum, CZTS/CZTSe, CdS, ZnO and metal grid.

Chapter 2

Scanning Probe Microscopy Techniques

2.1 Atomic force microscopy

Atomic force microscopy (AFM) was invented by G. Binnig, C. F. Quate, and Ch. Gerber in 1986 [39]. It measures the surface corrugation of the sample by detecting the force between the probe and sample. When there is a force between tip and sample, the cantilever deflects according to Hooker's law. The deflection of the cantilever is measured by the movement of the laser spot reflected by the cantilever on photodiode (Figure 2.1).

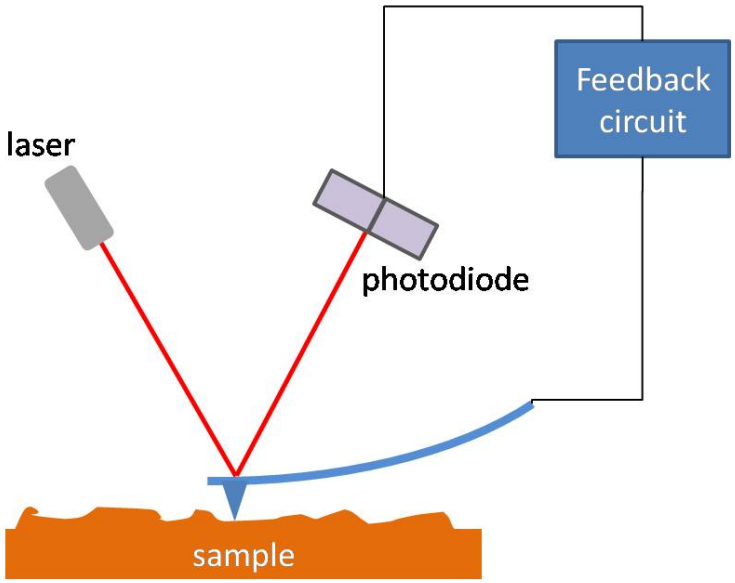

Figure 2.1 Diagram of AFM. The bending of the cantilever is detected by the laser and the photodiode

The AFM can be operated in different modes depending on the different usages. The most common modes for taking the topography image are the contact mode and tapping mode. In constant force contact mode, the feedback system in AFM is used to keep the deflection of the cantilever constant, and consequently keep the interaction force constant, by adjusting the vertical position of the tip. Thus, by recording the tip position while scanning across the sample, the topography profile of the surface of sample can be taken by AFM. In tapping mode, the piezo drives the cantilever to vibrate near its resonance frequency. As tip get close to the sample, the interaction force between the tip and sample causes the oscillation amplitude to decrease. The feedback system keeps the oscillation amplitude constant by adjusting the tip vertical position. While scanning, the computer records the surface profile of the sample.

By adding some external module or electronic equipment to AFM and using the proximate probes, the AFM tip can act as an electrical sensor to detect the electrical signals while the topography image is taking. Several AFM-based techniques were developed after the invention of AFM [40-44], including the scanning Kelvin probe microscopy (SKPFM), scanning spreading resistance microscopy (SSRM), scanning capacitance microscopy (SCM), and conductive AFM (C-AFM). These techniques can detect local electrical properties of the sample with high spatial resolution, such as the spreading resistance, Coulomb force, capacitance, and electric current, which are used to measure the resistivity, surface potential, carrier concentration, local conductivity, etc. on the surface of the sample. In this article, the SSRM and SKPFM are used on the cross-section of the thin film solar cell to map the carrier concentration and surface electrostatic potential across the solar cell devices.

2.2 Scanning spreading resistance microscopy

Scanning spreading resistance microscopy (SSRM) was first developed in nineteen nineties [45]. It measures the local spreading resistance of the sample around the tip. If the tip diameter and sample electrical parameters are know, the local resistivity and carrier concentration can be calculated from the measured spreading resistance. Because the tip used in SSRM is several tens of nanometers, the spatial resolution of the resistance image can be as high as 10nm.

Figure 2.2 is the schematic diagram of SSRM. The contact mode is used, and a bias voltage is applied between tip and sample. The measured resistance consists of spreading resistance, contact resistance, and back contact resistance of the sample. The back contact resistance is usually very small. Therefore, if the contact resistance is minimized, the measured resistance should be dominated by the spreading resistance. The methods to minimize the contact resistance include applying sufficient indentation force to tip and large enough bias voltage V_s between tip and sample. The heavily doped diamond coated tip is commonly used to make the tip conductive and to prevent wearing-off under high indentation force. Also, Because of the large indentation force on tip and relatively large bias voltages applied between tip and sample, it is necessary to perform the SSRM measurement in an inert environment (such as glove box) to avoid oxidation of the sample.

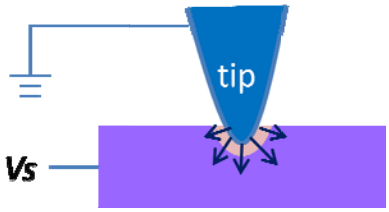

Figure 2.2 Diagram of SSRM. The tip is grounded and the sample is applied with V_s bias

If the radius of the tip is known, the measured spreading resistance can be converted to the local resistivity of the sample using

$$\rho = 4rR \tag{2.1}$$

where r is the radius of the tip, and R is the measured spreading resistance. The conductivity σ has the relationship with carrier concentration by

$$\sigma = N\mu e \tag{2.2}$$

where N is the carrier concentration, μ is the mobility of the sample, and e is the charge of the electron. Using $\rho = 1/\sigma$, equation (2.1) and (2.2), the carrier concentration can be calculated with the spreading resistance:

$$N = \frac{1}{4rR\mu e} \tag{2.3}$$

Thus, one can get the carrier concentration distribution on the sample from the SSRM resistance image.

2.3 Scanning Kelvin probe force microscopy

Scanning Kelvin probe force microscopy (SKPFM) was invented in 1991 [40]. It detects the surface electrical potential on sample by measuring the Coulomb force between tip and sample. If the tip and sample are electrically connected, the tip-sample contact potential difference (CPD) is the work function difference between tip and sample. The tip and sample can be seen as a capacitance. CPD generate the charge transfer on tip and sample, and thus generate a Coulomb force. The energy and the Coulomb force generated by CPD are

$$E = \frac{1}{2} C V_{CPD}^2 \tag{2.4}$$

$$F = \frac{\partial E}{\partial z} = \frac{1}{2}\frac{\partial C}{\partial z} V_{CPD}^2 \tag{2.5}$$

where C, z are the capacitance and distance between tip and sample, respectively. The CPD can be detected by measuring the Coulomb force. However, this Coulomb force is very hard to be measured because of the small capacitance between tip and sample, and the difficulty to separate it from the atomic force. To improve the Coulomb force measurement, an AC voltage $V_{AC}\sin(\omega t)$ is applied on tip. Then the electric energy and the Coulomb force are

$$E = \frac{1}{2}C[V_{CPD} + V_{AC}\sin(\omega t)]^2 \tag{2.6}$$

$$\begin{aligned} F = \frac{\partial E}{\partial z} &= \frac{1}{2}\frac{\partial C}{\partial z}\left(V_{CPD}^2 + \frac{1}{2}V_{AC}^2\right) + \frac{\partial C}{\partial z}V_{CPD}V_{AC}\sin(\omega t) - \frac{1}{4}\frac{\partial C}{\partial z}V_{AC}^2\sin(2\omega t) \\ &= F_0 + F_1 + F_2 \end{aligned} \tag{2.7}$$

where

$$\begin{aligned} F_0 &= \frac{1}{2}\frac{\partial C}{\partial z}\left(V_{CPD}^2 + \frac{1}{2}V_{AC}^2\right) \\ F_1 &= \frac{\partial C}{\partial z}V_{CPD}V_{AC}\sin(\omega t) \\ F_2 &= -\frac{1}{4}\frac{\partial C}{\partial z}V_{AC}^2\sin(2\omega t) \end{aligned} \tag{2.8}$$

F_1 oscillates with the same frequency as the AC voltage, and is proportional to V_{CPD}. It can be detected using a lock-in amplifier. If the tip and sample are applied with bias voltage V_t and V_s, respectively, then

$$V_{CPD} = W_t - W_s - V_t + V_s \tag{2.9}$$

where W_t and W_s are the work functions of tip and sample, respectively. Figure 2.3 is the schematic of the SKPFM set up [46]. The AFM uses tapping mode with two components of oscillation. One component of the oscillation is used to detect the topography signal. Another component of oscillation with the frequency of ω can detect F_1. The filter separates the signals of the two oscillations, so V_{CPD} can be measured. If the tip and sample are both grounded or applied with the same voltage, the measured

V_{CPD} is the difference of the work function between tip and sample. When taking the SKPFM image, the tip work function is fixed, so the image reflects the work function variation in different locations of the sample

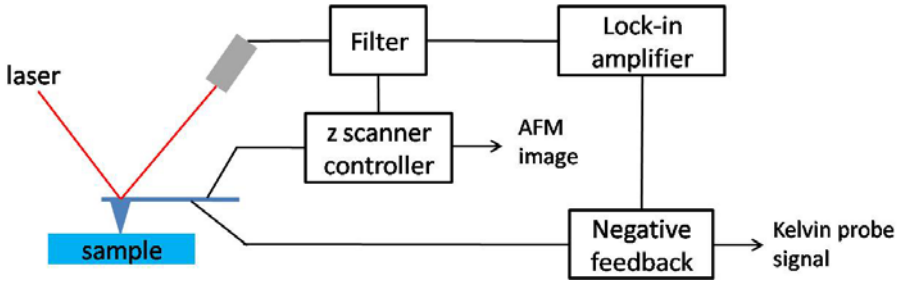

Figure 2.3 Diagram of SKPFM [46].

Chapter 3

Resistance Mapping on Cross-section of CdTe Solar Cells

CdTe thin film solar cells have been greatly improved in recent years, mainly with respect to the short circuit current (J_{sc}) and the fill factor (FF) [47]. However, the open circuit voltage (V_{oc}) of the devices (~0.85 V) [47] has stayed relatively low in comparison to the optimal band gap (~1.45 eV) for photovoltaic applications. Compared with minority carrier lifetime, doping concentration, etc., the junction formation is a critical factor determining the open circuit voltage of the device. Therefore, the electrical properties of the junction have been extensively studied. Most of these studies are macroscopic characterizations of the whole device, focusing on such features as capacitance and current-voltage. These characterizations have significantly improved the understanding of junction formation on macroscopic scales [48].

However, macroscopic characterizations alone are not enough to understand the details of junction formation, because CdTe solar cell devices are inhomogeneous. Grain boundaries and the inhomogeneity among and inside the grains are expected to affect the junction formation [49-51]. The intermixing of S and Te at the CdS/CdTe interface and the change of the intermixing with post CdTe-deposition processing also crucially impact the junction formation and V_{oc} [48]. To study the inhomogeneity in CdTe devices, microscopic electrical and optical characterizations with high spatial resolution are needed. Electron-injection-based methods, scanning probe microscopy-based electrical and optical probes have provided some valuable insights [49, 52-57]

Scanning spreading resistance microscopy (SSRM), an AFM-based technique, is an

excellent tool to map the distribution of the resistance and carrier distribution on samples with nanometer-scale resolution. The principle of SSRM was introduced in section 2.2. It has been extensively applied in characterization of carrier distribution in Si micro-devices [58-60]. The success of this technique relies on the minimization of probe/sample contact resistance [58-60], which is material dependent. Recently, the SSRM technique has been developed for characterizing the electrical properties of grains and grain boundaries in CIGS, CZTSe and CdTe [57, 61]. In this chapter, the SSRM measurement is conducted on polished cross-sections of CdTe solar cells.

3.1 Sample preparation

CdTe devices were deposited with the superstrate structure, involving a glass superstrate, a SnO_2 transparent conductive oxide (TCO) coating, an intrinsic ZnO (i-ZnO), a CdS buffer, a CdTe film, and a back contact [62]. CdTe and CdS were deposited by close space sublimation (CSS) and chemical bath deposition (CBD), respectively. Before facilitating the back contact, a $CdCl_2$ treatment at 400℃ was carried out. The thickness and the carrier concentration of the different layers are listed in Figure

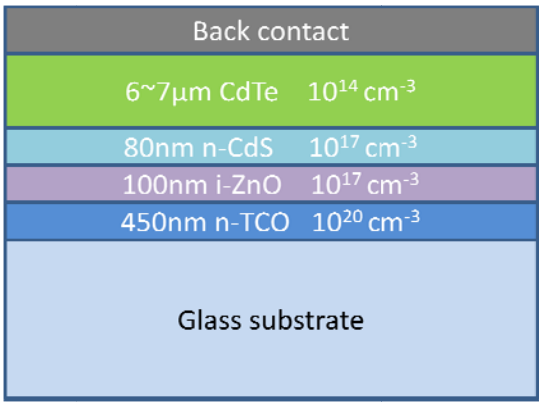

Figure 3.1 Schematic of the thickness and carrier concentration of the layers in CdTe

3.1

Figure 3.2 illustrates the process of polishing the cross-sectional surface of the device. The sample is first cleaved from large pieces. The cleaved surface is too rough to conduct the SSRM scanning, so the sample is put into a JEOL cross section polisher for fine polishing. In the JEOL polisher, the sample is covered by a titanium mask with flat edge. The area to be polished is exposed outside the mask. Then the polisher is pumped to vacuum and the Ar^+ ion beam hits the sample vertically from an ion gun. The sample material outside the mask is removed by the Ar^+ ions, resulting in a very flat cross-section. For the CdTe devices, the cross-section is usually polished for 6~10 hours with 4~6 kV Ar^+ beam: the higher the voltage of the Ar^+ beam, the shorter the time that is needed. After the polishing process is done, the mask is removed and the sample is glued onto a sample holder. The conductive wires are connected to the back contact layer and TCO layer, respectively, to apply the bias voltage across the device.

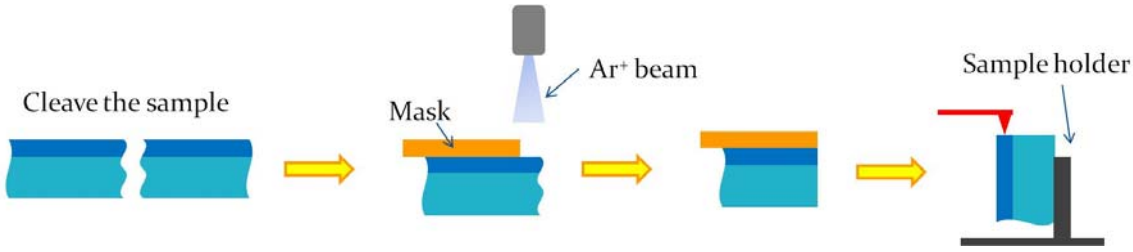

Figure 3.2 Process of polishing the cross-section of the sample using Ar^+ ion beam

3.2 Experiment

3.2.1 SSRM set up

The SSRM is based on a commercial Veeco D5000 AFM system with Nanoscope V controller. The AFM is set up in an Ar glove box with H_2O and O_2 concentration less

than 0.1 ppm. Because of the large indentation force (~1000 nN) applied by the tip and the relatively large bias voltages (3.5~4.5 V) applied between tip and sample, it is necessary to perform the SSRM measurement in an inert environment to avoid oxidation of the sample. Highly doped diamond-coated Si probes (Bruker-nano DDESP) were used to prevent wearing-off under the large indentation force.

The laser in AFM is required to measure the bending of the cantilever to take the topography image. Although the cantilever of the AFM probe blocks most of the laser, the sample can still be illuminated if the laser beam is larger than the cantilever width. Also, the scattering of the laser from other parts of the equipment indirectly illuminates the sample beneath the probe. To eliminate the influence of the AFM laser and get a resistance image in dark conditions, the AFM works under the "dark lift" mode. For each line of the image, the AFM scans twice. In the first time the laser is on and the AFM records the resistance in laser. In the second time the laser is turned off. The probe scans again in the same location along the topographic line profile obtained from the first scan, and simultaneously records the resistance signal in dark. Notice that the laser of the AFM incidents on the cross-section of the device. It is different from the illumination when the solar cell is operating, with which the light incident from glass side to the device side. It is difficult to achieve this kind of light set up yet.

In this experiment, the tip is virtually grounded, and a voltage V_s is applied to the sample. The SSRM output voltage V_{out} has a logarithmic scaling with the measured resistance:

$$\begin{cases} R_{tot} = 10^{V_{\text{out}}}, & \text{if } V_s > 0 \\ R_{tot} = 10^{-V_{\text{out}}}, & \text{if } V_s < 0 \end{cases} \tag{3.1}$$

Throughout this article, the SSRM output voltage is converted to R_{tot}.

To investigate the resistance distribution of the sample in forward or reverse bias, a

bias voltage V_b needs to be applied between the back contact layer and the Mo layer on the device. Figure 3.3 is a schematic of the external voltage applied to the sample. A sample voltage V_s is applied to the TCO. V_b denotes the relative voltage applied between the back contact and the TCO. The junction of the device is under forward bias if $V_b = 1\text{V}$, and under reverse bias if $V_b = -1\text{V}$.

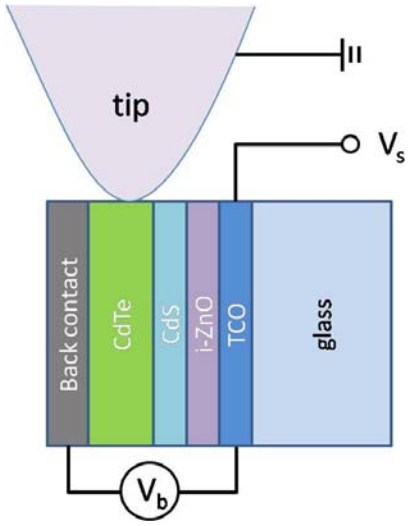

Figure 3.3 Schematic of the voltage applied to sample and tip for SSRM measurement on cross-section of CdTe sample

3.2.2 Optimizing the resistance signal

As described in section 2.2, the total measured resistance R_{tot} is composed of spreading resistance R_{sp}, contact resistance R_{tot} and back contact resistance R_b. R_b is much smaller than R_{sp} and R_c, as is evident if one considers that the series resistance of the device is at most a few Ω/cm^2 and that the current routes spread when reaching the back contact of the device. Therefore, if the contact resistance is minimized, the

measured resistance should be dominated by the spreading resistance R_{sp}.

On single-crystalline Si, it was simulated that local high-pressure metalliclike phases of β–tin and BCT5-Si with nonlocalized molecular orbitals of sp^3d^1 and sp^3d^2 were formed beneath the probe (see the diagram in Figure 3.4), leading the minimization of the contact resistance [60]. Hence, applying large indentation force from tip to sample can reduce the contact resistance in SSRM measurement. The contact between the highly doped diamond coated tip and the metallic β–tin Si (or BCT5-Si) beneath the tip should be Ohmic. Thus, the SSRM nanocontact is dominated by the metal-semiconductor (or Schottky) contact between the substrate Si and β–tin Si (or BCT5-Si) [60]. For CdTe, there is no such kind of research yet. Since the similar diamond-like structure between Si and CdTe, minimization of R_c on CdTe would also be accomplished by adequately indenting the probe into the material and applying a V_s larger than the onset value of the probe/sample barrier. Actually this was demonstrated in the previous SSRM studies on CIGS and CdTe films [57, 61].

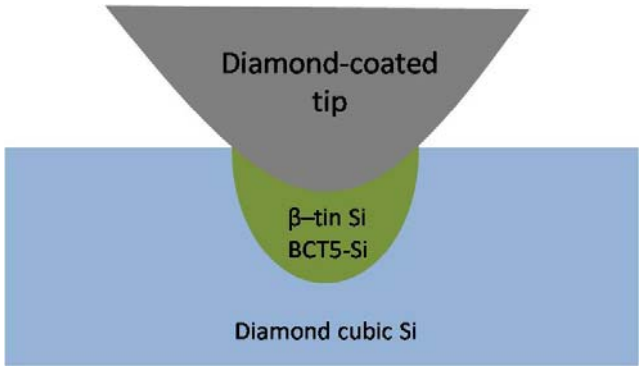

Figure 3.4 Cross-sectional view of the simulation of the Si structures at the maximum indentation depth for tip. The green area indicates the metallic β–tin Si and BCT5-Si. The blue area indicates the Si with diamond cubic structure. [60]

Figure 3.5(a) is the resistance measured on CdTe with different indentation forces when V_s is $+3.5$ V. The resistance value of each point is the average of 20 lines on a resistance graph with 2048 pixels per line. These data were taken with the AFM laser turned off in the "dark lift" mode, and thus represent the material property in the dark. Figure 3.5(a) shows that when the indentation force of the tip is larger than 750 nN, the resistance is minimized. Thus, the contact resistance is minimized and the total resistance is dominated by spreading resistance.

Figure 3.5(b) is the current-voltage (I-V) curve in the dark with the change of sample bias V_s between the tip and CdTe, when the indentation force on the tip is 1000 nN. The current is calculated using V_s/R. For each point, the current is calculated from the resistance averaged from a graph with 20×2048 pixels. The I-V curve shows the rectifying characteristic for a Schottky junction. When V_s is larger than the onset voltage 3 V, the current increases sharply. Since the SSRM nanocontact is not Ohmic, the measured resistance will change with the different sample bias. Table 3.1 lists the resistance values of the plots in Figure 3.5(b) from 0V to 7V. One sees that when the sample bias is larger than the onset voltage 3 V, the measured resistance reduces as the increase of the sample bias. In the range of the sample bias used in the experiment (3.5V~4.5V), the measured resistance of CdTe changes for about 0.4 orders of the magnitude. This factor should be considered when analyzing the change of the resistance in different sample bias.

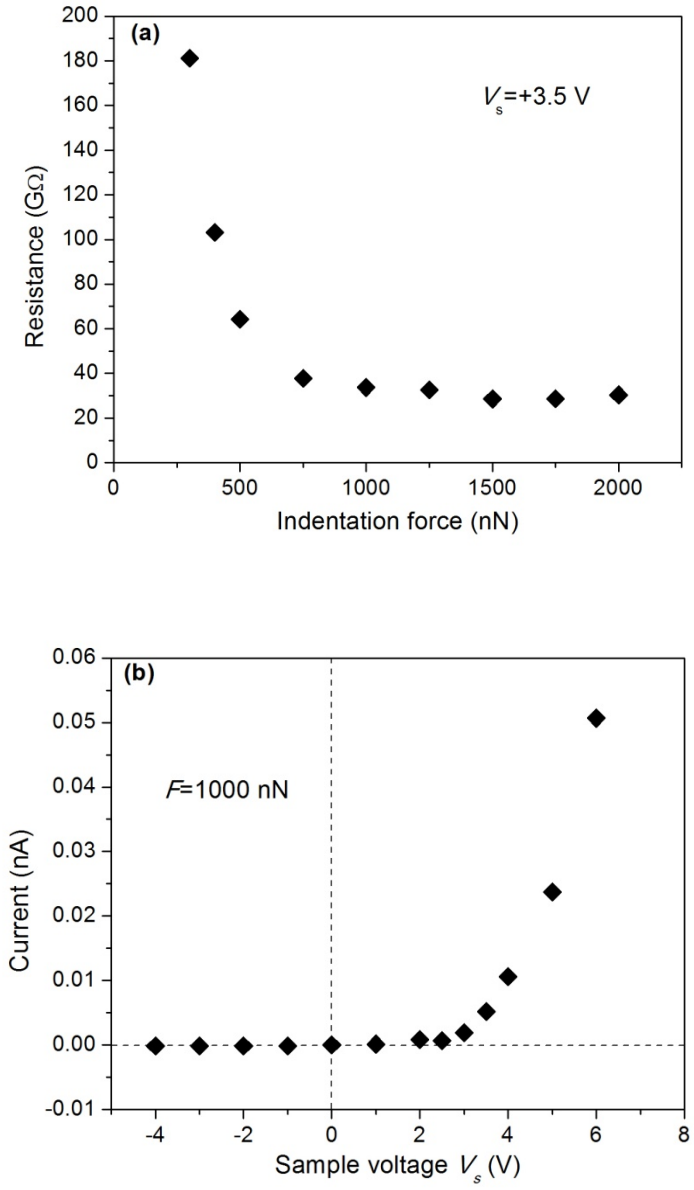

Figure 3.5 (a) Change in resistance R_{tot} with indentation force taken at $V_s = +3.5$ V, (b) I–V characteristic taken at $F = 1000$ nN.

Sample bias (V)	Resistance (MΩ)	Current (nA)
0	$10^{6.78}$	0
1	$10^{6.90}$	0.00012
2	$10^{6.38}$	0.00082
2.5	$10^{6.57}$	0.00067
3	$10^{6.20}$	0.00190
3.5	$10^{5.83}$	0.00518
4	$10^{5.58}$	0.01057
5	$10^{5.32}$	0.02372
6	$10^{5.07}$	0.05067
7	$10^{4.79}$	0.11384

Table 3.1 Resistance and current values of the plots in Figure 3.5(b).

3.3 Results and discussion

3.3.1 Resistance under dark and illuminated conditions

Figure 3.6(a) and (b) show SSRM resistance images taken on the cross-section of a CdTe device in the dark and with the AFM laser being turned on, respectively. An indentation force of $F = 1000$ nN and sample bias of $V_s = +4$ V minimize the contact resistance on CdTe. Figure 3.6 (c) is the corresponding AFM topography image taken simultaneously with Figure 3.6 (a). Because of the large indentation force, significant material on surface is removed by the diamond coated tip, and the surface morphology was largely changed on the scanned area. Thus, Figure 3.6 (c) reflects the topography after the removal of material. The color scales are logarithmical on the resistance images

and linear in the AFM image.

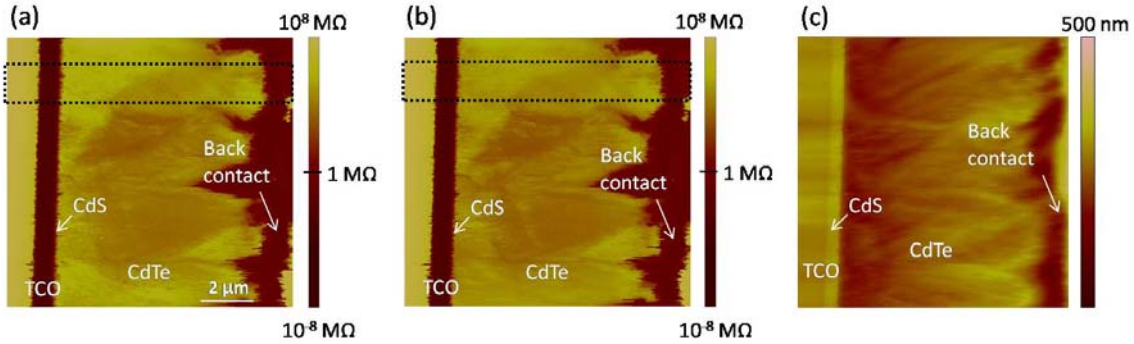

Figure 3.6 (a) SSRM resistance image in the dark, (b) SSRM resistance image with the AFM laser on, and (c) the corresponding topography image.

The TCO, CdTe, and back contact layers marked in Figure 3.6 can be distinguished in both the resistance and topography images. The CdS layer (~80 nm) and i-ZnO layer (~100 nm) are too thin to be identified in this 10-µm scale image. Figure 3.6 (a) and (b) illustrate that the resistance of the CdTe layer is highly nonuniform, with a range from 10^3 MΩ to 10^6 MΩ in the dark and from 10^3 MΩ to 10^5 MΩ in laser illumination. This nonuniformity inside CdTe is generated from inhomogeneous doping or the carrier concentration difference between grains. The region of CdTe close to TCO has the relatively larger resistance, which is caused by the carrier depletion near the p-n junction.

To have a better insight into the resistance distribution across the device, we obtained a resistance profile by averaging the 20 lines contained by the dashed rectangular region in Figure 3.6 (a) and (b). This area has a relatively uniform resistance. The averaged resistance profiles in dark and under laser illumination are shown in Figure 3.7(a). Under dark conditions, the resistance of the CdTe layer increases significantly from the back contact to the junction (the CdTe/CdS interface). The width (~3 µm) over which this resistance increase occurs is consistent with the depletion region of the device. Because

the carrier concentration in n-type CdS is about 1000 times larger than p-type CdTe, the junction of CdS/CdTe is an n^+-p junction, and the depletion region is almost all inside CdTe. Under the AFM laser illumination, this high resistance in the depletion region disappears. The depletion region should be dominated by photocarriers generated by the AFM laser.

The resistance profiles can be converted to carrier concentration profiles using equation (2.3). The radius of the diamond coated tip in this experiment is $r = 35$ nm. The hole mobility of CdTe is $\mu = 5\ \mathrm{cm^2V^{-1}s^{-1}}$ [63]. Thus, the relation between carrier concentration and resistance in CdTe is:

$$N = \frac{1}{4r\mu eR} = \frac{1}{4 \times 35\ \mathrm{nm} \times 5\ \mathrm{cm^2V^{-1}s^{-1}} \times (1.6 \times 10^{-19}\ \mathrm{C})} \times \frac{1}{R}\mathrm{cm^{-3}}$$
$$= 8.9 \times 10^{23} \times \frac{1}{R}\mathrm{cm^{-3}} \quad (3.2)$$

For other layers of the device, the coefficient before $1/R$ is determined by the value of the mobility. Because the change of the carrier concentration under different circumstances should mostly happen in the depletion region, and the depletion region is mostly inside the CdTe, we can focus on the electric properties of the CdTe layer. Also, the resistance change in different layers is much larger than the mobility difference of device layers, so equation (3.2) is a good estimate to calculate the carrier concentration across the whole device. Therefore, for the sake of simplicity we can use equation (3.2) for the entire device.

Figure 3.7 (b) is the carrier concentration profiles calculated from the resistance profiles in (a) using equation Figure 3.7. In the dark, the carrier concentration inside the CdTe layer is 10^{11}~10^{12} cm^{-3}. This is much smaller than the value measured by other methods [48, 64]. There are three possible factors that can significantly affect the estimate of carrier concentration from SSRM. The first is the effective contact area. We

used the nominal probe radius, which can be much larger than the effective contact radius because not every probe/sample contact area opens adequate conduction channels. Secondly, we took a literature value of mobility, which was measured over a large sample area. The mobility can, in reality, be highly nonuniform in this polycrystalline material. Thirdly, but not the last, as shown in our measurement, the resistance is highly nonuniform over the device. It can change over one order of magnitude from one location to another, so the estimate of carrier concentration from the local resistance measurement can largely deviate from the average over a macroscopic device area. In fact, SSRM is a technique imaging the resistance/carrier distribution qualitatively in high spatial resolution of nm-scale, rather than a technique giving an accurate quantitative resistance/carrier measurement. The different layers and the nonuniformity can be seen clearly from the SSRM resistance image, which is not possible in macroscopic methods. Although the uncertainty of the tip shape and tip/sample contact greatly influence the value of the measured resistance, the relative resistance in different positions or at different bias voltages measured by the same tip is quite accurate.

As shown in Figure 3.7 (a) and (b), the carrier generation under AFM laser illumination significantly affected the resistance and carrier concentration in the depletion region. The blue dashed line in Figure 3.7 (b) is the difference between carrier concentrations under illumination and in the dark in the CdTe layer. It shows that the photocarrier concentration generated from the AFM illumination is almost constant in CdTe, with a concentration on the order of 10^{11}~10^{12} cm^{-3}. In the situation of a working solar cell, the light is incident through glass onto the device, so the photocarriers mostly concentrate near on the CdTe/CdS junction. But in this SSRM measurement, the AFM laser is incident perpendicular to the cross-section surface, and the illumination is

uniform, so the photocarrier concentration in the CdTe layer is nearly constant.

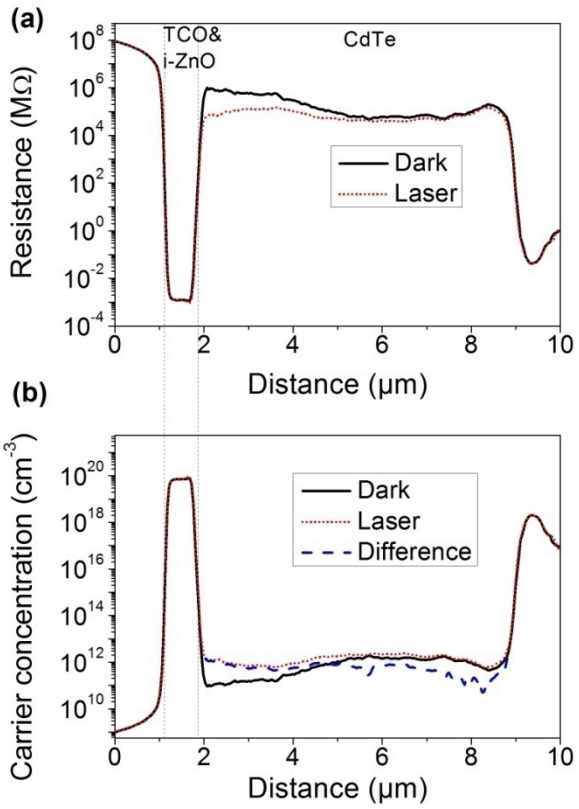

Figure 3.7 (a) The resistance profiles averaged over the rectangular areas in Figure 3.6(a) and (b). (b) The profiles of carrier concentration distribution calculated from (a).

The photocarrier concentration generated from the laser can also be estimated. Assume the intensity of the AFM laser is I; then we have

$$AIt = N_{photon}h\nu \tag{3.3}$$

where A is the area of the laser spot, t is the lifetime of the carriers in CdTe, N_{photon} is the number of photons arriving from the AFM laser in the interval t, and ν is the frequency of the photons. Assume the quantum efficiency is 100%: that is, each photon incident on CdTe generates an electron-hole pair. Then the number of photocarriers is

$$N = 2N_{photon} = \frac{2AIt}{h\nu} \tag{3.4}$$

Because the photons are mostly absorbed within penetration depth l, the photocarrier concentration is

$$n = \frac{N}{Al} = \frac{2It}{lh\nu} \tag{3.5}$$

The intensity of the AFM laser is 0.1 W/cm^2. Most of the laser is blocked by the probe cantilever. Assume only 1% of the laser is received by the local sample area beneath the probe: then I is 10^{-3} W/cm^2. Assuming a carrier lifetime of 0.5 ns [65], a penetration depth of 1 μm [48], and a laser photon frequency of 4×10^{14} Hz, the photocarrier concentration can be calculated as

$$n = \frac{2It}{lh\nu} = \frac{2 \times 0.1 \text{ W/cm}^2 \times 0.5 \text{ ns}}{1 \text{ μm} \times (6.63 \times 10^{-34} \text{ m}^2\text{kg/s}) \times (4 \times 10^{14} \text{ Hz})} = 3.8 \times 10^{12} \text{ cm}^{-3} \tag{3.6}$$

which is in the same order as the carrier concentration difference in Figure 3.7(b).

3.3.2 Resistance under forward and reverse bias

To investigate the resistance and carrier concentration distribution of the junction under forward bias and reverse bias, voltage was applied to the device between the TCO and back contact, as shown in Figure 3.8. The tip was virtually grounded. For $V_b = +1$ V forward bias measurement, 4.5 V and 3.5 V were applied to the back contact and TCO, respectively. For the corresponding $V_b = 0$ V reference bias, 4.5 V was applied to both the back contact and TCO. For $V_b = -1$ V reverse bias measurement, 3.5 V and 4.5 V were applied to the back contact and TCO, respectively. For the corresponding $V_b = 0$ V reference bias, 3.5 V was applied to both the back contact and TCO. The

reason for changing sample bias on CdTe when changing V_b polarity is that if the voltage difference between sample and tip is larger than 5 V, the high current can easily make the tip damaged and the resistance signal gets unstable.

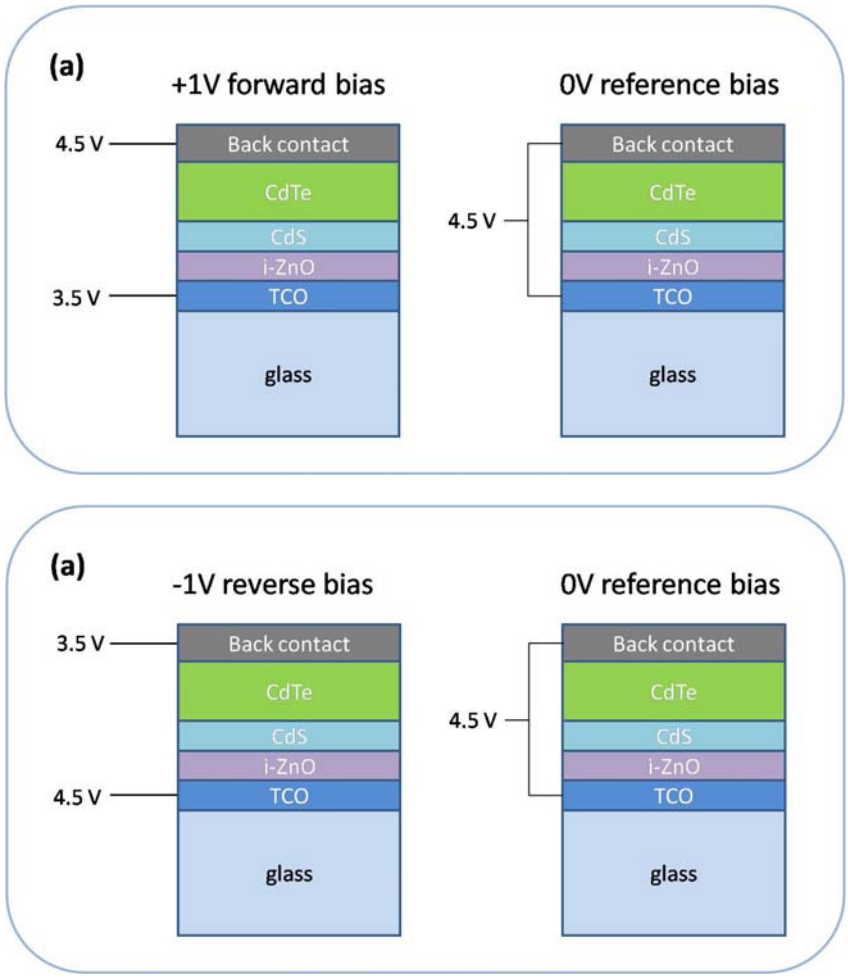

Figure 3.8 Schematic of the voltage connection for (a) +1V forward bias and (b) -1V reverse bias and the corresponding 0 V reference bias

We first investigate the resistance under forward and reverse bias at the 5 μm scale, so that the whole depletion region can be observed in the image. As shown in Figure 3.6,

the resistance in CdTe is highly nonuniform. If we take the resistance image for zero bias and for forward/reverse bias at different locations on the sample, the nonuniformity of the resistance in CdTe might be larger than the resistance change caused by forward/reverse bias. It will be difficult to identify the resistance change caused by forward/reverse bias. Thus, for the sake of comparison it is necessary to take the resistance images under different biases in exactly the same location on the sample.

To test whether the resistance signal keeps stable for multiple scans, we took resistance images four times at the same location on the sample under zero bias with a tip indentation force of 2000 nN. Figure 3.9 shows the resistance profiles of the four scans. Each profile is the average of 30 lines of the resistance image. The small fluctuations for different scans are caused by the fluctuation of the tip status when scanning. The diamond-coated tip removes about 50 nm depth of the material for each scan. The resistance in CdTe is relatively uniform within 100~200 nm depth, so the vertical nonuniformity of CdTe will not significantly influence the measurements. Figure 3.9 shows that it is practicable to scan multiple times in the same location of the sample to compare resistance profiles. To ensure that the tip status keeps stable for multiple scans, for both forward and reverse bias, we scanned four times in the same location to compare the resistance between zero bias and forward/reverse bias. The sample was applied with zero bias for the first and third time, and applied forward/reverse bias for the second and fourth scan. If the resistance profiles of zero bias in first and third scans overlap well, and the resistance profiles of forward/reverse bias in the second and fourth also overlap well, then the tip is stable and the measurement is reliable.

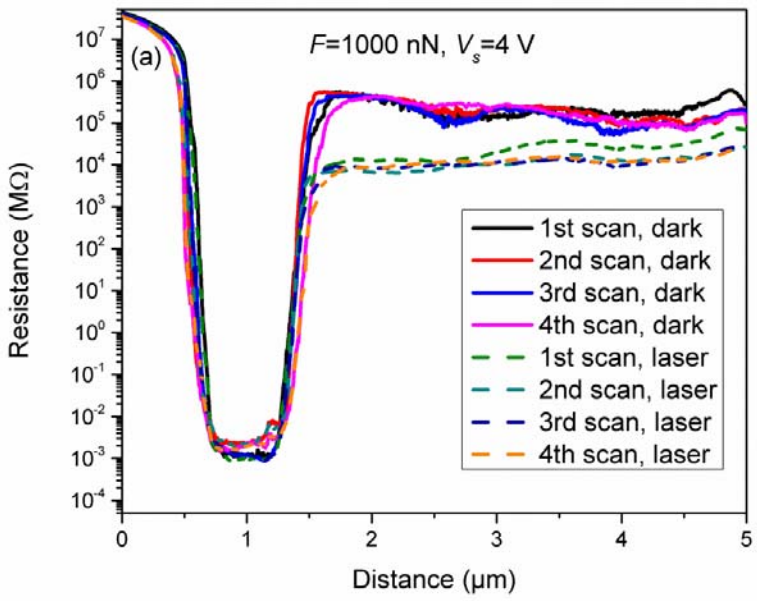

Figure 3.9 Test of the four scans in the same location. Each line is the average of 30 profile lines in a resistance image.

Figure 3.10 compares the resistance of the device under zero bias and forward bias. In Figure 3.10 (a), the resistance in thermoequilibrium state ($V_b = 0$ V in dark shown as the red line) is relatively large close to the CdTe/CdS interface because of carrier depletion in the depletion region. Approaching the right side, the resistance reduces, which is compatible with Figure 3.7. With a forward bias $V_b = +1$ V applied to the device [blue curve in Figure 3.10 (a)], the resistance in the deep depletion region drops more than one order of magnitude. When a p-n junction is in forward bias, the built in voltage is smaller than in equilibrium. The diffusion current across the junction increases, so the carriers inject into the depletion region. As a result, the resistance in depletion region drops in forward bias. Thus, the experimental result is compatible with the device physics. Notice that Figure 3.5 (b) shows that the measured resistance is different in

various sample bias because the tip-sample nanocontact is a Schottky junction. The measured resistance of CdTe changes for about 0.4 orders of the magnitude when the sample bias V_s is within the range of 3.5V~4.5V. This amount is much smaller than the resistance difference between V_b =0V and V_b =1V in forward bias in Figure 3.9. Thus, the resistance change in Figure 3.9 reflects the carrier concentration change of the junction in forward bias. Also, we took plenty of data in multiple samples with different tips. Figure 3.12 shows some of the data. The resistance drop in depletion region in forward bias is fairly repeatable.

When the AFM laser was turned on, as in Figure 3.10 (b), the resistance profile became flat compared with the thermoequilibrium state ($V_b = 0$ V in dark). The resistance in the deep depletion region dropped about two orders of magnitude as compared with the thermoequilibrium state, and about one order of magnitude as compared with the case of carrier injection ($V_b = +1$ V in dark). According to equation (3.2), the carrier concentration is inversely proportional to the resistance. The measurement indicates that the photocarrier concentration under illumination is about two orders of magnitude larger than in thermoequilibrium, and one order of magnitude larger than in the carrier injection case in forward bias. Thus under illumination, the photocarriers dominate the total carrier concentration. As a result, resistance was measured flat across the depletion region and only a very small increase of the resistance was observed when a +1 V forward bias was applied to the device.

From Figure 3.10, one sees that the resistance in TCO and i-ZnO layers in 1V forward bias increases both in dark and illumination. This is not the property of the junction. Since the carrier concentration in n-type TCO and i-ZnO is very large, the change of it in forward bias should be relatively too small to be measured. The reason

that we observed this resistance change in TCO and i-ZnO is that the contact resistance was not minimized in these layers, so the measured resistance is dominated by the tip-sample Schottky junction. The TCO layer was applied with smaller sample voltage in 1V forward bias than in 0V bias (see Figure 3.8), so the contact resistance in 1V bias is larger than 0V bias. Since the TCO and i-ZnO layers are very rigid, the tip needs to apply extremely large indentation force to reduce the contact resistance. [Notice that in Figure 3.6 (c), the material removed by the tip in TCO and i-ZnO is much less than in CdTe layer]. However, if we apply too large indentation force from tip to the sample, the diamond coating on the tip may wear off quickly. Because the depletion region is mostly on CdTe layer, it is more important to optimize the measurement in CdTe layer. Thus, we did not apply too large indentation force to minimize the resistance in TCO in the experiment.

The comparison of resistance profiles under zero bias and reverse bias in dark is shown in Figure 3.11(a). In reverse bias, carriers move out of the depletion region, so the resistance inside the depletion region in CdTe should be expected to increase. In Figure 3.11 (a), although there is a small resistance increase in the depletion region, the difference is much smaller than in Figure 3.10(a). A possible reason is that the potential on the sample is higher than the potential on the tip, since the sample bias is positive, so the tip will attract holes and repel electrons in the sample. In p-type CdTe, the electron is the minority carrier, so the effect of repelling electrons from the tip does not greatly affect the resistance, while the attraction of the holes by the tip reduces the measured resistance. This effect is not obvious when the carriers in sample are much more numerous than the attracted holes, as is the situation in Figure 3.10. When reverse bias is applied to the device, the carrier concentration in the depletion region is lower than 10^{11}

cm^{-3} and the holes attracted by the tip dominate the measured resistance; thus, the increase of the resistance in the depletion region is difficult to detect. This result is repeatable according to the data on different CdTe samples (see Figure 3.13).

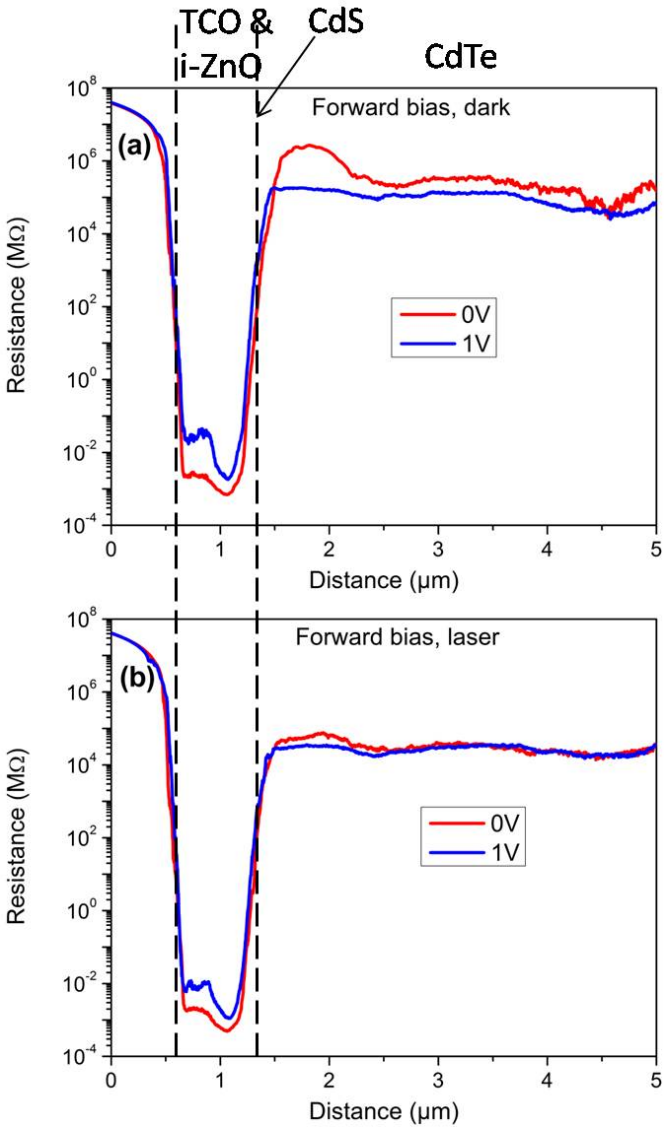

Figure 3.10 Resistance profiles on a 5-μm scale (a) in the dark and (b) with AFM laser illumination. The profiles were taken in the same local sample area with $V_b = 0\,\mathrm{V}$ and $+1\,\mathrm{V}$ forward bias.

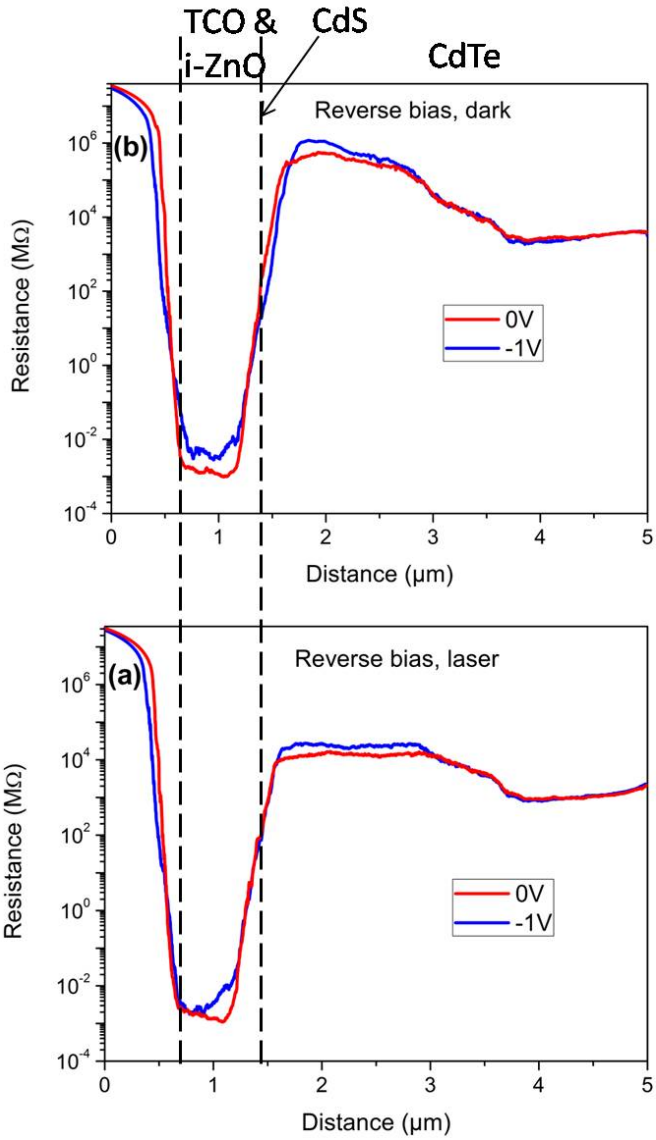

Figure 3.11 Resistance profiles on a 5-μm scale (a) in the dark and (b) with AFM laser illumination. The profiles were taken in the same local sample area with $V_b = 0\,\mathrm{V}$ and $-1\,\mathrm{V}$ reverse bias.

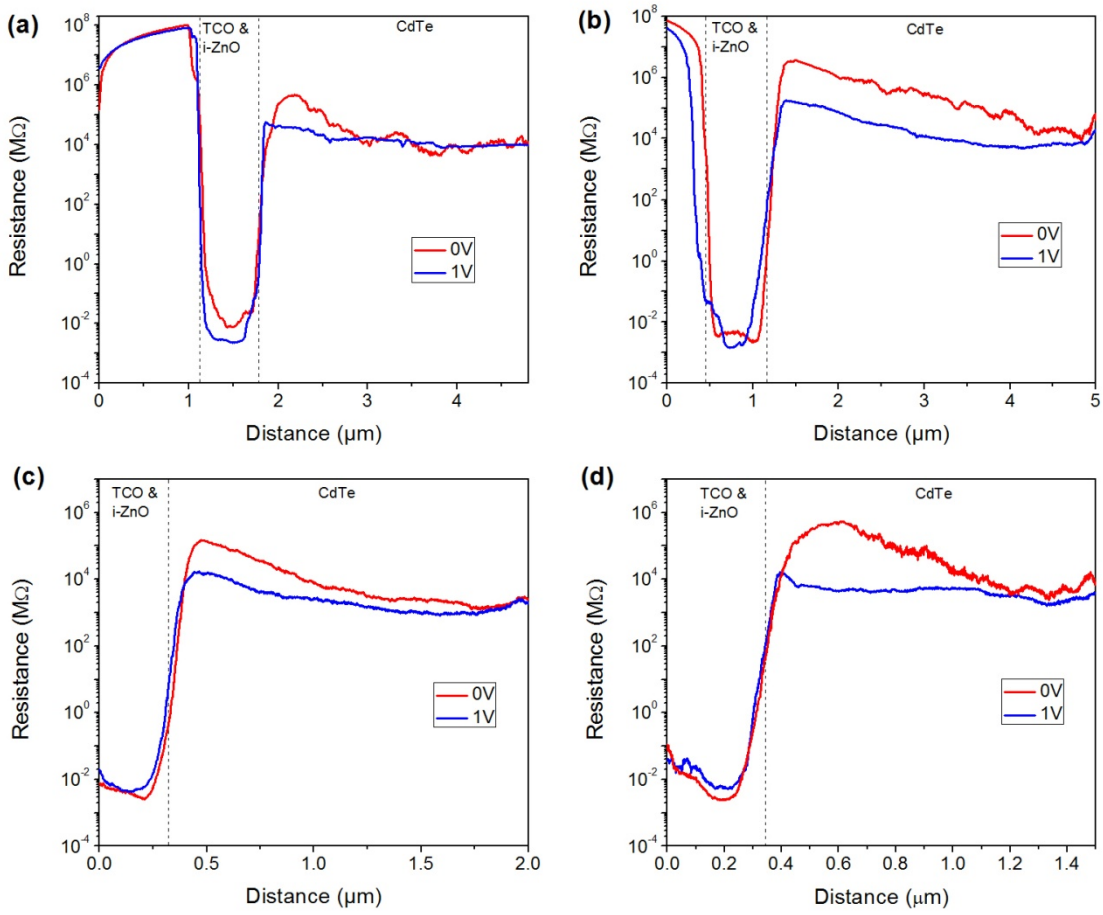

Figure 3.12 Resistance profiles data of 0V and 1V forward bias taken on the cross-sections of different samples

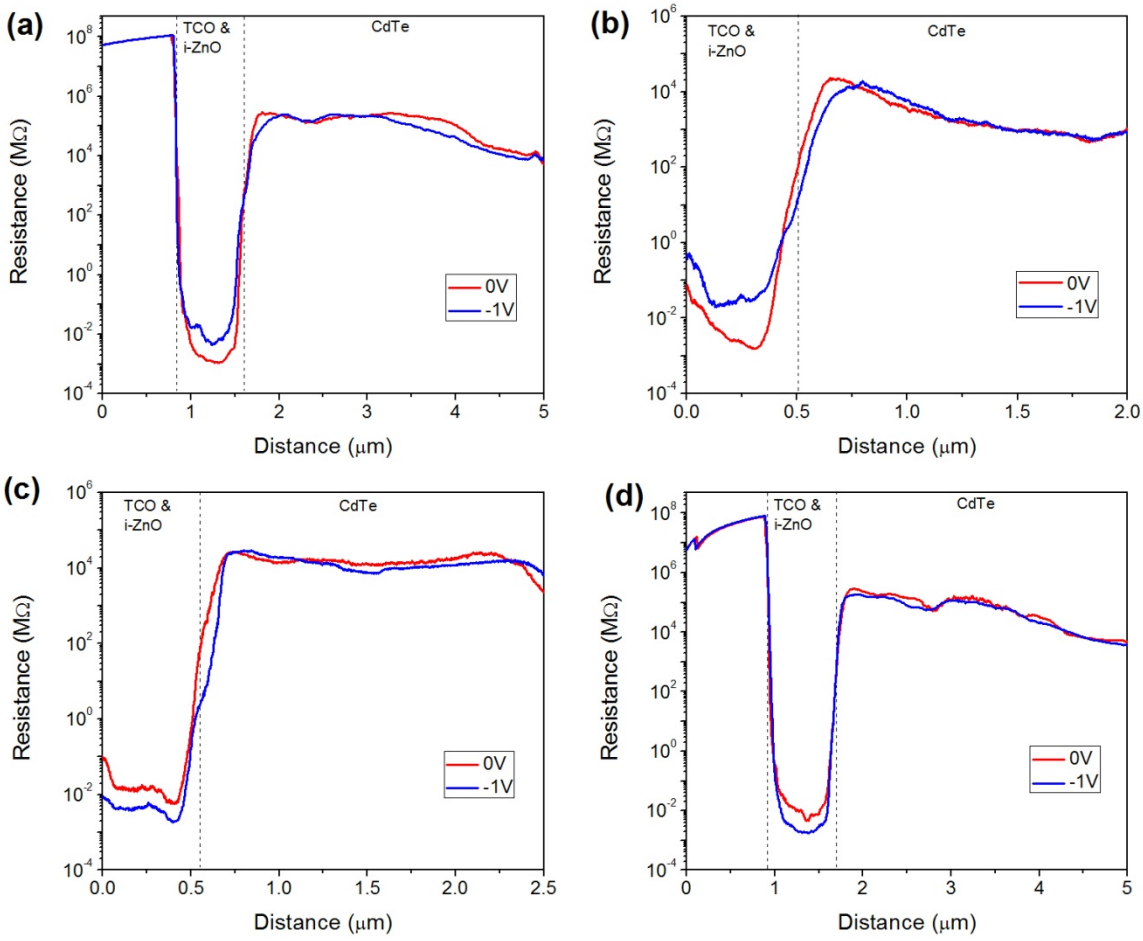

Figure 3.13 Resistance profiles data of 0V and -1V reverse bias taken on the cross-sections of different samples

We further study the change of the resistance near the junction under forward/reverse bias at a smaller scale. Figure 3.14 (a) is the resistance image near the CdS/CdTe junction at the 1.5 μm scale, taken with F = 1000 nN indentation force in dark. The upper half of this image is taken under zero bias; the lower half is taken under +1 V forward bias. In this 1.5 μm scale image, the position of the 80 nm CdS layer and 100 nm i-ZnO layer is critical. To correlate the resistance profile with the device layers, a 3 μm-scale

topography image with a small indentation force of $F = 25\,nN$ on the same location of the sample was taken [Figure 3.14 (b)] after taking the resistance image. Figure 3.14(b) shows that significant material was removed by the tip and the surface morphology was largely changed in the rectangular area scanned with 1000 nN force while taking the resistance image. Because the mechanical properties of the device layers are different, the amounts of material removed are different in different layers. In the area not scratched by the tip, a 550 nm layer can be identified, as marked in Figure 3.14 (b). It is the same thickness as the TCO layer (450 nm) and the i-ZnO layer (100 nm) and presumably corresponds to those layers. Because these two layers are very rigid, they could not be polished as flat by the Ar^+ beam as the other layers. It can be also seen that these layers were removed less in the dip scratched by the 1000 nN force applied by the tip. In Figure 3.14 (c), the topography image of Figure 3.14 (b) is superposed with Figure 3.14 (a). Since the thickness of i-ZnO (100 nm) and CdS (80 nm) is known, one can identify the boundaries of layers and correlate the resistance image with the positions of the layers.

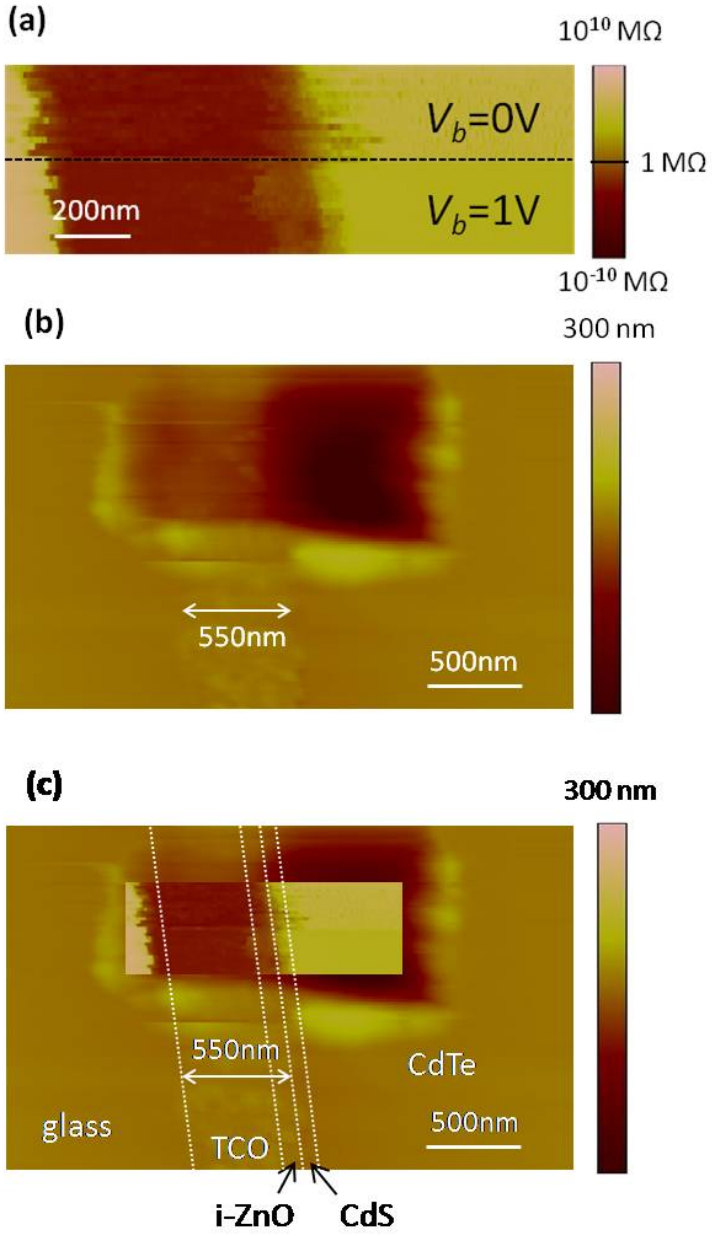

Figure 3.14 SSRM images of (a) $V_b = 0$ V and $V_b = +1$ V forward bias in dark. (b) is the topography image scanned with F=25 nN small indentation force after (a) was taken. (c) is the topography image from (b) being superimposed with the resistance image from (a). The locations of the different layers are marked.

Figure 3.15(a), the same as Figure 3.14(a), is the resistance image taken in the dark. Figure 3.15(b) is the corresponding topography image, showing that the tip did not significantly change when V_b was changed during scanning. The resistance profiles averaged from Figure 3.15(a) in dark and in illumination are shown in Figure 3.15(c). The drifts are corrected manually, and the layer positions are indicated. Generally, the location of the electrical junction should be the place where the hole density is equal to the electron density, where the total carrier concentration is minimum and the resistance is maximum (as shown in Figure 3.19 in section 3.4). Thus, the resistance close to the CdS/CdTe interface in Figure 3.15 should increase when approaching to the right side of the CdTe. However, the resistance profile shows a plateau inside CdTe in experimental data. The reason is that when the carriers get deeply depleted, the resistance measured by SSRM in the depletion region is dominated by carrier attraction by V_b applied to the probe, as discussed previously in this section. The saturated resistance under $V_b = +1$ V forward bias is smaller than in the thermoequilibrium state, because the injection of the carriers into the depletion region provides more holes to be attracted by the tip. Similarly, the photocarriers under illumination cause more holes to be detected by the tip, so that the saturated resistance is lower. The reduction of the resistance in the depletion region under AFM laser illumination and under forward bias can be observed, which is consistent with Figure 3.10

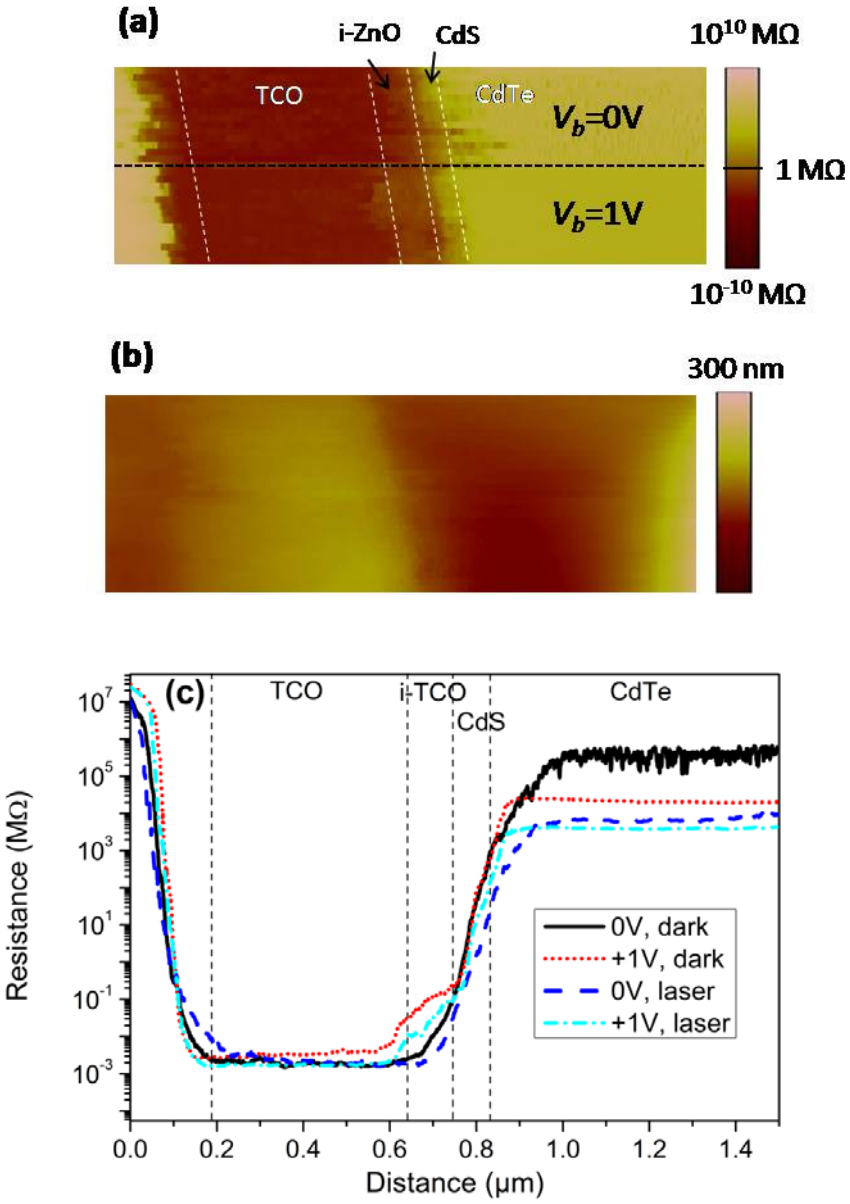

Figure 3.15 SSRM images of (a) $V_b = 0$ V and $V_b = +1$ V forward bias, and (b) the corresponding topography image. (c) is the resistance profiles averaged over the resistance images in (a) with drift corrected.

Figure 3.16 represents resistance and height images taken under zero bias and

$V_b = -1$ V reverse bias, and the corresponding averaged resistance profiles. Similarly to Figure 3.15, carrier attraction by the tip causes a plateau in the resistance in CdTe. The reduction of the resistance drop under illumination is consistent with Figure 3.7.

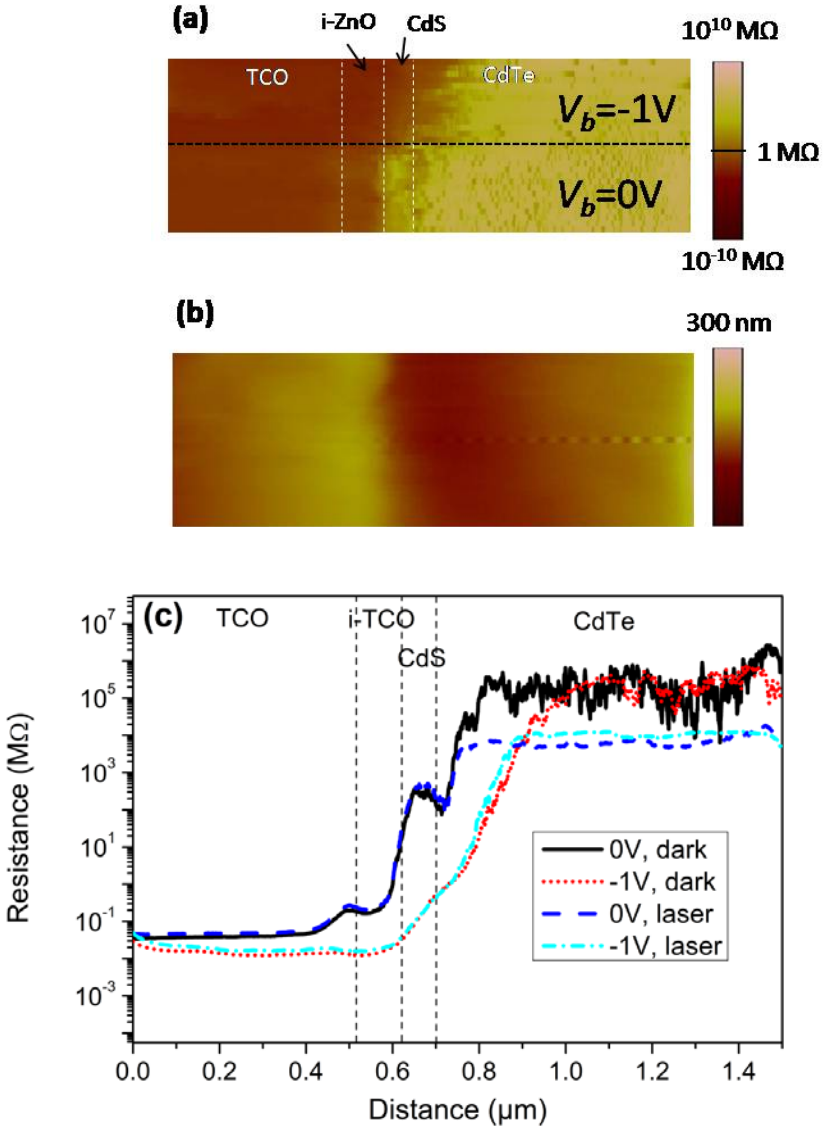

Figure 3.16 SSRM images of (a) $V_b = 0$ V and $V_b = -1$ V reverse bias, and (b) the corresponding topography images. (c) is the resistance profiles averaged over resistance images (a), with drift corrected.

Figure 3.15 and Figure 3.16 also indicate that the resistance profiles of 0V and -1V in CdTe in dark are very noisy. Because the resistance of CdTe in these situations is large, the current which flows from the sample to tip is very small. Thus, the signal to noise ratio of the current detected by the instrument is small in these conditions. The larger resistance of the sample, the noisy the data will be.

3.4 Simulation using PC1D software

PC1D is a software package widely used for solar cell simulation. It was developed at the University of New South Wales [66]. It numerically solves the basic equations for semiconductors using the finite element method [67]. The equations include the two-carrier semiclassical semiconductor transport equations:

$$J_n = \mu_n n \nabla E_{Fn}$$
$$J_p = \mu_p p \nabla E_{Fp} \tag{3.7}$$

the Fermi distribution function

$$n = N_C e^{-(E_C - E_{Fn})/kT}$$
$$p = N_V e^{-(E_{Fp} - E_V)/kT} \tag{3.8}$$

and Poisson's equation of electrostatics

$$\nabla \cdot (\varepsilon \nabla \Psi) = -\rho \tag{3.9}$$

The simulation of carrier concentration and resistance in CdTe solar cells using PC1D helps us better analyze and explain the experimental results of SSRM. The model of CdTe solar cells used in the simulation has the structure shown in Figure 3.17.

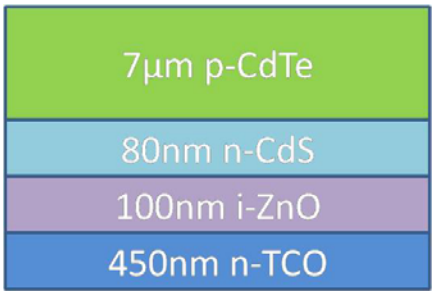

Figure 3.17 The structure of the CdTe model used in the simulation.

The parameters of the different layers, such as band gap, hole/electron effective mass, doping level, etc., are shown in Table 3.2.

	Doping type	Thickness (nm)	Doping level (cm^{-3})	Electron effective mass (m_e/m_0)	Hole effective mass (m_h/m_0)	Band gap (eV)	Dielectric constant	Affinity (eV)
TCO	n	450	10^{19}	0.4[68]	1.35[69]	3.57[70]	11.5[71]	4.9[72]
i-ZnO	n	100	10^{15}	0.24[73]	0.59[73]	3.24[74]	7.8[73]	4.5[75]
CdS	n	80	10^{17}	0.2[73]	0.8[76]	2.2[77]	8.9[78]	4.2[75]
CdTe	p	7000	10^{14}	0.1[79]	0.35[79]	1.5[48]	10.6[80]	4.4[81]

Table 3.2 Parameters used in the simulation of carrier concentration distribution in CdTe solar cells

The distribution of the hole and the electron concentrations across the device is shown in Figure 3.18. From the CdS/CdTe interface to the CdTe side of the depletion region, the hole density increases and the electron density decreases. Outside the

depletion region, the hole and electron densities reach the majority and minority doping levels in CdTe. The electrical junction is in the location where the electron density is equal to the hole density: this is marked as point B in Figure 3.18.

Figure 3.19 shows the simulated total carrier concentration and resistance. The black line in Figure 3.19(a) is the total carrier concentration calculated as the sum of the electron and hole density. The black line in Figure 3.19(b) is the resistance profile calculated from Figure 3.19(a) using equation (3.2). Figure 3.19 (a) and (b) illustrate that the electrical junction is in the location of the minimum value of the total carrier concentration and the maximum value of the resistance. The simulation shows that the depletion width is about 3 μm, and that the electrical junction is about 1.1 μm away from the CdS/CdTe interface. This is to be contrasted with the measured resistance profiles, which do not show a clear peak because of the carrier attraction by the tip. The depletion regions shown in the measured resistance profiles in Figure 3.7, Figure 3.10 and Figure 3.11 are all narrower and closer to the CdS/CdTe interface than the simulation.

To evaluate the affect of the hole attraction by the tip, we qualitatively draw the measured electron and hole density as dashed lines in Figure 3.18. The exact density of holes/electrons attracted/repelled by the tip is hard to estimate. Therefore, the values of the dashed lines in Figure 3.18 do not reflect the real measured values, but are adequate for a qualitative estimate. From Figure 3.18 one sees that the measured electrical junction marked as A, which is the position where the measured electron density equals the measured hole density, moves closer to the CdS/CdTe interface. One also sees that the measured depletion width decreases.

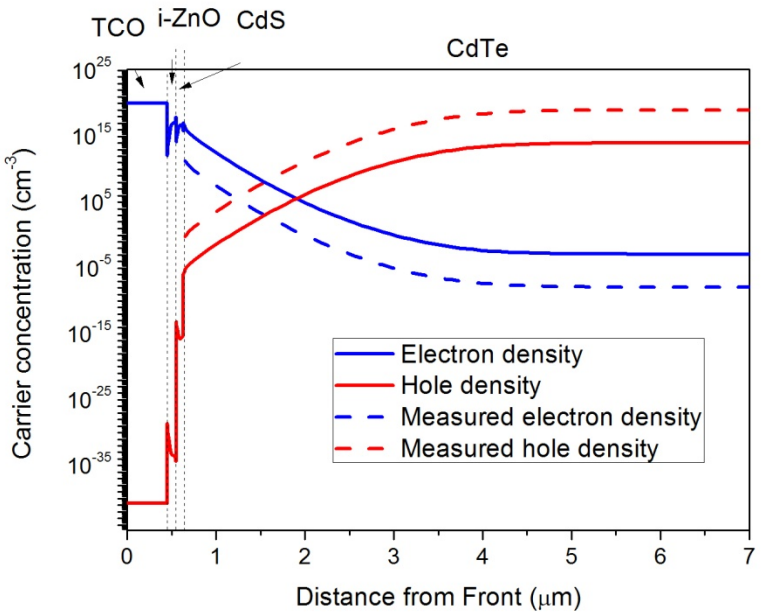

Figure 3.18 The simulated electron density (blue solid line) and hole density (red solid line) across the device. The dashed lines are the estimated electron and hole densities affected by the tip. A and B are the electrical junction affected and unaffected by the tip, respectively.

On the basis of equation (3.2) and the results shown in Figure 3.7, the photocarrier concentration generated by the AFM laser is around 10^{12} cm^{-3} in CdTe. Thus, we add 10^{12} cm^{-3} (blue dashed line) to the function shown by the black line in Figure 3.19(a) to get the carrier concentration profile due to the laser, which is shown as the red line in Figure 3.19(a). Figure 3.19(b) is the corresponding resistance profiles in the dark and under exposure to the laser. The injection of photocarriers by the laser causes the resistance peak in the depletion region to flatten into a plateau, which is consistant with the experimental result in Figure 3.15 and Figure 3.16.

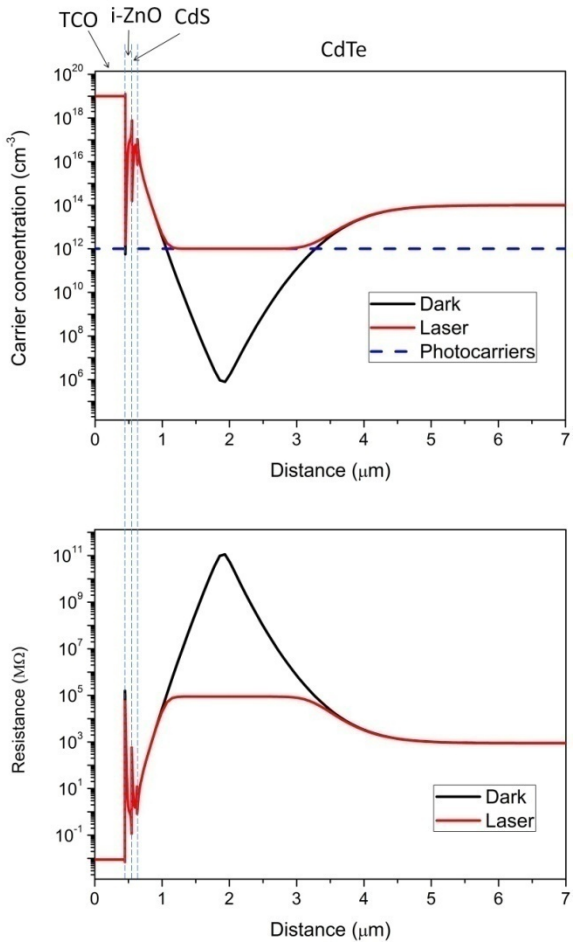

Figure 3.19 Simulated (a) carrier concentration and (b) resistance in a CdTe solar cell under dark (black solid line) and laser-illuminated (red solid line) conditions. We assume that the laser generates a uniform density of photocarriers (blue dashed line).

We further simulated the carrier concentration and resistance across the device under forward/reverse bias. Figure 3.20(a) shows the carrier concentration profiles for $V_b = 0\,\mathrm{V}$, $V_b = +1\,\mathrm{V}$ forward bias, and $V_b = -1\,\mathrm{V}$ reverse bias. Figure 3.20(b) represents the corresponding resistance profiles. The injection of carriers under $V_b = +1\,\mathrm{V}$ forward bias causes the reduction of resistance in the depletion region, which is indeed observed in the experimental result in Figure 3.15. The increase of the

resistance in the simulated depletion region under $V_b = -1$ V reverse bias is not observed in the experiment (Figure 3.16). Notice that the carrier concentration in the depletion region is as low as 10^6 cm^{-3} and 10^4 cm^{-3} for $V_b = 0$ V and $V_b = -1$ V, respectively. Therefore, the holes attracted by the tip dominate the carrier concentration in the depletion region which explains why the increase in the resistance cannot be observed in $V_b = -1$ V.

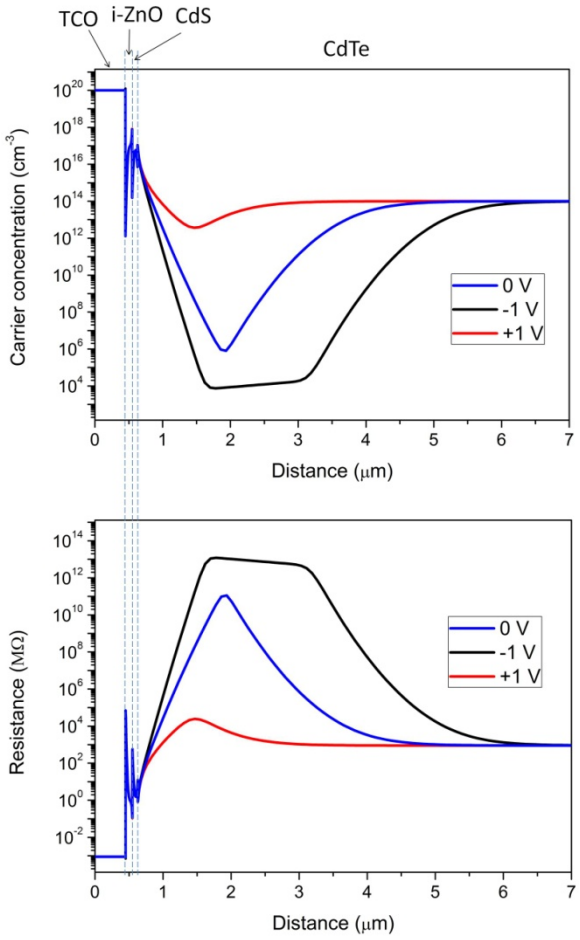

Figure 3.20 Simulated (a) carrier concentration and (b) resistance in a CdTe solar cell for the bias voltage 0V, -1V and +1V.

3.5 Conclusion

To summarize, we have studied the junction electrical properties of CdTe solar cells by mapping the resistance across the junction using SSRM. In order to minimize the probe/sample contact resistance R_c, it is critical to adequately indent the probe into the sample and apply a larger probe/sample voltage V_s than the onset value, so that the local spreading resistance of the sample beneath the probe can be measured. The multiple device layers were identified by resistance mapping. A high resistance region around the junction in the CdTe side was measured, due to carrier depletion. With carrier injection by applying a forward bias voltage V_b to the working device, the resistance in the deep depletion region decreased about one order of magnitude and the depletion region moved toward the CdS/CdTe interface. With AFM laser illumination, the resistance in the deep depletion region dropped about two orders of magnitude and the resistance across the entire device became relatively uniform due to the domination of photo-excited carriers over the carriers in the thermoequilibrium state and over the carriers injected by V_b. PC1D simulations of the resistance in dark and laser-illuminated conditions, and in forward and reverse bias, are presented. They are found to be consistent with the experimental results.

Chapter 4

Surface Potential Mapping on CIGS/CZTSe Solar Cells

Scanning Kelvin probe force microscopy (SKPFM) directly measure the electrostatic potential on surface of the sample with nanometer-scale spatial resolution. This technique was well used in investigating the electrical properties of the grains and grain boundaries on CIGS [82-84] and CZTSe [85, 86]. However, very rare studies about the cross-section of the CIGS and CZTSe device are reported [87, 88]. One of the difficulties is the technique to polish the cross-section of the device flat enough and keep the device not shunting. Previous measurement of the potential across CIGS junction was done on a model device deposited on the GaAs(110) substrate for determining the junction location [87]. However, the data should be improved because the cleaved cross-section, on which the SKPFM measurement was performed, had large corrugation so that suspicious artifacts could not be completely ruled out. The development of a polishing process using argon ion beam milling greatly improve the surface morphology, and achieved flat cross-sectional surface with a corrugation of ~20nm across the device that is adequate for the SKPFM measurements. In this chapter we will report our SKPFM results on the cross-section of the standard CIGS, ZnS(O,OH)/CIGS, CZTSe and CdTe devices.

4.1 Sample preparation

The standard CIGS, ZnS(O,OH)/CIGS and standard CZTSe devices are all deposited on Mo-coated soda-lime glass substrate. The standard CIGS device is composed with

~2μm three-stage co-evaporated CIGS, 60nm chemical-bath-deposited (CBD) CdS, 50nm intrinsic ZnO, 150nm ZnO:Al, Ni/Al grids and MgF_2 anti-reflective coating [33]. The ZnS(O,OH)/CIGS device is composed with ~2μm three-stage co-evaporated CIGS, 20nm ZnS(O,OH), 100nm ZnO:Al and Ni/Al grids. The structure of standard CZTSe device is ~1μm CZTSe, 60nm CBD CdS, 150nm ZnO:Al and Ni/Al grids. Figure 4.1 illustrates the structures of the three devices

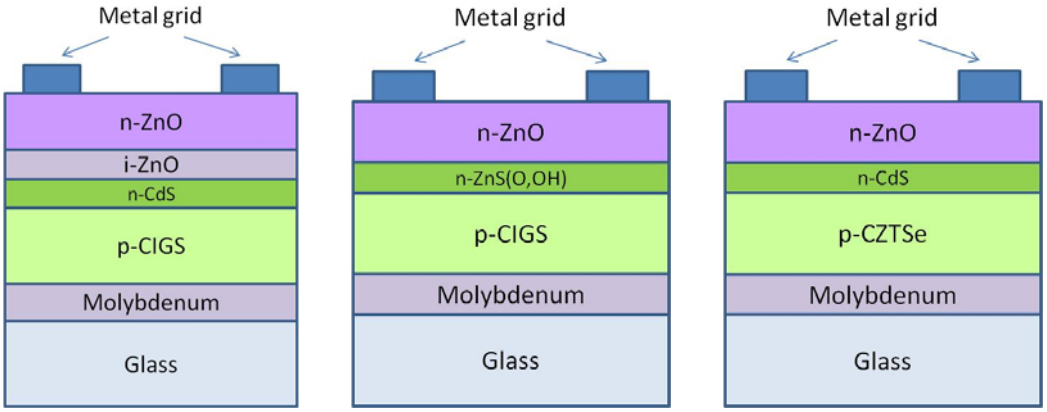

Figure 4.1 Schematic of (a) standard CIGS, (b) ZnS(O,OH)/CIGS, and (c) standard CZTSe solar cells

The cross section of the sample is prepared with the same method as described in section 3.1 for CdTe. However, SKPFM measurement requires better cross-sectional surface morphology than SSRM. Very thin layer of contamination on surface will highly influence the potential signal measured by SKPFM. Also, the corrugation of the cross-section should be within 30nm across the device layers to minimum the tip artifacts. Figure 4.2(a) shows a topography image of the cross-section with good surface morphology. The CIGS layer is well polished and the total corrugation across the device is within 30nm. Figure 4.2(b) shows the image of a not well-polished sample, where the

corrugation of CIGS is large. The factors of the large corrugation might be the short polishing time, unstable ion beam, or the bad sample quality.

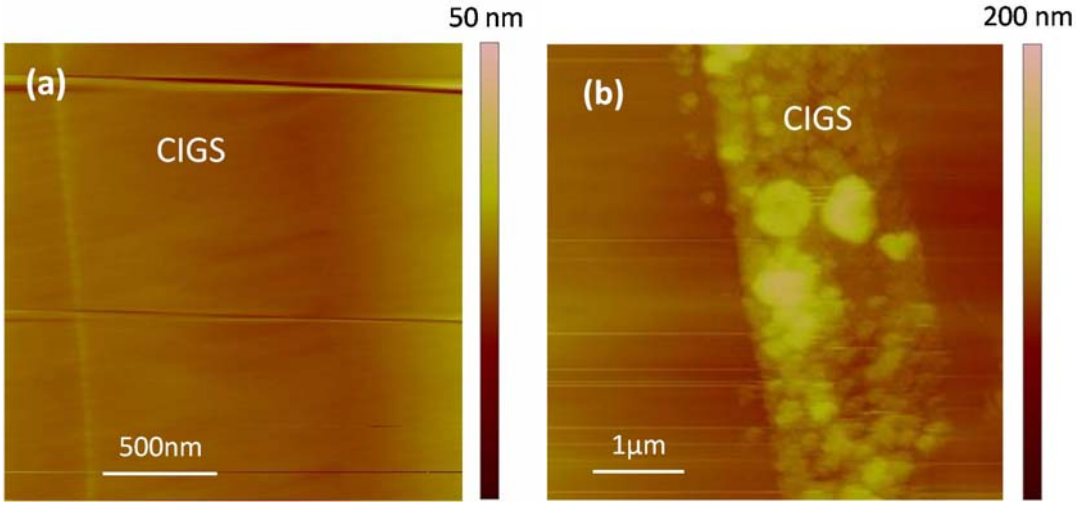

Figure 4.2 The AFM topography image of the (a) well-polished and (b) not well-polished cross-section of CIGS device.

Sometimes it is hard to polish the device flat enough if the cleaved surface of the sample is too rough. To achieve the flat enough cross-section, we polish at the same location of sample with ion beam for multiple times. In the first time, the cross-section is polished to get a relative flat area. Then the sample is polished again for one or more times to achieve a flat enough cross-section. Generally, the minimum time required for ion milling is 8 hours for 4kV ion beam, or 4 hours for 6kV ion beam.

4.2 Experimental setup

The AFM/SKPFM measurement was performed in Veeco AutoProbe CP scanning probe microscope using Pt-coated tips. In the experiment, the surface topography signal

was detected by the first resonance peak of the tip. The potential images were taken with both the low frequency and the second resonance peak. The two methods show the similar potential signal. The potential data presented in this thesis are all taken with low frequency. In the experiment, the tip and the molybdenum layer of the sample were virtually grounded. A bias voltage V_b was applied on the Ni/Al grid of the sample. Positive or negative V_b represent forward or reverse bias, respectively. The images were taken in the area with Ni/Al grid to avoid the tip dropping off during the scan. Figure 4.3 illustrates the setup for standard CIGS device. The setups for the other two devices are similar.

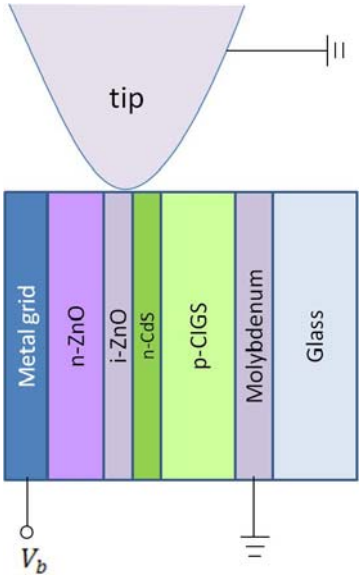

Figure 4.3 Schematic of the voltage applied on sample and on tip for SKPFM measurement on cross-section of standard CIGS sample

4.3 Results and discussions

4.3.1 Standard CIGS solar cells

The potential profiles along the junction of standard CIGS device in various bias V_b

across the cross-section of the device are shown in Figure 4.4. The corresponding AFM amplitude error image is on top. Each profile line is the average of 50 lines in the image to enhance the signal/noise ratio. The small potential variation for $V_b = 0\,V$ is due to the surface potential variation on different materials. The surface potential difference is smaller than the built-in potential in the bulk, which is due to the surface Fermi level pinning. If a bias voltage V_b is applied across the device, the position of Fermi level relative to the band configurations will not change, so the change in the surface potential should present the situation in bulk and the surface effect can be eliminated [87, 89, 90]. Figure 4.4(b) is the V_b-induced potential changes calculated by subtracting the potential profiles in different bias voltages with $V_b = 0\,V$. The variation of the potential for each profile between the metal grid and the molybdenum is smaller than the applied V_b. This is probably due to the potential losses in equipment, in other parts of the device and the long-range nature of Coulomb interaction [91]. The V_b-induced electric field [Figure 4.4 (c)] is calculated by taking the first derivative of the potential difference profiles in Figure 4.4 (b). Because the small perturbation in Figure 4.4 (b) may cause large noise in electric field difference profile, we smoothed the potential difference lines before taking the derivative.

Figure 4.4 (c) indicates that the peak of the V_b-induced electric field is close to the CdS layer. The small electric field peaks in other locations are induced by the contaminants on sample surface and the drift of the sample when taking the images. In order to identify the location of the V_b-induced electric field peak with high resolution, we took the smaller scale data near the junction on the cross-section of the CIGS, which is shown in Figure 4.5.

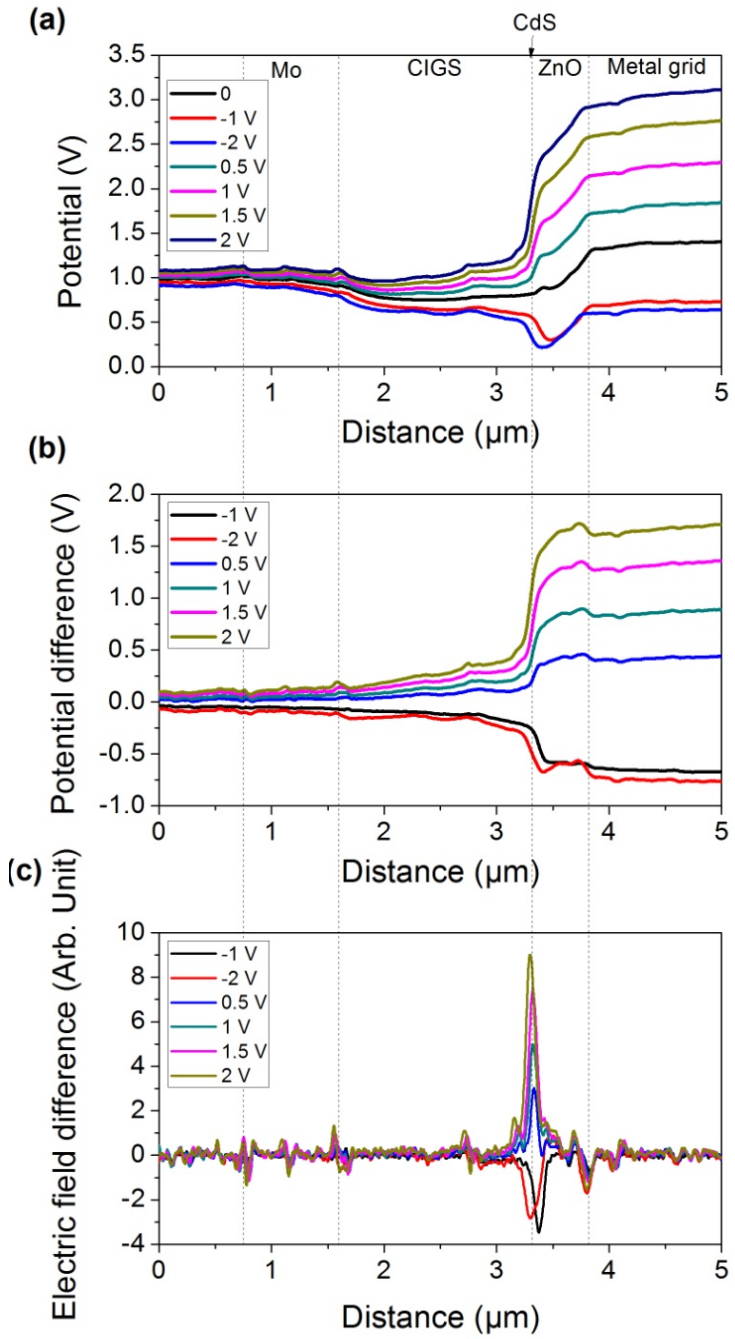

Figure 4.4 (a) The SKPFM electrical potential, (b) the V_b-induced electrical potential changes as subtracting $V_b = 0$ V in (a), and (c) the V_b-incuded change of the electric field as the derivative of (b), taken on the cross-section of standard CIGS device.

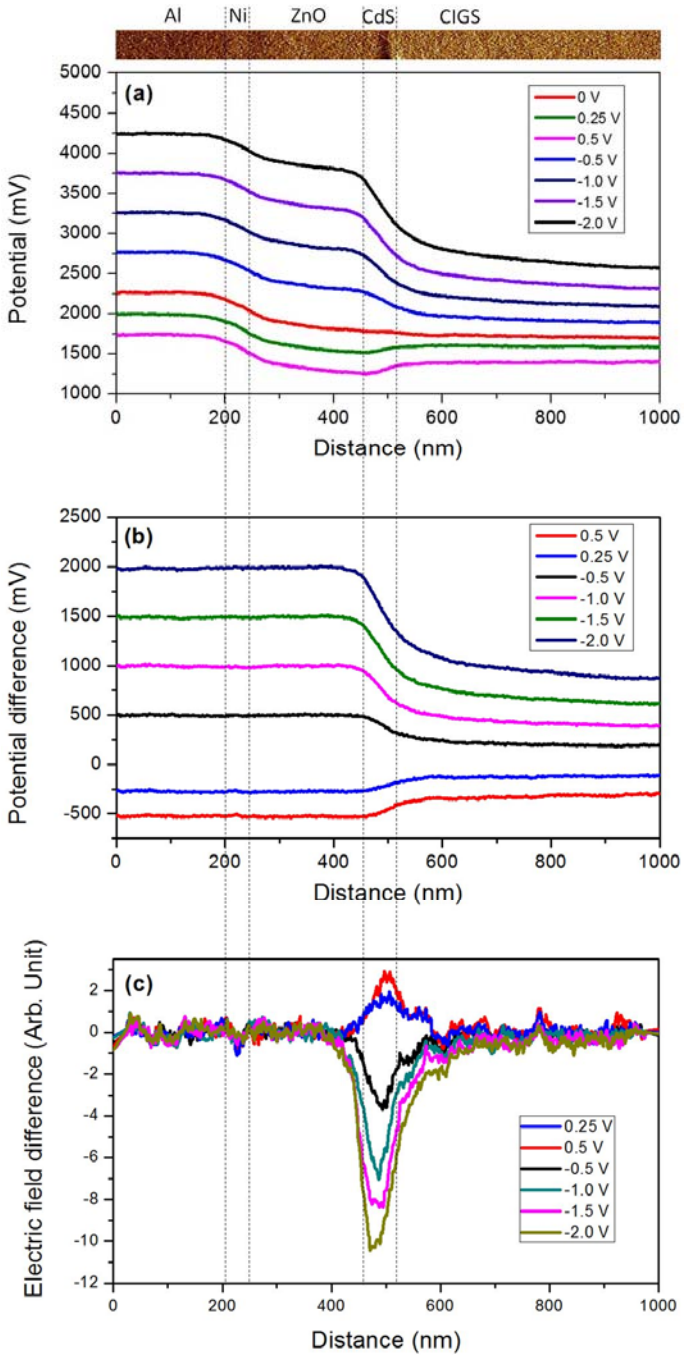

Figure 4.5 (a) The SKPFM electrical potential, (b) the V_b-induced electrical potential changes as subtracting $V_b = 0$ V in (a), and (c) the V_b-incuded change of the electric field as the derivative of (b), taken on cross-section of standard CIGS device. The corresponding AFM topography amplitude error image of the sample is on top.

It is difficult to identify the position of layers from the topography image on top of Figure 4.5. To correlate the profiles in Figure 4.5 with the position of the layers, we took a 1:1 AFM amplitude error image [Figure 4.6(a)] and an SEM image [Figure 4.6(b)] on the same location with Figure 4.5. Features A, B, C and D marked on AFM and SEM images can help to identify the position of the CdS buffer layer. The red point is the position of the V_b-induced electric field peak identified from the image above Figure 4.5. It illustrates that the peak of the electric field difference is inside the CdS layer and close to the CdS/CIGS interface. The position of the layers is marked in Figure 4.5. One sees that the electric field difference profiles extend to CIGS layer for about 200nm.

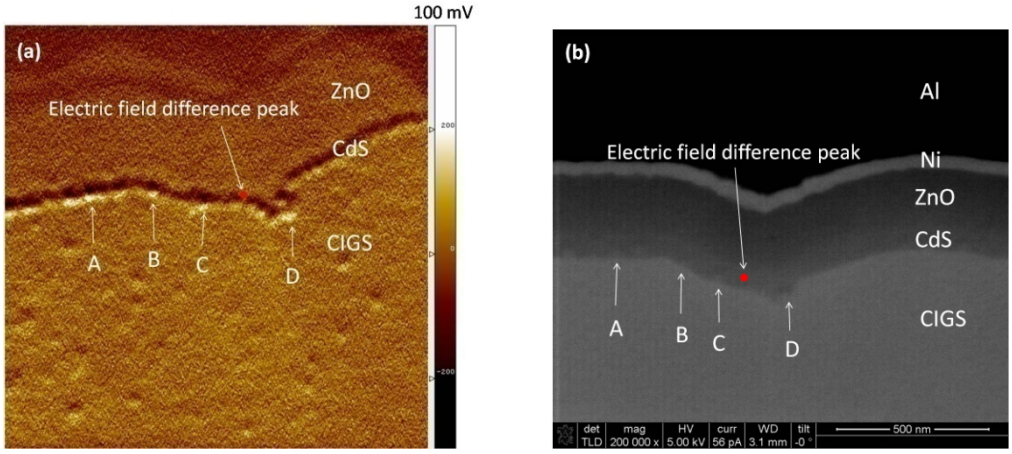

Figure 4.6 (a) The AFM amplitude error image and (b) SEM image taken on the same location with Figure 4.5. The marked features A, B, C and D can help to correlate the positions of layers in AFM and SEM images.

4.3.2 ZnS(O,OH)/CIGS and standard CZTSe solar cells

For ZnS(O,OH)/CIGS and the standard CZTSe devices, we used the same method to get the V_b-induced electric field profiles under different V_b as shown in Figure 4.7 and

Figure 4.8, respectively. The positions of the layers marked were also determined by comparing AFM and SEM images. The peaks of the V_b-induced electric field for these two devices are also inside the buffer layer close to metallurgical junction.

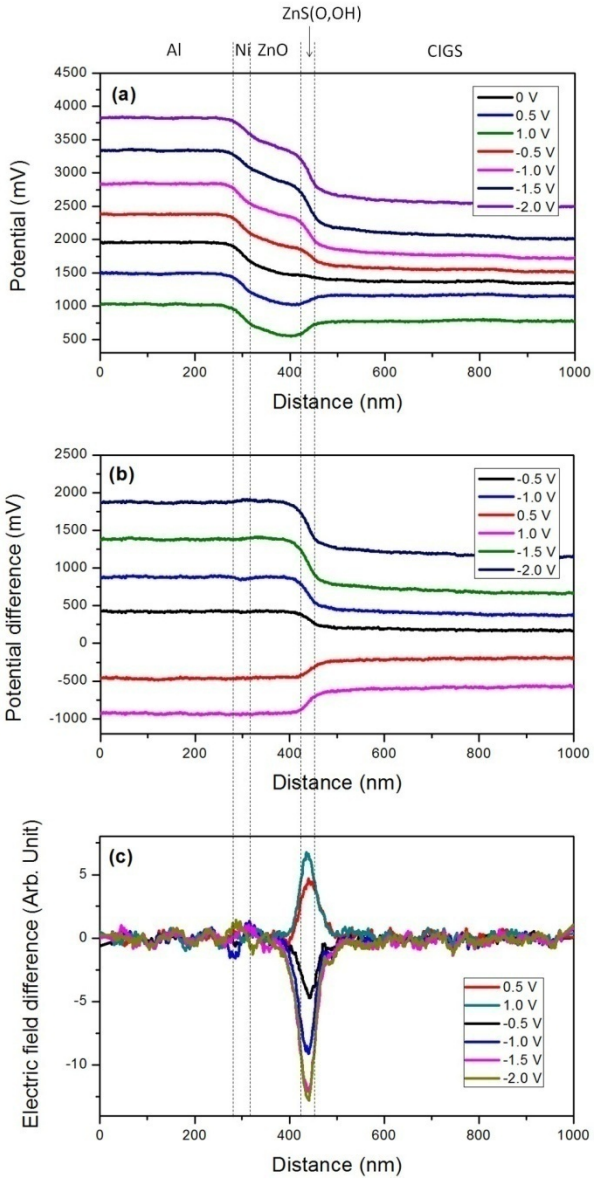

Figure 4.7 (a) The SKPFM electrical potential, (b) the V_b-induced electrical potential changes as subtracting V_b=0V in (a), and (c) the V_b-incuded change of the electric field as the derivative of (b), taken on cross-section of ZnS(O,OH)/CIGS device.

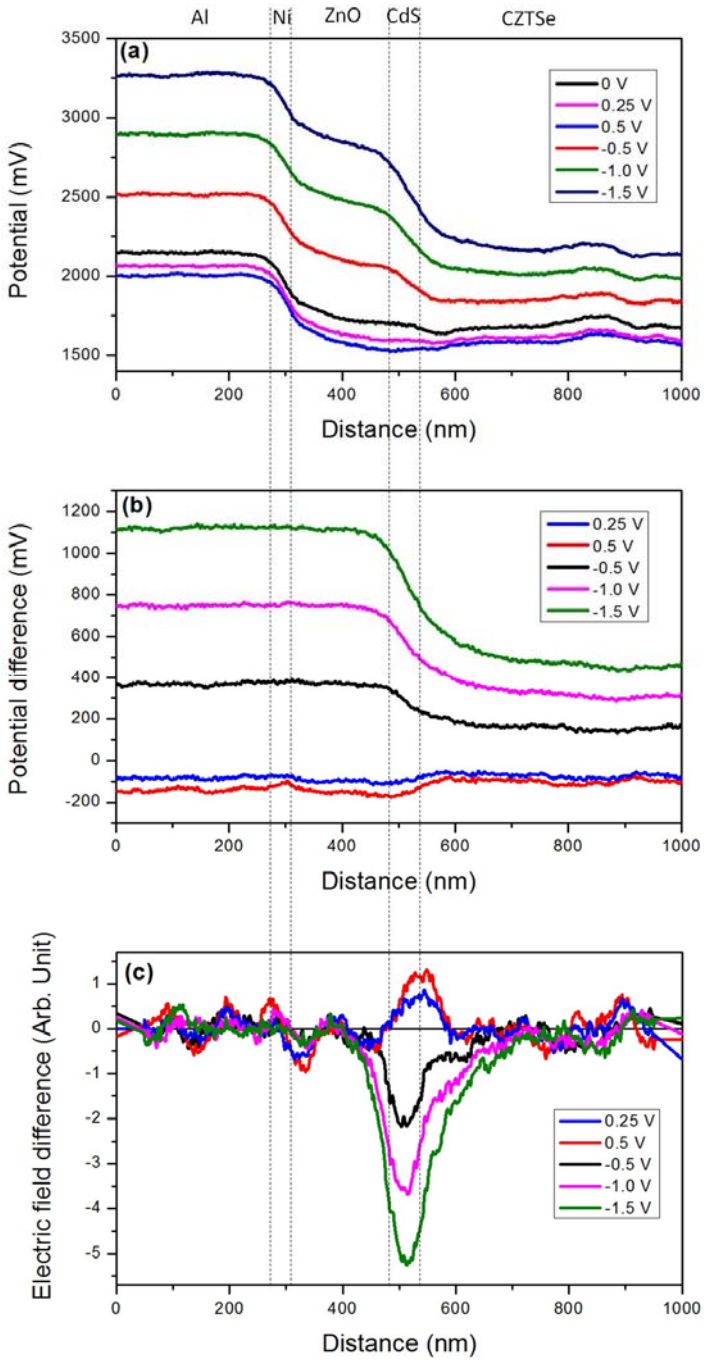

Figure 4.8 (a) The SKPFM electrical potential, (b) the V_b-induced electrical potential changes as subtracting V_b=0V in (a), and (c) the V_b-incuded change of the electric field as the derivative of (b), taken on cross-section of standard CZTSe device.

Compare the three electric field difference profiles in Figure 4.6, Figure 4.7 and Figure 4.8, one can find that the maximum of the electric field difference for these three devices are all inside CdS layer and are about 20nm away from the metallurgical junction. Considering the error in SKPFM measurement and in AFM/SEM is larger than 20nm, the resolution is not high enough to distinguish clearly whether the maximum of the electric field difference is in CIGS side or CdS side. The depletion widths for CIGS and CZTSe are both about 180nm. The depletion width for ZnS(O,OH)/CIGS layer is about 100nm, which is apparently narrower than CIGS and CZTSe devices.

4.4 Simulation using PC1D softward

Based on the previous research in other articles, the p-n junction could be either located on the CIGS/CZTSe side (homojunction) [92, 93], or is abrupt on the p-CIGS/n-CdS or p-CZTSe/n-CdS interface (heterojunction) [94-96]. To better study the structure of the junction from SKPFM data, we did simulation of the surface potential for CIGS, ZnS(O,OH)/CIGS and CZTSe devices in PC1D software [66]. Figure 4.9 indicates the heterojunction and homojunction models used in simulation for the three devices. For heterojunction, the p-n junction is in the location of metallurgical junction (CdS/CIGS or CdS/CZTSe). For homojunction, the p-n junction is buried inside CIGS or CZTSe. A layer of n-type CIGS/CZTSe is put in the device model in homojunction simulation. The p-n junction is in the location of p-CIGS/n-CIGS or p-CZTSe/n-CZTSe. Table 4.1 to Table 4.3 list the parameters for the material used in the simulation for CIGS, ZnS(O,OH)/CIGS and CZTSe, respectively.

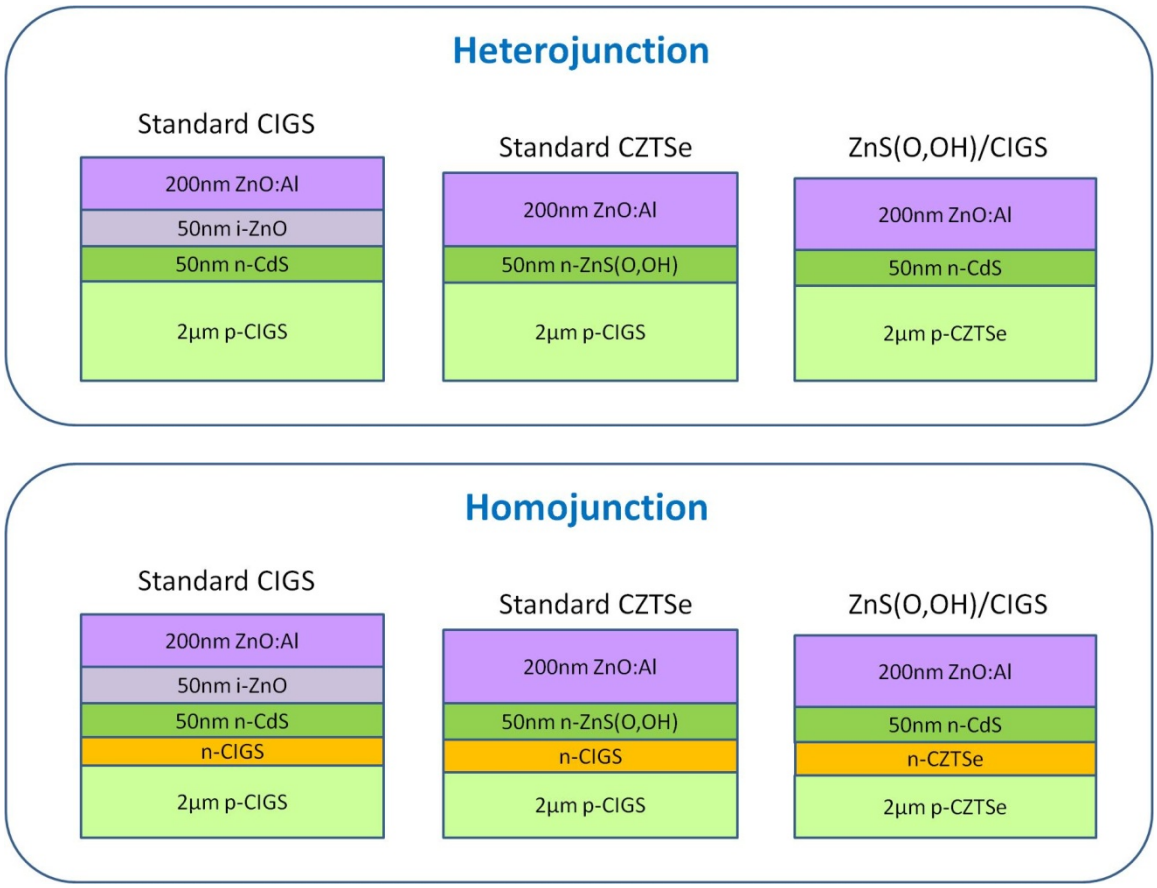

Figure 4.9 Schematic of heterojunction and homojunction model used in simulation for standard CIGS, ZnS(O,OH)/CIGS and standard CZTSe

	Doping type	Thickness (nm)	Doping level (cm^{-3})	Electron effective mass (m_e/m_0)	Hole effective mass (m_h/m_0)	Band gap (eV)	Dielectric constant	Affinity (eV)
ZnO:Al	n	200	10^{20}	0.24[73]	0.59[73]	3.24[74]	7.8[73]	4.5[75]
i-ZnO	n	50	10^{17}	0.24[73]	0.59[73]	3.24[74]	7.8[73]	4.5[75]
CdS	n	60	10^{17}	0.2[73]	0.8[76]	2.2[77]	8.9[78]	4.2[75]
CIGS	p/n	2000	2×10^{16}	0.09[97]	0.72[97]	1.12[98]	13.6[99]	4.58[75]

Table 4.1 Parameters used in the simulation of potential distribution in standard CIGS solar cells

	Doping type	Thickness (nm)	Doping level (cm^{-3})	Electron effective mass (m_e/m_0)	Hole effective mass (m_h/m_0)	Band gap (eV)	Dielectric constant	Affinity (eV)
ZnO:Al	n	200	10^{20}	0.24[73]	0.59[73]	3.24[74]	7.8[73]	4.5[75]
ZnS(O,OH)	n	20	10^{17}	0.39[73, 100]	0.23[73, 100]	3.8[74, 100]	8.05[73, 100]	3.9[75, 100]
CIGS	p/n	2000	2×10^{16}	0.09[97]	0.72[97]	1.12[98]	13.6[99]	4.58[75]

Table 4.2 Parameters used in the simulation of potential distribution in ZnS(O,OH)/CIGS solar cells

	Doping type	Thickness (nm)	Doping level (cm^{-3})	Electron effective mass (m_e/m_0)	Hole effective mass (m_h/m_0)	Band gap (eV)	Dielectric constant	Affinity (eV)
ZnO:Al	n	200	10^{20}	0.24[73]	0.59[73]	3.24[74]	7.8[73]	4.5[75]
CdS	n	60	10^{17}	0.2[73]	0.8[76]	2.2[77]	8.9[78]	4.2[75]
CZTSe	p/n	2000	5×10^{16}	0.012[101]	0.182[101]	1.0[102]	10[103]	4.5[104]

Table 4.3 Parameters used in the simulation of potential distribution in standard CZTSe solar cells

4.4.1 Heterojunction

Figure 4.10 represents the potential, potential difference, electric field and electric field difference profiles for heterojunction of standard CIGS device. The maximum of the electric field under different V_b is in the location of the CIGS/CdS interface, which is also the p-n junction for heterojunction. However, after subtracting with $V_b = 0$ V electric field as in Figure 4.10(b), the maximum of the V_b-induced electric field is in CdS layer, and the electric field difference profiles show plateaus inside the CdS and CIGS. It means the applied bias V_b generate a uniform electric field in CdS layer. The electric field peak induced by surface potential in p-n junction is canceled out in V_b-induced electric field profiles. In experiment, because of the size of the tip and the limitation of the resolution, we cannot see the plateau inside CdS layer and the abrupt change in CIGS/CdS interface. The measured V_b-induced electric filed exhibits as a peak with the maximum inside the CdS layer.

Usually, the diameter of the tip used in the experiment is about 50nm~100nm, which is comparable to the thickness of CdS layer. We average the adjacent points for

V_b-induced electric field profile to simulate the effect of the tip radius. Figure 4.11 shows the adjacent-averaging smooth of the 1.5 V V_b-induced electric field profile of Figure 4.10(d). The distance between each data point is about 5nm. Figure 4.11 shows that the considering the tip radius, the simulated V_b-induced electric field peak can be either in CdS layer or in CdS/CIGS boundary. Thus, the simulation result is compatible with the experimental results. The depletion width in Figure 4.10(d) is wider than the experiment [Figure 4.5(c)]. The possible reason might be a very thin amorphous layer on the surface of the polished area caused by ion beam, so the tip cannot detect the small potential change in the deep depletion region.

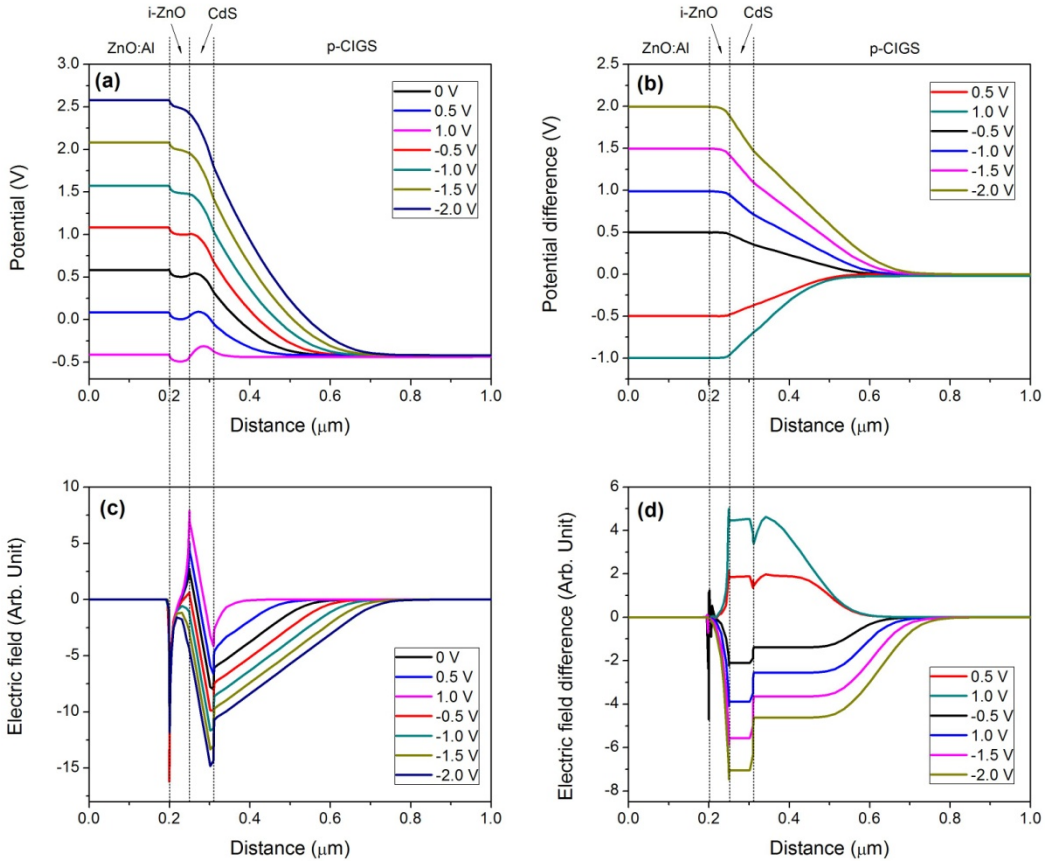

Figure 4.10 Simulated (a) potential, (b) potential difference, (c) electric field and (d) electric field difference profiles for heterojunction of standard CIGS device

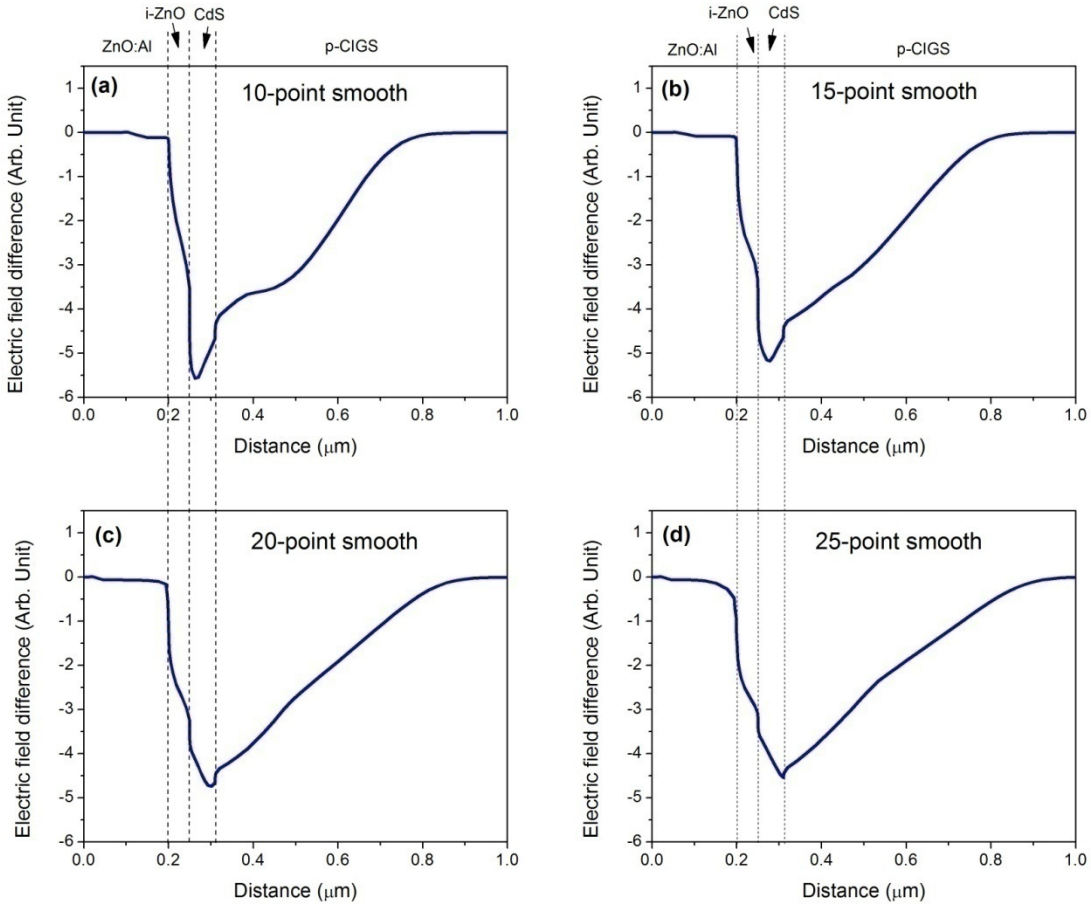

Figure 4.11 Adjacent-averaging smooth of the 1.5 V electric field difference profile for (a) 10-point smooth, (b) 15-point smooth, (c) 20-point smooth and (d) 25-point smooth

4.4.2 Homojunction

For buried homojunction, there is an n-CIGS/n-CZTSe layer beneath the CdS layer. Figure 4.12 shows the simulation for standard CIGS device with 30nm n-CIGS layer. The carrier concentration of n-CIGS is 2×10^{16} cm^{-3}. The simulated electric field peaks for difference bias voltage V_b are in p-n junction (n-CIGS/p-CIGS interface) in Figure 4.12(c) as expect. However, after subtracting by $V_b = 0$ V electric field, the electric

field peak in n-CIGS/p-CIGS cancel out and the V_b-induced electric field profiles show a plateau in CIGS layer. Figure 4.12(d) is similar with Figure 4.11(d). Thus, if the n-CIGS layer is thin, we cannot distinguish whether the junction is heterojunction or homojunction from the electric field difference profiles.

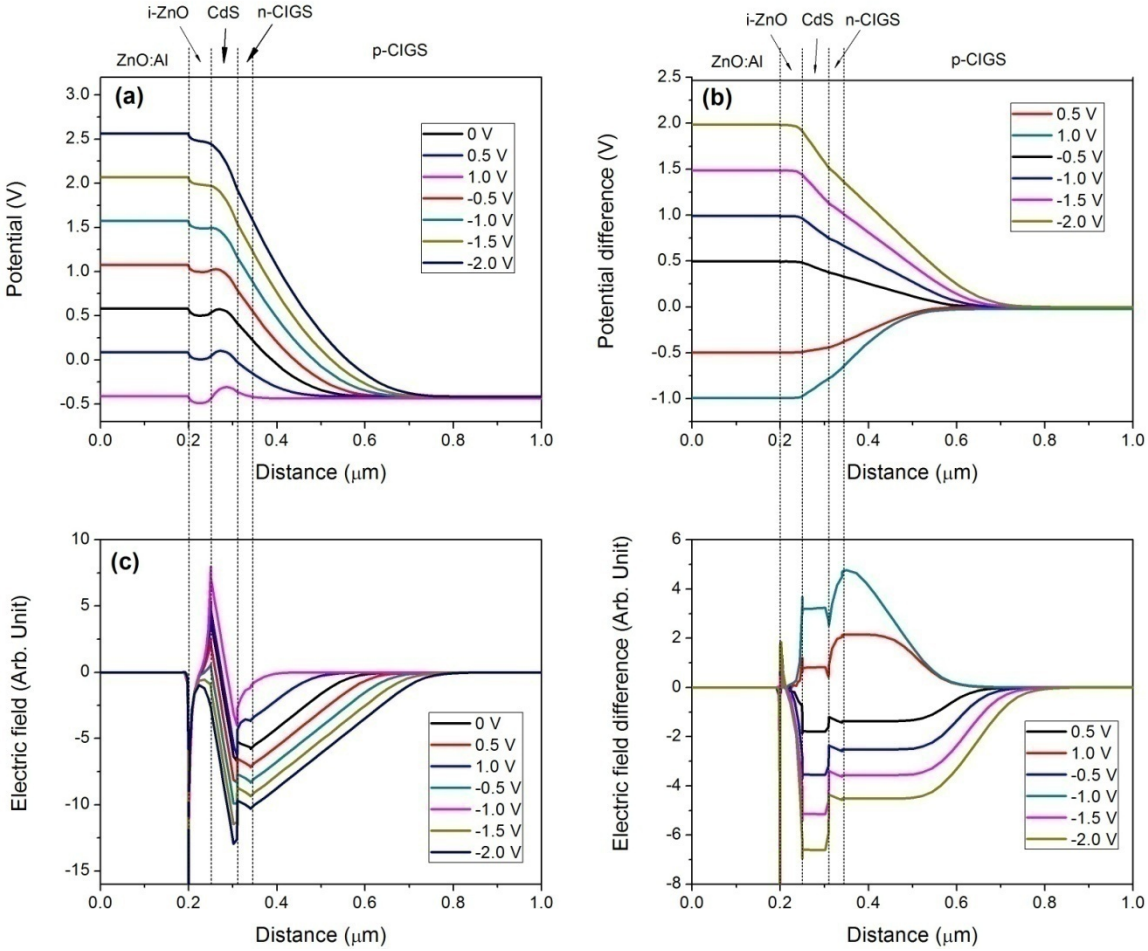

Figure 4.12 Simulated (a) potential, (b) potential difference, (c) electric field and (d) electric field difference profiles for homojunction of standard CIGS device with 30nm n-CIGS layer

Figure 4.13 is the simulation for standard CIGS device with 100nm n-CIGS. The

homojunction is 100nm beneath the CdS/CIGS interface. Figure 4.13(d) also shows that the electric field peak in the position of n-CIGS/p-CIGS cancel out when subtracted with the $V_b = 0\,V$ electric field, which is the same as the 30nm n-CIGS simulation in Figure 4.12(d). However, the maximum of the V_b-induced electric field is deep inside CIGS layer for the junction with 100nm n-CIGS. No experimental results on CIGS show this situation. Thus, the simulation demonstrates that there is no n-CIGS layer thicker than 100nm in the device. For ZnS(O,OH)/CIGS and CZTSe devices, the simulation results are similar. If the n-CIGS/n-CZTSe layer is thicker than a threshold, the maximum of the electric field difference is deep inside CIGS/CZTSe.

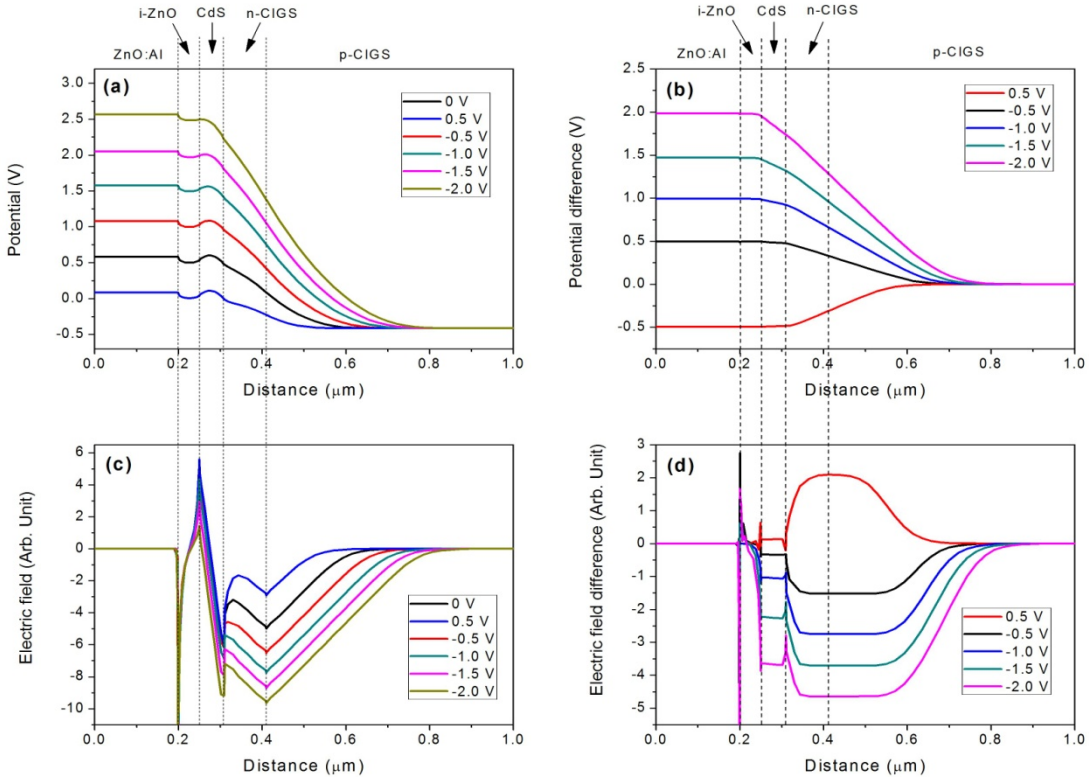

Figure 4.13 Simulated (a) potential, (b) potential difference, (c) electric field and (d) electric field difference profiles for homojunction of standard CIGS device with 100nm n-CIGS layer

Further simulation shows that the position of the electric field difference peak also depends on the carrier concentration of n-CIGS. Because the carrier concentration and the thickness of the n-CIGS/n-CZTSe are unknown, we plotted the electric field difference peak position with the change of the n-CIGS/n-CZTSe thickness under different carrier concentrations. Fig. 6 (a), (b) and (c) are the results of the peak position for standard CIGS, ZnS(O,OH)/CIGS and standard CZTSe device, respectively. The light blue area indicates the range of the experimental results. The 0 thickness of the x-axis indicates the heterojuction. All the three graphs in Fig. 6 illustrate that with the increase of the thickness of n-CIGS/n-CZTSe, the V_b-induced electric field peak position moves from buffer layer side to CIGS/CZTSe side. If the carrier concentration in n-CIGS/n-CZTSe is high, the electric field difference peak is inside the buffer layer only in the case that n-CIGS/n-CZTSe layer is very thin (within several tens of nanometers). If the carrier concentration in n-CIGS/n-CZTSe is very low, the electric field difference peak will be inside the buffer layer for a large range of n-CIGS/n-CZTSe thickness. Therefore, although we cannot distinguish heterojunction and homojunction from the SKPFM results, we can narrow the possible range and combination of the n-CIGS/n-CZTSe thickness and carrier concentration. Further investigation with other methods (such as scanning capacitance spectroscopy) is needed to identify the junction location

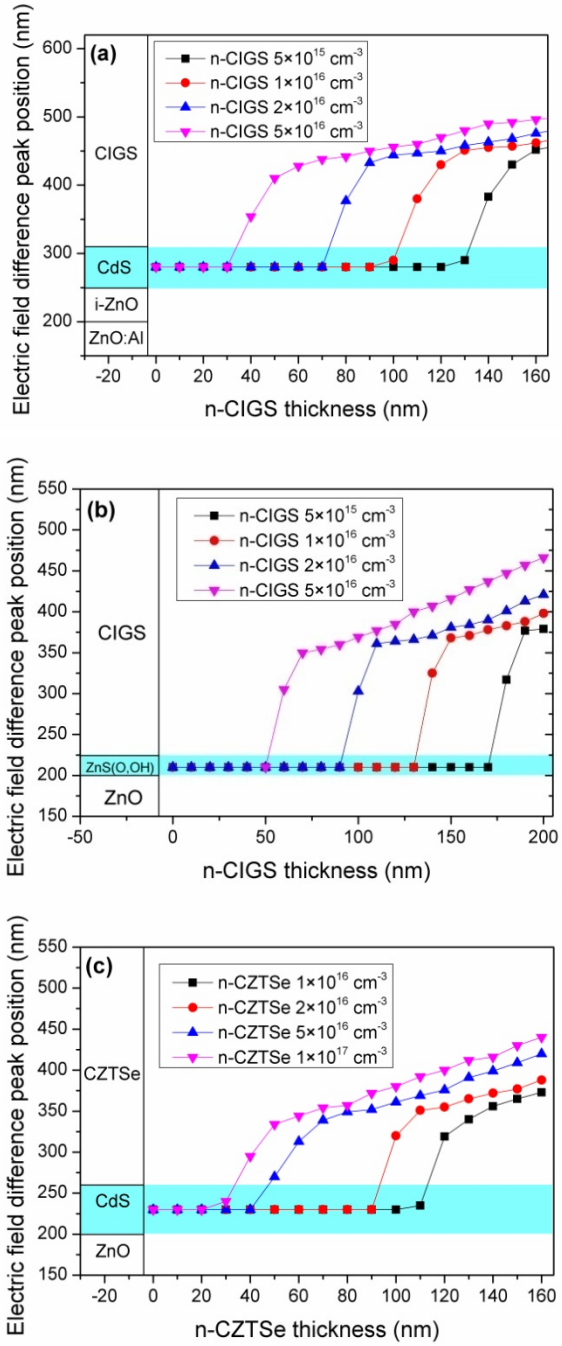

Figure 4.14 The peak position of the V_b-induced electric field difference with the change of the n-CIGS/n-CZTSe thickness under different carrier concentration in (a) standard CIGS, (b) ZnS(O,OH)/CIGS and (c) standard CZTSe devices.

4.5 Conclusion

We have measured the potential and the V_b-induced electric field using SKPFM in cross-section of standard CIGS, ZnS(O,OH)/CIGS and the standard CZTSe devices. The V_b-induced electric field peaks for all the three devices are inside buffer layer and close to the metallurgical junction. Both the situations of heterojunction and homojunction are simulated using the PC1D software. The simulation results for heterojunction and homojunction with thin n-CIGS/n-CZTSe layer are compatible with the experimental results, but we cannot distinguish whether the device is heterojunction or homojunction. If the thickness of n-CIGS/n-CZTSe layer is larger than a threshold, the maximum of the electric field difference profile will be deep inside CIGS/CZTSe layer, which is different from the experimental results. To further study the junction of the CIGS/CZTSe device, the electric field difference peak position with the change of the n-CIGS/n-CZTSe thickness and carrier concentration is calculated. The result provides the possible ranges of the n-CIGS/n-CZTSe thickness and carrier concentration.

Appendix A

Lateral Walker Design of Cross-sectional Scanning Tunneling Microscopy

The scanning tunneling microscopy (STM) was invented by G. Binnig, H. Rohrer, C. Gerber and E. Weibel in 1981 [105, 106]. It has been a powerful technique to explore the electrical properties of semiconductors, metals and superconductors.

The principle of the STM is the electron tunneling through finite potential barrier. Figure A.1 is the schematic of the STM. Usually it is operated in ultra high vacuum. There is no contact between tip and sample. Assume the tip and sample are the same material and the bias voltage between tip and sample is small. In classical theory, the electron is blocked and cannot travel through the vacuum if the potential of the electron is less than the vacuum potential barrier. However, from quantum mechanics, there is possibility for electron to tunnel through the potential barrier, and the tunneling current is

$$I \sim e^{-2\kappa z} \tag{A.1}$$

where z is the distance between tip and sample, and κ is the effective decay constant

$$\kappa = \sqrt{\frac{2m(V_B - E_F)}{\hbar^2}} \tag{A. 2}$$

where V_B is the vacuum barrier, and E_F is the Fermi level of tip and sample

Since the tunneling current is very sensitive with the distance between tip and sample, STM has very high depth resolution (~0.01nm). The lateral resolution is as high as 0.1nm, which is in the order of the atom size. Therefore, the arrays of the atoms on clean surface

can be identified in STM image, and the STM tip can be used to manipulate individual atoms.

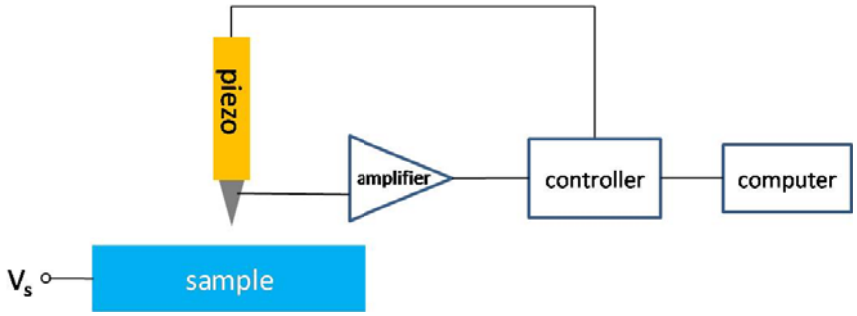

Figure A.1 Schematic of STM

Figure A.2 are the picture, side view and top view schematic of the Pan-type STM head, respectively [107, 108]. The piezo scanner with tip is mounted inside a sapphire prism. There are six shear piezo stacks fixed on Macor body to hold the sapphire prism. Each piezo stack is made by gluing four piezo plates with conducting expoxy, and the top of the piezo stack is glued with polished alumina pad. The stainless steel spring plate is used for applying an adjustable force for piezo stacks on prism.

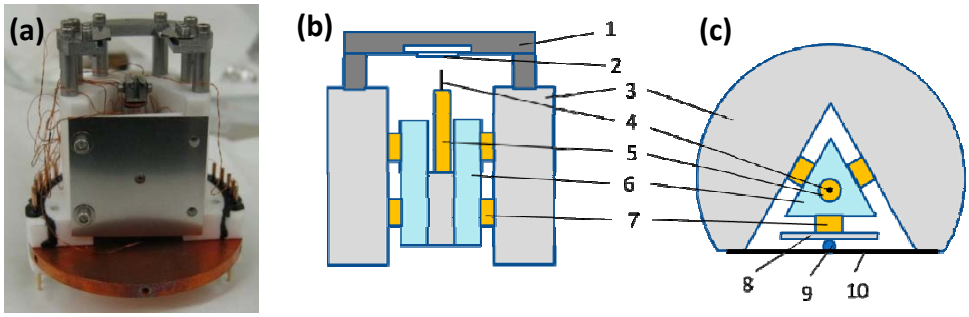

Figure A.2 (a) Picture of STM [109], (b) side view and (c) top view diagram of STM. (1) sample stage, (2) sample holder, (3) macor body, (4) tip, (5) piezo scanner, (6) prism, (7) piezo stack walker, (8) macor plate, (9) ruby ball, (10) stainless steel spring plate

Figure A.3 illustrates the principle of the coarse approach of the tip towards sample [110]. A sequence of voltages is applied to the six piezo stacks. When the voltage is applied on the first piezo stack, there is a shear motion of the piezo. However, because the total friction of the rest five piezo stacks is larger than the sliding friction of the first piezo stack, the sapphire prism will not move. Similarly, the prism stays in its original position until all the six piezo stacks are applied with the voltages. At the end, the voltages on all of the six piezo stacks drop simultaneously, which makes the piezo stacks move at the same time and drive the prism to move by one step with the distance *h*. This process is repeated to drive the prism to coarsely approach the sample. Then the piezo scanner tube is used for delicate approach. This process of the coarse approach is very reliable and rigid which is much desired for STM design.

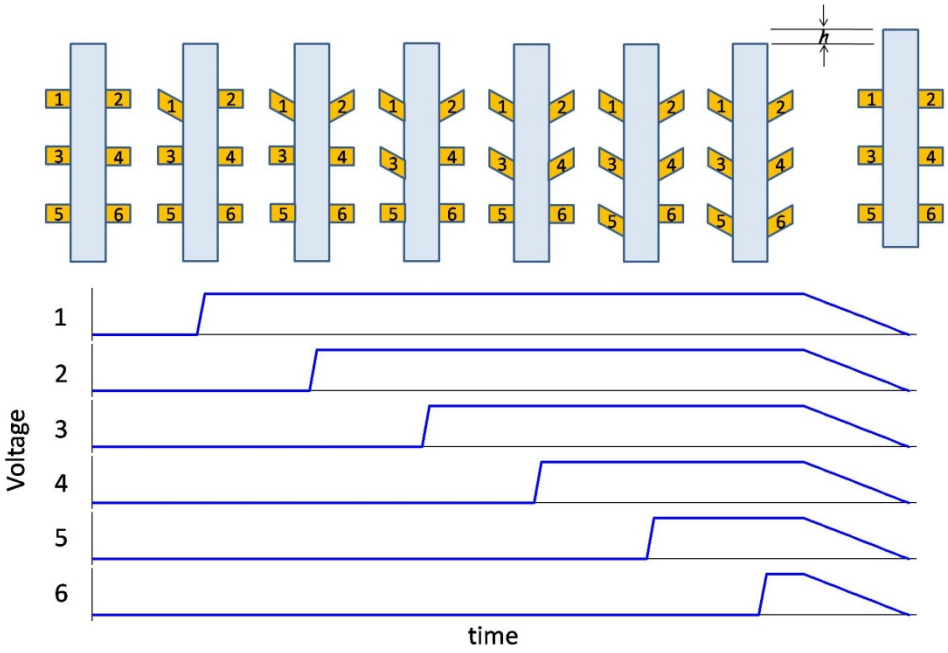

Figure A.3 Schematic of tip walker design. On top is the sequence of the shear piezo stacks to move the prism by one step. On bottom is the corresponding voltage applied on shear piezo stacks 1 to 6, respectively. The tip moves for a height of h in each circle.

For the delicate approach, the controller applies voltage on the piezo scanner tube to stretches it. If the tip detects the tunneling current, the STM will begin to scan. If there is no tunneling current even if the piezo scanner tube stretches to its maximum length, the controller will drive the piezo walkers to move the prism up for one step, and stretch the piezo scanner tube again to detect the tunneling current. This process will repeat until the tip detects the tunneling current. The maximum stretch of the scanner tube is set to be larger than the movement of the prism for each step.

The structure of the STM head in Figure A.2 is very rigid, which can keep the entire STM head stable and lower the noise level while scanning. However, the sample can only move along one direction, and the sample position cannot be controlled precisely outside chamber using the wobble stick. This structure of the STM head cannot be used to scan the cross-section of the sample, the width of which is usually less than 1mm. Also, sometimes the scan area is on the epitaxial layer with only several micrometers thickness on the cross-section of the sample. Thus, a cross-sectional STM (XSTM) head which the sample stage can be controlled within 100nm is desired.

Figure A.4 is the structure of the home-built XSTM. The tip approach part is identical with Figure A.3. For the upper part, the XSTM head consists of the top spring plate, three ruby balls, upper plate with three piezo stacks, sample stage, lower part with three piezo stacks, and three sticks. The sample stage is glued with three sapphire disks, and is sandwiched between six piezo stacks. The piezo stacks drive the sample stage to move laterally. The top spring plate and three ruby balls apply the vertical force to the upper plate, while make it fixed horizontally, so the sample stage will not rotate while moving. The range of the movement of sample stage is about 5mm×10mm.

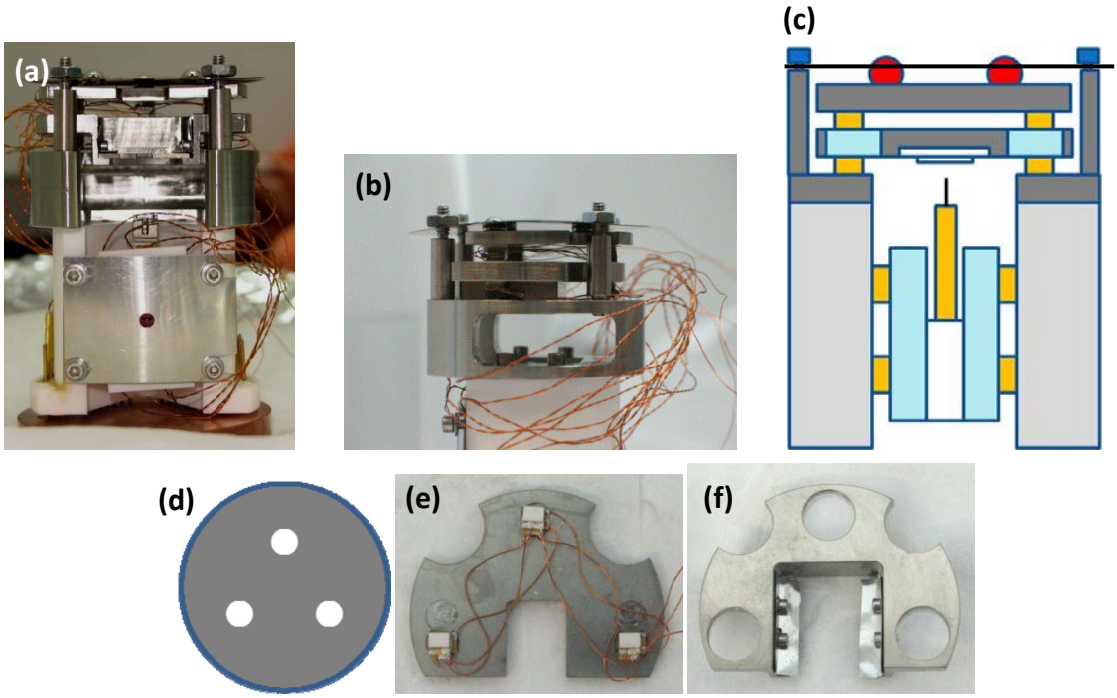

Figure A.4 The picture of (a) front view and (b) side view of XSTM. (c) the schematic of XSTM. The top view of (d) the spring plate, (e) the upper plate with shear piezo stacks, and (f) the sample stage

The process for moving the sample stage horizontally by the piezo stacks is different from the vertical movement of the tip. Instead applying voltage sequentially to each piezo stack, the same voltage as Figure A.5 is applied on all the six lateral piezo stacks simultaneously. The schematic of the movement of sample stage driven by lateral piezo stack walkers is shown in Figure A.6. The voltage applied on piezo stackes increases slowly in the interval t_1 as shown in Figure A.5. The shear motions of all the piezo stacks drive the sample stage moves to left side a bit [see Figure A.6 (b)]. In the interval t_2, the voltage drops quickly, so all the piezo stacks move back. Because of the inertia and the small sliding friction between the polished alumina and sapphire disk, the sample stage keeps moving for a distance [see Figure A.6 (c)]. Therefore, after one period of the voltage, the sample stage moves horizontally for one step. The distance the sample stage

can move for each step is determined by the force applied by the top spring plate, the temperature, and the pressure in vacuum chamber. The lateral walker of the XSTM was tested in air. The movement of the sample stage for each step of the piezo stack a is 30nm~100nm, depending the force between piezo and sapphire. In vacuum, because of the lack of the atoms in air as the lubricant between piezo and sapphire, the sample stage moves slower. In low temperature, the shear motion of the piezo is much smaller, so the sample stage also moves slower. The range of the movement of the sample stage is about 5mm×10mm, which is adequate for XSTM.

Because the XSTM head is larger and more complicated, it is not as rigid as the STM showed in Figure A.2(a). The noise level of XSTM is higher and the resolution is lower. The XSTM controls the sample laterally with the sacrifice of the high resolution. Thus, if it is not necessary to move the sample horizontally, the conventional STM can get images with better quality.

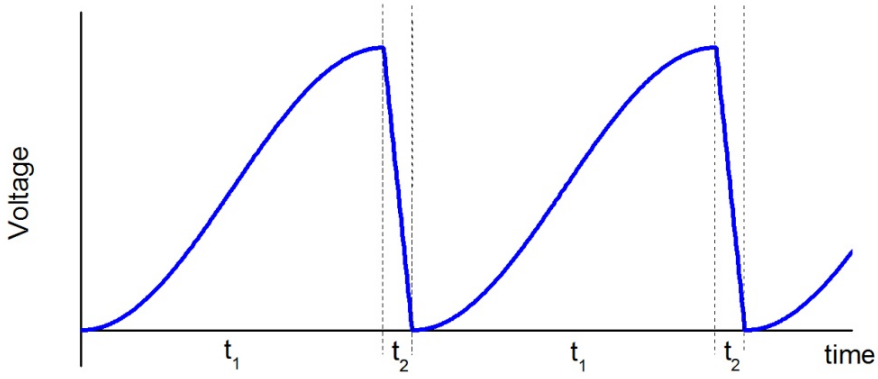

Figure A.5 Voltage applied on the six lateral shear piezo stacks of XSTM

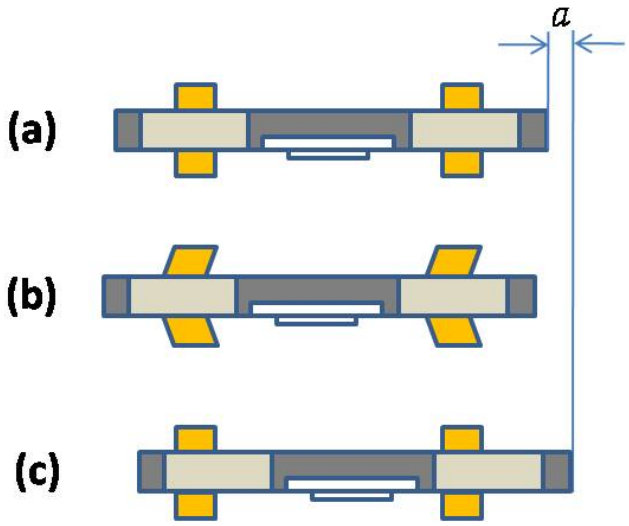

Figure A.6 Schematic of the lateral walker and sample stage at (a) the beginning of t_1, (b) the end of t_1, and (c) the end of t_2. The sample stage moves for a distance a in each circle.

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