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Multistate spin-transfer-torque random access memory

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Multistate spin-transfer-torque random access memory

by

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Report

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Dedication

This report is dedicated to family. For their endless love, support and encouragement.

Acknowledgements

This project would not have been possible without the kind support and help of many individuals and organizations. I would like to extend my sincere thanks to all of them.

Firstly, I would like to express my sincere gratitude to my supervisor Prof. Banerjee for the continuous support of my Master study and related research, for his patience, motivation, and immense knowledge. His guidance helped me in all the time of research.

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My thanks and appreciations also go to my friend, Tanmoy Pramanik, who worked along in every step of this project and in developing the project report. I wish best of the best for him in future.

Most importantly, none of this would have been possible without the love and patience of my family and my uncle Mohsen Mosleh. They have been a constant source of love, concern, support and strength all these years.

I hope my efforts will be helpful for the group in future and wish the best for Prof. Banerjee and every member in our group.

Abstract

Multistate spin-transfer-torque random access memory

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The University of Texas at Austin, 2016

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Spin-transfer-torque random access memory (STT-RAM) is an emerging non-volatile memory technology that stores information as the relative alignment of two ferromagnets in a magnetic tunnel junction stack. Due to high scalability, speed and endurance STT-RAM is being considered as a promising candidate for future universal memory. To improve storage density various multi-state configurations have been proposed for STT-RAM. Previously, using micromagnetic simulations, it was shown that shape anisotropy of a cross-shaped ferromagnet can be used to achieve multi-state operation in a STT-RAM bit. In this work, we attempt to demonstrate the multi-state operation of such cross-shaped ferromagnet experimentally. We have explored different approach to fabricate cross-shaped magnetic tunnel junctions. Using magnetic force microscopy we demonstrate equilibrium magnetization states of a patterned cross-shaped ferromagnet. Challenges and future perspectives have been discussed.

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INTRODUCTION

In 1988, Grünberg and Fert's group discovered and showed that the electrical resistance of a magnetic multilayer depends on the magnetic orientation of magnetic layers relative to each other[1], [2]. This discovery, which was called Giant magneto resistance (GMR), introduced a way to sense and determine the state of magnets in a magnetic multilayer stack by measuring the overall resistance when an electrical current is flown through the stack. The effect opened ways to integrate magnetic materials and their properties in electronic devices. The simplest structure, which can be used to demonstrate GMR effect, is called spin-valve, which consists of two ferromagnetic (FM) layers separated by a thin non-magnetic spacer layer (figure 1). When a voltage is applied across the magnetic structure, there will be a flow of electrons, which carry both electric charge and magnetic moment, spin, from one magnetic electrode to the other one.

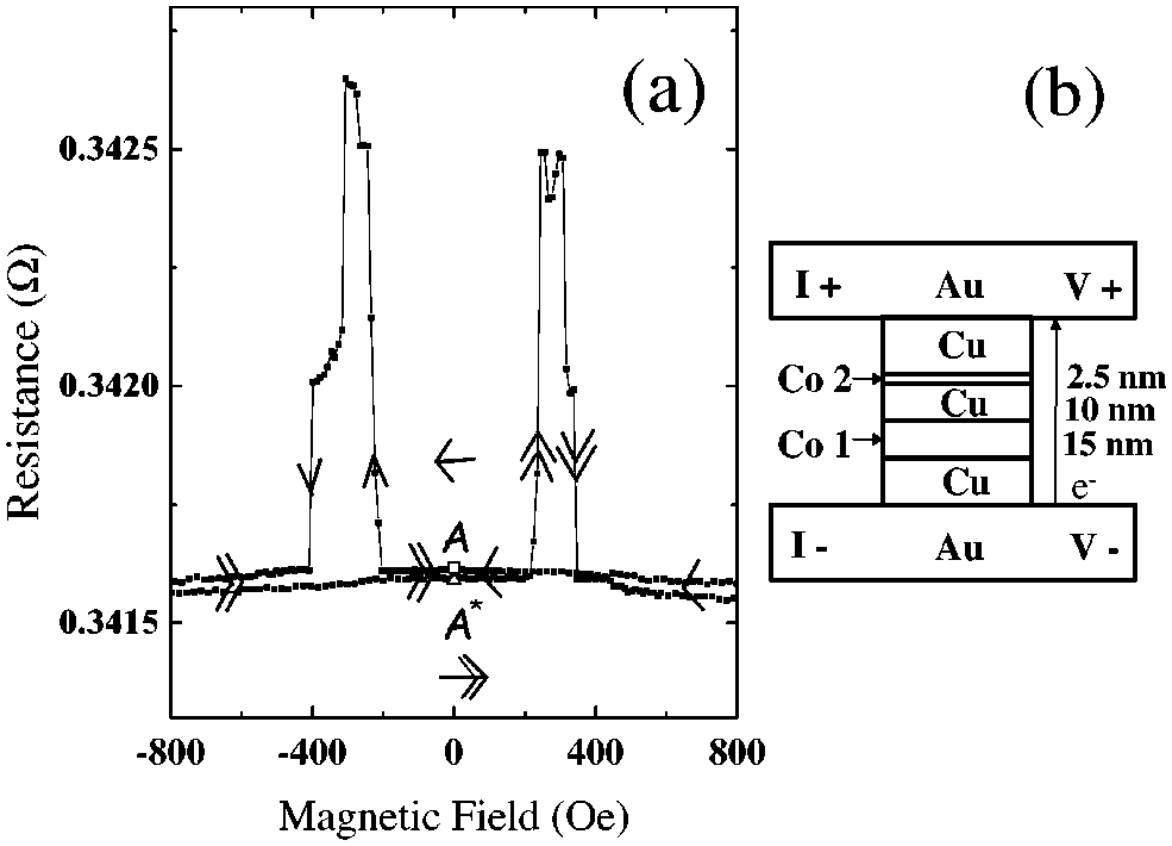

Figure 1 Giant magnetoresistance (left) of a current perpendicular to place spin valve (on right).Taken from [3]

When these electrons pass through the first ferromagnetic electrodes, their spins are polarized by the background ferromagnetic moments which causes majority of carriers having spins parallel to the magnetic moment of the first electrode. These spin polarized electrons experience different resistivity in the second ferromagnet due to spin scattering, depending on the alignment between the magnetic moment of the electrode and the polarization of electrons. In the case where they are aligned and parallel to each other, the spin scattering and hence the resistivity will be low and when they are in opposite directions, the resistivity will be high due to higher amount of scattering and loss of energy. Giant magnetoresistance is defined as the relative resistivity

difference between the parallel and anti-parallel state. If the parallel state resistance is given as RP and anti-parallel state resistance is given by RAP, then the MR is estimated as:

$$MR = \frac{R_{AP} - R_P}{R_P} \, x \, 100\%$$

GMR values in a typical spin valve can be much higher than magnetoresistance due to Lorenz force or anisotropic magnetoresistance (AMR) due to anisotropy effects. Spin valves are being used in the read head of hard disc to extract the state of each cell in the magnetic memory the bit of data associated with it.

The choice of the non-ferromagnetic spacer is determinant to the strength of GMR effect. When a thin layer of insulator is used as the spacer, the effect is called tunneling magnetoresistance (TMR) which heavily depends on the lattice and band structure of the tunneling barrier and the adjacent ferromagnetic layers (Figure 2). These magnetic multi-layers with a thin insulating tunnel barrier sandwiched between two ferromagnetic layers are called magnetic tunnel junctions (MTJ). In 1975, Julliere showed 14% TMR effect at 4.2K for the first time in a Fe/Ge-O/Co stack[4], [5]. This was followed by another remarkable discovery by Moodera et. al. with more than 10% TMR at room temperature with Al2O3 tunnel barrier[6]. Extensive researches were conducted to find the best materials and structures for these magnetic tunnel junctions (MTJ) to improve the TMR value. Using first principle calculations, Butler et. al. predicted possibility of achieving very high TMR in lattice matched Fe/MgO/Fe MTJ due to spin filtering effects [7]. In 2008, TMR ratios over 1000% at 5K and over 600% at 300K were achieved with a crystalline MgO tunneling barrier [8]. (May mention AlOx as another option.) These discoveries soon replaced the GMR read heads by TMR read heads due to higher resistance change and ease of sensing.

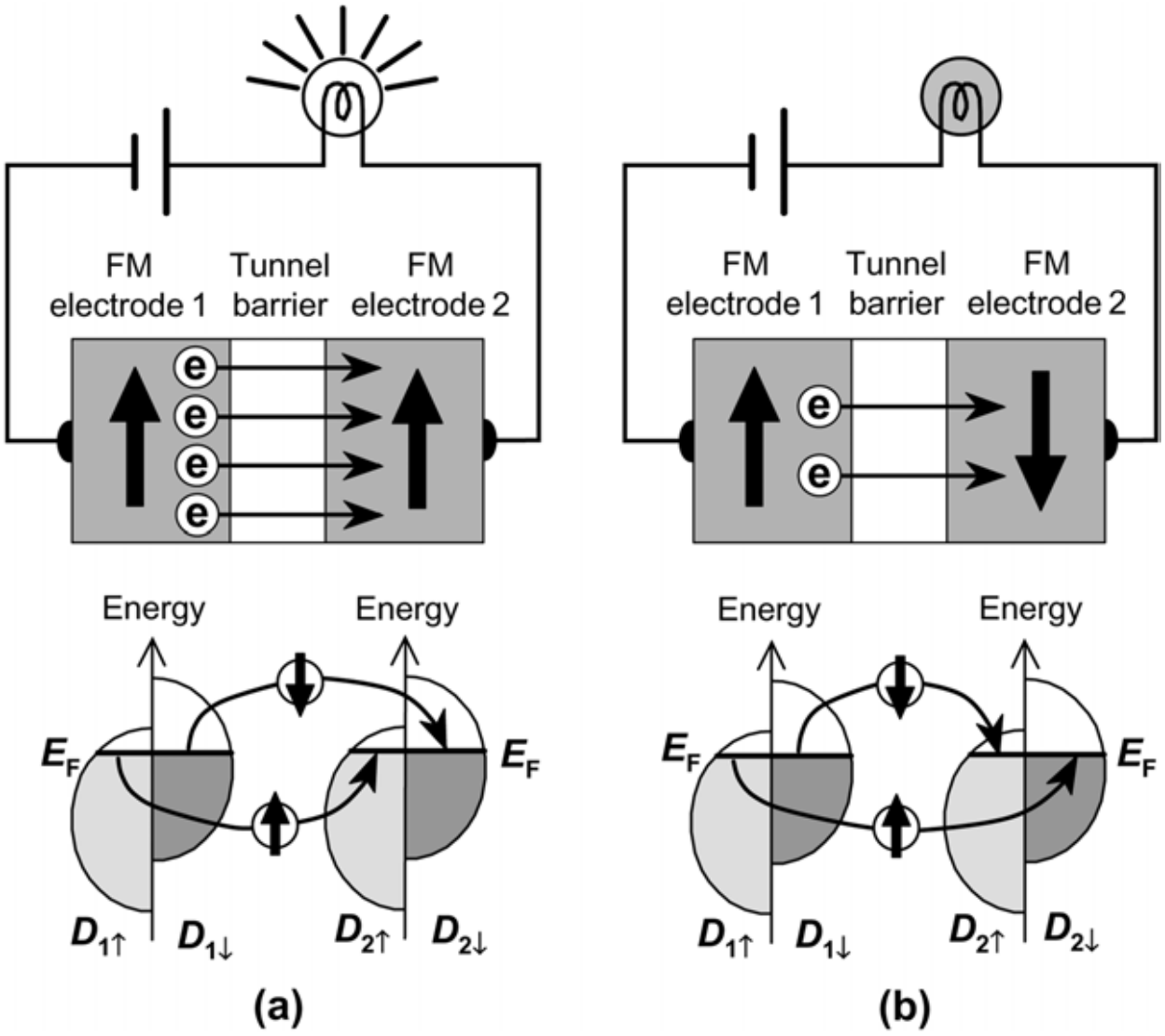

Figure 2 Simple illustration of the tunnel magnetoresistance effect (a) Two ferromagnetic electrodes are parallel resulting in a low resistance path (b) Anti-parallel alignment of the two ferromagnets[9].

Julliere proposed a simple relation between the spin polarization of the ferromagnetic electrodes and the tunnel magnetoresistance given as:

$$TMR = \frac{2P_1P_2}{1 - P_1P_2}$$

Where P1 and P2 are the spin polarization of the electrodes. For any other orientation between the two ferromagnets the resistance of the TMR stack is calculated as:

$$R(\theta) = \frac{R_P + R_{AP}}{2} * (1 + \frac{R_P - R_{AP}}{2} cos\theta)$$

Spin –transfer-torque switching :In 1996 Slonczewski's study on magnetic multilayers showed that by flowing a spin-polarized current into a ferromagnetic layer can change the magnetic state of the ferromagnet[10]. When a spin polarized current enters a magnetic material with the magnetic moment non-collinear with the spin polarization of the incoming electrons, the magnetic moments apply a torque to the electrons and tries to make their spin aligned with the magnetic moments of the ferromagnet. Vice versa, the current or the electrons apply a force in the opposite direction which is known as spin-transfertorque(STT). Or in another word, the spin-polarized current carries a non-zero spin current and exchanges some of its angular momentum with the magnetic materials. This angular momentum exchange is called spin torque transfer and can cause the magnetic moment of the ferromagnet to precess around its equilibrium direction or even flip toward the opposite direction if the STT is strong enough to overcome the energy barrier and damping mechanics that are caused by magnetic anisotropies such as shape or crystalline anisotropy. In ferromagnets with multiple magnetic domains, such spin torque can move the domain walls[11].

This effect can be used in magnetic memories to switch the magnet that holds the data only by applying a spin polarized current and without the need of a magnetic field. Therefore, it is possible to fully integrate magnetic memory device in current solid-state device fabrication and read and write data from and onto the magnetic cell only by applying an electric current. The read operation depends on the TMR effect discussed in the last section and the write operation depends on the STT effect.

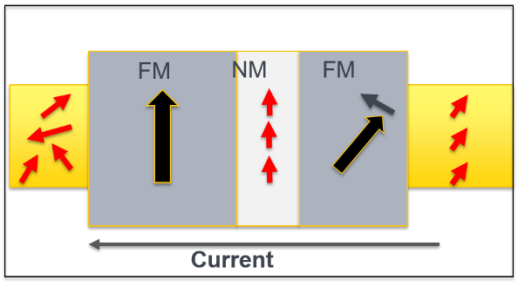

Figure 3: Simple illustration of the STT effect.

As described in the previous section, a spin-valve (MTJ) consists of 2 ferromagnetic materials separated by a non-ferromagnetic spacer (insulator) can used as a memory cell in this context. In a spin-transfer-torque random-access-memory (STT-RAM) a MTJ is used as the storage element. One of the ferromagnet is usually made harder to switch, by exchange biasing with an adjacent anti-ferromagnet, and thus called a fixed layer. The magnetization of the other ferromagnet, which is called free layer, can be altered by applying a spin-polarized current though the stack. When a voltage bias is applied on the structure, a flow of electrons is created from one ferromagnet to the other. This current is spin filtered and spin-polarized by the fixed FM (Figure 3). Assuming that the spacer layer is properly chosen and thin enough, the current retains its spin polarization aligned with the fixed FM after passing the spacer and inject spin current and angular momentum parallel to the fixed layer into the free layer. In a case where magnets start in antiparallel states, if the current is strong enough to overcome the damping of the easy axis of the free FM, the free FM flips by the polarized current and becomes aligned with the fixed FM. Reversing the bias and current, i.e. flowing electron current from the free layer towards the fixed layer applies a spin transfer torque in the opposite direction of the magnetic moment of the fixed layer onto the free layer which can cause the free layer to flip and become antiparallel to the fixed layer.

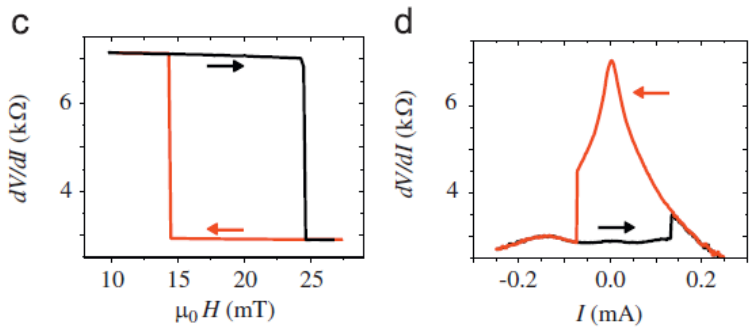

Figure 4 Magnetic field and STT induced switching of an MTJ nano-pillar. Taken from[12]

The strength of spin torque depends on the current density (J), spin polarization factor (η) and the angle between the spin polarized current and the magnetization of the free layer (θ). The torque could be written as[12]:

$$\dot{M}_{st} = \frac{\eta(\theta)\mu_B I}{qV}\, \widehat{M} \times (\widehat{M} \times \widehat{M}_{fixed})$$

Where, I is the spin polarized current, V is the free layer volume, M (Mfixed) is the free layer (fixed layer) moment. η captures the details of the layer structure. This torque term can be added to the Landau-Lifshitz-Gilbert equation to account for the STT effect and the magnetization dynamics can be calculated.

Assuming a macro-spin i.e. mono-domain switching for small patterned magnets, the minimum charge current i.e. the critical current required for STT-induced switching was calculated by Sun as[13], [14]:

$$J_{c0} = \frac{2e\alpha M_s t_F (H_K + 2\pi M_s)}{\hbar\eta}$$

Where, e is the electronic charge, α is the damping constant, M_s is the saturation magnetization, η is he spin-torque-efficiency factor of the current, H_K is the effective uniaxial anisotropy of the

free. H_K is decided by the magneto-crystalline or shape anisotropy, which controls the thermal stability for the memory bit. The main challenge that needs to be overcome in STT-RAM is to reduce this critical current while maintaining thermal stability in order to compete with other conventional and emerging memory technologies. Currently for a typical STT memory cell with dimensions ~100 nm, the critical current for STT switching is in the order of 10^6 -10^7 A/cm^2. With current CMOS technology, a transistor that supplies such a huge current needs to as large ~500 um^2 which will occupy a large area of the memory cell and hence limits the scaling of the memory cell and reduces packing density.

There are different approaches to decrease this critical current to maximize packing density while maintaining thermal stability of STT-RAMs. Some of them will be discussed here briefly.

The first and the most straight-forward way is to improve the spin polarization efficiency through magnetic stack engineering[12]. In early STT-RAM prototypes, a metallic or Al_2O_3 layer were being used as the spacer which caused the device to require large amount of current to switch due to low spin polarization efficiency in the spin-valve. Introduction of MgO based STT cells improve polarization from below 50% to more than 60%, which significantly reduced the switching current, increased the TMR of these devices. However, increasing polarization has diminishing return when it comes to reducing the critical switching current. As shown in [15] an increase in the polarization from 66% to 100% will only reduce the current by only 8%. Another approach is to use dual MgO barrier based MTJs, where the free layers can be excited by STT from two fixed layers, so that the effective switching current is reduced[16].

A better approach is to use perpendicular magnetic anisotropy (PMA) materials which provides a better trade of between switching current and thermal stability compared to the in-plane magnetic tunnel junctions[17]. But PMA materials may suffer from low TMR ratios.

A typical STT-RAM cell has one MTJ along with 1 drive transistor (Figure 5). As discussed before the cell size is limited by the transistor area, which is decided by the drive current requirement.

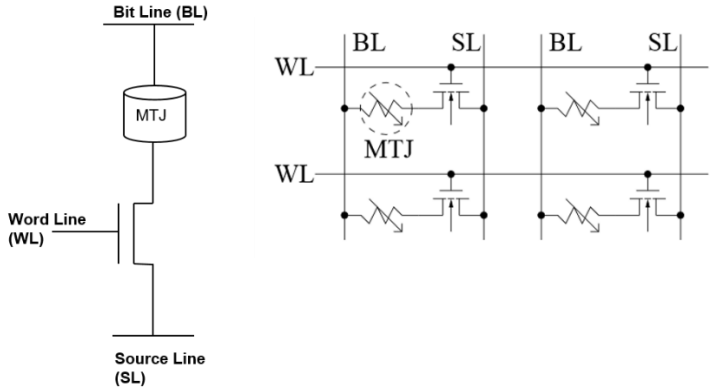

Figure 5 STT memory cells along with one driving transistors

So, storing more than one bit in a single MTJ could potentially increase the storage density in STT-RAM. Different approaches have been proposed for multi-bit operation of STT-RAM. Two MTJs with different critical switching current could be series stacked (Figure 6) to get 4 states and store 2 bits[18], [19].

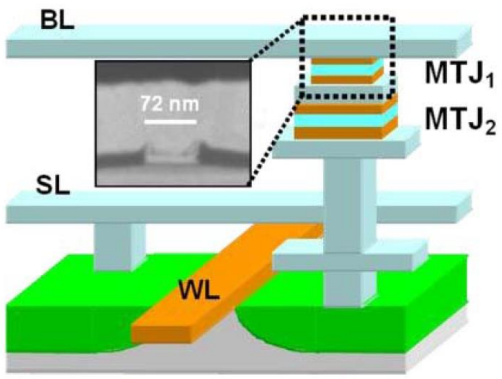

Figure 6 2bit/cell STT-RAM with series stacked MTJs. Taken from [18]

Another proposal was to prepare the free layer with two different domains inside it, so that the domains switch as different current density, giving rise to a multi-state operation[19]. Multi-state

operation can also be achieved by patterning the free layer FM in non-trivial shapes such as a cross-shaped ferromagnet[20].

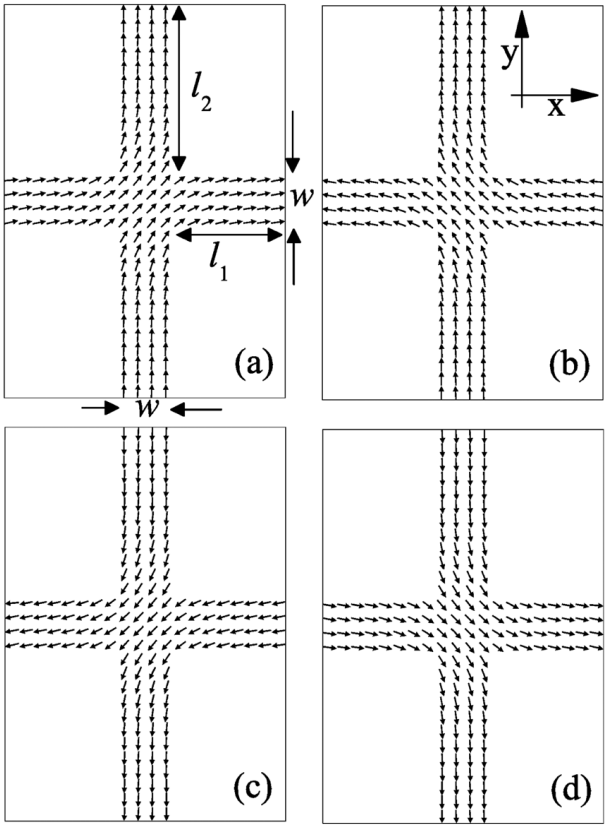

Figure 7 4 equilibrium magnetization states of a cross-shaped FM. Figure taken from [20]. Following [20], w = 20nm, l1=40nm, l2=60nm.

MULTI-STATE STT-RAM BIT WITH CROSS-SHAPED FERROMAGNET:

As shown in [20], a cross-shaped ferromagnet can have 4 different equilibrium magnetization states. When put into a magnetic tunnel junction with the fixed layer aligned suitably, the 4 equilibrium states (Figure 7) can result in different resistance of the stack. So this could be used as 2-bit memory. To switch the cross-shaped multi-state memory, varying level of current density could be used as discussed in detail in [20]. The cross-shaped multi-state STT-RAM cells

could be integrated on to a vertical drive transistor and can be arranged into a crossbar memory array for maximum packing density. Here we report experimental results on the cross-shaped FMs and magnetic tunnel junctions.

EXPERIMENTAL RESULTS:

In general, in order to observe and study STT switching, the active area of the device is required to be in the order of ~100 nm for two different reasons. First, for a typical magnetic spin-valve structure, the area of the magnets needs to be less than 250 nm so that the spin torque transfer becomes dominant over the Oersted's magnetic field caused by flowing current into the junction[12].

Secondly, for such small devices, it's safe to assume that there will be only few and ideally one magnetic domain per magnet (or branch in the case of cross shaped magnet). Therefore, the entire magnet (or in the case of cross shaped magnets, an entire branch) switches coherently as a mono-domain.

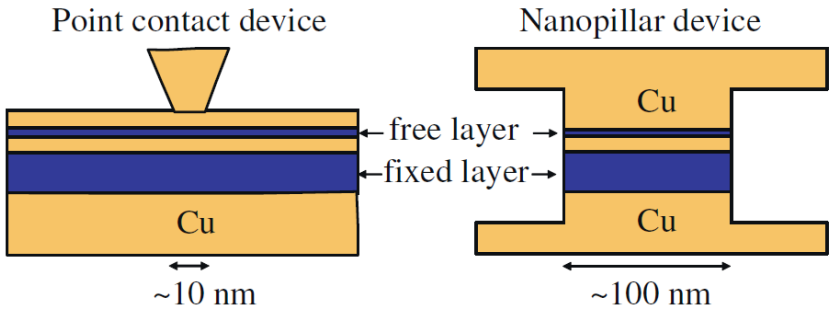

Figure 8 Two approached for STT-switching study: (Left) Point contact measurement (Right) Nano-pillar. Taken from [12]

Two major approaches are used to study STT switching in magnetic stacks. One is to inject an electric current to a tiny area of a magnetic stack using a sharp needle, which makes contact onto

one side of the magnetic stack (Figure 8). This method is called point contact measurements and doesn't require patterning the magnetic stack.

In the other approach, the magnetic multilayer is first patterned using E-Beam lithography and then, electrical contacts are made to the top and bottom of the isolated magnetic nano-pillar. In most cases, a patterned STT device requires less electric current to switch compared the point contact measurement approach with the same active area size, because the active area in the latter is coupled to the rest of the magnetic multilayer. However, there are many obstacles and fabrication difficulties are involved in patterning and making contact to such a small area with low resistive-area (RA) product, which is yet to be fully solved. For example, patterned devices suffer from sidewall leakage and are less stable than devices in the first approach. These challenges will be discussed later.

In order to study STT-RAMs with cross-shaped magnets, we have to use the second approach and fabricate a patterned nano-pillar device. Generally, two different types of lithography can be used to fabricate STT memory cells: (1) Stencil lithography and (2) Ion-milling (nano-sculpting).

(1) Stencil lithography

Stencil lithography is a bottom up fabrication process where a shadow mask is used to select certain area of the substrate for further fabrication processes such as etching and deposition [21], [22].

To fabricate magnetic cells using this method, we need to create shadow mask with openings in the order of 100nm close enough to the substrate to avoid shadowing effect during deposition of the magnetic multilayer.

First step of this process is to sputter deposit a thick layer of TaN (500 nm)/Ta (50nm) multilayer on a thermally oxidized silicon wafer. This layer serves as the bottom contact of the

devices as well as the seed layer for the magnetic stack that will be deposited later on. Then, 100 nm silicon oxide followed by 20 nm of Ta is deposited everywhere using e-beam evaporation and plasma sputtering respectively. This second Ta layer will be used as the shadow mask as well as the top contact. The SiO_2 layer isolates the top and bottom contact from each other.

Next, using e-beam lithography followed by 1 minute of CF_4 reactive plasma etching, holes/openings in the order of ~100 nm are created in the top Ta layer. These holes are of the same size and shape as the final nano-pillar devices. In the next step, the SiO_2 layer is removed in the vicinity of the initial hole (in the Ta layer) using a wet etch step with BOE (15 sec). Figure 9,10 and 11 show the Focused Ion Beam (FIB) cross section images of the holes.

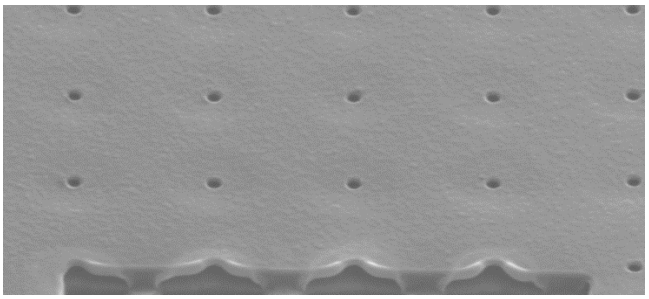

Figure 9 Stencil mask process: FIB cross-section image of array of 100 nm diameter holes etched into Ta/SiO2.

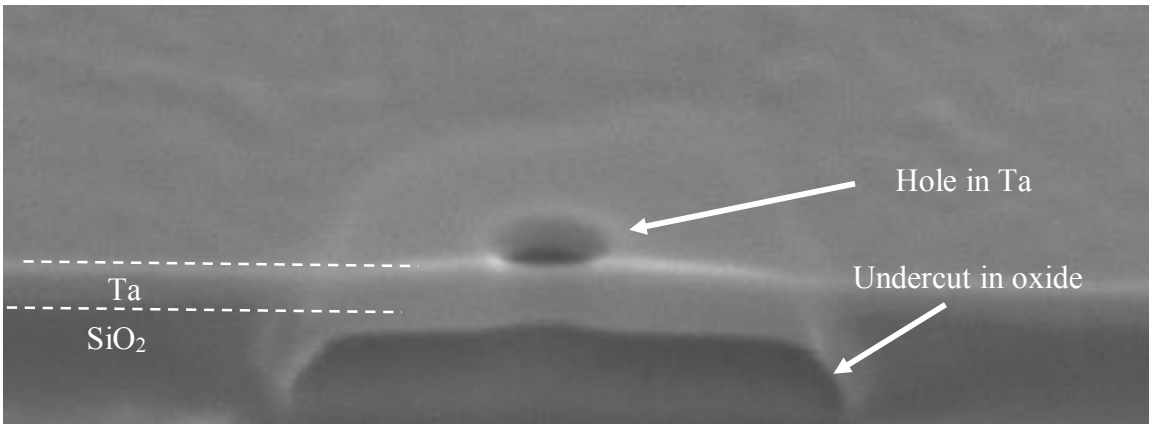

Figure 10 Stencil mask process: FIB cross-section image of hole etched into Ta/SiO2.

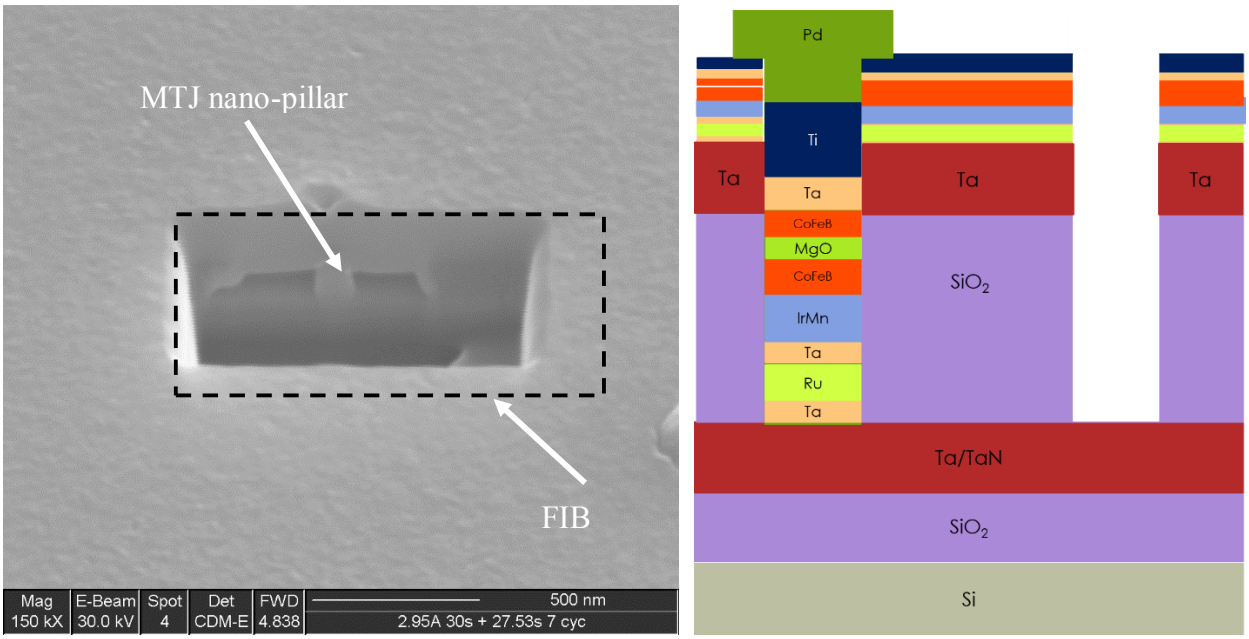

Figure 11 Stencil mask process: (left) FIB cross-section image of a nano-pillar deposited into a 100 nm hole.(right) Schematics of a complete device after patterning the top electrodes and

Performing these steps creates a stencil out of the top Ta layer (figure 9). Next, the MTJ layers are deposited using e-beam evaporation/sputter system into the holes and the MTJ pillars are formed (figure 10).

Finally, the top Ta electrode is patterned using photolithography and reactive plasma etching steps to separate the top contact from the rest of the top Ta layer and adjacent devices on the sample.

This method is simpler than nano-sculpting method and also since it's a self-aligned process, no fine alignment between different lithography steps is required and therefore smaller size devices can be easily fabricated. However various issues with the deposition of the magnetic stack into a hole, makes it a far worse choice for fabricating STTRAMS.

For example, due to the fact that an anisotropic deposition is needed to deposit the MTJ stack into a small opening with high aspect ratio, we had to use an evaporating deposition system

that is not appropriate for depositing MTJ stack layers and yields very low quality magnetic stack. If a sputtering tool is used instead for better quality of magnetic layers, due to higher pressure deposition and relatively isotropic deposition, there would be significant leakage along the sidewalls of the nano-pillars.

And finally, again due to the high aspect ratio of the hole, performing in situ cleaning to achieve a good contact between the bottom contact and the pillar becomes difficult or impossible. (We could not perform in situ cleaning in e-beam evaporation systems and plasma sputtering systems are not capable of anisotropic depositions.)

We attempted to fabricate STT-RAMs using stencil lithography in the early part of the project. However as mentioned due to not being able to perform in situ cleaning, achieving good ohmic contact with MTJ nano-pillars was not possible. Therefore, we decided to switch to nano-sculpting process using Ar ion milling which is used much more widely to make high quality MTJ devices.

(2) Nano sculpting

The more conventional approach to fabricate STT-RAMs is nano-sculpting using Ion milling and a top down process[23], [24]. In this process, a high quality MTJ stack is first blanket deposited on the entire substrate/wafer. Using e-beam lithography and a lift off step afterward, small hard-mask that define the area of the MTJ is planted on top of the magnetic stack. Next, the whole sample undergoes an etching step in an Ar ion-milling system. The MTJ stack is removed in areas not covered with the hard-mask and MTJ nano-pillar with shape of the hard-mask is formed under the hard-mask.

After defining the pillars, an insulator layer of SiO_2 is deposited using an e-beam evaporation system to passivate the nano-pillar as well as for isolation of the bottom and top

contact pads. Now, a second e-beam lithography followed by a plasma etching in CHF_3+O_2 plasma is used to remove SiO_2 from top of the pillars. This step needs to be accurately aligned with the first e-beam lithography (pillar definition using hard mask). Once the opening in the SiO_2 layer created, top contact can be deposited using a lithography and lift off step. However, it's crucial to have an appropriate in situ cleaning step right before the contact deposition without breaking the vacuum.

In these steps, we try to isolate top of the pillars from the substrate and create large contact to top of the pillars for electrical measurements.

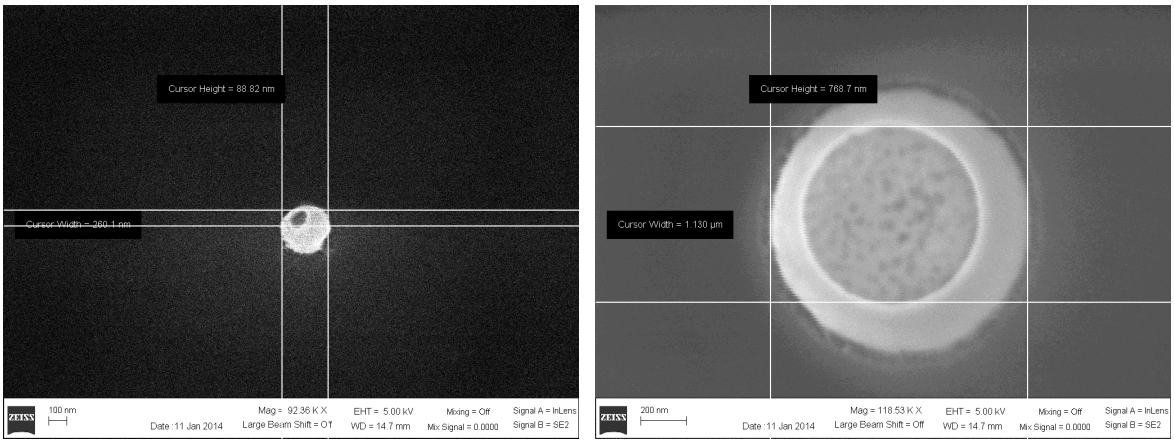

Figure 12 A patterned nano-pillar with (a) 300 nm diameter with a 80 nm contact hole on top (b) 1000 nm diameter with a 700 nm contact hole on top.

Figure 12 shows an MTJ pillar that is partially covered by the SiO_2 layer before deposition of the top contact.

Minimum size of devices made using this method, are limited by the accuracy of E-beam lithography system and the alignment accuracy when creating opening in the SiO_2 layer. We estimated to be able to fabricate a minimum feature size of 70 nm using JEOL E-beam aligner system with this method.

In order to further scale down this size, we need to pattern the mask for Ar ion milling step with imprint lithography instead of e-beam lithography. However, since it's difficult or simply impossible to align consecutive imprint lithography steps, the process needs to be self-aligned. To do so, metallic hard mask that was used previously should be replaced with the imprint lithography resist.

However, this resist should be able to survive the ion milling step to be used for lift off of the insulating later in the next step.

DEPOSITION:

To deposit a high quality (i.e. high TMR) MTJ multilayer stack, we need to use a sputter tool or molecular beam epitaxy (MBE) tool. The in-house sputter tool (base pressure ~4x 10^{-8} Torr) was loaded with CoFe, MgO, Ru and Ta sputter targets. MgO was deposited using RF sputtering and the rest of the metallic layers were deposited using DC sputtering. Starting from a thermally oxidized Si wafer, we deposited Ta/Ru/Ta layers that prepares a smooth under layer to start with as well as acts as a seed layer. It is very important to achieve the correct texture of the CoFe/MgO/CoFe interface for higher TMR. We could not confirm the crystalline properties of the deposited MgO layer. Also as the tool is frequently used for Indium-Tix-Oxide deposition, the MgO target got contaminated. For the MBE tool, though we had Fe and MgO sources available, a proper cap metal source was not available.

To avoid these issues, we started working with MTJ stacks supplied by INTEL. The detail of the MTJ stack is shown in Figure 13. The TMR and RA product estimated from the current in plane tunneling measurements (CIPT) is approximately 106 % and 12 $\Omega\mu m^2$.

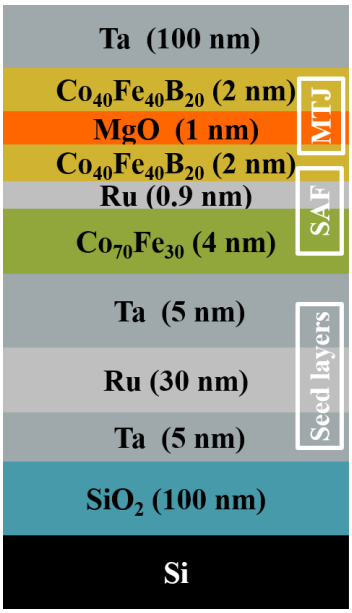

Figure 13 MTJ stack supplied by INTEL.

The stack is patterned following the process steps summarized above. As can be noted, the thick top Ta layer makes it very difficult to make good Ohmic contact on to the nano-pillar due to native Ta oxide. Initial devices fabricated from this MTJ stack, without in-situ cleaning step before the top contact metal deposition showed very high tunneling resistance due to the Ta oxide layer. This tunnel barrier resistance shadowed the low RA product MgO barrier completely.

MFM:

To confirm the four equilibrium states of a cross-shaped ferromagnet magnetic-force-microscopy (MFM) could be applied. For this purpose only patterned ferromagnetic structures are sufficient. Thin Co films of 20 nm thicknesses are deposited on to thermally grown SiO_2 by e-beam evaporation. After patterning the films into cross shapes, the magnetic domains were investigated by MFM measurements as shown in Fig. 1 and Fig. 2. Using external magnetic fields the cross-

shaped magnets were magnetized along different orientations before checking them by MFM. Devices as large as 1 micron (Fig. 14) were showing single magnetic domain per branch. Devices as small as 30 nm (Fig. 15) in width were thermally stable in all 4 states when they were switched by a magnetic field.

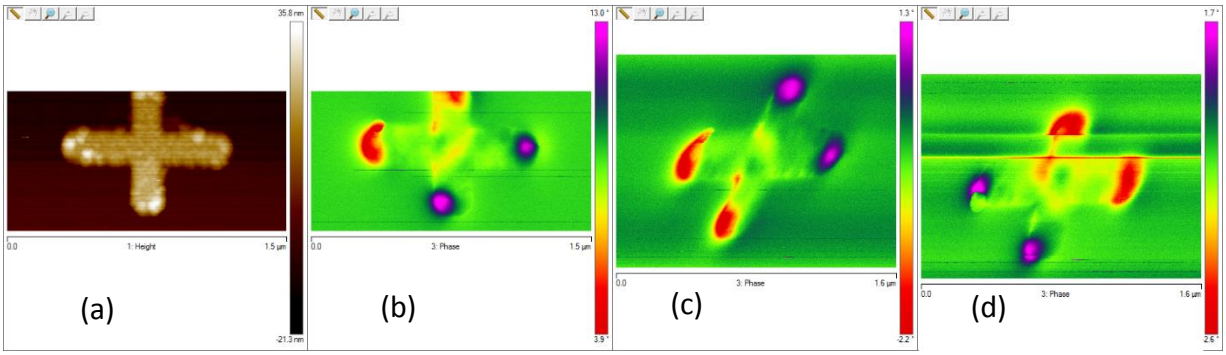

Figure 14 MFM images of a cross-shaped nanomagnet showing different states. The width of the branches are 100nm. Both vertical and horizontal branches are 900nm long.

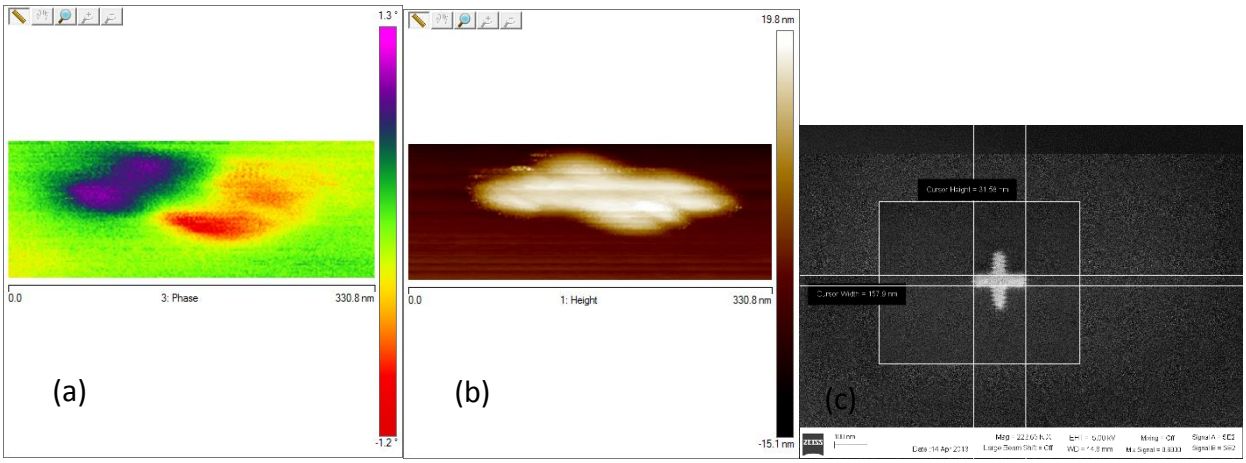

Figure 15. (a) & (b) MFM images of cross-shaped nanomagnet at a stable state. The widths of the branches are 30nm. Both vertical and horizontal branches are 100nm long. (c) SEM image of the same cross-shaped nanomagnet.

CONCLUSION AND DISCUSSION

We attempted to create multi-state memory cells by fabricating STTRAMs with cross-shaped magnets. We worked on different methods in order to fabricate such STTRAMs. However due to limitations on the available tools we were not able to achieve final goal to fabricate a fully functional multi-state STTRAMs.

Contact resistance and in situ cleaning steps turned out to be a critical factor in fabricating STTRAMs both using stencil lithography and patterning using Ion milling.

We studied cross-shaped MTJs using MFM measurements and OOMF simulations and showed four different stable magnetic states in the smallest cross-shaped magnets that we could fabricate with our current tools.

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