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2017

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Built-in-Self-Test and Foreground Calibration of SAR ADCs

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Built-in-Self-Test and Foreground Calibration of SAR ADCs

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Thesis

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

Master of Science in Engineering

The University of Texas at Austin

Dec 2017

Acknowledgements

Firstly, I would like to thank Prof. Nan Sun for his guidance, suggestions and support throughout the project. In fact, his analog class was instrumental in shaping my interests and initiating me into circuit design. I am also grateful to Prof. T R Viswanathan for our innumerable discussions and his advice to have a practical and holistic approach to research.

Also, I would extend my sincere thanks to my colleagues Sungjin Hong, Linxao Shen and Abhishek Mukherjee for their able mentorship and inputs specific to this work.

I would also take this opportunity to thank the 'Power and Isolation' team at Silicon Laboratories Inc., for a great learning experience during my internship. A special mention to my friends and roommates - Rohit Aggarwal, Phanindra Rao, Shashank Bassi, Praful Gupta, Chandra Shekhar, Kunal Punjabi and Venkat Suresh for being a part of this wonderful journey through graduate school.

Finally, this work would not have been possible without the love and encouragement of my parents – it is their motivation and assurance which keeps me going!

Abstract

Built-in-Self-Test and Foreground Calibration of SAR ADCs

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The University of Texas at Austin, 2017

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This thesis explores the scope of 'Built-in-Self-Test'(BIST) schemes to reduce the time cost complexity associated with the production tests for static linearity errors in Successive Approximation (SAR) ADCs. In this regard, an on-chip implementation of the 'Stimulus Based Error Identification and Removal' (SEIR) method [1] is sought to be pursued. As an extension, it is proposed that the estimated ADC non-linearities may then be suitably calibrated to achieve higher resolution. A brief review of the testing and calibration algorithm is undertaken. Further, this work elaborates on the design of a prototype front-end test generator and a buffer interface to calibrate a 10MHz 14 bit redundant SAR ADC in the TSMC 180nm process. Simulation results validating the circuit implementation of the integrated front-end system have been presented.

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Chapter 1: Introduction

1.1. Motivation

Technology scaling has driven most electronic systems to carry out signal processing and computations in the digital domain. It offers numerous advantages in terms of programmability, reconfigurability and ease of data storage. However, since real-world signals are inherently analog, 'Analog-to-Digital' data conversion has become a fundamental pre-processing operation. The impetus is to digitize the signals right up-front and subsequently exploit the flexibilities of digital signal processing. In most of these systems thus, the ADC forms a crucial performance defining subsystem.

Figure 1.1 shows a typical front-end system with the ADC block being the interfacing component between the analog and digital domains. The architecture and specification of the ADC is typically set by the system considerations of resolution, power and bandwidth.

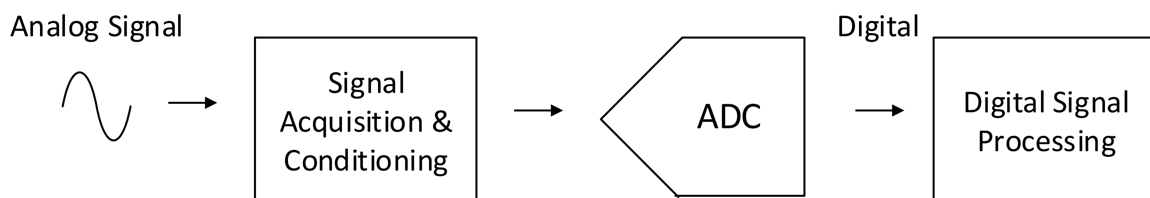

Figure 1.1: Typical Front-end Data Acquisition System

1.2. ADC Architecture Overview & Trends

This section briefly presents the application areas of the various data converter architectures as illustrated in Figure 1.2.

In the high- speed & low resolution segment, flash converters (and its derivatives of folding and interpolating ADCs) dominate the market. With its parallel comparisons for the

input signal against known set-up reference levels, it provides for the highest speed. However, it scales poorly to higher resolutions as it comes with an exponentially increase in area and power overhead for its comparators.

On the other extreme, the low speed and high precision application space is captured by delta-sigma converters. Based on the principle of oversampling and noise shaping, delta-sigma converters rely on digital post-processing and filtering to achieve high resolutions. The inherent oversampling requirement however limits its application extension to high speed domains.

Pipeline converters serve well for the medium to high speed segments. It is based on the principle of sequentially passing on the residue errors to successive stages to improve the resolution in a pipeline fashion. Each of the stages actively quantizes its input at every clock cycle, while trading off parallelism for latency.

Successive Approximation ADCs (SAR) have emerged as a power efficient solution in the medium resolution segment. Principally, it involves a binary search algorithm to compare the input against dynamically varying reference levels (based on previous comparison results). A typical implementation uses a capacitive DAC (operating on the principle of charge redistribution) and a comparator to successively cycle through the search. However, its extension to higher resolutions (> ~11) bits is limited by the stringent matching requirements of the capacitors in the DAC array [2].

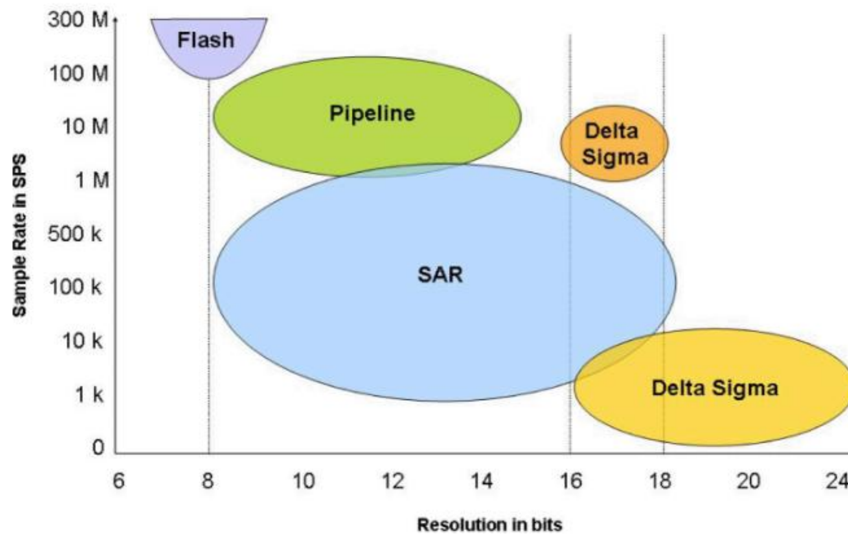

Figure 1.2: Data Converter Market Segment [16] (Based on Resolution and Sample Rate Specification)

Evidently thus, each of the architectures has their own design and performance trade – offs. Researchers often seek to push the boundaries of these limitations towards achieving better "figures of merit" by improving one or more parameters of power, resolution and bandwidth. Moving ahead with technology scaling, SAR ADC emerges as the most likely candidate for growth. With its minimal analog component complexity and digital compatibility, it is expected that at faster CMOS nodes, the bandwidth performance of SAR would also see the same progression. On the other hand, pipeline and delta sigma ADCs are not typically expected to see the same dividends with technology scaling. With shrinking voltage supplies (and headroom for the active devices) and lower intrinsic device gains, the design of power efficient analog blocks (OTAs for pipeline & loop filters for sigma delta) would be challenging.

As a result, a lot of research effort has been put to address the linearity concerns in high resolution SAR ADCs. Instead of trying to improve the matching accuracy through design techniques or fabrication advances, the cheaper solution proposed is to calibrate out these errors dynamically through digital assists. In other words, the idea is to extract the

actual search step sizes (or actual capacitor values) and correct for the same digitally (given that these static mismatches result in systematic errors). The next natural question then pertains to the detection of these very static errors in the SAR DAC array.

Typically, the static linearity performance of ADCs is characterized on the basis of specification tests. This involves validating the block for known inputs signals or sequences. In this regard, state-of-the art production tests for data converters make use of expensive off-chip testers and signal generators. In addition to the economic cost involved in housing the test set-ups, the time cost involved for each part adds significant overhead to the production flow. Thus, employing these production tests for linearity testing of high resolution and subsequent calibration is not a feasible solution commercially.

In this work, we explore the possibilities of a Built-In-Self-test (BIST) scheme for ADC linearity measurements and propose the same as a viable alternative for high resolution SAR ADC calibration.

Please note that while the general principles of on-chip ADC linearity testing may be universally applied to all architectures, this work specifically focuses on the static error DAC mismatches in a SAR ADC. A successful demonstration of the self test and calibration scheme for SAR ADCs would open up a new paradigm for high resolution nyquist rate converters.

The next part of this chapter reviews some fundamental static linearity metrics for ADCs – the Integral Non linearity Error (INL) and Differential Non Linearity Error (DNL). Following this, the scope of BIST schemes for linearity testing and subsequent calibration is evaluated.

1.3. ADC Performance metrics

This section reviews a few ADC performance parameters, especially critical in its static linearity characterizations.

The smallest resolution quantized by an ADC of N bits is given by

$$Resolution\ (LSB), \Delta = \frac{V_{FS}}{2^N} \tag{1.1}$$

where V_{FS} is the full scale reference of the ADC. A shown in Figure 1.3, an ideal ADC mapping function quantizes the entire voltage range into 2^N discrete digital codes - with each interval corresponding to the resolution Δ.

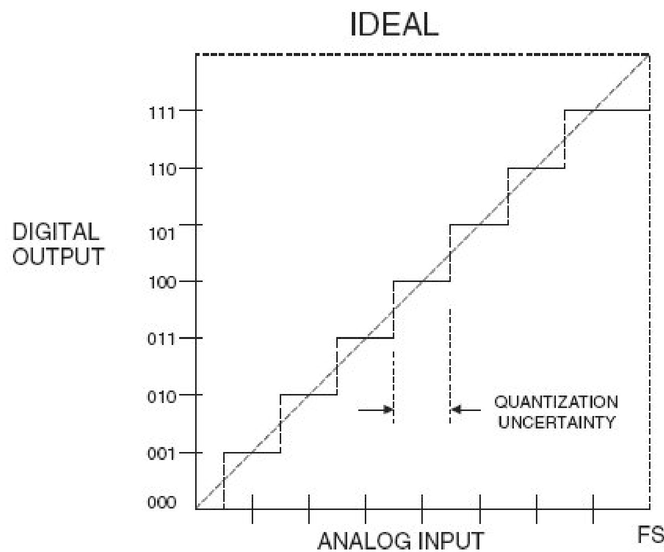

Figure 1.3: Ideal ADC Mapping Function (3 bit example) [3]

The ideal code transition points I[k] may then be defined as the analog input voltage where the ADC code switches from code *k-1* to code *k*. Also, the code width W[k] for code *k* is the difference between the transition points of two successive codes.

$$W[k] = I[k] - I[k-1] \tag{1.2}$$

In the ideal case, the code widths W[k] are each equal to the resolution Δ and the transition points may be given in terms of the lower bound $Vref_{,n}$ as:

$$I[k] = Vref, n + (k-1)\Delta \tag{1.3}$$

However, the presence of static non linearities causes a deviation in the ideal transfer function – manifesting in the form of changes to the ideal code widths and transition points. These variations are captured by the metrics of Integral Non linearity Error (INL) and Differential Non Linearity Errors (DNL) (Figure 1.4).

Integral Non linearity (INL): INL errors refer to the deviations in the ideal code transition points. If the actual code transition for code occurs at a voltage T[k], INL[k] may be given as:

$$INL[k] = \frac{T[k] - I[k]}{\Delta} \tag{1.4}$$

Differential Non Linearity Errors (DNL): The normalized difference in the actual code widths W'[k] against the ideal represents the DNL for the particular code:

$$DNL[k] = \frac{W'[k] - \Delta}{\Delta} \tag{1.5}$$

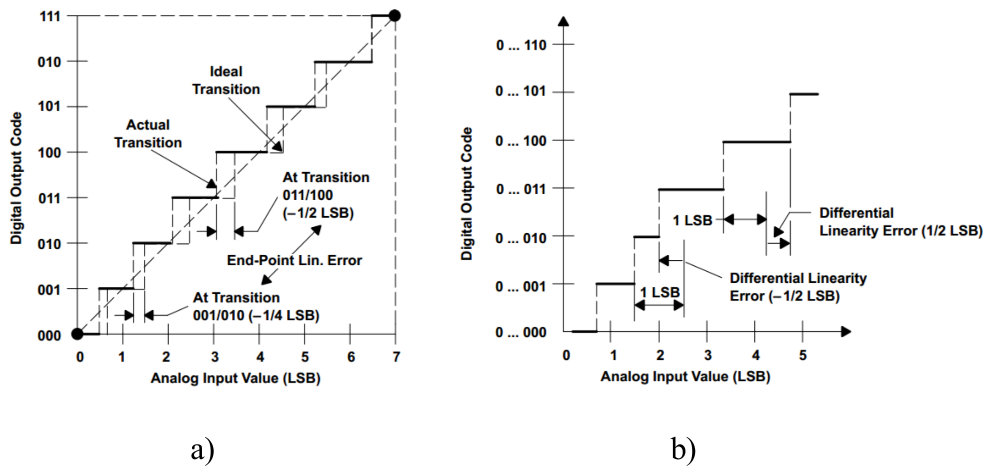

Figure 1.4: ADC Static Linearity Metrics – a) DNL and b) INL [4]

In the frequency domain of the output, DNL errors typically reflect as an increase in the quantization noise floor of the spectrum. INL errors, on the other hand, result in harmonic distortion affecting the SNDR performance.

1.4. Histogram test

Standard production tests for ADC linearity measurements exploit the code counts to estimate the transition levels. For a known input signal, the histogram of the ADC output codes is compared against the ideal expected probability distribution. Any deviation in the distribution would then be indicative of static errors in the transition levels/ code widths. Essentially, the computation of the INL and DNL from the histogram relies on the correlation between the code counts and the relative step sizes (or code widths) of each of the discrete levels. Once the actual transition times or step sizes are known, the INL and DNL estimation follows from Equation 1.2.

The choice of the input signal is a critical consideration for the histogram based test. In the ideal case, a quasi- static input which ensures sufficiently high hits per code is chosen. This is to ensure that the code counts obtained are statistically significant and

noise/measurement errors may be minimized. Conventionally, a linear ramp based histogram has been widely adopted. For an ideal ramp, a uniform distribution for the code counts is expected – which greatly simplifies the digital post – processing. Other methods involving sinusoidal signals have also been adopted, however requiring a more complex computation for the associated probability distribution.

In this work, a ramp based histogram self – test has been explored owing to the simplicity of the linearity estimation. However, one of the foremost challenges in the approach is the linearity requirement of the stimulus itself. State-of-the art testing schemes use off-chip expensive signal generators to ensure the desired test signal performance. However, this comes with an inherent associated time cost - thereby severely limiting its potential application for calibration of each part.

The motivation thus is to come up with a BIST method to replicate the histogram based measurement and compute the ADC non linearities. This may be subsequently used for calibration purposes. On- chip ramp signal generators in this regard have posed numerous design challenges. The most critical concern has been the linearity of the ramp signal itself. Since the purpose of the calibration approach is to progress towards high resolution SAR (> 12 bits), the associated ramp linearity requires to be at least an order higher than the ADC under test. In the event of unknown non-linearities in the ramp, the histogram of the code count can no longer be expected to be uniform and the standard methodology fails.

In the most basic sense, an on-chip ramp generation would involve a current source charging a capacitor. The rising ramp voltage is given as a function of time as:

$$V(t) = \frac{I.t}{C} \tag{1.6}$$

where I is the value of the current source used; C is the capacitor value being charged; t is the time for which the charge is being integrated on the capacitor.

The linearity of the ramp generator is typically limited by finite output impedance of the current source. This results in an exponential rise dictated by the associated time constant formed by the impedance and the capacitor. Further, the linearity requirement for the ramp must span across most of the ADC dynamic range (~70%) to ensure that most of the exercised code span is tested. Secondary effects may come from the non linearities of the capacitor itself and the driving buffer stages to the ADC. Also, variations across PVT prevent any attempt to characterize these non linearities upfront. Due to these factors, the design of an on-chip linear ramp generator to resolutions as high as ~14 bits is non-trivial.

As an alternative, A 'Stimulus Based Error Identification and Removal' (SEIR) method has been proposed by Jin *et al* [1] which seeks to relax this very ramp linearity requirement to enable on-chip implementations. The essence of the idea is to extract the non linear behavior of the input signal dynamically during testing and subsequently account for the same in the post processing. As a result, it may still suffice to have a much lower resolution for the input ramp to test high resolution ADCs. Chapter 2 elaborates on the algorithm and working principle of the SEIR algorithm.

1.5. Ideal characteristics of a BIST scheme

The design of the proposed front-end test and calibration circuit would be guided by the following general requirements of a typical BIST implementation [5]:

1. The circuit and hardware overhead for the testing blocks should not be a significantly more than the core under test itself. Aspects of concern would be the area of the test generator blocks and the power consumption (critical for background calibration schemes).

2. The test blocks should have a significantly higher precision, accuracy and yield than the device under test. Alternatively, the test algorithm should be highly tolerant to the non idealities and noise effects on the test signal/vectors.

3. The BIST circuit should itself be testable and programmable. There should be enough scope and flexibility provided to the chip user for configuring, debugging and probing test nodes.

4. The BIST algorithm should replicate the ideal state-of-the-art off-chip testing methodologies as closely as possible. In other words, the proposed solution should be exhaustive in its test coverage and must offer a reliable and robust alternative to conventional solutions.

The remainder of this thesis is organized as – Chapter 2 reviews the SEIR algorithm in the context of quasi-static linearity testing of ADCs. The next chapter presents the architecture and system level considerations for the proposed signal generator and ADC driving interface. Chapter 4 delves into the schematic level design details of these mixed – signal blocks. A brief description of SAR block under test (and its specific redundancy requirements) is presented in Chapter 5. Subsequently, Chapter 6 discusses the simulation results (post-layout) and outlines possible calibration schemes for the INL corrections. Finally, the thesis concludes with a summary of the work, along-with scope for future work.

Chapter 2: Stimulus Identification and Removal Algorithm

2.1. Algorithm Review

The SEIR test method introduced in [1] seeks to relax the stringent linearity requirement on the input ramp signal for histogram based quasi-static ADC performance testing. Instead of trying to guarantee the on-chip ramp resolution, the idea is to rather extract and parameterize the input signal. Once the input signal is fully characterized, the same can be incorporated in the expected probability distribution of the codes and the ADC linearity errors may be isolated. The work in [1] in fact demonstrates that a ramp good to ~7 bits suffices for testing 14 bit ADCs.

In this section, a brief review of the SEIR algorithm is demonstrated for a non linear ramp input. Let the input signal x(t) be represented as a superposition of the ideal ramp component and a non linear function F(t). Further, we assume that the domain for t be between [0,1] units.

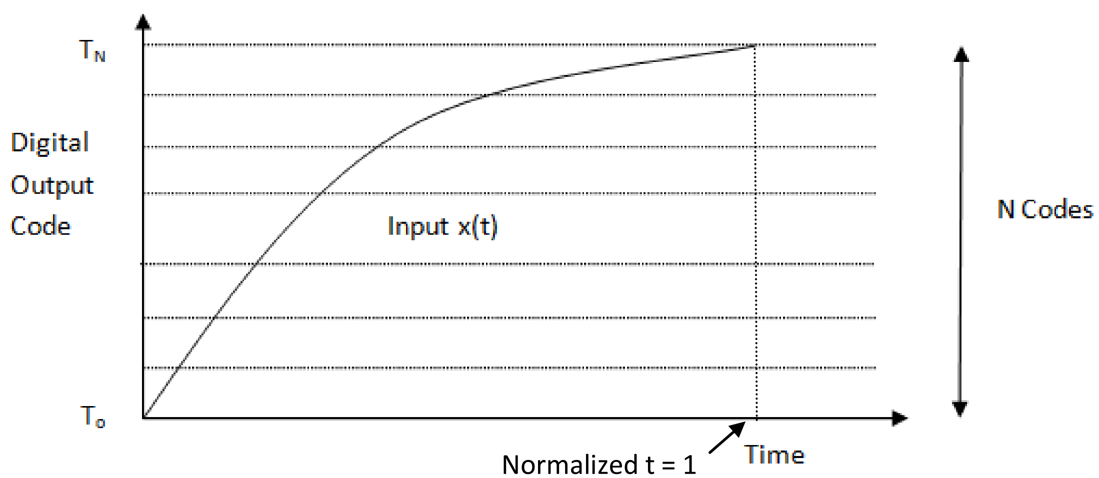

Figure 2.1: Representation of the input signal stimulus x(t). Ideally a ramp, this plot exaggerates the non-linear component of x(t).

The input signal (shown in Figure 2.1) is expressed in terms of its range between code levels T_o (first code) and T_N (last code) as:

$$x(t) = (T_N - T_o).t + T_o + F(t) \quad (2.1)$$

For an ideal ADC with INL = 0 for all codes, the ideal transition levels I(k) can then be formulated as:

$$I(k) = \frac{T_N - T_o}{N}.k + T_o \ , for\ k = 1\ to\ N \quad (2.2)$$

From the histogram data, let us denote the code counts obtained as C_k for codes k ϵ [0, N] where N is the total number of codes (equal to 2^n for n bits of ADC resolution). The estimated code transition times $(\widehat{t_k})$ for each code k are then given by the corresponding cumulative values:

$$\widehat{t_k} = \frac{\sum_{i=1}^{k} C_i}{\sum_{i=1}^{N} C_i}, for\ k = 1\ to\ N \quad (2.3)$$

For the estimated transition times, the corresponding output levels are then computed for the known input signal. The actual transition levels are then given by:

$$T(k) = x(\widehat{t_k}) = (T_N - T_o).\widehat{t_k} + T_o + F(t_k) \quad (2.4)$$

For an ideal ramp with F(t) = 0, the INL for each code is:

$$INL(k), LSBs = \frac{T_k - I_k}{\Delta} = N.\widehat{t_k} - k \quad (2.5)$$

However, in the presence of a non-linear component in the input F(t),

$$INL(k), LSBs = \frac{T(k) - I(k)}{\Delta} = N.\widehat{t_k} - k + F(\widehat{t_k}) \tag{2.6}$$

In as much as F(t) is unknown, Equation 2.6 cannot be evaluated for computing the INL for each code. The SEIR algorithm seeks to resolve this conflict and estimate F(t). It expresses this non-linear component as a sum of orthogonal basis functions:

$$x(t) = (T_N - T_o).t + T_o + \sum_{i=1}^{M} c_i\, f_i(t) \tag{2.7}$$

For this work, the basis functions are chosen to be a set of 'M' harmonic sinusoids. The idea is that the periodicity associated with these functions should be able to model the non-linear artifacts of the ADC transfer function.

$$f_i(t) = c_i.sin(pi * i * t) \tag{2.8}$$

Please note that for the domain of definition of t between [0,1], boundary conditions are set as $f_i(0) = 0 = f_i(1)$. To estimate c_i for the 'M' basis functions, the SEIR method proposes to run the histogram test for a functionally related input ramp shifted by a constant offset. It relies on the consistency of the non –linearity component of the ramp for the two runs (with the only difference being the offset). For an offset of α, the ramp may be expressed in terms of the same basis functions (and coefficients c_i) as:

$$x^{'(t)} = (T_N - T_o)t + T_0 + \sum_{i=1}^{M} c_i f_i(t) - \alpha \tag{2.9}$$

Again, the transition times $(\widehat{t'_k})$ may then be obtained from the histogram code counts C'i(k). The times however need to be normalized to fit the domain of definition t ϵ [0,1]. In fact, the difference of the first code counts C_o and C'_o holds the offset information and is used to compute $(\widehat{t'_k})$

$$\widehat{t'_k} = \frac{\sum_{i=1}^{N} C'_i + C'_0 - C_0}{\sum_{i=1}^{N} C_i} \tag{2.10}$$

The INL can be similarly expressed in terms of the transition times t'(k) as:

$$INL'(k), LSBs = \frac{T'(k) - I(k)}{\Delta} = N.\widehat{t'_k} - k + F\left(\widehat{t'_k}\right) - \alpha \tag{2.11}$$

The INL of the ADC is independent of the ramp signal used and so equations (2.10) and (2.6) are equated to yield a set of N equations for k ϵ [1, N]. These sets of equations consist of a lot more equations (N) than the unknown variables (M).

$$N.\widehat{t'_k} - k + F\left(\widehat{t'_k}\right) - \alpha = N.\widehat{t_k} - k + F(\widehat{t_k}) \tag{2.12}$$

which simplifies to

$$N\left(\widehat{t'_k} - \widehat{t_k}\right) = \sum_{i=1}^{M} c_i\left(f_i(\widehat{t_k}) - f_i(\widehat{t'_k})\right) + \alpha \, , for \; k = 1 \; to \; N$$

A **Least Square** (LS) Estimation method may be adopted to solve this set of over-constrained equations to get a best fit solution for the coefficients c_i's. The LS constraint can be expressed as:

$$Min\{\sum_{k=1}^{N}[N(\widehat{t'_k} - \widehat{t_k}) - \sum_{i=1}^{M} c_i \left(f_i(\widehat{t_k}) - f_i(\widehat{t_k'})\right) - \alpha]^2\} \quad (2.13)$$

In practice though, due to the restricted domain for definition of $f_i(t)$ between t ϵ[0,1], the equations are not valid for the codes [N-α, N]. This is because at t=1, the offset ramp would have only accumulated till a code of N – α.

2.2. Constancy of the offset generation

The Least Square Fit solution to the set of equation (2.12) assumes that the offset between the two ramp vectors remains constant throughout the entire ADC span maintaining the same functional relation. Any errors in the offset generation (in the order of the ADC resolution itself) would not be essentially compensated for by the LS fit. In fact, the premise of the equation (2.12) stand invalidated, thus making the testing ineffective. Researchers have focused on ensuring a constant offset between the two ramps for implementation on-chip. The critical aspect to note again is that the absolute value of the offset itself is not of a concern. This exact value would in fact emerge out of the LS fit solution - it is only required to ensure the constancy of the injected offset.

2.3. Characterization of the SEIR parameters

In this section, we briefly review the considerations associated with the choice of the parametric variables in the process – the associated trade –offs would be accounted for in the design phase.

1. Offset between the two ramps: The choice of the offset between the two ramps is made on the consideration of the noise effect the measurements. The offset is chosen significantly higher than the standard deviation of noise in the system so that the offset may not be swamped out by noise itself. If this happens, the variations and uncertainties in the offset value would progressively worsen the LS fit results. On the other hand, a large offset would reduce the effective number of equations to perform the LS algorithm. For an offset of α, only the first $N-\alpha$ equations can be used. However, as long as $N-\alpha$ is still much larger than the M unknowns, minimal changes may be expected to the fit. In this work, an offset of ~128LSBs is sought to be injected for the second ramp (based on the demonstrated results in [6]).

2. Number of coefficients in the basis functions: The basis function provides a skeletal parametric form to model the input non-linearities. Increasing the scope of the function by including higher harmonics (essentially increasing 'M') would in fact help in capturing higher frequency artifacts better. However, with more coefficients to be estimated, there is a penalty in terms of the robustness of the LS fit method. The number of harmonics of the sinusoidal basis functions considered in this work is 30 [6]. Indeed, the choice of the number of basis functions is not an aspect of the test circuit design itself. This post-processing step may be suitably modified based on the specific measurement data.

2.4. Error Sources

The SEIR algorithm implemented as the LS fit of the equation (2.12) may be typically subjected to the following error sources:

2.4.1. Estimation of the transition times

In a conventional histogram based test, the transition times for each code are mapped to their corresponding cumulative code counts. However, the smallest time unit that may be captured in this approach is proportional to the inverse of the total code count. For example, a unit increment in count for any code k is quantized to the time resolution given by:

$$Time\ resolution\ \delta t\ (Smallest\ time\ step) = \frac{1}{\sum_{i=1}^{N} C_i} = \frac{1}{N * Hits_per_code} \quad (2.14)$$

Further, this uncertainty in the time step corresponds to an error in the digital output (in LSBs) to the order of:

$$T(t_k), transition\ time\ quantization \sim N.\delta t = \frac{1}{Hits_per_code} \quad (2.15)$$

If we assume that this error distribution is uniform, its variance is given as:

$$\sigma, T(t_k)^2 = \frac{1}{12.(Hits_per_code)^2} \quad (2.16)$$

Indeed, a finer resolution may be obtained by increasing the total code counts. In other words, for a given ADC sampling rate, this would translate to an upper bound on the required ramp slope.

2.4.2. Errors due to unparametrized non-linearity

As alluded to in the previous section, the input ramp non-linearity may not be entirely parametrized by basis functions. Due to the limited number of basis functions, there could be residual unmodeled errors ($e(t_k)$). However, these errors would typically be high frequency artifacts – beyond the scope of what can be expressed in terms of the 'M' harmonic functions (Equation 2.17). The input signal ramp is itself not expected to have dominant high frequency non-linear components (in the order of 1LSB) – it is the circuit noise at high frequencies (riding over the stimulus signal) that remains unparametrized.

For a given measurement run, these errors may be minimized by increasing the number of basis functions as a part of the post processing computations. However, it does come with it trade –off in terms of the performance efficiency of the LS fit.

$$x(t_k) = (T_N - T_0)t + T_0 + \sum_{i=1}^{M} c_i f_i(t_k) + e(t_k) \tag{2.17}$$

2.5. Noise effects in the ramp signal

The analysis of the noise effect on the SEIR method may be evaluated in terms of low frequency and high frequency components.

Let us first analyze the low frequency contributions. Typically, the dominant sources for this noise would be the flicker noise of the circuit components and the reference supply drift. While it may seem that these noise effects may not severely affect the ramp signal and probably only result in non-linearities that can be captured by the basis function, the concern is however regarding the constancy of these artifacts (during the next measurement run with the offset). Equation 2.12 inherently assumes that the non-linearity in the input remains the same when the same set of basis coefficients are used for the model. In the presence of low frequency noise, the stationarity of the signal between the two runs may not be maintained. In other words, since the functional correlation between the two ramp signals is broken – they may in fact be now viewed as two independent histogram test measurement runs.

Flicker noise in the ramp signal may be minimized by increasing the device dimensions of the components in the front–end. Alternatively, filter stages with low frequency cut–off frequencies may be used in the signal path. However, these solutions would consume a lot of area overhead and will not be suited for a practical BIST implementation.

Alternatively, it is proposed to interleave between the two ramp signals [1]. This means that the ADC would sample/convert a value from the first ramp and follow it up with the offset version in the next cycle (Figure 2.2).

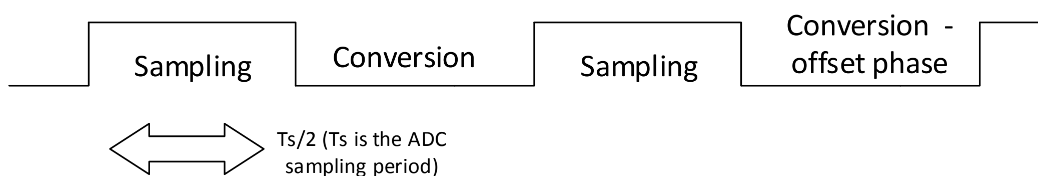

Figure 2.2: Interleaved ADC operation for the offset generation phase

This ensures that the two measurements are subject to the same non-linear function of the input – thus avoiding the need for complex noise reduction or filtering. Another way of stating this would be that the two ramps would retain their functional correlation when interleaved and thus the same basis coefficients may be used.

On the other hand, the high frequency noise components (mainly the thermal noise contributions) typically remain outside the scope of what may be represented by the basis functions. As described in Section 2.4.2, these high frequency components remain undetected in the measurement and manifests in the form of incorrect code counts. In other words, it is likely that the sampled value will be incorrectly assigned to the neighboring codes. This is more likely to occur for values close to the transition voltage edges. As a result, errors are introduced in the estimation of the transition time instants t_k. Assuming a Gaussian distribution, the standard deviation of the error (σ, $n(t_k)$) in the estimation of the transition time has been mathematically expressed as a function of the noise power (σ_s) and code counts (N) as [1]:

$$\sigma^2, n(t_k) \cong 0.5.\frac{\sigma_s}{N} \tag{2.18}$$

For a given system noise, the estimation errors may thus be minimized by increasing the hits per count, N. For the targeted value of N~30, ensuring that the circuit noise power on the stimulus ramp is within the resolution of the system (1 LSB) should be easily sufficient to suppress these time estimation errors in the INL measurement.

2.6. Ramp function with non-idealities

Incorporating the various sources of non-idealities described above, the input ramp stimulus may be expressed in terms of the unmodeled errors $e(t_k)$, time quantization errors $T(t_k)$ and the noise contribution term $n(t_k)$ as:

$$x(t) = (T_N - T_o).t + T_o + \sum_{i=1}^{M} c_i\, f_i(t) + e(t_k) + T(t_k) + n(t_k) \qquad (2.19)$$

Assuming a Gaussian distribution to each of the errors, the overall error in the INL estimation also follows a normal distribution with a mean of zero and a variance given by:

$${\sigma_{INL(k)}}^2 = {\sigma_{e(t_k)}}^2 + {\sigma_{T(t_k)}}^2 + {\sigma_{n(t_k)}}^2 \qquad (2.20)$$

As long as this assumption is valid, it implies that the statistical average of a large number of INL estimations (as long as the measurements cover the gamut of each of these error distributions significantly) should yield a better convergence to the true value. For the circuit noise component (typically assumed Gaussian and white), merely repeating the measurements over a large number of runs should significantly average out these effects and provide better fit LS fit results. On the other hand, averaging out the inherent input unmodeled errors and the time quantization errors might not be achieved easily through just repeated test runs. Thus, it is still essential to ensure that the input does not have systematic high-frequency components (for the chosen number of basis functions) and that sufficiently high hits per code are obtained.

Chapter 3: System Level Architecture

3.1. ADC Prototype

For the purpose of a demonstration of the BIST idea, a SAR ADC is sought to be tested for static linearity errors arising due to its DAC array capacitor mismatches. As highlighted in the introduction, one of the limiting challenges for the extension of SAR to higher resolutions is its static linearity concern.

This work uses an existing IP block for the SAR ADC. Only minor modifications have been made to the same to suit the requirements of this project. The changes mainly pertain to the DAC array to introduce redundancy for calibratability. In addition, an offset generation scheme has also been incorporated to the DAC array operation. Details of these project specific updates have been presented in Chapter 5. The overall specifications of the prototype differential ADC are presented in Table 3.1.

Table 3.1: Prototype ADC Specifications

Specification	Remarks
Resolution	14 bit (ENOB ~ 13 bits)
Sampling rate	10MHz
Voltage range	[0-2V]
Redundancy	3 bits

3.2. BIST Front-end

The overall BIST scheme architecture is shown in Figure 3.1. The front end generates the ramp signal for the histogram test and interfaces to the ADC through buffer driving amplifiers. The results of these linearity measurements feed into a calibration engine that stores these static errors and uses it for subsequent digital corrections.

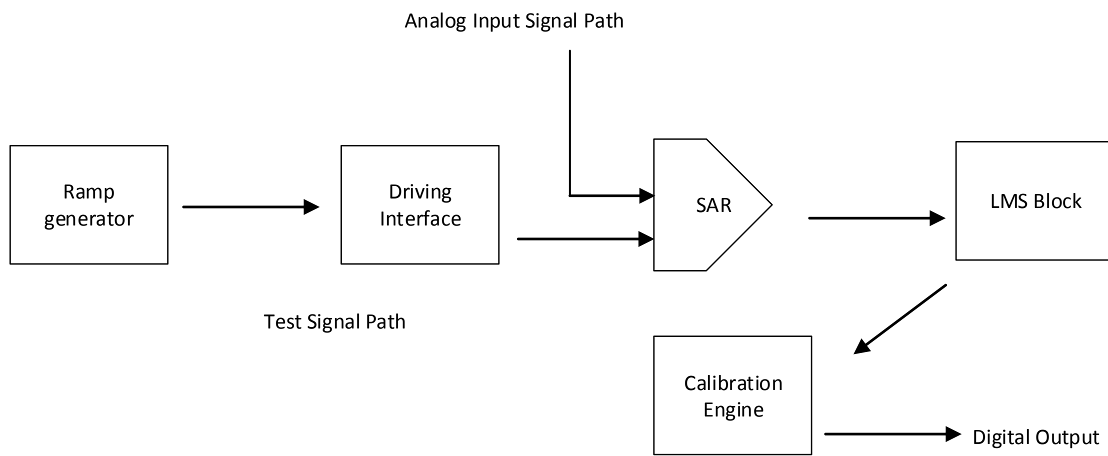

Figure 3.1: System Architecture of the BIST & Calibration scheme

3.3. Ramp Signal Characteristics

This section goes through the system level considerations for the architecture for the front-end ramp generator block from a design and implementation perspective.

The ADC full scale range ranges from 0 to 2V. For the purpose of testing, this work seeks to test the INL for the ADC codes spanning 30% to 70% of the full scale. This essentially translates to a voltage ramp with a resolution of >13 bits across a voltage range of 0.3V to 1.7V. Please note that though the algorithm is robust to linearity errors in the ramp input, we set a design target to try to achieve better than the desired 13 bits of resolution.

Striving for the best performance possible for the ramp would ensure that even with on-chip silicon linearity degradation, the modeling of same using the SEIR fit algorithm would not be computationally costly.

3.4. Single Ramp vs Repetitive Ramp Testing

The ramp slope is dictated by the requirements on the number of hits per code. As explained in the previous section, maximizing the hits per code is always beneficial in terms of suppressing the circuit noise effects and also to ensure that the quantization in the transition times from the histogram test are negligibly small. Based on previous characterization results for the number of samples each code [6], we set our system to achieve ~ 30 hits per code. This section evaluates the feasible architectures to obtain this desired code hit rate.

In a repetitive ramp stimulus, the code hits are obtained over multiple cycles of the input. The code counts obtained from all these ramp runs are accumulated together to construct the standard histogram. While this greatly relaxes requirement on the ramp slope, it brings it with the concern of ensuring that each ramp run exercises unique codes. This condition of ensuring coherent sampling is needed so that the ADC is characterized all throughout its granularity level. Various schemes have been proposed in literature in this regard. A popular demonstrated idea is to have a synchronous control on the ramp initiation by appropriately varying the initial conditions [7, 8]. These could be varying the phase of the ramp (by providing suitable time delays for each ramp) or providing different offset amounts in each ramp run (Figure 3.2). There would be an increased digital control overhead due to this.

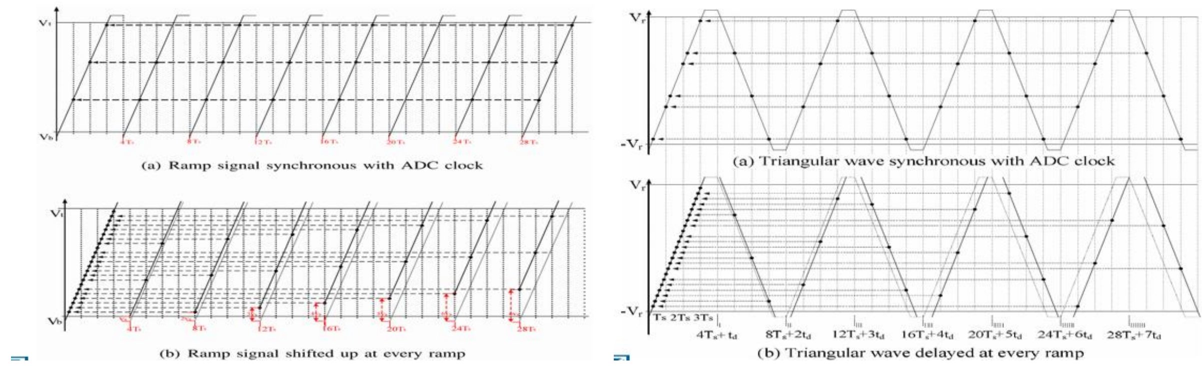

Figure 3.2: Repetitive Ramp Stimuli with varying offsets and time delays [7, 8]

The feasibility of this multi – ramp operation for our testing scheme is also greatly influenced by the stationarity of the signal non-linearities across these runs. If the code counts across all these runs are cumulatively considered for the INL computation, it requires each ramp to have the same characteristic function. As brought out in Chapter 2, drift and gain errors due to reference variations and low frequency noise would invalidate the SEIR algorithm. Guaranteeing constancy would impose strict requirements on the noise filtering. An alternate testing technique would be to compute the INL from the histogram of each these runs. Indeed, with fewer hits per code, the major concern would be the errors in the time quantization – however these errors could be statistically averaged out through the multiple runs. But, the major challenge in this scheme would be to ensure that sufficiently high ramp cycle tests are undertaken (to obtain a statistically significant distribution for the INL from these runs) and that the entire probability distribution of the time quantization error is swept through.

In lieu with all this, a single ramp with an adequately slow ramp rate for the desired sample count is considered in this work. The following subsection derives the requirements on the single cycle ramp generator.

3.5. Ramp slope requirement

For an ADC with a resolution of 13 bits and a required sample count of 30 for each code,

$$Total\ code\ counts = 2^{13}.30 = 245760 \tag{3.1}$$

In an interleaved system as proposed for our test, the requirement would double to 491520 codes. For a 10MHz sampling rate, this corresponds to a ramp rise time of:

$$Ramp\ Duration = \frac{491520}{10e6} \sim 50ms \tag{3.2}$$

For a ramp signal generated with capacitor charging, the desired value of current (assuming a capacitor value of ~ 10pF for on-chip implementation feasibility), we have:

$$I = C.\frac{V}{t} = 10pF.\frac{2V}{50ms} \sim 400pA \tag{3.3}$$

3.6. Ramp generation block

In the most basic sense, the ramp generation involves charging of a capacitor (initially discharged appropriately to lower supply rail) by a constant current. Figure 3.3 captures the implementation of the current source realized as a PMOS current source. Setting the appropriate bias voltage on the PMOS source would set up the desired current.

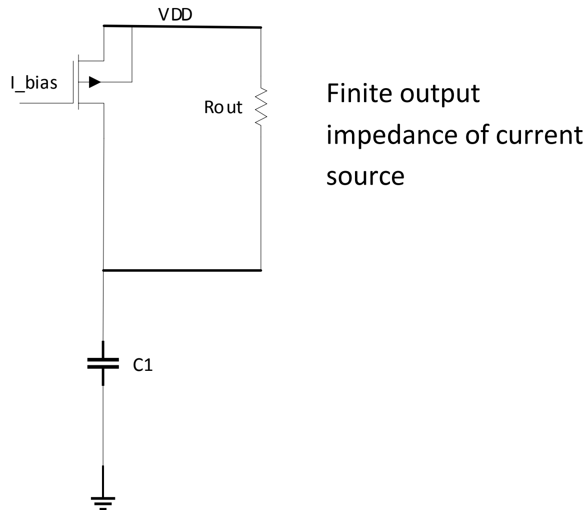

Figure 3.3: Constant current based capacitor charging

However, targeting a linearity of ~ 13 bits is challenging and the finite output impedance (channel length modulation effect) of the PMOS device limits the linearity. Instead of a linear rise, an exponential settling is obtained (typical of first order RC systems) as shown in Figure 3.4. The residue of this ramp function against a best-fit line is depicted in Figure 3.5.

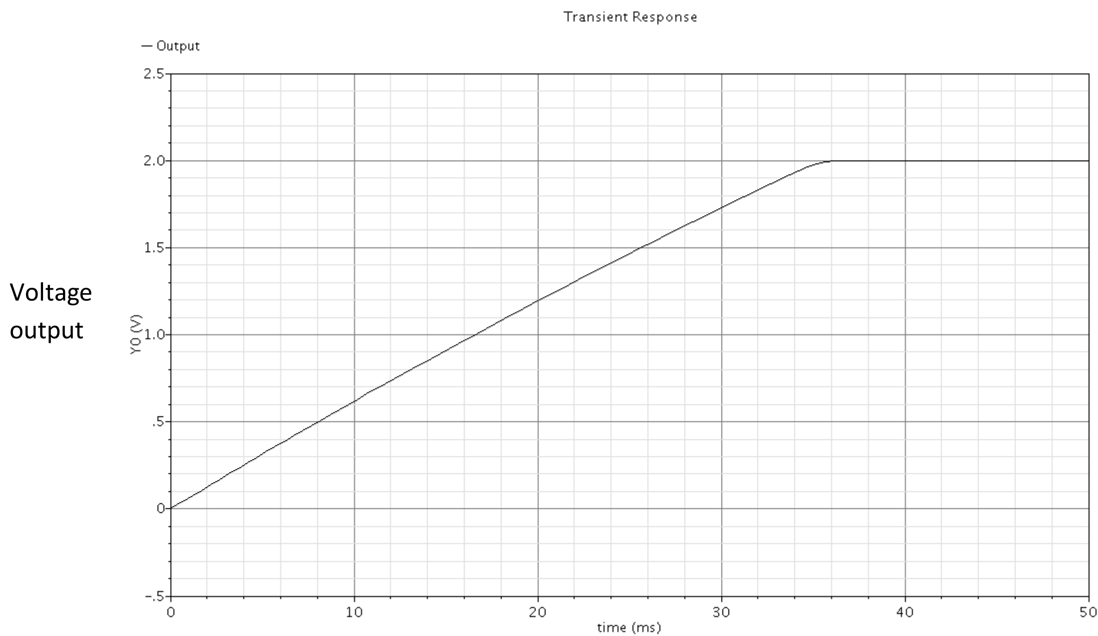

Figure 3.4: Exponential Non-linearity in the Ramp stimulus due to the finite output impedance

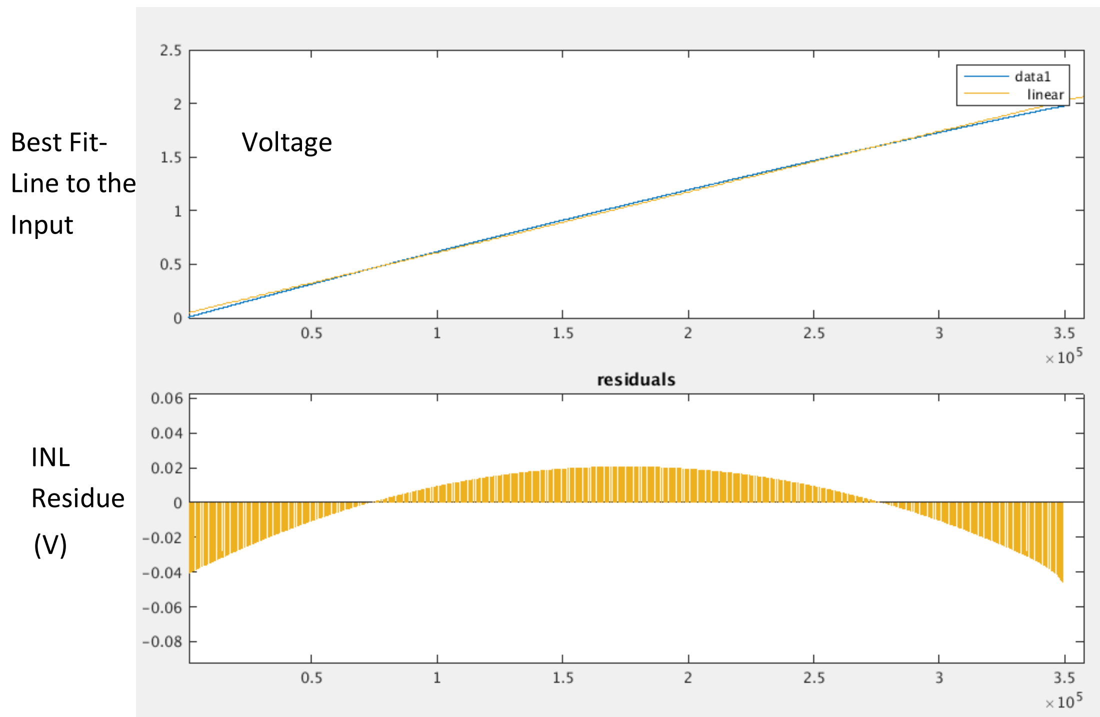

Figure 3.5: Best-fit Line to the exponential ramp yields a max INL of the order of 40mV (~ 6bits of linearity for 2V Full Scale)

As an alternative, consider a cascoded current source as shown in Figure 3.6. The drain of the current source node is now shielded from the output voltage changes and thus presents a constant current for the charging. However, this is true only as long as the cascode device remains in the saturation region. As device M2 gets squished out into the linear region, node VX tracks the output and the current value varies. Thus, the voltage ramp is limited in its voltage swing (to about a threshold voltage over the gate voltage of M2) and the linearity is not preserved over the entire range till 1.7V.

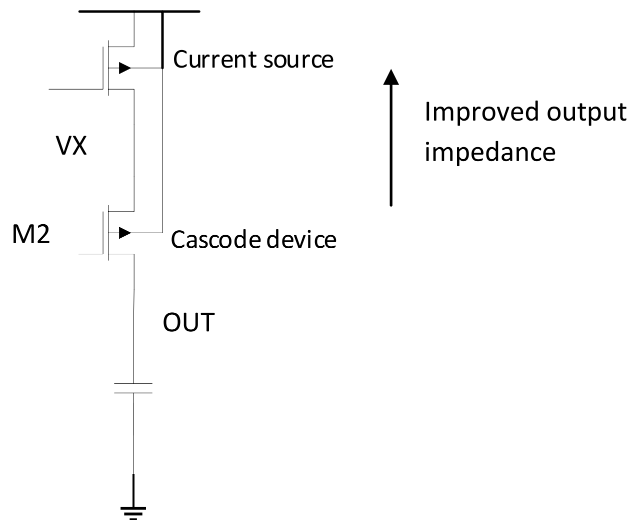

Figure 3.6: Cascoded Current Source charging

To ensure that the current source drain remains constant throughout the ramp range, an operational transconductance amplifier (OTA) based charging scheme, proposed in [9] is considered in this work. The capacitor to be charged forms the feedback network of the OTA (Figure 3.7). In the ideal case, the capacitor node VX is thus held at the common mode potential and the input current into the node generates an inverted ramping function at the output. Even though the PMOS current source presents finite output impedance, the current flowing into the feedback capacitor remains constant throughout the OTA's region of operation.

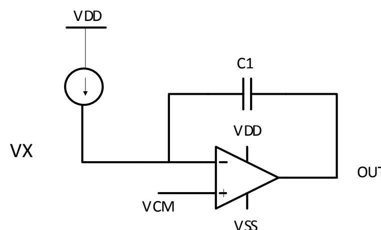

Figure 3.7: Ramp Generation using OTA based capacitor feedback

3.6.1. OTA open loop gain

The specification of the open loop gain "*A*" of the OTA is set based on the linearity requirement of the ramp. The PMOS current source (with its associated finite output impedance) may be represented in the form of its 'Thevenin' equivalent circuit as a voltage source of value 'IR_{out}' and a series impedance of R_{out} (Figure 3.8).

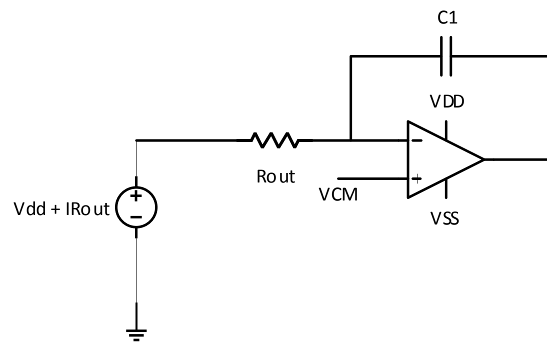

Figure 3.8: Thevenin Equivalent of the finite current source

In the presence of a finite op amp gain, the response to a step input current (other bias parameters such as VDD and VCM assumed to be constant and pre-set) is represented in the Laplace domain as:

$$\left(I.R_{out} + \frac{V_{out}}{A}\right) = \left(-V_{out} - \frac{V_{out}}{A}\right) sC.R_{out}$$

$$V_{out}(s) = -R_{out}.A.\frac{I(s)}{1 + (A+1)s.C.R_{out}}$$

Substituting I(s) = I_0(s)/s for a step input and taking the inverse Laplace transform, we have:

$$V_{out}(t) = I_o R_{out} A \, (1 - e^{-\frac{t}{\tau}}) \tag{3.4}$$

where τ = (A+1)R_{out}.C

Using a Taylor series expansion of $e^{-t/\tau}$,

$$V_{out}(t) = I_o . R_{out} A \, (\frac{t}{\tau} - \frac{1}{2!}(\frac{t}{\tau})^2 + \frac{1}{3!}(\frac{t}{\tau})^3 + \cdots) \tag{3.5}$$

Clearly, there are non-linear higher order terms in the expression for $V_{out}(t)$. However, with the OTA arrangement, the time constant τ of the system is greatly increased by a factor of the open loop gain "*A*". A conservative design choice for the gain should ensure that the higher order terms remain smaller than the overall resolution (smaller than 1 LSB). For the second order term, this constraint may be expressed as:

$$((I_o R_{out} A)/2) . \left(\frac{t}{\tau}\right)^2 < \Delta \tag{3.6}$$

For the ramping time of 60ms, a rough capacitor value of 10pF and R_{out} of 10GΩ (based on technology characterization of the impedance for a ~nA current source), the gain requirement comes to be in excess of 70dB. Satisfying the second order term ensures that the other higher order terms may also be neglected.

If enough gain > 70dB is provided, the expression for V_{out} reduces to the familiar first order linear ramp function:

$$V_{out}(t) = (I_o R_{out} A.t)/((A+1)R_{out} C) = \boldsymbol{I_o.At/(A+1)C} \tag{3.7}$$

Though the gain "A" may be large enough to ensure that the higher order non-linear terms may be neglected, it still results in a finite slope (or gain error). While such a finite gain error does not lead to non-linearity, the constancy of such the gain 'A' across the entire swing of 0.3 – 1.7V may not be easily achieved. The effect of the gain variation becomes pronounced in the form of static settling errors arising during the transient recovery from sampling kickbacks. Rather, the preferred design choice is to provide a sufficiently high gain for the OTA so that even with PVT variations, the resulting static errors stay within the bounds of the desired resolution. In other words, if the integrator's voltage output settles to within the desired resolution at the end of each sampling period, the overall linearity would be preserved. In this work, to achieve a linearity of > 13 bits ($\Delta = 2/2^{13}$), the tolerable static errors is set to $\Delta/2$.

$$Loop\ gain = \frac{Full\ Scale}{static\ error} = 2^{14} = 16384 = 84dB \tag{3.8}$$

3.6.2. OTA Bandwidth Requirements

The OTA acts as a buffer stage to the following sampling stages of the SAR ADC. These sampling stages introduce significant transient kickback effects at the buffer output. These voltage excursions may come from charge injection and/or clock feedthrough during the turn/off of the sampling switches.

The bandwidth of the OTA must be sufficiently high enough to ensure that these transients settle within the ADC sampling time. For an allocated 50ns of sampling time for the 10MHz ADC operation, the UGB of the OTA must provide for settling within this duration.

Indeed, settling errors for a first order system would not introduce non-linearity or distortions at the output – It would manifest only as a constant gain error. However, in the presence of non-dominant poles and stray parasitics in a practical implementation, it is difficult to guarantee a first order behavior across various operating conditions. Further, a finite bandwidth would also raise the sensitivity of the settling errors to the sampling clock instants (clock jitter). In consideration of these aspects, it is conservatively chosen to have a sufficiently high bandwidth for dynamic settling.

3.6.3. Input Swing

For the feedback based charging scheme, OTA input node is always held at the common mode voltage of 1V. This greatly reduces the input common mode range requirement. From an implementation perspective, this simplifies the input stage design – which may be realized as a single PMOS/NMOS differential pair.

3.6.4. Output swing

The ramp stimulus is sought to test the ADC for 70% of its code range from 0.3V to 1.7V. This requires the driving buffers (ramp generator OTA and the differential ramp generator OTA) have a loop gain in excess of 84 dB over this entire range.

3.7. Differential ramp generation

This section discusses the architectural considerations for the generation of the rising ramp counterpart (in order to have differential inputs to the ADC).

The most straightforward implementation for the differential ramp would be to have a similar charging scheme with an OTA based current sink (based out of an NMOS current source). However, this design would again require a charging capacitor (of the same value as that of the single ended case discussed). From a BIST implementation perspective, this is not preferred due to the area overhead associated with the additional capacitor.

Another consideration was to have a single ended to differential conversion (for the single ended falling ramp at the integrator output) using a fully differential OTA. This would require the differential OTA to be configured in a pseudo-differential mode with one of its inputs to be the lower supply rail (VSS) or the common mode (V_{CM}). The drawback with this approach is that the OTA input terminals now see a signal dependent term – which could lead to modulation of the input itself and potentially cause signal distortion.

Instead, we choose an OTA based regulation scheme to generate the differential ramp in this work. The OTA 2 shown in Figure 3.9 is configured as an inverting amplifier with the integrator ramp output as its input. For an ideal OTA and with appropriately set initial conditions, this OTA generates an inverted ramp at its output (V^{out-}) such that the common mode of the two ramps remains at the set value of 1V. The following section analyses the dynamic equations involved in the differential operation.

At the end of the transient settling in the sampling phase, let the integrator output be V^{out+} ; the OTA 2 output be V^{out-} and the negative terminal be represented as V_y. Also, it is assumed that the integrator output, OTA 2 output and node V_y are pre-set initially to VDD, VSS and V_{cm} respectively. By charge conservation,

$$C1(V_{CM} - VDD) + C2(V_{CM} - VSS) = C1\left(V_y - V^{out+}\right) + C2(V_y - V^{out-})$$

For an infinite OTA gain, we have $V_y = V_{CM}$ and if C1 = C2;

$$V^{out-} = VDD - V^{out+} + VSS = 2.V_{CM} - V^{out+}$$

And the differential ramp input to the ADC is:

$$\boldsymbol{Vin, ADC = V^{out+} - V^{out-} = 2V^{out+} - 2.V_{CM}} \quad (3.9)$$

Note that since node Vy is held at V_{CM}, the parasitic capacitance associated with this node does not draw charge during the transient settling and thus does not affect the dynamics of the system.

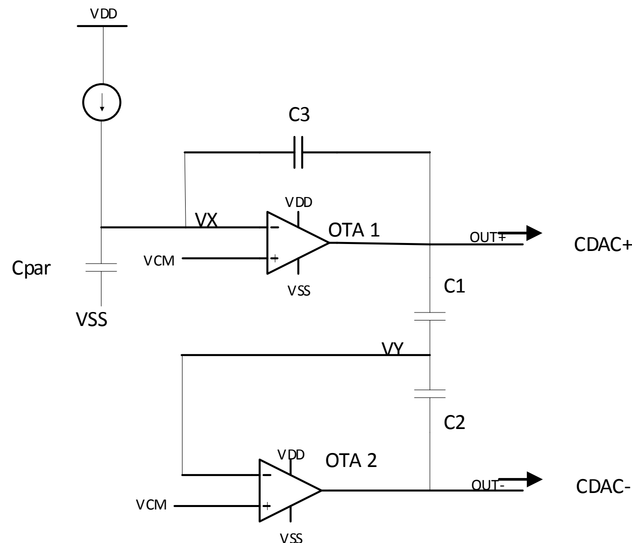

Figure 3.9: Differential Ramp Generation

3.7.1. Mismatch Effect

In practice, there could be a mismatch between the capacitors C1 and C2 that generates the common mode voltage at the OTA 2 input. The effect of the same would result in the rising ramp function V^{out-} to become:

$$V^{out-} = \frac{C1}{C2}.(VDD - V^{out+}) + VSS$$

The differential voltage to the SAR ADC thus may be given as:

$$\boldsymbol{Vin, ADC = V^{out+} - V^{out-} = \frac{C2 + C1}{C2}.V^{out+} - \frac{C1}{C2}.VDD - VSS} \quad (3.10)$$

Clearly thus, mismatch between the capacitors results only in a finite gain error (and an offset in the common mode) in the differential voltage to the ADC and no distortions. Therefore, matching of the capacitors is not as much of a concern for this application.

3.7.2. Finite Gain of OTA 2

The practical implication of a finite gain "*A*" for OTA 2 (for C1 = C2 = C) results in V^{out-} to be expressed as:

$$\boldsymbol{V^{out-} = \left(\frac{A}{A+2}\right).(VDD - V^{out+}) + \left(\frac{A}{A+2}\right).VSS}$$

$$\boldsymbol{= \left(\frac{A}{A+2}\right).2V_{CM} - \left(\frac{A}{A+2}\right).V^{out+}} \quad (3.11)$$

Even though it again only results in a gain error, the constancy of the finite gain "A" across the entire voltage output range may not be guaranteed – and thus as a conservative design choice, we specify the gain specification for the OTA to be as high as the required resolution.

Thus, for the chosen architecture, OTA 2 generating the differential ramp sees an effective feedback factor $\beta = 0.5$. This requires that the OTA 2 open loop gain then be 6dB higher (than the requirement for OTA 1) at **90dB**.

3.7.3. Initialization of DC operating points

The dynamic charging of the capacitors requires that the initial operating conditions be appropriately set. This is accomplished by an initialization phase *'start'* upfront. In this phase, the integrator (OTA 1) virtual ground V_X is pulled down to VSS (Figure 3.10) – resulting in the integrator output being pulled up to VDD. Further, the capacitors C1 and C2 are pre-charged to set the node V_Y to the common mode voltage (1 V). With the OTA 2 feedback loop broken, the total charge stored at node V_Y is given by:

$$Q, start = C1.(V_{CM} - VDD) + C2.(V_{CM} - VSS) \qquad (3.12)$$

In the next phase (*start'*), the current source charges up the node V_X – until OTA 1 comes out of the slewing region and enters the active amplification mode. Subsequently, with the node V_X held at V_{CM}, the current discharges the integrator output to yield the falling ramp signal.

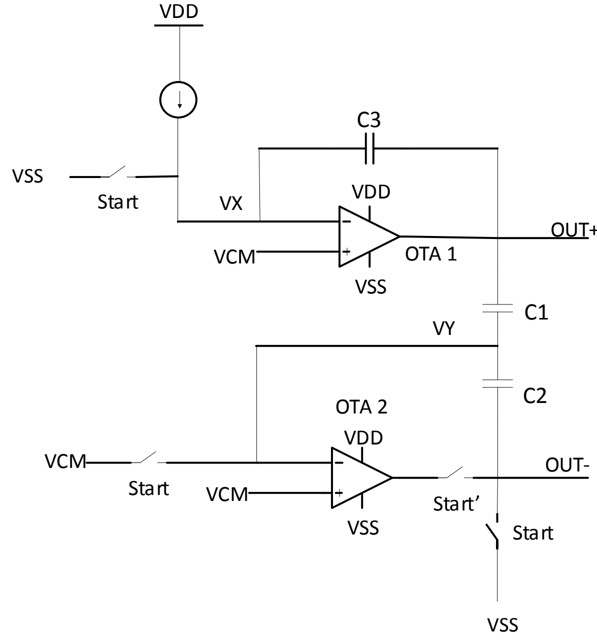

Figure 3.10: Initializing the Capacitor Nodes for the dynamic charging/discharging

For OTA 2 (with gain 'A' and a common mode output of $V_{out,cm}$ at the end of *start*), the node voltages at the beginning of *start'* may be obtained by charge conservation as:

$$Q, start' = C1.\left(V_{CM} - (V_{out-}/A) - VDD + (V_{out,cm}/A)\right)$$
$$+ C2.\left(V_{CM} - (V_{out-}/A) - V_{out-} + (V_{out,cm}/A)\right)$$
$$= C1.(V_{CM} - VDD) + C2.(V_{CM} - VSS) \quad (3.13)$$

For C1 = C2, this yields $V_{out-} = \left(\frac{A}{A+2}\right).VSS + (\frac{2}{A+2}).V_{out,cm}$. Thus, the node OUT- remains close to the lower rail VSS (for a high gain A) and begins to ramp up once VX charges to VCM.

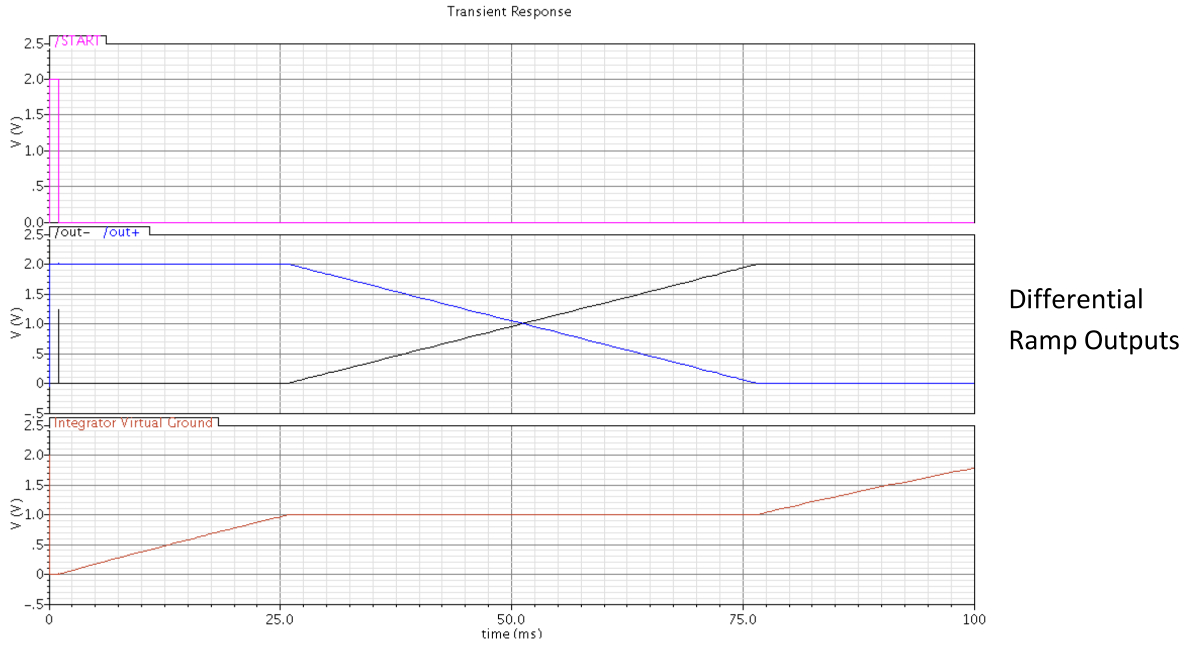

Figure 3.11: The initialization of the capacitor charging dynamics a) 'Start' signal presets the nodes b) Capacitor charging/discharge follows based on charge conservation

3.7.4. Small-Signal Loading Conditions - OTA

The frequency response of the OTA is critical during the sampling period of the ADC. This is to ensure that the ramp linearity is preserved at the OTA outputs and that all spurious transient effects are regulated. From a design perspective, the dynamic performance of the OTA is largely governed by its loading conditions - this section quantifies the same from a systems' perspective.

During the sampling, the effective load capacitance for the OTAs is given by (Refer to Figure 3.9 for notations):

$$OTA1\ C_{LTot} = C_{DAC+} + \left(C1 \| C2 \| C_{DAC-}\right) + \left(C_{par} \| C3\right) \quad (3.14)$$

$$OTA2\ C_{LTot} = (C1 \| C2) + C_{DAC-} \quad (3.15)$$

Any additional explicit load capacitor would appear in parallel to the above estimate.

And the effective feedback factors are $\beta_{OTA1} \cong 1$; $\beta_{OTA2} \cong 0.5$.

3.8. Ramp Offset Generation

For a SAR ADC, the offset may be conveniently generated in the DAC array itself by the addition of a dummy offset capacitor 'C_p'. The modified DAC array is shown in Figure 3.12 for a single ended case [6].

In the normal mode of operation, this offset capacitor is always connected to negative supply rail, $Vref_{,n}$ (during sampling and conversion cycles). The SAR algorithm continues as normal and the effect of this offset capacitor is the same as that of any parasitic capacitance at the input of the comparator. At the end of the conversion, the quantization error can be represented in terms of the bit decisions D(i) as:

$$V, error = -\frac{C_{total}}{C_p + C_{total}}.V_{in} + \frac{\sum_{i=0}^{n-1} D(i)C_i.Vref}{C_p + C_{total}}. \tag{3.16}$$

where C_{total} is the sum of the other DAC capacitances.

And the quantized output is given by:

$$\hat{V} = \frac{\sum_{i=0}^{n-1} D(i)C_i.Vref}{C_{total}} \tag{3.17}$$

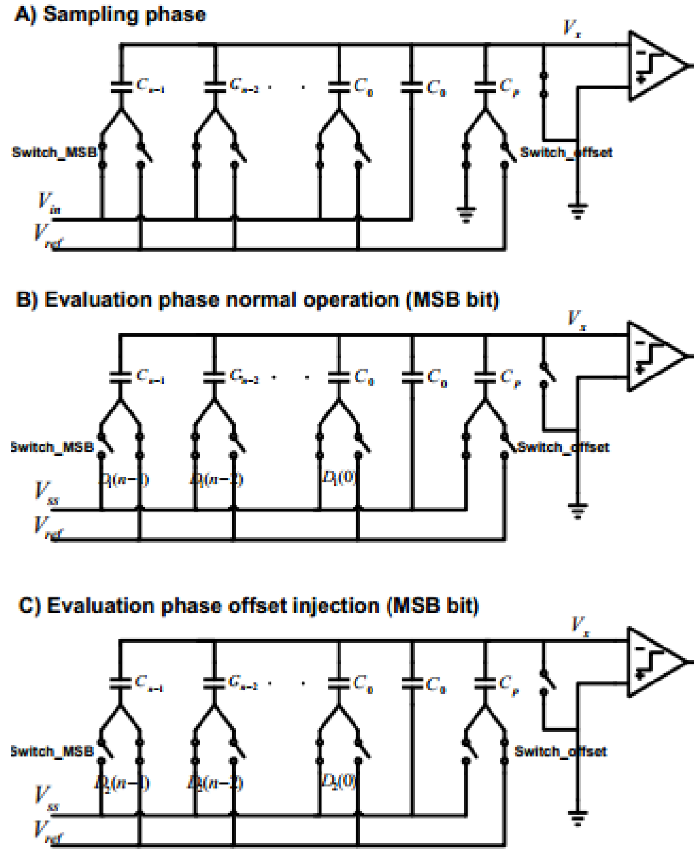

Figure 3.12: Offset Injection Using an Extra DAC Capacitor [6]

In the offset injected ramp, the offset capacitor is switched to $Vref_{,p}$ (positive supply rail) during the conversion phase. In the sampling phase though, it remains pulled down to $Vref_{,n}$ (negative supply rail). As a result, the voltage on the comparator input sees a constant offset of the order of C_p/C_{total}. The quantization error after n cycles is now given by:

$$V, error = -\frac{C_{total}}{C_p + C_{total}} . V_{in} + \frac{\left(\sum_{i=0}^{n-1} D(i)C_i + C_p\right) . Vref}{C_p + C_{total}} . \quad (3.18)$$

And the quantized output with the injected offset is:

$$\hat{V} = \frac{\sum_{i=0}^{n-1} D(i)C_i . Vref}{C_{total}} + \frac{C_p . Vref}{C_{total}} \quad (3.19)$$

For a differential SAR ADC implementation, the offset generation is realized by differentially switching the offset capacitor to opposite voltage reference levels during the conversion phase of the offset ramp cycle. In other words, if the offset capacitor on the positive side is set to $Vref_{,n}$ throughout, the negative counterpart is pulled up to $Vref_{,p}$ during the evaluation phase – resulting in an offset of the same order as the single ended case described above (C_p/C_{total}).

Chapter 4: Front-end Schematic Design

4.1. Current Reference block

In the previous section, it was derived that the requirement on the current reference comes out to in the sub-nA range for the targeted ramp rate. In this section, the current reference architecture to realize this has been presented.

In the most basic sense, a current reference would be obtained from the potential drop of a voltage reference across a resistor. We consider a V_{bg}/R (derived out of a bandgap voltage),V_{th}/R (MOS threshold voltage drop over a resistor) and a PTAT (thermal voltage based) implementation. To obtain a sub-nA current reference out of the above voltage references, the associated resistor values are summarized in Table 4.1.

Table 4.1: Current Reference Block Topologies

Current Reference	**Resistor Value for 1nA**
V_{bg}/R	1120MΩ
V_T/R	26MΩ
V_{th}/R	500MΩ (for V_{th} ~ 500mV)

With an objective to have an area optimized BIST implementation and thus smaller resistor values, the V_T/R reference is considered for this work. Indeed, the core design of this V_T/R (PTAT) core is based out of a bandgap reference – the only functional circuit addition for the bandgap being the appropriate summing of the PTAT and the CTAT voltages.

For the given application of test and calibration, the temperature dependence of this PTAT current is not of a concern. It may be safe to assume that the temperature remains

fairly constant during a given ramping cycle. Further, the absolute temperature itself would only manifest in subtle slope changes of the ramp (shown later with the results).

A conventional PTAT reference based on a supply independent biasing scheme is shown in Figure 4.1. We use this as a starting point to present a brief review of the circuit operation. Principally, a thermal voltage reference is obtained from the difference in the base-to-emitter (ΔV_{BE}) voltage of two differently sized identical bipolar junction transistors (BJTs). In the CMOS process, BJTs may be realized as MOS devices operating in the sub-threshold regime.

The Current-Voltage (I-V) characteristics of the MOS device in sub-threshold may be given as:

$$I = I_s . e^{\frac{V_{gs} - V_{th}}{V_T . \eta}} \tag{4.1}$$

Where $\boldsymbol{\eta}$ is the subthreshold factor (~1.4) associated with a MOS device (proportional to the ratio of the depletion and oxide capacitance), $\mathbf{V_t}$ is the thermal voltage and $\mathbf{V_{gs}}$ is the gate-to-source voltage of the MOS device and $\mathbf{I_s}$ is the saturation current (a function of the device dimensions).

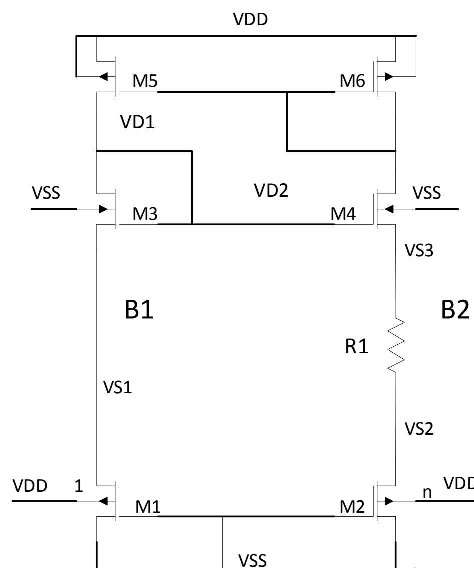

Figure 4.1: Conventional supply independent biasing based PTAT reference

Given ideal operating conditions, the currents in the two branches B1 and B2 are equal for the shared bias voltage for the PMOS loads. The two MOS devices (essentially BJTs) are sized in the ratio of 1:n. Subsequently, the current in the two legs B1 and B2 may be given as:

$$I = I_{s1}.e^{\frac{-V_{s1}-V_{th}}{V_T.\eta}} \tag{4.2}$$

and

$$I = I_{s2}.e^{\frac{-V_{s2}-V_{th}}{V_T.\eta}} \tag{4.3}$$

For a device sizing of the ratio of 1:n, $I_{s2} = n.I_{s1}$ and we have:

$$Vs1 - Vs2 = V_T.ln(n).\eta \tag{4.4}$$

For equal currents through the two legs, we also have $V_{s1} = V_{s3}$, as the identical devices M3 and M4 must have the same overdrive voltage. The current through each branch is given by

$$I = \frac{Vs3 - Vs2}{R} = \frac{V_T.ln(n).\eta}{R} \tag{4.5}$$

In practice, however, channel-length modulation effect causes unequal currents to flow through the two branches. This is due to the drain-to-source voltage mismatch of the PMOS loads MX and MY resulting from the biasing scheme. For a low current, the node VD2 would be typically pulled up close to one threshold drop below VDD, while node VD1 is set at a couple of overdrive voltages from VSS.

A more precise reference may be obtained by replicating one of the branches B1 [10]. As shown in Figure 4.2, instead of having M4 to be diode connected, the drain of M4 biases the NMOS M6. The current set-up in the branch B3 is then mirrored back to the main legs B1 and B2. Indeed, the channel-length modulation mismatch shows up in the currents of B2 and B3 – however, a much better current matching between B2 and B1 is obtained.

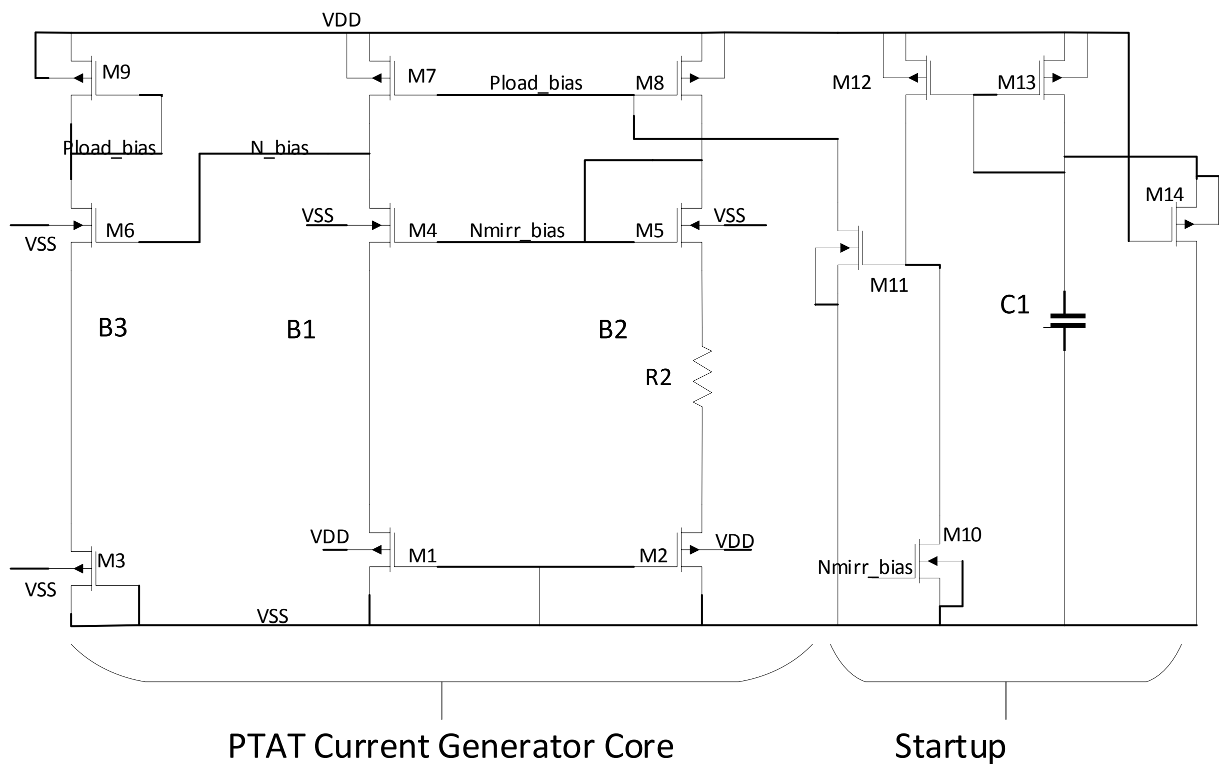

Figure 4.2: Proposed Current reference block – with start-up circuit

Figure 4.3 shows the schematic of the PTAT current generator core with the DC operating conditions (for the typical process corner). M1 and M2 have been sized appropriately for a sub- threshold mode of operation.

Figure 4.3: DC Operating points for the Current reference Core

The MOSFET devices M1 and M2 are sized in the ratio of 8:9. This yields a voltage difference across their source terminals as per Equation 4.5 as:

$$Vs1 - Vs2 = V_t . ln(n) . \eta \cong 4.3mV \; at \; 298K \;\; with \, \eta = 1.4 \qquad (4.6)$$

This is in close agreement the voltage difference of 4.18mV obtained from the DC simulation results.

.

The reference block needs a startup circuit during power-on to ensure that no degenerate DC conditions (zero quiescent current) are set. With the forced startup scheme shown, it is ensured that the nodes *'Pload_bias'* and *'Nmirr_bias'* do not settle around the supply rails of VDD and VSS respectively. As VDD is ramped up during power-on, the current charging the capacitor C1 is mirrored through M12 to turn on M11. This pulls down the node *'Pload_bias'*

and initiates flow of current through the core. When the circuit settles to the ideal operating condition, M10 turns on and shuts off the device M11. Subsequently thus, the startup circuit does not affect the PTAT current generation. M14 provides a path for the discharge of the charge on C1 during power down.

4.2. Operational Transconductance Amplifier

For convenience, it is sought to share the same OTA block for both the integrator and the differential ramp generator (OTA 1 and OTA 2 in Figure 3.9). Thus, the architecture and performance of the OTA is made sure to meet the specifications for both the blocks.

The topology is primarily chosen based on the gain and the output swing. A high gain requirement in excess of 90dB may be met by a cascode amplifier stage with a high output impedance. However, such a gain stage has limited headroom at the output due to the overdrive voltage drops across the cascode devices. This calls for a two stage amplifier design – where the first stage provides for most of the gain and the second stage gives the desired swing.

We consider a class AB transconductance output stage (push-pull inverter) in the 180nm process using 3V MOS devices. The following figure 4.4 is the voltage transfer characteristic (VTC) for the same. Shown alongside is the small signal voltage gain from the input to the output (derivative of the VTC curve). Clearly, an output swing from 0.2V to 1.8V is achieved for a nominally low input range of 1.04V-1.088 V. However, the voltage gain degrades to 11dB at the extreme of 1.8V. This essentially imposes the gain of the first stage to be as high as 80dB – which can be achieved easily achieved for the relaxed swing.

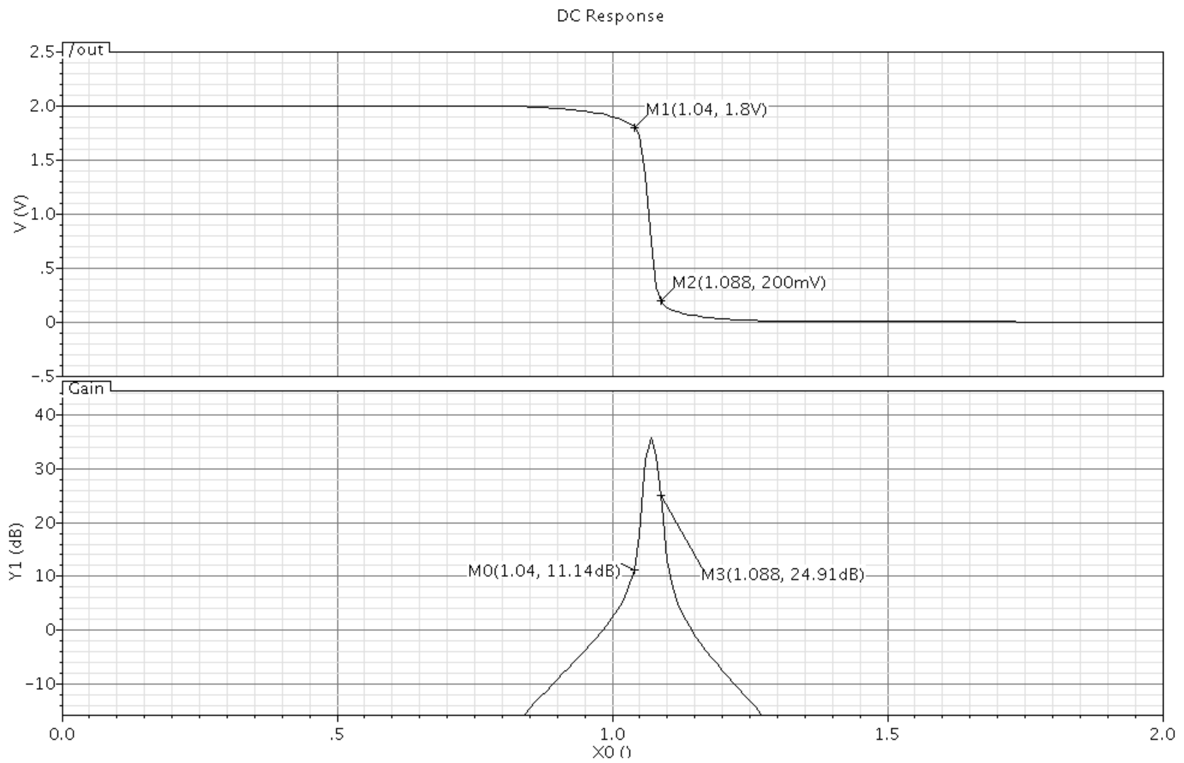

Figure 4.4: a) Voltage Transfer Characteristic (Output vs Input) for a class AB stage b) Gain variation across the input range

The first stage may be realized as a telescopic cascode with a gain of the order of $(g_m r_o)^2/2$. A relaxed input swing requirement rules out the design choice of a folded cascode topology. A telescopic stage (with a typical intrinsic device gain of ~165 for a channel length of 1um) provides adequately for the desired overall gain specification. The output swing of the telescopic amplifier (Figure 4.5) roughly lies in the range

$$3Vov,n \ < \ Vout < VDD - 2Vov,p \quad (4.7)$$

For the choice of a nominal overdrive voltage of 200mV, the first stage swing then lies between 0.6V – 1.6V. This is clearly well within the desired input range of the class AB second stage.

4.2.1. Frequency Compensation

Standard miller compensation scheme is used to provide for a stable frequency response for the two stage design. The compensation capacitor (C_c) between the stages is effectively amplified by the second stage gain (when referred to the first stage output) and forms the dominant pole of the system:

$$Dominant\ pole\ p1 = \frac{1}{R_{out\,1}.C_c.Gain_2}\ rad/s \tag{4.8}$$

where R_{out1} is the output impedance of the first stage; C_c is the compensation capacitor and $Gain_2$ represents the second stage gain.

However, this compensation scheme introduces a 'Right-Half-Plane' (RHP) zero which severely degrades the stability. The loop gain phase drops sharply around this zero while the magnitude function sees a slope increment. As a result, a highly unfavorable scenario for possible excess gain (>1) around 180 degrees shift is created.

$$RHP\ Zero \cong \frac{g_{m,second\ \ stage}}{C_c}\ rad/s \tag{4.9}$$

By adding a nulling resistor R_z in series to the compensation capacitor, the RHP zero is modified as:

$$RHP\ Zero, compensated \cong \frac{1}{C_c\left({g_{m,second\ \ stage}}^{-1} - R_z\right)}\ rad/s \tag{4.10}$$

The RHP zero may thus be pushed on to the LHP side by choosing $R_z > g_m$. Further, the output non-dominant pole may be suitably cancelled by making the zero coincide with the pole location.

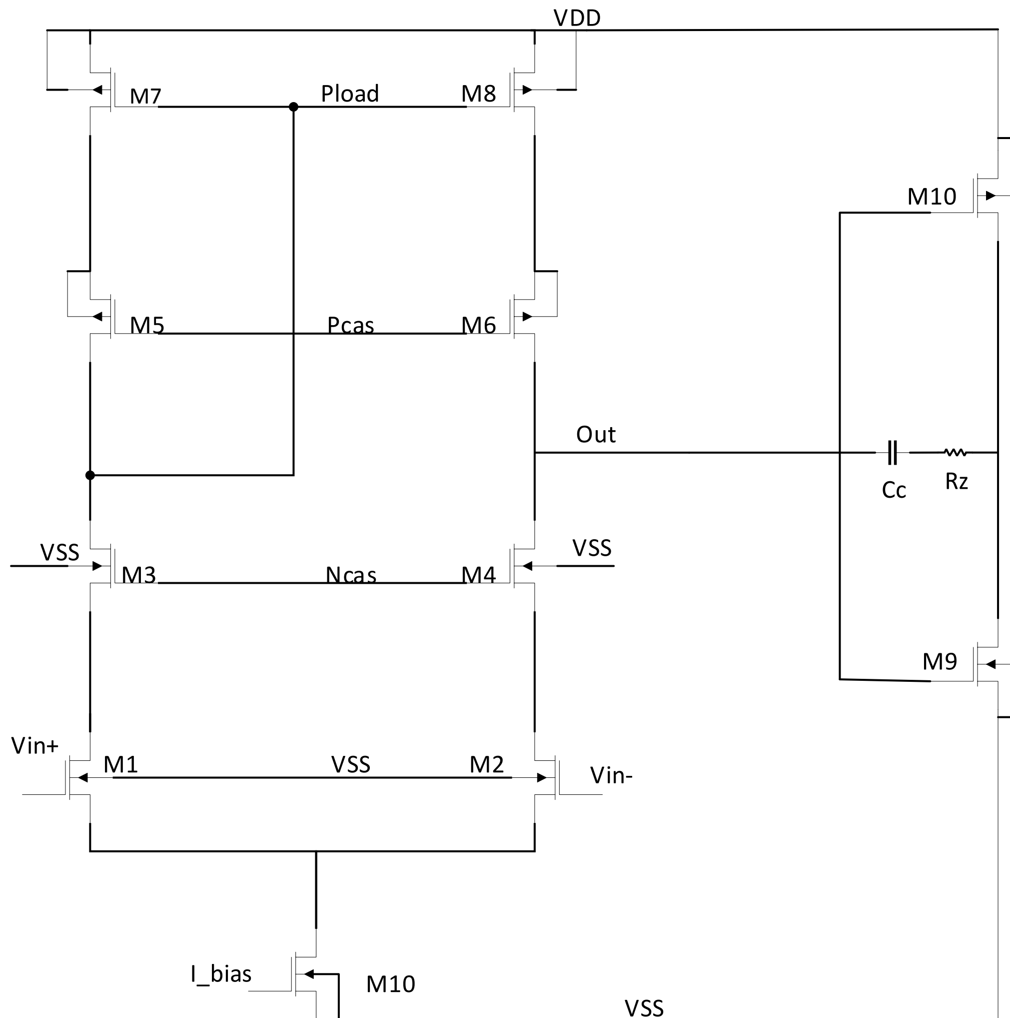

Figure 4.5: Two stage telescopic OTA with 'Miller compensation'

4.2.2. Design Methodology

In this section, the approach adopted for the choice of various OTA design parameters has been presented. The degrees of freedom in the design include the choice of the values of the compensation capacitor, the load capacitance, the bias currents and the device sizes. The

device length of the devices has already been chosen to be 1um – based on intrinsic gain requirements.

1. To begin with, a rough estimate for the values of C_c and C_l (compensation and load capacitance respectively) is made based on the noise budget for the integrator and the differential ramp generator OTA. As a conservative choice, the total integrated noise is sought to be comparable to the quantization noise power (equivalent to the SAR ENOB of ~ 13 bits) at 70uVrms. The total integrated noise at the output (assuming that the noise contributions of the first stage cascode devices are insignificant) is given by [11]:

$$v_{o.total}^2 \cong \frac{\gamma}{\beta}\frac{kT}{C_c}\left(1+\frac{g_{m1,load}}{g_{m,input}}\right)+\frac{kT}{C_{LTot}}(1+\gamma) \qquad (4.11)$$

where $g_{m1,input}$ is the transconductance of the input pair; $g_{m1,\,load}$ is the transconductance of the first stage PMOS load; Cc is the compensation capacitor and C_{LTot} is the total load capacitance.

2. Assuming a largely first order system response till the zero crossing of the loop gain, the UGB of the amplifier is given by in terms of input pair g_m as:

$$Crossover\ Frequency\ (Hz) = \frac{\beta . g_m}{2.pi.C_c} \qquad (4.12)$$

Knowing C_c and β, the required transconductance for the input differential pair is then computed. For this project, the bandwidth of the OTA is set to satisfy dynamic settling from sampling kickbacks within the sampling period of 50ns. As a conservative design choice, we budget 25ns for settling (so that both the integrator OTA1 and the differential ramp generator

OTA2 individually recover within 50ns). For a settling to a tolerance level of Δ/2 within 25ns, the required crossover frequency thus is:

$$Crossover\ Frequency, Hz\ (UGB) = \frac{ln(2^{N+1})}{\beta.2.pi.T_s} \quad (4.13)$$

where N is the bit resolution desired (13 in our case); β is the feedback factor (0.5 for OTA 2) and Ts is the settling time allocated (25ns). The UGB specification then comes out to be around **121 MHz** (with β = 0.5 for OTA 2). For the integrator (OTA 1), **60 MHz** of UGB suffices.

3. Using the gm/Id technology charts, the required value for the bias current is computed for a nominal overdrive voltage of ~150mV. Subsequently, the device widths are appropriately set to meet these biasing conditions.

4. The second stage is designed such that the non-dominant output pole (given by its effective transconductance) lies at atleast twice the frequency of the zero crossover. This is to ensure that an appreciably high phase margin (targeted close to 60 deg) may be obtained. The non-dominant pole is approximately given by:

$$Non-dominant\ pole\ (second\ stage\ output) \cong \frac{g_{m,second\ \ stage}}{2.pi.C_{LTot}}\ rad/s \quad (4.14)$$

where $g_{m,second\ stage} = g_{m,p} + g_{m,n}$ (sum of the transconductances of the PMOS and NMOS pair of the class AB stage) and C_{Ltot} is the load capacitance.

5. The nulling resistor is then chosen so as to roughly cancel out the non-dominant pole. (as brought out in the previous section).

The optimization phase involved iterating through the above steps to ensure that all the desired specifications are achieved across PVT. The only distinction made between the integrator (OTA 1) and OTA 2 comes from the respective β factor (1 and 0.5 respectively) – resulting in different values for C_c as a part of the frequency compensation (for the two different UGBs). The final design parameters for the OTA are summarized in Table 4.2.

Table 4.2: OTA Design Parameters

Design Parameter	**Value**
Biasing Current (I_d)	1st stage – 400uA each diff pair ; 1.4mA (second stage)
Compensation Capacitor (C_c)	3.8pF (OTA 2) ; 7.6pF (OTA 1)
Effective Load capacitor (C_{LTot})	3pF (including SAR DAC array; feedback capacitances and explicit capacitors)
Input Pair $G_{m,input}/I_d$	12.6
Input Pair Sizing (W/L)	200um/1um
Nulling Resistor (R_z)	281Ω

4.3. Frequency Response Results

The post–layout simulation results (with RC extraction) for the frequency response of the OTAs under the dynamic loading conditions is presented. The simulation is carried out using

the ‘stb’ analysis option. The family of plots across Figure 4.6 to Figure 4.11 include variations arising from the process corners (for the resistor, capacitors and 3.3V MOS device), temperature variations (0 to 80C) and over the entire output swing range (from 300mV to 1.7V).

In these plots, the vertical and horizontal dashed lines indicate the targeted UGB (~ 61 MHZ based on the required bandwidth calculated) and the 0dB gain level. Please note that for the OTA 2 (with β = 0.5), the 6dB line is considered as the effective zero crossing (the feedback factor would shift the magnitude plot down by 6dB). The choice of plotting the loop gain with a feedback factor of 1 simplifies the simulation test-bench set-up in not having to explicitly set the DC operating points of the OTA (with a capacitor feedback).

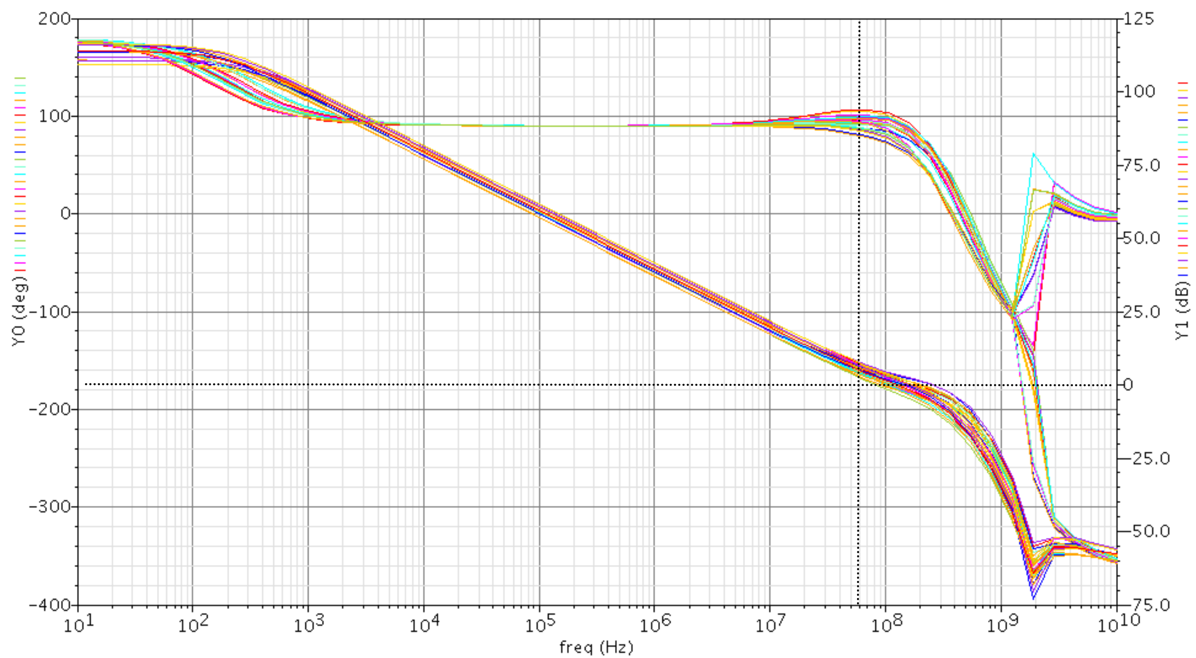

Figure 4.6: Magnitude and Phase plots of the loop gain for β = 1; Output Voltage at 1V

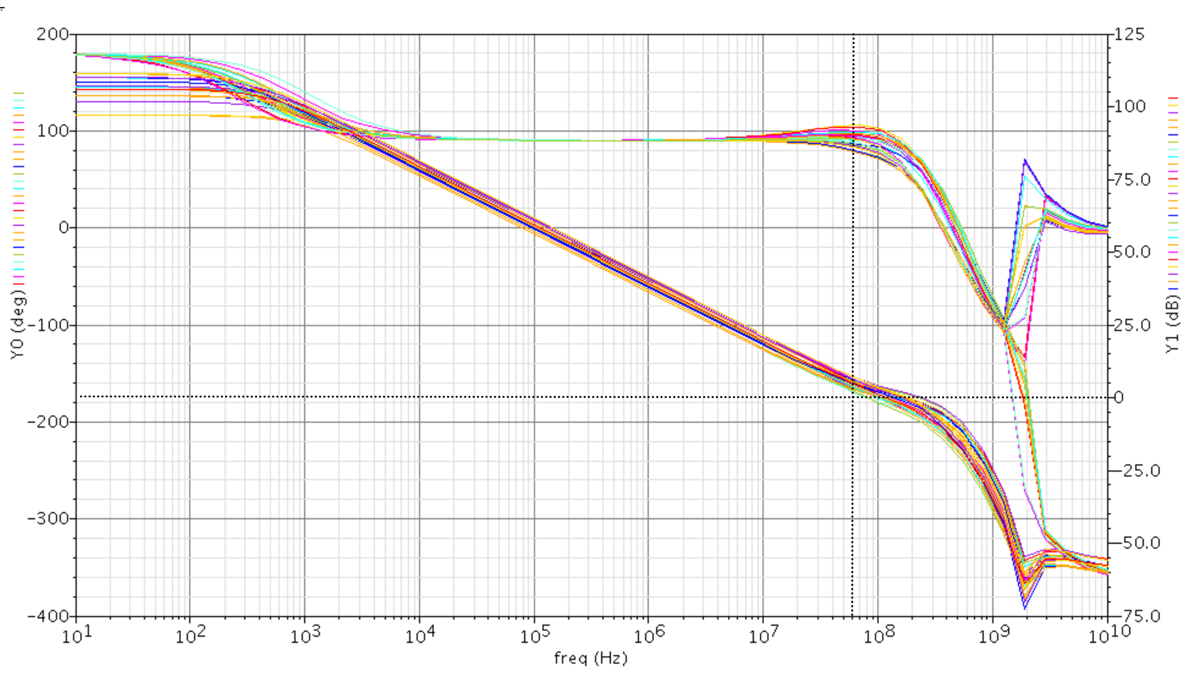

Figure 4.7: Magnitude and Phase plots of the loop gain for β = 1; Output Voltage at 300mV

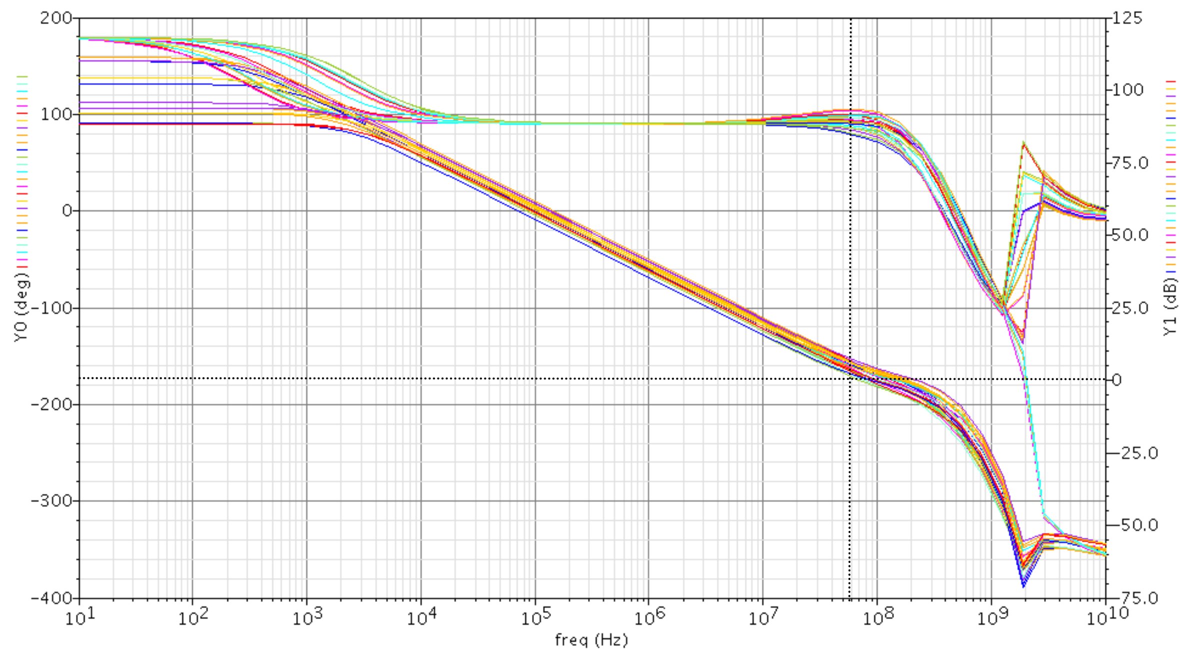

Figure 4.8: Magnitude and Phase plots of the loop gain for β = 1; Output Voltage at 1.7V

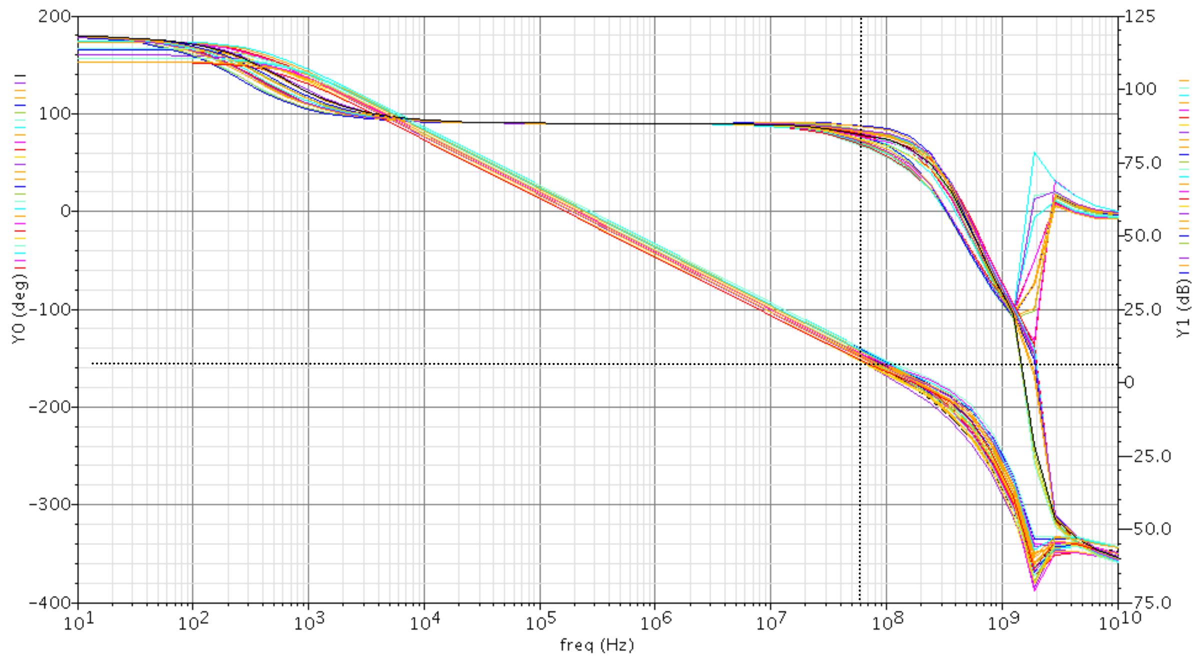

Figure 4.9: Magnitude and Phase plots of the loop gain for β = 0.5; Output Voltage at 1V

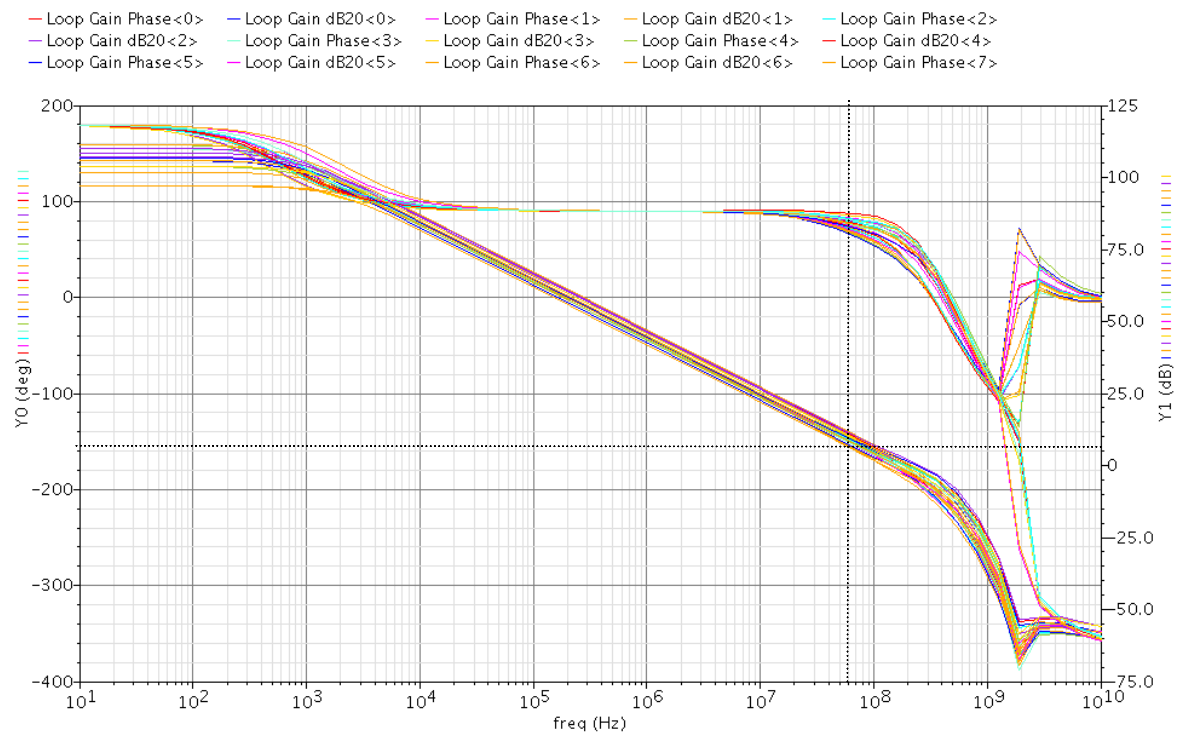

Figure 4.10: Magnitude and Phase plots of the loop gain for β = 0.5; Output Voltage at 300mV

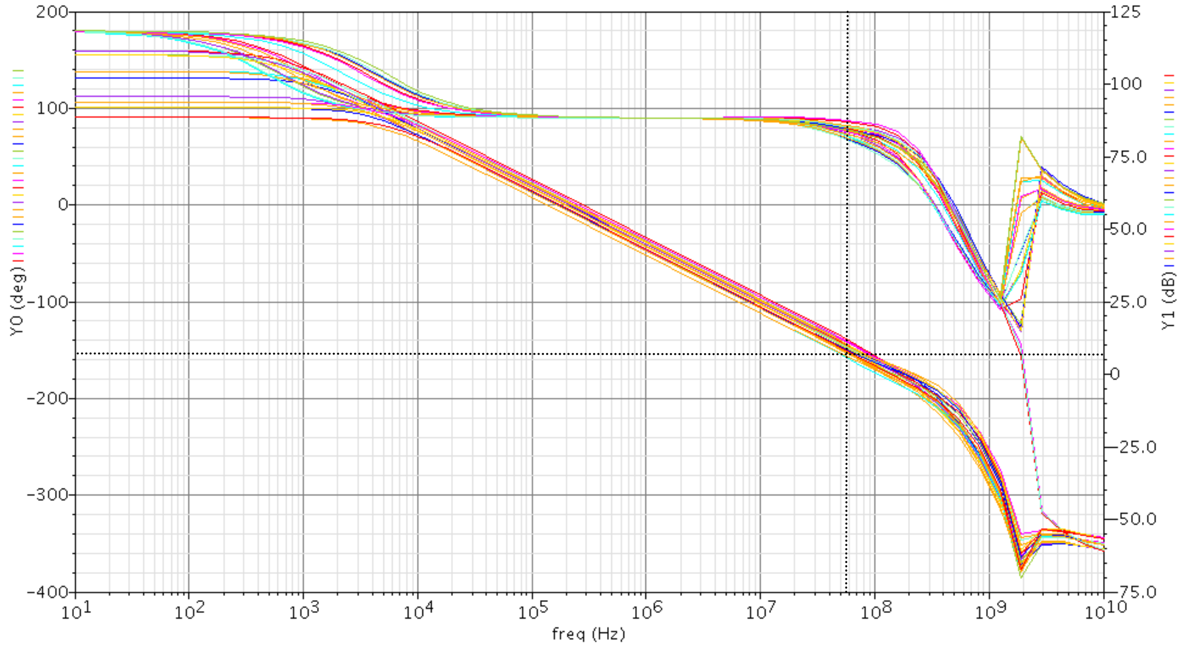

Figure 4.11: Magnitude and Phase plots of the loop gain for β = 0.5; Output Voltage at 1.7V

From the above plots, the frequency response performance (worst case) is summarized in Table 4.3 as:

Table 4.3: OTA Frequency Response Results

Metric	**Value**
Phase Margin	60 deg (OTA 1) ; 56 deg (OTA 2)
Unity Gain Bandwidth	68 MHZ (OTA 1) ; 55 MHZ (OTA 2)
Loop Gain	88 dB (OTA 1) ; 82 dB (OTA 2)

These worst case metrics are reported at the high temperature corner (80C) and for an output voltage swing around 1.7V. The results indicate a degradation of the performance of OTA 2 at this worst corner (falling short of the targeted specification in terms of the UGB and loop gain). The effect of the reduced loop gain and a reduced UGB would essentially contribute to setting errors from transient artifacts (both static and dynamic errors). However, this is not

much of a concern because of several factors. Firstly, the degradation is observed at an output voltage level of 1.7V. Practical SAR ADC inputs do not exercise the entire code range and so linearity testing for these codes is not as critical. Secondly, the gain requirement was derived for static errors resulting from full scale step input transients. Typically, the observed kickbacks are only in the range of 'millivolts' and so the static errors are not practically expected to be Δ/2 (half LSB). Thirdly, the specifications for the UGB and loop gain were to begin with highly conservative estimates. Given that the performance achieved for OTA 1 exceeds the targeted specification, the overall resolution for the differential operation (with twice the single ended LSB value) is still easily maintained. It can be easily understood that with 88 dB of gain for OTA 1 and in fact the whole sampling period of 50ns available for settling, the possible increase in settling errors for OTA 2 stand compensated.

4.4. Circuit Noise Contributions

This section discusses the potential sources of circuit noise and their impact on the BIST implementation. Simulation results for the designed front-end blocks have also been presented.

4.4.1. Noise Sources

For the chosen architecture, the major sources of circuit noise are given by:

1. Current Noise: The noise contributions from the active devices (thermal and flicker components) of the current reference block impacts the bias voltage of the MOS current source. Noise modulation of this node translates to a noise in the ideal current (with a factor g_m for the transconductance of the device) value flowing into the charging capacitor. In

addition, the MOS device acting as the current source also contributes a thermal noise component of the order of $4.k.T.\gamma.g_m$.

This total noise component in the current (say I_n) is integrated over the charging capacitor and appears at the output as:

$$Noise\ voltage\ v_n(t) = \int \frac{I_n(t)}{C}.dt \tag{4.15}$$

Analyzing in the frequency domain, we have

$$V_n(s) = \frac{I_n(s)}{s.C} \tag{4.16}$$

The inherent low pass filtering property associated with the integration operation significantly suppresses the high frequency components. On the other hand, the low frequency noise effects (the flicker noise contributions) appearing in the ramp output would be essentially modeled in the sinusoidal basis functions.

For the choice of parametrization using 30 harmonic coefficients, the noise contributions above around 300Hz would be of specific interest (corresponding to $1/15^{th}$ the time period of ramping) as they would lie beyond the scope of what can be potentially modeled. Any high frequency component over ~300Hz with a noise power of 1LSB would start to degrade the test measurement.

2. Driving stage Amplifier Noise: The contribution of an input-referred noise term $v_{n,ota1}(t)$ for the integrator at the output is:

$$Integrator\ Output, V_{out,ota1}(t) = v_{n,ota1}(t) - \frac{I.t}{C} \qquad (4.17)$$

Thus, the noise term appears directly at the output and rides over the ideal ramp.

For the differential ramp, the OTA 2 input noise $v_{n,ota2}(t)$ appears at the output with an amplification of a factor of 2 (for $\beta = 0.5$).

$$OTA\ 2\ Output\ Noise, Vn_{out,ota2}(t) = 2.v_{n,ota2}(t) \qquad (4.18)$$

4.4.2. Noise Results

The total integrated noise of the OTAs for a noise-bandwidth of 100MHz (~10 times the sampling frequency) is summarized in Table 4.4.

Table 4.4: OTA Output Noise (with $\beta = 1$)

Block	**Output Noise Power (σ)**
OTA 1	29 uV_{rms}
OTA 2	32 uV_{rms}

Thus, the noise contributions from the OTAs are within the desired bounds (less than the budgeted 1LSB) and so should not impact the accuracy of the SEIR algorithm.

For the current reference block, the noise spectrum beyond 300Hz is shown in Figure 4.12:

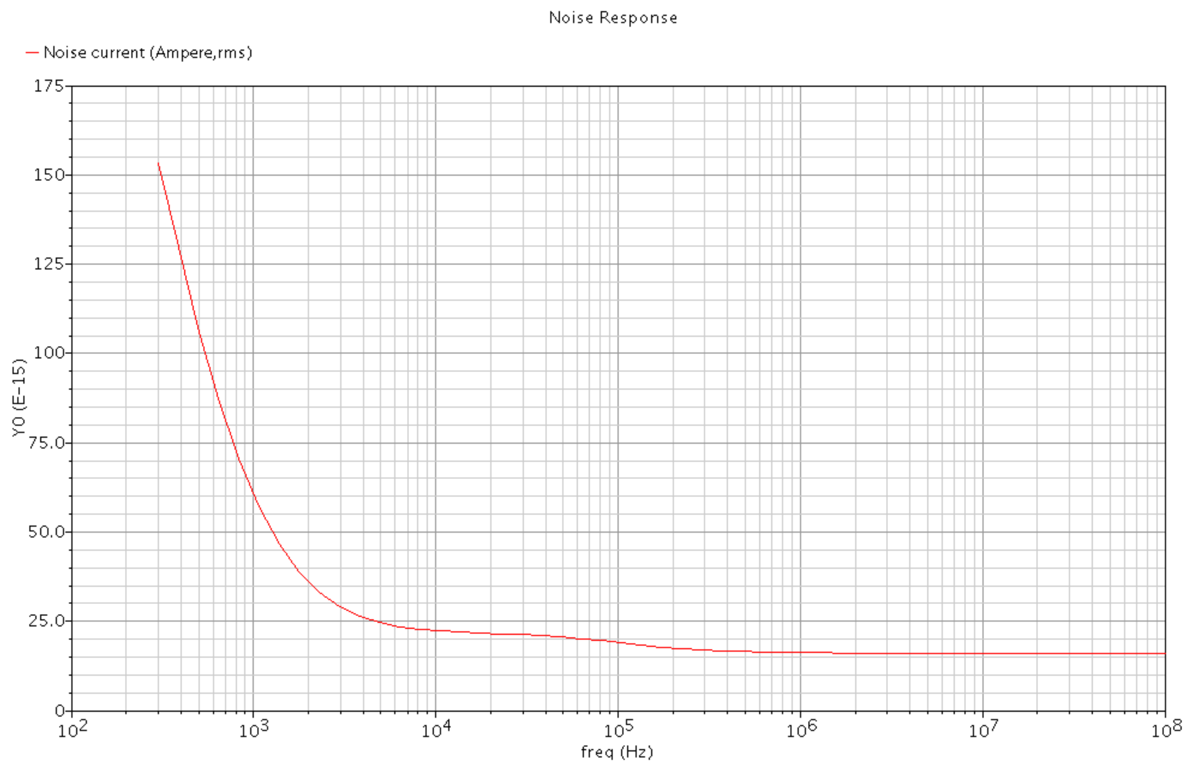

Figure 4.12: Current noise spectrum from 300Hz to 100MHz (unmodeled contributions)

From the above plot, the simulated noise power at 300 Hz is about 150fA, rms. The corresponding integrated noise power at the output is:

$$V_n(300Hz) = \frac{150fA}{(2.pi.300).14pF} \cong 6uV, rms \tag{4.19}$$

Clearly, the noise voltage Likewise, for higher frequencies, noise contribution is negligibly small compared to the system resolution and therefore is not of a concern.

Effect of low frequency Flicker Noise on the Ramp: This section analyses the low frequency noise effects on the SEIR algorithm and justifies the adoption of an interleaved approach for the testing using the two offset separated signals.

The effect of low frequency noise components originating from the front-end current reference and driving buffer stages manifests in the form of gain errors (resulting in different ramp slopes) and also subtle changes in the input non-linearities itself (Figure 4.13). This would severely affect the SEIR algorithm if the offset ramp is separately generated as a part of a different measurement run. The very premise of the functional relation (allowing for the use of the same basis functions) for the offset ramps becomes invalid and the LS fit results would no longer hold significance. Instead, if interleaving is used, the two offset signals are sampled from the same measurement run – which essentially can be parametrized by the same basis function.

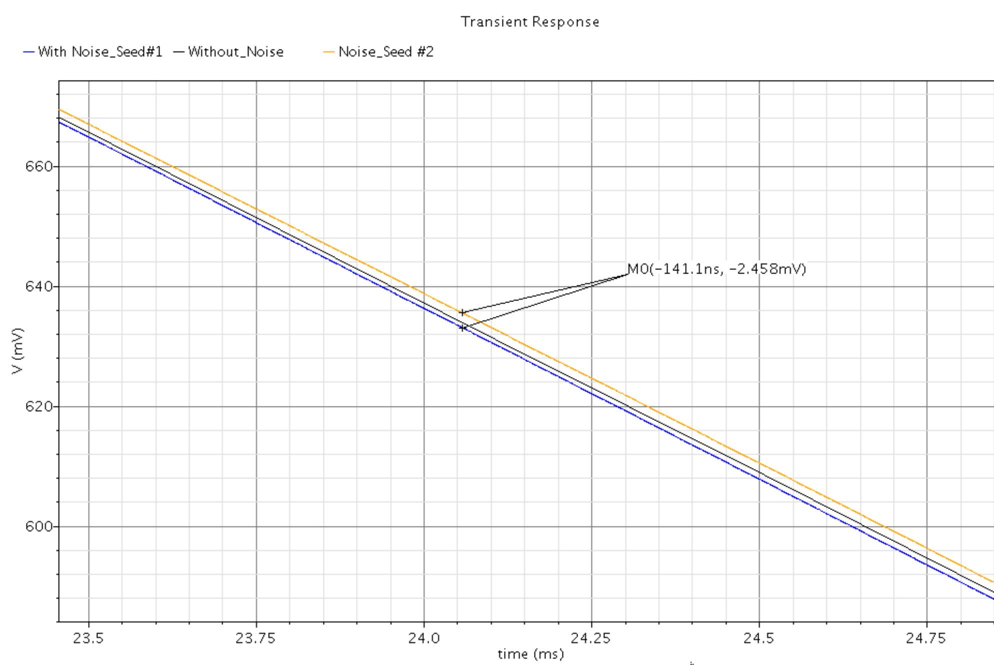

Figure 4.13: Flicker Noise Effect on the Ramp – Shown are the plots without noise and with two different noise seeds (Notice the gain error results in voltage differences as high as 2.5mV)

4.5. Corner/Temperature variations – Current reference

This section presents the simulation results for the variations in the simulated ramp rate as a function of the temperature effects and the resistor/capacitor corners.

4.5.1. Temperature Variations

The sensitivity of the ramp slope to temperature variations originates from the temperature coefficient of the resistor and the PTAT nature of the current. As shown in Figure 4.13, the subtle interaction between these two factors leads to a non-monotonic variation across a range of 0-80C.

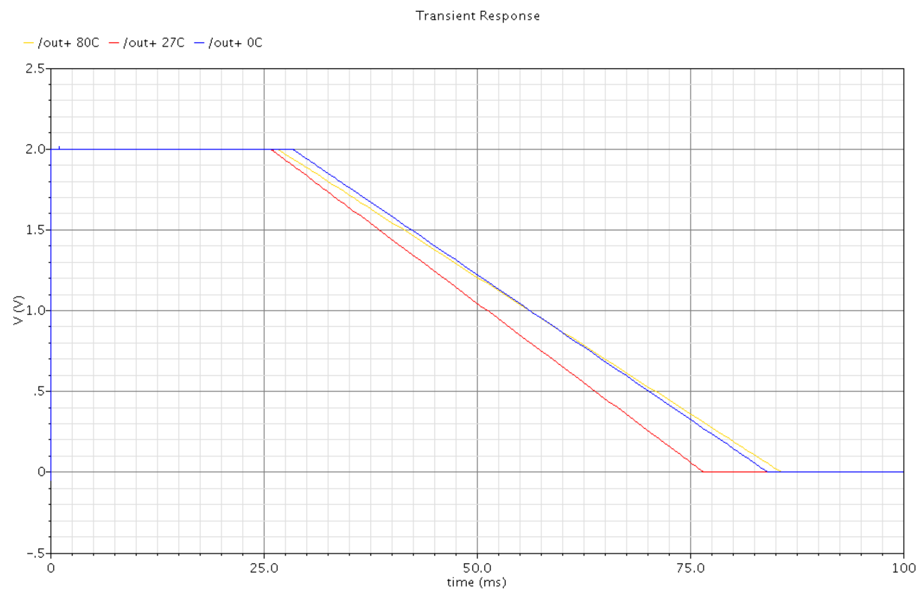

Figure 4.14: The ramp slope variation as a function of the temperature

This variation is not of a concern for the application – given that the degradation in the fall times is not severe. Even in the worst case, the ramp function ramps up to full scale in about 50ms. This is sufficiently high enough to guarantee the targeted hits per code.

4.5.2. Process Corner Variations

The sensitivity of the ramp rate to the charging capacitor value and the resistor value (in the current reference block) directly stems from Equation 1.6.

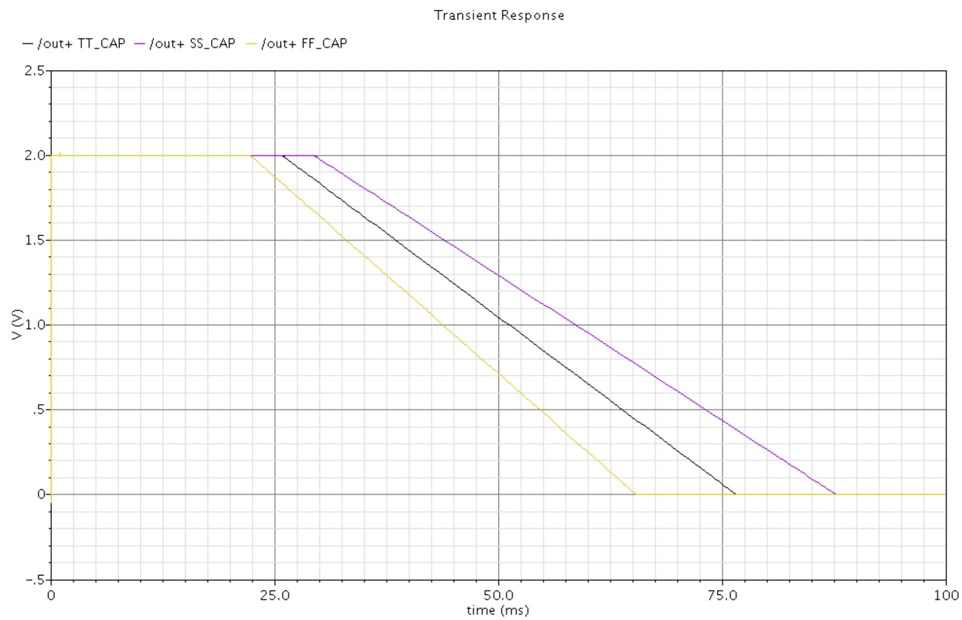

Figure 4.15: Ramp rate variation due to capacitor corners – Worst case fall time ~ 43 ms

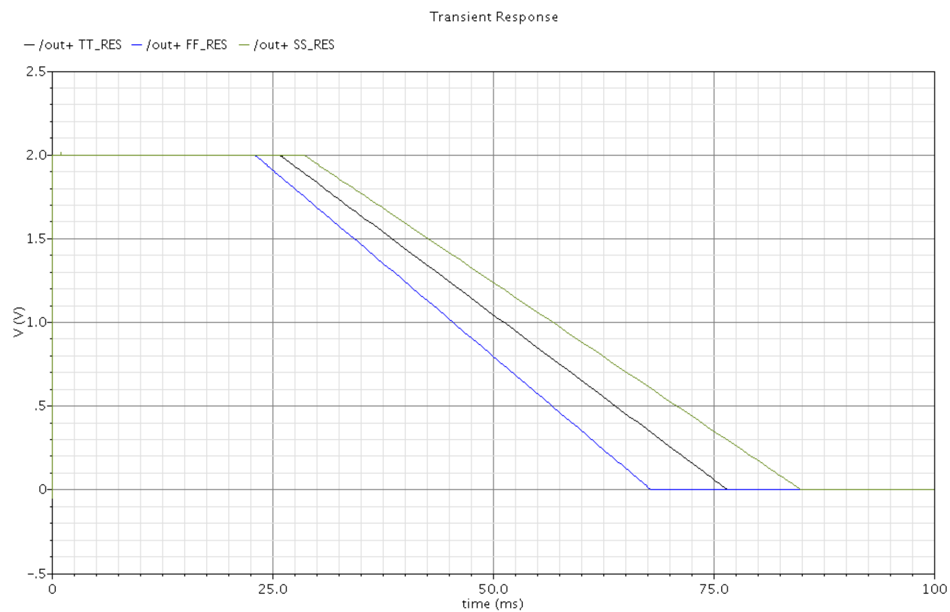

Figure 4.16: Ramp rate variation due to resistor corners – Worst case fall time ~ 42ms

The affect of the above process variations (Figure 4.14 and Figure 4.15) impacts the obtained hits per code. The lesser hits per code would subsequently lead to larger time quantization errors (in the code transition times in the histogram test) and lesser suppression for circuit noise. While the impact of the variation is not expected to be severe, a trim provision has been sought to be incorporated in the current reference core. This would comprise of a programmable resistor strings whose segments may be appropriately connected to modulate the ramp rate during testing.

4.6. Front-end Driving Interface

The overall design of the driving interface to the ADC (with the appropriate capacitor values) is shown in Figure 4.16. The values of the capacitors C1 and C2 are chosen to be 3pF each in order to ensure that the feedback factor for OTA 2 is maintained close to 0.5 (by accounting for the parasitic capacitance at node VY).

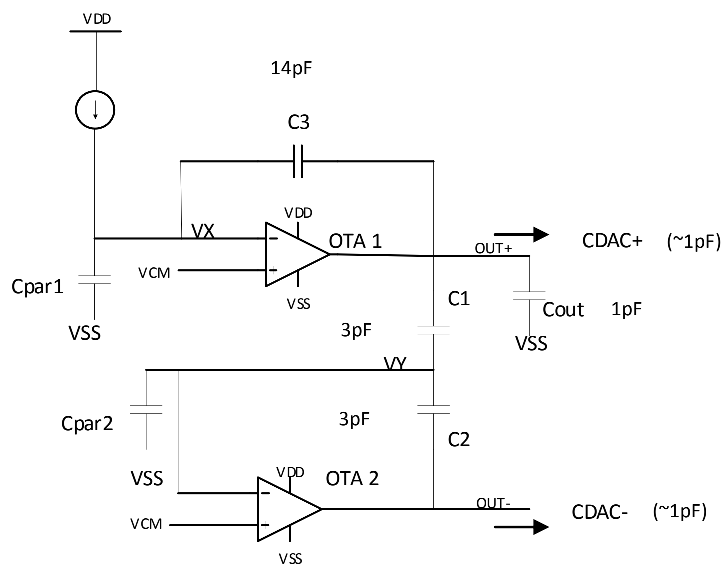

Figure 4.17: Front-End Driving Interface with the designed capacitor values

The capacitor C3 which forms the main charging ramp capacitor is set to 14pF based on the ramp rate variations across corners (results presented in Chapter 6). Also, for a total load capacitance of about 3pF each, an explicit load capacitor of 1pF is added at the OTA 1 output. Further, the total DAC array capacitance of the existing SAR IP is about 1pF. It is reasonable to assume that the addition of a few capacitor bits (towards the LSB level) for redundancy would not significantly affect this total ADC input capacitance.

4.7. Ramp Linearity

A simulation result is presented for the linearity of the single ended ramp output (OTA 1) with the whole integrated front-end comprising of the current reference and the integrator.

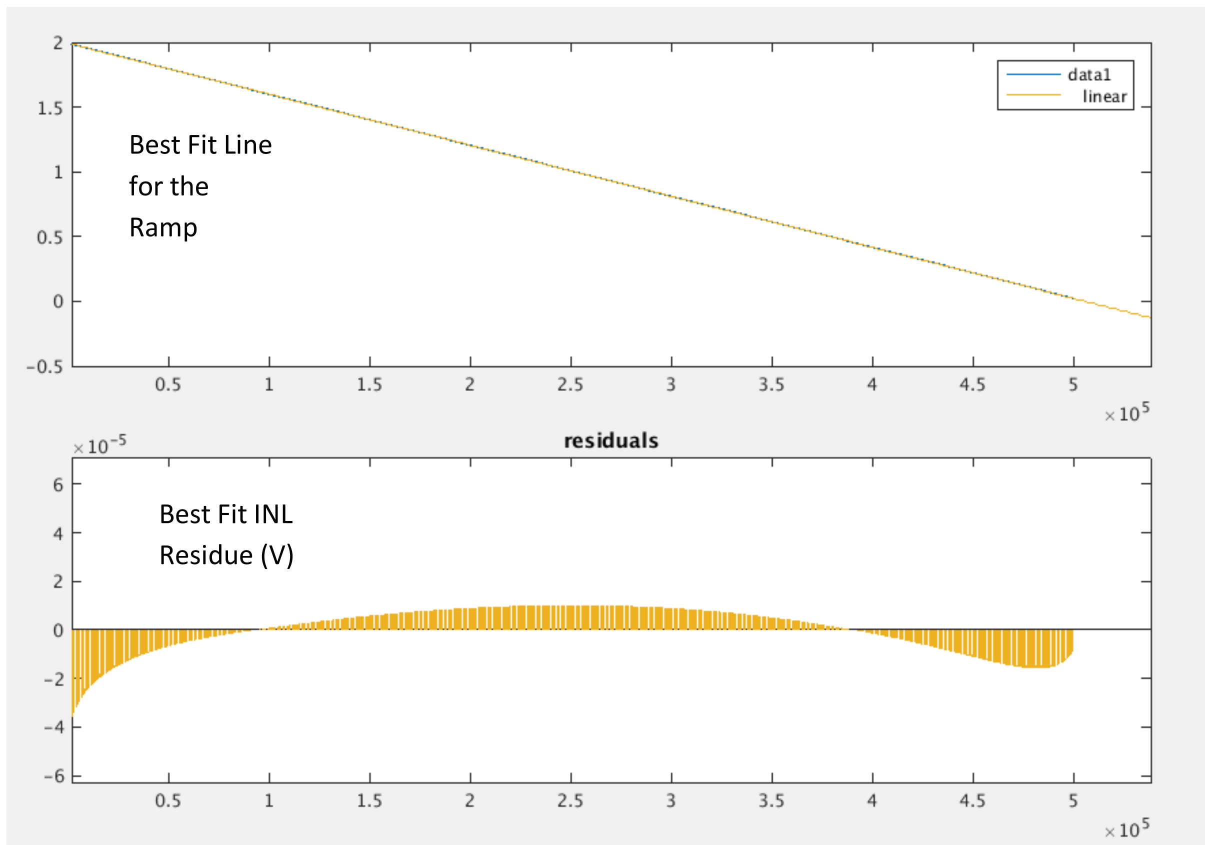

Figure 4.18: Ramp linearity for the OTA based charging scheme

As shown in Figure 4.17, the simulated ramp linearity is indeed better than the targeted resolution of over 13 bits (for 2V FS) across the entire voltage range. The OTA based feedback charging scheme greatly suppresses the finite output impedance effects of the MOS current source as expected.

Chapter 5: 14-bit Redundant SAR ADC

5.1. Redundancy in SAR

Conventionally, the SAR algorithm proceeds as a binary search of the input voltage against radix-2 reference levels. Even though this is indeed the most efficient and optimum algorithm, it results in non-overlapping search step sizes. In other words, this implies that the errors committed in the decision making at any step cannot be corrected through subsequent search paths.

To provide for some resilience to decision errors, redundancy is built into the search algorithm by having non-binary search steps. Essentially, the idea of redundancy is to allow for overlapping comparison levels so that multiple quantized output codes may represent the same input level. A redundant DAC array may be realized in the following two ways:

1. Sub-radix 2 DAC: The capacitor DAC array may be weighted with a radix value lesser than 2. This would result in overlapping search paths.
2. Extra capacitors in the DAC: Having multiple instances of a given weighted capacitor in the array would translate to redundant comparisons and hence overlapping paths downstream.

Essentially, redundancy at any of the conversion stages may be quantified by the difference between the search size of the particular step and the sum of the steps following it. For any decision level, errors within this bound can be potentially detected and corrected for [2].

$$Redundancy\ for\ code\ k, R(k) = \sum_{i=1}^{i=k-1} S(i) - S(k) \tag{5.1}$$

where R(k) is the redundancy for search step k, S(i) is the search size for the ith level.

A redundant SAR approach also offers the following advantages with respect to circuit implementation:

1. A redundant algorithm may in fact be able to speed up each of the SAR conversion cycles. Typically, the major time bottleneck is associated with the DAC dynamic settling for the higher MSB capacitors. Redundancy built into the system may be able to tolerate incomplete settling upfront – while pushing the burden of correcting incorrect decisions to the later steps. Indeed, redundancy requires additional cycles to achieve a desired resolution. But the time cost savings in the DAC settling may be suitably designed to outweigh the increase in the steps.

2. Calibratability: Calibratable errors refer to the linearity artifacts which maintain the division of the full-scale input range into equal segments – each represented by a discrete code. In other words, calibratability requires the quantization interval to be the same for all the digital codes (which then essentially forms the resolution). A redundant DAC implementation (without any additional linearity errors) ensures this very condition required for calibratability by guaranteeing uniform code widths - however at the expense of missing codes in the digital output. These missing codes can be easily corrected digitally by removing the same from the output code space and /or appropriately manipulating the obtained digital bit outputs (Figure 5.1). On the other hand, ADC transfer functions with missing levels (for super-radix 2) are not calibratable as it results in unequal analog voltage intervals for each

digital code. Linearization of such a system would not be feasible from the converted output codes as the analog information (over the range of the wide code) is completely lost.

Indeed, redundancy increases the number of steps in the search algorithm (or equivalently provides a lesser effective number of bits) as compared to the conventional DAC array. However, for this project, we incorporate redundancy to the DAC array primarily in order to ensure calibratability for the linearity errors.

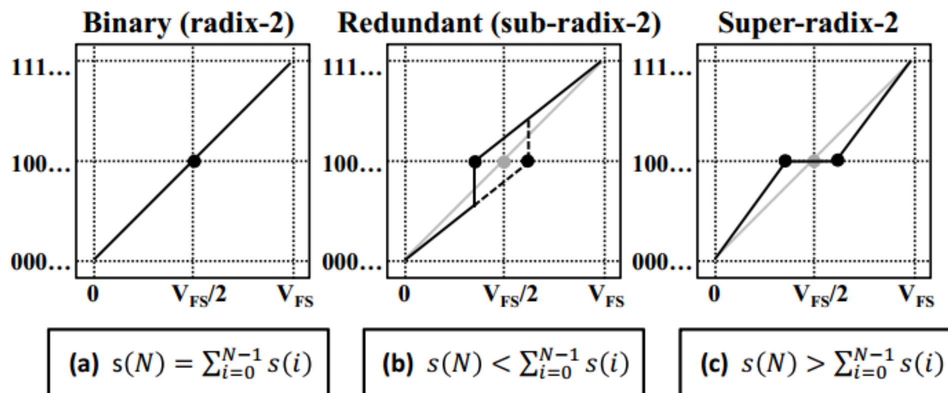

Figure 5.1: Effect of the search radix on the SAR transfer function a) Ideal operation b) Missing Codes c) Missing Levels [2]

5.2. DAC Array & Sampling scheme

The DAC array has been modified to incorporate 3 redundant bit capacitors – C1, C2 and C3 (Figure 5.2). As described in the previous section, this is undertaken to ensure that the linearity errors within the redundancy tolerance bound are calibratable. Having redundancy built even for the last LSB ensures that Equation (4.9) is satisfied for all the bit decisions.

Another implementation detail pertains to the LSB capacitors in the array. A conventional binary weighted DAC would require enormously large capacitor values for the MSB bits. This would potentially impose severe penalty on the bandwidth due to an

associated increase in the DAC settling times. As an alternative, the lower 6 LSB capacitors are realized as unit capacitors – but pulled up to reference levels that are successively divided by a radix of 2 ($Vref,_p/2$, $Vref,_p/4$, $Vref,_p/8$ and so on). This still ensures that during each bit decision making, an equivalent binary weighted charge is removed. However, the full scale range of the ADC stands to be reduced to a value given by:

$$Reduced\ Full\ scale = \frac{\sum_{i=1}^{N} C_i Vref_i}{\sum_{i=1}^{N} C_i} \sim 1.97V\ (for\ 2V\ Vref,_p) \quad (5.2)$$

This may be intuitively understood by noting that during the sampling, an input charge equivalent to the entire range may be accumulated on the actual physical capacitors – however, over the evaluation phase, a reduced fraction of the reference voltage is swept through for the comparisons.

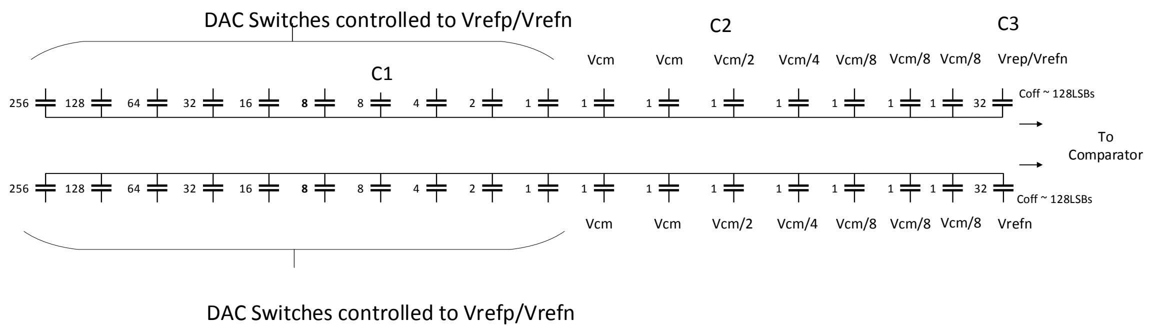

Figure 5.2: Modified DAC array for redundancy (capacitors C1, C2, C3) and offset injection. Total DAC capacitance is ~1.05pF.

The ADC employs a bidirectional switching scheme for the DAC array. As shown in Figure 5.3, the switching sequence is monotonic in the sense that each bit decision successively leads to only a discharge of the following DAC capacitors (of only one of the differential capacitors based on the previous decision). In the signal acquisition phase, the

input is sampled based on the 'bottom-plate sampling' technique. The bottom plate is pulled up to the common mode potential and the differential inputs are presented to the top plates. With this scheme, signal dependent charge injections are avoided and the only source of error is the input independent injections from the bottom plate switch (which are differentially cancelled out). Next, during the conversion phase, the top-plate capacitors (of both positive and differential arrays) are pulled up to $Vref_{,p}$ (or $Vref_{,p}/2$, $Vref_{,p}/4$ etc. for the LSB capacitors in our present case) and the bottom plates are left floating. As per charge conservation, the differential input subsequently develops on the two DAC arms and the first comparison is carried out to yield the MSB sign bit. Based on the result of the same, the MSB capacitor of one of the differential sides is appropriately pulled down to $Vref_{,n}$. This sets up the reference level for the next bit and the comparison is carried out. This process is subsequently repeated successively to yield all the other bits. In this switching scheme, an aspect to note is that the logic to switch the top-plate capacitor (based on the previous result) is inverted to that for the remaining bits. Including the first MSB result, the final digital output is encoded as 17 bits (with 3 bits of redundancy). In addition, an extra offset capacitor is added to both the differential arrays – and one of them is switched to $Vref_{,p}$ (from $Vref_{,n}$) during the offset injection phase.

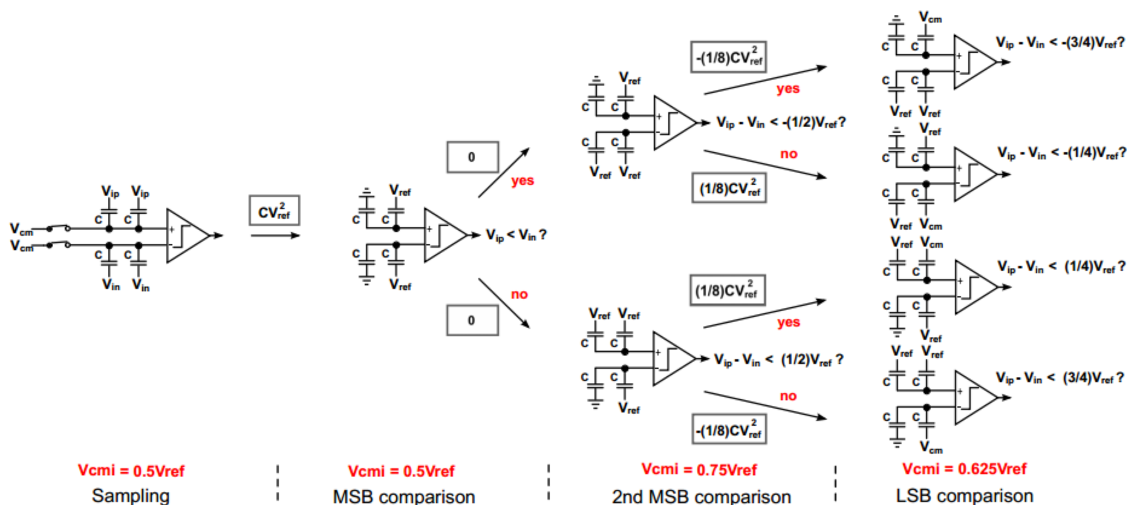

Figure 5.3: Bidirectional switching scheme [12]

5.3. SAR Comparator

The comparator block is based on the 'Strong Arm' latch operation [13]. It involves a pre-amplification of the differential input – followed by a regenerative positive feedback latching mechanism (Figure 5.4). Initially, in the reset phase (CLK = 0), the outputs VOUT+ and VOUT- are pulled high to ensure that the cross-coupled pair M5 and M6 are turned OFF and that there are no voltage offsets. Also, the drains of the differential input pair are pre-charged to VDD to prevent hysteresis effects. With the tail current source turn OFF when CLK = 0, the block does not consume any static power. During the active comparison phase (CLK = 1), the inputs draw differential currents from nodes VX+ and VX-. These currents (amplified by the transconductance of M1/M2) cause nodes VX+ and VX- to ramp down at different rates and thereby turning on the devices M3 and M4 (when a threshold drop has developed). Output nodes VOUT+ and VOUT- follow the same dynamic ramping till the accumulated difference triggers the latch to pull up one of them to VDD (and the other to VSS). This completes the comparison and the circuit returns to its idle zero power state.

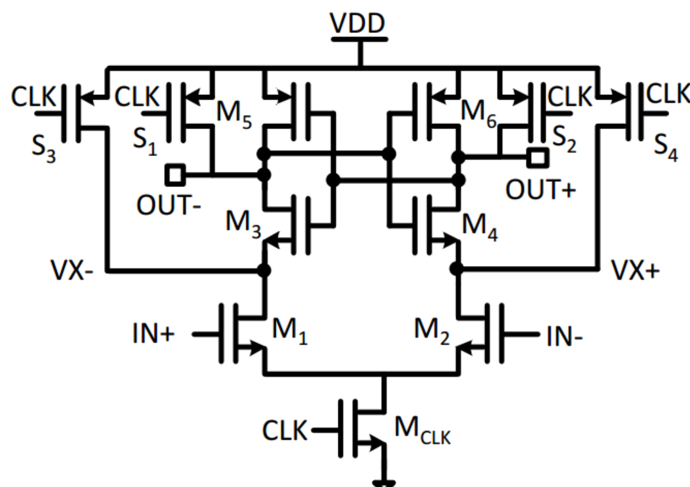

Figure 5.4: Strong-ARM Latch Comparator [2]

5.4. SAR Clock generation

For the 10MHz sampling operation, 50ns each is allocated for the sampling and conversion phases. Figure 5.5 captures the control signals and their corresponding timing instants for the SAR system. During the sampling phase, CLKS (top plate switch control) and CLKS_EARLY (bottom-plate switch control) are enabled to sample the inputs appropriately on the capacitor array. CLKS_EARLY is disabled earlier than CLKS as per the bottom plate sampling scheme. In the conversion phase, 18 intermediary clock cycles are generated for the 17 bit results (CLKC signal to clock the comparator) and the final latching operation (enabled by the CLK_LATCH signal shown). The only notable change to the clocking scheme is the CLK_OFFSET signal. This is enabled during the conversion phase of every alternate sample conversion – to have an offset added to the ramp signal.

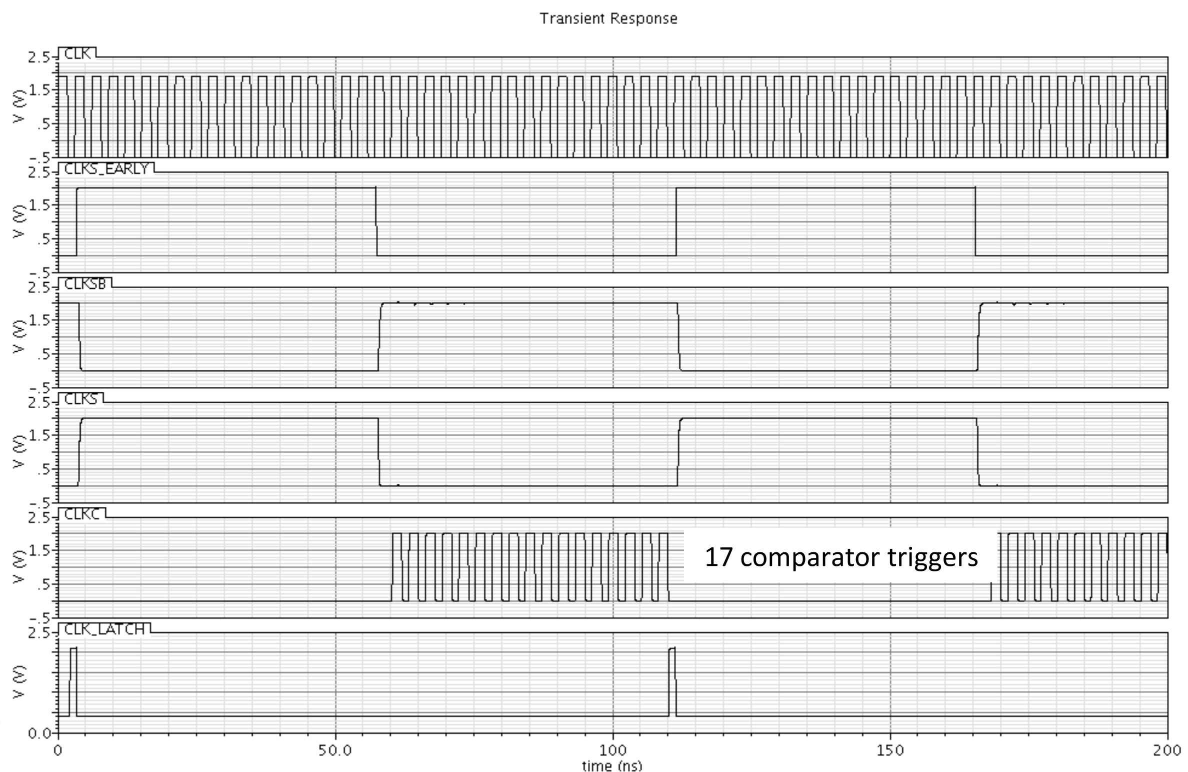

Figure 5.5: The clock sequences associated with the SAR operation

The clock generation unit consists of a delay ring of 18 flip-flop units with an inversion in the loop – each clocked at the system clock frequency of ~ 330 MHz. This generates a clocking sequence with a half cycle of 1/18th the system frequency at the output of each flip-flop. This is used to distinguish between the sampling and conversion phases. Further, inverter based time delays are used to distinguish the '*early*' signals involved in sampling. The system clock is used to clock the comparator for the 17 bit comparisons during the conversion phase.

The digital logic to the DAC top-plate switches is controlled asynchronously when the comparator completes a given bit decision. Based on the comparator result, the reference voltage to the top-plates of the differential capacitors of the next index are appropriately set. The sequencing of these control signals to the DAC array is provided by a series of shift registers which are successively triggered with every comparator decision.

5.5. Simulation Results – SAR ADC

A sine wave input is used to test the effective resolution of the ADC across the full scale dynamic range of -2 to 2V (provided by the differential operation). The time domain waveform for the reconstructed quantized representation of the analog input is shown in Figure 5.6. The reconstruction of the signal is effectively carried out by weighting the digital output bits by the corresponding radix value (determined by the capacitor values of the redundant array). This simulation assumes a sampling frequency of 9.25MHz and a noise bandwidth of 100MHz. Also, the offset injection phase is disabled.

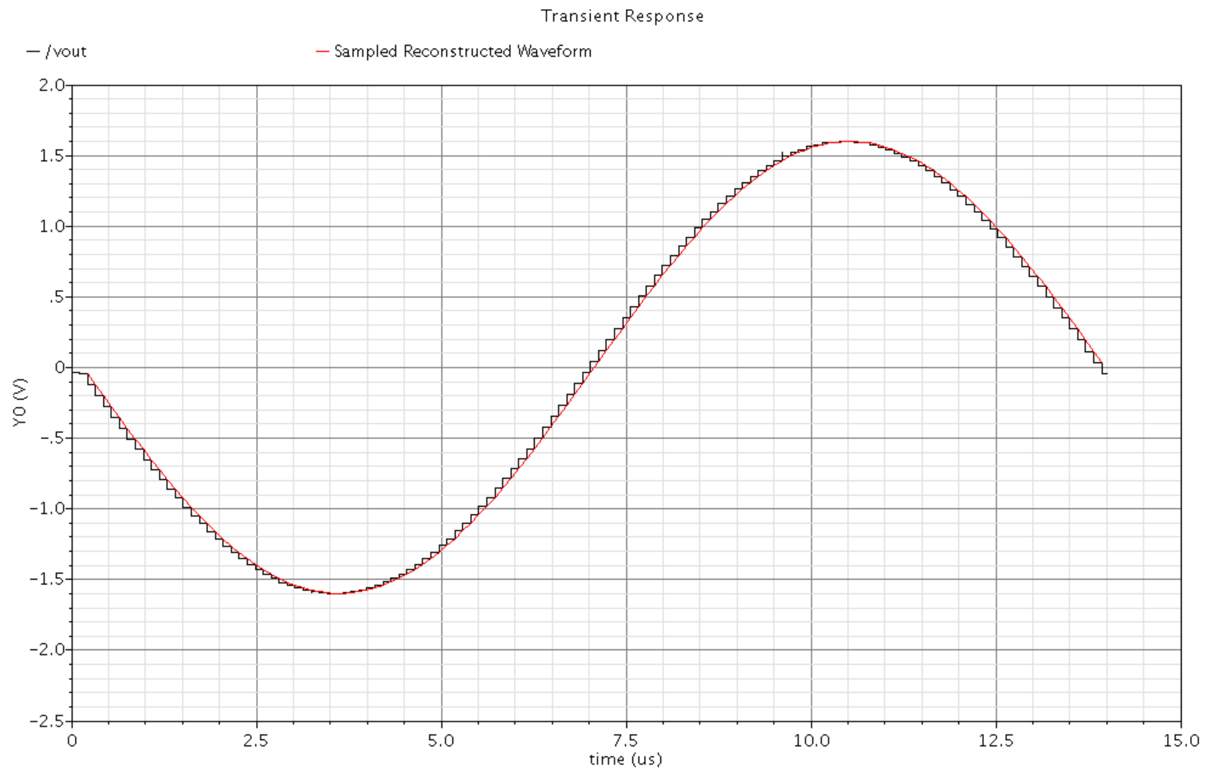

Figure 5.6: Time domain Reconstructed Input Sine Wave; Input Frequency = Fs/128 (~72KHz)

The effective resolution of the ADC can be thereby computed by taking the FFT (Fast Fourier Transform) of this time domain reconstructed waveform (Figure 5.7). The choice of the input frequency for the test is specifically chosen to be an odd sub-multiple of the sampling frequency (like Fs/128) to have exact integer number of cycles over the total number of sampled points. This eliminates the need for additional windowing functions to prevent spectral leakage artifacts. An effective Signal-to-Noise-Distortion Ratio (SNDR) of about 80 dB is obtained. This corresponds to an effective resolution of ~13.2 bits.

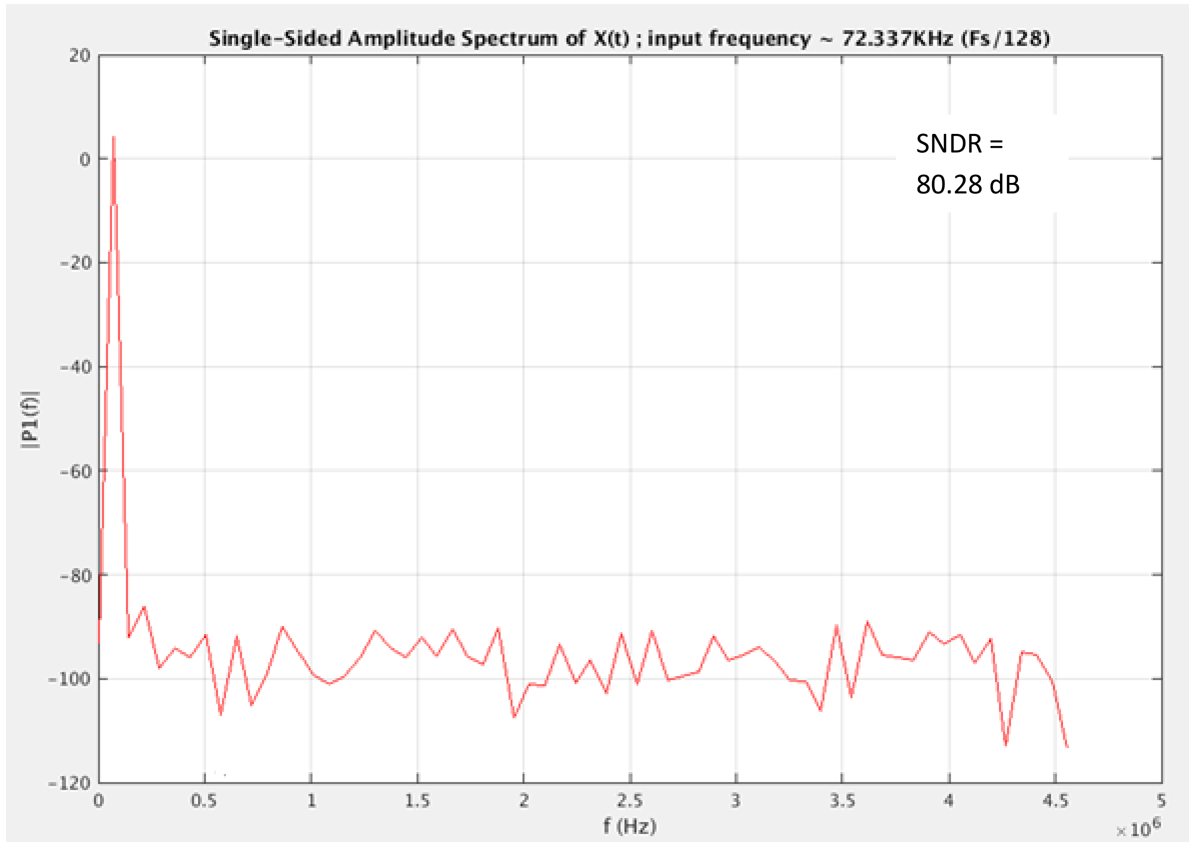

Figure 5.7: Single Sided FFT Spectrum of the Reconstructed Input with a reported SNDR of 80dB

The operation of the offset injection provided by the appropriate switching of the offset capacitor in the DAC array is verified by the simulation result presented in Figure 5.8 for a ramp input. In every alternate SAR comparison phase, an offset is generated for the converted output. For the chosen value of the offset capacitor (C_{off}) as 32fF, the effective offset generated by switching either of the positive or negative side capacitor from $Vref_{,n}$ to $Vref_{,p}$ is given by:

$$Offset\ injected = Vref_{effective} \cdot \frac{C_{off}}{C_{DAC}} \cong 60mV \qquad (5.3)$$

where $Vref_{,\ effective}$ is the reduced effective full scale range (~1.979V) due to the fractional reference levels used for the lower 6 bit indices.

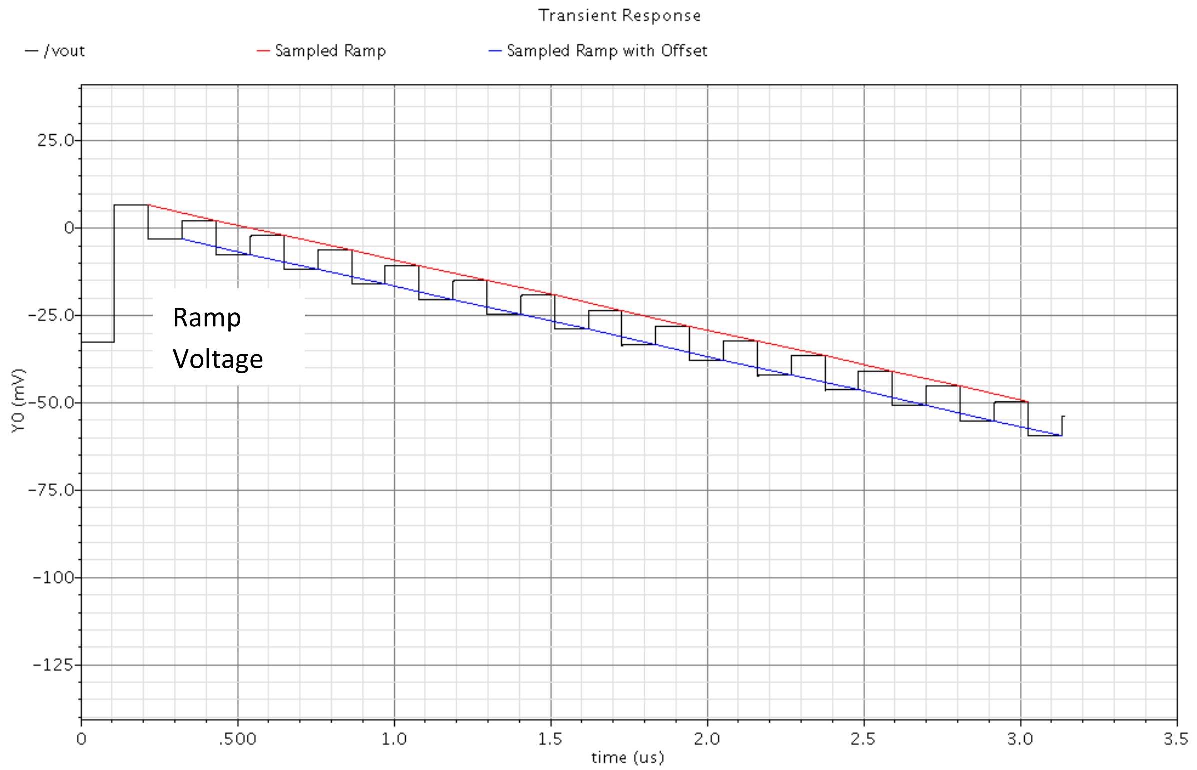

Figure 5.8: Demonstration of the interleaved offset injection cycle during the SAR conversion for a ramp input. An offset proportional to C_{off}/C_{total} is generated for alternate ramp samples

5.6. Charge kickback effects

The buffer amplifiers (the integrator OTA 1and the differential ramp generator OTA 2) are subject to the kickbacks and transient voltage excursions arising from the sampling artifacts of clock feedthrough and/or charge injections. In this section, the effect of the same on the front-end signal generating block is evaluated.

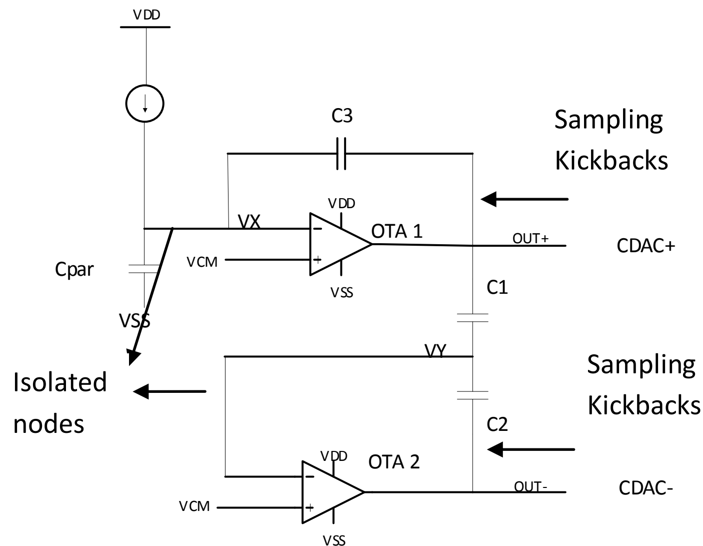

Figure 5.9: Representation of the kickbacks arising from the sampling interface and its effect on the OTA input nodes – the total charge at node VX is immune to the output node and is only dependent the input current source.

Figure 5.9 shows the voltages at the outputs and inputs of both the OTAs during the sampling instants. The high frequency glitches at the output propagate back to modulate the input voltage. This is due to the high output impedance of the OTA at these high kickback frequencies (essentially due to lower loop gain) – resulting in observable voltage changes at nodes VX and VY (Figure 5.9). However, since VX and VY are physically isolated from their respective outputs, the sampling artifacts do not cause any changes to the charge stored at these nodes. By charge conservation thus, the steady state output of the OTAs would still track the desired ramping function (Figure 5.10).

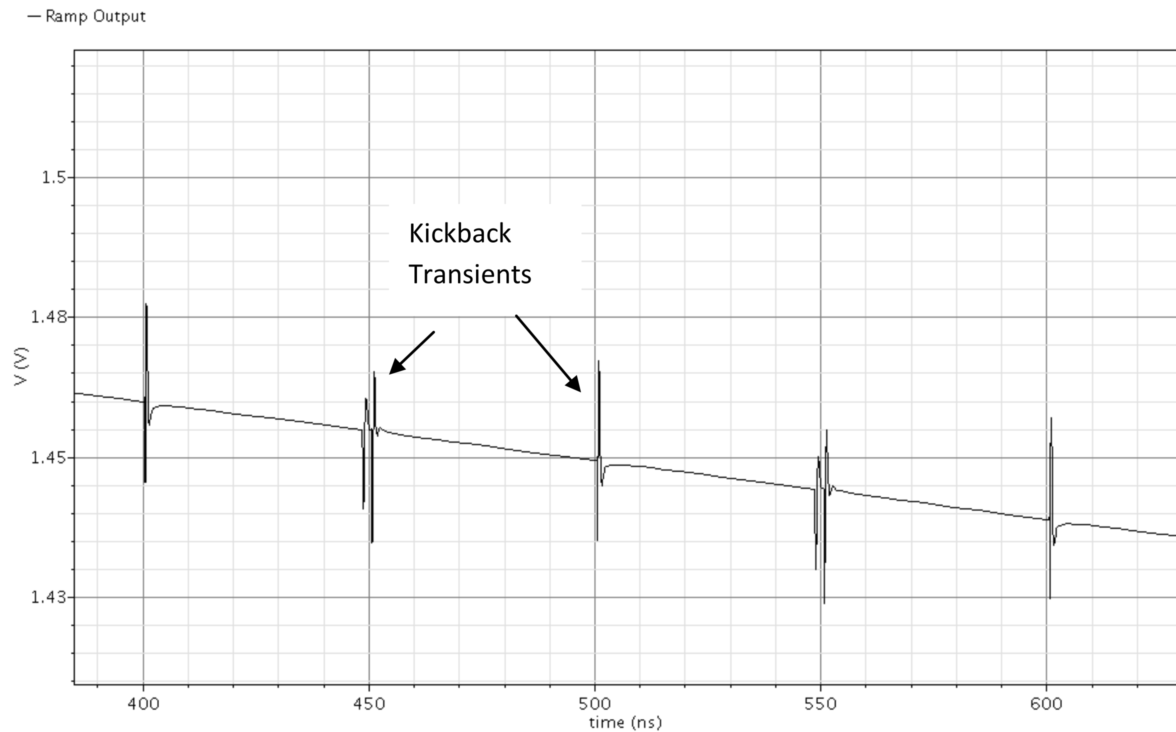

Figure 5.10: Sampling Kickback on the Integrator Output – Notice that the settling ensues to follow a steady ramp

Indeed, the OTAs must have sufficient bandwidth to ensure settling of these transients within the sampling period so that the dynamics of the sampling operation do not introduce any linearity errors in the stimulus ramp signal.

Chapter 6: Layout & Calibration Results

6.1. Layout

The layout of the front end ramp generator blocks comprising of the current reference, the driving stage amplifiers OTA 1 and OTA 2 and the initialization switches is shown in Figure 6.1.

Standard practices of common-centroid arrangement, multi-finger transistor stacking and use of dummy devices have been adopted in the layout. The charging capacitor (14pF) has been realized as a Metal-Insulator-Metal (MIM) structure between metal layers M5 and M6. The use of MIM capacitor in this regard has allowed for its stacking over the lower layers – thus significantly reducing its otherwise large area budget requirements.

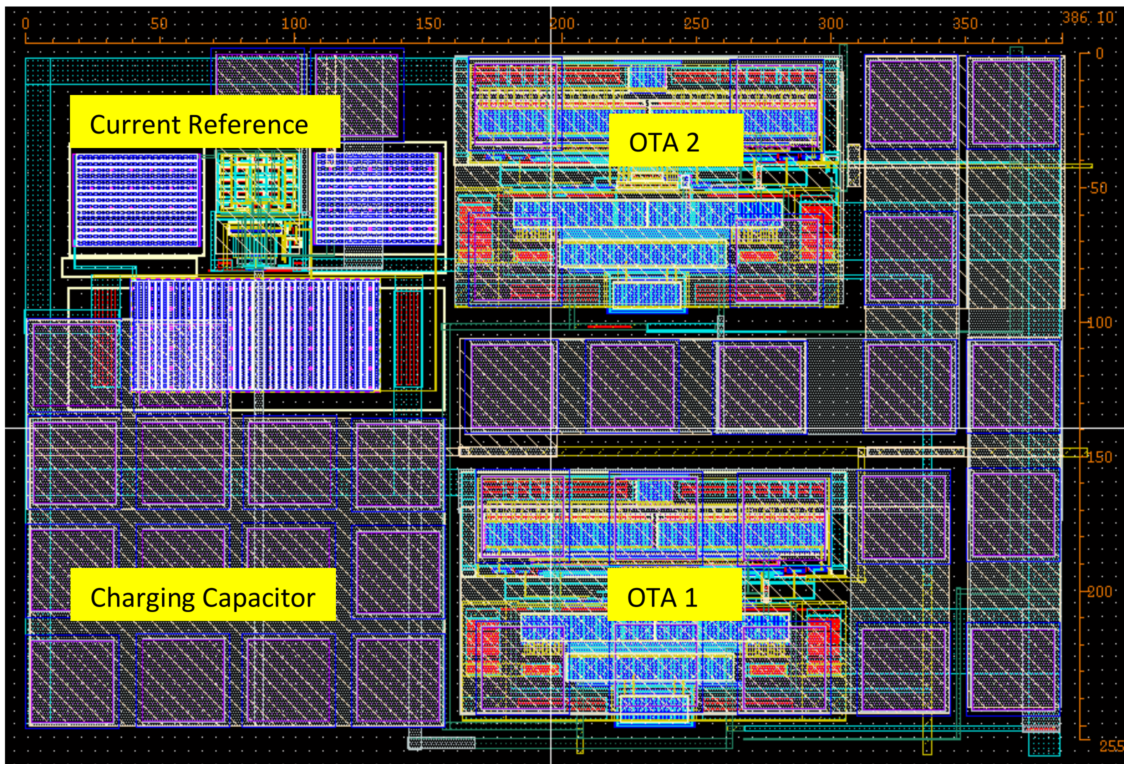

Figure 6.1: Layout of the Front-End Test Circuit (TSMC 180nm)

6.2. Calibration - SEIR Algorithm

A prototype of the SEIR based digital post processing for the ADC calibration was implemented in MATLAB. Also, a behavioral model for a 14-bit SAR ADC functionality was developed for an ease of simulation of the entire BIST operation. Figure 6.2 summarizes the algorithmic steps involved in the test and calibration.

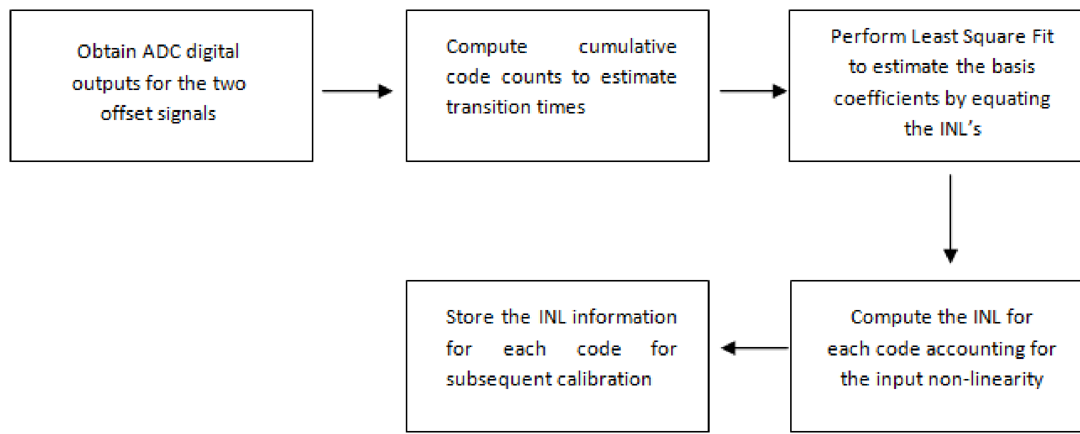

Figure 6.2: Algorithm of the digital calibration

Once the INL for all the 'N' digital codes of the ADC is computed, the calibration can be easily undertaken by adding these INL values to the output digital code appropriately.

$$Calibrated\ Output\ \widehat{D(k)} = INL(k) + D(k)\ , for\ k = 1\ to\ N \qquad (6.1)$$

where D(k) is the raw digital output of the ADC. For a redundant DAC array with a reduced ENOB (due to missing codes), the lower bits may be appropriately dropped (through a right shift operation) to yield the true binary representation of the input.

$$Calibrated\ Output\ \widehat{D(k)} = (INL(k) + D(k)) \gg m\,, for\ k = 1\ to\ N \qquad (6.2)$$

where the shift amount of ‘m’ corresponds to upto 2^m missing codes.

To demonstrate the working of the MATLAB processing with the SEIR approach, non-linear terms are intentionally added to the input stimulus. The input is modeled as the following function:

$$Input\ x(t) = \alpha.t + 0.4.sin\left(\frac{pi * t}{Ts}\right) + 0.1.sin\left(\frac{2 * pi * t}{Ts}\right) \qquad (6.3)$$

where Ts is the total duration of the ramping function (=30ms). Also, the input spans from 0 to 4V (for a 4V differential ADC dynamic range). Further, the algorithm is set to use 30 basis functions to model the input non-linearity. An offset of 128 LSB is added for the second ramp stimulus.

6.2.1. Conventional ADC

The implementation of the SEIR algorithm with the input non-linearity is demonstrated for a conventional binary weighted SAR ADC (without redundancy). Shown in Figure 6.3 are the plots of the estimated input non-linearity of the input (in LSBs) and the computed INL for the ADC.

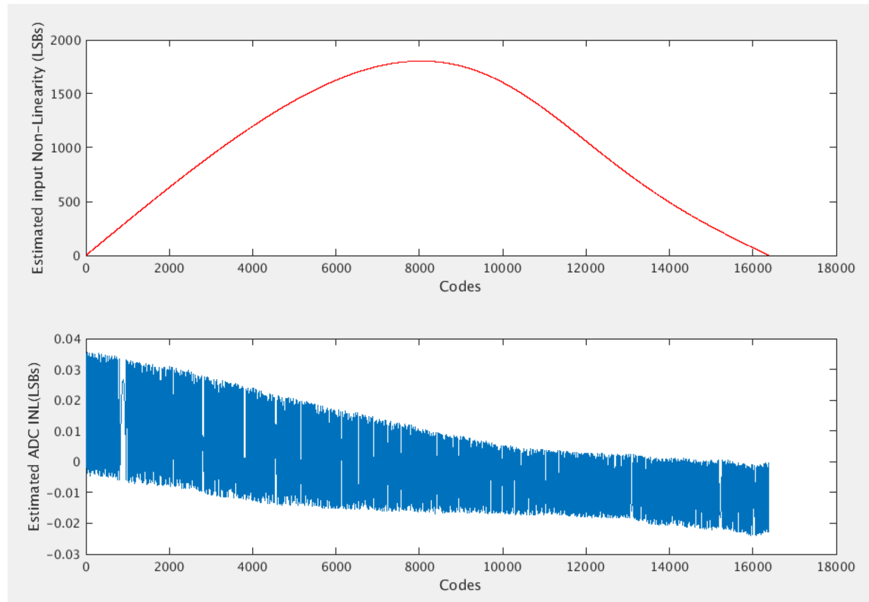

Figure: 6.3.SEIR fit results for Conventional ADC a) Estimated input non-linearity b) For an ideal DAC array, the ADC INL is corrected computed to be negligibly small than 1 LSB.

The algorithm correctly computes the input non-linearity and reports no INL errors for the ideal ADC.

6.2.2. Sub-radix 2 Redundant ADC

Next, the simulation is carried out for a redundant SAR ADC with a sub-radix 2 index of 1.86. This means that each capacitor of the DAC is weighted as powers of a factor of 1.86 (instead of the conventional case of 2).

For a 14 bit output, the redundant search results in a code span of $(1.86)^{14} \approx 5937$. This corresponds to a loss of 2 bits of resolution implying a shift amount of 2 for the calibrated output. Shown in Figure 6.4 is the transfer function of the ADC (as a function of the analog input samples) for the redundant SAR implementation with input non-linearity. The accompanying plot for the INL is the result prior to the calibration (wherein the actual redundant DAC capacitor weights have not been accounted for).

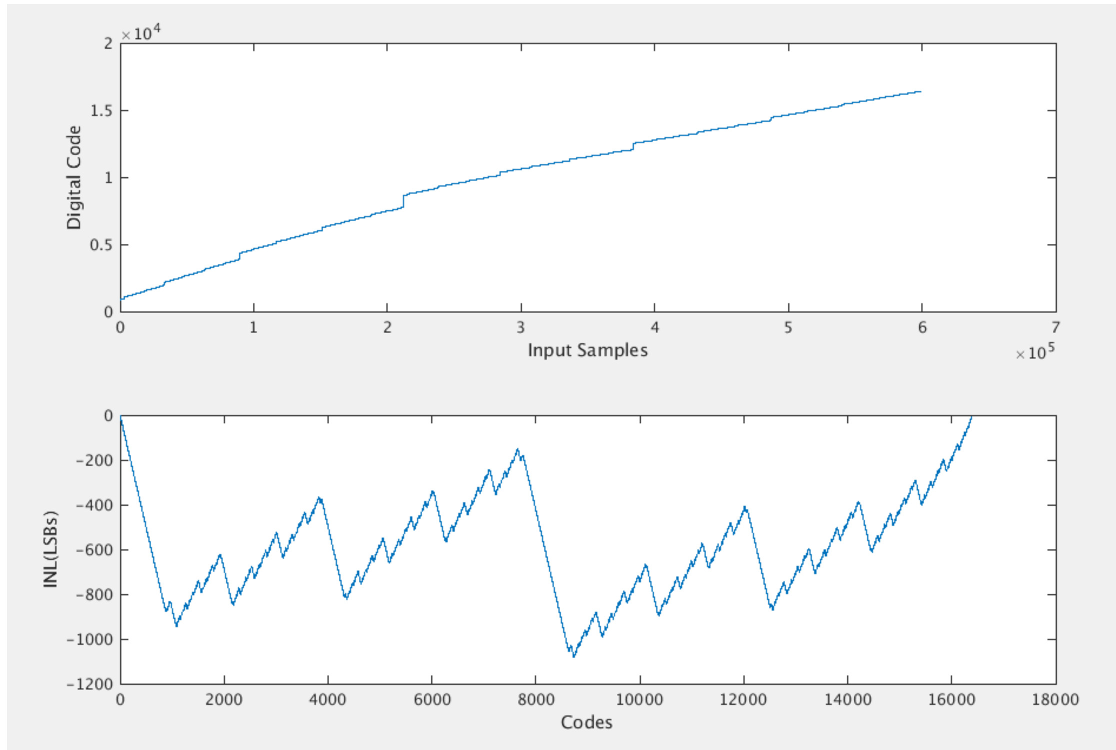

Figure: 6.4 SEIR fit results for Sub-radix redundant ADC a) ADC transfer function with redundancy b) INL errors before calibration (input non-linearity is however corrected for)

The digital output codes may now subsequently calibrated with the known INL values as shown in Figure 6.5. This results in an ideal transfer function with a reduced resolution of 2 bits (also evident from the plotted quantization error values of about 1.5LSBs). Shifting the codes by 2 (or a division by 4), the fit errors would reduce to within the quantization bound.

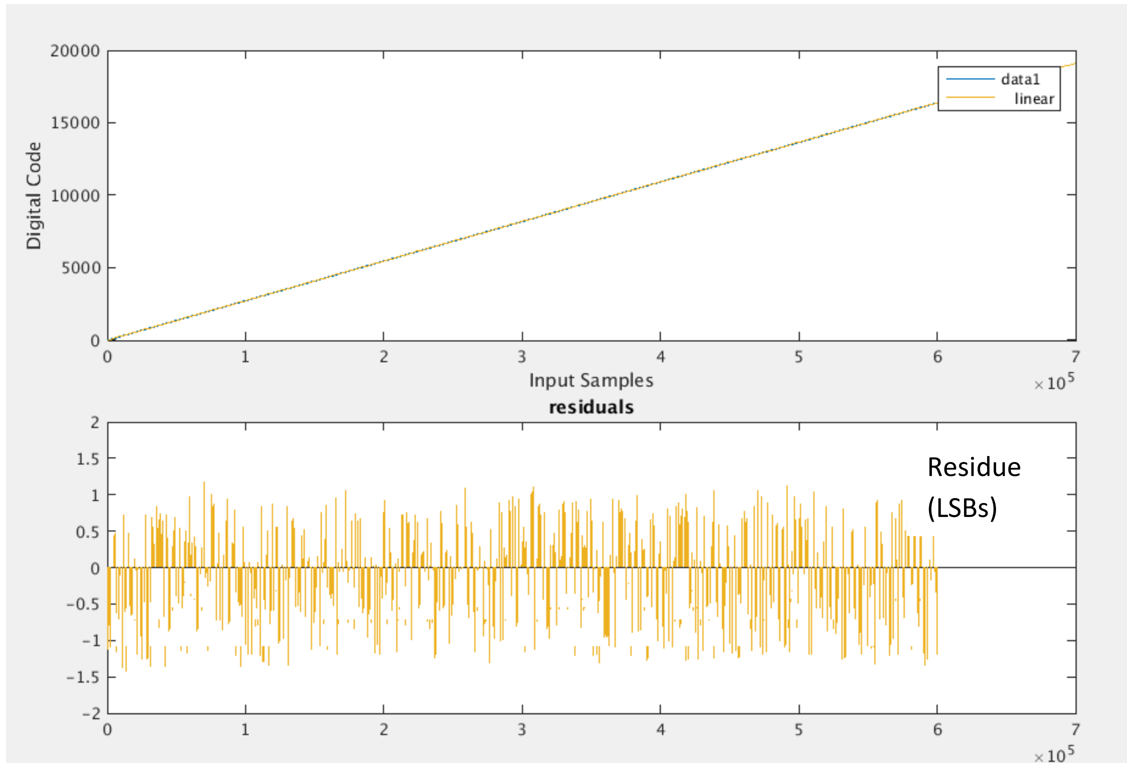

Figure 6.5: Post calibration Transfer Function and the Best-Fit residue plot for sub-radix 2 redundant ADC (Shifting out the digital sequence by 2 bits would reduce the straight line fit residues to within [-0.5LSBs, 0.5LSBs].

6.2.2. Redundant SAR with extra DAC capacitors

This section presents the simulation calibration flow for the actual SAR DAC implementation adopted for this project. Redundancy is achieved by the addition of 3 extra capacitors (described in Chapter 5).

The simulation set-up and the premise remains the same as the sub-radix DAC. With a 3 bit redundancy, the calibrated output would now require a division by a factor of 8 (shift by 3) to obtain the true resolution (Figure 6.7).

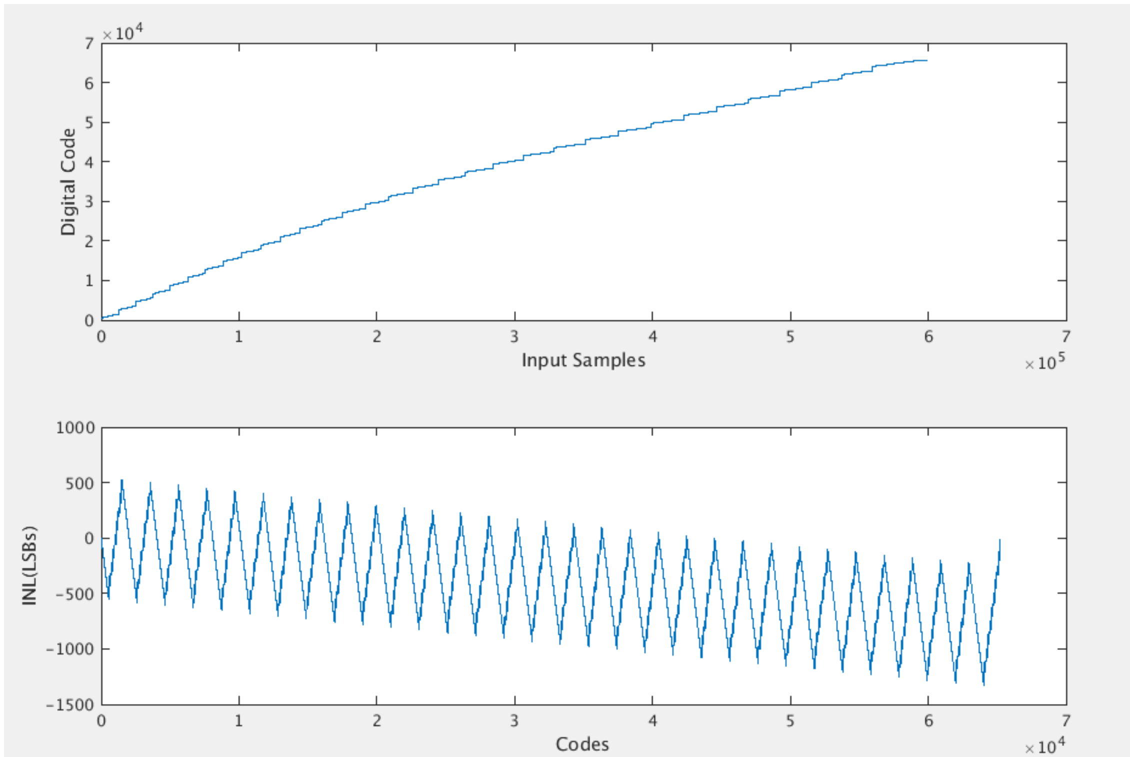

Figure 6.6: SEIR fit results for Proposed Redundant ADC a) ADC transfer function with redundancy b) INL errors before calibration

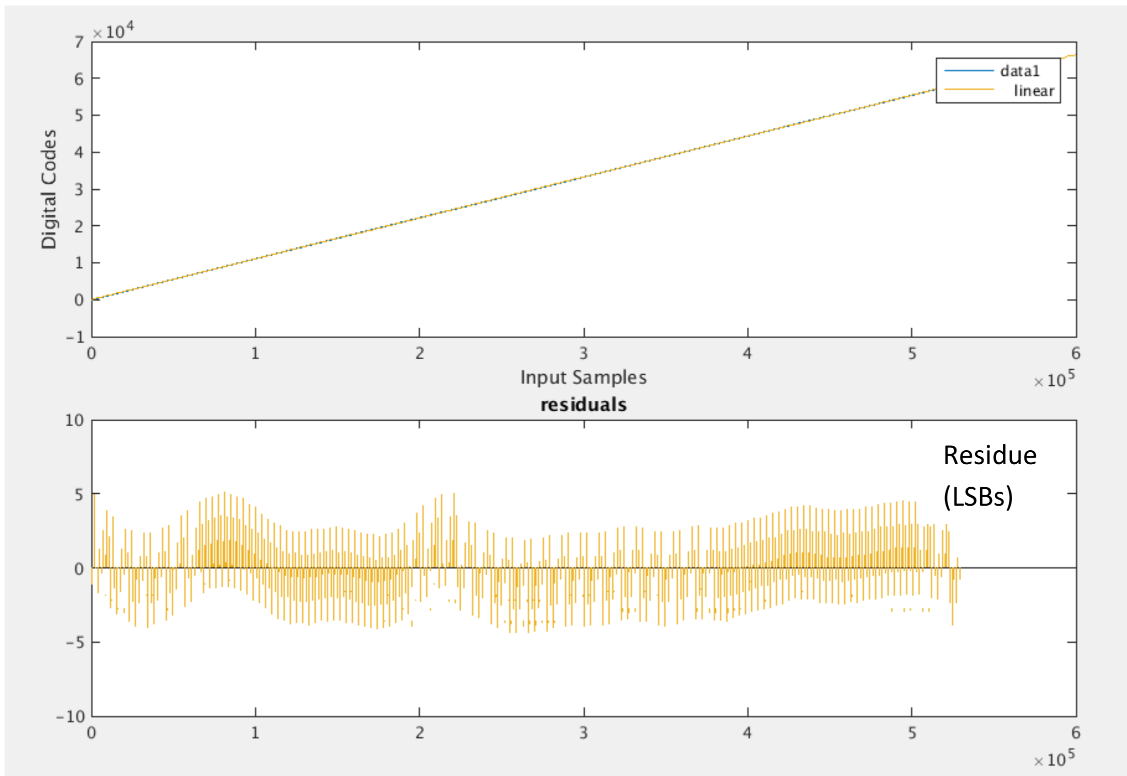

Figure 6.7: Post calibration Transfer Function and the Best-Fit residue plot for the proposed redundant ADC (Shifting out the digital sequence by 3 bits would reduce the straight line fit residues to within [-0.5LSBs, 0.5LSBs]).

Next, for the same redundant DAC array, the effect of practical circuit noise is simulated to observe the performance impact on the SEIR algorithm. A Gaussian noise source is added to the modeled input – with a mean of zero and noise power (standard deviation) equal to a resolution of 1LSB (~ 500uV for a 4V FS range). All other simulation parameters are kept the same. A noise power with a standard deviation of 1 LSB is infact pessimistic budget (the circuit noise from post-layout simulations report lower values). Nevertheless, the result of such a simulation should be indicative of the tolerance levels that the system can handle.

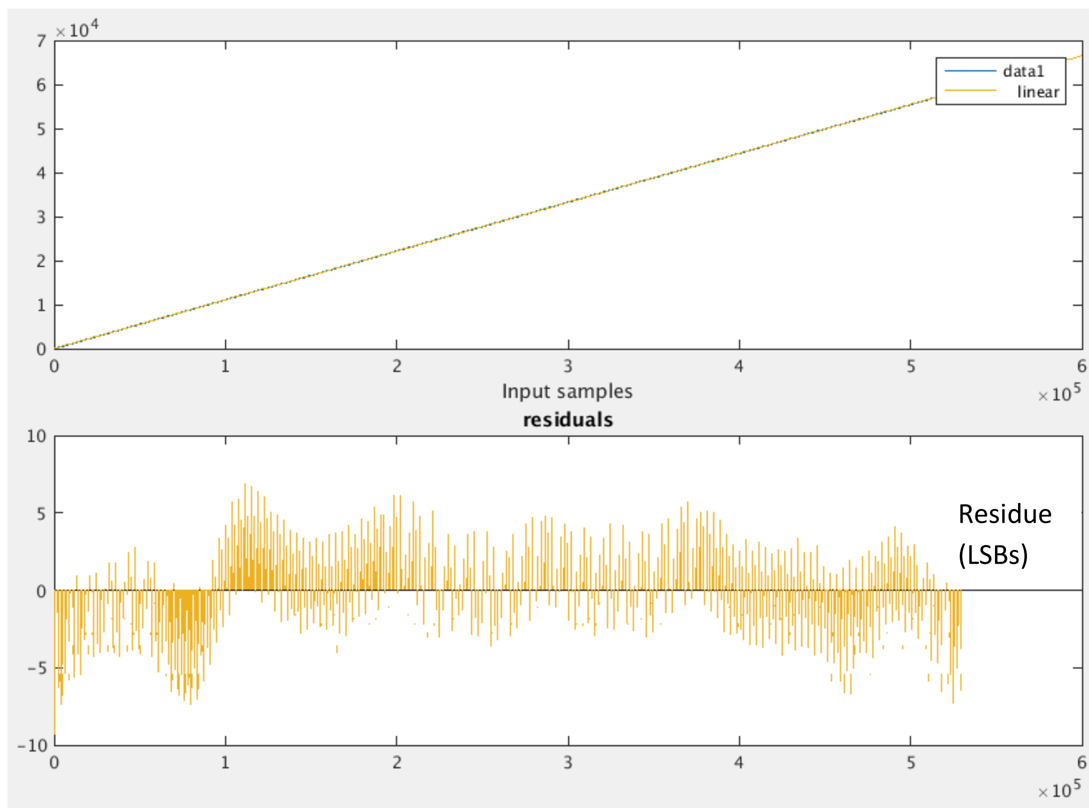

Figure 6.8: Post calibration Transfer Function and the Best-Fit residue plot with noise for redundant ADC – standard deviation of the noise σ = 1LSB

Figure 6.8 captures the SEIR estimate in the presence of noise. As is evident, there is no major impact on the INL estimation and the calibrated plot yields the same residue values

for the best-fit linear transfer function. Thus, it may be concluded that a noise level of 1LSB is not significant enough to affect the LS fit performance (for the given resolution with the assumed values for the hits per code & offset).

Finally, Figure 6.9 demonstrates the effectiveness of the SEIR algorithm and calibration on an actual differential ramp data-set from Cadence simulations (of the redundant ADC with extra DAC capacitors). The output of the front-end (which is linear to ~14 bits in simulations) differential ramp is fed to the redundant ADC model and the same result is obtained. By suitably accounting for the 3 redundant bits (division of the digital output by 8), we obtain the true calibrated representation of the quantized outputs.

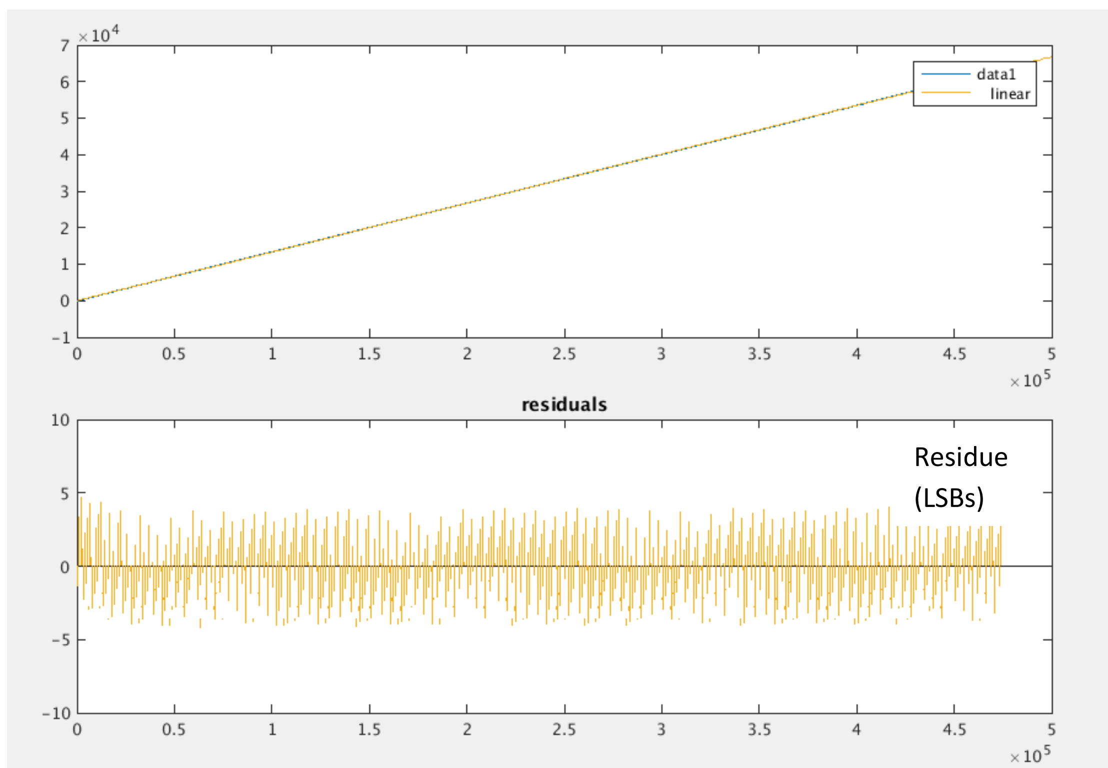

Figure 6.9: Post calibration Transfer Function and the Best-Fit residue plot for actual differential ramp from Cadence

Chapter 7: Summary & Future Work

This section summarizes the work undertaken as a part of this thesis and outlines the scope for future work in this regard.

7.1. Summary

The project investigates the challenges associated with Built-in-Self Test schemes for Mixed Signal integrated circuits. In addition to the general benefits of saving expensive production test time, an on-chip testing methodology would also make 'per-part' calibrations more commercially viable. This principle of self test and calibration has been sought to be demonstrated for high resolution SAR ADCs, whose linearity performance is typically limited by the DAC capacitance mismatches. In this regard, a front-end test circuit comprising of a ramp generator and a driving interface has been designed and implemented to carry out the standard histogram based test. Such an on-chip implementation has in fact been made feasible by the SEIR algorithm which relaxes the input linearity requirements – while pushing the burden of the test to requiring functionally related input test signals. This work also evaluates the robustness of the BIST scheme to circuit level non-idealities and its implications on the linearity test. For the input ramp, a post-layout linearity performance of ~14 bits has been obtained (to test a ~13bit ENOB ADC). Simulation results have indicated positive results and it is reasonable to expect a successful demonstration of a BIST based self-calibrating SAR ADC.

At the time of writing this thesis, the design is being finalized for taped out and measurement results need to be undertaken to actually validate the idea on-silicon.

7.2. Future Work

An on-chip testing and characterization of the proposed BIST scheme needs to be undertaken to validate the analysis and understand its implications for a real-world commercial application. It would be interesting to characterize the actual flow of the test adopted so that the computational cost and number of test iterations may be better recorded to benchmark the time-cost improvements against off-chip production tests. The scope of the BIST scheme could also be potentially expanded to include the performance characterizations of other metrics like DNL, offset and gain errors of the ADC.

The implementation of the 'Least Square Fit' algorithm for the SEIR approach also needs consideration. It would be worthwhile to evaluate the best way to carry out this post – processing. In mixed-signal SOCs, a hardware implementation of the calibration and LS fit blocks seems to be an obvious way as they can readily provide for the required computation resources. For standalone products, the commercial viability of the digital overhead needs to be carefully considered. For a simpler BIST implementation, it may as well be productive to have the post-processing in software externally – but then the time-cost increase would have to be properly weighed in.

Overall, moving ahead, it would be interesting to follow the trends emerging in such digitally assisted BIST schemes for analog and mixed signal blocks – it seems to evolve as a natural progression to sustain and improve the performance of analog circuits as we continue the path of technology scaling.

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Vita

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