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THERMO-MECHANICAL STRESS MEASUREMENT AND ANALYSIS IN THREE DIMENSIONAL INTERCONNECT STRUCTURES

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THERMO-MECHANICAL STRESS MEASUREMENT AND ANALYSIS IN THREE DIMENSIONAL INTERCONNECT STRUCTURES

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Dedication

To my beloved parents and my wife, Xinshan

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THERMO-MECHANICAL STRESS MEASUREMENT AND ANALYSIS IN THREE DIMENSIONAL INTERCONNECT STRUCTURES

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Three-dimensional (3-D) integration is effective to overcome the wiring limit imposed on device density and performance with continued scaling. The application of TSV (Through-Silicon Via) is essential for 3D IC integration. TSVs are embedded into the silicon substrate to form vertical, electrical connections between stacked IC chips. However, due to the large CTE mismatch between Silicon and Copper, thermal stresses are induced by various thermal histories from the device processing, and they have caused serious concerns regarding the thermal-mechanical reliability.

Firstly, a semi-analytic approach is introduced to understand stress distributions in TSV structures. This is followed by application of finite element analysis for more accurate prediction of stress behavior according to the real geometry of the sample. The conventional Raman method is used to measure the linear combination of in-plane stress components near silicon top surface

Secondly, the limitation of conventional Raman method is discussed: only certain linear combination of in-plane stress, instead of separate value for each stress components, can be obtained. Two different kinds of innovative Raman measurements have been developed and employed to study the normal stress components separately. Both of them take advantages of different laser polarization profiles to resolve the normal stress components separately based on experimental data. The top-down Raman measurements utilize so called "high NA effect" to obtain additional information, and can resolve all 3 normal stress components. Independent bending beam experiments are used to validate the results from cross-section Raman measurement on the same sample. The correlation between top-down Raman measurement and cross-section Raman measurement are investigated as well.

Lastly, as a typical example of 3D IC package, a stack-die memory package is presented. Finite element analysis combined with cross-section Raman measurement and high resolution moiré interferometry were employed to investigate the thermal-mechanical reliability and chip-package interaction of the stack-die memory structure.

Table of Contents

List of Tables xi

List of Figures xii

Chapter 1 Introduction 1

1.1 Background and motivation 1

1.1.1 Conventional interconnects and packaging methods 1

1.1.2 Cu/low-k interconnect 2

1.2 3-D integration with through-silicon Vias (TSVs) 3

1.2.1 Process flow for TSV fabrication 6

1.2.2 Reliability concerns in TSV structure 7

1.3 Scope of this thesis...9

Chapter 2 Near-Surface stress measurement with conventional raman measurement...11

2.1 Underlying theory of Raman spectroscopy...11

2.2 Effect of stress on the Raman modes of Silicon 14

2.3 Experimental descriptions..16

2.4 Analysis of near-surface stresses 17

2.5 Comparison between Raman and FEA results......................................22

2.6 Residual stress in oxide...24

2.7 Characterization of via stress field interaction.....................................26

2.8 Summary 28

Chapter 3 Extension of micro-Raman spectroscopy for full-component stress characterization of TSV structures 29

3.1 Top-down Raman measurement for full stress components determination 30

3.1.1 Secular equation in sample coordinates system.........................30

3.1.2 Raman measurements with high numerical aperture (NA) Configuration 31

3.1.3 Laser power, accumulation time optimization...........................37

3.1.4 Experimental design and results 39

3.1.5 Analysis and validation 42
3.2 Cross-section Raman measurements 45
3.2.1 Secular equation for cross section Raman measurements 45
3.2.2 Experimental samples and sample preparation..........................48
3.2.3 Experimental results, FEA simulations and analysis..................50
3.3 Bending beam experiments 55
3.4 Correlation between Raman measurement using high NA effect and cross-section Raman measurement..59
3.5 Summary..60
Chapter 4 Thermo-mechanical reliability of stack-die memory package............62
4.1 Introduction...62
4.2 Test structures 62
4.3 Finite element method for Stack-die memory structures........................64
4.3.1 Secular equation for cross section Raman measurements 64
4.3.2 Modeling of stack-die memory structure 71
4.4 Package level deformation..73
4.5 Impact of CPI on stress/strain distribution around TSV........................74
4.6 Characterization of thermo-mechanical behavior of stack-die memory package with high resolution moiré interferometry............................77
4.6.1 Regular moiré interferometry 78
4.6.2 Sample preparation and measurement 79
4.6.3 Results and discussion 81
4.6.4 High resolution moire interferemetry 81
4.7 Summary...86
Chapter 5 Conclusion and Outlook...87
5.1 Conclusion 87
5.2 Outlook 89

Appendix Sub-modeling Technique 91
Reference 97
Vita………………...102

List of Tables

Table 2.1: Polarization selection rules for back scattering from a (001) surface 13

Table 2.2: Thermomechanical properties used in finite element analysis 21

Table 3.1: Intensity for different Raman peaks under given polarization configuration 33

Table 3.2: Intensity for different Raman peaks vs. Polarization (Cross-Section Raman) 47

Table 3.3: Raman peak shift vs. stress distribution under different polarization 47

Table 4.1: Material property used for FEA simulation 69

Table 4.2: Material property used in FEM for stack-die memory structure 73

List of Figures

Figure 1.1: Illustration of a flip-chip packaging..1

Figure 1.2: Scaling effect on RC delay in interconnects......................................3

Figure 1.3: Gate and interconnect delay versus feature size [3]...........................4

Figure 1.4: Schematic diagrams showing the difference between 2-D and 3-D interconnects: (a) 2-D SiP integration; (b) SOC integration; (c) 3-D integration. [11]..5

Figure 1.5: Illustrations of Cu interconnect with TSV in 3-D stack die memory [Source: Matrix Semiconductor Inc.] 6

Figure 1.6: Via-middle process for TSV structures [16]......................................7

Figure 1.7: Mechanical issues in TSV structures [Source: Samsung [17]]: (a) Interfacial delamination; (b) Silicon Cracking; (c) Via extrusion (Pop-up) 9

Figure 2.1: Feynman diagram and related energy levels for a first-order Stokes scattering process [25] 13

Figure 2.2: Picture of Renishaw inVia Raman system.......................................17

Figure 2.3: Schematic of (a) fully filled TSV structure near the wafer surface; (b) top view of a 2 by 2 TSV array; (c) illustration of Raman scan path illustration...17

Figure 2.4: Near-surface stresses around an isolated TSV without oxide layer predicted by the semi-analytical solution ($\Delta T = -100^o C$, $D = 10$ µm). (a) Stress components at z = 0.2 µm; (b) Sum of the in-plane normal stresses at different depths[28]..20

Figure 2.5: Distributions of the stress sum ($\sigma_r + \sigma_\theta$) near the wafer surface (z = 0.3 μm) for (a) an isotropic Si model and (b) an anisotropic (001) Si wafer. [28] 22
Figure 2.6: (a) Measured Raman intensity and frequency for a TSV specimen with the surface oxide layer polished off. (b) Comparison of the near-surface stress distribution between Raman measurements and finite element analysis. Vertical dash lines indicate the Cu/Si interfaces ..23
Figure 2.7: Comparison of the near-surface stress distribution between Raman measurements and finite element analysis, for a TSV specimen annealed at 300°C for 1hr 24
Figure 2.8: (a) Raman peak shift around two adjacent TSV w/o copper; (b) Comparison of Raman peak shift between experimental data in (a) and FEA at z=0.2um with different residual stress in oxide layer....25
Figure 2.9: Raman peak shift and Intensity with D= 5um and pitch size of (a) P=9um; (b) P=11um; (c) P=12um; (d) P=20um 27
Figure 3.1: (a) Experimental set-up and (b) illustration of optical path for high numerical aperture 31
Figure 3.2: (a) Raman Spectrum for bare 100 wafers measured with 5X objective Lens. (b) Raman spectra measured for bare 100 wafer with 20X (NA =0.40), 50X (NA=0.75), 100X (NA=0.85) (c) “forbidden band” intensity as a function of numerical aperture (NA) 37
Figure 3.3: Spectrums of different Raman modes in experiment....38
Figure 3.4: Peak Position fluctuation vs. laser power 39

Figure 3.5 (a) Illustration of scan path along [110] for the 2x2 TSV arrays and Raman peak shifts results along scan path for (b) sample A and (c) sample B..41
Figure 3.6: (a) Modeling of a quarter structure and (b) in-plane shear stress distribution in Si around TSV for 2 by 2 TSV arrays.......................42
Figure 3.7: Comparison between experimental determined stress distribution and prediction of FEA simulation (a) Sample A annealed at 200C for 2 hours (Thermal load of -80C is used in FEA model) (b) Sample B annealed at 300C for 2 hours (Thermal load of -280C is used in FEA model)..44
Figure 3.8: Illustration of the Geometry of Sample 1 and Sample 2...................49
Figure 3.9: Schematic of experimental set-up for Raman spectroscopy.............50
Figure 3.10: Raman peak shift along the scan path for (a) Sample 1 (Annealed at 200C) (b) Sample2 (annealed at 400C). The experimental data are plotted by blue circle (Raman Peak shift under polarization 1) and red triangle (Raman peak shift under polarization 2), and the FEA simulated Raman peak shift are plotted as dotted line. RT=20C......52
Figure 3.11: Visual illustration of the 3D FEA model...53
Figure 3.12: Normal stress distribution for Sample 2 on cross-section at 5μm under TSV top surface..54
Figure 3.13: Comparison of the in-plane stresses distribution between Raman measurements and finite element analysis (FEA)............................55
Figure 3.14: Illustration of the bending beam system. [Taken from [37]]............57
Figure 3.15: Spatial relationships for the curvature calculation of specimen 57

Figure 3.16: Bending beam measurement for sample 1 and sample 2 in section 3.2 58

Figure 3.17: (a) Illustration of cross-section of region of measurement of sample B, x axis is along [110], y axis is along [001], and z axis is along [1-10] (b) Comparison of cross-section Raman measurement on sample B and FEA simulation results, a thermal load of -280C was used for FEA model 60

Figure 4.1: Illustration diagram for stack-die memory structure (from top), units: mm 63

Figure 4.2: Cross-section of stack-die memory structures 63

Figure 4.3: A representative volume element for a TSV array with x axis along [110], y axis along [1-10], z axis along [001]..................................67

Figure 4.4: (a) FEM model for one quarter of the BB sample, the TSV arrays are replaced by equivalent composite material with effective moduli. (b) Out of plane displacement of top surface under a thermal load of -300C..70

Figure 4.5: Comparison of beam curvature obtained from BB experiment (hollow circle) and FEM simulation with effective moduli method (solid circle and solid triangle). 70

Figure 4.6: (a) A half section FEM Model of stack die structure with symmetric boundary condition. (b) Same FEM model with EMC made transparent to show detailed structure under EMC. (c) TSV and solder level sub-model 72

Figure 4.7: Comparison of FEA and profilometer results of thermal deformation for the stack-die memory package 74

Figure 4.8: Illustration of sample preparation and locations of Cross-section Raman measurements in a die stack structure. 75
Figure 4.9: (a) Inset illustrating scan location of cross-section Raman measurement (b) Comparison of peak shift results from FEM and experimental measurement, -200C thermal load is used for FEM model. (c) Stress distribution at the measurement location calculated from FEA with sub-modeling technique..77
Figure 4.10: Optical system of moiré interferometer (Taken from [45]) 79
Figure 4.11: Optical image of sample cross-section 80
Figure 4.12: Modified PEMI for moiré test (taken from [45]).............................81
Figure 4.13: Fringe pattern for stack-die memory package for a thermal load of -60C (a) U field (b) V field...82
Figure 4.14: Phase maps for stack-die memory package 83
Figure 4.15: Phase maps of stack-die memory package with 8X resolution.........84
Figure 4.16: Shear strain distribution in the region of interest.............................85

Chapter 1 Introduction

1.1 Background and motivation

1.1.1 Conventional interconnects and packaging methods

In the manufacture of modern computer chips, the process flow can be divided into two steps: Front-End-of-the-Line (FEOL) process and Back-End-of-the-Line (BEOL) process. In the FEOL process, individual devices, such as transistors which amplify and switch electronic signals, are patterned and fabricated on the surface of a silicon wafer. Subsequently, in the BEOL process, insulating layers (dielectrics) and metal lines are deposited and fabricated to interconnect the devices on the wafer.

Chips are then integrated into chip package (or semiconductor device assembly) through several methods, such as the mature technology involving series of steps including die attach, wire bonding, and IC encapsulation and an advanced technology with flip chip packaging, etc. Particularly, in the flip chip packaging method, the silicon chip is flipped face down and electrically connected to the substrate through an area array of solder bumps. Fig 1.1

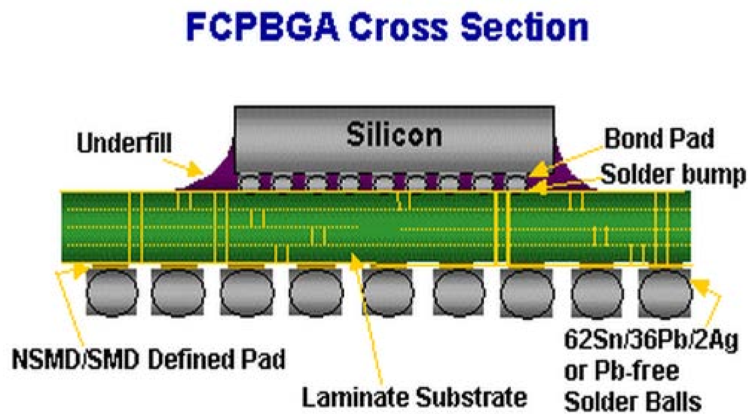


Fig. 1.1 Illustration of a flip-chip packaging [Source: Freescale website]

The flip chip method offers several advantages, such as smaller packaging size, large I/O density, and higher performance and reliability, and it is widely used as the current packaging technology.

1.1.2 Cu/low-k interconnect

The proposal of doubling the number of transistors on an IC chip every 24 months by Gordon Moore in 1965 (also called Moore's law) has been the most powerful driver for the advancement of the microelectronics industry in the past 46 years. This law emphasized lithography scaling and integration (in 2D) of all functions on a single chip, perhaps through system-on-chip (SoC). [1] The challenges are mainly due to the interconnect delays, also known as Resistive-capacitive (RC) delay, which can be expressed by the following formula [2]

$$RC = 2\rho\kappa\varepsilon_0\left(\frac{4L^2}{P^2} + \frac{L^2}{T^2}\right) \quad [1.1]$$

where $P = W + S$ is the pitch size between the neighboring interconnects, L is the line length, W is the interconnect line width, T is the height of the interconnects, ρ is the resistivity of the interconnect materials, κ is the dielectric constant of the dielectric materials between the interconnect lines, and ε_0 is the vacuum permittivity. A scaling effect on the RC delay is illustrated in Figure 1.2.

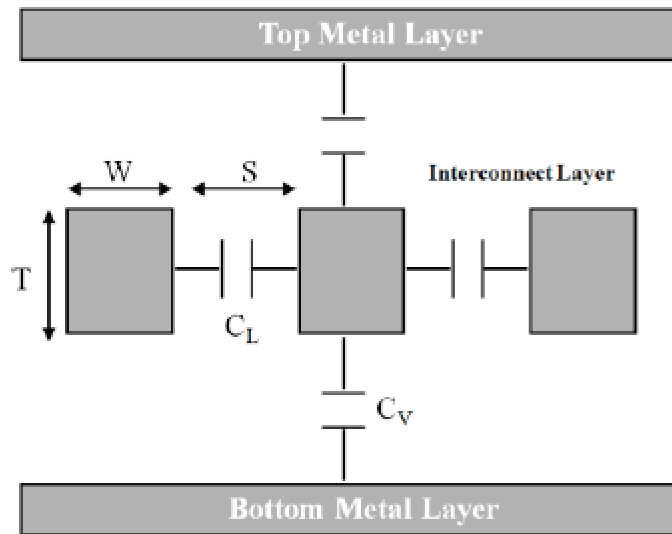


Fig. 1.2 Scaling effect on RC delay in interconnects

As shown in Figure 1.3, with the scaling of the gate length, gate oxide thickness, and junction depth, the corresponding scaling of interconnects will cause an increase in RC delay of interconnect. [3] This can limit the overall performance of the chip and cause serious challenges for future development of higher performance chips.

1.2 3-D integration with through-silicon Vias (TSVs)

3-D integration, where several classes of IC chips are stacked in the vertical direction, appears to be an effective way to overcome the wiring limitation imposed on chip performance, device density and power consumption beyond the current technology. [4] [5] [6] The 3-D integration can achieve a high circuit density and performance through a heterogeneous integration of multiple IC chips. The application of through-silicon via (TSV) is essential for 3D silicon integration and 3D IC integration [7] [8] [9]TSVs are processed either through the IC chips or in the silicon interposer to form vertical, electrical connections between stacked IC chips

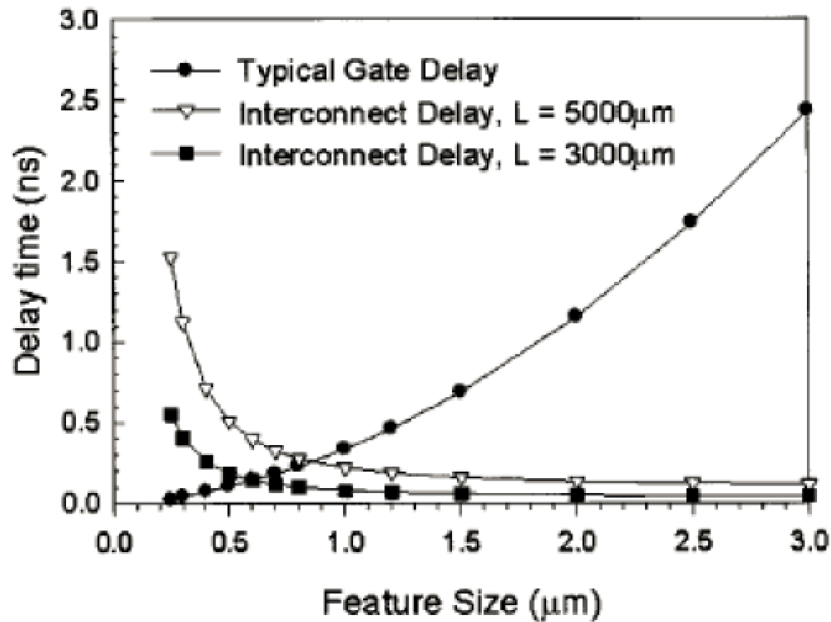


Fig. 1.3 Gate and interconnect delay versus feature size [3]

Major advantages of 3D integration include: (a) better electrical performance; (b) lower power consumption; (c) higher device density and smaller packaging form factor. [10] The benefits (a) and (b) can be interpreted from a conceptual illustration, as shown in Fig. 1.4. In Fig. 1.4(a), a logic chip and memory chip are connected by current 2-D interconnects. Wires that connect between chips can be as long as the lateral dimension of chips, i.e. a length of a centimeter scale. The relatively long transmission route could result in a signal delay that degrades the electrical performance. This is also known as the memory latency. In Figure 1.4(c), two IC chips are connected vertically using 3-D interconnects with TSVs. The wiring distance between two chips, if properly designed, can be as short as the vertical dimension between the chips, which is usually in the micron scale. Consequently, 3-D infrastructures can significantly reduce the memory latency and hence improve the chip performance.

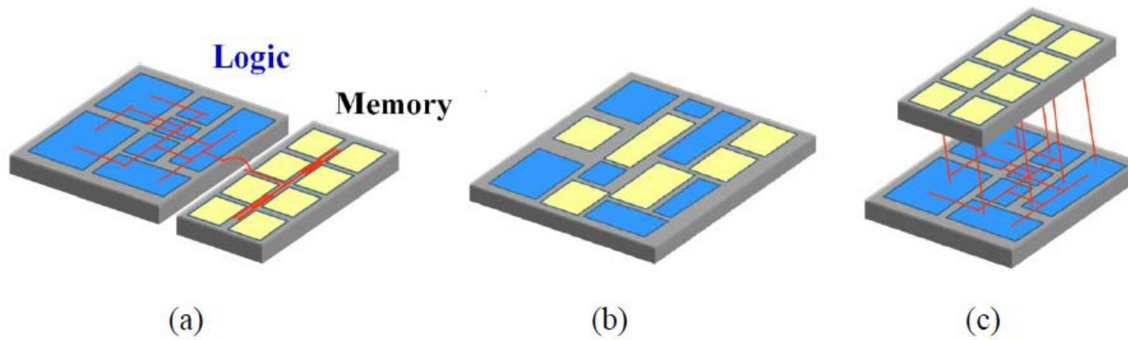


Fig. 1.4 Schematic diagrams showing the difference between 2-D and 3-D interconnects: (a) 2-D SiP integration; (b) SOC integration; (c) 3-D integration. [11]

The other benefit of 3-D integration is to increase the device density while to reduce the package form factor. An example of interconnects of Matrix 3D memory is illustrated in Figure 1.5. By stacking chips together, the device density in the unit area is increased by 4 times equivalently. In the meanwhile, by wafer-thinning, the total package thickness won't increase or even decrease. Therefore, 3-D integrated memory has a tremendous potential for mobile communication devices since it enables massive data storage in a more limited space

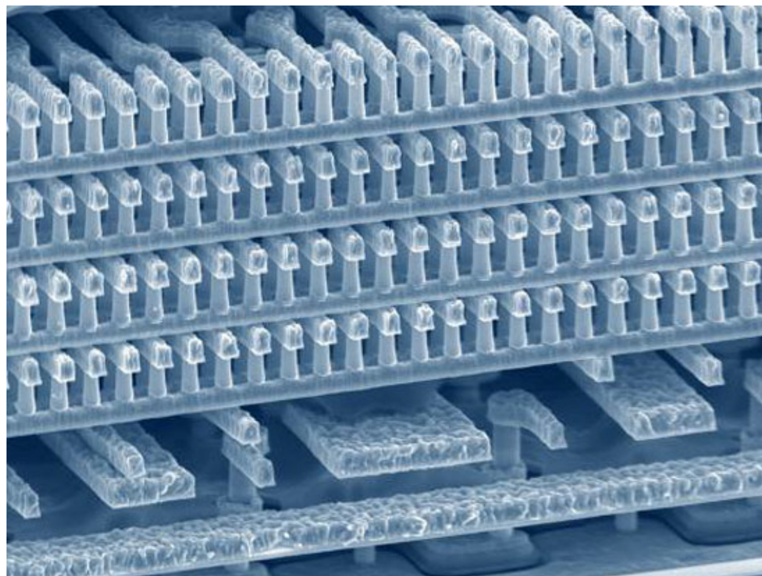


Fig. 1.5 Illustrations of Cu interconnect with TSV in 3-D stack die memory [Source: Matrix Semiconductor Inc.]

1.2.1 Process flow for TSV fabrication

The fabrication of TSVs involves three key processes [12] [13] [14] [15]: 1) via hole etching, 2) TSV filling by electroplating, and 3) Si wafer thinning and wafer bonding/deboning. Depending on when the TSV processing is done in the interconnect fabrication, the terms such as via first, via middle, and via last have evolved. Currently, the via-middle process is the most popular, and it is described in more detail below.

Via middle process

Fig 1.6 schematically illustrates the via-middle process, which is performed in between the FEOL and the BEOL fabrication process. A typical via-middle process to fabricate TSVs with a diameter of 10um and a depth of 50um in the Si substrate is described as the following. First, lithography is done to pattern via openings across the wafer. Second, Deep reactive-ion etching DRIE is used to create via holes of desired dimensions. This is then followed by deposition of oxide liner on the via side walls. The oxide layer reduces capacitance and improves electrical isolation between the TSVs and the silicon substrate. To prevent diffusion of Cu into Si substrate, a thin barrier layer (50nm usually) of Ta/TaN or Ti/TiN is deposited after the oxide layer. Third, a thin Cu seed layer is first deposited on the barrier layer and then the vias are filled by the electroplating process. A subsequent annealing step could be applied to stabilize the Cu grain structures and relax the residual stresses. Fourth, CMP is conducted to remove the Cu overburden, Ta/TaN layers and oxide liner. The fabrication of TSV structure is followed by the BEOL process in which interconnects are made and bonding pads are patterned. Finally, the Si substrate is thinned down to the optimized TSV height to expose the bottom of the TSV for the following BEOL process.

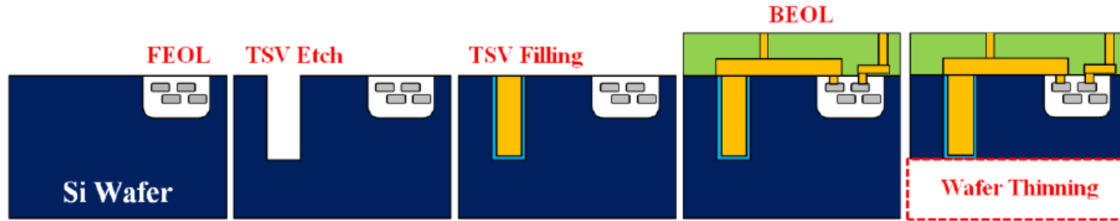


Fig. 1.6 Via-middle process for TSV structures [16]

1.2.2 Reliability concerns in TSV structure

As there are two side of a coin, when taking advantage of 3-D integration, the reliability concerns has been raised due to the introduction of TSV into the package. Due to the CTE mismatch between the Cu and silicon, thermal stresses are introduced during processing and thermal cycling of the TSV structures. [16].The thermal stress can cause interfacial delamination, cracking of Si, and mobility degradation of stress-sensitive devices.

Protrusion, also called pop-up, of TSV during the thermal treatment is another frequently observed failure mode for TSV.(Fig. 1.7a) The protrusion of TSV can cause further mechanical failures, such as cracking or lifting of the dielectric layers built up over TSVs. (Fig 1.7b, Fig. 1.7c) [17]The via pop-up phenomenon is considered to be combined results of several different mechanisms, such as microstructure evolution of copper in TSV, the boundary diffusion of Cu along the liner oxide, etc. Among all those factors, the thermal stress induced by the CTE mismatch is still considered to be the most important part, which will cause Cu to be deformed plastically.

To understand the failure mechanisms in the TSV structures, it is essential to experimentally characterize the induced stresses and material behaviors under thermo-mechanical conditions equivalent to TSV fabrication.

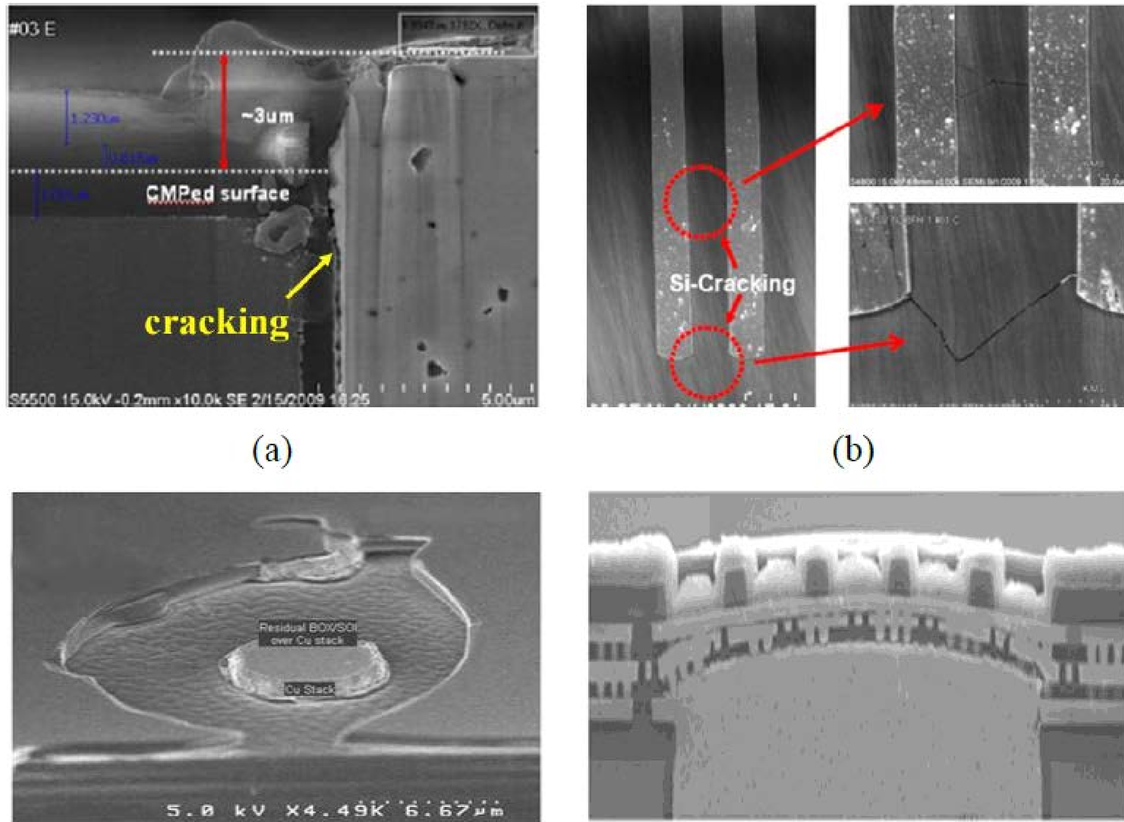


Fig. 1.7 Mechanical issues in TSV structures [Source: Samsung [17]]: (a) Interfacial delamination; (b) Silicon Cracking; (c) Via extrusion (Pop-up)

1.3 Scope of this thesis

In this thesis, analytic and numerical approaches are applied, along with experimental measurements to study thermal mechanical reliability issues in TSV for 3-D integration. Thermal stresses of TSV structures are analyzed. Raman spectroscopy is chosen to be the main method for experiment. [18] [19] [20] [21] [22] A comprehensive understanding is established for the thermo-mechanical stress and reliability of TSV structures. This thesis is organized as follows.

As an introduction, Chapter 1 presents a brief review of background and motivation for this work. This chapter covered the conventional interconnect and packaging scheme as well as the current challenge related to the interconnect. As an effective solution to overcome the

challenges, the advantages of 3D integration are introduced and the via-middle fabrication processes are described.

In chapter 2, a brief review of Raman spectroscopy is presented as well as the physics behind it, and then the Raman spectroscopy is employed to measures a certain combination of the near-surface stresses for periodic TSV arrays. The results are compared with semi-analytic solution as well as finite element analysis (FEA) to gain comprehensive understanding of the stress distribution. Moreover, the effect of residual stress in both side wall and top oxide layer and interaction of stress field from an adjacent via are evaluate experimentally.

In chapter 3, two innovative Raman techniques for stress measurement are presented and employed to the TSV structure for the stresses characterization. First, by introducing the so called "High numerical aperture" effect, additional information is obtained under a proper polarization configuration. Based on this method, all the normal stress components can be obtained from the experimental data. Second, Raman measurement on the axial cross-section of the TSV structure is presented. By controlling the polarization of the scattering light, two different Raman peak shift trends can be observed on the same scan location. With proper assumption based on FEA simulation, in-plane stress components can be determined on the cross-section of TSV from experimental data. These Raman results are verified by independent bending beam experiments in the last part of this chapter

Chapter 4 focuses on the thermal reliability characterization on the stack-die memory structure. Various experimental methods such as Moiré interferometry and profilometer are applied to characterize the package level deformation, and cross-section Raman measurements are applied to characterize the local strain distribution around TSV. An effective module method

is developed based on finite element analysis (FEA) for evaluating the package level thermal mechanical behavior. Combing with the sub-modeling technique, the local strain field near TSV is obtained by FEA. Experimental and simulation results are compared and analyzed.

In conclusion, Chapter 5 summarizes the results from the present study and suggests potential directions for the future work.

Chapter 2 Near-Surface Stress Measurement with Conventional Raman Spectroscopy

2.1 Underlying Theory of Raman spectroscopy

For short, Raman scattering or the Raman effect is the inelastic scattering of a photon due to photon-phonon interactions. It was first discovered by C. V. Raman and K. S. Krishnan in liquids [23], and by G. Landsberg and L. I. Mandelstam in crystals [24]. Different formularization are used to explain the mechanism of Raman scattering [25] [26] [27], and here the approach presented in [25] is followed. The collective lattice vibration can be described by means of phonon:

$$Q_j = A_j \exp[\pm(q_j \cdot r - \omega_j t) \qquad [2.1]$$

For each possible vibration j, q_j represents the wave vector and ω_j represents the frequency. Q_j is the normal coordinate of the vibration and A_j is a constant. When monochromatic light of frequency ω_i is incident on a crystal in a direction $\mathbf{k_i}$, the associated electric field **E** will induce at position **r** an electric moment **P**, which is related to **E** through

$$P = \varepsilon_0 \boldsymbol{\chi} \cdot E_0 \exp[i(k_i \cdot r - \omega_i t)] \qquad [2.2]$$

where, χ is the susceptibility tensor, which describes the response of the crystal to the electric field [25]. χ is a function of lattice vibration, and can be expanded in Taylor series with respect to the normal coordinate of the vibration Qj:

$$\chi = \chi_0 + (\frac{\partial \chi}{\partial Q_j})_0 Q_j + (\frac{\partial \chi}{\partial Q_j \partial Q_k})_0 Q_j Q_k + \cdots \qquad [2.3]$$

The first term in equation [2.3] corresponds to elastic scattering of photon, which is also known as Rayleigh scattering. The second and third term give rise to the first order and second order Raman scattering respectively. Higher order terms in equation [2.3] are ignored. Substituting equation [2.3] into [2.2] yields:

$$P = \varepsilon_0 \chi_0 \cdot E_0 \exp[i(k_i \cdot r - \omega_i t)] + \varepsilon_0 E_0 (\frac{\partial \chi}{\partial Q_j})_0 A_j \exp\left[-i\left(\omega_i \pm \omega_j\right)t\right] \exp[i\left(k_i \pm q_j\right) \cdot r\right) \quad [2.4]$$

If $(\frac{\partial \chi}{\partial Q_j})_0$ is non-zero, besides the Rayleigh scattering light, the scattering light with frequency of $\omega_i + \omega_j$ and $\omega_i - \omega_j$ will be observed as well, which corresponds to anti-Stokes and Stokes Raman scattering, respectively. The intensity of the scattering light is given by

$$I = C \sum_j \left| e_i \cdot R_j \cdot e_s \right|^2 \qquad [2.5]$$

Where C is a constant and R_j is the Raman tensor of the phonon j. The R_j are second-rank tensors and coordinate system dependent. For silicon, under coordinate system x//[100], y//[010] and z//[001], the Raman tensor is in the form of:

$$\boldsymbol{R_1} = \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & d \\ 0 & d & 0 \end{pmatrix}, \quad \boldsymbol{R_2} = \frac{1}{\sqrt{2}} \begin{pmatrix} 0 & 0 & d \\ 0 & 0 & 0 \\ d & 0 & 0 \end{pmatrix}, \quad \boldsymbol{R_3} = \begin{pmatrix} 0 & d & 0 \\ d & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} \qquad [2.6]$$

By combining equation [2.5] and [2.6], the polarization selection rule for back scattering from a (001) surface can be determined as shown in Table 2.1

Table 2.1 Polarization selection rules for back scattering from a (001) surface [25]

Polarization		Visible		
e_i	e_s	R_x	R_y	R_z
Back scattering from (001)				
(100)	(100)	—	—	—
(100)	(010)	—	—	x
(1-10)	(1-10)	—	—	x
(110)	(1-10)	—	—	—

According to Table 2.1, for back scattering from a (001) surface, only one longitudinal mode (corresponds to Rz) can be observed.

From a quantum physical point of view, Raman scattering involves the destruction of a photon with frequency ω_j, incident from a light source, and the creation of a photon with frequency ω_s. Fig. 2.1 shows a typical Feynman diagram and the related energy levels for a first order Stokes scattering process [25] , and the detailed calculation for the scattering cross-section is discussed in detail in [27].

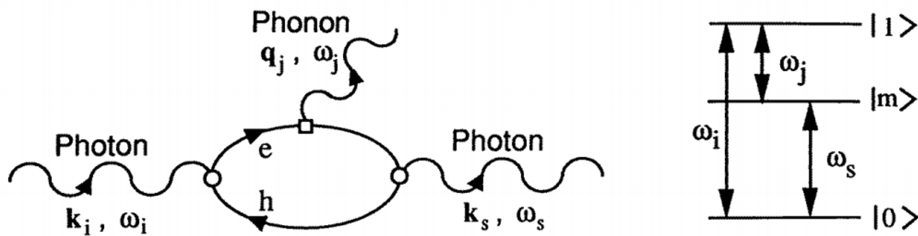


Figure 2.1 Feynman diagram and related energy levels for a first-order Stokes scattering process [25]

2.2 Effect of Stress on the Raman Modes of Silicon

One of the first papers addressing theoretically the effect of stress on the Raman modes was that by Ganesan *et al* [28]. The famous secular equation is introduced to describe the relation between presented strain and frequency of Raman scattering [28] [29]. Under the crystal coordinate system x // [100], y //[010] and z// [001], secular equation is in the form of

$$\begin{vmatrix} p\varepsilon_{11}+q(\varepsilon_{22}+\varepsilon_{33}) & 2r\varepsilon_{12} & 2r\varepsilon_{13} \\ 2r\varepsilon_{12} & p\varepsilon_{22}+q(\varepsilon_{33}+\varepsilon_{11}) & 2r\varepsilon_{23} \\ 2r\varepsilon_{13} & 2r\varepsilon_{23} & p\varepsilon_{33}+q(\varepsilon_{11}+\varepsilon_{22}) \end{vmatrix} - \lambda\mathbf{I} = 0$$

[2.7]

Here p, q and r are the material constants, the so-called phonon deformation potentials. The difference between the Raman frequency of each mode in the presence of stress, and in the absence of stress, ω_0, can be calculated from the eigenvalues λ_j:

$$\lambda_j = \omega_j^2 - \omega_{j0}^2 \; or \; \Delta\omega_j = \omega_j - \omega_{j0} \approx \frac{\lambda_j}{2\omega_{j0}} \qquad [2.8]$$

In principle, with known strain distribution in silicon, all three Raman modes (two transverse optical modes and one longitudinal optical mode) can be solved by combining equation [2.7] and [2.8]. Those Raman peaks are usually indistinguishably close, so generally, the Raman measured is the weighted average of all 3 modes:

$$\Delta\omega = \frac{I_1\Delta\omega_1 + I_2\Delta\omega_2 + I_3\Delta\omega_3}{I_1 + I_2 + I_3}$$

[2.9]

However, based on the selection rules in Table 2.1, only longitudinal Raman mode ($\Delta\omega_3$) is visible for back scattering from (100) surface. Now consider a specific example, the stress is assumed to be biaxial on (001) Si surface:

$$\varepsilon_{xz} = \varepsilon_{yz} = 0, \sigma_{zz} = 0$$

[2.10]

Substitute [2.10] to secular equation [2.7], combined with [2.8], the only visible Raman mode can be calculated:

$$\Delta\omega_3 \approx \frac{\lambda_3}{2\omega_0} = \frac{p\varepsilon_{zz} + q(\varepsilon_{xx} + \varepsilon_{yy})}{2\omega_0}$$

[2.11]

With Hook's law, the relation between Raman peak shift and in-plane stress can be obtained:

$$\Delta\omega_3 \approx \frac{\lambda_3}{2\omega_0} = \frac{pS_{12} + q(S_{11} + S_{12})}{2\omega_0}(\sigma_{xx} + \sigma_{yy}) \qquad [2.12]$$

Using

$$S_{11} = 7.68 \times 10^{-12} Pa^{-1}$$
$$S_{12} = -2.14 \times 10^{-12} Pa^{-1}$$
$$S_{44} = 12.7 \times 10^{-12} Pa^{-1}$$

, $p = -1.43\omega_0^2, q = -1.89\omega_0^2\ and\ r = -0.59\omega_0^2$ [29], from equation [2.12],

$$\sigma_{xx} + \sigma_{yy}(\text{MPa}) = -470\Delta\omega_3(cm^{-1}) \qquad [2.13]$$

[2.13] is under the crystal coordinate system, it can be easily converted to the equation under polar coordinate system as the sum of in-plane stresses is invariant during coordinate transformation. Thus, in polar coordinate system:

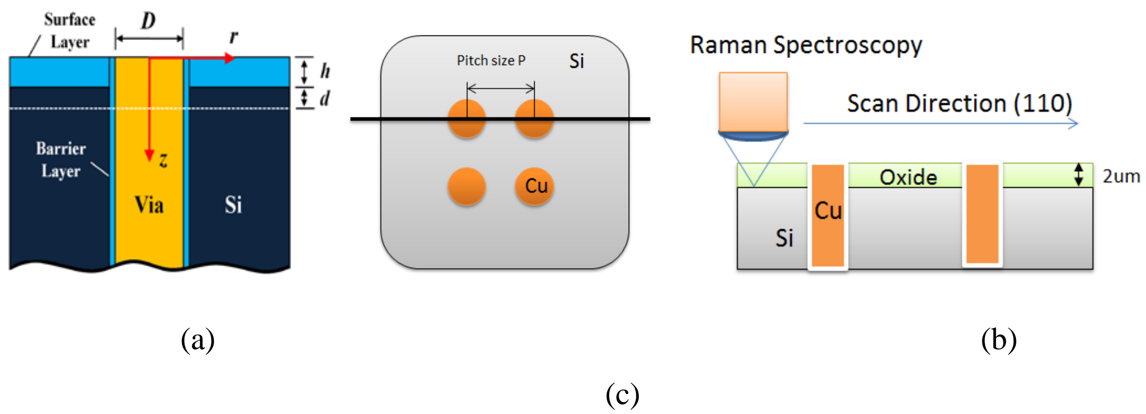
$$\sigma_r + \sigma_\theta(\text{MPa}) = -470\Delta\omega_3(cm^{-1}) \qquad [2.14]$$

From this it follows that compressive uniaxial or biaxial stress will result in an increase of the Raman frequency (positive$\Delta\omega_3$), while tensile stress will cause a decrease (negative$\Delta\omega_3$).

2.3. Experimental Descriptions

A Renishaw inVia system (Fig. 2.2) was used for the Raman measurements, equipped with 532nm laser and a focused laser spot size of about 0.8 μm by a 100x objective (NA = 0.85). Two types of TSV samples are investigated in this chapter. The Sample 1 consists of a large periodic TSV arrays. The diameter of the TSV is 10um with 50um pitch in the x direction and 40um pitch in the y direction. The depth of the TSV is 55um. The surface of silicon is coved by a thin layer (~0.2um) of oxide. The sample 2 consists of a periodic 2 by 2 arrays of Cu vias of diameter (D) of 5.5μm with a 9~20 μm pitch size. The surface of Si is covered by an oxide layer of about 2μm thickness (h). In addition, an oxide barrier layer of about 0.25 μm thick was deposited at the via/Si interface. The general structures of the TSV are similar as illustrated in Figs. 2.3 (a), (b), and (c), which show the scanning profile along (110) direction on 100 wafer across two adjacent vias. With Eq. [2.13], the sum of the two principal stresses in Si can be deduced directly from the Raman shift, which is a volume average over the region defined by the area of the focused laser spot and the penetration depth.

Fig. 2.2 Picture of Renishaw inVia Raman system



(a) (b)

(c)

Fig. 2.3 Schematic of (a) fully filled TSV structure near the wafer surface; (b) top view of a 2 by 2 TSV array; (c) illustration of Raman scan path illustration

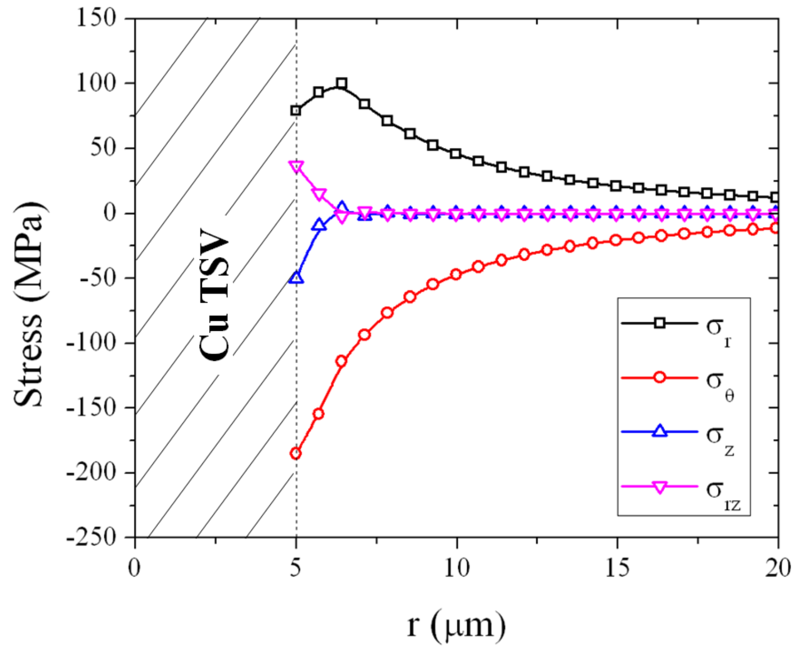
2.4 Analysis of Near-surface Stresses

An approximate analytical solution for the stress field induced by coefficient of thermal expansion (CTE) mismatch between Copper and Silicon around a circular TSV embedded in a Si

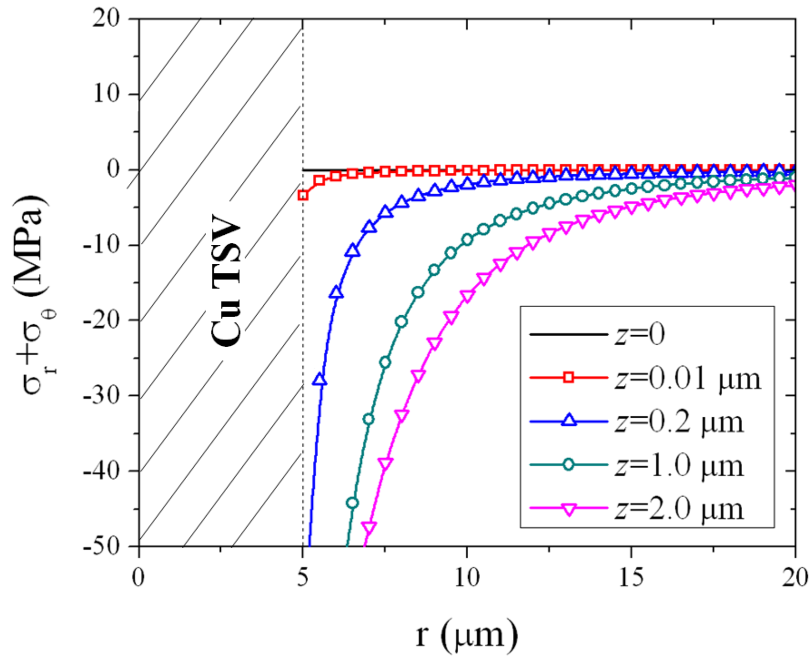
wafer was obtained by S. Ryu [30]. Using the 3D analytical solution, the sum of the in-plane stresses is studied in comparison with the Raman measurements. The sum of the radial and circumferential stresses in the TSV structures is obtained as

$$\sigma_r + \sigma_\theta = \frac{-E\varepsilon_T}{2\pi(1-\nu)} \int_0^{\frac{D}{2}} \int_0^{2\pi} \left(\frac{3z^3}{R^5} - \frac{2(1+\nu)z}{R^3} \right) \rho \, d\rho \, d\theta \qquad [2.15]$$

It is found that, while the stress sum is identically zero both at the wafer surface ($z = 0$) and far away from the surface ($z \to \infty$), it varies with the depth (z) in the near-surface region as shown in Fig. 2.4(b). The stress sum is negative everywhere for $z > 0$ and $r > D/2$, The magnitude decays monotonically as r increases and diminishes to zero far away from the via. Since the two stress components have opposite signs as shown in Fig. 2.4(a), the magnitude of their sum in Fig. 2.4(b) is relatively small. Near the wafer surface ($z < 2$ μm), the magnitude of the stress sum increases with increasing depth. This suggests that the Raman signal depends on the laser penetration depth and a typical penetration depth may be determined for the Raman measurement. On the other hand, while the stress magnitude is increasingly high approaching the Si/TSV interface, the Raman signal becomes noisy due to the reduction in the Raman intensity. Thus, the Raman data very close to the interface must be interpreted with caution.



(a)



(b)

Fig. 2.4 Near-surface stresses around an isolated TSV without oxide layer predicted by the semi-analytical solution ($\Delta T = -100^{o}C$, $D = 10\,\mu m$). (a) Stress components at z = 0.2 μm; (b) Sum of the in-plane normal stresses at different depths. [30]

Although the semi-analytical solution is a powerful tool to understand the qualitative stress distribution around TSV, the major assumptions made to simplify the results, will result in discrepancy of the stress distribution from the real case. Numerical analysis-based finite element method is utilized to gain better understanding of the stress distribution near the TSV structures. Two major assumptions are lifted in our numerical model: First, different materials in the TSV structure—the Cu via and the oxide—are considered with their elastic moduli to be taken as linear elastic and isotropic, 110GPa and 70GPa, respectively. The detailed property used in the model is listed in Table 2.2. The thin Ta layer, 0.2um thick, has negligible effect on the stress state in Si, thus ignored in the finite element analysis (FEA) for stresses. Second, the elastic anisotropy of Si is taken into account using the anisotropic elastic constants for Si crystal with a cubic symmetry. A 3-D FEA model consists of three different materials (Cu, Oxide, and Si) is used to simulate the periodic TSV array used for the Raman measurements. By symmetry, only a quarter of TSV array structure is modeled. To further reduce the computation time, the wafer thickness is taken to be 500 μm in the FEA model instead of 700 μm in the real specimen, while the TSV depth is still 55 μm. The top surface is traction free, and the out-of-plane displacement (z-direction) at the bottom surface is set to be zero. With such boundary conditions, increasing the wafer thickness has negligible effect on the near-surface stress distribution. Linear 3-D solid elements (Solid 185) in the ANSYS software are used, with a fine mesh near the surface (element size = 0.1 μm in the thickness direction and 0.2 μm in the lateral direction) and an increasingly coarse mesh away from the surface and TSV.

Table 2.2 Thermomechanical properties used in finite element analysis

Material	CTE (ppm/°C)	Young's Modulus (GPa)	Poisson's ratio
Cu	17	110	0.35
Si	2.3	130	0.28
Oxide	0.55	72	0.16

The contours of the in-plane stress sum are calculated at the depth z =0.3μm. As the stress components in out-plane direction are ignored, the summation of in-plane stress should be invariant among different coordinates system. In previous study, the summation is calculation in polar coordinates system, and the results are shown in Fig. 2.5, the summation $\sigma_r + \sigma_\theta$ is the same as $\sigma_{xx} + \sigma_{yy}$ in Cartesian coordinates. Using the anisotropic elastic property for the (001) silicon, the stress distribution as shown in Fig. 2.5b exhibits a four-fold symmetry, reflecting the cubical symmetry of silicon crystal.

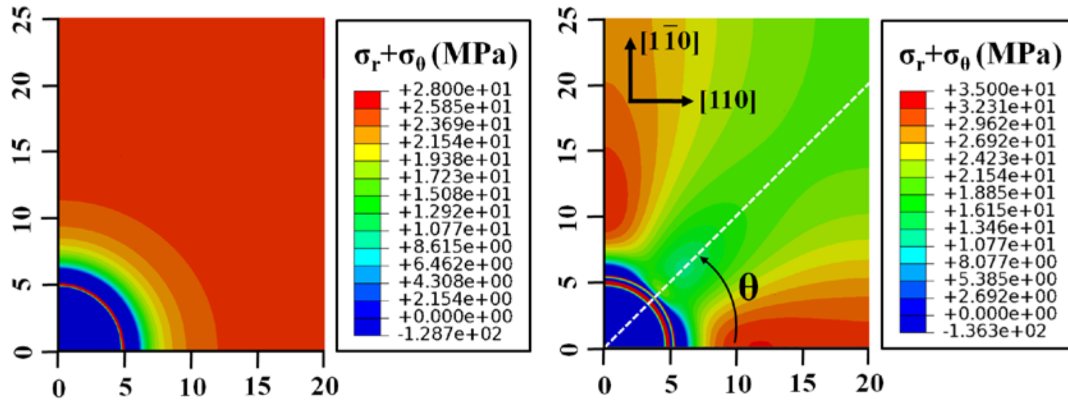
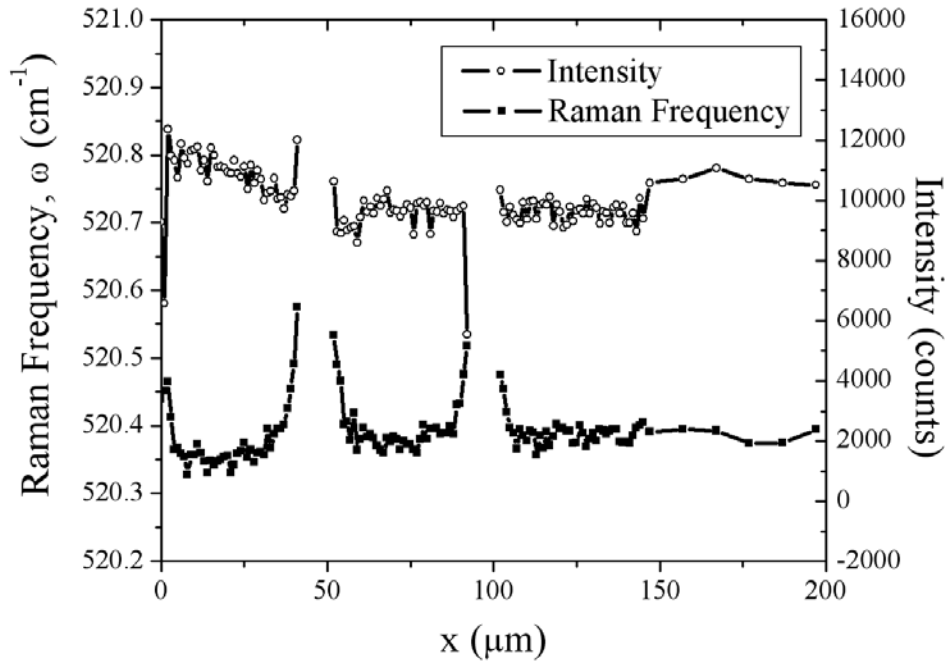


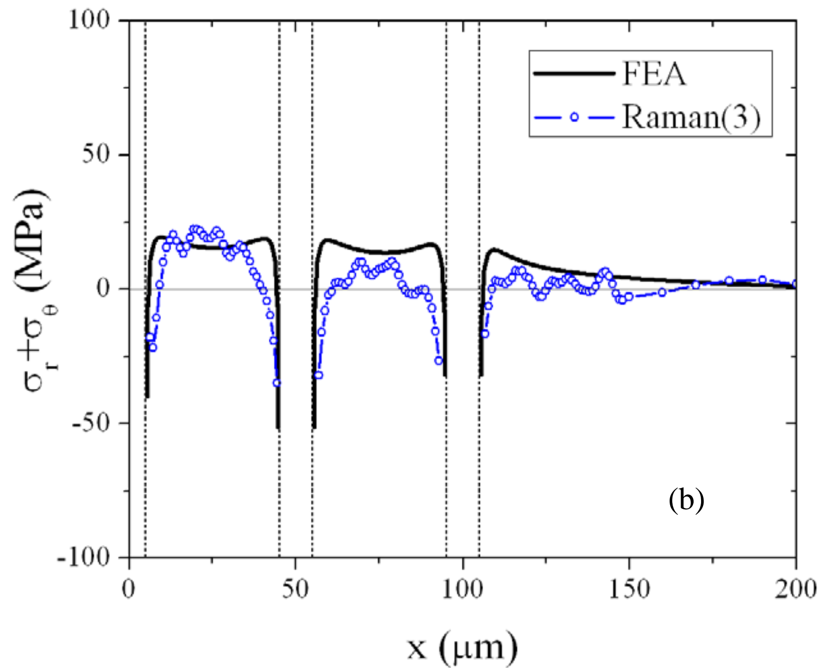
Figure 2.5 Distributions of the stress sum ($\sigma_r + \sigma_\theta$) near the wafer surface (z = 0.2 μm) for (a) an isotropic Si model and (b) an anisotropic (001) Si wafer. [30]

2.5 Comparison between Raman and FEA Results

Using Eq. [2.13], the measured Raman frequencies can be converted to the stress sum. To determine the reference frequency, ω_0, the Raman scans were not only performed between the vias but also extended to the bare silicon surface far away from the vias, where the stress sum is expect to be zero. As shown in Fig. 2.6a, the average Raman frequency obtained from the far-field measurement gives the reference frequency. For this measurement, the surface oxide layer on the TSV sample was mechanically polished, and the sample was subsequently subject to an annealing step at 200C for 2 hours. All the Raman measurements were conducted after cooling down to the room temperature. In Fig. 2.6b, the measured Raman frequencies are converted to stress summation by Eq. [2.11], to compare with the stresses obtained from the FEA model. For the FEA model, the materials (Si, Cu and Oxide) were assumed to be linear elastic. As a result, the stress magnitude from the FEA model depended linearly on the temperature change, from a reference temperature at which the stress is zero. In a separate study using the bending beam technique, the reference temperature for the TSV specimen was determined to be around 100C, and thus $\Delta T = -70\ ^oC$ [31] for the Raman measurements at room temperature. With $\Delta T = -70\ ^oC$ the results from the FEA model are in reasonable agreement with the Raman data as shown in Fig 2.6(b). It is noted that the stress magnitude is relatively low in this case, which makes the Raman measurement difficult due to the relatively large noise-to-signal ratio.



(a)



(b)

Fig. 2.6 (a) Measured Raman intensity and frequency for a TSV specimen with the surface oxide layer polished off. (b) Comparison of the near-surface stress distribution between Raman measurements and finite element analysis. Vertical dash lines indicate the Cu/Si interfaces.

Additional Raman measurements were performed for the TSV samples annealed at 300C for 1 hour. In Fig. 2.7, the stresses from the Raman measurements were compared to the FEA results with$\Delta T = -270C$. It was assumed that the annealing at 300C relaxed the stresses in the TSV specimen and thus raised the reference temperature for the induced thermal stresses upon cooling down to the room temperature. Compared to Fig. 2.6, the stress magnitude in Si has increased and fitting to the FEA results improved due to the higher reference temperature. This is consistent with the bending beam measurement reported in the literature [31]

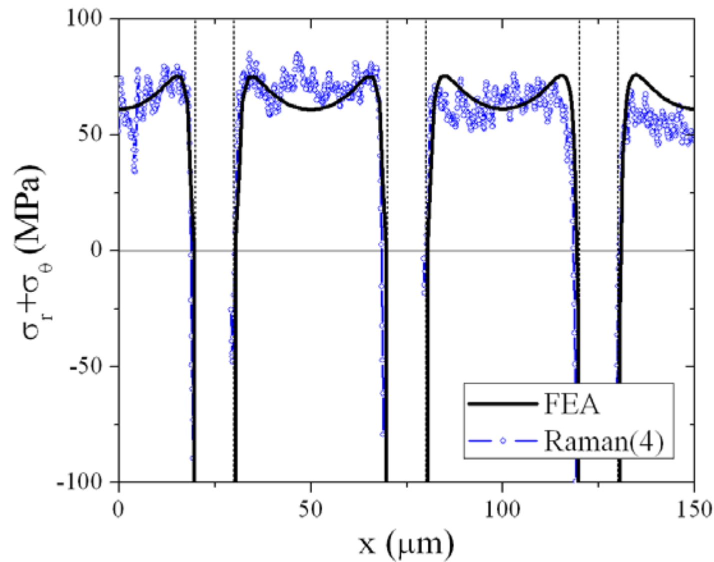
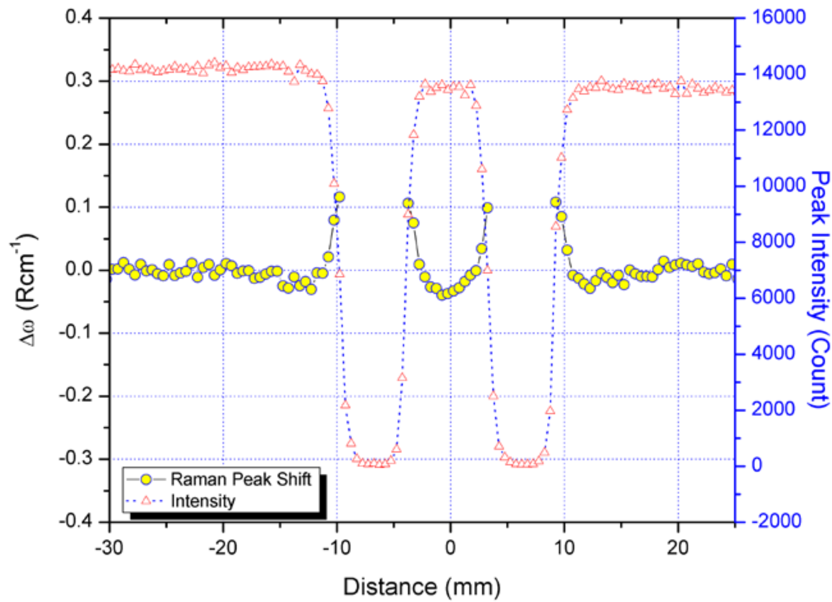


Fig 2.7 Comparison of the near-surface stress distribution between Raman measurements and finite element analysis, for a TSV specimen annealed at 300°C for 1hr.

2.6 Residual Stress in Oxide

During the study, for sample 1, comparison of the near-surface stress distribution between FEA and Raman measurements on TSV samples having top oxide layer showed a minor discrepancy. One possible explanation for the discrepancy could be the residual stress level

within the top and side wall oxide layer. For detailed study of the oxide layer effect, sample 2 is chosen as its top oxide layer is significantly higher than sample 1. A 2 by 2 TSV array on sample 2 was prepared by dipping into nitric acid to etch off copper in the TSVs, and then Raman spectroscopy was performed at room temperature (Fig. 2.8 (b)). Various residual stress levels are assumed in FEA model for comparative fitting with the experimental data. As shown in Fig. 2.8 (a), FEA with an assumption of 150MPa residual compressive stress in the oxide layer gives a better agreement with the experimental data than the assumption of 50MPa compressive stress gives. Similar level of compressive stress state in oxide thin film has been reported previously by the beam curvature technique. [31]



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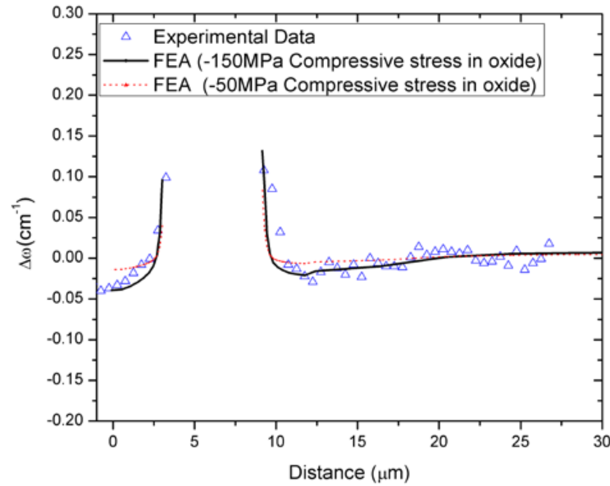
(a)



(b)

Figure 2.8 (a) Raman peak shift around two adjacent TSV w/o copper; (b) Comparison of Raman peak shift between experimental data in (a) and FEA at z=0.2um with different residual stress in oxide layer

2.7 Characterization of Via Stress Field Interaction

Thermal stresses induced in the TSV structures can affect the device performance by degrading the carrier mobility. Keep-out zone (KOZ) has been brought out as a reference for industry design. The effects due to stress interactions in a TSV array on the KOZ were investigated theoretically. The effect of stress interaction was found to depend on the ratio of pitch to diameter of the TSV array. To evaluate the stress interaction experimentally, 2 X 2 TSV arrays were annealed at 300C for 12 hours to assure full stress relaxation in copper, and then cooled down to room temperature. As shown in Figs. 2.9 (a), (b), and (c), the minima of the Raman shift between the two TSVs is non-zero, and decreases with the increase of pitch size between the two vias. This is due to the stress field interactions between the two adjacent vias. In Fig. 2.9 (d), the interaction between the two adjacent vias diminishes to nearly zero and the two adjacent vias could be considered to be isolated from each other. From the comparison among

Figures 2.9(a) through 2.9(d), it can be concluded that, for a -280C thermal load, a pitch to diameter ratio of 4 could be considered the distance where the stress interaction between the two TSVs does not exist any longer.

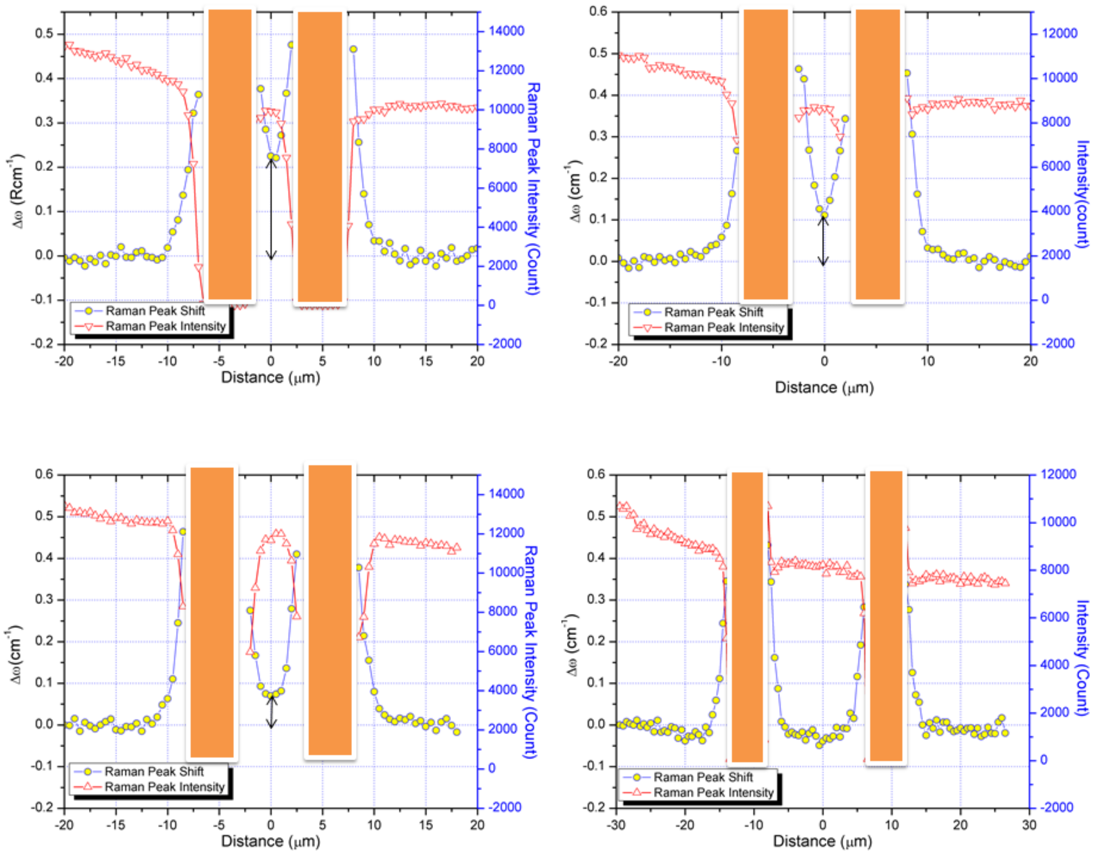


Fig. 2.9 Raman peak shift and Intensity with D= 5um and pitch size of (a) P=9um; (b) P=11um; (c) P=12um; (d) P=20um

2.8 Summary

A brief introduction to the Raman spectroscopy and the physics behind it is given. The Micro-Raman spectroscopy has been employed to study the thermal mechanical behaviors of TSV structures.

The local distribution of near-surface stress in Si has been measured, in comparison with stress analysis of the TSV structure based on a semi-analytic approach and finite element analysis. The effect of residual stress in surface oxide layer and the interaction of stress field of neighboring TSV are evaluated experimentally.

Chapter 3 High Numerical Aperture Effect and Raman Measurements

In Chapter 2, it was shown how to provide high-resolution scans of the stress distribution in Si near the TSV. However, stress mapping using the conventional Raman technique has serious limitations since it is unable to measure all the lattice vibration modes described in the Raman theory. For example, for TSVs embedded in a (001) wafer, the only measurable polarization of vibration is the longitudinal optical phonon mode along (001) [32] . Even for this vibration mode, only the sum of the in-plane normal stress components can be deduced [33]. The in-plane normal stress components near TSV surface, however, are about equal in magnitude but opposite in sign [33, 34]. Thus not only the stress components cannot be separately determined, but the magnitude of the Raman signal (for sum of the stresses) is generally quite small. This seriously limits the accuracy and usefulness of the conventional Raman technique. Finite element analysis (FEA) is commonly used to calculate the individual stress components and the results are correlated to the micro-Raman measurement. The FEA simulation has considerable uncertainties by itself and requires careful validation of the assumptions made on the material properties and the constitutive relation, e.g. elastic or elastic-plastic used in the analysis.

In this chapter, two Raman techniques, top-down and cross-section of TSV structures, were first developed to measure the normal stress components separately. Different polarization conditions and so-called "high numerical aperture (NA)" effect were utilized in the experiments to observe the different Raman modes in order to deduce additional information for the stresses. Then an independent bending beam experiment was carried out to validate the cross-section

Raman measurement. In the last part, the correlation between two different Raman measurement methods was discussed.

3.1 Top-down Raman Measurement for Full Stress Components Determination

3.1.1 Secular Equation in Sample Coordinates System

Following the discussion in Chapter 2, the following secular equation is deduced with respect to the sample system, where x//[110], y //[1-10], and z//[001]:.

$$\begin{vmatrix} A-\lambda & (p-q)\epsilon'_{12} & 2r\epsilon'_{13} \\ (p-q)\epsilon'_{12} & B-\lambda & 2r\epsilon'_{23} \\ 2r\epsilon'_{13} & 2r\epsilon'_{23} & C-\lambda \end{vmatrix} = 0$$

, where

$$A = p'\epsilon'_{11} + q'(\epsilon'_{22} + \epsilon'_{33})$$

$$B = q'\epsilon'_{11} + p'\epsilon'_{22} + q\epsilon'_{33}$$

$$C = p\epsilon'_{33} + q(\epsilon'_{11} + \epsilon'_{22})$$

$$p' = \frac{p+q}{2} + r, \quad q' = \frac{p+q}{2} - r \qquad [3.1]$$

To obtain a general solution for the secular equation is non-trivial with the presence of all six strain tensor elements. However, the out of plane shear components $(\epsilon'_{13}, \epsilon'_{23})$ are usually small because of the zero traction near the surface, and the in-plane shear components (ϵ'_{12}) can also be ignored at certain location for specific structure. In this simplified case the secular matrix is diagonal and the eigenvalues can be directly obtained as:

$$\lambda'_1 = p'\epsilon'_{11} + q'\epsilon'_{22} + q\epsilon'_{33},$$

$$\lambda'_2 = q'\epsilon'_{11} + p'\epsilon'_{22} + q\epsilon'_{33},$$

$$\lambda_3' = q\epsilon_{11}' + q\epsilon_{22}' + p\epsilon_{33}'. \quad [3.2]$$

If $\lambda_1', \lambda_2', and\ \lambda_3'$ can be determined in an experiment, three independent strains (and corresponding stress components) could be determined. However, for the conventional Raman measurement only λ_3' is visible due to the limitation of polarization directions of scattered light. [7]

3.1.2 Raman Measurements with High Numerical Aperture (NA) Configuration:

It is possible to take advantage of high numerical apertures objective for Raman measurements in directions other than the z direction on a micrometric scale. Such an experimental set up is schematically described in Fig. 3.1.

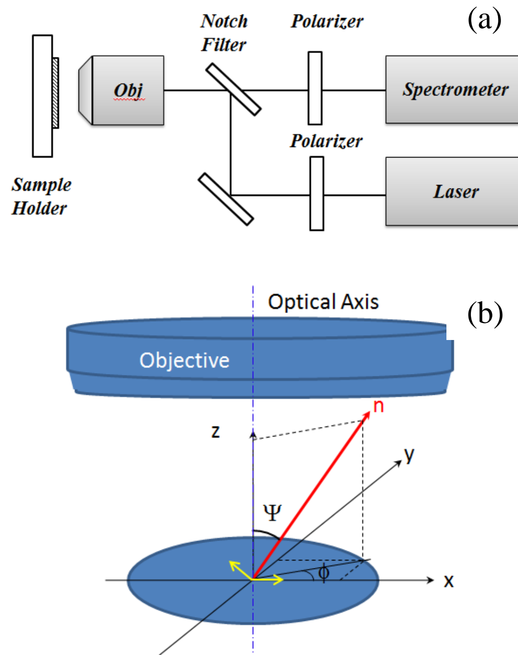


Fig. 3.1 (a) Experimental set-up and (b) illustration of optical path for high numerical aperture effect

Following E. Bonera [34], a geometrical optical model is used to describe the scattering process. Although the electric field across the focal volume is not constant due to the physical

nature of light, it is dominant in one direction and the effect from other polarized directions can be ignored. With the sample volume being considered point-like, the scattering light is not influenced by the presence of interface or optical constant inhomogeneity.

In the analysis, the sample coordinates are taken to be x//[110], y//[1-10], z//[001], where z is along the optical axis as shown in Fig. 3.1(b).

The incident light is polarized. As an example, the electric field is assumed to be along [100] direction:

$$\boldsymbol{e_i} = \left(\frac{1}{\sqrt{2}}\boldsymbol{e_x} + \frac{1}{\sqrt{2}}\boldsymbol{e_y}\right) \quad \textbf{[3.3]}$$

Following the geometrical optic model, if the polarization direction of incident and scattered beams are set to be parallel to each other, the scattered polarization measured for this configuration can be written as

$$\boldsymbol{e_s}(\boldsymbol{n}) = \frac{\boldsymbol{1}}{\sqrt{|\boldsymbol{n}\times(\boldsymbol{e_z}\times\boldsymbol{e_i})|^2}}\left(\boldsymbol{n}\times(\boldsymbol{e_z}\times\boldsymbol{e_i})\right)$$

$$\boldsymbol{n} = sin\Psi cos\phi\ \boldsymbol{e_x} + sin\psi sin\phi\ \boldsymbol{e_y} + cos\psi\ \boldsymbol{e_z}$$

Thus

$$\boldsymbol{e_s}(\boldsymbol{n}) = \frac{1}{N}(cos\psi\ \boldsymbol{e_x} + cos\psi\ \boldsymbol{e_y} - sin\psi(cos\phi + sin\phi)\ \boldsymbol{e_z} \quad \textbf{[3.4]}$$

where

$$N = \sqrt{2cos^2\psi + sin^2\psi(cos\phi + sin\phi)^2} \quad [3.5]$$

Considering an excitation with frequency ω_i, the measured intensity:

$$I_k(\hbar\omega) = C \int |\boldsymbol{e}'_s(\boldsymbol{n}) \cdot \boldsymbol{R_k} \cdot \boldsymbol{e_i}|^2 d\Omega\,, k = 1,2,3$$

where C is a constant in the form of:

$$C = \frac{\omega_i^4}{(4\pi\varepsilon)^2 c^4} E_i^2 L_k(\hbar\omega) \quad [3.6]$$

L_k is the Lorentzian line shape centered in the phonon energy, and R_k is the Raman tensor of the vibrational mode k (k=1, 2, 3) , and is calculated under the sample coordinate system as following:

$$\boldsymbol{R_1} = \frac{1}{\sqrt{2}}\begin{pmatrix} 0 & 0 & d \\ 0 & 0 & d \\ d & d & 0 \end{pmatrix}, \quad \boldsymbol{R_2} = \frac{1}{\sqrt{2}}\begin{pmatrix} 0 & 0 & d \\ 0 & 0 & -d \\ d & -d & 0 \end{pmatrix}, \quad \boldsymbol{R_3} = \begin{pmatrix} d & 0 & 0 \\ 0 & -d & 0 \\ 0 & 0 & 0 \end{pmatrix} \quad [3.7]$$

Under this condition, the following equation can be derived:

$$I_1 = C \int_0^{\Theta} \int_0^{2\pi} (\frac{\sqrt{2}}{N} dsin\psi(cos\phi + sin\phi))^2\, sin\psi\; d\phi d\psi = 0.7035 d^2 C$$

$$I_2 = I_3 = 0 \quad [3.8]$$

Similarly, the measured intensity for a different vibration mode under different polarization configurations has been calculated and listed in the Table 3.1. Table 3.1 shows that by selecting a certain set of polarization configurations, Mode 1 and Mode 2 can be measured separately from Mode 3.

Table 3.1 Intensity for different Raman peaks under given polarization configuration

$\boldsymbol{e_i}$ **(Silicon crystal)**	$\boldsymbol{I_1}$	$\boldsymbol{I_2}$	$\boldsymbol{I_3}$
$\frac{1}{\sqrt{2}}\boldsymbol{e_x}+\frac{1}{\sqrt{2}}\boldsymbol{e_y}$ (010)	**0.7035**	**0**	**0**
$\frac{1}{\sqrt{2}}\boldsymbol{e_x}-\frac{1}{\sqrt{2}}\boldsymbol{e_y}$ (100)	**0**	**0.7035**	**0**
$\boldsymbol{e_x}$ (110)	**0.3442**	**0.3442**	**2.2529**

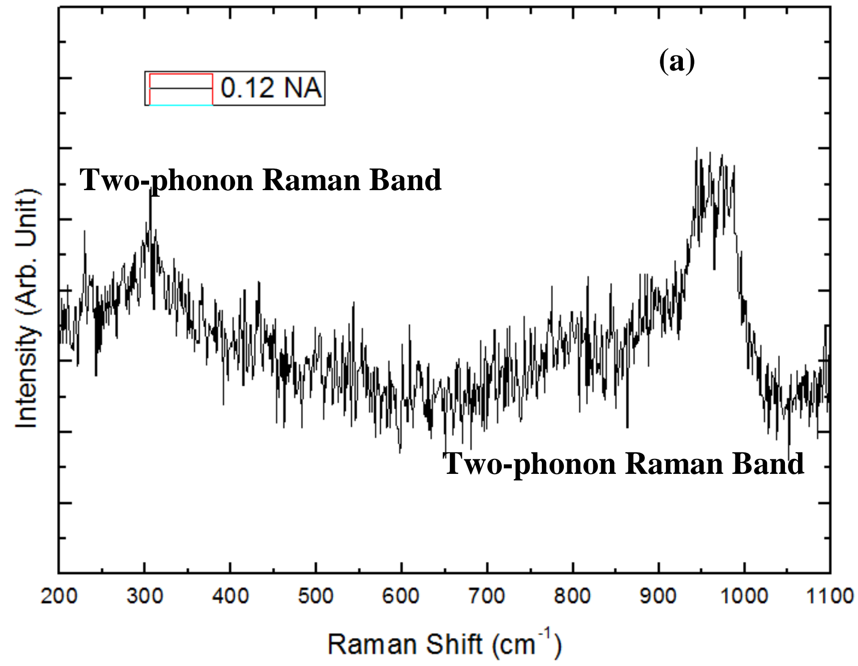
Combining with the eigenvalue solution from the secular equation, it would be possible to determine the stress components separately.

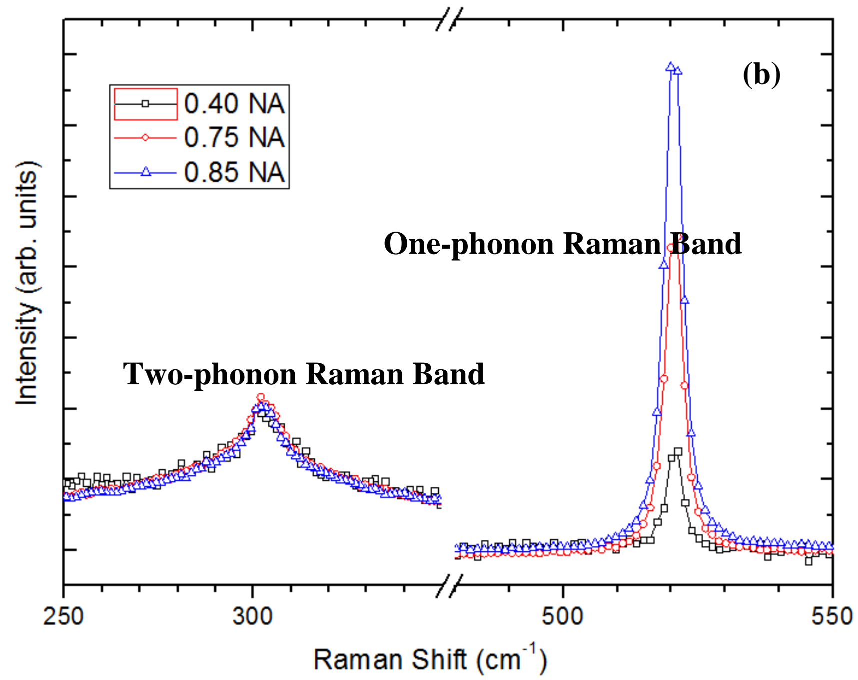
To validate the theory, the following polarization configuration was applied: The incident polarizer and scattering polarizer were parallel, and the incident light was polarized along (010) silicon crystal direction. This specific polarization configuration was chosen because the high numerical aperture effect is a secondary effect, so the signals from this effect will be low compared to that from the conventional Raman measurements (mode 3). Under this polarization configuration, from equation [3.3], the mode 3 is invisible even if there is high numerical aperture effect. In this case, the mode 3 signals will not overwhelm the signals from High NA effect, making it possible to observe other Raman modes.

Different objective lenses were applied to change the numerical aperture during the experiment. In this study, a RENISHAW InVia Raman Microscope system equipped with 532nm wavelength laser is used for the Raman measurements. A 3000 l/mm grating was installed to achieve a high resolution of the Raman peak position. The penetration depth of the 532nm laser is around 0.3μm under the Si surface.

Fig. 3.2(a) shows the Raman spectrum of stress-free Si (100) wafer measured with 5X (NA=0.12) objective lens, 532nm laser and 10mW power. As the conventional Raman measurement predicted in Table 2.1, the one-phonon band is forbidden and can't be observed in the spectra. As the numerical aperture increases, the "forbidden band" appears in the Raman spectra as shown in Fig. 3.2(b). The spectra are normalized to two-phonon Raman band at 300 cm^{-1} involving two TA phonons, as the two-phonon Raman band intensity is not sensitive to the NA.

Figure 3.2(c) shows the calculated one-phonon Raman band peak intensity vs. NA. Here, the intensity is normalized by the intensity at NA=0.85 (solid line). The ratio of intensity between NA=0.75 and NA=0.85 is experimentally determined at different laser power.


(a)
0.12 NA
Two-phonon Raman Band
Two-phonon Raman Band
Intensity (Arb. Unit)
200
300
400
500
600
700
800
900
1000
1100
Raman Shift (cm-1)


(b)
0.40 NA
0.75 NA
0.85 NA
One-phonon Raman Band
Two-phonon Raman Band
Intensity (arb. units)
250
300
500
550
Raman Shift (cm-1)

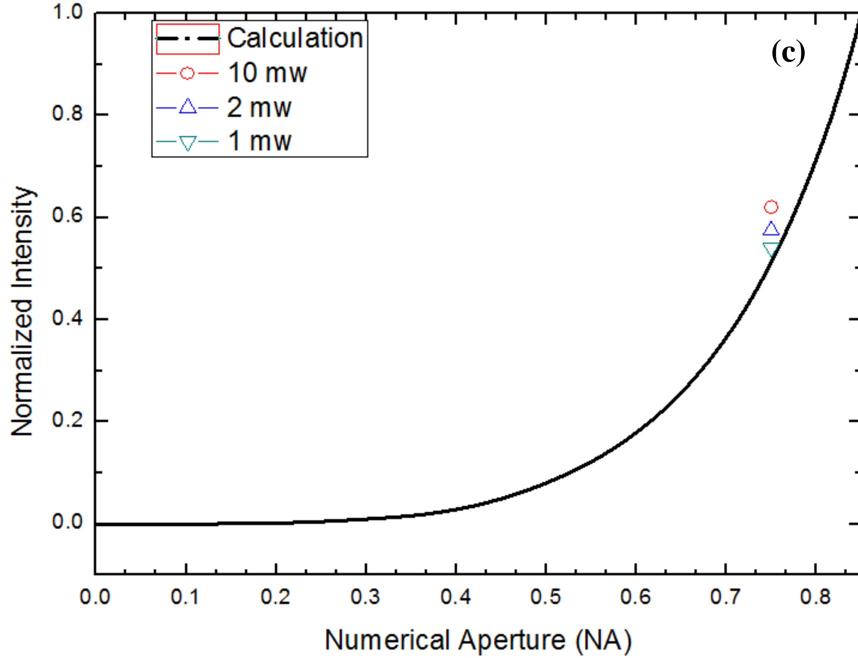


Fig. 3.2 (a) Raman Spectrum for bare 100 wafers measured with 5X objective Lens. (b) Raman spectra measured for bare 100 wafer with 20X (NA =0.40), 50X (NA=0.75), 100X (NA=0.85) (c) "forbidden band" intensity as a function of numerical aperture (NA)

3.1.3 Laser power and Accumulation Time Optimization

Although mode 1 and mode 2 are observable with high numerical aperture, the signals are weak compared to mode 3. Fig. 3.3 shows a typical silicon Raman peak of [100] stress-free Si wafer for mode 1, 2 and 3. The peak position of three modes should be the same in the absence of stress. Although the accumulation time for mode 1 and 2 was doubled compared to mode 3, the intensity of mode 1 and 2 were still much lower than that of mode 3. Lower intensity may cause high noise background and introduce a larger system error.

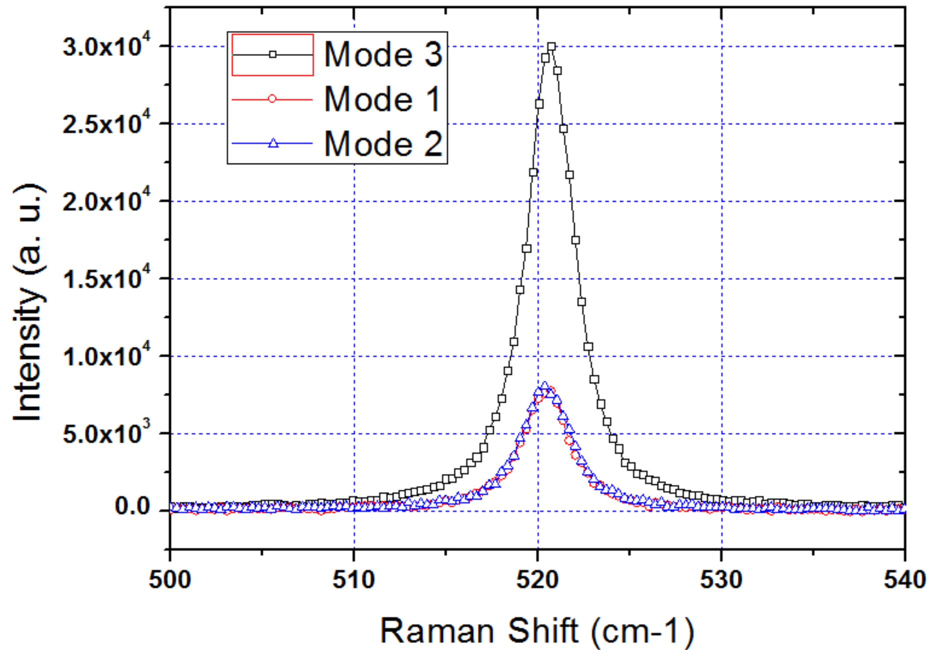


Fig. 3.3 Spectrum of different Raman modes in experiment

To determine the optimized laser power and accumulation time, and to evaluate the system error for the measurement of mode 1&2, a series of experiments with different laser power and accumulation times were carried out at the same location on a stress free bare wafer. In this case, mode 1 and mode 2 should be degenerated. An example of the results is shown in Fig. 3.4, where the product of laser power and accumulation time was kept constant. As the reference frequency at the same location of silicon wafer should be a constant, the fluctuation in the measurement results should represent the system error. The overall fluctuation increased slightly as the laser power increased, and they were roughly in the range of ±0.03cm^{-1}. Measurement with the laser power of 1mw showd more stable trend for the first several points; what's more, it showed a lower overall fluctuation (±0.015cm^{-1}). Another concern during the measurement is the local heating due to scanning for an extended time. If the wafer is heated by laser, the Raman peak will shift to the negative side, however, no clear

trend was observed for the laser power of 1mw after 500sec exposure. Based on the consideration above, the laser power of 1mw was chosen as the optimized laser power condition to be applied in the experiments.

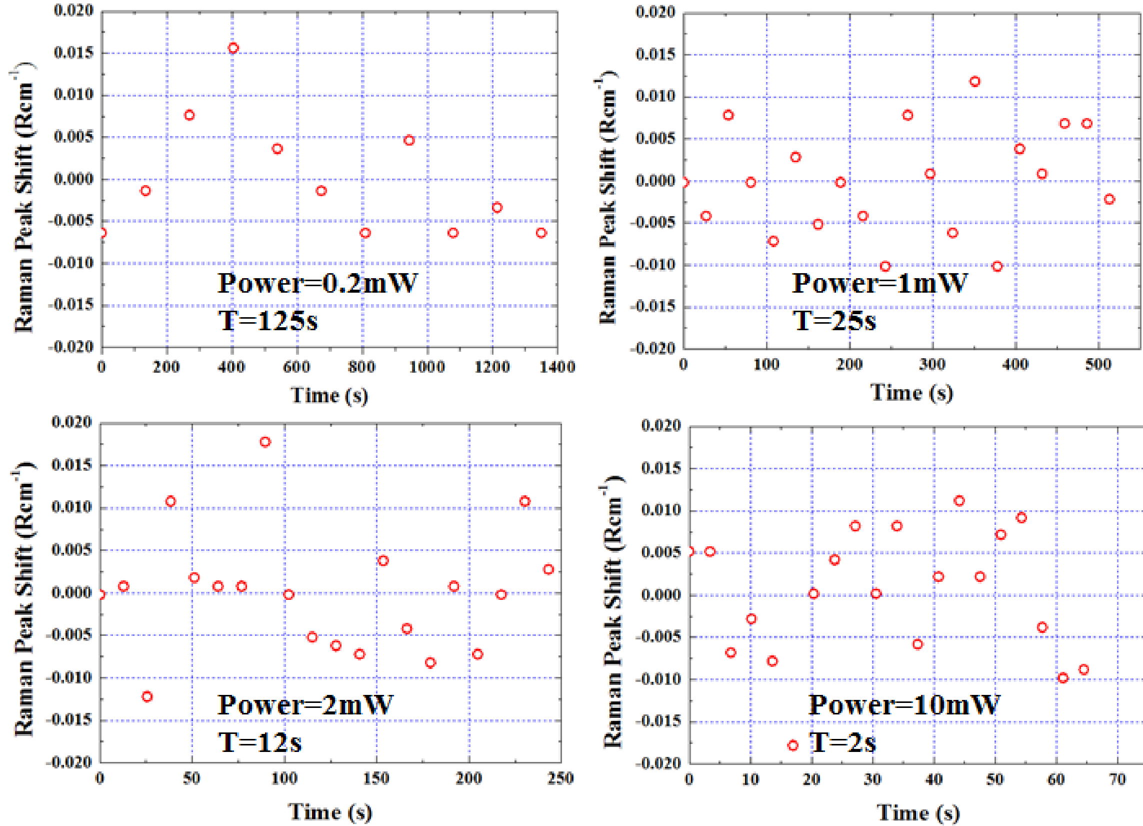


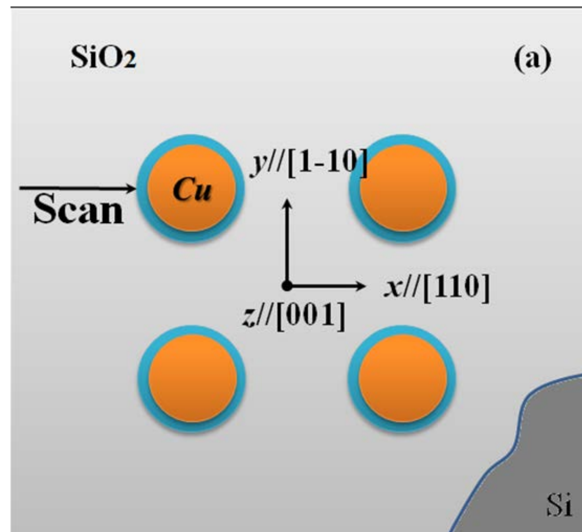
Fig. 3.4 Peak Position fluctuation vs. laser power

3.1.4 Experimental Design and Results

Top-down Raman measurement was applied for a full characterization of the near-surface stress components. Samples used were [001] silicon wafers with blind TSV arrays embedded on top, and the top surface of Si was covered by a layer of 2 µm thick oxide. The diameter of TSV was 5 um, and the depth 55um. Among different TSV arrays, 2 by 2 TSV arrays with a pitch of 10 µm were selected for the measurement. Two sets of samples with the

same structures were annealed at 200C (Sample A) and 300C (Sample B) in vacuum chamber with 100mtorr with forming gas for 2 hours, respectively, to build up different residual stress levels. The scan path was on the top surface along [110] direction as illustrated in Fig. 3.5(a).

Three specific polarization configurations (as shown in Table 3.1) were chosen to perform Raman measurements on the designed TSV structure. The trends of three different Raman peak shifts were observed corresponding to three different modes mentioned in the theory section, as illustrated in Fig. 3.5(b) Sample A and (c) Sample B. Mode 1, 2 and 3 correspond to the polarization conditions listed in Table 3.1. Mode 3 is the Raman peak shift usually measured in the conventional Raman measurement, and the appearance of mode 1 and mode 2 provide additional information that could be used to deduce the magnitude of all three normal stress components. The experimental results for sample A and B presented a similar trend but different magnitude, which implied that stress/strain distribution was same in sign but higher residual thermal stress was built up in Sample B due to the higher annealing temperature. Detailed stress distribution will be presented with the assistance of FEA simulation.



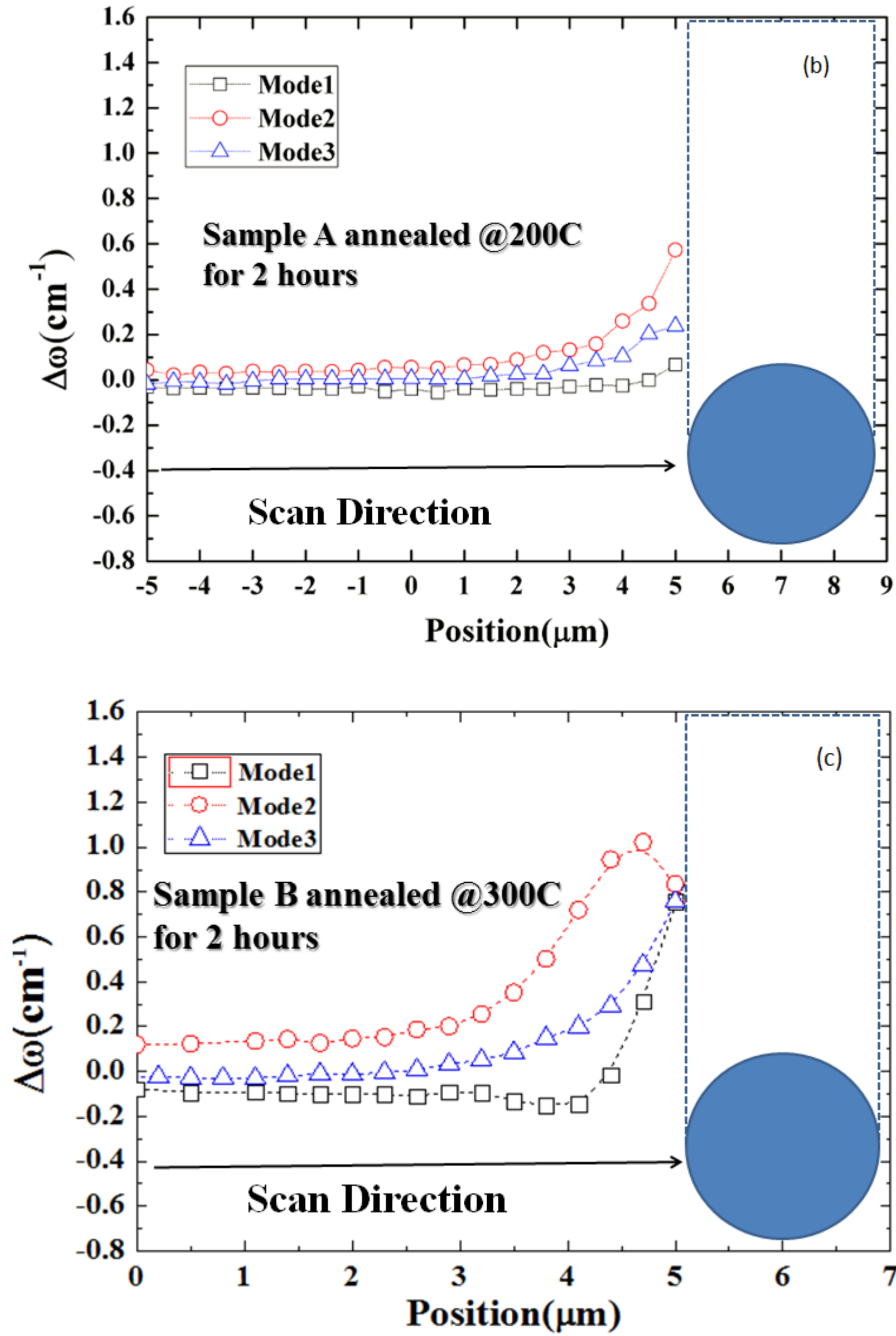


Fig. 3.5 (a) Illustration of scan path along [110] for the 2x2 TSV arrays and Raman peak shifts results along scan path for (b) sample A and (c) sample B

3.1.5 Analysis and Validation

FEA simulation was carried out for better understanding of the near surface stress distribution of the samples. As shown in Figure 3.6(a), only one quarter of the 2 by 2 TSV array structure was chosen with symmetric boundary conditions on the edges. Following the discussion in Chapter 2, the same assumptions and material properties were used. The calculated in-plane shear stress distribution is presented in Fig. 3.6(b).

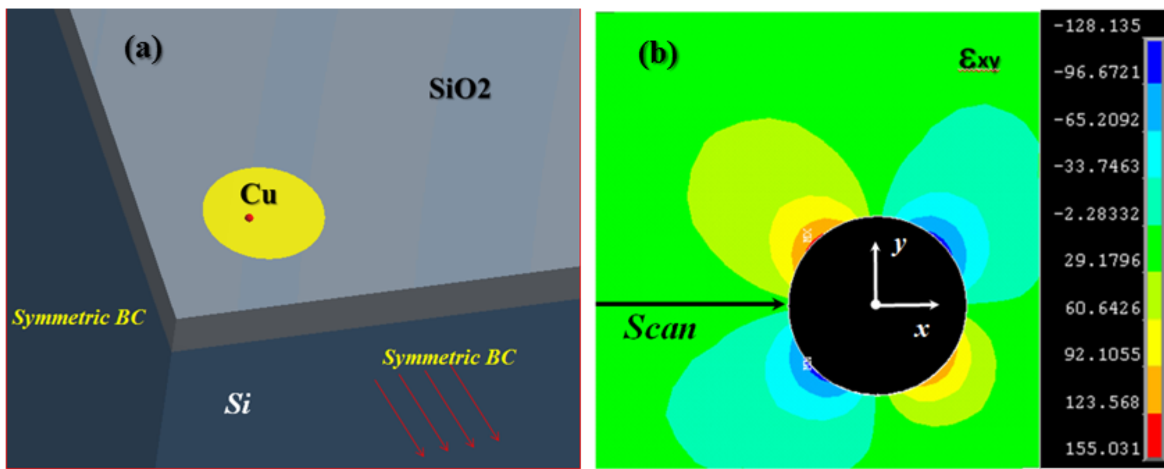


Fig. 3.6 (a) Modeling of a quarter structure and (b) in-plane shear stress distribution in Si around TSV for 2 by 2 TSV arrays

As demonstrated in the FEA simulations along the scan line shown by the arrow in Fig. 3.6(b), the in-plane shear stress was small and can be ignored. Thus equation [3.2] can be applied to the measurements.

For Raman measurements, the Raman signal is in fact an average of Raman Peak shift of different modes weighted by peak intensity. The peak intensity for separate mode under the specific polarization was determined as shown in Table 3.1. Thus the relation among all stress components and measured Raman signal can be written as:

$$\Delta\omega_1 = -2.30\sigma_{xx} - 0.38\sigma_{yy} - 1.93\sigma_{zz}$$
$$\Delta\omega_2 = -0.38\sigma_{xx} - 2.30\sigma_{yy} - 1.93\sigma_{zz}$$
$$\Delta\omega_3 = -1.93\sigma_{xx} - 1.93\sigma_{yy} - 0.75\sigma_{zz} \quad [3.9]$$

Three normal stress components were calculated by simultaneously solving the three equations resulted from three different Raman measurements. The normal stress components determined by experimental data were plotted in Fig. 3.7 as discrete symbols. With the optimized condition, the accuracy of Raman spectroscopy varied from ±0.015cm^{-1} for Mode 3 to ±0.03cm^{-1} for Mode 1 and 2, corresponding to 20~30MPa errors in the measured stresses.

Different stress-free temperatures (Reference temperatures) were chosen in the FEA model to fit the experiment results for sample A and sample B. For sample A, a stress free temperature of 100C (-80C thermal load) was chosen, and for sample B, a reference temperature of 300C (-280C thermal load) was chosen. The comparison between FEA simulation and experiment results are plotted in Fig. 3.7. The results showed a reasonable agreement with each other within the range of measurement error. Comparison between the residual stress build up in sample A and B indicated that the stress relaxation mechanisms were stronger (grain growth, creep, surface diffusion. etc.) at 300C. For sample B, a thorough stress relaxation occurred within 2 hours at 300C, which caused a high residual stress built up when cooled down to room temperature. However, for sample A, the stresses were only partially released during the thermal annealing at 200C, which caused a stress free temperature to be lower than 200C.

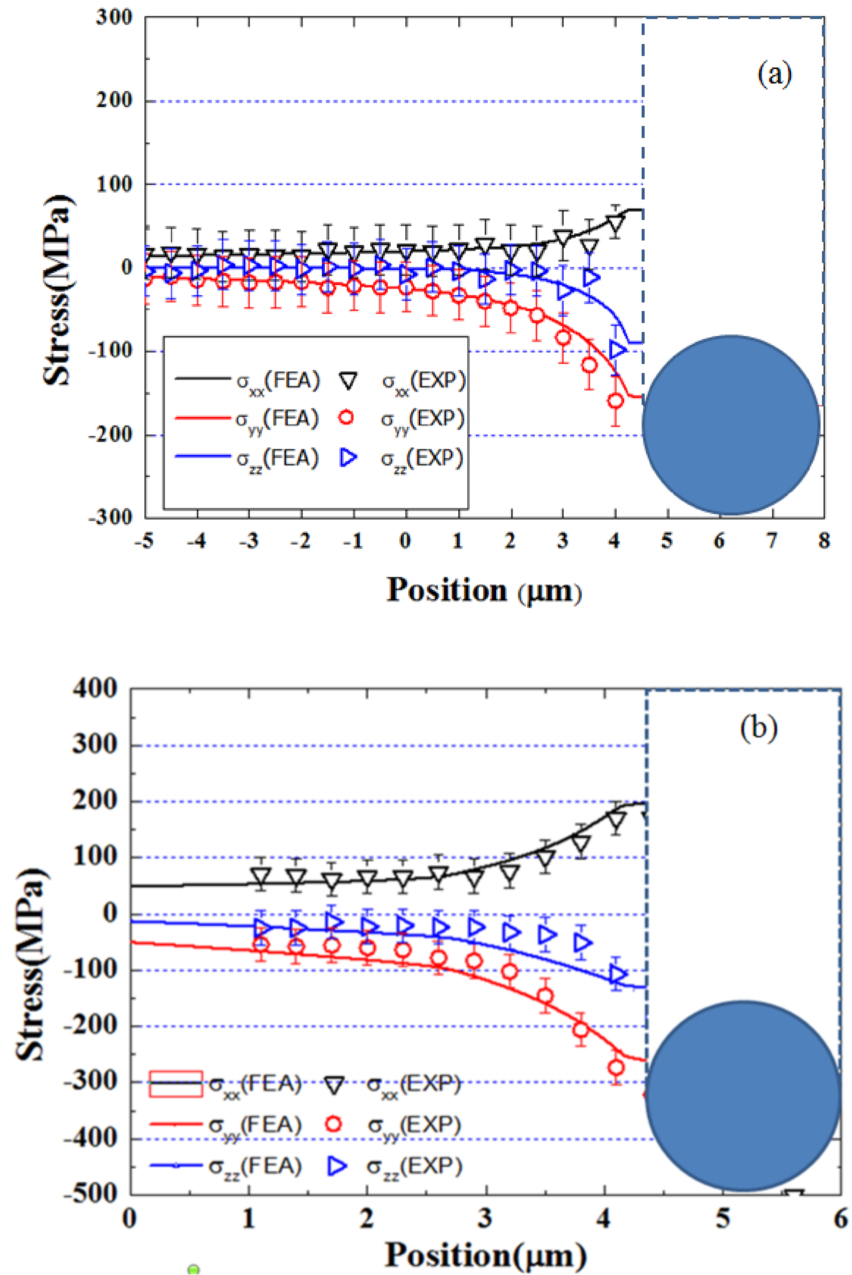


Fig. 3.7 Comparison between experimental determined stress distribution and prediction of FEA simulation (a) Sample A annealed at 200C for 2 hours (Thermal load of -80C is used in FEA model) (b) Sample B annealed at 300C for 2 hours (Thermal load of -280C is used in FEA model)

3.2 Cross-section Raman Measurements

As most of 3D TSV structures are fabricated in the (100) wafer, and the vias arrange along [110] directions, the cross-section Raman measurements are different from the top-down Raman measurements. Usually the cross-section is along [110] directions. More Raman modes are enabled, and according to the polarization configuration, different Raman peak shift can be observed. If the shear stress components are ignored, each Raman peak shifts are related to the linear combination of the normal stress components. And with reasonable assumptions, each in-plane stress component can be solved based on the Raman experimental data within the scope of current study.

3.2.1 Secular equation for cross section Raman measurements

To investigate the possible visible Raman modes, the secular equations are revisited. The cross-section measurement can be considered equivalently to a Raman measurement on (110) wafers. The secular equation will be discussed in the following Cartesian coordinate system: the x-axis is along the [110] direction, y-axis is along [001] and z axe is along [1-10]. By similar transformation as in section 3.1, the secular equation will be in the following form:

$$\begin{vmatrix} p'\epsilon'_{11} + q\epsilon'_{22} + q'\epsilon'_{33} - \lambda & 2r\epsilon'_{12} & (p-q)\epsilon'_{13} \\ 2r\epsilon'_{12} & q(\epsilon'_{11} + \epsilon'_{33}) + p\epsilon'_{22} - \lambda & 2r\epsilon'_{23} \\ (p-q)\epsilon'_{13} & 2r\epsilon'_{23} & q'\epsilon'_{11} + q\epsilon'_{22} + p'\epsilon'_{33} - \lambda \end{vmatrix} = 0$$

where

$$\boldsymbol{p}' = \frac{\boldsymbol{p}+\boldsymbol{q}}{\boldsymbol{2}} + \boldsymbol{r}$$

$$\boldsymbol{q}' = \frac{\boldsymbol{p}+\boldsymbol{q}}{\boldsymbol{2}} - \boldsymbol{r} \qquad \textbf{[3.10]}$$

where p, q, and r are called Raman phonon deformation tensor, which are constants for Silicon. Again, specifically for the scope of the current measurement, the shear components don't contribute too much to the observable Raman peak shift (as will be shown in the later FEA simulation). By ignoring all the shear components in the above secular equation, the solution can be easily obtained as:

$$\boldsymbol{\lambda_1 = p'\epsilon'_{11} + q\epsilon'_{22} + q'\epsilon'_{33}}$$

$$\boldsymbol{\lambda_2 = q\epsilon'_{11} + p'\epsilon'_{22} + q\epsilon'_{33}}$$

$$\boldsymbol{\lambda_3 = q'\epsilon'_{11} + q\epsilon'_{22} + p'\epsilon'_{33}} \qquad \textbf{[3.11]}$$

For each eigenvalue, $\Delta\omega = \omega - \omega_0 = \frac{\lambda}{2\omega_0}$, where ω_0 is the Raman peak position for stress free silicon. Combining the solution with Hook's law, the relation between the Raman shifts and the stress distribution on cross-sectional silicon surface can be determined.

$$\Delta\omega_1 = -2.31\sigma_{xx} - 1.93\sigma_{yy} - 0.38\sigma_{zz}$$

$$\Delta\omega_2 = -1.93\sigma_{xx} - 0.76\sigma_{yy} - 1.93\sigma_{zz}$$

$$\Delta\omega_3 = -0.38\sigma_{xx} - 1.93\sigma_{yy} - 2.31\sigma_{zz} \qquad \textbf{[3.12]}$$

The intensity of different Raman modes can be determined by equation [3.6], The Raman tensor under the new coordinates system is:

$$R_1 = \frac{1}{\sqrt{2}}\begin{bmatrix} 0 & d & 0 \\ d & 0 & -d \\ 0 & -d & 0 \end{bmatrix}, \quad R_2 = \frac{1}{\sqrt{2}}\begin{bmatrix} 0 & d & 0 \\ d & 0 & d \\ 0 & d & 0 \end{bmatrix}, \quad R_3 = \begin{bmatrix} d & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -d \end{bmatrix} \qquad [3.13]$$

Due to the surface roughness introduced by the sample preparation, the scattering light collected from the high numerical aperture effect was not enough to provide additional information in this kind of measurement. Although different Raman modes cannot be separated

out, additional information could still be obtained by altering the polarization configuration during the measurement.

Table 3.2 shows an example of normalized intensity for different Raman modes under the specific polarization conditions. Under polarization configuration in row 1, the Raman peak shift observed was from the contribution of longitudinal mode (LO), but under the polarization configuration in row 2, only a mixture of two TO modes could be observed. According to the calculation, the ratio of those two TO modes was 1:1.

Table 3.2 Intensity for different Raman peaks vs. Polarization (Cross-Section Raman)

e_i	e_s	I_1	I_2	I_3
e_x **Si*(110)***	e_x **Si*(110)***	***0***	***0***	***1***
e_x **Si*(110)***	e_y **Si*(001)***	***0.5***	***0.5***	***0***

Based on the calculated intensities of different modes, the relation between the stress distribution and the observed Raman peak shifts could be expressed as shown in Table 3.3.

Table 3.3 Raman peak shift vs. stress distribution under different polarization

e_i	e_s	$\Delta\omega = \sum_i I_i \omega_i$
e_x **Si*(110)***	e_x **Si*(110)***	$\Delta\omega = -0.38\sigma_{xx} - 1.93\sigma_{yy} - 2.31\sigma_{zz}$
e_x **Si*(110)***	e_y **Si*(001)***	$\Delta\omega = -2.12\sigma_{xx} - 1.35\sigma_{yy} - 1.16\sigma_{zz}$

Usually, the out of plane stress components for the cross-sectional sample were small enough to be ignored (as will be shown in FEA in section 3.2.3). With this assumption, the two in-plane stress components can be determined from the experimental Raman data under different polarization configuration.

3.2.2 Experimental samples and Sample preparation

In order to compare with experimental results from the bending beam method (will be discussed in section 3.3), another set of silicon beams with blind TSV arrays were selected for the cross-section Raman measurements. The geometry of the sample is illustrated in Fig. 3.8. The blind TSVs were embedded in (100) wafers, and aligned along the [110] direction, with diameters of 5.5μm and depth of 55μm. The pitch of TSV array was 40μm. Samples were covered by a thin layer of oxide with a thickness of 0.3μm. Sample 1 and 2 with the same structure were placed in a vacuum chamber with 100mtorr forming gas to avoid oxidation. The sample 1 were heated up slowly with a rate of 2ºC/min to a maximum temperature of 200C and slowly cooled down to the room temperature. Sample 2 experienced 3 thermal cycles: RT→ 200ºC → 350ºC→ RT→ 400C→RT with the same heating ramp rate of 2ºC/min. The purpose of such thermal treatment was to carry out another independent experiment named "bending beam" for validation, the details will be discussed in the next section.

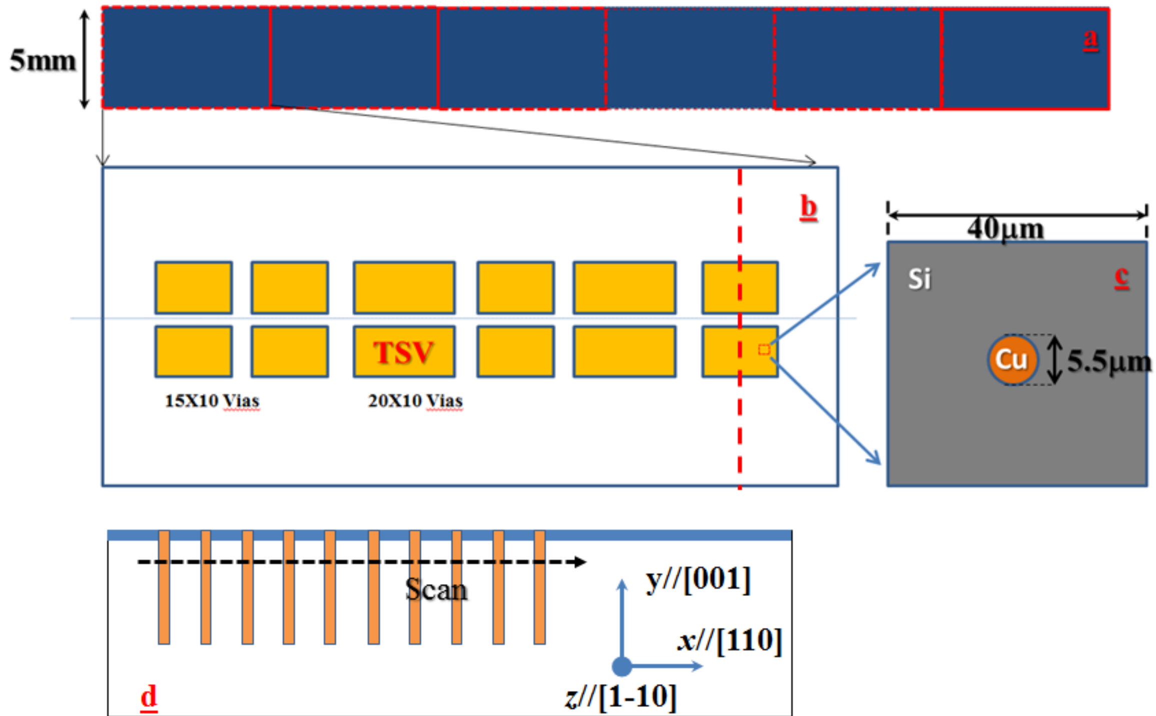


Fig. 3.8 Illustration of the Geometry of Sample 1 and Sample 2

After the annealing process, samples were first carefully diced along the [110] direction at the TSV array edge, and then cut by a FIB to expose the cross-section of TSV arrays. (The cutting path is illustrated in Fig. 3.8 as the red line). The FIB cutting was clean, and the interface of Cu/oxide/Silicon appeared to remain bonded. The perfect bonding condition is used as a simplified boundary condition for FEA simulations and the result seems to give a better account for the local stress distribution.

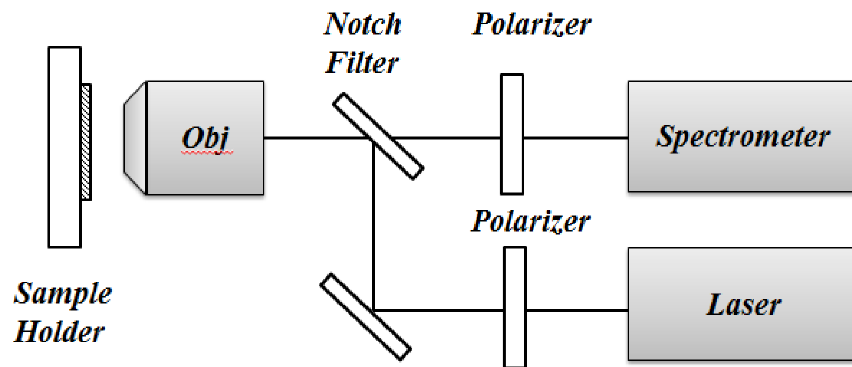


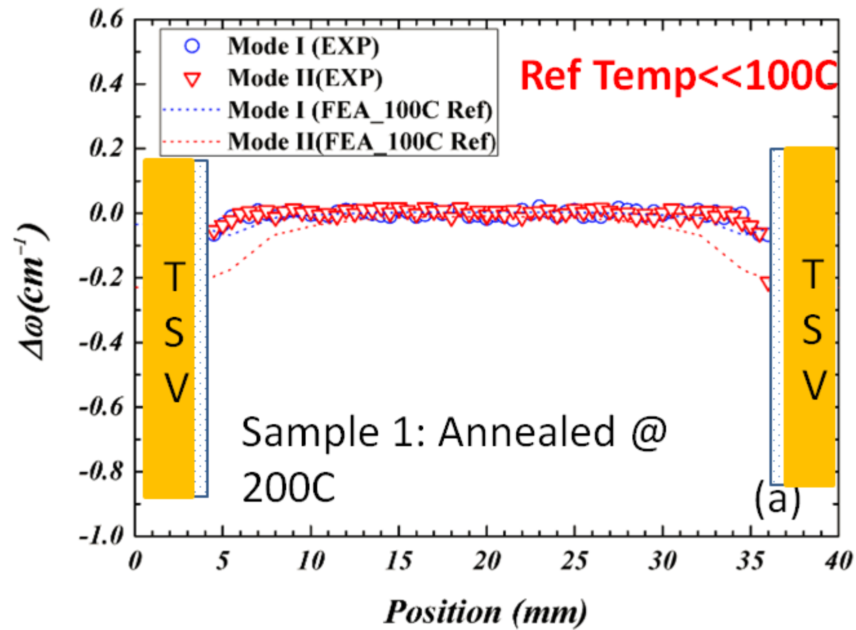
Fig 3.9 Schematic of experimental set-up for Raman spectroscopy

The same Raman spectroscopy used in the previous study was chosen to carry out the cross-section measurement. The polarizer added before the spectrometer (as shown in Fig. 3.9) was used to collect the scattering light with polarization either parallel or perpendicular to that of the incident laser. In this way, different polarization configurations could be applied as listed in Table 3.3, and Raman peak shift from different Raman modes (or mixture) could be detected.

3.2.3 Experimental results, FEA simulations, and analysis

At room temperature, the cross-section measurement was carried out on the cross-section at 5μm under the top TSV surface as illustrated in Fig. 3.8(d). The results of Raman peak shift are shown in Fig. 3.10. For the Cross-sectional Raman scans on both samples, the Raman peak shift was shifted towards negative side when approaching the interface between Silicon/barrier layer and Cu. According to the equations in Table 3.3, this implies that the summation of normal stress components is tensile. Furthermore, for sample 2, the Raman peak shift measured under polarization condition 1 (row 1 in Table 3.3) was always higher than that under polarization condition 2 (row 2 in Table 3.3). This implies that the normal stress components along the x

direction (σ_{xx}) should be tensile, as the Raman peak shift under polarization condition 2 is more sensitive to this stress components based on its having a larger coefficient. For sample 1, the overall Raman peak shifts are small, less than 0.1 cm^{-1}. This result indicates that the residual stresses in sample 1 build-up from the thermal annealing are very small. Meanwhile, no significant difference between the Raman shifts measured under polarization1 and polarization 2 is observed. As the out of plane stresses (σ_{zz}) are expected to be small based on the traction free boundary condition for the cross-section of TSV arrays, the normal stress components along the x direction (σ_{xx}) should be very small.



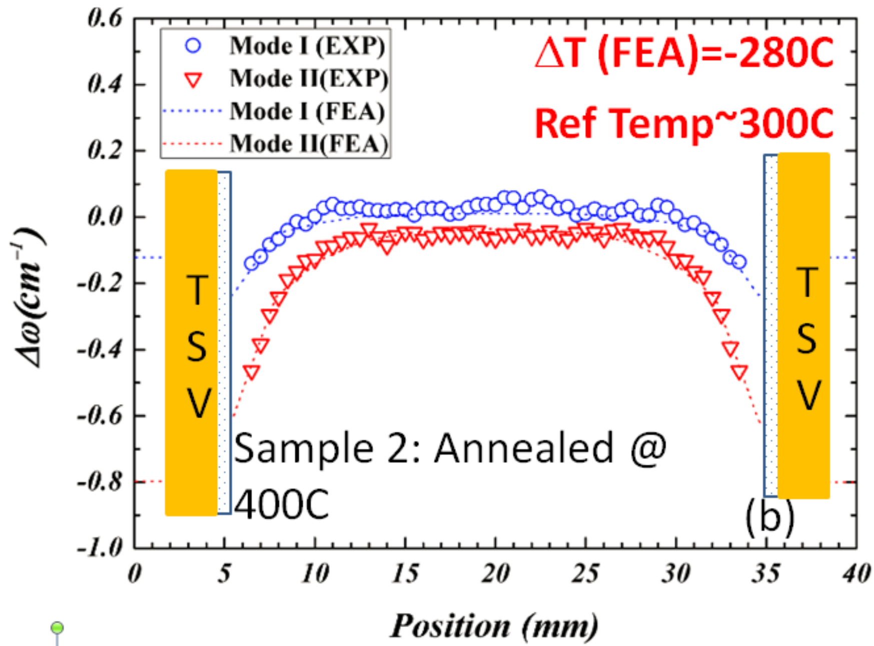


Fig. 3.10 Raman peak shift along the scan path for (a) Sample 1 (Annealed at 200C) (b) Sample2 (annealed at 400C). The experimental data are plotted by blue circle (Raman Peak shift under polarization 1) and red triangle (Raman peak shift under polarization 2), and the FEA simulated Raman peak shift are plotted as dotted line. RT=20C

Before proceeding to make further assumptions to analyze the experimental data, a deeper understanding of stress distribution profile on the cross-section surface is necessary. An FEA model was developed for this purpose. Following the assumptions and material properties used in Chapter 2, models according to the geometry of different samples were built for stress prediction. A visual illustration of the model is shown in Fig. 3.11, and traction free boundary condition is imposed on the cross-section surface to simulate the experimental condition.

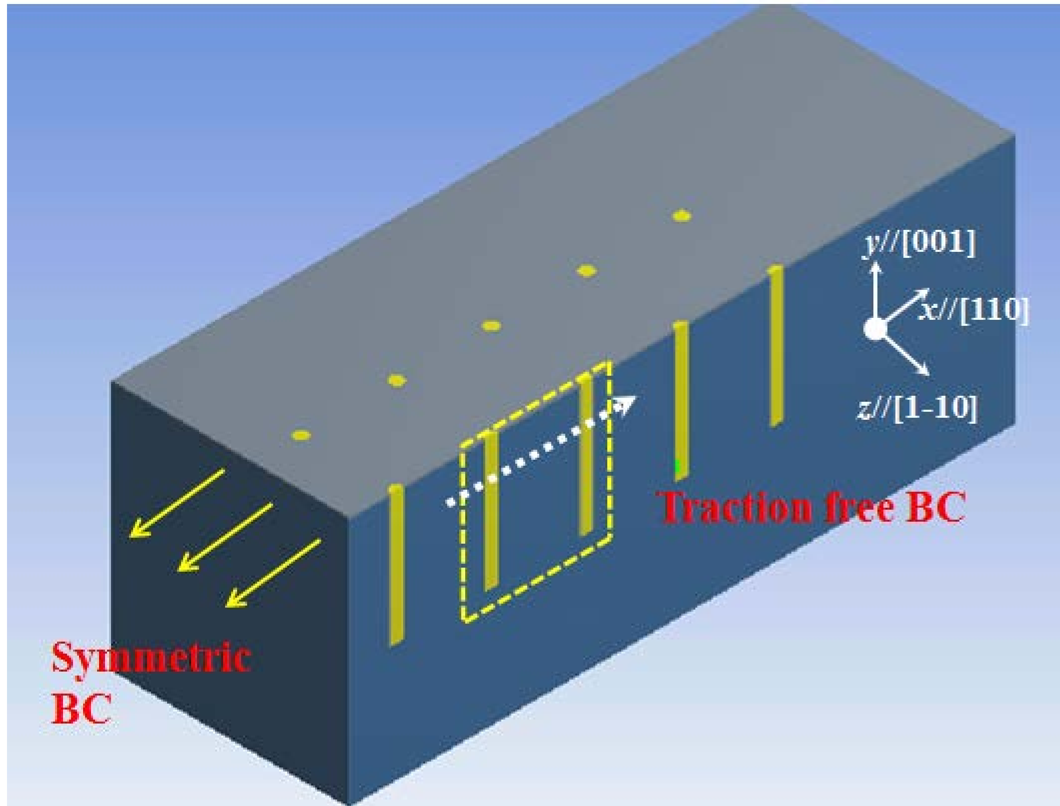


Fig. 3.11 Visual illustration of the 3D FEA model

The stress distribution in the region of interest (area in the rectangular area in Fig. 3.11) can be calculated by FEA simulation. Three normal stress components along the dotted line were converted into the Raman peak shift based on the equations in Table 3.3. Different reference temperatures (stress free temperature) were selected in the FEA model to fit the experimental results, and the comparison was plotted in Fig. 3.10. For sample 1, a reference temperature of 100C was selected. The comparison in Fig. 3.10(a) shows that the experimental results are lower than the FEA simulation, which indicates that the stress free temperature of sample 1 after annealing is even lower than 100C, and perhaps closer to room temperature. For sample 2, a reference temperature of 300C was selected to fit the experimental results. Experimental results and FEA simulation are in good agreement as illustrated in Fig. 3.10(b), which indicates the

stress free temperature of sample 2 after 400C annealing is around 300C. There results will be further validated in next section (section 3.3) by bending beam experiment.

The distribution of three normal stress components of sample 2 from FEA simulation is shown in Fig. 3.12. The magnitude of the out of plane stress (σ_{zz}) is non-zero only at the edge of interface between Cu and Silicon/barrier layer. Based on this observation, it is reasonable to ignore the out-of-plane stress term (σ_{zz}) in Table 3.3. Thus, the in-plane stress components can be obtained by solving equations in table 3.3 using experimental data. The in-plane stress components of sample 2 determined by the experimental data were compared with FEA simulation and plotted in Fig. 3.13. Good agreement was achieved. The stress components along the [110] (x) direction was dominant and always tensile. The magnitude of this stress component increased when approaching the interface of TSV, and a maximum value of around 200MPa was observed based on the experiment.

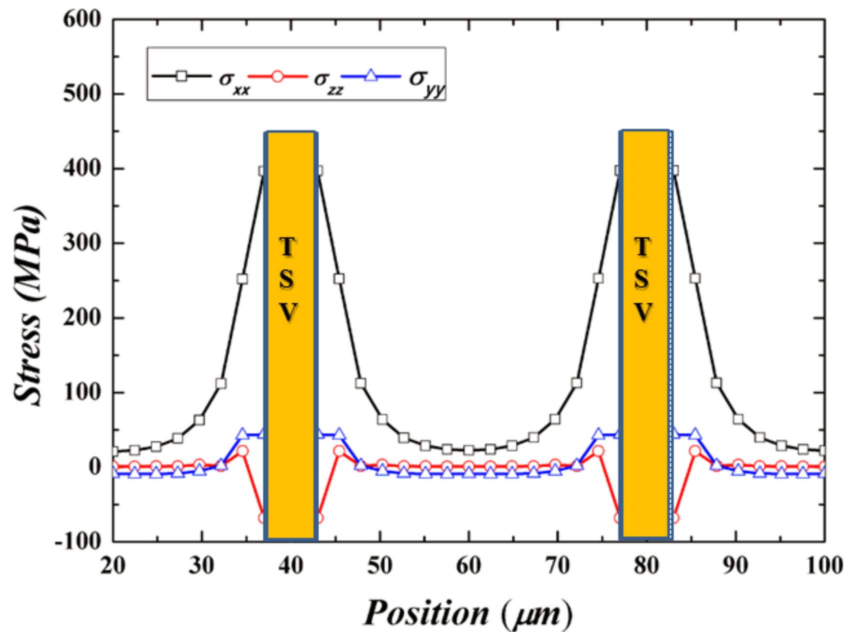


Fig. 3.12 Normal stress distribution for Sample 2 on cross-section at 5μm under TSV top surface

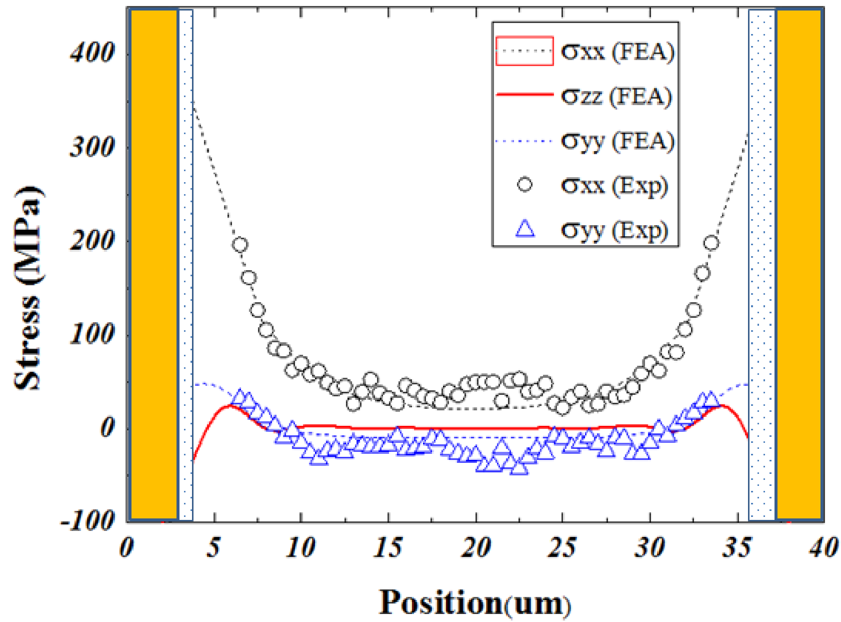


Fig. 3.13 Comparison of the in-plane stresses distribution between Raman measurements and finite element analysis (FEA)

3.3 Bending Beam Experiments

The bending beam technique is similar to the wafer curvature methods for characterizing stresses in thin films [35]. The average stress in a thin film can be determined based on the wafer curvature measurement by using Stoney's formula. This method has been successfully extended to characterize the average stress of blind TSV arrays during thermal cycling, and determine the average residue stress state after certain thermal history. [36] [31] In this section, as a complementary experimental method, same samples in section 3.2 were used for bending beam measurement. The Residual stress of samples under the same thermal history was determined by bending beam experiment independently. The results from cross-section Raman measurement and bending beam measurement were compared at the end of this section.

Fig. 3.14 shows a schematic setup of the system used by bending beam measurement. In the bending beam system, samples are usually in the shape of a narrow beam (5mmX50mm), and placed in a vacuum chamber with 100mtorr forming gas to avoid oxidation. Hot plate inside the chamber is used to control the thermal condition of the samples. Two parallel He-Ne laser beams are directed to top surface of the sample beams through the glass window on top of the vacuum chamber, and then reflected onto two photo detectors. During the thermal cycling, the position of the reflected laser spots will change due to the curvature change of sample surface, and the positions will be traced by the photo detector with a LabVIEW system. The curvature change during the thermal cycling can be determined by the following equation:

$$k - k_0 = \frac{1}{R} - \frac{1}{R_0} = \frac{S_0 - S}{2LM} \qquad [3.14]$$

Where R is the radius of curvature, L is the distance between two laser spots on the specimen (L=2.75cm), and M is the distance between the specimen and the photo sensors (M=2.248m). The subscript "0" stands for the baseline values at the reference (initial) state. The detailed spatial relationships for the curvature calculation are illustrated in Fig. 3.15[39]

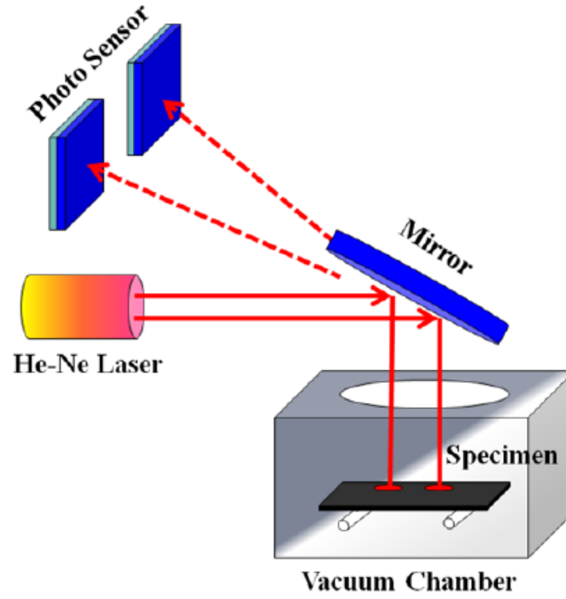


Fig. 3.14 Illustration of the bending beam system. [Taken from [37]]

Sample 1 and 2 depicted in section 3.2.2 were actually annealed in the bending beam system. The curvature during the annealing as well as the reference temperature was obtained, as illustrated in Fig. 3.16. Details of the experiment procedure were similar to Ref [37]

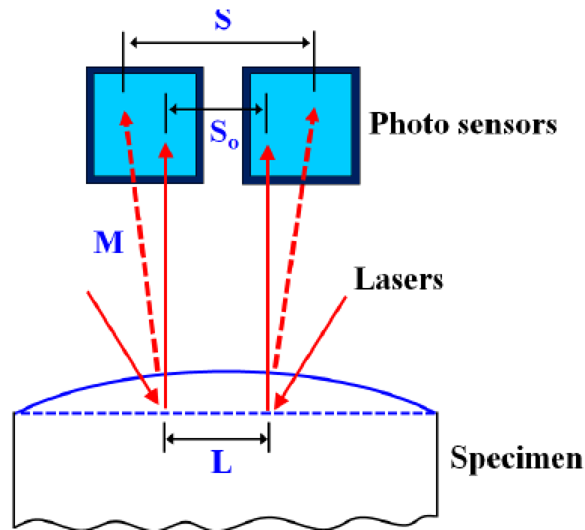


Fig. 3.15 Spatial relationships for the curvature calculation of specimen

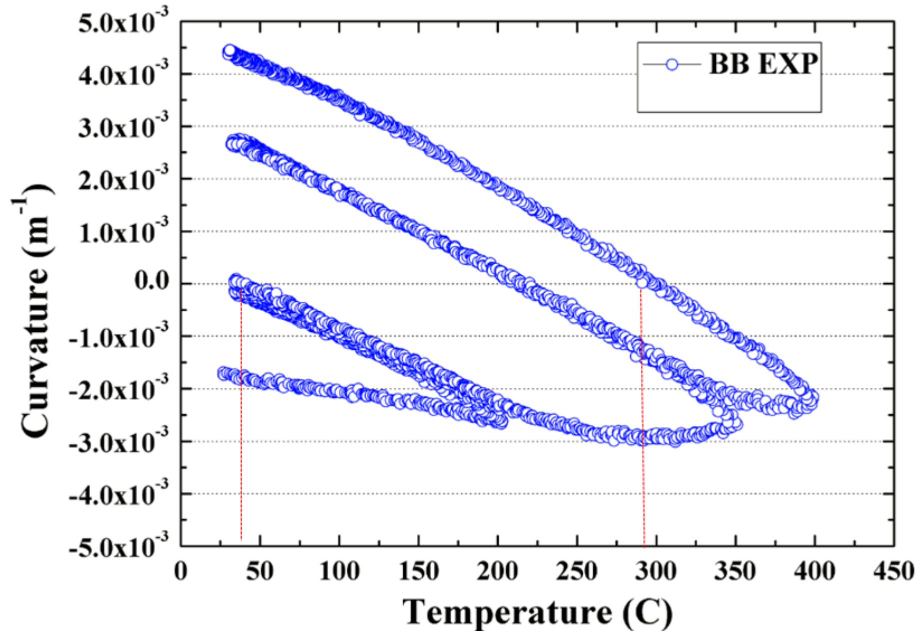


Fig. 3.16 Bending beam measurement for sample 1 and sample 2 in section 3.2

The zero curvature reference used in Fig. 3.16 was obtained by BB measurement on the same sample with Cu etched off as a reference. The zero curvature indicates the stress free state of the sample under a specific thermal history. For sample 1, which was annealed at a maximum temperature of 200C, the beam curvature was close to 0 when cooled down to room temperature. This implies the sample is close to stress free at room temperature. For sample 2, during the cooling procedure from a maximum annealing temperature of 400C, the curvature of the sample reached zero at around 300C. Therefore, the stress free temperature of sample 2 was determined to be around 300C. The experimental conclusion agrees well with the prediction from cross-section Raman measurement as well as the FEA simulation in section 3.2.

3.4 Correlation between Raman Measurement using High NA Effect and Cross-section Raman Measurement

The stress distributions obtained by these two kinds of Raman measurement cannot be compared directly because of the different measurement locations. Furthermore, during the sample preparation for cross-section Raman measurement, the TSV structures were polished and then cut using FIB to expose the cross-section, so the geometry and boundary conditions for the samples were different. However, samples under the same thermal history should share the same stress-free temperature, which can be considered as an effective characterization of thermal residual stress. Thus, the Raman measurement with High NA effect and cross-section Raman measurement were carried out on the same sample, and their stress free temperatures were compared with the assistance of FEA simulation.

Sample B in section 3.1 was selected for the cross-section Raman measurements for the comparison. Instead of 2 by 2 TSV arrays, 5 by 5 TSV arrays at different location on Sample B were chosen for the convenience of sample preparation. The basic structure of TSV remained the same, but the pitch of the TSV array was 20μm instead of 10μm. Following the same procedure described in section 3.2, cross-section Raman measurements were carried out on the cross-section of TSV arrays at 5μm under the top surface as illustrated in Fig. 3.17(a). The FEA model used in Section 3.2.3 was modified to describe the 20μm pitch of sample B. A thermal load of -280C (stress free temperature =300C) was chosen for the simulation, which is the same thermal load used for FEA model of sample B during the Raman measurement with High NA effect. The stresses from the FEA model were converted to Raman peak shift based on equations in Table 3.3. The comparison between experimental results and simulation were plotted in Fig. 3.17(b). The FEA and experimental results were found to be in good agreement, which implied that the

stress-free temperature of sample B remains the same for both Raman measurements, and the two Raman measurement results are consistent with each other.

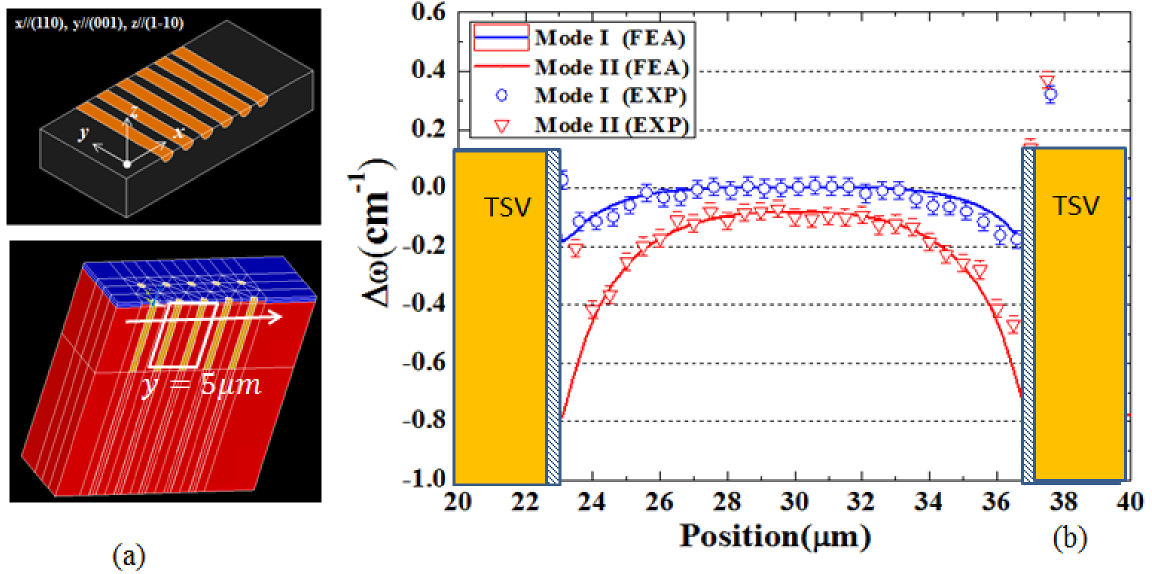


Fig. 3.17 (a) Illustration of cross-section of region of measurement of sample B, x axis is along [110], y axis is along [001], and z axis is along [1-10] (b) Comparison of cross-section Raman measurement on sample B and FEA simulation results, a thermal load of -280C was used for FEA model

3.5 Summary

The Raman spectroscopy shows its advantage in measuring local stress distribution in silicon. In this chapter, two different kinds of Raman measurement have been developed to study the thermal mechanical behaviors of TSV structures at different location. Besides utilizing different laser polarization profiles, the top view Raman measurements also used so-called "high NA effect" to obtain additional information. Based on this approach, the local distribution of near-surface stress in Si has been measured, and all 3 normal stress components were determined. From the cross-section Raman measurements, the stress distributions far away from the top surface have been characterized. However, only the in-plane stress distribution on the

TSV cross-section could be determined by experimental data with reasonable assumption based on FEA simulation.

The results for cross-section Raman measurements was first validated independently by bending beam measurement, and then correlated to top-down Raman measurement with the assistance of FEA simulation. The comparison showed good consistency among the results from different experimental methods.

Together, these experimental methods provide a complementary approach for characterizing the thermo-mechanical behaviors of TSV structure. The residual stress built up in TSV by different thermal history are compared and discussed.

Chapter 4 Thermo-mechanical reliability of Stack-die memory package

4.1 Introduction

Three dimensional (3D) die stacking incorporating through-silicon via (TSV) has the potential to overcome the wiring limit of interconnect structures [38] [39]. However, the difference in thermal expansion between Cu and Si in TSV structures can introduce significant thermal stresses in the 3D integration structure. Meanwhile, during packaging processes, thermal stresses arise from the mismatch in the CTEs between dies and substrate. There stresses are harmful. They can directly couple into the Cu/low-k interconnects to drive interfacial delamination, and also cause the TSV pop-up and reduce the carrier mobility to degrade device performance. [40] Characterization of the thermal deformation as well as the stress/strain distributions of the stack-die structure is therefore important for understanding the thermal mechanical reliability issues.

In this chapter, finite element method combined with high resolution moiré interferometry and cross-section Raman measurement is used to study the Chip-package interaction and its impact on the reliability of stack-die memory package with TSV structures.

4.2 Test Structures

The test structure used in current study is a 5-stacked memory die as shown in the Fig. 4.1. For each die, Cu TSV was fabricated by deep etching of Si followed by barrier and seed layer deposition and via filling by electroplating. Diameter of the TSV (through silicon via) was 8μm and the vias were spaced 50μm apart along $[1\bar{1}0]$ direction. Series of temporary bonding and wafer thinning were conducted to reveal the TSVs and reduce the final thickness of each layer to

50μm. The layers were connected with Sn-based micro bumps with underfill in between. After die stacking, the structure was encased in epoxy molding compound (EMC) and mounted on an 11mmx9.9mm PCB board. The specimen was cut at the die edge first and polished inward to expose the cross-section of interest. Fig. 4.2 illustrates the cross section views of the stack-die memory package.

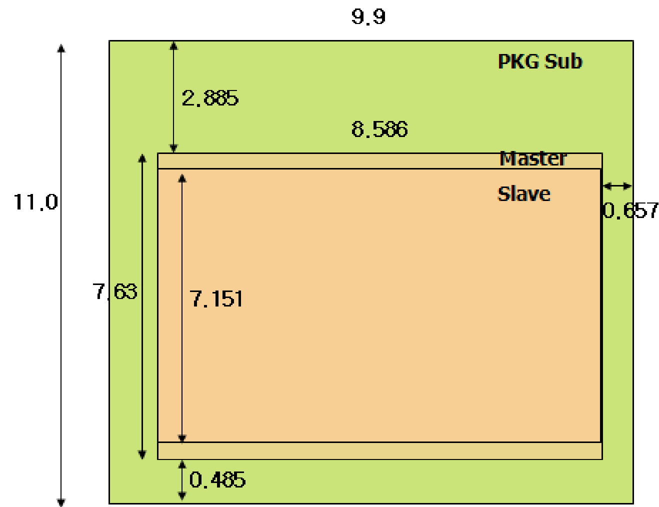


Fig. 4.1 Illustration diagram for stack-die memory structure (from top), units: mm

Fig. 4.2 Cross-section of stack-die memory structures

4.3 Finite element method for stack-die memory structure

4.3.1 Effective moduli method for wafer level simulation

FEA modeling is used to simulate the warpage of the stack-die memory package. Wafer level modeling is known to be difficult due to a huge number of TSVs and complicated TSV structures. In order to overcome such challenge, the wafer level warpage modeling methodology for TSV wafer has been developed. The effective mechanical properties of one TSV structure have been calculated by considering the same deformation response for both the actual TSV structure and effective model. The 3D wafer level effective model is verified numerically and experimentally.

The TSV array can be considered as composite material with copper fiber imbedded in the silicon binding material. The approach of effective moduli can be applied under the situation when the average stress state instead of detail local stress distribution is more important. The results from the present research can provide guidelines on the mechanical design for Si interposers to minimize the occurrence of out-of-plane warpage from assembling processes of 3D-IC packaging.

The Simple Rule of Mixture for composite material gives first order approximation for longitudinal property, but inaccurate estimation for the transverse property

$$\bar{E}_1 = E_{f1}V_f + E_mV_m$$

$$\bar{v}_{21} = v_{f2}V_f + v_mV_m$$

$$\frac{1}{\overline{\overline{E_2}}} = \left(\frac{1}{E_{f2}}\right)V_f + \left(\frac{1}{E_m}\right)V_m$$

$$\frac{1}{\bar{G}_{12}} = \left(\frac{1}{G_{f12}}\right) V_f + \left(\frac{1}{G_m}\right) V_m \qquad [4.1]$$

$$\bar{\alpha}_1 = \frac{\alpha_{f1} E_{f1} V_f + \alpha_m E_m V_m}{E_{f1} V_f + E_m V_m}$$

$$\bar{\alpha}_2 = \alpha_{f2} V_f + \alpha_m V_m + \left(\frac{E_{f1} v_m - E_m v_{f21}}{\bar{E}_1}\right)(\alpha_m - \alpha_{f1}) V_f V_m \qquad [4.2]$$

where E represents Young's modulus, V the volume ratio, and α the thermal expansion coefficient. The subscript "f" represents fiber, "m" the bounding material, "1" the longitudinal direction (along the fiber direction), and "2" the transverse direction.

To obtain a better estimation than the simple rule of mixture for the transverse material property, Schapery [41] offered another choice for transverse CTE calculation:

$$\bar{\alpha}_2 = \alpha_m V_m (1 + v_m) + \alpha_{f1} V_f \left(1 + v_{f21}\right) - \bar{\alpha}_1 \bar{v}_{21} \qquad [4.3]$$

For $\bar{E}_2$ and $\bar{G}_{12}$, Halpin and Tsai modified rule of mixture (MROM) has been widely used

$$\frac{\bar{E}_2}{E_m} = \frac{1 + \zeta \eta V_f}{1 - \eta V_f},\ \eta = \frac{\gamma - 1}{\gamma + \zeta_y},\ \gamma = \frac{E_{f2}}{E_m}$$

$$\frac{\bar{G}_{12}}{G_m} = \frac{1 + \zeta \eta V_f}{1 - \eta V_f}, \eta = \frac{\gamma - 1}{\gamma + \zeta_s},\ \gamma = \frac{G_{f12}}{G_m}$$

[4.4]

, where ζ is the fitting parameter. At present, no rules of mixture exist to predict the transverse - transverse properties.

Although the analytical approaches are effective in some simple situation, there are limitations which cannot be overcome by the analytical solutions. 1. Different assumptions are

involved to simplify the derivation, and some of them are not practical. For example, in most of the derivation, the binding material property was considered to be isotropic. 2. Analytical solutions either fail to give accurate transverse property, or have some unknown fitting parameter, which is relied on numerical method or experiment. 3. No analytical solution is available for transverse-transverse property prediction (e.g. G_{23}, ν_{23}). In the present study, instead of using analytical solution with fitting parameter, FEM (finite element method) micromechanical analysis is applied to TSV arrays, which are considered as unidirectional laminates, subject to multi-axial loading conditions. Following the approach in ref [42], a unified periodical boundary condition was applied to prediction of nine elastic constants of a unidirectional TSV RVE (Representative Volume Element), as show in Fig. 4.3

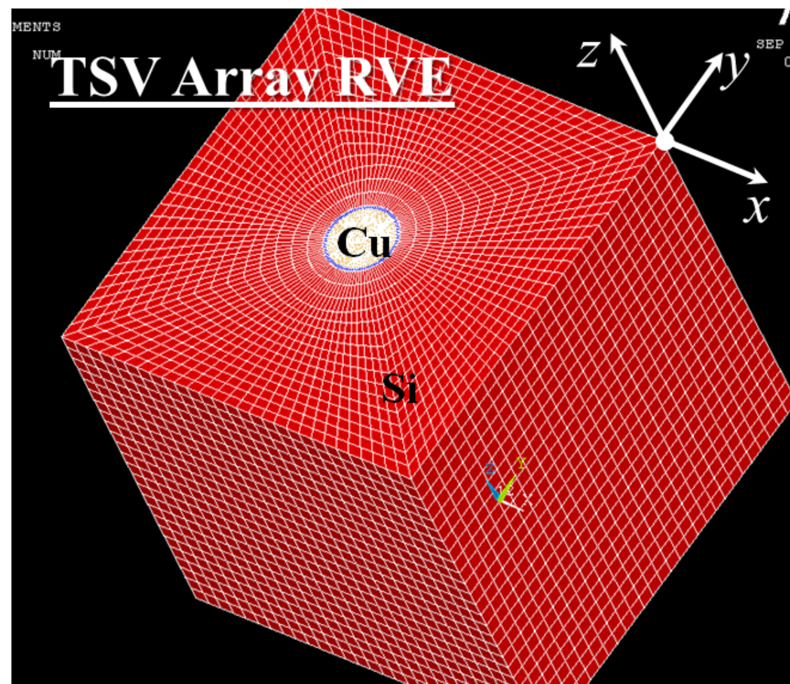


Fig. 4.3 A representative volume element for a TSV array with x axis along [110], y axis along $[1\bar{1}0]$, z axis along [001]

For any parallelepiped RVE models, the following unified periodic boundary conditions were obtained.

$$u_i^{j+}(x,y,z) - u_i^{j-}(x,y,z) = c_i^j (i,j = 1,2,3) \qquad [4.5]$$

, where u represents the displacement on the TVE surface, index " j^+" and "j^-" denotes positive and negative X_j direction, respectively. The constants, c_1^1, c_2^2 and c_3^3, represent the average stretch or contraction of the RVE model due to the action of the three normal traction components. The constants $c_1^2 = c_2^1$, $c_1^3 = c_3^1$ and $c_2^3 = c_3^2$, correspond to the shear deformations due to the three shear traction components. The average strain and stress components can be simply obtained by

$$\bar{\varepsilon}_{ij} = \frac{1}{2}\frac{c_i^j \Delta x_i + c_j^i \Delta x_j}{\Delta x_i \Delta x_j}$$

$$\bar{\sigma}_{ij} = \frac{\Delta x_j}{V}\iint_{Si} \sigma ij \, dS = \frac{Pij}{Sj}, \textit{ no summation over } j \qquad [4.6]$$

In a matrix notation, the constitutive relation of this effective material can be written as:

$$[\bar{\varepsilon}] = [S][\bar{\sigma}]$$

, where S_{ij} is the compliance matrix:

$$[S] = \begin{bmatrix} S_{11} & S_{12} & S_{13} & 0 & 0 & 0 \\ S_{12} & S_{22} & S_{23} & 0 & 0 & 0 \\ S_{13} & S_{23} & S_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & S_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & S_{55} & 0 \\ 0 & 0 & 0 & 0 & 0 & S_{66} \end{bmatrix}$$

And the relation between the engineering elastic constants and S_{ij} is:

$$
\begin{aligned}
E_1 &= \frac{1}{S_{11}} \quad \nu_{12} = -\frac{S_{12}}{S_{11}} \quad G_{12} = \frac{1}{2S_{44}} \\
E_2 &= \frac{1}{S_{22}} \quad \nu_{13} = -\frac{S_{13}}{S_{11}} \quad G_{13} = \frac{1}{2S_{55}} \\
E_3 &= \frac{1}{S_{33}} \quad \nu_{23} = -\frac{S_{23}}{S_{22}} \quad G_{23} = \frac{1}{2S_{66}}
\end{aligned} \qquad [4.7]
$$

In order to validate the accuracy of the model, the effective moduli method was applied to the bending beam sample structure mentioned in chapter 3.3. For the bending beam experiment, in the linear region, the global bending of sample doesn't depend on detailed stress distribution around TSV but the average effect. Two thermal procedures were considered according to the bending beam experimental results. 1. Sample cooled down from 400C to room temperature. The bending beam (BB) experiment showed that the stress-free temperature of the sample was 300C. 2. Sample cooled down from 350C, and the BB results in this case showed the stress-free temperature of 217C (based on Fig. 3.16).

The detailed 3D TSV model consisting of Cu TSV and surrounding Si material in an area of one pitch of TSV (shown in Fig. 4.3) was simulated under mechanical and thermal-mechanical loadings, respectively. A pitch of 40um was selected for the RVE based on the sample geometry. Table 4.1 presents the material property of Si, Cu and silicon dioxide in the detailed TSV model. The anisotropic material property of Si was considered as well.

Table 4.1 Material property used for FEA simulation

Material	CTE(ppm)	Modulus(GPa)	Poisson Ratio
Cu	16.7	110	0.35
SiO_2	1.4	75	0.2
Si	2.6	N/A	N/A

Silicon is consider as anisotropic material, the stiffness matrix (unit $10^{11}\ Pa$) used in the FEA model (x//100,y//010, z//001):

$$\mathbf{C} = \begin{bmatrix} 1.66 & 0.64 & 0.64 & 0 & 0 & 0 \\ 0.64 & 1.66 & 0.64 & 0 & 0 & 0 \\ 0.64 & 0.64 & 1.66 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0.80 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0.80 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0.80 \end{bmatrix}$$

The effective material properties for the BB sample were calculated based on equation 4.6 and 4.7, and they are listed below:

Compliance matrix:

$$[S] = \begin{pmatrix} 5.97 & 0.40 & -2.15 & & & \\ -0.40 & 6.044 & -2.15 & & & \\ -2.15 & -2.15 & 7.72 & & & \\ & & & 12.73 & & \\ & & & & 12.73 & \\ & & & & & 19.74 \end{pmatrix}$$

CTE:

$$\alpha_x = 2.82 \times 10^{-6}$$
$$\alpha_y = 2.82 \times 10^{-6} \quad v.s \quad \alpha_{s_i} = 2.3 \times 10^{-6}$$
$$\alpha_z = 2.80 \times 10^{-6}$$

Due to the symmetry of the sample, one quarter model with symmetric boundary condition were used. The blind TSV arrays were replaced by the equivalent material with calculated effective material property as shown in Fig. 4.4(a). As an example, the out of plane (z direction)

displacement of top sample surface after cooling down from 400C with a stress-free temperature of 300C is illustrated in Fig. 4.4(b).

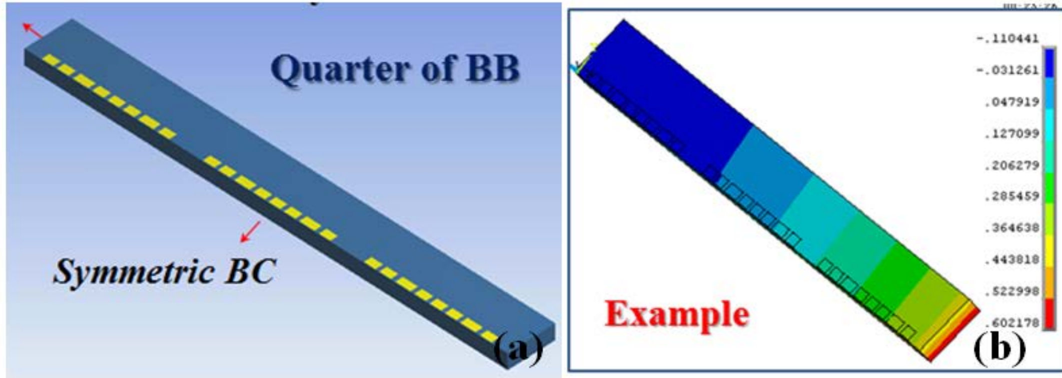


Fig. 4.4 (a) FEM model for one quarter of the BB sample, the TSV arrays are replaced by equivalent composite material with effective moduli. (b) Out of plane displacement of top surface under a thermal load of -300C

FEA results were verified by the experimental results from the bending beam measurement in section 3.3. Fig. 4.5 shows the curvature of sample top surface at different temperature during cooling schedule 1 and 2. The FEA and BB results are found to be in good agreement.

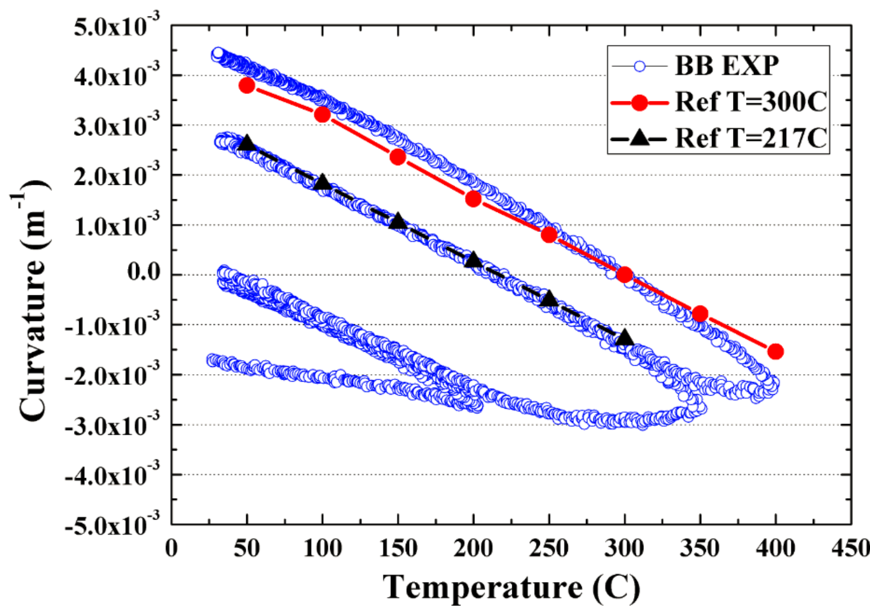


Fig. 4.5 Comparison of beam curvature obtained from BB experiment (hollow circle) and FEM simulation with effective moduli method (solid circle and solid triangle).

4.3.2 Modeling of stack-die memory structure

A 3D FEA model was developed based on a 2-level sub-modeling technique to investigate the impact of thermal-mechanical reliability issues in the stack-die memory package, with a particular focus on the effect of change in chip-induced stresses around TSV structures. Multilevel Sub-Modeling Technique was adopted for this purpose.

Level 1: Package level. Level 1 was used to investigate the thermal deformation of the whole flip-chip package. At this level, a half section of the package was modeled using the symmetry condition as illustrated in Fig. 4.6(a) and 4.6(b). The effective moduli method was applied at this level to simplify the simulation. The TSV arrays as well as solder/underfill array were replaced by equivalent composite material.

Level 2: TSV & solder level: a sub-model focusing on the TSV region of interest with much finer mesh as shown in Fig. 4.6(c) was built. From the simulation results for the package level modeling, the detailed strain/stress distribution was revealed. The built-in cut boundary technique in ANSYS [43] was used for sub-modeling. The simulation results were used to verify the experimental results from X-section Raman spectroscopy in section 4.4. All the material properties used in the FEA model is listed in Table 4.2.

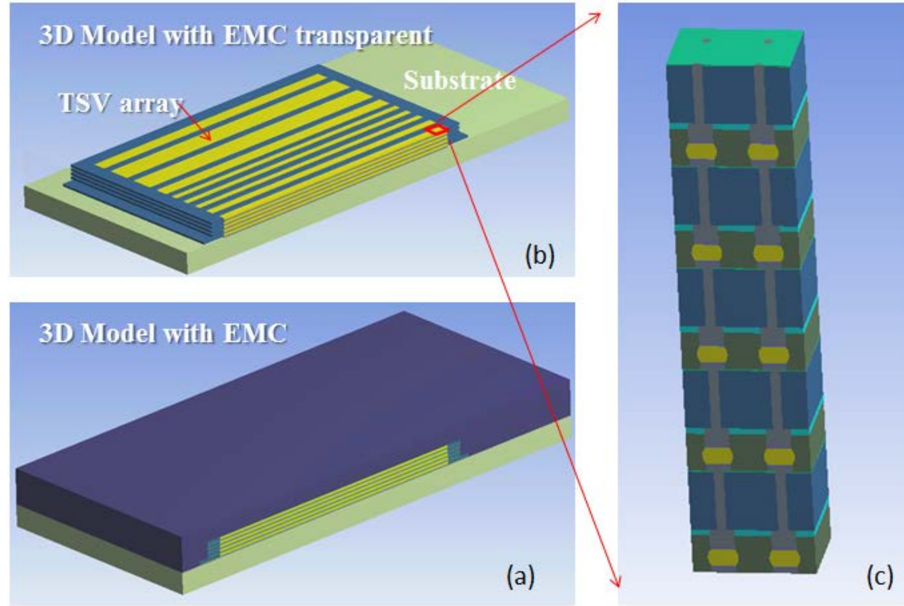


Fig. 4.6 (a) A half section FEM Model of stack die structure with symmetric boundary condition. (b) Same FEM model with EMC made transparent to show detailed structure under EMC. (c) TSV and solder level sub-model

Table 4.2 Material property used in FEM for stack-die memory structure

Material	CTE(ppm)	Modulus(GPa)	Poisson Ratio
Cu	16.7	110	0.35
SiO2	1.4	75	0.2
Solder	21.5	88.5	0.4
Si	2.6	Anisotropic	Anisotropic
SiN	3.3	310	0.27

Tg material property

Material	CTE(ppm)	Modulus(GPa)	Tg
EMC	8/34	23.6	140
Underfill	31/65	5.8	87
PCB	15/3	26.5	185

4.4 Package Level Deformation

The FEA results for the package level modeling can be verified using the experimental data from surface profiler. A thermal load of -200C was applied in the FEA simulation according to the process condition of the stack-die structure. Fig. 4.7 shows the z-displacement (package warpage) distribution along the die center line. The FEA and experimental results are found to be in good agreement.

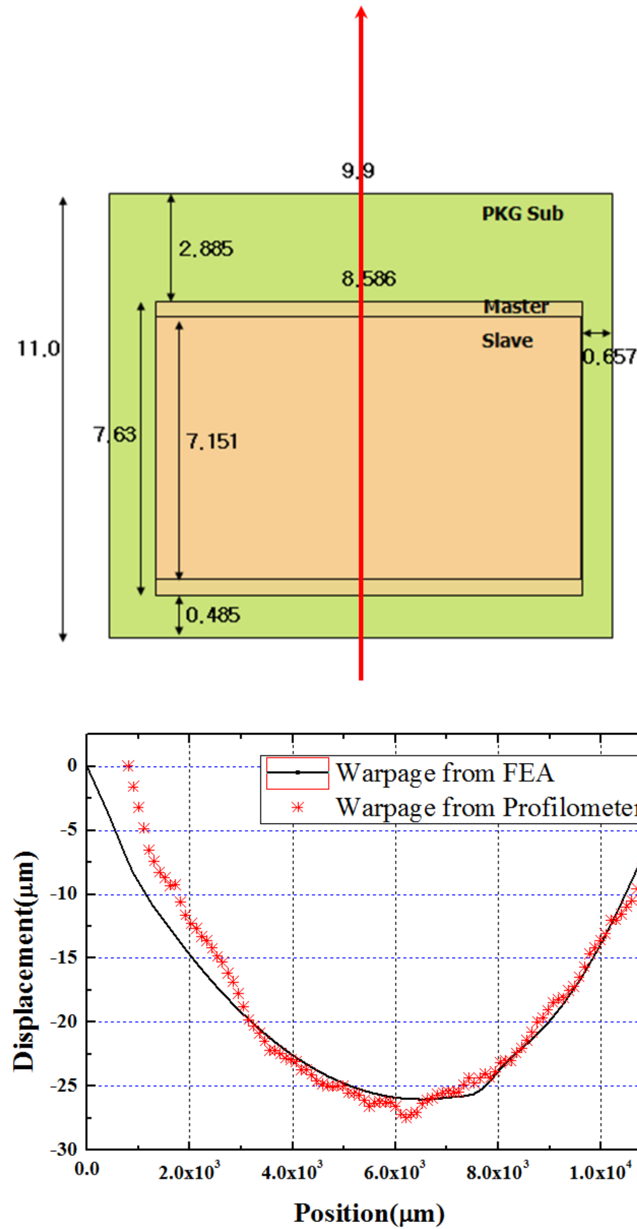


Fig. 4.7 Comparison of FEA and profilometer results of thermal deformation for the stack-die memory package

4.5 Impact of CPI on Stress/strain Distribution around TSV

Based on the discussion in Chapter 2 and 3, with the assistance of FEM simulation, the stress/strain distribution around blind TSV were well illustrated by Micro-Raman spectroscopy measurement. However, during packaging processes, thermal stresses arise from the mismatch in CTEs between the chip and substrate, and can be directly coupled into the Cu/low-k interconnect as well as through silicon via structures. As the stress distribution is important for device performance and surface delamination, the cross-section Micro-Raman measurement is applied to investigate the change of stress distribution around TSV in the stack-die memory structure due to the Chip-package interaction.

For sample preparation, EMC (epoxy molding compound) on top of the package were polished down to expose the top die. Edge of the stack-die memory package was polished to expose the stacked-die structure. The TSV structures located close to the center of the cross-section, and were exposed by careful FIB process, as illustrated in Fig. 4.8.

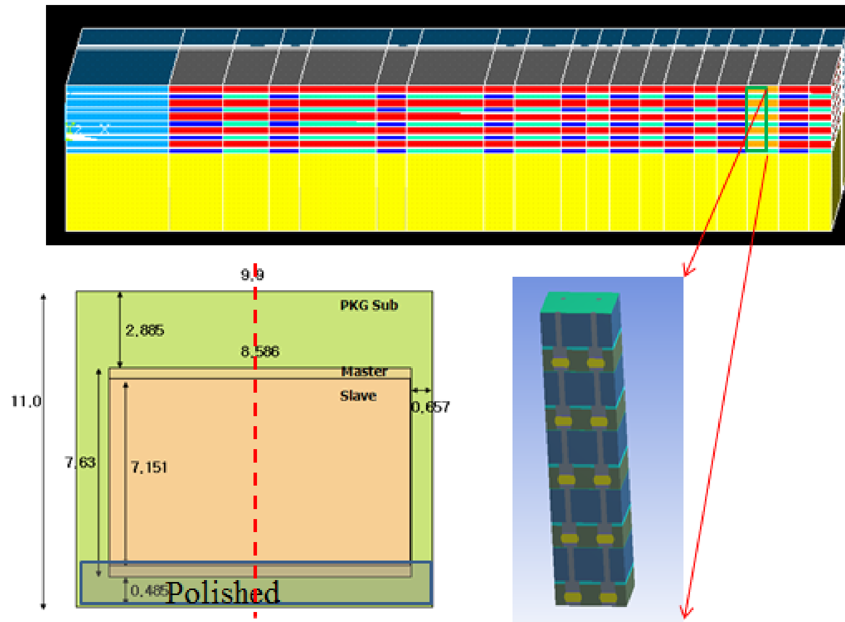


Fig. 4.8 Illustration of sample preparation and locations of Cross-section Raman measurements in a die stack structure.

The measurement was carried out at 25μm under surface of the top die, as illustrated in Fig. 4.9(a). FEM model in section 4.2 was modified to accommodate the sample geometry, and the Raman peak shifts were calculated based on the strain distributions obtained from the FEM model. A thermal load of -200C was assumed in the model. The Raman peak shift results from FEM calculation and experiment are compared in Fig. 4.9(b). The corresponding stress distributions in the scan area from the FEM model were also illustration in Fig. 4.9(c).

Different from the common trends of Raman peak shift for blind TSVs shown in chapter 3, the trend for the TSV in the top die shows a different trend for one band. This is caused by the change in the sign of the stresses in y direction (along the vertical TSV direction).

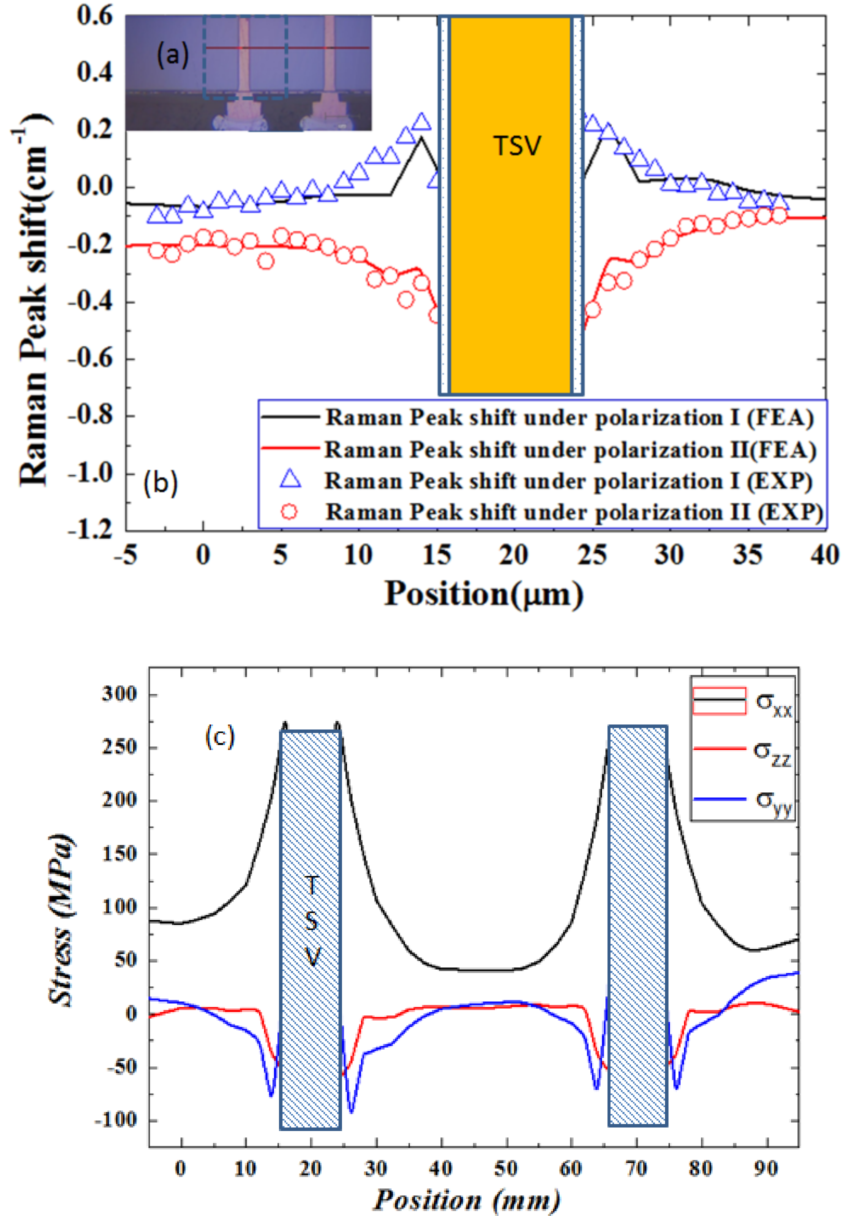


Fig. 4.9 (a) Inset illustrating scan location of cross-section Raman measurement (b) Comparison of peak shift results from FEM and experimental measurement, -200C thermal load is used for FEM model. (c) Stress distribution at the measurement location calculated from FEA with sub-modeling technique.

4.6 Characterization of Thermal-Mechanical Behavior of Stack-die Memory Package with High Resolution Moiré Interferometry

Cross-section Raman measurement has its advantage to characterize local stress distribution with high space resolution. However, it can only measure the stress distribution in a

small area and only in silicon matrix. The large CTE mismatch between the die and substrate can cause the package to bend and generate significant thermal stresses in solder joints under thermal loads. Such stresses are harmful not only to the reliability of solder bumps but also to the stability of Cu/low-k interconnect especially at the proximity of solder UBM, raising mechanical reliability concerns in flip-chip packages. A complimentary method is necessary to investigate into these reliability issues. In this section, high resolution moiré interferometry is used to measure the deformation of flip-chip packages under pre-set thermal loading.

4.6.1 Regular moiré interferometry

Moiré interferometry is a whole-field optical interference technique with high resolution and high sensitivity for measuring the in-plane displacement and strain distributions [44]. The optical system of the interferometer is schematically shown in Fig. 4.10 [45]. The incoming laser beam from the optical fiber is reflected by mirror 1 and 2 and then impinges onto the surface of the reference grating, which splits the laser beam into four beams (2U and 2V beams). The four laser beams are reflected onto the surface of sample grating. A moiré image is formed by the interaction of the virtual grating created by the reference grating with the deformed specimen grating and recorded by the digital camera [45]. The displacement field and strain distribution can be deduced from the moiré images.

$$u = \frac{N_x}{f_s}, v = \frac{N_y}{f_s}$$

$$\varepsilon_x = \frac{\partial u}{\partial x} = \frac{1}{2f_s}\frac{\partial N_x}{\partial x} \approx \frac{1}{2f_s}\frac{\Delta N_x}{\Delta x}$$

$$\varepsilon_y = \frac{\partial u}{\partial y} = \frac{1}{2f_s}\frac{\partial N_y}{\partial y} \approx \frac{1}{2f_s}\frac{\Delta N_y}{\Delta y}$$

$$\varepsilon_{xy} = \frac{1}{2}\left(\frac{\partial u}{\partial x} + \frac{\partial v}{\partial y}\right) \approx \frac{1}{4f_s}\left(\frac{\Delta N_y}{\Delta x} + \frac{\Delta N_x}{\Delta y}\right)$$

[4.8]

where u is the displacement along the x direction, v is the displacement along the y direction. N_x, N_y are the fringe order of the u, v field moiré fringe pattern, respectively and f_s is the frequency of the specimen grating.

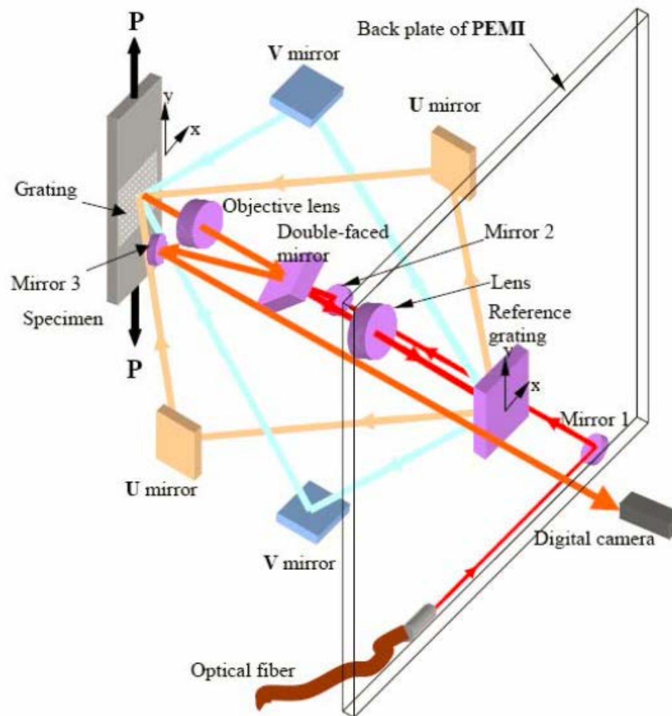


Fig. 4.10: Optical system of moiré interferometer (Taken from [45])

This method has been successfully used to measure the thermal-mechanical deformation in electronic packages to investigate package reliability [46] [47] [48]. A sensitivity of 417nm per fringe contour can be reached with a specimen grating of 1200 lines/mm.

4.6.2 Sample preparation and measurement

After treating the polished surface with acetone, a low-viscosity, brittle adhesive was used to attach 1200 lines/mm gratings on the polished surface of the specimen at a temperature of 82 C. The deformation at this temperature was taken as that of a reference state. The moiré test was performed at the room temperature, 22 ºC, providing a thermal loading of -60ºC. The thermal load that can be used for moiré studies is limited by the glass transition temperature (Tg) of the underfill. An optical microscope picture of the cross-section is shown in Fig. 4.11. Only the region close to die edge that usually has the largest thermal strain in the package was analyzed in the moiré test.

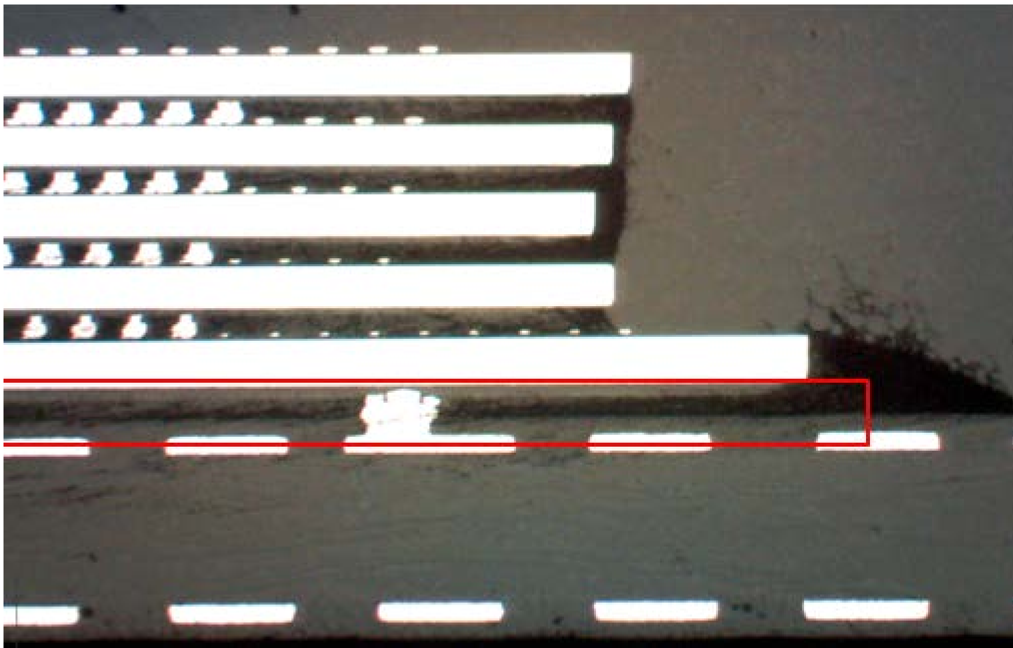


Fig. 4.11 Optical image of sample cross-section

The equipment used in the moiré test is a modified IBM portable Engineering moiré Interferometer (PEMI) system as shown in Fig. 4.12 [45]. The high resolution moiré interferometry is a very sensitive measurement technique and a careful system alignment is

required before each measurement in order to obtain quality images with high accuracy. A standard 1200 lines/mm gratings was first placed on the sample holder to align the optical system as a reference grating. After the system was carefully aligned, the prepared sample was evaluated by following the steps outlined in reference [45]. The moiré fringe patterns were then recorded and analyzed.

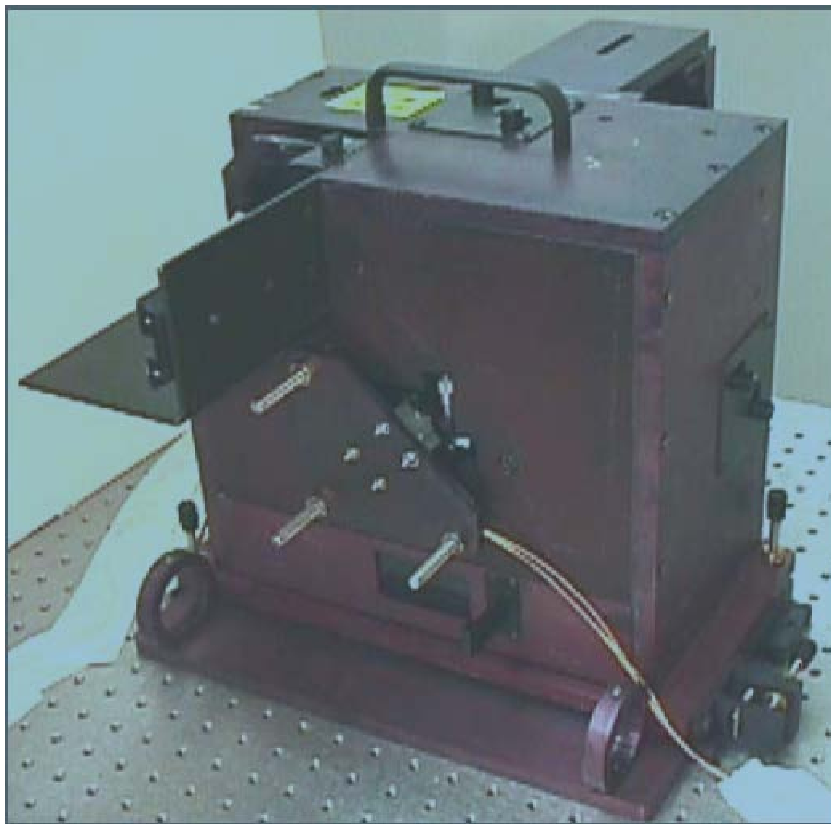


Fig. 4.12 Modified PEMI for moiré test (taken from [45])

4.6.3 Results and discussion

The fringe patterns obtained under a thermal load of -60C are shown in Fig. 4.13. The U and V fields in the diagram denote the deformation pattern along the vertical and horizontal directions, respectively. Each fringe represents a displacement of 417nm in this case. Package bending can be deduced from the V field pattern by counting the number of fringes in the image.

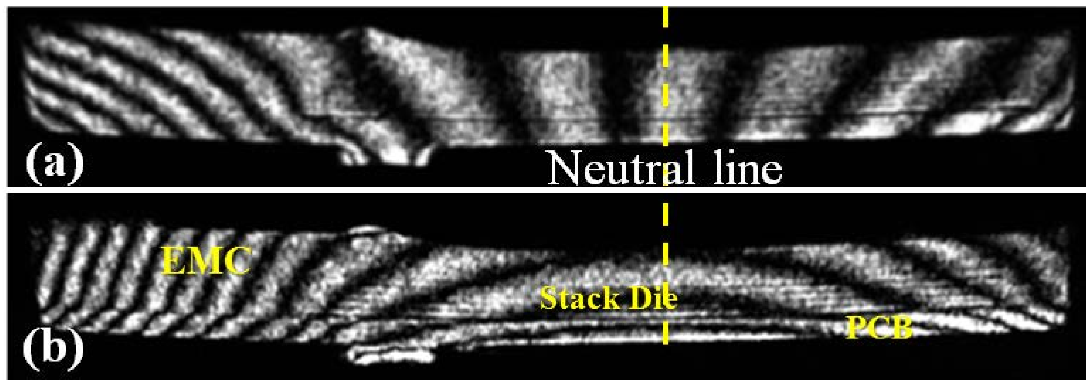


Fig. 4.13 Fringe pattern for stack-die memory package for a thermal load of -60C (a) U field (b) V field

4.6.4 High resolution moiré interferometry

The precision of the regular moiré tests is limited by the ability to interpolate the moiré fringes, which is rather restricted since the fringe pattern appears as a series of broad dark lines. Therefore, a high resolution moiré test based on phase shifting technique was employed to investigate the deformation near the solder layer which will be discussed later in this chapter.

The sensitivity of 'regular' Moiré interferometry should be adequate for assessing the overall thermal deformation, but is not sufficient for measuring thermal deformation in high-density electronic packages, particularly for small features. Therefore a high resolution moiré measurement is required with improved resolution at local areas such as the die corner. In a regular moiré pattern, the spacing between fringes corresponds to a phase angle difference of 2π,

which corresponds to 417nm in displacement. With the application of the phase-shifting technique, in which four continuous images are taken with a phase difference of $\pi/2$ and then combined as in Eq. 4.3 and Eq. 4.4 to exact the phase angle between fringes, the change of the phase angle can be captured.

$$I_1(x,y) = I_0(x,y) + I'(x,y)\cos[\emptyset(x,y)]$$
$$I_2(x,y) = I_0(x,y) - I'(x,y)\sin[\emptyset(x,y)]$$
$$I_3(x,y) = I_0(x,y) - I'(x,y)\cos[\emptyset(x,y)]$$
$$I_2(x,y) = I_0(x,y) + I'(x,y)\sin[\emptyset(x,y)] \qquad [4.9]$$

where $I_0(x,y)$ and $I'(x,y)$ are the background and periodically varying intensities in the interference pattern and $\emptyset(x,y)$ is the phase angle of the interference pattern at each pixel location (x, y). The phase angle is then determined as

$$\emptyset(x,y) = \arctan[\frac{I_4(x,y) - I_2(x,y)}{I_1(x,y) - I_3(x,y)}] \qquad [4.10]$$

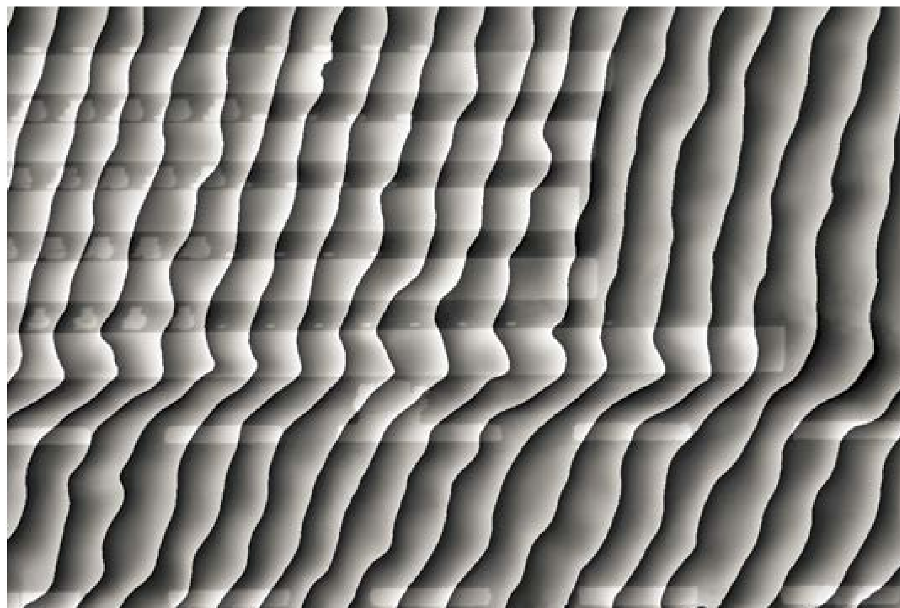
Once the phase angle distribution between two interference fringes is obtained, the displacement distribution can be determined by measuring the change of the phase angle.

$$u(x,y) = \frac{1}{2f_s}\frac{\emptyset_u(x,y)}{2\pi}$$
$$v(x,y) = \frac{1}{2f_s}\frac{\emptyset_v(x,y)}{2\pi} \qquad [4.11]$$

Furthermore, due to the small size and low thermal load, carrier fringes were introduced by shifting the neutral line away from the die center to enhance the visibility of the slowly varying fringe gradient. In this case, each fringe no longer represents a displacement of 417nm, but the strain from the differential of the displacement remains the same. [49]

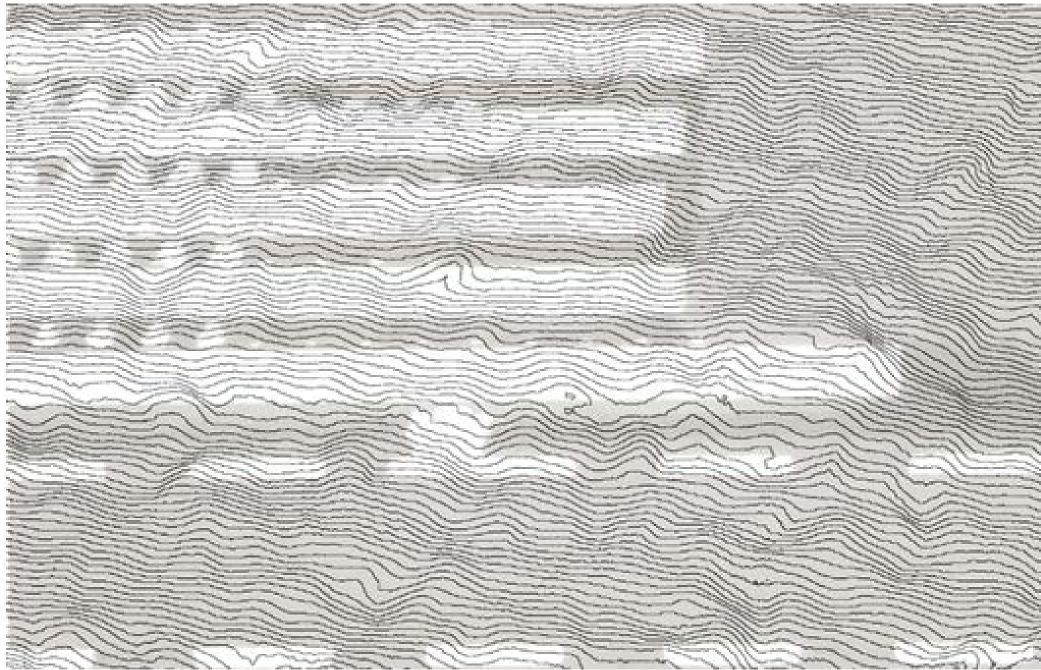
A high resolution phase shifted moiré analysis was carried out at the die corner. The phase maps obtained are illustrated in Fig. 4.14. To indicate the location of the deformation, optical images of the cross-section were superimposed onto the phase map. The phase map can be subdivided further by a factor of 8 based on the grayscale of the phase map to obtain more detailed deformation information as illustrated in Fig. 4.15.

U field

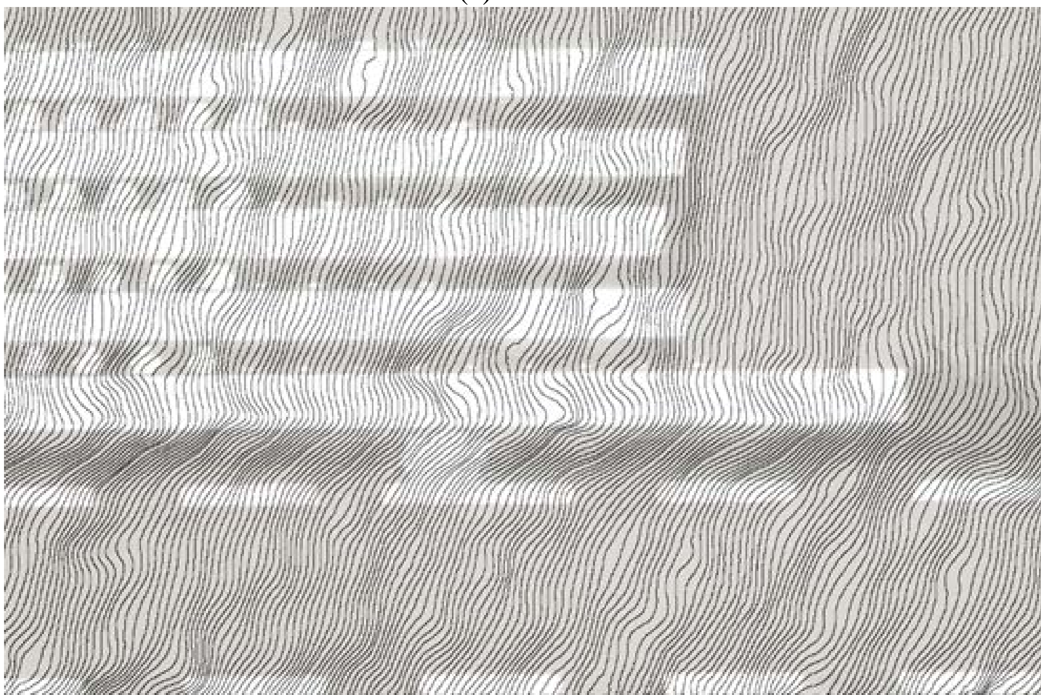


V field

Fig. 4.14 Phase maps for stack-die memory package



(a) U field



(b) V field

Fig. 4.15 Phase maps of stack-die memory package with 8X resolution

These phase maps were evaluated by the moiré analysis software to determine the strain distributions. Strain analyses were carried out along three lines: the bottom die/solder interface

(Line1), the centerline of solder bumps (Line 2) and the solder/substrate interface (Line 3). Shear strains and normal strain along the line direction are plotted along lines 1, 2 and 3 as illustrated in Fig. 4.16.

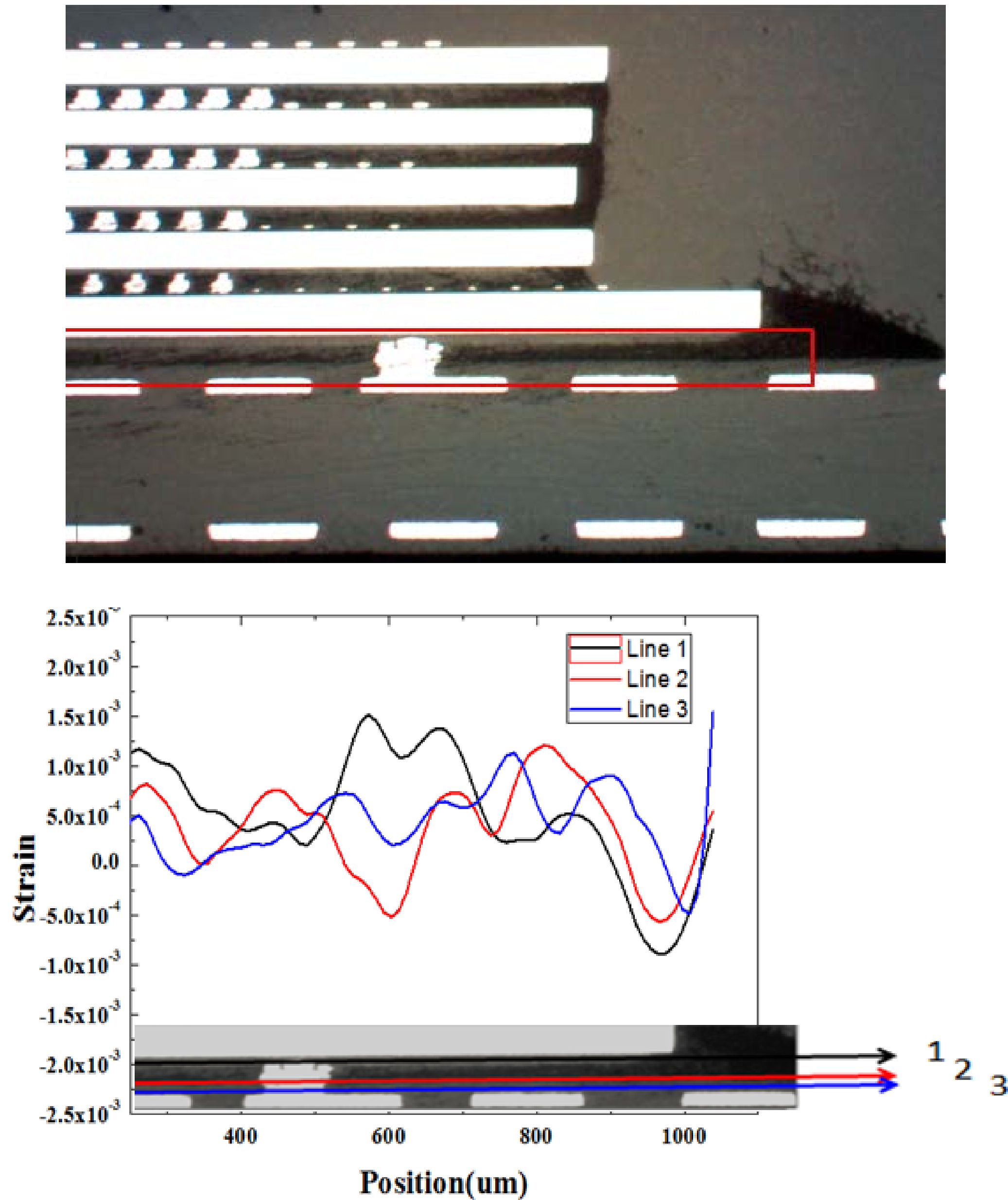


Fig. 4.16 Shear strain distribution in the region of interest

Based on these diagrams, several useful observations can be obtained. First, the overall shear strains are small, but along all three lines, they increase when the die edge is approached.

Second, peak values of shear strain are observed at outer corner of the solder ball between master die and substrate (Line1) and at die edge (Line 1). Therefore those areas have the largest shear strain and stress concentration and are more prone to underfill delamination failures.

4.7 Summary

As a typical example of 3D IC package, a stack-die memory package is presented. Finite element analysis combined with cross-section Raman measurement and high resolution moiré interferometry were employed to investigate the thermal-mechanical reliability and chip-package interaction of the stack-die memory structure. Firstly, an effective moduli method is developed to overcome the challenge in wafer level modeling. The method is validated by bending beam experiment, and then applied to characterize the wafer level warpage of the stacked-die memory structure. Secondly, combined with the effective moduli method, sub-modeling technique is employed to investigate the TSV/solder level stress distribution. Cross-section Raman measurement is carried out at the cross-section top dies to investigate the stress distribution around TSV structure, which is found to be affected by package-induced stress. The experimental results and FEA simulation are presented to be in good agreement. Lastly, high resolution moiré interferometry was used to measure the package induced deformation and stress. Large thermal strain is observed in the solder/underfill layer, especially at die corner. Together, a complementary approach to characterize the thermo-mechanical reliability of stack-die memory package is presented.

Chapter 5 Conclusions and Outlook

5.1 Conclusions

Three-dimensional (3-D) integration is effective to overcome the wiring limit imposed on device density and performance with continued scaling. The application of TSV (Through-Silicon Via) is essential for 3D IC integration. TSVs are embedded into the silicon substrate to form vertical, electrical connections between stacked IC chips. However, due to the large CTE mismatch between Silicon and Copper, thermal stresses are induced by various thermal histories from the device processing, and they have caused serious concerns regarding the thermal-mechanical reliability. In this dissertation, various experimental methods, including Micro-Raman spectroscopy and high resolution Moiré were used to characterize thermo-mechanical reliability of 3D IC structures.

First, a semi-analytic approach is introduced to serve as a proper approach to understand stress distributions in TSV structures. [30] This is followed by application of finite element analysis for more accurate prediction of stress behavior according to the real geometry of the sample. The conventional Raman method is used to measure the linear combination of in-plane stress components near silicon top surface. The comparison between experimental results and FEA calculation shows a reasonable agreement, but there is minor discrepancy when approaching the TSV. The effect of residual stress in both surface and sidewall oxide layer is investigated by conventional Raman spectroscopy. The results show that the stress state of oxide layer does contribute to the minor discrepancy observed, and should be considered as an important factor for the near surface stress distribution.

Second, the limitation of conventional Raman method is discussed: only certain linear combination of in-plane stress, instead of separate value for each stress components, can be obtained. In Chapter 3, two different kinds of innovative Raman measurements have been developed and employed to study the normal stress components separately. Both of them take advantages of different laser polarization profiles to resolve the normal stress components separately based on experimental data. The top view Raman measurements utilize so called "high NA effect" to obtain additional information, and can resolve all 3 normal stress components. From the cross-section Raman measurements, only the in-plane stress distribution can be determined with reasonable assumption based on FEA simulation. As an effective way to evaluate the average stress induced in TSV structure, independent bending beam experiments are used to validate the results from cross-section Raman measurement on the same sample. The correlation between top-down Raman measurement and cross-section Raman measurement are investigated as well. With the assistance of finite element analysis, these comparisons show good consistency among different experiment methods.

In the last chapter, as a typical example of 3D IC package, a stack-die memory package is presented. Finite element analysis combined with cross-section Raman measurement and high resolution moiré interferometry were employed to investigate the thermal-mechanical reliability and chip-package interaction of the stack-die memory structure. Firstly, an effective moduli method is developed to overcome the challenge in wafer level modeling. The method is validated by bending beam experiment, and then applied to characterize the wafer level warpage of the stacked-die memory structure. Secondly, combined with the effective moduli method, sub-modeling technique is employed to investigate the TSV/solder level stress distribution. Cross-section Raman measurement is carried out at the cross-section top dies to investigate the stress

distribution around TSV structure, which is found to be affected by package-induced stress. The experimental results and FEA simulation are presented to be in good agreement. Lastly, high resolution moiré interferometry was used to measure the package induced deformation and stress. Large thermal strain is observed in the solder/underfill layer, especially at die corner. Together, a complementary approach to characterize the thermo-mechanical reliability of stack-die memory package is presented.

5.2 Outlook

For future studies, a few possible topics are suggested. First, as discussed in Chapter 3.1, top view Raman measurement with “high numerical aperture effect” is able to determine the normal stress components separately. This would be a meaningful experimental method to determine “keep-away-zone” (KOZ). The stress induced by TSV can affect the carrier mobility due to the piezo-resistivity effect to degrade the performance of the MOSFET devices [50] [51] [52]. For TSV structures, a tensile stress of 100 MPa was found to enhance the electron mobility of up to 7% for n-type Si. For p-type Si, however, the stress can either enhance or degrade the hole mobility, depending on the transistor channel direction [52]. It has also been reported that the TSV-induced stresses can cause up to 30% shift in the saturation drain currents (I_{DSAT}) of the transistor to degrade the device performance [53]. Simulation work has been carried out to determine the range keep-out-zone [54], but it is difficult to determine the range of KOZ experimentally by other stress measurement method, even the conventional Raman measurement. With the top-down Raman measurement, the mobility change can be calculated based on the normal stress components obtained from experiment. The range of KOZ can be evaluated directly by experiment without knowing the thermal history of TSV structures.

Second, chip-packaging interaction (CPI) is becoming a critical reliability issue for 3D IC packages with Cu/low-k chips, TSV interconnect and organic substrate. One interesting topic would be to investigate the crack driving force induced by chip-package interaction in the ultra low-k interconnects. Due to the small scale of the ultra low-k interconnects, sub-modeling would be required to analyze the chip-packaging interaction. However, conclusions merely from the FEA simulation would not be convincing due to the various assumptions involved. The experiment approach in Chapter 4 presents both the localized stress profile (cross-section Raman measurement) as well as overall package-induced stress/deformation (high resolution moiré interferometry). Such an experimental approach would be an effective method to validate the results from sub-modeling of specific 3D IC packages, and thus render the prediction from the FEA model more reliable and valuable.

Appendix: Sub-modeling Technique

In finite element analysis, the finite element mesh is sometimes too coarse to produce satisfactory results in a specific region of interest, such as a stress concentration region in a stress analysis.

Submodeling is also known as the cut-boundary displacement method or the specified boundary displacement method. The cut boundary is the boundary of the submodel which represents a cut through the coarse model. Displacements calculated on the cut boundary of the coarse model are specified as boundary conditions for the submodel.

Submodeling is based on St. Venant's principle, which states that if an actual distribution of forces is replaced by a statically equivalent system, the distribution of stress and strain is altered only near the regions of load application. The principle implies that stress concentration effects are localized around the concentration; therefore, if the boundaries of the submodel are far enough away from the stress concentration, reasonably accurate results can be calculated in the submodel.

The ANSYS program does not restrict submodeling to structural (stress) analyses only. Submodeling can be used effectively in other disciplines as well. For example, in a magnetic field analysis, you can use submodeling to calculate more accurate magnetic forces in a region of interest.

Aside from the obvious benefit of giving you more accurate results in a region of your model, the submodeling technique has other advantages:

- It reduces, or even eliminates, the need for complicated transition regions in solid finite element models.

- It enables you to experiment with different designs for the region of interest (different fillet radii, for example).
- It helps you in demonstrating the adequacy of mesh refinements.

Some restrictions for the use of submodeling are:

- It is valid only for solid elements and shell elements.
- The principle behind submodeling assumes that the cut boundaries are far enough away from the stress concentration region. You must verify that this assumption is adequately satisfied.

The process for using submodeling is as follows:

- Create and analyze the coarse model.
- Create the submodel.
- Perform cut boundary interpolation.
- Analyze the submodel.
- Verify that the distance between the cut boundaries and the stress concentration is adequate.

1. Create and Analyze the Coarse Model

The first step is to model the entire structure and analyze it. The initial model is referred to as the coarse model. This does not mean that the mesh refinement has to be coarse, only that it is relatively coarse compared to the submodel. The analysis type may be static (steady-state) or transient and follows the same procedure as described in the individual analysis guides. Some additional points to keep in mind are listed below.

Jobname - You should use different jobnames for the coarse model and the submodel. This way, you can keep files from being overwritten. Also, you can easily refer to files from the coarse model during cut boundary interpolation.

Element Types -- Only solid and shell elements support the submodeling technique. Your analysis may include other element types (such as beams added as stiffeners), but the cut boundary should only pass through the solids or shells.

A special submodeling technique called shell-to-solid submodeling allows you to build your coarse model with shell elements and your submodel with 3-D solid elements. This technique is discussed in Shell-to-Solid Submodels.

Modeling -- In many cases, the coarse model need not include local details such as fillet radii, as shown in the following figure. However, the finite element mesh must be fine enough to produce a reasonably accurate degree of freedom solution. This is important because the results of the submodel are almost entirely based on interpolated degree of freedom results at the cut boundary

Files - Both the results file (Jobname.RST, Jobname.RMG, etc.) and the database file (Jobname.DB, containing the model geometry) are required from the coarse-model analysis. Be sure to save the database before going on to create the submodel. To save the database, use one of these methods:

2. Create the Submodel

The submodel is completely independent of the coarse model. Therefore, the first step after the initial analysis is to clear the database at the Begin level. (Another way is to leave and re-enter the ANSYS program.) To clear the database at the Begin level, use one of these methods:

Then enter PREP7 and build the submodel. Some points to remember are:

- Use the same element type (solid or shell) that was used in the coarse model. Also, specify the same element real constants (such as shell thickness) and material properties. (Another type of submodeling - shell-to-solid submodeling - allows you to switch from shell elements in the coarse model to 3-D solid elements in the submodel; see Figure 9.9.)

- The location of the submodel (with respect to the global origin) must be the same as the corresponding portion of the coarse model

Be aware that node rotation angles might be changed by application of nodal constraints [**DSYM**], by transfer of line constraints [**SFL**], or by transfer of area constraints [**SFA**], as well as by more obvious methods [**NROTAT** and **NMODIF**]. The presence or absence of node rotation angles in the coarse model has no effect upon the submodel. Loads and boundary conditions for the submodel will be covered in the next two steps.

3. Perform Cut-Boundary Interpolation

This is the key step in submodeling. You identify the nodes along the cut boundaries, and the ANSYS program calculates the DOF values (displacements, potentials, etc.) at those nodes by interpolating results from the full (coarse) model. For each node of the submodel along the cut boundary, the ANSYS program uses the appropriate element from the coarse mesh to determine the DOF values. These values are then interpolated onto the cut boundary nodes using the element shape functions.

The following tasks are involved in performing the cut boundary interpolation:

1. Identify and write the cut-boundary nodes of the submodel to a file (Jobname.NODE by default). You can do this in PREP7 by selecting nodes along the cut boundaries and then using NWRITE to write the nodes to a file.
2. Restore the full set of nodes, write the database to *Jobname.DB*, and leave PREP7. You must write the database to *Jobname.DB* because you need to continue with the submodel later.
3. To do the cut boundary interpolation (and the temperature interpolation), the database must contain the geometry for the coarse model. Therefore, you must resume the database using one of the methods shown below, making sure to identify the name of the coarse-model database file:
4. Enter POST1, which is the general postprocessor (**/POST1** or menu path **Main Menu> General Postproc**). Interpolation can only be performed in POST1.
5. Point to the coarse results file (**FILE** or menu path **Main Menu> General Postproc> Data & File Opts**).
6. Read in the desired set of data from the results file (**SET** or menu path **Main Menu> General Postproc> Read Results> *option***).
7. Initiate cut-boundary interpolation by CBDOF command.
8. By default, the **CBDOF** command assumes that the cut boundary nodes are on file Jobname.NODE. The ANSYS program will then calculate the cut boundary DOF values and write them in the form of **D** commands to the file *Jobname.CBDO*.
9. All interpolation work is now done, so leave POST1 [**FINISH**] and restore the submodel database (**RESUME** or menu path **Utility Menu> File> Resume from**). (Be sure to use the submodel database jobname.)

4. Analyze the Submodel

In this step, you define the analysis type and analysis options, apply the interpolated DOF values (and temperatures), define other loads and boundary conditions, specify load step options, and obtain the submodel solution.

The first step is to enter SOLUTION (**/SOLU** or menu path **Main Menu> Solution**).

Then define the appropriate analysis type (usually static) and analysis options.

To apply the cut boundary DOF constraints, simply read in the file of **D** commands (created by **CBDOF**) using one of these methods (for example, **/INPUT**,,CBDO).

It is important that you duplicate on the submodel any other loads and boundary conditions that existed on the coarse model. Examples are symmetry boundary conditions, surface loads, inertia forces (such as gravity), concentrated force loads, etc. Then specify load step options (such as output controls) and initiate solution calculations using SOLVE command.

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