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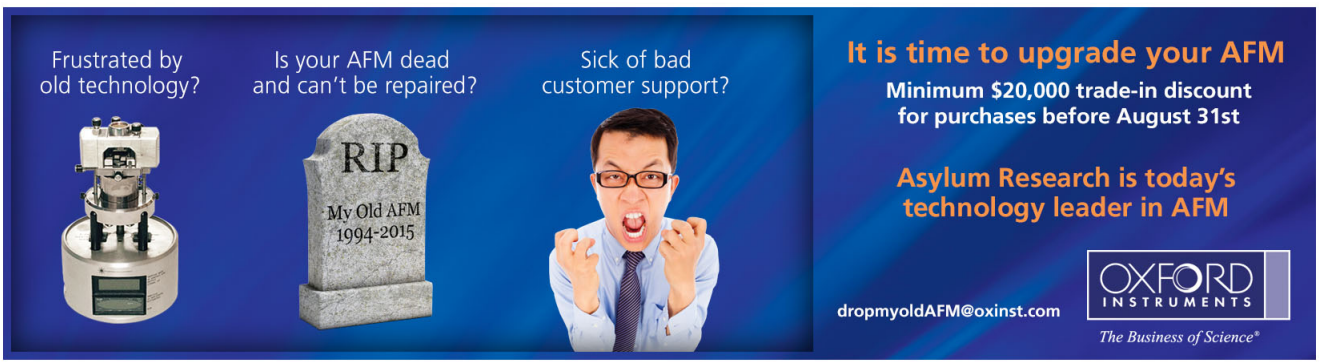

Stabilization of multiple resistance levels by current-sweep in SiO_x-based resistive switching memory

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Using current-sweep measurements, the set process in SiO_x-based resistive random access memory (RRAM) has been found to consist of multiple resistance-reduction steps. Variation in set behaviors was observed and attributed to different defect distributions in the resistance switching region. Physical mechanism of electroforming process is discussed, which further explains the observed variation of defect distributions. A compliance current study confirms that the achievable memory states of SiO_x RRAM are determined by its set behavior. This finding provides additional insight on achieving multi-bit memory storage with SiO_x RRAM. © *2015 AIP Publishing LLC*.
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Nonvolatile memories (NVM) are ubiquitous in portable electronic products such as mobile phones, digital cameras, notebook computers, mp3 players, and Universal Serial Bus (USB) flash drives. The most widespread NVM device, flash memory, is based on the use of polycrystalline silicon (Si) as a floating gate to store charge injected from a Si transistor channel.[1] However, flash memory is facing several challenges such as scalability limits, slow write/erase speed, and high power consumption.[2,3] Therefore, researchers have considered new storage materials and novel structures in nonvolatile memory devices to replace the conventional floating gate flash. Leading contenders currently include phase change memory, magnetic random access memory, ferroelectric random access memory, and resistive random access memory (RRAM).[4–7] RRAM technologies are of particular interest due to its high density, low cost, low power consumption, fast switching speed, and simple cell structure (ideally a cross-bar architecture).[8–10] RRAM based on silicon oxide (SiO_x) stands out among other RRAM because it has a unique unipolar operation mode, high on/off ratio, excellent scalability, good high temperature performance, and compatibility with standard CMOS technology.[11] Much work has been done to optimize the structure, fabrication procedure, dielectric material, and to understand the operating mechanisms of SiO_x-based RRAM.[12–21] In these studies, voltage sweep measurements were the fundamental characterization method to obtain switching parameters, such as set voltage, reset voltage, and high-resistance state (HRS) to low-resistance state (LRS) resistance ratio.

Voltage sweep measurements provide useful resistive switching data for benchmarking the performance of SiO_x-based RRAM devices. However, due to the voltage-triggered switching mechanisms of SiO_x-based RRAM, the voltage sweep measurement only succeeds in characterizing the detailed reset behavior of the device, but fails to properly capture the details of the set process. Therefore, we used its counterpart, the current sweep measurement, to improve data acquisition and enhance the understanding of the physics related to the set process. The results show that the set process is not a one-step resistance change phenomenon. Instead, the set process captured by current sweep measurements consists of multiple resistance reduction occurrences. These multiple resistance reduction steps are in good agreement with previously reported compliance current (CC) study results.[15,22] Different set behaviors are observed, often within a single sample, which are attributed to the random distribution of hydrogenated defects that is determined primarily by the electroforming step. The different set behaviors can potentially be explained by defect distribution, with a more continuous defect distribution being related to multiple discrete memory states within the device. These results are useful in guiding efforts to achieve multi-bit programming by optimizing the defect distribution and/or the electroforming process.

Heavily doped n-type (100) silicon wafers with resistivity of 10^{-3} Ω cm were used as substrate for SiO_x RRAM device fabrication. Native oxide was first removed using buffered oxide etch (BOE). Then a layer of SiO_x with a thickness of 51 nm was deposited using electron-beam evaporation at 130 °C. A 250 nm-thick tantalum nitride (TaN) layer was deposited onto the SiO_x layer using reactive sputtering and was then patterned and dry-etched using carbon tetrafluoride (CF_4) to form the top electrode. The SiO_x in the field region was then removed with BOE, resulting in an RRAM device with an etched SiO_x edge between top TaN and bottom silicon electrodes, called metal-insulator-semiconductor (MIS) devices. A Lake Shore Cryotronics vacuum probe chamber (<1 mTorr) and Agilent B1500A device analyzer were used to electroform devices and perform voltage and current sweep measurements. Note that we did not observe any degradation/stability issues for the middle states achieved with both switching methods, and the measured current levels are the average of 30 repeated measurements. Resistive switching parameters were extracted for all samples: "Set Voltage" (V_{set}) is the voltage where the transition

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from the HRS to the LRS occurs in the current-voltage (I–V) response; and similarly, "Reset Voltage" (V_{reset}) is the voltage where the transition from LRS to HRS begins to occur (for example, see Fig. 1(a)).

Fig. 1(a) is the voltage sweep measurement result showing both HRS and LRS curves with V_{set} and V_{reset} labeled. The inset shows the electroforming process of the device, which is achieved with a 0 V to 15 V and back to 0 V voltage double sweep. An unusual electrical characteristic of SiO_x-based RRAM is the backward-scan effect where the duration of the reverse sweep during electroforming or reset determines whether a state change occurs. We have proposed a resistive switching model involving the transformation between a hydrogen bridge (Si-H-Si) defect in the LRS and a hydrogen doublet (Si-HH-Si) defect in the HRS driven by proton (H^+) transfer.[22,23] In this model, electron de-trapping from Si-HH-Si initiates H^+ emission to form Si-H-Si during the set process, and electron tunneling or thermal energy induces the capture of H^+ by Si-H-Si to re-form Si-HH-Si during the reset process. At large applied voltage ($> \sim 5$ V), the reset process dominates over the set process, and the device is reset to a HRS if the applied voltage is quickly dropped to zero. However, if the backward DC sweep is too slow, when the voltage drops below ~5 V H^+ emission from Si-HH-Si (set process) can dominate H^+ capture by Si-H-Si (reset process) so that a change in state from HRS to LRS occurs, thus leading to the backward-scan effect. In the voltage sweep measurement result, Fig. 1(a), the set process shows a very sharp current increase at V_{set}. Based on this observation, an intuitive hypothesis would describe the set process as being a one-step physical phenomenon that instantaneously changes the resistance of the device from a high value to a low value. However, such a hypothesis is in contradiction with a previously reported compliance current study,[15] where it was found that device resistance could be controlled by adjusting the compliance current limit during the set process to achieve multiple resistance/memory states. Such a discrepancy suggests that the steep current increase measured by the voltage sweep is not providing enough detailed information to fully understand the set process of the SiO_x RRAM device.

To further understand the set process, current sweep measurements were performed to better characterize the SiO_x RRAM set process. Fig. 1(b) shows the current sweep measurement result for RRAM device switching from HRS to LRS. The x-axis is the applied current and the y-axis on the left is the measured voltage across the device. The y-axis on the right is the measured conduction current through the device. As expected, the measured conduction current is the same as the applied current. However, as discussed in more detail later, at conduction current ~7 mA, the measured conduction current drops suddenly. The same device was used for both voltage and current sweep measurements, where the device was previously switched to HRS using the same 0 V to 10 V voltage sweep so that both measurements characterize the same physical resistive switching phenomenon.

It may be noted that there are several voltage peaks and valleys in the current range between 3×10^{-6} A and 2×10^{-3} A in Fig. 1(b). Each peak to valley transition indicates that the voltage across the device has decreased dramatically whereas the conduction current remained the same. In other words, the resistance of the device decreased multiple times during the set process. It was also observed that each current peak occurred at a consistent voltage level, defined as the Trigger Voltage ($V_{trigger}$), which is about 3.2 V, which is closed to the set voltage value obtained using the voltage sweep.[15]

The steep voltage rise at conduction current ~7 mA observed in the current sweep indicates the onset of device reset. Due to the self-compliant nature of the SiO_x-based RRAM device,[24] the reset voltage is larger than the set voltage. We have observed similar behavior when varying the gate voltage of a MOSFET in series with the RRAM device in order to control the external resistance of the circuit.[24] For MIS devices, contact resistance between the probe and TaN top electrode can be relatively large due to the high hardness

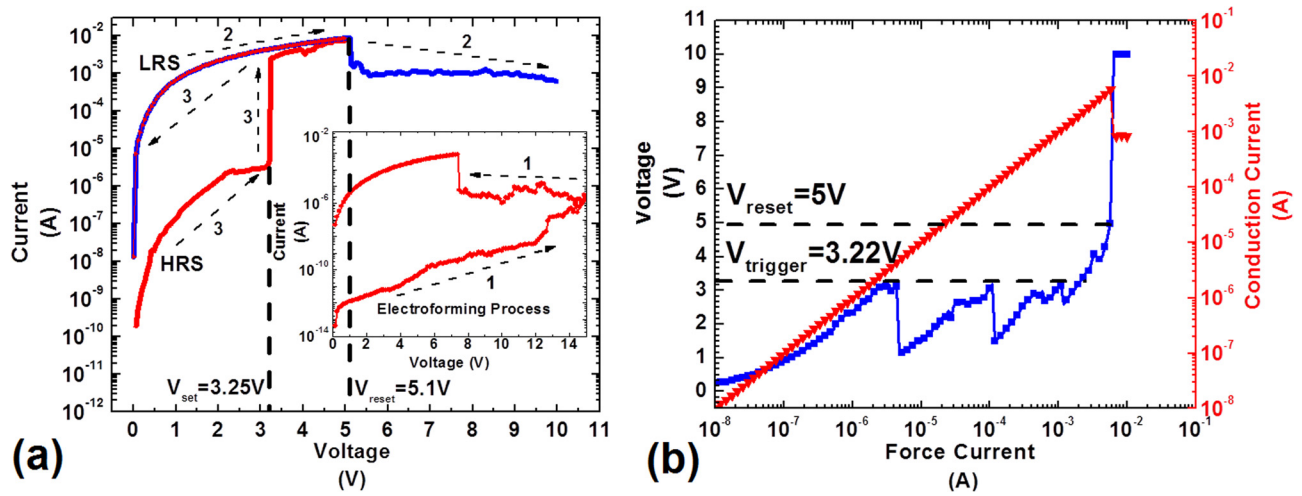

FIG. 1. (a) Voltage sweep I–V plot showing resistive switching behaviors of the SiO_x-based RRAM device. Set voltage V_{set} and reset voltage V_{reset} are identified in the plot. The inset shows the electroforming I-V curve using a forward/reverse voltage sweep. The DC voltage sweep sequences are as follows. (1) Electroforming with a voltage sweep from 0 V to 15 V and back to 0 V. After electroforming the device is in LRS. (2) Reset process with a voltage sweep from 0 V to 10 V. (3) Set process with a voltage sweep from 0 V to 5 V and back to 0 V. (b) Current sweep V-I plot for the same device with trigger voltage $V_{trigger}$ and reset voltage V_{reset} identified.

of the TaN material, and the heavily doped Si substrate further increases the external series resistance. As a result, there is a larger voltage drop across the series resistance in the MIS devices, and therefore MIS devices require higher applied voltage to initiate the reset process. The reset process takes place when the voltage reaches a threshold level (i.e., reset voltage of 5.1 V in this example),[17] and the resistance begins to increase while the conduction current decreases. After the set process, the device stays in the LRS. Further increase in force current causes the device to reset. And beyond the reset point, applied current and conduction current (red curve in Fig. 1(b)) are no longer the same. Any further increase in applied current causes the voltage across the device to increase until it reaches the voltage compliance limit, which in this case is 10 V. Above this point, the conduction current stayed at 10^{-3} A, the same value as measured by the voltage sweep in Fig. 1(a). The reset voltages obtained using voltage sweep (5.1 V) and current sweep (5.0 V) are in good agreement.

A CC study was then performed on the same device. The RRAM device was first switched to HRS using a 0 V to 10 V DC voltage sweep. Then, a 0 V to 4 V DC voltage sweep with varying compliance current (4×10^{-5} A, 3×10^{-4} A, no compliance) was used to switch the device to different memory states. The intermediate resistance states achieved by switching the device with compliance current were also observed during the current sweep measurement (see Fig. 2). This not only suggests that current sweep is a viable method to achieve multiple memory states in a single device but also proves to be more informative when characterizing the set behavior of the SiO_x-based RRAM device. Note that we did not observe any degradation issues for either switching technique, which may be due to the "self-compliant" nature of the device.

It may also be noted that the set property of the SiO_x-based RRAM device exhibits some variation. As shown in Fig. 3, three different devices fabricated on the same wafer showed a variety of set behaviors captured by current sweep measurements. As the current is ramped-up, the voltage always reaches the same trigger voltage (~3.2 V) when the set transition occurs (e.g., the voltage drop). This finding agrees with the hydrogenated defect-switching model for SiO_x-based RRAM devices, where the energy level of switching defects in SiO_x dictates the same trigger voltage no matter where the defects are located in the filament.[19] The number of transitions, on the other hand, is found to vary from device to device. For example, Device I exhibits only one transition, but Devices II and III have 4 and 8 transitions, respectively. This may be the result of varying defect distributions generated by the electroforming process for each device. In other words, there is a distribution of defects within the switching or the "gap" region along the filament which transform between the conductive hydrogen bridge defect (responsible for the LRS) and the non-conductive hydrogen doublet defect (responsible for the HRS).[19] Therefore, the number of switching defects and their distribution within the gap determines whether the set process shows a single large transition (for the case of a single defect group in the gap) or multiple smaller transitions (for the case of continuously distributed defects), as shown in the insets of Fig. 3.

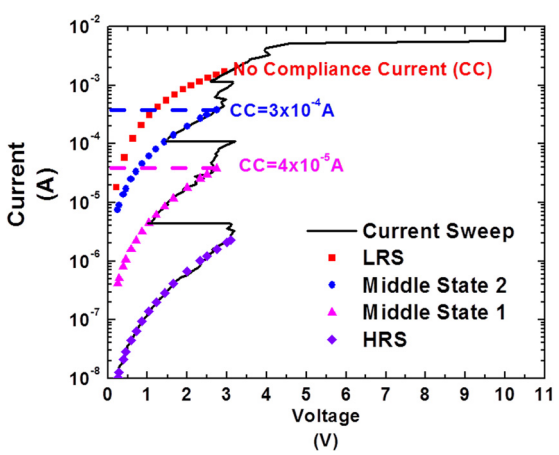

FIG. 2. Current sweep I-V plot with overlaying compliance current result (CC: 4×10^{-5} A, 3×10^{-4} A, none).

A review of electroforming mechanisms would help explain how the random nature of the percolation pathway can lead to the observed variation in the set process. Electroforming in SiO_x materials is thought involve oxygen reduction mechanisms that create a Si-rich conductive filament (CF).[11,20,21] The canonical view of the oxygen reduction process can be summarized as follows. Under the high electric fields applied during electroforming, high-energy electron impacts break Si-O bonds to release O^{2-} ions and form Si-Si oxygen vacancy defects, leading to a percolation pathway that can cause stress induced leakage current, dielectric soft breakdown, and time dependent dielectric breakdown.[25,26] It can also lead to oxide hard breakdown when a critical defect density is reached.[24] It is reasonable to expect that similar percolation pathways are created by the electroforming process. However, a percolation pathway formed by Si-Si defects alone cannot explain unipolar reversible switching in SiO_x materials.[19] Hydrogen is ubiquitous in SiO_x materials and is often considered to be an intrinsic defect.[25,27] The hydrogen bridge (Si-H-Si) has been identified as the most likely defect responsible for stress induced leakage current,[25] and its inter-conversion product can potentially promote the oxygen reduction reaction.[14,19] Previous reports have described in detail how defects along the CF may transform between the hydrogen bridge (Si-H-Si) and the hydrogen doublet (Si-H H-Si) through proton exchange reactions with a water molecule, and how such localized transformations provide a reasonable model of resistive switching in SiO_x materials.[18,19] The good endurance and retention properties of SiO_x-based RRAM suggest that the hydrogenated defect clusters remain localized and do not migrate after the electroforming process is complete. Therefore, the spatial distribution of defects in the switching region is determined primarily by the electroforming process, and the number of defects that participate in reversible switching will determine how many transitions are observed during the set process. As a result, a larger number of defects will likely be associated with a higher number of set transitions, as observed in Fig. 3.

In practice, the ability to discern multiple resistance states will require the ability to clearly distinguish each resistance state from other states, which typically means that there

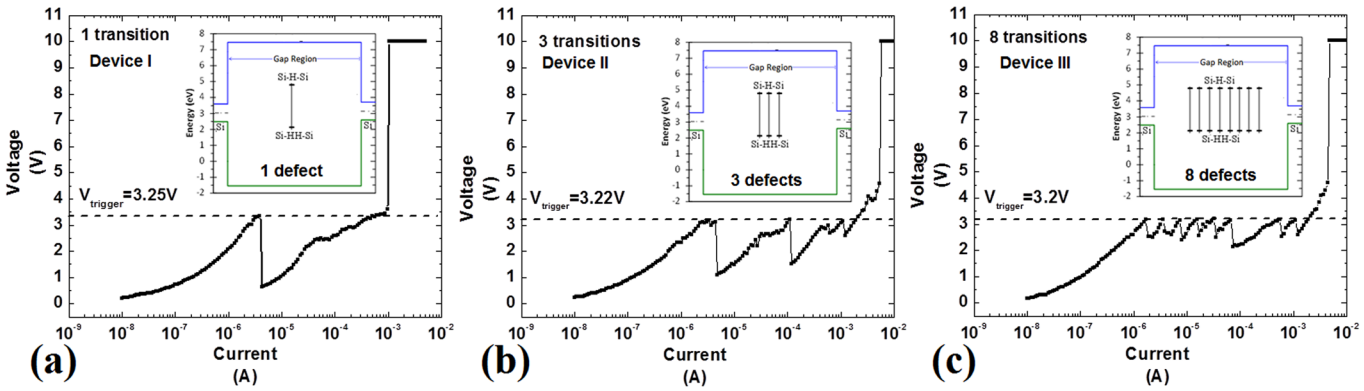

FIG. 3. Current sweep V-I plots for: (a) Device I; (b) Device II; and (c) Device III. The insets show the hypothesized hydrogenated defect distributions within the switching "gap" region corresponding to each device.

should be at least 1 order of magnitude separation between the resistance values of multiple states. Thus, it is important to characterize how many discrete memory states (resistance levels) can be programed using either a compliance-current-limited voltage sweep or the current sweep method. The continuously distributed defects in Device III (Fig. 3(c)) would definitely favor more discrete states, while the single defect in Device I (Fig. 3(a)) may only result in a single pair of resistance states. Voltage sweep measurements with compliance current limits varying over a range from 10^{-6} A to 10^{-3} A were performed on Devices I, II, and III. The results shown in Fig. 4 confirm the correlation between set behavior and the number of achievable discrete memory states, which are presumably due to different defect distributions in the three devices. Device III achieved a total of 6 different resistance levels, whereas Device I only achieved 2. Clearly, Device III would outperform Device II and Device I for applications requiring multiple bits per cell. Due to the random nature of percolation pathway electroforming, it may be challenging to develop a specific process or a certain electroforming procedure that would consistently lead to the multi-set behavior exhibited by Device III. In our future work, we will investigate various forming gas anneals and electroforming in a hydrogen containing ambient in order to controllably provide varying distributions of hydrogenated defects as possible methods to achieve repeatable multi-state operation.

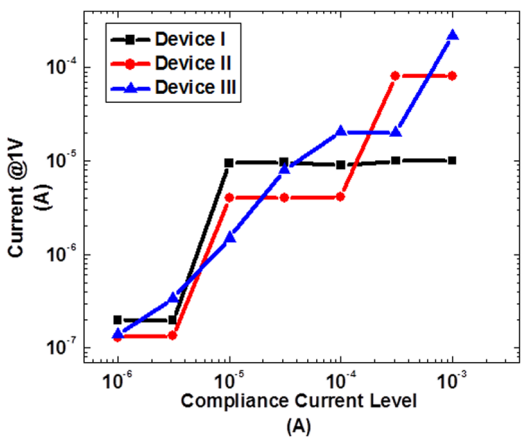

FIG. 4. Measured current at 1 V (memory state) for Devices I, II, and III after being set with varying compliance currents (10^{-6} A to 10^{-3} A) plotted against the compliance current limit.

In conclusion, current sweep measurements on SiO_x RRAM devices show very different set behaviors as compared to voltage sweep measurements, where multiple resistance steps were clearly identified by the current sweep. This phenomenon is in agreement with a previous compliance current study and suggests that current sweeps provide a more precise characterization of the set process. By investigating the set behavior of different devices, it was found that the number of resistance steps can change dramatically from device to device. This variation was attributed to the random nature of percolation pathway during electroforming. Finally, our results show how a continuous defect distribution has the potential advantage of achieving multi-bit memory storage and described possible methods for optimizing the defect distribution using hydrogen-based anneals.

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