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Fabrication of Silicon Nanowires with Controlled Nano-scale Shapes Using Wet Anisotropic Etching

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Fabrication of Silicon Nanowires with Controlled Nano-scale Shapes Using Wet Anisotropic Etching

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Dedication

I dedicate this dissertation to my new niece, Buttercup.

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Fabrication of Silicon Nanowires with Controlled Nano-scale Shapes Using Wet Anisotropic Etching

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The University of Texas at Austin, 2015

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Silicon nanowires can enable important applications in energy and healthcare such as biochemical sensors, thermoelectric devices, and ultra-capacitors. In the energy sector, for example, as the need for more efficient energy storage continues to grow for enabling applications such as electric vehicles, high energy storage density capacitors are being explored as a potential replacement to traditional batteries that lack fast charge/discharge rates as well as have shorter life cycles. Silicon nanowire based ultra-capacitors offer increased energy storage density by increasing the surface area per unit projected area of the electrode, thereby allowing more surface "charge" to reside. The motivation behind this dissertation is the study of low-cost techniques for fabrication of high aspect ratio silicon nanowires with controlled geometry with an exemplar application in ultra-capacitors.

Controlled transfer of high aspect ratio, nano-scale features into functional device layers requires anisotropic etch techniques. Dry reactive ion etch techniques are commonly used since most solution-based wet etch processes lack anisotropic pattern transfer capability. However, in silicon, anisotropic wet etch processes are available for the fabrication of nano-scale features, but have some constraints in the range of geometry of patterns that they can address. While this lack of geometric and material versatility

precludes the use of these processes in applications like integrated circuits, they can be potentially realized for fabricating nanoscale pillars. This dissertation explores the geometric limitations of such inexpensive wet anisotropic etching processes and develops additional methods and geometries for fabrication of controlled nano-scale, high aspect ratio features. Jet and Flash Imprint Lithography (J-FIL™) has been used as the preferred pre-etch patterning process as it enables patterning of sub-50 nm high density features with versatile geometries over large areas. Exemplary anisotropic wet etch processes studied include Crystalline Orientation Dependent Etch (CODE) using potassium hydroxide (KOH) etching of silicon and Metal Assisted Chemical Etching (MACE) using gold as a catalyst to etch silicon.

Experiments with CODE indicate that the geometric limitations of the etch process prevent the fabrication of high aspect ratio nanowires without adding a prohibitive number of steps to protect the pillar geometry. On the other hand, MACE offers a relatively simple process for fabricating high aspect ratio pillars with unique cross sections, and has thus been pursued to fabricate fully functional electrostatic capacitors featuring both circular and diamond-shaped nano-pillar electrodes. The capacitance of the diamond-shaped nano-pillar capacitor has been shown to be ~77.9% larger than that of the circular cross section due to the increase in surface area per unit projected area. This increase in capacitance approximately matches the increase calculated using analytical models. Thus, this dissertation provides a framework for the ability to create unique sharp cornered nanowires that can be explored further for a wider variety of cross sections.

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Chapter 1: Introduction

Anisotropic etch techniques are used for controlled transfer of nano-scale features into a thin film or a bulk substrate. Isotropic etchants, which include most liquid etchants, are not feasible for high aspect ratio pattern transfer needed in nanofabrication since isotropic etching leads to non-vertical lateral etching that can undercut the etch mask. This results in loss of feature definition (sharp corners) and critical dimensions (CDs)[1,2]. A diagram depicting the difference between isotropic and anisotropic etching is shown in Figure 1-1. Dry plasma etching processes are used for many applications because of their ability to etch anisotropically. However, such processes require expensive vacuum equipment as well as a variety of consumable gases that may be difficult to facilitate[1,3]. In crystalline silicon, anisotropic wet etch processes are available at the nano-scale. These processes combine the inexpensive nature of wet chemical etching and the controlled anisotropic nature found in dry etching. However, in addition to being limited to crystalline silicon, they are constrained in the complexity of geometry of patterns that they can address[1]. For these reasons, these processes cannot be used in applications like fabrication of integrated circuits which need features of different geometries on the same die, and also need etching of metals, and amorphous dielectrics. The core of this research will explore such inexpensive wet anisotropic etching processes for controlled fabrication of nano-scale features in applications that do not possess the geometry and material complexity found in typical semiconductor manufacturing.

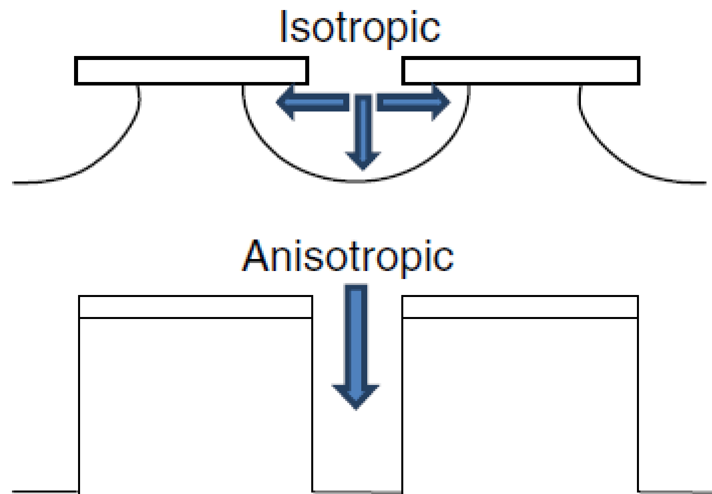


Figure 1-1: Diagram showing isotropic versus anisotropic etching.[4]

1.1 MOTIVATION

The cost of a unit process step depends on the throughput, tool capital cost as well as the cost of consumables. Dry plasma-based etching can be quite expensive, as its throughput is limited in addition to the need for complex vacuum tooling and gas mixtures[1,3]. On the other hand wet processes are relatively inexpensive because wafers can potentially be processed in batches without the need for complex tools. The challenge with using wet etchants for anisotropic etching, however, is that there are unique geometric constraints that make fabricating arbitrary features difficult, as will be seen in Chapter 2 and Chapter 3. If these constraints can be overcome, wet etch techniques like crystallographic orientation dependent etching (CODE) and metal assisted chemical etching (MACE) can inexpensively provide high degrees of anisotropy, comparable to plasma-based etching[1,5]. The main motivation for this study is to reduce fabrication costs by leveraging controlled patterning of feature geometry so as to use wet etching instead of dry etching processes for transferring the pattern onto a crystalline substrate specifically fabrication of high aspect ratio nanowires. There are many applications that

require high aspect ratio nano-scale features such as thermoelectrics[6], biochemical sensors[7], and electronic devices[8,9], and ultra-capacitors[10-12]. This investigation has been conducted in the context of an exemplar application: high storage energy density ultra-capacitors which can potentially benefit from these high aspect ratio nanowires.

1.2 Nano-patterning Processes

There are three main categories of nanopatterning processes: (i) top-down which uses a mask or a template to pattern a sacrificial layer on a substrate, (ii) bottom-up which is the preferential growth and assembly of molecules to create a pattern, and (iii) a combination of the first two where a pattern defined by a top-down process helps direct the assembly of molecules in a bottom-up process[13].

Photolithography is a photon based top-down patterning technique that has been the mainstay of the semiconductor industry but it is limited by diffraction. Overcoming diffraction limits requires the use of expensive processes like double patterning to obtain a resolution better than ~45 nm[13,14]. The next generation of photolithography is extreme ultraviolet but several technical challenges still need to be overcome to make it a viable option[13-15]. Electron-beam lithography can achieve high resolutions but at the price of very low throughput[16].

Imprint lithography is a class of mechanical top-down patterning techniques that has demonstrated sub-10 nm resolution[17]. Thermal nano-imprint lithography, and UV nano-imprint lithography are the two primary techniques that fall under the gamut of imprint lithography. Specifically, this work uses Jet-and-Flash Imprint Lithography, which is a variant of UV nanoimprint lithography as the preferred patterning step.[13,18]

Bottom-up patterning techniques rely on nanoscale phase separation and subsequent self-assembly of a solution to create the desired nanoscale periodic structures.

Block co-polymer solutions, inorganic nano-particle and polystyrene nanosphere dispersions are most commonly used[16]. These solutions can be dispensed on the substrate using techniques such as spin-coating. When the solvent that suspends the solution evaporates, nanophase separation occurs, creating a pattern of nanodomains. In block co-polymer patterning, one of the blocks can be selectively removed, leaving behind the desired pattern. Likewise, self-assembled nano-particles can be sintered to give a pattern, and polystyrene nano-spheres can self-assemble into a periodic pattern that can be used as a mask for subsequent pattern transfer. These techniques can only result in periodic regular patterns and also have trouble with long-range order. Currently, research is being done to mitigate the problems with long-range order by using top-down techniques to create lower resolution features that can guide bottom-up self-assembly.[16,19,20]

1.3 Wet Anisotropic Etching

The three primary types of wet anisotropic etching techniques being used today include (i) crystallographic orientation dependent etching (CODE), (ii) electrochemical etching, and (iii) metal assisted chemical etching (MACE)[3,21-23]. CODE and MACE will be the focus of this study because electrochemical etching has a limit to the possible feature size it can produce due to the effect of the space charge region (SCR). The size of the SCR is dependent on the resistivity of the Si wafer. Wafers with resistivity less than 0.02 ohm-cm are needed to fabricate features less than 50 nm. These wafers need to be highly doped to obtain the required resistivity which limits the potential applications.[24,25] For instance, highly doped silicon has surface traps that reduce conductivity and the surface atoms are highly reactive to the electrolyte which reduces electrochemical stability for capacitors that use liquid electrolytes[26].

1.3.1 Crystallographic Orientation Dependent Etching (CODE)

Crystallographic orientation dependent etching (CODE) is an anisotropic etching technique of crystalline silicon where the etch rate changes based on the crystallographic orientation of the surface exposed to the etch solution. The benefits of crystallographic orientation dependent etching is that very smooth sidewalls and sharp corners can be fabricated compared to the other methods of anisotropic wet etching[1,27]. Unfortunately, the shape and orientation of the features being etched are constrained due to the dependence on the crystallographic planes. This process has been used for applications in MEMS and etching through wafer vias[28-30]. Table 1-1 lists some common CODE techniques. From Table 1-1, it is evident that Potassium hydroxide (KOH) has a high anisotropic ratio etch rate and is also relatively more benign to handle. Hence, KOH has been used as the preferred etchant for Si.

Table 1-1: Comparison of Anisotropic Wet Etchants.

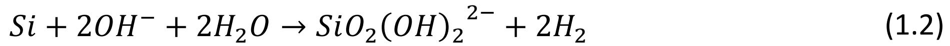
Etchant	Pros	Cons
Ethylenediamine Pyrocatechol (EDP)	Anisotropic	highly toxic and requires special handling[1,23]
Hydrazine	Anisotropic	highly toxic, potentially explosive, and requires special handling[1,23,31]
Potassium Hydroxide (KOH)	Anisotropic, high etch rate, high anisotropic ratio, and non-organic (easier to dispose of than TMAH)[23] excellent uniformity and reproducibility[32]	not compatible with CMOS (mobile K+ ion contamination)[1,23]
Tetramethylammonium Hydroxide (TMAH)	anisotropic, compatible with CMOS, and highly selective to SiO_2[23]	more expensive to dispose of organic solutions than non-organic, low etch rate, low anisotropic ratio[1,23,31]

1.3.1.1 Etching Mechanism of KOH

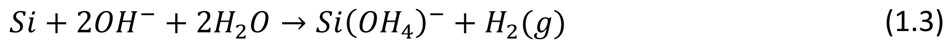
KOH is an alkaline etchant that is described by several slightly different etching mechanisms, three of which are given in Equations 1.1-1.3. Equation 1.1 and Equation 1.3 are very similar but Equation 1.1 doesn't show the hydroxide ion even though it is needed to catalyze the reaction and keep the product soluble[23,33]. All the reactions produce gaseous hydrogen which can affect surface roughness by acting like a local mask if it adheres to the silicon surface. Isopropanol (IPA) can be added to the etching solution

to increase the wettability of the etchant and keep the hydrogen bubbles from sticking to the surface[31]. Another method of reducing the effect of hydrogen bubbles is to agitate the solution through ultra-sonication[34].

$$Si + 4H_2O \rightarrow Si(OH)_4 + 2H_2 \quad (1.1)$$



$$Si + 2OH^- + 2H_2O \rightarrow SiO_2(OH)_2{}^{2-} + 2H_2 \quad (1.2)$$



$$Si + 2OH^- + 2H_2O \rightarrow Si(OH_4)^- + H_2(g) \quad (1.3)$$

1.3.1.2 CODE of Si using KOH

KOH etches single crystalline silicon at different rates depending on the exposed surface's crystallographic orientation. Miller indices are used to denote different planes and directions of crystalline silicon*. Figure 1-2 shows examples of the three main planes considered when talking about the anisotropic etching of silicon. Etch anisotropy is defined as the ratio of the lateral etch amount and the etch depth. This value has been found to vary significantly in the literature since it is based on experimental setup and the composition of the etch solution[5,35-37]. A typical anisotropic ratio is reported to be $r_{(110)}: r_{(100)}: r_{(111)} \cong 600: 300: 1$ where r is the etch rate for the given plane[5]. The (111) slow etching planes define the sidewalls of concave features etched into Si. Examples include rectangular/square grooves that are created in (100) silicon with edges aligned to the [110] directions as shown in Figure 1-3; and hexagonal/rhombus cavities with the two sets of vertical (111) planes aligned to the [112] direction and one set of (111) planes aligned to the [110] directions as shown in Figure 1-4 for (110) silicon wafers. (Pal, P. 2013)

* Parentheses are placed around the inverse of the intercepts of a given plane. For example, (110) means that the x and y axes are intersected at 1/1 where 1 is the normalized length of a side of the cubic and the plane is parallel to the z axis since 1/∞=0.

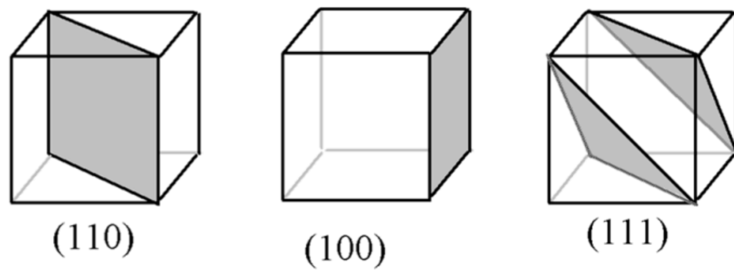


Figure 1-2: Examples of miller indices†

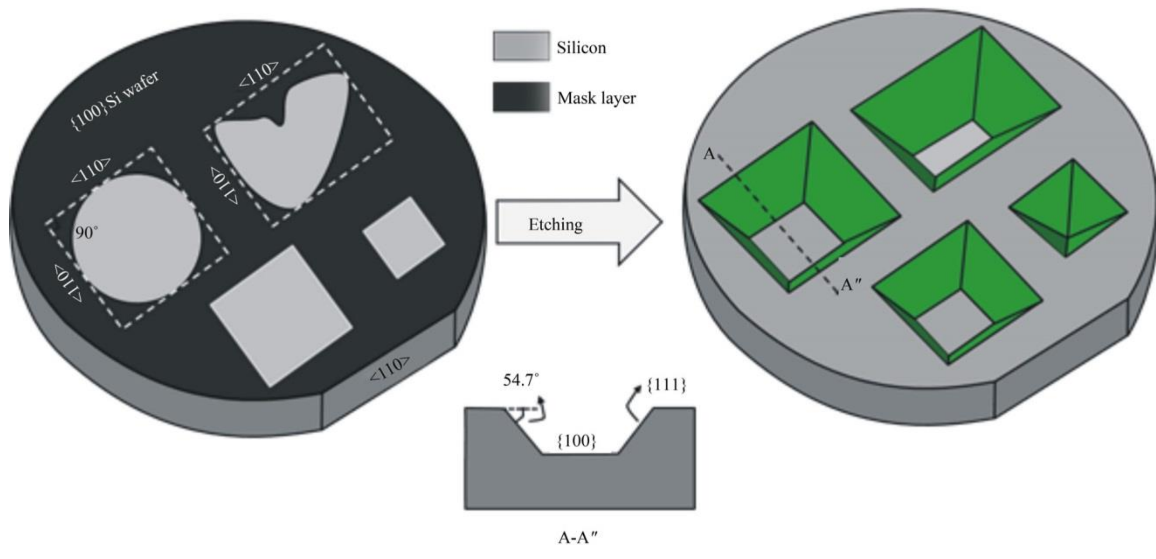


Figure 1-3: Anisotropically etched features in (100) Si wafers.[38]

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† modified from
http://upload.wikimedia.org/wikipedia/commons/f/f5/Indices_miller_plan_exemple_cube.png

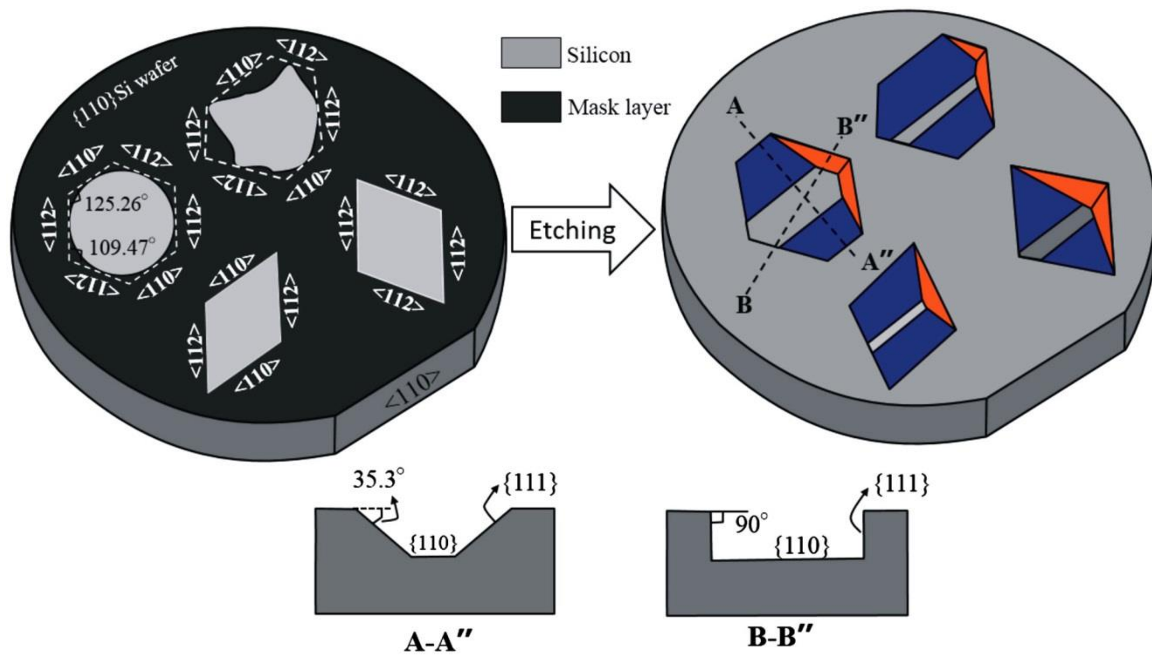


Figure 1-4: Anisotropically etched features in (110) Si wafers.[38]

The primary explanation for the dependence of etch rates on crystallographic orientation is the number of back bonds and the density of dangling bonds for a given perfect crystallographic surface. Each back bond attached to a given atom of Si has to be broken for that atom to be etched away. This requires more energy compared to the removal of dangling bonds. The probability that a given atom will be removed decreases with an increase in energy needed to break all the bonds. A (111) surface has three back bonds and only one sparsely placed dangling bond while a (100) surface has two back bonds and two dangling bonds and a (110) surface has only one back bond with one dangling bond that are more closely packed.[23,39,40] Figure 1-5 and Figure 1-6 show the back bonds and dangling bonds for silicon atoms on the three major crystallographic orientations.

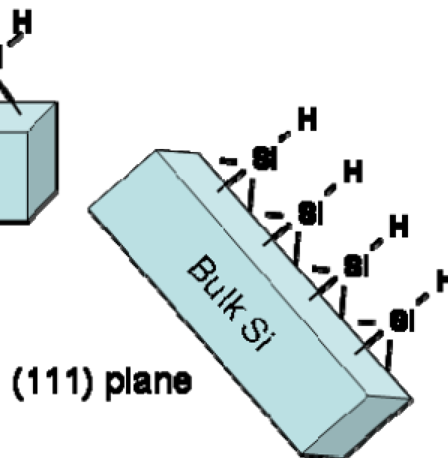


Figure 1-5: Hydrogen terminated bonds are the dangling bonds.[40]

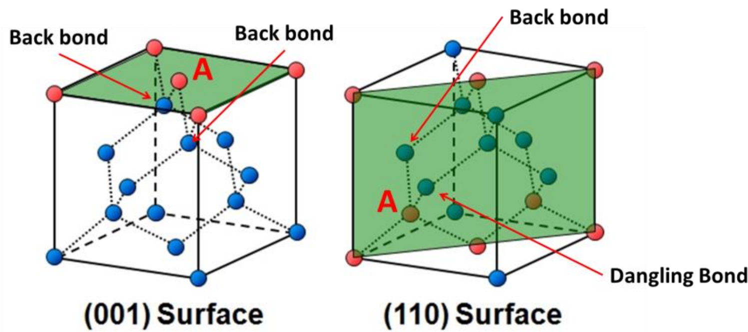


Figure 1-6: Back bonds and dangling bonds are denoted for a surface atom A on the surface represented by the green plane‡

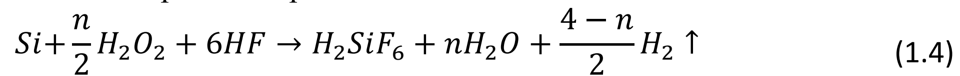
1.3.2 Metal Assisted Chemical Etching (MACE)

Metal assisted chemical etching (MACE) is an anisotropic wet etch technique that has been shown to be able to fabricate high aspect ratio features in c-Si, a-Si, and GaAs.[3,41-47]

‡ http://www.fujitsu.com/img/PR/2008/20081216-01al.jpg

1.3.2.1 MACE Mechanism for c-Si

The etch mechanism occurs when silicon with a patterned noble metal layer (commonly Ag, Au, and Pt) is submerged in a solution containing water, an oxidant (most commonly hydrogen peroxide - H_2O_2), and hydrofluoric acid (HF). The noble metal acts as a catalyst for the reduction of the H_2O_2 (cathode reaction), thereby creating positively charged electron holes. These holes are then injected through the metal to the metal-silicon interface thereby oxidizing the silicon underneath the metal (anode reaction). The oxidized silicon is dissolved by the HF that diffuses from the sides of the metal catalyst and the soluble products diffuse away. This redox reaction can also produce hydrogen gas. There is some dispute about the actual reactions at the metal-silicon interface but most researchers agree that Equation 1.4 is the overall redox reaction shown in Figure 1-7. The variable $n = 2\ to\ 4$ is determined by the ratio of oxidant to HF which determines the etch regime that occurs. The differences between regimes will be discussed in Section 3.2.1. The metal catalyst then fills in the hole created by the dissolved silicon and the process repeats.[3,45,47-49]



$$Si + \frac{n}{2} H_2O_2 + 6HF \rightarrow H_2SiF_6 + nH_2O + \frac{4-n}{2} H_2 \uparrow \quad (1.4)$$

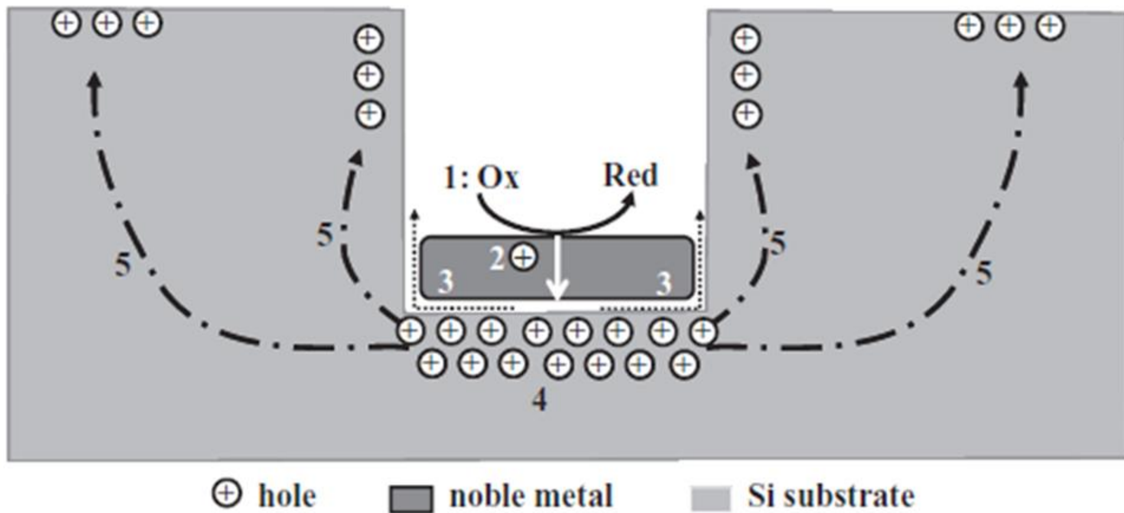


Figure 1-7: Schematic of MACE reactions.[3]

1.3.3 CODE and MACE Comparison

Given that both CODE and MACE can enable highly anisotropic wet etching, it is instructive to compare the two processes with respect to their pros and cons, and the specific geometries that they can address. These have been summarized in Table 1-2 and Table 1-3 respectively. The details captured in Table 1-3 have been discussed later in Sections 2.1-2.2 and Sections 3.1-3.2.

Table 1-2: General comparison of CODE and MACE.

Etch Technique	Advantages	Disadvantages
CODE	Smooth side walls, sharp edges possible	(111) etch stop planes restrict final feature shape to rectangular for (100) wafers and rhombuses and hexagons for (110) wafers
MACE	More arbitrary feature geometries possible, etched patterns defined by the geometry of the catalyst during the etch process	Noble metal left at the bottom of etched feature, rougher sidewalls

Table 1-3: Comparison between CODE and MACE of mask features (details in Chapter 2 and Chapter 3).

Pattern of Hard Mask or Catalyst	CODE	MACE
Dots	Mask lift-off due to undercutting and loss of features	Catalyst can wander from uneven forces (3D motion)[50-52], can prefer to etch along [100] direction depending on solution composition
Layer with openings/Mesh	Non-vertical stop planes prevent high aspect ratio etching, inverted pyramids, hexagon with four vertical sidewalls and two non-vertical that meet in the middle	Deep pillars can be fabricated, mesh prevents lateral motion of individual parts of the catalyst
Lines	Depth of lines depends on the length of the lines, increase in width depends on misalignment to the vertical (111) planes for (110) wafers, long inverted pyramids etched for (100) wafers	Etch direction of flat lines depends on solution composition and wafer orientation, if metal nano-rods are used as catalyst then the rods can return to surface (not just downward etch)[50]

1.4 Proposed Nano-fabrication processes

Jet and Flash Imprint Lithography (J-FIL™), a UV nano-imprint lithography process developed at The University of Texas at Austin and Molecular Imprints, has been used as the preferred pre-etch patterning process as it enables patterning of sub-50 nm high density features with different geometries over large areas. The basic imprint process is shown in Figure 1-8.

Figure 1-8: Process flow for J-FIL™[53]

1.4.1 iCODE Process

Imprint-enabled Crystallographic Orientation Dependent Etching (iCODE) uses J-FIL™ to pattern the hard mask that has been used to perform CODE on (110) silicon. For this, the imprint template needs to be accurately aligned with the correct crystallographic planes to enable <111> plane sidewalls, and hence, get deep, vertically etched features. The two most common hard mask materials for KOH etching are silicon dioxide (SiO_2) and silicon nitride (Si_3N_4). SiO_2 is thermally grown and a low pressure chemical vapor deposition (LPCVD) furnace is used to deposit Si_3N_4. The etch selectivity of Si/SiO_2 in a KOH solution varies with the solution concentration and temperature but is nominally 500, whereas Si_3N_4 can be considered to be not attacked by KOH[1]. Once the hard mask is patterned, the sample is submerged in a heated solution of KOH and deionized (DI) water.

1.4.2 iMACE Process

Imprint-enabled Metal Assisted Chemical Etching (iCODE) uses J-FIL™ to pattern the metal catalyst used to perform MACE on (100) silicon. There are two main methods to pattern the metal catalyst before it is used in the MACE process. The first method consists of transferring a resist pattern into a thin noble metal film such as Ag, Au, and Pt (gold was used in this project) via etching or ion milling. Imprint lithography is used to define the resist pattern after the film is vacuum deposited on the Si wafer. Then, a descum process is used to remove the residual layer[54] and expose the underlying Au film for etching. The gold film can be etched by either an iodine based solution (Gold Etchant TFA)[55] or an argon (Ar) and chlorine (Cl) plasma[56,57]. Finally, the resist is stripped and the sample is submerged in a solution of DI water, hydrogen peroxide (H_2O_2), and hydrogen fluoride (HF) at room temperature for MACE.

The second method to pattern the metal catalyst is a bilayer lift-off based process. Figure 1-9 shows an example of a bilayer lift-off process. A silicon wafer is first coated with polyvinyl alcohol (PVA). A resist pattern with holes is imprinted on top of the PVA and then the wafer is planarized with a proprietary silicon containing resist called Silspin™ manufactured by Molecular Imprints. The Silspin™ is etched back in a dry etch process following which an O_2 is used to preferentially etch the organic material (imprint resist and PVA) and oxidize the Silspin™ into SiO_2 which does not get removed. The O_2 plasma also etches the organic material isotropically so as to create a bowed sidewall profile. Metal is then deposited using e-beam evaporation, but does not become a continuous film because of the bowed sidewall profile. Finally, the PVA is dissolved in water leaving behind the patterned metal with the same tone as the imprint.

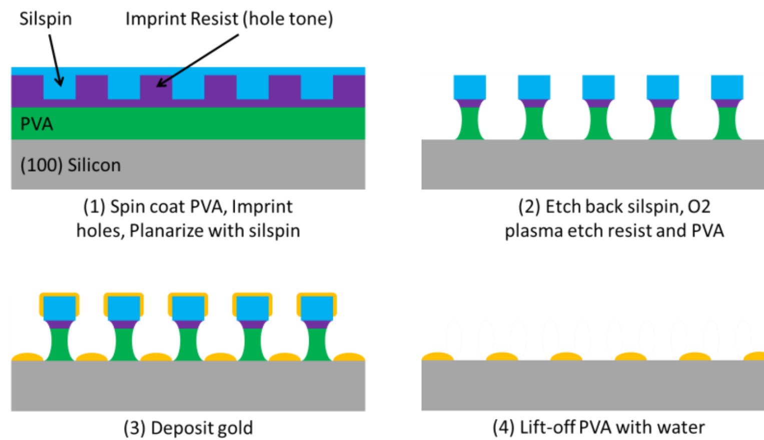


Figure 1-9: Example process flow for imprint bilayer lift-off process.

1.5 Research and Structure of the Dissertation

This dissertation is organized such that the second and third chapters detail the two processes used in this study. Chapter 2 details the advantages and limitations of iCODE and Chapter 3 details the advantages and limitations of iMACE. Chapter 4 discusses patterning of gold for the iMACE process and the exemplar application enabled by iMACE: Increase the energy storage density of ultra-capacitors by increasing the surface area per unit projected area of the electrodes with silicon pillars fabricated using iMACE. Finally, Chapter 5 summarizes the intellectual merit and future work.

Chapter 2: Imprint-enabled Crystallographic Orientation Dependent Etching (iCODE)

Imprint-enabled Crystallographic Orientation Dependent Etching (iCODE) is a process where J-FIL™ is leveraged to pattern sub-50nm hard mask features for the CODE process, which is an anisotropic etch technique where monocrystalline silicon is etched at different rates based on the exposed surface's crystal orientation (see Section 1.3.1.2). This process has been explored to enable inexpensive etching of high aspect ratio nanowires in Si.

2.1 Preliminary Experiments

Preliminary experiments were performed to explore the geometric constraints of the iCODE process by using different initial template patterns. All iCODE experiments were performed on (110) Si wafers because this orientation of Si wafers has four vertical (111) etch stop planes, as discussed previously in Section 1.3.1.2, that can be used to fabricate high aspect ratio features. Table 2-1 summarizes the purpose and results of the preliminary experiments. These have been detailed further in the following sections.

Table 2-1: Purpose and results of etching of the preliminary experiment mask geometries.

Mask Geometries	Purpose	Result
Dots (250 nm diameter circles in radial pattern)	Test whether the vertical etch stop planes would automatically create rhombus shaped pillars without need for alignment to the vertical (111) planes	Undercutting leads to the hard mask detaching, hillock formation , and finally feature loss
Gratings (500 nm Lines and 150 nm Spaces)	Test optical/manual alignment and achievable anisotropy	Optical/manual alignment is precise enough for the CDs used in the preliminary and proof of concept experiments
Rhombuses (Intersection of rotated gratings)	Same test as the dots but with sides that are aligned to the vertical (111) planes	Undercutting leads to the hard mask detaching, hillock formation , and finally feature loss

2.1.1 Dots (convex hard mask)

As a preliminary experiment to test whether the vertical etch stop planes would automatically create rhombus shaped pillars, dots were used as the pattern geometry of choice. Figure 2-1 is an SEM image of the dot pattern after it was transferred into the Si_3N_4 hard mask. The features are ~250 nm wide and ~120 nm high dots in a radial pattern with a pitch of 380 nm to 1.8 µm. Subsequent 5 sec anisotropic wet etching led to the hard mask being undercut, as shown in Figure 2-2, and eventually resulting in the

hard mask being completely removed. Short pyramids, shown in Figure 2-3, were revealed just after the hard mask detached from the Si after a 10 sec etch. The experiment showed that the anisotropic etch does not automatically stop at the vertical (111) planes which will be discussed in Section 2.2.2.

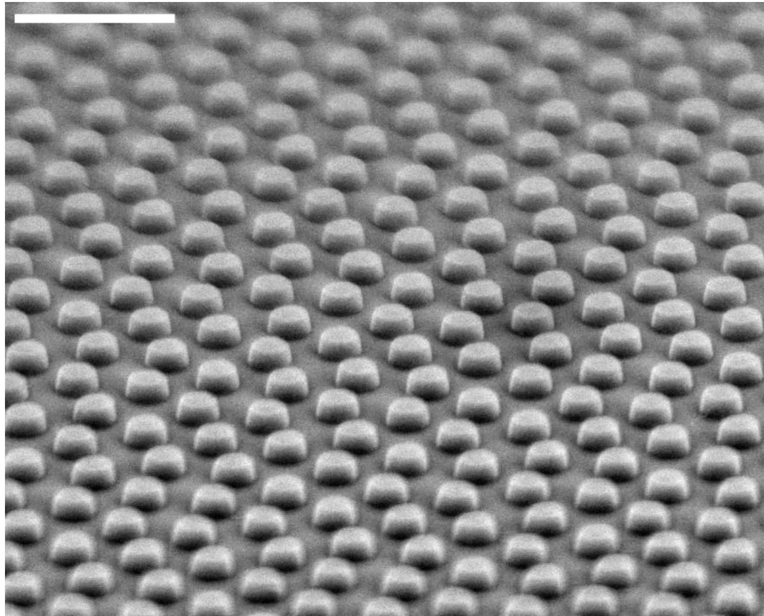


Figure 2-1: Radial pattern of ~230 nm dots in Si_3N_4 hard mask on Si. Scale bar is 1 μm.

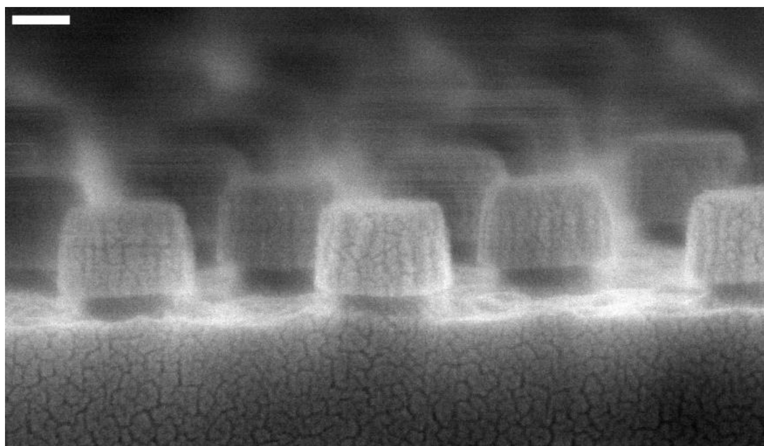


Figure 2-2: SEM image showing the undercutting of the hard mask. Scale bar is 100 nm.

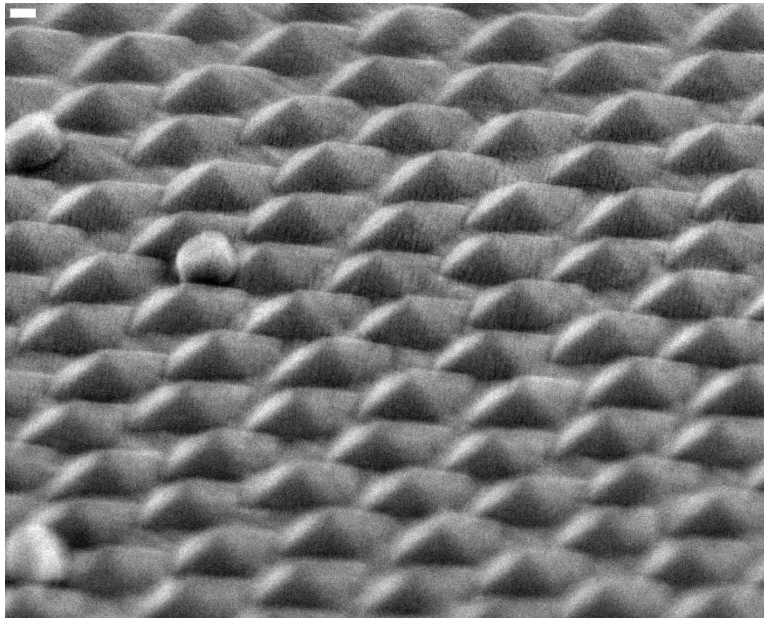


Figure 2-3: Pyramid features (hillocks) remaining just after the hard mask detached. Scale bar is 100 nm.

2.1.2 Lines

The iCODE process was used on a lines and spaces pattern to test the anisotropy of the process, test the precision of an optical/manual alignment scheme, and observe how misalignment to the vertical (111) planes affects the final feature dimensions. An optical/manual alignment procedure was used because the available imprint tool does not have the equipment necessary for automatic theta alignment. The alignment is done iteratively using the following steps:

1) The wafer is loaded onto the wafer chuck and the chuck is moved under the imprint template,
2) The angle between the sides of the die on the template and the wafer flat is observed using a camera mounted above the transparent template,
3) The chuck is moved back to the load/unload position and the wafer is unloaded,
4) The wafer is rotated by hand,

5) Steps 1) - 4) are repeated until the best visual alignment is reached.

Figure 2-4 shows a SEM image of gratings that were etched using a hard mask with the features well aligned to the vertical (111) etch stop planes. A misalignment of less than 0.5° was measured between the imprint and a cleaved side using an optical microscope. With increasing misalignment, greater undercutting of the mask occurs, as can be seen in Figure 2-5. Here, the initial alignment of the gratings was worse than the previous set of gratings as can be seen by the ~37 nm mask undercutting for a similar etch time.

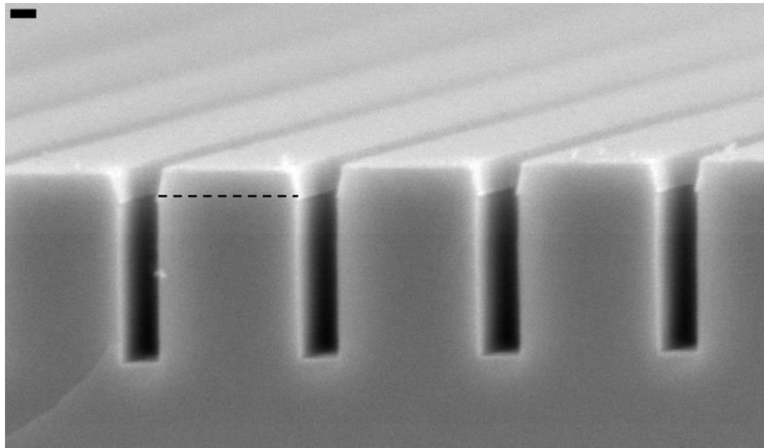


Figure 2-4: Well aligned gratings with minimal undercutting. Interface between Si and SiO_2 marked with a dashed line. Scale bar is 100 nm.

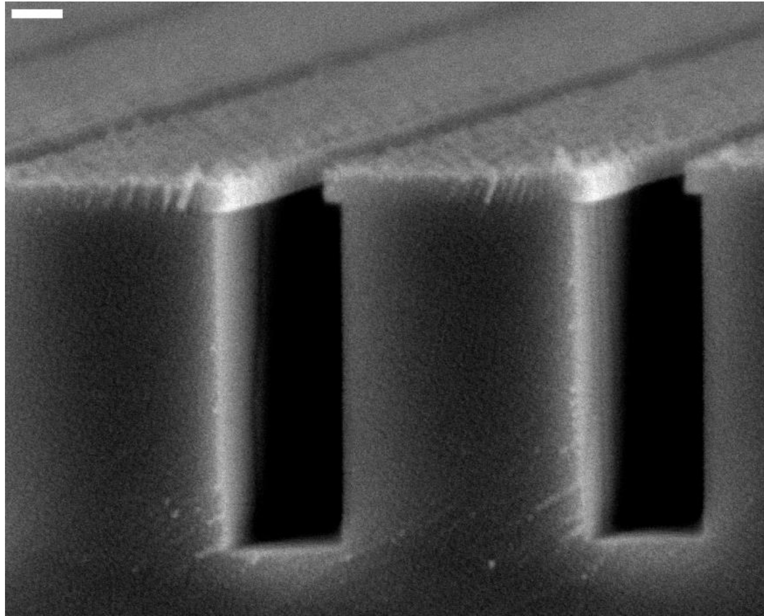


Figure 2-5: Etched gratings with slight misalignment showing more undercutting of the hard mask. Scale bar is 100 nm.

The anisotropy of iCODE was also tested by observing the changes in dimension after increasing the etch time. Figure 2-6 is a SEM image of the same gratings that were shown previously in Figure 2-5 but were etched for 15 min instead of 90 sec. The sidewalls are no longer vertical as can be seen by the change in trench width from ~313 nm at the top to ~252 nm at the bottom. The taper is most likely due to the different compositions of the etch solution along the gratings vertical direction. This difference in composition is hypothesized to be because of restricted transport of the reactants and products to the bottom of the trenches. The hard mask is also undercut by ~70 nm and the etch depth is ~6.5 µm. This equals an anisotropy of ~93 which is not as high as has been reported in literature[5,35-37]. The anisotropy can be affected by many factors such as solution composition, flow of etch solution, geometry of features, and alignment to the (111) planes. These parameters will also influence the uniformity of the etch process as well as surface roughness[58,59]. These parameters were not optimized since these

experiments were preliminary and were done to observe the parasitics in the iCODE process.

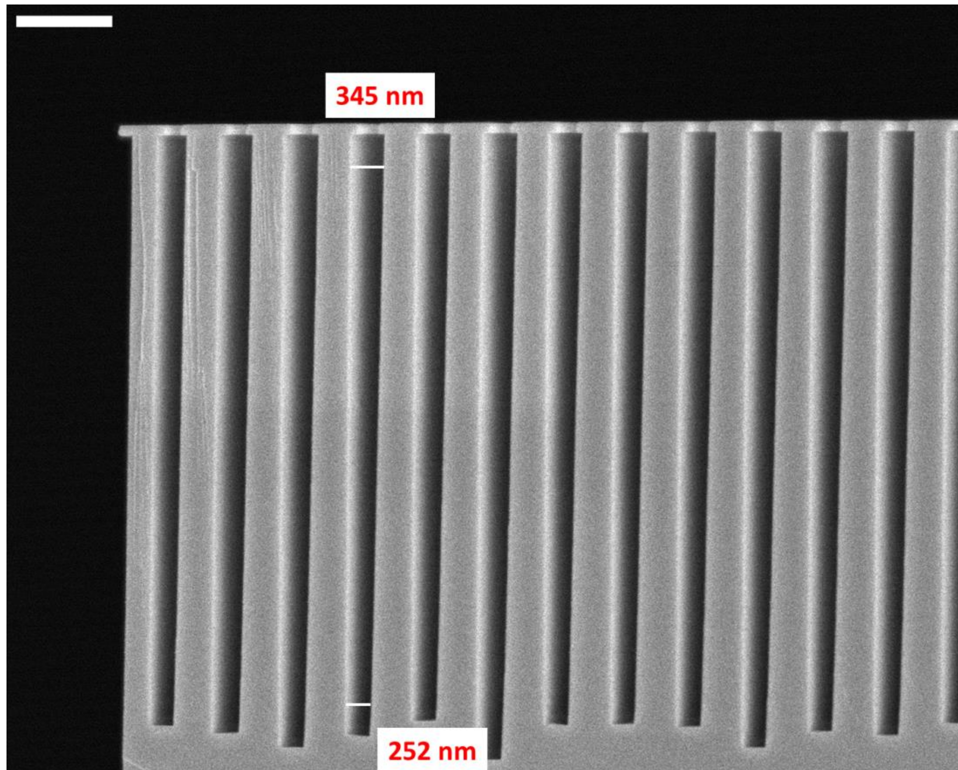


Figure 2-6: High aspect ratio trenches. Scale bar is 1 µm.

2.1.3 Rhombus with Sides Aligned to vertical (111) planes

The results from attempting to create pillars from a dot pattern show that severe undercutting occurs, leading to the removal of the hard mask. A second set of experiments were performed to observe the results of changing the pattern to have a convex geometry where the sides are aligned to the vertical (111) planes. These planes form a rhombus with angles of 109.47° and 70.53°. Since such a geometry was not readily available on a template, the patterning was done in a two-step process, with each step involving the patterning of a lines and spaces template as given in Section 2.1.2. Figure 2-7 is a simplified process flow of the process for patterning the hard mask in the

form of rhombus. First, a SiO_2 hard mask was patterned with a grating pattern of 150nm lines and 500nm spaces that was aligned to one family of vertical (111) planes using the optical/manual method of alignment discussed in Section 2.1.2. The alignment was done with optical/manual alignment procedure. Then, a descum etch (O_2 and Ar) was used to remove the residual layer and then a SiO_2 dry etch (Ar, CHF_3, and CF_4) was used to transfer the pattern into the hard mask. The hard mask was patterned again but with the gratings aligned to the second family of vertical (111) planes.

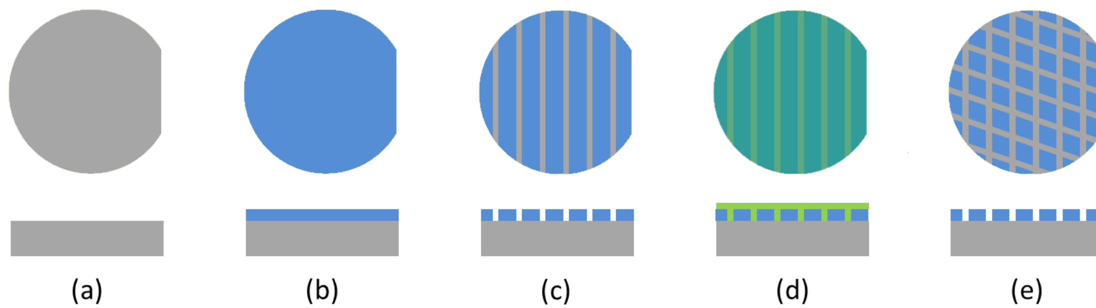


Figure 2-7: Process flow for rhombus shape mask double patterning. (a) (110) Si wafer (b) SiO2 hard mask growth (c) Gratings patterned and etched into hard mask (d) Planarization with polymer (e) Gratings rotated by 109.47° patterned and etched into hard mask.

The wafer was etched in a KOH solution after the SiO_2 hard mask was fully patterned. Figure 2-8 shows the resultant mask after double patterning gratings aligned to both the families of (111) planes. Figure 2-9, Figure 2-10, and Figure 2-11 show that there was severe undercutting of the corner of the rhombuses after 20sec KOH etch instead of etching vertically, which eventually lead to lift-off of the hard mask just like the experiments with the dots. The crossing of (111) planes did not help with creating pillars with slow etching sides as expected. The reasons for this will be discussed in Section 2.2.2. The dashed lines in Figure 2-11 show the vertical (111) planes where the mask sides ended and the etch process was expected to stop.

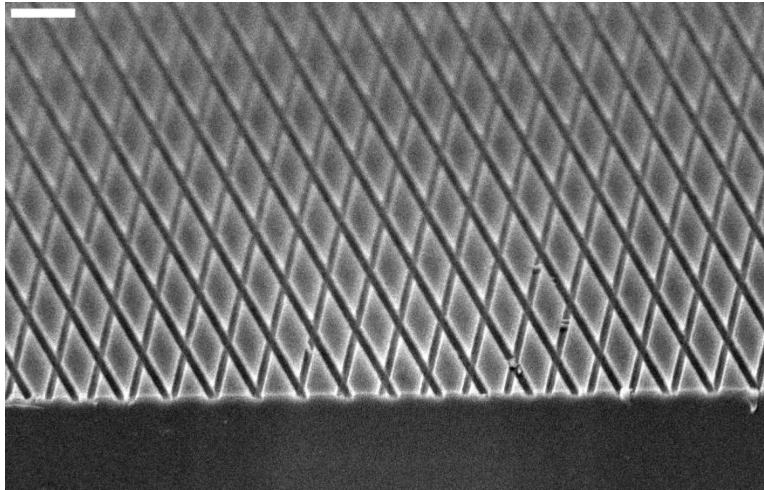


Figure 2-8: Top-down SEM image of the double patterned hard mask. Scale bar is 1 μm.

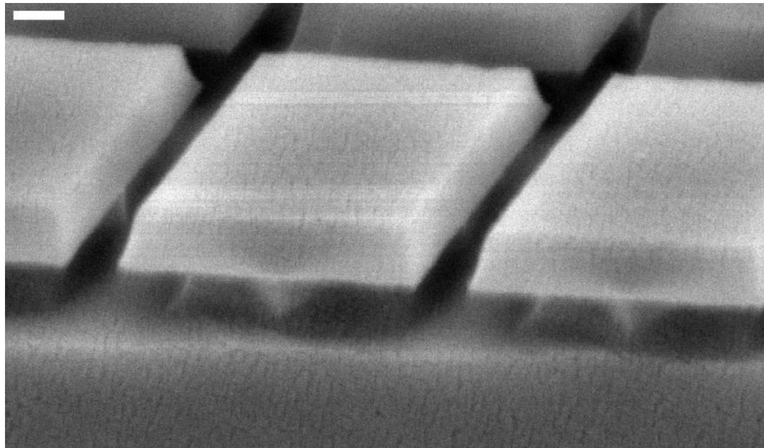


Figure 2-9: Visible undercutting of mask after 20 sec KOH etch. Scale bar is 100 nm.

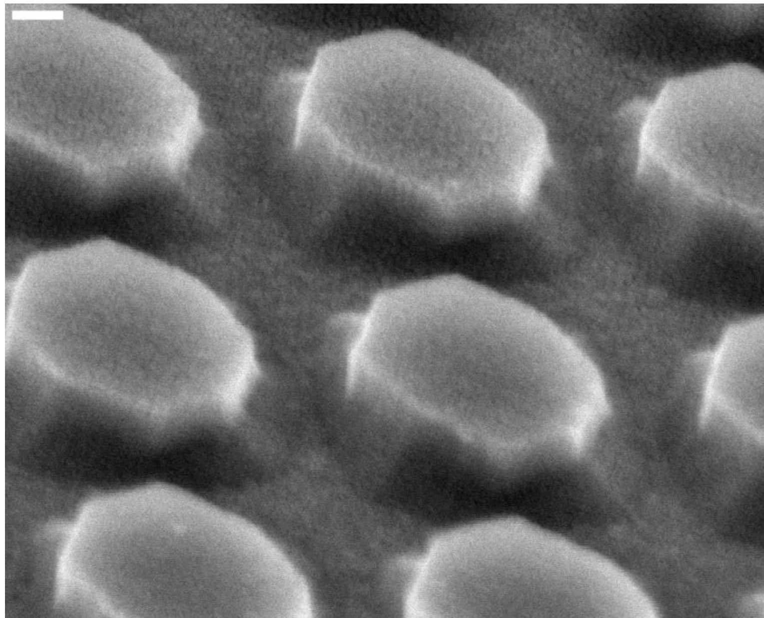


Figure 2-10: Undercutting of mask after 20 sec KOH etch with hard mask removed. Scale bar is 100 nm.

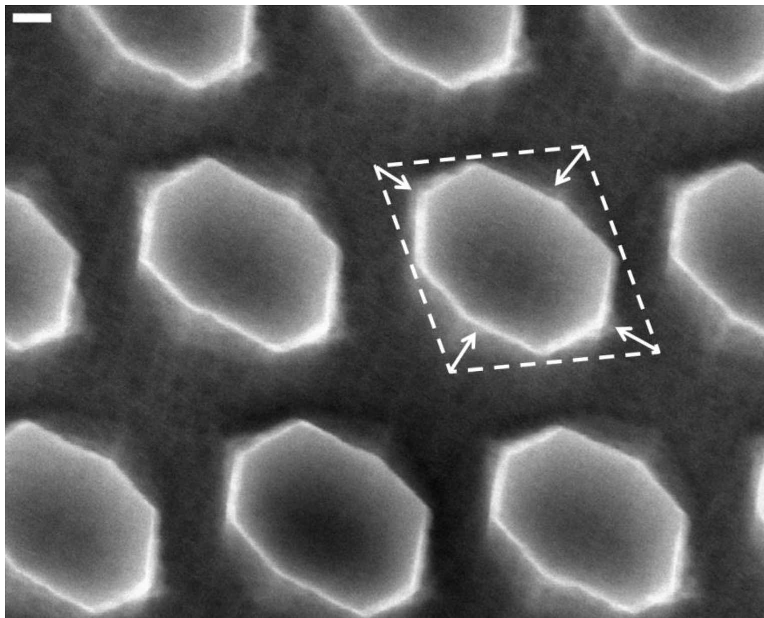


Figure 2-11: Top-down view of undercutting from KOH etching with the hard mask removed. The dashed lines are the (111) planes where the etch process was thought to stop. The four arrows show how the corners etch. Scale bar is 100 nm.

2.2 Problem Fundamentals

As described in the previous section, the preliminary experiments show that there are several constraints on the CODE process that limits the ability to etch arbitrary feature geometries. These constraints include undercutting of the mask that occurs at the corners during KOH etching even when the sidewalls are aligned to the (111) etch stop planes, and the change in etch rate and undercutting due to misalignment with the (111) planes. A third etch depth constraint is exemplified with the experiments that were carried out to overcome the convex edge etching.

2.2.1 Alignment

Alignment of the feature sides with respect to the (111) planes determines the amount of undercutting of the mask that occurs and the initial lateral etch rate. The anisotropy of an etch is determined by the amount of undercutting or the ratio of the lateral etch amount and the etch depth. Misalignment of the mask with respect to the (111) planes leads to higher initial etch rates until the etching planes self-align to the (111) planes. Figure 2-12 shows how the lateral etch rate changes with respect to the angle between the masked features and the (111) planes. This phenomenon is explained with ledges where one face of the ledge is the (111) plane. The ledges etch along the (111) plane since the other face of the ledge will be a faster etching plane. The density of the ledges decreases as the orientation of the widening feature rotates to be more aligned to the (111) plane. In Figure 2-13, the left trench is perfectly aligned so there is almost no lateral etching compared to the depth. The middle trench is slightly misaligned so some of the (111) planes are cut revealing faster etch planes which start etching along the (111) plane. The right trench is misaligned by twice as much as the middle and there are twice as many ledges per length which means the etch rate is twice as high. Figure 2-14 shows

the change in feature dimension due to misalignment of gratings from the vertical (111) planes.[60]

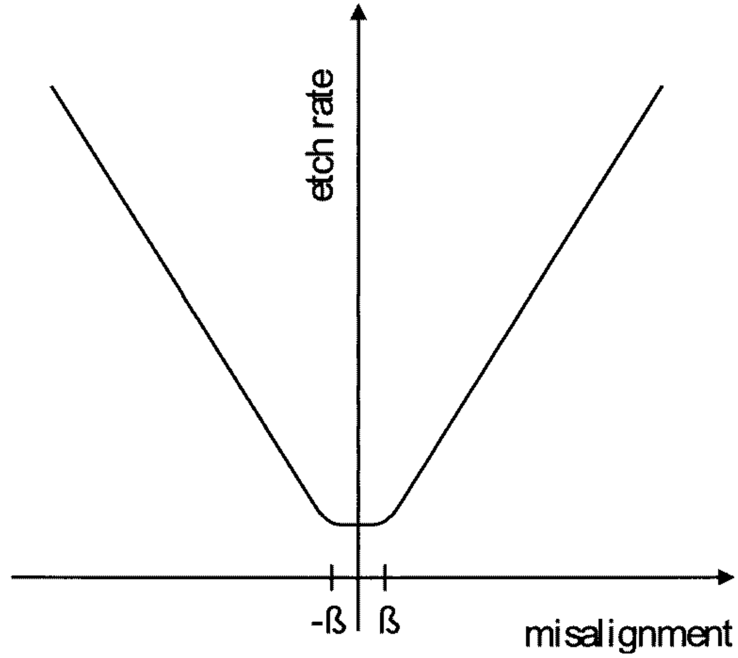


Figure 2-12: Lateral etch rate versus misalignment.[37]

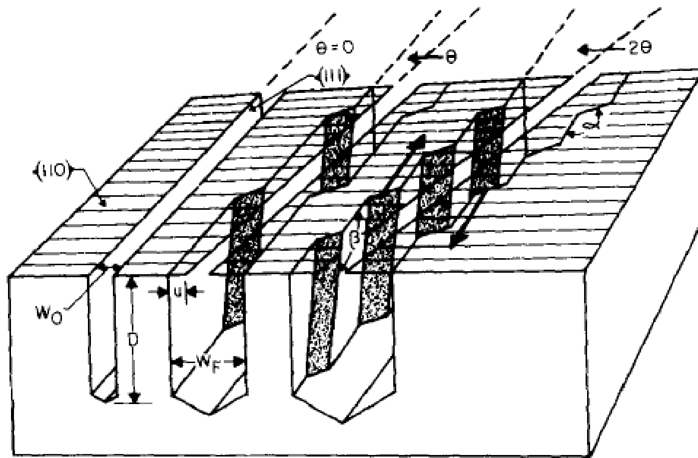


Figure 2-13: Misalignment of trenches etched in (110) silicon showing ledges, final width, and etch direction.[60]

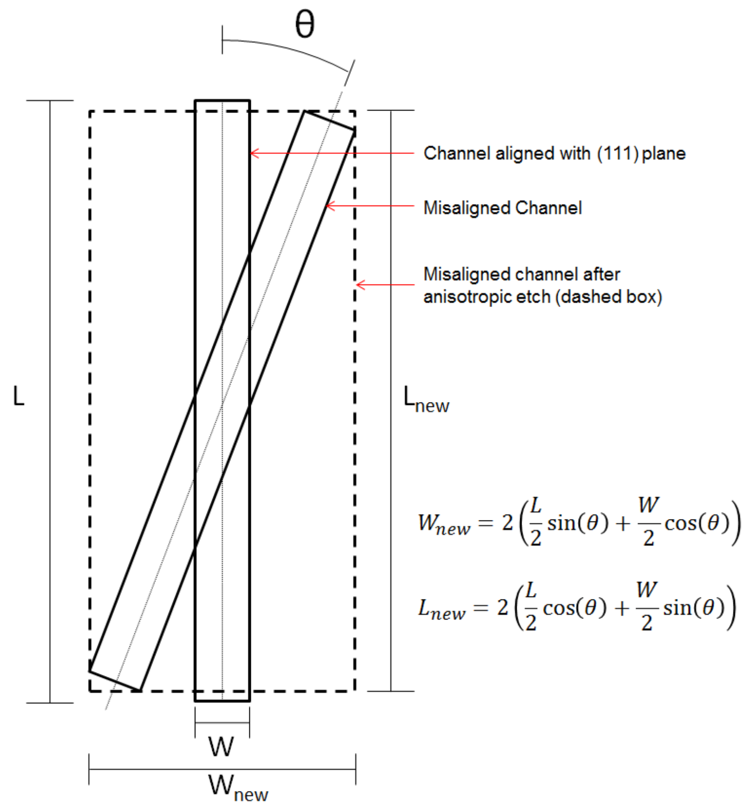


Figure 2-14: Change in trench dimensions due to misalignment.

There are two main components to reducing misalignment. First, the amount of misalignment between the (111) planes and the template features needs to be measured. Nominally, the major flat of (110) silicon wafers are aligned to the (111) planes but the flat can have an alignment error of 0.5° to 5° depending on the grade of the wafer. This amount of error is unacceptable for applications on the nanoscale so other methods are needed to precisely determine the (111) plane orientation[36,37,61]. Second, the lithography tool needs to have a theta stage to be able to rotate the wafer and align the template features to the (111) plane. While the actuation of the wafer can be done with commercial theta stages, the main difficulty lies in accurately determining the true (111) planes. Commercial theta stages can be found with theta resolutions as high as 0.00004 degrees

which is well beyond the current sensing resolution which can be as high as 0.01 degrees[61]§.

2.2.2 Convex Corner Undercutting – Edge Parasitics

The preliminary experiments done in Section 2.1.3 show that convex edges etch away even when their sides are aligned to (111) etch stop planes. This has to do with the structure of the Si atoms at the convex and concave edges created by the intersection of two (111) planes. Figure 2-15 shows the structure of the 70.53° convex edge at AA' and the 109.47° convex edge at BB'. The edge atoms along AA' each have two dangling bonds and two back bonds like the (100) plane so they etch faster than the (111) plane and lateral etch occurs which undercuts any mask. The two sets of atoms beside BB' each have one dangling bond but they are closer together than the (111) which means there is a higher density of dangling bonds similar to the (110) plane. On the other hand the atoms of the concave edges, shown in Figure 2-16, have zero dangling bonds so are very stable compared to any plane.[39] The stability of concave edges versus the instability of convex edges is summed up by Batterman when he stated, "On a concave surface, the plane at a relative minimum in etch rate versus orientation will limit, while on a convex surface the converse will hold."[62]

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§ https://www.newport.com/Motorized-Rotation-Stage-Selection-Guide/140222/1033/content.aspx viewed on June 15, 2015

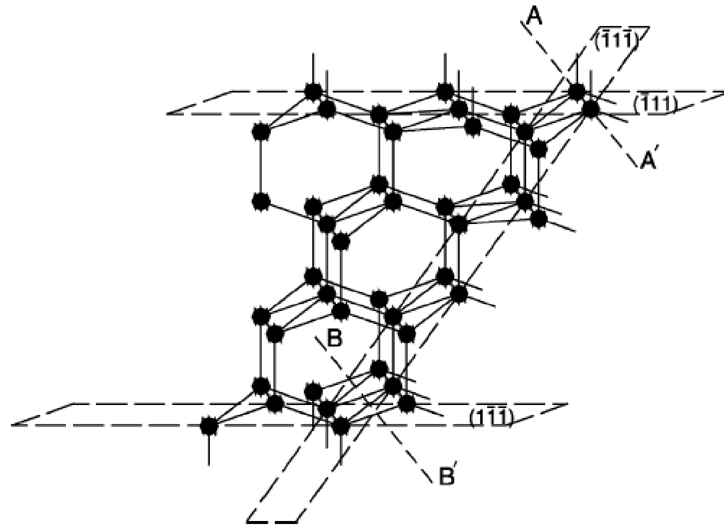


Figure 2-15: Convex edges created by (111) planes.[39]

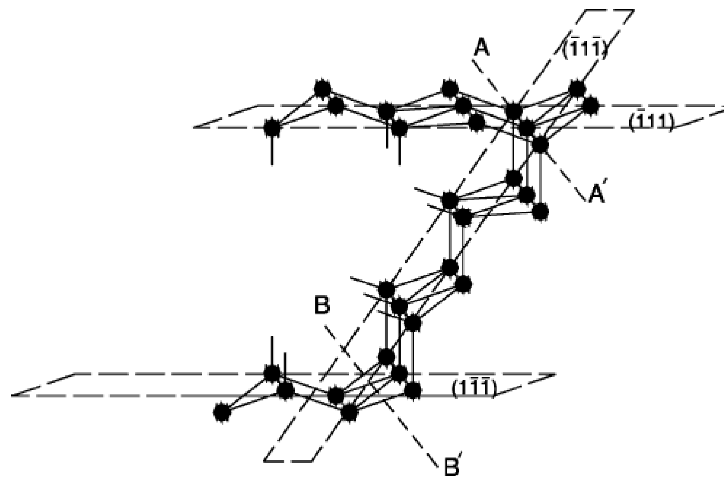


Figure 2-16: Concave edges created by (111) planes.[39]

2.2.2.1 Corner Compensation to Overcome Undercutting

The main method developed to mitigate the undercutting due to mask geometries with convex corners is called corner compensation[63-65]. This method uses knowledge of the etch rates of different planes to design mask geometries with extra protrusions on the convex corners that result in the desired shape after a timed anisotropic etch for a given

depth. Figure 2-17 shows an example of a corner compensation feature and Figure 2-18 shows SEM images of the feature at different etch times. The compensation feature shrinks as the initial pattern is anisotropically etched since the convex corners are equivalent to fast etch planes.

The two drawbacks of this method are: (i) the etch process has to be timed, and (ii) the size of the compensation feature is dependent on the desired depth. The process window can be as small as a few seconds depending on the sharpness requirements needed for the edge since overetching leads to flattening of the corner and underetching results with part of the compensation feature remaining on the edge. The etch time is determined by the etch rate and the desired depth which dictates how large the feature needs to be. A large compensation feature means that the spacing between desired features has to be large as well, thus reducing feature density. Many different potential geometries have been developed to mitigate these drawbacks as shown in Figure 2-19.

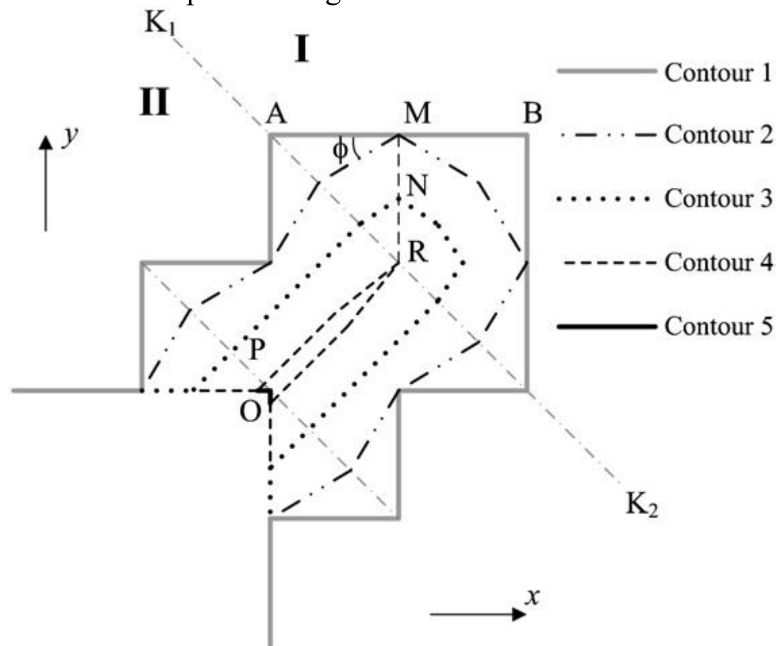


Figure 2-17: Example of a corner compensation feature as it is anisotropically etched. Original pattern (Contour 1) to final desired convex corner (Contour 5).[63]

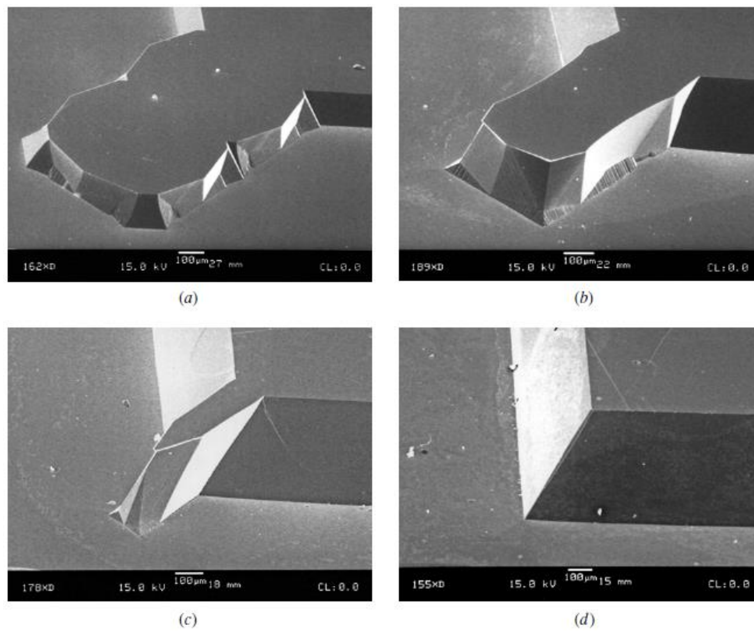


Figure 2-18: SEM images of the corner compensation feature shown in Figure 2-16 at different etch times.[63]

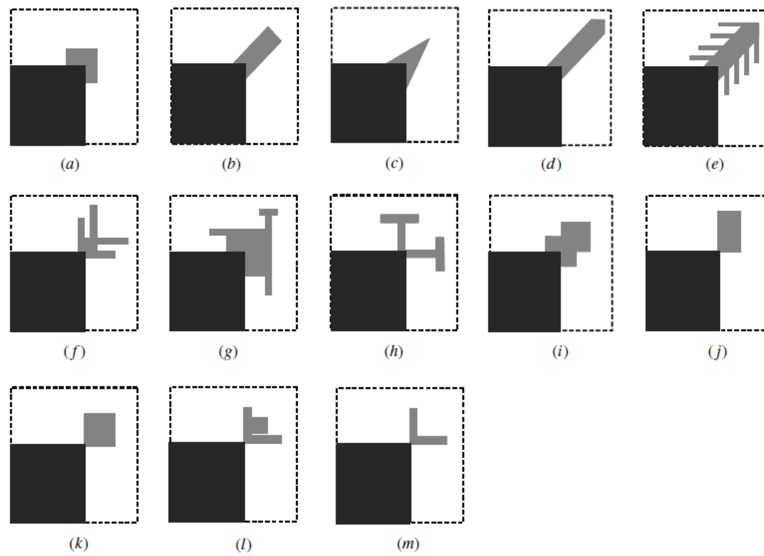


Figure 2-19: Examples of convex corner compensation designs.[64]

2.2.2.2 Edge Protection to Overcome Undercutting

Instead of relying on a timed etch to fabricate sharp convex edges, an alternative technique relies on the edge being protected with a hard mask to create an etch stop. After the SiO_2 hard mask is patterned with the first set of gratings aligned to the vertical-(111) planes, the silicon is KOH etched to the desired depth of the pillars. The Si was etched only 650nm for the preliminary experiments. A thin SiO_2 is grown on the sides of the etched trench to provide protection during the second etch. The wafer is planarized with a polymer so the second set of gratings can be patterned along the second family of vertical (111) planes. The etch process is repeated to create the other sides of the pillars. The new process flow is shown in Figure 2-20 and Figure 2-21.

Imprint 1, Dry Etch 1, Wet Etch 1 Imprint 2, Dry Etch 2, Wet Etch 2

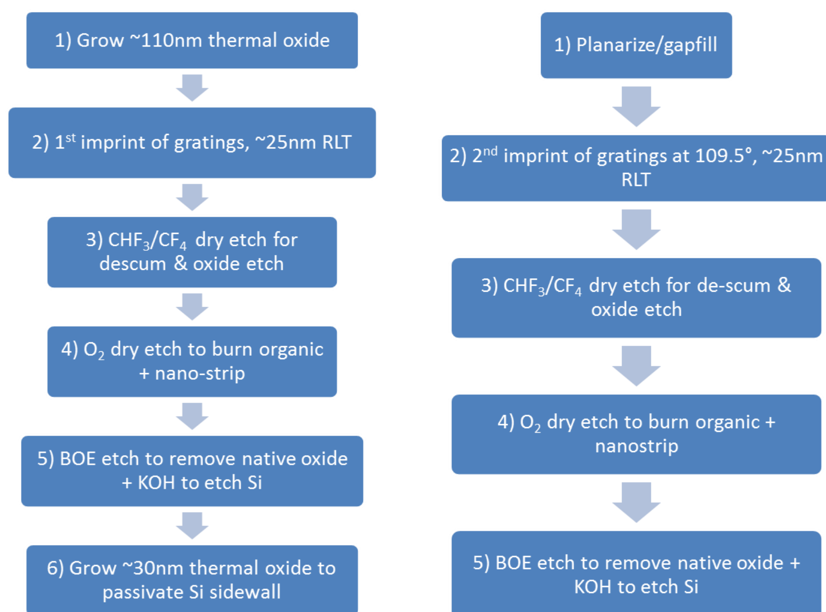


Figure 2-20: Process flow for edge protection using two sequential sets of imprint, dry etch, and KOH wet etch steps.

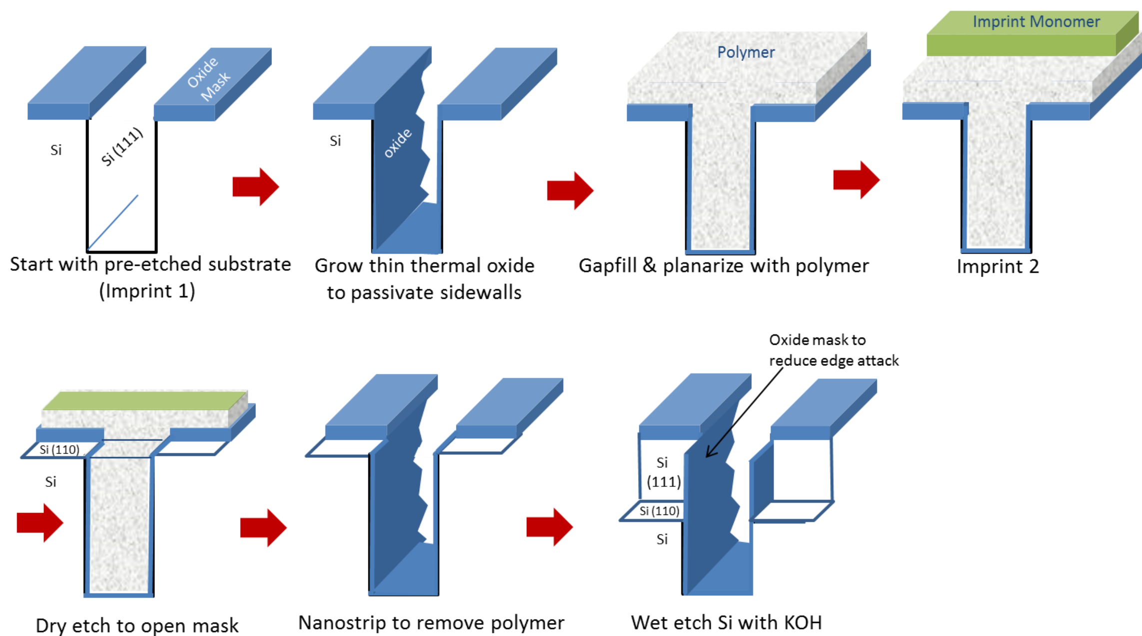


Figure 2-21: Graphic depicting the new process flow starting after the initial set of gratings were etched into silicon.

Figure 2-22, Figure 2-23, and Figure 2-24 are taken at the end of the edge protection process flow. Figure 2-22 shows the features after the second set of gratings have been etched with iCODE but before the SiO_2 hard mask and sidewalls have been removed. The SiO_2 sidewall was able to keep the vertical edges from being etched away but also kept the second etch from progressing below the point where the sidewall protected the non-vertical (111) plane. As mentioned in Section 1.3.1.2, the non-vertical (111) plane is at an angle of 54.7° from the vertical (111) plane. The SiO_2 sidewalls divided the second set of gratings into many pits. The problem with etching pits is described in the Section 2.2.3. The etch was deeper than it would have been if the top of the SiO_2 sidewall had not been slightly etched during the pattern transfer into the hard mask. This masked the non-vertical (111) planes starting ~50nm below the surface and

exposed the top of the Si pattern. Figure 2-23 and Figure 2-24 show the features with the oxide removed.

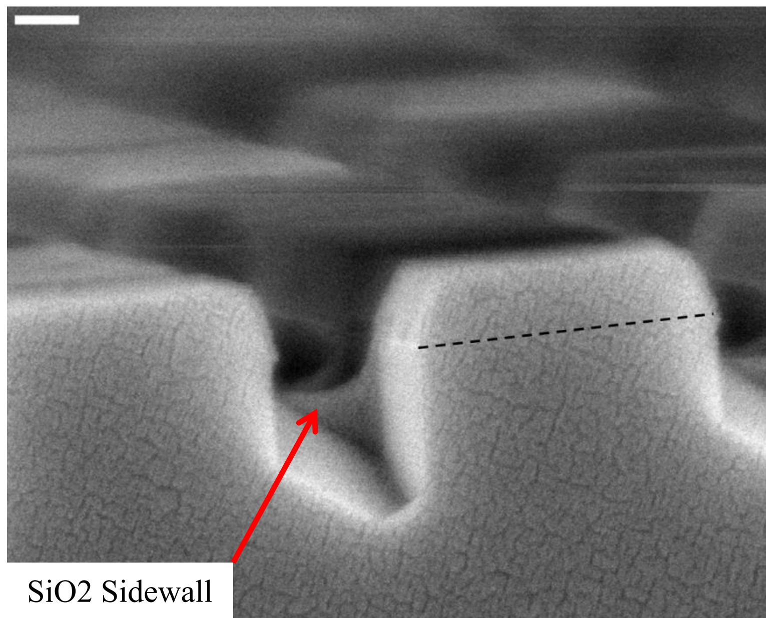


Figure 2-22: SEM image of the features after the second set of gratings are etched but before the SiO2 hard mask and side wall have been removed. Interface between Si and SiO_2 marked with a dashed line. Scale bar is 100 nm.

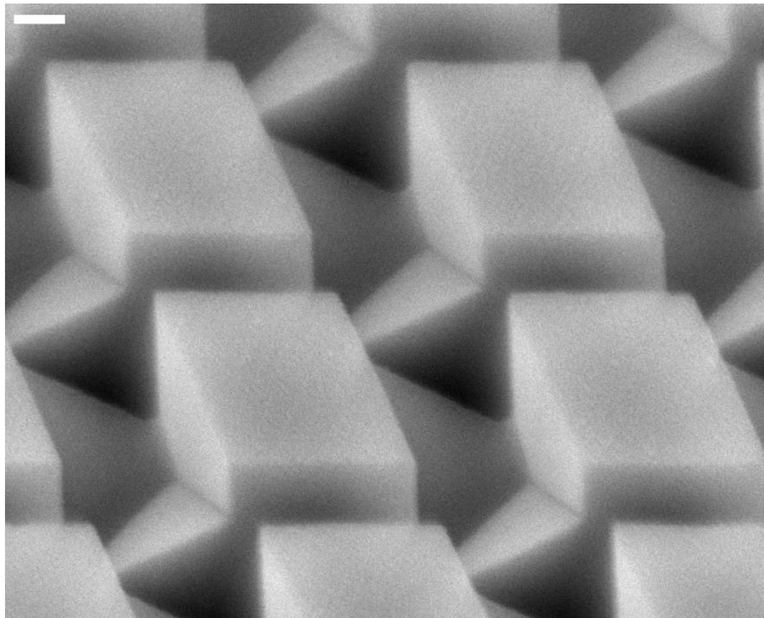


Figure 2-23: Features created by KOH etching using two imprint and two etch steps after a buffered oxide etch (BOE) to remove oxides. Scale bar is 100 nm.

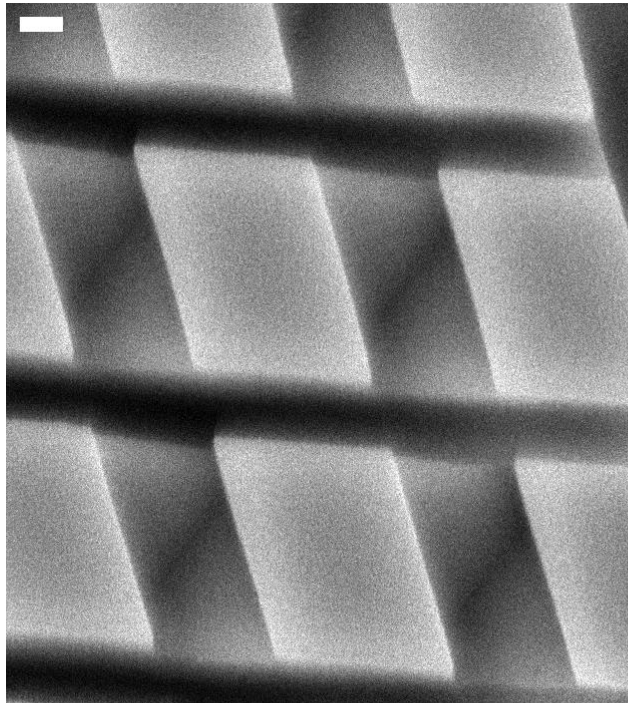


Figure 2-24: Features created by KOH etching using two imprint and two etch steps after a buffered oxide etch (BOE) to remove oxides. Scale bar is 100 nm.

2.2.3 Non-vertical Etch Stop Planes

The second etch step in the previous section highlighted the etch depth constraint imposed by the non-vertical (111) planes. Concave features etched into Si wafers with CODE tend to become certain concave shapes bounded by (111) slow etching planes depending on the surface orientation. A pit etched into a (100) silicon wafer, will tend to become an inverted pyramid or v-groove with sides aligned to <110> direction. The (111) surfaces are at 54.74° angle with the (100) surface. Figure 2-25 shows an example of anisotropic etch of a concave feature into a (100) wafer.

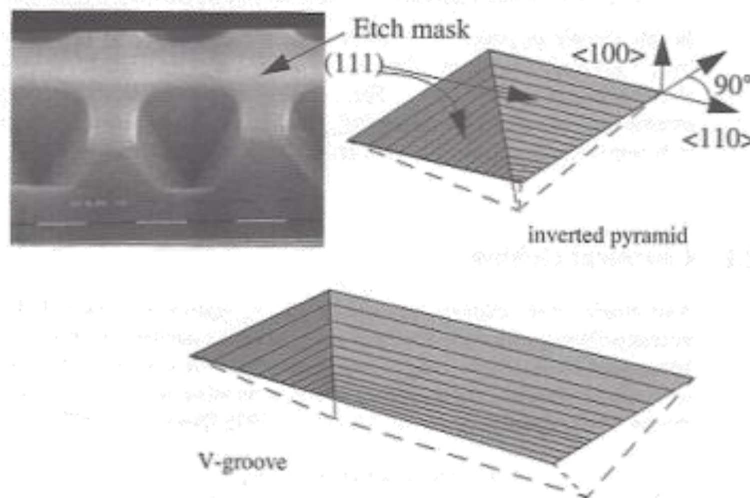


Figure 2-25: A SEM photo and schematic of the final shape of etched pits in (100)-silicon.[23]

Etching into (110) silicon wafers will produce hexagons with two of the opposing sides sloping downwards since four of the (111) planes intersect the (110) surface at a right angle and two with a 35.26° angle. The vertical planes intersect each other at a 109.47° angle. Figure 2-26 shows the shape of a feature etched with CODE in a (110) wafer. This project will focus on (110) silicon wafers because the vertical (111) planes can be used to create features with smooth, vertical sidewalls whereas (100) wafers will always have sloped walls that converge and prevent deep etching.

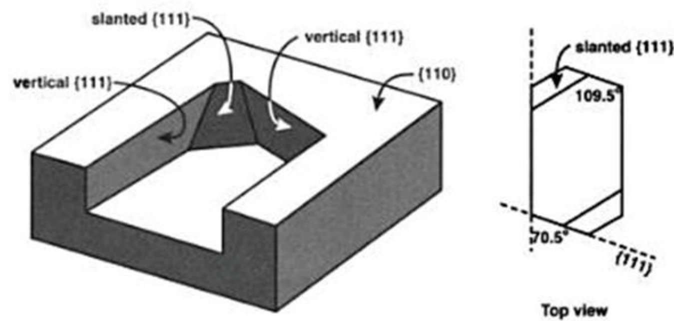


Figure 2-26: Etched features are defined by four vetical (111) planes and two sloped (111) planes shown. (Modified from [66])

Figure 2-27 shows the angle and distance relationships for a pit etched in a (110) wafer. D_{max} is the maximum etch depth which is limited by the intersection of the non-vertical (111) planes that are protected by the mask. Long trenches that are aligned to the vertical (111) planes can be deeply etched because the non-vertical (111) planes start far apart at the ends of the line on the surface of the wafer. Adding the SiO_2 sidewalls to protect the convex edge reduces the distance between the non-vertical (111) planes to the same length as the width of the trench. The max etch depth is approximately 144nm because the sidewalls are ~500 nm apart and the non-vertical (111) planes intersect the surface at a 35.26 degree angle. If the SiO_2 sidewall could be selectively removed, then the second etch would be similar to etching a second set of trenches and the potential depth would be the same as the first set of trenches. Figure 2-28 shows the change in etch depth due to the non-vertical (111) planes that were protected by the SiO_2 hard mask at the end of the trenches.

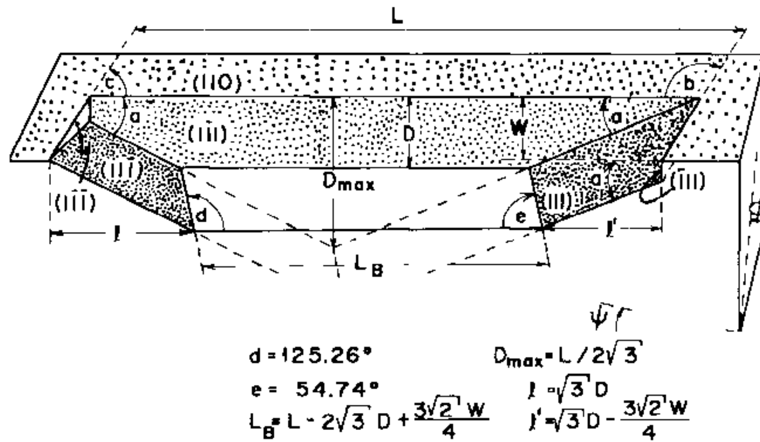


Figure 2-27: Graphic of the dependence of max etch depth on mask size.[67]

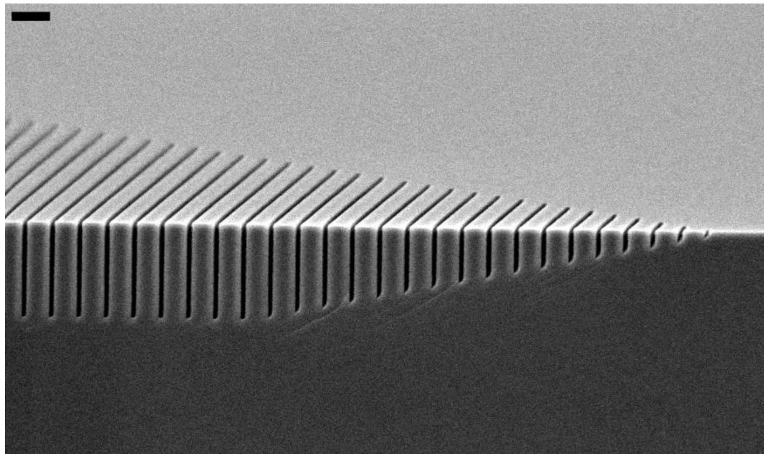


Figure 2-28: SEM image of etched trenches shows the non-vertical (111) planes restricting etch depth near their line ends. Scale bar is 1 μm.

2.2.3.1 Methods of Overcoming the Etch Depth Restriction for Concave Features

Several methods were attempted to overcome the restriction on etch depth for the second set of features by selectively removing the sidewall. The first method attempted to selectively remove the SiO_2 sidewall by using ultra-sonication during etching. The theory was that by the time the etch process reached the non-vertical (111) planes, the sidewall protecting the planes would be unsupported on both sides and weaker than the portion of the sidewall attached to the pillars. The ultra-sonication would make the thin,

unsupported sidewall collapse, allowing the etch to continue deeper, and the process would continue. The ultra-sonication however, ended up delaminating the entire sidewall resulting the second line etching away while the first gratings were deepened as shown in Figure 2-29 and Figure 2-30.

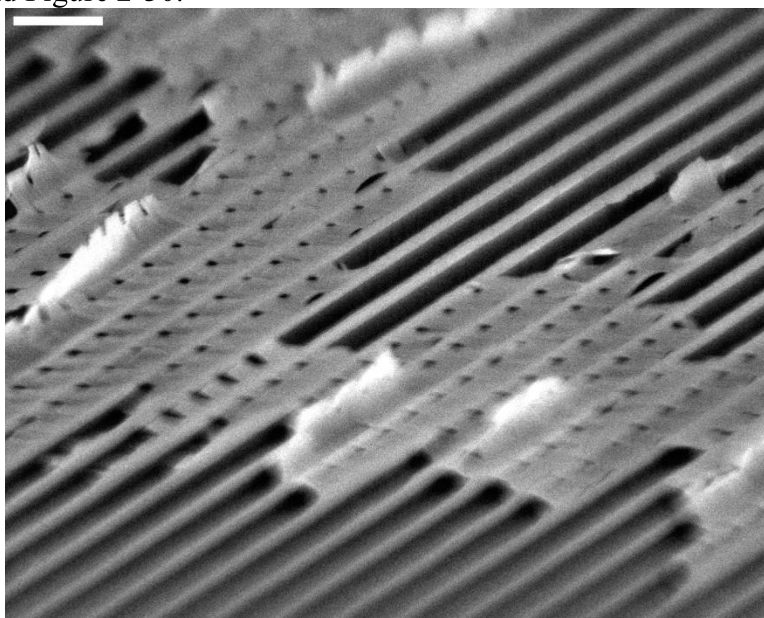


Figure 2-29: Collapsed SiO_2 sidewall after ultra-sonication. Scale bar is 1 μm.

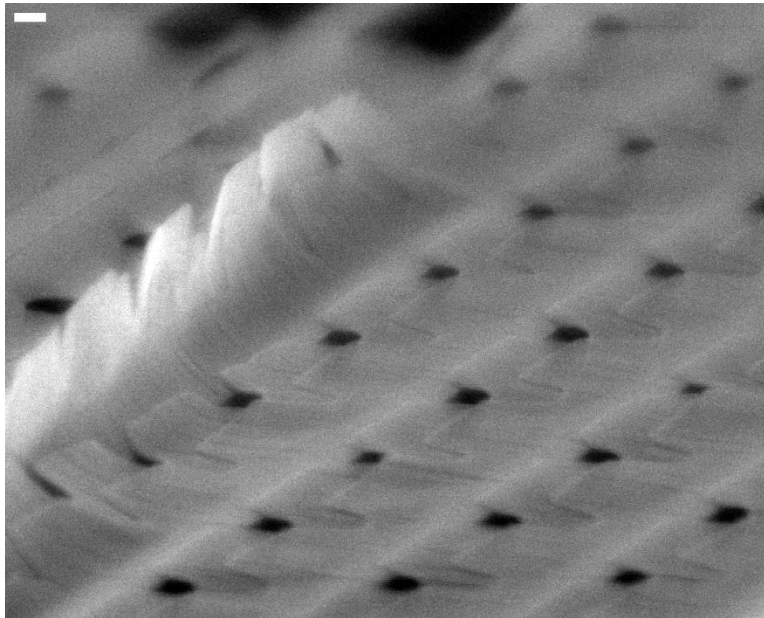


Figure 2-30: Collapsed SiO_2 sidewall after ultra-sonication. Scale bar is 100 nm.

The second method to increase the etch depth attempted to selectively dry etch the planarization layer along the second set of gratings so that the revealed sidewall could be removed with a buffered oxide etch (BOE). A silicon containing resist was used as a mask for the dry etch of the polymer planarization layer (Satoshi, T. 2010). The new process flow is shown in Figure 2-31. The method was unsuccessful because the dry etch created a passivation layer on the sidewall that kept the SiO_2 from being removed by the BOE and the silicon containing resist used as a mask delaminated easily. Figure 2-32 and Figure 2-33 are examples of the silicon containing resist delaminating from the first trenches. However, this process also required more dry etching, thereby substantially increasing the cost of the process. This method was, thus, not pursued further.

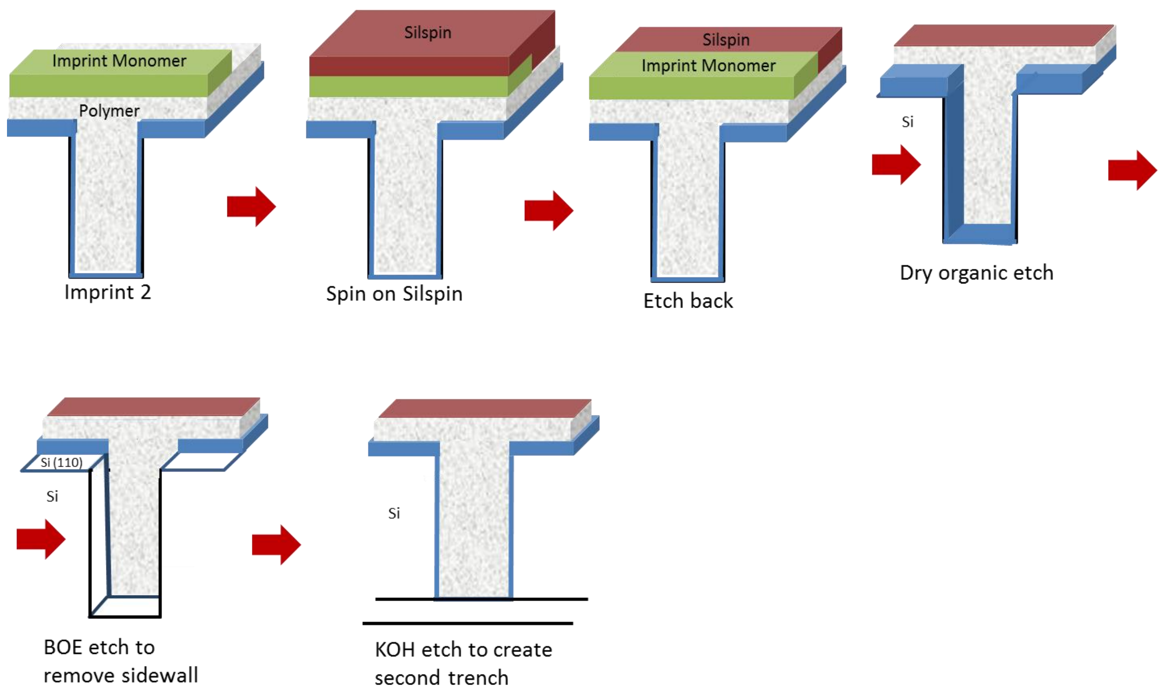


Figure 2-31: New process flow starting after planarization and imprint utilizing silicon containing resist to act as a mask for an organic etch to selectively remove the SiO_2 sidewall.

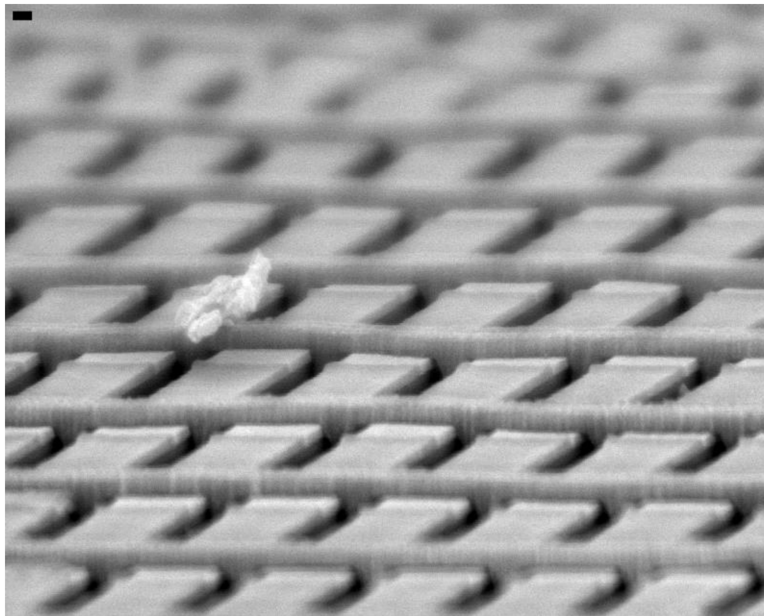


Figure 2-32: Delamination of silicon containing resist features. Scale bar is 100 nm.

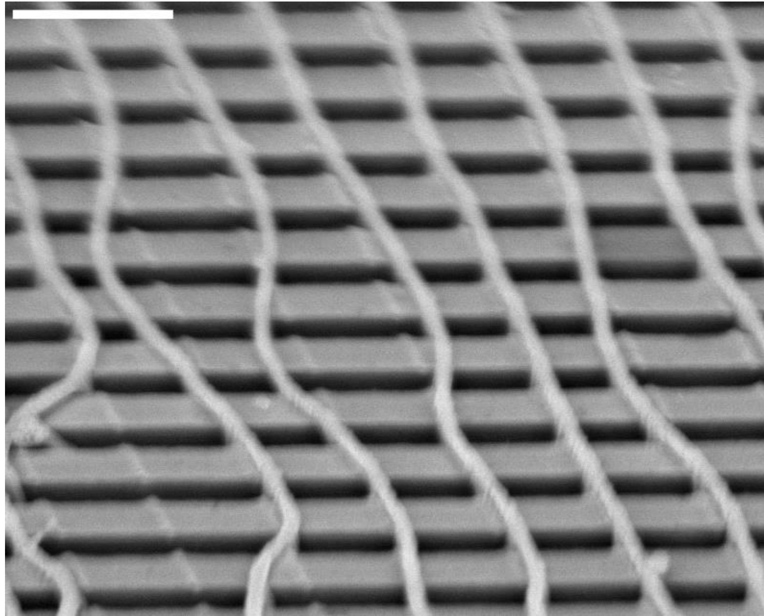


Figure 2-33: Delamination of silicon containing resist features. Scale bar is 1 μm.

A final attempted method was to utilize MACE to etch the second set of gratings and then use a brief KOH to clean up the sidewalls. Unfortunately, MACE preferentially etches along the [100] directions which are not vertical in (110) wafers. This phenomenon will be discussed in Section 3.2.

2.3 CONCLUSIONS

As discussed in this chapter, high aspect ratio trenches can be etched with KOH if the gratings can be aligned with a family of vertical (111) planes and the non-vertical (111) planes will also limit the maximum etch depth. Fabricating high aspect ratio pillars with sides aligned with intersecting vertical (111) planes requires additional considerations. One method is to add compensation features for timed etches but the added features takes up space and reduces maximum feature density. Another method is to protect the feature edges that act like fast etch planes but the protection needs additional steps and complexity to add before etch and afterwards. These added

complexity reduces the benefit of using CODE so the focus of this study moved entirely to the MACE process discussed in the next chapter.

Chapter 3: Imprint-enabled Metal Assisted Chemical Etching (iMACE)

Imprint-enabled Metal Assisted Chemical Etching (iMACE) is a process where J-FIL™ is leveraged to pattern sub-50 nm noble metal catalyst features for the MACE process. MACE is an anisotropic etch technique where a metal catalyzes the etch reaction at the silicon/metal interface. Thus, the silicon underneath the metal is preferentially etched.

3.1 Preliminary Experiments

Preliminary experiments with iMACE were done to etch lines into (110) Si wafers using silver as the catalyst material to complement the iCODE process for fabricating high aspect ratio pillars. There are two methods to perform iMACE using silver as the catalyst. The first method uses silver nitrate mixed in the etch solution[3,68,69]. The silver nucleates out of the solution at the Si/solution interface. Vacuum deposition of silver is the other method[3]. The deposition for both methods occurs after a masking material is patterned so the silver only comes in contact with silicon that is exposed. The presence of silver at the silicon surface initiates an etching reaction as given in Equation 1.4. Figure 3-1 shows the result of etching gratings with 150 nm trenches and 500 nm spaces using a silver iMACE process. Undercutting of the silicon nitride mask occurs because silver is soluble in the etching solution and nucleates on the sidewalls of the silicon trenches. This leads to lower anisotropy and can disrupt the critical dimension of nanoscale features or completely remove the features.

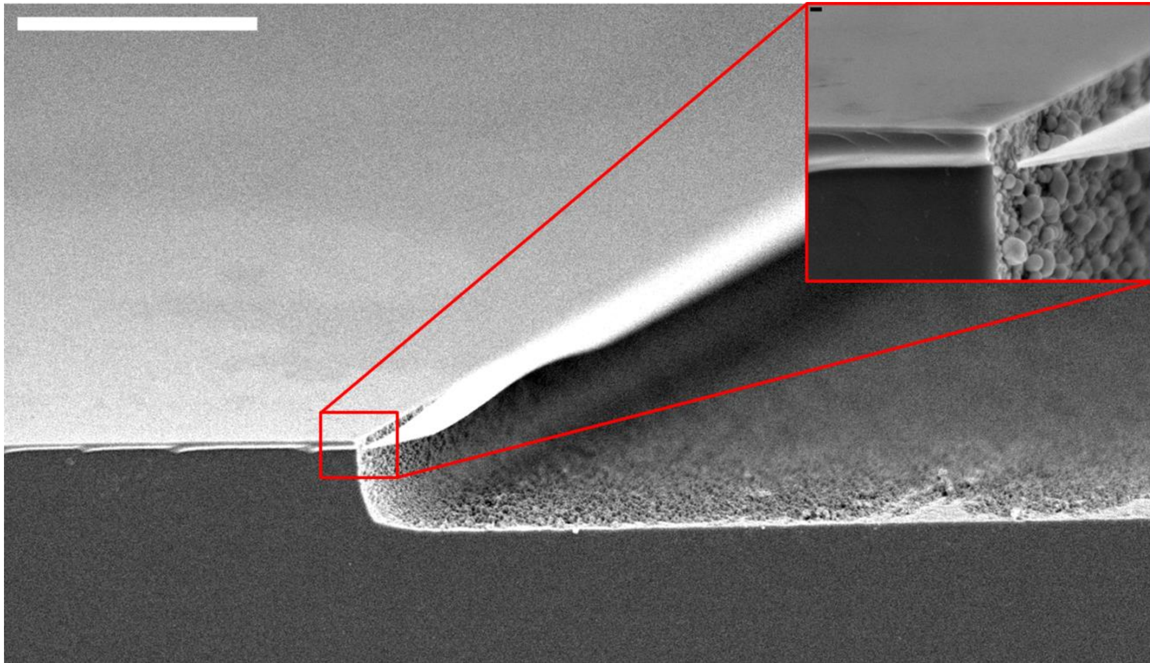


Figure 3-1: Attempt at etching gratings using a silver iMACE process. Silver nucleation present on the sidewalls shown in inset. Scale bar is 10 µm.

To circumvent this problem, the metal catalyst was changed to gold instead of silver because gold is not soluble in the etch solution. The gold was deposited on a patterned masking layer using a vacuum deposition process. Figure 3-2 shows the results of using gold instead of silver as the catalyst. Less undercutting of the same mask as the one used with silver, occurs with gold but two new phenomena are revealed. First, microporous silicon can be seen near the top sides of the etched trenches[2,3,70,71]. Secondly, a change in the etch direction as the etch progresses can also be observed. Both of these phenomena will be discussed in Section 3.2.

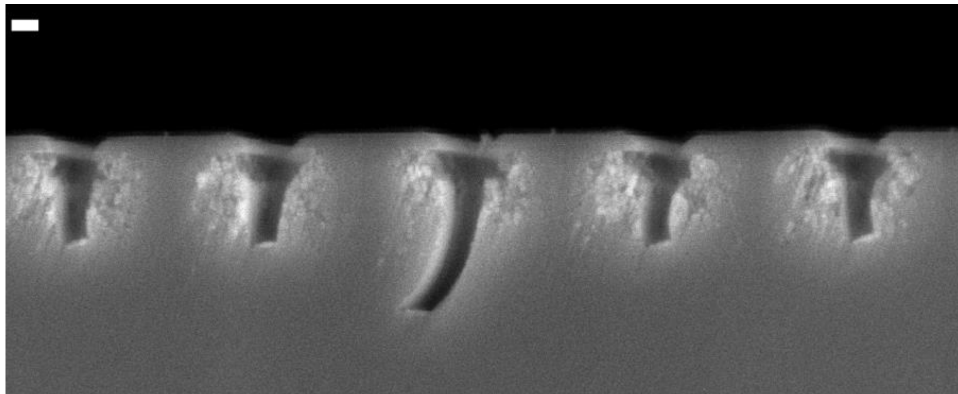


Figure 3-2: Gold MACE of gratings where the etch process switches from vertical to the [100] direction. Microporous silicon present on the sidewalls at the top of the trenches. Scale bar is 100 nm.

An additional set of experiments was performed on the reverse tone of the previous pattern to test the effect of the increasing the catalyst width to ~600 nm from ~150 nm. As seen in Figure 3-3, the bottoms of the trenches after a 40 sec etch, are slightly bowed upwards which shows that the edges etch faster and the gold catalyst can bend[72,73]. This effect is more pronounced for longer etches as shown in Figure 3-4, where the etch process was performed for 80 sec. The gold catalyst can also be seen to be peeling up because of the cleaving for the SEM sample preparation.

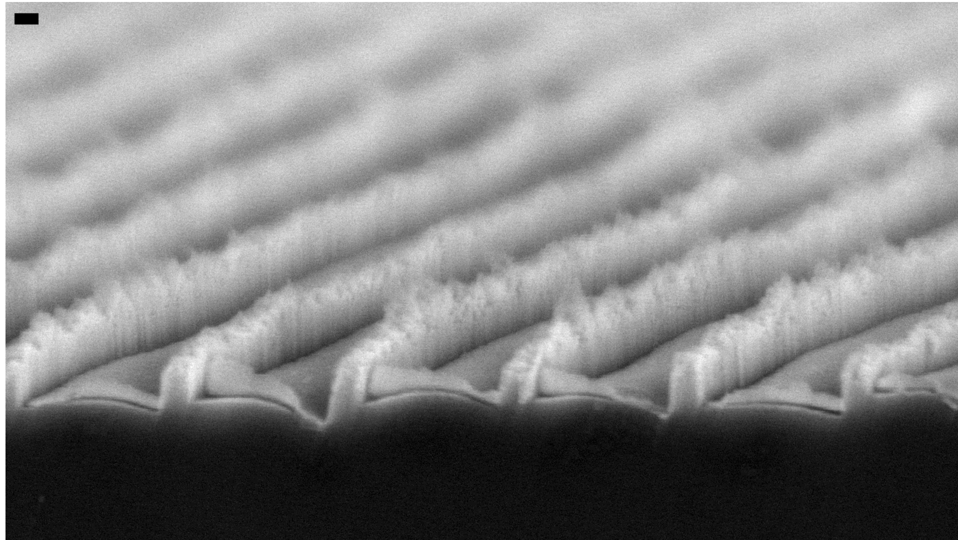


Figure 3-3: SEM image of wider trenches etched with iMACE for 40 sec. Gold delamination visible at the bottom of trench due to cleaving. Scale bar is 100 nm.

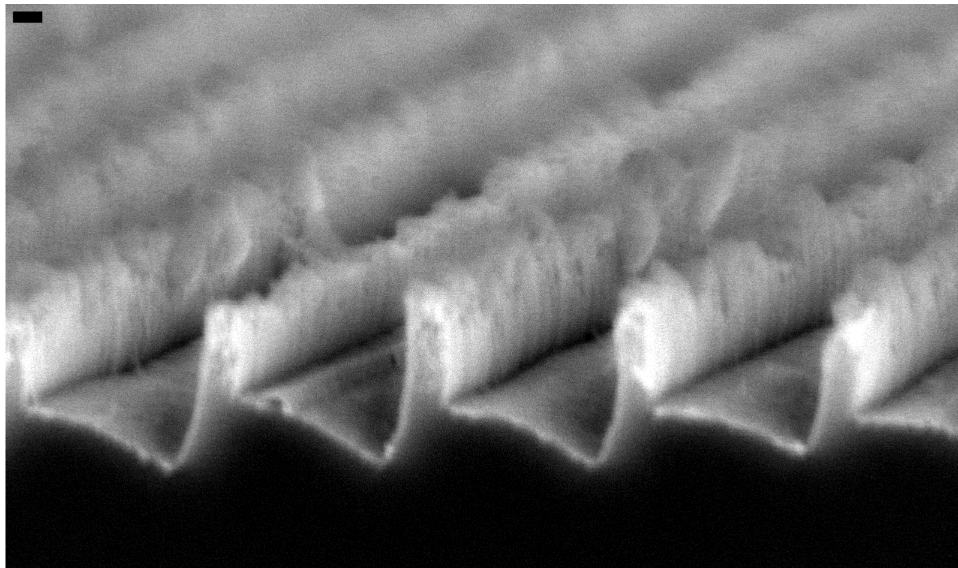


Figure 3-4: SEM image of wider trenches etched with iMACE for 80 sec. Gold delamination visible at the bottom of trench due to cleaving. Scale bar is 100 nm.

3.2 Problem Fundamentals

As described in the previous section, the preliminary experiments show that there are several phenomena associated with the iMACE process. These phenomena include (i) formation of microporous silicon on the sides of the etched features and (ii) changing of the etch direction. In addition, the mechanical stability of the catalyst also has to be considered. Parameters affecting these phenomena are discussed in the following sections.

3.2.1 Etch Solution Composition

The proportions of DI water, H_2O_2, and HF in the etch solution determines the etch regime for the MACE process, which affects both microporous silicon formation and etch direction. The effect of chemical composition on etch regime for MACE is similar to the role of current density in anodic dissolution of silicon in a galvanic cell since they both determine the ratio of holes to HF on the silicon surface. These regimes are shown in Figure 3-5 where $\rho = HF/(HF + H_2O_2)$. In this study, a very low ρ or a higher ratio of H_2O_2 to HF was avoided because it results in electropolishing and craters. The main regime where MACE was performed has a combination of microporous silicon (<2 nm holes on the sidewalls) at low ρ and porous silicon which in the context of the graph is when the etch process only occurs under the catalyst at high ρ. Etching in only the porous silicon regime is desirable because it is when the highest anisotropy can be achieved except that the etch process prefers to etch along crystallographic directions and has a slower etch rate. The formation of microporous silicon on the sides of the etched feature and the preferential etch direction will both be explored in the following sections.[47]

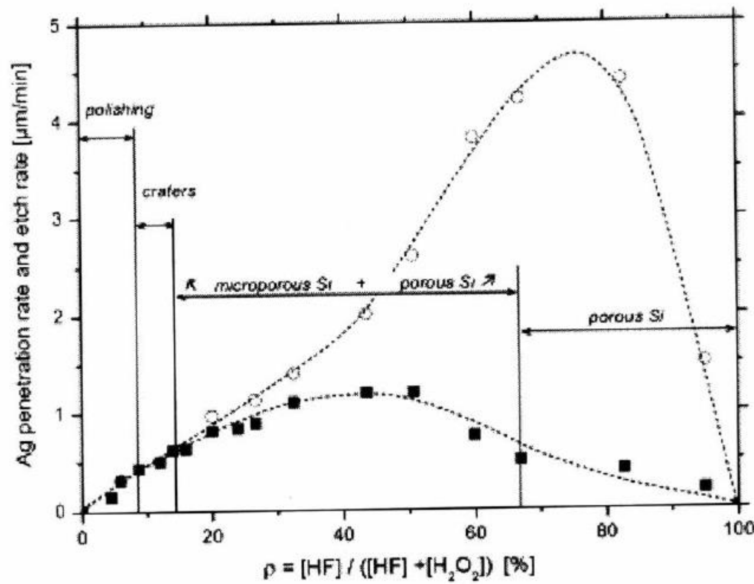


Figure 3-5: Etch regimes for MACE. Open circles: penetration rate of Ag nanoparticles. Filled squares: HF-H_2O_2 etch rate.[47]

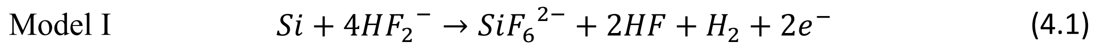
3.2.1.1 Microporous Silicon

The MACE process depends on a noble metal that catalyzes the reduction of an oxidant in the etching solution which creates electron holes that are injected in the Si. Then, HF dissolves the silicon oxidized by the hole injection faster than the surrounding silicon. The proportions of chemicals in the etching solution have to be optimized so that the injection of electron holes (reduction of H_2O_2) is balanced with the consumption of holes (HF dissolution of oxidized Si). Excess holes that are not quickly consumed will diffuse away from underneath the metal catalyst to the walls of the feature being etched as shown by step 5 in Figure 1-7. The excess holes create microporous silicon similar to electrochemical (anodization cell) or stain etching and promote lateral etching which reduces the anisotropy of the process. This occurs for n=4 in Equation 1.4.[2,3,47,70,71]

3.2.1.2 Preferential Etch Direction (Porous Silicon)

It has been observed from the preliminary experiments that the etched features on

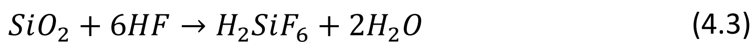
non-(100) wafers are sometimes not vertical but at an angle to the surface. Commonly the slanted direction is along the [100] crystallographic direction. Huang et al has ascribed this phenomenon to the two competing dissolution processes that are dependent on the concentration of H_2O_2 in the solution at the interface between the metal catalyst and Si surface. These models are only describing the reaction at the Si/metal interface and do not include the reduction of the oxidant.[74]



Model I $$Si + 4HF_2^- \rightarrow SiF_6^{2-} + 2HF + H_2 + 2e^- \quad (4.1)$$

Model I (Equation 4.1) is the direct dissolution of Si in the divalent state and occurs when the oxidant concentration or hole generation is too low. This reaction is limited by the transfer of electrons. When a hole reaches the silicon surface, it polarizes the hydrogen terminated surface silicon bond (dangling bond) allowing fluoride ions to break the original bond and create a Si-F bond instead. A second fluoride ion can then attack the neighboring Si-H bond because the first Si-F bond is also polarized. This continues until all the surface silicon bonds have been broken. For a (111) silicon surface there is only one dangling bond which has to weaken three Si-Si back bonds as opposed to the two dangling bonds that are used to weaken two Si-Si back bonds for a (100) surface orientation. This prompts the etch process to occur faster along the [100] direction. This preferential etch direction is similar to the etch mechanism for CODE as discuss in Section 1.3.1.2 and in anodic dissolution of silicon.[47,74]

Model II $$Si + 2H_2O \rightarrow SiO_2 + 4H^+ + 4e^- \quad (4.2)$$



$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \quad (4.3)$$

In Model II (Equations 4.2 and 4.3), silicon oxide is formed at the interface between the metal catalyst and Si and then the oxide is dissolved by the HF. The reaction occurs when the oxidant concentration is high enough so that the holes are injected through the metal into the Si and the oxide forms faster than it is etched away. The

etching occurs directly under the metal, since the oxide formation happens preferentially at the metal/Si interface (where the holes are injected) which is the vertical direction and independent of the wafer orientation and the dissolution of the oxide in HF is an isotropic process which also ignore wafer orientation.[47,74]

There is a window of oxidant concentration where both reactions are occurring so the etch is at an angle between the vertical direction and the [100] direction. A high enough applied voltage through the wafer can also increase the number of holes injected at the metal/Si interface which will switch the etching to Model II. Keeping the concentration of H_2O_2 high enough that Model II is the dominant reaction at the bottom of the pits created by the sidewall requires new reactants to diffuse in and products to diffuse out of the etched feature. As the depth of the pit increases the H_2O_2 concentration decreases and the etch direction eventually changes from vertical to along the [100] direction. An example of this is shown in Figure 3-2, where the concentration of H_2O_2 at the start of the etch process is so high that microporous silicon is formed but later the concentration lowers to the point where microporous silicon is not formed but the etch direction changes.[74,75]

3.2.2 Metal Catalyst Geometry

The geometry of the metal catalyst also influences the anisotropy of the MACE process and the etch direction. The catalyst geometry has also been shown to cause 3D motion of the catalyst[50-52].

3.2.2.1 3D Etch Motion

Certain catalyst geometries have been known to cause 3D motion of the catalyst. For example, in the case of a metal particle as catalyst, it has been theorized that the redox reaction of MACE creates an electric field across the metal particle which induces

a force. This force causes a self-induced electrophoretic motion towards the anode reaction or the silicon substrate. This explains why MACE is independent of the direction of gravity as shown in Figure 3-6 where a sample of silicon is etched equally on three sides at the same time.

Depending on the shape and size of the catalyst, the asymmetric forces can also cause in-plane and/or out-of-plane rotation. For example, a square with extrusions like the one shown in Figure 3-7 or the star in Figure 3-8 will have an in-plane rotation due to the moment created by the force generated at the arms. The motion is perpendicular to the plane of contact between the catalyst and the Si surface.[45,50-52]

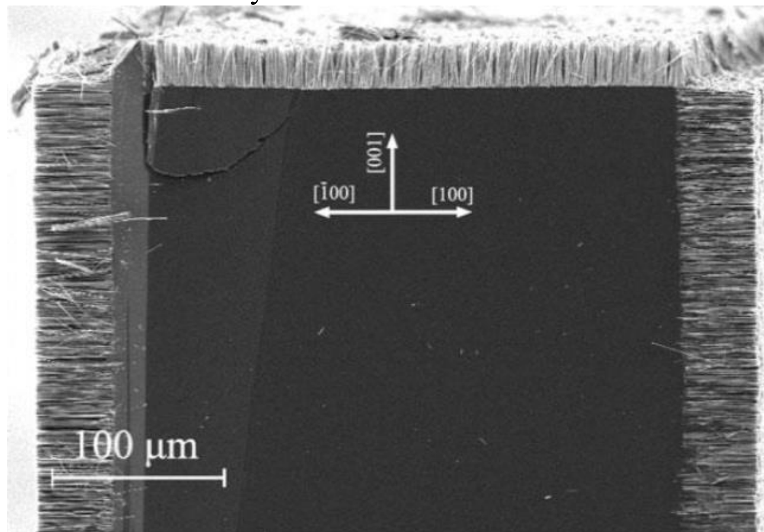


Figure 3-6: Silicon etched from multiple sides using MACE.[45]

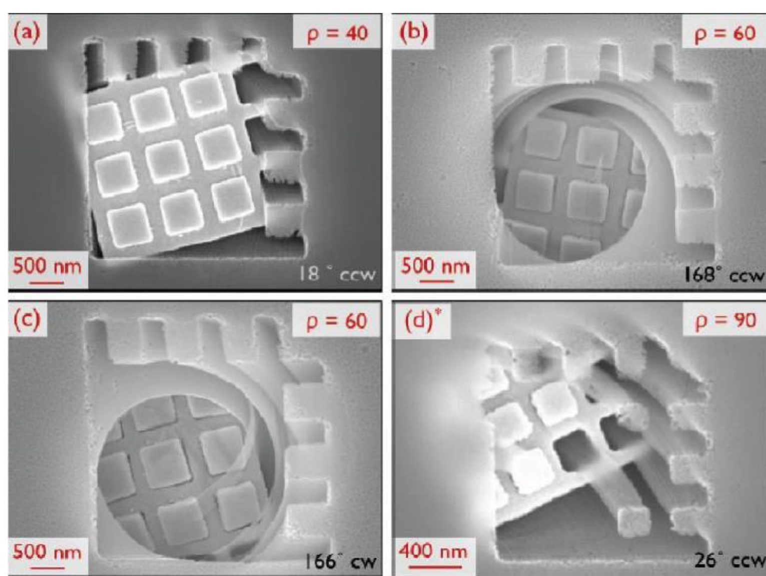


Figure 3-7: A spiral fabricated by the in-plane rotation of a square catalyst with asymmetric extrusions.[50]

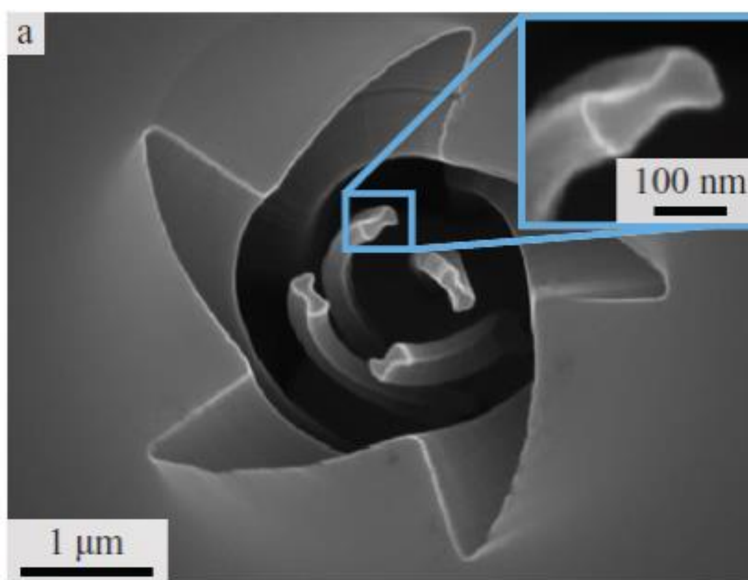


Figure 3-8: A spiral fabricated by the in-plane rotation of a star catalyst with asymmetric extrusions.[52]

If the catalyst is composed of individual metal particles, the particles can move through the silicon in all directions. The etch direction at any given time is dependent on

where the metal/Si interface is located, defects in the silicon, and perturbations in the etch solution flow. Figure 3-9 illustrates the random motion that can occur if the catalyst is made of individual metal particles unless there is an electric field acting on the particles. Vertical etching can occur if the lateral motion of the catalyst can be constrained. Once enough individual metal particles are connected into a continuous film or mesh, any part of the catalyst interacts with its neighbors by pushing or pulling on them which cancels out the lateral motion over the whole area, whereas the vertical etch direction is maintained because each part prefers to etch towards the Si. Chang et al has shown that if the spacing between holes in the mesh is too small then there will not be enough catalyst linked together to cancel lateral motion and constrain the etch direction to the perpendicular direction.[3,74,76]

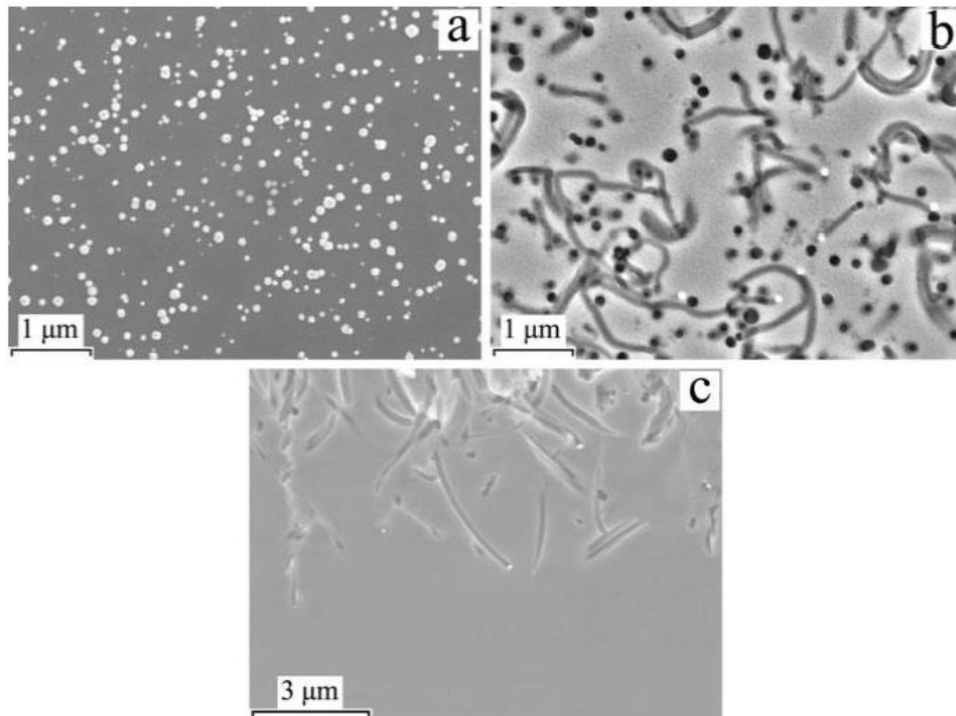


Figure 3-9: SEM image of initial nano-particle catalyst (a), top-down view (b) and cross section view (c) after the MACE process.[77]

3.2.2.2 Catalyst Mechanical Stability

It is important for the metal catalyst to maintain uniform contact with the silicon to keep the shape being etched uniform. The ability to etch a uniform feature determines the anisotropy for the MACE process. The geometry of the metal catalyst influences the direction and magnitude of the forces generated on the catalyst. If the metal bends, folds, or wrinkles because of these forces, then the effective pattern that is etched is different from the desired pattern. An example of how the width of the feature changes when the catalyst bends is shown in Figure 3-10.

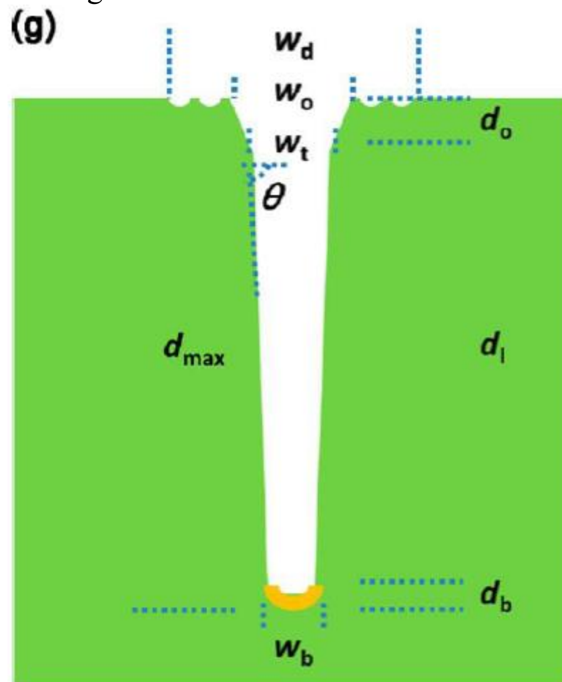


Figure 3-10: Diagram depicting the change in etch width from a bending catalyst.[72]

One of the catalyst deformation mechanisms is delamination of the metal from the silicon surface due to the production of hydrogen gas during the etching reaction[70]. The hydrogen bubbles can also stick to the surface and cause micro masking similar to that in KOH etching. This effect can be mitigated by reducing the surface tension of the etchant

by adding surfactants or other low surface tension fluids like isopropanol[22,31]. There is also a critical size of the catalyst, which can be understood from Figure 3-3 and Figure 3-11. If the distance along which the HF has to diffuse is too large, the HF cannot reach the center of the catalyst before the edges etch and collapse. This phenomenon was observed in the preliminary experiments discussed before in Section 3.1. Micropores can be added to the catalyst, as shown in Figure 3-12, so the diffusion length is small enough for the whole area to etch uniformly as the HF can travel through the holes as well as from the edges of the catalyst. The creation of pillars can be eliminated if the pores are small enough. As will be discussed later in Chapter 4, the patterns used to create the high aspect ratio nanowires for ultra-capacitors in this study, consist of dense features with spacing of 100 nm. This is small enough that the etch rate is uniform between features without needing to add micropores.[2,3,43,72,73]

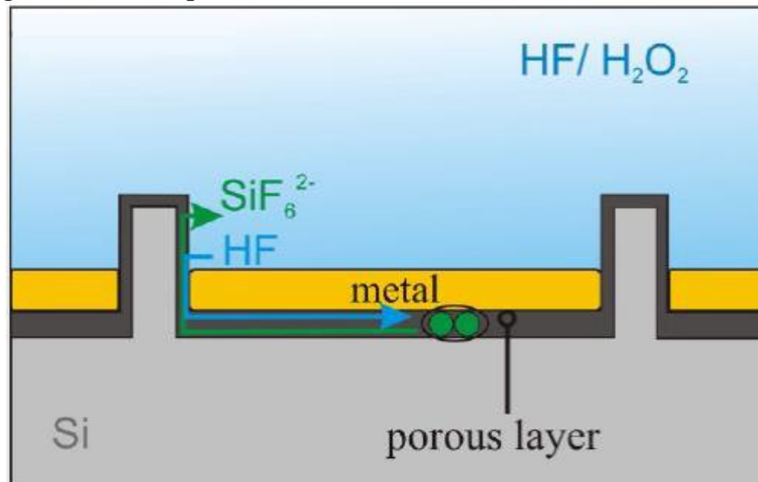


Figure 3-11: Diffusion of MACE reactants and products from edges to the center of the catalyst. (modified from[73])

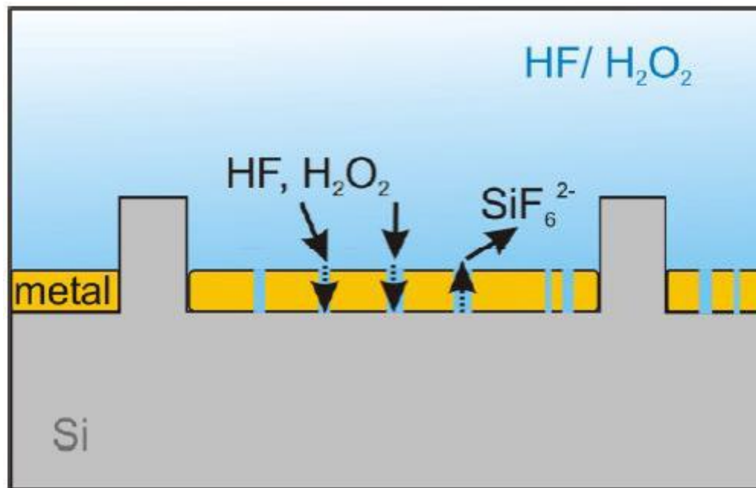


Figure 3-12: Diffusion of MACE reactants and products through a porous catalyst. (modified from[73])

3.3 CONCLUSIONS

The preliminary experiments and literature review have shown that the MACE process can be used to etch high aspect ratio features with constraints on the composition of the etch solution and the form of the metal catalyst. Microporous silicon will form if too much hydrogen peroxide is used because excess holes are generated and diffuse away from the catalyst. Electropolishing can occur if the amount of hydrogen peroxide exceeds the amount for microporous silicon formation which will result in total feature loss. Too little hydrogen peroxide will result in the etch process following the (100) direction which need not be the vertical direction. A catalyst metal mesh is needed to keep the metal from wandering during the MACE process. Taking all this learning into account, the following chapter describes the processes used to pattern a gold layer to create a mesh for the MACE process to fabricate high aspect ratio nanoscale features with unique cross section geometries. The target application for having a high surface area per unit projected area is increased capacitance, and hence better performance of silicon nanowire capacitors.

Chapter 4: Fabrication of Silicon Nanowires with High Surface Area per Unit Projected Area

The knowledge of the iMACE process, as discussed in Chapter 3, has been used to fabricate nanowires with increased surface area per unit projected area. There are two components to increasing the surface area per unit projected area: (i) increasing the aspect ratio of nanowires and (ii) patterning nanowires with non-circular cross section geometry. For both of these options, it is still important to maintain the fidelity of the gold mesh during the course of the entire MACE step. Hence, the first section of this chapter discusses efforts to reliably pattern the gold layer to be used as the catalyst during MACE process. The next section discusses the fabrication of high aspect ratio nanowires and its limitations pertaining to the collapse of the nanowires. The third section then briefly discusses the benefits of non-circular cross section geometries of nanowires. The final section compares the performance of circular and non-circular nanowire geometries with capacitors as an exemplar device to validate the effect of using different cross section geometries on increasing the capacitance per unit area.

4.1 Patterning Gold Mesh for MACE Process

iMACE was chosen to replace iCODE as the method for fabricating high aspect ratio pillars because it can be highly anisotropic without the tight geometry constraints of iCODE. Other research groups have used MACE to fabricate high aspect ratio pillars but have used nanosphere lithography, block co-polymers, and anodized aluminum oxide (AAO) templates to pattern the metal catalyst. Nanosphere lithography can get high fill factors but does not have long range order. The long range order worsens for smaller spheres so sub-20 nm features cannot be fabricated without a dry etch step to reduce the size of the original spheres which leads to a lower fill factor and reduces the feature

density. Block co-polymers also have problems with long range order without using a top-down patterning technique to direct the assembly. AAO templates can pattern smaller features but they cannot achieve fill factors higher than 50%. All the mentioned methods can only pattern periodic circular pillars but imprint lithography can pattern a greater variety of shapes, including squares, which would have a larger fill factor compared to circular cross section pillars for the same critical dimension. Various non-circular geometries can also be used to improve the area moment of inertia, which will increase the stiffness of the nanowires, thus allowing for higher aspect ratio pillars and larger surface area to projected unit area.[3,42-46]

4.1.1 Wet Etch of Gold

The first attempt at fabricating pillars used a template with 100 nm pillars and a pitch of 200 nm to create holes in a sacrificial polymer layer that was on a material stack of (100) Si, 2 nm of titanium (Ti) as an adhesion layer, and 15 nm of Au. After a descum etch, holes in the polymer were opened allowing an iodine solution-based gold etch to transfer the holes to the metal layers underneath which created a catalyst mesh for the MACE process. Initially, the gold etchant was used without diluting it but the etch rate was high enough that the process lacked control and the catalyst was over etched. However, even with very dilute concentrations of the etchant (1:10 gold etchant to DI water) and a lower etch rate, the gold catalyst could not be controllably etched. This over-etching prevented the catalyst from being a continuous mesh, and formed individual gold islands that were not constrained to move in only the vertical direction (see Section 3.2.2 on vertical MACE). Figure 4-1 shows the gold pattern that was fabricated due to over etching and Figure 4-2 shows the result when the over etched catalyst was used in the MACE process. The SEM image shows the features created when the gold catalyst is

able to move in any direction because it is spilt into many islands instead of a continuous mesh.

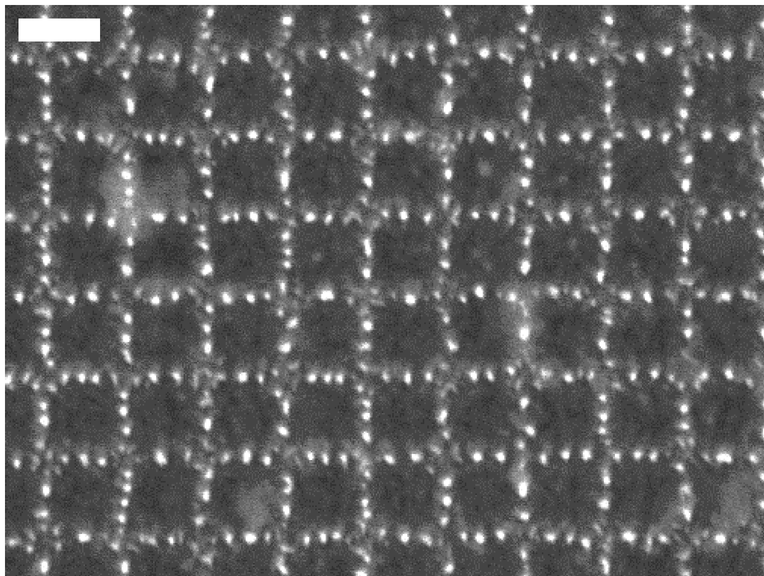


Figure 4-1: Over etched gold mesh showing non-continuous metal catalyst. Scale bar is 200 nm.

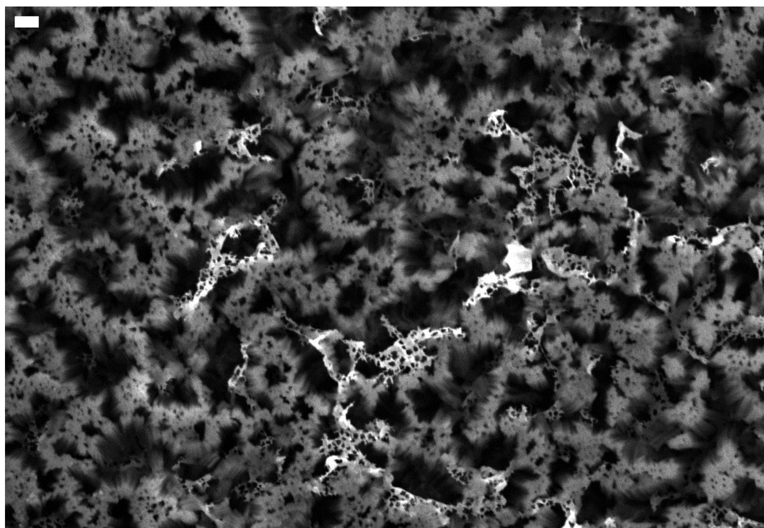


Figure 4-2: Result of MACE using the over etched gold mesh. Scale bar is 1 μm.

4.1.2 Dry Etch of Gold

Gold is most commonly etched with wet chemistry but some groups have successfully etched gold with a dry etch using Cl_2 and Ar gases. (Aydemir, A. 2012) (Efremov, A. M. 2003) The dry etch resulted in a continuous gold mesh but with irregular shaped holes as seen in Figure 4-3. This led to the fabrication of irregular pillars when the gold mesh was used as the catalyst in a 2 min MACE process (62 mL H_2O, 20 mL 30% H_2O_2, and 18 mL 49% HF) as shown in Figure 4-4 and Figure 4-5. Figure 4-6 shows the cross section of the same sample. The aspect ratio was calculated to be around 11.7. The samples were etched further to increase the aspect ratio but feature collapse was observed after an additional 3 min etch. The modes of failure of the nanowires are discussed in the Section 4.2. The irregular shaped pillars etched using MACE also indicate that, if properly controlled, it might be possible to fabricate pillars with unique cross section geometries with sharp corners.

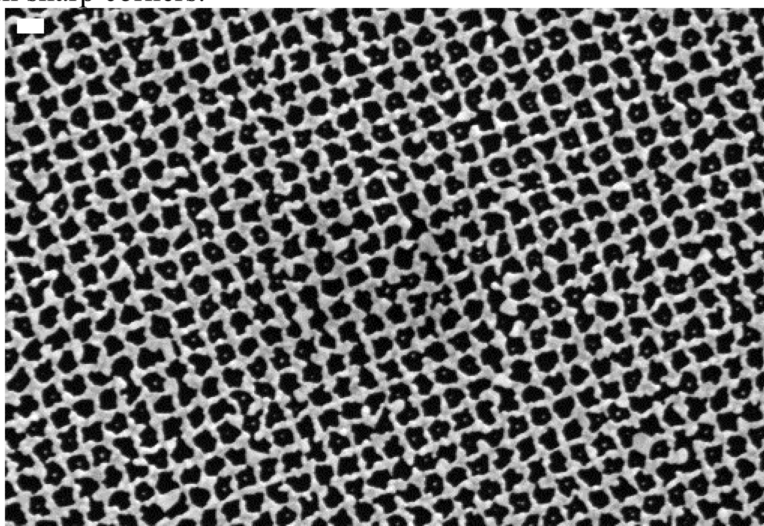


Figure 4-3: Gold mesh fabricated using an inductively coupled plasma (ICP) etch. Scale bar is 200 nm.

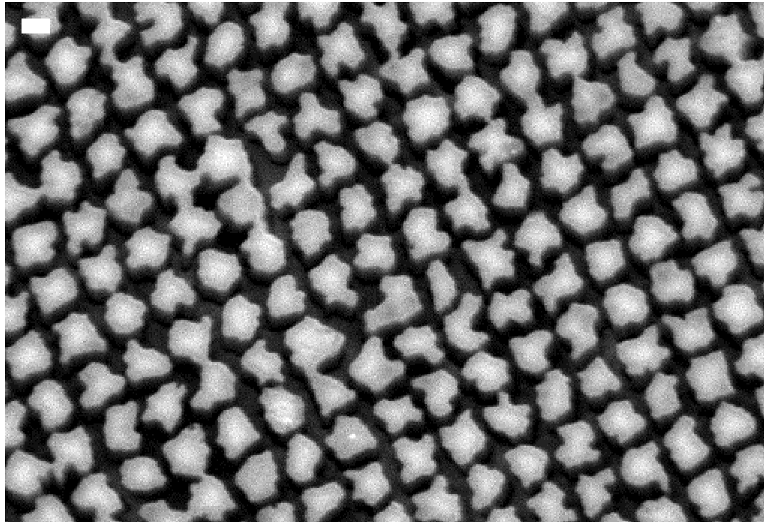


Figure 4-4: Irregular pillars etched using MACE after dry etching of gold to form a continuous mesh. Scale bar is 100 nm.

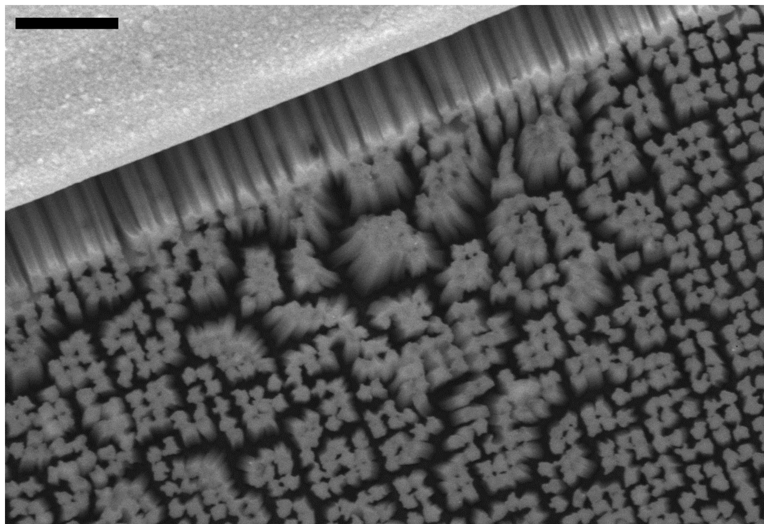


Figure 4-5: Irregular pillars etched using MACE after dry etching of gold to form a continuous mesh. Feature clumping can be seen. Scale bar is 1 μm.

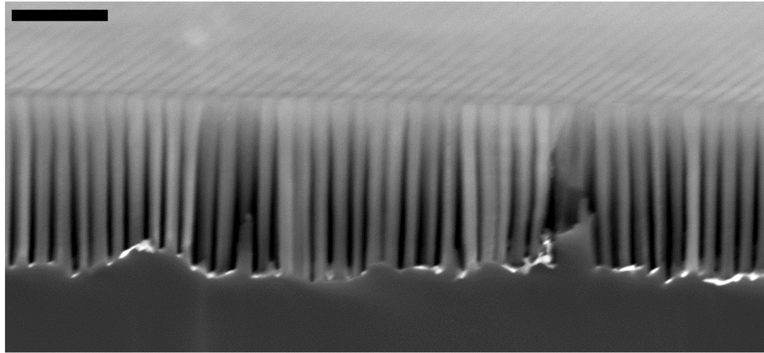


Figure 4-6: Cross section SEM of 1.7 μm tall irregular pillars etched using MACE after dry etching of gold. Scale bar is 1 μm.

4.1.3 Bi-layer Lift-off Process

The bi-layer lift off process shown in Figure 4-7 was used to pattern the gold catalyst mesh with a higher degree of geometric shape precision than has been obtained using gold etch techniques. The process starts by spin coating a wafer with PVA to act as the lift-off layer later in the process. After an array of holes are patterned on top, Silspin™ is deposited so that these holes are filled. The Silspin™ is etched back by using a CHF_3 and O_2 etch to create an array of Silspin™ cylinders surrounded by polymer. The polymer layers can then be etched in plasma O_2 to oxidize the Silspin™ which acts like a hard mask for the isotropic etch of the polymer. This etch creates overhangs essential to creating sharp edges during the gold deposition in an e-beam evaporator so the metal does not tear during lift-off. Approximately ~2 nm of titanium was used as an adhesion layer to avoid gold delamination during lift-off. As shown in Figure 4-9, the resulting gold mesh fabricated using the bi-layer lift-off process has higher fidelity features of the template (100 nm holes, 200 nm pitch) than those shown in Figure 4-3 but there are still cracks between some of the holes in the mesh. The resulting nanowires fabricated after performing MACE using the gold mesh are shown in Figure 4-10.

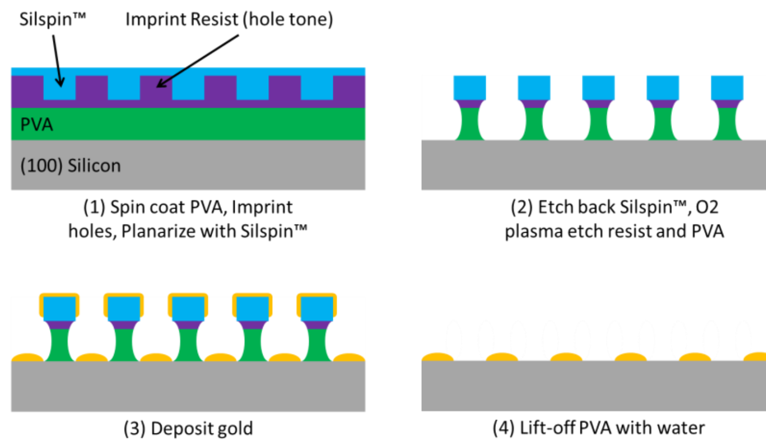


Figure 4-7: Process flow of bi-layer lift-off using a template that prints holes in the resist.

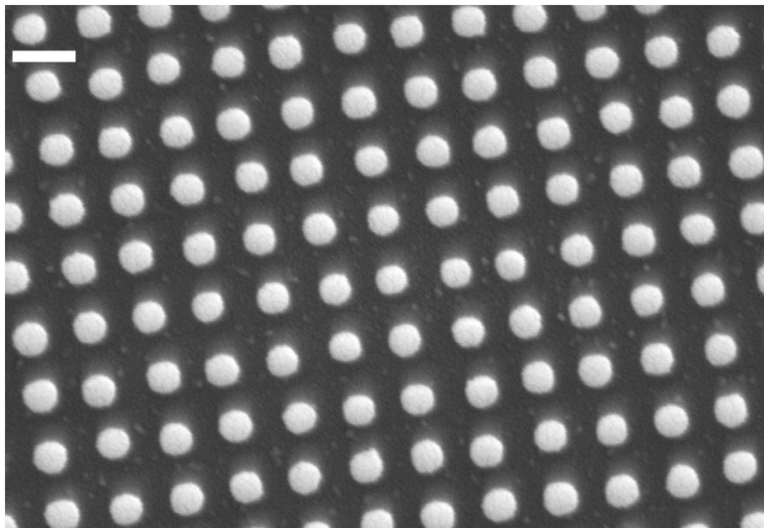


Figure 4-8: Silspin™ pillars before Ti/Au deposition. Scale bar is 200 nm.

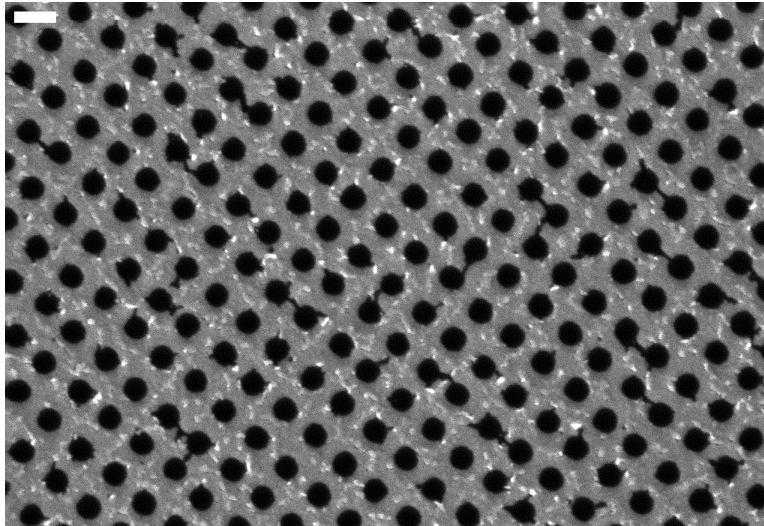


Figure 4-9: Gold catalyst mesh fabricated using bi-layer lift-off process. Scale bar is 200 nm.

Figure 4-10: Nanowires fabricated using gold mesh fabricated using bi-layer lift-off process. Scale bar is 200 nm.

4.1.4 Reverse Tone Bi-layer Lift-off Process

As discussed in Section 4.2.2, using a dry etch to pattern the gold catalyst can allow the creation of non-circular geometries. This approach was this used to design a process for fabrication of a catalyst mesh with diamond-shaped holes. The template with diamond-shaped features was fabricated by Anshuman Cherala as part of his research to

determine the relaxation of sharp corners of imprint resist. The diamond features were created when SiO_2 was deposited via ALD on a template with circular pillars arranged in a rectilinear grid. Enough material was deposited on the features so that neighboring pillars touch creating diamonds in the interstitial space as shown in Figure 4-11. The difficulty with this template is that the features are a reverse tone of the template used in the previous patterning methods. This requires using the reverse tone bi-layer lift process shown in Figure 4-12. Pillars are transferred from the imprint resist after descum to a silicon dioxide hard mask. The hard mask then allows for an overhang to form during an isotropic plasma O_2 etch. The results of the process are shown in Figure 4-13, Figure 4-14, and Figure 4-15. Unfortunately the resulting mesh has defects such as connecting diamonds and diamonds that are rotated as well as incomplete lift-off. The connected diamonds are a result of the ALD not closing the gaps consistently across the template. The rotated diamonds most likely occur because the mask features for gold deposition are on top of thin pillars that can twist. This defect was not investigated more thoroughly because it does not occur in the next patterning method since the silicon dioxide mask is no longer present and the size and weight on the pillar is reduced. The failed lift-off occurs when the overhang is too small and the gold is a continuous film that the water cannot bypass to dissolve the PVA.

Figure 4-11: Diamond shape created by ALD deposition on template with circular nanoscale pillars.

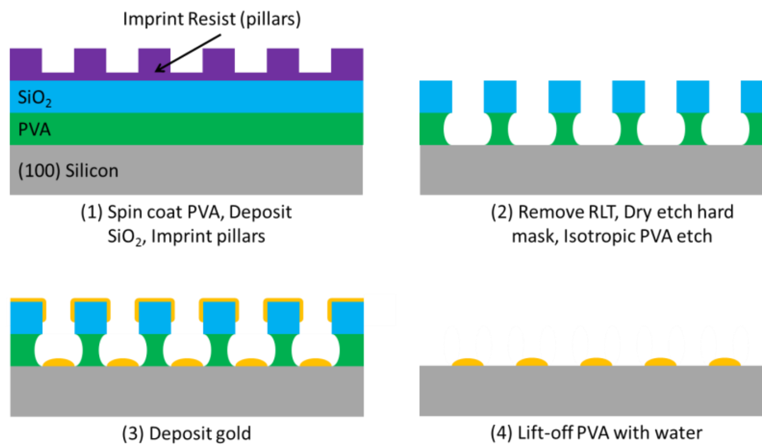


Figure 4-12: Reverse tone bi-layer lift-off process with resist pillars instead of holes.

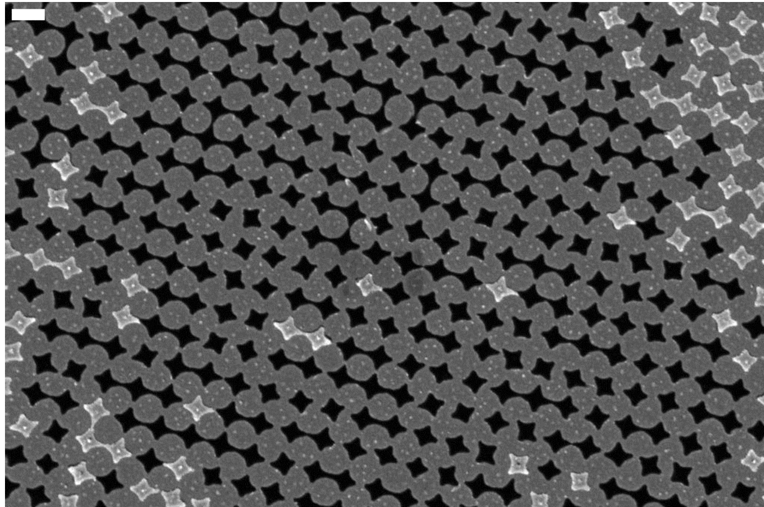


Figure 4-13: Gold mesh with diamond patterns. Defects include connected diamonds, rotated diamonds, and incomplete lift-off. Scale bar is 200 nm.

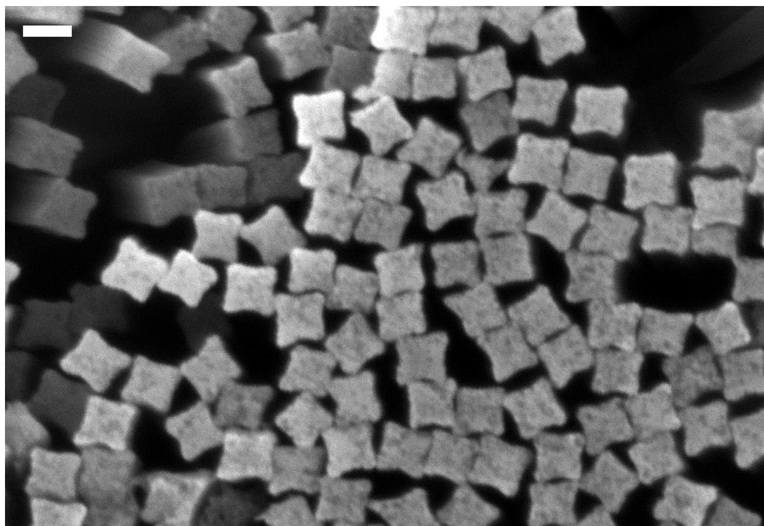


Figure 4-14: Diamond pillars created by gold mesh. Scale bar is 100 nm.

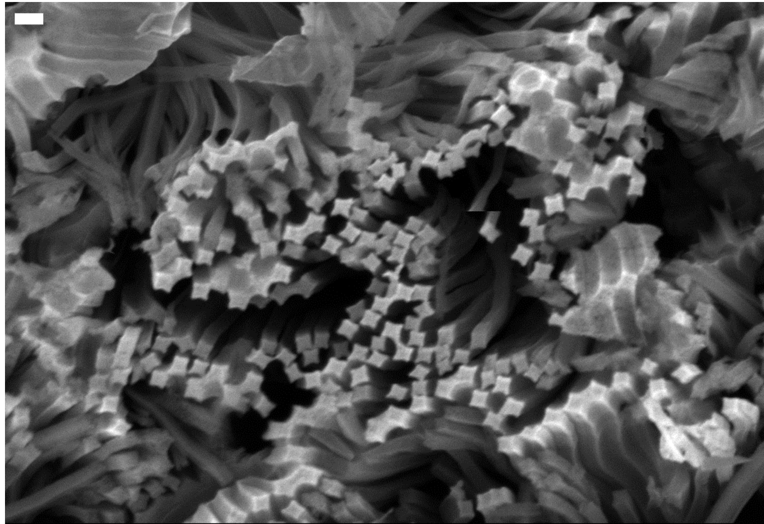


Figure 4-15: Diamond pillars with defects resulting from imperfect catalyst mesh. Scale bar is 200 nm.

4.1.5 Simplified Bi-layer Lift-off Process

A simplified bi-layer lift-off process was created to decrease complexity and improve pattern fidelity by reducing the number of etch steps. The process flow is shown in Figure 4-16. The hard mask used in the reverse tone bi-layer lift-off process is removed and one organic etch is able to create a sufficient overhang for the deposition step due to the differences in the imprint resist and the lift-off layer (PVA). The simplified process flow results in better pattern fidelity as shown in Figure 4-17, Figure 4-18, Figure 4-19, and Figure 4-20. This process can be used by both patterns. There are no cracks between circles and the diamonds are not connected or rotated.

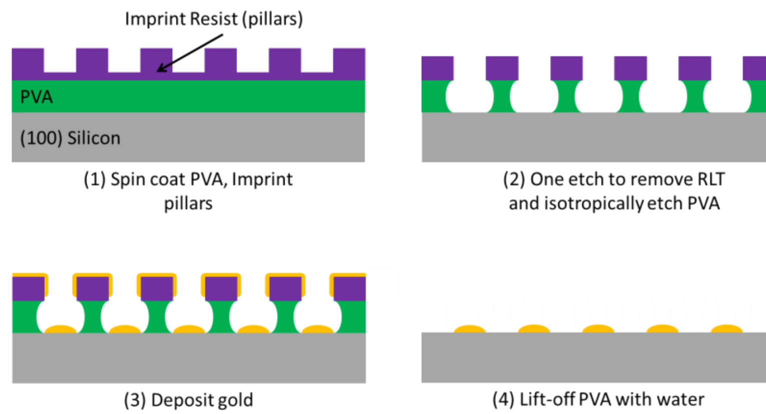


Figure 4-16: Simplified bi-layer lift-off process where SiO_2 hard mask is removed and the selectivity between the imprint resist and PVA only needs one polymer etch to create a sufficient overhang for the gold deposition.

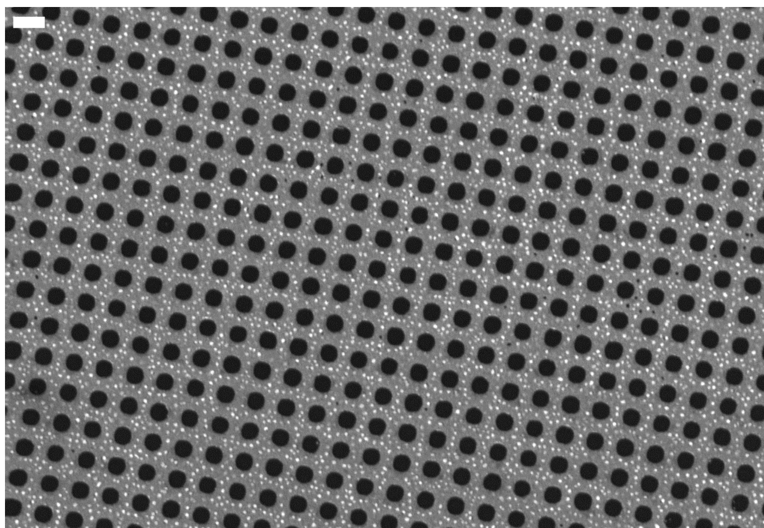


Figure 4-17: Gold mesh with circular holes created using simplified process. Scale bar is 200 nm.

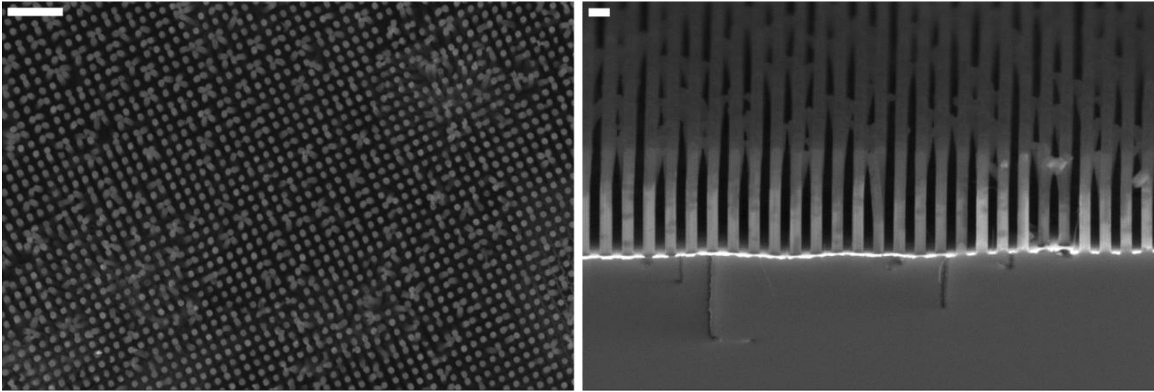


Figure 4-18: (Left) Top down SEM of pillars etched using simplified circular mesh. Scale bar is 1 μm. (Right) Cross section SEM of pillars etched using simplified circular mesh. Scale bar is 200 nm.

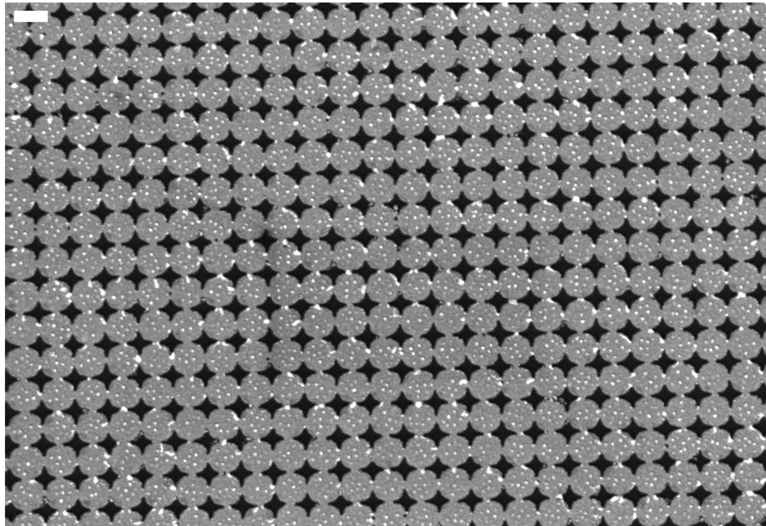


Figure 4-19: Gold mesh with diamond holes created using simplified process. Scale bar is 200 nm.

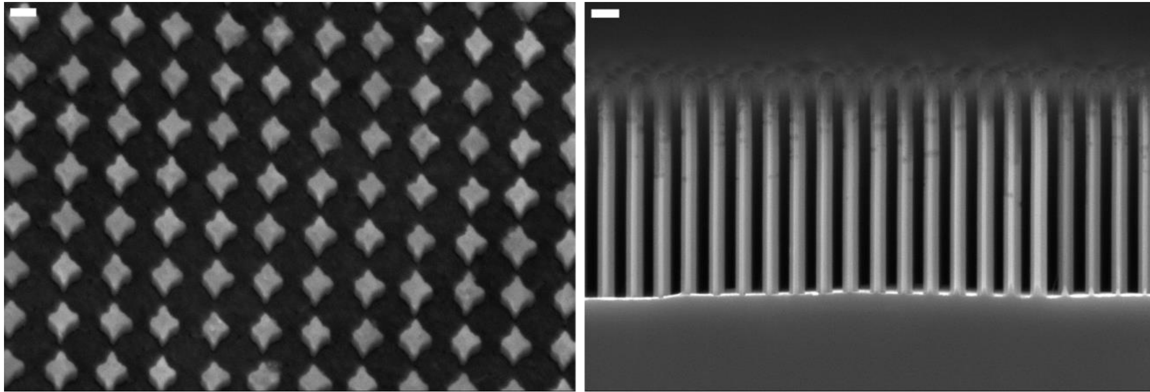


Figure 4-20: (Left) Top down SEM of pillars etched using simplified diamond mesh. Scale bar is 100 nm. (Right) Cross section SEM of pillars etched using simplified diamond mesh. Scale bar is 200 nm.

4.2 Increasing Surface Area per Unit Projected Area Through High Aspect Ratio Features

As discussed previously, the surface area per unit projected area can be increased by increasing the height of the nanowires. However, the feature heights cannot be increased arbitrarily because of issues with collapse. To investigate the limits of feature height, the sample with irregular nanowire cross sections, as seen in Figure 4-4, was etched for another 3 min to test the stability of the resulting nanowires. This increased the aspect ratio of the nanowires to ~28, but the nanowires bent and adhered to each other forming clumps as shown in Figure 4-21. Figure 4-22 and Figure 4-23 also show collapsed nanowires with circular and diamond cross sections respectively.

There are three main modes of failure which cause features to collapse: (i) buckling due to the weight of the nanowire, (ii) capillary forces acting on the nanowire when the etch solution is drying, and (iii) surface forces occurring during handling of the wafer. These forces will be discussed in Section 4.2.1. There are also two phenomena that keep the features from returning to a vertical position after they have collapsed: (i)

adhesion to the substrate, and (ii) adhesion to neighboring nanowires. These phenomena will be discussed in Section 4.2.2.[78-84]

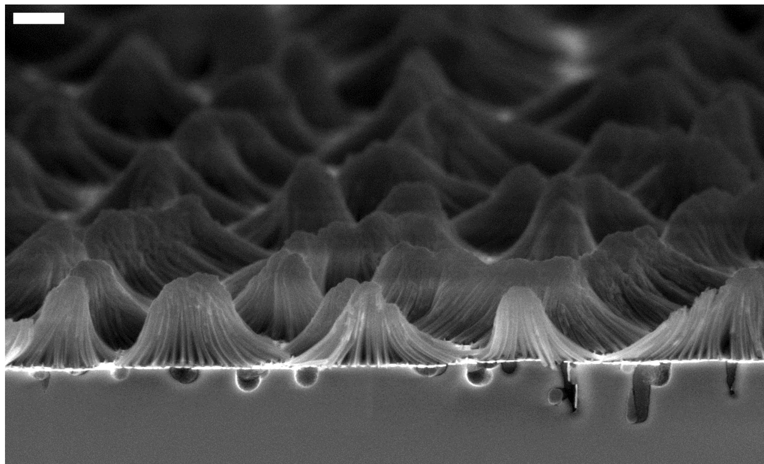


Figure 4-21: Cross section of collapsed irregular pillars. Scale bar is 1 μm.

Figure 4-22: Top down view of collapsed circular pillars. Scale bar is 200 nm.

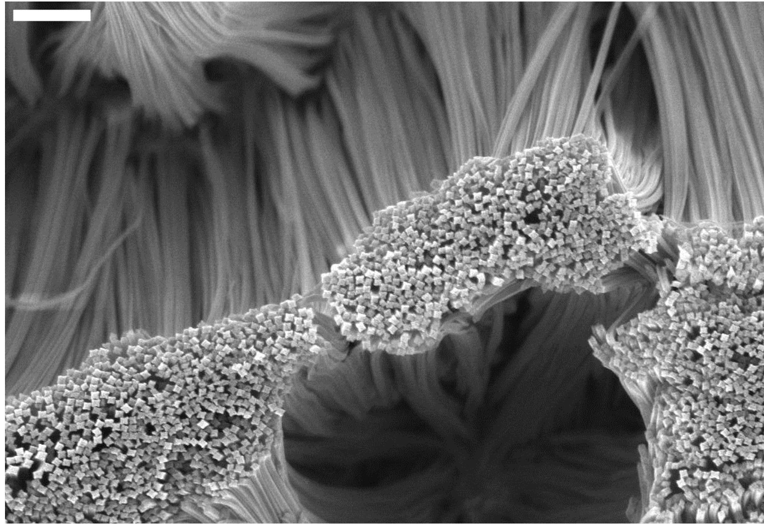


Figure 4-23: Top down view of collapsed diamond pillars. Scale bar is 1 μm.

4.2.1 Forces Responsible for Collapsing Pillars

The three forces that cause high aspect ratio features to collapse are (i) surface forces occurring during handling of the wafer, (ii) buckling due to the weight of the nano-pillar, and (iii) capillary forces acting on the nano-pillar when the etch solution is drying. It is hard to analytically determine, model, or measure the forces that act on the nanowires from external forces like those created during handling of the wafer. The effect of these external forces will be observed if the elastic restoring force cannot overcome the adhesion forces that will keep the pillars bent if the other forces can be eliminated.

The critical height at which the nano-pillar will begin to buckle under its own weight can be calculated using the Equation 4.1[81], where E is the Young's modulus (150 GPa for Si), I is the area moment of inertia ($\frac{\pi}{3}r^4$ for a circular cross section), A is the area (πr^2 for a circular cross section), ρ is the density (2.3290 g/cm^3), g is the acceleration of gravity (9.81 m/s^2), and B is the first zero of the Bessel function of the first kind of order -1/3, which is equal to 1.86635.

$$h_{crit,buckling} = \left(\frac{9B^2EI}{4\rho gA}\right)^{1/3} \quad (4.1)$$

Capillary forces acting on the nanowires occur when the MACE solution is removed after etching and the etching solution dries. These forces are complex to calculate because they depend on the shape of the meniscus that forms between pillars. The meniscus has been determined analytically for cylindrical cross sections but requires some assumptions to be made.[84] Equations 4.2-4.4[82,83] are used to calculate the maximum height before the capillary force between circular pillars is larger than the elastic restoring force where d is the diameter of the circular pillar, p is the center-to-center pitch, E is the Young's modulus (150 GPa for Si), θ is the contact angle for the etch solution, γ_{lv} is the surface tension between the etch solution and air, and f(r) is a function of $r = p/d$. The meniscus can also be solved for numerically without the need for making the simplifying assumptions. The numerical method can potentially be used to solve for the meniscus for arbitrary cross section geometries and pillar placement but will be extremely difficult especially for geometries with sharp corners[84]. Figure 4-24 shows the boundary conditions used to calculate the meniscus profile used to needed to determine capillary forces for two cylinders. Capillary forces are considered to be the main for behind feature collapse. Several approaches to reduce the effect of the capillary forces on the nanowires are discussed in Section 4.2.3.

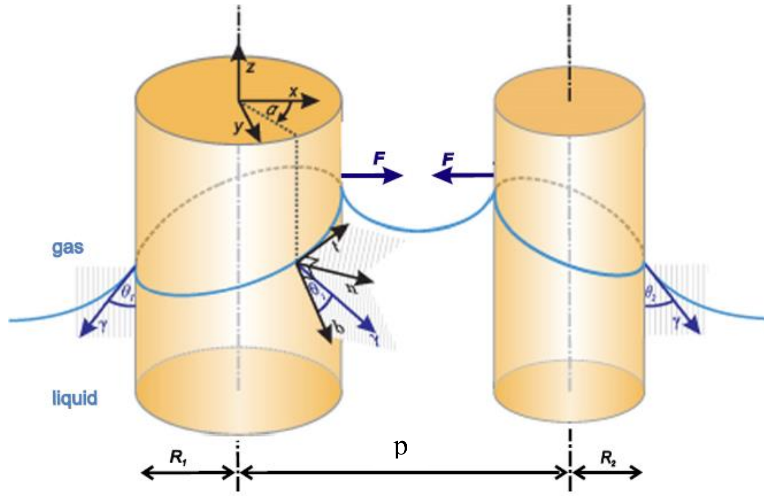


Figure 4-24: Boundary conditions used to calculate the meniscus profile for two cylinders.[84]

$$h_{crit,cap} = \left(\frac{3Ed^4}{32\sqrt{2}(\cos\theta)^2 \gamma_{lv} f(r)} \right)^{1/3} \tag{4.2}$$

$$f(r) = \frac{1}{r-k}\left(\sqrt{\frac{2}{k^2-1}} + \sqrt{\frac{1}{2k^2-1}} \right) \tag{4.3}$$

$$r = \frac{1}{k}\left(\frac{\sqrt{2}(k^2-1)^{-1/2} + (2k^2-1)^{-1/2}}{\sqrt{2}(k^2-1)^{-3/2} + 2(2k^2-1)^{-3/2}} \right) + k = \frac{p}{d} \tag{4.4}$$

4.2.2 Forces Responsible for Keeping Collapsed Nanowires Adhered Together

Once the wires have been bent due to the transient capillary and external forces discussed above, a static force is required to resist the elastic restoring force to keep the pillars bent if the feature collapse is observed. This static force can be described by the work of adhesion between two surfaces. The two cases that can occur are the pillars are adhering to the substrate (Equation 4.5) or to each other (Equation 4.6). The exemplar application of ultra-capacitors, as discussed later in Section 4.4, needs high density features which mean that the probability of the pillars making contact with their neighbors is higher than making contact with the substrate so this study focuses on pillar

adhesion with neighbors. The critical height at which the pillars will begin to adhere to their neighbors can be calculated by balancing the energy of adhesion with the bending strain energy and the elastic energy created by the deformation at the contact region. Figure 4-25 illustrates the deformation that occurs when two cylinders adhere to each other. The contact width is given by $2r_c$ where r_c is defined by Equation 4.8 and U_c is the elastic energy in the pillar due to the deformation of the pillar along the length of contact. Figure 4-26 shows that the adhesion between pillars occurs at the ends because the tips are easier to deflect which requires less adhesion energy to balance out. It should be noted that the geometry of the pillars where they make contact will determine the contact width so a pillar with sharp contacting corners will allow for larger aspect ratios. Statically charging the pillars after they have been dried and clumped together maybe a way to force the pillars apart due to the repelling forces of same charge, while ensuring that the charge is evenly applied without causing high amperage points that could damage the pillars.[78,80,81,85]. This was beyond the scope of this work.

$$h_{crit,sub} = \frac{\pi^{5/3}}{2^{11/3}3^{1/2}}(1-\upsilon^2)^{-1/6}\left(\frac{E}{2\gamma_{SV}}\right)^{2/3} d^{5/3} \tag{4.5}$$

$$h_{crit,neighbor} = \left(\frac{36EI\left(\frac{p-d}{2}\right)^2}{2\gamma_{sv}(2r_c)-U_c}\right)^{1/4} \tag{4.6}$$

$$U_c = \frac{E\pi(r_c)^4}{32(1-\upsilon^2)R^2} \tag{4.7}$$

$$r_c = \left(\frac{32R^2\gamma_{sv}(1-\upsilon^2)}{\pi E}\right)^{1/3} \tag{4.8}$$

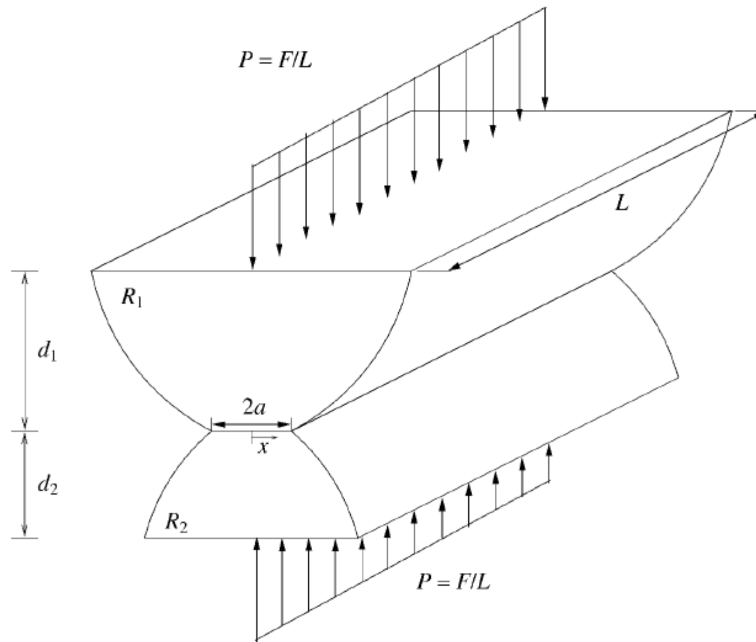


Figure 4-25: Contact width for two deforming cylinders.[85]

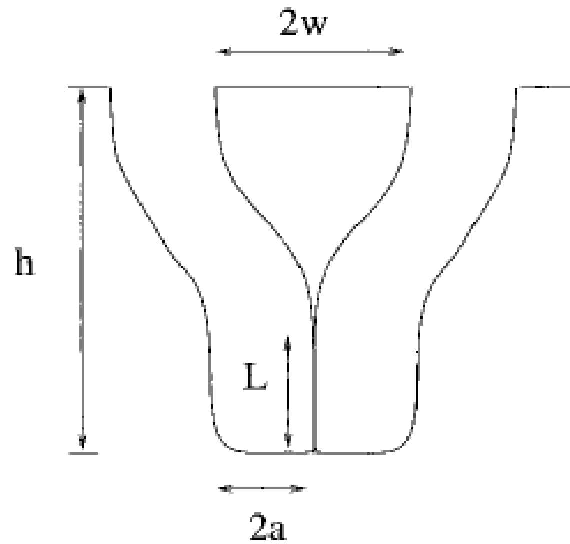


Figure 4-26: Bending due to contact of two pillars.[81]

4.2.3 Mitigating Feature Collapse Induced by Capillary Forces during Drying

In general, the adhesion to the neighboring pillars becomes the height limiting factor if the capillary forces can be mitigated. There are several methods used to either

reduce or remove capillary forces. This section will review some but not all the possible methods.

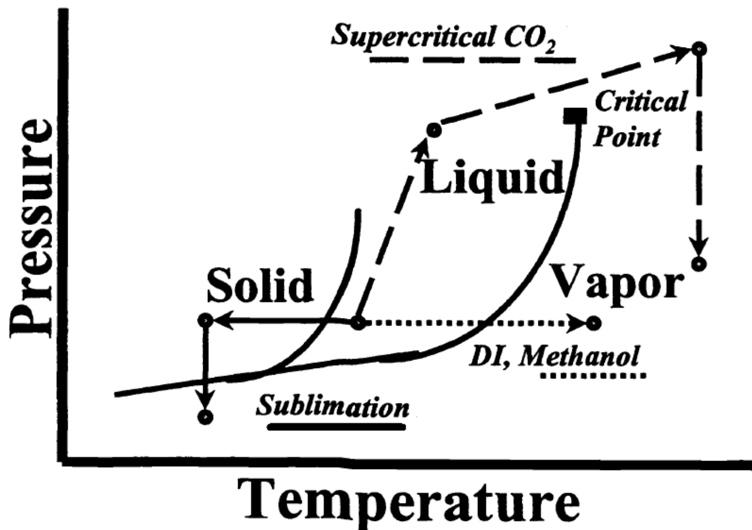


Figure 4-27: Three drying methods displayed on a phase diagram. (modified from [86])

4.2.3.1 Evaporation Drying with Low Surface Tension Fluids

The first method is a modified version of evaporation drying where the etch solution is first exchanged with DI water and then a fluid with low surface tension. Figure 4-27 shows that normal evaporation drying crosses the liquid-vapor boundary which causes stiction. Karthik Balasundaram et al have reported that they been able to achieve ~180 aspect ratio features without collapse by exchanging the DI water with a solution of methanol and DI water and then baking the samples in an oven at 60-80 °C. This method was attempted with the 100 nm pillars with 200 nm spacings but was unsuccessful because the feature sizes are smaller and closer together than those used by Karthik Balasundaram (550 nm features) and the report did not include details on how the fluid was exchanged and the setup used to reduce external forces due to handling the wafer. The smaller pitch makes exchanging fluids difficult and slow so uneven etching

continues even when rinsing in water, thus influencing the stability of the pillars. Also handling is more of an issue with 100 nm features versus 550 nm features.[86-88]

4.2.3.2 Critical Point Drying (CPD)

A commonly used method for drying a sample without causing stiction is critical point drying (CPD). This method utilizes the fact that CO_2 can be made to move around the critical point of the phase diagram so as not to cross the liquid-vapor boundary. This is achieved by a tool, which exchanges a fluid that the sample is in, with liquid CO_2. Normally the water used to rinse an etched sample has to first be exchanged with ethanol before it is put in the tool because water and liquid CO_2 are not miscible. Once only liquid CO_2 remains, the chamber is pressurized, then heated, and finally depressurized so the liquid becomes a vapor without crossing the boundary and the sample is dry. This process is shown in Figure 4-27 and was used by Shih-Wei Chang to fabricate nano-wires with an aspect ratio of 220 shown in Figure 4-28. CPD was not used in this study because the only tool available has a limit on the sample size and requires driving to a different facility which adds to the amount of handling required.[46,86,88]

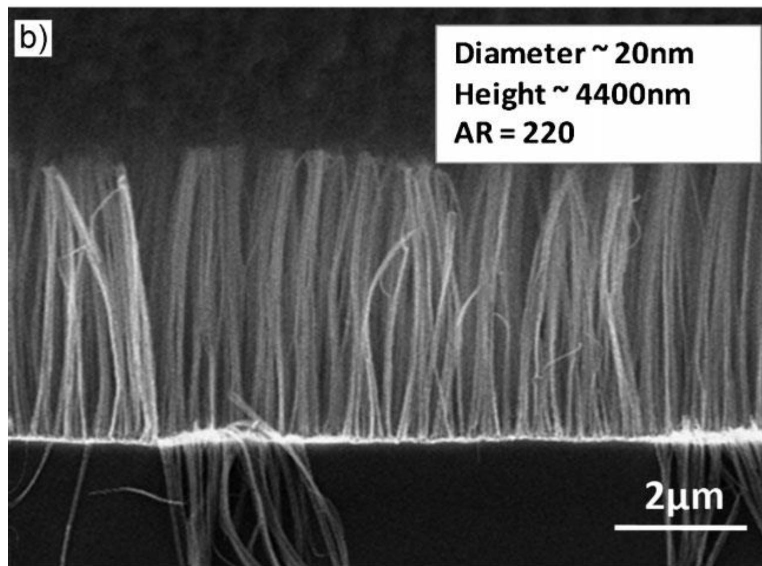


Figure 4-28: Nano-wires with aspect ratio of 220 using CPD patterned with nanosphere lithography.[46]

4.2.3.3 Sublimation

Sublimation is another process that avoids crossing the liquid-vapor boundary as shown in Figure 4-27. First the DI water used to rinse the sample is exchanged with a fluid that is easy to sublimate like t-butyl alcohol (26 °C melting temperature) or p-dichlorobenzene (56 °C melting temperature). A sublimation apparatus like the one shown in Figure 4-29, is then used to lower the temperature of the fluid inside the chamber until it solidifies and then the pressure is lowered until the solid changes directly to vapor.[86,88,89] The initial attempts at using sublimation to mitigate capillary forces were unsuccessful. Potential reasons for the failures are the inadequate setup for smooth fluid exchange and the amount of travel between the etch bench, the sublimation apparatus (different facility), and the scanning electron microscope used to characterize the results.

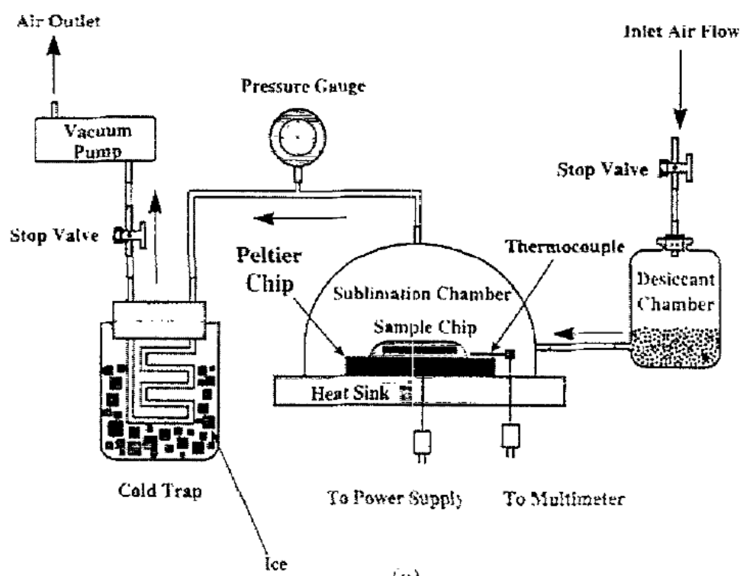


Figure 4-29: Sublimation apparatus used to lower temperature then lower pressure inside the chamber.[88]

4.2.3.4 Silanization

Silanization is the process by which a surface is covered by self-assembly with organofunctional alkoxysilane molecules which reduces the surface energy of the coated surface or makes the surface hydrophobic. This will reduce the capillary forces acting on the nanowires while drying as well as keeping the pillars from sticking together. Experiments were carried out to test whether silanization will keep the nano-pillar array from collapsing. Silanization was performed after etching the pillars to a depth of ~750 nm which is a height shorter than the critical height of collapse. The samples were coated with vapors from Sylon CT (Sigma Aldrich) for 3 minutes. Then, the samples were washed in isopropanol and dried. Pillar collapse in the silanized sample was compared with a control sample that was etched for the same amount of time using an SEM. Qualitatively, the results showed the same amount of pillar collapse in both samples, and hence, was not pursued further.

4.3 Increasing Surface Area per Unit Projected Area Through Unique Feature Geometry

The second component to increasing surface area per unit projected area is to change the geometry of the pillars to have larger perimeters. The motivation is to increase the perimeter without compromising stiffness, which would reduce the critical height of collapse. The geometry of the pillars will also affect the contact area between pillars during collapse. The goal is to keep the contact area small, so that there is less adhesion between pillars. The influence of changing geometry was validated by fabricating functional capacitor devices using nanowires with circular and diamond cross-sectional geometries, while keeping the pitch between neighboring pillars the same. The diamond cross section nanowires were fabricated using the template described in Section 4.1.4. Section 4.4 will introduce ultra-capacitors, their fabrication using nanowires, and the results of the comparison.

4.3.1 Other Unique Cross Section Geometries

The diamond cross section template was used to pattern the catalyst for MACE because that was the template available with large area patterns other than the templates with circles. Figure 4-36 shows some potential geometries that will increase perimeter without compromising stiffness. For example, the top left pattern is made from connecting four circles of the same size as the pillars fabricated in previous sections. If the perimeter of the original circles equals C per unit cell then the perimeter of the top left pattern is 5C per unit cell while the stiffness is approximately 100 times the stiffness of the circular cross section. The top right pattern is even more compact with the perimeter per unit cell being twice that of the circles.

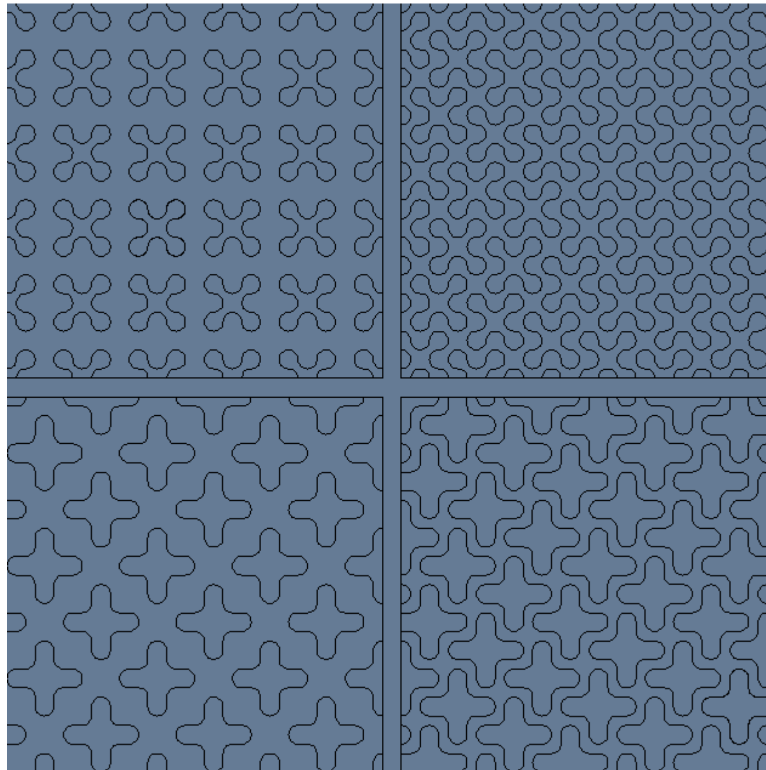


Figure 4-36: CAD drawing of potential high perimeter, high stiffness geometries for nanowires.

4.4 Using Ultra-capacitors to Validate the Increase in Surface Area per Unit Projected Area due to Unique Feature Geometry

4.4.1 Ultra-capacitor Background

Efficient energy storage is crucial for many applications such as the electric vehicle. Traditionally batteries have been used in electric cars because they have high energy storage densities but they lack fast charge/discharge rates as well as have shorter life cycles[90,91]. Capacitors are a potential replacement to batteries because they can deliver more power than batteries but they lack the energy storage densities of batteries [90,91]. Ultra-capacitors can combine the high power and long life cycles of traditional capacitors with the high energy storage density of batteries as shown in Figure 4-30. Current research is focused on increasing the energy density of ultra-capacitors by

increasing the surface area to volume ratio of the electrodes of ultra-capacitors.[91] More surface area means that there are more spaces for charges to reside which increases the energy storage density. This has been achieved in the literature by using forests of carbon nanotubes[92], as well as bulk porous silicon[93]. However, with both these materials, it is difficult to control the size distribution, including the diameter and height of carbon nanotubes, as well as the pore size for porous silicon. This has an effect on the size distribution of the gaps between neighboring electrodes, which ultimately drives the performance of the capacitor. If these gaps are too small, then the electrolyte in electrochemical double-layer capacitors (EDLC) cannot reach parts of the electrode, or the gaps are closed when performing atomic layer deposition (ALD) for electrostatic ultra-capacitors. If the gaps are too large, then the effective surface area to volume ratio is not maximized. These deviations from the norm reduce the effective surface area to volume ratio and hence, the overall storage density of the device. These two materials are also more difficult to integrate with silicon based electronics.[92]

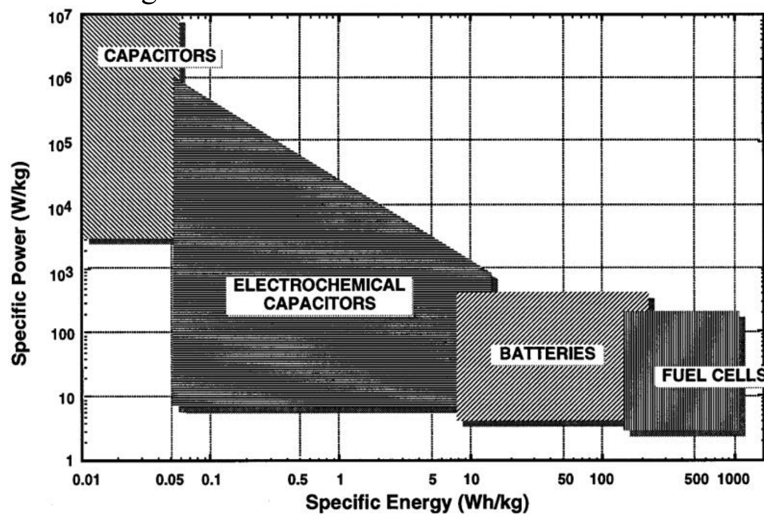


Figure 4-30: Plot showing the role of ultra-capacitors (electrochemical capacitors in image) in combining the positive features of both batteries and traditional capacitors[94]

In this study, the main focus will be to increase the surface area to volume ratio for ultra-capacitors by fabricating nano-scale high aspect ratio, high fill factor pillars with strict geometry control. Here, fill factor is defined as the ratio of the area of the feature to unit cell area defined by the pitch. It is believed that strict geometry control should lead to more robust performance of the ultra-capacitor by reducing the variance in the surface area per unit projected area.

Equation 4-9 is the basic capacitance equation for a parallel capacitor which shows the effect of increasing surface area, A. The surface area in the case of nanowires would be the area of the unit cell plus the feature height times cross section perimeter.[92]

$$C_{parallel\,plate} = \frac{A\varepsilon_0\varepsilon_S}{d} \tag{4.9}$$

A schematic of an EDLC with pillar electrodes is shown in Figure 4-31. As the capacitor material, Si can be highly reactive to the electrolytes used in capacitors and has surface traps that reduce the overall conductivity[26]. While these weaknesses can be mitigated by covering the silicon nanowires in graphene[12,26], better integration of the ultra-capacitors with electronics can be achieved by changing the capacitor type from an EDLC to a traditional electrostatic capacitor. Instead of storing charge in the electrolyte/electrode interface, charge can be stored in the electric field created by separating a metal such as tantalum nitride (TaN) deposited by atomic layer deposition (ALD) and the silicon nanowires with a dielectric such as aluminum oxide (Al_2O_3). Yujia Zhai et al used this method to fabricate metal-insulator-silicon nano-capacitors using the process flow shown in Figure 4-32. A similar process flow is described in Section 4.3.2 to compare the capacitances of different geometry pillars.[10]

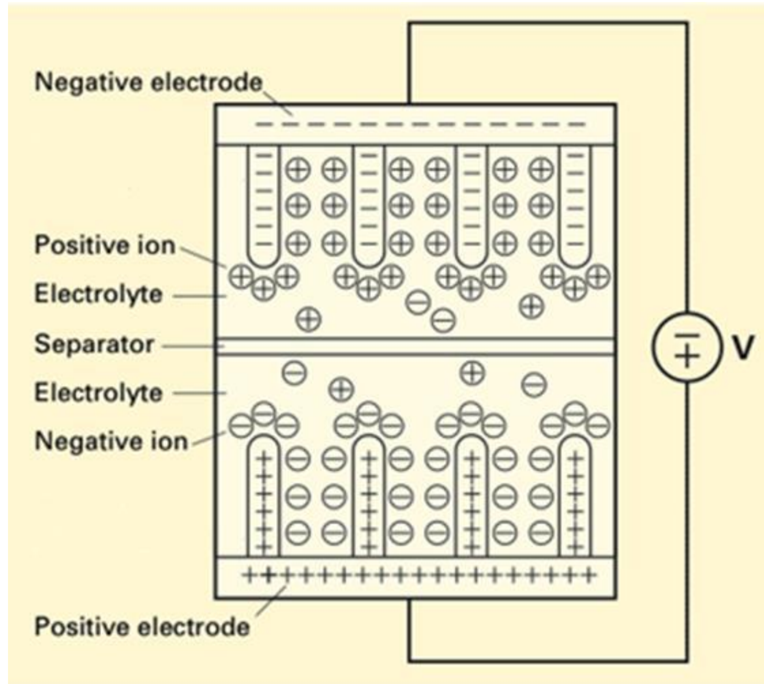


Figure 4-31: Schematic of an ultra-capacitor with nanowires which create more surface area.**

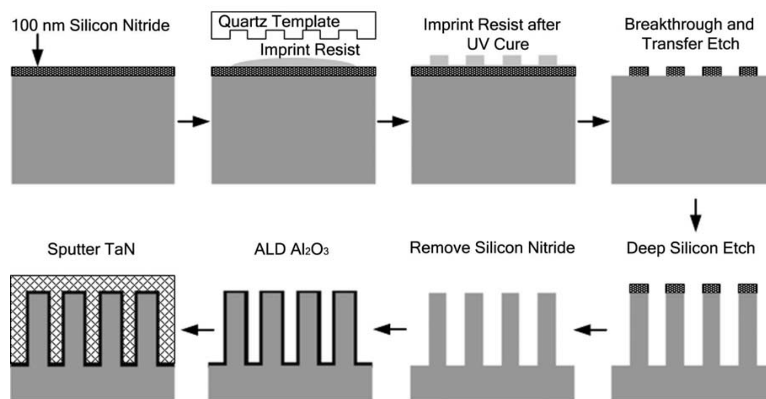


Figure 4-32: Process flow to fabricate metal-insulator-silicon nano-capacitors with nanowires.[10]

** modified from http://mitei.mit.edu/news/novel-ultracapacitor

4.4.2 Capacitor Fabrication

Metal-insulator-silicon nanowire based ultra-capacitors were fabricated by Akhila Mallavarapu using both the circular and diamond cross section pillars etched using the MACE process. Figure 4-33 shows the process flow used to create the capacitors after the MACE etch step and removal of the gold with an iodine based gold etchant. First, approximately 11 nm of hafnium dioxide, the dielectric is deposited using ALD. Then the gaps are filled with 50 nm of titanium nitride to be the second electrode. Aluminum was sputtered onto the backside of the wafer to create better contact for the measurements. The sample was divided into 300 μm by 300 μm capacitors by using photolithography to define separate samples for testing with a CV probe station.

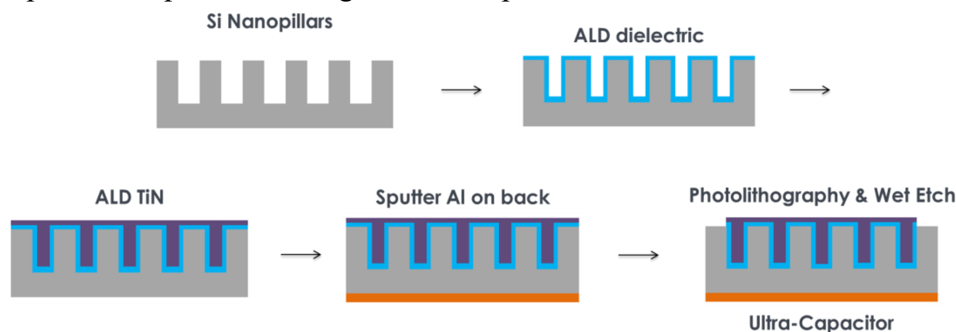


Figure 4-33: Process flow to fabricate an ultra-capacitor from nanowires.

4.4.3 Comparison of Capacitance for Circular and Diamond Cross Section Geometry

Circular cross section nanowire based capacitors were compared with diamond cross section nanowires capacitors to show that non-circular cross section pillars can increase surface area to project unit area and therefore the overall capacitance per unit area.

4.4.3.1 Analytical Calculations

The capacitance of a cylindrical nanowire based capacitor can be calculated using Equations 4.10-4.12. The planar capacitance accounts for the top of the pillars and the area be between pillars. The capacitance from the nanowire's sidewall is a function of its height (h) and the inner (a) and outer (b) radii of the dielectric ring as shown in Figure 4-34A. The equation accounts for the difference in surface area due to the dielectric thickness. For the capacitors with circular cross section, the projected area is 200 nm by 200 nm, a is 50 nm, and b is 61 nm. The dielectric constant used in the analytical calculations was back calculated using the parallel plate capacitor equation and data from a capacitor with known thicknesses. This was done because the method of deposition can influence the actual dielectric constant value compared to theoretical values. In the case of the diamond cross section shown in Figure 4-34B, the calculations were performed using the titanium nitride electrodes which are assumed to be pillars with circular cross sections of 100 nm radius. The projected increase in capacitance for a diamond cross section was calculated to be ~64%.

$$C_{unit} = C_{planar} + C_{cylinder} \tag{4.10}$$

$$C_{planar} = \frac{A_{projected}\varepsilon_0\varepsilon_S}{d} \tag{4.11}$$

$$C_{cylinder} = \frac{2\pi\varepsilon_0\varepsilon_S h}{\ln(b/a)} \tag{4.12}$$

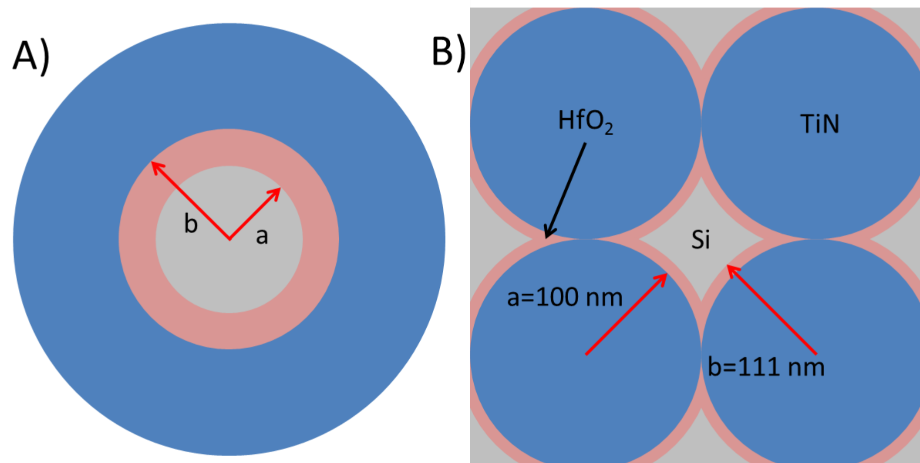


Figure 4-34: A) Circular cross section capacitor where a is the radius of the inner electrode and b is the radius of the outer electrode. B) Diamond cross section capacitor model with equivalent a and b.

Table 4-1: Calculated capacitances per unit projected area for circular and diamond cross section nanowire based capacitors.

	Circular Cross Section	Diamond Cross Section
C_{planar} (nF)	4.83E-07	4.83E-07
$C_{cylinder}$ (nF)	2.37E-06	4.21E-06
C_{unit} (nF)	2.85E-06	4.70E-06
$C_{total\ per\ area}$ (μF/ cm^2)	7.14	11.74
$C_{total\ per\ area\ per\ pillar\ height}$ (μF/ cm^2/nm)	12.62	22.24

4.4.3.2 Experimental Results

Forty capacitors of both types were measured using an Agilent B1500A CV probe station. As shown in Table 4-2, the capacitances vary significantly due to the variance in the etch depths across the wafer. Different etch rates occur because of differences in the nanoimprint RLT which result in feature height variations that change the catalyst mesh

during the gold deposition. Even though there are variations the averages of both the etch depths and capacitances, the data supports the claim that the diamond cross section will increase capacitance due to larger surface area per unit projected area. The experimental capacitances for both types of capacitors are lower than the calculated capacitances due to a change in the feature critical dimensions and other parasitics during the fabrication process. The capacitance per unit projected area of the diamond cross section capacitors are ~77.9% larger than the circular cross section capacitors. The increase is larger than expected which could be due to the effects of the sharp corners of the diamonds but this is outside the scope of the project. Figure 4-35 shows the average capacitances as the applied voltage changes.

Table 4-2: Results of experimental data collected of circular cross section versus diamond cross section capacitors.

	Circular Cross Section	**Diamond Cross Section**
Average Etch Depth (nm)	565.6	527.8
Standard Deviation of Etch Depth (nm)	166.9	150.5
Average Capacitance per Unit Area (μF/cm^2)	5.47	9.73
Standard Deviation of Capacitance per Unit Area (μF/cm^2)	1.69	2.13
Capacitance per Unit Area per Pillar Height (μF/cm^2/nm)	9.67	18.44

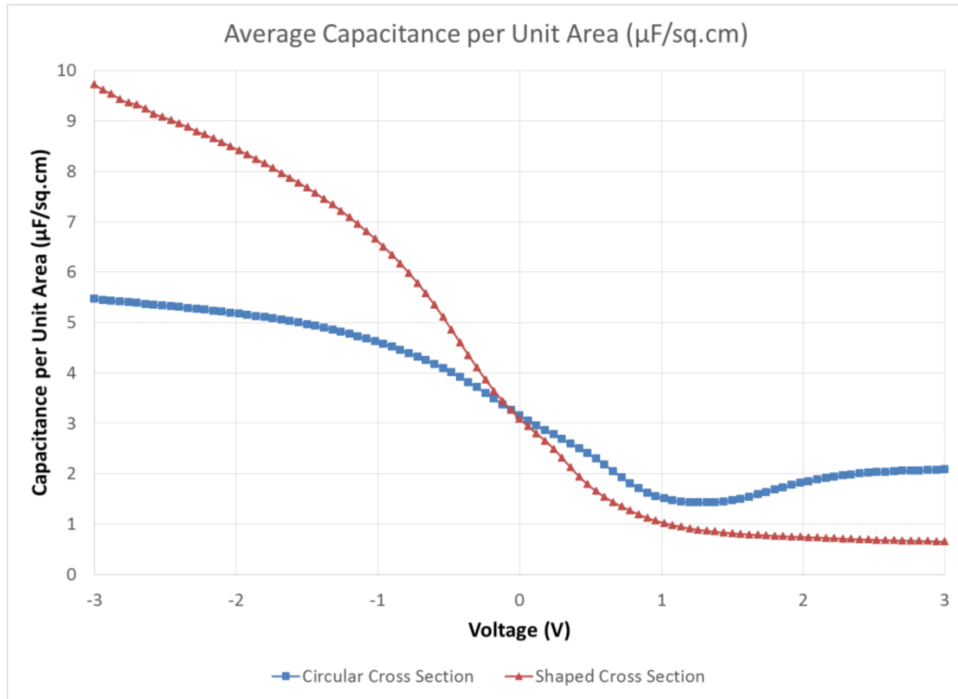


Figure 4-35: Experimentally obtained average capacitance per unit area for both circular and diamond cross sections (40 samples each).

Chapter 5: Conclusions and Future Work

5.1 Conclusions

In this work, two anisotropic wet etch processes have been studied to determine if they can produce dense high aspect ratio nanowires with controlled geometry over large areas, with the aim of enabling applications such as high energy density ultra-capacitors, that rely on increased surface area per unit projected area.

Imprint-enabled Crystallographic Orientation Dependent Etching (iCODE) of silicon with KOH leverages the etch stop (111) planes to define the final feature geometry. This etch process has been shown to be able to produce high aspect ratio trenches with (111) planes as the trench sidewalls but not high aspect ratio holes or pillars where the sides are defined by intersecting families of (111) planes. The limitations stem from the non-vertical (111) planes that limit the etch depth in the case of etching holes and the fast lateral etch rate of the edges where two (111) plane intersect and act like (110) and (100) planes in the case of pillars. In the literature, corner compensation techniques, wherein sacrificial features are added to the corners of the pattern so that the etch process can be timed to stop before the desired edge is removed, have been used to overcome the limitations due to the lateral etch. However, this technique is not viable for this work because the size of the added compensation feature is dependent on the desired etch depth, which drastically reduces the achievable feature density for high aspect ratio features. Hence, a method to protect the edges of the pillars from lateral etching was designed wherein rhombus shaped nanowires were attempted to be fabricated using two line-space patterning steps aligned to the vertical (111) planes on a (110) silicon wafer, with the second line-space pattern rotated by 70.53°. A protective SiO_2 sidewall was grown after etching the first set of sides for the nanowire. During the second etch, this sidewall transformed the vulnerable edge into a continuous (111) etch stop plane.

Unfortunately, after the etch process, the protective sidewall also led to the creation of pits with limited etch depth rather than the desired lines. Several methods were unsuccessfully attempted to selectively remove this sidewall, so the focus of this work shifted to using the Imprint-enabled Metal Assisted Chemical Etching (iMACE) process.

As opposed to iCODE, the iMACE process has been shown to be a viable method for producing large-area, dense, high aspect ratio nanowires. This process relies on a noble metal catalyzing the reduction of an oxidant which produces holes. The silicon underneath the metal oxidizes when these holes are injected through the metal which causes a preferential etch at the interface. The creation of dense, high aspect ratio patterns is largely dependent on two parameters – composition of the etch solution and fidelity and geometry of metal catalyst pattern. By controlling the proportion of oxidant to HF in the etch solution during the etching process, lateral etching is minimized by reducing the amount of excess holes that can diffuse to feature sidewalls. Perhaps most importantly, the metal catalyst needs to be patterned to create a continuous large-area mesh to bind the catalyst together and prevent it from etching in different directions. Several methods were investigated to fabricate a gold mesh starting from a large-area imprint lithography pattern. A bi-layer lift-off process using PVA as a sacrificial lift-off layer was shown to produce a mesh with the highest shape fidelity. This method was also shown to be compatible with pillars having non-circular, sharp-cornered cross sections, as long as the geometry of the shapes does not compromise the stability of the gold during the etch process i.e. folding or wrinkling. The sharp corners are retained even with the need to etch a small boundary around the gold edges to allow for the diffusion of the reactants to and products away from the metal/silicon interface.

A limitation of processing high aspect ratio pillars in solution is that they tend to collapse during drying when capillary forces overcome the bending stiffness of the

pillars. The collapsed pillars do not return to a vertical position if the adhesion energy between pillars is greater than the strain energy of the bent pillars. The collapsed pillars also have reduced effective surface area available for use in later processes. Avoiding feature collapse limits the depth to which the MACE process can be carried out, thus limiting feature height to approximately ~2 μm at about 100 nm half-pitch circular and shaped pillar structures. The ability to avoid feature collapse is dependent on the spacing between pillars, the second moment of inertia of the pillars, the surface energy, and the height of the silicon pillars. There are several methods discussed in the literature, such as critical point drying and sublimation, which have been used to mitigate capillary forces. However, these methods could not be translated directly to this work, because of prohibitive equipment limitations. The maximum height achieved with iMACE was ~14 μm but the feature collapse could not be completely avoided with sublimation drying or low surface tension fluids.

In addition to circular cross-section nanowires, the ability to etch pillars with unique non-circular shapes has also been demonstrated with iMACE. This can be useful towards further increasing surface area per unit projected area for increasing energy storage density in ultracapacitors. Metal-insulator-silicon nano-capacitors were fabricated on both circular and diamond cross-section nanowires. The diamond cross-section nanowires have an increase in capacitance per unit projected area of ~77.9%, compared to circular cross-section nanowires with similar etch depth. This increase in capacitance demonstrates the effectiveness of iMACE of non-circular shaped cross sections especially if feature collapse can be avoided and the etch depth increased.

5.2 FUTURE WORK

The iMACE process involves several unit steps that can be potentially improved for better process performance, reliability and scalability. For instance, a study can be performed to determine the optimum thickness of the PVA layer in conjunction with the subsequent isotropic etch needed to create an overhang for the gold deposition and lift-off. A custom wet etch apparatus can also be designed to facilitate the smooth exchange of the etch solution with water or another liquid for mitigation of feature collapse before the drying techniques are used. The overall cost of the iMACE process can also be decreased if the process can be modified by replacing the expensive plasma-based dry etch steps with relatively inexpensive solution-based or other etching steps. With an improved process, other applications that require high surface area to unit projected area such as thermoelectrics[6], biochemical sensors[7], and electronic devices[8,9], can be investigated. A variety of large perimeter, large moment of inertia geometries as shown in Section 4.3.1 can also be investigated by using e-beam lithography. Then, the geometries with the best performance can be made into imprint templates so as to push the limits of the high surface area to unit projected area using the iMACE process over large areas.

During this work, some phenomena were observed that can be potentially useful in the context of the iMACE process, but need to be investigated more thoroughly. One such phenomenon was observed when performing MACE on a sample that had been imaged previously using an SEM, where, quite unexpectedly, etching did not occur in the areas of the sample that had been imaged at high magnification. It was initially hypothesized that the residual charges on the surface recombined with the holes generated during the etch process which prevented the silicon from oxidizing and the etch process from initiating. Further investigation invalidated this hypothesis since the

phenomenon was also observed long after the charge should have dissipated. Other hypotheses that can be explored in future include the SEM charging caused the gold to separate from the silicon preventing the etch process from occurring or that the charging damaged the silicon underneath the gold.

Another phenomenon occurs when either the isotropic etch is insufficient to remove residue between the polymer pillars or the CHA deposition is non-uniform. These parasitics prevent the gold mesh from etching pillars but instead causes microporous silicon to form underneath the gold. The theory is that some form of contamination prevent the gold from fully contacting the silicon and prevent the mesh from moving down into the silicon. The gold mesh still reduces the oxidant so holes are still being injected into the silicon forming the microporous silicon.

Appendix: Details for Nanowire Fabrication using the Simplified Bi-layer Lift-off Process

Step 1) Clean 4” (100) Si wafers using a standard piranha clean (1:2 H_2O_2:H_2SO_4, self-heat for 5 min, clean wafers for 8 min, dry using SRD).

Step 2) Spin coat 4 wt% 31 kDa ~96 nm thick polyvinyl alcohol (PVA) onto wafer at 4000 rpm for 2 min and bake at 100°C for 2 min.

Step 3) Imprint nano-pillars with the desired cross section onto the PVA from a template that has the inverse tone using J-FIL™ (desired RLT is ~30 nm).

Step 4) Perform RIE using 5 sccm of O_2 and 20 sccm of Ar at a pressure of 15 mT, and a RIE power of 60 W for 92 sec (it is important to calibrate the etch rate first, since it may change with time).

Step 5) Deposit an adhesion layer of Ti (~2 nm) using an e-beam evaporator (max deposition rate of 0.3 Å/s).

Step 6) Deposit Au as the metal catalyst for the MACE process (~10 nm) using an e-beam evaporator (max deposition rate of 0.6 Å/s).

Step 7) Perform lift-off of Au by dissolving PVA in water and ultra-sonicating for 10 min.

Step 8) Perform MACE using a solution of 9:3:4 H_2O:H_2O_2:HF for 4.5 min for an etch depth of 1.6 μm.

Step 9) Remove gold by soaking in Gold Etchant Type TFA for 2 min.

Step 10) Dry using capillary mitigation technique.

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