**The Dissertation Committee for Tengfei Jiang Certifies that this is the approved version of the following dissertation:**

# MICROSTRUCTURE AND PROCESSING EFFECTS ON STRESS AND RELIABILITY FOR THROUGH-SILICON VIAS (TSVS) IN 3D INTEGRATED CIRCUITS

**Committee:**

Paul S. Ho, Supervisor

Rui Huang

Li Shi

Jang-Hi Im

Jie-Hua Zhao

# MICROSTRUCTURE AND PROCESSING EFFECTS ON STRESS AND RELIABILITY FOR THROUGH-SILICON VIAS (TSVS) IN 3D INTEGRATED CIRCUITS

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**Tengfei Jiang, B.E.; M.S.**

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# Dedication

To my parents

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# Microstructure and Processing Effects on Stress and Reliability for Through-Silicon Vias (TSVs) in 3D Integrated Circuits

Tengfei Jiang, Ph.D.

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Supervisor: Paul S. Ho

Copper (Cu) Through-silicon via (TSV) is a key enabling element that provides the vertical connection between stacked dies in three-dimensional (3D) integration. The thermal expansion mismatch between Cu and Si induces complex stresses in and around the TSV structures, which can degrade the performance and reliability of 3DICs and are key concerns for technology development. In this dissertation, the effects of Cu microstructure and processing conditions on the stress characteristics and reliability of the TSV structure are studied.

First, the stress characteristics of Cu TSV structures are investigated using the substrate curvature method. The substrate curvature measurement was supplemented by microstructure and finite element analyses (FEA) to investigate the mechanisms for the linear and nonlinear stress-temperature behaviors observed for the TSV structure. Implications of the near surface stress on carrier mobility change and device keep-out zone (KOZ) are discussed.

Second, via extrusion, an important yield and reliability issue for 3D integration, is analyzed. Synchrotron x-ray microdiffraction technique was introduced for direct measurements of local stress and material behaviors in and around the TSV. Local plasticity near the top of the via was observed which provided direct experimental evidence

to support the plasticity mechanism of via extrusion. An analytical model and FEA were used to analyze via extrusion based on local plasticity.

Next, the effect of Cu microstructure effect on the thermomechanical behaviors of TSVs is investigated. The contribution from grain boundary and interfacial diffusion on via extrusion and the relaxation mechanisms are discussed. Potential approaches to minimize via extrusion are proposed.

Finally, the stress characteristics of 3D die stack structures are studied using synchrotron x-ray microdiffraction. High resolution stress mappings were performed and verified by finite element analysis (FEA). FEA was further developed to estimate the stress effect on device mobility changes and the warpage of the integrated structure.

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# Chapter 1: Introduction

## 1.1. BACKGROUND AND MOTIVATION FOR 3D INTEGRATION

For nearly four decades, the semiconductor industry has been driven by Moore's Law to improve device density, performance, and performance-to-cost ratio. The success of the industry is largely built upon constant innovations in both device and interconnect technologies. Through technology advancements such as transistor scaling, implementation of strained Si technology, high-k plus metal gate technology (HiK-MG), and more recently, multiple gate field-effect transistors including FinFET, better device performance has been achieved [1]–[5]. Development in on-chip interconnect technology, such as replacing Al with Cu as the interconnection material, implementation of the dual damascene process, and the introduction of low-k materials, has also contributed to the improvement of chip performance [6]–[8]. However, beyond the 14 nm node, basic materials and processing issues have emerged to challenge Moore's Law, including increased interconnection RC delay, plasma damages, and the porosity limit of ultralow-k dielectrics. These problems are compounded by the growing demands for mobile computing which calls for high performance chips with smaller form factor, better power dissipation, and multiple functionality. This has led to the development of three-dimensional (3D) integration, a new integration scheme that can overcome the limitations of conventional 2D interconnect scaling to improve interconnect performance, device density, power consumption, and package form factor [9]–[13].

## 1.2. 3D INTEGRATION

In 3D integration, two or more thin dies are stacked and connected by through-silicon vias (TSVs), as illustrated in Fig. 1.1. Such a vertical integration scheme offers several advantages [14]–[16]. First, chip performance can be significantly improved with

an increased I/O count to reduce memory access time. Second, power consumption can be improved by reducing the interconnect wire length with vertical interconnects. Additionally, when multiple chips are stacked on top of each other, higher device density and functionality can be achieved with a smaller form factor. Finally, the concept of 3D chip stacking can potentially enable heterogeneous integration of chips with different functionality. This is illustrated in Fig. 1.2, where wafers of specific functions, such as processors, memories, MEMS, sensors, etc., can be separately fabricated and then vertically interconnected to create an integral functional device. Such an integration scheme has significant advantages over the system on chip (SoC) approach (Fig. 1.2b) in terms of cost, functionality, performance, and form factor [15].

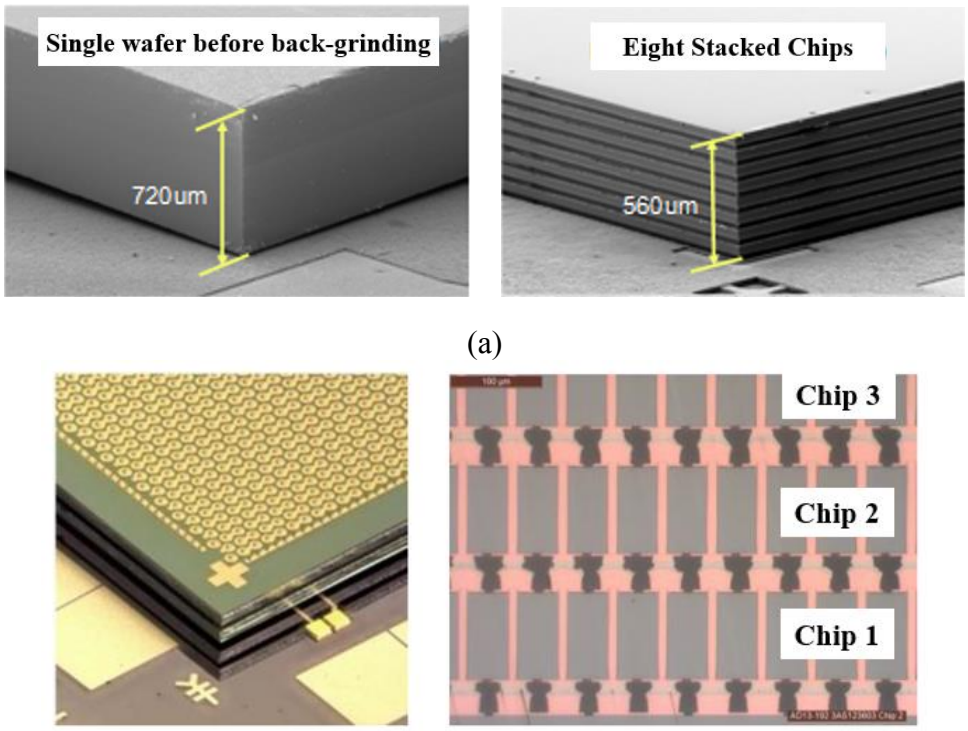



Figure 1.1. 3D integration by TSV. (a) SEM images of thickness comparison for a single wafer before back-grinding (Left) vs. stacking of eight chips (50 μm each) connected by TSVs and microbumps (Right). (b) Optical images showing a 3-die stacks and a cross-sectional view of three thin chips connected by TSVs and microbumps [14], [17], [18].

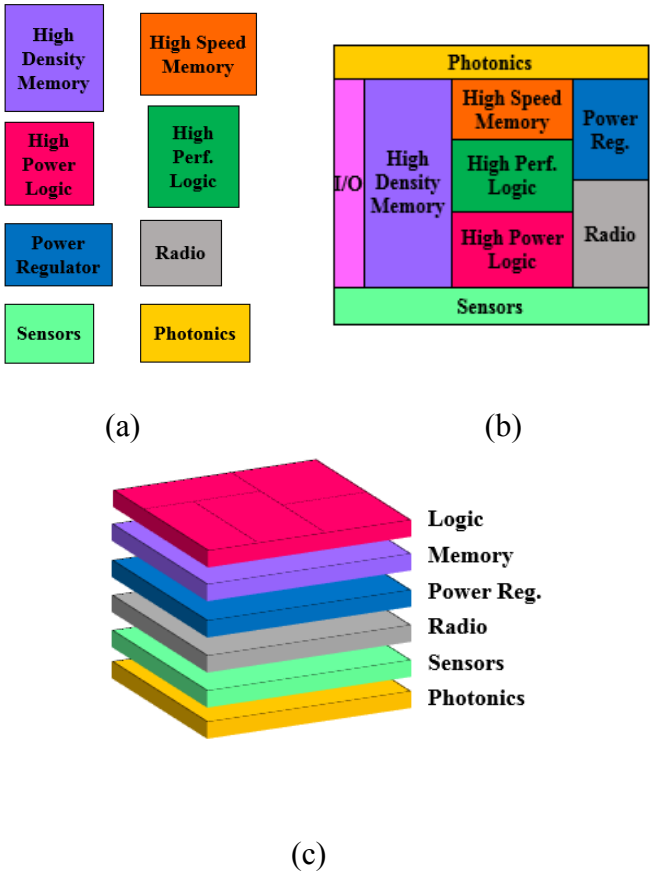



Figure 1.2. 3D stacking for heterogeneous integration. (a) Individual components. (b) System on chip (SoC) integration, where components of different functionality are integrated on a single chip. (c) 3D die stacking for heterogeneous integration where thin chips with different functionality are vertically stacked and interconnected. (adapted from [18])

## 1.3. THROUGH-SILICON VIA (TSV) TECHNOLOGY FOR 3D INTEGRATION

Through-silicon via (TSV) is a key element in 3D integration that enables vertical connection between thin dies. Cu has been widely used as via filling material due to its superior thermal and electrical performance, and its compatibility with the back-end-of-

the-line (BEOL) processes. The fabrication of Cu TSVs typically involves the following steps [14], [15], [19]–[22].

(a) Via etching. There are at least two ways to form the high aspect ratio (thickness/diameter) TSVs, namely deep reactive-ion etching (DRIE) and laser drilling. DRIE is more widely used as it can produce much smaller via holes. All TSVs fabricated are blind vias, as the vias are etched into Si with a depth a little more than the chip thickness after grinding, which is primarily determined by the application. Typically, for memory stacks, the thickness of chips ranges from 20 to 50μm, and for interposers, the thickness of the chips is 50 to 200 μm. The aspect ratio of TSVs is at least 5, and could be as large as 50. Scallops formed during DRIE by the Bosch process where the uniformity of via depth, undercut beneath the photoresist, selectivity of photoresist, and throughput are a few challenges for via etching.

(b) Deposition of a dielectric layer. To prevent current leakage and cross-talk of neighboring TSVs, a dielectric isolation layer, generally an oxide liner, must be present. For most 3D ICs, it is desirable to deposit the oxide layer at a relatively low temperature, typically 250-300˚C. Therefore, plasma-enhanced chemical vapor deposition (PECVD) is a commonly used method.

(c) Deposition of barrier and seed layers. To prevent contamination by diffusion of Cu into Si, a diffusion barrier layer is required before via filling. The most commonly used barrier materials are Ti, Ta, and their nitrides, which also serve as an adhesion layer for the subsequent Cu seed layer. Typically, physical vapor deposition (PVD) is used to deposit the metallic barrier materials (Ti or Ta) and Cu seed layers, while metalorganic chemical vapor deposition (MOCVD) is used for TiN or TaN deposition. It is important to achieve continuous coverage at the bottom and side walls of the TSV with optimized process parameters.

(d) Via filling by electroplating (EP). Void-free filling of high aspect ratio TSVs is critical for 3D IC technology, which requires superconformal, or bottom-up plating. Most commercial electroplating solutions are copper sulfate-based, which also contain additives serving as suppressors, accelerators, and levelers, although the exact chemistry of the electroplating bath is often kept confidential. Many factors can affect via filling, including chemistry of the electroplating solution, current density, quality of the seed layer, and feature dimensions. The electroplating parameters also affect the Cu microstructure in the via, although the effect has not been systematically studied.

(e) Removal of overburden. At the end of via filling by electroplating, a Cu overburden layer up to tens of microns thick can be left on the wafer surface. The overburden is removed by chemical-mechanical polishing (CMP), where slurry selection is important to minimize dishing in the via.

In Fig. 1.3, the fabrication flow for blind TSVs is illustrated, and in Fig. 1.4, SEM images corresponding to various steps in the via fabrication process are shown.

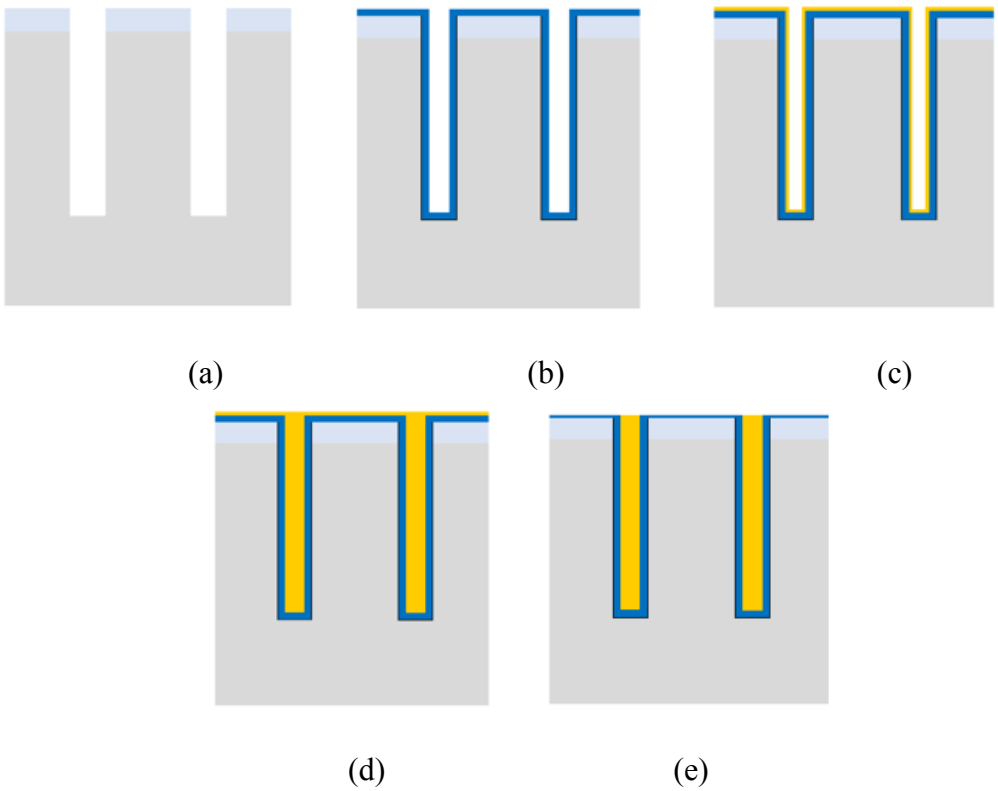



Figure 1.3. Illustration of TSV fabrication process. (a) deep reactive-ion etching (DRIE) to form via holes, (b) deposition of dielectric layer, (c) deposition of barrier and seed layer, (d) via filling by electroplating (EP) of Cu, and (e) CMP removal of overburden.

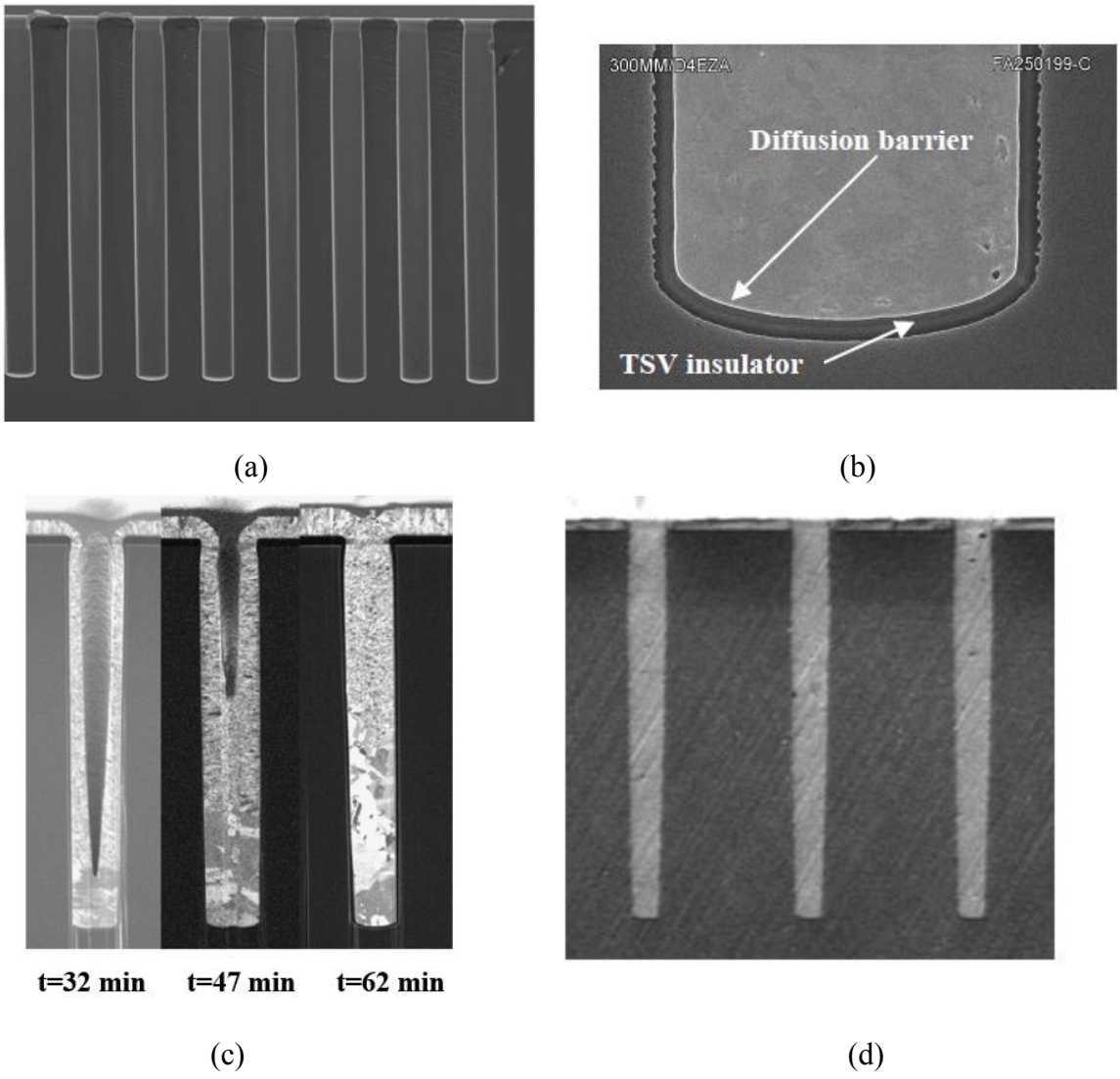



Figure 1.4. (a) DRIE of 5 × 50 µm (diameter × height) via holes. (b) A fully filled via showing the oxide liner (TSV insulator) and barrier layers at the bottom of the TSV. (c) Superconformal Cu filling of TSVs. (d) Blind vias after CMP removal of overburden. [23]–[25]

Depending on the sequence of the TSV fabrication relative to device fabrication, or the front-end-of-line (FEOL) process, there are three different, namely the via-first scheme, the via-middle scheme, and the via-last scheme [15], [22]. Currently, the via-middle scheme is most widely adopted, where the TSVs are made into the wafer after FEOL

devices are fabricated and before the starting of back-end-of-the-line (BEOL) interconnect layers process. Examples of TSV structure by via-middle proess are shown in Fig. 1.5.

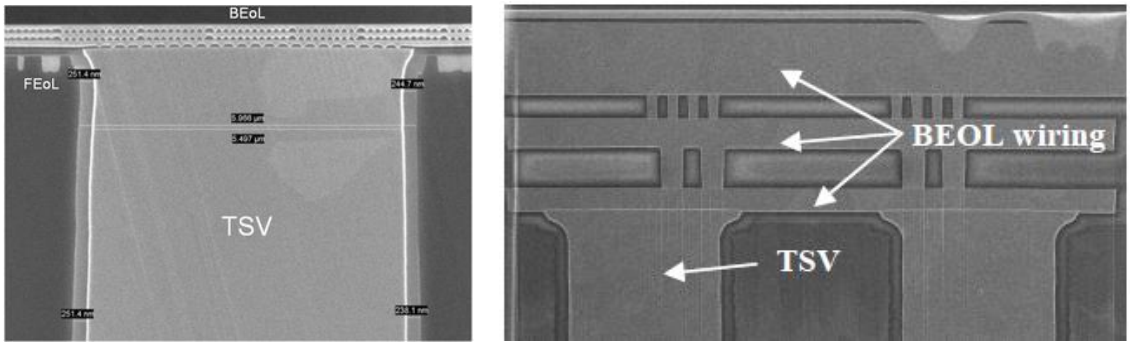



Figure 1.5. Two TSV structures fabricated by via-middle process with BEOL structures [24], [26].

After BEOL metallization, device wafers containing blind vias need to go through a few more fabrication steps to form chip stacks for 3D ICs. A typically integration process includes the followings steps [14], [15], [27]–[29]. The first step is front side bumping, which involves deposition and curing of a polymer passivation layer, deposition of under-bump metallization (UBM) layers, electroplating of microbumps, and solder reflow at about 250$^{o}$C. Next, the device wafer is bonded to a temporary carrier wafer for backside processing. The backside of the wafer is thinned down by back-grinding to a few μms before the TSVs. It is important not to expose the Cu vias during backside grinding to avoid Cu contamination. Instead, a Si etch-back process is used to reveal nails of Cu vias while they are still protected by the oxide liners. This is followed by the deposition of a SiN layer as passivation and a $SiO_2$ layer for CMP buffer. After the backside of the TSV is revealed by CMP, microbumps are formed using a process similar to that of the front side but without reflow. With bumps formed on both sides, the thin wafer is removed from the carrier wafer, mounted on a dicing tape, and diced. The die stacking is typically made by

thermo-compression bonding, where the bottom chip is attached to an organic substrate first, followed by attaching of upper chips one-by-one. The underfill can be pre-applied or a one-step underfilling process can be conducted to fill the gaps between the dies. Finally, the chip stack is encapsulated in epoxy molding compound (EMC), cured, and mounted on a PCB substrate with solder balls. The key steps of the die stacking process based on a via-middle scheme are illustrated in Figure 1.6.

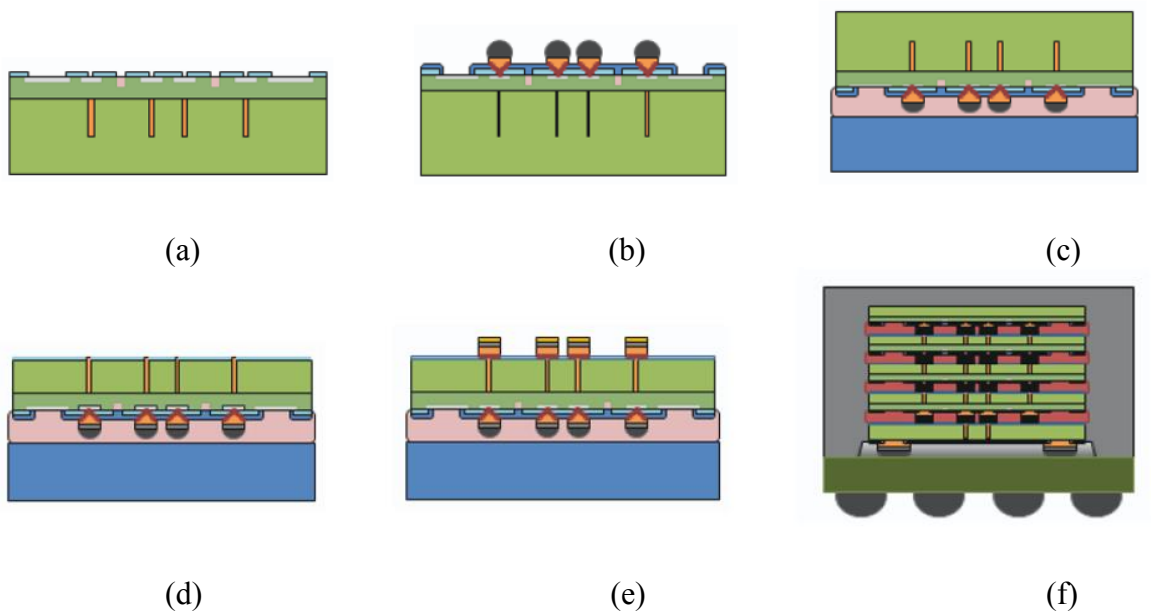



Figure 1.6. Fabrication of a 3D die-stack structure using the via-middle scheme. (a) BEOL metallization, (b) front side bumping and solder reflow, (c) mounting to a temporary carrier wafer, (d) wafer thinning and TSV reveal, (e) back side bumping, (f) die stacking by thermos-compression bonding and encapsulation by EMC [27].

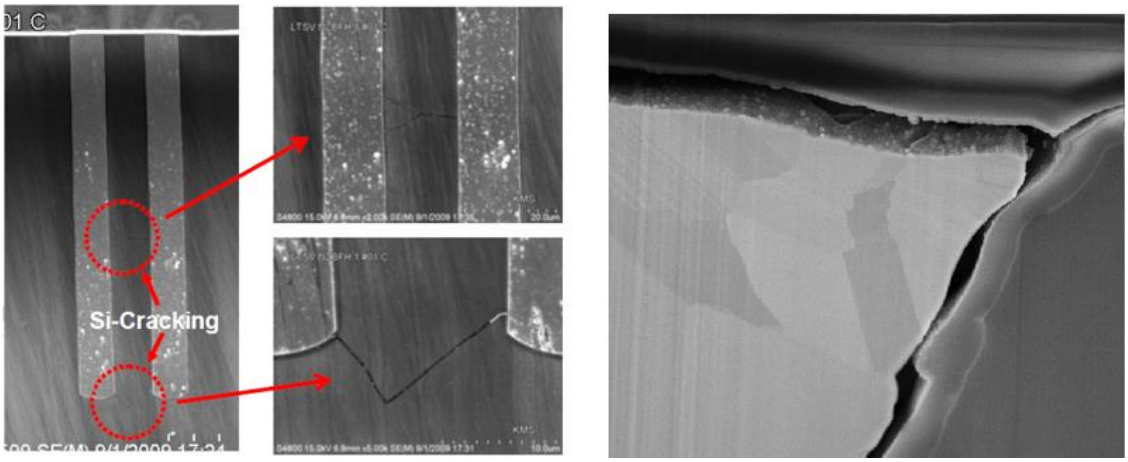
## 1.4. THERMAL STRESS AND RELIABILITY ISSUES FOR 3D INTEGRATION WITH TSVS

Thermo-mechanical reliability is an important issue for 3D ICs. Thermal stresses arise during various stages of 3D ICs fabrication due to the mismatch of coefficient of thermal expansion (CTE) among materials in the integrated system. For Cu TSV structures fabricated by via middle process, the large CTE mismatch between Cu ($\alpha$=17ppm/$^{o}$C) and

Si ($\alpha$=2.3ppm/$^{o}$C) develops considerable stress in and round the vias when the structure goes through temperature excursions during BEOL processes, sometimes reaching temperatures as high as 400$^{o}$C. Several yield and reliability issues have been reported for TSV structures, which are briefly reviewed below.

(1) Si cracking and interfacial delamination.

The thermal stress around the TSV can be large enough to cause cracking in Si and delamination at the via/Si interface. Examples of such failures are shown in Fig. 1.7.

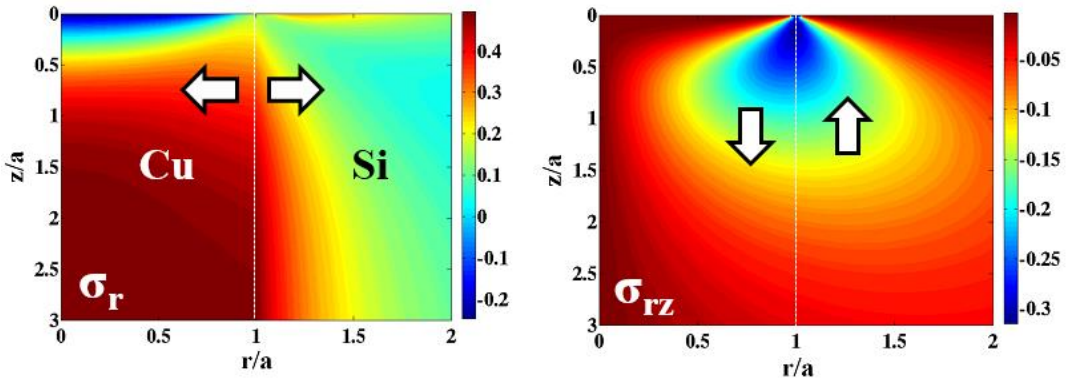



(a) (b)

Figure 1.7. Examples of reliability issues caused by stress in and around Cu TSVs. (a) cracking of Si. (b) Interfacial delamination. [19], [30]

The driving force for delamination was recently investigated where a semi-analytical solution was developed to describe the near-surface stress field of an isolated TSV embedded in the silicon wafer [31]. The results reveal non-uniform stress distribution in and around the via, and both radial and shear stresses act to drive interfacial delamination in a mixed-mode fracture (Fig. 1.8). The driving force for delamination is higher during cooling as the radial stress ($\sigma_r$) at the via/Si interface is tensile during cooling compared to

compressive during heating. In the same study, it was also found that reducing the via diameter, D, decreased the driving force for both Si cracking and interface delamination. Both failure modes have been observed previously [19].




(a) (b)

Figure 1.8. Near-surface stress distributions predicted by the semi-analytical solution for a thermal load ΔT= -250°C. (a) radial stress $(\sigma_r)$ and (b) shear stress ($\sigma_{rz}$). The stress magnitude is normalized by a reference thermal stress $\sigma_T = -E\varepsilon_T/(1-\nu)$ with $\varepsilon_T = (\alpha_{Cu} - \alpha_{Si})\Delta T$ [31].

(2) Device mobility degradation.

Due to the piezoresistivity effect, stress in Si, especially near the surface where transistors are located, can affect the carrier mobility to degrade device performance [32], as shown in Fig. 1.9. This requires a keep-out zone (KOZ) be defined around the TSV, where the placement of active devices should be avoided.

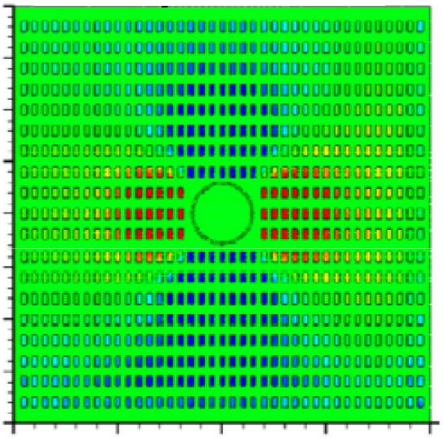
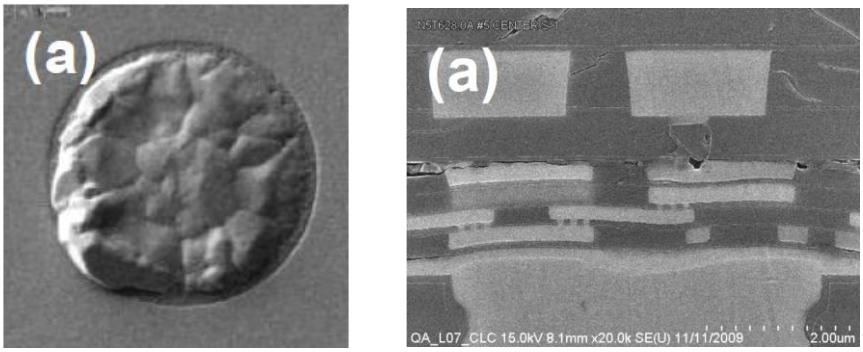


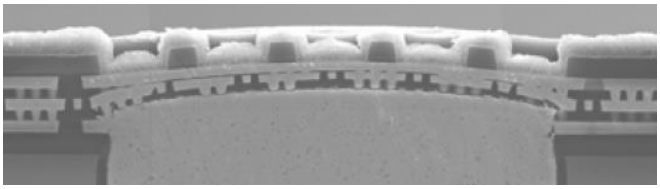
Figure 1.9. Mobility variation near a TSV [33].

(3) Via extrusion.

Via extrusion describes the irreversible vertical protrusion of Cu, which can deform the BEOL layers at the top of TSV to fail the interconnect lines, as shown in Fig. 1.10. Via extrusion is an important yield and reliability issue for 3D IC development, which is the subject of study in this dissertation.




(a) (b)



(c)

Figure 1.10. (a) Top view and (b) & (c) cross-sectional views of via extrusion [19], [34].

On the package level, CTE mismatch among the chip and the packaging components, such as the underfill, Sn-based micro-bumps, and the molding compound, as well as the thermos-compression process, can generate stress fields to affect circuit functionality and mechanical integrity of the 3D ICs. An example of such stress effect on circuit performance is shown in Fig. 1.11. For a 3D IC containing two dies, two digital-to-analog converters (DACs) modules that are located at different locations in the logic die (bottom die) show different amount of current deviation. Particularly, DAC1, which is located near the edge of the DRAM die (top die), showed significantly larger current shift, as a result of the larger stress field at that location [35].

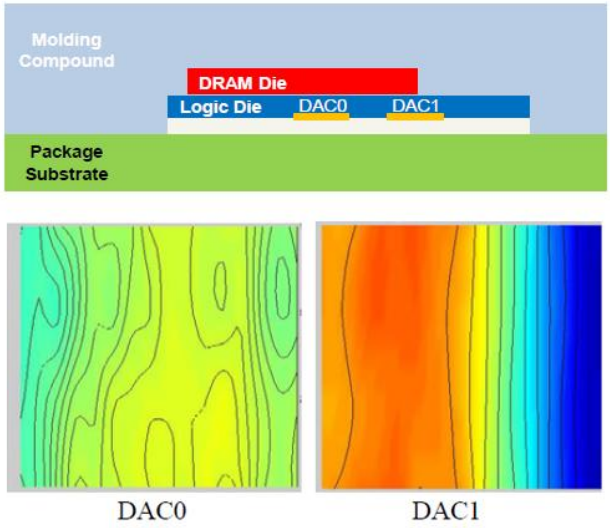



Figure 1.11. Currents deviation in two DAC transistor arrays in a two-die stack structure [35].

For 3D IC development, it is imperative to address the thermo-mechanical reliability issues. This in turn demands characterization of thermal stresses both in the TSV structures and in the 3D die stack structures. For process optimization, it is also important to understand and address the basic mechanism of stress-related reliability issues. These are the motivations of this dissertation.

## 1.5. SCOPE OF THE PRESENT WORK

In this dissertation, experimental measurements and modeling analyses are combined to study the stress characteristics and reliability for TSV structures and 3D die stacks. This dissertation is organized as the follows.

In Chapter 2, substrate curvature method is used to measure the stress characteristics of Cu TSV structures. To interpret the results, microstructure analysis by electron backscatter diffraction (EBSD) and modeling by finite element analyses (FEA) are performed. The distinct stress-temperature behaviors of TSV structures are discussed

and the implications of the near surface stress on carrier mobility and device keep-out zone (KOZ) are discussed.

Chapter 3 is focused on the via extrusion reliability. Synchrotron x-ray microdiffraction technique is introduced which has the unique capability to directly measure the local stress and material behaviors in and around the TSVs. An important finding from the synchrotron experiments is the local plasticity near the top of the via, which provides a direct evidence to support the plasticity mechanism of via extrusion. A simple analytical model is deduced along with FEA to analyze via extrusion during thermal cycling.

In Chapter 4, three different TSV structures are investigated and the effect of Cu microstructure on the thermo-mechanical behaviors of TSVs is discussed. Additional mechanisms for via extrusion, including the contribution from grain boundary and interfacial diffusion are discussed. Potential approaches to minimize via extrusion are proposed.

In Chapter 5, synchrotron x-ray microdiffraction technique is applied for stress characteristics of 3D die stack structures. High resolution stress mappings were obtained and the general behaviors of the die stack structure are analyzed by finite element analysis (FEA). FEA was further developed to estimate the stress effect on device mobility changes and the warpage of the integrated structure.

Finally, the main contributions of this dissertation are summarized in Chapter 6, and outlook for future work is given.

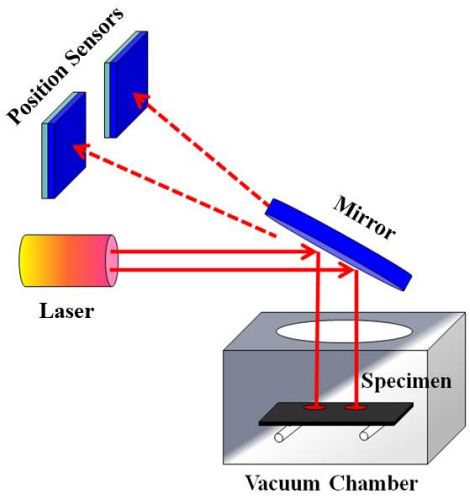
# Chapter 2: Thermo-mechanical Characterization of TSV Structures

In this chapter, the stress characteristics of Cu TSV structures are investigated. Substrate curvature method was used to measure the thermo-mechanical behavior of TSV samples during thermal cycling. The results were compared with electroplated Cu thin films to show the distinct triaxial stress characteristics of TSVs in contrast to the biaxial stress of thin films. The substrate curvature measurement was supplemented by microstructure and finite element analyses to investigate the mechanisms of the linear and nonlinear temperature-curvature behaviors observed for the TSV structure. The implication of the near surface stress on device keep-out zone (KOZ) is discussed.

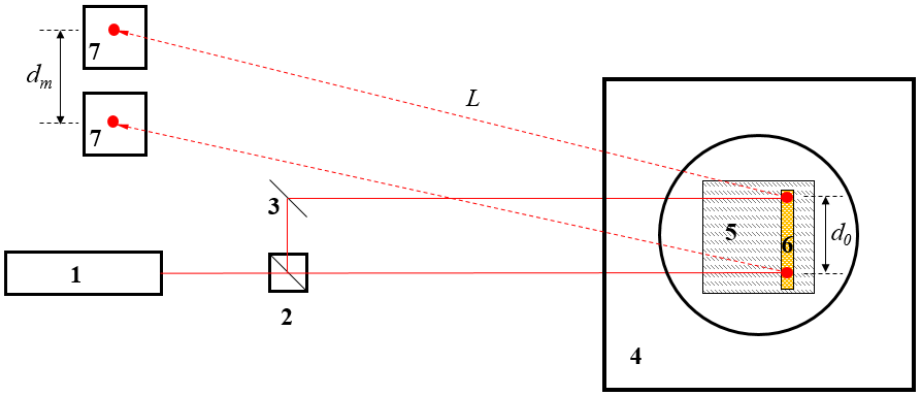
## 2.1. SUBSTRATE CURVATURE METHOD

The substrate curvature method uses an optical system to measure the bending of the sample induced by the stress. This method has been widely used for stress measurement of thin films and periodic line structures and was recently applied to TSV structures [36]–[41]. In this method, an optical system using a scanning laser beam or multiple beams is used to measure the radius of curvature of the sample [36], [37], [42], [43]. In Fig. 2.1a, such as system consists of an optical lever with two parallel laser beams is illustrated. The plan view of the optical path is shown in Fig. 2.1b with key components of the system numbered. A laser beam from the He-Ne laser (1) is split into two parallel beams by a beam splitter (2) and a mirror (3). The two parallel beams are reflected onto the sample by another mirror (not shown in Fig 2.1b), which also directs the reflected beams onto two position sensors. The sample stage is housed inside a vacuum chamber on a copper heating plate, which can heat the sample up to 450$^{o}$C. In a typical measurement, the chamber is evacuated and then backfilled with $N_2$ to a pressure of about 100 Torr to prevent oxidation of the sample. The system is capable of *in-situ* measurement of the sample curvature as a function

of temperature and time. The stage is designed to mount a sample in the shape of a beam, with a beam width of 3.5-5mm and beam length of 40-50mm. In this setup, only the bending along the beam length direction is measured. To induce a sample curvature during heating or cooling, the top and bottom halves of the sample need to have different amounts of thermal expansion, a requirement satisfied by most structures with a built-in asymmetry such as thin film on a thick substrate and the blind vias used in this study.




(a)




(b)

Figure 2.1. (a) Illustration of the substrate curvature system showing laser beams reflected by the sample onto photo sensors. (b) Plan view of the optical path of the measurement system. Key components of the system are: 1: He-Ne laser, 2: Beam splitter, 3: Mirror, 4: Vacuum chamber, 5: Cu heating plate, 6: Sample, and 7: Position detectors.

In the present setup, the distance between the two laser spots is $d_0$ and the distance between the sample and the position detector is $L$, which are calibrated to be $d_0$ = 3.5 cm and $L$=2.3m. Under thermal cycling, the sample bends and changes the distance between

the two laser spots on the detectors, $d_m$. Based on the geometry of the set-up, the curvature of the sample, $\kappa$, can be deduced as:

$$k = -\frac{d_m - d_0}{2d_0 L} \tag{2.1}$$

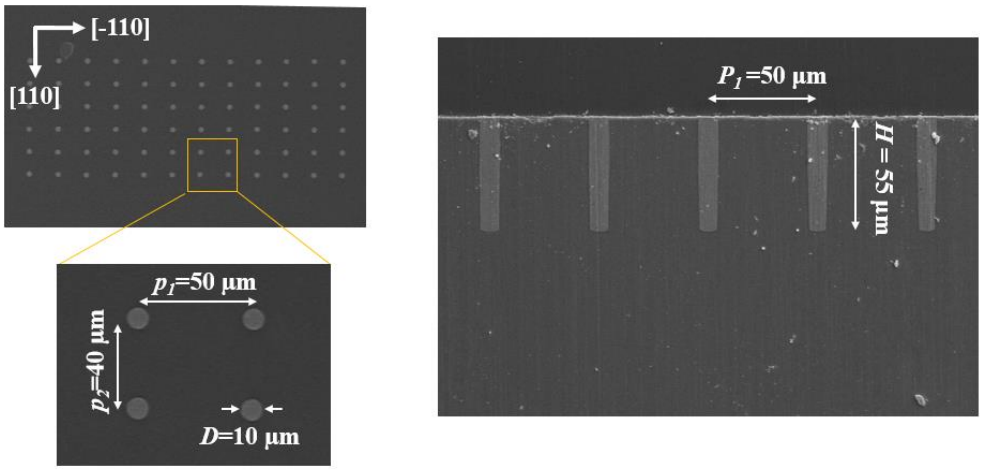
Given the resolution of the position detector of about 0.1μm, the resolution of the measured curvature can reach about $6 \times 10^{-7}$ $m^{-1}$ , corresponding to about 0.01 MPa change in thermal stress for a typical 1 μm film on a 760 μm Si substrate [43], [44]. The actual resolution of the measurement system is somewhat less due to factors such as vibration, temperature fluctuation, and lens aberration.

## 2.2. TEST STRUCTURE

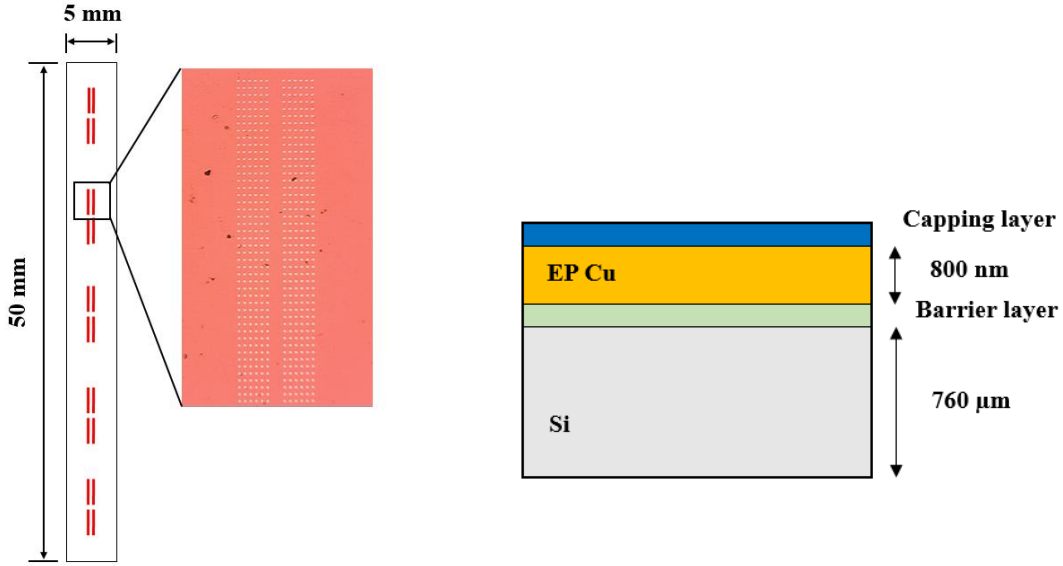
The TSV sample used for the curvature measurements was a blind via structure for which the TSV wafers were fabricated without thinning, leaving the TSVs embedded partially into but not completely through, the wafer. The TSV structure used for this part of the study will be referred to as TSV-A. For TSV-A, periodic patches of TSV arrays were patterned on (001) Si wafers which were 780 μm thick. The via diameter was 10 μm and the via height was 55 μm. At the via side wall, the thickness of the Ta barrier layers was 0.1μm and that for the oxide liner was 0.4μm. The vias were spaced 40 μm along the [110] direction and 50 μm along the $[1\bar{1}0]$ direction. The wafers had been annealed at 100ºC for 30 min after the TSVs were fabricated followed by chemical mechanical planarization (CMP). There was an oxide layer of 0.8 μm thick left on the wafer surface. The SEM images of TSV-A is shown in Fig. 2.2a.

The wafer was diced into 5 mm by 50 mm beams with the TSV arrays located near the centerline of the sample, as illustrated in Fig. 2.2b. The distribution of TSVs was

reasonably uniform across the sample, which allows relatively uniform bending of the sample during the curvature measurement. The volume ratio of Cu to Si was 0.015% for the TSV sample. The surface oxide was mechanically removed for the curvature measurements. The thin film sample used for comparison contained 0.8 μm electroplated Cu film electroplated on 780 μm Si wafer with a 20 nm TaN+Ta barrier/adhesion layer. There was a 50 nm SiN capping layer on top of the Cu film. The thin film sample was diced into 5 mm by 50 mm strips. The volume ratio of Cu to Si in the thin film sample was 0.103%. The measured curvatures of the thin film were normalized by the Cu volume ratio to facilitate comparison with the curvatures of the TSV structure. For both TSV and thin film structures, the diced strip was placed with the TSVs and Cu film facing downward in the chamber to allow laser reflections from the backside of the Si strip. In such a setup, the sign convention of the bending curvature is defined in Fig. 2.3. The curvature becomes more negative when the bottom side of the sample bends more.




(a)




(b) (c)

Figure 2.2. (a) SEM of TSV-A sample. (b) Illustration of the curvature sample for TSV-A. (c) Illustration of the curvature sample for the thin film structure.

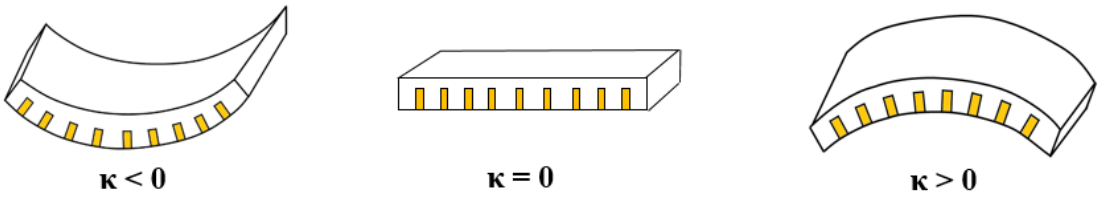
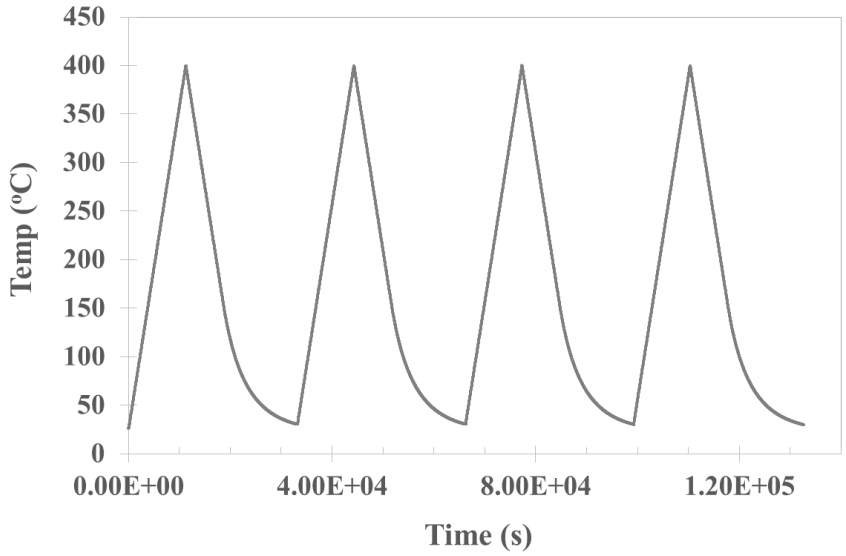



Figure 2.3. Sign convention of the measured curvature.

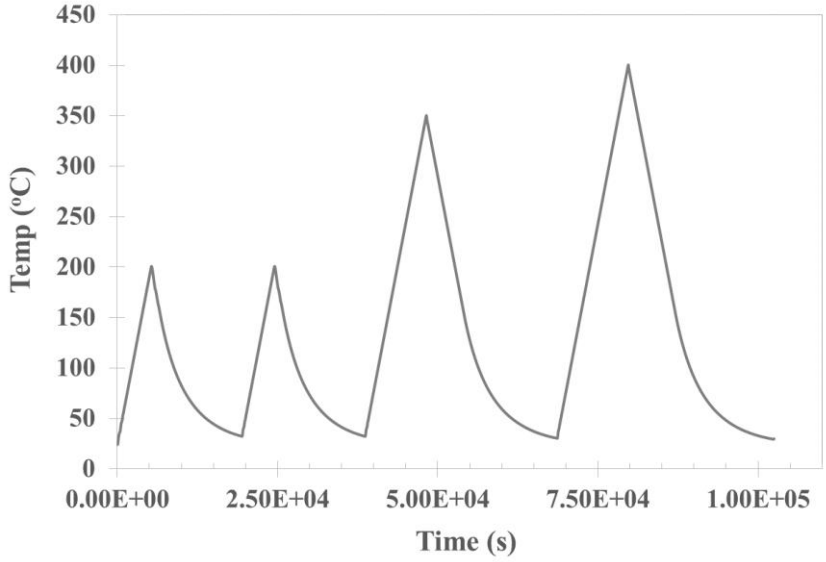
## 2.3. CHARACTERIZATION OF THE CURVATURE-TEMPERATURE BEHAVIORS OF TSVS

### 2.3.1. Curvature measurement

Curvature measurements were carried out under thermal cycling for both TSV-A and thin film structures. Two temperature-time (T-t) profiles were employed as shown in Fig. 2.4. In the first profile, the samples were thermal cycled from room temperature (RT) to 400$^{o}$C for 4 times. For the second profile, the samples were subject to four thermal cycles with the first two cycles between room temperature and 200$^{o}$C, followed by one cycle to 350$^{o}$C and another cycle to 400$^{o}$C. The heating rate was kept at 2$^{o}$C/min, and the cooling rate was initially at 2$^{o}$C/min then slowed down when the temperature was below 100$^{o}$C due to the limited cooling rate in the chamber. At the completion of the thermal cycling measurements, $HNO_3$ was used to remove the Cu in the vias and the Cu thin film from the substrate. The same strip without Cu was then measured again under identical thermal cycling profiles, and the curvature was subtracted from that previously obtained before Cu was etching off. A net curvature change, $\Delta\kappa$, obtained in this manner represented the thermo-mechanical behavior of Cu TSVs in the sample.




(a)




(b)

Figure 2.4. Thermal cycling profiles used for the curvature measurement. (a) four cycles to and from 400ºC. (b) two cycles to and from 200 ºC followed by one cycle to 350 ºC and 400 ºC.

The curvature behaviors measured for TSV-A and thin film after normalized by Cu volume under the first thermal cycling profile are plotted in Fig. 2.5. For the Cu thin film,

upon heating in the 1st cycle, the curvature decreased first linearly, then nonlinearly with temperature decrease (Fig. 2.5a). Also, the curvature changed from positive to negative as the stress in the film changed from tensile to compressive. During cooling, the negative curvature first decreased linearly, then nonlinearly at around 300°C. The curvature after cooling back to room temperature reached a slightly higher value than that before thermal cycling. In the 2nd cycle, the curvature decreased first linearly up to about 150°C, then nonlinearly. During cooling, the curvature overlapped that of the 1st cycle to form a hysteresis loop at the end of the cycle. The curvatures of the 3rd and 4th cycles showed a similar behavior and overlapped with that of the 2nd cycle. The shapes of the heating and cooling cycles were nearly identical except for the 1st cycle.

In comparison, the curvature of the TSV-A sample (Fig. 2.5b) showed a very different shape from that of the thin film. The curvature varied nonlinearly throughout the entire heating portion of the 1st cycle, which included a slight increase of the curvature in the latter half of the cycle. In contrast to heating, the curvature increased nearly linear during cooling, leading to a large positive value after cooling back to room temperature. The cooling curvature reached zero at around 325°C, indicating a zero averaged stress in TSVs at that temperature. In the 2nd cycle, the heating and cooling curvatures almost overlapped that observed during cooling in the 1st cycle. The behavior was similar in the 3rd and 4th cycles, almost overlapping with the 2nd cycle. At the end of the last cycle, the curvature was slightly larger than that after the 1st cycle. No hysteresis loop was discernible for TSV-A sample.

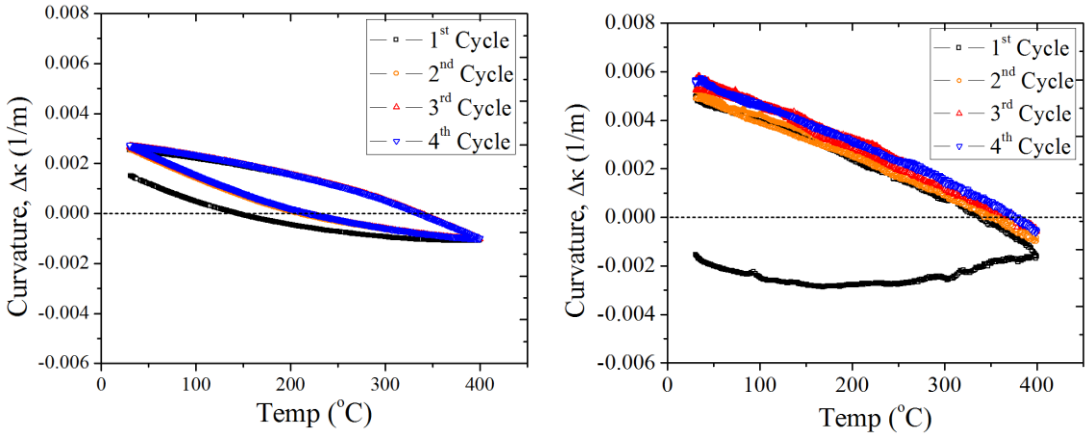



Figure 2.5. Curvature-temperature behaviors measured under the first thermal cycling profile for (a) electroplated Cu thin film and (b) TSV-A.

The curvatures of both TSV-A and the Cu thin film measured with the second T-t profile were shown in Fig. 2.6. For the thin film sample (Fig. 2.6a), the curvature behavior in the first 2 cycles formed a hysteresis loop, similar to that in Fig. 2.5b. In the 3rd cycle, the heating curve first traced that of the 2nd cycle up to 200°C, and then followed a nonlinear relaxation up to 350°C. During cooling, the curvature increased first linearly then nonlinearly, reaching a higher positive value at room temperature. In the 4th cycle, the curvature shape was similar to that in Fig. 2.5b, forming a hysteresis loop.

For TSV-A, as shown in Fig. 2.6a, the first two cycles resembled that of Fig. 2.5a where the curvature in the 1st cycle was nonlinear during heating and then linear during cooling. For the 2nd cycle, both heating and cooling curvatures were linear. In the 3rd cycle, the curvature first traced that of the 2nd cycle during heating, and then nonlinearly beyond 200°C. The cooling curvature was largely linear all the way to room temperature, leading to a room temperature curvature much larger than that of the 2nd cycle. Similar behavior was observed for the last cycle. For this sample, each time when the peak temperature

increased, the room temperature curvature after cooling increased and no hysteresis loop was observed.

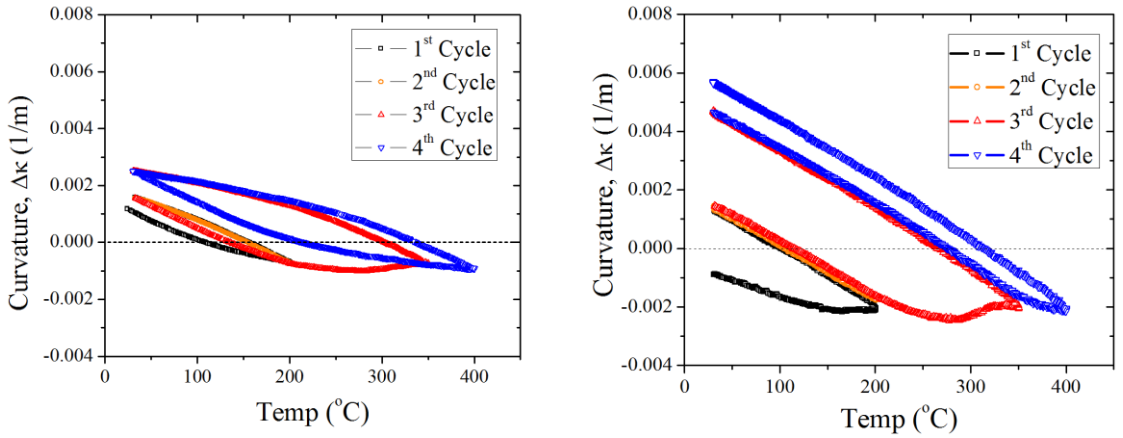



Figure 2.6. Curvature-temperature behaviors measured under the second thermal cycling profile for (a) TSV-A and (b) electroplated Cu thin film.

In another measurement for the TSV structure, the same temperature-time profile was used except that the heating rate was increased from 2°C/min to 6°C/min. The results from the two heating rates are shown in Fig. 2.7. The two plots closely resemble each other, indicating that heating rate has no apparent effect on curvature relaxation, therefore indirectly suggesting that creep is not a dominant mechanism for stress relaxation during heating.

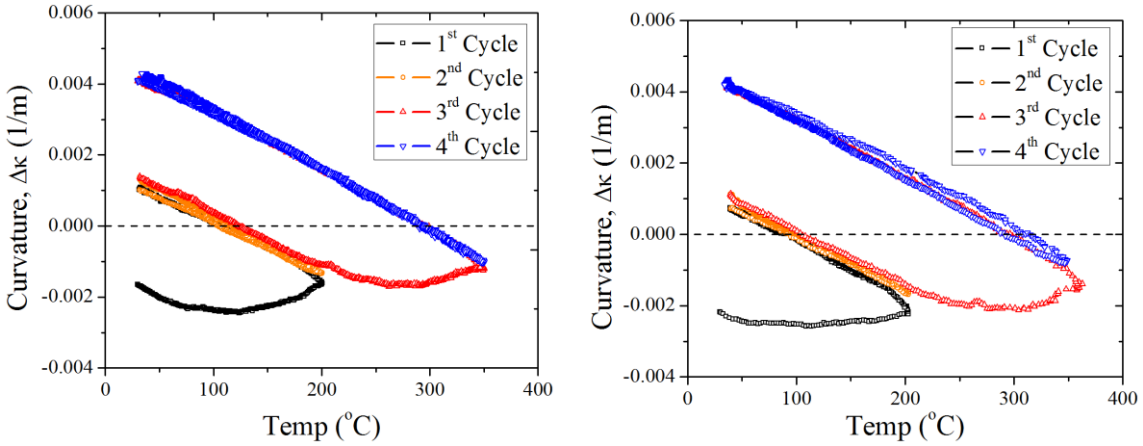
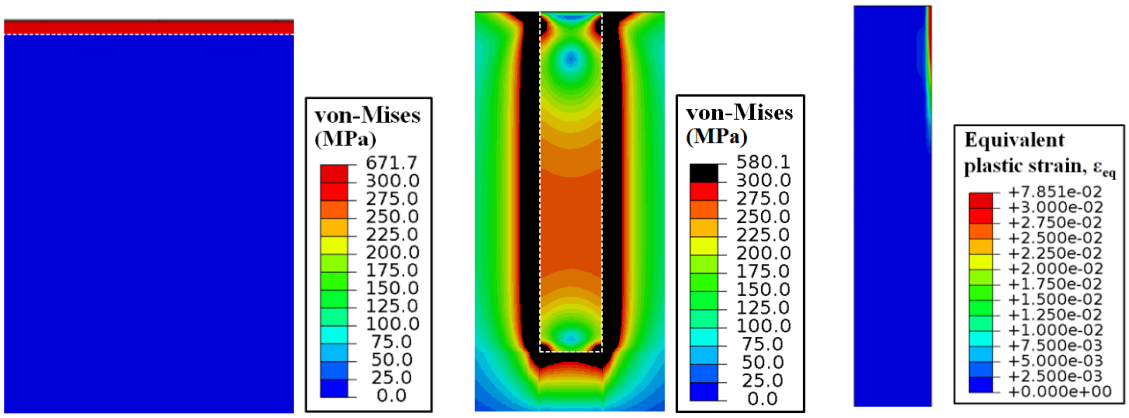



Figure 2.7. Effect of heating rate on curvature-temperature behaviors of TSV-A. (a) 2°C/min. (b) 6°C/min.

### 2.3.2. Stress analysis

One clear distinction between TSV structure and thin film was the curvature behavior during cooling. The cooling curves for TSVs were nearly linear, corresponding to a linear elastic behavior, in contrast to the hysteresis loops observed in thin films. To analyze the stress characteristics contributing to the different curvature behaviors, finite element analysis was performed for both structures. Three-dimensional (3D) models were built using a commercial software, ABAQUS (v6.12). For TSV structure, half of the via was modeled with symmetric boundary conditions in the [110] and $[1\bar{1}0]$ directions to simulate periodic via arrays. Linear 3-D solid elements (C3D8R) and fine meshes were used for the Cu via and thin film while an increasingly coarse mesh size going away from the via was used for Si. The material properties used in the model are: Young's modulus, $E_{Cu}$ = 110 GPa, $E_{si}$=130 GPa, and $E_{oxide}$ = 70 GPa; Poisson's ratio, $\nu_{Cu}$ = 0.35, $\nu_{Si}$ = 0.28, and $\nu_{oxide}$ = 0.16; the coefficient of thermal expansion (CTE), $\alpha_{Cu}$ = 17 ppm/°C, $\alpha_{Si}$ = 2.3 ppm/°C and $\alpha_{oxide}$ = 0.55 ppm/°C. First, stresses were calculated based on an elastic model assuming a thermal load of $\Delta T$ = -270°C, which corresponded to the cooling of the TSV

sample from 350°C in the 3rd cycle (Fig. 2.6a). The von-Mises stress, which is the effective shear stress driving plastic deformation, is plotted in Fig. 2.8.




(a) (b) (c)

Figure 2.8. (a) Distribution of von-Mises stresses for thin film and (b) distribution of von-Mises stress for TSV structures. (c) Equivalent plastic strain in the TSV.

The von-Mises stress calculated for Cu thin film was found to be uniform and biaxial due to the two-dimensional confinement of the Cu film by the Si substrate, as shown in Fig. 2.8a,. The yield strength, $\sigma_y$, of electroplated Cu is typically in the range of 150 MPa to 300 MPa, depending on the grain size [45], [46]. The result shows that the shear stress in the entire film exceeds yield strength as high as 300 MPa, therefore the entire film would undergo plastic deformation. The large-scale plasticity in the Cu thin film constitutes the major contribution to the formation of hysteresis loops during thermal cycles, as shown in Fig. 2.5a and 2.6a [39], [47], [48]. In contrast, the distribution of the von-Mises stress in the TSV was non-uniform, as shown in Fig. 2.8b. This can be attributed to the triaxial stress state in the via due to the confinement by the surrounding Si. For the thermal load used, the von-Mises stress in the via remains low less than the yield strength, except for the small

regions at the top and bottom of the via near the via/Si interface. Assuming a yield strength of 300 MPa, the plasticity would occur only in the regions colored black at the four corners of the via in Fig.2.8b. An elastic-plastic FEA model was further developed to show the localized nature of plasticity. A quarter via was modeled assuming Cu being perfectly elastic-plastic with a yield strength of 300 MPa. For $\Delta T = -270^{o}C$, the equivalent plastic strain in Cu was shown in Fig. 2.8c, clearly depicting the local plasticity. Since the volume fraction of Cu in the TSV sample was already small, the regions of localized plasticity within Cu vias was too small to deviate the overall curvature from elastic behavior. Overall, the Cu TSV sample behaved largely linear elastic during cooling so no hysteresis loop was observed. By comparing Fig. 2.8a and 2.8b, the occurrence of local plasticity is a key characteristic that distinguishes the TSV structure from thin films. The implications of local plasticity on via extrusion will be discussed in the following chapters.

### 2.3.3. Microstructure analysis

Both the TSV and thin film samples displayed nonlinear curvatures during heating. For the thin film sample, the curvature became nonlinear at a relatively high temperature following an initial linear region upon heating. Such a curvature behavior has been commonly observed for electroplated Cu thin films and is attributed to stress relaxation mechanisms such as plasticity and grain growth [48], [49]. For the TSV, the FEA in the previous section has excluded plasticity as an underlying mechanism to account for the observed stress relaxation. To understand the stress relaxation mechanism in the TSV sample, microstructure analysis was performed.

Several TSV-A strips were diced and polished using the method described in the previous section. Each sample was subjected to a single thermal cycle to a temperature,

with $T_m$= 100, 150, 200, 250, 300, 350, and 400$^o$C, respectively. The curvature-temperature behaviors were plotted for each $T_m$ in Fig. 2.9. Afterwards, focused ion beam (FIB) was used to cross-section the vias of the thermal-cycled samples as well as a control without thermal cycle for microstructure analysis. The focused ion milling was conducted in a FEI x835 DualBeam system. In the ion milling process, relatively large beam currents were used in the beginning for fast material removal and the beam current was decreased to a level of 50pA towards the end to minimize the damage to the final cross-sections.

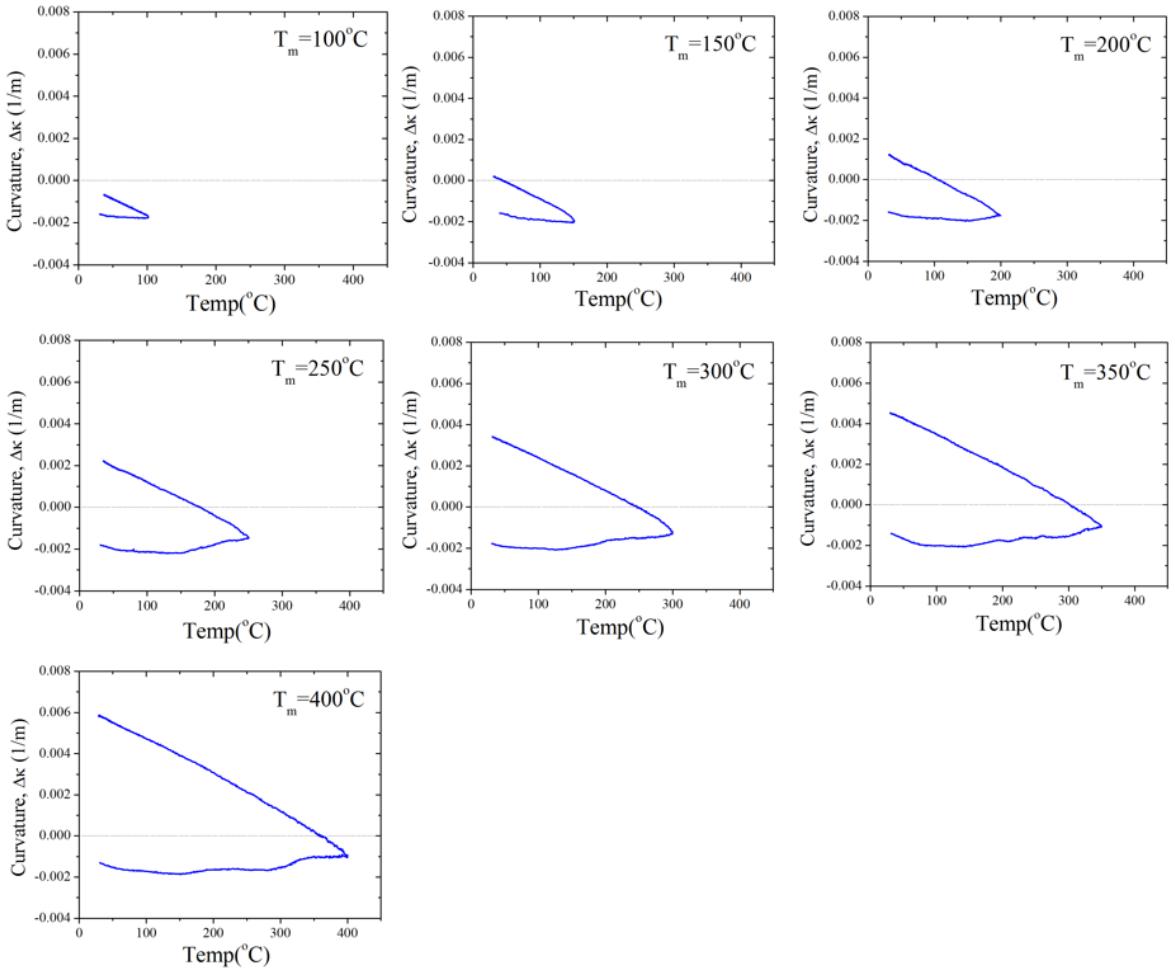



Figure 2.9. Curvature-Temperature behaviors of TSV-A subjected to single temperature thermal cycling tests.

The ion-induced secondary electron images of the via cross-sections are shown in Fig. 2.10, where grain contrast can be observed due to ion channeling effect. In the images, low index directions appeared darker because of the deeper ion penetration depth and the lower secondary ion yield for those low index directions [50]. The grain contrast show that the as-received via contained a large number of small grains, and the vias after thermal cycling to high temperatures (300-400ºC) contained relatively large grains. Qualitatively, Fig. 2.10 show a gradual increase of grain sizes from the as-received via, indicating grain

growth as the vias were thermal cycled to higher temperatures. In addition, small voids were observed, especially for vias thermal cycled to higher temperatures, which could be attributed to mass transport during grain growth.

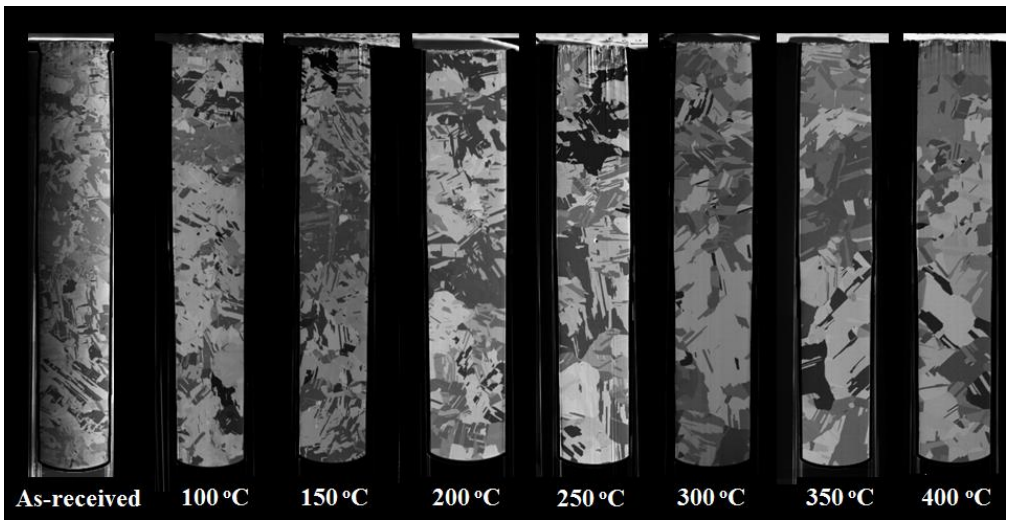



Figure 2.10. Cross-sectional FIB images of TSVs after single temperature thermal cycling measurements. The as-received sample is shown as a reference.

For quantitative analysis of Cu microstructure, electron backscatter diffraction (EBSD) measurements were carried out on the via cross-sections. An EDAX TEAM™ EBSD analysis system housed in a ZEISS Neon® 40 SEM was used for the measurement. The samples were placed in a SEM chamber and tilted at 70° with respect to the stage normal. For the measurement setup, the sample coordinates (RD, TD &ND) were defined in Fig. 2.11, where RD direction was parallel to the TSV axial direction, TD direction was along the via radial direction, and ND direction was normal to the TSV cross-section [51]. The via cross-sections were raster scanned by the electron beam at a step size of 0.1 μm, and the diffraction pattern from each point in the scan grid was collected by a phosphor

detector and automatically indexed with respect to Cu in the OIM$^{TM}$ Data Analysis software.

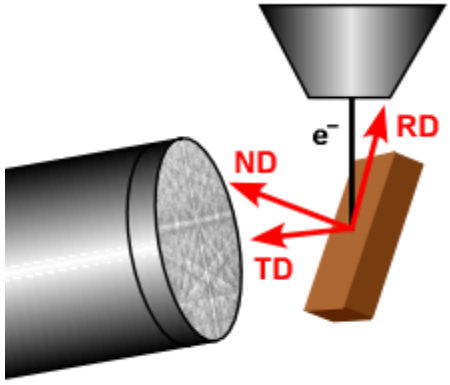
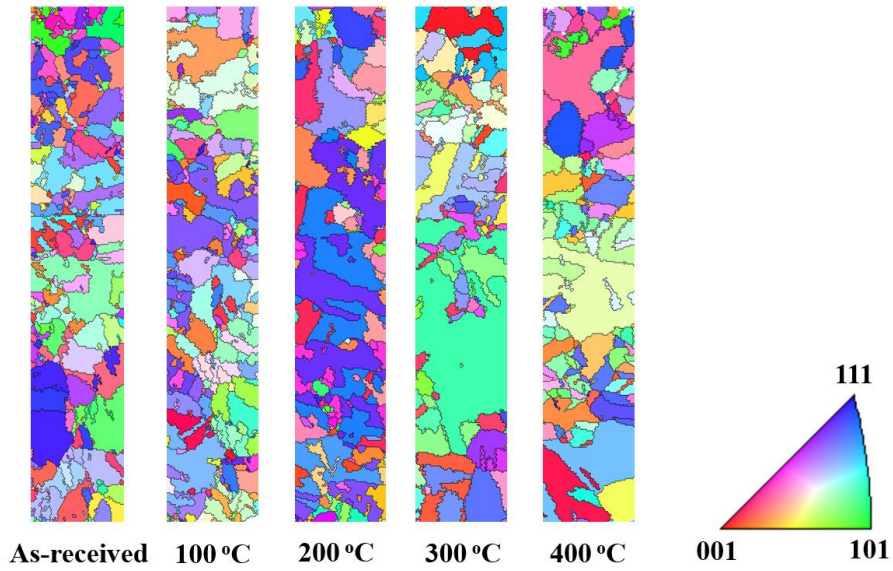



Figure 2.11. Sample coordinates (RD, TD & ND) in the EBSD system [51].

Based on the indexed data, crystal orientation maps along the via axial direction (RD) for the as-received and thermal cycled vias to 100, 200, 300 and 400ºC were shown in Fig. 2.12. Each color in the orientation map corresponded to a particular grain orientation according to the inverse pole figure. The average grain size for each sample was calculated and plotted in Fig. 2.12b.




(a)

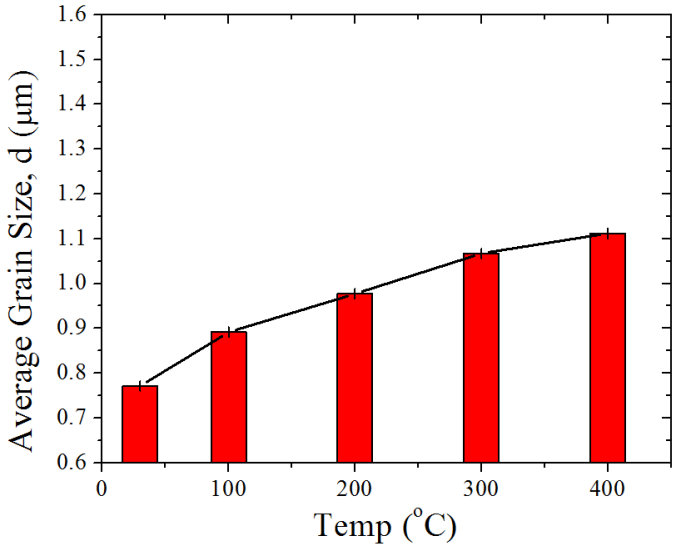
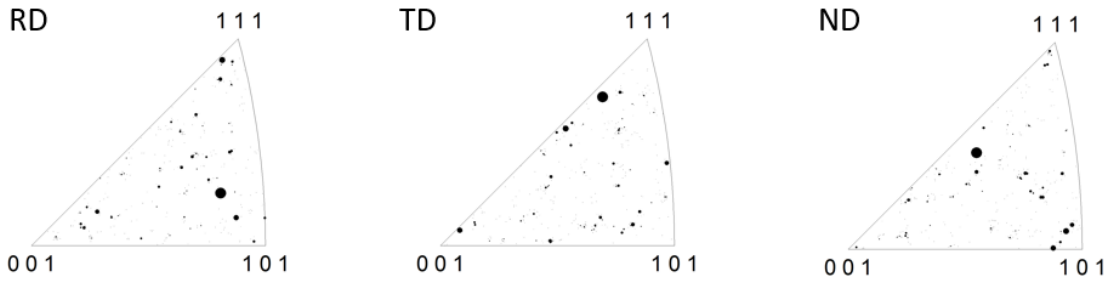



Figure 2.12. EBSD of the as-received via and vias after single temperature thermal cycling. (a) Crystal orientation map. (b) Average Cu grain size.

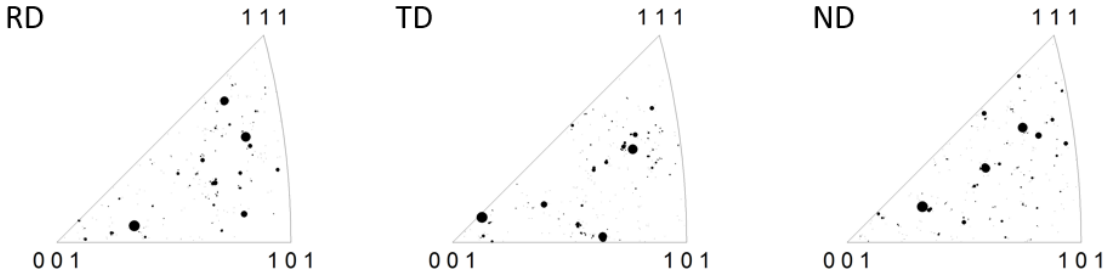
The average grain size for the via in the as-received TSV specimen was 0.77 μm. After thermal cycling to 100, 200, 300, and 400ºC, the average grain size has increased by 15.6%, 26.7%, 38.4%, and 44.2%, to 0.89, 0.98, 1.08, and 1.12 μm, respectively. Note that

the EBSD measurements in general overestimated the grain size, especially for small grains due to the discrete scan step and the limited resolution of the measurement system. Fig. 2.12b clearly showed grain growth in the via with increasing thermal cycling temperature. Grain growth is a known mechanism for stress relaxation which is commonly observed in Cu thin films, and can dominate the relaxation mechanism for the TSV structure as well [52], [53]. This will be further discussed.

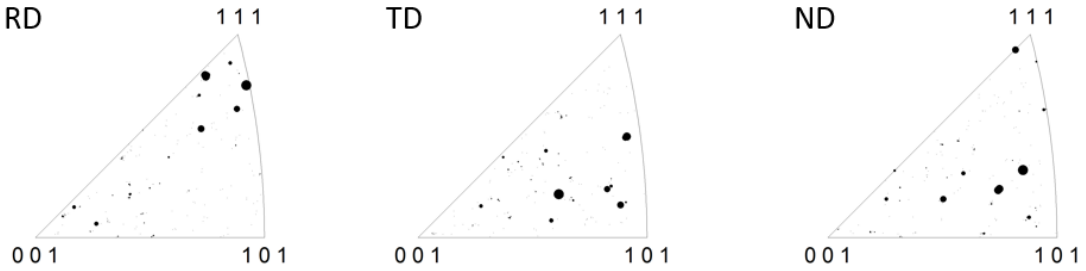
For all the vias measured, random grain orientations were observed. This was in agreement with studies reported by other groups [54], [55]. In Fig. 2.13, the inverse pole figures (IPFs) for the ND, RD, and TD directions were plotted for as-received and thermal cycled vias. The random grain orientation suggested a statistically isotropic Cu microstructure in TSVs both before and after thermal cycling.



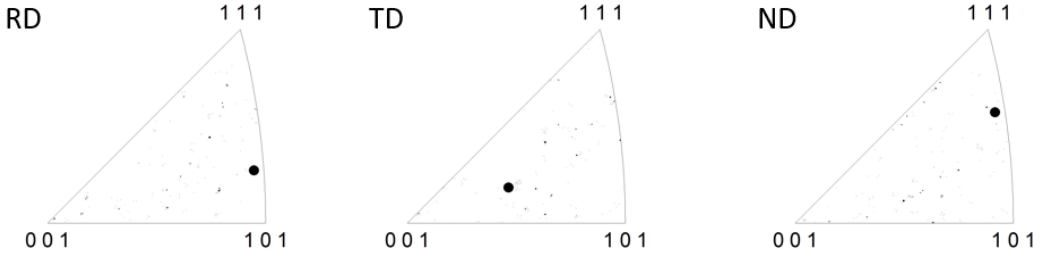

(a)



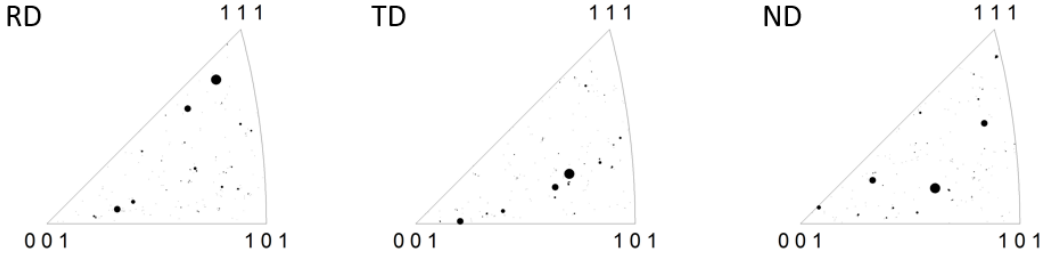

(b)




(c)




(d)




(e)

Figure 2.13. Inverse pole figures plotted along RD, TD, and ND directions for (a) the as-received TSV, (b)-(e) vias after thermal cycling to 100°C, 200°C, 300°C, and 400°C, respectively.

In all samples, it was found that a large number of boundaries were of Σ3 and Σ9 coherent boundary types, which are twin boundaries for Cu [56]. The fractions of each boundary types were summarized in Table 2.1. The results suggested that there existed a

large fraction of twin boundaries in both the as-received and thermal-cycled vias, independent of the peak temperatures the samples had been subjected to. This suggests that twinning had occurred during processing of TSVs and did not change under thermal cycling. Although twinning has been shown as an effective mechanism for stress relaxation in Cu thin films [48], it did not seem to contribute to the stress relaxation in TSV structures since the amount of twining remained relatively constant under thermal cycling. The presence of twin boundaries, however, can increase the Cu yield strength and affect other thermo-mechanical properties of the TSVs [56], [57].

Table 2.1. Percentage of Σ3 and Σ9 boundaries in the as-received and thermal cycled TSVs.

| | As-received (%) | 100ºC (%) | 200ºC (%) | 300ºC (%) | 400ºC (%) |
|---|---|---|---|---|---|
| Σ 3 | 62.5 | 64.0 | 69.3 | 70.1 | 60.3 |
| Σ 9 | 10.9 | 10.7 | 9.1 | 12.9 | 9.4 |
| Total | 73.5 | 74.7 | 78.4 | 83.0 | 70.0 |

## 2.4. DISCUSSION

### 2.4.1. Curvature-temperature behavior of TSV structures

The curvature-temperature behavior of TSV structures was distinctly different from that of Cu thin films, reflecting the unique thermo-mechanical characteristics of TSV structures. With stress and microstructure analyses, the curvature-temperature behavior of the TSV structure can be interpreted as discussed in this section.

The nonlinear curvature-temperature relation during heating of the first cycle can be primarily attributed to stress relaxation by grain growth. Similar curvature behaviors due to grain growth have been observed for Cu thin films [52], [53]. In general, grain

growth can eliminate grain boundaries and reduce the excess volume, so it is favored when the average stress in the Cu vias is compressive during heating [47]. The 3D confinement by the Si substrate induces a triaxial stress in the Cu via, in contrary to the biaxial stress in electroplated Cu thin film structure. As a result, local plastic deformation would occur primarily near the top and bottom of the vias, while most of the via remained elastic. During cooling, with the Cu grain structure stabilized, the vias behaved mostly linearly elastic during the cooling cycle. The combination of nonlinear curvature during heating and linear curvature during cooling led to the accumulation of a residual curvature and thus a residual stress at the end of the cooling cycle.

The magnitude of the residual curvature appeared to be directly related to the peak temperature in the heating cycle. In Fig. 2.14, the curvatures measured in the single temperature thermal cycling tests are overlapped into one plot. When the sample was thermal cycled to a higher temperature, the amount of relaxation was larger during heating, leading to a larger residual stress after cooling. By comparing Fig. 2.5a and 2.6a, despite the different thermal cycling history, the magnitude of the residual curvature appeared to be similar when the same peak temperature was reached. This was because grain growth, and thus stress relaxation, was largely dictated by the peak temperature in the heating cycle [58], [59]. In general, it is stress relaxation due to grain growth during the heating cycle that determines the residual stress in the TSV structure at the end of the cooling cycle. Fig. 2.14 also showed that slopes of the cooling curvatures were almost identical, suggesting that the elastic properties of the Cu vias were not affected by the grain growth, likely due to the isotropic grain orientation.

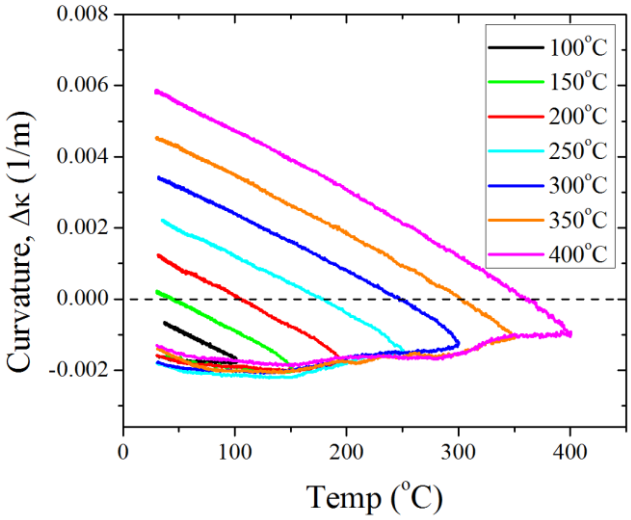



Figure 2.14. Curvatures for TSV samples subject to one time thermal cycling to temperatures between 100ºC and 400ºC.

In Fig. 2.15, the measured curvatures were converted to stress for both thin film and TSV structures for quantitative discussion of the residual stress. For thin film samples, the curvature can be converted to stress using Stoney's equation, as shown in Fig. 2.15b [43]. For TSV structures, an analytic solution is not available so FEA was used for the curvature conversion. The detailed procedure of the conversion can be found elsewhere [41], [60], and is briefly described here. A 3D model for a quarter of the beam sample was constructed with symmetric boundary conditions. The material properties were the same as those described in section 2.3.2 with Cu assumed to be isotropic and linear elastic. An average curvature was determined along the centerline of the beam for a thermal load of $\Delta T = 200^{o}C$. The rate of curvature change, $\Delta\kappa/\Delta T$, was calculated to be $\Delta\kappa/\Delta T = -1.88\times10^{-5}$ $m^{-1}/^{o}C$, close to the measured curvature change of $-1.47\times10^{-5}$ $m^{-1}/^{o}C$. A scaling factor, $\beta = \sigma_{xx}/\Delta\kappa$, was obtained from the model, which was then used to convert the measured curvature to stress.

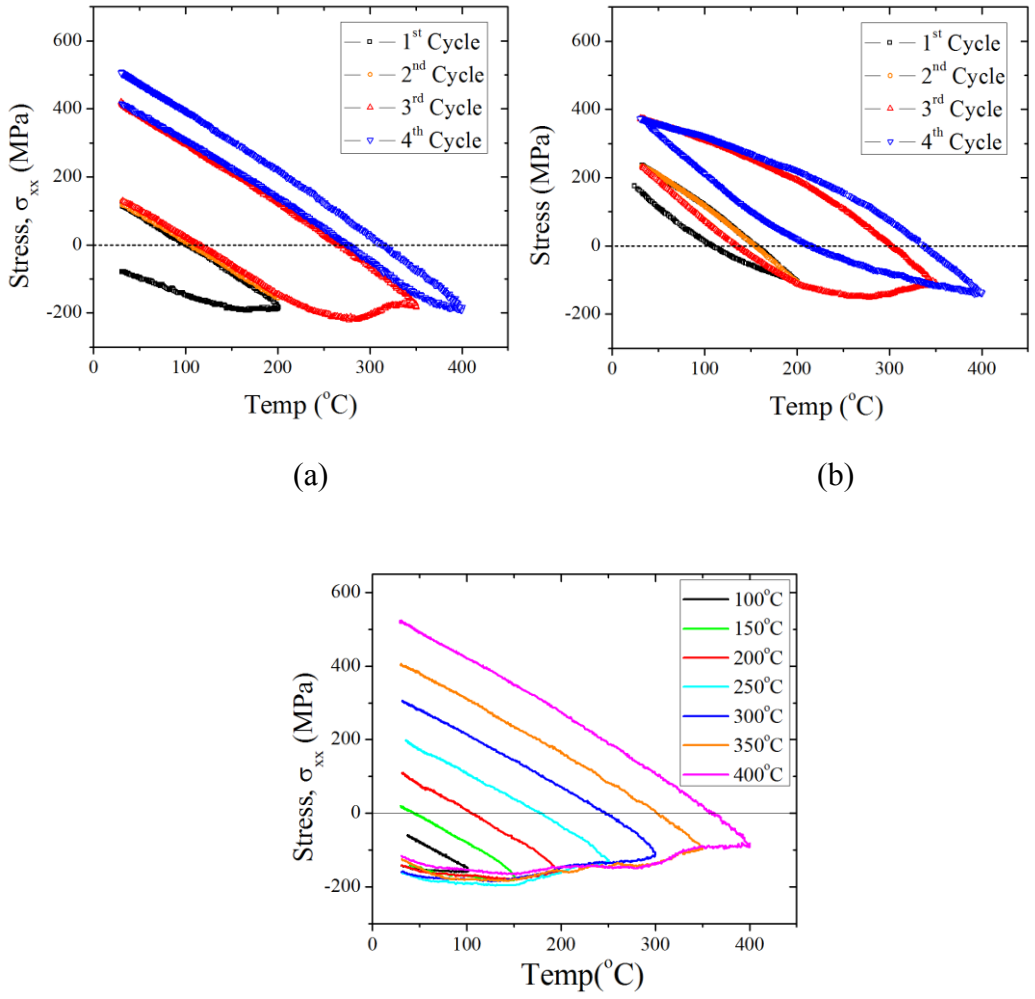



Figure 2.15. Stress-temperature behaviors of (a) and (c) TSV, and (b) thin film structures.

The residual stress in the TSV structure will increase when the TSV is subjected to heating under thermal cycling. For the thin film, while stress relaxation by grain growth during heating occurs, the presence of the large-scale plasticity during cooling significantly reduces the residual stress. The effect on the residual stress can be seen by comparing Fig. 2.15a and 2.15b, where the residual stress in the TSV was larger than that in the thin film after cooling from 400°C. Although the amount of stress relaxation during heating cycles

was about the same, the residual stress at the end of the cooling cycles were significantly higher for the TSV. Such a residual stress has direct impact on the device keep-out zone (KOZ) which will be discussed in the following section.

### 2.4.2. Residual stress and keep-out zone (KOZ)

The residual stress determined by the curvature measurement can affect the carrier mobility through the piezoresistivity effect of Si. This has important implications on the keep-out zone (KOZ) for CMOS devices near TSVs, an important reliability issue and design parameter for 3-D integration [61]–[65].

For (001) Si, assuming axis 1 along the [110] crystal direction of Si and axis 2 along the [-110] crystal direction of Si, the change of the drain current ($\Delta I_d$) and mobility ($\Delta\mu$) can be related to stress through the following relation [32].

$$\frac{\Delta I_d}{I_d} = \frac{\Delta\mu}{\mu} = -\frac{\Delta\rho}{\rho} = -(\pi_{11}\sigma_{11} + \pi_{22}\sigma_{22}) \tag{2.2}$$

In Eq.2.2, $\pi_{11}$ and $\pi_{11}$ are the piezoresistance coefficients Si, which has been transformed into the coordinate system defined above. The coefficients have different values for NMOS and PMOS as listed in Table 2.2. The out-of-plane stress was dropped in deriving Eq. 2.2 since the active devices were located close to the wafer surface.

Table 2.2. Piezoresistance coefficients for <110> channel NMOS and PMOS in unit of (%/GPa).

| (001) wafer | Horizontal | Vertical |
|---|---|---|
| (%/GPa) | $\pi_{11}$ | $\pi_{22}$ |
| <110> NMOS | -31.05 | -17.45 |
| <110> PMOS | 71.8 | -66.3 |

For <110> channel CMOS devices, the devices with the channel direction along the radial direction of the Cu TSV are defined as horizontal devices, and the devices with the channel direction along the tangential direction of the Cu TSV are defined as vertical devices. This is illustrated in Fig. 2.16.

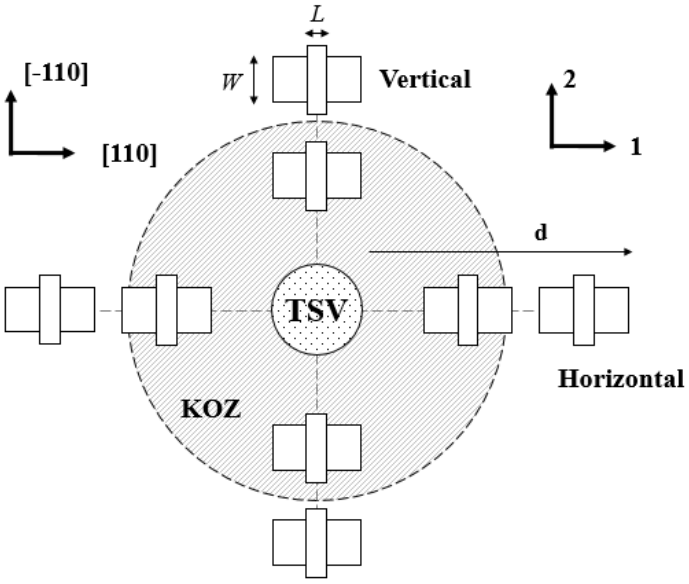



Figure 2.16. Illustration of the coordinate system and MOSFET placement. *L* and *W* are the gate length and width, respectively. The shaded area indicates the KOZ. *d* is the distance away from the TSV, with the periphery of the TSV at d=0.

A linear elastic FEA model was constructed to analyze the KOZ. Anisotropic elastic properties of Si were considered and a thermal load of $\Delta T = -250^{o}C$ was used in the model. The distribution of the in-plane normal and shear stresses is shown in Fig. 2.17. For the vertical and horizontal CMOS devices, $\sigma_{11}$ and $\sigma_{22}$ are plotted as a function of the distance from the TSV in Fig. 2.18.

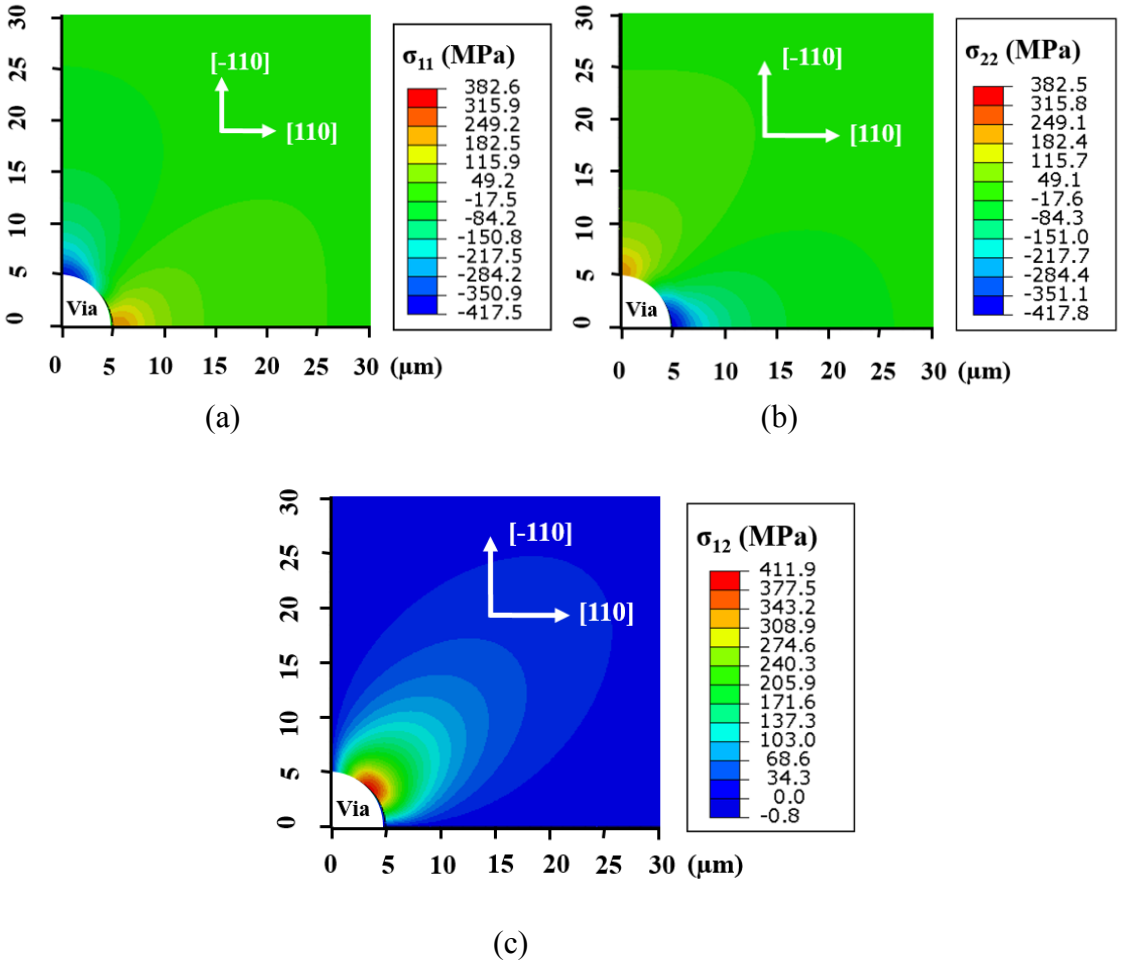



Figure 2.17. Contours of in-plane stresses. (a) normal stress, $\sigma_{11}$. (b) normal stress, $\sigma_{22}$. (c) shear stress, $\sigma_{12}$.

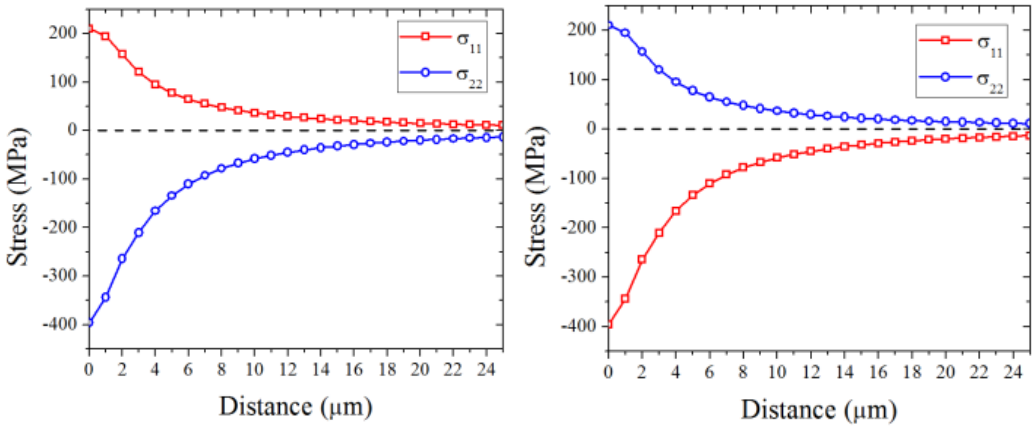
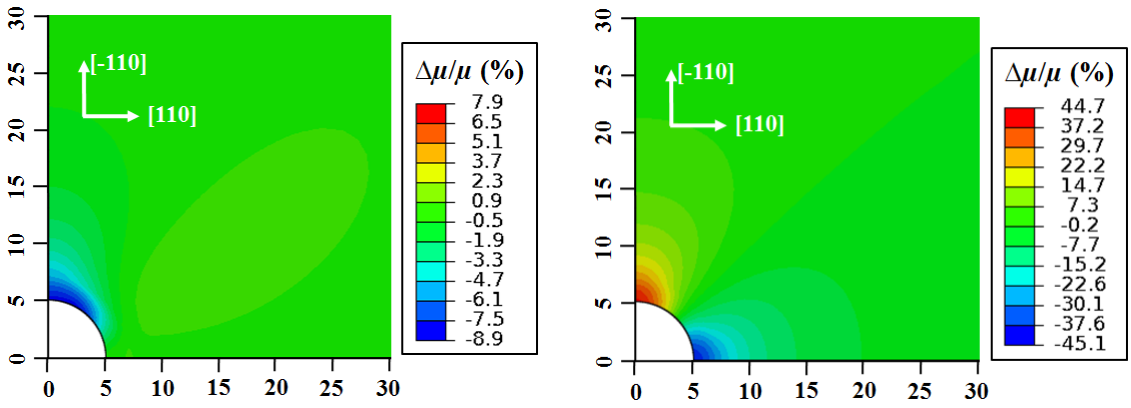



Figure 2.18. $\sigma_{11}$ and $\sigma_{22}$ as a function of distance from the TSV for (a) vertical and (b) horizontal CMOS devices.

From both Fig. 2.17 and Fig. 2.18, it was clear that $\sigma_{11}$ and $\sigma_{22}$ have opposite signs for the vertical and horizontal direction and are not symmetric. Eq. 2.2 indicates that the mobility change depend on the two normal stress components, $\sigma_{11}$ and $\sigma_{22}$. Therefore, it is expected that the resulting mobility change will be different for the vertical and horizontal directions.

For NMOS and PMOS, the contours of mobility change ($\Delta\mu/\mu$) were calculated and shown in Fig. 2.19. For NMOS devices, the mobility change was larger in the vertical direction and much smaller in the horizontal direction. The maximum mobility change was about 9%. For PMOS devices, the mobility change was much larger, and the magnitude of change was similar for the horizontal and vertical directions. The maximum mobility change reached about 45%.




(a) (b)

Figure 2.19. Contours of mobility variation for (a) NMOS and (b) PMOS.

In order to note the difference between NMOS and PMOS devices more clearly, the mobility change along the vertical and horizontal directions were plotted in Fig. 2.20. If the KOZ was defined as the region with mobility change exceeding 5%, for NMOSFET, the KOZ didn't exist for horizontal devices, and the size of the KOZ was about 2 μm for vertical devices. For PMOSFET, the KOZ size was much larger about 12 μm for both horizontal and vertical devices. This result suggests that different KOZ rules should be considered for NMOS and PMOS devices with different placement.

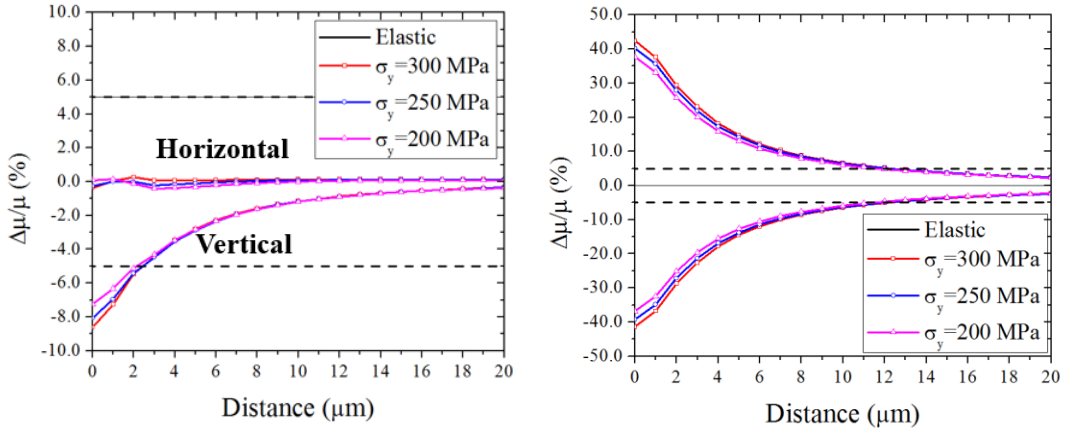



Figure 2.20. Mobility change along the vertical and horizontal directions for (a)NMOS and (b) PMOS.

To show the effect of local plasticity on KOZ, an elastic-plastic model was constructed where Cu was assumed to be elastic and perfectly plastic with different yield strength values. The profile of mobility change calculated by the elastic-plastic model were also plotted in Fig. 2.20. The amount of mobility change was found to reduce slightly at the TSV/Si interface, as the maximum stress was reduced by plasticity. However, as the distance away from the via increased, the difference between the elastic-plastic and the pure elastic models became smaller. This indicated that the localized plasticity had small effect on the KOZ. Therefore, the KOZ was mostly controlled by the elastic stress in Si, which was largely determined by stress relaxation in the Cu via during heating, as discussed in the previous section.

## 2.5. SUMMARY

In this chapter, the thermo-mechanical characteristics of Cu TSVs are studied by combining the substrate curvature method with stress and microstructure analyses and found to be distinctly different from Cu thin films. First and foremost, the stress state in

TSV is triaxial, while the stress in thin films is biaxial. For Cu thin films, with a biaxial stress state, the von-Mises stress is often sufficient to cause large-scale plastic yield in the entire film. In contrast, with a triaxial stress state, the TSV behaves linearly elastic with only localized plasticity near the top and bottom at the via/Si interface. Hysteresis loops were observed for thin films due to the large-scale plasticity during thermal cycling, while for the TSV structure, the localized plastic deformation had negligible effect on the overall curvature, and hysteresis loops were not observed. This led to a large residual stress in the Cu TSV at the end of the cooling cycle that can significant impact the keep-out zone for devices. The residual stress was found to be determined by stress relaxation occurring during the heating cycle, which was controlled in turn by grain growth in the Cu TSV, depending on the peak temperature in the heating cycle. Since the grain growth in Cu was primarily controlled by the electroplating process, the results indicate the possibility to reduce the residual stress in TSV by optimizing Cu electroplating, particularly its chemistry, which will be discussed in following chapters.

# Chapter 3: Plasticity and Via Extrusion

Via extrusion is an important yield and reliability concern for 3D integration as it can cause failure in the TSVs and in the adjacent interconnect structures during fabrication or thermal cycling. In this chapter, synchrotron x-ray microdiffraction technique is used to directly measure the local stress and material properties in Cu near the via/Si interface. The mechanism of via extrusion based on local plasticity by dislocation glide is discussed, with results from the synchrotron x-ray microdiffraction providing direct experimental evidence of the presence of local plasticity. An analytical model is developed, and used together with FEA to analyze the via extrusion caused by plasticity. The analysis is extended to two TSV structures with different grain sizes and mechanical properties.

## 3.1. SYNCHROTRON X-RAY MICRODIFFRACTION TECHNIQUE

### 3.1.1. Introduction of synchrotron x-ray based techniques

X-ray diffraction has been a key technique for materials characterization taking advantage of the fact that the wavelength of x-ray is the same order of magnitude as the interplanar spacing in a crystalline material [66]. Traditional x-ray diffraction techniques can offer a plethora of information of the crystal but have only limited spatial resolution due to the large size of the x-ray probe. As the dimension of microelectronics devices and structures continue to scale down to submicron or even nanometer range, there is an increasing need for high spatial resolution x-ray diffraction techniques to probe the structure and deformation behavior of materials in microelectronics systems.

X-rays produced by a synchrotron source are ideal for such applications. Synchrotron x-rays are emitted when electron traveling at relativistic speed changes direction, which generates x-ray flux and brightness several orders of magnitude higher than that from laboratory x-ray sources [67]. With the recent development of third-

generation synchrotron sources and advanced optics, x-ray probes of submicron spatial resolution have been achieved, enabling a wide variety of exciting applications [68]. Three common techniques using synchrotron x-rays are: diffraction for studying structures of materials, spectroscopy for measuring bonding and electronic structure, and imaging for analyzing certain material properties across a sample [69]. In addition to better spatial resolution for thin and small structures, additional advantages of synchrotron x-ray techniques include large penetrating depth to probe buried structures for nondestructive measurement, ability for *in situ* measurement under various time, temperature, and pressure conditions, and wide energy range for versatile experiment design [69]. The often limited access to synchrotron facilities, however, is a major constraint for application of synchrotron x-ray based techniques.

### 3.1.2. Synchrotron x-ray microdiffraction beamline at ALS

In this work, synchrotron x-ray microdiffraction technique was used to study TSV structures. Synchrotron x-ray microdiffraction measurements were conducted at Beamline 12.3.2 of the Advanced Light Source (ALS) at the Lawrence Berkeley National Laboratory (LBNL). This beam line is built upon a superbend source and can provide high brightness x-rays with a spectral range of 5-22 KeV [70]. The schematic layout of the beamline is shown in Fig. 3.1 [70]. Downstream from the superbend source, the x-ray beam is focused by the M1 toroidal mirror (1:0.72) at 13m from the source to about 160 μm × 50 μm FWHM (horizontal by vertical) onto a set of roll slits. The roll slits, at 22.4 m from the source, are used to define the size of the virtual secondary source. The x-ray beam then reaches the 4-crystal monochromator, which consists of two identical channel cut Si (111) crystals mounted on rotary stages to allow either white beam or monochromatic beam to pass through. The beam continues through a second set of slits (also known as the JJ slits),

which serves as an aperture, to a pair of Kirkpatrick-Baez (KB) mirrors. The KB mirrors focus the x-ray beam into a submicron size of about 0.8 μm × 0.8 μm FWHM on to the sample with the focal position at 24.8 m from the source [70], [71].

The sample stage is comprised of an upper stage and a lower stage as shown in Fig. 3.2a. The lower stage is used for coarse positioning in the X, Y, Z directions and for aligning the rotation axes (φ and χ). For reflection mode, the lower stage is set at $\chi=45^{o}$. The sample is mounted on the upper stage, which moves at a submicron resolution for scanning samples. The coordinate systems for the upper stage (sample reference frame) and the lower stage (lab reference frame) are shown in Fig. 3.2b. Special accessories can be designed to mount the upper stage to allow in-situ measurements at high temperatures and under controlled environment [70], [71]. The diffraction patterns are collected by a DECTRIS Pilatus 1M pixel array detector featuring large sensor area of 169 × 179 mm and fast readout time of 7ms, positioned vertically at ~147 mm from the sample [70], [72]. The beamline is also equipped with a vortex-EM Si-drift fluorescence detector which records x-ray fluorescence signals for elemental mapping and precise sample positioning [70].

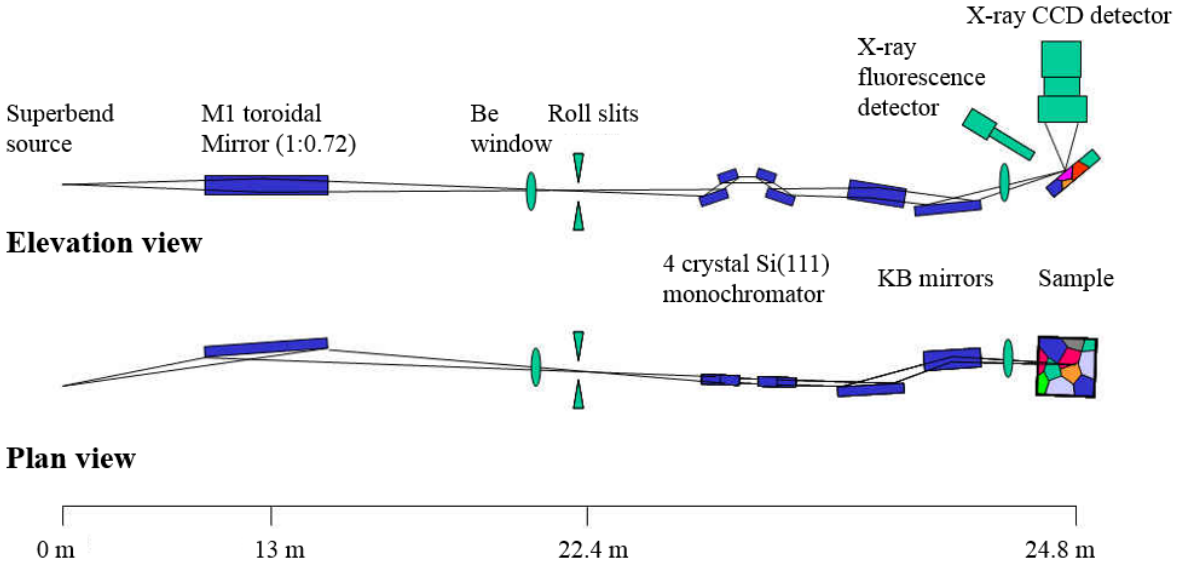
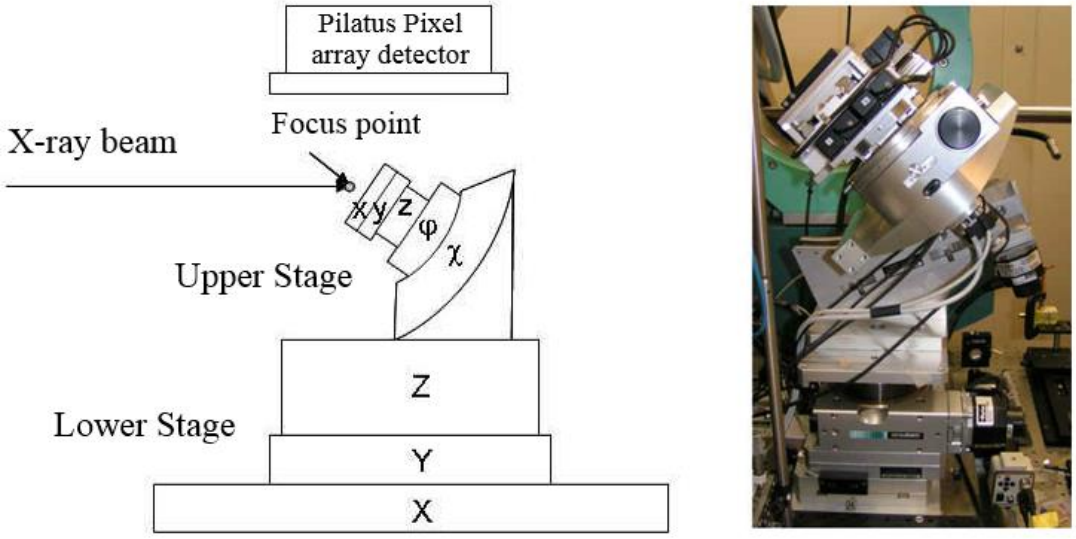
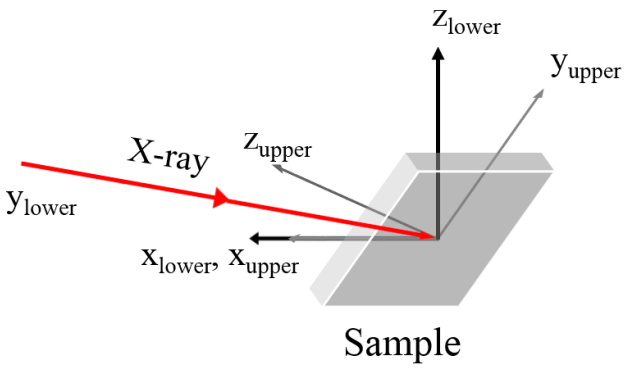



Figure 3.1. Schematic layout of the x-ray microdiffraction beamline 12.3.2 at ALS [70].




(a)




(b)

Figure 3.2. (a) Schematic drawing and photograph of the stage. (b) Illustration of the coordinate systems for the upper and lower stages [70].

### 3.1.3. Diffraction measurement and data analysis

#### *3.1.3.1. X-ray Microdiffraction*

X-ray microdiffraction measurement can be conducted either using white beam, or polychromatic beam, or by monochromtic beam. Typically, white beam is selected when the grain size in the sample is greater than or about equal to the size of the x-ray beam. The white beam generates Laue patterns containing a large number of reflections from the illuminated crystal in a single exposure. The white beam technique used at Beamline 12.3.2 is known as *scanning white beam x-ray microdiffraction* (μSXRD). Unlike conventional laboratory x-ray diffraction techniques which use fixed photon energy to measure the diffraction angle while rotating the sample, μSXRD is setup to perform scanning of the sample by translating the upper stage in the x and y directions. Laue images are collected from a 2D grid on the sample and are analyzed to yield information of the material such as the grain orientation, deviatoric strain tensors, and plasticity. When the grain size of the sample is much smaller than the beam size, e.g. grain size < 100 nm, monochromatic beam can be used to obtain diffraction rings from the sample similar to power diffraction.

Monochromatic beam can also be used to scan a range of energies around an *hkl* reflection to determine the lattice spacing. Detailed data analysis procedure for the white beam and monochromatic beam microdiffractions are discussed in the following subsections. Most of the measurements in this study were conducted using μSXRD since it is a more efficient way to collect a large amount of information about the sample.

#### *3.1.3.2.Calibration*

The diffraction geometry of the system must be calibrated before any measurement for proper data analysis. More specifically, five independent parameters need to be determined: the x and y coordinates of the "center channel" on the detector ($x_c$,$y_c$), the distance between the sample and the "center channel" on the detector ($d_d$), and two angles specifying the tilt of the detector with respect to the incident x-ray beam (pitch, β and yaw), as shown in Fig. 3.3. For calibration, the Laue pattern from a reference sample, typically an unstrained single crystal, such as a (001) Si wafer, is obtained. With known lattice parameters for the reference sample, the peak positions in the Laue pattern are a function of the five geometry parameters. Using a nonlinear least squares method, refinement of these parameters is achieved by minimizing the following function

$$\alpha_0 = \frac{\sum_i w_i(\alpha_i^{th} - \alpha_i^{exp})^2}{\sum_i w_i} \tag{3.1}$$

where $\alpha_i^{th}$ and $\alpha_i^{exp}$ are differences in angle between pairs of theoretical and experimental scattering vectors, and $w_i$ is a weighting factor.

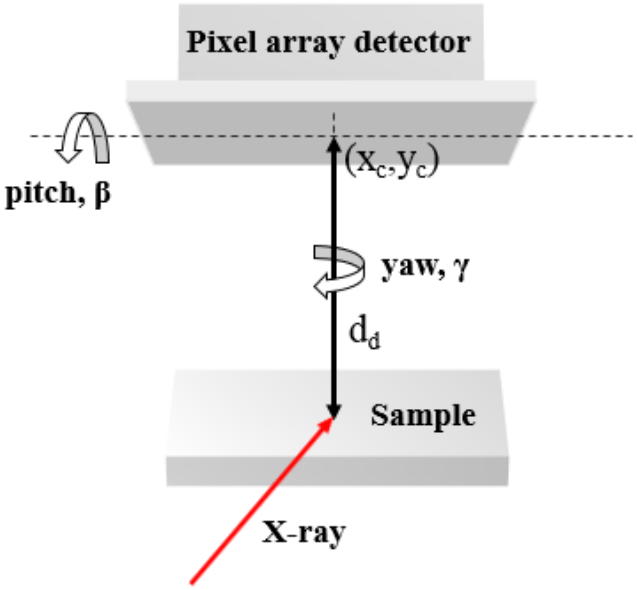



Figure 3.3. Illustration of the geometry parameters for calibration.

### *3.1.3.3.Indexation*

The Laue patterns generated from the microdiffraction are analyzed using the X-ray Microdiffraction Analysis Software (XMAS) developed at ALS [73]. The software first reads the diffraction image and subtracts the background intensity, a peak search routine is then performed to identify the position of the peaks. The peaks are classified by their integrated intensities and fitted with a 2D Gaussian, Lorentzian, or Pearson VII function. The accuracy of the fitted peak position is a major factor limiting the accuracy of strain determined by the μSXRD method [71]. The 2D Lorentzian function has been found to provide the best fit for most measurements. Other input parameters that affect the accuracy of the peak fitting include the *box size* for peak searching, which defines the number of pixels to be fitted with the function, and the *multiplicative factor*, which sets the threshold

intensity for the peaks in subsequent analyses [73]. These parameters usually need to be adjusted for each set of measurement for best results.

Once the peak positions are determined, the software then indexes the Laue patterns based on a given set of calibration parameters and an input crystal file. The crystal file (*.cri file) contains the unit cell parameters a, b, c, and α, β, γ, as shown in Fig. 3.4, and the Wyckoff positions and occupancy, and can be created by the user if a particular material of interests is not in the existing database. The XMAD crystal parameters of Cu and Si are listed in table 3.1.

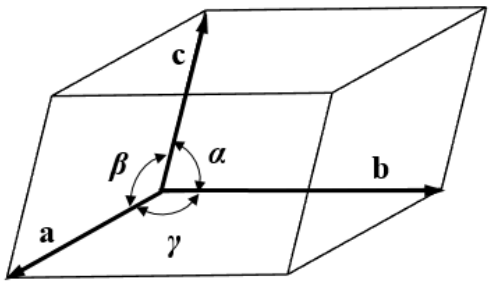



Figure 3.4. Unit cell parameters a, b, c, and α, β, γ.

Table 3.1. XMAS crystal parameters for Cu and Si.

| Element | Space group no. | a,b,c (nm) | α, β, γ (°) | Wyckoff positions and occupancy |
|---|---|---|---|---|
| **Si** | 227 | 0.54300 | 90 | 0,0,0, 1.0 |
| **Cu** | 225 | 0.36078 | 90 | 0,0,0, 1.0 |

For the indexation of the Laue pattern, the directions of the diffracted beams are calculated from the peak positions, and the directions of the experimental scattering vectors, $\boldsymbol{q}_{\text{exp}}$, can be calculated as $\boldsymbol{q}_{exp} = \boldsymbol{k}_{out} - \boldsymbol{k}_{in}$, where $\boldsymbol{k}_{in}$ and $\boldsymbol{k}_{out}$ are vectors for the incident beam and outgoing diffracted beam, and $|\boldsymbol{k}_{in}| = |\boldsymbol{k}_{out}|$ if assuming elastic scattering. For a set of brightest reflections, the angles between the experimental scattering vectors are then compared to a reference list of angles of theoretical scattering vectors. The program searches for triplets of angular matches between the experimental and theoretical angles, with an angular tolerance defined in the calibration parameters. For each triplet of *hkl* indices found, the list of reflections that should be present is calculated. The grain is indexed when the largest number of matching reflections is found. The algorithm implemented in the program is able to index more than ten overlapping grains [71]. The indexation by XMAS for a reference (100) Si sample is illustrated in Fig. 3.5.

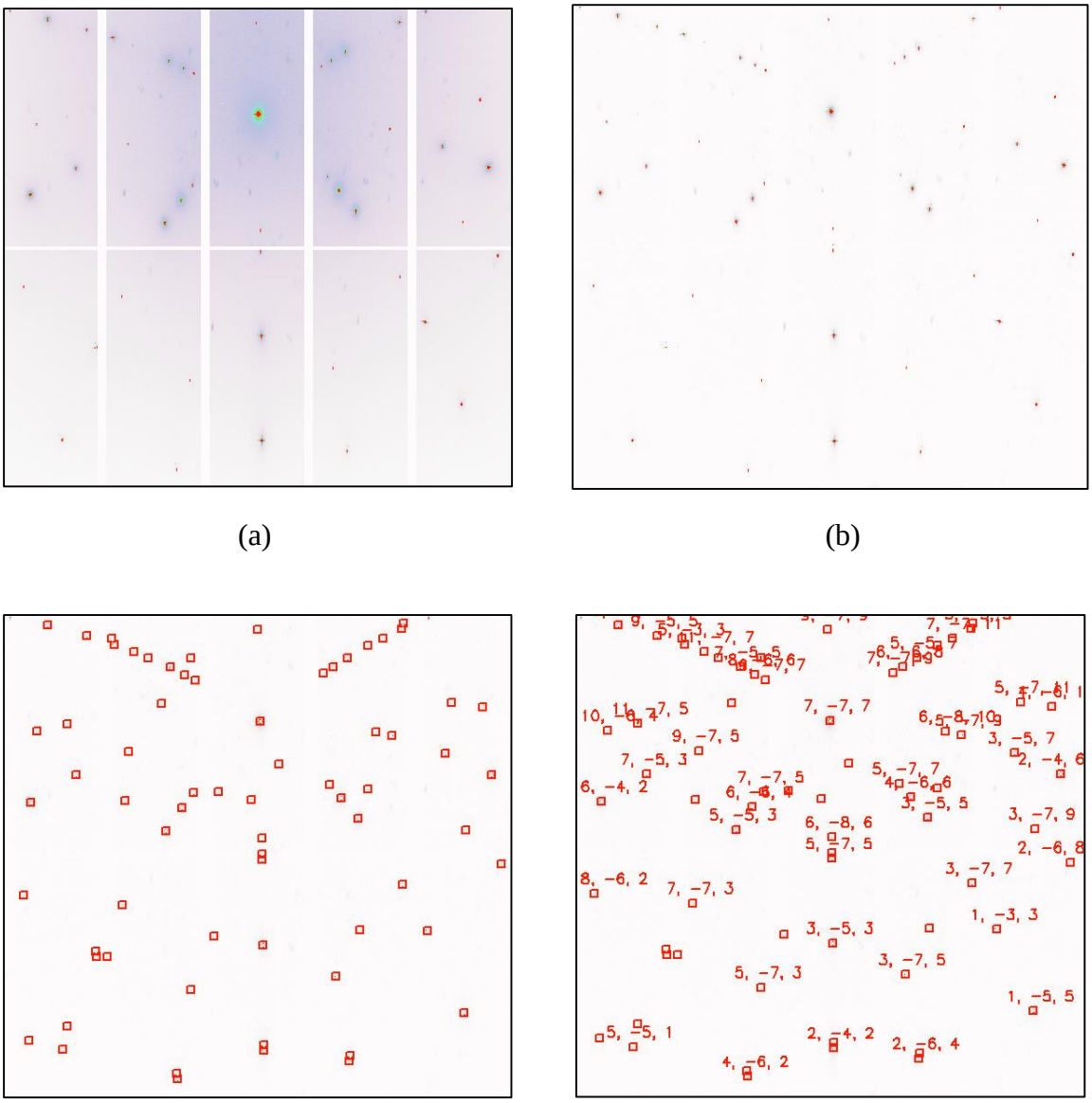



Figure 3.5. Laue pattern (a) before background subtraction. (b) After background subtraction. (c) After peak search. Each square represents a peak position. (d) After indexation of Si.

### *3.1.3.4. Strain refinement and stress determination*

The complete strain tensor $\varepsilon_{ij}$, is defined as

$$\varepsilon_{ij} = \varepsilon'_{ij} + \Delta = \begin{bmatrix} \varepsilon'_{11} & \varepsilon_{12} & \varepsilon_{13} \\ \varepsilon_{12} & \varepsilon'_{22} & \varepsilon_{23} \\ \varepsilon_{13} & \varepsilon_{23} & \varepsilon'_{33} \end{bmatrix} + \begin{bmatrix} \delta & 0 & 0 \\ 0 & \delta & 0 \\ 0 & 0 & \delta \end{bmatrix} \tag{3.2}$$

where $\varepsilon'_{ij}$ is the deviatoric strain and $\Delta$ is the dilatational strain with $\delta = (\varepsilon_{11} + \varepsilon_{22} + \varepsilon_{33})/3$ [74].

Indexation of the Laue pattern deduces the positions of the *hkl* reflections, but the absolute energies of the individual *hkl* reflections in the Laue pattern are not known. Therefore, white beam diffraction can obtain only the deviatoric strain tensor from the distortion of the unit cell but not the dilatational strain which is related to the change of the unit cell volume. For the deviatoric strain, the angular deviation of the atomic planes, or unit cell distortion, can be obtained by comparing the positions of the indexed Laue reflections to those in an unstrained Laue pattern. Using the same minimization procedure with fixed diffraction geometrical parameters, Eq. 3.1 is used for strain refinement to determine the relative values of lattice parameters (b/a, c/a, and α, β, γ), which can then be used to calculate the deviatoric strains, $\varepsilon'_{ij}$ [71]. The error of the measured strain is typically smaller than $\pm 2 \times 10^{-4}$. The equivalent strain can be calculated from the deviatoric components as

$$\varepsilon_{eq} = \frac{2}{3}\sqrt{\frac{1}{2}[(\varepsilon'_{11} - \varepsilon'_{22})^2 + (\varepsilon'_{22} - \varepsilon'_{33})^2 + (\varepsilon'_{11} - \varepsilon'_{33})^2 + 6({\varepsilon'_{12}}^2 + {\varepsilon'_{13}}^2 + {\varepsilon'_{23}}^2)]} \tag{3.5}$$

For thin film samples with biaxial stress state, where the out-of-plane stress, $\sigma_{zz}$, is zero, the full strain tensor can be obtained by the white beam microdiffraction alone. For most other samples, to obtain the dilatational strain Δ, monochromatic beam can be used to scan a range of energies around at least one *hkl* reflection to obtain the exact energy of the reflection, $E_{hkl}$. Based on the Bragg's law and the Planck–Einstein relation, the absolute lattice spacing can be calculated as

$$d_{hkl} = \frac{hc}{2E_{hkl}sin\theta} \tag{3.3}$$

where *h* is the Planck constant, c is the speed of light, and θ is the Bragg angle. Therefore, the dilatational strain can be deduced as [75]

$$\delta = \frac{\Delta d}{d} = -\frac{\Delta E}{E} \tag{3.4}$$

There are several practical limits in using monochromatic beam microdiffraction. First, it is a more time-consuming process. Second, there could be a slight change of the diffraction volume when switching from the white beam to the monochromatic beam because of hardware limitations and/or the change of penetration depth. The accuracy of monochromatic beam microdiffraction can also be affected by slight errors in determining the energy peak position, especially when the peak is broadened [76].

The stress in the sample can be obtained through the Hooke's law of linear elasticity as

$$\sigma_{ij} = C_{ijkl}\varepsilon_{kl} \tag{3.6a}$$

and

$$\sigma'_{ij} = C_{ijkl}\varepsilon'_{kl} \tag{3.6b}$$

where $\sigma'_{ij}$ is the deviatoric stress, $C_{ijkl}$ is the stiffness matrix of the material. Based on the deviatoric stress components, the von-Mises stress can be calculated as

$$\sigma_{eq} = \sqrt{\frac{1}{2}[(\sigma'_{11} - \sigma'_{22})^2 + (\sigma'_{22} - \sigma'_{33})^2 + (\sigma'_{11} - \sigma'_{33})^2 + 6({\sigma'_{12}}^2 + {\sigma'_{13}}^2 + {\sigma'_{23}}^2)]} \tag{3.7}$$

### *3.1.3.5. Local plastic yielding*

The methods mentioned in the previous section are good for only obtaining the elastic deformation of the crystal. A unique capability of the white beam microdiffraction is to determine the plastic deformation in the sample from the shape of Laue reflection peaks. The plastic deformation in the crystal may involve curved and polygonised lattice planes [77]. With the presence of a lattice curvature, the θ value for a particular *hkl* plane may have a range of values. As white beam x-rays contain a wide energy range, Bragg's law can be satisfied even with the variation in the θ value. Unlike the single and sharp peaks measured for undeformed crystal planes, the diffracted peak for deformed lattice planes will be broadened due to the range of θ values in the curved crystal. The width of a Laue diffraction peak thus contains the information about the dislocation density inside a grain [78]–[82]. When polygonization occurs in the crystal to form low-angle boundaries, multiple discreet peaks can be observed [77]–[83]. The different shapes of the Laue peak are illustrated in Fig. 3.6.

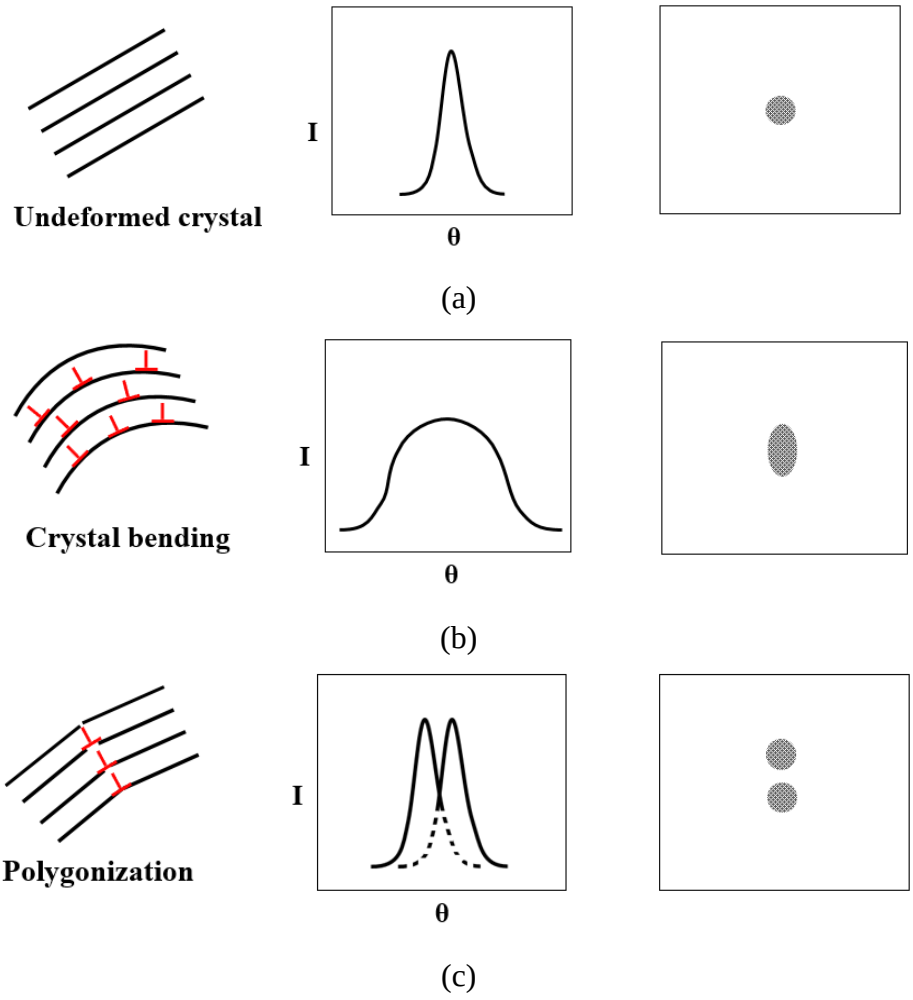



Figure 3.6. Schematics showing the intensity profile and spot shape on the detector of a Laue reflection for (a) undeformed crystal, (b) curved crystal planes, and (c) polygonized crystal planes. Geometrically necessary dislocations (GNDs) are illustrated in (b) and (c) (adapted from [77]).

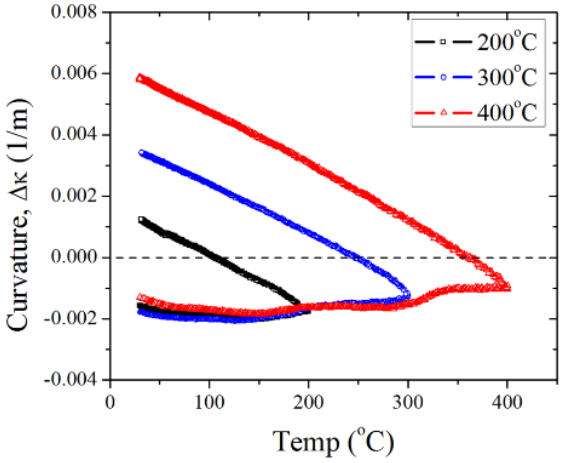
For a Laue pattern, the XMAS program fits each indexed reflection with a 2D ellipse, and averages of the longest and shortest axes of the fitted ellipse for all the reflections are calculated as the average peak width (APW), which is an output parameter of XMAS. The angular resolution of the measured peak broadening is $0.01^{o}$. In addition, a *Peak Study* utility in XMAS allows an individual Laue peak to be analyzed. The peak can be plotted in 2D and 3D coordinate systems including the detector coordinates, the

reciprocal space, and the theta-chi (θ-χ) space, where θ is the Bragg's angle and χ is the angle between the projection of the diffracted beam in the $XZ_{lab}$ plane and the $Z_{lab}$ axis. In the reciprocal space or the θ- χ space, the peak broadening, $\Delta\theta_{FWHM}$, can be obtained to estimate the radius of curvature of the crystal bending, R. As a simplified estimate, the density of geometrically necessary dislocation (GND), $\rho_G$, can be calculated based on the Cahn-Nye relationship as $\rho_G = 1/Rb$ , where $b$ is length of the Burgers vector [84], [85].

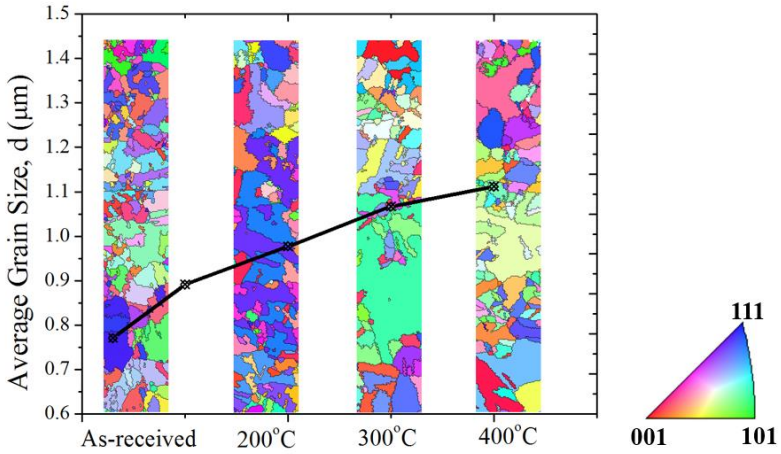
## 3.2. WHITE BEAM SCANNING X-RAY MICRODIFFRACTION (μSXRD) STUDY OF TSV-A

### 3.2.1. Test structure and measurement of extrusion

TSV-A structure was used for the white beam μSXRD study. The via diameter was D=10 μm and via depth was H=55 μm, as described in detail in chapter 2. Samples were prepared with different thermal histories, including the as-received sample and samples after thermal cycling from room temperature (RT) to 200, 300 and 400°C. Thermal cycling measurements were carried out in the same fashion as described in chapter 2 and the measured curvature-temperature behaviors were shown in Fig. 3.7a. The corresponding crystal orientation maps and grain sizes for each condition were plotted in Fig. 3.7b, which showed the grain growth as discussed in chapter 2.




(a)




(b)

Figure 3.7. (a) Curvature-temperature behaviors of TSV samples thermal cycled to 200ºC, 300ºC and 400ºC, respectively. (b) Crystal orientation and grain size obtained by EBSD for each condition.

Atomic force microscopy (AFM) scans were performed on top of several vias for each thermal cycling condition, where extruded via surfaces can be seen at different thermal cycling temperatures. Line profiles across via centers were extracted and plotted in Fig. 3.8. Both the as-received via and vias thermal cycled to 200ºC were about 26nm above the wafer surface and had relatively flat top surfaces. For the vias thermal cycled to

300 ºC, the via extrusion profile emerged to have a "donut" shape and continued to grow at 400°C, reaching about 140nm at some points. An as-received via and a via thermal cycled to 400ºC were examined by SEM with the stage tilted at 52º, where hillocks of individual grains can be clearly seen (Fig. 3.9).

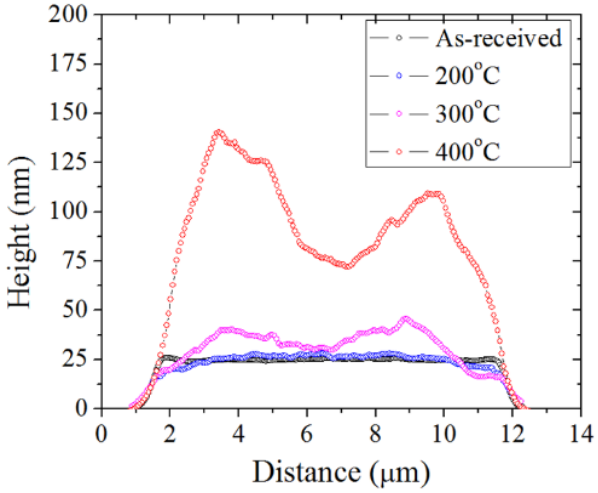



Figure 3.8. Average via extrusion induced by thermal cycling from R.T. to 400°C and measured by AFM. The extrusion heights are obtained by averaging measurements of 5 vias for each case.

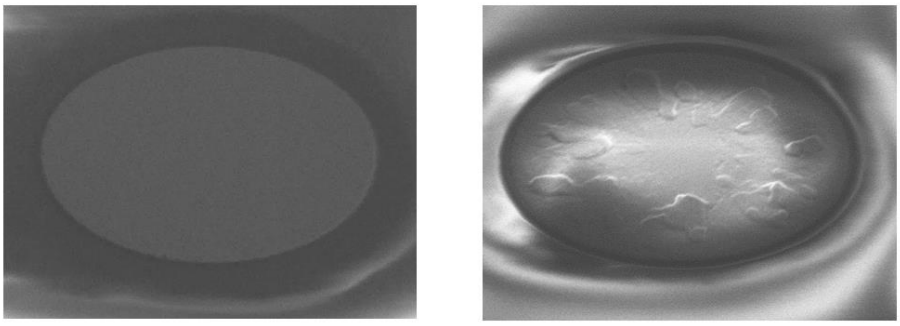



Figure 3.9. Secondary electron images of the via top surface before and after thermal cycled to 400ºC. The samples were imaged with the stage tilted at 52º.

### 3.2.2. White beam μSXRD measurement setup

For the white beam μSXRD measurement, all samples were mechanically polished with the polished surface parallel to the Si [110] plane and perpendicular to the wafer surface before a row of vias was exposed (Fig. 3.10). Without exposing the Cu vias, such a sample preparation method allowed the x-ray to penetrate through Si to measure Cu in the vias while avoiding polishing-induced stress and deformation in Cu.

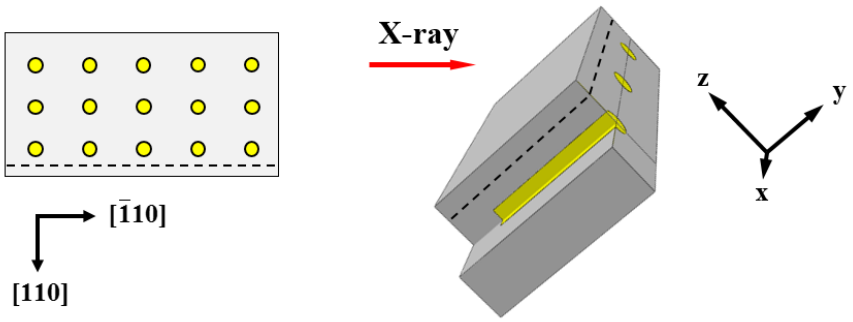



Figure 3.10. Illustrations of the TSV-A sample used for μSXRD measurements. The dashed line indicates the location of the polished plane.

To locate the position of the TSV, x-ray fluorescence (XRF) maps similar to the one shown in Fig. 3.11 were collected with the software setup to count for photons within an energy range of 7.5 - 8.5 KeV, corresponding to the characteristic line of Cu. An area of 30 μm by 70 μm (x by y) was then selected around the via for white beam scans with a step size of 1 μm/step. Using the procedure described earlier, the Laue patterns in the scan matrix were indexed for both Cu and Si.

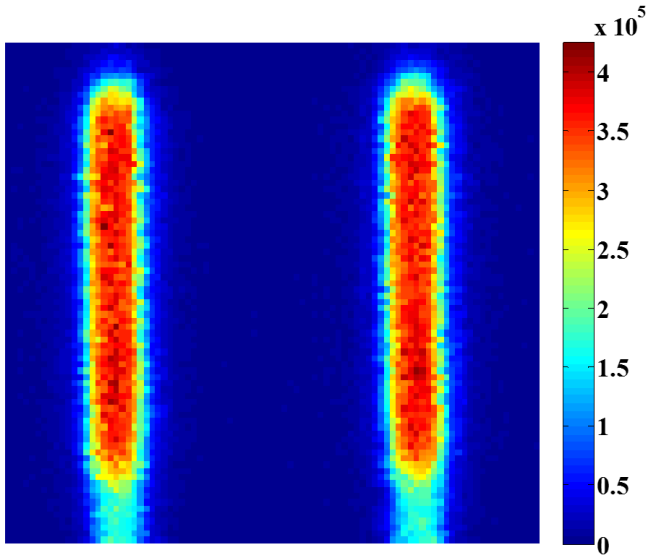



Figure 3.11. X-ray fluorescence map of Cu vias in TSV-A sample.

### 3.2.3. Local plasticity in Cu

In Fig. 3.13, the average peak width (APW) is plotted for the as-received TSV and TSVs after thermal cycling to 200, 300, and 400ºC. For the as-received and the via after 200ºC thermal cycling, the APWs showed very similar values. The APW increased for the via after thermal cycling to 300ºC and increased further after thermal cycling to 400ºC, particularly in the area near the top of the vias. The APW in the middle of the via was small and did not vary much for all samples.

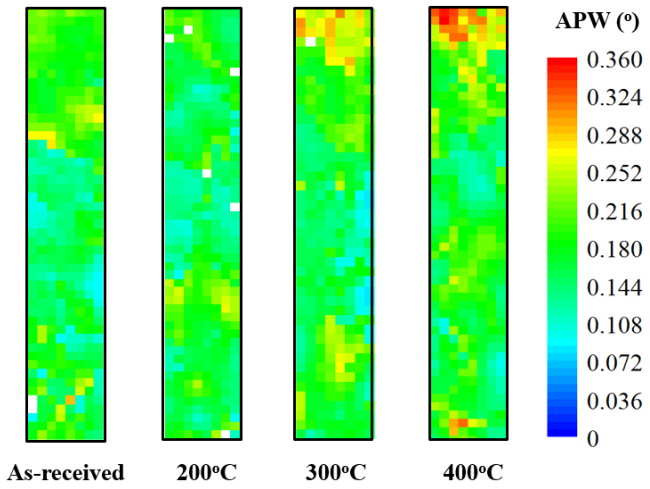



Figure 3.12. Average peak width (APW) of Cu for the as-received via and vias after thermal cycling to 200°C, 300°C, and 400°C.

Several individual Laue reflections for Cu grains near the top and in the middle of the via were further examined for the as-received and the 200°C and 400°C thermal cycled samples. It was found that for the as-received and 200°C thermal cycled vias, Laue reflections were relatively sharp for grains both near the top and towards the middle of the via. For the 400°C thermal cycled via, the peaks were relatively sharp in the middle of the via, but showed pronounced peak broadening near the top of the via, indicating the presence of local plasticity in the Cu grains. Peak splitting was also observed, suggesting the formation of subgrains. As an example, the peak shapes of the $(1\bar{1}3)$ Laue reflection from Cu grains near the top of the via and the middle of the via were compared in Fig. 3.13 for the as received via and vias thermal cycled to 200°C and 400°C. The results showed that plasticity occurred significantly after thermal cycling to 400°C, but barely observable after thermal cycling to 200°C. In addition, plasticity was found to be concentrated primarily near the top of the via. The localized nature of the plasticity was consistent with the FEA results discussed in chapter 2.

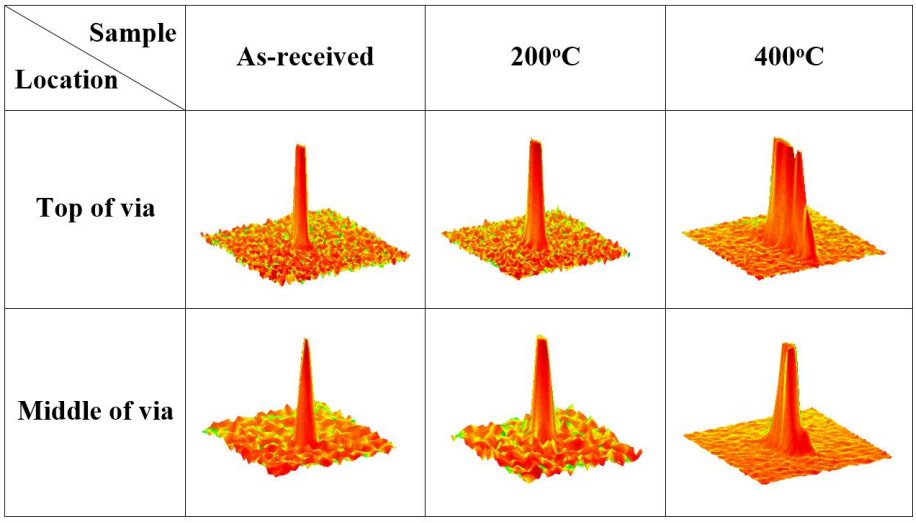



Figure 3.13. Peak shapes of the $(1\bar{1}3)$ Laue reflection from grains near the top and in the middle of the vias for the as-received sample and samples subjected to thermal cycling of 200°C and 400°C.

### 3.2.4. Stress-induced deformation in Si

For Si, the out-of-plane orientation, φ, defined as the angle between the [001] crystal direction and the (110) polished surface normal, was calculated. Interestingly, a gradient of the out-of-plane orientation, Δφ, became visible around the top of the via under thermal cycling, as shown in Fig. 3.14. The change of Si lattice orientation near the TSV can be attributed to the elastic deformation of Si caused by the residual stresses in Si around the TSV. The local lattice rotation of Si on one side of the via was in opposite sign from the other side, indicating an axially symmetric bending of the Si lattice around the Cu via. The orientation gradient was not clear in the as-received sample but became observable after heating to 200°C. The bending deformation became more pronounced near the top of the via after thermal cycling to 400°C, suggesting a higher residual stress in Si around the Cu via. The overall deformation characteristics were consistent with the measured curvature-temperature behaviors for these samples shown in Fig. 3.7., and were also related to the KOZ discussion in the previous chapter.

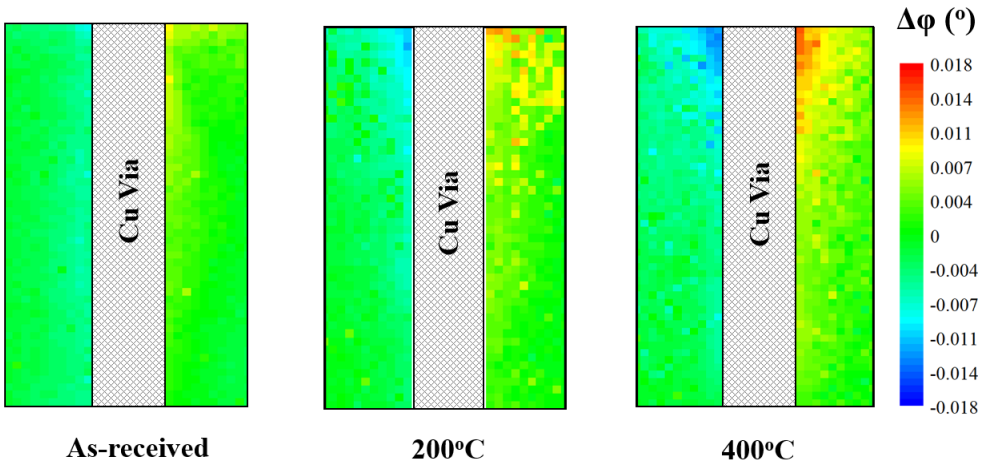



Figure 3.14. Relative change of the out-of-plane orientation in Si around the TSV for the as-received sample and samples after thermal cycling to 200°C and 400°C. The diameter of the Cu via is 10 μm.

## 3.3. ANALYSIS OF VIA EXTRUSION BASED ON LOCAL PLASTICITY

### 3.3.1. Local plasticity mechanism for via extrusion

Via extrusion phenomenon, which is the irreversible expansion of Cu via in the axial direction after thermal processing, is illustrated in Fig. 3.15. Consider a TSV structure with a flat top surface after CMP (Fig. 3.15a). When Cu expands during heating ($\alpha_{Cu} > \alpha_{Si}$), the confinement of Si drives the upward extrusion of via, which reaches the maximum height at the peak temperature (Fig. 3.15b). During cooling, the volume shrinkage of Cu will reduce the amount of the extrusion by elastic recovery. If Cu were completely elastic, there would be no residual deformation after cooling. It thus becomes clear that inelastic processes occurred during thermal processing causes the non-recoverable deformation, or via extrusion (Fig. 3.15c). So far, FEA has been widely used to simulate via extrusion, where various inelastic mechanisms, such as plasticity, interfacial sliding, and/or

diffusional creep, have been used to account for the nonlinearity of Cu [86]–[88]. So far, experimental evidences are lacking in supporting the FEA assumptions.

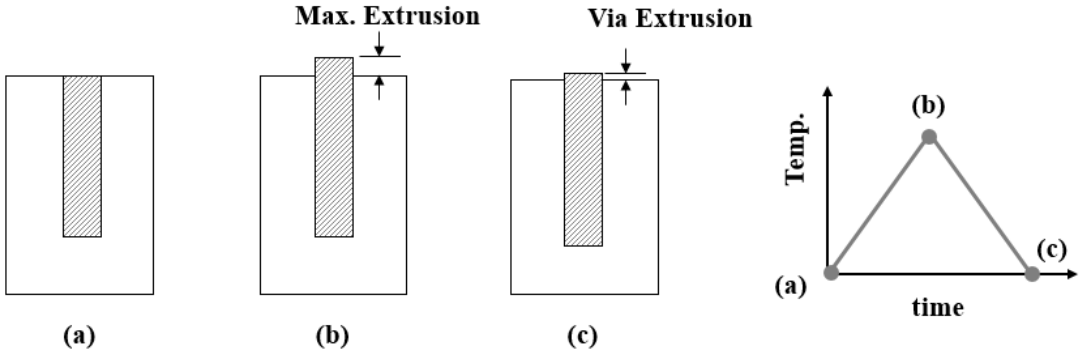



Figure 3.15. Illustration of the via extrusion process during a thermal cycle. (a) wafer surface after CMP. (b) extrusion reaches the maximum at the highest temperature. (c) residual deformation after cooling.

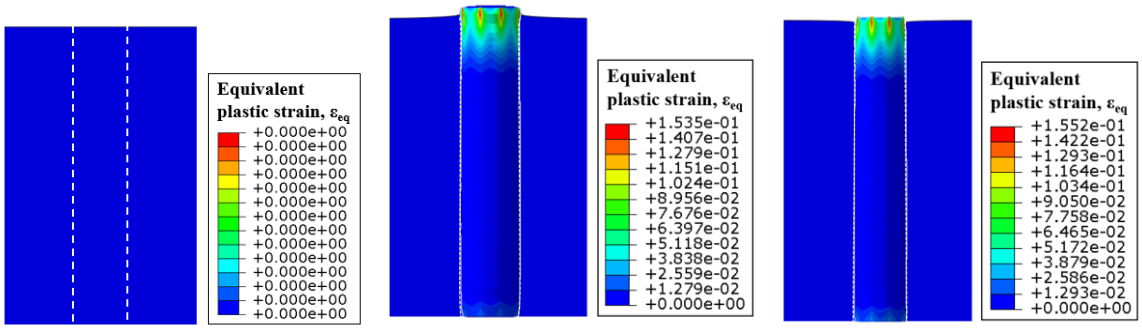
The white beam μSXRD measurement provided important experimental evidence to verify the presence of local plasticity near the via top, which was proposed as a key mechanism causing via extrusion in the measured samples. The increased local plasticity observed with increasing thermal cycling temperature was consistent with the via extrusion behavior shown in Fig. 3.8. For vias thermal cycled to 200$^{o}$C, when local plasticity was absent, no extrusion was observed. For vias thermal cycled to 300$^{o}$C, a small amount of local plasticity was measured and the via extrusion was small. For vias thermal cycled to 400$^{o}$C, significantly more local plasticity was observed with corresponding larger via extrusion height. In addition, results from the wafer curvature measurements showed overall stress built-up in the TSV structure during thermal cycling. Together, the stress built-up and plasticity lead to Cu extrusion or "pop-up" of the TSV top surface after thermal cycling, as confirmed by the AFM scans. Therefore, the white beam μSXRD provided

direct evidence to support local plasticity as a dominant mechanism to induce the unrecoverable deformation of the Cu via, or via extrusion.

In the remainder of chapter 3, via extrusion will be analyzed based on local plasticity mechanism. It needs to be pointed out that other relaxation mechanisms involving mass transport, such as diffusional creep, could also contribute to via extrusion. These other factors will be further discussed in Chapter 4.

### 3.3.2. Thermo-mechanical analysis of via extrusion based on local plasticity

Using a simple 3D elastic-plastic model, the via extrusion behavior under thermal cycling from RT to 300°C was analyzed. In this analysis, Cu was assumed to be elastic-perfect plastic with yield strength of 200 MPa. The equivalent plastic strain in Cu and via deformation at RT, 300°C and after cooling back to RT were shown in Fig. 3. 16.




(a) (b) (c)

Figure 3.16. Elastic-Plastic FEA model of via extrusion for thermal cycling to 300°C. The equivalent plastic strain in Cu and the deformation shape were shown for different stages of the thermal cycling: (a) at RT before heating, (b) after reaching 300°C and (c) after cooling to RT. (scale factor =30).

To account for the plastic mechanism for via extrusion, a simplified elastic-plastic analytical model was constructed [89]. The model assumed a free sliding at via/Si interface to estimate the upper bound of via extrusion. For a TSV heated from RT with a thermal

load of ΔT, the CTE mismatch between Cu and Si would induce a biaxial compressive stress in the via:

$$\sigma_r = \sigma_\theta = -\Delta T(\alpha_{Cu} - \alpha_{Si})\left(\frac{1-\nu_{Cu}}{E_{Cu}} + \frac{1+\nu_{Si}}{E_{Si}}\right)^{-1} \tag{3.8}$$

where $\sigma_r$ and $\sigma_\theta$ were the radial and circumferential stresses, E, ν, and α were the thermos-mechanical properties of Cu and Si ($\alpha_{Cu}$ = 17 ppm/ºC, $\alpha_{Si}$ = 2.3 ppm/ºC, $E_{Cu}$ = 110 GPa, $E_{Si}$ = 130 GPa, $\nu_{Cu}$ = 0.35, and $\nu_{Si}$ = 0.28, respectively. Both Cu and Si were assumed linear elastic in the model. The initial stress was assumed to be zero before heating and the non-uniform stress distribution near the surface was ignored.

The difference in the elastic strain between via and Si in the axial direction z resulted in an elastic extrusion $\Delta H_e$.

$$\frac{\Delta H_e}{H} = \varepsilon_{z,Cu} - \varepsilon_{z,Si} = \Delta T(\alpha_{Cu} - \alpha_{Si})(1 + \frac{2\nu_{Cu}}{E_{Cu}}\left(\frac{1-\nu_{Cu}}{E_{Cu}} + \frac{1+\nu_{Si}}{E_{Si}}\right)^{-1}$$
$$= \beta_e \Delta T = 20.64 ppm \Delta T \tag{3.9}$$

where $H$ is the via height and $\beta_e$ is the rate of extrusion as a function of temperature.

If no plastic yielding had occurred, the elastic extrusion would decrease at the same rate upon cooling and diminish to zero at room temperature after a full thermal cycle. Considering the case where plastic yielding occurred and assuming Cu was prefect plasticity with a yield strength of $\sigma_y$, the Cu via would deform plastically above a critical temperature, $\Delta T_y$, proportional to the yield strength $\sigma_y$:

$$\Delta T_y = \frac{\sigma_y}{\alpha_{Cu} - \alpha_{Si}}\left(\frac{1-\nu_{Cu}}{E_{Cu}} + \frac{1+\nu_{Si}}{E_{Si}}\right) \tag{3.10}$$

Since plastic deformation conserves volume, the volume change of the Cu via due to thermal expansion is $\Delta V/V = 3\alpha_{Cu}(\Delta T - \Delta T_y)$, and the change of the via radius due to thermal expansion is $\Delta R/R = \alpha_{Si}(\Delta T - \Delta T_y)$. Therefore, the plastic extrusion, $\Delta H_p$, could be deduced as:

$$\frac{\Delta H_p}{H} = \frac{\Delta V}{V} - \frac{2\Delta R}{R} = (3\alpha_{Cu} - 2\alpha_{Si})(\Delta T - \Delta T_y) = \Delta\beta_p(\Delta T - \Delta T_y)$$
$$= (46.4ppm)(\Delta T - \Delta T_y) \quad (3.11)$$

Eq. 3.11 showed that the plastic extrusion would increase linearly with temperature but with a much higher rate than the elastic extrusion ($\Delta H_p > \Delta H_e$). Therefore, plasticity would lead to significantly more via extrusion at high temperatures.

Assuming no reverse yielding during cooling, the residual extrusion $\Delta H_r$ after a full thermal cycle to a maximum temperature of $T_m$ became

$$\Delta H_r = H(\beta_p - \beta_e)(\Delta T_m - \Delta T_y) \quad (3.12)$$

Eq. 3.12 showed that the magnitude of the residual extrusion depended on the peak temperature of the thermal cycle and the yield strength of Cu. Assuming the yield strength of Cu was $\sigma_y$=200 MPa, for $\Delta T_m$=300°C and 400°C, the via extrusion behaviors during a thermal cycle were plotted for the analytical model and FEA as in Fig. 3.17.

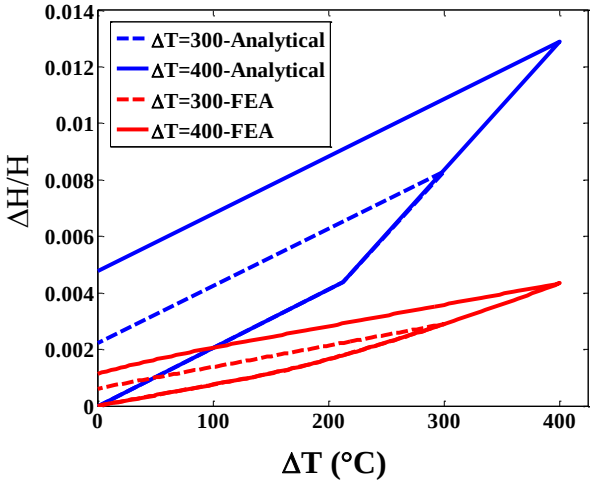



Figure 3.17. Comparison of the extrusion ratio (ΔH/H) between the analytical model and FEA.

In Figure 3.17, the analytical model showed that below the critical temperature of 239ºC with a yield strength of 200MPa, there would be no residual extrusion at room temperature. In addition, the extrusion calculated by FEA was much lower than that of the analytical model, because the FEA assumed the Cu/Si interface was perfectly bonded. In previous FEA studies, when a traction-separation law (TSL) was used to describe the Cu/Si interface, stronger interfaces were found to reduce the effect of plasticity on extrusion [89].

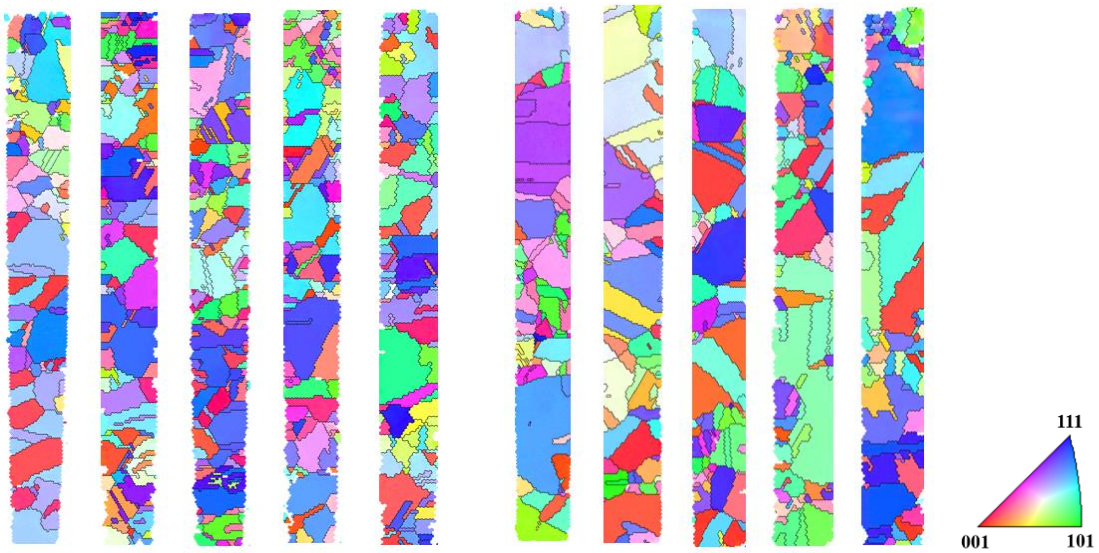
## 3.4 EFFECT OF GRAIN SIZE ON YIELD STRENGTH AND VIA EXTRUSION

The plasticity mechanism for via extrusion was examined for two TSV structures with different grain sizes, where the average grain size was found to affect the average mechanical properties of the TSV, and consequently via extrusion.

### 3.3.1 Test structure

Two TSV samples with large grains (LG) and small grains (SG) were studied. The dimensions of LG and SG TSVs were identical at 5.5 μm ×55 μm (diameter × height), and

the thickness of both wafers were 780 μm. Microstructure analysis by EBSD found that the average grain size of LG vias was 3.86 μm, which was about 36% larger than that of SG vias of 2.84 μm (Fig. 3.18). Both LG and SG TSV samples were fabricated using a standard via-middle process with completed front-end-of-line (FEOL) and back-end-of-line (BEOL) structures. Different electroplating chemistries were used for via filling but similar high temperature post-plating annealing (400-430$^{o}$C) was carried out before the BEOL layers were deposited.




(a) (b)

Figure 3.18. Crystal orientation maps of (a) small grain (SG) vias and (b) large grain (LG) vias.

### 3.3.2 Via extrusion

With the BEOL layers on top of the wafer surface, via extrusion was measured from SEM images of the via cross-sections. The average extrusion was about 118.6 nm for SG via and 147.8 nm for LG via. The BEOL layers in both samples sustained damages due to extrusion, where the extent of the damages being more severe in the LG sample. Cracks in

BEOL layers and delamination between the via top and the BEOL stacks were found in LG samples, while only deformed BEOL layers were observed in SG samples. The grain size and extrusion for the SG and LG TSVs are plotted in Fig. 3.19, and the average grain size and the via extrusion are summarized in Table 3.2

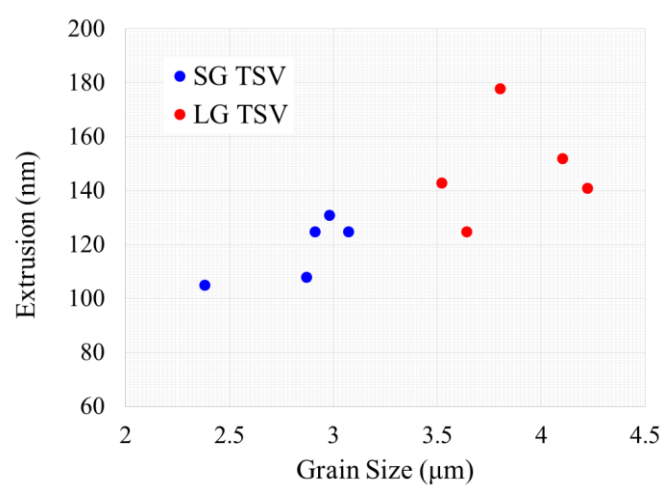



Figure 3.19. Correlation between grain size and via extrusion for TSV-A and TSV-B.

Table 3.2. Averaged grain sizes and via extrusion for LG and SG vias.

| | $\overline{D}$ (μm) | Via extrusion (nm) |
|---|---|---|
| SG TSV | 2.84 | 118.6 |
| LG TSV | 3.86 | 147.8 |

### 3.3.3 Nanoindentation measurement of mechanical properties

To study the mechanical properties of the Cu vias, nanoindentation measurements were carried out. FIB was used to remove the BEOL layers and expose the via surface.

Quasi-static indentations were performed at the via top surface in a Hysitron TI 950 TriboIndenter® system with a Berkovich diamond tip. A two-segment load vs. time profile was obtained at a loading/unloading rate of 100 nN/s with a peak load of 800 μN. The measured load (P) - displacement (h) responses for LG and SG vias were plotted in Fig. 3.20.

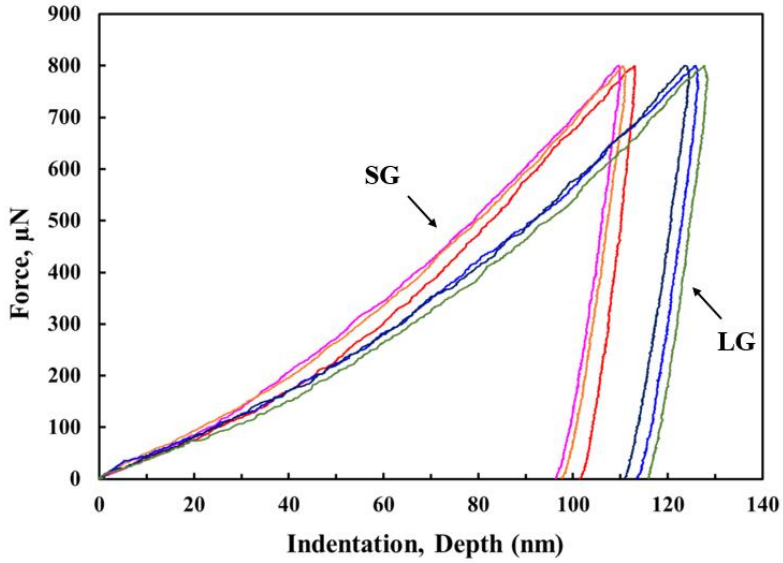



Figure 3.20. Load-displacement curves obtained from nanoindentation measurements for LG and SG TSVs.

Using the Oliver-Pharr method, the elastic moduli of the vias were deduced from the unloading curves [90]. The average reduced modulus was found to be 117 GPa for the SG vias and 93 GPa for the LG vias. The elastic modulus of LG vias was lower than what typically expected for electroplated Cu (~110 GPa) [39], which might be related to the grain structures near the top surface of the via. Figure 3.20 shown that for the same peak load, $P_{max}$, the maximum displacement, $h_{max}$, and the depth of the residual impression, $h_c$, were both smaller for SG vias. This led to a larger hardness, $H = P_{max}/A_C$ of 1.63G

Pa for SG vias, comparing to H=1.35 GPa for LG vias. Using a method described in a previous study, finite element analysis (FEA) was conducted to simulate the nanoindentation process [91], and the yield strength deduced was 250 MPa for SG vias and 190 MPa for LG vias.

### 3.3.4 Grain size effect on via extrusion

A clear correlation between the grain size and amount of extrusion can be seen in Fig. 3.19. It was well known that the grain size in a material could affect the dislocation movement and the yield strength, as commonly described by the Hall-Petch grain strengthening model:

$$\sigma_y = \sigma_o + \frac{k_y}{d} \tag{3.14}$$

where $\sigma_y$ was the yield strength, $\sigma_o$ was the starting stress for dislocation movement, $k_y$ was the strengthening coefficient. The Hall-Petch relationship suggested that TSVs with large grains would have smaller yield strength, which was consistent with the results obtained for the LG and SG vias. Considering the analysis described in the previous section, it was then expected that TSVs with large grains would have more plastic yielding and thus more extrusion. This could be seen in Fig. 3.21 when the analytical model was applied to calculate the via extrusion in SG and LG TSVs for different thermal loads using the material properties measured from nanoindentation.

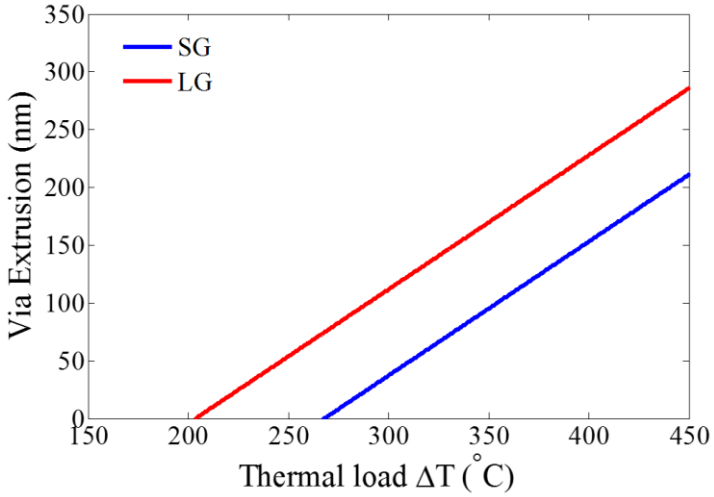



Figure 3.21. Via extrusion as a function of thermal load, $\Delta T = T_{max} - RT$, calculated by the analytical model for SG and LG TSVs.

It needs to be emphasized again that the analytical model only considered plastic yielding by dislocation glide as the dominant extrusion mechanism. The TSV microstructure and mass transport process, which can also contribute to via extrusion in these samples, were not considered. More detailed discussion of via extrusion including these factors will be presented in Chapter 4.

## 3.4 DISCUSSION AND SUMMARY

An interesting observation from AFM was that the extrusion profiles were not uniform and seemed to contour with the local grain structures near the top of the via, particularly evidenced by the donut shape at 400°C. Such an observation is in agreement with results from a previous study [92]. This suggests that the local plasticity of individual grains near the top could be important in controlling the amount of via extrusion. In a recent study by IMEC, via extrusion was investigated as a function of the process temperature and for two groups of via with sizes of 5x50 µm and 10x100 µm [88]. Large ensembles of

vias were used to measure the stochastic behavior and search for optimal post-plating anneal. Via extrusions were found to follow a lognormal distribution, where the average via extrusion at 50% was about half for the smaller TSVs as expected because of the lower thermal stresses. However, the largest extrusions at 99.9% of the lognormal distribution were found to be about the same for both sets of TSVs, independent of via size and post-plating anneal conditions. This result is important since in general, the overall reliability of a system containing many TSVs is determined by the largest TSV extrusions, i.e. the weakest link, in spite of their small percentage (about 0.1%). The problem is statistical in nature and the tail distribution of the largest extrusions would be the limiting factor for the overall system reliability. This problem is of significant interests but requires specially designed statistical test structures for further investigation. This is beyond the scope of this work and will be proposed for future studies.

In this chapter, via extrusion, an important yield and reliability issue for 3D integration, was analyzed. Synchrotron x-ray microdiffraction technique was introduced to probe the local stress and material properties near the via/Si interface. Local plasticity at the via/Si interface near the top of the via was observed and the result was consistent with the via extrusion behavior. The results from the synchrotron x-ray microdiffraction provided direct experimental evidence to support the plasticity mechanism of via extrusion. An analytical model and FEA were used to describe the via extrusion caused by plasticity. Other aspects of the via extrusion problem were discussed.

The via extrusion analysis described above is based on a simple 3D elastic-plastic model where the TSV is considered to be homogenous with average material properties and the effect of grain structure is taken into account only through the yield strength via the Hall-Petch relationship. While the model is capable in demonstrating that plasticity is important in controlling via extrusion but there are important grain structure effects that

can affect via extrusion. Such effects are important although were not taken into account and will be discussed in the following chapter.

# Chapter 4: Materials and Processing Effects on Via Extrusion

In Chapters 2 and 3, stress relaxation by grain growth and local plasticity mechanism have been discussed by treating TSV as homogeneous with average material properties. In this chapter, additional relaxation mechanisms that cause via extrusion, in particular diffusional creep, are discussed by comparing different TSV test structures. The microstructure effects, including contribution from grain boundary and interfacial diffusion, are discussed. Potential solutions to minimize grain growth by suppressing diffusion are proposed and demonstrated.

## 4.1. DEFORMATION MECHANISM IN TSV STRUCTURE

Deformation mechanisms have been extensively studied for bulk Cu and Cu thin films. In general, for bulk Cu at low temperatures ($T<0.5T_m$, $T_m$ is the melting point in K), plastic deformation is dominated by dislocation glide where multiple independent slip systems operate. At high temperatures ($T>0.5T_m$), creep mechanism aided by stress-driven diffusion is a major contribution to plastic deformation, and the material shows rate-dependent plasticity. The creep mechanism can be further divided into: (1) power law creep by thermally activated dislocation glide or combination of dislocation glide and climb, and (2) diffusional creep involving stress-driven atomic diffusion. Diffusional creep can be further classified as "Nabarro-Herring creep", which is lattice diffusion-limited and "Coble creep", which is grain boundary diffusion-limited [83], [93]–[95]. Frost and Ashby have constructed deformation mechanism maps for bulk materials based on rate equations that govern different mechanisms as a function of stress (normalized by shear modulus, $\mu$), grain size and temperature (normalized by the melting temperature, $T_m$) for various materials. An example of a deformation mechanism map for bulk Cu with grain size of 0.1 mm is shown in Fig. 4.1.

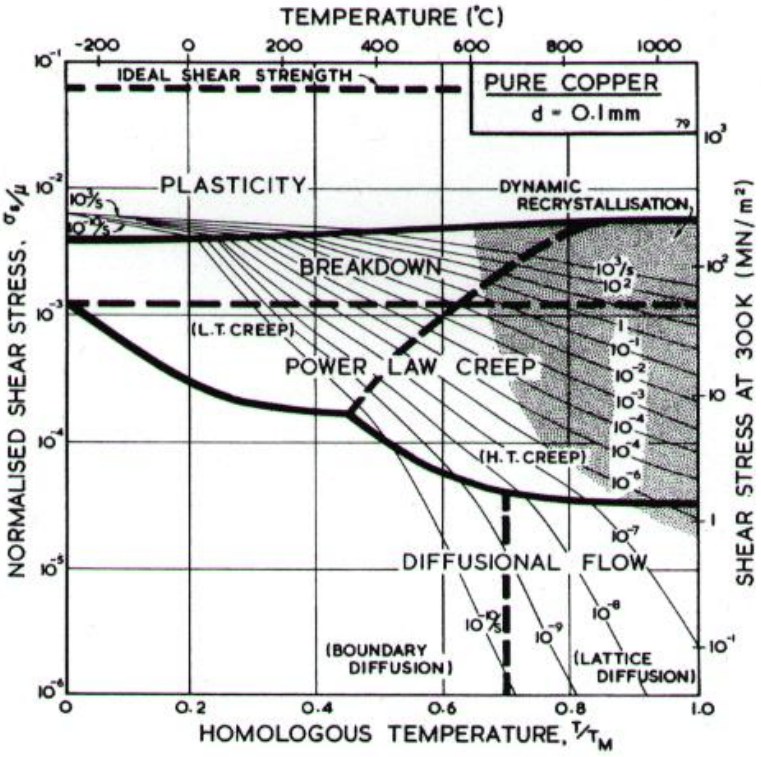



Figure 4.1. A deformation mechanism map for Cu with a grain size of 0.1mm [93].

For Cu thin film, substrate curvature methods have been extensively used to study the deformation mechanisms for both passivated and unpassivated films, which were found to be very different from that of bulk Cu [96]–[100]. Cu thin film deposited on a substrate with thickness in the micron range is typically highly textured with columnar grain structures. Stresses in the film can be relaxed by dislocation glide and diffusional creep. When the adhesion between the film and substrate is good, dislocation glide is often limited by dislocation source supplied by the interface instead of obstacles. Below 0.5 $T_m$, creep in the film involves atomic diffusion along the grain boundaries to and from the film surface. Good film adhesion constrains creep and noticeably improves film strength at high temperatures [96], [99], [101]–[104]. Suppressing surface diffusion, for example through

the application of a passivation film, can reduce diffusional creep by inhibiting the source of migrating atoms or vacancies [40], [96], [99], [100], [105]. Illustrations of the relaxation mechanisms in unpassivated and passivated film, as well as the thermo-mechanical behaviors of unpassivated film, are shown in Fig. 4.2 [99].

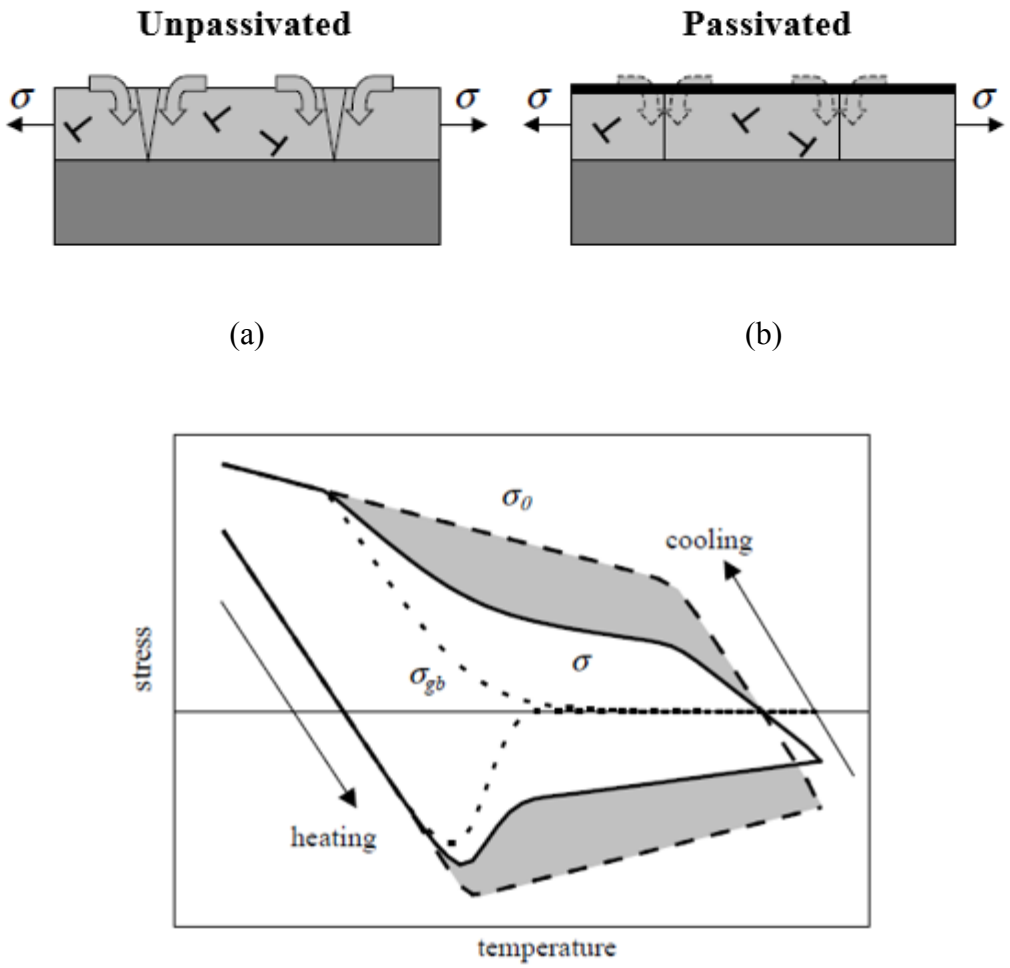



Figure 4.2. Stress relaxation mechanism for (a) unpassivated and (b) passivated films for $T<0.5T_m$. In unpassivated film, stresses are relaxed by glide and constrained diffusional creep. In passivated film, stresses are relaxed only by dislocation glide. (c) Illustration of stress evolution in unpassivated Cu film during thermal cycling. Shaded area is the average stress relaxed by diffusional creep. [99]

Quantitatively, it has been proven difficult to describe the mechanism underlying the thermos-mechanical behaviors in Cu thin films. Many studies have been performed using constitutive creep equations for bulk Cu to model the stress-temperature behavior of

Cu thin film. Steady state strain rate equations for bulk Cu have also been used to analyze relaxation measurements in an attempt to quantify the creep mechanisms [40], [97]–[101]. While qualitative description of the behaviors of Cu thin films has been reported, the thermos-mechanical models developed so far all lacks the ability to quantitatively describe the general behaviors of Cu thin films. This is primarily because Cu thin film is characterized by a biaxial stress state constrained by substrate, rendering very different relaxation mechanisms from bulk Cu. As a result, the constitutive equations derived for Cu bulk cannot be simply extended to thin films [100].

In this study, the discussion of the inelastic processes in TSV structures will be focused on three relaxation mechanisms, including: (1) microstructure evolution including grain growth, a mechanism that has been discussed in Chapter 2; (2) dislocation glide, either via athermal plastic yielding when the stress in the TSV exceeds the flow stress (yield strength), or by thermally assisted dislocation glide (power law creep); (3) diffusional creep with mass transport along grain boundary and along the via/liner interface. There mechanisms are chosen based on the deformation mechanism map while taking into account the common processing window and the microstructure evolution observed in TSVs.

The discussion on the deformation mechanisms in this chapter is mostly qualitative and inferred based on results from stress and material studies of three different TSV structures. In general, the stress characteristics and microstructure in TSVs are more complicated than thin films. As discussed in previous chapters, the stress is highly non-uniform in the TSV and the near-surface stress is important in controlling the driving stress and the deformation behavior. There is no equivalent of "Stoney's equation" to describe the stress state in TSV structures, making it difficult to quantitatively analyze the deformation mechanisms. In addition, the TSV samples used in this study were provided

by different sources and we had no control over the fabrication condition as well as the via dimensions and patterns on the wafers. It is, therefore, more difficult to delineate various factors affecting the deformation mechanisms. In spite of these limitations, useful information have been deduced from the experiments performed, which have led to potential approaches for improving via extrusion reliability of TSVs.

## 4.2. THERMO-MECHANICAL BEHAVIORS OF THREE TSV STRUCTURES

### 4.2.1. Test structures

In addition to TSV-A, which was studied in chapters 2 and 3, two additional blind via structures, referred to as TSV-B and TSV-C, were investigated in this chapter. TSV-B and TSV-C have the same dimension of 5.5 × 50 μm (diameter × height) and were fabricated using standard via-middle processing sequence but with different electroplating chemistry and post-plating annealing conditions. No annealing was carried out after electroplating for TSV-B, while TSV-C had been annealed at 430°C for 10min in Ar atmosphere after electroplating but before CMP. The via density in the wafer was about the same as TSV-A and TSV-C samples, which was about a third of that for TSV-B. The specifications of the three TSV samples are summarized in Table 4.1.

Table 4.1. Three TSV structures used in the study. $V_{Cu}/V_{ttl}$ was the volume density of Cu vias in the curvature sample.

| | Diameter, D (μm) | Height, H (μm) | Pitch, p (μm) | Post-plating annealing | EP Chemistry | $V_{Cu}/V_{ttl}$ |
|---|---|---|---|---|---|---|
| TSV-A | 10 | 55 | 40/50 | 100°C, 30 min | A | 0.0148 % |
| TSV-B | 5.5 | 50 | 40 | No annealing | B | 0.0475% |
| TSV-C | 5.5 | 50 | 40 | 430C for 10min | C | 0.0132% |

### 4.2.2. Curvature-temperature behaviors and microstructure analysis

The thermo-mechanical characteristics of the different TSVs were studied by substrate curvature measurement. The results are shown in Fig. 4.3 and will be discussed later.

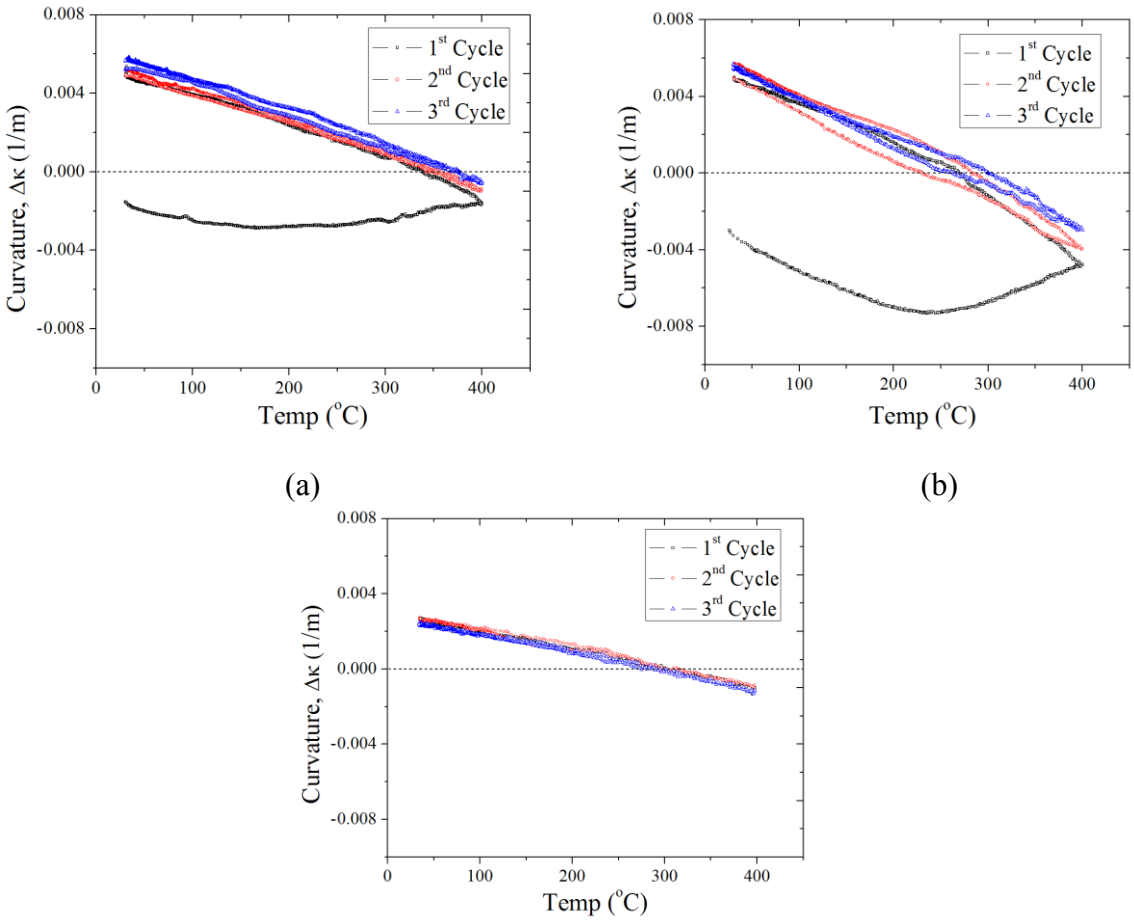
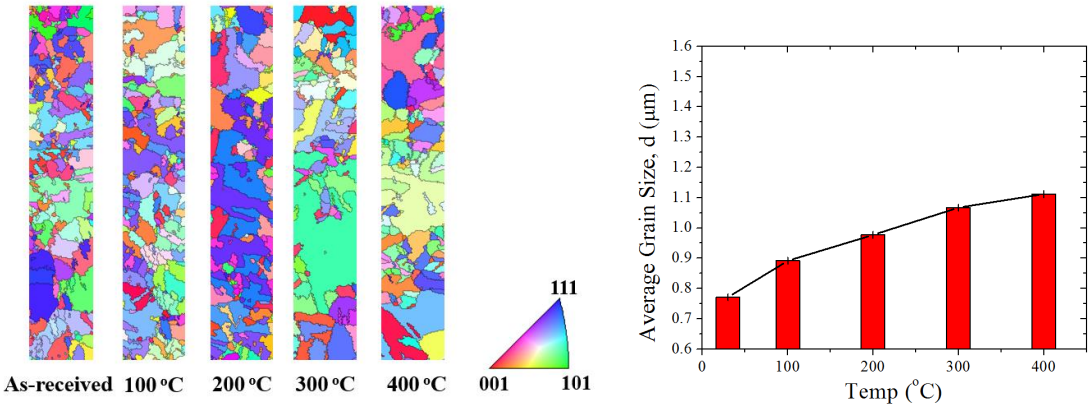
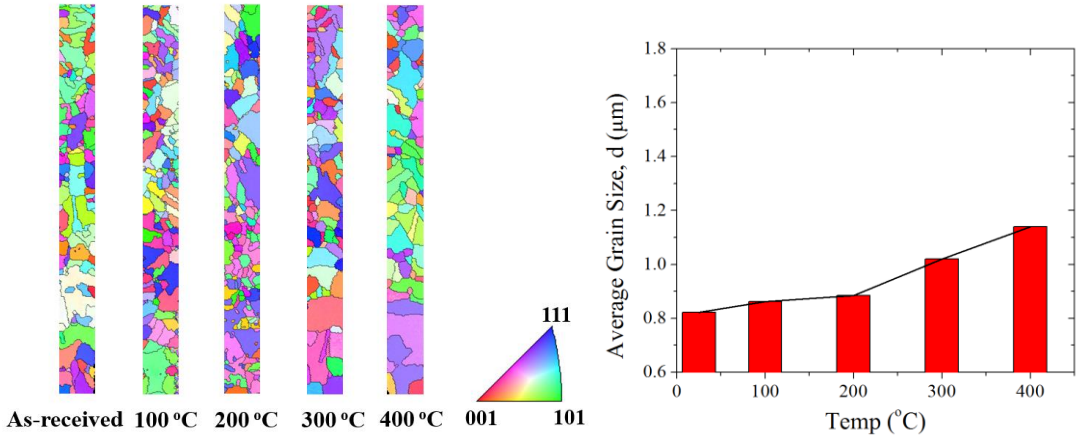



Figure 4.3. Curvature-temperature behaviors of (a) TSV-A, (b) TSV-B, and (c) TSV-C thermal cycled to 400°C for three times.

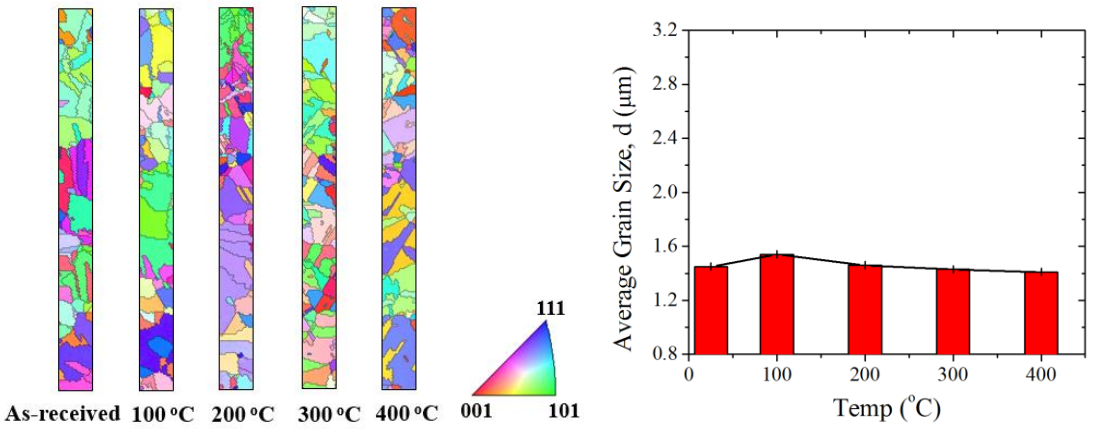
For TSV-B and TSV-C, microstructure analyses on vias subjected to single temperature cycling tests were conducted by EBSD, and the results are shown in Fig. 4.4, where previous results from Chapter 2 for TSV-A are shown together for comparison.




(a)




(b)




(c)

Figure 4.4. EBSD crystal orientation map and grain sizes of vias after single temperature thermal cycling measurements for (a) TSV-A, (b) TSV-B, and (c) TSV-C.

Different grain growth behavior was observed for the three TSV structures. Continued grain growth can be seen in TSV-A, while no apparent grain growth was observed in TSV-C. For TSV-B, little change in the grain size was observed below 200°C, but more grain growth was observed beyond 200°C. In addition, the percentages of Σ3 and Σ9 types of twin boundaries for the three types of vias are summarized in Table 4.2. For each TSV structure, there is no systematic change in the amount of twin boundaries with increased thermal cycling temperatures. Overall, the amount of twin boundaries is the largest in TSV-C and smallest in TSV-B.

Table 4.2. Percentage of Σ3 and Σ9 boundaries in the as-received and thermal cycled vias for TSV-A, TSV-B, and TSV-C.

| | As-received (%) | | | 100°C (%) | | | 200°C (%) | | | 300°C (%) | | | 400°C (%) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | A | B | C | A | B | C | A | B | C | A | B | C | A | B | C |
| Σ 3 | 62.5 | 55.5 | 77.4 | 64.0 | 58.1 | 72.6 | 69.3 | 63.8 | 71.6 | 70.1 | 60.5 | 76.3 | 60.3 | 60.7 | 79.9 |
| Σ 9 | 10.9 | 10.9 | 11.4 | 10.7 | 8.5 | 8.2 | 9.1 | 9.3 | 9.1 | 12.9 | 8.6 | 6.7 | 9.4 | 8.7 | 7.8 |
| Total | 73.5 | 66.4 | 88.7 | 74.7 | 66.6 | 80.8 | 78.4 | 73.1 | 80.7 | 83.0 | 69.1 | 82.0 | 70.0 | 69.4 | 87.7 |

The curvature-temperature behavior of TSV-C could be understood based on the analysis for TSV-A in chapter 2. As a brief review, for TSV-A, grain growth occurred during the first heating half-cycle, thereafter, the microstructure became stabilized as the following cycles did not exceed the previous peak temperatures. Nonlinear relaxation due to grain growth was observed only in the first heating half-cycle, and the curvature was nearly linear during cooling and in subsequent cycles. For TSV-C, EBSD analysis revealed no apparent changes in the microstructure with increased thermal cycling temperature, suggesting that TSV-C had been annealed at a temperature exceeding that in thermal cycling, so that its microstructure remained stable during thermal cycling experiments. For TSV-B, EBSD measurement found limited grain growth below 200°C, which coincided with the linear curvature behavior observed in the initial heating half-cycle. However, there were three distinct features in Fig. 4.3b for TSV-B that are difficult to explain based on the grain growth analysis alone. First, in the first heating half-cycle, the relaxation observed at high temperatures (above 300°C) was much larger in comparison with that of the TSV-A, and with a much faster relaxation rate. Second, there was noticeable nonlinearity in the beginning of the first cooling half-cycle when the temperature was above ~300°C. Such behaviors could not be explained by grain growth and seems to imply that additional

relaxation processes related to creep at high temperatures had occurred in TSV-B. Finally, in the last three cycles to 400°C, although large-scale relaxation was not observed, the heating and cooling curves deviated slightly from linearity but did not overlap. Instead, small but noticeable hysteresis loops were formed, which were further evidences of additional plastic deformation in TSV-B.

The different relaxation behavior in TSV-B at high temperatures could be more clearly seen from isothermal measurements where all three samples were heated to 400°C and held for 1 hour before cooling to RT. The curvature changes as a function of time (t) are plotted in Fig. 4.5. To compare the different extent of relaxation under an isothermal relaxation condition, the curvatures at t=0 for the three samples were shifted to the same point in plotting Fig. 4.5. Both TSV-A and TSV-C showed minimal curvature relaxation at 400°C, indicating that the magnitude of creep was rather small in those samples under the isothermal test condition. Significantly more relaxation was observed in TSV-B, indicating that a creep behavior due to grain boundary diffusion and/or interface diffusion, occurred in TSV-B.

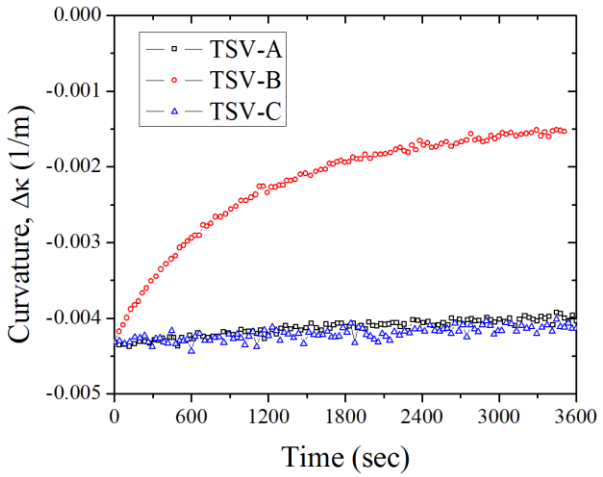



Figure 4.5. Isothermal relaxation measurement at 400°C for TSV-A, TSV-B and TSV-C.

### 4.2.3. Measurement of via extrusion

Via extrusion in all three TSV samples was examined by AFM scans on samples subjected to a single thermal cycling to 400ºC. The extrusions for as-received vias before thermal cycling were also measured as references. The extrusion profiles extracted across the top of the vias are plotted in Fig. 4.6.

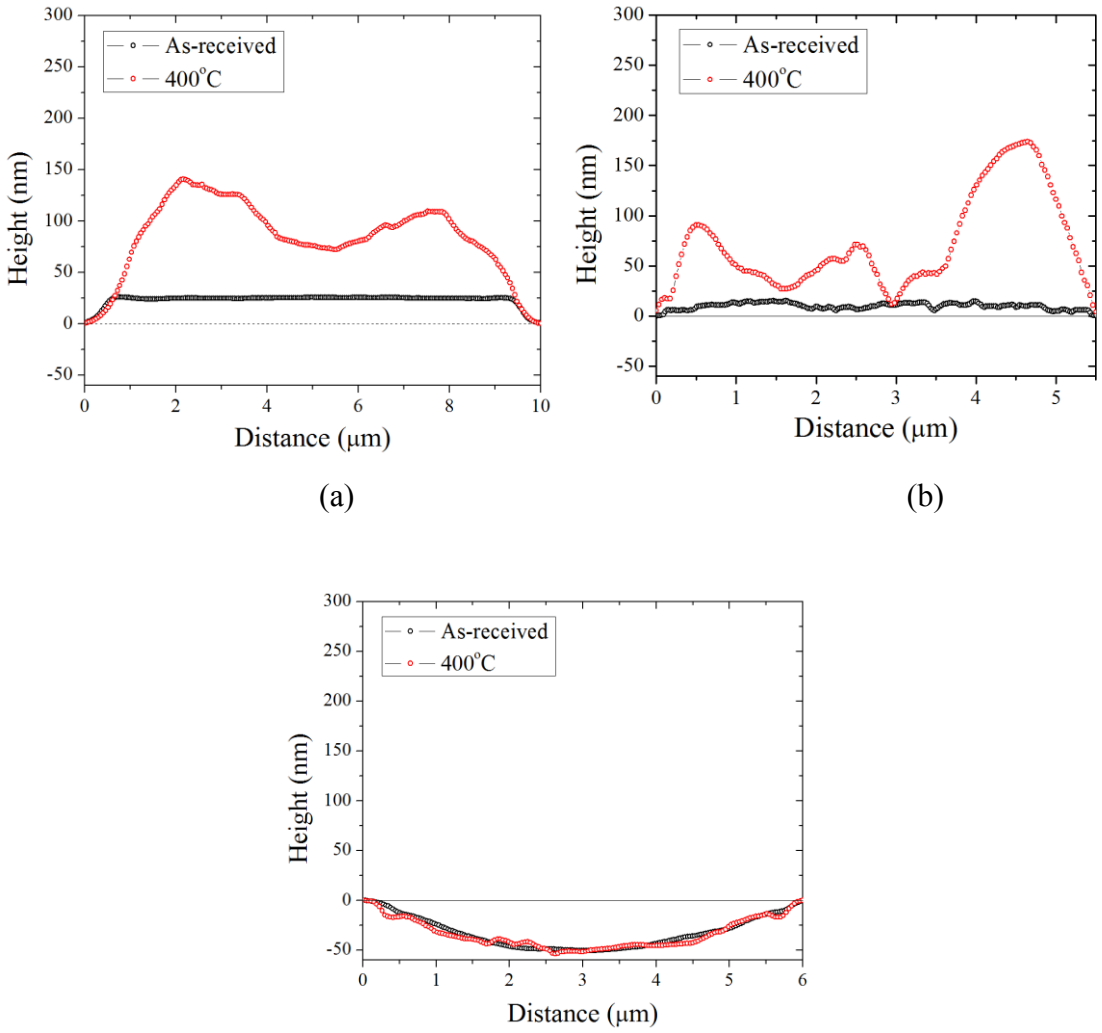



Figure 4.6. Height profile across the via diameter for (a) TSV-A, (b) TSV-B, and (c) TSV-C.

For TSV-C (Fig. 4.6c), the depression of the via top surface was due to the dishing effect induced by chemical-mechanical polishing (CMP). There was no apparent via extrusion after thermal cycling to 400$^{o}$C, and surface profile of the via after thermal cycling almost coincided with that of the reference via, except for slightly increased surface roughness seen near grain boundaries. This was to be expected, as results in the previous sub-section showed that TSV-C behaved elastically and no inelastic processes seemed to exist. For TSV-A, since the curvature relaxation in Fig. 4.5 is small and almost overlapped with that of TSV-C, it was assumed that creep also had minimal contribution to the inelastic processes in the structure. Based on the discussion in chapters 2 and 3, grain growth and dislocation glide-related plastic deformation were likely the mechanisms responsible for the extrusion observed in Fig. 4.6a. For TSV-B, all three mechanisms seemed to be present to cause the observed extrusion shown in Fig. 4.6b. It was also observed that significantly more extrusion occurred close to the rim of the via in TSV-B, while near the center of the via, the amount remained low. Such an observation suggests that comparing to grain boundary diffusion, diffusion along the via/liner interface can contribute more to the extrusion of TSV-B, although at this time, it is not possible to separate the contributions from these two mechanisms.

### 4.2.4. TOF-SIMS study of incorporated additives

In this study, we are interested to study the effect of electroplating chemistry used to produce the TSV samples, which is generally known to be important in controlling the Cu microstructure and materials properties of the TSVs [53], [106]–[108]. Using time-of-flight secondary ion mass spectrometry (TOF-SIMS), the additive elements incorporated in the three TSV samples were measured. The TOF-SIMS measurements were conducted

on the via cross-sections prepared by FIB. Both the reference samples (as-received) and samples after thermal-cycling to 400ºC were measured for all three types of vias. Since TOF-SIMS was a surface sensitive technique, the cross-sections were first sputtered with $Cs^+$ ion to remove surface contaminations due to air exposure, and then $Bi_1^+$ primary beam was raster-scanned to measure $Cl^-$, $F^-$, $S^-$, and $CN^-$, which were elements commonly incorporated in electrodeposited Cu [20], [108]. For each sample, the element counts were normalized to the amount of $Cu^-$. The results are summarized in Table 4.3.

Table 4.3. Counts of $Cl^-$, $F^-$, $S^-$, and $CN^-$ elements in the via.

| Counts / Element | TSV-A | | TSV-B | | TSV-C | |
|---|---|---|---|---|---|---|
| | Reference | 400ºC | Reference | 400ºC | Reference | 400ºC |
| $Cl^-$ | 3.11 | 1.33 | 1.26 | 0.26 | 337.6 | 334.1 |
| $F^-$ | 87.8 | 17.91 | 10.9 | 4.63 | 147.2 | 213.5 |
| $S^-$ | 1.48 | 0.31 | 0.60 | 0.15 | 7.3 | 10.8 |
| $CN^-$ | 3.88 | 1.12 | 0.61 | 0.30 | 114.3 | 87.2 |

For both TSV-A and TSV-B, the counts of $Cl^-$, $F^-$, $S^-$, and $CN^-$ elements decreased after thermal cycling to 400ºC, which could be related to the out-diffusion of additive species during grain growth [53]. For TSV-C, the concentrations of additive elements were comparable before and after thermal cycling. In this case, the out-diffusion of additives was limited, leading to a stable grain structure during thermal cycling. It appeared that TSV-C had much more additive elements in the Cu via than the other two TSV samples, and TSV-B had the least amount of additives. This suggests that the high

concentration of additives helped to stabilize the grain structure in TSV-C, likely by inhabiting boundary migration [53], [109]. It should be pointed out that such quantitative comparison was valid only when the Cu matrix was identical in all samples [110]. Since the different electroplating conditions could result in variation of ionization probabilities in the Cu vias, such direct comparison should be regarded as semi-quantitative. The measured additive concentration could also be affected by the non-uniform distribution of additive elements in the via, depending on where the cross-section was cut through the via.

### 4.2.5. Discussion

Comparing the results from the three different TSV structures, there appear to be different relaxation mechanisms in TSV structures responsible for the different via extrusions observed. First, the difference can be attributed to the diffusion characteristics of grain boundaries which are interfaces separating two crystals with different crystallographic orientation. At the grain boundary, the arrangement of atoms is disordered and thus can serve as paths for fast vacancy diffusion [95]. Stress driven atomic flow along the via/liner interface and grain boundaries can both contribute to diffusive creep for via extrusion. In the present study, it was difficult to delineate the contributions from either diffusion processes. However, AFM scans of the extrusion profile in TSV-B had consistently shown a rim of larger extrusion close to the via/liner interface. Assuming surface diffusion was not a limiting factor, this suggests that the interface in TSV-B can serve as a faster diffusion path to supply the mass transport for via extrusion. The result also suggested that reducing either, or both, the interface diffusion and grain boundary diffusion would be beneficial in reducing via extrusion in TSV-B. One possible approach is to use a cap layer to retard the diffusion of Cu atoms and vacancies. This approach is similar in principle as the use of metal cap layers at the nanoline/trench interface for Cu

interconnects, which have been proven effective to improve EM performance [111], [112]. In this study, the cap layer effect was found to be effective in several initial studies and the results are discussed in the following sub-section.

## 4.3. EFFECT OF CAP LAYER ON VIA EXTRUSION

### 4.3.1. Test structure

The test structure with a cap layer is illustrated in Fig. 4.7. In one study, a 16nm Co thin film was deposited using e-beam evaporation as the cap layer onto the top surface of TSV-B wafer. TSV wafers without the cap layer was used as the reference. Both the reference and the sample with Co cap layer were annealed at 400ºC for 1 hour with a heating rate of about 6ºC/min in a forming gas atmosphere.

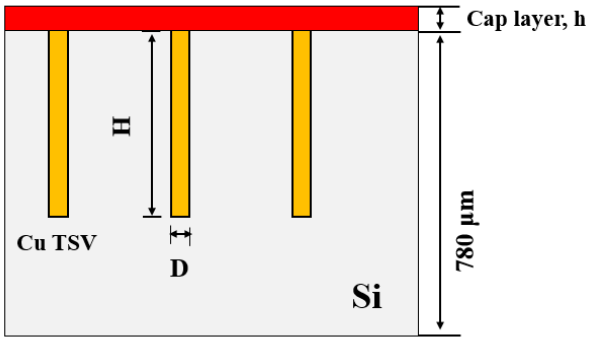


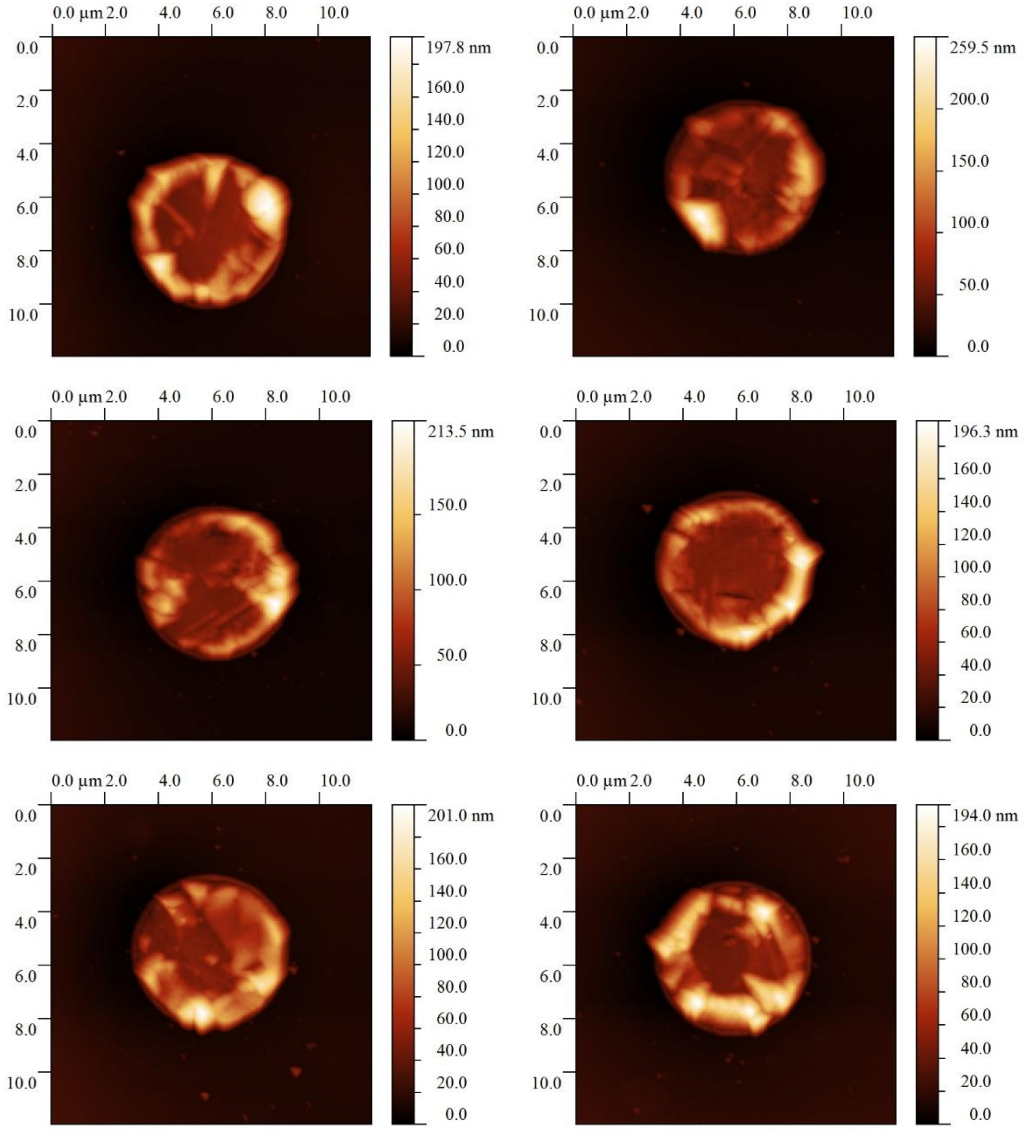

Figure 4.7. Illustration of the cap layer with a thickness of h, on a wafer containing blind vias with dimension of D×H.

### 4.3.2. Via extrusion measurement

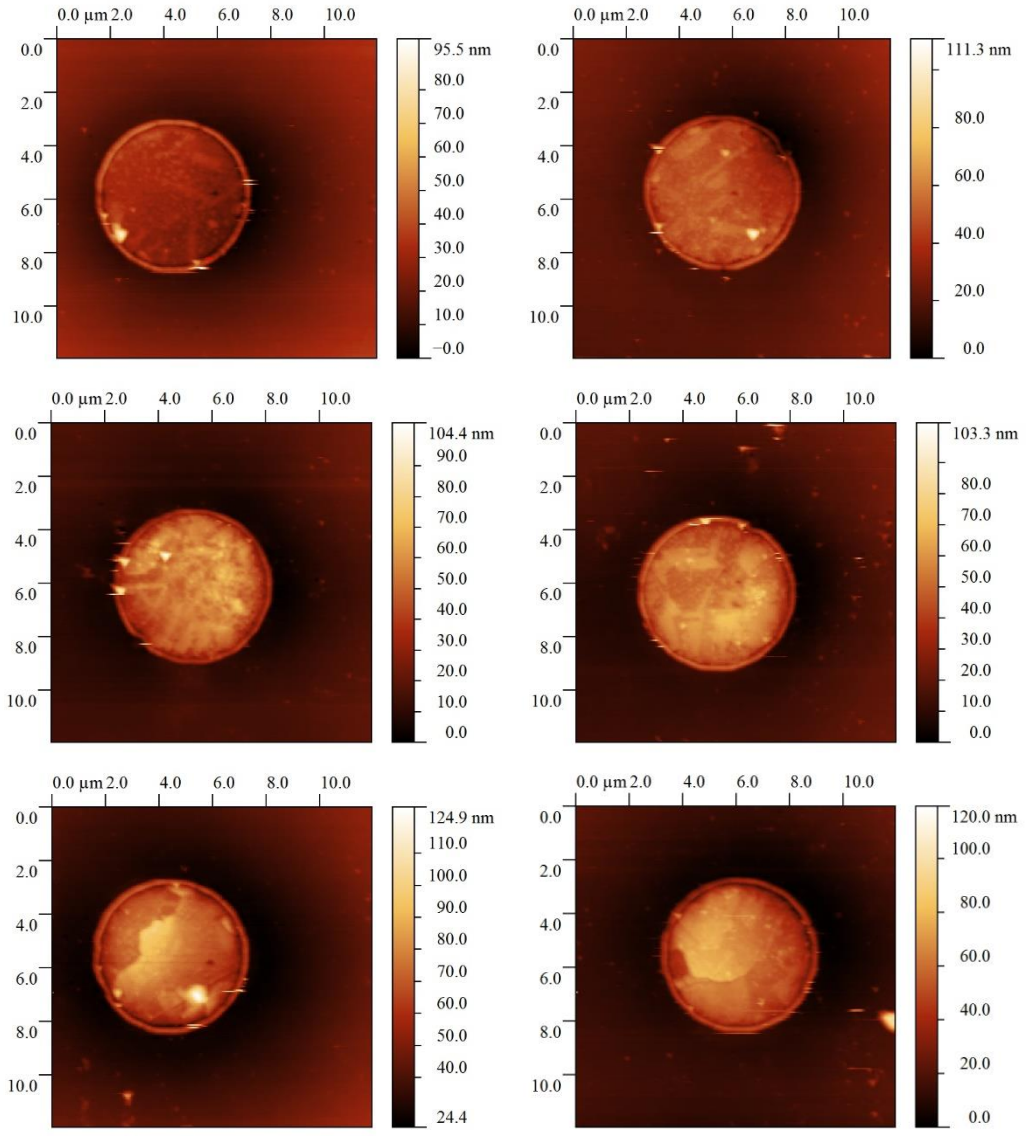
Before annealing, the height of the via, $h_0$, was obtained by AFM scan to be 5.6 nm. After annealing, AFM scans were performed for several vias in both samples to examine via extrusion. Based on the AFM scans, the average height of each via, $h_{avg}$, was obtained by averaging the height of all scanned points in the via, along with the maximum

height, $h_{max}$, in the via. Two extrusion values were then calculated: the average extrusion, defined as $\Delta_{avg} = h_{avg} - h_0$, and the maximum via extrusion, defined as $\Delta_{max} = h_{max} - h_0$.

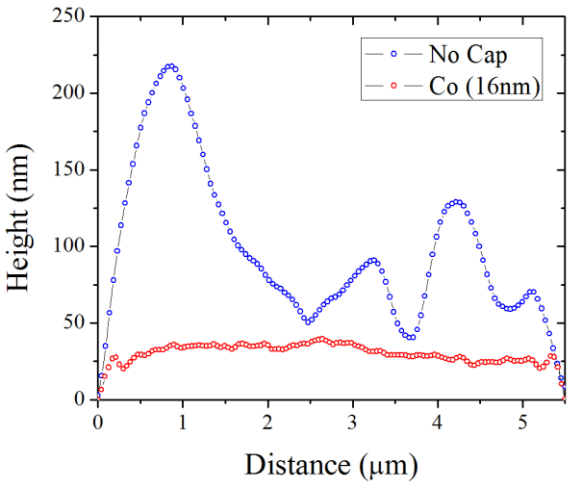
Representative AFM images for vias with and without a Co cap layer are shown in Figs. 4.8a and 4.8b. Line profiles across the width of a via for each case were extracted and plotted in Fig. 4.8c. Comparing to the reference sample, via extrusion was found to be significantly smaller in the capped sample. The height variation within the via was also much reduced in the capped sample.


0.0 µm 2.0 4.0 6.0 8.0 10.0
0.0 2.0 4.0 6.0 8.0 10.0
197.8 nm 160.0 140.0 120.0 100.0 80.0 60.0 40.0 20.0 0.0
259.5 nm 200.0 150.0 100.0 50.0 0.0
213.5 nm 150.0 100.0 50.0 0.0
196.3 nm 160.0 140.0 120.0 100.0 80.0 60.0 40.0 20.0 0.0
201.0 nm 160.0 140.0 120.0 100.0 80.0 60.0 40.0 20.0 0.0
194.0 nm 160.0 140.0 120.0 100.0 80.0 60.0 40.0 20.0 0.0

(a)


0.0 µm 2.0 4.0 6.0 8.0 10.0
95.5 nm
111.3 nm
104.4 nm
103.3 nm
124.9 nm
120.0 nm

(b)

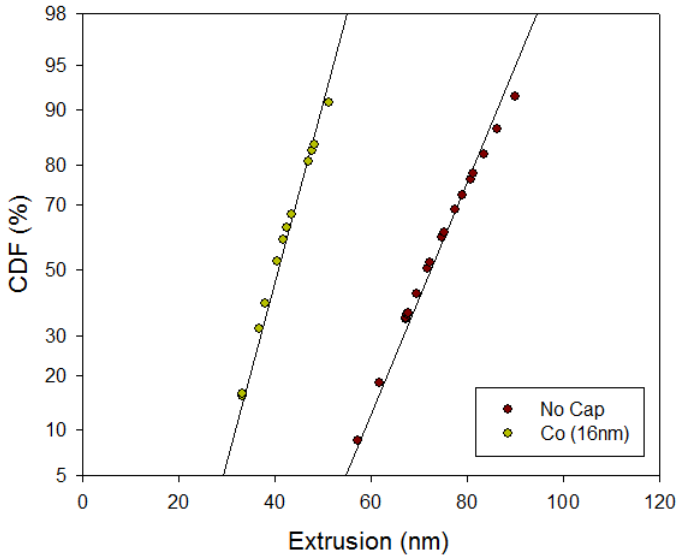



(c)

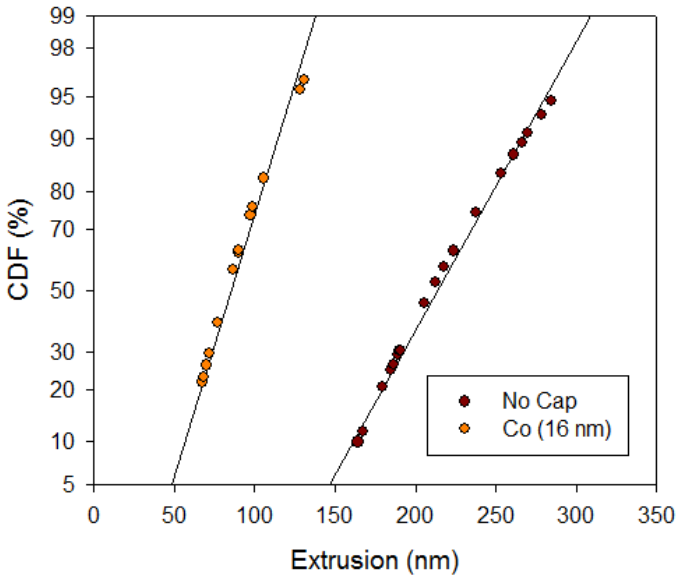
Figure 4.8. AFM scans of via extrusion for TSV-B (a) reference vias without a cap layer, (b) vias with 16nm Co cap after annealing at 400°C for 1 hr, and (c) height profiles for a reference sample and a sample with 16nm Co cap layer.

### 4.3.3. Effect of cap layer on statistics of via extrusion

For both samples, the average extrusion, $\Delta_{avg}$, and maximum extrusion, $\Delta_{max}$, were fitted to lognormal distributions. The probability density function (PDF), $f(\Delta)$, can be expressed as $f(\Delta) = \frac{1}{\sqrt{2\pi}\sigma\Delta} exp\left[-\frac{(ln\Delta - ln\Delta_{50})^2}{2\sigma^2}\right]$, where $\Delta$ is the height of via extrusion, $\sigma$ is the standard deviation which describes the width of the distribution and $\Delta_{50}$ is the median via extrusion. The cumulative distribution function (CDF), $F(\Delta)$, can be obtained by integrating PDF over $\Delta$ as $F(\Delta) = \int_0^{\Delta} f(\Delta)$, and $F(\Delta)$ represents the probability of a random via in the total population having extrusion smaller than $\Delta$. For both the reference and capped samples, the CDFs of the average extrusion, $\Delta_{avg}$ , were plotted in Fig. 4.9a, and the CDFs for the maximum extrusion, $\Delta_{max}$, were plotted in Fig. 4.9b. The straight lines suggested a lognormal fit to the extrusion data.




(a)




(b)

Figure 4.9. Cumulative distribution function (CDF) plots of (a) average via extrusion and (b) maximum via extrusion for the reference sample and sample with 16nm Co cap.

Figs 4.9a and 4.9b shown that for both average extrusion and maximum extrusion, the median extrusion values ($\Delta_{50}$) and the width of the distribution ($\sigma$) decreased when a cap layer was present. More specifically, this result showed that the cap layer was able to reduce the median of $\Delta_{max}$ by about 64%. The spread of the distribution was also reduced when the cap layer. This resulted in much improved statistical distribution in the maximum extrusion. In other words, the probability of failure due to via extrusion will be reduced by the cap layer.

### 4.3.4. Effect of cap layer on stress relaxation

To examine the effect of cap layer on stress relaxation, substrate curvature measurements were performed on the reference sample and the sample with the 16nm Co cap. To simulate the annealing condition, both samples were heated at 6$^{o}$C/min to 400$^{o}$C and held for 1 hour, before cooling down to RT. The curvature changes as a function of temperature are plotted in Fig. 4.10. For comparison, the curvature at t=0 was artificially shifted to the same point. It was clear that the presence of a Co layer reduced the rate of stress relaxation, as seen from the difference of curvature changes. The result showed that the mass transport responsible for stress relaxation is reduced due to the addition of the Co cap layer. The implication on via extrusion is discussed in the following subsection.

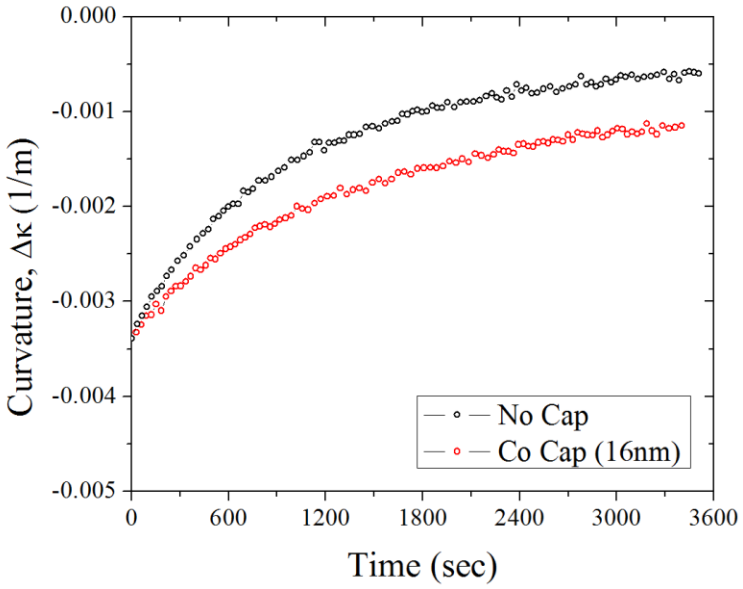



Figure 4.10. Isothermal annealing of the reference sample and sample with 16nm Co cap layer at 400°C for 1 hour.

### 4.3.5. Discussion

The results from this study show that a very thin Co layer (16nm) was able to reduce via extrusion rather significantly. This effect can be understood by considering the mass transport process that contributes to via extrusion. As illustrated in Fig. 4.11, atomic diffusion, driven by stress gradients along the grain boundaries and/or the via/liner interface, will accumulate Cu atoms on the via surface. When the cap layer is present, similar to the case for Cu thin films, surface diffusion will be suppressed due to reductions in the mass transport of atoms and vacancies at grain boundaries and interfaces [99], [111], [112]. This effectively suppresses the mass transport for via extrusion, as illustrated in Fig. 4.11b. Another possibility is that the cap material, in this case Co, had reacted with the Cu underneath forming an alloying layer at the interface or had partially dissolved into the Cu grain boundaries. In either case, the interfacial or grain boundary mass transport could also be reduced due to an alloying effect [113]. Further studies following this initial

demonstration of the cap layer are needed to elucidate the mechanism of the cap layer effect on via extrusion. Such a study will be proposed.

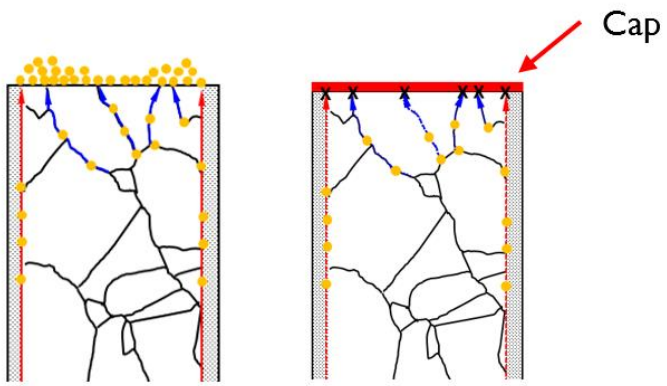



Figure 4.11. Illustration of the effect of cap layer on via extrusion. (a) Without cap layer, diffusion along grain boundary and via/Si interface can results in via extrusion. (b) Cap layer eliminates diffusion and reduces extrusion.

After the initial demonstration of the Co cap layer effect, we were searching for other candidate materials as cap layers to reduce via extrusion. In a preliminary study, 50nm Ti, Ni, and Al films were deposited as alternative cap layers on TSV-B samples. The same annealing experiments were carried out and the via extrusion was measured by AFM. All cap materials were able to substantially reduce via extrusion, although Co and Ni seemed to be the most effective, whereas Al was the least effective. The results suggested that the cap layer effect provides a general approach to reduce via extrusion. With further studies, it would be possible to optimize the material and thickness of the cap layer to reduce via extrusion more effectively. Such studies will be proposed in the final chapter for future research.

## 4.4. DISCUSSION

### 4.4.1. Mechanisms for via extrusion

Three relaxation mechanisms for via extrusion have been proposed: (1) stress relaxation by grain growth, (2) plastic yielding by dislocation glide, and (3) diffusional creep along grain boundaries and/or the via/liner interface. So far, by comparing the results from experiments performed on three different TSV structures, each of these mechanisms has been identified and qualitatively discussed. In TSV-B, the results suggested that all three mechanisms were present, and diffusional creep was likely to be dominant based on the study in sub-section 4.3. For TSV-A, a preliminary study found that a Co cap layer can reduce extrusion subjected to annealing, although to a lesser extent comparing to TSV-B. Therefore, it is assumed that in TSV-A, diffusional creep was present but small, as the stress relaxation behavior in Fig. 4.5 was more similar to that of TSV-C. Since no obvious extrusion was observed in TSV-C, it was assumed that none of the mechanisms were active in TSV-C. These mechanisms for the three TSV structures are summarized in Table 4.5.

Table 4.4. Summary of via extrusion mechanisms in TSV-A, TSV-B, and TSV-C

| Mechanisms | TSV-A | TSV-B | TSV-C |
|---|---|---|---|
| Grain growth | Present throughout thermal cycling | Present beyond 200ºC | Not observed |
| Dislocation glide | Confirmed by peak broadening in μSXRD | To be investigated | Minimal |
| Diffusional creep | Small but present | Large relaxation | Minimal |

### 4.4.2. Approaches to reduce via extrusion

An interesting observation was that an "ideal" TSV structure was achieved in TSV-C, where inelastic processes causing via extrusion seemed to be absent. Although the detailed fabrication conditions for TSV-C were not known, by re-examining TSV-C, certain guidelines to improve via extrusion reliability can be deduced.

First of all, TSV-C had been annealed at 430ºC, which helped to stabilize the grain structure during thermal cycling tests. In the past few years, the importance of stabilized grain structure had been realized by the industry, and a high temperature post-plating annealing step had been widely incorporated in the via middle process after electroplating of Cu and before CMP [34], [114], [115]. Although this approach appeared straight-forward, there are other factors which have to be considered in order to implement the step effectively. First, TSVs with different geometry and electroplating chemistry may have different grain growth behaviors, therefore an annealing recipe that was effective for one set of TSVs may not be ideal for another set. The annealing conditions, including the ramp rate, peak temperature, duration, and atmosphere, need to be optimized, not only for the

purpose of reducing via extrusion but the effect on fabrication cost also has to be considered.

Second, TOF-SIMS revealed TSV-C contained a relatively large amount of additive elements incorporated during electroplating. Typically, the additives were segregated at grain boundaries, which could affect the properties of TSV in several ways. For example, the impurity elements could pin grain boundary movement and increase the resistance for dislocation glide. The impurity elements can also affect microstructure evolution in the TSV and the thermos-mechanical properties of the Cu vias which in turn, changes the via extrusion characteristics. Again further studies are required to optimize the annealing process.

Third, it appeared that diffusion, both along grain boundaries and along the via/liner interface, was very limited in TSV-C. In Cu, it is known that cohesive twin boundaries, especially $\sum 3$ boundaries, have significantly smaller diffusivity than high angle boundaries [116]. Microstructure studies have found that TSV-C has the largest amount of $\sum 3$ boundaries, which would be beneficial in reducing grain boundary diffusion. Similar observation was reported in a recent study by IMEC, where smaller extrusion was observed for vias with larger portion of twin boundaries [117]. At the via/liner interface, it was expected that strong adhesion at the interface would improve the resistance to diffusion [59], [118]. A good adhesion at the interface also limits the dislocation source, therefore contributing to increased yield strength in the TSV, which is similar to the role of substrate adhesion in thin film structures [99], [104]. Overall, to reduce diffusional creep, it is desirable to have a TSV structure with a large amount of twin boundaries and good adhesion at the sidewall interface, particularly for the top section near the via surface. It is expected that the deposition parameters, thickness, roughness, and residual stress of the liner will affect the interface properties. So far, it has been difficult to quantify the effect

of the via/liner interface on via extrusion, largely due to the lack of proper test structures and suitable techniques. To obtain a desirable grain structure with a large amount of twin boundaries will likely require optimization of the electroplating process, the annealing conditions, and the properties of the seed layer. This is an area that is important but has not systematically studied so far. In addition, a cap layer can also reduce the mass transport responsible for diffusive creep, as demonstrated before for Cu interconnect lines. In general, the material chosen for the cap layer must be compatible with the current microelectronics fabrication processes. Candidate materials included Co, Ti, Ni and Al and their compounds, such as NiAl. Adding the cap layer, however, introduces additional fabrication steps and increases the manufacturing cost, which needs to be taken into consideration in its implementation.

### 4.4.3. Comparing microstructure of TSVs to Cu interconnect lines.

Grain structure of the TSV plays an important role in controlling via extrusion. In addition to grain boundary diffusion, it is known that through grain boundary strengthening, the yield strength is directly related to grain size by the Hall-Petch relationship. Furthermore, Cu is highly anisotropic, with the elastic modulus along the <111> direction about 3x of that along the <100> direction (Fig. 4.12) [119]. The elastic anisotropy further complicates the inelastic processes, in that the grain size and orientation can affect the amount and the distribution of plastic deformation and thus via extrusion.

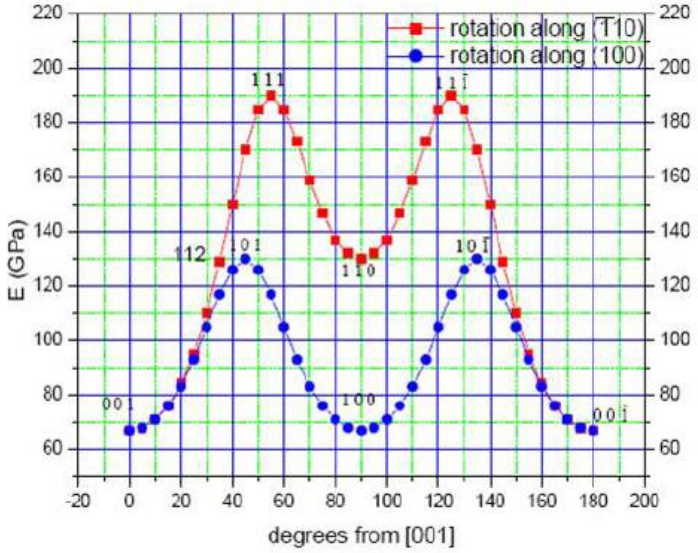



Figure 4.12. Elastic modulus of Cu plotted along different crystal directions [119].

Grain growth in Cu thin films has been extensively studied and found to be driven by minimization of the overall energy in the system, including contributions from grain boundaries, surfaces, interfaces, stress/strain energies, and pinning due to impurities [53], [120]. In Cu, surface energy is the smallest for close-packed {111} planes, while strain energy is the lowest for {100} planes [120]. Therefore, minimization of strain energy would favor the {100} texture, while minimization of surface energy would favor the {111} texture. For electroplated Cu films, the competition between surface energy and strain energy minimization has led to thickness-dependent textures, which is illustrated in Fig. 4.13 [120].

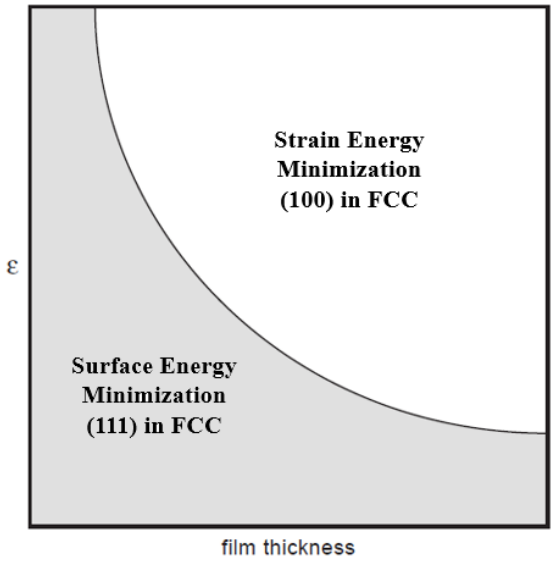



Figure 4.13. A texture map showing the expected texture favored by grain growth as a function of the elastically accommodated strain and the film thickness (adapted from [120]).

For Cu nanolines used in advanced interconnect technology at 90nm (120nm line width) and 45nm nodes (70nm linse width), the texture is dominated by <111> orientations normal to the trench sidewall, as driven by minimization of sidewall interface energy. With further dimensional scaling, for 28nm node (45nm line width) and 22nm node (40nm line width), the texture transitioned to that of <111> along the length of the trench [121], [122]. This is shown in Fig. 4.14. Concurrently, as the line width scaled down from 90nm node to 22nm node, a reduction of twin boundaries has been observed. Such texture changes have important implications on EM reliability of interconnect lines [122] and the effect for via extrusion has to be better understood.

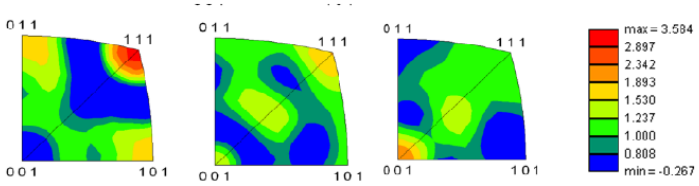
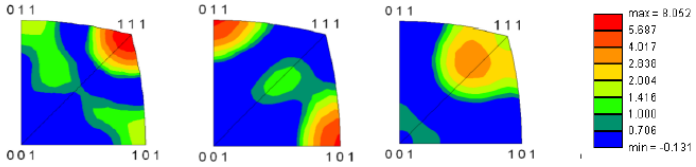
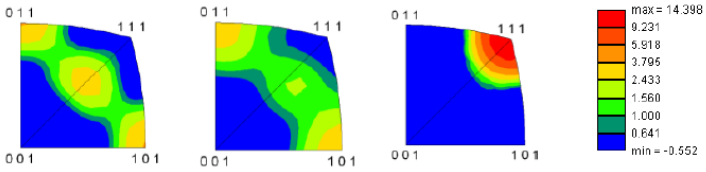
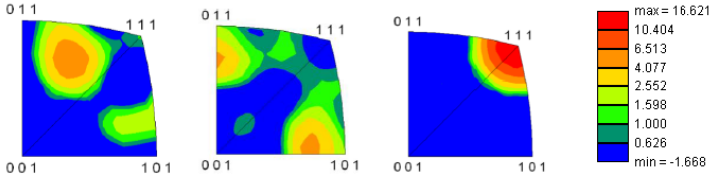
| Technology | Line Width (nm) | Trench Width | Trench Normal | Trench Length | Texture Strength (MRD) |
|---|---|---|---|---|---|
| 90 nm | 120 |  | | | |
| 45nm | 70 |  | | | |
| 28nm | 45 |  | | | |
| 22nm | 40 |  | | | |



Figure 4.14. Texture evolution of Cu nanolines from 90nm to 22nm nodes [122].

TSV structures have some resemblance to Cu nanolines in that both are confined structures and are filled with electroplated Cu. However, due to the size difference, the microstructure in TSVs is very different from that of Cu interconnect lines. When textures in the three TSV structures are plotted, no preferred texture can be observed. This is shown in Figs. 4.15-4.17, where RD direction corresponds to the axis of the TSV, TD direction is along the radial direction, and ND direction is perpendicular to the normal of the via cross-section. Instead, a significant amount of twin boundaries are found in TSV structures, as previously shown in Table 4.2. The presence of twin boundaries and the lack of texture in

TSVs are likely to be related, as multiple twinning of {111} grains produces new orientations and subsequently weakens the overall texture [48]. Considering the role of twin boundaries in reducing grain boundary diffusion, such a random texture is preferable. It is possible that when the dimension of TSVs becomes smaller with future technology, the effect of the via/liner interface may become large enough to increase the texture in the TSV, which will be an interesting topic for further studies.

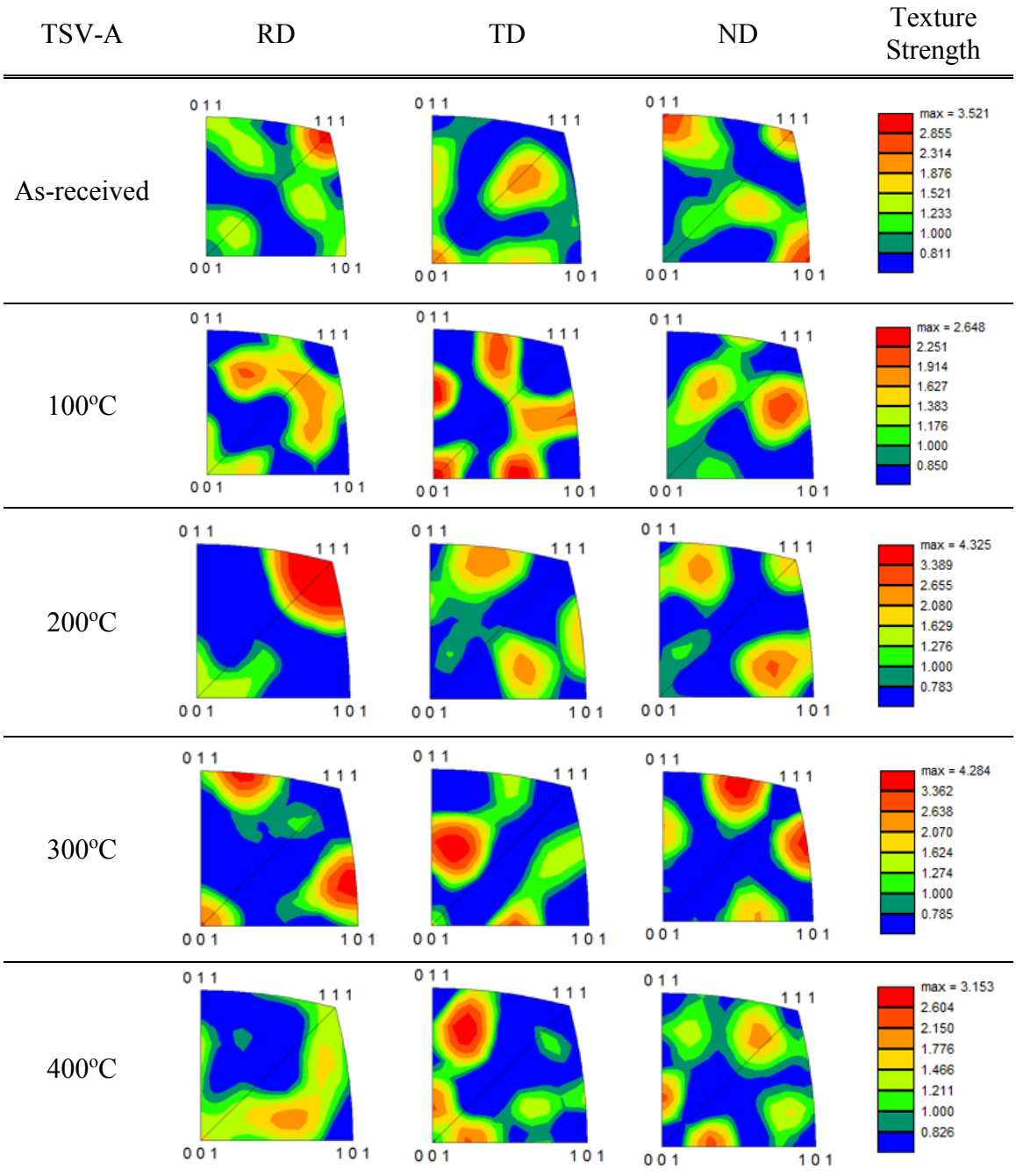



Figure 4.15. Texture in TSV-A for as-received and thermal cycled vias.

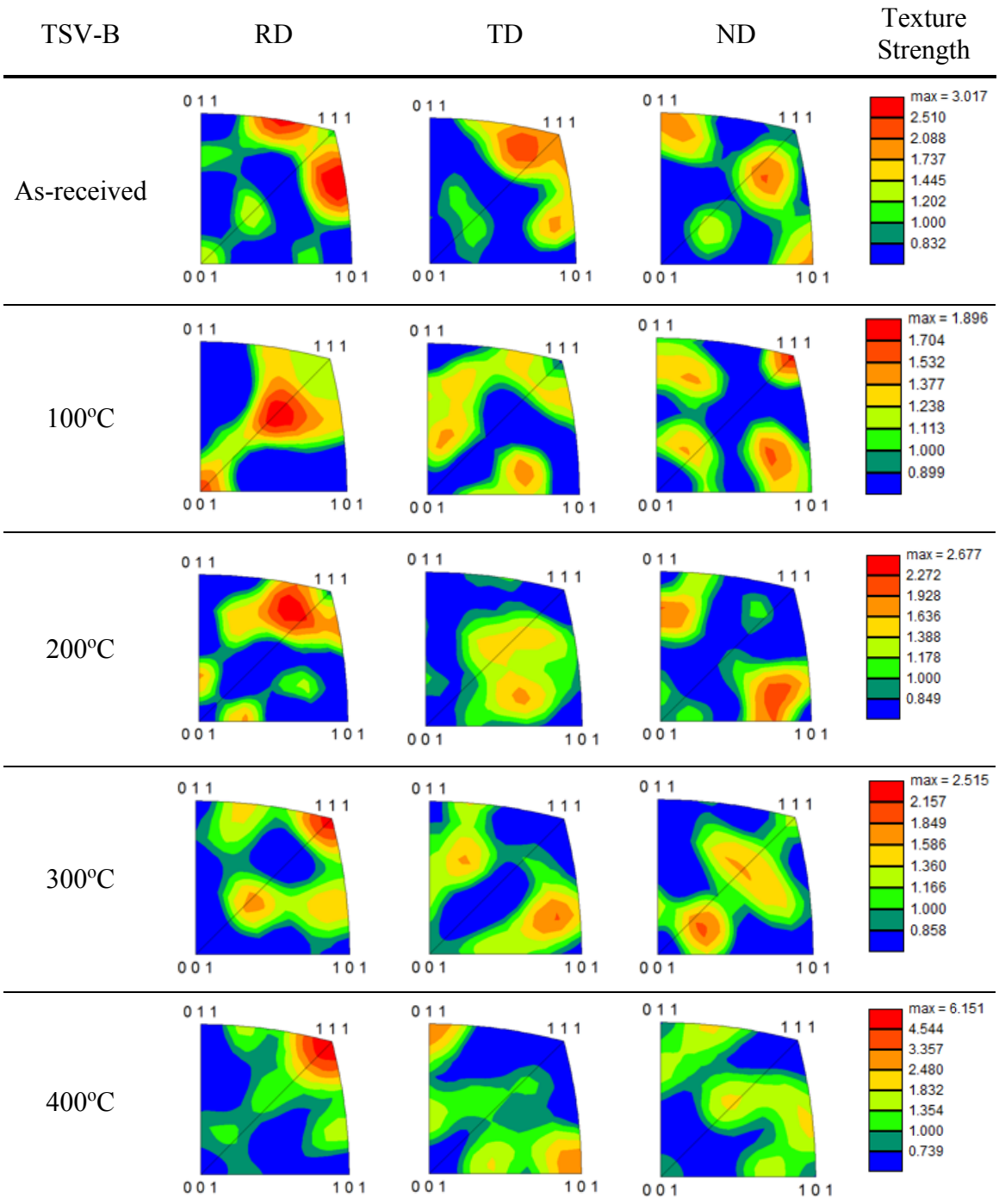



Figure 4.16. Texture in TSV-B for as-received and thermal cycled vias.

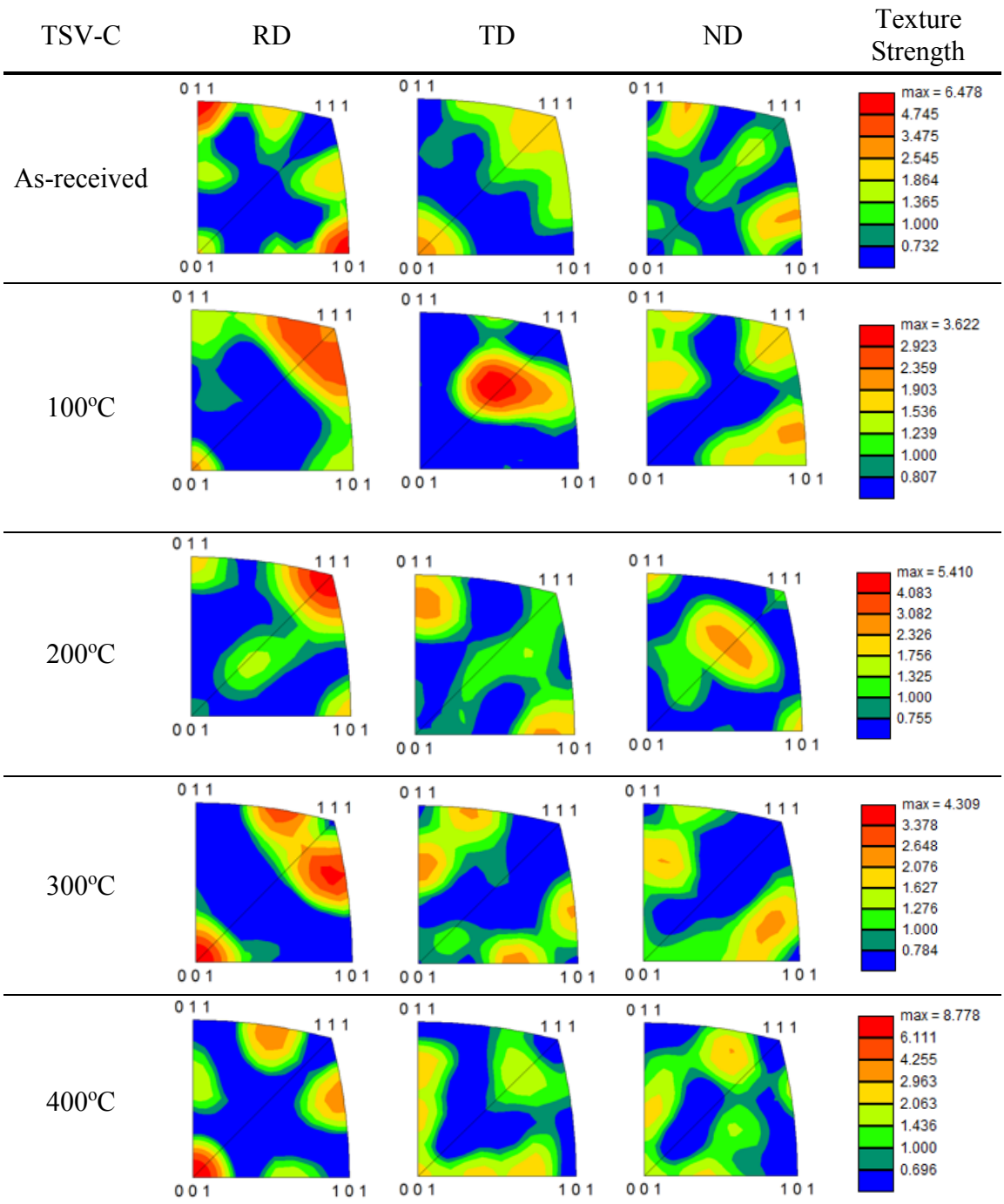



Figure 4.17. Texture in TSV-C for as-received and thermal cycled vias.

## 4.5. SUMMARY

In this chapter, three TSV structures have been examined and different via extrusion behaviors were observed. The mechanisms of via extrusion were discussed based on the inelastic processes in these TSV structures. The results qualitatively show that to reduce and eventually eliminate via extrusion, three basic mechanisms need to be addressed. These include: (1) minimize microstructure change, (2) increase the yield strength in Cu and/or to reduce the stress level in the TSV, and (3) reduce mass transport at grain boundaries and interfaces. Microstructure of the TSV plays an important role in controlling all three inelastic processes. Eventually, to improve the via extrusion reliability requires optimization of the via fabrication process, especially the electroplating chemistry, linear/seed layer properties, and annealing conditions. This provides a general guideline for future development of reliability TSV structures.

# Chapter 5: Stress and Reliability of 3D Die Stacks

In Chapters 2-4, the discussion on stress and reliability was focused on individual TSVs. In this chapter, synchrotron x-ray micro-diffraction technique is applied to measure the thermal stress in a multi-stack Hybrid Memory Cube (HMC) structure. The thermal stress in the die stack structure due to material property mismatch between the chips, solder bumps, and the packaging materials is discussed with FEA.

## 5.1. TEST VEHICLE

The Hybrid Memory Cube (HMC) technology represents the latest development in 3D die stacking. In the HMC test structure, a memory stack consisted of eight DRAM dies was stacked on a logic die, which was attached to a substrate. The top die and bottom die in the DRAM stack was DRAM 7 and DRAM 0, respectively. This is illustrated in Fig. 5.1. The fabrication of the HMC was similar to that described in Chapter 1. Each thin die contains TSVs made by via-middle processes, FEOL devices, and complete BEOL wiring structures. The via diameter was 8 μm and the thin dies were connected by Sn based microbumps.

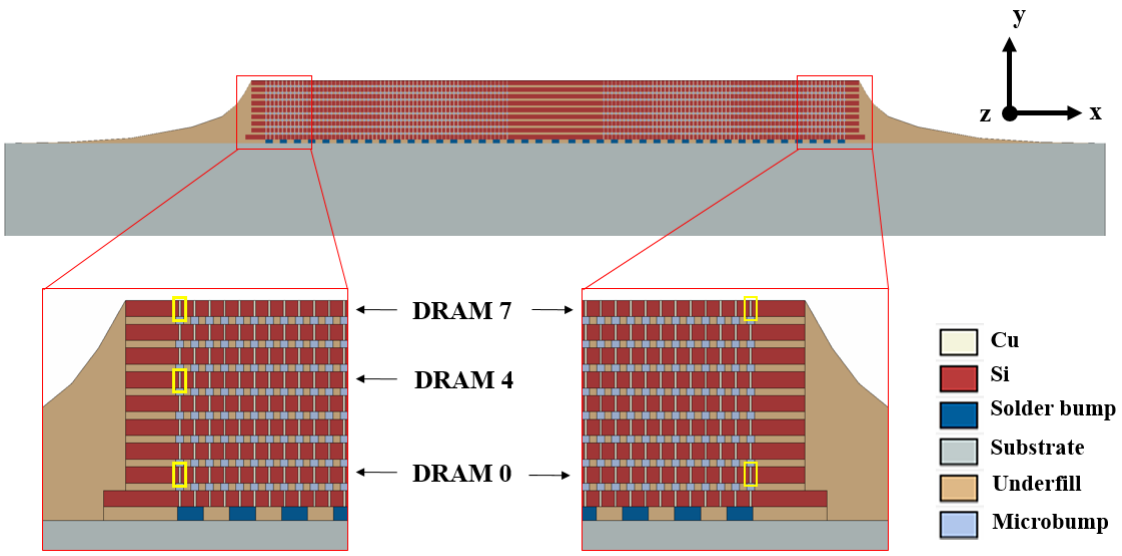



Figure 5.1. Schematic of the HMC test vehicle. The measured vias are in DRAM 7, DRAM 4, and DRAM 0 at the left edge of the package, and in DRAM 7, DRAM 0 at the right edge of the package, which are highlighted.

## 5.2. SYNCHROTRON X-RAY MICRODIFFRACTION MEASUREMENTS

A number of techniques have been developed to measure stresses for TSV structures, such as micro-Raman spectroscopy and wafer curvature method [41], [123]–[126]. However, these techniques cannot be readily applied to die-stack structures due to the multi-die stack geometry where TSVs are embedded. As discussed in Chapter 3, using highly focused and high brilliance x-ray beam, synchrotron x-ray microdiffraction technique has the unique capability of high-resolution measurement at precise locations in the sample with minimal sample preparation[71], [127]. The capability of synchrotron x-ray microdiffraction to study stress characteristics of key components in 3D die stacks, including the Cu via, Si, and the μ-bumps, has been demonstrated [128], [129].

For the x-ray microdiffraction measurement, the HMC sample was polished parallel to a row of TSV/microbump without exposing the Cu vias. Scanning white beam x-ray microdiffraction (μSXRD) were carried out at beamline 12.3.2 of the Advanced Light Source (ALS) at the Lawrence Berkeley National Laboratory (LBNL). The spectral range of the x-ray used in the measurement was 5-22KeV and the x-ray beam size was about 0.8 μm × 0.8 μm FWHM. The HMC sample was mounted on a high precision stage in a 45$^{o}$ reflection geometry, and the x-ray microbeam was raster-scanned on the sample at 1 μm/step. The Laue reflection from each point in the scan matrix was collected and analyzed in the X-ray Microdiffraction Analysis Software (XMAS) using procedures described in Chapter 3.

To locate the TSVs embedded underneath the polished surface, x-ray fluorescence (XRF) maps similar to the one shown in Fig. 5.2 were collected with the software setup to count for photons within an energy range of 7.5 - 8.5 KeV, corresponding to the characteristic line of Cu. Based on the XRF intensity maps, a scan area of 30×70 μm was defined around the TSV of interest, whereby the diffraction patterns were collected. In this study, micro-diffraction measurements were performed around TSVs chosen in five locations in the stack, including one via each at the left and right edges of the package in DRAM 7, one via at the left edge of the package in DRAM 4, and one via each at the left and right edges of the package in DRAM 0, as illustrated in Fig. 5.1.

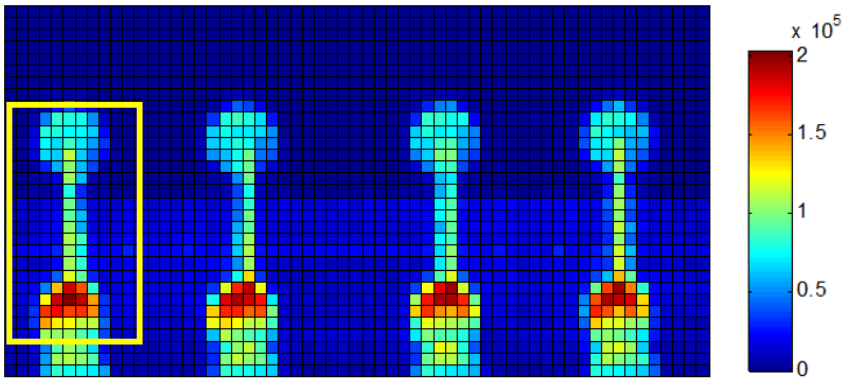



Figure 5.2. X-ray fluorescence map of Cu vias in one DRAM die in HMC. The yellow box illustrates the area for white beam scanning.

### 5.2.1. Measurement of stress in Si

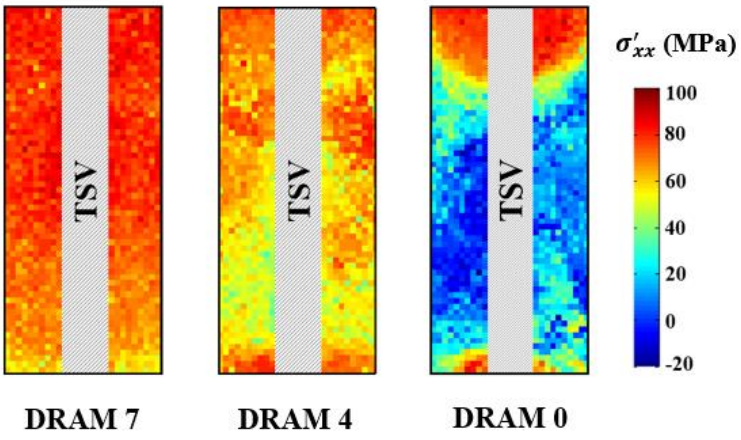
By indexing the diffraction patterns with respect to Si, the deviatoric strain tensor was obtained from the distortion of the unit cell. By following the constitutive relations, the deviatoric strain tensor can be converted to the deviatoric stress tensor [71]. The deviatoric stress tensor, $\sigma'_{ij}$, is defined in the following equation

$$\sigma_{ij} = \sigma'_{ij} + P = \begin{bmatrix} \sigma'_{11} & \sigma_{12} & \sigma_{13} \\ \sigma_{12} & \sigma'_{22} & \sigma_{23} \\ \sigma_{13} & \sigma_{23} & \sigma'_{33} \end{bmatrix} + \begin{bmatrix} p & 0 & 0 \\ 0 & p & 0 \\ 0 & 0 & p \end{bmatrix} \quad (5.1)$$

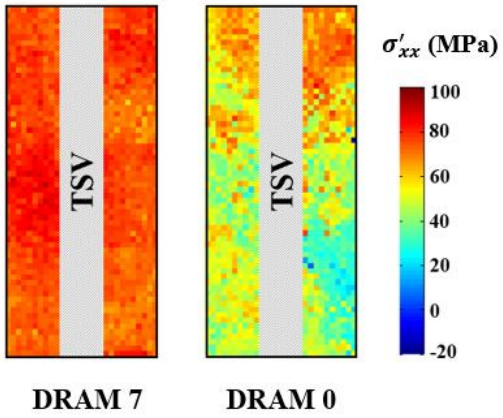
where $\sigma'_{ij}$ is the deviatoric stress and p is the hydrostatic stress with $p = (\sigma_{11} + \sigma_{22} + \sigma_{33})/3$. The error in the measured strain is reported $\pm 2 \times 10^{-4}$ and the resulting error in the stress is projected to be 15~25 MPa. The von-Mises stress can be calculated from the deviatoric stress components as

$$\sigma_{eq} = \sqrt{\frac{1}{2}[(\sigma'_{11} - \sigma'_{22})^2 + (\sigma'_{22} - \sigma'_{33})^2 + (\sigma'_{11} - \sigma'_{33})^2 + 6({\sigma'_{12}}^2 + {\sigma'_{13}}^2 + {\sigma'_{23}}^2)]} \quad (5.2)$$

In Figs. 5.3-5.6, the deviatoric stress components, $\sigma'_{xx}$, $\sigma'_{xy}$, $\sigma'_{yy}$, and $\sigma'_{zz}$ are plotted for the five vias measured.

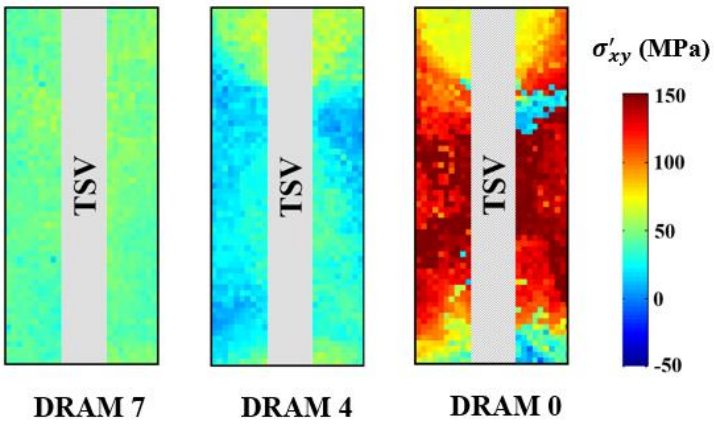



(a)

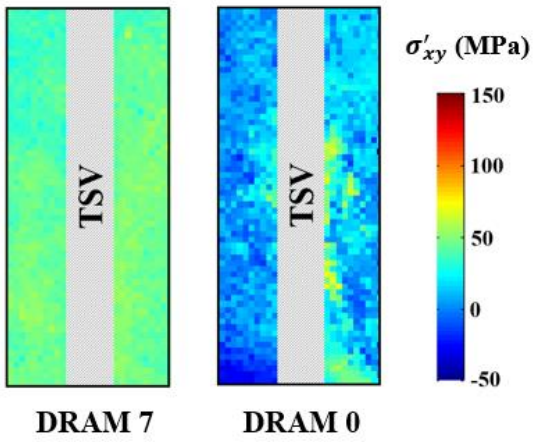



(b)

Figure 5.3. Deviatoric stress $\sigma'_{xx}$ for TSVs at (a) the left edge of the structure and (b) the right edge of the structure in different DRAM die levels.

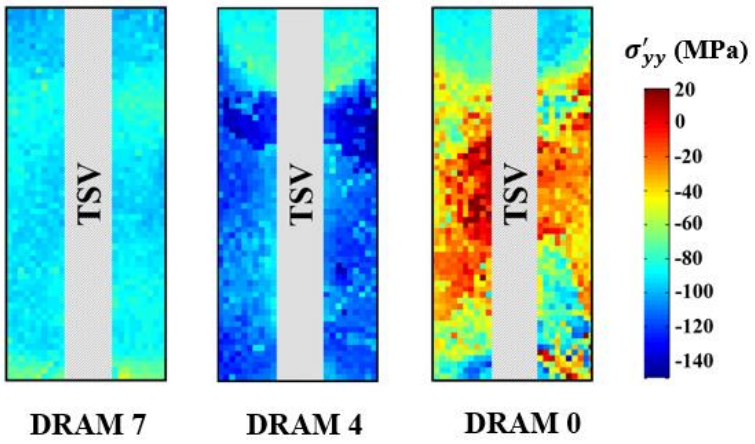



(a)

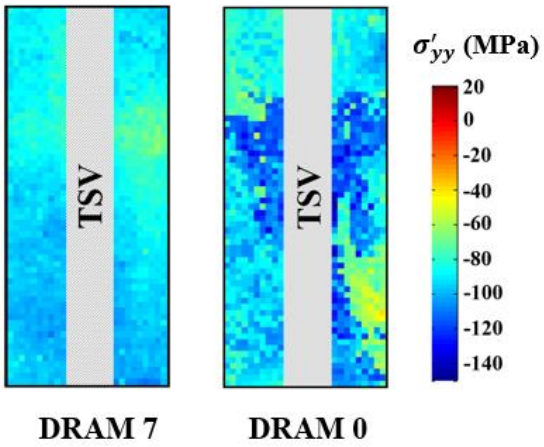



(b)

Figure 5.4. Deviatoric stress $\sigma'_{xy}$ for TSVs at (a) the left edge of the structure and (b) the right edge of the structure in different DRAM die levels.

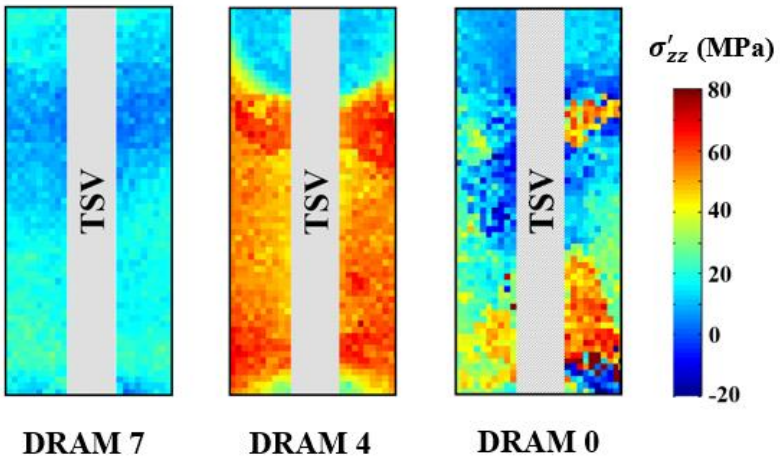



(a)

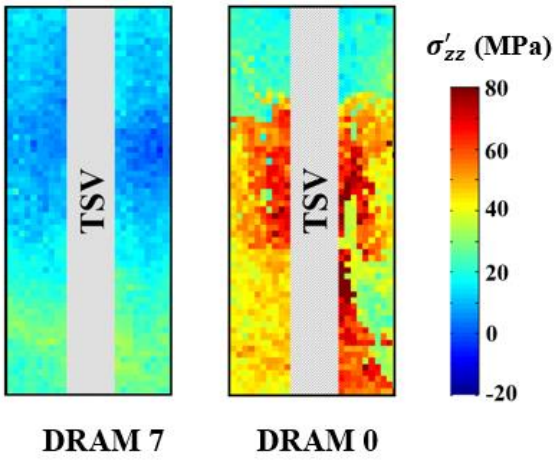



(b)

Figure 5.5. Deviatoric stress $\sigma'_{yy}$ for TSVs at (a) the left edge of the structure and (b) the right edge of the structure in different DRAM die levels.




(a)




(b)

Figure 5.6. Deviatoric stress $\sigma'_{zz}$ for TSVs at (a) the left edge of the structure and (b) the right edge of the structure in different DRAM die levels.

The results in Figs. 5.3a-5.6a for TSVs at the left edge of the die stack show a clear trend in stress distribution receding from the top DRAM 7 to the bottom DRAM 0 of the DRAM stack. In Fig. 5.3a, $\sigma'_{xx}$ is the largest at the top DRAM 7 of the stack, and decreases towards the bottom of the stack reaching the lowest value in DRAM 0. For $\sigma'_{xy}$, $\sigma'_{yy}$, and $\sigma'_{zz}$, the trend of stress variation is somewhat mixed. In Figs. 5.4a, comparing to DRAM 7,

$\sigma'_{xy}$ is smaller in DRAM 4, but larger in DRAM 0. In Figs. 5.5a, $\sigma'_{yy}$ is the smallest in DRAM 0, and the largest in DRAM 4. For $\sigma'_{zz}$ in Figs. 6a, the stress is the smallest in DRAM 7, and increases towards the bottom of the die stack, although DRAM 4 has the highest values. Difference in stress distribution between the left edge and the right edge of the die stack can also be seen by comparing Figs. 5.3-5.6b.

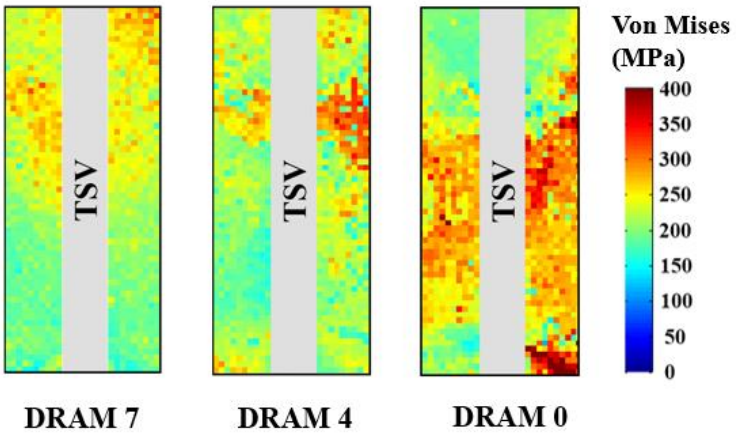
A gradient of stress distribution can be seen in each individual scans. For DRAM 7, the stress is relatively uniform with small variations. For DRAM 4 and DRAM 0, the stress variation inside the scan area is more pronounced where large variations mostly occur near the TSV and microbumps. For example, in Figs. 5.5b and 5.6b, the stress values in DRAM 0 become noticeably larger near the TSV and in the lower portion of the TSV. In Fig. 5.3a, high stress concentrations near the top and bottom of DRAM 0 can be seen, which correspond to locations near the microbumps.

The trend of stress distribution and the gradient of stress distribution can be seen from the average and standard deviation of the measured stress components, as summarized in Table 5.1.

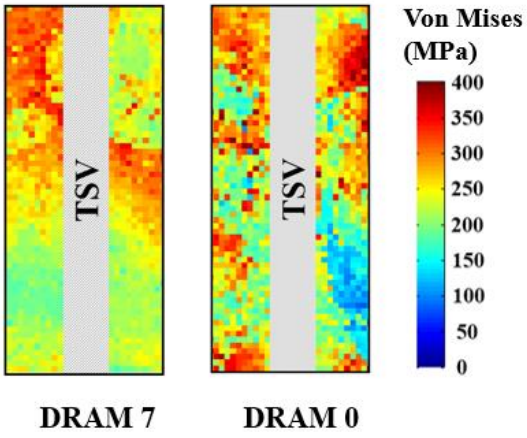
Table 5.1. Average and standard deviation (SD) of the measured deviatoric stress components and von-Mises stresses for vias on the left (L) and right (R) edges in DRAM 7, DRAM 4, and DRAM 0. (DRAM 4 (R) was not measured.)

| | $\sigma'_{xx}$ (SD) | $\sigma'_{xy}$ (SD) | $\sigma'_{yy}$ (SD) | $\sigma'_{zz}$ (SD) | von-Mises (SD) |
|---|---|---|---|---|---|
| DRAM 7 (L) | 74.7 (7.6) | 44.0 (5.3) | -89.4 (6.8) | 14.9 (5.6) | 218.3 (29.8) |
| DRAM 4 (L) | 62.0 (9.4) | 28.2 (14.8) | -108.6 (16.5) | 46.9 (16.1) | 222.4 (36.2) |
| DRAM 0 (L) | 26.3 (26.1) | 109.8 (37.5) | -49.0 (29.8) | 22.8 (19.0) | 247.5 (63.8) |
| DRAM 7 (R) | 75.6 (4.9) | 43.3 (5.7) | -90.8 (7.8) | 15.3 (7.8) | 249.1 (40.6) |
| DRAM 0 (R) | 50.9 (12.8) | 9.4 (16.0) | -92.8 (17.1) | 42.1 (15.6) | 242.8 (58.2) |

In Fig. 5.7, the von-Mises stress distributions calculated from the deviatoric stress components are plotted. Overall, the von-Mises stress increases from the top to the bottom of the die stack and the trend is more clearly seen on the left edge of the die stack (Figs. 7a). High stress concentration can be seen in Fig. 7a close to the TSV in the middle of DRAM 0. The von-Mises stress at the right edge of the die stack (Fig 7b) is slightly larger than that at the left edge, and the distribution is more non-uniform at the right edge. For vias at the right edge, high stress concentrations can be seen near the TSV and also near the ends of the TSVs.




(a)




(b)

Figure 5.7. The von Mises stress for TSVs at (a) the left edge of the structure and (b) the right edge of the structure in different DRAM die levels.

### 3.1. FINITE ELEMENT ANALYSIS

To simulate the stress and deformation in the memory stack, finite element analysis (FEA) was performed. Due to the sensitive nature of the details of material properties and manufacturing processes, the simulations in this paper are meant to demonstrate the general

capabilities of numerical calculations in correlating with actual measurements as well as in providing assessment and direction for future product and process changes. Therefore, output of the model may not necessarily replicate the micro-diffraction data or the actual stress state in the HMC product. Two-dimensional (2D) FEA models were constructed using the commercial package, ABAQUS (v6.12), assuming a plane strain condition. The model considered half of the die stack with symmetric boundary condition as shown in Fig. 5.8.

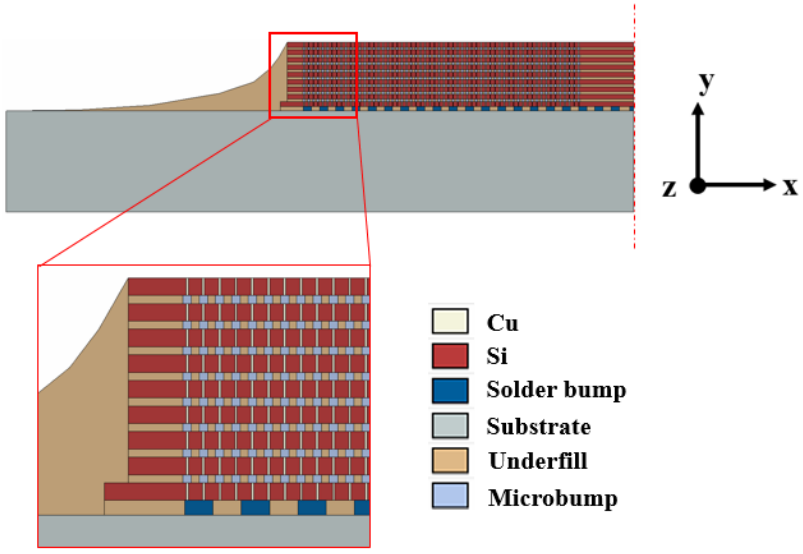



Figure 5.8. Half model of the HMC for FEA.

The FEA model considered the main components of the HMC die stack, including thin Si wafers, Cu TSVs, microbumps, substrate, solder bumps connecting the logic die to the substrate, and the underfill. The material properties used in the model were of 'typical' values and are listed in Table 5.2. Plasticity is taken into account for Cu TSVs, microbumps, and solder bumps, with the yield strength, $\sigma_y$, assumed to be 200MPa, 100 MPa, and 25MPa, respectively.

Table 5.2. Material properties used in FEA.

| Material | Property | | |
|---|---|---|---|
| | E (GPa) | ν | CTE (ppm/ $^{o}$C) |
| Substrate | 50 | 0.25 | 14 |
| Underfill | 10 | 0.3 | 30 |
| Solder bumps | 50 | 0.35 | 22 |
| Si | 130 | 0.28 | 2.3 |
| Cu | 110 | 0.35 | 17 |
| μ-bump | 130 | 0.35 | 18 |

To account for the die stack fabrication, the FEA model assumes certain stress-free, reference temperatures: 210$^{o}$C for the entire die stack and 100$^{o}$C for the substrate. The reference temperature of the underfill is assumed to be 160$^{o}$C.

In Fig. 5.9, the distribution of von-Mises stress in the 3D package is plotted. Large von-Mises stress can be seen concentrated near the solder bumps connecting the logic die and the substrate.

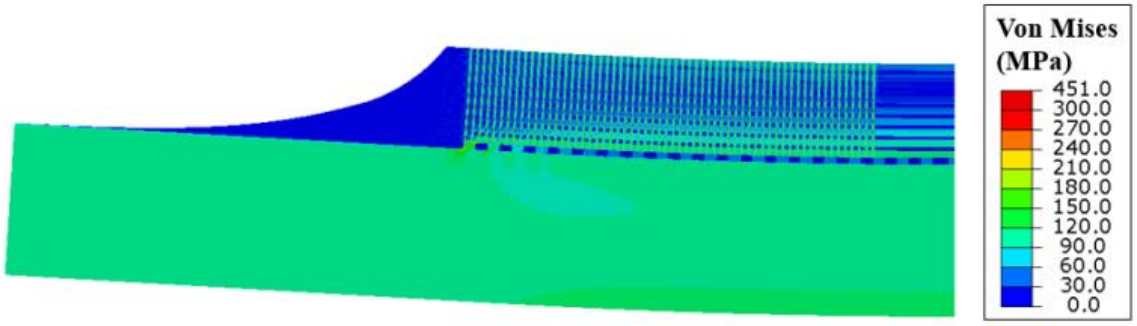
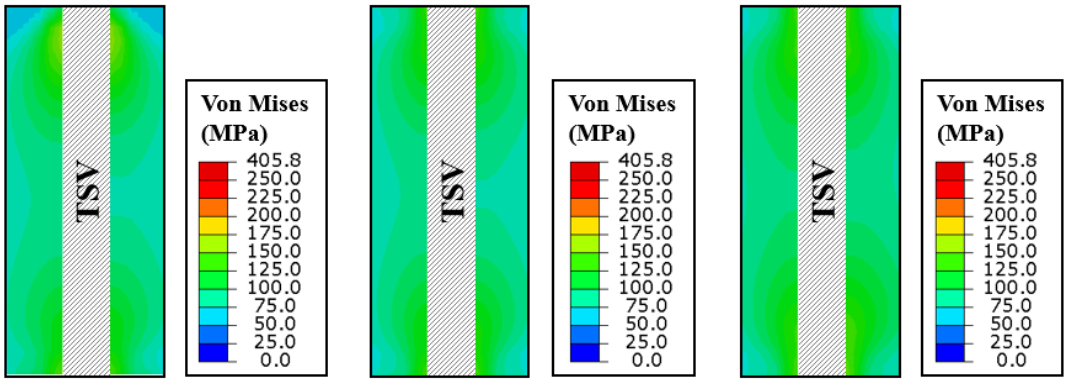



Figure 5.9. Distribution of von-Mises stress in the HMC stack.

The von-Mises stress distribution for a via located at the edge of the chip stack is plotted for DRAM 7, 4, and 0 in Fig. 5.10. The results show that from the top to the bottom of the DRAM stack, the von-Mises stress increases. The trend is consistent with experimental observations in Fig. 5.7. However, the magnitude of von-Mises stress calculated by FEA is lower than that obtained by x-ray microdiffraction.




(a) (b) (c)

Figure 5.10. Distribution of von-Mises stress near TSV in (a) DRAM 7, (b) DRAM 4, and (c) DRAM 0.

In Figs. 5.11-5.14, the deviatoric stress components $\sigma'_{xx}$, $\sigma_{xy}$, $\sigma'_{yy}$, and $\sigma'_{zz}$ from FEA are plotted for the chip stack and around the TSVs at the edge of the DRAM stack in DRAM 7, 4 and 0, corresponding to measured locations.

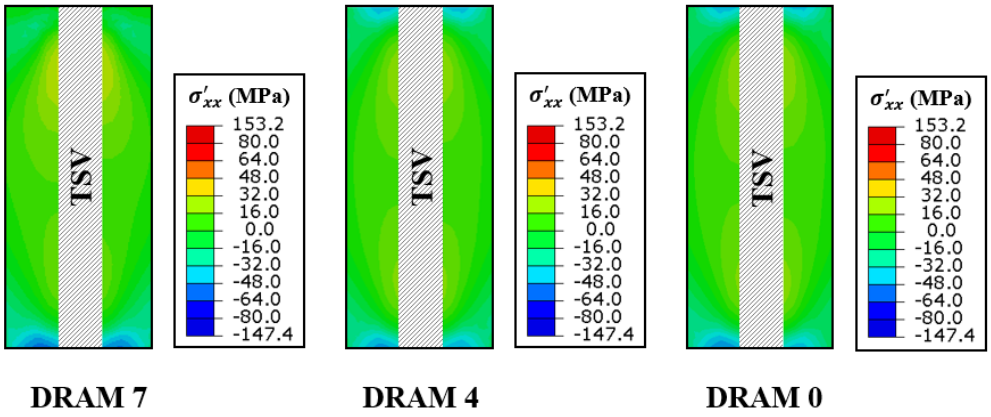



Figure 5.11. Distribution of deviatoric stress $\sigma'_{xx}$ in the die stack and near the TSV in DRAM 7, DRAM 4, and DRAM 0.

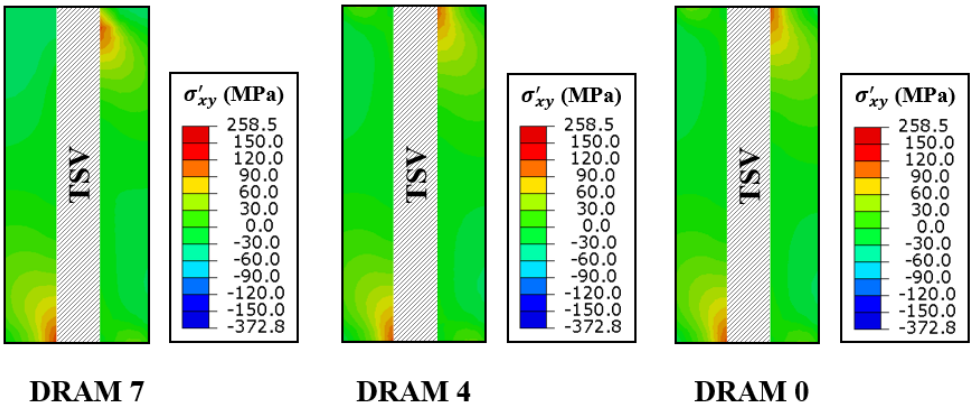



Figure 5.12. Distribution of deviatoric stress $\sigma_{xy}$ in the die stack and near the TSV in DRAM 7, DRAM 4, and DRAM 0.

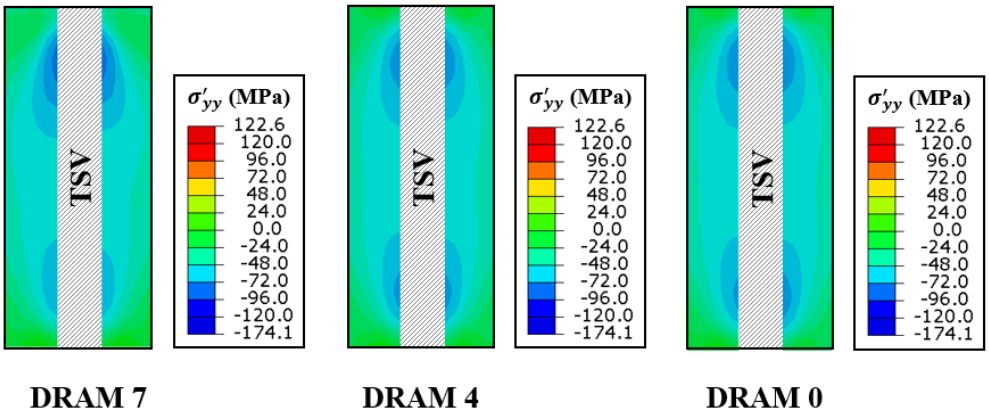



Figure 5.13. Distribution of deviatoric stress $\sigma'_{yy}$ in the die stack and near the TSV in DRAM 7, DRAM 4, and DRAM 0.

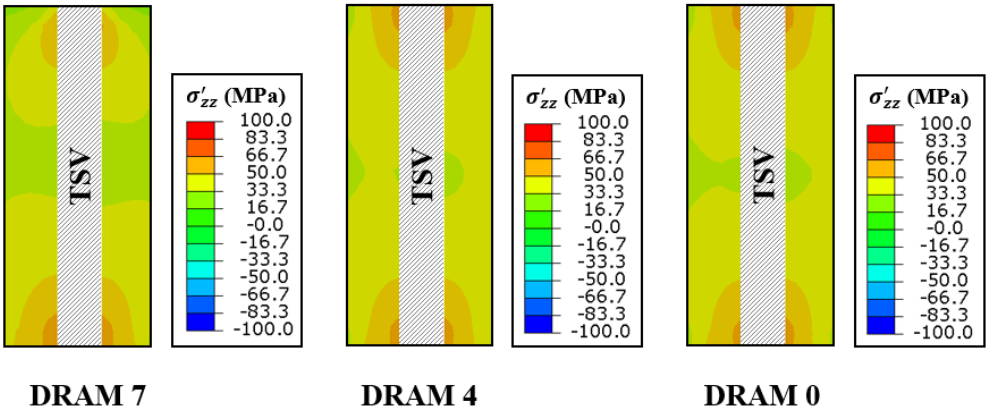



Figure 5.14. Distribution of deviatoric stress $\sigma'_{zz}$ in the die stack and near the TSV in DRAM 7, DRAM 4, and DRAM 0.

For the top and bottom of the DRAM stack (DRAM 7 and DRAM 0), the stresses predicted by FEA show similar trends as the x-ray micro-diffraction measurement. For example, both FEA and measurement show that $\sigma'_{xx}$ and $\sigma'_{zz}$ are largest in DRAM 7 and smallest in DRAM 0, and that $\sigma_{xy}$ and $\sigma'_{yy}$ are largest in DRAM 0 and smallest in DRAM 7. FEA show that the deviatoric stress components in DRAM 4 are intermediate between

that of DRAM 7 and DRAM 0, which sometime deviates from experimental observations. In the stress distribution by FEA, stress concentration occurs near the μ-bumps at top and bottom ends of the TSV, and close to the TSV. Similar stress concentrations have been observed in the measured stress distribution, although the exact areas of concentration are not identical. Overall, the magnitude of the deviatoric stresses in FEA is smaller than that from the actual measurement, which is also the case for the von-Mises stress.

## 5.3. DISCUSSION

Overall, the x-ray micro-diffraction measurement and FEA show qualitative agreement with each other. This suggests that the reference temperatures assumed in FEA is a simplified but reasonable representation of the processing condition. Within the DRAM stack, different stress magnitude and distribution can be seen in the top and bottom of the stack. Such differences can be traced to the die stacking process and the overall deformation of the package. Interestingly, the measurements show that at the same die level, the stresses at the left edge and the right edge have small but noticeable differences. Such asymmetry does not exist in FEA because of the symmetric boundary condition assumed in the model. Multiple factors could lead to the asymmetry, such as TSV alignment variation, induced strain/stress differences, residual surface stresses arising from polishing, etc. Such asymmetry is difficult to model but was captured by the x-ray micro-diffraction measurement. This demonstrates the ability of this technique for direct stress measurement in a complicated multi-stacked die structure such as the HMC for reliability assessment.

Quantitatively, there is some discrepancy between the stress measured by x-ray micro-diffraction and that from FEA. Overall, stress levels predicted by FEA are smaller than by experiments, indicating that FEA underestimated stress. The model is 2D assuming

a plane strain condition, which can cause different stress distribution from a 3D model. In the FEA, different reference temperatures are used for the chip stack, substrate and underfill to simulate the die stacking process although they are simplified and can be different from the actual stress-free temperatures of different components. In a separate FEA study, it is found that if higher reference temperatures are assumed for the chip stack and the underfill, the stress in Si will become larger. In addition, in the actual assembly process, the temperature field may not be uniform in each component, which could cause variation in stress distribution. The material properties used in FEA can also be different from those in the actual sample, particularly relevant is the plastic yielding of the Cu TSV that affects the stress relaxation and thus can reduce the stress in its surrounding Si. Therefore Cu microstructure may have a significant contribution to the formation or relaxation of the stress gradients observed in the sample. In FEA, a relatively low yield strength of 200MPa is assumed for Cu. The actual yield strength of the TSV in the die-stack structure can be larger, which will lead to larger stresses in Si. The temperature dependent material properties of polymeric materials in the package were not considered in the modeling analysis, which can also affect the calculated stress. Despite such limitations, the results demonstrated good qualitative agreement between FEA and measurement.

### 5.3.1. Stress Effect on Device Mobility

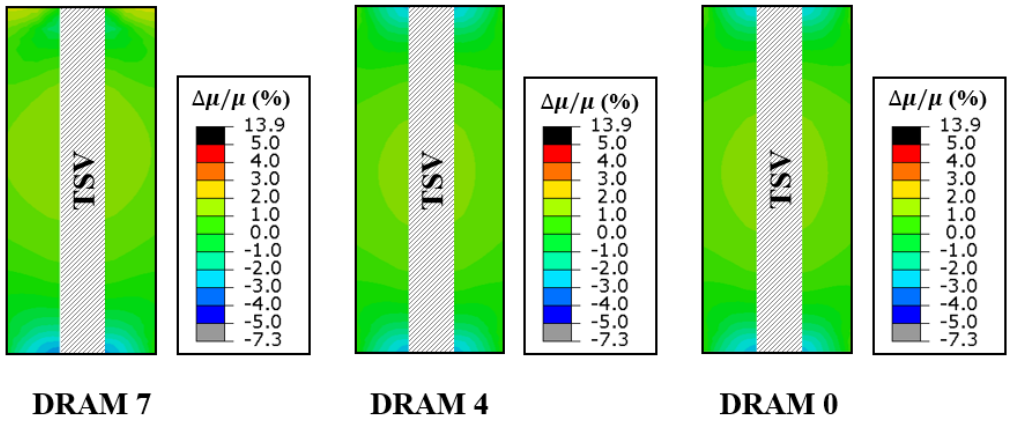
With the qualitative agreement established between FEA and measurement, FEA is applied to evaluate the stress effect on device mobility. The stress effect on mobility ($\Delta\mu$) can be related through the piezoresistance relation $\Delta\mu/\mu = -\Delta\rho/\rho = -(\pi_{11}\sigma_{11} + \pi_{22}\sigma_{22})$ for (001) Si, where axis 1 is along the [110] crystal direction of Si and axis 2 is

along the [-110] crystal direction of Si [32]. $\pi_{11}$ and $\pi_{22}$ are the piezoresistance coefficients Si and the values for <110> channel NMOS and PMOS as listed in Table 5.3.

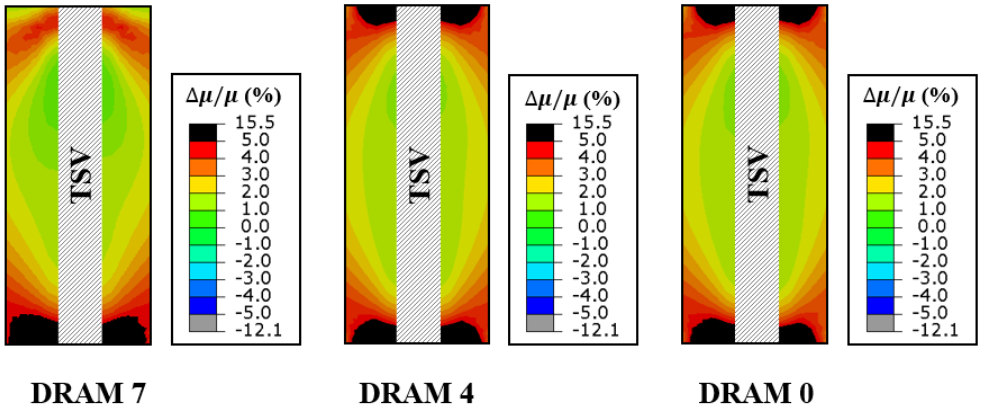
Table 5.3. Piezoresistance coefficients

| (%/GPa) | $\pi_{11}$ (%/GPa) | $\pi_{22}$ (%/GPa) |
|---|---|---|
| <110> NMOS | -31.05 | -17.45 |
| <110> PMOS | 71.8 | -66.3 |

The calculated mobility changes for MOSFET with channel direction along the horizontal direction (x) for TSVs at the edge of the 3D package in DRAM 7, DRAM 4, and DRAM 0 are shown in Fig. 5.15




(a)



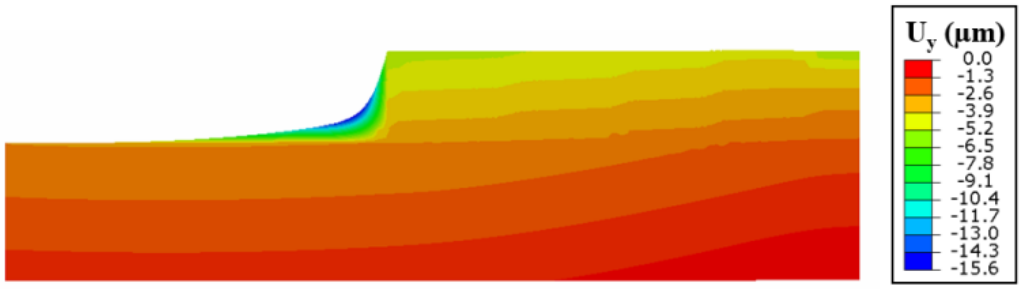

(b)

Figure 5.15. Mobility changes for (a) NMOS and (b) PMOS near the edge of the package in DRAM 7, DRAM 4, and DRAM 0.

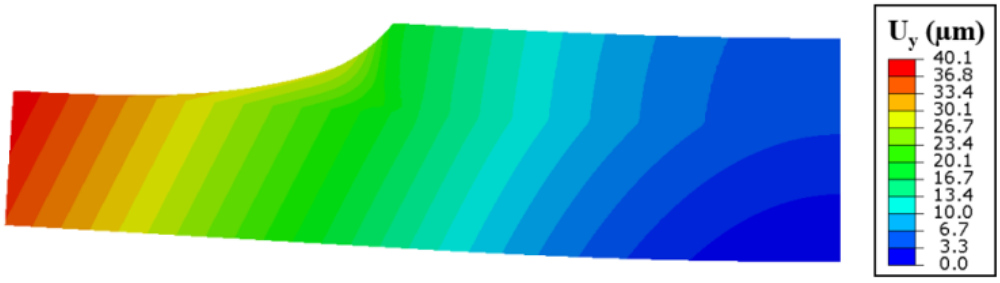
The results show that if the stress effect on mobility change is generally small, less than 5% for NMOSFET around vias for DRAM 7, DRAM 4, and DRAM 0. For PMOSFET, however, regions with mobility change can exceed 5%.

### 5.3.2. Analysis of warpage of the 3D package

Warpage is a complicated three dimensional phenomenon arising from CTE mismatch coupled with compliance differences and enhanced by possible thermal gradients. Warpage also exists at many levels through processing from wafer bow to die warpage to final package warpage and often with physical constraint due to processing condition. Therefore, to understand the impact of warpage on the detected stress gradient a simplified 2D version of a partially package sample was simulated. Warpage during reflow process for surface mounting, a heating step to 250°C was simulated in FEA. The contours of the vertical displacement, $U_y$, at room temperature and at 250°C during reflow are shown in Fig. 5.16.




(a)




(b)

Figure 5.16. Out of plane displacement of the HMC stack (a) at room temperature, and (b) at 250°C during reflow for surface mounting on PCB.

In Fig. 5.16, the contour change of the sample during heating from RT to 250ºC is plotted. With increasing temperature, the warpage becomes more positive (smiley face) to reach a maximum of 36.7 μm at 250ºC. The warpage as a function of temperature is also plotted in Figs. 5.17 and 5.18.

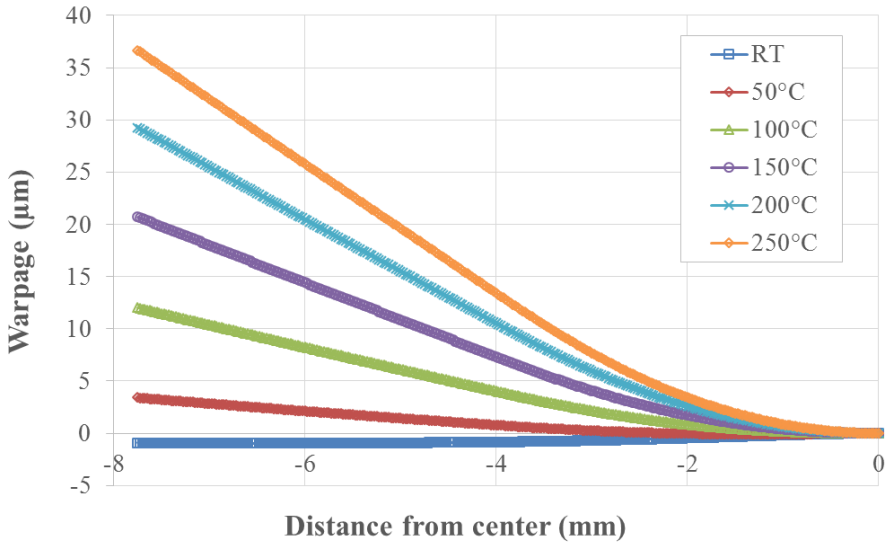



Figure 5.17. Warpage evolution of the 3D package at different temperatures.

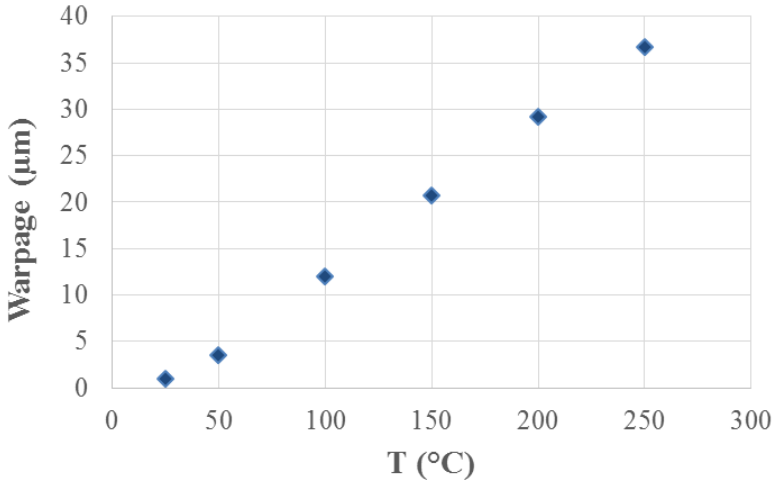



Figure 5.18. Warpage of the 3D package at different temperatures.

Overall, the FEA model shows bending of the substrate is towards the chip side, suggesting more shrinkage in the chip stack dominates the direction out of plane displacement. The change in warpage observed in the model suggests packaging materials property mismatch may be a factor in the stress differences detected with the x-ray micro-diffraction experiment. Therefore materials properties of the packing components will be critical for accurate modeling and reducing packaging stresses. It needs to be pointed out that the test vehicle did not include the Cu lid. Therefore the FEA didn't consider the Cu lid, which could have significant effect on the stress distribution and warpage.

## 5.4. CONCLUSIONS

The stresses in different die levels for a HMC structure are directly measured by synchrotron x-ray micro-diffraction with sub-micron resolution. Different stress distribution in different die levels and stress concentration near the TSV and µ-bumps have been observed. Stress asymmetry between two edges of the die stack is also observed. A 2D FEA model was set up to calculate the warpage and stress distribution in the die stack

structure. The model considered different reference temperatures for the chip stack, substrate and the underfill to account for the die stacking process. Overall, good qualitative agreement was obtained between the synchrotron x-ray micro-diffraction measurement and FEA. Quantitatively, FEA underestimates the magnitude of the stress where factors causing the discrepancy are discussed. .

This work demonstrates that synchrotron x-ray micro-diffraction is an effective technique to study the thermal stresses in a complicated multi-stacked die structure such as the HMC structure. The results from synchrotron x-ray micro-diffraction can be combined with FEA modeling to provide a unique approach for stress characterization of TSV in multi-stacked die structures. Once the FEA model is validated, the analysis can be extended to assess the effect of materials properties and processing on stress characteristics and reliability impact for reliability assessment of 3D integrated structures.

# Chapter 6: Conclusions and Outlook

Three-dimensional (3D) integration utilizing vertical die stacking is a promising approach to overcome the limitations of conventional Moore's law scaling. 3D integration brings about several advantages, including enhanced chip performance, reduced power consumption, and smaller form factor, which are particularly important for mobile technology development. Cu through-silicon via (TSV) is a critical enabling component for 3D die stacking. The CTE mismatch between Cu and Si generates thermal stresses in and around the TSV which cause reliability concerns due to device mobility degradation and via extrusion. The materials mismatch in the 3D package can introduce complex stresses to affect chip performance and reliability. Solutions addressing the thermos-mechanical reliability issues for 3D integration should be based on understanding of stress characteristics and failure mechanisms. For process optimization, it is also important to understand the effect of Cu microstructure on stress and reliability.

In this work, experimental measurements and modeling analysis were combined to investigate the stress characteristics and reliability for TSV structures and 3D die stacks. In Chapter 2, the substrate curvature method was employed to study the thermo-mechanical behavior of a blind via structure, TSV-A. The result was compared with that of passivated Cu thin films with unique features observed for TSV structures. Grain growth during heating was observed by microstructure analysis and deemed largely responsible for the non-linear stress relaxation during heating. Triaxial stress state in the confined TSV structure was shown by FEA, with a small amount of local plasticity emerging near the via top surface during cooling. An important finding was that the stress relaxation during thermal cycling induces stress accumulation at room temperature at the end of a thermal cycle. The residual stress can affect carrier mobility which was analyzed by FEA. In

Chapter 3, a novel characterization technique, synchrotron x-ray microdiffraction, was introduced. This technique has the unique capability for direct measurements of stress and plasticity with sub-micron resolution, which is particularly useful for probing the local plasticity in Cu and near-surface stress Si in TSV structures. This technique was applied to TSV-A structure, where peak broadening of Cu grains near the top of the via was observed, suggesting the presence of local plasticity. The evolution of local plasticity can be correlated to the amount of via extrusion in samples subjected to thermal loads. The result provided direct experimental evidence to support the local plasticity mechanism for via extrusion. The effect of plasticity on via extrusion was further analyzed using an analytical solution and FEA, which treated the via as homogeneous with simplified thermal processing. The analysis was applied to two TSV structures and found the Cu grain size can affect its yield strength and thus plasticity and via extrusion. In Chapter 4, the problem of via extrusion was further investigated to search for methods to reduce via extrusion. Three inelastic processes leading to unrecoverable via extrusion were proposed, including grain growth, dislocation glide, and diffusional creep. These processes were investigated using three different blind via structures, TSV-A, TSV-B, and TSV-C, and their thermos-mechanical behaviors were discussed. TSV-C, which showed the most resistance to via extrusion, was used as an example to develop potential approaches to reduce extrusion. A stable grain structure, high yield strength, large amount of twin boundaries, and strong via/liner interface are found to be desirable for improving via extrusion reliability. A cap layer deposited on top of the via was proposed to limit grain boundary and interfacial diffusion. The cap layer was indeed found to be effective in reducing via extrusion and demonstrated for TSV-B, where a 16 nm Co layer was shown to reduce via extrusion by nearly 70%. In general, Cu microstructure plays a central role in controlling via extrusion reliability. The role of microstructure for via extrusion was further discussed by comparing

to electromigration in Cu interconnects. Finally, in Chapter 5 synchrotron x-ray microdiffraction was applied for stress characterization of a 3D die stack structure. FEA was used to discuss the effect of stress on KOZ and warpage.

Based on the results from this dissertation, several interesting topics are suggested for future studies to advance basic understand of via extrusion for improving TSV reliability.

1. Effect of electroplating conditions on microstructure of TSVs. Microstructure plays an important role in the inelastic processes causing via extrusion. For electroplated Cu, incorporated additives can directly affect the microstructure in TSV. To achieve a microstructure that resists via extrusion during thermal processing, it is important to understand how additives in the electroplating bath affect microstructure development. This will require systematic studies involving characterization of TSV structures fabricated with selected electroplating chemistries. Other factors, including the properties of seed layers, via density and geometry, and overburden layer are also important and should be studied.

2. Characterization of inelastic deformation processes for via extrusion. To better understand the inelastic processes during via extrusion, more detailed analysis should be performed by isothermal relaxation measurements. In-situ synchrotron x-ray microdiffraction can be a powerful approach to investigate the evolution of plasticity during thermal cycling. These studies will further clarify the mechanisms for via extrusion.

3. Cap layer to reduce via extrusion. The effectiveness of a cap layer in reducing via extrusion has been demonstrated. It would be important to elucidate the mechanisms of the cap layer in reducing mass transport and via extrusion, which may require TEM studies to examine the structure of the cap/TSV interface. Studies should also be performed in searching for an optimized material and thickness for the cap layer.

4. Statistics of via extrusion. A typical 3DIC is designed to contain hundreds, even thousands of TSVs. For such a large ensemble of TSVs, statistics of via extrusion will become important, as the overall reliability of the system is determined by a small number of vias (about 0.1%) with the largest extrusion. This problem could become more important as technology advances with scaling of TSV dimensions. The statistics of via extrusion is related to the statistical distribution of grain size and orientation in the TSV. To investigate this issue, systematic studies have to be carried out with special statistical test structures containing via chains designed and fabricated.

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# Vita

Tengfei Jiang was born and raised in Beijing, China. She studied at the Tsinghua University in Beijing, China and obtained the Bachelor of Engineering degree in Materials Science and Engineering in 2006. She then studied at The Ohio State University in the Department of Materials Science and Engineering, obtaining the Master of Science degree in 2009. She entered the Materials Science and Engineering Ph.D. program at the University of Texas at Austin in 2010.

Email address: jiangt@mail.utexas.edu

This dissertation was typed by Tengfei Jiang.