The Dissertation Committee for Jaehyun Ahn Certifies that this is the approved version of the following dissertation:

Optoelectronic Devices for Power Conservation and Generation

Committee:

Sanjay Banerjee, Supervisor

Edward Yu

Leonard Frank Register

S.V Sreenivasan

Brian Korgel

Optoelectronic Devices for Power Conservation and Generation

by

Jaehyun Ahn

Dissertation

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

Doctor of Philosophy

The University of Texas at Austin

December 2018

Dedication

To my beloved family and god

Acknowledgements

I would like to sincerely thank my supervisor, Professor Sanjay K. Banerjee during this incredible journey. His guidance, support, and patience has truly helped me to get back up from the endless failures in the cleanroom. I would like to acknowledge my committee members, Professor Edward Yu, Professor L. Frank Register, Professor S.V Sreenivasan and Professor Brian Korgel for their support. I would like to thank Jean L. Toll for taking care of everything (from receipts to visa documentations) during my time at MER.

I would like to thank all my friends, colleagues, group members, seniors, staff members during my Ph. D. Among them, I would like to especially commemorate Jongwook Sohn and his wife Soojin Lee. From the first day I landed in Austin, your kindness has been a priceless treasure to me. I would like to thank Dr. Taegon Kim from Samsung Electronics, and Leo Mathew, Dr. Rajesh Rao from Advanced Novel Devices for their technical discussion and support which has led to publications.

Lastly, I thank my mom, dad, and baby sis for their love. They are the pillars of my existence.

Optoelectronic Devices for Power Conservation and Generation

Jaehyun Ahn, Ph.D.

The University of Texas at Austin, 2018

Supervisor: Sanjay K. Banerjee

Energy conservation and generation have become increasingly important in society. Here, we pursue novel transistor technologies based on three-dimensional (3D) FinFETs and two-dimensional (2D) materials to make low power, high speed transistors. We also develop quasi-2D silicon thin film solar cells for power generation.

First, a novel approach of doping III-V semiconductors is presented. Oxygen rich silicon oxide (SiO_x, where $x > 2$) is found to behave as a solid dopant source when deposited on InGaAs, followed by thermal annealing. Oxygen, when diffused into InGaAs, act as n-type dopants where the active carrier concentration reaches up to 1.4×10^{18} cm^3. Besides the simple, CMOS compatible doping technique of solid source doping, another interesting factor is the dopant concentration can be altered by the deposited dopant thickness, which adds an additional control knob therefore allowing enhanced control over the doping process. Thermally induced compressive stress within InGaAs due to the difference in coefficient of thermal expansion (CTE) between InGaAs and SiO_x is known to increase the number of vacancies within InGaAs therefore giving rise to active dopant concentration. This approach can be used to make high speed, low power transistors.

Second, study of thin indium metal contacts on InGaAs is presented. Unlike silicon, III-V compound semiconductors such as InGaAs decomposes around 450 ˚C which result in out-diffusion of indium and gallium and decrease in metal-InGaAs contact resistance.

By adding a thin layer of indium between the metal-InGaAs interface, the out-diffusion of gallium was minimized.

Third, solar cells based on graphene-silicon (GS) heterojunction architecture are demonstrated on bendable crystalline silicon substrates. Flexible, thin silicon films are fabricated by using the thermal expansion difference between electroplated nickel and bulk silicon, which generates residual strain upon thermal cycling. By controlling the amount of thermal stress, silicon thicknesses between 8 and 35 μm are exfoliated through a kerf-less mechanical method. Together with multi-layer graphene (MLG) grown by chemical vapor deposition (CVD) and atomic layer deposition (ALD) of Al_2O_3 as a silicon passivation layer, power conversion efficiencies (PCE) of 7.4 % were achieved on bendable silicon substrates.

Finally, Chapter 7 summarizes the all the chapters from this dissertation and some thoguhts for future work.

Table of Contents

List of Tables xi

List of Figures xii

Chapter 1. Introduction 1

1.1. III-V Compound Semiconductors: InGaAs 3

1.1.1 Challenges in Fin doping 4

1.2. AlGN/GaN Compound Semiconductor and 2DEG layer 4

1.3. Two-Dimensional Materials 6

1.4. Kerf-less Exfoliation of Semiconductors 7

1.5. Organization of Dissertation 9

Chapter 2. Nanoscale doping of compound semiconductors by solid phase dopant diffusion 11

1.1. Introduction 11

1.2. Sample Preparation 12

1.3. Results and Discussion 13

1.4. Conclusion 20

Chapter 3. Low Contact Resistivity Indium Metal Contacts on InGaAs and GaAs Exfoliation 21

3.1. Introduction 21

3.2. Experimental 24

3.3. Ker-less Exfoliation of GaAs 36

3.4. Conclusion 37

Chapter 4. Demonstration of bendable GaN HEMT for RF applications 39

4.1. Introduction 39

4.2. Exfoliation of AlGaN/GaN 2DEG Layer on Silicon Substrate 40

4.3. Demonstration of AlGaN/GaN HEMT on Silicon Substrate 42

4.3.1. Photomask Drawing for HEMT Structure 42

4.3.2. AlGaN/GaN Etch and Channel Definition 44

4.3.3. Specific contact resistivity of AlGaN/GaN layer 48

4.3.4. I-V Characteristics of AlGaN/GaN HEMT 49
4.4. Kerf-less exfoliation of non-planar, multi-layer architecture 51
Chapter 5. Graphene-Al_2O_3-Silicon Heterojunction Solar Cells on Flexible Silicon Substrates 53
5.1. Introduction 53
5.2. Experimental 54
5.2.1. Growing, doping, and transfer of multilayer graphene 54
5.2.2. Fabrication of thin silicon films with metal backing 58
5.2.3. Graphene-silicon (and graphene-insulator-silicon) SBSC fabrication 59
5.3. Results and discussion 62
5.3.1. GS-SBSC 62
5.3.2. GIS cells with ALD Al_2O_3 65
5.4. Conclusion 69
Chapter 6. CVD grown h-BN for Photovoltaic and Electronic Device Applications 71
6.1. Introduction 71
6.2. Experimental 72
6.2.1. h-BN Growth and Characterization 72
6.3. Photovoltaic application of CVD h-BN 74
6.3.1. Graphene/h-BN/c-Si Solar Cell Fabrication 74
6.3.2. Results and Discussion 74
6.4 Electronic application of CVD h-BN 78
6.4.1. Graphene/h-BN FET 78
6.4.2. Fabrication of Graphene/h-BN FET 78
6.4.2. Results and Discussion 79

Chapter 7. Conclusion and Future Work 80

Appendix.....84

References.....87

Vita 93

List of Tables

Table 2.1: RBS measurement of SiO_x deposited samples with different gas flow rate.....14

Table 6.1: Open circuit voltage (Voc), short circuit current (Jsc), fill factor (FF), power conversion efficiency (PCE) and cell area for graphene/h-BN/Al2O3/exfoliate silicon (GBIS), graphene/h-BN/exfoliation silicon (GBS), graphene/Al2O3/exfoliated silicon(GIS), and graphene/exfoliated silicon (GS) solar cells. 76

List of Figures

Figure 1.1: Best Research-Cell Efficiency graph by NREL. 1

Figure 1.2: Electron and hole mobility of semiconductors including silicon, germanium and III-V compound semiconductors. 3

Figure 1.3: Left: Schematic of Fin structure with ion implantation beam line, Middle, Right: Simulation result of doping profile of silicon fin with different implant energy, dose and beam angle. 4

Figure 1.4: Schematic and band diagram of AlGaN/GaN 2DEG layer. 5

Figure 1.5: Schematic of kerf-less exfoliation process. 7

Figure 1.6: Graphic chart of this dissertation.....9

Figure 2.1: Schematic diagram of solid dopant based doping process 12

Figure 2.2: RBS measurement of SiO_x deposited samples with differend gas flow rate.....13

Figure 2.3: I-V characteristics for InGaAs layer after SRSO and ORSO doping process. Inset shows the result from the untreated InGaAs as a reference with a magnified scale 15

Figure 2.4: SIMS profile of (a) silicon and (b) oxygen for SRSO & ORSO treated 100 nm thick InGaAs samples 16

Figure 2.5: (a) Sheet resistnace and active doping concentration of oxygen implanted InGaAs samples. (b) TOF-SIMS profile of oxygen implanted InGaAs sample.....17

Figure 2.6: Illustration of vacancy formation and dopant diffusion in InGaAs .18

Figure 3.1: Electrical resisvity of various metal/Ga alloy and Gallium between 300 and 500 (K) from literature survey 22

Figure 3.2: Schematic of ideal/real case metal/InGaAs interface phenomenon and theoretical models for each case 23
Figure 3.3: AFM & Optical microscope image of indium contact after ultra-sonication 24
Figure 3.4: Schematic diagram and process flow of TLM fabrication 25
Figure 3.5: Sheet and contact resistance of various TLM devices before and after annealing (10 mintue anneal).....26
Figure 3.6: TLM pad resistance as a function of pad spacing for various metal ohmic contacts on n-$In_{53}GaAs$ (30 nm)/InAlAs (130 nm)/InP with doping concentration of $3x10^{19}$.....26
Figure 3.7: Effect of indium thickness in indium (5, 10 nm)/Ti(30 nm) on InGaAs before and after annealing.....27
Figure 3.8: STEM image and EDS mapping of In, Ga, and As, elements. Brightness of the color is proportional to the counts of each element.....28
Figure 3.9: EDS of In (30 nm) before and after 400 ˚C anneal 29
Figure 3.10: SIMS profile of Ti (30 nm)/In (10 nm) on n-$InGa_{53}As$.....30
Figure 3.11: HRXRD analysis of indium (30 nm) on n-$InGa_{53}As$ before and after 300 ˚C and 400 ˚C anneal 31
Figure 3.12: Schematic band diagram of In/ $In_{0.53}GaAs$ structure with (a) low (b) high temperature anneal. Diffusion depth may be ultra-shallow (10 ~ 30 Å) 32
Figure 3.13: HRTEM image of indium (30 nm)/InGaAs (a) before and (b) after 400 ˚C annealing. Inter-mixing is oberserved at the interface.....33
Figure 3.14: Schematic diagrams of typical gate last MOSFETs fabrication. Indium and Mo were used and S/D contact metal.....34

Figure 3.15: Summary of V_g vs. I_d characteristics in Gate late processed InGaAs MOSFETs with indium (30 nm) or Mo (30 nm) source/drain contacts at channel length of (a) L= 5 μm, and (b) L= 10 μm 35

Figure 3.16: Comparison of linear scaled drive current and transconductance between In and Mo on InGaAs 35

Figure 3.17: Source/drain contact resistance (R_{SD}) & channel length offset (L_{off}) comparisons between (a) indium (30 nm) and (b) Mo (30 nm) on InGaAs. R_{SD} and L_{off} were linearly extrapolated 36

Figure 3.18: Top: Photo image of after nickel electroplating and after exfoliation of GaAs. Bottom: Cross-sectional SEM image of exfoliated GaAs. 37

Figure 4.1: Exfoliation result of AlGaN/GaN 2DEG layer on silicon substrate and fabrication procedure of sample after exfoliation 40

Figure 4.2: Top left: Image of AlGaN/GaN on bulk silicon. Right: Image of AlGaN/GaN/c-Si on EVA sheet after exfoliation. Bottom : Hall measurement result of bulk and exfoliated 2DEG layer 41

Figure 4.3: L-edit image of final mask design as well as TLM and HEMT structure 43

Figure 4.4: Top: Cross sectional SEM image of AlGaN/GaN on silicon substrate after 9 min etch at 100 W. Bottom: Cross sectional SEM image of AlGaN/GaN on silicon substrate after nickel mask removal. AlGaN surface is smooth after nickel etch. 45

Figure 4.5: AFM scan of bare AlGaN/GaN before (top) process (average roughness= 0.8 nm) after (bottom) ICP etch and nickel mask removal (average roughness = 1.3 nm). 46

Figure 4.6: Etch rate of GaN on Si and SiC using ICP etch 47

Figure 4.7: Specific contact resistivity of AlGaN/GaN layer for different temperature and time by RTA.....49
Figure 4.8: Optical image of AlGaN/GaN HEMT. V_{DS}-I_{DS} and V_{GS}-I_{DS}/g_m mesurement result 50
Figure 4.9: Top: Optical image of exfoliated AlGaN/GaN HEMT with and without additional Ti adhesion layer. Bottom left: Schematic of final structure before exfoliation. Dotted line represents exfoliated path. Bottom right: Parent silicon wafer after exfoliation.....51
Figure 5.1: (a) Illustration of graphene growth. Methane decomposes on the catalytic surface of the Cu-Ni alloy and carbon dissolves into the substrate at high temperature. On slow cooling, the carbon precipitates out of the Cu-Ni alloy in the form of MLG. (b) Raman spectrum of MLG after transfer onto SiO_2/Si substrate showing a highly crystalline film and a histogram of the G peak position over a scanned area of 40 x 30 μm MLG showing that the film is uniform in quality. (c) AFM scan of the edge of a transferred MLG showing the thickness to be ~ 10 nm. (d) Transmission of un-doped and pre-doped MLG over a broad light spectrum.....56
Figure 5.2: (a) Schematic of silicon exfoliation process by deposition of metal layer, thermal cycling, and exfoliation. (b) Scanning electron microscope (SEM) cross-section image of a thin exfoliated silicon layer. Inset: Photographic image of an exfoliated 4-inch Si wafer. (c) Experimental result of silicon film thickness relationship with thermal cycling temperature 58
Figure 5.3: (a) Schematic of GIS Solar cell fabrication process. For GS-SBSC, all is identical except excluding Al_2O_3 layer deposition process. (b) Photographic image of a completed GIS solar cell.....60

Figure 5.4: (a) Qualitative energy band diagram of GS-SBSC with and without $AuCl_3$ doping. P-doped MLG creates a shift in potential resulting in improved cell performance. (b) J-V plot of un-doped MLG and pre-doped MLG with no interlayer oxide layer. (c) lnJ-V plot measured in dark with linear fit (solid lines) of the forward current for ideality factor and SBH extraction. (d) dV/d(lnJ)-J plot for series resistance (R_S) extraction.....62

Figure 5.5: (a) V_{OC}, J_{SC} and FF versus Al_2O_3 thickness for GIS solar cells on exfoliated silicon film. (b) Qualitative band diagram of GS cells with and without interlayer oxide 66

Figure 5.6: GIS cell performance (a) J-V and (b) EQE plots for optimized GIS device with 1 nm Al_2O_3 insulator layer. (c) *n* and R_S extracted from dark current in forward bias for the optimized GIS device.....68

Figure 6.1: Laser optical image of CVD h-BN after transferring on to SiO_2/Si substrate. 73

Figure 6.2: Top left: Optical image of CVD h-BN after wet transfer. Right: Vertical composition of transferred graphene/h-BN stack. Bottom left: Schematic of graphene/h-BN/silicon solar cell. 77

Figure 6.3: Top: I_D/V_G and I_D/V_G characteristic of graphene/h-BN FET. Bottom: Optical image and illustration of graphene/h-BN FET. 79

Figure 7.1: Cross-sectional SEM image of InGAs fin. 81

Figure 7.2: Difference in perovskite transparency by solvent engineering. 82

Figure 7.3: Resistive switching properties of thin h-BN grown by MOCVD. ...83

Chapter 1. Introduction

As of 2018, silicon is still the dominant material for both photovoltaic devices and electronic transistors. For integrated circuits, the leading semiconductor manufacturers such as Intel, Samsung and TSMC are fabricating transistors with a pitch of just 14 nanometers (nm) wide, which is less than 150 atoms. While advanced lithographic processes such as extreme ultraviolet lithography (EUVL) is making its debut, it is indeed no doubt that we are quickly running out of physical space for future scaling.

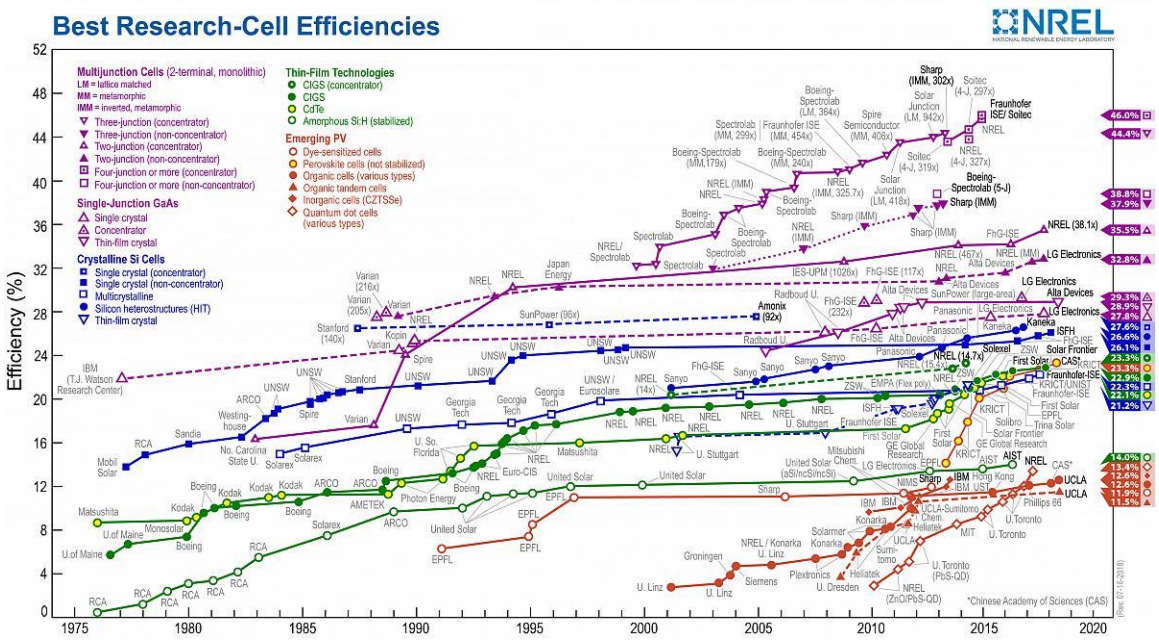


Figure 1.1. Best Research-Cell Efficiency graph by NREL [1]

As for silicon-based solar cells, according to reports from National Renewable Energy Laboratory (NREL), the power conversion efficiency (PCE) for silicon-based solar

cells have shown an increase of less than 3 % during the last decade, which is shown in figure 1.1. [1]

For decades, extensive research has been made on finding alternative materials to replace silicon as well as new, innovative techniques to improve optoelectronic device performance.

In this dissertation, we investigate post-silicon candidate materials in various optoelectronic applications including field effect transistors (FETs), high electron mobility transistors (HEMT) and photovoltaics for efficient power conservation and generation.

1.1 III-V Compound Semiconductor: InGaAs

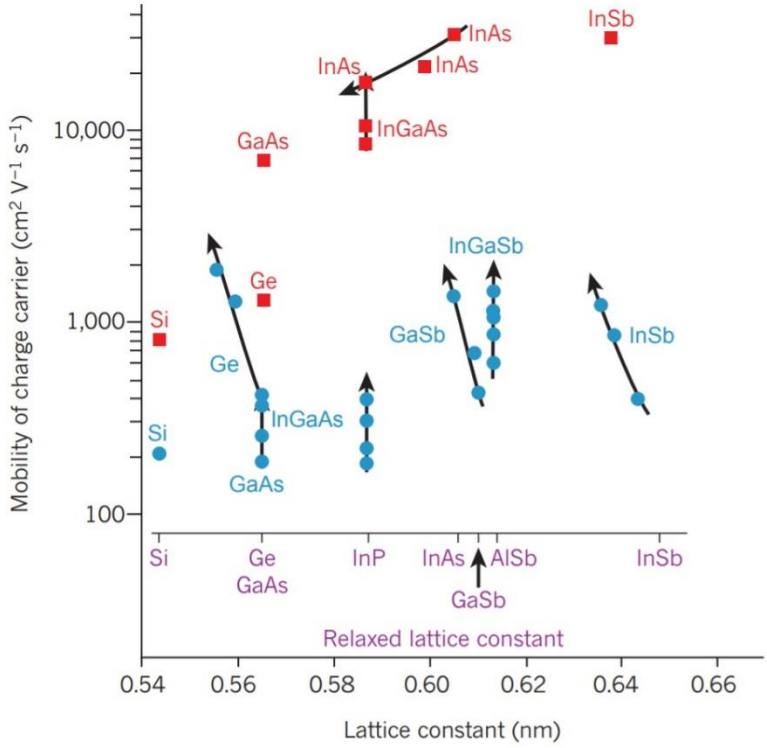
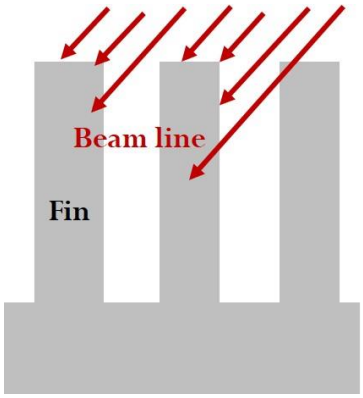
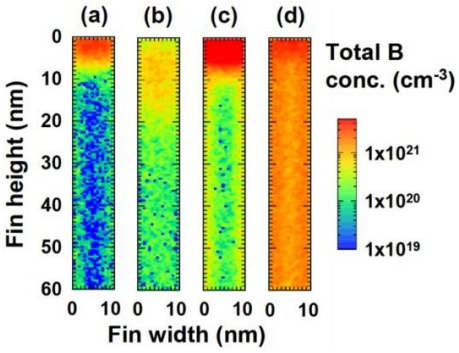


Figure 1.2. Electron and hole mobility of semiconductors including silicon, germanium and III-V compound semiconductors. [2]

InGaAs is a ternary III-V compound semiconductor which has been noticed as a potential replacement for silicon-based FETs due to its very high electron mobility (μ_e) compared to silicon. Figure 1.2. shows the mobility of various semiconductors and their lattice constants. [2] High mobility of InGaAs leads to high velocity which improves the performance of electronic devices. Also, high mobility compound semiconductors can reduce the device operating voltage without compromising the switching speed which can reduce the power dissipation or density as devices continue to scale down. [3]

1.1.1 Challenges in Fin doping





	Energy	Dose	Tilt
a	0.5	10^{15}	10^{o}
b	2	10^{15}	10^{o}
c	0.5	$5x10^{15}$	10^{o}
d	0.5	10^{15}	45^{o}

Figure 1.3. Left: Schematic of Fin structure with ion implantation beam line, Middle, Right: Simulation result of doping profile of silicon fin with different implant energy, dose and beam angle. [4]

One of the key challenges for high quality transistors as it scales down is effectively doping the semiconductor to minimize parasitic resistances. Regarding semiconductor doping, ion implantation has been the dominant method of doping due to its precise controllability. However, as the scaling down continues, transistor architecture has shifted from a 2D planar structure to a tall, narrow 3D structure generally now referred to as “Fin”. Unlike conventional planar structures, 3D structures such as Fin face challenges when doping with ion implantation. Due to it directionality, ion beams generate shadowing effects which result in non-uniform doping when doping an array of fins as illustrated in Figure 1.3. While studies have shown that tilting the beam angle can resolve doping uniformity for a single fin, the on-current (I_{on}) for a single FinFET is too low for practical use which eventually requires an array of fins. [4]

An alternative way of doping semiconductors is by diffusing the dopants through a thermal drive-in process which is illustrated in figure 1.4. While this method has been less

common compared to ion implantation, it has been reconsidered with various names such as ‘solid source diffusion’, ‘spin-on-dopant’ (SOD), ‘monolayer doping’ (MLD) and ‘solid phase doping’.

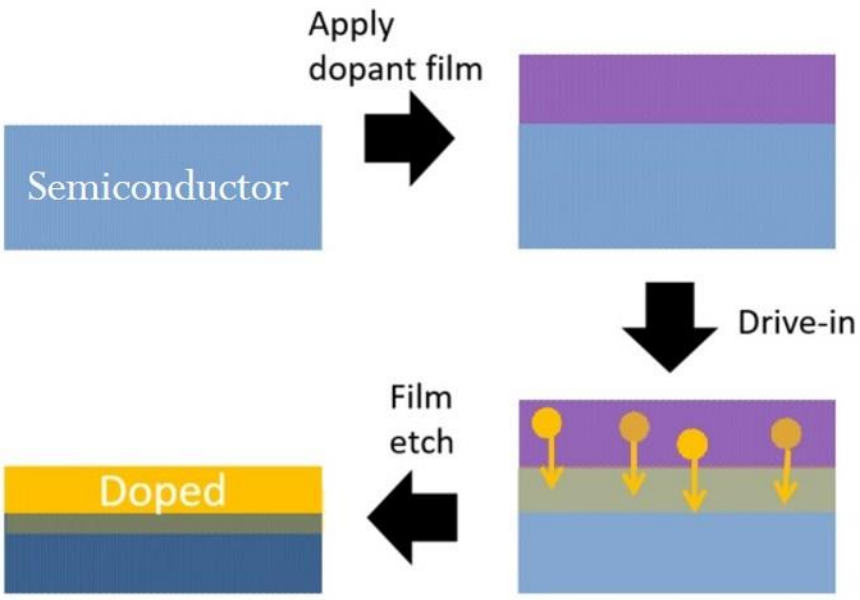


Figure 1.4. Schematic diagram of semiconductor doping by thermal drive-in process.

1.2 AlGaN/GaN Compound Semiconductor and 2DEG layer

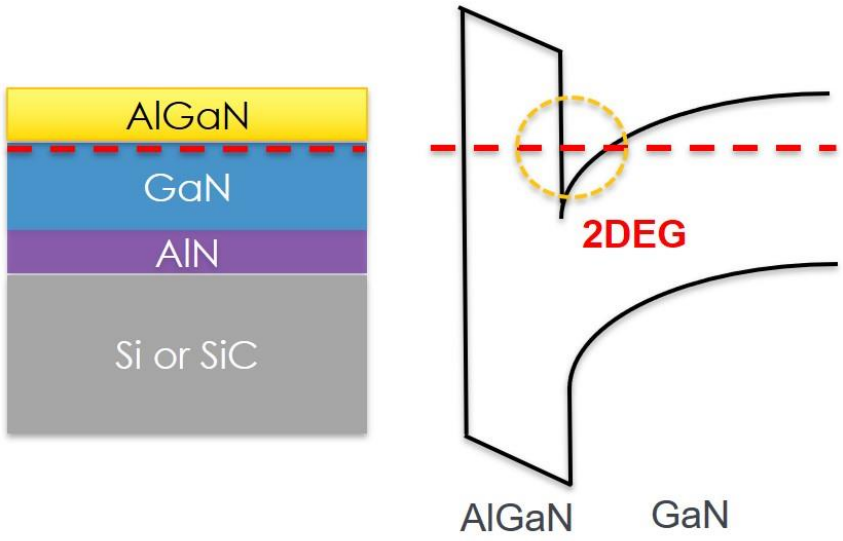


Figure 1.5. Schematic and band diagram of AlGaN/GaN 2DEG layer.

GaN is binary III-V compound semiconductor with a wide band gap of 3.4 eV making it favorable for high power and frequency applications. While GaN was typically grown or deposited on silicon carbide (SiC), recently, it has been successfully grown on silicon, which triggered new interest in this semiconductor, due its compatibility with conventional CMOS processing and reduction in substrate cost.

A unique feature of this III-V semiconductor is that, it can form a two-dimensional electron gas (2DEG) when combined with other compound semiconductors such as AlGaN. Figure 1.5 illustrates the multi-layer III-V semiconductor structure to form such 2DEG and its band diagram. A buffer layer (AlN) is usually grown on top of bulk substrate followed by the GaN/AlGaN to form the 2DEG. This 2DEG is a layer of electrons which are free two travel parallel to the interface while simultaneously confined perpendicular to the sheet of electrons, making it quasi two-dimensional.

1.3 Two-Dimensional Materials

Graphene is a 2D material consisted of carbon atoms in a hexagonal lattice bonding structure. A monolayer of graphene is a zero band gap material with electron mobilities reaching over 100,000 $cm^2/V \cdot s$. Ever since the discovery of graphene by the famous 'scotch tape' method, extensive study on graphene along with other 2D materials have be conducted. [5]

Hexagonal boron nitride (h-BN) is another type 2D material in which boron and nitrogen atoms are bonded in a hexagonal array. While graphene is a semi-metal material, h-BN is a dielectric material with exceptional chemical stability, high mechanical flexibility, thermal conductivity and oxidation resistance gaining great interest. [6-7]

While exfoliated 2D materials generally show superior quality and device performance, its size limits from any practical applications. Thus, growing large area 2D materials by methods such as chemical vapor deposition (CVD) have also been extensive researched for various optoelectronic applications.

1.4 Kerf-less Exfoliation of Semiconductors

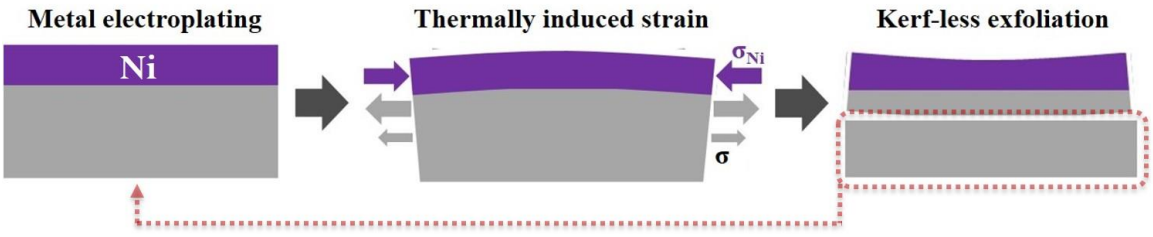


Figure 1.6. Schematic of kerf-less exfoliation process.

Flexible optoelectronic devices have gained much interest from wearable devices to internet of things (IoT). Conventional bendable devices are made on flexible materials such as polymers, plastics or thin glass. For devices fabricated on semiconductor wafers, the common method is thinning down the silicon wafer through wet etching.

Recently, a mechanical exfoliation process of semiconductors which does not require semiconductor etch has been developed. [8] The process consists of depositing a metal layer (through electron beam evaporation and electroplating) on top of the semiconductor followed by a thermal cycling process. Thermally induced stress is created along the metal/semiconductor interface due to the thermal expansion mismatch between the two materials. When the amount of stress is properly controlled, the stress is kept within the interface. A crack is induced at the edge of the semiconductor wafer which results in the release of stress propagates along the semiconductor surface. By controlling the amount of stress, we can control the thickness of the exfoliated semiconductor thickness. Figure 1.6 illustrates the kerf-less exfoliation process. Some advantages of this technique are,

(1) This process can be applied to any semiconductors with the right exfoliation recipe.

(2) The parent wafer can be re-used for fabrication or exfoliation.

(3) The thickness of semiconductor film can be accurately controlled.

1.5 Organization of Dissertation

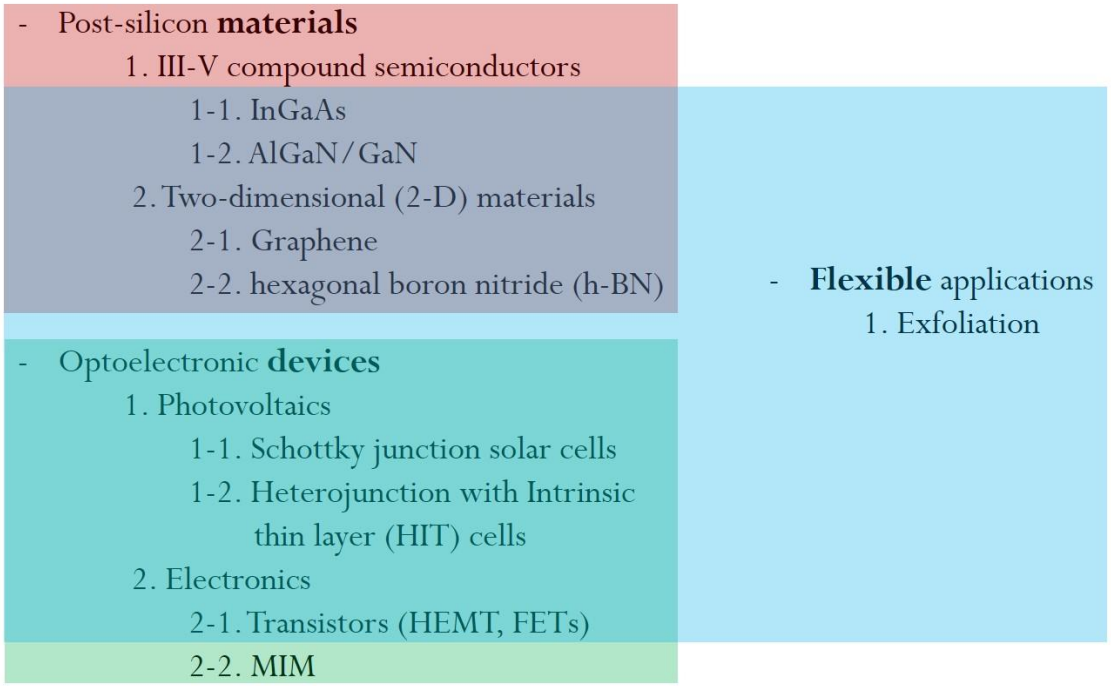


Figure 1.7. Graphic chart of this dissertation.

Figure 1.7 organizes the dissertation into three categories; materials, devices, and flexible applications. Materials are highlighted in red, devices in green and flexible applications of materials and devices are overlapped in blue.

This dissertation is consisted of 7 chapters, Chapter 2 and 3 covers InGaAs, which describes a new way of effectively doping the material as well as introducing a thin layer of indium between the InGaAs and metal contact pad to prevent the out-diffusion of indium during hot temperature processes.

GaN, which is another type of type of III-V compound semiconductor is described in chapter 4, focusing on exfoliation of AlGaN/GaN 2DEG and demonstration of HEMT devices.

Chapter 5, 6 covers 2D materials including graphene and h-BN and its application in bendable organic/inorganic solar cells, FETs and resistive switching applications.

Finally, Chapter 7 summarizes the work followed by future work regarding this dissertation.

Chapter 2. Nanoscale Doping of Compound Semiconductors by Solid Phase Dopant Diffusion *

2.1. INTRODUCTION

In the unceasing pursuit of scaling down semiconductor devices, high mobility compound semiconductors have gained great interest as future candidate materials beyond silicon [9-12]. To successfully develop devices in the post-silicon regime, effective doping of these compound semiconductors is essential. It is often more challenging to remove ion implantation-induced damage in compound semiconductors than in silicon due to incongruent evaporation during annealing, which leads to increased junction leakage and interferes with dopant activation [13-17]. In addition, there are challenges with ion implantation for doping of 3 dimensional (3-D) structures, such as fin field effect transistors (FinFETs), where shadowing effects of the ion beam result because ion implantation is a line-of-sight process. Such shadowing effects require changes in structure optimization for FinFETs, which, in turn, requires increases in process complexity, cost and time. To overcome these limitations, alternative doping strategies have been studied for compound semiconductors, such as monolayer doping (MLD), solid phase regrowth (SPR) and surface charge transfer doping [18-21].

In this chapter, we propose a novel method for solid phase doping of compound semiconductors, in this case InGaAs. With this method, we demonstrate that silicon or

* This chapter is based on Reference: J. Ahn, H. Chou, D. Koh, T. Kim, A. Roy, J. Song, and S. K. Banerjee, Nanoscale doping of compound semiconductors by solid phase dopant diffusion. *Appl. Phys. Lett.,* **2016**, *108*, 122107. J.A., H.C. and T.K. designed the experiments (DOE), J.A. and D.K. carried out device fabrication, J.A, H.C, A.R, and J.S. conducted characterization of devices.

oxygen atoms from a deposited SiO_x layer on InGaAs can diffuse into InGaAs during post-deposition annealing, as illustrated in figure 2.1.

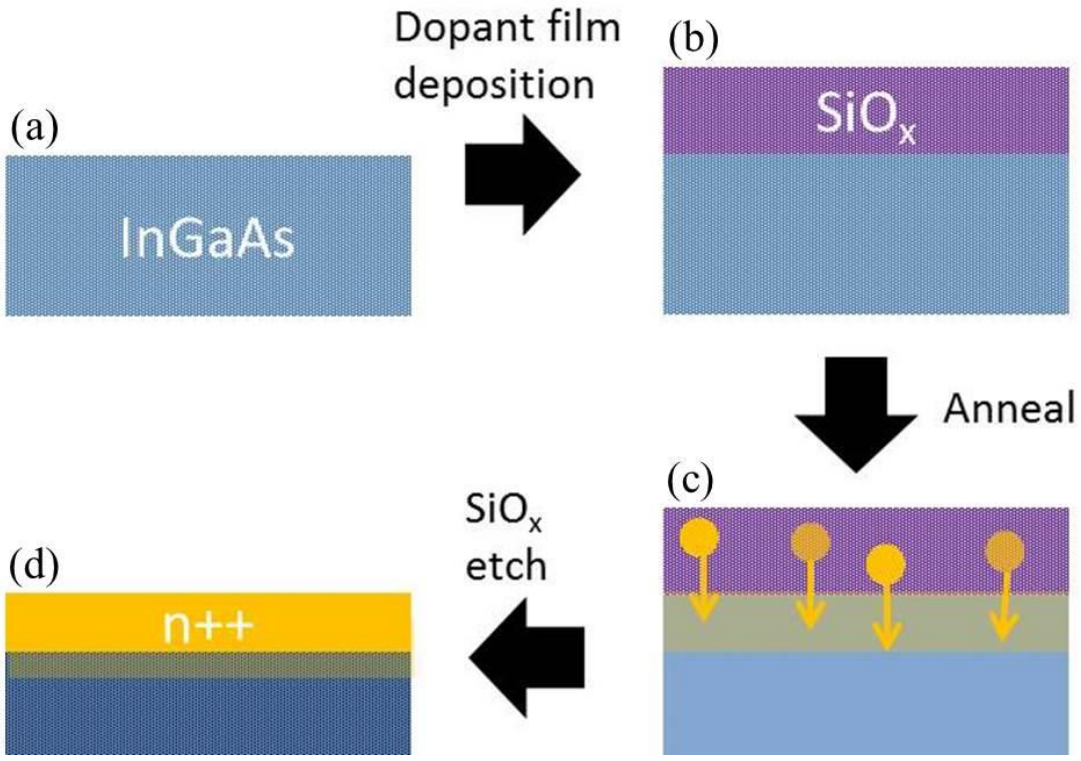


Figure 2.1: Schematic diagram of solid dopant based doping process.

2.2. SAMPLE PREPARATION

The InGaAs samples were cleaned prior to deposition. The samples consist of GaAs (300 nm), InP (850 nm), InAlAs (300 nm) and $In_{0.53}Ga_{0.47}As$ film (300 nm) grown on silicon substrates by molecular beam epitaxy (MBE). The deposition of SiO_x films was carried out by plasma enhanced chemical vapor deposition (PECVD) at 285 ˚C and 900 mTorr with RF power of 30 W and various N_2O/SiH_4 gas flow ratios [22]. The

samples were then annealed in a N_2 ambient for 10 minutes at 700 ˚C. The SiO_x films were then etched off with HF and metal contacts (Mo/Ti/Au=20/40/100 nm) were immediately deposited on the InGaAs samples using electron beam evaporation patterned via metal shadow mask for electrical transport and Hall effect measurements.

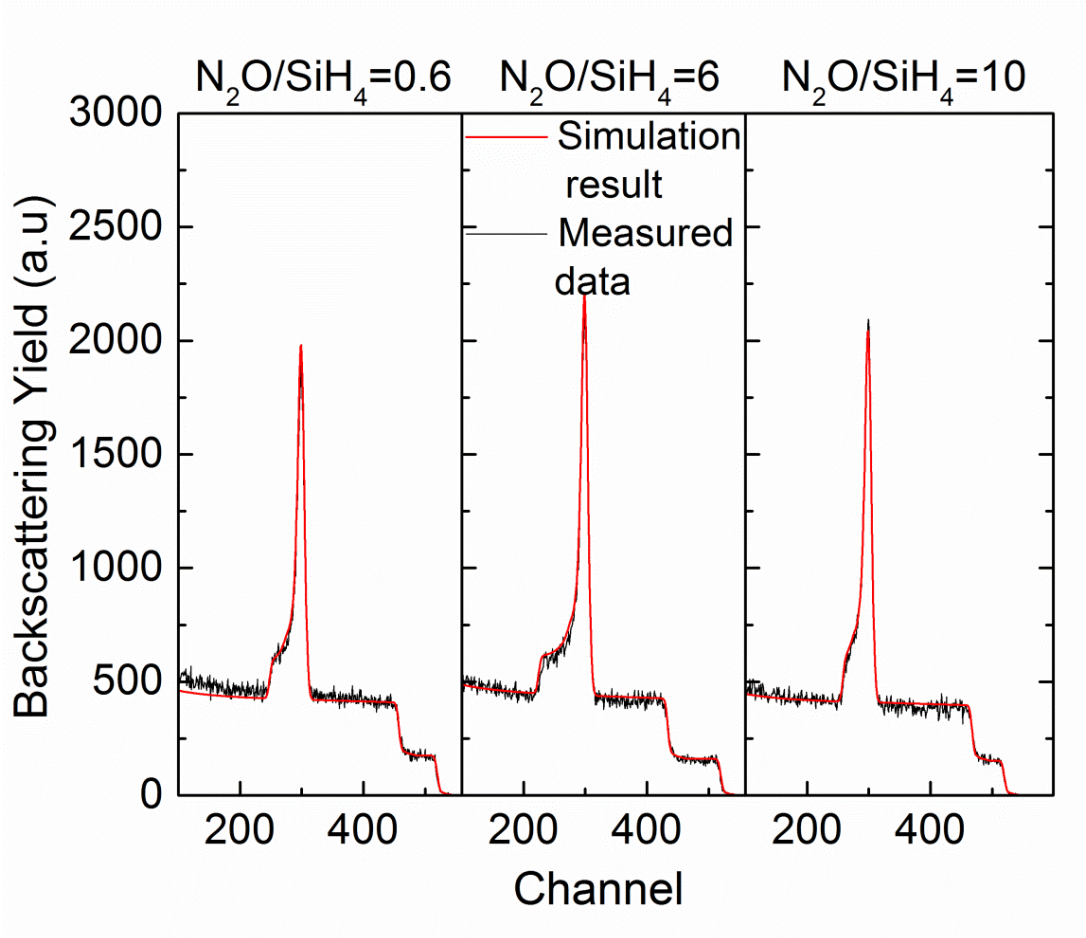


Figure 2.2: RBS measurement of SiO_x deposited samples with different gas flow rate.

2.3. Results and Discussion

Figure 2.2 shows the Rutherford backscattering spectrometry (RBS) analysis results for the various SiO_x films which were deposited on silicon substrates in parallel with the InGaAs films. RBS measurement was done with a NEC 6SDH-2 accelerator and ion

beam analysis system. In order to enhance the oxygen scattering cross-section, He^{2+} incident ions were used at an energy of 3.05 MeV. In addition, the RBS data was taken at a laboratory scattering angle of 170^0 with a detector of 14 keV nominal energy resolutions. These SiO_x films used for characterization were deposited on silicon substrates that were put in the deposition chamber simultaneously with InGaAs film substrates. From the RBS measurements, we were able to determine the composition and thickness of each SiO_x film. The RUMP code was used for quantitative analysis of the measured RBS spectra [23]. Table I summarizes the Si –to-O ratio for three different gas flow deposition conditions. Depending on the gas flow ratio, the deposited SiO_x films resulted in silicon rich silicon oxide (SRSO, SiO_x, $x<2$) or oxygen-rich silicon oxide (ORSO, SiO_x, $x>2$) [24].

	Element ratio	
N_2O/SiH_4 ratio	**Silicon**	**Oxygen**
0.6	1	0.6
6	1	6
10	1	10

Table 2.1: RBS measurement of SiO_x deposited samples with different gas flow rate.

In order to verify the doping efficacy of our technique, current-voltage measurements were made for InGaAs samples doped by SRSO and by ORSO. Figure 2.3 shows the I-V characteristics in the InGaAs layer after SiO_x film deposition, annealing and etch. A higher doping level was obtained with ORSO compared to SRSO.

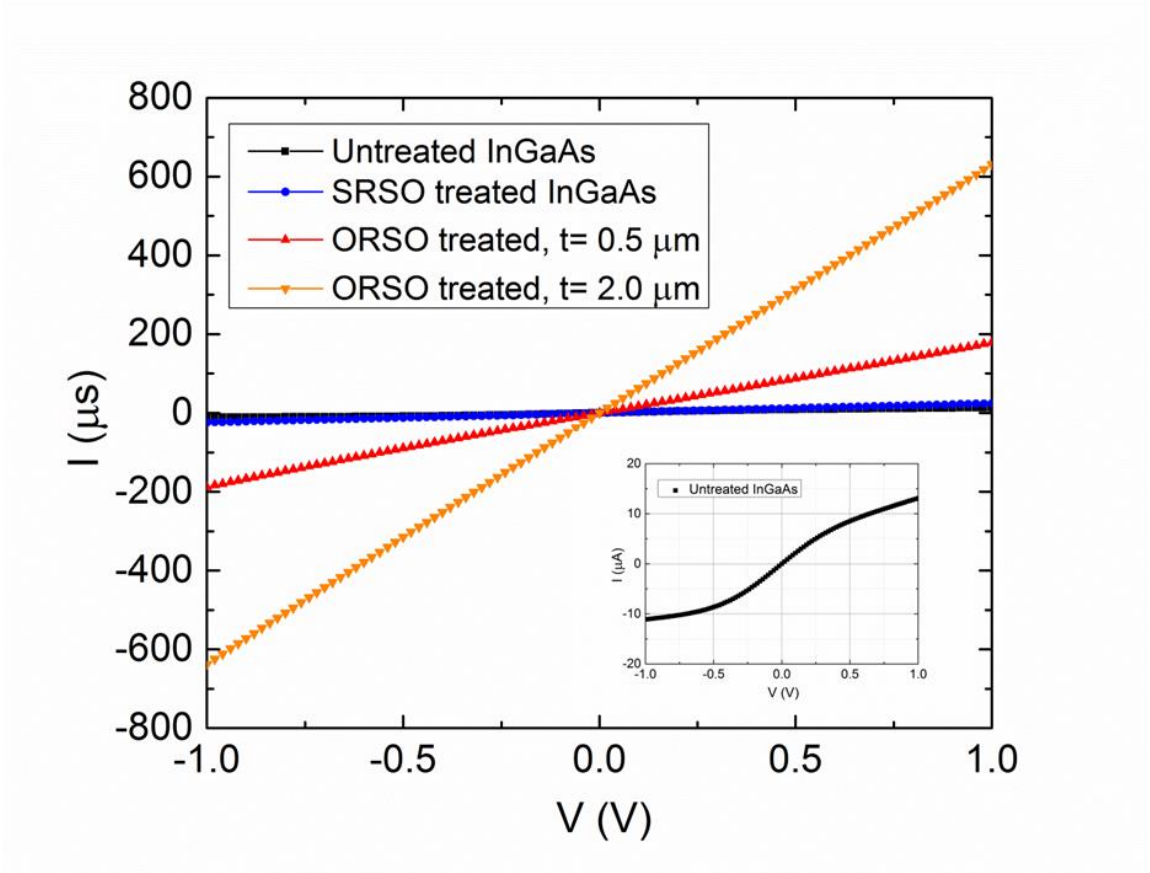


Figure 2.3: I-V characteristics for InGaAs layer after SRSO and ORSO doping process. Inset shows the result from the untreated InGaAs as a reference with a magnified scale.

In addition, the current in InGaAs from the ORSO-deposited sample was two orders of magnitude higher in comparison to the SRSO-deposited sample, when the thickness of the ORSO and SRSO films were similar. When a thicker (2 µm) ORSO film was deposited (compared to the thinner, 0.5 µm, film), the current flow in the InGaAs layer was three times greater than in the current in the thinner ORSO film. These results indicate that oxygen in-diffusion is related to InGaAs doping.

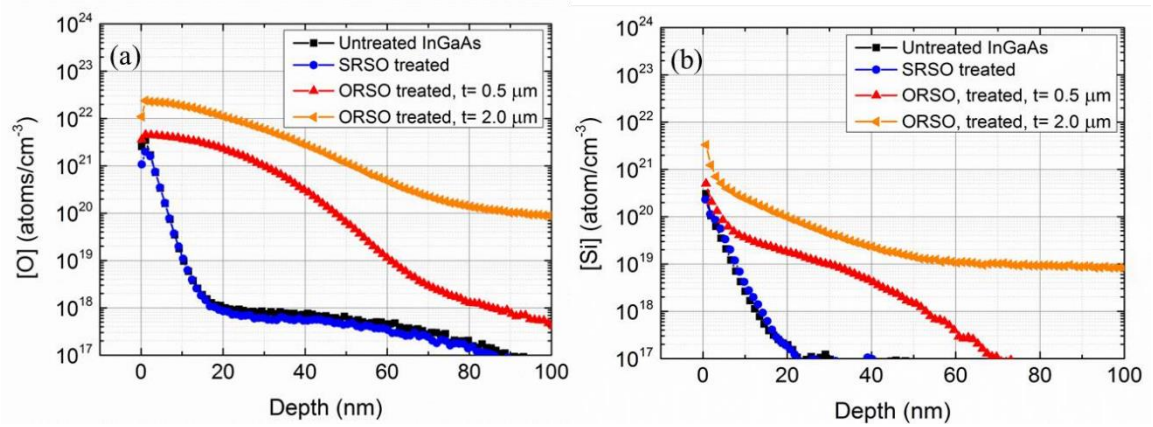


Figure 2.4: SIMS profile of (a) silicon and (b) oxygen for SRSO & ORSO treated 100 nm thick InGaAs samples.

Figure 2.4 shows the secondary ion mass spectrometry (SIMS) depth profiling results for the InGaAs layers after doping. The analysis shows that (1) more oxygen than silicon is incorporated in the InGaAs and (2) the oxygen concentration is further increased in the InGaAs layer with a thicker ORSO film. This is consistent with the findings from the I-V measurements. To confirm the role of oxygen inside InGaAs, ion implantation was conducted for comparison. 20 keV oxygen ions were implanted into InGaAs at three different doses ($3x10^{13}$, $3x10^{14}$ and $3x10^{15}$ cm^{-2}), giving an implant depth of 41 nm [25]. Following implantation, the samples were capped with 20 nm of Al_2O_3 by atomic layer deposition (ALD) and annealed with the same conditions as the SiO_x treated samples. A control InGaAs sample was deposited with Al_2O_3, annealed, and etched to remove Al_2O_3, and tested as a control to confirm that the Al_2O_3 capping layer does not play any role in InGaAs doping.

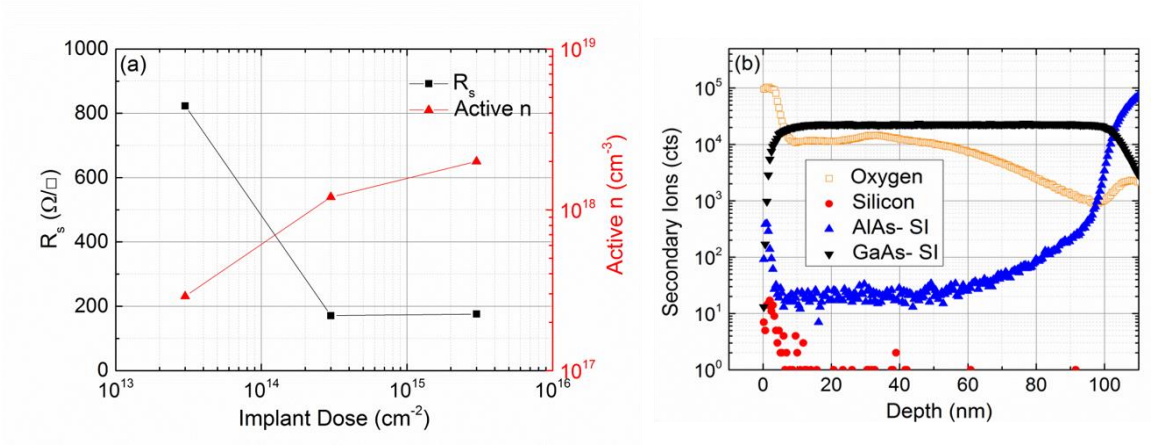


Figure 2.5: (a) Sheet resistance and active doping concentration of oxygen implanted InGaAs samples. (b) TOF-SIMS profile of oxygen implanted InGaAs sample.

Figure 2.5(a) shows that there is an increase in active dopant concentration in oxygen-implanted samples in proportion to oxygen dose, and a reduction in sheet resistance. To show that ion implantation did not otherwise alter the structure of the InGaAs sample, depth profiles of the oxygen-implanted InGaAs samples were taken with time-of-flight SIMS (TOF-SIMS) as shown in Figure 2.5 (b). The depth profiles show that no silicon or other out-diffusion of underlying layers occurred to impact the InGaAs film. This indicates that oxygen indeed appears to act as an n-type dopant at active dopant concentrations that have not been reported to date. The SIMS depth profile shows the dopant distribution with respect to depth, whereas the current-voltage measurement reflects an average dopant concentration. The InGaAs sample doped with thick ORSO film showed an active doping concentration of 1.4×10^{18} cm^{-3}, which is comparable to other doping methods including ion implantation.

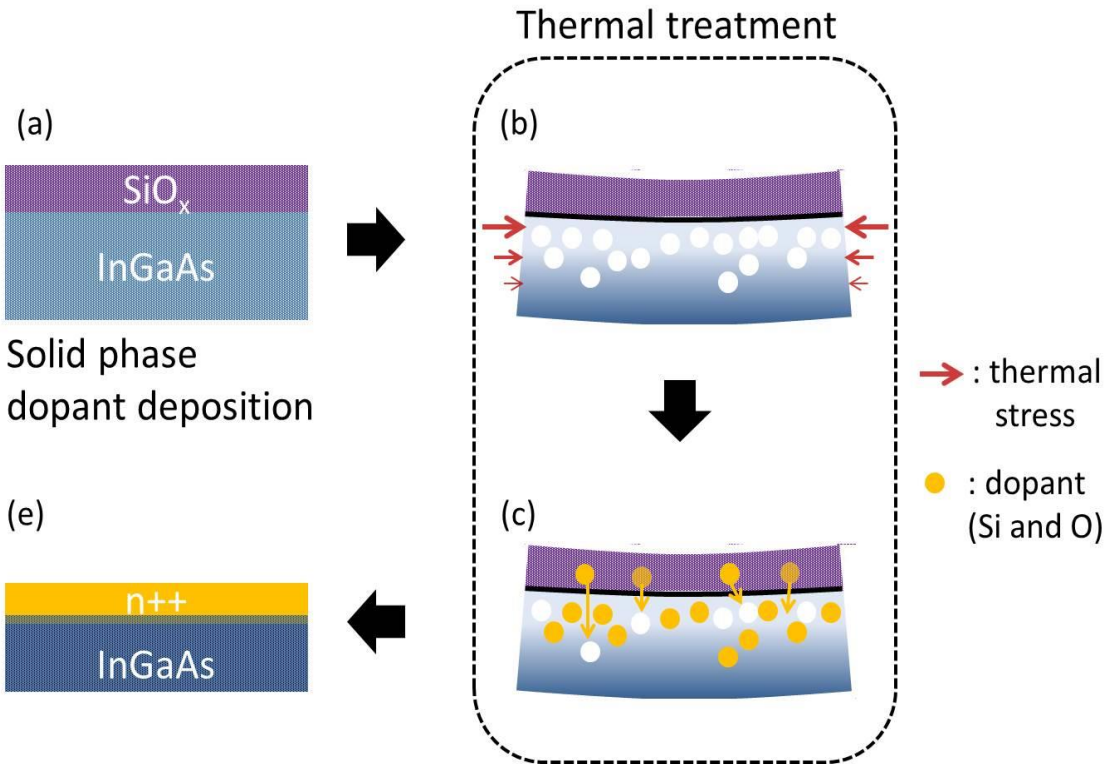


Figure 2.6: Illustration of vacancy formation and dopant diffusion into InGaAs.

It has been previously reported that an increase in compressive stress within a GaAs substrate can generate vacancies via enhanced gallium diffusion and arsenic-antisite defects [26-27]. This extrinsic stress occurs because of the difference in the coefficient of thermal expansion (CTE) between SiO_2 ($0.55x10^{-6}$ K^{-1}) and GaAs ($6.86x10^{-6}$ K^{-1}). Similarly, vacancies can be formed due to the thermal stress between SiO_x and InGaAs in the InGaAs substrate (figure 2.6(b)). In addition, the amount of vacancies generated within InGaAs is greater in the thicker ORSO (2 µm) than in the thinner ORSO (0.5 µm). This is because increasing the film thickness generates more stress, which leads to an enhancement of the vacancy formation phenomenon. This, in turn, increases the probability for dopants to diffuse into InGaAs (figure 2.6(c)).

In addition to the conventional annealing temperature and time process parameters, our method provides an additional parameter available to control doping (i.e. solid source film thickness and stoichiometry). The high concentration of oxygen compared to silicon inside InGaAs can be understood by considering the diffusivity of each element, which is dictated by an Arrhenius relation. Oxygen has a lower activation energy for diffusion (E_A= 1.1 eV) compared to silicon (E_A =2.2~2.8 eV) in GaAs, an analogue of InGaAs [28]. In the case that oxygen has a lower energy barrier for diffusion into InGaAs, it allows a higher doping concentration at a given temperature.

Oxygen impurities in III-V semiconductors have typically been considered as contaminants that create energy levels near mid-gap [29-32]. However, oxygen has also been shown to increase the free carrier density in GaAs and InGaAs in some cases, presumably due to differences of the where the oxygen sits in the lattice and how it affects the bandstructure [32-34]. Although the fundamental mechanism of how oxygen acts as a dopant was not elucidated in our work, the use of ORSO demonstrates a new approach for effectively doping III-V compound semiconductors. It also points out a potential unintentional doping effect when applying silicon processes to compound semiconductors, such as for silicon dioxide-based device isolation. While this isolation method is effective for conventional silicon-based technology, unintended doping can occur for compound semiconductors during a similar process steps and can negatively affect device performance.

2.4. Conclusion

In conclusion, we were able to demonstrate a simple technique for doping compound semiconductors through PECVD SiOx. As oxygen has a lower activation energy for diffusion, it diffuses more easily than silicon into InGaAs, leading to n-type doping. This solid phase doping method can be applied to other semiconductors by choosing appropriate films. Our method provides an alternative way to overcome one of the challenges of doping compound semiconductors, such as InGaAs.

Chapter 3. Low Contract Resistivity Indium Metal Contacts on InGaAs and GaAs exfoliation

In this chapter, we studied the interfacial characteristics, electrical properties, and thermal stability of indium ohmic contacts on n-type $In_{0.53}GaAs$. TEM, XRD, SIMS and EDS analysis show ultra-shallow diffusion of indium into $In_{53}GaAs$ layer after annealing and formation of higher indium concentrated thin In_xGaAs ($x > 0.53$) phases at the indium/$In_{53}GaAs$ interface. Electrical measurements of TLM patterns and InGaAs MOSFETs show indium contacts (8×10^{-7} $\Omega\cdot cm^2$) are comparable to Mo (3.2×10^{-6} $\Omega\cdot cm^2$) based devices even after annealing temperatures of 400 ^oC. A thin layer of GaAs, an analogue of InGaAs, was successfully spalled using the kerf-less mechanical exfoliation technique.

3.1. INTRODUCTION

One major challenge in achieving high performance III-V MOSFETs is minimizing the parasitic resistance, including metal/semiconductor contact resistance.

One cause of increased contact resistance for metal/InGaAs is the out-diffusion of gallium at elevated temperatures which form gallium-based alloys with high resistivity. [34] Therefore, low resistivity of metal/Ga alloy is needed. From literature survey, indium/Ga alloy have lower resistivity compared with other Ga based alloys and equal resistivity with Gallium which is plotted in Fig 3.1. [35] Fig 3.2 describes the ideal and practical models of metal/semiconductor interface characteristics. Applying inter-diffusion, strong chemical reactions and formation of new metallurgical compounds, the mixed interface Schottky model is considered for detailed understanding of metal-InGaAs interface. To achieve low contact resistivity based on the mixed interface Schottky model, low workfunction,

electronegativity and electrical resistivity are required. From these conditions, indium, (electronegativity: 1.78, workfunction: 4.12 eV, electrical resistivity: 83 nΩ·m) is a suitable candidate.

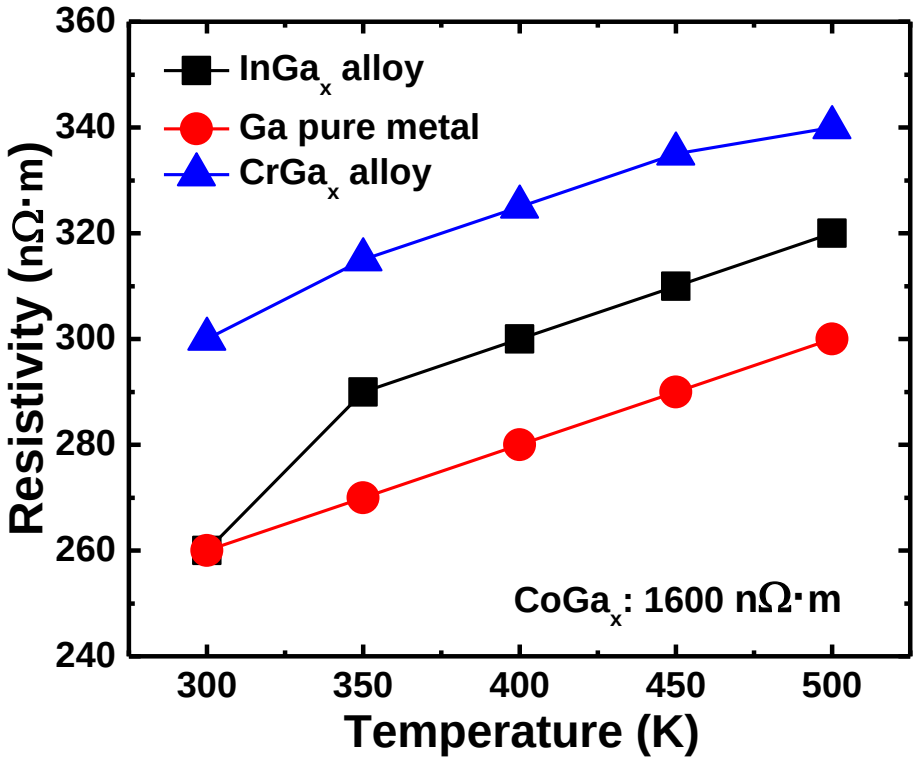


Figure 3.1: Electrical resistivity of various metal/Ga alloy and Gallium between 300 and 500 (K) from literature survey.

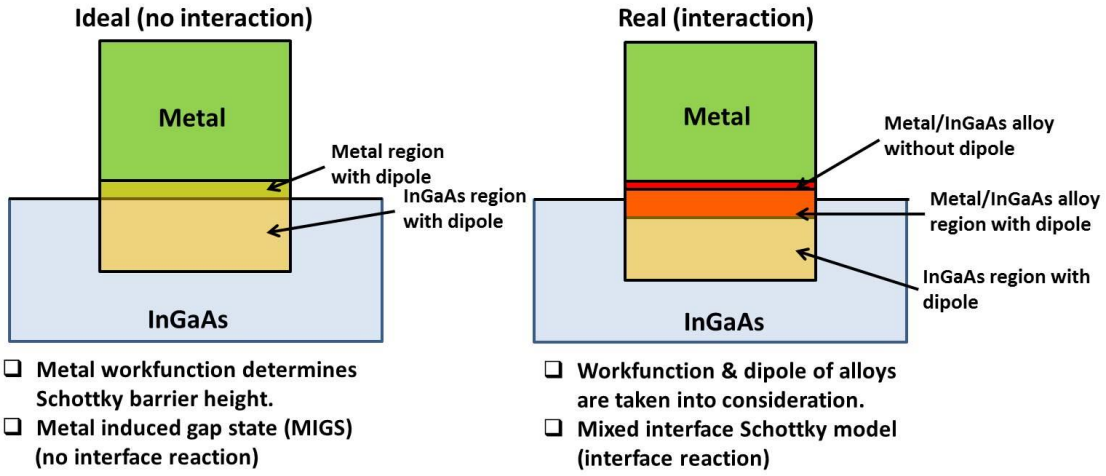


Fig 3.2: Schematic of ideal/real case metal/InGaAs interface phenomenon and theoretical models for each case.

3.2. EXPERIMENTAL

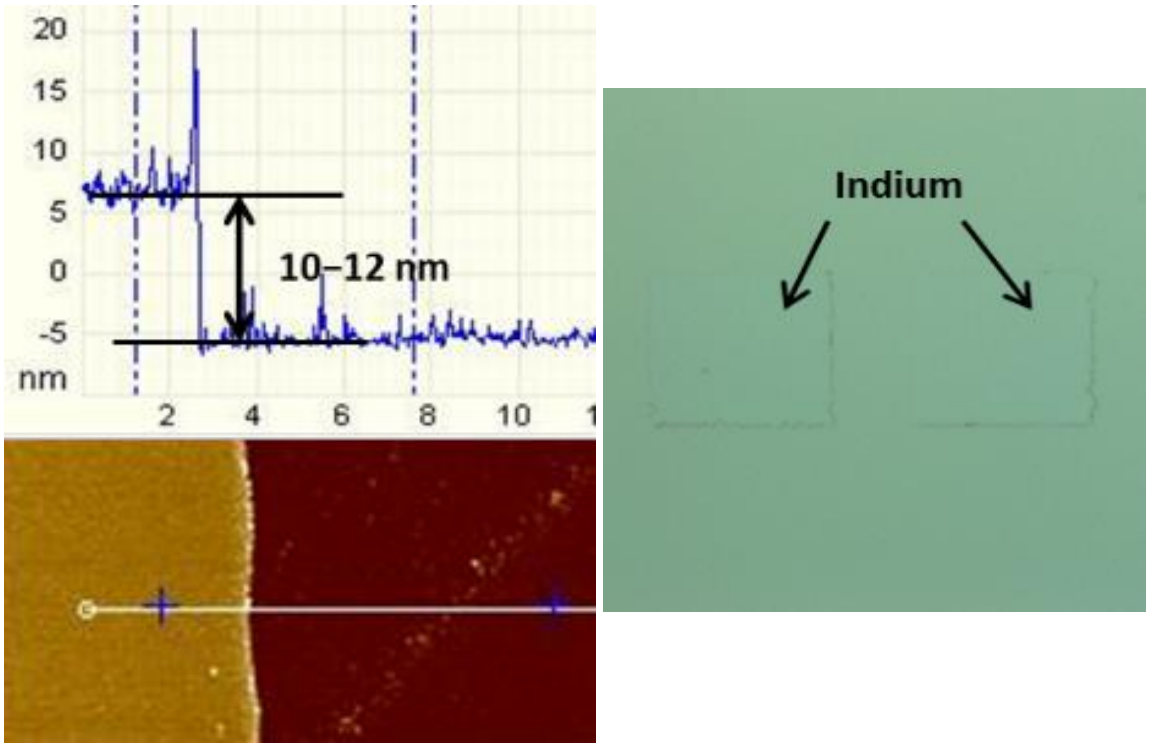


Figure 3.3: AFM & Optical microscope image of indium contact after ultra-sonication.

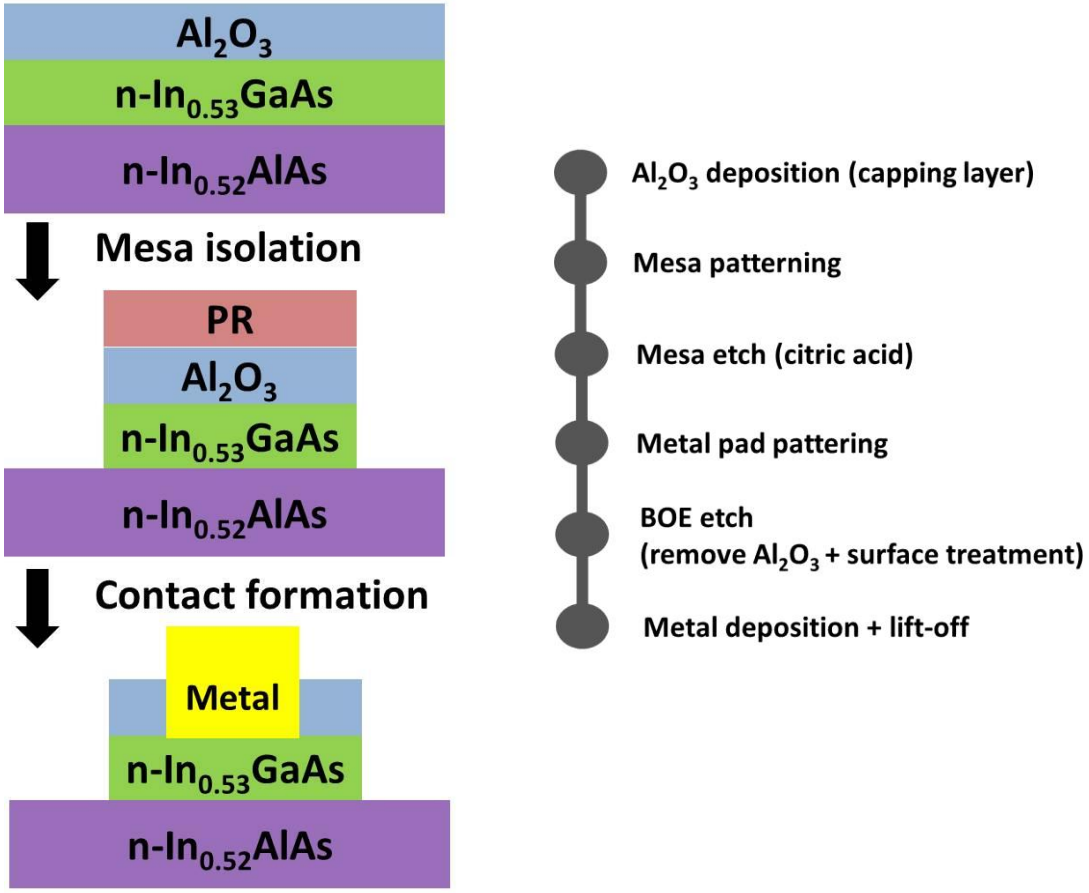


Figure 3.4: Schematic diagram and process flow of TLM fabrication.

AFM and optical images in Fig. 3.3 show that 10 ~ 12 nm of indium remains intact after e-beam evaporation, followed by 10 min, ultra-sonication. Fig. 3.4 describes the schematic for TLM pattern fabrication. 30 nm thickness of gold is used as pad metal for probing the TLMs and MOSFETs. Indium contacts show good thermal stability of resistance, comparable with Mo and Ti, after 400^{o}C annealing. (Fig. 5) In Fig. 3.6, indium contact shows lower specific contact resistivity (ρ_c) than Mo after 400^{o}C annealing. Optimization of surface treatment can further lower ρ_c. Indium contacts with various thicknesses do not show any significant degradation with Ti in Fig. 3.7.

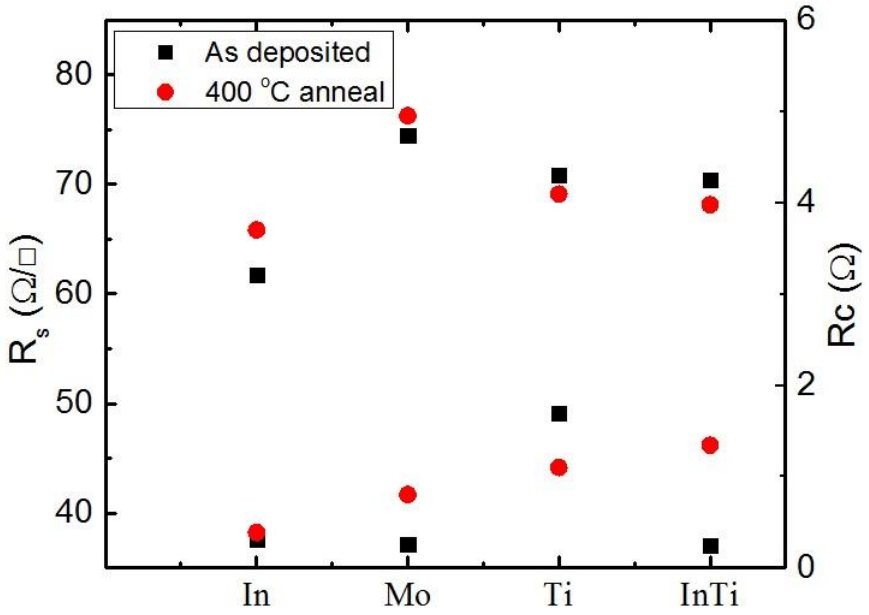


Figure 3.5: Sheet and contact resistance for various TLM devices before and after annealing (10 minute anneal).

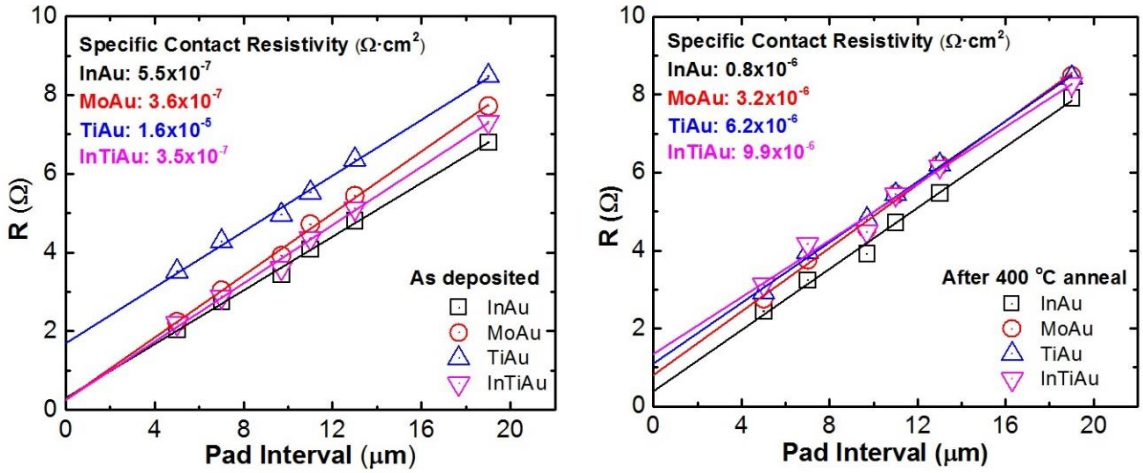


Figure 3.6: TLM pad resistance as a function of pad spacing for various metal ohmic contacts on n-$In_{53}GaAs$ (30 nm)/InAlAs (130 nm)/InP with doping concentration of 3×10^{19}.

Fig. 3.8 shows STEM image and EDS mapping results of indium TLM devices before and after annealing. The color brightness is proportional to the number of counts during EDS mapping. From Fig 8, the interface of indium/InGaAs became uneven after annealing, which indicates the inter-mixing. And Ga is diffused out to the metal contact while arsenic shows distinct boundaries. The trench in TEM is the area of mesa etch, not any result of metal diffusion. Fig. 3.9 shows the EDS line scan result of the two samples, which further supports the increase of indium content after annealing. The color brightness of each image is proportional to the counts of each element.

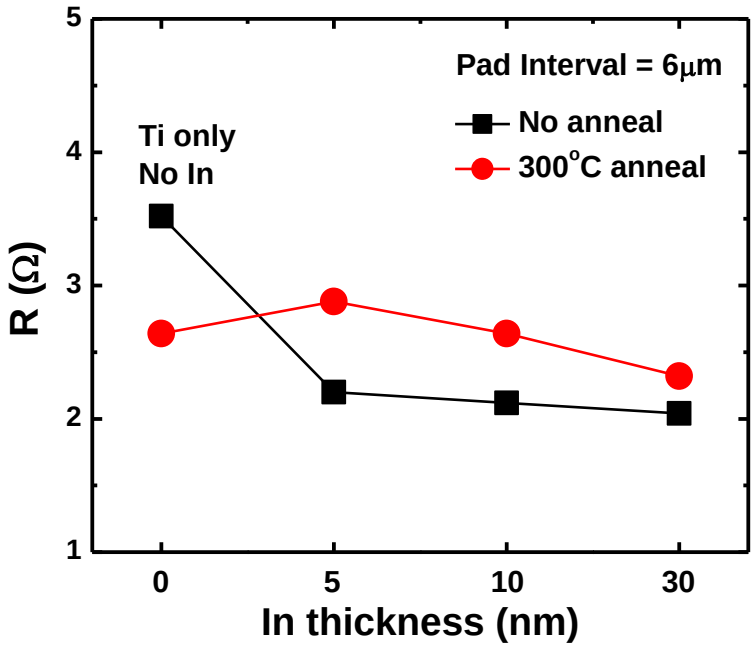


Figure 3.7: Effect of indium thickness in indium (5, 10 nm)/Ti(30 nm) on InGaAs before and after annealing.

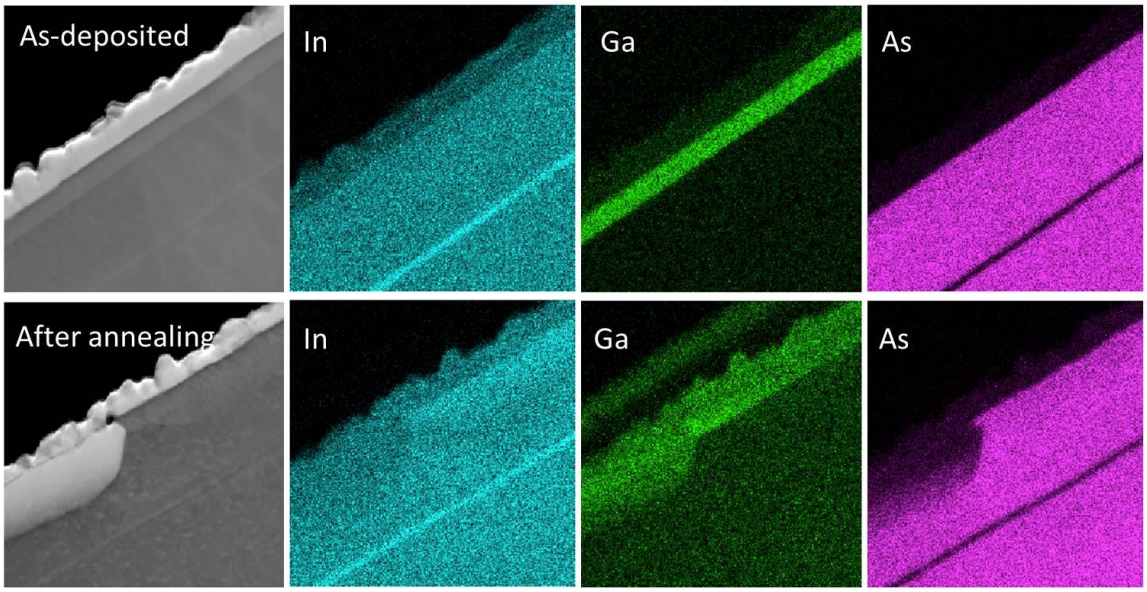


Figure 3.8: STEM image and EDS mapping of In, Ga, and As, elements. Brightness of the color is proportional to the counts of each element.

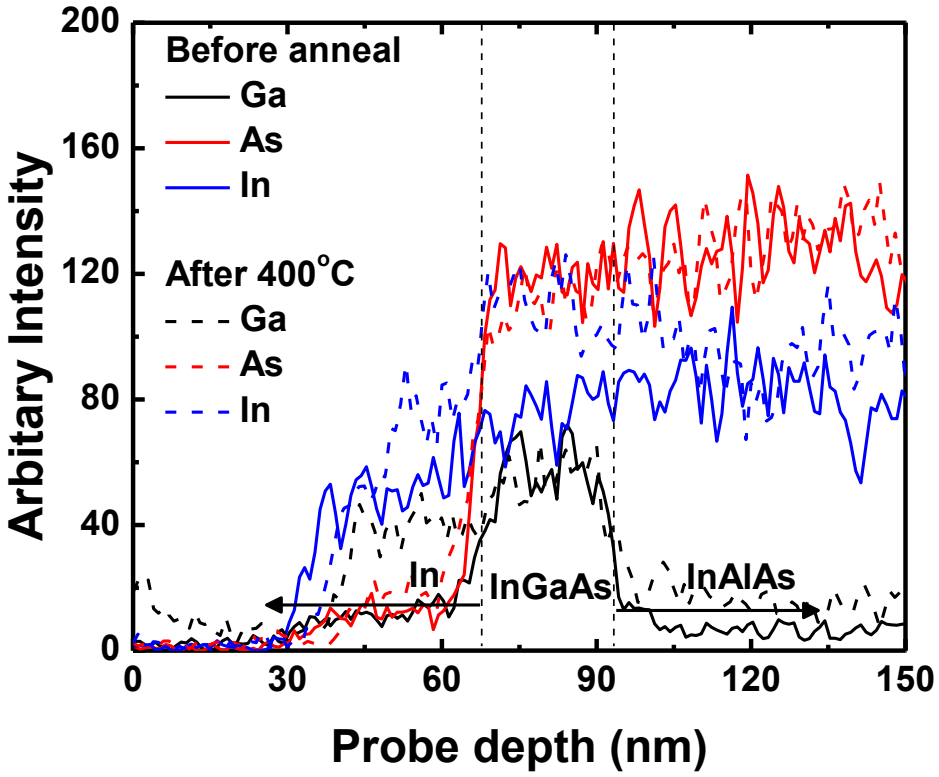


Figure 3.9: EDS of In (30 nm) before and after 400°C anneal.

Fig 3.10 is SIMS analysis of Ti/indium on InGaAs. Indium/InGaAs boundary is not discernible, which may indicate the interfacial reaction of indium/InGaAs. HRXRD analysis of indium (30 nm) before and after 300, 400°C annealing (Fig. 3.11) show minute change of InGaAs signal (all InP signals are aligned), which indicates ultra-shallow diffusion depth of the increased indium concentration on $In_{0.53}GaAs$ after annealing. (The change of indium concentration was simulated using Bede RADS and shows that indium inside InGaAs increased from 53% to 60% with roughly 10 ~ 30 Å diffusion depth with limited fitting accuracy.) And indium diffusion was reported in which indium diffuses into GaAs with anneal [36]. Fig 3.12 illustrates the schematic band

diagram of indium/$In_{0.53}GaAs$ structure before and after annealing, deduced from EDS analysis and literature.

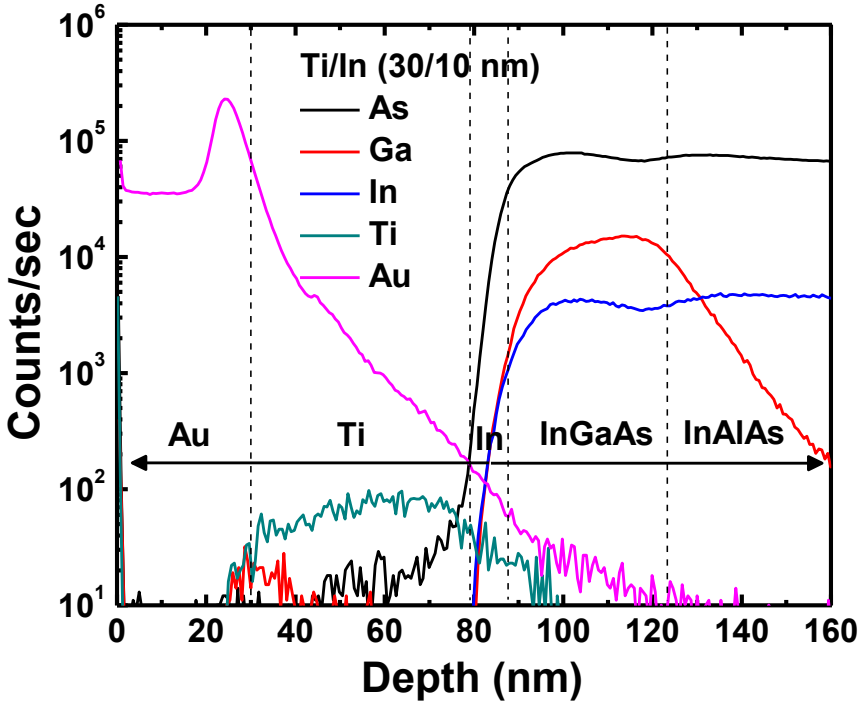


Figure 3.10: SIMS profile of Ti (30 nm)/In (10nm) on n-$In_{53}GaAs$.

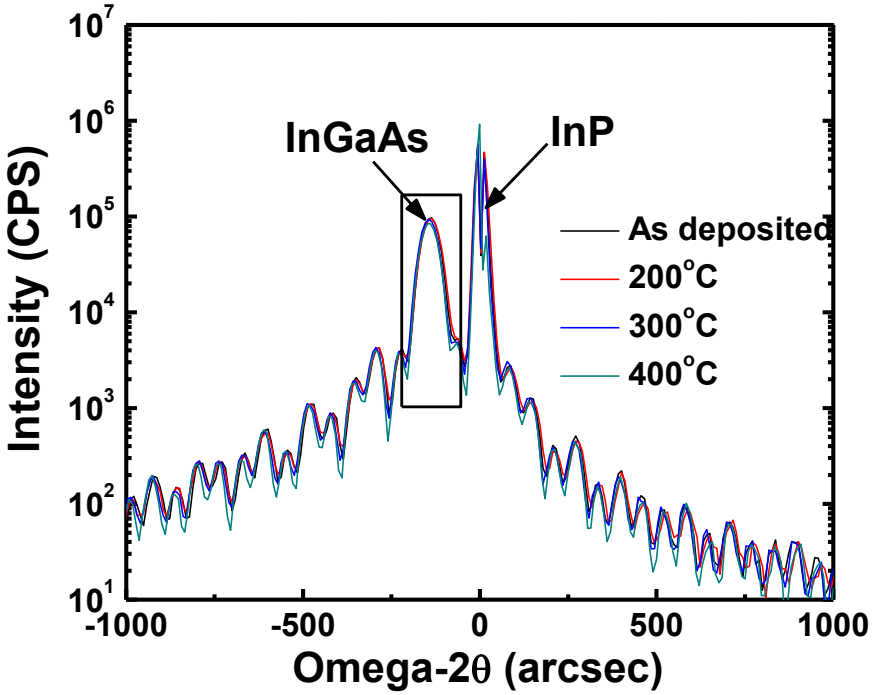


Figure 3.11: HRXRD analysis of indium (30 nm) on n-$In_{53}GaAs$ before and after 300°C and 400°C anneal.

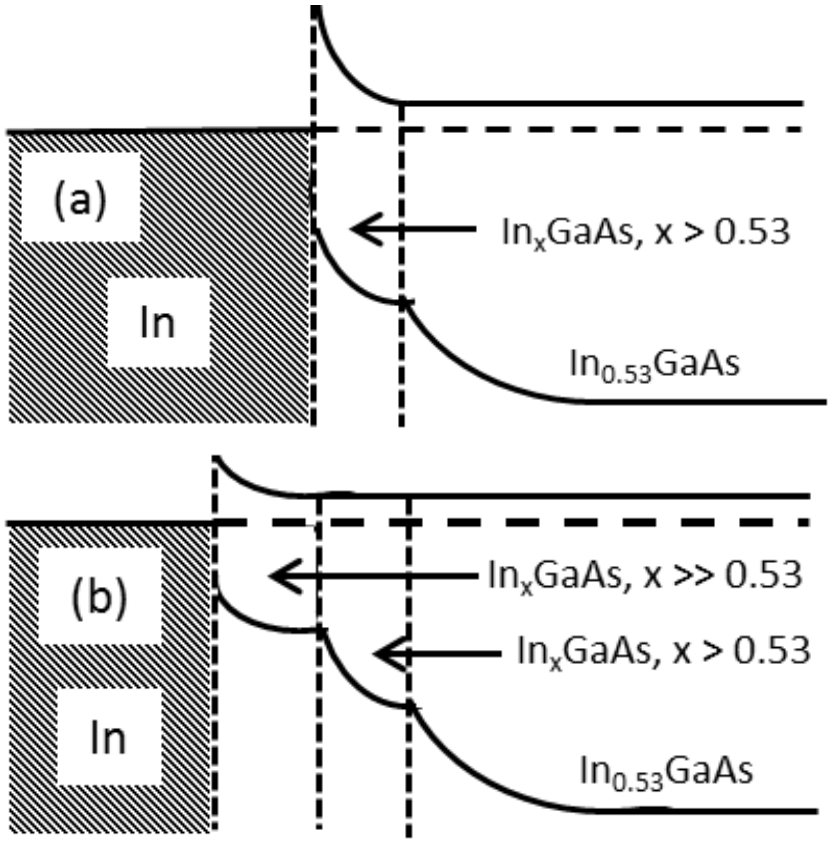


Figure 3.12: Schematic band diagram of In / $In_{0.53}GaAs$ structure with (a) low (b) high temperature anneal. Diffusion depth may be ultra-shallow (10 ~ 30Å).

TEM analysis (Fig. 3.13) shows inter-mixing at the interface of indium/InGaAs before and after 400^{o}C annealing. Fig 3.14 describes the fabrication process of gate-last MOSFET fabrication used in this study (Si ion implantation at 35 keV, $5\times10^{14}/cm^2$, activation temperature at 700^{o}C 10sec). Post deposition anneal (PDA) was conducted at temperature 400 ^{o}C to reduce the interface trap density (D_{it}) of Al_2O_3. Fig. 3.15 is a summary of V_g vs. I_d characteristics in gate-last processed InGaAs MOSFETs with indium (30 nm)/Au (30 nm) or Mo (30 nm)/Au (30 nm) source/drain contacts at channel length of (a) L = 5 μm and (b) L = 10 μm. Indium contacts show similar drive current at

various channel lengths, compared with that of Mo, consistent with TLM results. Slightly higher subthreshold swing of Mo may be due to the change of surface morphology, caused by high energy transfer from Mo to InGaAs. Utilizing sputtering instead of e-beam evaporation may avoid this issue. V_{th} and DIBL are also similar between indium and Mo contacts in Fig. 3.16. Source/drain contact resistance (R_{SD}) and channel length offset (L_{off}) for (a) indium and (b) Mo in Fig. 3.17 were linearly extrapolated from the results of Fig. 3.15. Indium and Mo contacts show the same R_{SD}, but Mo clearly shows higher value of L_{off}. Higher thermal energy required for Mo during e-beam evaporation may have impacted the lateral diffusion of Si dopants, compared with indium.

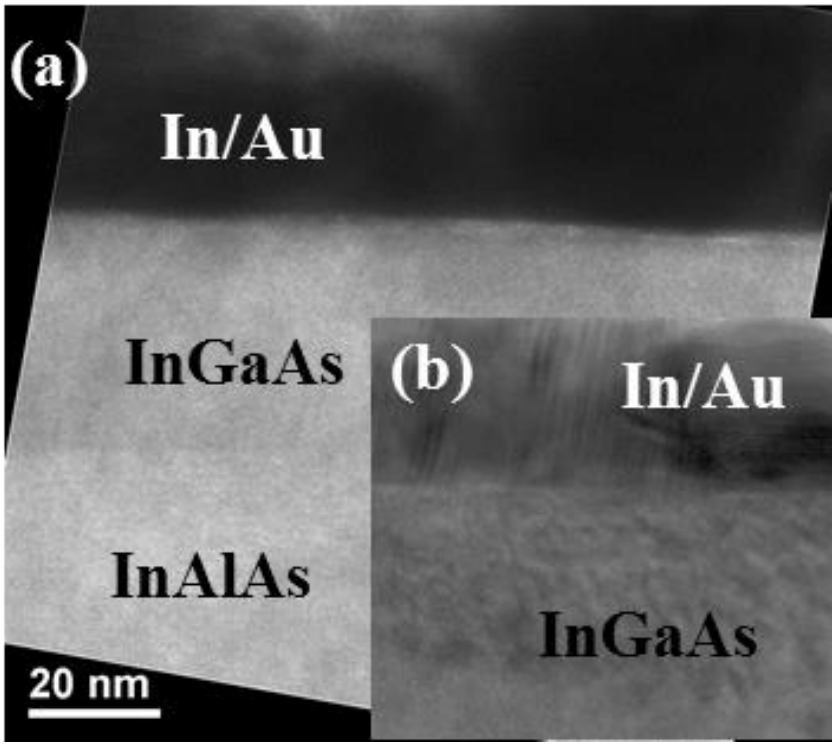


Figure 3.13: HRTEM image of indium (30 nm)/InGaAs (a) before and (b) after 400°C annealing. Inter-mixing is observed at the interface.

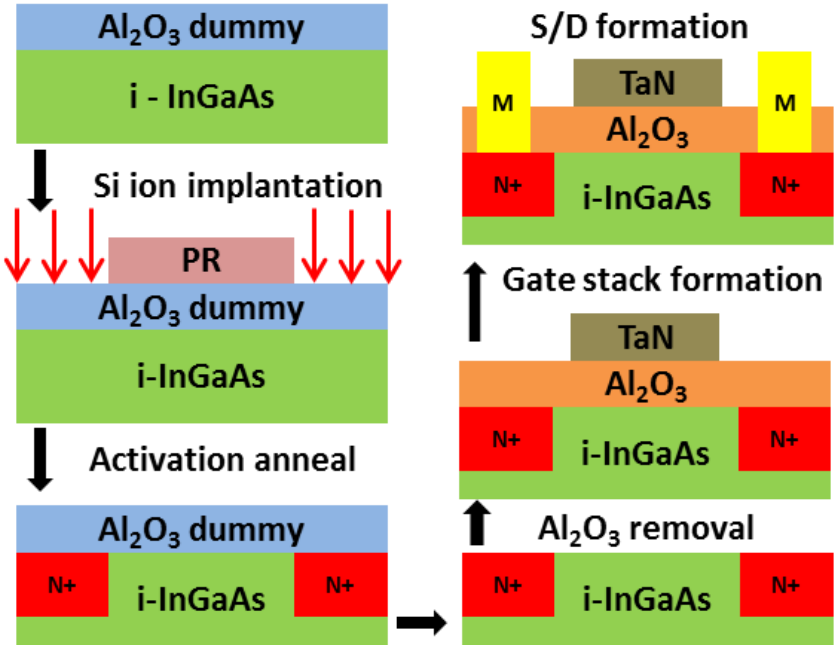


Figure 3.14: Schematic diagrams of typical gate last MOSFETs fabrication. Indium and Mo were used as S/D contact metal.

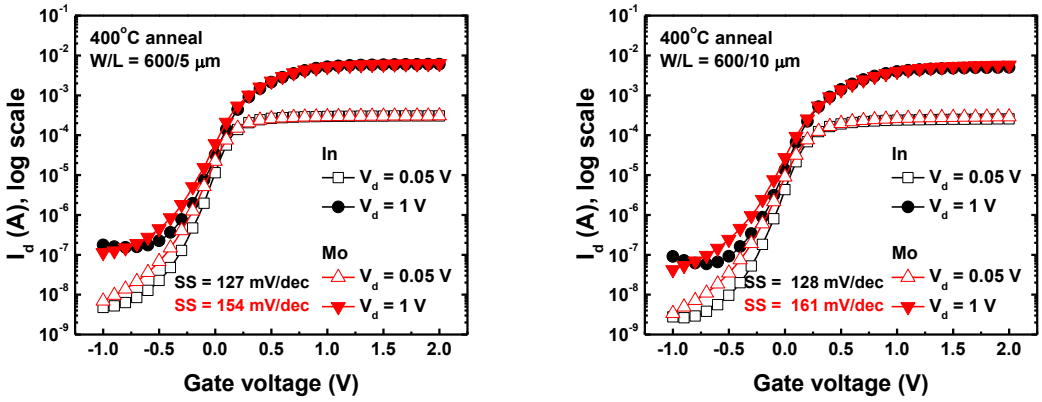


Figure 3.15: Summary of V_g vs. I_d characteristics in Gate last processed InGaAs MOSFETs with indium (30 nm) or Mo (30 nm) source/drain contacts at channel length of (a) L = 5 μm and (b) L = 10 μm.

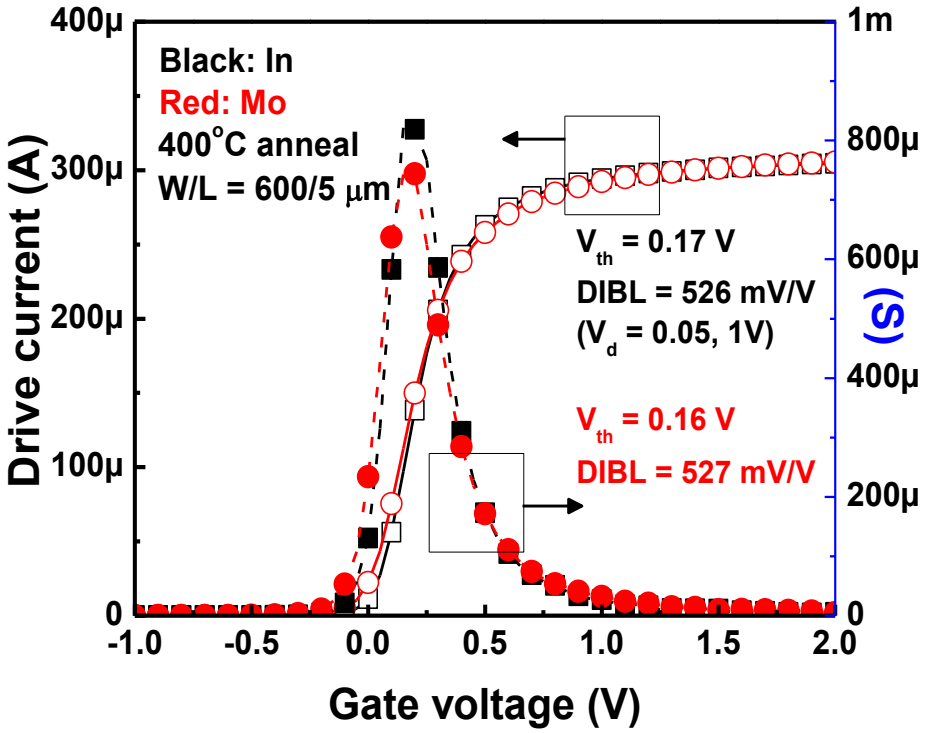


Figure 3.16: Comparison of linear scaled drive current and transconductance between In and Mo on InGaAs.

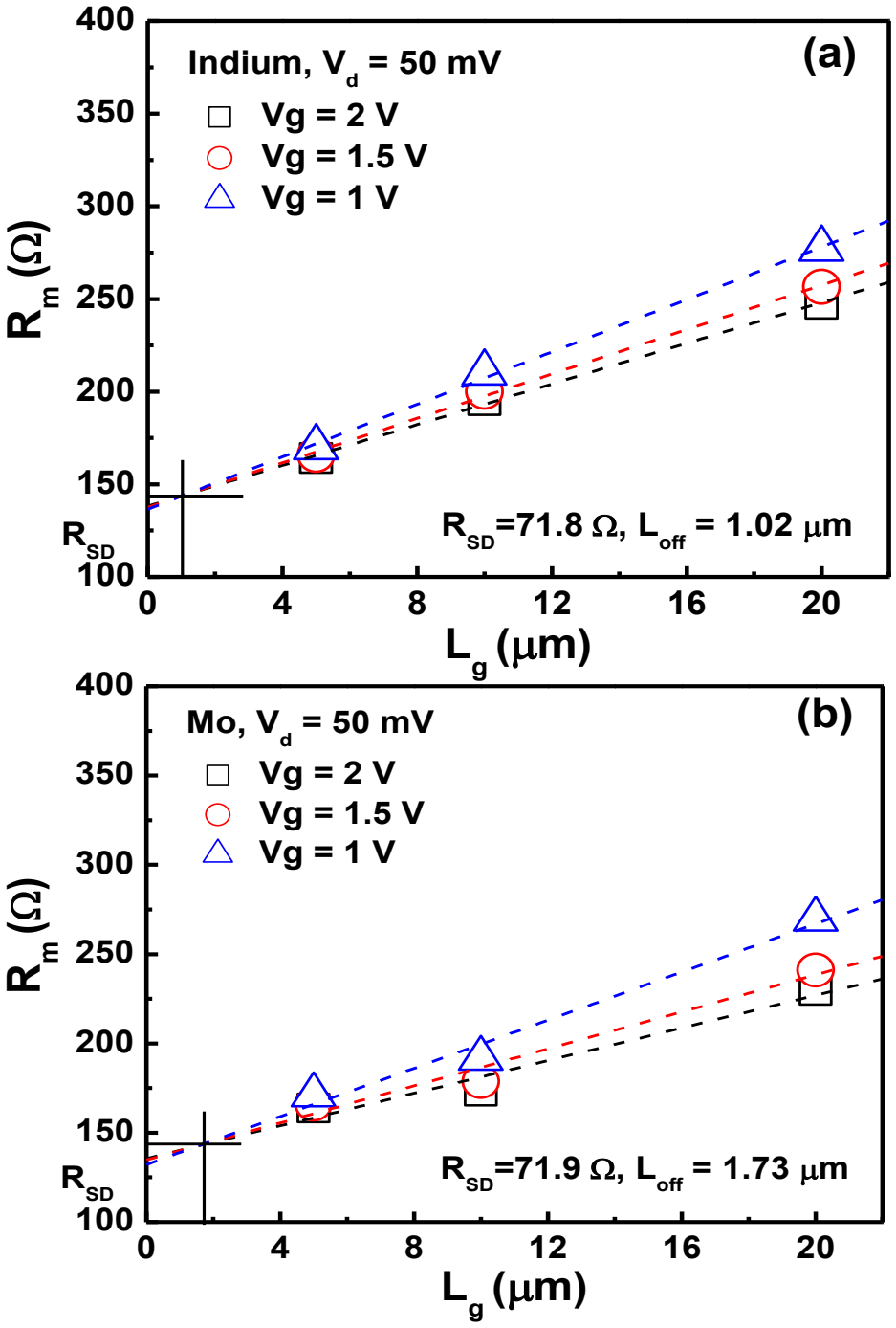


Figure 3.17: Source/drain contact resistance (R_{SD}) & channel length offset (L_{off}) comparisons between (a) indium (30 nm) and (b) Mo (30 nm) on InGaAs. R_{SD} and L_{off} were linearly extrapolated.

3.3. KERF-LESS EXFOLIATION OF GAAS

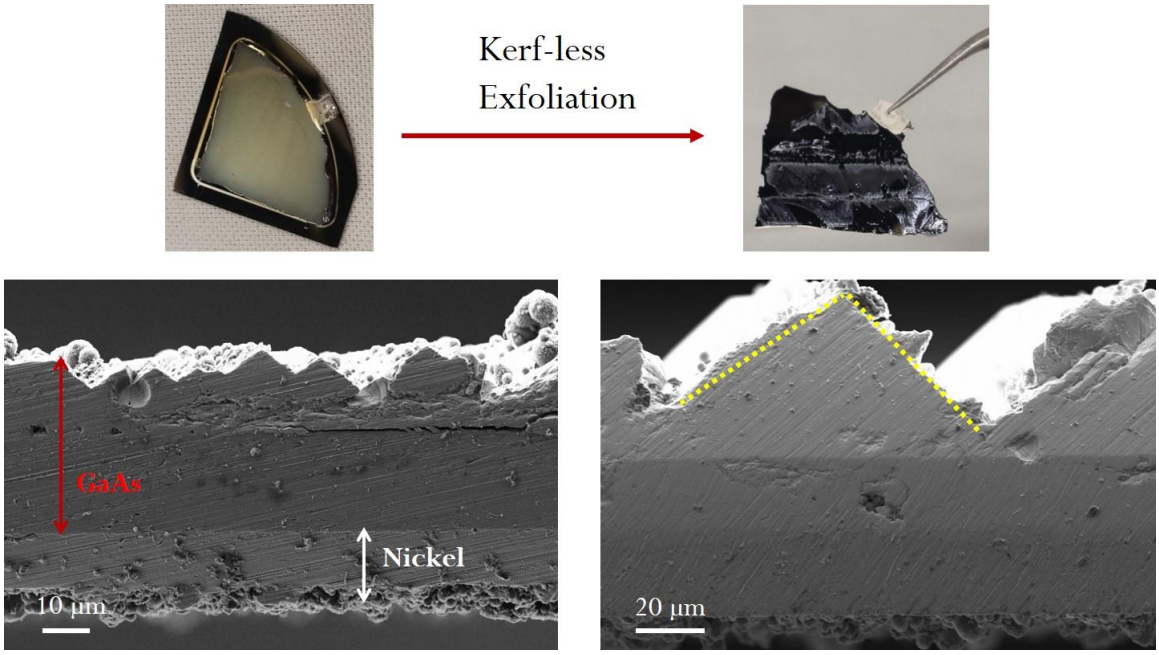


Figure 3.18: Top: Photo image of after nickel electroplating and after exfoliation of GaAs. Bottom: Cross-sectional SEM image of exfoliated GaAs.

Figure 3.18 shows the exfoliated result of GaAs sample. The exfoliation procedure is similar to the explanation in chapter 1. The nickel thickness and the thermal cycling condition were optimized to exfoliate GaAs which is an analogue of InGaAs. An interesting aspect of GaAs exfoliation is that the exfoliated surface showed a zig-zag shape regardless of the exfoliation recipe for successfully exfoliated samples. This represents that the zig zag surface is related to the material properties of GaAs. While the exfoliated surface may have limitations in applications due to it rough surface, utilizing the nickel contact side through pre-process before exfoliation followed by nickel removal can be applied for bendable electronic and photovoltaic devices. This method will be demonstrated in detail in the following chapter.

3.4. CONCLUSION

For the first time, we have studied the interface characteristics, electrical properties, and thermal stability of indium ohmic contacts on n-type $In_{0.53}GaAs$. TEM, SIMS and EDS analysis show inter-mixing at the interface and the increase of indium content after annealing, resulting in the formation of ultra-shallow In_xGaAs ($x > 0.53$) phases on $In_{0.53}GaAs$ which may contribute to the lower specific contact resistivity of indium (8×10^{-7} $\Omega \cdot cm^2$), comparable with Mo contacts (3.2×10^{-6} $\Omega \cdot cm^2$). Gate-last process MOSFET data show similar drive current, R_{sd} and lower L_{off} making indium contact a potential candidate for high performance InGaAs FET devices. Finally, kerf-less exfoliation of GaAs was successfully demonstrated.

Chapter 4. Demonstration of Bendable AlGaN/GaN 2DEG layer on silicon and HEMT fabrication

4.1. INTRODUCTION

AlGaN/GaN based III-V semiconducting heterostructures have brought great interest due to their unique properties of two-dimensional electron gas (2DEG) at the interface. At this interface, the electron movement is confined in one dimension and free from impurity scattering. This allows such III-V materials to fabricate high electron mobility transistors (HEMTs) which is suitable for applications in high-power and high-frequency electronic devices used in various fields such as wireless communications, light emitting devices (LEDs), and photodetectors.

In this chapter, kerf-less mechanical exfoliation of AlGaN/GaN 2DEG layer grown on silicon substrate is conducted. Experimental results show that the high mobility layer is maintained after exfoliation. Next, demonstrations of fabricating AlGaN/GaN HEMTs is presented. Finally, comparison of exfoliating multi-layer structures to single layer are discussed.

4.2. EXFOLIATION OF ALGAN/GAN 2DEG LAYER ON SILICON SUBSTRATE

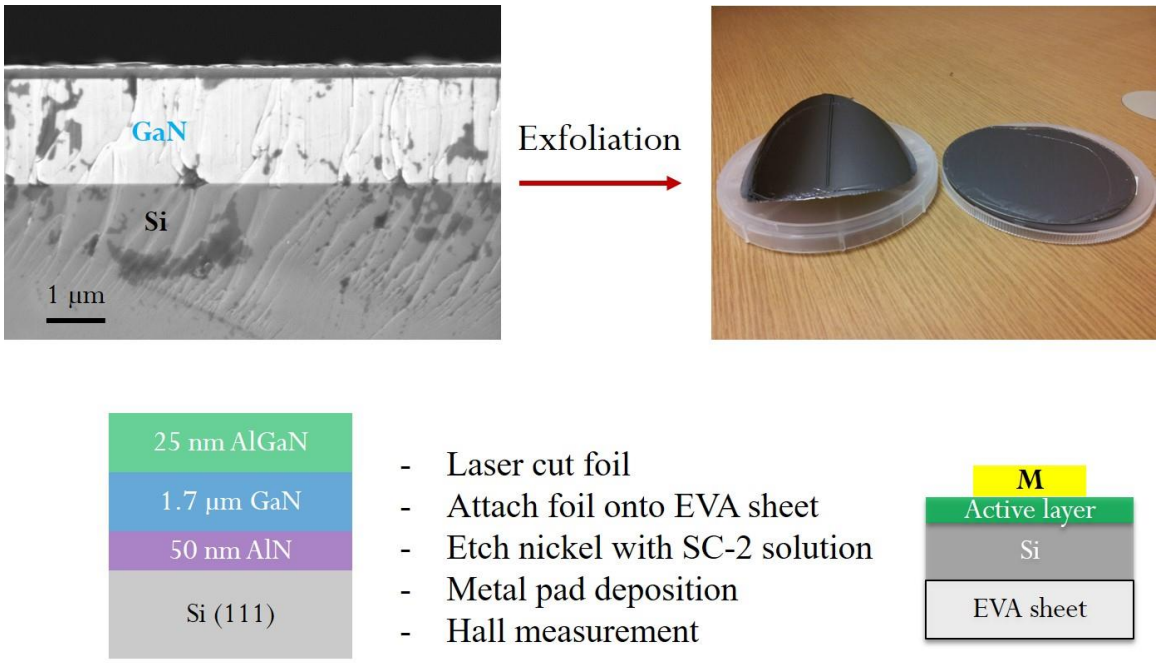
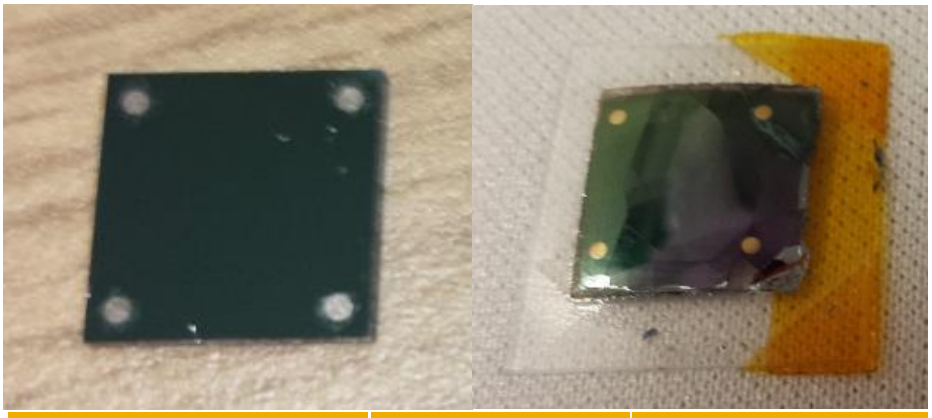


Figure 4.1. Exfoliation result of AlGaN/GaN 2DEG layer on silicon substrate and fabrication procedure of sample after exfoliation.

AlGaN/GaN 2DEG layer is grown on <111> silicon substrate. The growth starts off with growing 50 nm of AlN layer on top of silicon. This layer is referred to as the nucleation layer; this layer is to mitigate stress as well as to avoid cracking of the top AlGaN/GaN layer. [37] Next, 1.7 um of GaN and 25 nm of AlGaN is grown to create the 2DEG layer. The exfoliation process of AlGaN/GaN on silicon substrate is similar to GaAs which was explained in chapter 3.4. After exfoliation, the Ni/Ti/AlGaN/GaN/Si foil was

cut and patched to an ethylene-vinyl acetate (EVA) sheet. Detailed process after exfoliation as well as exfoliated result is shown in figure 4.1.

To check if the 2DEG layer was affected during the exfoliation process, hall measurement was conducted on both bulk and exfoliated sample.



	Bulk sample	**Exfoliated sample**
Sheet resistance (R_s,Ω/□)	469	1056
Sheet Concentration (n_s, cm^{-2})	0.98 x 10^{13}	0.97 x 10^{13}
Hall mobility (μ, $cm^2/V \cdot s$)	1353	608

Figure 4.2. Top left: Image of AlGaN/GaN on bulk silicon. Right: Image of AlGaN/GaN/c-Si on EVA sheet after exfoliation. Bottom: Hall measurement result of bulk and exfoliated 2DEG layer.

Fig 4.2 shows the bulk and exfoliated AlGaN/GaN on silicon samples and their hall measurement results. The same sheet concentration implies that the 2DEG was not affected even after exfoliation. The high sheet resistance on exfoliated samples could be due to higher contact resistance between the AlGaN and metal pad.

4.3. Demonstration of AlGaN/GaN HEMT on Silicon Substrate

4.3.1. Photomask drawing for HEMT structure

To fabricate AlGaN/GaN HEMT, a series of photomasks were first drawn using L-edit program which is shown in Fig 4.3. A number of features that were considered during drawing list as follows.

(1) Structures such as HEMT, TLM, Hall measurement, SOLT (for RF testing) were included in the photomask.

(2) Source/drain pads were drawn to accommodate both 100 & 150 um pitch probes for RF measurement.

(3) Alignment marks were drawn to accommodate MA6, MJB4, Raith & Jeol lithography tools inside cleanroom.

(4) Gate length variations of 0.3 um to 5 um were inserted to investigate gate length effect as well as to consider future potential mask use with only photolithography.

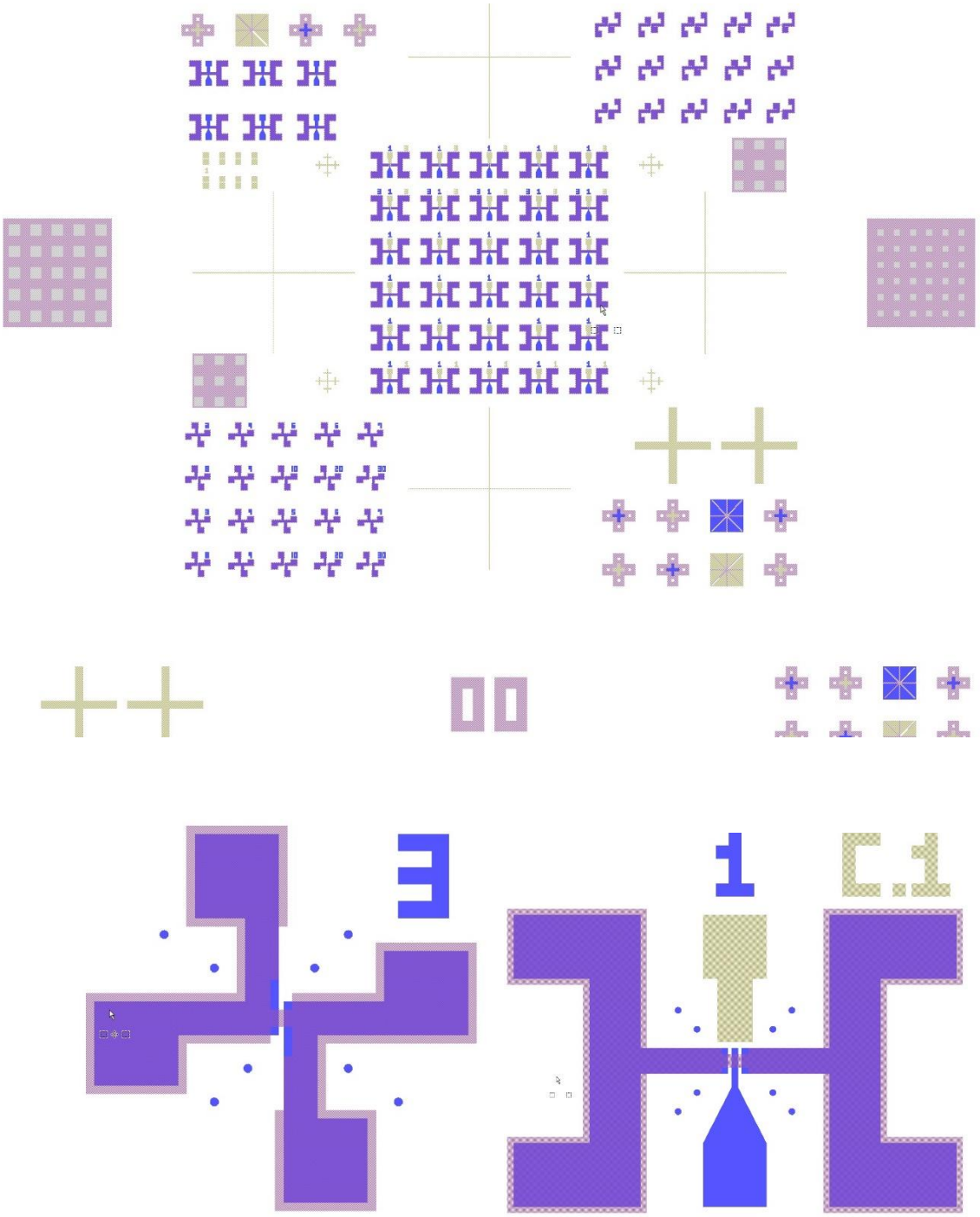


Figure 4.3. L-edit image of final mask design as well as TLM and HEMT structure.

4.3.2. AlGaN/GaN etch and channel definition

To fabricate AlGaN/GaN HEMT, we start off by defining the 2DEG channel layer. This process requires lithography and etch of AlGaN/GaN layer. After cleaning the AlGaN surface with acetone and IPA, a thin layer of SiO_2 (PECVD, 27 nm) is deposited. This SiO_2 layer serves as a barrier so that the AlGaN surface does not come in direct contact with the photoresist as well as a barrier for nickel etchant. Next, photolithography of channel pattern followed by nickel deposition (200 nm, e-beam evaporation) and lift-off (overnight in acetone) is conducted. Before etching AlGaN/GaN, the sample is dipped in BOE for 20 secs to remove the SiO_2 layer. AlGaN/GaN layer is etched using the Oxford ICP. The ICP etch recipe for GaN is 2 sccm of BCl_3, 20 sccm of Cl_2, 20 ˚C tested at 50 W & 100 W respectively.

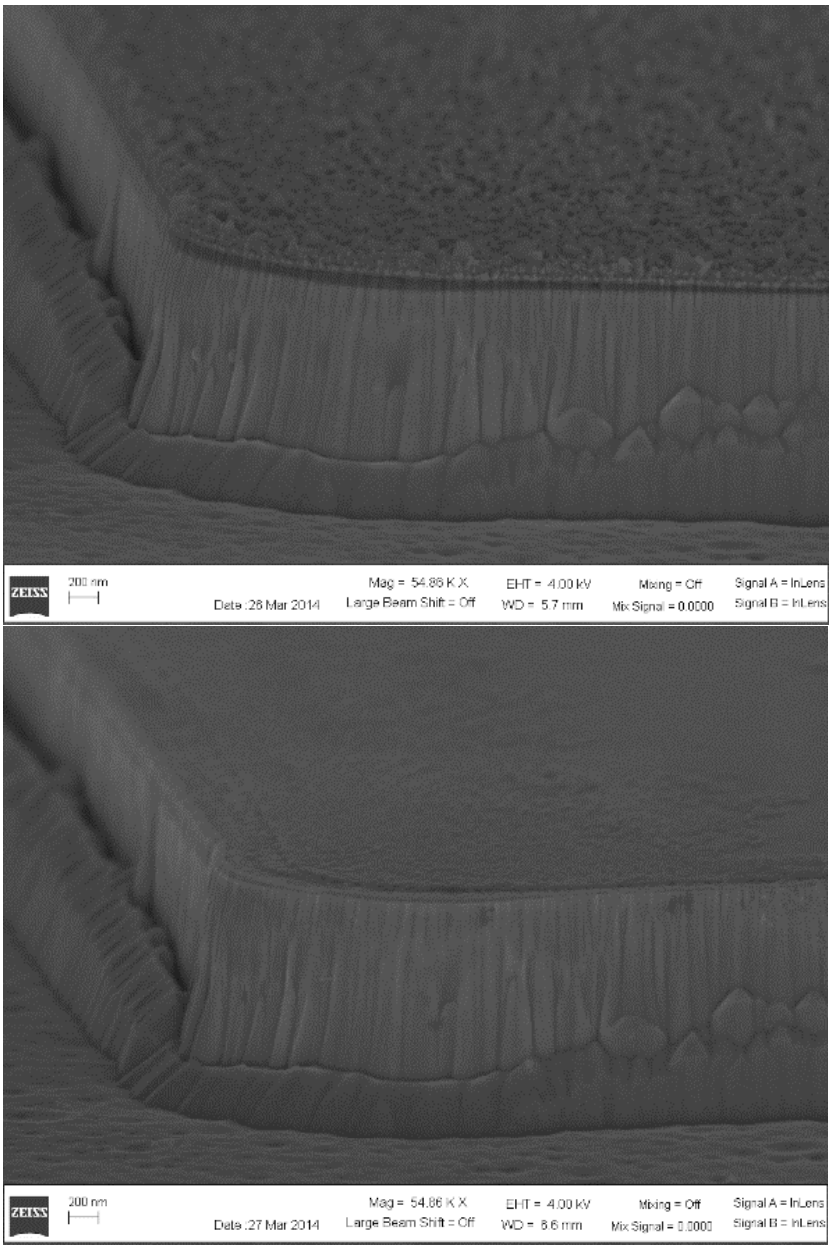


Figure 4.4. Top: Cross sectional SEM image of AlGaN/GaN on silicon substrate after 9 min etch at 100 W. Bottom: Cross sectional SEM image of AlGaN/GaN on silicon substrate after nickel mask removal. AlGaN surface is smooth after nickel etch

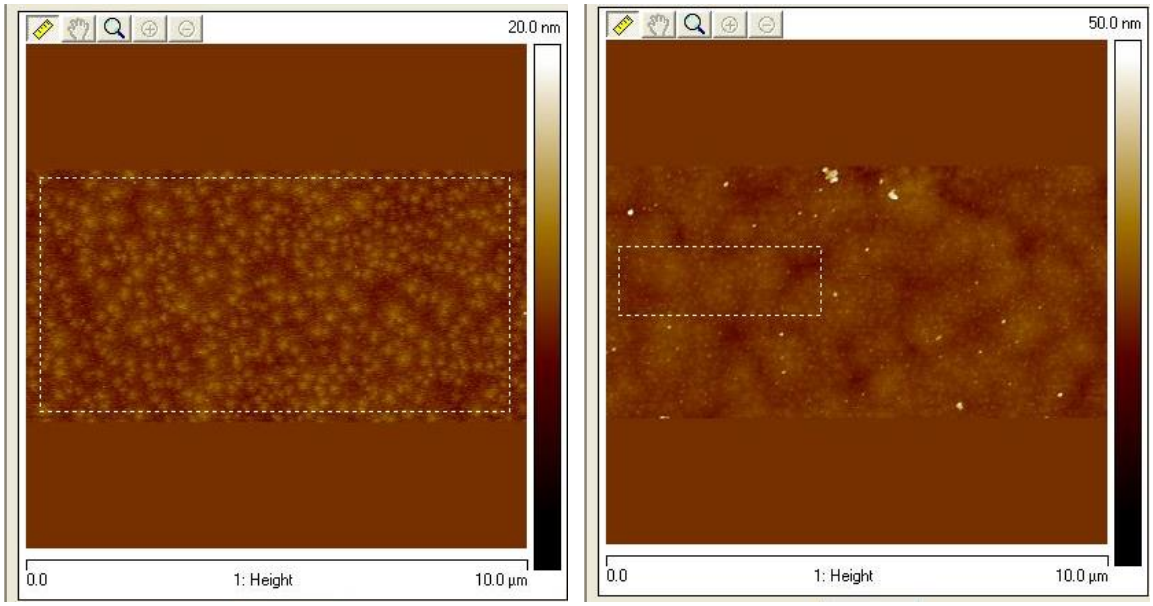


Figure 4.5. AFM scan of bare AlGaN/GaN before(left) process (average roughness= 0.8 nm) after (right) ICP etch and nickel mask removal (average roughness = 1.3 nm)

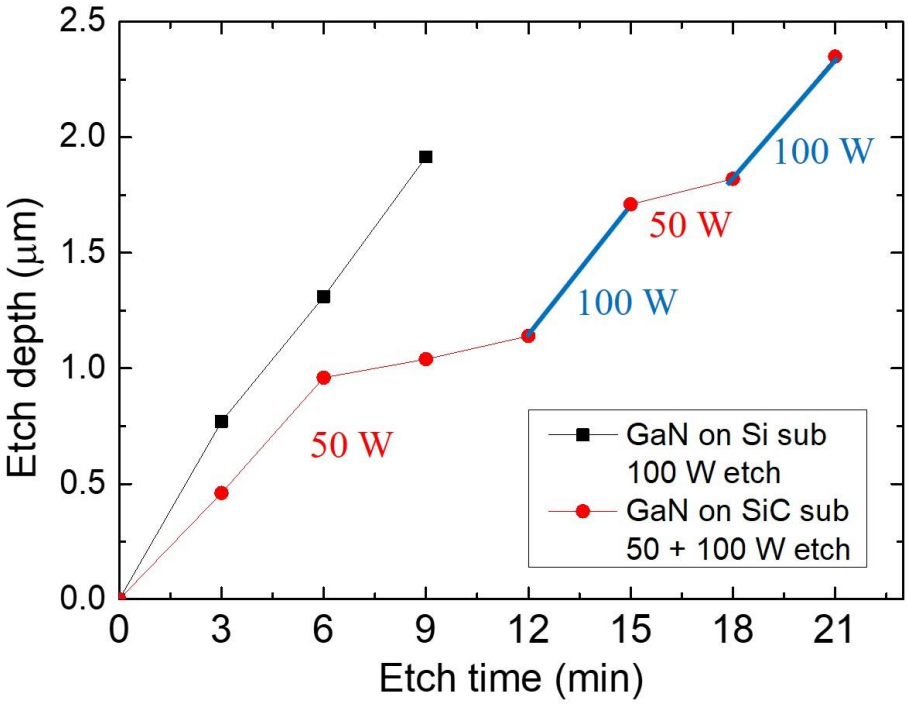


Figure 4.6. Etch rate of GaN on Si and SiC using ICP etch.

GaN etch rate was defined by measuring the etched thickness using the profilometer. Fig 4.6 shows the etch rate of GaN for 50 W and 100 W conditions. Since the thickness of GaN is 1.7 um, 9 min etch at 100 W was enough to fully etch GaN and thus prevent any parasitic current path. After etching, nickel is removed by dipping sample in nickel etchant followed by BOE to remove SiO_2. Fig 4.4 and 4.5 shows the cross-sectional SEM image of etched AlGaN/GaN layer before and after nickel removal as well as the AlGaN surface roughness measured by AFM.

4.3.3. Specific Contact Resistivity of AlGaN/GaN layer

To fabricate AlGaN/GaN HEMT, achieving high quality ohmic contact, at the source and drain region is required. To achieve such low resistance, Ti/Al metallization method is generally performed. [38-40] This method involves depositing Ti/Al on AlGaN surface followed by high temperature annealing, which results in an alloy form of Ti/Al and AlGaN/GaN showing low resistance. To minimize the oxidation of Al during the annealing step, metals such as Ni, Ti, Pt and Mo are overlaid on top of Ti/Al. [41-47]. To measure the contact resistivity of etched AlGaN/GaN layer, a TLM structure is fabricated by defining contacts with different channel length. Photolithography followed by metal lift-off of with Ti/Al/Ni/Au = 20/100/40/100 nm was conducted. To achieve ohmic contact, TLM sample was annealed in a rapid thermal annealing (RTA) system starting from 800 ˚C for 60 secs in N_2 ambient. Fig. 4.7 plots the specific contact resistivity values after annealing at different temperatures and time. Results show that ohmic contact is achieved after annealing at 900 ˚C. To further reduce the contact resistance for high quality HEMT, extracting the specific contact resistivity at higher temperatures were conducted. Fig 4.7 shows the specific contact resistivity of AlGaN/GaN layer on both silicon and silicon carbide after annealing beyond 900 ˚C. Both samples showed resistivity decrease over a magnitude when annealing time and temperature was increased and reached as low as $8x10^{-6}$ ohm·cm^2.

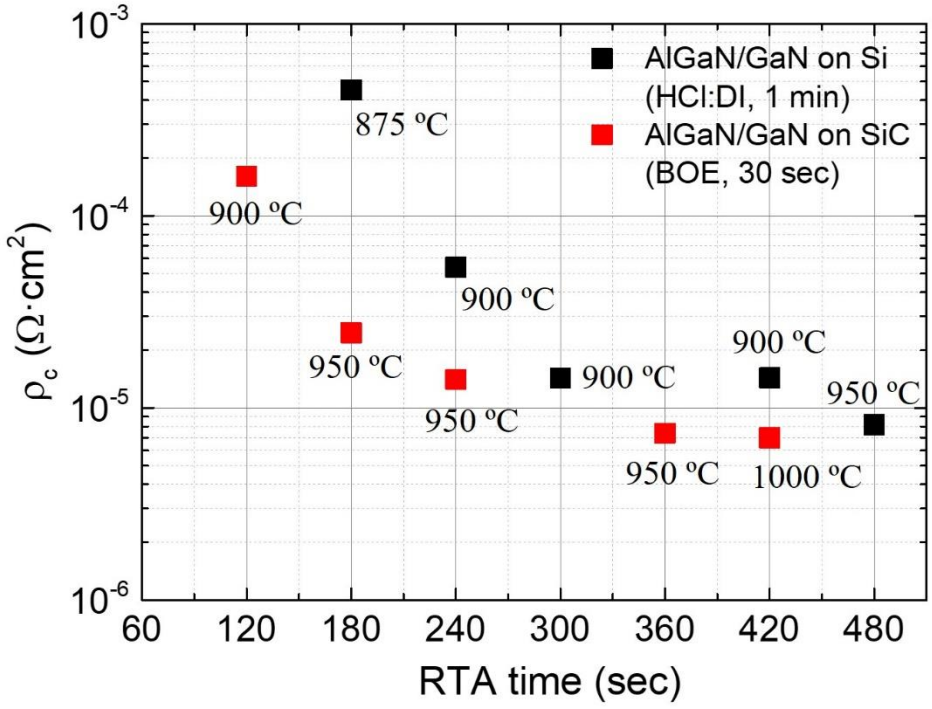


Figure 4.7. Specific contact resistivity of AlGaN/GaN layer for different temperature and time by RTA.

4.3.4. I-V Characteristics of AlGaN/GaN HEMT

After channel definition and ohmic contact of formation, the gate pattern was defined using photolithography and e-beam lithography for gate lengths smaller than 3 μm. Gate metal of Ni/Au= 50/100 nm was deposited using e-beam evaporator and lift-off using Remover PG for e-beam lithography. Fig 4.8 shows the final device with its I-V characteristic results.

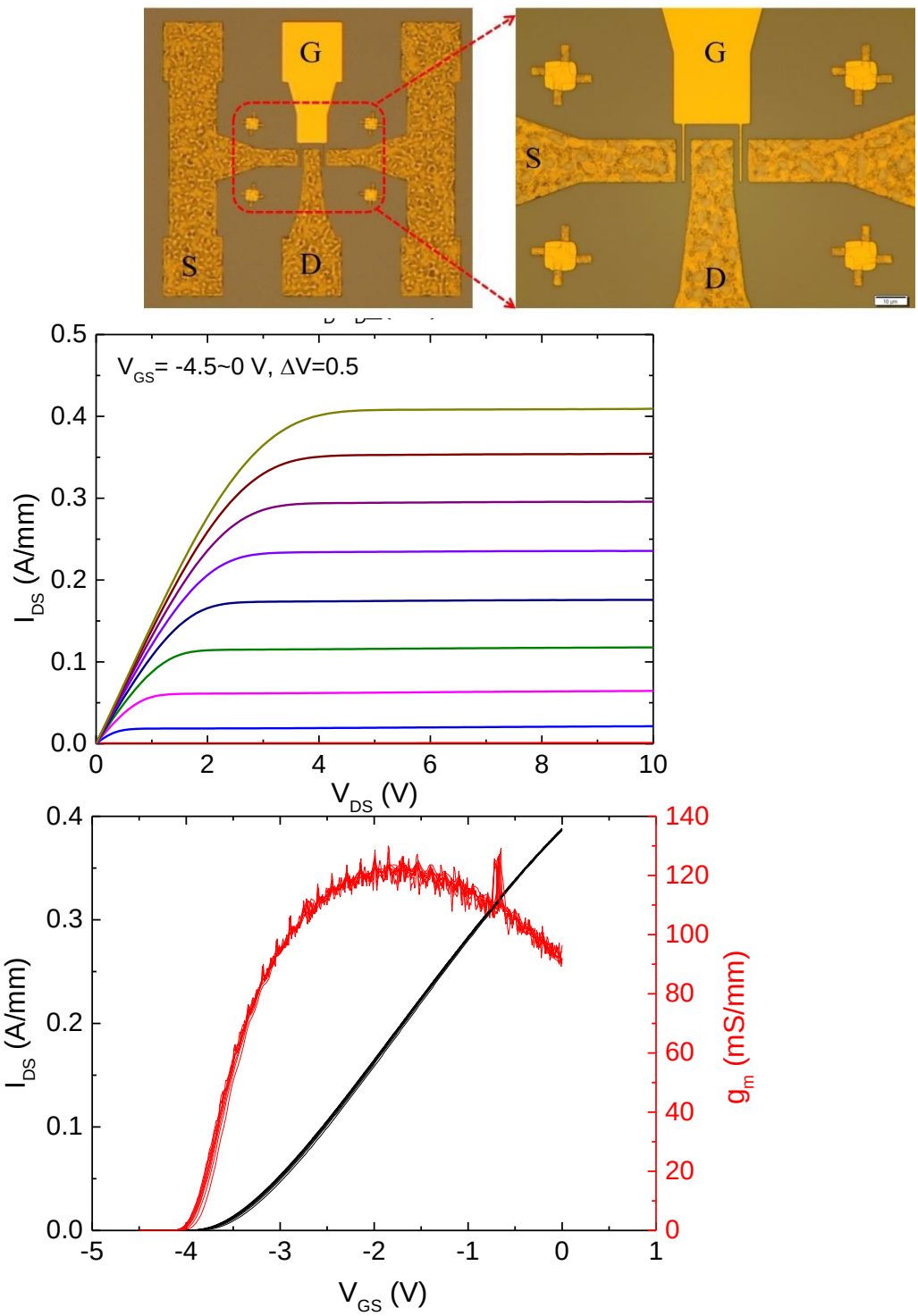


Figure 4.8. Optical image of AlGaN/GaN HEMT. V_{DS}-I_{DS} and V_{GS}-I_{DS}/gm measurement result.

AlGaN/GaN HEMT shows the following measurement parameters;

- Pinch-off Voltage= -4 V
- Maximum current density= 409 mA/mm at V_{GS}= 9.5 V (Saturates after V_{GS}= 5 V)
- On-resistance= ~500 Ω·mm (V_{GS}= 0V)
- On-off ratio ~ 10^7
- Peak extrinsic g_m= 122 mS/mm at V_{GS} = -1.65V

4.4. Kerf-less exfoliation of non-planar, multi-layer architecture

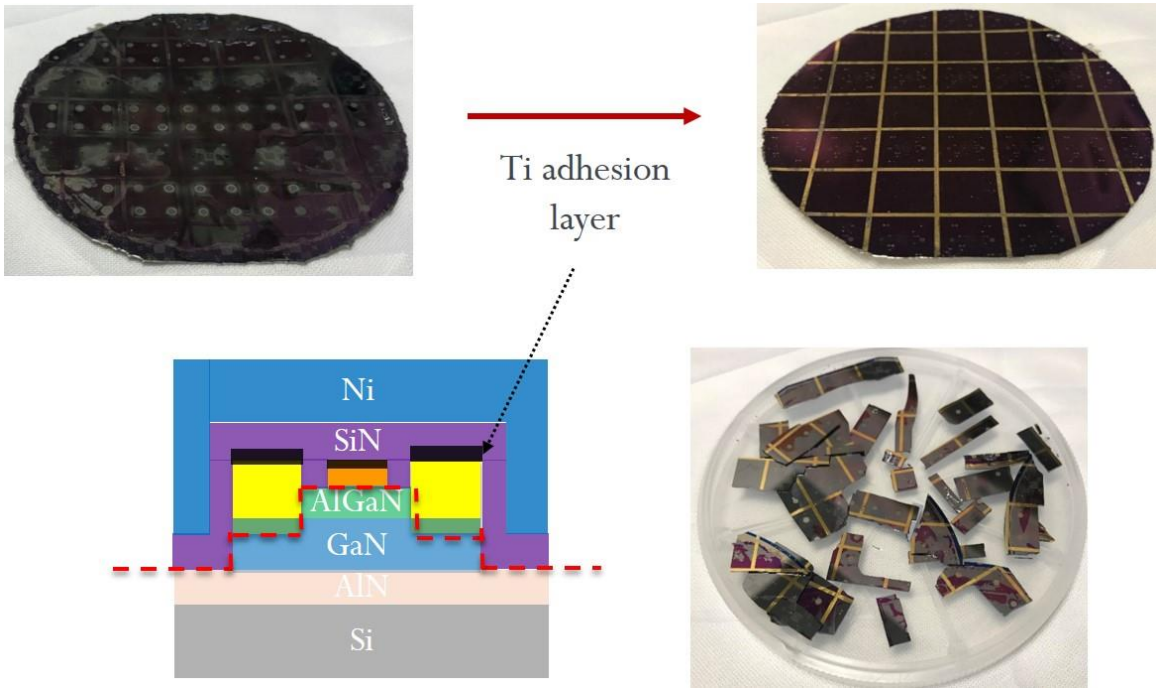


Figure 4.9. Top: Optical image of exfoliated AlGaN/GaN HEMT with and without additional Ti adhesion layer. Bottom left: Schematic of final structure before exfoliation. Dotted line represents exfoliated path. Bottom right: Parent silicon wafer after exfoliation.

Once the demonstration of AlGaN/GaN HEMT on bulk silicon was successful, exfoliation of the electronic devices was conducted. After fabricating the HEMT structures on silicon substrate, Si_3N_4 was deposited using PECVD followed by Ti/Ni seed layer. The Si_3N_4 layer is needed to protect the HEMT from subsequent nickel etchant after exfoliation. Fig 4.9 shows the exfoliation result of AlGaN/GaN HEMT devices on silicon substrate. Unlike the planar structure case, the exfoliation mainly occurred between the Si_3N_4 and electroplated Ni interface. This can be explained by the adhesion difference between each interface. When a Ti adhesion layer was inserted between the HEMT metal contacts and the Si_3N_4 layer, the exfoliation occurred between the HEMT metal contacts and the AlGaN interface which is illustrated as the dotted line in figure 4.9.

While exfoliation of HEMT structure on silicon was conducted at various conditions including change in electroplated nickel thickness, thermal cycling condition and initial cracking, the exfoliation did not occur within the silicon substrate.

Another difference between the planar structure in chapter 4.2 is that the bulk, parent wafer cracks into small pieces shown in figure 4.9. (bottom right image) This did not occur for the planar architecture samples which implies that the thermally induced stress distribution for the multi-layer structure is different and complex.

Chapter 5. Graphene-Al_2O_3-Silicon Heterojunction Solar Cells on Flexible Silicon Substrates *

5.1. INTRODUCTION

Two-dimensional materials have been studied extensively since the seminal work with graphene in 2004 [48-51]. The appeal of this class of materials arises from their unique electronic, optical, and physical properties. For example, graphene has remarkable mechanical properties and flexibility [52], it is optically transparent (absorbing less than 3% of incident light per layer) [53], and it is highly conductive electrically and thermally [54]. One application for graphene which has garnered early attention is its use as a transparent conducting film [55-56]. For many applications, the current market standard transparent conductor is indium tin oxide (ITO) and graphene can provide unique advantages over ITO, namely mechanical flexibility, and lower cost with earth abundant materials [57]. As a transparent conductor, graphene can advance energy generation in solar cell applications. To this end, graphene has been used to form a heterojunction with semiconductors such as silicon and GaAs, resulting in graphene semiconductor-Schottky barrier solar cells (GS-SBSC) [58-59]. While early work gave efficiencies of less than 2 % in power conversion efficiency (PCE), researchers have boosted the efficiencies of these GS-SBSC up to 15.6 % by various techniques such as graphene doping, insertion of a thin insulator between the graphene and silicon, anti-reflective coating, and semiconductor and backside passivation [60-65].

* This chapter is based on Reference : J. Ahn, H. Chou, and S.K. Banerjee Graphene-Al_2O_3-Silicon Heterojunction Solar Cells on Flexible Silicon Substrates *Journal of Applied Physics,* **2017**, *121*, 163105. J.A. and H.C. contributed equally to this work.

Thin solar cells possess the advantage of reducing the material cost as well as potentially increasing the PCE [66]. Additionally, thin solar cells can be made flexible, which opens a whole new range of applications such as wearable devices [67-68]. Utilizing the inherent flexibility of graphene, GS-SBSC fabricated on thinned Si body have been demonstrated with efficiencies up to 8.4% [69-70]. These flexible GS-SBSC are fabricated on bendable silicon films which are produced by wet etching a bulk Si wafer.

In this chapter, we demonstrate GS-SBSC on bendable, thin silicon foils obtained by a kerf-less mechanical exfoliation technique. The exfoliation process does not require the strong etchants of the other processes and the "parent" wafer can be subsequently used to generate additional thin silicon films, and both aspects bolster the effort of reducing material cost. We also study the effects of an Al_2O_3 interlayer between the exfoliated silicon and doped graphene, giving a graphene-insulator-silicon (GIS) solar cell. This thin insulator layer, deposited by atomic layer deposition (ALD), increases the overall performance of the device by preventing recombination and increasing charge carrier lifetime.

5.2. EXPERIMENTAL

5.2.1. Growing, doping, and transfer of multilayer graphene

Multi-layer graphene (MLG) was grown by chemical vapor deposition (CVD) on Cu-Ni alloy foils in a low-pressure system. A single layer of graphene can be grown in a self-limiting process on pure copper due to the low solubility of carbon in copper [71-72]. Although other reports have shown high performance using single layer graphene (SLG), it has also been shown that MLG enhances the solar cell performance. [64, 73-74]

Therefore, in thes devices, we incorporate MLG. By growing on a Cu-Ni alloy instead, the solubility of carbon is increased and MLG can be formed by precipitating carbon out (in the form of graphene) during cooling, as has been shown previously [75-76]. The dissolution and precipitation process is shown schematically in Figure 5.1 (a). Methane was flowed at 3 sccm and carried by hydrogen gas flowed at 10 sccm to the foil substrate at held at 1050° C. After the high temperature growth, the chamber was cooled also under 3 sccm flow of methane and 10 sccm flow of hydrogen. After growth and graphene transfer as described below, the MLG film is characterized by confocal Raman spectroscopy (Renishaw inVia, 532 nm wavelength laser) and atomic force microscopy (AFM), which is shown in Figure 4.1 (b) and (c). The Raman characterization gives a spectrum consistent for MLG and a narrow distribution for the G band position [77-78]. The AFM scan at the edge of a MLG film shows a step height of ~ 10 nm, which corresponds to 27 – 29 layers of graphene. After synthesis, the MLG is charge-transfer doped p-type by spin coating a 10mM solution of $AuCl_3$ in nitromethane at 2000rpm for 1 minute [79-80]. The doping effect is verified by measuring the sheet resistance and optical transmission, as shown in Figure 4 (d). The $AuCl_3$ dopant does adversely impact the transmission of the MLG layer, and there is a trade-off between loss in transmission due to more graphene layers and doping, and a boost in conductivity. After the doping process, the CVD graphene is transferred using a PMMA-assisted wet etching method [81].

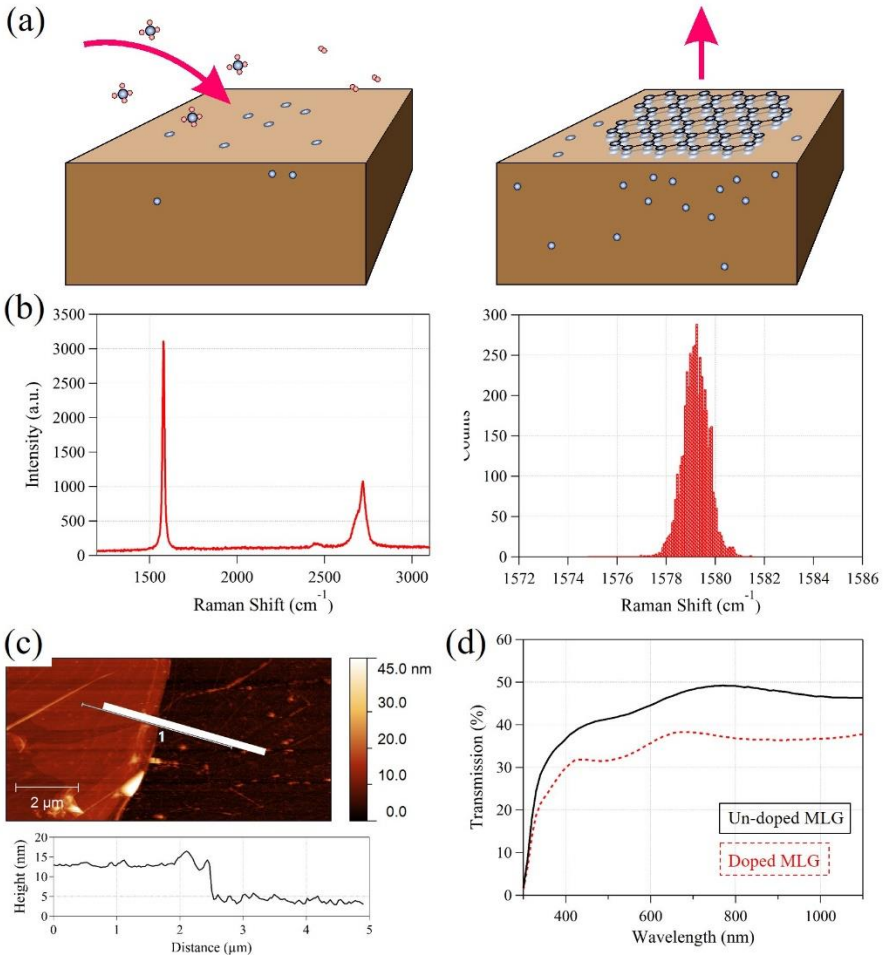


Figure 5.1: (a) Illustration of graphene growth. Methane decomposes on the catalytic surface of the Cu-Ni alloy and carbon dissolves into the substrate at high temperature. On slow cooling, the carbon precipitates out of the Cu-Ni alloy in the form of MLG. (b) Raman spectrum of MLG after transfer onto SiO_2/Si substrate showing a highly crystalline film and a histogram of the G peak position over a scanned area of 40 x 30 µm MLG showing that the film is uniform in quality. (c) AFM scan of the edge of a transferred MLG showing the thickness to be ~ 10 nm. (d) Transmission of un-doped and pre-doped MLG over a broad light spectrum.

A PMMA film is spin coated onto the graphene at 2000rpm and baked for 1 min. at 90° C. The PMMA-graphene stack is floated on 0.5 M ammonia persulfate solution to etch away the Cu-Ni alloy substrate. The PMMA-graphene is then rinsed in deionized water to remove any etchant or byproducts from the Cu-Ni removal process. The PMMA-graphene is lifted from the water directly by the target substrate, the silicon foil. The doping was done prior to the for reasons discussed below.

As we show below, the tradeoff favors utilizing MLG (as opposed to single layer graphene, SLG) and doping it. Doping the graphene (with $AuCl_3$) reduces the graphene sheet resistance which is measured by van der Pauw method. Un-doped and pre-doped MLG were transferred onto SiO_2/Si bulk substrate followed by metal contact formation using silver paste for measurement. Sheet resistances of 448 and 11 Ω/□ were obtained for un-doped and doped MLG, respectively, with an encapsulating layer of PMMA on top.

5.2.2. Fabrication of thin silicon films with metal backing

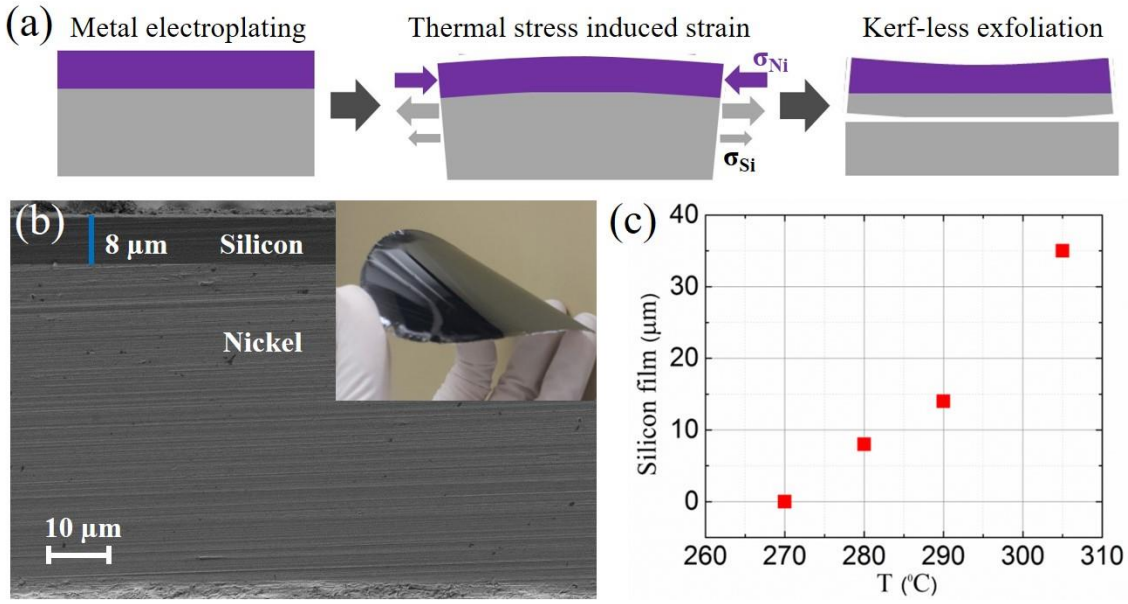


Figure 5.2: (a) Schematic of silicon exfoliation process by deposition of metal layer, thermal cycling, and exfoliation. (b) Scanning electron microscope (SEM) cross-section image of a thin exfoliated silicon layer. Inset: Photographic image of an exfoliated 4-inch Si wafer. (c) Experimental result of silicon film thickness relationship with thermal cycling temperature

Figure 5.2 illustrates the kerf-less exfoliation process based on spalling and resulting exfoliated silicon film on metal foil. Bulk silicon wafers (n-type, <100>, 1 ~ 5 Ω·cm) were covered with a dual-layer of hydrogenated amorphous silicon (α-Si:H) using remote plasma chemical vapor deposition (RPCVD). 5 nm, intrinsic α-Si:H was deposited on the front side to passivate the surface, and 7 nm, n^+ doped α-Si:H was deposited on the back side to achieve ohmic contact with backside metal [82]. Chromium (10 nm) and Nickel (100 nm) were sequentially deposited onto the back surface by electron beam evaporation as a seed layer for electroplating 50 ~ 55 µm of Ni onto the

metal seed layer with current density fixed to 30 A/cm^2. At this step, the backside of the GS-SBSC device was complete and the kerf-less exfoliation process was done [83-84]. Exfoliation was initiated with a crack at the edge of the wafer after the thermal annealing process and followed by controlled spalling. The exfoliated silicon thickness was controlled by the thermal cycling process (270 °C ~ 310 °C, 10 min.) which thermally induced stress at the metal/silicon interface due to the difference in coefficient of thermal expansion (CTE) in the different materials. Silicon thicknesses down to 8 μm can be successfully exfoliated with surface RMS roughness less than 2 nm. Other parameters such as metal thickness, annealing time, current density during electroplating and mechanical exfoliation condition can further control the silicon thickness [85]. Solar cells fabricated by this method reduce the material cost through re-use of the parent wafer for subsequent exfoliation. This method is also beneficial with respect to handling issues and preventing cracks in thin silicon films because of the mechanical support provided by the electroplated Ni layer.

5.2.3. Graphene-silicon (and graphene-insulator-silicon) SBSC fabrication

The exfoliated silicon film with Ni metal backing foil was first sonicated in acetone and iso-propyl alcohol (IPA), followed by RCA clean. An SC-1 clean removes silicon particles from the exfoliation process. Silicon films with thicknesses of 35 μm were used to maximize absorption, while maintaining the flexibility of the film. Immediately before any subsequent process, the native oxide was removed from the silicon surface in diluted HF. In the case where an interlayer oxide was inserted (GIS cells), Al_2O_3 was deposited by atomic layer deposition in a Cambridge nanotech Fiji F200 ALD system, using tri-methyl aluminum (TMA) and water precursors at 200 ˚C. To

fabricate the GS-SBSC device (or GIS cell), MLG was transferred using the method described above onto the silicon surface (without an intervening Al_2O_3 layer) and then allowed to dry in ambient. The sample was then heated up to 110 ˚C for 10 min. to improve graphene/substrate adhesion. To further aid adhesion and remove wrinkles in the MLG, an additional application of PMMA was made on top of the PMMA-graphene [86-87]. The PMMA was spin coated at 3000rpm for 1 min. and then baked at 90 °C for 1 min. It has been previously reported that removing the PMMA after graphene transfer can degrade the graphene quality [69]. To effectively dope the graphene while retaining the graphene quality, the graphene is pre-doped prior to PMMA coating.

Silver paste was directly applied onto the PMMA/$AuCl_3$/graphene to form top contact of the graphene. Acetone solvent within the silver paste dissolved the PMMA allowing direct contact between silver paste and graphene. All remaining areas were covered with black tape to ensure precise measurements. The active area of the solar cells is 0.17 ~ 0.37 cm^2. Figure 5.3 illustrates the GS-/GIS- SBSC device fabrication and includes a photograph of a completed GIS cell.

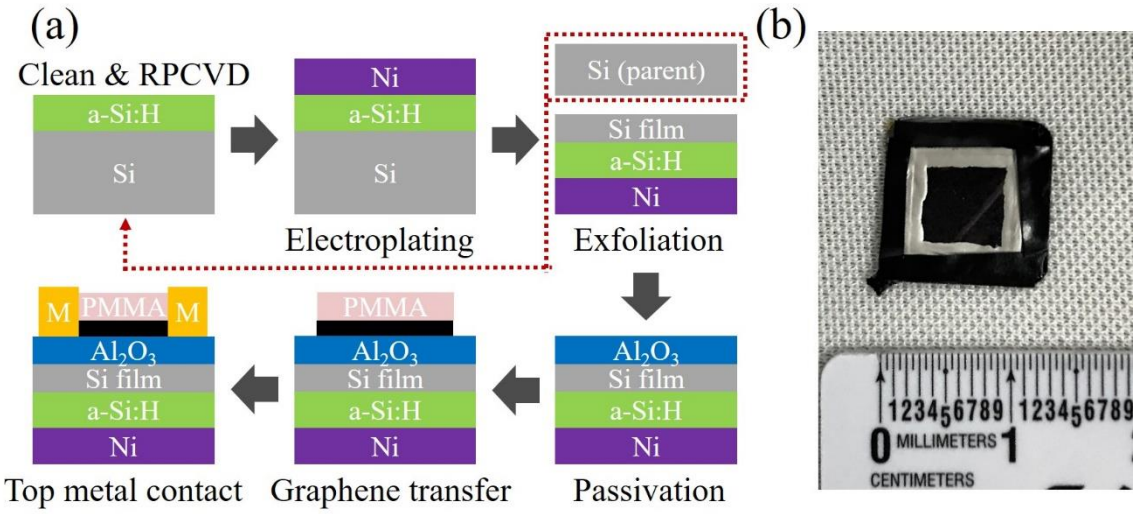


Figure 5.3: (a) Schematic of GIS Solar cell fabrication process. For GS-SBSC, all is identical except excluding Al_2O_3 layer deposition process. (b) Photographic image of a completed GIS solar cell.

5.3. Results and discussion

5.3.1. GS-SBSC.

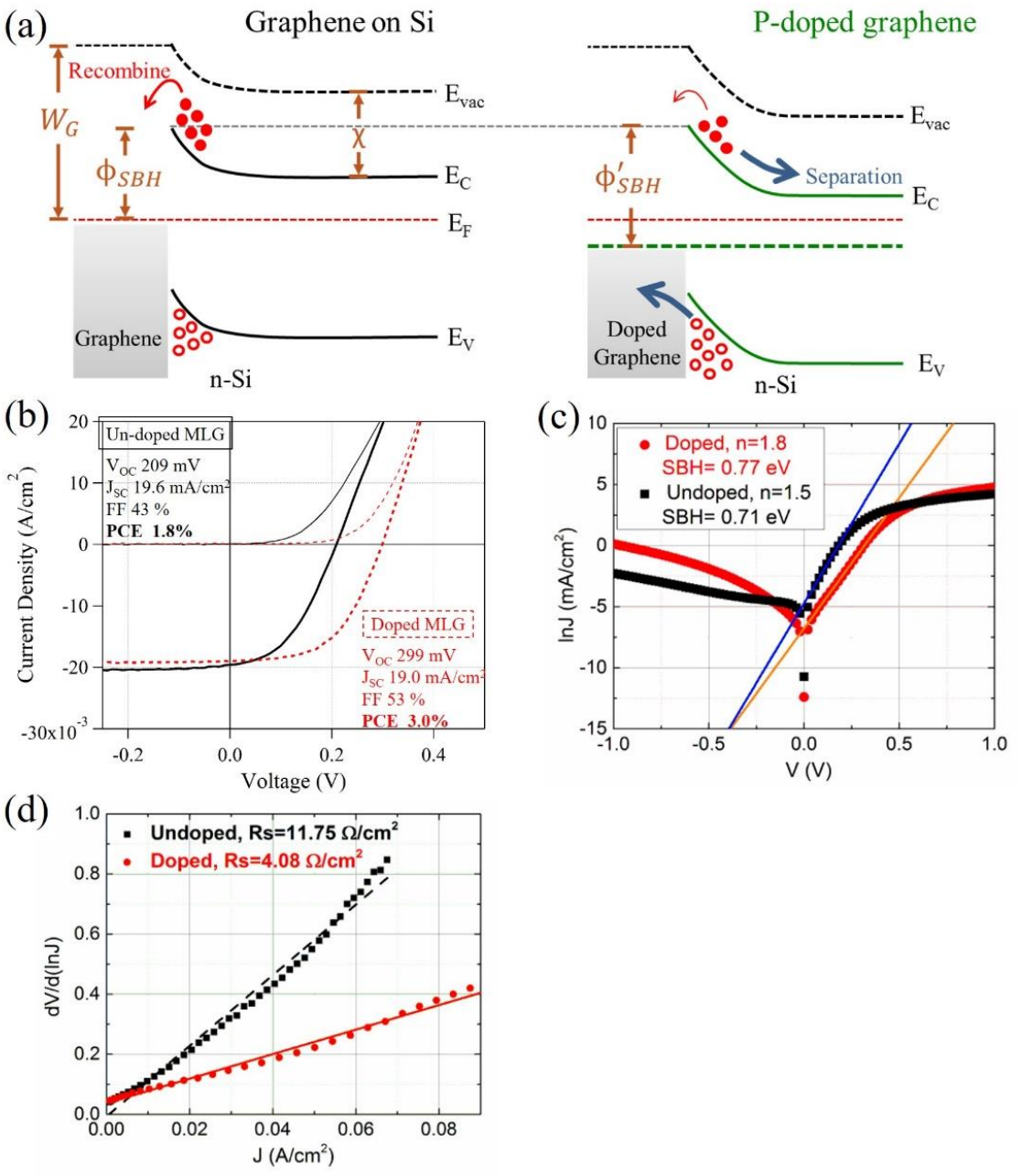


Figure 5.4: (a) Qualitative energy band diagram of GS-SBSC with and without $AuCl_3$ doping. P-doped MLG creates a shift in potential resulting

in improved cell performance. (b) J-V plot of un-doped MLG and pre-doped MLG with no interlayer oxide layer. (c) lnJ-V plot measured in dark with linear fit (solid lines) of the forward current for ideality factor and SBH extraction. (d) dV/d(lnJ)-J plot for series resistance (R_S) extraction.

Figure 5.4 (b) shows the current density-voltage (J-V) characteristics of un-doped and pre-doped heterojunction GS-SBSC on thin exfoliated silicon films. GS-SBSC were measured using an ABET solar simulator (Model: Sun 2000) and were calibrated using a reference solar cell (ABET model #15150) prior to measurement. Results show that doping the graphene increases open circuit voltage (V_{OC}) from 209 to 299 mV, fill factor (FF) from 43 to 53 % and improving the PCE from 1.8 to 3.0 %. The increase in performance after doping can be explained by analyzing the GS-SBSC dark I-V graph and band diagram. Figure 5.4 (a) illustrates the band diagram for un-doped and p-type doped graphene on n-type silicon. According to the Schottky-Mott rule of Schottky barrier formation, the Schottky barrier height (SBH, ϕ_{SBH}) between MLG and thin silicon film is described based on the work function of the MLG (W_G) and the electron affinity of the silicon (χ), $\phi_{SBH} \sim W_G - \chi$. Doping the MLG with $AuCl_3$ is known to shift the MLG work function (ϕ'_{SBH}) [56] and can be extracted from the equation

$$J_s = A^* T^2 \exp\left(\frac{-\phi_{SBH}}{kT}\right) \quad (1)$$

where J_S is the saturation current extrapolated at V = 0 from the linear portion of the forward current (solid lines in figure 2.4 (c), un-doped J_S = 8.9 μA/cm^2, doped J_S = 1.14 μA/cm^2), A* is the Richardson constant (~ 112 A/cm^2·K^2 for n-Si), *T* is the absolute

temperature, q is the electron charge and k is the Boltzmann constant. The SBH for un-doped and doped GS-SBSC was found to be 0.71 and 0.77 eV, respectively.

The change in saturation current results in a change of V_{OC} given by the following relation,

$$V_{oc} = \frac{nkT}{q} \ln\left(\frac{J_{ph}}{J_s}\right) \tag{2}$$

where n is the ideality factor of the graphene/silicon interface, and J_{ph} is the light-induced photocurrent density of the solar cell [88]. The ideality factor can be extracted by fitting the device response in the dark, giving n of 1.5 and 1.8, respectively, and shown in Figure 5.4 (c). Following the above equation, an increase in n and decrease in J_S leads to an increase in V_{OC} for doped MLG solar cells. The drop in short circuit current (J_{SC}) can be explained due to the decrease in transmitted photons after doping. There is a loss in transmission through the MLG due to $AuCl_3$ charge-transfer doping, which results in a decrease of light reaching the silicon absorber as shown in Figure 5.1 (d).

The increase in FF is due to the reduction in series resistance (R_S) after graphene doping. The R_S for un-doped and doped GS-SBSC are extracted using the slope of the dV/d(lnJ) plot, which is shown in Figure 5.4 (d). The R_S is shown to decrease from 11.75 to 4.08 $\Omega \cdot cm^2$ for doped GS-SBSC cells. Since FF is strongly related to R_S, the decrease in R_S gives the increase in FF. Overall, the GS-SBSC is improved from 1.8 % PCE to 3.0 % PCE upon doping with 10 mM $AuCl_3$ in nitromethane.

5.3.2. GIS cells with ALD Al_2O_3

To build upon the efficiency improvements of doped GS-SBSC, a thin insulating layer of Al_2O_3 was inserted between the graphene and silicon and form a graphene-insulator-semiconductor (GIS) cell. Previous studies have shown that materials such as silicon oxide [64], graphene oxide (GO) [61], and 2-D materials such as hexagonal boron nitride (h-BN) [89] and MoS_2 [74] increases the overall efficiencies of GS solar cells. Introducing an inter-layer between graphene and silicon were proven to improve the overall performance of GS heterojunction solar cells by blocking carriers from recombining at the interface, reducing the density of interface states, and increasing the carrier lifetime (τ). Here, we introduce another inter-layer material, Al_2O_3, which was selected because it has been shown to effectively passivate c-Si by suppressing surface recombination and increase τ [90-92]. To check the passivation quality of our Al_2O_3, we deposited a thin layer on both sides of a cleaned float zone (FZ) n-type silicon wafer (1 ~ 5 Ω·cm) and measured the carrier lifetime by photoconductance method (Sinton instruments WCT-120). The carrier lifetime before and after deposition was 2 and 27 μs, respectively, with 2 nm of Al_2O_3, which is comparable to the 33 μs lifetime for a cell with a graphene oxide (GO) interlayer [61].

Figure 5.5 (a) compares the V_{OC} and J_{SC} of GIS cells on thin silicon films with different Al_2O_3 thicknesses. The J_{SC} shows limited variation for the different Al_2O_3 thicknesses, while the V_{OC} tends to increase up to 1 nm Al_2O_3 and then saturates. This increase in V_{OC} upon including the Al_2O_3 layer shows that the interlayer indeed passivates the Si surface of the GIS cells.

To extract additional information about the GIS device performance, we consider the diode characteristics. For the case of a device with the metal-insulator-semiconductor

(MIS) structure, with the thin insulator material at the interface, the saturation current density J_S is described as

$$J_s = A^* T^2 \exp(\frac{-\phi_{SBH}}{kT}) \exp(-d\sqrt{\phi_T}) \quad (3)$$

where ϕ_T is the barrier height presented by Al_2O_3, and d is the Al_2O_3 thickness [93]. Figure 5.5 (b) illustrates the band diagram of GIS structure. While the current density is inverse exponentially proportional to insulator thickness, changing the thickness does not

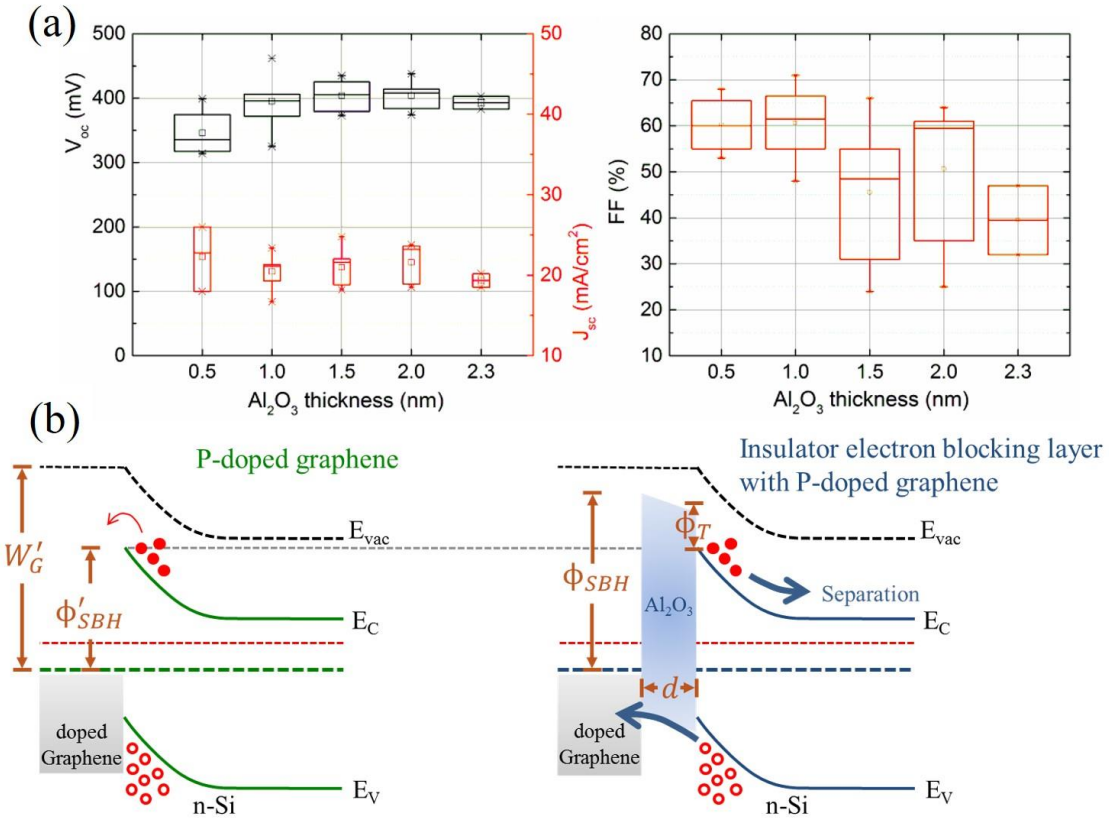


Figure 5.5: (a) V_{OC}, J_{SC} and FF versus Al_2O_3 thickness for GIS solar cells on exfoliated silicon film. (b) Qualitative band diagram of GS cells with and without interlayer oxide.

drastically affect J_{SC}, which is consistent with previous publications [61, 64]. For our GIS structure with Al_2O_3, while increasing the Al_2O_3 thickness initially increases the V_{OC}, a competing process of photocurrent suppression seems to occur with thicker Al_2O_3 devices, resulting in V_{OC} saturation. This phenomenon is also consistent with previous studies, such as with Si native oxides [64]. The addition of Al_2O_3 also gives a boost to the FF compared with the GS-SBSC, as seen in Figure 5.4 (a) and 5.5 (a). This phenomenon may be understood by considering the interaction between MLG and its substrate. ALD deposition of the Al_2O_3 gives a uniform and conformal high k dielectric substrate for the MLG, compared with bare
silicon, and it is understood to impact the mobility (and R_S) of graphene [94-96]. For the GIS cells, enhancement in hole transport in the MLG would lower the device R_S with thin Al_2O_3. As the oxide layer is made thicker, the insulating nature of the layer becomes dominant and an increase in R_S and decrease in FF is observed [61].

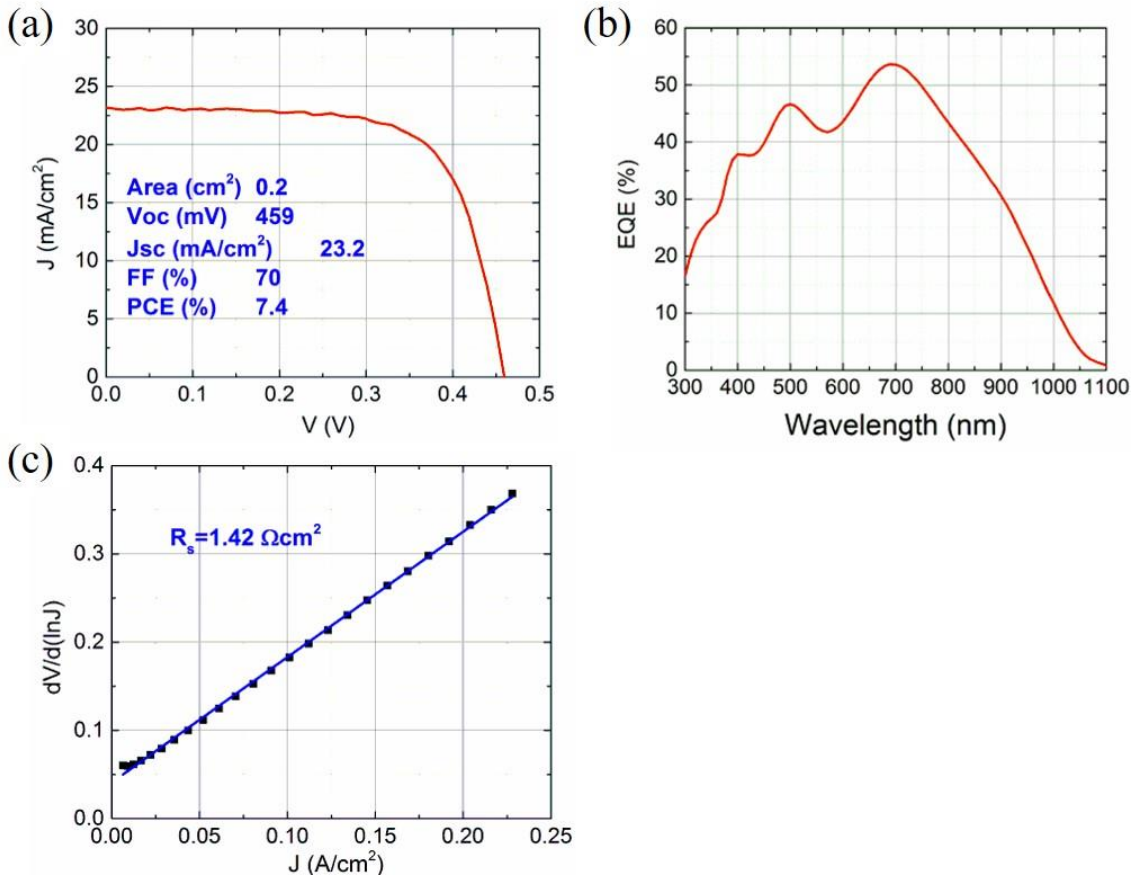


Figure 5.6: GIS cell performance (a) J-V and (b) EQE plots for optimized GIS device with 1 nm Al_2O_3 insulator layer. (c) *n* and R_S extracted from dark current in forward bias for the optimized GIS device.

Figure 5.6 shows the J-V and external quantum efficiency (EQE) measurements for the optimum GIS device with *n* and R_S values extracted from dark current. The highest efficiency of the GIS solar cell on exfoliated thin silicon film was 7.4 % with an Al_2O_3 interlayer thickness of 1 nm, showing V_{OC} of 459 mV, J_{SC} of 23.2 mA/cm^2 and FF

of 70 %. A low R_S leading to high FF, given by controlling the Al_2O_3 thickness, provided the path to optimize the GIS device and maximize efficiency.

Previous GS and GIS solar cell devices have been reported to have unstable performance over time. For example, some devices have utilized volatile dopants for the graphene layer which degraded over time [97] or utilized PMMA encapsulation to show stability for a few days [69]. To check the stability of our devices, the optimum GIS sample was initially measured after fabrication and then left in ambient before re-measurement. The temperature and humidity of the facility is maintained at approximately 21 ˚C and 50 %. The device performance showed < 1 % degradation after 40 days, which is the longest stability of GIS cells reported so far [61,69, 97]. We attribute the increase in stability of this GIS cells to a combination of high quality CVD MLG and ALD AL_2O_3 materials and encapsulation with PMMA.

5.4. CONCLUSION

We report flexible graphene-Al_2O_3-silicon solar cells, with a crystalline 35 μm thick silicon absorber with 7.4 % PCE with stable performance over 40 days under ambient conditions. Our investigation shows that the performance of the cell is controlled by the interfacial Al_2O_3 dielectric thickness. The ability to control the ALD deposition process, along with incorporation of other fabrication processes such as $AuCl_3$ doping, CVD MLG growth, and thin silicon exfoliation, allowed the optimization of the GIS device. The other functional layers in the cell can potentially be optimized for further improvements. For example, the thickness of the thin silicon would determine the amount of incident light absorbed [73]. Also, texturing the front and/or back surface of the silicon or adding

metamaterials could enhance the light absorption of the device by acting as an anti-reflection layer. The GIS cells performance would depend on the type of insulator. Other 2-D materials may also be compatible considering this flexible device. [74, 89] By utilizing new materials and new processes, the scope of possible applications for thin and flexible solar cells can be futther expanded.

Chapter 6. CVD grown h-BN for Photovoltaic and Electronic Device Applications

6.1. INTRODUCTION

Hexagonal boron nitride (h-BN) is a two-dimensional (2-D) material with unique properties. Some properties include, a wide bandgap of 5.9-6.1 eV making it optically transparent, mechanic flexibility due to its thickness, high thermal conductivity and small lattice mismatch (1.7 %) with graphene, making h-BN a strong candidate in graphene/h-BN based electronics and photovoltaics.

In this chapter, we study the effects of CVD grown h-BN as a silicon surface passivation and electron blocking/hole transporting layer for bendable graphene/h-BN/c-Si (GBS) solar cells. We also study the effects h-BN as a gate dielectric for graphene/h-BN based field effect transistors (FETs). We demonstrate that CVD grown h-BN does not effective passivate the silicon surface which may be due to the physical damage during transfer as well as metal contaminants. We also observe h-BN functioning as a gate dielectric in a gate area as large as 500 μm^2.

6.2. EXPERIMENTAL

6.2.1. CVD h-BN growth

h-BN was grown on a nickel foil using a CVD system. Prior to growth, the nickel foil was cleaned by sonicating in acetone followed by IPA at room temperature for 10 mins. Next, the foil was washed with 10% (by volume) hydrochloric acid (HCL) and nitric acid (HNO_3) to remove metallic surface impurities. The foil was then loaded into the CVD chamber which was pumped down to 10^{-6} Torr. Next, the chamber was heated to 1000°C under H_2 flow of 50 sccm and was held for 15 minutes to eliminate any unwanted nickel oxide. Diborane (B_2H_6) and ammonia (NH_3) were flown at a rate of 10 and 30 sccm, respectively, for 15 minutes while the H_2 flow remained unchanged. The total pressure during the growth time was held at 700 mTorr.

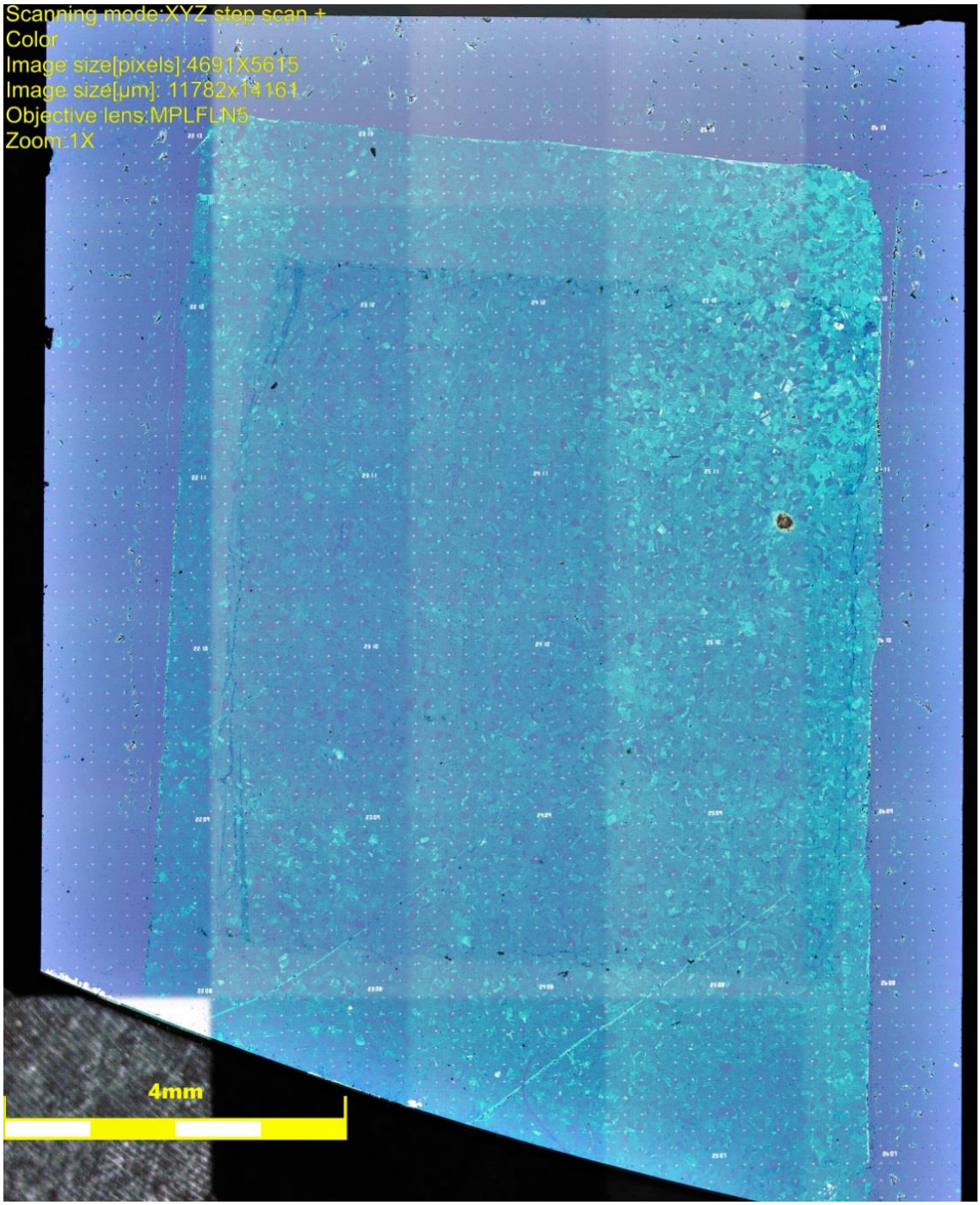


Figure 6.1. Laser optical image of CVD h-BN after transferring on to SiO_2/Si substrate.

6.3. PHOTOVOLTAIC APPLICATION OF CVD H-BN

6.3.1. Graphene/h-BN/c-Si Solar Cell Fabrication

Graphene/h-BN/c-Si solar cells on exfoliated silicon substrates were fabricated similar to GIS solar cells described in chapter 5.2.3. After exfoliation of c-Si followed by surface cleaning, h-BN is transferred using the wet transfer technique much like graphene as described in chapter 5.2.1. Nickel foil is etched by floating the sample on nitric acid (10% HNO_3:DI=1:9 by volume) solution overnight at room temperature. After the nickel has been fully removed, PMMA/h-BN film is transferred on to DI water to clean away any remaining residues on the h-BN surface. After repeating this cleaning procedure three times, the h-BN is transferred on to the target substrate. Figure 6.1 shows the laser microscope image of CVD h-BN after transfer. In order to maintain a PMMA residue free graphene/h-BN interface as well as to reduce the fabrication process, we have devised a simple technique of scooping the PMMA/graphene sample with h-BN/Ni foil. This technique eliminates any PMMA residue between graphene and h-BN resulting in a cleaner interface as well as discarding the need of any post vacuum annealing process to remove any possible residue during transfer.

6.3.2. RESULTS AND DISCUSSION

Table 6.1 shows the solar cell measurement results of GBS cells. For comparison, GIS, GBIS & GS cell results are included. Results indicate that RTCVD grown h-BN does not act as a silicon passivation layer which is contradictory to some published papers. [98, 99] Some possible explanations could be, first the h-BN quality after transfer. Non-uniform growth of h-BN as well as damage such as tears and wrinkles during transfer could prevent the passivation of silicon. Figure 6.2. shows the optical image of CVD h-BN after wet

transfer. Because the h-BN used to fabricate solar cells are below 2 nm in thickness those transparent, to better observe the quality of h-BN after transfer, thicker h-BN was transferred to a SiO_2/Si substrate for analysis. As seen through the optical image, the h-BN is non-uniform in thickness and some areas (purple) either have a very thin layer of h-BN or no h-BN at all. This non-uniformity could lead to insufficient passivation of the silicon surface. Another possibility is the presence of residues between the graphene/h-BN interface. As seen from the schematic in figure 6.2, graphene and h-BN is in contact after transfer. While the graphene is thoroughly rinsed with DI water, there remains the possibility of unwanted residues underneath the graphene. Past studies have shown that PMMA residues, metal ions from the films they were used to grow the 2D material and remains of metal etchants were found between the graphene/h-BN interface which could prevent silicon passivation. [100]

Sample	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	PCE (%)	Area (cm^2)
GBIS	463	12.0	68.2	3.8	0.33
GBS	291	22.6	50.0	3.3	0.202
GIS	459	23.9	70.0	7.4	0.2
GS	356	18.6	50.4	3.3	0.664

Table 6.1: Open circuit voltage (Voc), short circuit current (Jsc), fill factor (FF), power conversion efficiency (PCE) and cell area for graphene/h-BN/Al2O3/exfoliate silicon (GBIS), graphene/h-BN/exfoliation silicon (GBS), graphene/Al2O3/exfoliated silicon (GIS), and graphene/exfoliated silicon (GS) solar cells.

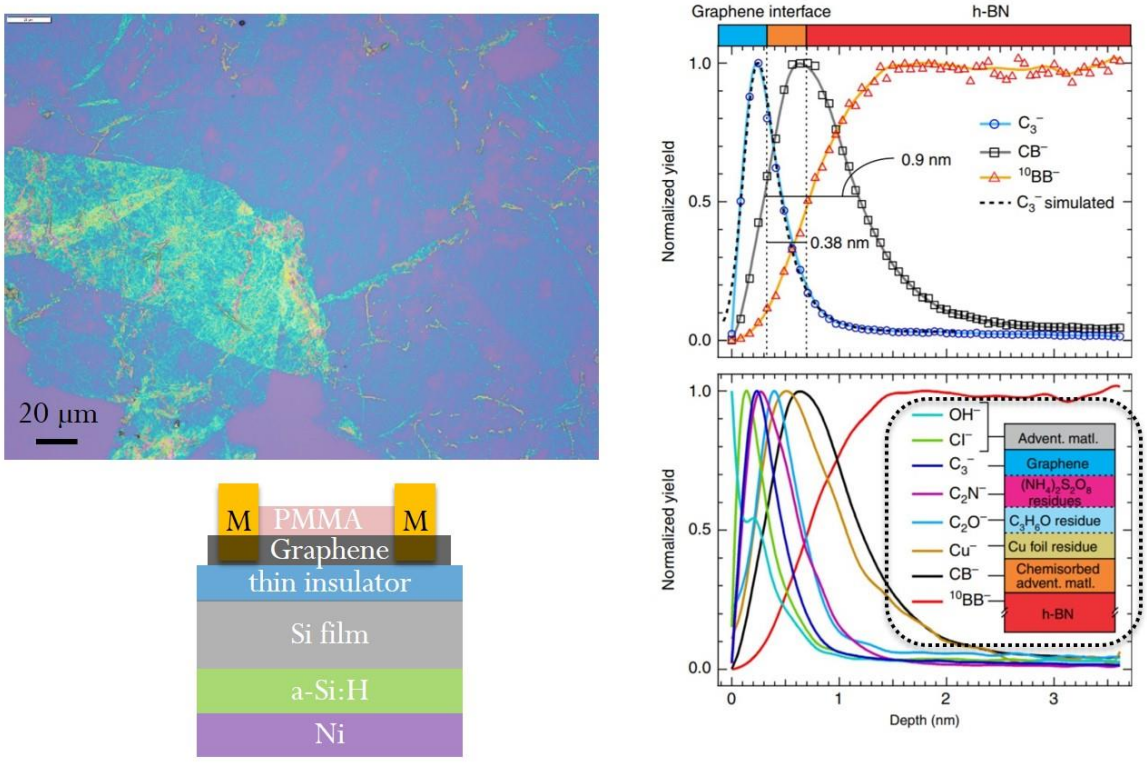


Figure 6.2. Top Left: Optical image of CVD h-BN after wet transfer. Right: Vertical composition of transferred graphene/h-BN stack [100]. Bottom Left: Schematic of graphene/h-BN/silicon solar cell.

6.4. ELECTRONIC APPLICATION OF CVD H-BN

6.4.1. Graphene/h-BN FET

Another promising application for CVD h-BN is using it as a gate dielectric for FETs, especially with two-dimensional channel materials such as graphene and Transition metal dichalcogenides (TMDs). Some unique properties of h-BN are atomic flatness, low dielectric screening, and zero dangling bonds. Graphene/h-BN FETs are demonstrated to characterize CVD h-BN's quality as gate dielectric as well as a potential candidate for all two-dimensional flexible FET.

6.4.2. Fabrication of Graphene/h-BN FET

Highly doped c-Si with x nm of SiO2 was used as substrate material. Graphene/h-BN multi-layer film was created as the same method for GBS solar cells previously discussed in chapter 5.3. After transfer, PMMA is removed by vapor acetone followed by forming gas annealing at 380 C for 8 hours. Next, graphene channel is patterned by photolithography and oxygen plasma etch followed by a 2^{nd} forming gas anneal to remove any residual photoresist. Source/drain metal pads are formed by photolithography and lift-off of Cr/Au (5/50 nm) followed by another forming gas anneal. The top h-BN layer, which serves as the top gate dielectric is transferred using the wet transfer technique. Again, PMMA is removed by vapor acetone and forming gas anneal. Finally, top gate metal is patterned by another photolithography and lift-off of Cr/Au (5/50 nm).

6.4.3. Results and Discussion

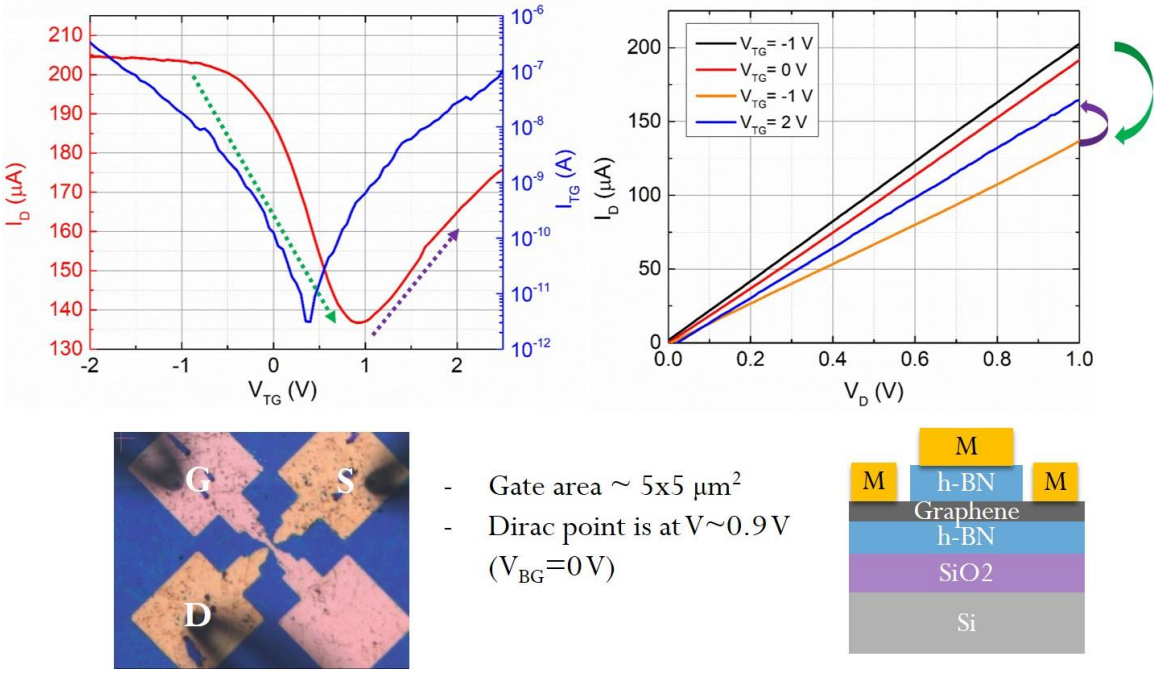


Figure 6.3. Top: I_D/V_G and I_D/V_G characteristic of graphene/h-BN FET. Bottom: Optical image and illustration of graphene/h-BN FET.

Figure 6.3 shows the device characteristics of CVD graphene/h-BN FET. The Dirac point is located around 0.9 V with negligible gate leakage indicating that RTCVD grown h-BN functions as a gate dielectric.

Chapter 7. Conclusion and Future Work

In this dissertation, various optoelectronic devices for power conversion and generation have be researched: from InGaAs band engineering, flexible organic/inorganic photovoltaics to CVD h-BN applications and AlGaN/GaN 2DEG HEMTs.

In InGaAs band engineering, achieving damage-free, uniform, abrupt, ultra-shallow junctions while simultaneously controlling the doping concentration on the nanoscale is an ongoing challenge to the scaling down of electronic device dimensions. We demonstrated a simple method of effectively doping III-V compound semiconductors, specifically InGaAs, by a solid phase doping source. This method is based on the in-diffusion of oxygen and/or silicon from a deposited non-stoichiometric silicon dioxide (SiO_x) film on InGaAs, which then acts as donors upon activation by annealing. The dopant profile and concentration can be controlled by the deposited film thickness and thermal annealing parameters, giving active carrier concentration of 1.4 $x10^{18}$ cm^{-3}. The results also indicate that conventional silicon-based processes must be carefully reviewed for compound semiconductor device fabrication to prevent unintended doping

We have also demonstrated Schottky junction and graphene-insulator-silicon (GIS) solar cells on flexible, thin foils, which utilize the electrical conductivity and optical transparency of graphene as the top transparent contact. Multi-layer graphene was grown by chemical vapor deposition on Cu-Ni foils, followed by p-type doping with Au nanoparticles and encapsulated in PMMA, which showed high stability with minimal performance degradation over more than one month under ambient conditions. Bendable silicon film substrates were fabricated by a kerf-less exfoliation process based on spalling, where the silicon film thickness could be controlled from 8 to 35 μm based on the process recipe. This method allows for re-exfoliation from the parent Si wafer and incorporates the

process for forming the backside metal contact of the solar cell. GIS cells were made with a thin insulating Al2O3 atomic layer deposited film, where the thin Al_2O_3 film acts as a tunneling barrier for holes, while simultaneously passivating the silicon surface, increasing the minority carrier lifetime from 2 to 27 μs. By controlling the Al_2O_3 thickness, an optimized cell with 7.4 % power conversion efficiency (PCE) on a 35 μm thick silicon absorber was fabricated.

For future work, demonstration of InGaAs FinFETs combined with the SRSO solid phase doping and indium metal contact process can be considered. The solid phase doping process can effective dope the source drain extension (SDE) regions of FinFETs and the indium metal layer could achieve low contact resistance, resulting in a high performance FinFET.

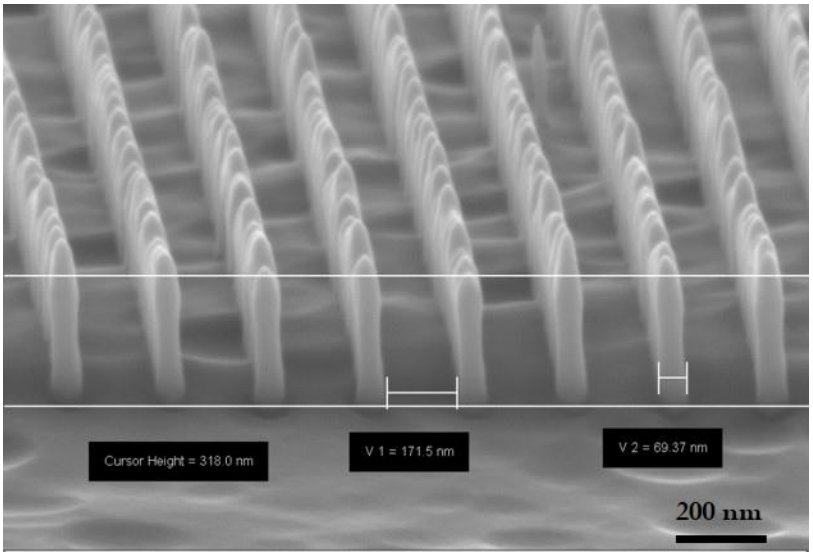


Figure 7.1. Cross-sectional SEM image of InGAs fin.

For organic/inorganic solar cells on flexible substrates, demonstrating tandem cells could lead to higher PCE. Recently, perovskite solar cells have gained extensive attention due to its low cost and simple fabrication process. Band gap of perovskite absorbing layer can be tuned chemically from 1.5 to 2.2 eV, which is suitable with silicon based solar cells. (E_g=1.14 eV). However, unlike conventional single junction perovskite solar cells, for tandem cell architecture, the transparency of the perovskite layer will be the critical factor. One way of overcoming this challenge is through solvent engineering.

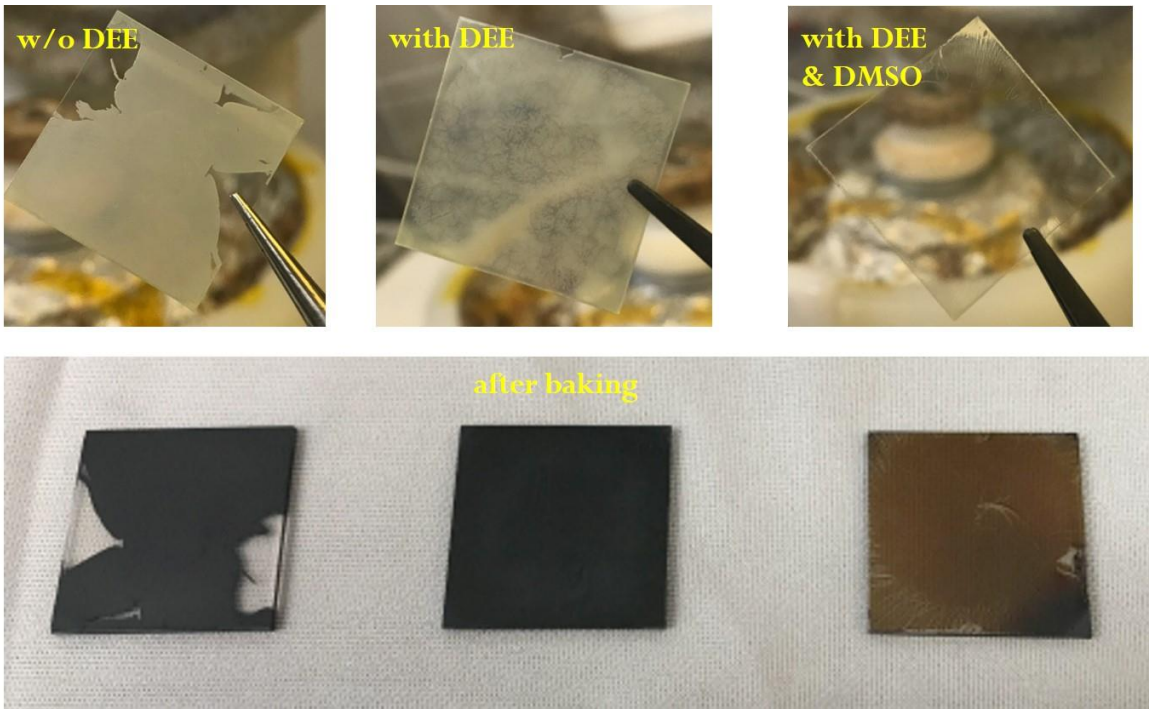


Figure 7.2. Difference in perovskite transparency by solvent engineering.

Finally, for large area 2D materials, demonstration of novel device architecture such as all 2D transistors on flexible substrates can be studied. Through multi-layer 2D stacking, the top gate could be replaced with multilayer graphene while implanting the 2D channel

material with a non zero band gap material such as bilayer graphene or MoS_2. Also, high quality CVD h-BN can be used to study the resistive switching behavior of 2D dielectrics.

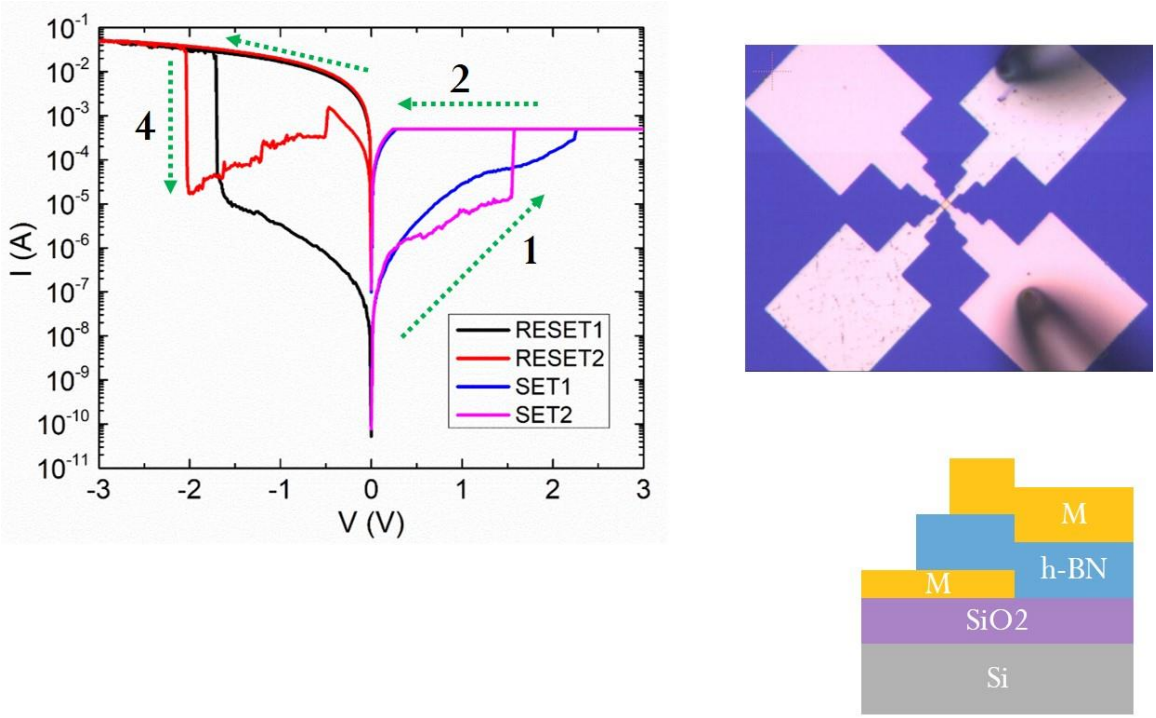


Figure 7.3. Resistive switching properties of thin h-BN grown by MOCVD.

Appendix

List of Publications

1. S. Lee, **J. Ahn**, L. Mathew, R. Rao, Z. Ahang, J. H. Kim, S. K. Banerjee & E. T. Yu, "Highly Improved Passivation of c-Si Surfaces Using a Gradient intrinsic a-Si:H Layer on Silicon Heterojunction Solar Cells", *Journal of Applied Physics*, 123, 163101 (2018)
2. **J. Ahn**, H. Chou, & S. K. Banerjee. "Improved efficiency of Graphene-silicon Schottky junction solar cells by insertion of Al_2O_3 layer" *Journal of Applied Physics*, 121, 163105 (2017)
3. **J. Ahn**, H. Chou, D. Koh, T. Kim, J. Song & S. K. Banerjee. "Nanoscale doping of compound semiconductors by solid phase diffusion" *Applied Physics Letters*, 108, 122107 (2016)
4. D. Koh, S.-H. Shin, **J. Ahn**, S. Sonde, H.-M. Kwon, T. Orzali, T.-W. Kim, D.-H. Kim and S. K. Banerjee. "Damage free Ar ion plasma surface treatment on InGaAs-on-Silicon MOS device" *Applied Physics Letters*, 107, 183509 (2015)
5. Y. Zhang, A. Hosseini, **J. Ahn**, D. Kwong, B. Fallahazad, E. Tutuc and R. T. Chen. "Vertically Integrated Double-layer On-Chip Silicon Membranes for 1-to-12 waveguide fanouts" *Applied Physics Letters*, 100, 181102 (2012)
6. **J. Ahn**, H. Subbaraman, L. Zhu, S. Chakravarty, E. Tutuc and R. T. Chen. "2D Silicon-based surface-normal vertical cavity photonic crystal waveguide array for high-density optical interconnects", *SPIE OPTO* (2013)
7. Y. Zhang, A. Hosseini, **J. Ahn**, D. Kwong, B. Fallahazad, E. Tutuc and R. T. Chen. "Silicon-based Double-layer 1x12 Multimode Interference oupler for Three-dimensional Photonic Integration" *IEEE. TuD4* (2012

Appendix

List of Fabrication recipes

- Photolithography using MA6

Spin coat AZ5214 3000~6000 rpm, thinner photoresist results higher resolution

Bake at 90 ˚C for 2 min

Expose condition: 7 sec, soft contact (light source:CI1, 7.5 mW), Al Gap: 15 μm,

Wec type: Cont

Develop for 40 – 50 sec in developer followed by 1 min rinse in DI water

- Image reversal recipe using MA6 and AZ5214 as photoresist

Spin coat AZ5214 3000~6000 rpm, thinner photoresist results higher resolution

Bake at 90 ˚C for 2 min

Expose condition: 3 sec, soft contact (light source:CI1, 7.5 mW), Al Gap: 15 μm,

Wec type: Cont

Post bake at 110 ˚C for 90 sec

Flood exposure using MA6 for 50 sec

Develop for 50 – 90 sec in developer followed by 1 min rinse in DI water

- Electroplating using EP-2 (Right side bath)

Deposit Ti or Cr (adhesion layer, 5 nm)/Ni (seed layer, 50 nm) using electron beam evaporator (CHA1 or CHA2)

Apply a thin layer of silver paste between Ni and metal electrode attached on the teflon holder for electroplating

Apply nail polish on exposed semiconductor surfaces to prevent any unwanted electroplating (including all edges and backside of semiconductor wafer).

References

[1] HTTPS://WWW.NREL.GOV/PV/ASSETS/PDFS/PV-EFFICIENCIES-07-17-2018.PDF

[2] J. A. DEL ALAMO, NATURE, **479**, 317-323 (2011)

[3] D.J. Frank, IBM J. Res. Dev. 46, 235-244 (2002)

[4] L. PELAZ, L/ MARQUES, M. ABOY, P/ LOPEZ, I. SANTOS, R. DUFFY, IEDM, 513-516 (2009), DOI: 10.1109/IEDM.2009.5424309

[5] K.S. Novoselove, A.K. Geim, S.V. Morozov, D. Jirang, M. I. Katsnelson, I.V. Grigorieva, S. V. Dubonos and A. A. Firsov, Nature, 438, 197-200 (2005)

[6] A. LIPP, K. A. SCHWETZ, K. HUNOLD, J. EUR. CERAM. SOC. 5, 3-9 (1989)

[7] Y. CHEN, J. ZOU, S. J. CAMPBELL, G. LE CAER, APPL. PHYS, LETT. 84, 3420-2432 (2004)

[8] L. MATHEW AND D. JAWARANI, U.S. PATEN 7, 749,884 (6 JULY 2010)

[9] D. S. UM, S. LIM, Y. LEE, H. LEE, H. J. KIM, W. C. YEN, Y. L. CHUEH, H. KO, ACS NANO, **8**, 3080 (2014)

[10] ITRS, INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS (2013) HTTP://WWW.ITRS.NET/LINKS/2013ITRS/HOME2013.HTM

[11] P. D. Kirsch, R.J.W Hill, J. Huang, W. Y. Loh, T.-W. Kim, M.H. Wong, B. G. Min, C. Huffman, D. Veksler, C.D. Young *et al*, Int. Symp. VLSI Technol. Syst. Appl. 1-2. (2012)

[12] R. J. W. Hill, J. Huang, W. Y. Loh, T. Kim, M. H. Wong, D. Veksler, T. H. Cunningham, R. Droopad, J. Oh, C. Hobbs, P. D. Kirsch, and R. Jammy, Silicon Compatible Materials, Processes, and Technologies for Advanced Integrated Circuits and Emerging Applications 2, 45 179 (2012)

[13] A. G. Baca, P. C. Chang, A. A. Allerman, and T. J. Drummond, Proc. Electrochem. Soc. **99**, 155 (1999)

[14] S. K. Ghandhi, *Ion Implantation. In VLSI Fabrication Principles* (Wiley Inter-Science, 1994) pp 389-393

[15] T. E. Haynes, and O. W. Holland, Appl Phys Lett. **59**, 452 (1991)

[16] T. E. Haynes, and O. W. Holland, Appl Phys Lett **58**, 62 (1991)

[17] W. Wesch, and M. C. Ridgway, Mat Sci Semicon Proc. **7**, 35 (2004)

[18] J. C. Ho, A. C. Ford, Y. L. Chueh, P. W. Leu, O. Ergen, K. Takei, G. Smith, P. Majhi, J. Bennett, and A. Javey, Appl Phys Lett, **95**, 072108. (2009)

[19] E. D. Marshall, W. X. Chen, C. S. Wu, S. S. Lau, and T. F. Kuech, Appl Phys Lett, **47**, 298 (1985)

[20] J. D. Yearsley, J. C. Lin, E. Hwang, S. Datta, and S. E. Mohney, J Appl Phys, **112**, 5 (2012)

[21] K. Takei, R. Kapadia, Y. J. Li, E. Plis, S. Krishna, and A. Javey, J Phys Chem C, **117**, 17845 (2013)

[22] N. Daldosso, G. Das, S. Larcheri, G. Mariotto, G. Dalba, L. Pavesi, A. Irrera, F. Priolo, F. Iacona, and F. Rocca, J Appl Phys. **101**, 11 (2007)

[23] L. R. Doolittle, Nucl. Instrum Meth B, **15**, 227 (1986)

[24] F. Ay, and A. Aydinli, Optical Materials **26**, 33 (2004)

[25] S. Doshi, P. N. K. Deenapanray, H. H. Tan, and C. Jagadish, J Vac Sci Technol B **21**, 198 (2003)

[26] A. Pepin, C. Vieu, M. Schneider, H. Launois, and Y. Nissim, J Vac Sci Technol B **15**, 142 (1997)

[27] M. B. Dutt, and B. L. Sharma, *Diffusion in compound semiconductors*. In D. L. Beke, Diffusion in Semiconductors (Springer Berlin Heidelberg, 1998) pp 3-11

[28] W. Orellana and A. C. Ferraz, Phys. Rev. B, 61, 5325 (2000)

[29] H. P. Komsa and A. Pasquarello, Phys. B, 407, 2833 (2012)

[30] T. Mattila and R. Nieminen, Phys. Rev. B, 54, 16676 (1996)

[31] S. Loualiche, A. Gauneau, A. Le Corre, D. Lecrosnier, and H. L'Haridon, Appl. Phys. Lett. 51, 1361 (1987)

[32] R. A. Stall, R. J. Wunder, V. Swaminathan, and H. M. Cox, Appl Phys Lett. **47**, 518 (1985)

[33] A. Le Corre, J. Caulet, M. Fauneau, S. Loualiche, H. L'Haridon, D. Lecrosnier, A. Roizes and J. P. David, Appl Phys Lett. **51**, 1597 (1987)

[34] I. Kim, Material Letters. 57, 4033 (2003)

[35] Revelis, V. G et al. Fiz Met & Metalloved. 37, 67 (1974)

[36] H. J. Kim et al., J. Appl. Phys. 67, 4183 (1990)

[37] First Power Performance Demonstration of Flexible AlGaN/GaN High Electron Mobility Transistor, IEEE Electron Device Letter, vol.37 No.5 p.553 (2016)

[38] Q.Z. Lui, L. S. Yu, F. Deng, S. S. Lau, Q. Chen, J. W. Yang and M. A. Khan, Appl. Phys Lett. 71, 1658 (1997)

[39] S. Ruvimov, Z. Liliental-Weber, J. Washburn, K. J. Duxstad, E. E. Haller, Z. F. Fan, N. S. Mohammad, W. Kim, A. E. Botchkarev, and H. Morkoc, Appl. Phys. Lett, 69, 1556 (1996)

[40] D. Buttrari, A. Chini, G. Meneghesso, E. Zanoni, B. Moran, S. Heikman, N. Q. Zhang, L. Shen, R. Coffie, S. P. Denbaars, and U. Mishra, IEEE Electron Device Lett. 23, 76 (2002)

[41] Z. Fan, S. N. Mohamad, W. Kim, O. Aktas, A. E. Botchkarev, and H. Morkoc, Apply. Phys. Lett. 68, 1672 (1996)

[42] D. F. Wang, F. Shiwei, C. Lu, A. Motayed, M. Jah, S. N. Mohammad, K. A. Jones, and L. S. Riba, J. Appl. Phys. 89, 6214 (2001)

[43] E. F. Chor, D. Zhang, H. Gong, G. L. Chen, and T. Y. F. Liew, J. Appl. Phys. 90, 1242 (2001)

[44] S. J. Cai, R. Li, Y. L. Chen, L. Wong, W. G. Wu, S. G. Thomas, and K. L. Wnag, Electron. Lett. 34, 2354 (1998)

[45] C. T. Lee and H. W. Kao, Appl. Phys. Lett. 76, 2364 (2000)

[46] A. P. Zhang, G. T. Dang, F. Ren, J. M. Van Hove, J. J. Klaassen, P. P. Chow, X. A. Cao, and S. J. Pearton, J. Vac. Sci. Technol. A 18, 1149 (2000)

[47] D. Selvanathan, L. Zhou, V. Kumar, and I. Adesida, Phys. Stat. Sol. (1) 194, N\no.2, 583-586 (2002)

[48] G. R. Bhimanapati, Z. Lin, V. Meunier, Y. Jung, J. Cha, S. Das, D. Xiao, Y. Son, M. S. Strano, V. R. Cooper, L. Liang, S. G. Louie, E. Ringe, W. Zhou, S. S. Kim, R. R. Naik, B. G. Sumpter, H. Terrones, F. Xia, Y. Wang, J. Zhu, D. Akinwande, N. Alem, J. A. Schuller, R. E. Schaak, M. Terrones, and J. A. Robinson, ACS Nano 9, 11509 (2015).

[49] A. C. Ferrari, F. Bonaccorso, V. Fal'ko, K. S. Novoselov, S. Roche, P. Bøggild, S. Borini, F. H. L. Koppens, V. Palermo, N. Pugno, J. A. Garrido, R. Sordan, A. Bianco, L. Ballerini, M. Prato, E. Lidorikis, J. Kivioja, C. Marinelli, T. Ryh€anen, A. Morpurgo, J. N. Coleman, V. Nicolosi, L. Colombo, A. Fert, M. Garcia-Hernandez, A. Bachtold, G. F. Schneider, F. Guinea, C. Dekker, M. Barbone, Z. Sun, C. Galiotis, A. N. Grigorenko, G. Konstantatos, A. Kis, M. Katsnelson, L. Vandersypen, A. Loiseau, V. Morandi, D. Neumaier, E. Treossi, V. Pellegrini, M. Polini, A. Tredicucci, G. M. Williams, B. Hee Hong, J.-H. Ahn, J. Min Kim, H. Zirath, B. J. van Wees, H. van der Zant, L. Occhipinti, A. Di Matteo, I. A. Kinloch, T. Seyller, E. Quesnel, X. Feng, K. Teo, N. Rupesinghe, P. Hakonen, S. R. T. Neil, Q. Tannock, T. L€ofwander, and J. Kinaret, Nanoscale 7, 4598 (2015).

[50] F. Bonaccorso, L. Colombo, G. Yu, M. Stoller, V. Tozzini, A. C. Ferrari, R. S. Ruoff, and V. Pellegrini, Science 347, 1246501 (2015).

[51] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, Science 306, 666 (2004).

[52] C. Lee, X. Wei, J. W. Kysar, and J. Hone, Science 321, 385 (2008).

[53] R. R. Nair, P. Blake, A. N. Grigorenko, K. S. Novoselov, T. J. Booth, T. Stauber, N. M. R. Peres, and A. K. Geim, Science 320, 1308 (2008).

[54] M. Fuhrer, C. Lau, and A. MacDonald, MRS Bull. 35, 289 (2010).

[55] K. S. Kim, Y. Zhao, H. Jang, S. Y. Lee, J. M. Kim, K. S. Kim, J. Ahn, P. Kim, J. Choi, and B. H. Hong, Nature 457, 706 (2009).

[56] S. Bae, H. Kim, Y. Lee, X. Xu, J.-S. Park, Y. Zheng, J. Balakrishnan, T. Lei, H. R. Kim, Y. Il Song, Y.-J. Kim, K. S. Kim, B. Ozyilmaz, J.-H. Ahn, B. H. Hong, and S. Iijima, Nat. Nanotechnol. 5, 574 (2010).

[57] Y. Song, W. Fang, R. Brenes, and J. Kong, Nano Today 10, 681 (2015).

[58] X. Li, H. Zhu, K. Wang, A. Cao, J. Wei, C. Li, Y. Jia, Z. Li, X. Li, and D. Wu, Adv. Mater. 22, 2743 (2010).

[59] W. Jie, F. Zheng, and J. Hao, Appl. Phys. Lett. 103, 233111 (2013).

[60] X. Miao, S. Tongay, M. K. Petterson, K. Berke, A. G. Rinzler, B. R. Appleton, and A. F. Hebard, Nano Lett. 12, 2745 (2012).

[61] L. Yang, X. Yu, M. Xu, H. Chen, and D. Yang, J. Mater. Chem. A 2, 16877 (2014).

[62] D. Xu, X. Yu, L. Zuo, and D. Yang, RSC Adv. 5, 46480 (2015).

[63] E. Shi, H. Li, L. Yang, L. Zhang, Z. Li, P. Li, Y. Shang, S. Wu, X. Li, J. Wei, K. Wang, H. Zhu, D. Wu, Y. Fang, and A. Cao, Nano Lett. 13, 1776 (2013).

[64] Y. Song, X. Li, C. Mackin, X. Zhang, W. Fang, T. Palacios, H. Zhu, and J. Kong, Nano Lett. 15, 2104 (2015).

[65] W. Jie and J. Hao, Nanoscale 6, 6346 (2014).

[66] P. Kowalczewski and L. C. Andreani, Sol. Energy Mater. Sol. Cells 143, 260 (2015).

[67] M. B. Schubert and J. H. Werner, Mater. Today 9, 42 (2006).

[68] M. J. Yun, S. I. Cha, S. H. Seo, and D. Y. Lee, Sci. Rep. 4, 5322 (2014).

[69] T. Jiao, D. Wei, J. Liu, W. Sun, S. Jia, W. Zhang, Y. Feng, H. Shi, and C. Du, RSC Adv. 5, 73202 (2015).

[70] K. Ruan, K. Ding, Y. Wang, S. Diao, Z. Shao, X. Zhang, and J. Jie, J. Mater. Chem. A 3, 14370 (2015).

[71] X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo, and R. S. Ruoff, Science 324, 1312 (2009).

[72] X. Li, W. Cai, L. Colombo, and R. S. Ruoff, Nano Lett. 9, 4268 (2009).

[73] T. Jiao, D. Wei, X. Song, T. Sun, J. Yang, L. Yu, Y. Feng, W. Sun, W. Wei, H. Shi, C. Hu, and C. Du, RSC Adv. 6, 10175 (2016).

[74] Y. Tsuboi, F. Wang, D. Kozawa, K. Funahashi, S. Mouri, Y. Miyauchi, T. Takenobu, and K. Matsuda, Nanoscale 7, 14476 (2015).

[75] S. Chen, W. Cai, R. D. Piner, J. W. Suk, Y. Wu, Y. Ren, J. Kang, and R. S. Ruoff, Nano Lett. 11, 3519 (2011).

[76] Y. Wu, H. Chou, H. Ji, Q. Wu, S. Chen, W. Jiang, Y. Hao, J. Kang, Y. Ren, R. D. Piner, and R. S. Ruoff, ACS Nano 6, 7731 (2012).

[77] A. C. Ferrari, Solid State Commun. 143, 47 (2007).

[78] A. C. Ferrari, J. C. Meyer, V. Scardaci, C. Casiraghi, M. Lazzeri, F. Mauri, S. Piscanec, D. Jiang, K. S. Novoselov, S. Roth, and A. K. Geim, Phys. Rev. Lett. 97, 187401 (2006).

[79] Y. Shi, K. K. Kim, A. Reina, M. Hofmann, L. J. Li, and J. Kong, ACS Nano 4, 2689 (2010).

[80] K. K. Kim, A. Reina, Y. Shi, H. Park, L. J. Li, Y. H. Lee, and J. Kong, Nanotechnology 21, 285205 (2010).

[81] J. W. Suk, A. Kitt, C. W. Magnuson, Y. Hao, S. Ahmed, J. An, A. K. Swan, B. B. Goldberg, and R. S. Ruoff, ACS Nano 5, 6916 (2011).

[82] E. U. Onyegam, D. Sarkar, M. M. Hilali, S. Saha, L. Mathew, R. A. Rao, R. S. Smith, D. Xu, D. Jawarani, R. Garcia, M. Ainom, and S. K. Banerjee, Appl. Phys. Lett. 104, 153902 (2014).

[83] R. A. Rao, L. Mathew, S. Saha, S. Smith, D. Sarkar, R. Garcia, R. Stout, A. Gurmu, E. Onyegam, and D. Ahn, in 2011 37th IEEE Photovoltaic Specialists Conference (PVSC) (IEEE, 2011), pp. 1504–1507.

[84] L. Mathew and D. Jawarani, U.S. patent 7749884 B2 (2010).

[85] Y. H. Lee, Y.-J. Kim, S. M. J. Han, H. Song, and J. Oh, Appl. Phys. Lett. 109, 132101 (2016).

[86] X. Li, Y. Zhu, W. Cai, M. Borysiak, B. Han, D. Chen, R. D. Piner, L. Colombo, and R. S. Ruoff, Nano Lett. 9, 4359 (2009).

[87] Y. Chen, X. L. Gong, and J. G. Gai, Adv. Sci. 3, 1500343 (2016).

[88] D. K. Schroder, Semiconductor Material and Device Characterization (John Wiley & Sons, 2006).

[89] J.-H. Meng, X. Liu, X.-W. Zhang, Y. Zhang, H.-L. Wang, Z.-G. Yin, Y.- Z. Zhang, H. Liu, J.-B. You, and H. Yan, Nano Energy 28, 44 (2016).

[90] R. Hezel and K. Jaeger, J. Electrochem. Soc. 136, 518 (1989).

[91] B. Hoex, S. B. S. Heil, E. Langereis, M. C. M. Van De Banden, and W. M. M. Kessels, Appl. Phys. Lett. 89, 042112 (2006).

[92] B. Hoex, J. Schmidt, P. Pohl, M. C. M. Van de Sanden, and W. M. M. Kessels, J. Appl. Phys. 104, 44903 (2008).

[93] H. C. Card and E. H. Rhoderick, J. Phys. D: Appl. Phys. 4, 1589 (1971).

[94] M. Houssa, High K Gate Dielectrics (CRC Press, 2003).

[95] L. Liao, J. Bai, Y. Qu, Y. Huang, and X. Duan, Nanotechnology 21, 15705 (2010).

[96] A. Y. Serov, Z.-Y. Ong, M. V. Fischetti, and E. Pop, J. Appl. Phys. 116, 34507 (2014).

[97] J. H. Meng, X. Liu, X. W. Zhang, Y. Zhang, H. L. Wang, Z. G., Yin, Y. Z. Zhang, H. Liu, J. B. You, H. Yan, Nano Energy, 28, 44-50 (2016)

[98] Z. Fan, S. N. Mohammad, W. Kim, O. Aktas, A. E. Botchkarev and H. Morkoc, Appl. Phys. Lett. 68, 1672 (1996)

[99] X. Li, S. Lin, X. Lin, Z. Wu, P. Wang, S. Zhang, H. Zhong, W. Xu, Z. Wu, and W. Fang, Optical Express, 24, no.1, 134-145 (2016)

[100] H. Chou, A. Ismach, R. Ghosh, R. Ruoff and A. Dolocan, Nature Communications, 6, 7482 (2015)

Vita

Jaehyun Ahn was born in Busan, South Korea on January 1983, the son of Jonghan Ahn and Myungsook Park. He attended Seoul High School, from which he graduated in 2001. He attended Korea University in Seoul, South Korea, where he received Bachelor of Engineering degree in Electrical, Electronic and Communications Engineering in 2008. He received Master of Science degree in Electronic and Computer Engineering from Korea University, Seoul, South Korea in 2010. He enrolled in The University of Texas at Austin in the fall of 2010 and began his study for Doctor of philosophy in Electrical and Computer Engineering. His doctoral research on power conversion and generation of optoelectronic devices was supervised by Professor Sanjay K. Banerjee.

Permanent email address: xellove@gmail.com

This dissertation was typed by Jaehyun Ahn.