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Design of Circuits for Sub-Threshold Voltages:

Implementation of Adders

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Design of Circuits for Sub-Threshold Voltages:

Implementation of Adders

by

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Report

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Implementation of Adders

by

Ankith Giliyar Shanthiraj, MSE

The University of Texas at Austin, 2016

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CO-SUPERVISOR: Nur Touba

The demand and the need for low-power circuits is an ever increasing trend particularly due to the added overhead of design of efficient cooling systems or more sophisticated and expensive packaging techniques. In most new emerging applications that demand low power consumption such as biomedical implants, wearable devices, micro-sensor nodes and countless others, energy efficiency emphasis far supersedes the traditional focus on improving the speed. Such energy constrained systems can be operated at considerably reduced performance levels in order to save power and extend their battery lifetimes. Sub-Threshold design has proven useful for ultra-low power and low energy applications since the dynamic power is reduced quadratically with supply voltage; the least energy operation usually takes place in the sub-threshold region.

This work provides a comprehensive analysis of the CMOS standard cell characterization in the sub-threshold region, layout, logical library extraction, optimization and top-level implementation of 2 of the parallel prefix adders of different word sizes in 45nm technology with comparison between the sub-threshold region and strong inversion regions of operation. The analysis is done on PPA: power (energy), performance and area, the common metrics for any chip design. The switching activities of the circuits were captured using dynamic gate level simulation to perform the time based peak power analysis. Static timing analysis was performed to estimate the delay of the critical path for each circuit.

The analysis and results presented in this report will be helpful in choosing a specific adder configuration for an integrated circuit based on the constraints related to its application.

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Chapter 1: Introduction:

1.1 Importance of Leakage Power:

As the world uses more and more mobile electronic products, controlling power consumption is the primary limiter of scaling semiconductor process technologies and adding features to integrated circuits. This power consumption is divided between active power ($P_{active} \sim CV^2f$), which is the power used while the product is performing its various functions, and leakage power ($P_{leakage} \sim IV$), which is the power consumed by unintended leakage that does not contribute to the IC's function. Leakage power has become a top concern for IC designers in deep submicron process technology nodes (65nm and below) because it has increased to 30-50% of the total IC power consumption. In addition, the leakage problem is worse than generally thought because the simple, traditional leakage power estimation of multiplying the average transistor leakage by the transistor width of the entire IC grossly underestimates the actual product leakage.

Leakage power is primarily the result of unwanted subthreshold current in the transistor channel when the transistor is turned off. Even when the device is in sleep mode or turned off, leakage power is the one that drains the battery. So, what if, for certain type of applications, the operation itself can be performed in leakage condition to extend the battery life and period of operation?

1.2 Problem Description:

Several extensive studies and techniques have been devised for power optimization in the medium performance levels. More recently, there has been a keen interest and focused research in the area of sub-threshold operation of circuits with acceptable performance. But, with scaling in the supply voltage and relatively constant level of the threshold voltage due to leakage concerns, the significant advantages offered by the sub-threshold operation has diminished. This report concisely presents the efforts in implementing an adder, as an example prototype, in the sub-threshold region of operation and evaluating the benefits it offers as well the trade-offs associated with it.

1.3 Importance of Adder as a Prototype for Testing:

The addition circuitry forms the basic core of the ALU of processing cores and its efficiency and performance is critical to the overall system. It is one of the fundamental circuitry on any chip for any purpose so much so that it is implemented as a custom standard cell in many commercial applications. Consequently, over the years, a significant amount of research has gone into designing low-latency adder topologies by primarily cutting down on the carry propagation delay [1] [2] [3]. These efforts led to the design of the parallel prefix computation method for fast carry propagation [4] and hence two parallel-prefix architectures are compared here across two different input adder widths .

1.4 Application Areas:

Sub-Threshold operation is mainly targeted at emerging applications e.g., micro-sensor nodes and wireless sensor networks or a wide range of medical applications such as hearing-aids and pacemakers, wearable computing and self-powered devices which have energy consumption as their primary concern instead of performance, with the ultimate goal of harvesting the energy needed from the surroundings itself. Sub-threshold operation is currently used for some low-power applications such as watches and hearing aids [8]. Emerging ultralow-power applications such as distributed sensor networks are a natural fit with sub-threshold circuits and the need is only growing.

Chapter 2: Approach and Design Methodology

2.1 Literature Survey:

References [5] and [6] show that the sub-threshold operation of circuits can give us significant reduction in the energy consumption as against operation in deep saturation. Certain techniques for device modelling in sub-threshold region are discussed in [7] and will be useful if our design needs to be fabricated on a chip and post-silicon validation performed. The critical step in the design of circuits for this region of operation is the analysis of design charts that need to be done initially [8] [9] [10]. Since the current in the sub-threshold region is an exponential function of the gate voltage [9], it affects the voltage transfer characteristics (VTC) and the optimum W_{pmos}/W_{nmos} ratio that can be used. References [10] [11] and [12] briefly give an insight into the steps involved in the design of a datapath circuit (adder) and reference [14] particularly proves useful during the comprehensive characterization of the libraries which are to be used by the tools for computation.

2.2 Design Specification and Overview:

For ultra-low power and portable applications, design of digital sub-threshold logic is investigated with transistors operated in the sub-threshold region (supply voltage corresponding to logic 1, less than the threshold voltage of the transistor). In this technique, the sub-threshold leakage current of the device is used for computation. Standard design techniques suitable for super-threshold design can be used in the sub-threshold region. However, it has been shown that a complete co-design at all levels of hierarchy (device, circuit, and architecture) is necessary to reduce the overall power consumption while achieving acceptable performance (hundreds of kilohertz) in the sub-threshold regime of operation.

This flow intends to use just the 4 cells, INVX1, INVX4 (4 times the drive strength), NAND2X1 and NOR2X1 in the realization of the data path circuitry. The standard cells used for the design were characterized at 45nm technology with the operating conditions of 1V and 27^{o}C.

The verilog netlist was generated from Cadence Virtuoso® so that this could be used for further analysis and for automatic placement and routing.

The target is to achieve the implementation of tree adders operable at several KHz clock frequencies and offering an energy consumption lower than that of the strong inversion by 10^2 to 10^3 orders of magnitude. The Energy-Delay Product (EDP) and Power Delay Product (PDP) are also computed and evaluated in reference to [5] but making note of the fact that the results in [5] were presented for a supply voltage of 3.3V while the current 45nm technology has a nominal supply voltage of 1V. The area occupied and the power consumption of the resulting design are also presented to the reader. This report describes in detail the design flow for the implementation of circuits in sub-threshold voltage levels addressing key design issues to be considered and the tools and the associated files necessary to realize it.

2.3 Verification and Activity File Generation for Power Analysis

For the gate level simulation, a particular set of pseudo random input vectors, written as a verilog testbench were provided to each of the parallel prefix adder configurations for a given word size. The functional correctness of each of the adder configurations was verified. The simulation was also helpful in dumping the states of the internal nodes of the design for a given simulation time. This is used for the peak power analysis. The CAD tool used for the gate level simulation is Synopsys VCS® and the states of the internal nodes of the circuit are dumped in the file format .vcd.

The .vcd file dumped by VCS is taken into the Synopsys power analysis tool, Primetime-PX for performing the time based peak power analysis. Primetime-PX reads in the design in the form of Verilog Netlist generated from Cadence along with the 45nm standard cell library in the Synopsys .db format. The library contains the tables of the characterized values of internal energy per transition which were done initially during the flow. It also contains the state and path dependent leakage power numbers for each cell. The resultant waveforms generated are in the .fsdb format and have been plotted using the Synopsys Cosmoscope waveform tool. The waveforms provide a histogram of the peak power values at each point of time where there is a change in input vectors. The peak power values include the leakage power and the dynamic power at the particular time stamps.

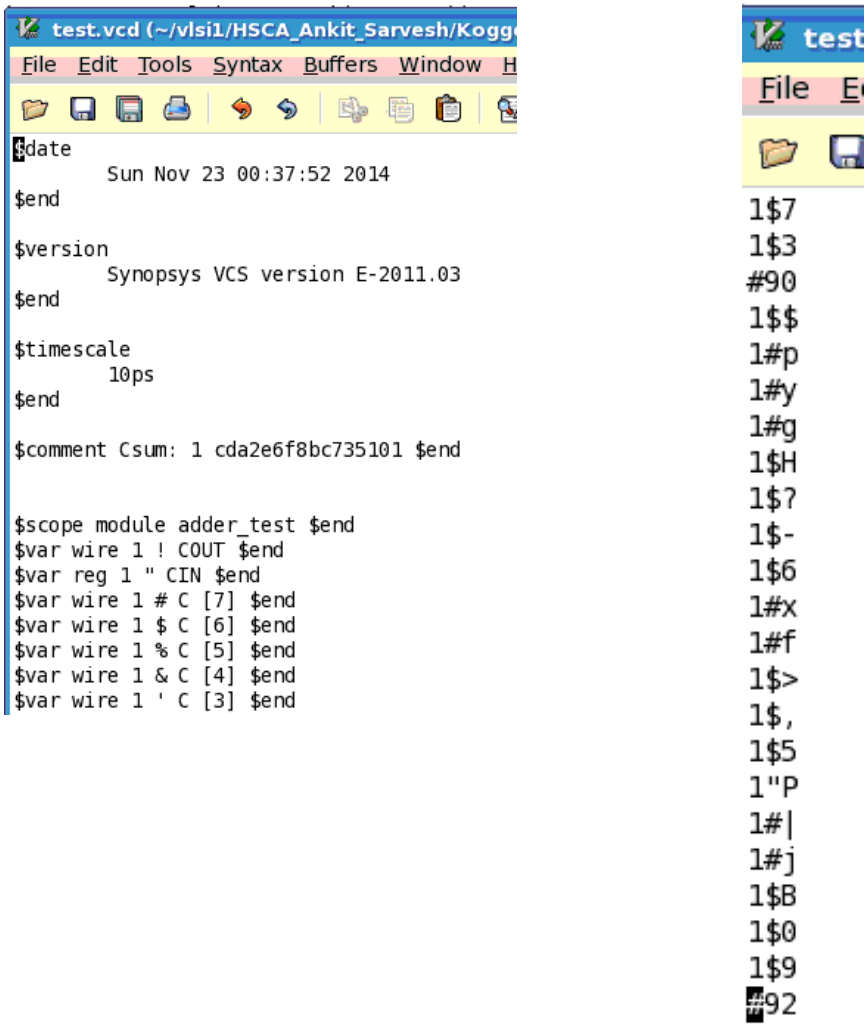


Figure 1: Snippet of a .vcd file with symbols assigned to nets and the value at the time stamp

2.4 Estimation of Critical Delay Using Static Timing Analysis

For the pre-layout static timing analysis, Synopsys STA tool, Primetime® was used to estimate the delay of the critical path of each circuit. The cell delay and the transition tables in 45nm standard cell library for the NAND, NOR and the INVERTER cells were considered in the calculation. For measuring the interconnect delays, wire load models present in the libraries were used.

For the post-layout static timing analysis, the SPEF file generated from encounter after the placement and routing was used instead of the wire load models to generate more realistic delay values of the critical paths.

2.5 Physical Design – Placement and Routing

The physical design of each of the configurations was generated using Cadence Encounter®. The LEF file was provided for the 45nm standard cell technology node along with the layer geometry information. Automatic placement and routing with pre-place and in-place optimization was performed to generate a layout without any design rule violations or functionality changes. The parasitic extraction was then performed to generate the SPF file which models the cell and interconnect delays as RC networks. This file helps in generating a more realistic delay values compared to the pre layout delay values estimated above.
The physical area of the chip after placement and routing was generated from Cadence Encounter.

2.6 List of EDA Tools Used for Design and Analysis

1. Synopsys VCS: Synopsys VCS is an RTL functional simulator that can simulate Verilog, VHDL, and System C models. It was used to verify the functionality of the structural netlists generated from Synopsys Design Compiler or Cadence Virtuoso Schematic editor. This tool was also used in generating the vcd files for peak power analysis.

2. Synopsys Design Compiler: Synopsys DC is a synthesis tool. It maps a behavior model of a design (RTL hardware description model) using a standard cell library into a gate-level netlist.

3. Cadence Virtuoso Schematic Editor: This editor was used to describe the connectivity between standard cells using GUI.

4. Cadence Encounter: This tool was used to perform automatic placement and routing. The input to this tool will be a synthesized gate level netlist. The output is a placed and routed design.

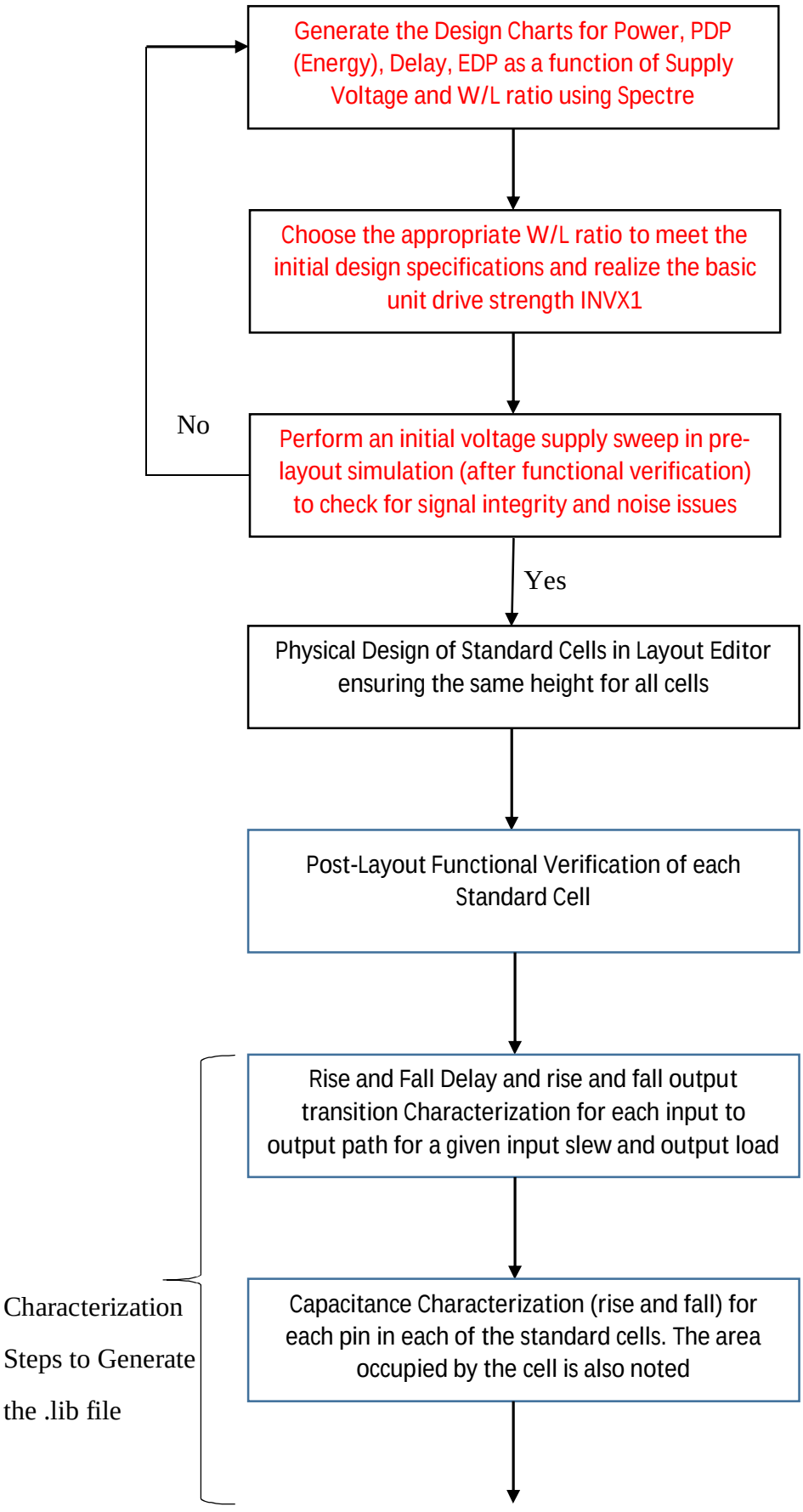
5. Mentor Graphics Caliber: This tool was used to perform DRC and LVS checks after APR and extract the parasitics for accurate timing and power analysis post-layout.

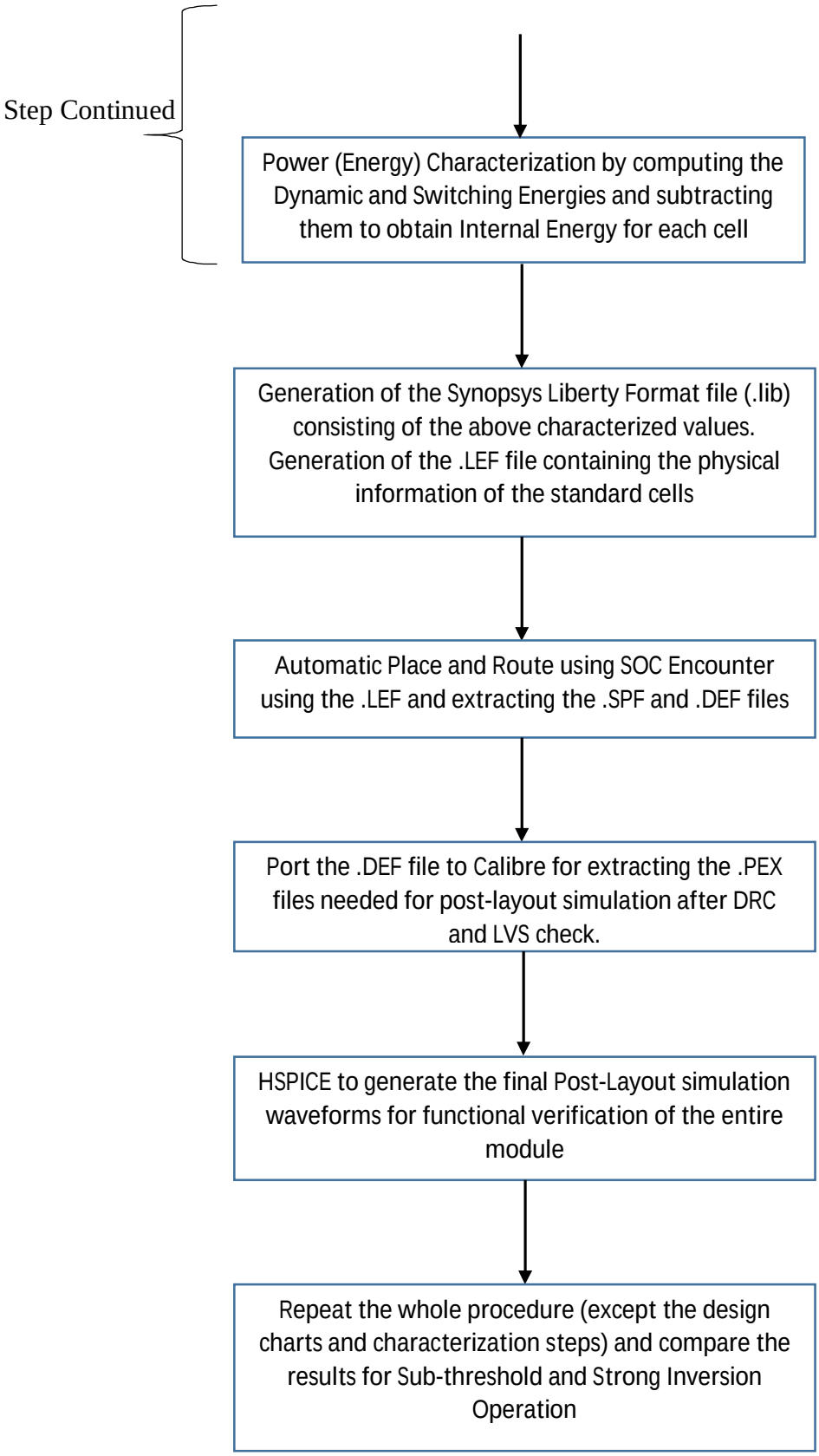
6. Synopsys Primetime: Synopsys PrimeTime is the industry standard tool for timing sign-off. It delivers accurate timing signoff analysis that helps pinpoint timing problems prior to tapeout.

7. Synopsys Primetime-PX: PT-PX analyzes static and dynamic power based on the activity file which provides the static probability and toggle rate information.

8. Synopsys Cosmoscope: Viewing the peak power waveforms dumped by PT-PX in **.fsdb** format

Chapter 3: Design Flow Overview:




Step Continued
Power (Energy) Characterization by computing the Dynamic and Switching Energies and subtracting them to obtain Internal Energy for each cell
Generation of the Synopsys Liberty Format file (.lib) consisting of the above characterized values. Generation of the .LEF file containing the physical information of the standard cells
Automatic Place and Route using SOC Encounter using the .LEF and extracting the .SPF and .DEF files
Port the .DEF file to Calibre for extracting the .PEX files needed for post-layout simulation after DRC and LVS check.
HSPICE to generate the final Post-Layout simulation waveforms for functional verification of the entire module
Repeat the whole procedure (except the design charts and characterization steps) and compare the results for Sub-threshold and Strong Inversion Operation

Chapter 4: Choosing the Design Parameters:

4.1 Sizing and Operating Voltage

4.1.1 Transistor Sizing

In the normal strong inversion region, the ratio of PMOS to NMOS transistor sizes is usually taken as the ratio of the mobilities of the corresponding charge carriers which is approximately equal to 2. Due to the exponential ratio of the transistor currents in the sub threshold region, the plot of delay vs transistor sizes shows that the ratio flattens out and hence provides the freedom of choosing the sizes and at the same time achieving the near optimum delay values.

The 45nm NCSU FREE PDK transistor models are used in this work. The width of the NMOS was fixed at 120nm. The threshold voltage of the NMOS and PMOS models are as follows:

Table 1: Typical Vth Values

Transistor	|Vth| (V)
NMOS_VTL	0.471
PMOS_VTL	0.423

For choosing the size of PMOS for the Standard INVX1 cell, the plots of Average Delay/Energy and EDP (Energy Delay Product) vs. PMOS width was generated in HSPICE as follows.

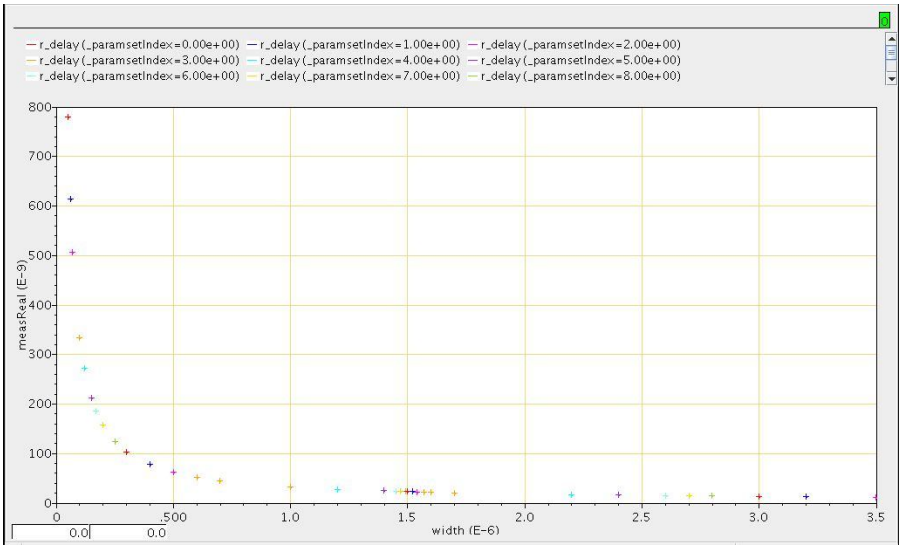


Figure 2: Rise Delay (ns) vs PMOS width (um)

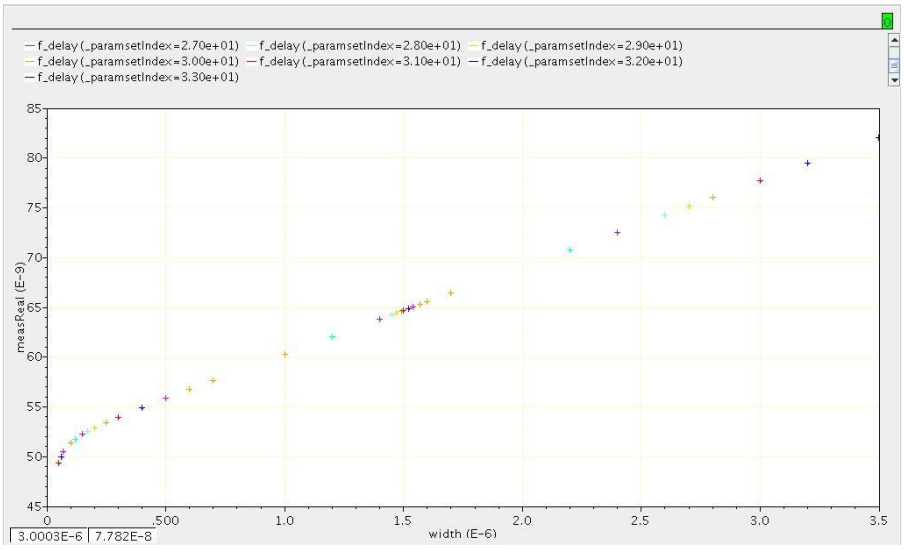


Figure 3: Fall Propagation Delay (ns) vs PMOS width (um)

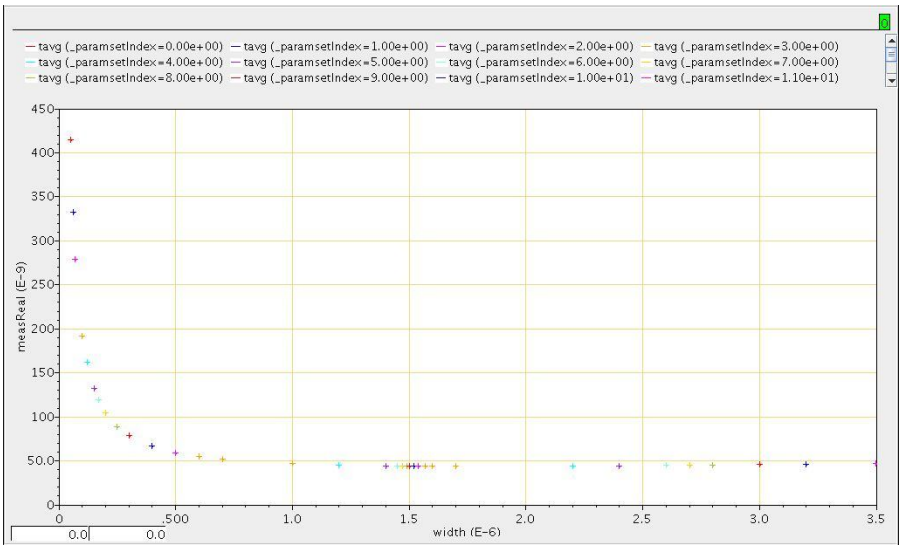


Figure 4: Average Propagation Delay (ns) vs PMOS width (um)

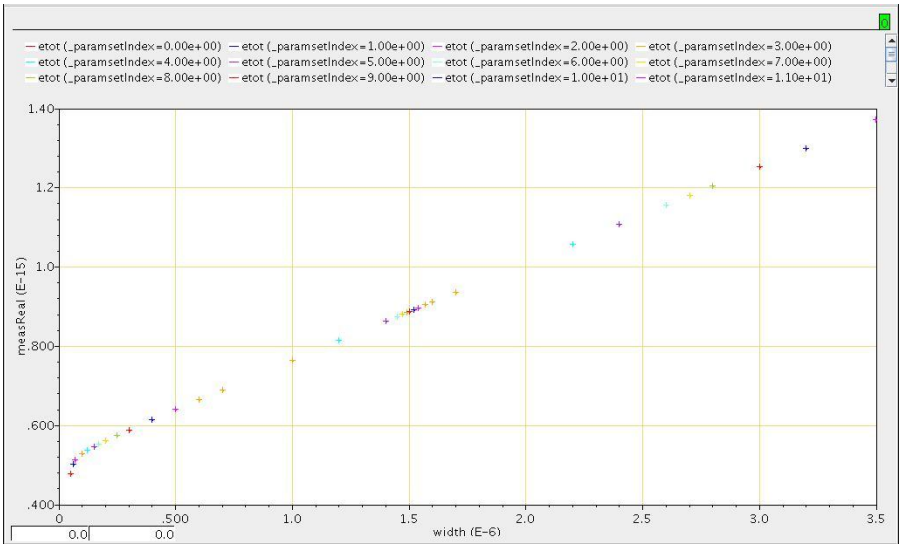


Figure 5: Energy per operation (10^-15J) vs PMOS width (um)

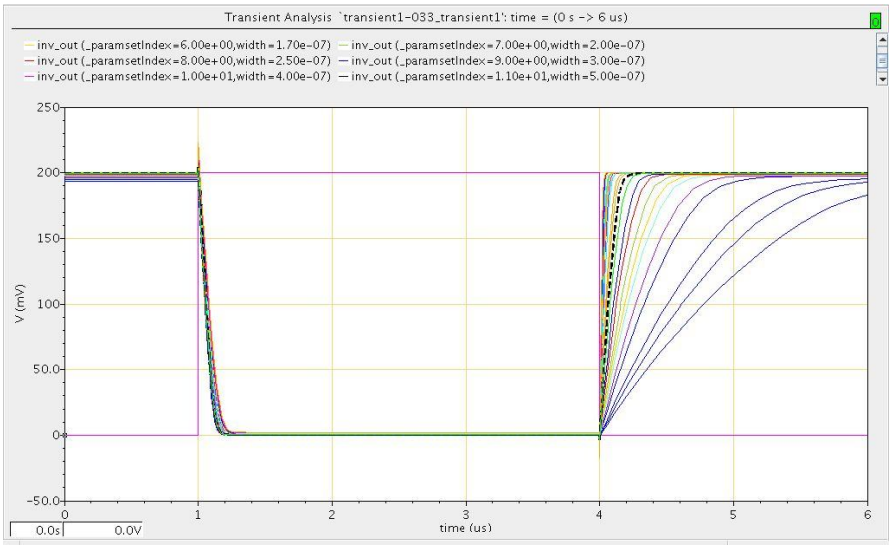


Figure 6: Transient Response of the inverter for different PMOS widths (dotted line corresponds to the PMOS width chosen (500nm)

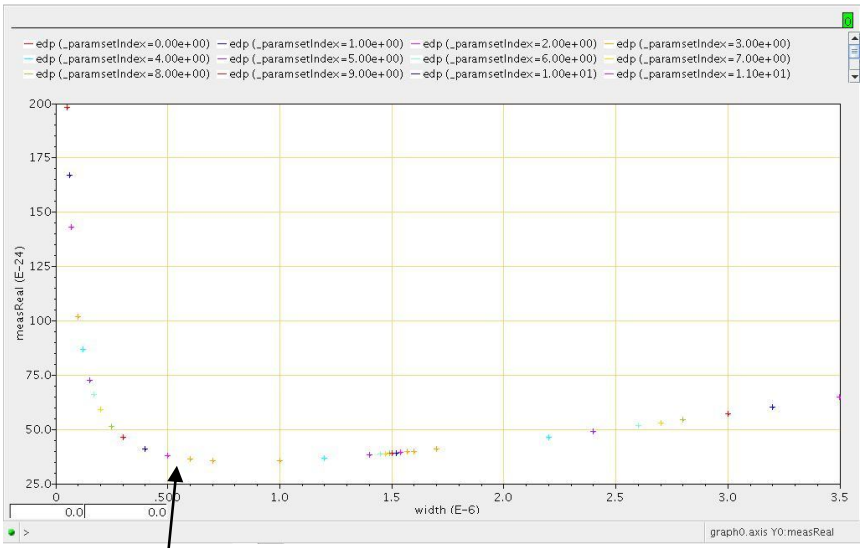


Figure 7: EDP(Energy delay product)(10^-24 Js) vs PMOS width(um)

Min EDP Range ~ 500-700nm

The above simulations were performed at Vdd=0.2V. From the plots, it can be seen that the EDP shows a minimum at PMOS widths in the range from 500-700nm (Figure 7). Taking Delay (from Figure 4) and area into consideration, the size of the PMOS for the baseline inverter is fixed at 500nm.

4.1.2 Choosing the operating Voltage

Choosing the operating voltage plays an important role for the design of the circuits in the sub threshold region. The following factors depend on the choice of value of the supply voltage:

a. The stability of operation(Signal integrity)
b. Achieving the target frequency
c. Providing considerable energy reduction when compared with the strong inversion region of operation.

4.1.2.1 Signal Integrity:

The baseline inverter was simulated for different values of voltages to consider the above factors into account and choose a suitable value of voltage.

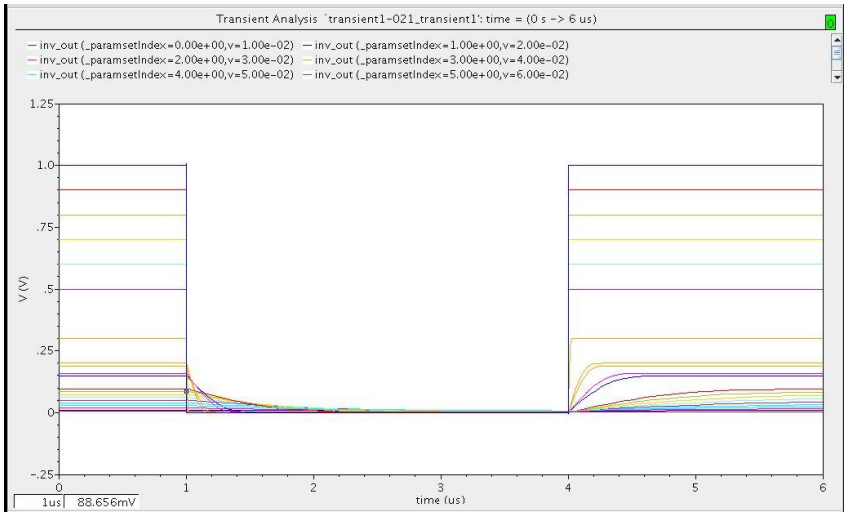


Figure 8: Transient response of the inverter for different Vdd (0.1-1.0V)

From Figure 9 below, there is a voltage drop of 5mV at Vdd=0.1V while Vdd=0.2V shows stable operation.

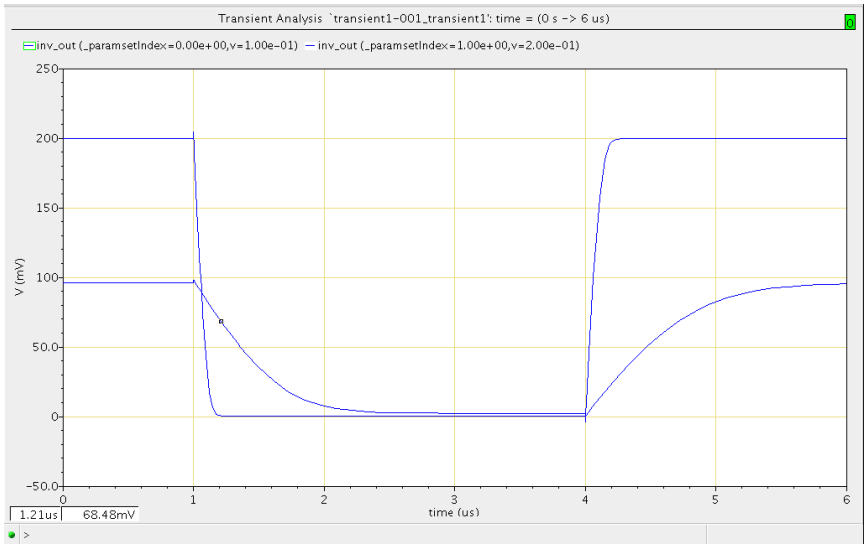


Figure 9: Transient response of INVX1 (Vdd=0.1V and Vdd=0.2V)

Operating at voltages below 0.2V leads to lesser stability in operation due to improved noise margins than the lower Vdd supplies.

4.1.2.2 Propagation Delay (Target Performance Metric)

The average propagation delay rises exponentially with decrease in Vdd in the sub-threshold region. Hence choosing the supply voltage to achieve the target operating frequency plays an important role.

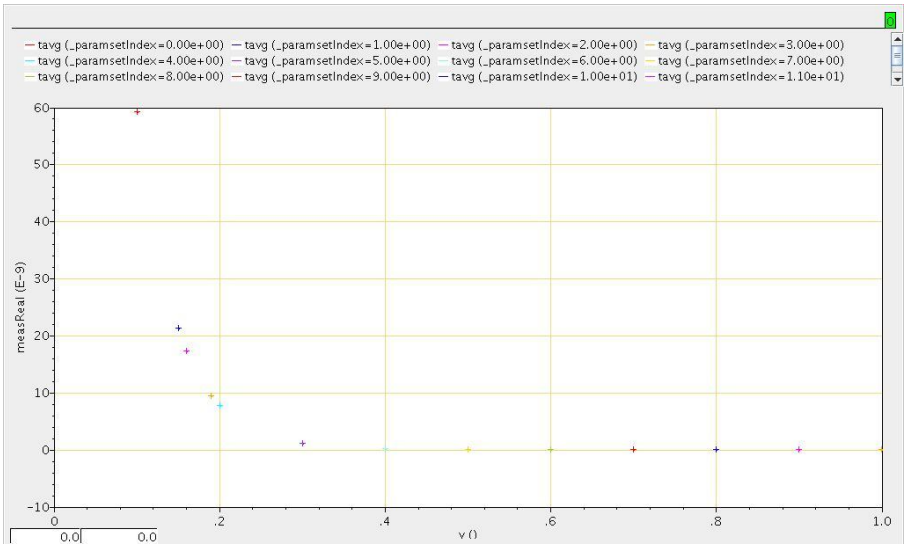


Figure 10: Average Delay (ns) of INVX1 vs Vdd (0.1 - 1V)

.

From the plots, it is evident that in the normal strong inversion region, the delay value decreases linearly with decrease in supply voltage.

4.1.2.3 Energy per Operation:

Since the main goal of the designs in sub-threshold region is to reduce the power consumption, the energy consumed per single operation was plotted across various voltages as seen in Figure 11. It is seen that the improvement in the energy consumption is pretty much flat at voltages below 0.2V while the delay degradation is huge at voltages below 0.2 V as seen in Figure 10.

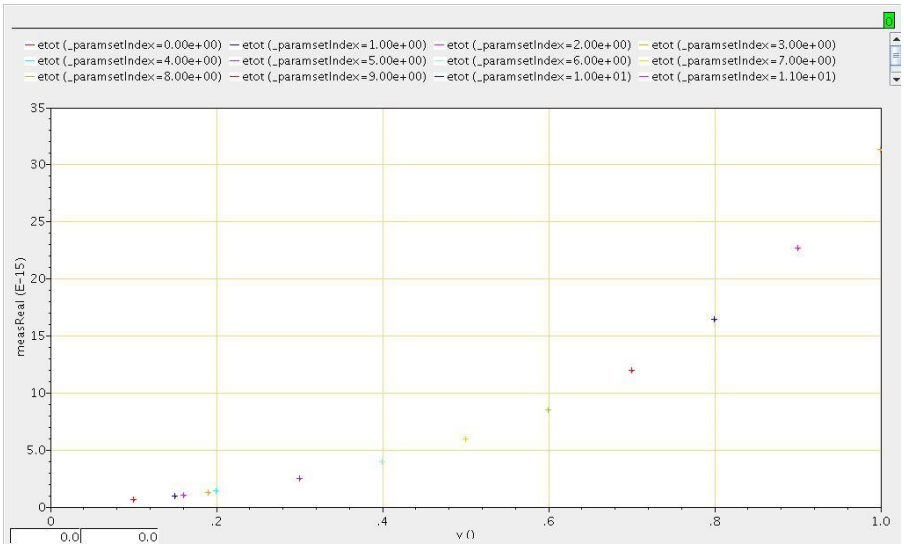


Figure 11: Energy (10^-15 J) per operation of INVX1 vs Vdd (0.1 - 1V)

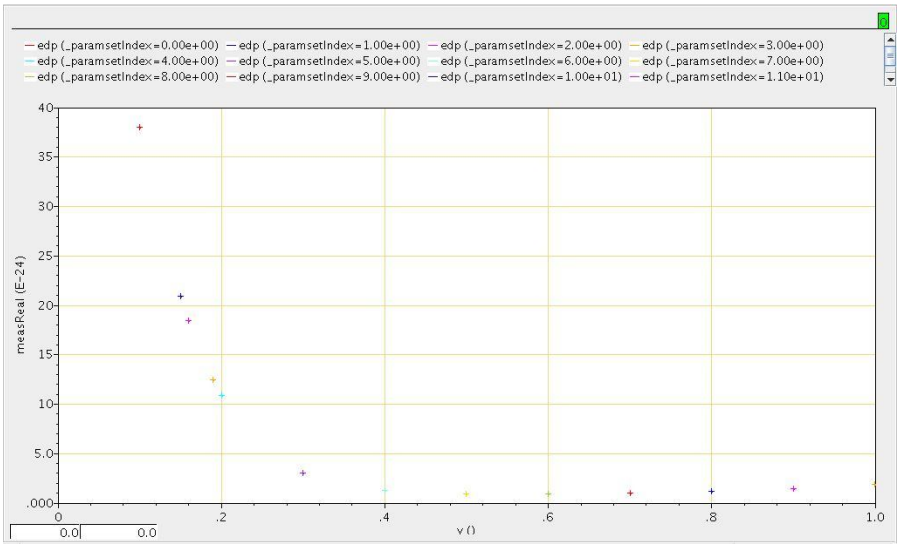


Figure 12: EDP (10^-24 Js) of INVX1 vs Vdd (V) (0.1V – 1V)

Plotting EDP vs supply voltage bolsters the choice of 0.2V as the supply voltage for standard cell design and characterisation to obtain the libraries.

Hence the following operating voltage and transistor sizes are used for the standard cell design and characterisation, which will form the basic blocks of the adder circuits to be designed.

Table 2: Chosen Design Parameters

Operating Voltage(V)	Size of NMOS_VTL(nm)	Size of PMOS_VTL(nm)
0.2	120	500

4.2 Physical Design of Standard Cells:

As mentioned previously, the flow intended to use just the 4 standard cells: INVX1, INVX4, NAND2X1 and NOR2X1 to design the adder. From the design charts and pre-layout simulation waveforms, it was decided to use a W/L ratio close to 4 for an operating supply voltage of 0.2V. So the NMOS length was set to 120nm and the PMOS length was chosen to be 500nm for the layout of the INVX1. Similarly, the NAND2X1 and NOR2X1 were designed with widths such that the equivalent rise and fall transitions would have the same drive strength as that of the baseline inverter INVX1.

Since the standard cells all have the same height to ensure that they can be abutted together and placed to share the power supply lines, it was quickly determined that the INVX4 width would be the critical one and would decide the height of the other cells.

The physical layouts of the Standard cells are shown in Figures 13, 14, 15 and 16 below.

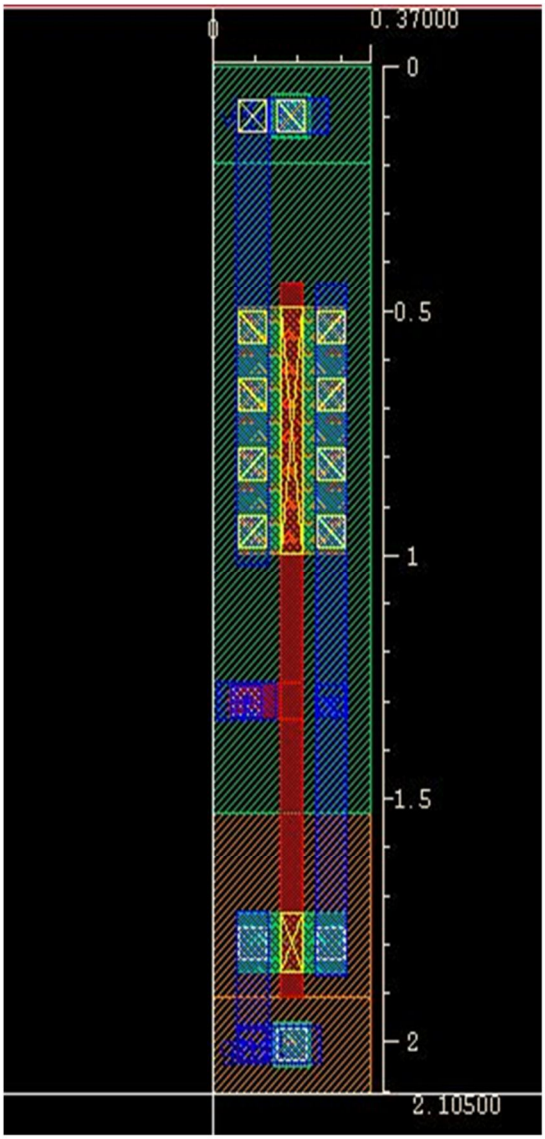


Figure 13: INVX1 Layout

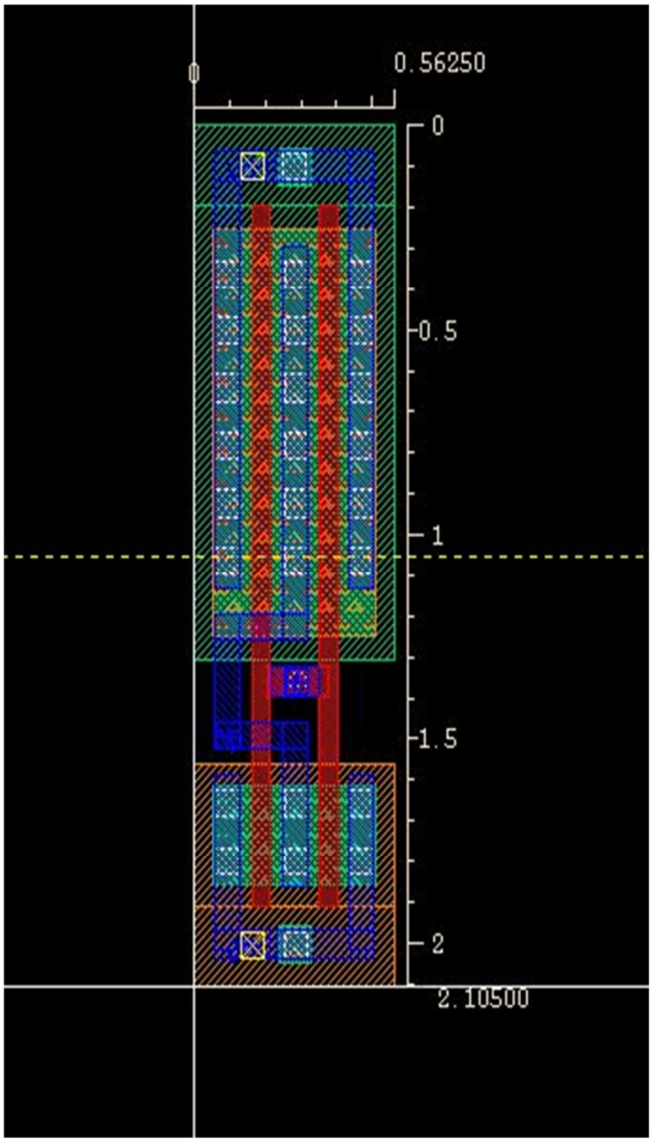


Figure 14: INVX4 Layout

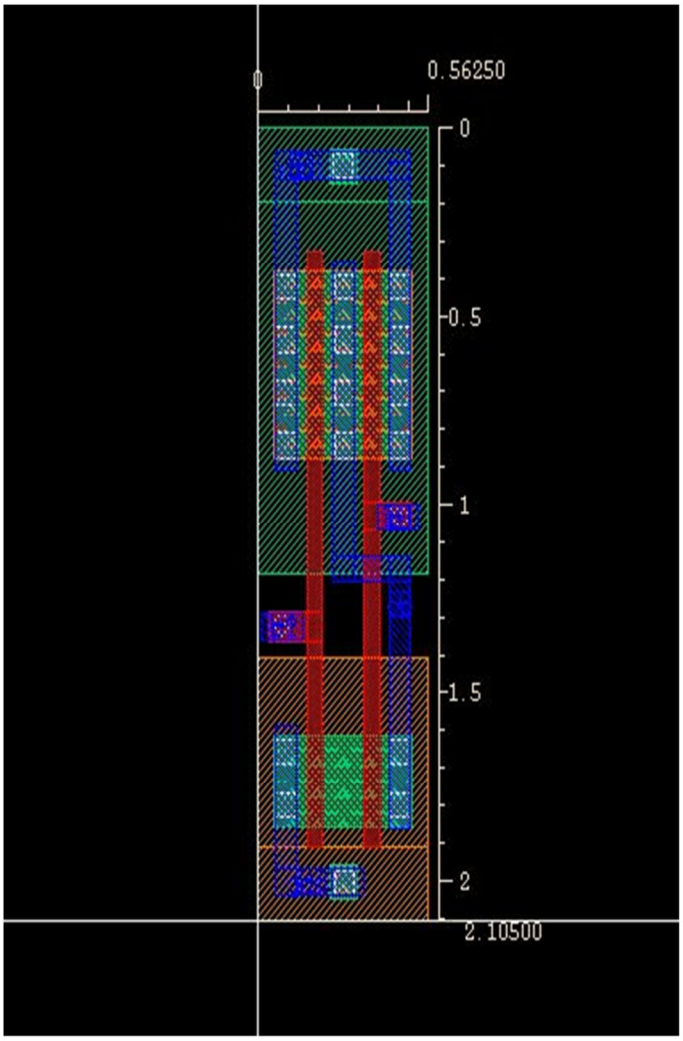


Figure 15: NAND2X1

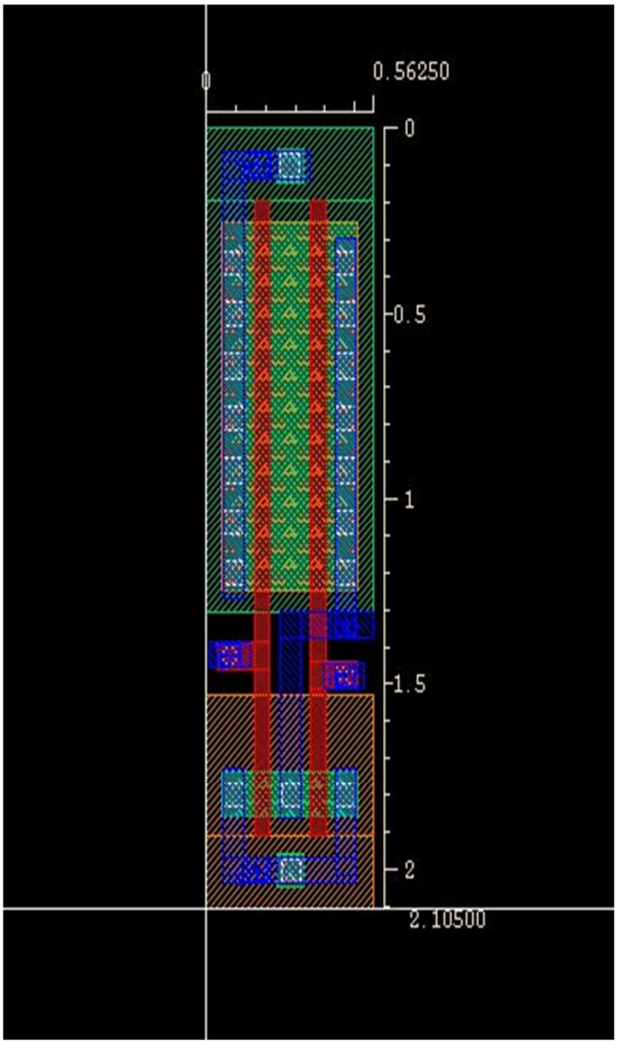


Figure 16: NOR2X1

4.2.1 Optimization Steps:

- Symmetric placement of the NMOS and PMOS wells and gate poly's in accordance with the Euler path analysis to ensure minimum poly length and no criss-cross of poly's interconnected by metal layers.
- Use of only metal 1 layer to interconnect pins and contacts. Care taken to ensure minimum length of the metal layer as well as appropriate separation from each other to reduce cross-talk while keeping the width of the cell small.
- Multiple contacts were used to connect the diffusion layers to input/output/power supply pins to reduce the effective resistance offered by them.

- Multi-finger transistor layout was used to reduce the effective height of the cell and keep the effective aspect ratio of the standard cell designed acceptable for floor planning (in accordance with the Shape Function)

The post-layout functional verification was done in HSPICE and the delay values were higher than the pre-layout simulation. Noise and glitches did not affect the signal integrity and the output values were settling to 0.2V during the rise transition and 0V during the fall transition (Figure 17).

4.3 Characterization

After performing the physical design, the standard cells were characterised for

1. Cell Rise Delay
2. Cell Fall Delay
3. Cell Rise Transition
4. Cell Fall Transition
5. Input Pin Capacitances
6. Cell Leakage Power
7. Cell Internal energy per transition
8. Cell Area.

HSPICE was used for the characterisation of the cells. The values generated from HSPICE were used to generate the logical library in the Synopsys Liberty Format (.lib).

This library will be further used for finding the critical path delay of the adder circuit designed to operate in sub threshold region. The library will also be used to perform peak power analysis using PrimeTime PX.

4.3.1 Rise/Fall Delay and Rise/Fall Transition

The standard cells were characterised for rise/fall delays and rise/fall transitions by varying the input pin transition values and output load capacitance values and generating the transient response in HSPICE for the standard cells.

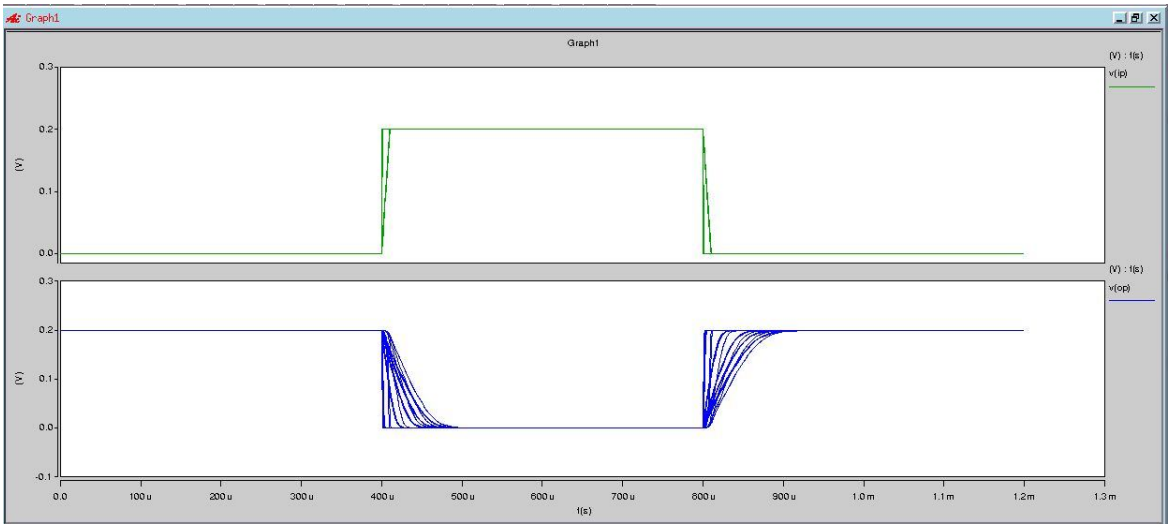


Figure 17: Post layout simulation for INVX1

index	load(F)	risefall(s)	r_delay(s)	f_delay(s)	r_transition(s	f_transition(s)
1	1.00E-13	1.00E-10	5.99E-07	5.33E-07	1.25E-06	1.06E-06
2	1.00E-13	1.00E-09	6.00E-07	5.34E-07	1.25E-06	1.06E-06
3	1.00E-13	1.00E-08	6.02E-07	5.36E-07	1.25E-06	1.06E-06
4	1.00E-13	1.00E-07	6.28E-07	5.60E-07	1.25E-06	1.06E-06
5	1.00E-13	1.00E-06	8.96E-07	8.25E-07	1.29E-06	1.11E-06
6	1.00E-13	1.00E-05	2.98E-06	2.66E-06	4.07E-06	4.05E-06
7	2.00E-13	1.00E-10	1.19E-06	1.06E-06	2.49E-06	2.10E-06
8	2.00E-13	1.00E-09	1.19E-06	1.06E-06	2.49E-06	2.10E-06
9	2.00E-13	1.00E-08	1.19E-06	1.06E-06	2.49E-06	2.10E-06
10	2.00E-13	1.00E-07	1.21E-06	1.09E-06	2.48E-06	2.10E-06
11	2.00E-13	1.00E-06	1.48E-06	1.35E-06	2.49E-06	2.10E-06
12	2.00E-13	1.00E-05	4.07E-06	3.78E-06	4.71E-06	4.59E-06
13	1.50E-12	1.00E-10	8.84E-06	7.86E-06	1.86E-05	1.57E-05
14	1.50E-12	1.00E-09	8.86E-06	7.85E-06	1.85E-05	1.56E-05
15	1.50E-12	1.00E-08	8.84E-06	7.87E-06	1.85E-05	1.57E-05
16	1.50E-12	1.00E-07	8.88E-06	7.89E-06	1.85E-05	1.57E-05
17	1.50E-12	1.00E-06	9.13E-06	8.14E-06	1.86E-05	1.57E-05
18	1.50E-12	1.00E-05	1.18E-05	1.08E-05	1.87E-05	1.59E-05
19	3.00E-12	1.00E-10	1.77E-05	1.57E-05	3.70E-05	3.13E-05
20	3.00E-12	1.00E-09	1.77E-05	1.57E-05	3.70E-05	3.13E-05

Figure 18: Sample table showing the characterised rise/fall delay and transition for INVX1

The following specifications are used for the definition of propagation delays and the transitions seen at the output pins.

Cell Rise Delay: 50% of VDD of the input to 50% of VDD of the rising output
Cell Fall Delay: 50% of VDD of the input to 50% of VDD of the falling output
Cell Rise Transition:10% of VDD of the rising output to 90% of VDD
Cell Fall Transition: 10% of VDD of the falling output to 90% of VDD

Similar simulations were performed for INVX4, NAND2X1 and NOR2X1. The simulation waveforms and sample characterisation tables are shown below.

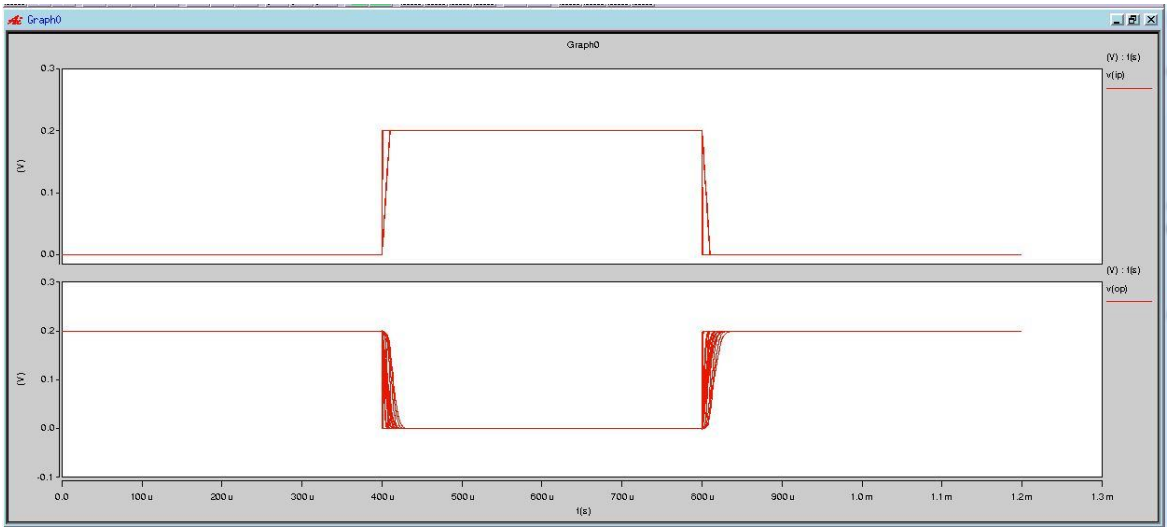


Figure 19: Post Layout Simulation INVX4

index	load(F)	risefall(s)	r_delay(s)	f_delay(s)	r_transition(s)	f_transition(s)
1	1.00E-13	1.00E-10	1.55E-07	1.33E-07	3.19E-07	2.60E-07
2	1.00E-13	1.00E-09	1.55E-07	1.34E-07	3.19E-07	2.61E-07
3	1.00E-13	1.00E-08	1.58E-07	1.36E-07	3.20E-07	2.60E-07
4	1.00E-13	1.00E-07	1.84E-07	1.61E-07	3.20E-07	2.60E-07
5	1.00E-13	1.00E-06	4.54E-07	4.19E-07	5.11E-07	4.79E-07
6	1.00E-13	1.00E-05	1.47E-06	1.04E-06	2.95E-06	2.96E-06
7	2.00E-13	1.00E-10	3.01E-07	2.58E-07	6.25E-07	5.09E-07
8	2.00E-13	1.00E-09	3.01E-07	2.59E-07	6.26E-07	5.10E-07
9	2.00E-13	1.00E-08	3.03E-07	2.61E-07	6.25E-07	5.10E-07
10	2.00E-13	1.00E-07	3.29E-07	2.86E-07	6.26E-07	5.10E-07
11	2.00E-13	1.00E-06	6.02E-07	5.54E-07	7.35E-07	6.44E-07
12	2.00E-13	1.00E-05	2.10E-06	1.69E-06	3.46E-06	3.47E-06
13	1.50E-12	1.00E-10	2.20E-06	1.89E-06	4.60E-06	3.75E-06
14	1.50E-12	1.00E-09	2.20E-06	1.88E-06	4.60E-06	3.75E-06
15	1.50E-12	1.00E-08	2.20E-06	1.89E-06	4.59E-06	3.76E-06
16	1.50E-12	1.00E-07	2.23E-06	1.91E-06	4.60E-06	3.75E-06
17	1.50E-12	1.00E-06	2.49E-06	2.17E-06	4.60E-06	3.75E-06
18	1.50E-12	1.00E-05	5.22E-06	4.86E-06	6.10E-06	5.53E-06
19	3.00E-12	1.00E-10	4.39E-06	3.76E-06	9.19E-06	7.49E-06

Figure 20: Sample table showing the characterised Rise/Fall Delay/Transition values for INVX4

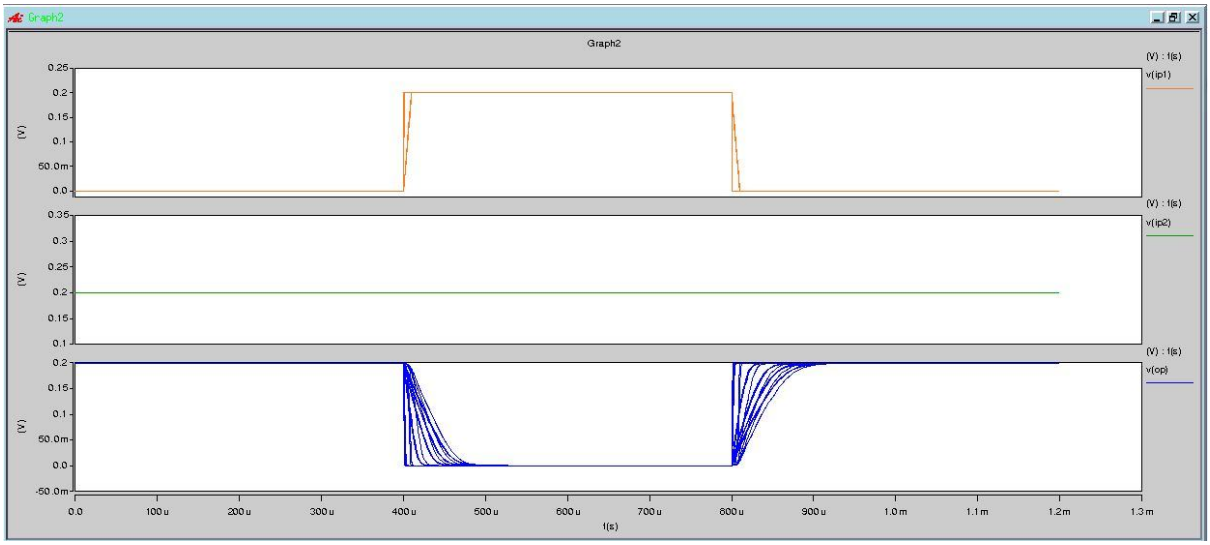


Figure 21: Post Layout Simulation NAND2X1 (IP1 → OP timing arc)

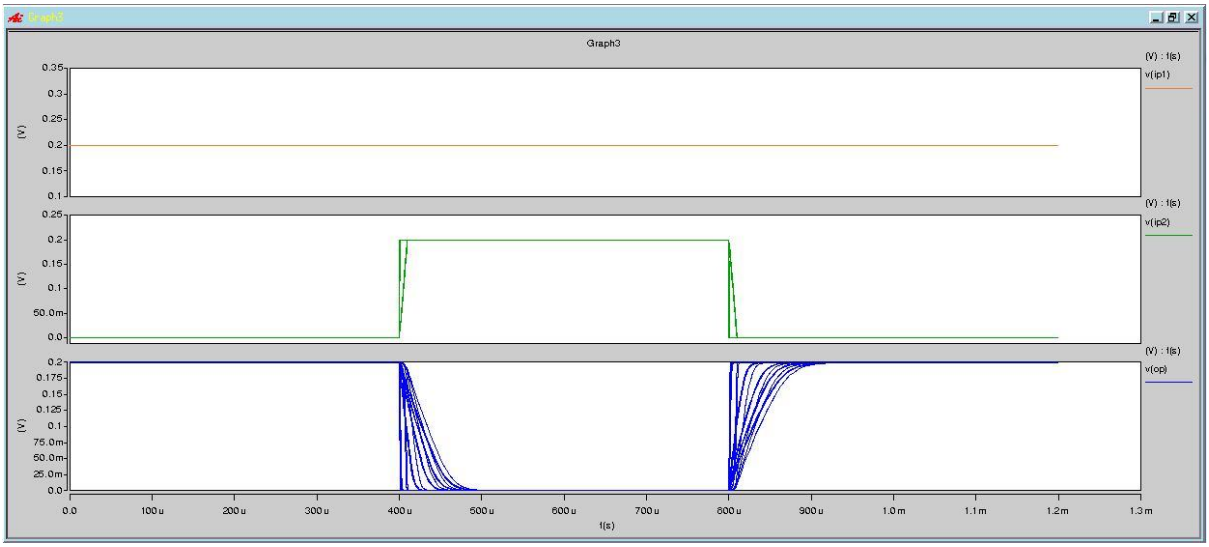


Figure 22: Post Layout Simulation NAND2X1 (IP2 → OP timing arc)

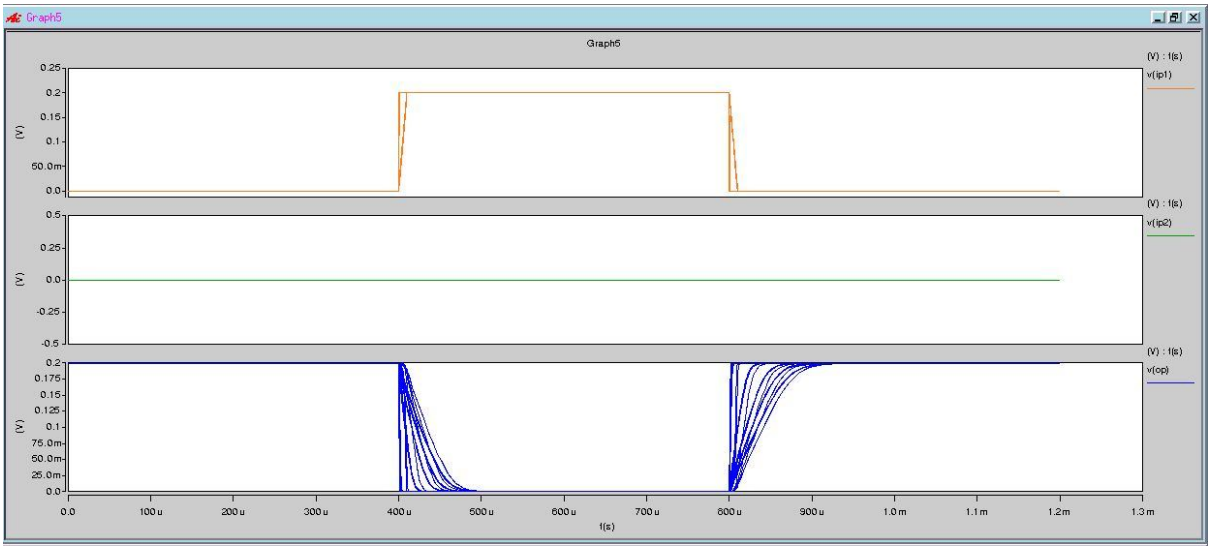


Figure 23: Post Layout Simulation NOR2X1 (IP1 → OP timing arc)

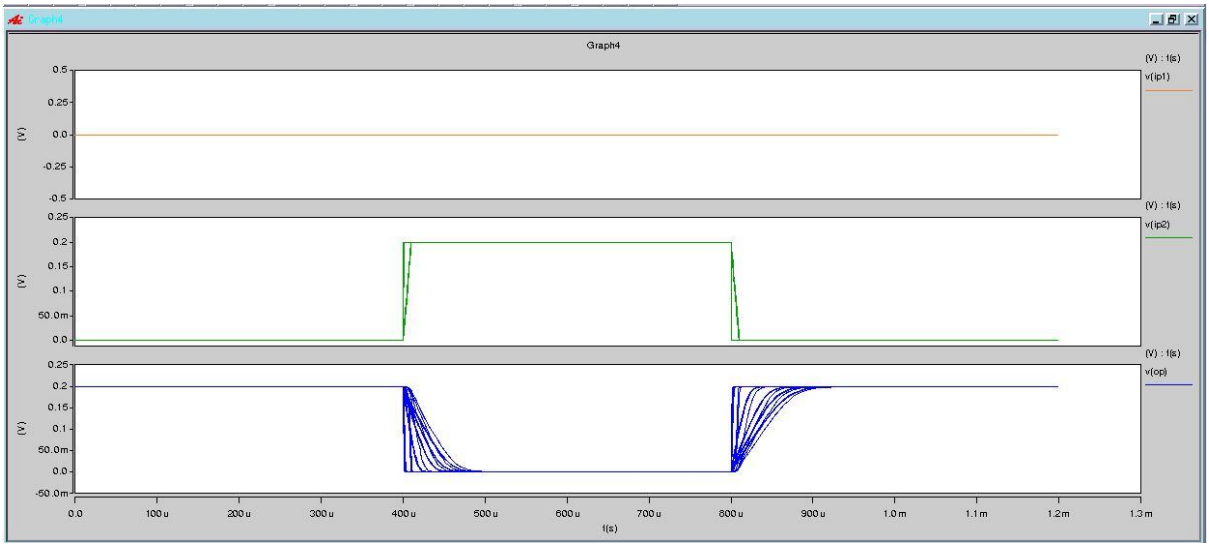


Figure 24: Post Layout Simulation NOR2X1 (IP2 → OP timing arc)

The detailed characterisation tables for delay/transitions are provided in the Appendix section.

4.3.2 Input Pin Capacitance

Post layout, the gate capacitances of the INVX1, INVX4, NAND2X1 and NOR2X1 were calculated using HSPICE and these values were used to generate the final .lib.
The capacitance values play a crucial role in the timing and power analysis of the adder circuitry. The appendix section gives the detailed .lib that was generated.

4.3.3 Power

The power dissipation of the cell can be divided into two main parts: static (leakage) power and dynamic power.

1) LEAKAGE POWER: The power dissipated when no switching activity occurs. This is mostly due to gate leakage current, junction leakage current and sub threshold conduction current when VGS = 0.

2) DYNAMIC POWER: This is the sum total of the power dissipated when switching activities occur and this power accounts for a major portion of the overall power dissipation. This category is further subdivided into 2 categories:

- Switching Power: This is the power dissipated due to the charging and discharging of the capacitors at the output node which consists of the C_L and the gate capacitances of the next stage that the cell drives.
- Internal Power: This is the part of dynamic energy which is dissipated by the cell in addition to the switching power. Physically, internal energy is dissipated, in pulses, due to short circuit conditions that occur during switching and due to charging/discharging of the internal capacitances of the cell itself.

The actual Synopsys model for power dissipation and the method of characterization that has been followed are along the lines of those given in [14].

4.3.3.1 Characterization for Cell Leakage Power:

HSPICE was used to characterise the cells for leakage power values. The state dependant leakage values were calculated as follows:

Table 3: Characterized Leakage Power for INVX1

Pstat0H(W)	Pstat1L(W)	Average Leakage Power(W)
3.638e-11	3.130e-11	3.384e-11

Pstat0h → corresponds to the leakage power consumed when the input pin (IP) of the INVX1 is at logic '0'

Pstat1L → corresponds to the leakage power consumed when the input pin (IP) of the INVX1 is at logic '1'

It is considered there is an equal probability for the pin IP to be at logic '0' or logic '1' and hence the average leakage power is the average of the Pstat0H and Pstat1L values.

Similarly, for a 2 input gate such as NAND2X1, there will be four states given as follows.

Table 4: Characterized Leakage Power for NAND2X1

Pstat00H(W)	Pstat01H(W)	Pstat10H(W)	Pstat11H(W)	Average Leakage Power(W)
3.195e-11	7.572e-11	6.449e-11	6.331e-11	5.887e-11

Pstat00H → corresponds to the leakage power consumed when the input pins (IP1, IP2) of the NAND2X1 are at logic ‘00’
Pstat01H → corresponds to the leakage power consumed when the input pins (IP1, IP2) of the NAND2X1 are at logic ‘01’
Pstat10H → corresponds to the leakage power consumed when the input pins (IP1, IP2) of the NAND2X1 are at logic ‘10’
Pstat11L → corresponds to the leakage power consumed when the input pins (IP1, IP2) of the NAND2X1 are at logic ‘11’

The probability of each state is taken as 0.25 to arrive at the average leakage power.

The HSPICE .sp scripts, the leakage power tables and the generated .lib are provided in the Appendix section.

4.3.3.2 Characterization for Internal Rise/Fall Energy Per Transition

During characterization, the energy values are defined in the library using any one of the following equations:

- internal rise energy = dynamic rise energy measured - CV^2, and
  internal fall energy = dynamic fall energy measured

- internal rise energy = dynamic rise energy measured - 1/2*CV^2, and
  internal fall energy = dynamic fall energy measured - 1/2 *CV^2
  where:

C is the capacitance of the load capacitor
V is the source voltage used during power characterization
CV^2 is the energy consumed by the load capacitor during the rise transition, on the output of the gate.

The latter method is widely used in the industry and hence this method was used to characterise the cell for internal rise/fall energy. The Tables and the .lib for the 4 standard cells INVX1, INVX4, NAND2X1 and NOR2X1 are provided in the Appendix section. The snippet of the INVX1 Table is shown below.

index	loadc	input slew	rise_switching_energy(J)	fall_switching_energy(J)	rise_dynamic_energy(J)	fall_dynamic_energy(J)	rise_internal_energy(nJ)	fall_internal_energy(nJ)
1	1.00E-13	1.00E-10	2.00E-15	2.00E-15	2.18E-15	2.21E-15	1.79E-07	2.08E-07
2	1.00E-13	1.00E-09	2.00E-15	2.00E-15	2.18E-15	2.21E-15	1.79E-07	2.07E-07
3	1.00E-13	1.00E-08	2.00E-15	2.00E-15	2.18E-15	2.21E-15	1.78E-07	2.08E-07
4	1.00E-13	5.00E-08	2.00E-15	2.00E-15	2.18E-15	2.20E-15	1.81E-07	2.04E-07
5	1.00E-13	1.00E-07	2.00E-15	2.00E-15	2.18E-15	2.21E-15	1.80E-07	2.05E-07
6	1.00E-13	1.00E-06	2.00E-15	2.00E-15	2.18E-15	2.20E-15	1.78E-07	1.99E-07
7	2.00E-13	1.00E-10	4.00E-15	4.00E-15	4.15E-15	4.19E-15	1.52E-07	1.93E-07
8	2.00E-13	1.00E-09	4.00E-15	4.00E-15	4.15E-15	4.19E-15	1.52E-07	1.92E-07
9	2.00E-13	1.00E-08	4.00E-15	4.00E-15	4.15E-15	4.19E-15	1.52E-07	1.91E-07
10	2.00E-13	5.00E-08	4.00E-15	4.00E-15	4.15E-15	4.19E-15	1.53E-07	1.93E-07
11	2.00E-13	1.00E-07	4.00E-15	4.00E-15	4.15E-15	4.20E-15	1.51E-07	1.97E-07
12	2.00E-13	1.00E-06	4.00E-15	4.00E-15	4.15E-15	4.19E-15	1.48E-07	1.85E-07

Figure 25: Sample Internal Energy Table for INVX1

4.4 Area

The areas of the cells were calculated post layout in Cadence Virtuoso Layout Editor and the values were entered in the .lib for reference.

Chapter 5: Results

The tables below show the final computed **values from post-layout simulation** for each of the standard cells that were to be used in the implementation of the adder architectures.

1) INVX1:

Table 5: Comparison of INVX1 performance parameters

Index	Vdd (V)	rise_delay (ns)	fall_delay (ns)	Avg_Delay (ns)	Total Energy (fJ)	EDP (Js)
1	0.2	59.9	53.3	**56.6**	**41.3**	2.34E-20
2	1	0.37	0.499	**0.435**	**1120**	4.88E-22

2) INVX4:

Table 6: Comparison of INVX4 performance parameters

Index	Vdd (V)	rise_delay (ns)	fall_delay (ns)	Avg_Delay (ns)	Total Energy (fJ)	EDP (Js)
1	0.2	15.5	13.3	**14.4**	**176**	2.54E-20
2	1	0.109	0.142	**0.125**	**9390**	1.18E-21

3) NAND2X1:

Table 7: Comparison of NAND2X1 performance parameters

Index	Vdd (V)	rise_delay (ns)	fall_delay (ns)	Avg_Delay (ns)	Total Energy (fJ)	EDP (Js)
1	0.2	60.4	55.7	**58.1**	**88.8**	5.16E-20
2	1	0.375	0.428	**0.402**	**4700**	1.89E-21

4) NOR2X1:

Table 8: Comparison of NOR2X1 performance parameters

Index	Vdd (V)	rise_delay (ns)	fall_delay (ns)	Avg_Delay (ns)	Total Energy (fJ)	EDP (Js)
1	0.2	71.2	55.0	**63.1**	**158**	9.99E-20
2	1	0.402	0.52	**0.461**	**3940**	1.82E-21

The parallel-prefix adder topologies were then constructed using these standard cells in the schematic editor and then taken through the entire design flow and the results of the comparison with the strong inversion region where the supply voltage is 1V is shown below.

Please find the detailed timing and power reports from which these values were derived in the Appendix section.

i) KOGGE STONE ADDER:

a) 8 bits:

Table 9: Comparison of the Kogge-Stone 8-bit adder performance parameters

Index	Supply Voltage Vdd (V)	Critical Path Delay	Average Power Consumption (W)	Frequency of Operation	Power Improvement Ratio
1	0.2	**3 µs**	**1.43E-8**	~333 kHz	310
2	1	**0.33 ns**	**4.441E-6**	~3 GHz	

b) 16 bits:

Table 10: Comparison of the Kogge-Stone 16-bit adder performance parameters

Index	Supply Voltage Vdd (V)	Critical Path dDelay	Average Power Consumption (W)	Frequency of Operation	Power Improvement Ratio
1	0.2	**3.5 µs**	**3.219E-8**	~285 kHz	282
2	1	**0.42 ns**	**9.06E-6**	~2.3 GHz	

ii) LADNER-FISCHER ADDER ARCHITECTURE:

a) 8 bits:

Table 11: Comparison of the Ladner-Fischer 8-bit adder performance parameters

Index	Supply Voltage Vdd (V)	Critical Path Delay	Average Power Consumption (W)	Frequency of Operation	Power Improvement Ratio
1	0.2	**3.3 µs**	**1.335E-8**	~300 kHz	312
2	1	**0.38 ns**	**4.159E-6**	~2.6 GHz	

b) 16 bits:

Table 12: Comparison of the Ladner-Fischer 16-bit adder performance parameters

Index	Supply Voltage Vdd (V)	Critical Path Delay	Average Power Consumption (W)	Frequency of Operation	Power Improvement Ratio
1	0.2	**4.1 µs**	**2.934E-8**	~245 kHz	282
2	1	**0.51 ns**	**8.275E-6**	~2 GHz	

Chapter 6: Conclusion

It can be seen from the result tables that the sub-threshold region of operation provides an improvement in power efficiency (and also consequently energy) by 10^2 orders of magnitude while allowing the circuits to operate at several 100's of kHz of operation. However, the increase in delay is roughly of the order of 10^3 and thus the applications using these power efficient circuits cannot be tailored for high speed simultaneously in advanced technology nodes (L < 50nm , VDD < 1V). Thus the EDP does not improve, as evident from the tables of the standard cells itself and consequently a trade-off exists between energy efficiency and performance. This is differing from our literature survey [2], [3] since the advancement in technology and scaling of supply voltages (while still ensuring strong inversion) has significantly improved speed and reduced power consumption already.

However, it is interesting to note that the power improvement ratio remains nearly the same for increase in the adder width. It also doesn't vary much for both Kogge-Stone and Ladner-Fischer adders even though they vastly vary in complexity and fan-out metrics.

In essence, the subthreshold region of operation for adders offers a potentially exciting region of research targeted at applications where energy is the primary concern and not performance. As seen, preliminary analysis with average power shows that there can be a significant improvement in the energy consumption if delays in the order of μs can be tolerated.

Appendix

A.1 Hspice Scripts:

The scripts used to obtain the rise and fall delay and transition values, power and leakage estimation are attached below. Please note that only the sample script used for NAND2X1 is attached herewith for each parameter and the scripts for the other cells are almost the same with variations in the number of input pins and the order of pin labels depending upon the *.pex.netlist file for each.

A.1.1 Output Delay and Transition (Rise and Fall): Shown Only For One Input

```
**********************************
* Post Layout simulation
* EE 382M-VLSI I Project
* SarveshGanesan/ Ankith G Shanthiraj
**********************************

.options CONVERGE=1 GMINDC=1.0000E-12 accurate list node

**********************************
* Models for 45nm
**********************************

.inc '$PDK_DIR/ncsu_basekit/models/hspice/tran_models/models_nom/NMOS_VTL.inc'
.inc '$PDK_DIR/ncsu_basekit/models/hspice/tran_models/models_nom/PMOS_VTL.inc'

**********************************
* Circuit Include
**********************************

.include "nand2x1_alt.pex.netlist"

**********************************

.global

***********change the slew**********
*.paramrisefall = 50p
**********************************

**********change the cap***********
capout OP 0 load
**********************************

*********Pin Specification**********
** Pin orders should be matched with 'inverter.pex.netlist' ****

x1 IP2 GND! IP1 OP VDD! nand2x1_alt

**********************************

VGND GND! 0 0
VVDD VDD! 0 0.2

.TEMP 25

VIN1 IP1 0 pwl (0 0 400000n 0 '400000n+risefall' 0.2 800000n 0.2 '800000n+risefall'
0 1200000n 0)
VIN2 IP2 0 0.2
```

```
******** Adjust stop time for the simulation to get the waveform you want
*************
*.tran 10p 1n
***********************************

.TRAN 0.01n 1200000n SWEEP DATA=D
.DATA D
+ load risefall
+ 0.1p 0.1n
+ 0.1p 1n
+ 0.1p 10n
+ 0.1p 100n
+ 0.1p 1000n
+ 0.1p 10000n

+ 0.2p 0.1n
+ 0.2p 1n
+ 0.2p 10n
+ 0.2p 100n
+ 0.2p 1000n
+ 0.2p 10000n

+ 1.5p 0.1n
+ 1.5p 1n
+ 1.5p 10n
+ 1.5p 100n
+ 1.5p 1000n
+ 1.5p 10000n

+ 3p 0.1n
+ 3p 1n
+ 3p 10n
+ 3p 100n
+ 3p 1000n
+ 3p 10000n

+ 4p 0.1n
+ 4p 1n
+ 4p 10n
+ 4p 100n
+ 4p 1000n
+ 4p 10000n

+ 5p 0.1n
+ 5p 1n
+ 5p 10n
+ 5p 100n
+ 5p 1000n
+ 5p 10000n

.ENDDATA


.MEASURE R_DELAY
+TRIG V(IP1) VAL=0.1 FALL=1
+TARG V(OP) VAL=0.1 RISE=1


.MEASURE F_DELAY
+TRIG V(IP1) VAL=0.1 RISE=1
+TARG V(OP) VAL=0.1 FALL=1


.MEASURE R_TRANSITION
+TRIG V(OP) VAL=0.02 RISE=1
+TARG V(OP) VAL=0.18 RISE=1
```

```
.MEASURE F_TRANSITION
+TRIG V(OP) VAL=0.18 FALL=1
+TARG V(OP) VAL=0.02 FALL=1

.MEAS rd_in_us PARAM = 'R_DELAY*1000000'
.MEAS fd_in_us PARAM = 'F_DELAY*1000000'
.MEAS rt_in_us PARAM = 'R_TRANSITION*1000000'
.MEAS ft_in_us PARAM = 'F_TRANSITION*1000000'
.op
.option post
.option measform=3

.END
```

A.1.2 Dynamic Power Computation:

```
**********************************
* Post Layout simulation
* EE 382M-VLSI I Project
* SarveshGanesan/ Ankith G Shanthiraj
**********************************

.options CONVERGE=1 GMINDC=1.0000E-12 accurate list node

**********************************
* Models for 45nm
**********************************

.inc '$PDK_DIR/ncsu_basekit/models/hspice/tran_models/models_nom/NMOS_VTL.inc'
.inc '$PDK_DIR/ncsu_basekit/models/hspice/tran_models/models_nom/PMOS_VTL.inc'

**********************************
* Circuit Include
**********************************

.include "nand2x1_alt.pex.netlist"

**********************************

.global

***********change the slew**********
.paramrisefall = 0.1n
**********************************

**********change the cap***********
*capout OP 0 10p
**********************************

*********Pin Specification**********
** Pin orders should be matched with 'inverter.pex.netlist' ****

x1 IP2 GND! IP1 OP VDD! nand2x1_alt

**********************************

VGND GND! 0 0
VVDD VDD! 0 0.2

.TEMP 25


.paramvspl='0.2v'
vddddgndvspl
xhnd3buf1a  ddgnd ip1  ip1a dd nand2x1_alt
xhnd3buf1b  ddgnd ip1a  ip1b dd nand2x1_alt
xhnd3buf2a  ip2gnddd  ip2a dd nand2x1_alt
```

```
xhnd3buf2b  ip2agnd d  ip2b dd nand2x1_alt
xload1  ip2bgnd  ip1b  oplddd nand2x1_alt
xeval  ip2bgnd ip1b  opevaldd nand2x1_alt
.paramloadc='0fF'
cloadopevalgndloadc
*vip1 IP1 gndpwl (0ns vspl 0.001u 0 5u 0 5.001u vspl 30u vspl)
*vip2 IP2 gndpwl (0ns vspl 10u vspl 10.001u 0 15u 0 15.001u vspl 30u vspl)
vip1 IP1 gndpwl (0u vspl '0u+risefall' 0 5u 0 '5u+risefall' vspl 30u vspl)
vip2 IP2 gndpwl (0u vspl 10u vspl '10u+risefall' 0 15u 0 '15u+risefall' vspl 30u
vspl)

.measure eswriseparam='0.5*loadc*vspl*vspl'
.measure eswfallparam='eswrise'
** Measurement of ip1 -> op energies
.measure edynrise1 integral p(xeval) from=5us to=10us
.measure edynfall1 integral p(xeval) from=0us to=5us
.measure eintrise1 param='(edynrise1-eswrise)*1000000000'
.measure eintfall1 param='(edynfall1-eswfall)*1000000000'


** Measurement of ip2 -> op energies
.measure edynrise2 integral p(xeval) from=15us to=20us
.measure edynfall2 integral p(xeval) from=10us to=15us
.measure eintrise2 param='(edynrise2-eswrise)*1000000000'
.measure eintfall2 param='(edynfall2-eswfall)*1000000000'

.measure eintriserparam='(eintrise1+eintrise2)/2.0'
.measure eintfallerparam='(eintfall1+eintfall2)/2.0'
** Finding the relative portions of each type of energy

.op
.option post nomod accurate
.option converge=1 gmindc=1e-12
.tran 0.1ns 30us SWEEP DATA=D
.DATA D
+ loadcrisefall
+ 0.1p 0.1n
+ 0.1p 1n
+ 0.1p 10n
+ 0.1p 50n
+ 0.1p 100n
+ 0.1p 1000n

+ 0.2p 0.1n
+ 0.2p 1n
+ 0.2p 10n
+ 0.2p 50n
+ 0.2p 100n
+ 0.2p 1000n

+ 1.5p 0.1n
+ 1.5p 1n
+ 1.5p 10n
+ 1.5p 50n
+ 1.5p 100n
+ 1.5p 1000n

+ 3p 0.1n
+ 3p 1n
+ 3p 10n
+ 3p 50n
+ 3p 100n
+ 3p 1000n

+ 4p 0.1n
+ 4p 1n
+ 4p 10n
+ 4p 50n
```

```
+ 4p 100n
+ 4p 1000n

+ 5p 0.1n
+ 5p 1n
+ 5p 10n
+ 5p 50n
+ 5p 100n
+ 5p 1000n

.ENDDATA
.option post
.option measform=3
.end



*.alter 1: for 25fF load:
*.paramloadc='25fF'
*.alter 2: for 50fF load:
*.paramloadc='50fF'
*.alter 3: for 75fF load:
*.paramloadc='75fF'
*.alter 4: for 100fF load:
*.paramloadc='100fF'
*.alter 5: for 150fF load:
*.paramloadc='150fF'
*.alter 6: for 250fF load:
*.paramloadc='250fF'
*.alter 7: for 500fF load:
*.paramloadc='500fF'
*.end
```

A.1.3 Leakage Power (Static Power Dissipation)

```
***********************************
* Post Layout simulation
* EE 382M-VLSI I Project
* SarveshGanesan/ Ankitn G Shanthiraj
***********************************

.options CONVERGE=1 GMINDC=1.0000E-12 accurate list node

***********************************
* Models for 45nm
***********************************

.inc '$PDK_DIR/ncsu_basekit/models/hspice/tran_models/models_nom/NMOS_VTL.inc'
.inc '$PDK_DIR/ncsu_basekit/models/hspice/tran_models/models_nom/PMOS_VTL.inc'

***********************************
* Circuit Include
***********************************

.include "nand2x1_alt.pex.netlist"

***********************************

.global

***********change the slew**********
.paramrisefall = 0.1n
***********************************

**********change the cap***********
capout OP 0 10p
```

```
**********************************

*********Pin Specification**********
** Pin orders should be matched with 'inverter.pex.netlist' ****

x1 IP2 GND! IP1 OP VDD! nand2x1_alt

**********************************

VGND GND! 0 0
VVDD VDD! 0 0.2

.TEMP 25

VIN1 IP1 0 pwl (0 0 400000n 0 '400000n+risefall' 0.2 800000n 0.2 '800000n+risefall'
0 1200000n 0)
VIN2 IP2 0 0.2

.paramspl='0.2v' ** Use 3.3V Power Supply
vspstatspstatgndspl
xstat00hgndgndgnd op00h spstat nand2x1_alt ** For input = 00
xstat01hspstatgndgnd op01h spstat nand2x1_alt ** For input = 01
xstat10hgndgndspstat op10h spstat nand2x1_alt ** For input = 10
xstat11lspstatgndspstat op11l spstat nand2x1_alt ** For input = 11
.measure pstat00h avgp(xstat00h) from=400000ns to=800000ns ** These time intervals
.measure pstat01h avgp(xstat01h) from=400000ns to=800000ns ** are arbitrary for
.measure pstat10h avgp(xstat10h) from=400000ns to=800000ns ** combinational cells
.measure pstat11l avgp(xstat11l) from=400000ns to=800000ns ** here we use 1 ns
.measure pstat_avparam='(pstat00h+pstat01h+pstat10h+pstat11l)/4'
.measure pstat_avlparam='(pstat00h+pstat01h+pstat10h)/3'
.measure pstat_avhparam='pstat11l'
.tran 0.01ns 1200000ns

.END
```

A.1.4 Pin Capacitances Estimation:

```
**********************************
* Post Layout simulation
* EE 382M-VLSI I Project
* Ankith G Shanthiraj/ Sarvesh Ganesan
**********************************

.options CONVERGE=1 GMINDC=1.0000E-12 accurate list node

**********************************
* Models for 45nm
**********************************
.inc '$PDK_DIR/ncsu_basekit/models/hspice/tran_models/models_nom/NMOS_VTL.inc'
.inc '$PDK_DIR/ncsu_basekit/models/hspice/tran_models/models_nom/PMOS_VTL.inc'

**********************************
* Circuit Include
**********************************

.include "nand2x1_alt.pex.netlist"

**********************************

.global

***********change the slew**********
.paramrisefall = 50p
**********************************

**********change the cap************
```

```
*capout OP 0 load
**********************************

*********Pin Specification**********
** Pin orders should be matched with 'inverter.pex.netlist' ****

x1 IP2 GND! IP1 OP VDD! nand2x1_alt

**********************************

VGND GND! 0 0
VVDD VDD! 0 0.2

.TEMP 25

VIN1 IP2 0 pwl (0 0 400000n 0 '400000n+risefall' 0.2 800000n 0.2 '800000n+risefall'
0 1200000n 0)
VIN2 IP1 0 0.2
******** Adjust stop time for the simulation to get the waveform you want
*************
*.tran 10p 1n
**********************************
.TRAN 0.01n 1200000n

.measure qin1 integral i(VIN2) from 40000n to 45000n
.measure cin1 param= 'abs(qin1/0.2)'

.measure qin2 integral i(VIN2) from 80000n to 85000n
.measure cin2 param= 'abs(qin2/0.2)'


.op
.option post
.option measform=3

.END
```

A.2. Characterization Information Generated

A.2.1 INVX1:

$DATA1 SOURCE='HSPICE' VERSION='E-2010.12-SP2 32-BIT'										
$OPTION MEASFORM=3										
.TITLE '**********'										
index	load(F)	risefall(s)	r_delay(s)	f_delay(s)	r_transitic	f_transitic	rd_in_us	fd_in_us	rt_in_us	ft_in_us
1	1.00E-13	1.00E-10	5.99E-07	5.33E-07	1.25E-06	1.06E-06	0.5989	0.5328	1.2515	1.0576
2	1.00E-13	1.00E-09	6.00E-07	5.34E-07	1.25E-06	1.06E-06	0.5997	0.5337	1.2496	1.0575
3	1.00E-13	1.00E-08	6.02E-07	5.36E-07	1.25E-06	1.06E-06	0.6019	0.5358	1.2468	1.0567
4	1.00E-13	1.00E-07	6.28E-07	5.60E-07	1.25E-06	1.06E-06	0.6276	0.5603	1.2506	1.0551
5	1.00E-13	1.00E-06	8.96E-07	8.25E-07	1.29E-06	1.11E-06	0.8958	0.8251	1.2881	1.1055
6	1.00E-13	1.00E-05	2.98E-06	2.66E-06	4.07E-06	4.05E-06	2.9771	2.6591	4.0651	4.0503
7	2.00E-13	1.00E-10	1.19E-06	1.06E-06	2.49E-06	2.10E-06	1.1882	1.0556	2.4852	2.0967
8	2.00E-13	1.00E-09	1.19E-06	1.06E-06	2.49E-06	2.10E-06	1.1898	1.058	2.4862	2.1022
9	2.00E-13	1.00E-08	1.19E-06	1.06E-06	2.49E-06	2.10E-06	1.1907	1.0595	2.4885	2.1007
10	2.00E-13	1.00E-07	1.21E-06	1.09E-06	2.48E-06	2.10E-06	1.2141	1.0849	2.4799	2.101
11	2.00E-13	1.00E-06	1.48E-06	1.35E-06	2.49E-06	2.10E-06	1.4809	1.3449	2.4871	2.104
12	2.00E-13	1.00E-05	4.07E-06	3.78E-06	4.71E-06	4.59E-06	4.0741	3.7833	4.7129	4.5912
13	1.50E-12	1.00E-10	8.84E-06	7.86E-06	1.86E-05	1.57E-05	8.8428	7.8631	18.5684	15.6524
14	1.50E-12	1.00E-09	8.86E-06	7.85E-06	1.85E-05	1.56E-05	8.8601	7.8544	18.5031	15.6405
15	1.50E-12	1.00E-08	8.84E-06	7.87E-06	1.85E-05	1.57E-05	8.8431	7.8718	18.492	15.6778
16	1.50E-12	1.00E-07	8.88E-06	7.89E-06	1.85E-05	1.57E-05	8.8756	7.8924	18.4882	15.6698
17	1.50E-12	1.00E-06	9.13E-06	8.14E-06	1.86E-05	1.57E-05	9.1275	8.1347	18.5651	15.6754
18	1.50E-12	1.00E-05	1.18E-05	1.08E-05	1.87E-05	1.59E-05	11.7904	10.7808	18.6495	15.86
19	3.00E-12	1.00E-10	1.77E-05	1.57E-05	3.70E-05	3.13E-05	17.7007	15.7121	37.0426	31.2665
20	3.00E-12	1.00E-09	1.77E-05	1.57E-05	3.70E-05	3.13E-05	17.7035	15.7096	37.0013	31.3154
21	3.00E-12	1.00E-08	1.77E-05	1.57E-05	3.70E-05	3.13E-05	17.7143	15.7128	36.9986	31.2945
22	3.00E-12	1.00E-07	1.77E-05	1.57E-05	3.70E-05	3.13E-05	17.7081	15.7345	37.0318	31.3299
23	3.00E-12	1.00E-06	1.80E-05	1.60E-05	3.71E-05	3.13E-05	17.9851	16.0093	37.0744	31.3421
24	3.00E-12	1.00E-05	2.06E-05	1.86E-05	3.70E-05	3.14E-05	20.5668	18.5947	36.9866	31.3574
25	4.00E-12	1.00E-10	2.36E-05	2.09E-05	4.94E-05	4.17E-05	23.6008	20.9329	49.3608	41.6832
26	4.00E-12	1.00E-09	2.36E-05	2.10E-05	4.94E-05	4.18E-05	23.6094	20.9838	49.3844	41.7933
27	4.00E-12	1.00E-08	2.36E-05	2.09E-05	4.94E-05	4.18E-05	23.5946	20.9373	49.375	41.7458
28	4.00E-12	1.00E-07	2.36E-05	2.10E-05	4.93E-05	4.18E-05	23.5859	20.9927	49.281	41.7865
29	4.00E-12	1.00E-06	2.39E-05	2.12E-05	4.95E-05	4.17E-05	23.8528	21.1906	49.4806	41.6744
30	4.00E-12	1.00E-05	2.65E-05	2.38E-05	4.94E-05	4.17E-05	26.4527	23.7584	49.4204	41.6976
31	5.00E-12	1.00E-10	2.95E-05	2.62E-05	6.17E-05	5.21E-05	29.4938	26.1725	61.7279	52.136
32	5.00E-12	1.00E-09	2.95E-05	2.62E-05	6.17E-05	5.21E-05	29.4678	26.1654	61.7079	52.1189
33	5.00E-12	1.00E-08	2.95E-05	2.62E-05	6.17E-05	5.22E-05	29.4543	26.2019	61.6734	52.2307
34	5.00E-12	1.00E-07	2.95E-05	2.62E-05	6.16E-05	5.22E-05	29.5072	26.2387	61.5987	52.2066
35	5.00E-12	1.00E-06	2.97E-05	2.65E-05	6.17E-05	5.22E-05	29.744	26.4624	61.706	52.2171
36	5.00E-12	1.00E-05	3.23E-05	2.90E-05	6.17E-05	5.22E-05	32.3421	29.0311	61.6678	52.2206

Fig 26 : Output Delay and Transition Values

$DATA1 SOURCE='HSPICE' VERSION='E-2010.12-SP2 32-BIT'								
$OPTION MEASFORM=3								
.TITLE '**********'								
index	loadc	input slew	rise_switching_energy(J)	fall_switching_energy(J)	rise_dynamic_energy(J)	fall_dynamic_energy(J)	rise_internal_energy(nJ)	fall_internal_energy(nJ)
1	1.00E-13	1.00E-10	2.00E-15	2.00E-15	2.18E-15	2.21E-15	1.79E-07	2.08E-07
2	1.00E-13	1.00E-09	2.00E-15	2.00E-15	2.18E-15	2.21E-15	1.79E-07	2.07E-07
3	1.00E-13	1.00E-08	2.00E-15	2.00E-15	2.18E-15	2.21E-15	1.78E-07	2.08E-07
4	1.00E-13	5.00E-08	2.00E-15	2.00E-15	2.18E-15	2.20E-15	1.81E-07	2.04E-07
5	1.00E-13	1.00E-07	2.00E-15	2.00E-15	2.18E-15	2.21E-15	1.80E-07	2.05E-07
6	1.00E-13	1.00E-06	2.00E-15	2.00E-15	2.18E-15	2.20E-15	1.78E-07	1.99E-07
7	2.00E-13	1.00E-10	4.00E-15	4.00E-15	4.15E-15	4.19E-15	1.52E-07	1.93E-07
8	2.00E-13	1.00E-09	4.00E-15	4.00E-15	4.15E-15	4.19E-15	1.52E-07	1.92E-07
9	2.00E-13	1.00E-08	4.00E-15	4.00E-15	4.15E-15	4.19E-15	1.52E-07	1.91E-07
10	2.00E-13	5.00E-08	4.00E-15	4.00E-15	4.15E-15	4.19E-15	1.53E-07	1.93E-07
11	2.00E-13	1.00E-07	4.00E-15	4.00E-15	4.15E-15	4.20E-15	1.51E-07	1.97E-07
12	2.00E-13	1.00E-06	4.00E-15	4.00E-15	4.15E-15	4.19E-15	1.48E-07	1.85E-07
13	1.50E-12	1.00E-10	3.00E-14	3.00E-14	2.57E-15	1.53E-14	2.74E-05	-1.47E-05
14	1.50E-12	1.00E-09	3.00E-14	3.00E-14	2.57E-15	1.53E-14	2.74E-05	-1.47E-05
15	1.50E-12	1.00E-08	3.00E-14	3.00E-14	2.59E-15	1.53E-14	2.74E-05	-1.48E-05
16	1.50E-12	5.00E-08	3.00E-14	3.00E-14	2.65E-15	1.52E-14	2.74E-05	-1.48E-05
17	1.50E-12	1.00E-07	3.00E-14	3.00E-14	2.73E-15	1.51E-14	2.73E-05	-1.49E-05
18	1.50E-12	1.00E-06	3.00E-14	3.00E-14	3.76E-15	1.37E-14	2.62E-05	-1.64E-05
19	3.00E-12	1.00E-10	6.00E-14	6.00E-14	1.31E-15	1.73E-14	5.87E-05	-4.27E-05
20	3.00E-12	1.00E-09	6.00E-14	6.00E-14	1.31E-15	1.73E-14	5.87E-05	-4.27E-05
21	3.00E-12	1.00E-08	6.00E-14	6.00E-14	1.33E-15	1.73E-14	5.87E-05	-4.27E-05
22	3.00E-12	5.00E-08	6.00E-14	6.00E-14	1.42E-15	1.72E-14	5.86E-05	-4.28E-05
23	3.00E-12	1.00E-07	6.00E-14	6.00E-14	1.54E-15	1.71E-14	5.85E-05	-4.29E-05
24	3.00E-12	1.00E-06	6.00E-14	6.00E-14	3.00E-15	1.52E-14	5.70E-05	-4.48E-05
25	4.00E-12	1.00E-10	8.00E-14	8.00E-14	9.83E-16	1.79E-14	7.90E-05	-6.21E-05
26	4.00E-12	1.00E-09	8.00E-14	8.00E-14	9.86E-16	1.79E-14	7.90E-05	-6.21E-05
27	4.00E-12	1.00E-08	8.00E-14	8.00E-14	1.01E-15	1.78E-14	7.90E-05	-6.22E-05
28	4.00E-12	5.00E-08	8.00E-14	8.00E-14	1.11E-15	1.77E-14	7.89E-05	-6.23E-05
29	4.00E-12	1.00E-07	8.00E-14	8.00E-14	1.23E-15	1.76E-14	7.88E-05	-6.24E-05
30	4.00E-12	1.00E-06	8.00E-14	8.00E-14	2.82E-15	1.56E-14	7.72E-05	-6.44E-05
31	5.00E-12	1.00E-10	1.00E-13	1.00E-13	7.92E-16	1.82E-14	9.92E-05	-8.18E-05
32	5.00E-12	1.00E-09	1.00E-13	1.00E-13	7.94E-16	1.82E-14	9.92E-05	-8.18E-05
33	5.00E-12	1.00E-08	1.00E-13	1.00E-13	8.17E-16	1.82E-14	9.92E-05	-8.18E-05
34	5.00E-12	5.00E-08	1.00E-13	1.00E-13	9.20E-16	1.81E-14	9.91E-05	-8.19E-05
35	5.00E-12	1.00E-07	1.00E-13	1.00E-13	1.05E-15	1.80E-14	9.90E-05	-8.21E-05
36	5.00E-12	1.00E-06	1.00E-13	1.00E-13	2.72E-15	1.59E-14	9.73E-05	-8.41E-05

Fig 27 : Dynamic Power and Internal Energy Computation Tables

A.2.2 INVX4

$DATA1 SOURCE='HSPICE' VERSION='E-2010.12-SP2 32-BIT'										
$OPTION MEASFORM=3										
.TITLE '**********'										
index	load	risefall	r_delay	f_delay	r_transitic	f_transitic	rd_in_us	fd_in_us	rt_in_us	ft_in_us
1	1.00E-13	1.00E-10	1.55E-07	1.33E-07	3.19E-07	2.60E-07	0.1546	0.133	0.319	0.2601
2	1.00E-13	1.00E-09	1.55E-07	1.34E-07	3.19E-07	2.61E-07	0.1549	0.1335	0.3192	0.2605
3	1.00E-13	1.00E-08	1.58E-07	1.36E-07	3.20E-07	2.60E-07	0.1577	0.1359	0.3195	0.2604
4	1.00E-13	1.00E-07	1.84E-07	1.61E-07	3.20E-07	2.60E-07	0.1838	0.1614	0.3195	0.2597
5	1.00E-13	1.00E-06	4.54E-07	4.19E-07	5.11E-07	4.79E-07	0.4543	0.4189	0.5112	0.4789
6	1.00E-13	1.00E-05	1.47E-06	1.04E-06	2.95E-06	2.96E-06	1.4669	1.0437	2.9515	2.9623
7	2.00E-13	1.00E-10	3.01E-07	2.58E-07	6.25E-07	5.09E-07	0.3006	0.2579	0.6247	0.5091
8	2.00E-13	1.00E-09	3.01E-07	2.59E-07	6.26E-07	5.10E-07	0.3012	0.2588	0.6264	0.5099
9	2.00E-13	1.00E-08	3.03E-07	2.61E-07	6.25E-07	5.10E-07	0.3032	0.2607	0.6251	0.5096
10	2.00E-13	1.00E-07	3.29E-07	2.86E-07	6.26E-07	5.10E-07	0.3293	0.286	0.6255	0.51
11	2.00E-13	1.00E-06	6.02E-07	5.54E-07	7.35E-07	6.44E-07	0.6019	0.554	0.7349	0.6444
12	2.00E-13	1.00E-05	2.10E-06	1.69E-06	3.46E-06	3.47E-06	2.1044	1.6941	3.4546	3.4705
13	1.50E-12	1.00E-10	2.20E-06	1.89E-06	4.60E-06	3.75E-06	2.2	1.8864	4.6003	3.7537
14	1.50E-12	1.00E-09	2.20E-06	1.88E-06	4.60E-06	3.75E-06	2.1974	1.8835	4.5964	3.749
15	1.50E-12	1.00E-08	2.20E-06	1.89E-06	4.59E-06	3.76E-06	2.1966	1.8889	4.5922	3.7546
16	1.50E-12	1.00E-07	2.23E-06	1.91E-06	4.60E-06	3.75E-06	2.2248	1.9119	4.5969	3.7525
17	1.50E-12	1.00E-06	2.49E-06	2.17E-06	4.60E-06	3.75E-06	2.4863	2.1728	4.597	3.7545
18	1.50E-12	1.00E-05	5.22E-06	4.86E-06	6.10E-06	5.53E-06	5.2189	4.8571	6.0996	5.5341
19	3.00E-12	1.00E-10	4.39E-06	3.76E-06	9.19E-06	7.49E-06	4.3909	3.7634	9.1879	7.4939
20	3.00E-12	1.00E-09	4.39E-06	3.76E-06	9.19E-06	7.49E-06	4.3921	3.759	9.1929	7.4872
21	3.00E-12	1.00E-08	4.39E-06	3.76E-06	9.17E-06	7.49E-06	4.3924	3.762	9.1691	7.4928
22	3.00E-12	1.00E-07	4.41E-06	3.79E-06	9.20E-06	7.49E-06	4.4109	3.7931	9.1981	7.4941
23	3.00E-12	1.00E-06	4.66E-06	4.05E-06	9.17E-06	7.50E-06	4.6621	4.0459	9.1687	7.4956
24	3.00E-12	1.00E-05	7.37E-06	6.70E-06	9.90E-06	8.40E-06	7.3656	6.7016	9.9005	8.3983
25	4.00E-12	1.00E-10	5.85E-06	5.02E-06	1.22E-05	1.00E-05	5.8536	5.0196	12.2326	9.9964
26	4.00E-12	1.00E-09	5.84E-06	5.02E-06	1.22E-05	9.99E-06	5.8417	5.0164	12.2162	9.9911
27	4.00E-12	1.00E-08	5.85E-06	5.02E-06	1.22E-05	1.00E-05	5.8498	5.0202	12.2409	9.9949
28	4.00E-12	1.00E-07	5.87E-06	5.04E-06	1.22E-05	9.99E-06	5.8734	5.0425	12.213	9.9923
29	4.00E-12	1.00E-06	6.14E-06	5.30E-06	1.23E-05	9.99E-06	6.1348	5.2947	12.2546	9.9915
30	4.00E-12	1.00E-05	8.81E-06	7.94E-06	1.26E-05	1.06E-05	8.8087	7.9399	12.6284	10.5581
31	5.00E-12	1.00E-10	7.31E-06	6.28E-06	1.53E-05	1.25E-05	7.3057	6.2749	15.2696	12.4967
32	5.00E-12	1.00E-09	7.31E-06	6.28E-06	1.53E-05	1.25E-05	7.314	6.2759	15.2763	12.4969
33	5.00E-12	1.00E-08	7.29E-06	6.27E-06	1.53E-05	1.25E-05	7.2942	6.2742	15.2681	12.4851
34	5.00E-12	1.00E-07	7.33E-06	6.29E-06	1.53E-05	1.25E-05	7.3343	6.2882	15.3133	12.4741
35	5.00E-12	1.00E-06	7.59E-06	6.54E-06	1.53E-05	1.25E-05	7.5862	6.5352	15.2904	12.4641
36	5.00E-12	1.00E-05	1.03E-05	9.18E-06	1.56E-05	1.29E-05	10.2574	9.18	15.5481	12.8486

Fig. 28 : Output Delay and Transition (Rise and Fall) Values

$DATA1 SOURCE='HSPICE' VERSION='E-2010.12-SP2 32-BIT'								
$OPTION MEASFORM=3								
.TITLE '************************************'								
index	loadc	input slew	rise_switching_energy(J)	fall_switching_energy(J)	rise_dynamic_energy(J)	fall_dynamic_energy(J)	rise_internal_energy(nJ)	fall_internal_energy(nJ)
1	1.00E-13	1.00E-10	2.00E-15	2.00E-15	2.75E-15	2.88E-15	7.51E-07	8.76E-07
2	1.00E-13	1.00E-09	2.00E-15	2.00E-15	2.75E-15	2.87E-15	7.52E-07	8.74E-07
3	1.00E-13	1.00E-08	2.00E-15	2.00E-15	2.75E-15	2.88E-15	7.51E-07	8.76E-07
4	1.00E-13	5.00E-08	2.00E-15	2.00E-15	2.75E-15	2.87E-15	7.53E-07	8.73E-07
5	1.00E-13	1.00E-07	2.00E-15	2.00E-15	2.75E-15	2.87E-15	7.53E-07	8.72E-07
6	1.00E-13	1.00E-06	2.00E-15	2.00E-15	2.76E-15	2.85E-15	7.58E-07	8.48E-07
7	2.00E-13	1.00E-10	4.00E-15	4.00E-15	4.74E-15	4.86E-15	7.40E-07	8.64E-07
8	2.00E-13	1.00E-09	4.00E-15	4.00E-15	4.74E-15	4.86E-15	7.42E-07	8.62E-07
9	2.00E-13	1.00E-08	4.00E-15	4.00E-15	4.74E-15	4.86E-15	7.41E-07	8.63E-07
10	2.00E-13	5.00E-08	4.00E-15	4.00E-15	4.75E-15	4.86E-15	7.45E-07	8.60E-07
11	2.00E-13	1.00E-07	4.00E-15	4.00E-15	4.74E-15	4.86E-15	7.41E-07	8.59E-07
12	2.00E-13	1.00E-06	4.00E-15	4.00E-15	4.74E-15	4.84E-15	7.39E-07	8.36E-07
13	1.50E-12	1.00E-10	3.00E-14	3.00E-14	2.49E-14	3.04E-14	5.13E-06	3.61E-07
14	1.50E-12	1.00E-09	3.00E-14	3.00E-14	2.49E-14	3.04E-14	5.13E-06	3.61E-07
15	1.50E-12	1.00E-08	3.00E-14	3.00E-14	2.49E-14	3.04E-14	5.13E-06	3.57E-07
16	1.50E-12	5.00E-08	3.00E-14	3.00E-14	2.49E-14	3.03E-14	5.09E-06	3.30E-07
17	1.50E-12	1.00E-07	3.00E-14	3.00E-14	2.49E-14	3.03E-14	5.10E-06	3.08E-07
18	1.50E-12	1.00E-06	3.00E-14	3.00E-14	2.49E-14	2.98E-14	5.11E-06	-2.19E-07
19	3.00E-12	1.00E-10	6.00E-14	6.00E-14	1.86E-14	4.83E-14	4.14E-05	-1.17E-05
20	3.00E-12	1.00E-09	6.00E-14	6.00E-14	1.85E-14	4.83E-14	4.15E-05	-1.17E-05
21	3.00E-12	1.00E-08	6.00E-14	6.00E-14	1.86E-14	4.83E-14	4.14E-05	-1.17E-05
22	3.00E-12	5.00E-08	6.00E-14	6.00E-14	1.87E-14	4.81E-14	4.13E-05	-1.19E-05
23	3.00E-12	1.00E-07	6.00E-14	6.00E-14	1.89E-14	4.79E-14	4.11E-05	-1.21E-05
24	3.00E-12	1.00E-06	6.00E-14	6.00E-14	2.06E-14	4.47E-14	3.94E-05	-1.54E-05
25	4.00E-12	1.00E-10	8.00E-14	8.00E-14	1.50E-14	5.45E-14	6.50E-05	-2.55E-05
26	4.00E-12	1.00E-09	8.00E-14	8.00E-14	1.50E-14	5.45E-14	6.50E-05	-2.55E-05
27	4.00E-12	1.00E-08	8.00E-14	8.00E-14	1.50E-14	5.45E-14	6.50E-05	-2.55E-05
28	4.00E-12	5.00E-08	8.00E-14	8.00E-14	1.52E-14	5.42E-14	6.48E-05	-2.58E-05
29	4.00E-12	1.00E-07	8.00E-14	8.00E-14	1.54E-14	5.40E-14	6.46E-05	-2.60E-05
30	4.00E-12	1.00E-06	8.00E-14	8.00E-14	1.82E-14	4.96E-14	6.18E-05	-3.04E-05
31	5.00E-12	1.00E-10	1.00E-13	1.00E-13	1.24E-14	5.87E-14	8.76E-05	-4.13E-05
32	5.00E-12	1.00E-09	1.00E-13	1.00E-13	1.24E-14	5.87E-14	8.76E-05	-4.13E-05
33	5.00E-12	1.00E-08	1.00E-13	1.00E-13	1.25E-14	5.86E-14	8.75E-05	-4.14E-05
34	5.00E-12	5.00E-08	1.00E-13	1.00E-13	1.27E-14	5.83E-14	8.73E-05	-4.17E-05
35	5.00E-12	1.00E-07	1.00E-13	1.00E-13	1.30E-14	5.80E-14	8.70E-05	-4.20E-05
36	5.00E-12	1.00E-06	1.00E-13	1.00E-13	1.65E-14	5.29E-14	8.35E-05	-4.71E-05

Fig 29 : Dynamic Power and Internal Energy Computation Tables

A.2.3 NAND2X1:

$DATA1 SOURCE='HSPICE' VERSION='E-2010.12-SP2 32-BIT'										
$OPTION MEASFORM=3										
.TITLE '**********'										
index	load (in F)	risefall (sl	r_delay	f_delay	r_transitic	f_transitic	rd_in_us	fd_in_us	rt_in_us	ft_in_us
1	1.00E-13	1.00E-10	6.05E-07	5.60E-07	1.27E-06	1.05E-06	0.6049	0.5576	1.2715	1.0535
2	1.00E-13	1.00E-09	6.05E-07	5.58E-07	1.27E-06	1.05E-06	0.6053	0.5595	1.2716	1.0518
3	1.00E-13	1.00E-08	6.08E-07	5.60E-07	1.27E-06	1.05E-06	0.6078	0.5602	1.2707	1.053
4	1.00E-13	1.00E-07	6.32E-07	5.77E-07	1.27E-06	1.05E-06	0.6324	0.5772	1.2681	1.0511
5	1.00E-13	1.00E-06	9.00E-07	7.63E-07	1.31E-06	1.13E-06	0.9003	0.7634	1.308	1.1312
6	1.00E-13	1.00E-05	3.17E-06	1.67E-06	3.89E-06	4.07E-06	3.1681	1.665	3.8943	4.0705
7	2.00E-13	1.00E-10	1.19E-06	1.10E-06	2.51E-06	2.08E-06	1.1926	1.0979	2.5124	2.08
8	2.00E-13	1.00E-09	1.19E-06	1.10E-06	2.51E-06	2.08E-06	1.193	1.0996	2.5076	2.0823
9	2.00E-13	1.00E-08	1.20E-06	1.10E-06	2.51E-06	2.08E-06	1.1957	1.1007	2.5136	2.0833
10	2.00E-13	1.00E-07	1.22E-06	1.12E-06	2.51E-06	2.08E-06	1.2198	1.1172	2.5109	2.0819
11	2.00E-13	1.00E-06	1.48E-06	1.30E-06	2.51E-06	2.10E-06	1.4842	1.2979	2.514	2.0985
12	2.00E-13	1.00E-05	4.17E-06	2.80E-06	4.61E-06	4.87E-06	4.1683	2.7976	4.6088	4.8697
13	1.50E-12	1.00E-10	8.82E-06	8.13E-06	1.86E-05	1.54E-05	8.8212	8.1279	18.6188	15.4298
14	1.50E-12	1.00E-09	8.84E-06	8.14E-06	1.86E-05	1.54E-05	8.8373	8.1397	18.621	15.429
15	1.50E-12	1.00E-08	8.84E-06	8.14E-06	1.87E-05	1.55E-05	8.8411	8.1439	18.6588	15.4479
16	1.50E-12	1.00E-07	8.86E-06	8.16E-06	1.87E-05	1.55E-05	8.8633	8.158	18.6655	15.4464
17	1.50E-12	1.00E-06	9.11E-06	8.32E-06	1.87E-05	1.54E-05	9.1081	8.3242	18.6489	15.4332
18	1.50E-12	1.00E-05	1.18E-05	1.02E-05	1.88E-05	1.58E-05	11.7646	10.1544	18.7619	15.8304
19	3.00E-12	1.00E-10	1.77E-05	1.62E-05	3.73E-05	3.09E-05	17.6293	16.2361	37.2546	30.8909
20	3.00E-12	1.00E-09	1.76E-05	1.63E-05	3.72E-05	3.09E-05	17.6486	16.2557	37.2072	30.8799
21	3.00E-12	1.00E-08	1.77E-05	1.63E-05	3.73E-05	3.09E-05	17.6617	16.2582	37.2566	30.8904
22	3.00E-12	1.00E-07	1.77E-05	1.63E-05	3.72E-05	3.08E-05	17.6655	16.2698	37.2059	30.8136
23	3.00E-12	1.00E-06	1.79E-05	1.65E-05	3.73E-05	3.09E-05	17.9161	16.4648	37.2753	30.9021
24	3.00E-12	1.00E-05	2.05E-05	1.82E-05	3.73E-05	3.09E-05	20.5183	18.2247	37.2554	30.898
25	4.00E-12	1.00E-10	2.35E-05	2.17E-05	4.96E-05	4.12E-05	23.487	21.6558	49.5934	41.1857
26	4.00E-12	1.00E-09	2.35E-05	2.17E-05	4.96E-05	4.12E-05	23.5187	21.69	49.6161	41.1625
27	4.00E-12	1.00E-08	2.35E-05	2.17E-05	4.96E-05	4.12E-05	23.5276	21.7004	49.5937	41.1728
28	4.00E-12	1.00E-07	2.36E-05	2.17E-05	4.97E-05	4.11E-05	23.5726	21.743	49.6549	41.1342
29	4.00E-12	1.00E-06	2.38E-05	2.19E-05	4.96E-05	4.12E-05	23.7943	21.8463	49.6199	41.2071
30	4.00E-12	1.00E-05	2.64E-05	2.36E-05	4.97E-05	4.12E-05	26.4106	23.6435	49.6607	41.1775
31	5.00E-12	1.00E-10	2.94E-05	2.71E-05	6.21E-05	5.14E-05	29.4097	27.0571	62.1233	51.4405
32	5.00E-12	1.00E-09	2.94E-05	2.71E-05	6.21E-05	5.14E-05	29.4219	27.0572	62.0611	51.4409
33	5.00E-12	1.00E-08	2.94E-05	2.71E-05	6.22E-05	5.15E-05	29.4244	27.1103	62.2289	51.4674
34	5.00E-12	1.00E-07	2.94E-05	2.71E-05	6.21E-05	5.15E-05	29.4384	27.1313	62.0783	51.5016
35	5.00E-12	1.00E-06	2.96E-05	2.73E-05	6.20E-05	5.15E-05	29.6448	27.2679	61.9995	51.4698
36	5.00E-12	1.00E-05	3.22E-05	2.91E-05	6.20E-05	5.14E-05	32.2061	29.0965	62.0233	51.3903

Fig. 30 : Output Delay and Transition (Rise and Fall) Values for **ip1 -> op** Path

$DATA1 SOURCE='HSPICE' VERSION='E-2010.12-SP2 32-BIT'										
$OPTION MEASFORM=3										
.TITLE '*************************************'										
index	load	risefall	r_delay	f_delay	r_transitic	f_transitic	rd_in_us	fd_in_us	rt_in_us	ft_in_us
1	1.00E-13	1.00E-10	6.09E-07	5.60E-07	1.28E-06	1.05E-06	0.6092	0.5601	1.277	1.0532
2	1.00E-13	1.00E-09	6.10E-07	5.60E-07	1.28E-06	1.05E-06	0.6098	0.5602	1.2785	1.0511
3	1.00E-13	1.00E-08	6.11E-07	5.63E-07	1.28E-06	1.05E-06	0.6112	0.5631	1.2779	1.0521
4	1.00E-13	1.00E-07	6.37E-07	5.86E-07	1.28E-06	1.05E-06	0.6371	0.5856	1.277	1.0528
5	1.00E-13	1.00E-06	9.04E-07	7.95E-07	1.31E-06	1.12E-06	0.904	0.7952	1.3118	1.1163
6	1.00E-13	1.00E-05	3.17E-06	1.89E-06	3.90E-06	3.88E-06	3.1737	1.8861	3.8985	3.8748
7	2.00E-13	1.00E-10	1.20E-06	1.10E-06	2.52E-06	2.08E-06	1.1957	1.1015	2.5173	2.0787
8	2.00E-13	1.00E-09	1.20E-06	1.10E-06	2.51E-06	2.08E-06	1.1978	1.1029	2.5133	2.0828
9	2.00E-13	1.00E-08	1.20E-06	1.11E-06	2.51E-06	2.08E-06	1.1996	1.1075	2.5112	2.0822
10	2.00E-13	1.00E-07	1.22E-06	1.13E-06	2.52E-06	2.08E-06	1.224	1.1266	2.5198	2.0813
11	2.00E-13	1.00E-06	1.49E-06	1.34E-06	2.52E-06	2.09E-06	1.4851	1.336	2.5169	2.0915
12	2.00E-13	1.00E-05	4.17E-06	3.04E-06	4.61E-06	4.66E-06	4.1713	3.0374	4.6057	4.655
13	1.50E-12	1.00E-10	8.84E-06	8.14E-06	1.86E-05	1.55E-05	8.8414	8.1397	18.6324	15.4496
14	1.50E-12	1.00E-09	8.84E-06	8.14E-06	1.87E-05	1.54E-05	8.8407	8.1396	18.649	15.416
15	1.50E-12	1.00E-08	8.84E-06	8.14E-06	1.86E-05	1.54E-05	8.8418	8.1437	18.6237	15.4261
16	1.50E-12	1.00E-07	8.86E-06	8.18E-06	1.86E-05	1.55E-05	8.8586	8.1782	18.6386	15.4621
17	1.50E-12	1.00E-06	9.09E-06	8.38E-06	1.87E-05	1.54E-05	9.0891	8.3836	18.6486	15.4256
18	1.50E-12	1.00E-05	1.18E-05	1.05E-05	1.87E-05	1.58E-05	11.7655	10.4944	18.7285	15.7489
19	3.00E-12	1.00E-10	1.76E-05	1.63E-05	3.72E-05	3.09E-05	17.636	16.2944	37.2348	30.8473
20	3.00E-12	1.00E-09	1.76E-05	1.63E-05	3.72E-05	3.08E-05	17.64	16.291	37.1806	30.8233
21	3.00E-12	1.00E-08	1.77E-05	1.63E-05	3.72E-05	3.09E-05	17.6509	16.2862	37.1943	30.856
22	3.00E-12	1.00E-07	1.77E-05	1.63E-05	3.72E-05	3.09E-05	17.6854	16.3234	37.1745	30.9081
23	3.00E-12	1.00E-06	1.79E-05	1.66E-05	3.72E-05	3.08E-05	17.8995	16.5603	37.1792	30.8437
24	3.00E-12	1.00E-05	2.05E-05	1.86E-05	3.72E-05	3.09E-05	20.5141	18.5559	37.2039	30.8744
25	4.00E-12	1.00E-10	2.35E-05	2.17E-05	4.97E-05	4.12E-05	23.4874	21.7319	49.686	41.178
26	4.00E-12	1.00E-09	2.35E-05	2.17E-05	4.97E-05	4.12E-05	23.5264	21.6954	49.6675	41.1711
27	4.00E-12	1.00E-08	2.35E-05	2.17E-05	4.96E-05	4.12E-05	23.4994	21.7152	49.6226	41.1806
28	4.00E-12	1.00E-07	2.35E-05	2.17E-05	4.96E-05	4.12E-05	23.5318	21.7	49.5683	41.1582
29	4.00E-12	1.00E-06	2.38E-05	2.19E-05	4.96E-05	4.12E-05	23.7691	21.911	49.5478	41.1572
30	4.00E-12	1.00E-05	2.63E-05	2.41E-05	4.95E-05	4.12E-05	26.3408	24.0459	49.5298	41.1859
31	5.00E-12	1.00E-10	2.94E-05	2.71E-05	6.21E-05	5.14E-05	29.3883	27.0937	62.0796	51.4105
32	5.00E-12	1.00E-09	2.94E-05	2.72E-05	6.19E-05	5.14E-05	29.4154	27.1798	61.8867	51.4386
33	5.00E-12	1.00E-08	2.94E-05	2.71E-05	6.19E-05	5.14E-05	29.4036	27.1075	61.8855	51.3696
34	5.00E-12	1.00E-07	2.94E-05	2.71E-05	6.21E-05	5.15E-05	29.4094	27.1221	62.055	51.5154
35	5.00E-12	1.00E-06	2.96E-05	2.74E-05	6.19E-05	5.15E-05	29.643	27.3745	61.9048	51.4857
36	5.00E-12	1.00E-05	3.22E-05	2.94E-05	6.20E-05	5.15E-05	32.2364	29.403	61.994	51.4685

Fig. 31 : Output Delay and Transition (Rise and Fall) Values for **ip2 -> op** Path

$DATA1 SOURCE='HSPICE' VERSION='E-2010.12-SP2 32-BIT'												
$OPTION MEASFORM=3												
.TITLE '**********'												
index	loadc	risefall	eswrise	eswfall	edynrise1	edynfall1	eintrise1	eintfall1	edynrise2	edynfall2	eintrise2	eintfall2
1	1.00E-13	1.00E-10	2.00E-15	2.00E-15	2.34E-15	2.41E-15	3.41E-07	4.07E-07	3.24E-16	4.69E-16	1.68E-06	-1.5E-06
2	1.00E-13	1.00E-09	2.00E-15	2.00E-15	2.34E-15	2.41E-15	3.4E-07	4.06E-07	3.24E-16	4.69E-16	1.68E-06	-1.5E-06
3	1.00E-13	1.00E-08	2.00E-15	2.00E-15	2.34E-15	2.40E-15	3.4E-07	4.04E-07	3.25E-16	4.69E-16	1.68E-06	-1.5E-06
4	1.00E-13	5.00E-08	2.00E-15	2.00E-15	2.34E-15	2.41E-15	3.4E-07	4.05E-07	3.25E-16	4.68E-16	1.68E-06	-1.5E-06
5	1.00E-13	1.00E-07	2.00E-15	2.00E-15	2.34E-15	2.40E-15	3.4E-07	4.04E-07	3.26E-16	4.67E-16	1.67E-06	-1.5E-06
6	1.00E-13	1.00E-06	2.00E-15	2.00E-15	2.34E-15	2.39E-15	3.43E-07	3.94E-07	3.40E-16	4.49E-16	1.66E-06	-1.6E-06
7	2.00E-13	1.00E-10	4.00E-15	4.00E-15	4.29E-15	4.37E-15	2.87E-07	3.71E-07	3.24E-16	4.69E-16	3.68E-06	-3.5E-06
8	2.00E-13	1.00E-09	4.00E-15	4.00E-15	4.29E-15	4.37E-15	2.85E-07	3.73E-07	3.24E-16	4.69E-16	3.68E-06	-3.5E-06
9	2.00E-13	1.00E-08	4.00E-15	4.00E-15	4.29E-15	4.37E-15	2.94E-07	3.69E-07	3.25E-16	4.69E-16	3.68E-06	-3.5E-06
10	2.00E-13	5.00E-08	4.00E-15	4.00E-15	4.29E-15	4.37E-15	2.87E-07	3.71E-07	3.25E-16	4.68E-16	3.68E-06	-3.5E-06
11	2.00E-13	1.00E-07	4.00E-15	4.00E-15	4.29E-15	4.37E-15	2.89E-07	3.7E-07	3.26E-16	4.67E-16	3.67E-06	-3.5E-06
12	2.00E-13	1.00E-06	4.00E-15	4.00E-15	4.28E-15	4.36E-15	2.84E-07	3.59E-07	3.40E-16	4.49E-16	3.66E-06	-3.6E-06
13	1.50E-12	1.00E-10	3.00E-14	3.00E-14	2.77E-15	1.52E-14	2.72E-05	-1.5E-05	3.70E-16	7.35E-16	2.96E-05	-2.9E-05
14	1.50E-12	1.00E-09	3.00E-14	3.00E-14	2.77E-15	1.52E-14	2.72E-05	-1.5E-05	3.70E-16	7.35E-16	2.96E-05	-2.9E-05
15	1.50E-12	1.00E-08	3.00E-14	3.00E-14	2.79E-15	1.52E-14	2.72E-05	-1.5E-05	3.70E-16	7.35E-16	2.96E-05	-2.9E-05
16	1.50E-12	5.00E-08	3.00E-14	3.00E-14	2.84E-15	1.51E-14	2.72E-05	-1.5E-05	3.71E-16	7.38E-16	2.96E-05	-2.9E-05
17	1.50E-12	1.00E-07	3.00E-14	3.00E-14	2.91E-15	1.50E-14	2.71E-05	-1.5E-05	3.73E-16	7.41E-16	2.96E-05	-2.9E-05
18	1.50E-12	1.00E-06	3.00E-14	3.00E-14	3.81E-15	1.35E-14	2.62E-05	-1.7E-05	3.89E-16	7.83E-16	2.96E-05	-2.9E-05
19	3.00E-12	1.00E-10	6.00E-14	6.00E-14	1.53E-15	1.72E-14	5.85E-05	-4.3E-05	4.50E-16	7.17E-16	5.96E-05	-5.9E-05
20	3.00E-12	1.00E-09	6.00E-14	6.00E-14	1.53E-15	1.72E-14	5.85E-05	-4.3E-05	4.50E-16	7.17E-16	5.96E-05	-5.9E-05
21	3.00E-12	1.00E-08	6.00E-14	6.00E-14	1.55E-15	1.72E-14	5.85E-05	-4.3E-05	4.51E-16	7.17E-16	5.96E-05	-5.9E-05
22	3.00E-12	5.00E-08	6.00E-14	6.00E-14	1.63E-15	1.71E-14	5.84E-05	-4.3E-05	4.52E-16	7.18E-16	5.96E-05	-5.9E-05
23	3.00E-12	1.00E-07	6.00E-14	6.00E-14	1.73E-15	1.70E-14	5.83E-05	-4.3E-05	4.53E-16	7.20E-16	5.96E-05	-5.9E-05
24	3.00E-12	1.00E-06	6.00E-14	6.00E-14	3.04E-15	1.50E-14	5.70E-05	-4.5E-05	4.65E-16	7.30E-16	5.95E-05	-5.9E-05
25	4.00E-12	1.00E-10	8.00E-14	8.00E-14	1.20E-15	1.78E-14	7.88E-05	-6.2E-05	4.63E-16	6.76E-16	7.95E-05	-7.9E-05
26	4.00E-12	1.00E-09	8.00E-14	8.00E-14	1.21E-15	1.78E-14	7.88E-05	-6.2E-05	4.63E-16	6.76E-16	7.95E-05	-7.9E-05
27	4.00E-12	1.00E-08	8.00E-14	8.00E-14	1.22E-15	1.78E-14	7.88E-05	-6.2E-05	4.64E-16	6.76E-16	7.95E-05	-7.9E-05
28	4.00E-12	5.00E-08	8.00E-14	8.00E-14	1.31E-15	1.77E-14	7.87E-05	-6.2E-05	4.65E-16	6.77E-16	7.95E-05	-7.9E-05
29	4.00E-12	1.00E-07	8.00E-14	8.00E-14	1.42E-15	1.75E-14	7.86E-05	-6.2E-05	4.66E-16	6.77E-16	7.95E-05	-7.9E-05
30	4.00E-12	1.00E-06	8.00E-14	8.00E-14	2.86E-15	1.54E-14	7.71E-05	-6.5E-05	4.74E-16	6.78E-16	7.95E-05	-7.9E-05
31	5.00E-12	1.00E-10	1.00E-13	1.00E-13	1.01E-15	1.81E-14	9.90E-05	-8.2E-05	4.61E-16	6.40E-16	9.95E-05	-9.9E-05
32	5.00E-12	1.00E-09	1.00E-13	1.00E-13	1.02E-15	1.81E-14	9.90E-05	-8.2E-05	4.61E-16	6.40E-16	9.95E-05	-9.9E-05
33	5.00E-12	1.00E-08	1.00E-13	1.00E-13	1.04E-15	1.81E-14	9.90E-05	-8.2E-05	4.61E-16	6.40E-16	9.95E-05	-9.9E-05
34	5.00E-12	5.00E-08	1.00E-13	1.00E-13	1.13E-15	1.80E-14	9.89E-05	-8.2E-05	4.62E-16	6.40E-16	9.95E-05	-9.9E-05
35	5.00E-12	1.00E-07	1.00E-13	1.00E-13	1.24E-15	1.79E-14	9.88E-05	-8.2E-05	4.63E-16	6.41E-16	9.95E-05	-9.9E-05
36	5.00E-12	1.00E-06	1.00E-13	1.00E-13	2.76E-15	1.57E-14	9.73E-05	-8.4E-05	4.70E-16	6.36E-16	9.95E-05	-9.9E-05

Fig 32 : Dynamic Power and Internal Energy Computation Tables

A.2.4 NOR2X1:

$DATA1 SOURCE='HSPICE' VERSION='E-2010.12-SP2 32-BIT'										
$OPTION MEASFORM=3										
.TITLE '************************************'										
index	load	risefall	r_delay	f_delay	r_transitic	f_transitic	rd_in_us	fd_in_us	rt_in_us	ft_in_us
1	1.00E-13	1.00E-10	7.12E-07	5.49E-07	1.37E-06	1.09E-06	0.7111	0.5489	1.3698	1.089
2	1.00E-13	1.00E-09	7.11E-07	5.50E-07	1.37E-06	1.09E-06	0.7117	0.5503	1.3665	1.0888
3	1.00E-13	1.00E-08	7.16E-07	5.52E-07	1.37E-06	1.09E-06	0.7156	0.5524	1.367	1.086
4	1.00E-13	1.00E-07	7.39E-07	5.76E-07	1.37E-06	1.09E-06	0.7391	0.5759	1.3666	1.0871
5	1.00E-13	1.00E-06	9.56E-07	8.40E-07	1.40E-06	1.14E-06	0.9558	0.8398	1.4031	1.1371
6	1.00E-13	1.00E-05	2.45E-06	2.84E-06	3.97E-06	3.96E-06	2.4445	2.8379	3.9725	3.9598
7	2.00E-13	1.00E-10	1.39E-06	1.07E-06	2.70E-06	2.13E-06	1.392	1.068	2.7035	2.132
8	2.00E-13	1.00E-09	1.39E-06	1.07E-06	2.70E-06	2.13E-06	1.3925	1.0685	2.7022	2.1316
9	2.00E-13	1.00E-08	1.40E-06	1.07E-06	2.71E-06	2.13E-06	1.3952	1.0722	2.706	2.129
10	2.00E-13	1.00E-07	1.42E-06	1.10E-06	2.71E-06	2.13E-06	1.4227	1.0959	2.7064	2.127
11	2.00E-13	1.00E-06	1.64E-06	1.36E-06	2.70E-06	2.13E-06	1.6363	1.3565	2.7034	2.132
12	2.00E-13	1.00E-05	3.63E-06	3.86E-06	4.84E-06	4.54E-06	3.6254	3.862	4.8429	4.5415
13	1.50E-12	1.00E-10	1.02E-05	7.82E-06	2.01E-05	1.57E-05	10.2372	7.8148	20.0623	15.67
14	1.50E-12	1.00E-09	1.02E-05	7.82E-06	2.00E-05	1.57E-05	10.243	7.8158	20.0389	15.6632
15	1.50E-12	1.00E-08	1.02E-05	7.82E-06	2.01E-05	1.57E-05	10.2433	7.8173	20.067	15.669
16	1.50E-12	1.00E-07	1.03E-05	7.84E-06	2.01E-05	1.57E-05	10.3068	7.8399	20.0848	15.6943
17	1.50E-12	1.00E-06	1.05E-05	8.08E-06	2.00E-05	1.57E-05	10.4677	8.0837	20.0278	15.6949
18	1.50E-12	1.00E-05	1.26E-05	1.07E-05	2.02E-05	1.59E-05	12.5987	10.7077	20.184	15.852
19	3.00E-12	1.00E-10	2.04E-05	1.56E-05	4.01E-05	3.13E-05	20.4226	15.5964	40.0612	31.3275
20	3.00E-12	1.00E-09	2.04E-05	1.56E-05	4.02E-05	3.13E-05	20.433	15.6004	40.1669	31.3152
21	3.00E-12	1.00E-08	2.04E-05	1.56E-05	4.01E-05	3.14E-05	20.4364	15.6008	40.1334	31.3486
22	3.00E-12	1.00E-07	2.05E-05	1.56E-05	4.01E-05	3.14E-05	20.49	15.6198	40.0549	31.3465
23	3.00E-12	1.00E-06	2.07E-05	1.59E-05	4.00E-05	3.13E-05	20.6653	15.8829	40.0248	31.2951
24	3.00E-12	1.00E-05	2.27E-05	1.85E-05	4.01E-05	3.13E-05	22.7391	18.4576	40.0636	31.3014
25	4.00E-12	1.00E-10	2.72E-05	2.08E-05	5.34E-05	4.18E-05	27.2291	20.7806	53.3577	41.7756
26	4.00E-12	1.00E-09	2.73E-05	2.08E-05	5.34E-05	4.17E-05	27.2594	20.8074	53.4211	41.6639
27	4.00E-12	1.00E-08	2.73E-05	2.08E-05	5.34E-05	4.18E-05	27.2608	20.8078	53.3966	41.7523
28	4.00E-12	1.00E-07	2.73E-05	2.08E-05	5.34E-05	4.17E-05	27.2997	20.8353	53.4012	41.6974
29	4.00E-12	1.00E-06	2.75E-05	2.11E-05	5.34E-05	4.17E-05	27.4874	21.0698	53.4277	41.6613
30	4.00E-12	1.00E-05	2.96E-05	2.36E-05	5.34E-05	4.18E-05	29.5807	23.6036	53.4089	41.78
31	5.00E-12	1.00E-10	3.40E-05	2.60E-05	6.67E-05	5.22E-05	34.0191	25.9602	66.7066	52.2036
32	5.00E-12	1.00E-09	3.41E-05	2.60E-05	6.69E-05	5.22E-05	34.0762	25.9773	66.8689	52.2296
33	5.00E-12	1.00E-08	3.41E-05	2.60E-05	6.69E-05	5.21E-05	34.0895	25.9869	66.9134	52.0781
34	5.00E-12	1.00E-07	3.41E-05	2.60E-05	6.69E-05	5.21E-05	34.0937	26.0216	66.8519	52.0853
35	5.00E-12	1.00E-06	3.43E-05	2.63E-05	6.67E-05	5.21E-05	34.3048	26.2663	66.7177	52.0851
36	5.00E-12	1.00E-05	3.64E-05	2.88E-05	6.69E-05	5.21E-05	36.429	28.8025	66.9261	52.0796

Fig. 33 : Output Delay and Transition (Rise and Fall) Values for **ip1 -> op** Path

$DATA1 SOURCE='HSPICE' VERSION='E-2010.12-SP2 32-BIT'										
$OPTION MEASFORM=3										
.TITLE '*************************************'										
index	load	risefall	r_delay	f_delay	r_transitic	f_transitic	rd_in_us	fd_in_us	rt_in_us	ft_in_us
1	1.00E-13	1.00E-10	7.02E-07	5.37E-07	1.37E-06	1.07E-06	0.7018	0.5365	1.3688	1.0684
2	1.00E-13	1.00E-09	7.02E-07	5.37E-07	1.37E-06	1.07E-06	0.702	0.537	1.3692	1.0681
3	1.00E-13	1.00E-08	7.02E-07	5.39E-07	1.37E-06	1.07E-06	0.7022	0.5391	1.3703	1.0671
4	1.00E-13	1.00E-07	7.22E-07	5.65E-07	1.37E-06	1.07E-06	0.7218	0.5649	1.3686	1.068
5	1.00E-13	1.00E-06	9.03E-07	8.27E-07	1.42E-06	1.12E-06	0.9033	0.827	1.421	1.1162
6	1.00E-13	1.00E-05	2.17E-06	2.81E-06	4.21E-06	3.96E-06	2.1654	2.8095	4.2079	3.9601
7	2.00E-13	1.00E-10	1.38E-06	1.06E-06	2.71E-06	2.11E-06	1.3817	1.0542	2.7078	2.1111
8	2.00E-13	1.00E-09	1.39E-06	1.05E-06	2.71E-06	2.11E-06	1.383	1.0551	2.7073	2.1072
9	2.00E-13	1.00E-08	1.38E-06	1.06E-06	2.71E-06	2.11E-06	1.3857	1.0569	2.7058	2.1083
10	2.00E-13	1.00E-07	1.40E-06	1.09E-06	2.70E-06	2.11E-06	1.3989	1.0846	2.7007	2.1123
11	2.00E-13	1.00E-06	1.58E-06	1.34E-06	2.71E-06	2.12E-06	1.5761	1.3424	2.7074	2.1154
12	2.00E-13	1.00E-05	3.34E-06	3.84E-06	5.12E-06	4.54E-06	3.3352	3.8428	5.1175	4.5366
13	1.50E-12	1.00E-10	1.02E-05	7.80E-06	2.01E-05	1.57E-05	10.2127	7.7977	20.0806	15.6916
14	1.50E-12	1.00E-09	1.02E-05	7.81E-06	2.01E-05	1.57E-05	10.2216	7.8064	20.0537	15.6785
15	1.50E-12	1.00E-08	1.02E-05	7.82E-06	2.01E-05	1.57E-05	10.2264	7.8184	20.0546	15.6865
16	1.50E-12	1.00E-07	1.02E-05	7.83E-06	2.00E-05	1.57E-05	10.2285	7.8341	20.0336	15.685
17	1.50E-12	1.00E-06	1.04E-05	8.09E-06	2.01E-05	1.57E-05	10.4096	8.0925	20.0881	15.6776
18	1.50E-12	1.00E-05	1.22E-05	1.07E-05	2.03E-05	1.59E-05	12.2014	10.7104	20.2561	15.8744
19	3.00E-12	1.00E-10	2.04E-05	1.56E-05	4.01E-05	3.13E-05	20.3986	15.5936	40.0502	31.3346
20	3.00E-12	1.00E-09	2.04E-05	1.56E-05	4.00E-05	3.14E-05	20.4131	15.6	40.0353	31.3562
21	3.00E-12	1.00E-08	2.04E-05	1.56E-05	4.01E-05	3.13E-05	20.4227	15.6189	40.0997	31.3261
22	3.00E-12	1.00E-07	2.04E-05	1.56E-05	4.01E-05	3.13E-05	20.4254	15.6236	40.1331	31.3236
23	3.00E-12	1.00E-06	2.06E-05	1.59E-05	4.01E-05	3.14E-05	20.6388	15.8903	40.094	31.354
24	3.00E-12	1.00E-05	2.24E-05	1.85E-05	4.01E-05	3.14E-05	22.3695	18.4632	40.1054	31.3526
25	4.00E-12	1.00E-10	2.72E-05	2.08E-05	5.35E-05	4.17E-05	27.1889	20.798	53.4925	41.7289
26	4.00E-12	1.00E-09	2.72E-05	2.08E-05	5.34E-05	4.18E-05	27.203	20.8003	53.3991	41.8095
27	4.00E-12	1.00E-08	2.72E-05	2.08E-05	5.35E-05	4.18E-05	27.2306	20.8172	53.4776	41.7841
28	4.00E-12	1.00E-07	2.72E-05	2.08E-05	5.35E-05	4.18E-05	27.2318	20.8356	53.5419	41.7882
29	4.00E-12	1.00E-06	2.74E-05	2.10E-05	5.34E-05	4.18E-05	27.3933	21.0391	53.4014	41.7457
30	4.00E-12	1.00E-05	2.92E-05	2.36E-05	5.36E-05	4.18E-05	29.1653	23.6025	53.5514	41.7701
31	5.00E-12	1.00E-10	3.40E-05	2.60E-05	6.67E-05	5.22E-05	33.985	25.9408	66.7396	52.1746
32	5.00E-12	1.00E-09	3.40E-05	2.59E-05	6.69E-05	5.21E-05	33.9971	25.966	66.8454	52.1136
33	5.00E-12	1.00E-08	3.40E-05	2.60E-05	6.68E-05	5.22E-05	34.0111	25.9948	66.835	52.2381
34	5.00E-12	1.00E-07	3.40E-05	2.60E-05	6.67E-05	5.21E-05	34.0272	26.0107	66.6722	52.1341
35	5.00E-12	1.00E-06	3.42E-05	2.62E-05	6.67E-05	5.21E-05	34.2233	26.2126	66.7207	52.1218
36	5.00E-12	1.00E-05	3.59E-05	2.88E-05	6.68E-05	5.22E-05	35.9448	28.7479	66.8396	52.1722

Fig. 34 : Output Delay and Transition (Rise and Fall) Values for **ip2 -> op** Path

$DATA1 SOURCE='HSPICE' VERSION='E-2010.12-SP2 32-BIT'												
$OPTION MEASFORM=3												
.TITLE '**********'												
index	loadc	risefall	eswrise	eswfall	edynrise1	edynfall1	eintrise1	eintfall1	edynrise2	edynfall2	eintrise2	eintfall2
1	1.00E-13	1.00E-10	2.00E-15	2.00E-15	2.35E-15	2.41E-15	3.50E-07	4.10E-07	2.35E-15	2.39E-15	3.46E-07	3.92E-07
2	1.00E-13	1.00E-09	2.00E-15	2.00E-15	2.35E-15	2.41E-15	3.50E-07	4.10E-07	2.35E-15	2.39E-15	3.48E-07	3.94E-07
3	1.00E-13	1.00E-08	2.00E-15	2.00E-15	2.35E-15	2.41E-15	3.50E-07	4.10E-07	2.35E-15	2.39E-15	3.45E-07	3.92E-07
4	1.00E-13	5.00E-08	2.00E-15	2.00E-15	2.35E-15	2.41E-15	3.50E-07	4.09E-07	2.35E-15	2.39E-15	3.45E-07	3.93E-07
5	1.00E-13	1.00E-07	2.00E-15	2.00E-15	2.35E-15	2.41E-15	3.51E-07	4.08E-07	2.35E-15	2.39E-15	3.45E-07	3.90E-07
6	1.00E-13	1.00E-06	2.00E-15	2.00E-15	2.36E-15	2.39E-15	3.63E-07	3.93E-07	2.35E-15	2.38E-15	3.48E-07	3.83E-07
7	2.00E-13	1.00E-10	4.00E-15	4.00E-15	4.32E-15	4.37E-15	3.22E-07	3.71E-07	4.28E-15	4.36E-15	2.84E-07	3.58E-07
8	2.00E-13	1.00E-09	4.00E-15	4.00E-15	4.32E-15	4.37E-15	3.22E-07	3.70E-07	4.28E-15	4.36E-15	2.82E-07	3.60E-07
9	2.00E-13	1.00E-08	4.00E-15	4.00E-15	4.32E-15	4.37E-15	3.22E-07	3.70E-07	4.29E-15	4.35E-15	2.85E-07	3.53E-07
10	2.00E-13	5.00E-08	4.00E-15	4.00E-15	4.32E-15	4.37E-15	3.20E-07	3.70E-07	4.28E-15	4.36E-15	2.83E-07	3.58E-07
11	2.00E-13	1.00E-07	4.00E-15	4.00E-15	4.32E-15	4.37E-15	3.23E-07	3.69E-07	4.28E-15	4.35E-15	2.82E-07	3.52E-07
12	2.00E-13	1.00E-06	4.00E-15	4.00E-15	4.34E-15	4.35E-15	3.35E-07	3.52E-07	4.28E-15	4.34E-15	2.82E-07	3.41E-07
13	1.50E-12	1.00E-10	3.00E-14	3.00E-14	1.61E-14	2.92E-15	1.39E-05	-2.71E-05	1.24E-14	4.68E-15	1.76E-05	-2.53E-05
14	1.50E-12	1.00E-09	3.00E-14	3.00E-14	1.61E-14	2.92E-15	1.39E-05	-2.71E-05	1.24E-14	4.68E-15	1.76E-05	-2.53E-05
15	1.50E-12	1.00E-08	3.00E-14	3.00E-14	1.61E-14	2.94E-15	1.39E-05	-2.71E-05	1.24E-14	4.68E-15	1.76E-05	-2.53E-05
16	1.50E-12	5.00E-08	3.00E-14	3.00E-14	1.60E-14	3.01E-15	1.40E-05	-2.70E-05	1.24E-14	4.71E-15	1.76E-05	-2.53E-05
17	1.50E-12	1.00E-07	3.00E-14	3.00E-14	1.59E-14	3.09E-15	1.41E-05	-2.69E-05	1.23E-14	4.75E-15	1.77E-05	-2.53E-05
18	1.50E-12	1.00E-06	3.00E-14	3.00E-14	1.43E-14	4.24E-15	1.57E-05	-2.58E-05	1.14E-14	5.26E-15	1.86E-05	-2.47E-05
19	3.00E-12	1.00E-10	6.00E-14	6.00E-14	1.83E-14	1.62E-15	4.17E-05	-5.84E-05	1.55E-14	2.78E-15	4.45E-05	-5.72E-05
20	3.00E-12	1.00E-09	6.00E-14	6.00E-14	1.83E-14	1.63E-15	4.17E-05	-5.84E-05	1.55E-14	2.78E-15	4.45E-05	-5.72E-05
21	3.00E-12	1.00E-08	6.00E-14	6.00E-14	1.83E-14	1.65E-15	4.17E-05	-5.84E-05	1.55E-14	2.79E-15	4.46E-05	-5.72E-05
22	3.00E-12	5.00E-08	6.00E-14	6.00E-14	1.82E-14	1.74E-15	4.18E-05	-5.83E-05	1.54E-14	2.85E-15	4.46E-05	-5.72E-05
23	3.00E-12	1.00E-07	6.00E-14	6.00E-14	1.80E-14	1.86E-15	4.20E-05	-5.81E-05	1.53E-14	2.93E-15	4.47E-05	-5.71E-05
24	3.00E-12	1.00E-06	6.00E-14	6.00E-14	1.59E-14	3.55E-15	4.41E-05	-5.65E-05	1.37E-14	4.06E-15	4.63E-05	-5.59E-05
25	4.00E-12	1.00E-10	8.00E-14	8.00E-14	1.89E-14	1.31E-15	6.11E-05	-7.87E-05	1.65E-14	2.19E-15	6.35E-05	-7.78E-05
26	4.00E-12	1.00E-09	8.00E-14	8.00E-14	1.89E-14	1.31E-15	6.11E-05	-7.87E-05	1.65E-14	2.19E-15	6.35E-05	-7.78E-05
27	4.00E-12	1.00E-08	8.00E-14	8.00E-14	1.89E-14	1.33E-15	6.11E-05	-7.87E-05	1.65E-14	2.21E-15	6.35E-05	-7.78E-05
28	4.00E-12	5.00E-08	8.00E-14	8.00E-14	1.88E-14	1.44E-15	6.13E-05	-7.86E-05	1.64E-14	2.28E-15	6.36E-05	-7.77E-05
29	4.00E-12	1.00E-07	8.00E-14	8.00E-14	1.86E-14	1.57E-15	6.14E-05	-7.84E-05	1.63E-14	2.37E-15	6.37E-05	-7.76E-05
30	4.00E-12	1.00E-06	8.00E-14	8.00E-14	1.64E-14	3.40E-15	6.37E-05	-7.66E-05	1.45E-14	3.71E-15	6.55E-05	-7.63E-05
31	5.00E-12	1.00E-10	1.00E-13	1.00E-13	1.93E-14	1.13E-15	8.08E-05	-9.89E-05	1.72E-14	1.83E-15	8.28E-05	-9.82E-05
32	5.00E-12	1.00E-09	1.00E-13	1.00E-13	1.93E-14	1.13E-15	8.08E-05	-9.89E-05	1.72E-14	1.83E-15	8.28E-05	-9.82E-05
33	5.00E-12	1.00E-08	1.00E-13	1.00E-13	1.92E-14	1.16E-15	8.08E-05	-9.88E-05	1.71E-14	1.84E-15	8.29E-05	-9.82E-05
34	5.00E-12	5.00E-08	1.00E-13	1.00E-13	1.91E-14	1.27E-15	8.09E-05	-9.87E-05	1.71E-14	1.92E-15	8.30E-05	-9.81E-05
35	5.00E-12	1.00E-07	1.00E-13	1.00E-13	1.90E-14	1.40E-15	8.10E-05	-9.86E-05	1.69E-14	2.02E-15	8.31E-05	-9.80E-05
36	5.00E-12	1.00E-06	1.00E-13	1.00E-13	1.66E-14	3.33E-15	8.34E-05	-9.67E-05	1.50E-14	3.50E-15	8.50E-05	-9.65E-05

Fig 35 : Dynamic Power and Internal Energy Computation Tables

A.3. The Final .lib

```
/*
delay model :       typ
check model :       typ
power model :       typ
capacitance model : typ
other model :       typ
*/
library(gscl45nm) {

delay_model :table_lookup;
in_place_swap_mode :match_footprint;

  /* unit attributes */
time_unit : "1us";
voltage_unit : "1V";
current_unit : "1uA";
pulling_resistance_unit : "1kohm";
leakage_power_unit : "1nW";
capacitive_load_unit (1,pf);

slew_upper_threshold_pct_rise : 80;
slew_lower_threshold_pct_rise : 20;
slew_upper_threshold_pct_fall : 80;
slew_lower_threshold_pct_fall : 20;
input_threshold_pct_rise : 50;
input_threshold_pct_fall : 50;
output_threshold_pct_rise : 50;
output_threshold_pct_fall : 50;
nom_process : 1;
nom_voltage : 1.1;
nom_temperature : 27;
operating_conditions( typical ) {
process : 1;
voltage : 0.2;
temperature : 27;
  }
default_operating_conditions : typical;

lu_table_template(delay_template_4x5) {
    variable_1 :total_output_net_capacitance;
    variable_2 :input_net_transition;
    index_1 ("1000.0, 1001.0, 1002.0, 1003.0");
    index_2 ("1000.0, 1001.0, 1002.0, 1003.0, 1004.0");
  }
lu_table_template(delay_template_5x1) {
    variable_1 :input_net_transition;
    index_1 ("1000.0, 1001.0, 1002.0, 1003.0, 1004.0");
  }
lu_table_template(delay_template_6x1) {
    variable_1 :input_net_transition;
    index_1 ("1000.0, 1001.0, 1002.0, 1003.0, 1004.0, 1005.0");
  }
lu_table_template(delay_template_6x6) {
    variable_1 :total_output_net_capacitance;
    variable_2 :input_net_transition;
    index_1 ("1000.0, 1001.0, 1002.0, 1003.0, 1004.0, 1005.0");
    index_2 ("1000.0, 1001.0, 1002.0, 1003.0, 1004.0, 1005.0");
  }
power_lut_template(energy_template_4x5) {
    variable_1 :total_output_net_capacitance;
    variable_2 :input_transition_time;
    index_1 ("1000.0, 1001.0, 1002.0, 1003.0");
    index_2 ("1000.0, 1001.0, 1002.0, 1003.0, 1004.0");
  }
power_lut_template(energy_template_6x6) {
```

```
    variable_1 :total_output_net_capacitance;
    variable_2 :input_transition_time;
    index_1 ("1000.0, 1001.0, 1002.0, 1003.0, 1004.0, 1005.0");
    index_2 ("1000.0, 1001.0, 1002.0, 1003.0, 1004.0, 1005.0");
  }
lu_table_template(hold_template_3x6) {
    variable_1 :related_pin_transition;
    variable_2 :constrained_pin_transition;
    index_1 ("1000.0, 1001.0, 1002.0");
    index_2 ("1000.0, 1001.0, 1002.0, 1003.0, 1004.0, 1005.0");
  }
power_lut_template(passive_energy_template_5x1) {
    variable_1 :input_transition_time;
    index_1 ("1000.0, 1001.0, 1002.0, 1003.0, 1004.0");
  }
power_lut_template(passive_energy_template_6x1) {
    variable_1 :input_transition_time;
    index_1 ("1000.0, 1001.0, 1002.0, 1003.0, 1004.0, 1005.0");
  }
lu_table_template(recovery_template_3x6) {
    variable_1 :related_pin_transition;
    variable_2 :constrained_pin_transition;
    index_1 ("1000.0, 1001.0, 1002.0");
    index_2 ("1000.0, 1001.0, 1002.0, 1003.0, 1004.0, 1005.0");
  }
lu_table_template(recovery_template_6x6) {
    variable_1 :related_pin_transition;
    variable_2 :constrained_pin_transition;
    index_1 ("1000.0, 1001.0, 1002.0, 1003.0, 1004.0, 1005.0");
    index_2 ("1000.0, 1001.0, 1002.0, 1003.0, 1004.0, 1005.0");
  }
lu_table_template(removal_template_3x6) {
    variable_1 :related_pin_transition;
    variable_2 :constrained_pin_transition;
    index_1 ("1000.0, 1001.0, 1002.0");
    index_2 ("1000.0, 1001.0, 1002.0, 1003.0, 1004.0, 1005.0");
  }
lu_table_template(setup_template_3x6) {
    variable_1 :related_pin_transition;
    variable_2 :constrained_pin_transition;
    index_1 ("1000.0, 1001.0, 1002.0");
    index_2 ("1000.0, 1001.0, 1002.0, 1003.0, 1004.0, 1005.0");
  }



/* -------------- *
 * Design : INVX1 *
 * -------------- */
cell (INVX1) {
cell_footprint :inv;
area : 0.77885;
cell_leakage_power : 0.03384;
pin(A)  {
direction : input;
capacitance : 0.0000261;
rise_capacitance :  0.0000261;
fall_capacitance :  0.0000261;

  }
pin(Y)  {
direction : output;
capacitance : 0;
rise_capacitance : 0;
fall_capacitance : 0;
max_capacitance : 0.238796;
function : "(!A)";
timing() {
```

```
related_pin : "A";
timing_sense :negative_unate;
cell_rise(delay_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.1, 1.0, 10.0");
values ( \
           "0.5989, 0.5997, 0.6019, 0.6276, 0.8958, 2.9771", \
           "1.1882, 1.1898, 1.1907, 1.2141, 1.4809, 4.0741", \
           "8.8428, 8.8431, 8.8601, 8.8756, 9.1275, 11.7904", \
           "17.7007, 17.7035, 17.7081, 17.7143, 17.9851, 20.5668", \
           "23.5859, 23.5946, 23.6008, 23.6094, 23.8528, 26.4527", \
           "29.4543, 29.4678, 29.4938, 29.5072, 29.744, 32.3421"); }

rise_transition(delay_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.1, 1.0, 10.0");
values ( \
          "1.2515, 1.2496, 1.2468, 1.2506, 1.2881, 4.0651", \
"2.4852, 2.4862, 2.4885, 2.4799, 2.4871, 4.7129", \
"18.5684, 18.5031, 18.492, 18.4882, 18.5651, 18.6495", \
"37.0426, 37.0013, 36.9986, 37.0318, 37.0744, 36.9866", \
"49.3608, 49.3844, 49.375, 49.281, 49.4806, 49.4204", \
"61.7279, 61.7079, 61.6734, 61.5987, 61.706, 61.6678");
      }
cell_fall(delay_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.1, 1.0, 10.0");
values ( \
          "0.5328, 0.5337, 0.5358, 0.5603, 0.8251, 2.6591", \
         "1.0556, 1.058, 1.0595, 1.0849, 1.3449, 3.7833", \
         "7.8544, 7.8631, 7.8718, 7.8924, 8.1347, 10.7808", \
         "15.7096, 15.7121, 15.7128, 15.7345, 16.0093, 18.5947", \
         "20.9329, 20.9373, 20.9838, 20.9927, 21.1906, 23.7584", \
         "26.1654, 26.1725, 26.2019, 26.2387, 26.4624, 29.0311");
      }
fall_transition(delay_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.1, 1.0, 10.0");
values ( \
          "1.0576, 1.0575, 1.0567, 1.0551, 1.1055, 4.0503", \
"2.0967, 2.1022, 2.1007, 2.101, 2.104, 4.5912", \
"15.6524, 15.6405, 15.6778, 15.6698, 15.6754, 15.86", \
"31.2665, 31.3154, 31.2945, 31.3299, 31.3421, 31.3574", \
"41.6832, 41.7933, 41.7458, 41.7865, 41.6744, 41.6976", \
"52.136, 52.1189, 52.2307, 52.2066, 52.2171, 52.2206");
      }
    }
internal_power() {
related_pin : "A";
rise_power(energy_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
       index_2 ("0.0001, 0.001, 0.01, 0.05, 0.1, 1");
values ( \
          "0.0000001793, 0.0000001788, 0.0000001780, 0.0000001811, 0.0000001795,
0.0000001777", \
"0.0000001517, 0.0000001515, 0.0000001517, 0.0000001528, 0.0000001506,
0.0000001483", \
"0.0000274300, 0.0000274300, 0.0000274100, 0.0000273500, 0.0000272700,
0.0000262400", \
"0.0000586900, 0.0000586900, 0.0000586700, 0.0000585800, 0.0000584700,
0.0000570000", \
"0.0000790200, 0.0000790100, 0.0000789900, 0.0000788900, 0.0000787700,
0.0000771800", \
"0.0000992100, 0.0000992100, 0.0000991800, 0.0000990800, 0.0000989500,
0.0000972800");

      }
fall_power(energy_template_6x6) {
```

```
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.05, 0.1, 1");
values ( \
          "0.0000002075, 0.0000002073, 0.0000002075, 0.0000002044, 0.0000002053,
0.0000001986", \
"0.0000001929, 0.0000001918, 0.0000001914, 0.0000001929, 0.0000001974,
0.0000001854", \
"-0.0000147300, -0.0000147400, -0.0000147500, -0.0000148200, -0.0000149100, -
0.0000163500", \
"-0.0000427000, -0.0000427000, -0.0000427200, -0.0000428200, -0.0000429400, -
0.0000447900", \
"-0.0000621300, -0.0000621300, -0.0000621600, -0.0000622600, -0.0000623900, -
0.0000643600", \
"-0.0000817800, -0.0000817800, -0.0000818100, -0.0000819100, -0.0000820500, -
0.0000840900");
      }
    }
  }
}


/* -------------- *
 * Design : INVX4 *
 * -------------- */
cell (INVX4) {
cell_footprint :inv;
area : 1.1840625;
cell_leakage_power : 0.1393;
pin(A)  {
direction : input;
capacitance : 0.0001085;
rise_capacitance : 0.0001085;
fall_capacitance : 0.0001085;
  }
pin(Y)  {
direction : output;
capacitance : 0;
rise_capacitance : 0;
fall_capacitance : 0;
max_capacitance : 1.04105;
function : "(!A)";
timing() {
related_pin : "A";
timing_sense :negative_unate;
cell_rise(delay_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3.0, 4.0, 5.0");
        index_2 ("0.0001, 0.001, 0.01, 0.1, 1.0, 10.0");
values ( \
          "0.1546, 0.1549, 0.1577, 0.1838, 0.4543, 1.4669", \
"0.3006, 0.3012, 0.3032, 0.3293, 0.6019, 2.1044", \
"2.1966, 2.1974, 2.2, 2.2248, 2.4863, 5.2189", \
"4.3909, 4.3921, 4.3924, 4.4109, 4.6621, 7.3656", \
"5.8417, 5.8498, 5.8536, 5.8734, 6.1348, 8.8087", \
"7.2942, 7.3057, 7.314, 7.3343, 7.5862, 10.2574");
      }
rise_transition(delay_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3.0, 4.0, 5.0");
        index_2 ("0.0001, 0.001, 0.01, 0.1, 1.0, 10.0");
values ( \
          "0.319, 0.3192, 0.3195, 0.3195, 0.5112, 2.9515", \
"0.6247, 0.6264, 0.6251, 0.6255, 0.7349, 3.4546", \
"4.6003, 4.5964, 4.5922, 4.5969, 4.597, 6.0996", \
"9.1879, 9.1929, 9.1691, 9.1981, 9.1687, 9.9005", \
"12.2326, 12.2162, 12.2409, 12.213, 12.2546, 12.6284", \
"15.2696, 15.2763, 15.2681, 15.3133, 15.2904, 15.5481");
      }
cell_fall(delay_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3.0, 4.0, 5.0");
```

```
        index_2 ("0.0001, 0.001, 0.01, 0.1, 1.0, 10.0");
values ( \
          "0.133, 0.1335, 0.1359, 0.1614, 0.4189, 1.0437", \
"0.2579, 0.2588, 0.2607, 0.286, 0.554, 1.6941", \
"1.8835, 1.8864, 1.8889, 1.9119, 2.1728, 4.8571", \
"3.759, 3.762, 3.7634, 3.7931, 4.0459, 6.7016", \
"5.0164, 5.0196, 5.0202, 5.0425, 5.2947, 7.9399", \
"6.2742, 6.2749, 6.2759, 6.2882, 6.5352, 9.18");
      }
fall_transition(delay_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3.0, 4.0, 5.0");
        index_2 ("0.0001, 0.001, 0.01, 0.1, 1.0, 10.0");
values ( \
          "0.2601, 0.2605, 0.2604, 0.2597, 0.4789, 2.9623", \
"0.5091, 0.5099, 0.5096, 0.51, 0.6444, 3.4705", \
"3.7537, 3.749, 3.7546, 3.7525, 3.7545, 5.5341", \
"7.4939, 7.4872, 7.4928, 7.4941, 7.4956, 8.3983", \
"9.9964, 9.9911, 9.9949, 9.9923, 9.9915, 10.5581", \
"12.4967, 12.4969, 12.4851, 12.4741, 12.4641, 12.8486");
      }
    }
internal_power() {
related_pin : "A";
rise_power(energy_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3.0, 4.0, 5.0");
        index_2 ("0.0001, 0.001, 0.01, 0.05, 0.1, 1");
values ( \
          "0.0000007513, 0.0000007521, 0.0000007514, 0.0000007525, 0.0000007529,
0.0000007584", \
"0.0000007396, 0.0000007422, 0.0000007407, 0.0000007449, 0.0000007408,
0.0000007387", \
"0.0000051300, 0.0000051270, 0.0000051320, 0.0000050860, 0.0000050960,
0.0000051060", \
"0.0000414100, 0.0000414600, 0.0000414300, 0.0000413000, 0.0000410900,
0.0000393600", \
"0.0000650100, 0.0000650200, 0.0000649800, 0.0000647900, 0.0000645700,
0.0000618400", \
"0.0000875600, 0.0000875600, 0.0000875000, 0.0000872800, 0.0000870000,
0.0000835400");
      }
fall_power(energy_template_6x6) {
        index_1 ("0.01, 0.02, 1.5, 3.0, 4.0, 5.0");
        index_2 ("0.0001, 0.001, 0.01, 0.05, 0.1, 1");
values ( \
          "0.0000008763, 0.0000008741, 0.0000008755, 0.0000008731, 0.0000008716,
0.0000008483", \
"0.0000008643, 0.0000008616, 0.0000008628, 0.0000008598, 0.0000008589,
0.0000008359", \
"0.0000003609, 0.0000003607, 0.0000003570, 0.0000003302, 0.0000003080, -
0.0000002189", \
"-0.0000116800, -0.0000116800, -0.0000117200, -0.0000118700, -0.0000120800, -
0.0000153500", \
"-0.0000254800, -0.0000255000, -0.0000255400, -0.0000257700, -0.0000260400, -
0.0000304100", \
"-0.0000413400, -0.0000413400, -0.0000414100, -0.0000416600, -0.0000419900, -
0.0000471300");
      }
    }
  }
}


/* ---------------- *
 * Design : NAND2X1 *
 * ---------------- */
cell (NAND2X1) {
area : 1.1840625;
cell_leakage_power : 0.05887;
```

```
pin(A)  {
direction : input;
capacitance : 0.000049545 ;
rise_capacitance : 0.00004954;
fall_capacitance : 0.00004955;
;
  }
pin(B)  {
direction : input;
capacitance : 0.000025295;
rise_capacitance : 0.00002525;
fall_capacitance : 0.00002534;  }
pin(Y)  {
direction : output;
capacitance : 0;
rise_capacitance : 0;
fall_capacitance : 0;
max_capacitance : 0;
function : "(!(A B))";
timing() {
related_pin : "A";
timing_sense :negative_unate;
cell_rise(delay_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.1, 1.0, 10.0");
values ( \
            "0.6049,0.6053,0.6078,0.6324,0.9003,3.1681", \
"1.1926,1.193,1.1957,1.2198,1.4842,4.1683", \
"8.8212,8.8373,8.8411,8.8633,9.1081,11.7646", \
"17.6293,17.6486,17.6617,17.6655,17.9161,20.5183", \
"23.487,23.5187,23.5276,23.5726,23.7943,26.4106", \
"29.4097,29.4219,29.4244,29.4384,29.6448,32.2061");
   }
rise_transition(delay_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.1, 1.0, 10.0");
values ( \
        "1.2715,1.2716,1.2707,1.2681,1.308,3.8943", \
"2.5124,2.5076,2.5136,2.5109,2.514,4.6088", \
"18.6188,18.621,18.6588,18.6655,18.6489,18.7619", \
"37.2546,37.2072,37.2566,37.2059,37.2753,37.2554", \
"49.5934,49.6161,49.5937,49.6549,49.6199,49.6607", \
"62.1233,62.0611,62.2289,62.0783,61.9995,62.0233");
        }
cell_fall(delay_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.1, 1.0, 10.0");
values ( \
              "0.5576,0.5595,0.5602,0.5772,0.7634,1.665", \
"1.0979,1.0996,1.1007,1.1172,1.2979,2.7976", \
"8.1279,8.1397,8.1439,8.158,8.3242,10.1544", \
"16.2361,16.2557,16.2582,16.2698,16.4648,18.2247", \
"21.6558,21.69,21.7004,21.743,21.8463,23.6435", \
"27.0571,27.0572,27.1103,27.1313,27.2679,29.0965");
  }
fall_transition(delay_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.1, 1.0, 10.0");
values ( \
"1.0535,1.0518,1.053,1.0511,1.1312,4.0705", \
"2.08,2.0823,2.0833,2.0819,2.0985,4.8697", \
"15.4298,15.429,15.4479,15.4464,15.4332,15.8304", \
"30.8909,30.8799,30.8904,30.8136,30.9021,30.898", \
"41.1857,41.1625,41.1728,41.1342,41.2071,41.1775", \
"51.4405,51.4409,51.4674,51.5016,51.4698,51.3903");
    }
    }
timing() {
```

```
related_pin : "B";
timing_sense :negative_unate;
cell_rise(delay_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.1, 1.0, 10.0");
values ( \
         "0.6092,0.6098,0.6112,0.6371,0.904,3.1737", \
"1.1957,1.1978,1.1996,1.224,1.4851,4.1713", \
"8.8407,8.8414,8.8418,8.8586,9.0891,11.7655", \
"17.636,17.64,17.6509,17.6854,17.8995,20.5141", \
"23.4874,23.4994,23.5264,23.5318,23.7691,26.3408", \
"29.3883,29.4036,29.4094,29.4154,29.643,32.2364");

      }
rise_transition(delay_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.1, 1.0, 10.0");
values ( \
           "1.277,1.2785,1.2779,1.277,1.3118,3.8985", \
"2.5173,2.5133,2.5112,2.5198,2.5169,4.6057", \
"18.6324,18.649,18.6237,18.6386,18.6486,18.7285", \
"37.2348,37.1806,37.1943,37.1745,37.1792,37.2039", \
"49.686,49.6675,49.6226,49.5683,49.5478,49.5298", \
"62.0796,61.8867,61.8855,62.055,61.9048,61.994");
    }
cell_fall(delay_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.1, 1.0, 10.0");
values ( \
            "0.5601,0.5602,0.5631,0.5856,0.7952,1.8861", \
"1.1015,1.1029,1.1075,1.1266,1.336,3.0374", \
"8.1396,8.1397,8.1437,8.1782,8.3836,10.4944", \
"16.2862,16.291,16.2944,16.3234,16.5603,18.5559", \
"21.6954,21.7,21.7152,21.7319,21.911,24.0459", \
"27.0937,27.1075,27.1221,27.1798,27.3745,29.403");
    }
fall_transition(delay_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.1, 1.0, 10.0");
values ( \
            "1.0532,1.0511,1.0521,1.0528,1.1163,3.8748", \
"2.0787,2.0828,2.0822,2.0813,2.0915,4.655", \
"15.4496,15.416,15.4261,15.4621,15.4256,15.7489", \
"30.8473,30.8233,30.856,30.9081,30.8437,30.8744", \
"41.178,41.1711,41.1806,41.1582,41.1572,41.1859", \
"51.4105,51.4386,51.3696,51.5154,51.4857,51.4685");
    }
    }
internal_power() {
related_pin : "A";
rise_power(energy_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.05, 0.1, 1");
values ( \
          "0.000000341 , 0.000000340 , 0.000000340, 0.000000340, 0.000000340,
0.000000343", \
"0.000000287, 0.000000285, 0.000000294, 0.000000287, 0.000000289, 0.000000284", \
"0.000027230, 0.000027230, 0.000027210, 0.000027160, 0.000027090, 0.000026190", \
"0.000058470, 0.000058470, 0.000058450, 0.000058370, 0.000058270, 0.000056960", \
"0.000078800, 0.000078800, 0.000078780, 0.000078690, 0.000078580, 0.000077140", \
"0.000098990, 0.000098980, 0.000098970, 0.000098880, 0.000098760, 0.000097250");
 }
fall_power(energy_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.05, 0.1, 1");
values ( \
          "0.000000407, 0.000000406, 0.000000404, 0.000000405, 0.000000404,
0.000000394", \
```

```
"0.000000371, 0.000000373, 0.000000369, 0.000000371, 0.000000370, 0.000000359", \
"-0.000014780, -0.000014780, -0.000014790, -0.000014870, -0.000014960, -
0.000016500", \
"-0.000042780, -0.000042780, -0.000042800, -0.000042890, -0.000043010, -
0.000044990", \
"-0.000062220, -0.000062220, -0.000062240, -0.000062350, -0.000062480, -
0.000064580", \
"-0.000081870, -0.000081880, -0.000081900, -0.000082010, -0.000082140, -
0.000084320");
      }
    }
internal_power() {
related_pin : "B";
rise_power(energy_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.05, 0.1, 1");
values ( \
          "-0.000001676, -0.000001676, -0.000001675, -0.000001675, -0.000001674, -
0.000001660", \
"0.000003676, 0.000003676, 0.000003675, 0.000003675, 0.000003674, 0.000003660", \
"0.000029630, 0.000029630, 0.000029630, 0.000029630, 0.000029630, 0.000029610", \
"0.000059550, 0.000059550, 0.000059550, 0.000059550, 0.000059550, 0.000059540", \
"0.000079540, 0.000079540, 0.000079540, 0.000079540, 0.000079530, 0.000079530", \
"0.000099540, 0.000099540, 0.000099540, 0.000099540, 0.000099540, 0.000099530");

      }
fall_power(energy_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.05, 0.1, 1");
values ( \
          "-0.000001531, -0.000001531, -0.000001531, -0.000001532, -0.000001533, -
0.000001551", \
"-0.000003531, -0.000003531, -0.000003531, -0.000003532, -0.000003533, -
0.000003551", \
"-0.000029270, -0.000029270, -0.000029260, -0.000029260, -0.000029260, -
0.000029220", \
"-0.000059280, -0.000059280, -0.000059280, -0.000059280, -0.000059280, -
0.000059270", \
"-0.000079320, -0.000079320, -0.000079320, -0.000079320, -0.000079320, -
0.000079320", \
"-0.000099360, -0.000099360, -0.000099360, -0.000099360, -0.000099360, -
0.000099360");
      }
    }
  }
}


/* --------------- *
 * Design : NOR2X1 *
 * --------------- */
cell (NOR2X1) {
area : 1.1840625;
cell_leakage_power : 0.05271;
pin(A)  {
direction : input;
capacitance : 0.00003037 ;
rise_capacitance : 0.00003037;
fall_capacitance : 0.00003037; }
pin(B)  {
direction : input;
capacitance : 0.00003037 ;
rise_capacitance : 0.00003037;
fall_capacitance : 0.00003037; }
pin(Y)  {
direction : output;
capacitance : 0;
rise_capacitance : 0;
```

```
fall_capacitance : 0;
max_capacitance : 0;
function : "(!(A+B))";
timing() {
related_pin : "A";
timing_sense :negative_unate;
cell_rise(delay_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.1, 1.0, 10.0");
values ( \
          "0.7111, 0.7117, 0.7156, 0.7391, 0.9558, 2.4445", \
"1.392, 1.3925, 1.3952, 1.4227, 1.6363, 3.6254", \
"10.2372, 10.243, 10.2433, 10.3068, 10.4677, 12.5987", \
"20.4226, 20.433, 20.4364, 20.49, 20.6653, 22.7391", \
"27.2291, 27.2594, 27.2608, 27.2997, 27.4874, 29.5807", \
"34.0191, 34.0762, 34.0895, 34.0937, 34.3048, 36.429");
      }
rise_transition(delay_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.1, 1.0, 10.0");
values ( \
           "1.3698, 1.3665, 1.367, 1.3666, 1.4031, 3.9725", \
"2.7035, 2.7022, 2.706, 2.7064, 2.7034, 4.8429", \
"20.0623, 20.0389, 20.067, 20.0848, 20.0278, 20.184", \
"40.0612, 40.1669, 40.1334, 40.0549, 40.0248, 40.0636", \
"53.3577, 53.4211, 53.3966, 53.4012, 53.4277, 53.4089", \
"66.7066, 66.8689, 66.9134, 66.8519, 66.7177, 66.9261");

      }
cell_fall(delay_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.1, 1.0, 10.0");
values ( \
          "0.5489, 0.5503, 0.5524, 0.5759, 0.8398, 2.8379", \
"1.068, 1.0685, 1.0722, 1.0959, 1.3565, 3.862", \
"7.8148, 7.8158, 7.8173, 7.8399, 8.0837, 10.7077", \
"15.5964, 15.6004, 15.6008, 15.6198, 15.8829, 18.4576", \
"20.7806, 20.8074, 20.8078, 20.8353, 21.0698, 23.6036", \
"25.9602, 25.9773, 25.9869, 26.0216, 26.2663, 28.8025");
      }
fall_transition(delay_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.1, 1.0, 10.0");
values ( \
          "1.089, 1.0888, 1.086, 1.0871, 1.1371, 3.9598", \
"2.132, 2.1316, 2.129, 2.127, 2.132, 4.5415", \
"15.67, 15.6632, 15.669, 15.6943, 15.6949, 15.852", \
"31.3275, 31.3152, 31.3486, 31.3465, 31.2951, 31.3014", \
"41.7756, 41.6639, 41.7523, 41.6974, 41.6613, 41.78", \
"52.2036, 52.2296, 52.0781, 52.0853, 52.0851, 52.0796");
      }
    }
timing() {
related_pin : "B";
timing_sense :negative_unate;
cell_rise(delay_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.1, 1.0, 10.0");
values ( \
          "0.7018,0.702,0.7022,0.7218,0.9033,2.1654", \
"1.3817,1.383,1.3857,1.3989,1.5761,3.3352", \
"10.2127,10.2216,10.2264,10.2285,10.4096,12.2014", \
"20.3986,20.4131,20.4227,20.4254,20.6388,22.3695", \
"27.1889,27.203,27.2306,27.2318,27.3933,29.1653", \
"33.985,33.9971,34.0111,34.0272,34.2233,35.9448");


      }
```

```
rise_transition(delay_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.1, 1.0, 10.0");
values ( \
          "1.3688,1.3692,1.3703,1.3686,1.421,4.2079", \
"2.7078,2.7073,2.7058,2.7007,2.7074,5.1175", \
"20.0806,20.0537,20.0546,20.0336,20.0881,20.2561", \
"40.0502,40.0353,40.0997,40.1331,40.094,40.1054", \
"53.4925,53.3991,53.4776,53.5419,53.4014,53.5514", \
"66.7396,66.8454,66.835,66.6722,66.7207,66.8396");
    }
cell_fall(delay_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.1, 1.0, 10.0");
values ( \
         "0.5365,0.537,0.5391,0.5649,0.827,2.8095", \
"1.0542,1.0551,1.0569,1.0846,1.3424,3.8428", \
"7.7977,7.8064,7.8184,7.8341,8.0925,10.7104", \
"15.5936,15.6,15.6189,15.6236,15.8903,18.4632", \
"20.798,20.8003,20.8172,20.8356,21.0391,23.6025", \
"25.9408,25.966,25.9948,26.0107,26.2126,28.7479");

      }
fall_transition(delay_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.1, 1.0, 10.0");
values ( \
          "1.0684,1.0681,1.0671,1.068,1.1162,3.9601", \
"2.1111,2.1072,2.1083,2.1123,2.1154,4.5366", \
"15.6916,15.6785,15.6865,15.685,15.6776,15.8744", \
"31.3346,31.3562,31.3261,31.3236,31.354,31.3526", \
"41.7289,41.8095,41.7841,41.7882,41.7457,41.7701", \
"52.1746,52.1136,52.2381,52.1341,52.1218,52.1722");
     }
    }
internal_power() {
related_pin : "A";
rise_power(energy_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.05, 0.1, 1");
values ( \
          "0.000000350, 0.000000350, 0.000000350, 0.000000350, 0.000000351,
0.000000363", \
"0.000000322, 0.000000322, 0.000000322, 0.000000320, 0.000000323, 0.000000335", \
"0.000013900, 0.000013900, 0.000013900, 0.000014000, 0.000014100, 0.000015700", \
"0.000041700, 0.000041700, 0.000041700, 0.000041800, 0.000042000, 0.000044100", \
"0.000061100, 0.000061100, 0.000061100, 0.000061300, 0.000061400, 0.000063700", \
"0.000080800, 0.000080800, 0.000080800, 0.000080900, 0.000081000, 0.000083400");
      }
fall_power(energy_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.05, 0.1, 1");
values ( \
         "0.000000410, 0.000000410, 0.000000410, 0.000000409, 0.000000408,
0.000000393", \
"0.000000371, 0.000000370, 0.000000370, 0.000000370, 0.000000369, 0.000000352", \
"-0.000027100, -0.000027100, -0.000027100, -0.000027000, -0.000026900, -
0.000025800", \
"-0.000058400, -0.000058400, -0.000058400, -0.000058300, -0.000058100, -
0.000056500", \
"-0.000078700, -0.000078700, -0.000078700, -0.000078600, -0.000078400, -
0.000076600", \
"-0.000098900, -0.000098900, -0.000098800, -0.000098700, -0.000098600, -
0.000096700");
      }
    }
internal_power() {
related_pin : "B";
```

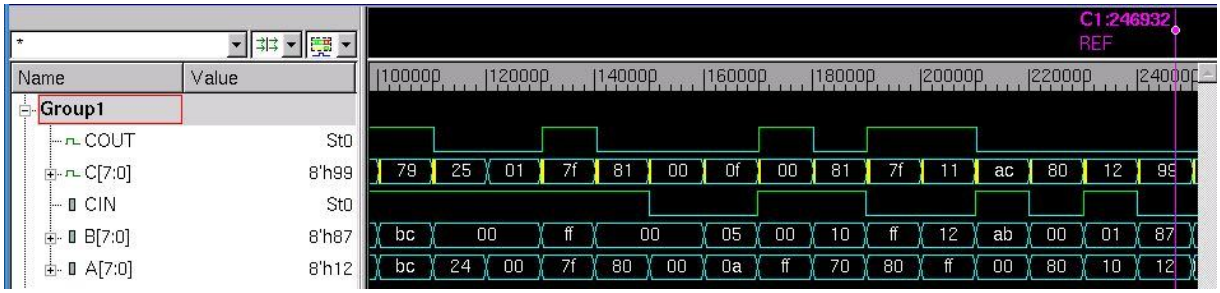
```
rise_power(energy_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.05, 0.1, 1");
values ( \
         "0.000000346, 0.000000348, 0.000000345, 0.000000345, 0.000000345,
0.000000348", \
"0.000000284, 0.000000282, 0.000000285, 0.000000283, 0.000000282, 0.000000282", \
"0.000017600, 0.000017600, 0.000017600, 0.000017600, 0.000017700, 0.000018600", \
"0.000044500, 0.000044500, 0.000044600, 0.000044600, 0.000044700, 0.000046300", \
"0.000063500, 0.000063500, 0.000063500, 0.000063600, 0.000063700, 0.000065500", \
"0.000082800, 0.000082800, 0.000082900, 0.000083000, 0.000083100, 0.000085000");
      }
fall_power(energy_template_6x6) {
        index_1 ("0.1, 0.2, 1.5, 3, 4, 5");
        index_2 ("0.0001, 0.001, 0.01, 0.05, 0.1, 1");
values ( \
         "0.000000392, 0.000000394, 0.000000392, 0.000000393, 0.000000390,
0.000000383", \
"0.000000358, 0.000000360, 0.000000353, 0.000000358, 0.000000352, 0.000000341", \
"-0.000025300, -0.000025300, -0.000025300, -0.000025300, -0.000025300, -
0.000024700", \
"-0.000057200, -0.000057200, -0.000057200, -0.000057200, -0.000057100, -
0.000055900", \
"-0.000077800, -0.000077800, -0.000077800, -0.000077700, -0.000077600, -
0.000076300", \
"-0.000098200, -0.000098200, -0.000098200, -0.000098100, -0.000098000, -
0.000096500");
      }
    }
  }
}

}
```

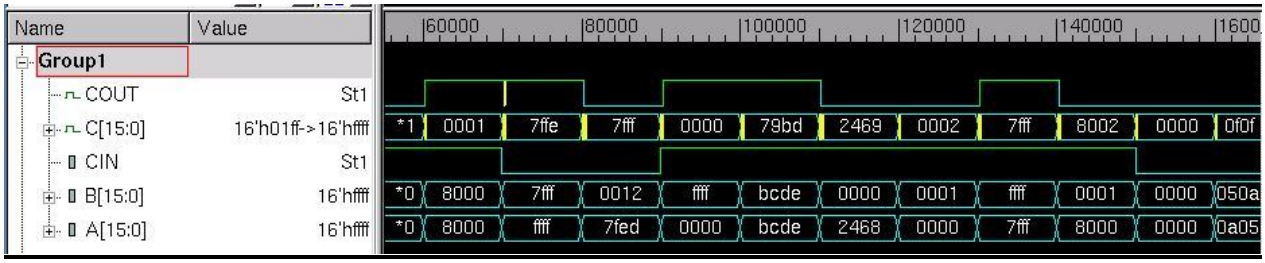
A.4 VCS Functional Verification waveforms for Kogge-Stone and Ladner-Fishcher Adders

A.4.1 KOGGE-STONE:

a) 8 bits:

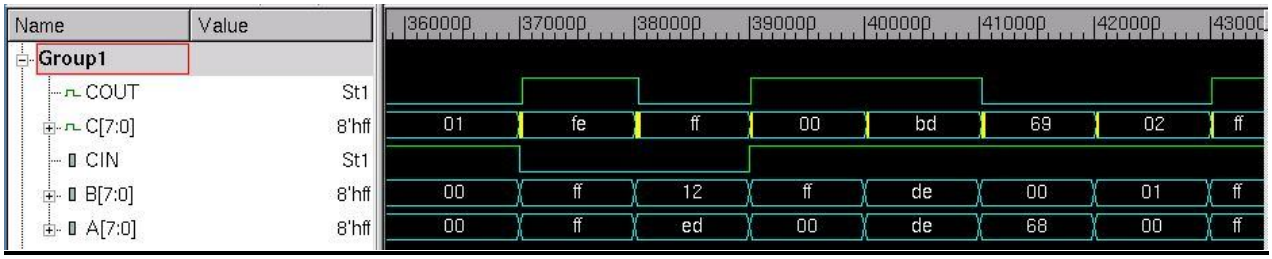


b) 16 bits:



A.4.2 LADNER-FISCHER:

a) 8 bits:



b) 16 bits:

A.5. Post Layout Critical Path Timing Reports: (Only the reports for the sub-threshold implementation is included)

A.5.1 KOGGE-STONE

a) 8 bit:

```
****************************************
Report : timing
       -path_type full
       -delay_type max
       -max_paths 1
Design : Kogge_8
Version: F-2011.06-SP1
Date   : Fri Dec 5 22:27:10 2015
****************************************


Startpoint: B[2] (input port)
```

```
  Endpoint: C[7] (output port)
  Path Group: (none)
  Path Type: max

  Point                                     Incr       Path
  -----------------------------------------------------------
input external delay                     0.00       0.00 r
B[2] (in)                                0.00       0.00 r
  I35/ip1 (gipi_cell)                      0.00       0.00 r
  I35/I6/Y (INVX1)                         0.01       0.01 f
  I35/I7/Y (NAND2X1)                       0.03       0.04 r
  I35/pi (gipi_cell)                       0.00       0.04 r
  I32/pi (prefix_block)                    0.00       0.04 r
  I32/I2/Y (NAND2X1)                       0.03       0.07 f
  I32/I3/Y (NAND2X1)                       0.02       0.09 r
  I32/I4/Y (INVX1)                         0.02       0.11 f
  I32/Gi_bar (prefix_block)                0.00       0.11 f
  I33/gi_bar (prefix_block)                0.00       0.11 f
  I33/I3/Y (NAND2X1)                       0.02       0.13 r
  I33/Gi (prefix_block)                    0.00       0.13 r
  I94/g_dash (prefix_block)                0.00       0.13 r
  I94/I2/Y (NAND2X1)                       0.03       0.16 f
  I94/I3/Y (NAND2X1)                       0.02       0.18 r
  I94/I4/Y (INVX1)                         0.02       0.21 f
  I94/Gi_bar (prefix_block)                0.00       0.21 f
  I110/Gi_bar (Cin)                        0.00       0.21 f
  I110/I1/Y (NAND2X1)                      0.02       0.23 r
  I110/Cout (Cin)                          0.00       0.23 r
  I117/ip1 (XOR_two_inputs)                0.00       0.23 r
  I117/I0/Y (INVX1)                        0.02       0.25 f
  I117/I2/Y (NAND2X1)                      0.02       0.27 r
  I117/I4/Y (NAND2X1)                      0.03       0.30 f
  I117/op (XOR_two_inputs)                 0.00       0.30 f
C[7] (out)                               0.00       0.30 f
data arrival time                                   0.30
  -----------------------------------------------------------
  (Path is unconstrained)
```

b) 16 bit:

```
****************************************
Report : timing
      -path_type full
      -delay_type max
      -max_paths 1
Design : Kogge_16
Version: F-2011.06-SP1
Date   : Fri Dec  5 22:30:02 2015
****************************************


Startpoint: B[2] (input port)
  Endpoint: C[15] (output port)
  Path Group: (none)
  Path Type: max

  Point                                     Incr       Path
  -----------------------------------------------------------
input external delay                     0.00       0.00 r
B[2] (in)                                0.00       0.00 r
```

```
  I35/ip1 (gipi_cell)                        0.00       0.00 r
  I35/I6/Y (INVX1)                           0.01       0.01 f
  I35/I7/Y (NAND2X1)                         0.03       0.04 r
  I35/pi (gipi_cell)                         0.00       0.04 r
  I32/pi (prefix_block)                      0.00       0.04 r
  I32/I2/Y (NAND2X1)                         0.03       0.07 f
  I32/I3/Y (NAND2X1)                         0.02       0.09 r
  I32/I4/Y (INVX1)                           0.02       0.11 f
  I32/Gi_bar (prefix_block)                  0.00       0.11 f
  I33/gi_bar (prefix_block)                  0.00       0.11 f
  I33/I3/Y (NAND2X1)                         0.02       0.13 r
  I33/Gi (prefix_block)                      0.00       0.13 r
  I94/g_dash (prefix_block)                  0.00       0.13 r
  I94/I2/Y (NAND2X1)                         0.03       0.16 f
  I94/I3/Y (NAND2X1)                         0.02       0.19 r
  I94/Gi (prefix_block)                      0.00       0.19 r
  I104/g_dash (prefix_block)                 0.00       0.19 r
  I104/I2/Y (NAND2X1)                        0.03       0.21 f
  I104/I3/Y (NAND2X1)                        0.02       0.24 r
  I104/I4/Y (INVX1)                          0.02       0.26 f
  I104/Gi_bar (prefix_block)                 0.00       0.26 f
  I133/Gi_bar (Cin)                          0.00       0.26 f
  I133/I1/Y (NAND2X1)                        0.02       0.28 r
  I133/Cout (Cin)                            0.00       0.28 r
  I130/ip1 (XOR_two_inputs)                  0.00       0.28 r
  I130/I0/Y (INVX1)                          0.02       0.30 f
  I130/I2/Y (NAND2X1)                        0.02       0.32 r
  I130/I4/Y (NAND2X1)                        0.03       0.35 f
  I130/op (XOR_two_inputs)                   0.00       0.35 f
C[15] (out)                                  0.00       0.35 f
data arrival time                                       0.35
  ---------------------------------------------------------------
  (Path is unconstrained)
```

A.5.2 LADNER FISCHER:

a) 8 bit:

```
****************************************
Report : timing
      -path_type full
      -delay_type max
      -max_paths 1
Design : Ladner_Fisher_8
Version: F-2011.06-SP1
Date   : Fri Dec  5 22:32:03 2015
****************************************


Startpoint: B[1] (input port)
  Endpoint: C[6] (output port)
  Path Group: (none)
  Path Type: max

  Point                                    Incr       Path
  ---------------------------------------------------------------
input external delay                       0.00       0.00 r
B[1] (in)                                  0.00       0.00 r
  I40/ip1 (gipi_cell)                        0.00       0.00 r
```

```
  I40/I6/Y (INVX1)                          0.01       0.01 f
  I40/I7/Y (NAND2X1)                        0.03       0.04 r
  I40/pi (gipi_cell)                        0.00       0.04 r
  I0/pi (prefix_block)                      0.00       0.04 r
  I0/I2/Y (NAND2X1)                         0.03       0.06 f
  I0/I3/Y (NAND2X1)                         0.02       0.09 r
  I0/Gi (prefix_block)                      0.00       0.09 r
  I46/g_dash (prefix_block)                 0.00       0.09 r
  I46/I2/Y (NAND2X1)                        0.03       0.12 f
  I46/I3/Y (NAND2X1)                        0.02       0.14 r
  I46/Gi (prefix_block)                     0.00       0.14 r
  I29/Y (INVX1)                             0.02       0.16 f
  I28/Y (INVX4)                             0.01       0.17 r
  I73/g_dash (prefix_block)                 0.00       0.17 r
  I73/I2/Y (NAND2X1)                        0.02       0.20 f
  I73/I3/Y (NAND2X1)                        0.02       0.22 r
  I73/I4/Y (INVX1)                          0.02       0.24 f
  I73/Gi_bar (prefix_block)                 0.00       0.24 f
  I139/Gi_bar (Cin)                         0.00       0.24 f
  I139/I1/Y (NAND2X1)                       0.02       0.26 r
  I139/Cout (Cin)                           0.00       0.26 r
  I185/ip1 (XOR_two_inputs)                 0.00       0.26 r
  I185/I0/Y (INVX1)                         0.02       0.29 f
  I185/I2/Y (NAND2X1)                       0.02       0.31 r
  I185/I4/Y (NAND2X1)                       0.03       0.33 f
  I185/op (XOR_two_inputs)                  0.00       0.33 f
C[6] (out)                                0.00       0.33 f
data arrival time                                    0.33
  ---------------------------------------------------------------
  (Path is unconstrained)
```

b) 16 bits:

```
****************************************
Report : timing
      -path_type full
      -delay_type max
      -max_paths 1
Design : Ladner_Fisher_16
Version: F-2011.06-SP1
Date   : Fri Dec  5 22:34:19 2015
****************************************


Startpoint: B[1] (input port)
  Endpoint: C[12] (output port)
  Path Group: (none)
  Path Type: max

  Point                                     Incr       Path
  ---------------------------------------------------------------
input external delay                      0.00       0.00 r
B[1] (in)                                 0.00       0.00 r
  I88/ip1 (gipi_cell)                       0.00       0.00 r
  I88/I6/Y (INVX1)                          0.01       0.01 f
  I88/I7/Y (NAND2X1)                        0.03       0.04 r
  I88/pi (gipi_cell)                        0.00       0.04 r
  I99/pi (prefix_block)                     0.00       0.04 r
  I99/I2/Y (NAND2X1)                        0.03       0.06 f
  I99/I3/Y (NAND2X1)                        0.02       0.09 r
```

```
  I99/Gi (prefix_block)                    0.00       0.09 r
  I102/g_dash (prefix_block)               0.00       0.09 r
  I102/I2/Y (NAND2X1)                      0.03       0.12 f
  I102/I3/Y (NAND2X1)                      0.02       0.14 r
  I102/Gi (prefix_block)                   0.00       0.14 r
  I112/Y (INVX1)                           0.02       0.16 f
  I110/Y (INVX4)                           0.01       0.17 r
  I49/g_dash (prefix_block)                0.00       0.17 r
  I49/I2/Y (NAND2X1)                       0.02       0.20 f
  I49/I3/Y (NAND2X1)                       0.02       0.22 r
  I49/Gi (prefix_block)                    0.00       0.22 r
  I292/Y (INVX4)                           0.02       0.24 f
  I294/Y (INVX4)                           0.01       0.25 r
  I269/g_dash (prefix_block)               0.00       0.25 r
  I269/I2/Y (NAND2X1)                      0.02       0.28 f
  I269/I3/Y (NAND2X1)                      0.02       0.30 r
  I269/I4/Y (INVX1)                        0.02       0.32 f
  I269/Gi_bar (prefix_block)               0.00       0.32 f
  I274/Gi_bar (Cin)                        0.00       0.32 f
  I274/I1/Y (NAND2X1)                      0.02       0.34 r
  I274/Cout (Cin)                          0.00       0.34 r
  I280/ip1 (XOR_two_inputs)                0.00       0.34 r
  I280/I0/Y (INVX1)                        0.02       0.37 f
  I280/I2/Y (NAND2X1)                      0.02       0.39 r
  I280/I4/Y (NAND2X1)                      0.03       0.41 f
  I280/op (XOR_two_inputs)                 0.00       0.41 f
C[12] (out)                              0.00       0.41 f
data arrival time                                   0.41
  ---------------------------------------------------------------
  (Path is unconstrained)
```

A.6. POWER ANALYSIS:

I. POWER REPORTS (only the sub-threshold reports are included)

Now, each net in the adder module has a static probability of either being in state 0 or state 1 and a toggle rate (high to low and low to high transitions) associated with it generated from .vcd file from VCS run that the Synopsys Primetime PX tool uses to generate the average power reports.

A.6.1 KOGGE-STONE:

<u>a) 8bit</u>

```
Information: Running time_based power analysis... (PWR-601)
Information: The waveform options are:
            File name:  primetime_px.fsdb
            File format:      fsdb
            Time interval:    0.01ns
            Hierarchical level:     all

Information: Power analysis is running, please wait ...

Information: analysis is done for time window (0ns - 6200ns)
```

```
****************************************
Report : Time Based Power
Design : Kogge_8
Version: F-2011.06-SP1
Date   : Fri Dec  5 22:27:10 2015
****************************************

  Attributes
  ----------
i  -  Including register clock pin internal power
u  -  User defined power group

Internal  Switching  Leakage    Total
Power Group             Power     PowerPowerPower   (     %)  Attrs
--------------------------------------------------------------------------------
-----
io_pad                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                  0.0000    0.0000    0.0000    0.0000 ( 0.00%)
clock_network              0.0000    0.0000    0.0000    0.0000 ( 0.00%)  i
register                   0.0000    0.0000    0.0000    0.0000 ( 0.00%)
combinational           4.422e-10 1.186e-09 1.267e-08 1.430e-08 (100.00%)
sequential                 0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 1.186e-09   ( 8.29%)
  Cell Internal Power  = 4.422e-10   ( 3.09%)
  Cell Leakage Power   = 1.267e-08   (88.61%)
                         ---------
Total Power            = 1.430e-08  (100.00%)

X Transition Power     =    0.0000
Glitching Power        =    0.0000

Peak Power             = 2.923e-06
Peak Time              =   4400.33
```

b) 16 bits:

```
Information: Running time_based power analysis... (PWR-601)
Information: The waveform options are:
            File name:  primetime_px.fsdb
            File format:      fsdb
            Time interval:    0.01ns
            Hierarchical level:     all

Information: Power analysis is running, please wait ...

Information: analysis is done for time window (0ns - 18500ns)

****************************************
Report : Time Based Power
Design : Kogge_16
Version: F-2011.06-SP1
Date   : Sat Dec  6 00:41:57 2015
****************************************
  Attributes
  ----------
i  -  Including register clock pin internal power
u  -  User defined power group
```

```
Internal  Switching  Leakage    Total
Power Group             Power     PowerPowerPower   (     %)  Attrs
--------------------------------------------------------------------------------
-----
io_pad                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                  0.0000    0.0000    0.0000    0.0000 ( 0.00%)
clock_network              0.0000    0.0000    0.0000    0.0000 ( 0.00%)  i
register                   0.0000    0.0000    0.0000    0.0000 ( 0.00%)
combinational           8.486e-10 2.406e-09 2.894e-08 3.219e-08 (100.00%)
sequential                 0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 2.406e-09   ( 7.47%)
  Cell Internal Power  = 8.486e-10   ( 2.64%)
  Cell Leakage Power   = 2.894e-08   (89.89%)
                         ---------
Total Power            = 3.219e-08  (100.00%)

X Transition Power     =    0.0000
Glitching Power        =    0.0000

Peak Power             = 5.803e-06
Peak Time              =   1400.33
```

A.6.2 LADNER-FISCHER

a) 8 bits:

```
Information: Running time_based power analysis... (PWR-601)
Information: The waveform options are:
            File name:  primetime_px.fsdb
            File format:      fsdb
            Time interval:    0.01ns
            Hierarchical level:     all

Information: Power analysis is running, please wait ...

Information: analysis is done for time window (0ns - 6200ns)

****************************************
Report : Time Based Power
Design : Ladner_Fisher_8
Version: F-2011.06-SP1
Date   : Fri Dec  5 22:32:03 2015
****************************************

  Attributes
  ----------
i  -  Including register clock pin internal power
u  -  User defined power group

Internal  Switching  Leakage    Total
Power Group             Power     PowerPowerPower   (     %)  Attrs
--------------------------------------------------------------------------------
-----
io_pad                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                  0.0000    0.0000    0.0000    0.0000 ( 0.00%)
```

```
clock_network              0.0000    0.0000    0.0000    0.0000 ( 0.00%)  i
register                   0.0000    0.0000    0.0000    0.0000 ( 0.00%)
combinational           4.180e-10 1.109e-09 1.182e-08 1.335e-08 (100.00%)
sequential                 0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 1.109e-09   ( 8.31%)
  Cell Internal Power  = 4.180e-10   ( 3.13%)
  Cell Leakage Power   = 1.182e-08   (88.56%)
                         ---------
Total Power            = 1.335e-08  (100.00%)

X Transition Power     =    0.0000
Glitching Power        =    0.0000

Peak Power             = 2.922e-06
Peak Time              =   4400.33
```

b) 16 bits:

```
Information: Running time_based power analysis... (PWR-601)
Information: The waveform options are:
            File name:  primetime_px.fsdb
            File format:      fsdb
            Time interval:    0.01ns
            Hierarchical level:     all

Information: Power analysis is running, please wait ...

Information: analysis is done for time window (0ns - 18500ns)

****************************************
Report : Time Based Power
Design : Ladner_Fisher_16
Version: F-2011.06-SP1
Date   : Sat Dec  6 00:43:08 2015
****************************************
  Attributes
  ----------
i  -  Including register clock pin internal power
u  -  User defined power group

Internal  Switching  Leakage    Total
Power Group             Power     PowerPowerPower   (     %)  Attrs
--------------------------------------------------------------------------------
-----
io_pad                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                  0.0000    0.0000    0.0000    0.0000 ( 0.00%)
clock_network              0.0000    0.0000    0.0000    0.0000 ( 0.00%)  i
register                   0.0000    0.0000    0.0000    0.0000 ( 0.00%)
combinational           7.950e-10 2.162e-09 2.636e-08 2.932e-08 (100.00%)
sequential                 0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 2.162e-09   ( 7.37%)
  Cell Internal Power  = 7.950e-10   ( 2.71%)
  Cell Leakage Power   = 2.636e-08   (89.91%)
                         ---------
Total Power            = 2.932e-08 (100.00%)
```

```
X Transition Power      =    0.0000
Glitching Power         =    0.0000

Peak Power              = 5.801e-06
Peak Time               =   1400.33
```

A.6.3 PEAK POWER WAVEFORM COMPARISON:

A pseudo-random set of input test vectors were provided and the power dissipated within the adder at each timestamp is noted as a discrete value in the waveform to give the peak power analysis.

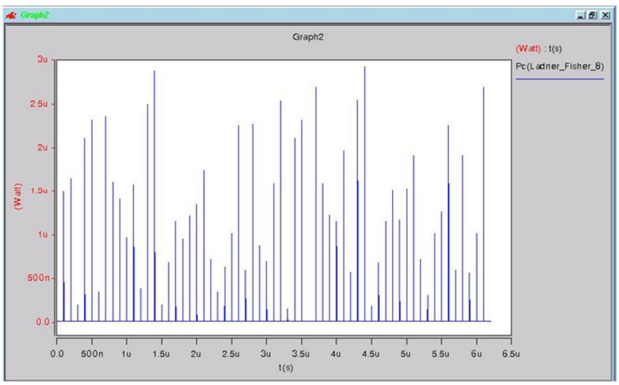


Fig 36a. Ladner-Fisher(8 bits 0.2V)

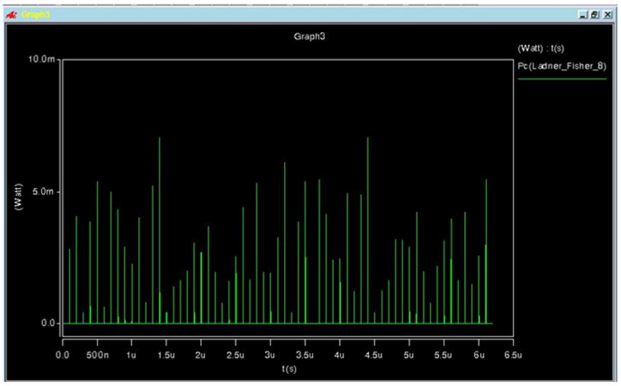


Fig 36b.Ladner-Fisher(8 bits 1V)

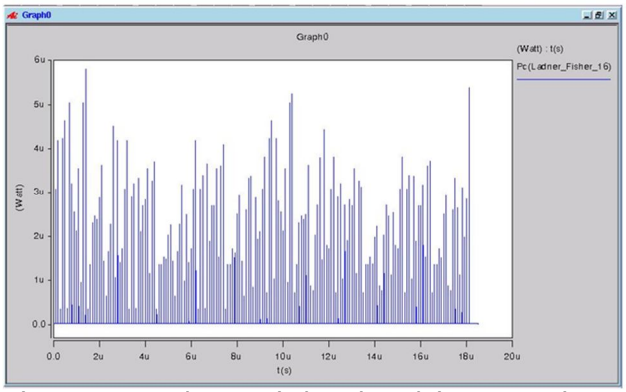


Fig 37a. Ladner-Fisher(16 bits 0.2V)

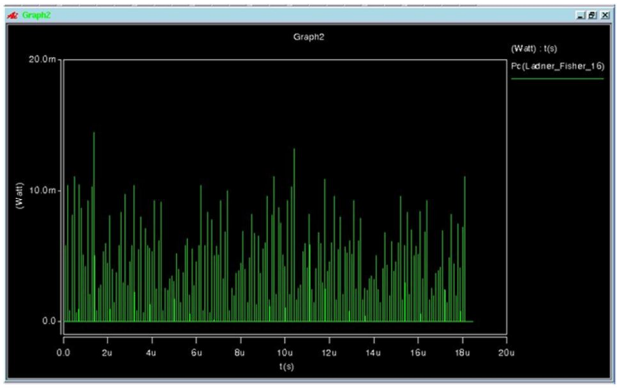


Fig 37b.Ladner-Fisher(16 bits 1V)

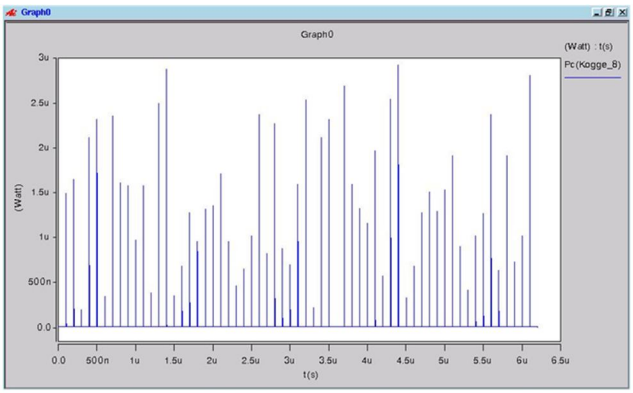


Fig 38a. Kogge-Stone(8 bits 0.2V)

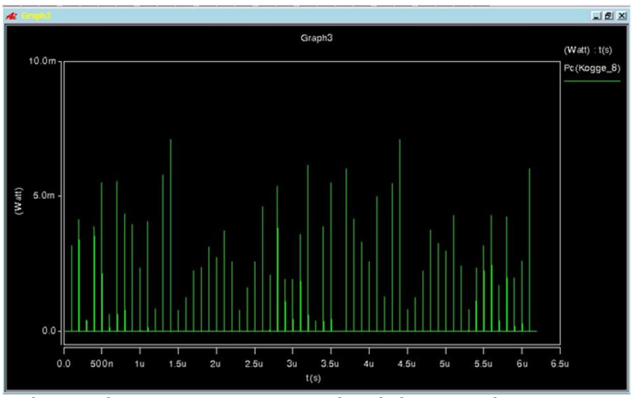


Fig 38b. Kogge-Stone(8 bits 1V)

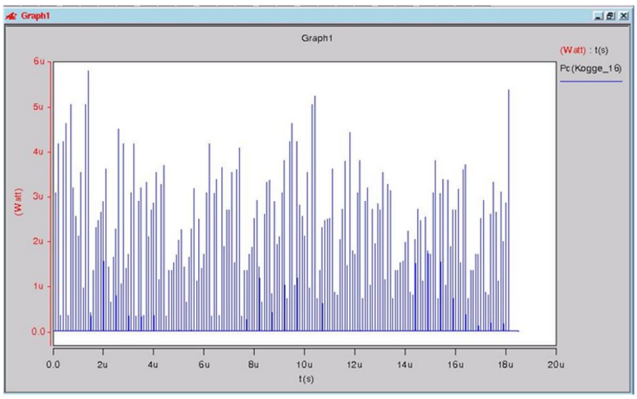


Fig 39a. Kogge-Stone(16 bits 0.2V)

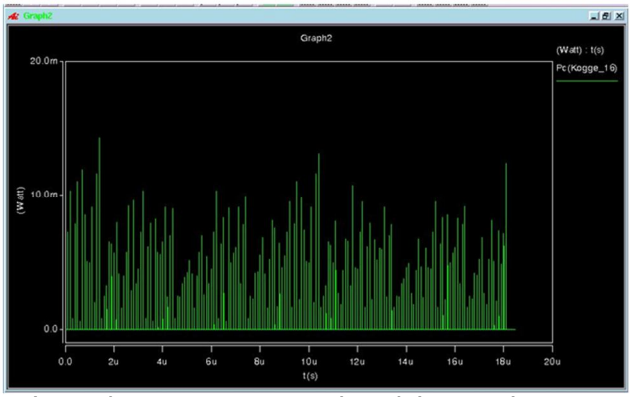


Fig 39b. Kogge-Stone(16 bits 1V)

Bibliography

[1] Gilchrist, B., Pomerene, J. H., and Wong, S. Y., “Fast carry logic for digital computers,” *IRE Transactions on Electronic Computers,* Vol. 4, pp. 133-136, 1955.

[2] MacSorley, O. L., “High-speed arithmetic in binary computers,” *Proceedings of the IRE,* vol. 49, pp. 67-91, 1961.

[3] Bedrij, O. J., “Carry-select adder,” *IRE Transactions on Electronic Computers,* vol. 3, pp. 340-346, 1962.

[4] Ladner, R. E., and Fischer, M. J., “Parallel prefix computation,” *Journal of the ACM (JACM),* vol. 27, pp. 831-838, 1980

[5] Soeleman, H., and Roy, K., “Ultra-low power digital subthreshold logic circuits,” *Proceedings of the 1999 International Symposium on Low Power Electronics and Design* pp. 94-96, ACM, 1999.

[6] Soeleman, H., Roy, K., and Paul, B. C., “Robust subthreshold logic for ultra-low power operation,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol 9, pp. 90-99, 2000

[7] Paul, B. C., Raychowdhury, A., and Roy, K., “Device optimization for digital subthreshold logic operation,” *IEEE Transactions on Electron Devices,* vol *52*(2), pp. 237-247, 2005.

[8] Calhoun, B. H., Wang, A., and Chandrakasan, A, “Modeling and sizing for minimum energy operation in subthreshold circuits,” *IEEE Journal of, Solid-State Circuits* vol *40*(9), pp. 1778-1786, 2005

[9] H. Soeleman, K. Roy, and B. Paul, "Robust Sub-Threshold Logic for Ultra Low Power Operation," *IEEE Transactions on VLSI Systems,* Special issue on low-power design, pp.90-99, February 2001.

[10] B. Paul, H. Soeleman, and K. Roy, "An 8X8 Sub-Threshold Digital CMOS Carry Save Array Multiplier," *Proceedings of the 27th European Solid State Circuits Conference, ESSCIRC, IEEE*, pp. 377-380, September 2001.

[11] Tran, A. T., and Baas, B. M., "Design of an energy-efficient 32-bit adder operating at subthreshold voltages in 45-nm CMOS," *Third International Conference on Communications and Electronics (ICCE),* pp. 87-91, August 2010.

[12] Nyathi, Jabulani, and Brent Bero, "Logic circuits operating in subthreshold voltages," *Proceedings of the 2006 International Symposium on Low Power Electronics and Design, 2006. (ISLPED)* IEEE, pp. 131-134, October 2006.

[13] Calhoun, B. H., Khanna, S., Mann, R. W., and Wang, J., *"Sub-threshold Circuit Design with Shrinking CMOS Devices," ISCAS,* pp. 2541-2544, May 2009.

[14] Jos Budi Sulistyo, *On the Characterization of Library Cells,* Thesis (Master of Science), Virginia Polytechnic Institute and State University, 2000